

UNITED STATES DISTRICT COURT  
WESTERN DISTRICT OF TEXAS  
WACO DIVISION

PARKERVISION, INC.,

Plaintiff,

v.

INTEL CORPORATION,

Defendant.

Case No. 6:20-cv-00108-ADA

JURY TRIAL DEMANDED

**PLAINTIFF PARKERVISION'S  
REPLY CLAIM CONSTRUCTION BRIEF**

## TABLE OF CONTENTS

|      |                                                                                                                                                                                                                                                                                                          |    |
|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|
| I.   | Introduction. ....                                                                                                                                                                                                                                                                                       | 1  |
| II.  | ParkerVision’s description of the patented technology is accurate. ....                                                                                                                                                                                                                                  | 1  |
| III. | Intel avoids providing this Court with a complete picture of the patented technology. ....                                                                                                                                                                                                               | 2  |
| IV.  | Intel seeks to improperly dismiss previous claim construction rulings. ....                                                                                                                                                                                                                              | 4  |
| V.   | Disputed terms for construction. ....                                                                                                                                                                                                                                                                    | 5  |
| A.   | Energy “storage” module/element/device terms. ....                                                                                                                                                                                                                                                       | 5  |
| B.   | “modulated carrier signal” (’528 patent, claims 1, 5, 14) ....                                                                                                                                                                                                                                           | 7  |
| C.   | “switch” (’528 patent, claims 1, 5, 17; ’444 patent, claim 3; ’474 patent, claim 1; ’513 patent, claim 19; ’518 patent, claim 50; ’736 patent, claims 1, 11; ’673 patent, claims 1, 13); “switching device” (’725 patent, claim 1; ’528 patent, claim 8); “switching module” (’902 patent, claim 1)..... | 8  |
| D.   | “sampling aperture” (’528 patent, claim 1) ....                                                                                                                                                                                                                                                          | 9  |
| E.   | “a down-converted signal being generated from said sampled energy” (’902 patent, claim 1) ....                                                                                                                                                                                                           | 10 |
| F.   | “the [] switch is coupled to the [] storage element at a [] node and coupled to a [] reference potential” (’474 patent, claim 1) ....                                                                                                                                                                    | 14 |
| G.   | “under-samples” (’444 patent, claim 2; ’474 patent, claim 6) ....                                                                                                                                                                                                                                        | 16 |
| H.   | The <i>six</i> terms (11 claims) into which Intel seeks to inject “aliasing rate” ....                                                                                                                                                                                                                   | 17 |
| I.   | “a capacitor that reduces a DC offset voltage in said first down-converted signal and said second down-converted signal” (’444 patent, claim 4).....                                                                                                                                                     | 20 |
| J.   | “DC offset voltage” (’444 patent, claim 4) ....                                                                                                                                                                                                                                                          | 21 |
| K.   | Terms alleged to be indefinite. ....                                                                                                                                                                                                                                                                     | 21 |

## I. Introduction.

Intel continues to push its false narrative regarding the patented technology and fails to provide any basis as to why well-reasoned, prior court constructions of disputed terms are wrong. Tellingly, Intel purposefully avoids providing details as to how the patented technology actually works because this would expose the flaws in Intel’s constructions.

## II. ParkerVision’s description of the patented technology is accurate.

Intel attempts to create the false narrative, arguing that ParkerVision is trying to change what the patents-in-suit say about the patented technology. See D.I. 58 (“Intel. Resp. Br.”) at 2-5. With this narrative, Intel implies that ParkerVision’s description of the technology strays from the intrinsic evidence.<sup>1</sup> *Id.* Intel is wrong.

In particular, Intel points out that the patents-in-suit refer to “under-sampling systems” and “energy transfer systems.” Intel then complains that ParkerVision describes “under-sampling systems” as “voltage” sampling systems, and “energy transfer systems” as “energy” sampling systems. But that’s what they are.<sup>2</sup>

In particular, the patents-in-suit pertain to the use of *sampling* to *down-convert* a signal. Context is key here. Specifically, there are only two things that can be *sampled* to *down-convert* a signal: (1) voltage and (2) flow of energy over time (current). Ex. 1 ¶15 (“Steer Decl.”). Voltage is sampled by taking and holding input voltage values (using a “holding” module)<sup>3</sup>.

---

<sup>1</sup> Intel asserts that it does not agree with other yet-to-be identified portions of ParkerVision’s technology description. Intel Resp. Br. at 5 n. 5. Yet, after two briefs and two expert declarations, Intel has still not fully explained the technology or how ParkerVision got it wrong.

<sup>2</sup> Intel’s assertion that the patents do not use the term “voltage” sampling or “energy” sampling is beside the point. See Intel Resp. Br. at 2.

<sup>3</sup> Contrary to Intel’s position, so-called “under-sampling systems” are “voltage” sampling systems. Indeed, when discussing “under-sampling systems,” the patents refer to a sample and hold system. A sample and hold system is a “voltage” sampling system because sample and hold systems use the change in discrete measurements in voltage to create a down-converted signal. ’518 patent, 31:44-48 (“[T]he under-sample points 1905 correlate to voltage points 1908.

Current, which is the flow of electrons, is sampled by transferring and capturing energy over time (using a “storage” module). *Id.* As such, there are *only two* systems that can *sample* to *down-convert* a signal – the same two systems discussed in the patents-in-suit: (1) “voltage” sampling system (referred to in the patents as “under-sampling systems”) and (2) “energy” sampling system (referred to in the patents as “energy transfer” systems). *Id.* The patents-in-suit merely use “under-sampling systems” as a *naming convention* to connote “voltage” sampling systems and distinguish “voltage” sampling systems from “energy” sampling (energy transfer) systems. *Id.* at ¶16. This is the reason why ParkerVision’s description of the technology in its opening brief refers to “voltage” sampling systems and “energy” sampling systems. ParkerVision is not trying to change what the invention is; it is simply describing the technology.

### **III. Intel avoids providing this Court with a complete picture of the patented technology.**

There are complexities to the technology in this case. Unlike ParkerVision who explains specifically how the patented technology down-converts a radio frequency signal, Intel focuses on naming conventions and tries to avoid providing the Court with a complete picture of the technology. Notably, Intel presents the technology in drips and drabs – only so much as it believes necessary to push its narrative. This is no accident. With a proper understanding of the technology, Intel’s constructions do not withstand scrutiny.

Instead of focusing on important details, Intel makes broad pronouncements regarding the technology. *First*, Intel devotes significant pages in its briefs arguing that down-converting at an aliasing rate is “the” invention and, therefore, all claims in all of the patents must include the

---

... [E]ach voltage point 1908 can be held at a relatively constant level until the next voltage point is received. This results in a stair-step output which can be smoothed or filtered if desired...”); *see also id.* at 32:41-48, 34:1-8; 34:66-35:6; 36:24-31; 37:19-26; 41:34-41; 42:38-45; 44:10-17; 45:13-20; 50:22-28; 51:61-67.

concept of an aliasing rate. The implication is that the claims are missing this concept. But as discussed in Section IV.H below, the claims *already* include the concept of an aliasing rate. *See also* D.I. 51 (“ParkerVision Op. Br.”) at 28-34; D.I. 57 (“ParkerVision Resp. Br.”) at 4-5, 23-30. Intel simply does not like *where* the aliasing rate language is found in the claims. So, under the guise of construction, Intel seeks to inject *additional* instances of aliasing rate into the claims to support its non-infringement case.

*Second*, Intel devotes significant pages attempting to convince the Court that “under-sampling” is synonymous with the use of negligible apertures. Not only has another district court already rejected this same argument, but the patent specification directly contradicts that argument. The specification explains that under-sampling is performed by an energy transfer system using non-negligible apertures. *See e.g.*, ’518 patent, 67:5-10 (“FIGS. 83A-F illustrate example timing diagrams for the energy transfer system 8202 in FIG. 82. . . . FIG. 83C illustrates an example under-sampling signal 8304, including *energy transfer* pulses 8306 having non-negligible apertures . . .”),<sup>4</sup> 92:25-27, 63-65; 120:54-58 (claim 97); *see also* ParkerVision Resp. Br. at 2-3, 20-22. The claims of the patents-in-suit also demonstrate that energy transfer systems, which use non-negligible apertures as the specification explains, perform under-sampling. For example, claim 97 of the ’518 patent recites “under-sampling . . . to transfer energy.” Transfer of energy is performed by an “*energy transfer system*.” Independent claim 1 of the ’474 patent recites a “*storage element(s)*,” which Intel admits connotes an *energy transfer system*. D.I. 53 (“Intel Op. Br.”) at 36. Claim 6, which depends from claim 1, then recites “under-sampl[ing] an input signal.” *see also* ParkerVision Resp. Br. at 2-3, 20-22.<sup>5</sup>

---

<sup>4</sup> Unless otherwise indicated, all emphasis has been added.

<sup>5</sup> Figures 84A-D also disclose an energy transfer system. “The operation of the energy transfer system 6302 shall now be described with reference to the flowchart 4619 and the timing

#### IV. Intel seeks to improperly dismiss previous claim construction rulings.

As set forth in the chart below, *three* federal Judges construed terms related to the same ParkerVision technology/patent specification that is in dispute here. Each Judge provided a well-reasoned opinion for his construction. Indeed, Intel has not identified any errors in the Judges' reasoning. There simply are none. Instead, unhappy with these constructions, Intel baselessly asserts that the Court should not adopt *any* of these constructions. And Intel goes as far as *falsely* asserting that when construing the term "universal frequency down-converter," the Jacksonville court was unaware of the language in a patent specification. But Intel is just flat wrong.<sup>6</sup>

Though not binding on this Court, these constructions should not be rejected out of hand as Intel suggests. ParkerVision's arguments, which are consistent with the reasoning of the three Judges and the intrinsic record, demonstrate that these prior constructions are correct.

| Terms           | Prior Court Constructions                                                                                    |
|-----------------|--------------------------------------------------------------------------------------------------------------|
| "under-samples" | "sampling at an aliasing rate" / "sampling at less than or equal to twice the frequency of the input signal" |

*diagrams of FIGS. 84A-84D.*" '518 patent; 92:63-65. And the specification states that the FSK signal 816 having frequency 8412 in Figure 84B is "under-sampled." *Id.* at 92:25-26 ("When the second frequency 8412 is under-sampled, the PSK signal 8404 has a frequency of approximately 1 MHZ . . .").

<sup>6</sup> With regard to "universal frequency down-converter," Intel falsely asserts that the Jacksonville court was oblivious to certain facts.

But in that case, *it does not appear that either party brought to the court's attention (or that the court recognized) that the '371 patent, like the Asserted Patents in this case, incorporates the '551 patent by reference into its specification. . . . It appears, therefore, that the court was not made aware of ParkerVision's description of its "present invention" as a structure that down-converts by aliasing.*

Intel Resp. Br. at 17. The court order, however, makes it clear that the court was well aware of these facts. D.I. 51-2 at 6 (noting that "[t]he '371 patent . . . 'incorporate[s] by reference,' among other things, the teachings of the '551 Patent. See, e.g., '371 Patent col. 1 ll. 10-27.")

|                                      |                                                                                                                                    |
|--------------------------------------|------------------------------------------------------------------------------------------------------------------------------------|
|                                      | D.I. 51-2 at 10 (Judge Dalton)                                                                                                     |
| “switch” / “switch module”           | “device with an input and output that can take two states, open and closed, as dictated by an independent control input”           |
|                                      | D.I. 51-3 at 32. (Judge Byron)                                                                                                     |
| “universal frequency down-converter” | “circuitry that generates a down-converted output signal from an input signal”                                                     |
|                                      | D.I. 51-2 at 38 (Judge Dalton)                                                                                                     |
| “modulated carrier signal”           | “electromagnetic signal at transmission frequency having at least one characteristic that has been modulated by a baseband signal” |
|                                      | D.I. 51-1 at 28-29 (Judge Davis)                                                                                                   |

**V. Disputed terms for construction.**

**A. Energy “storage” module/element/device terms.**

| <b>Claim Terms</b>                                                             | <b>ParkerVision’s Construction</b>                                                                                                                           | <b>Intel’s Construction</b>                                                                          |
|--------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------|
| “energy storage element”<br>’528 patent, claim 1                               | “an element of an energy transfer system that stores non-negligible amounts of energy from an input electromagnetic signal for driving a low impedance load” | “an element that stores a non-negligible amount of energy from an input electromagnetic (EM) signal” |
| “energy storage module”<br>’902 patent, claim 1                                | “a module of an energy transfer system that stores non-negligible amounts of energy from an input electromagnetic signal for driving a low impedance load”   | “a module that stores a non-negligible amount of energy from an input electromagnetic (EM) signal”   |
| “energy storage element”<br>’513 patent, claim 19<br>’736 patent, claims 1, 11 | “an element of an energy transfer system that stores non-negligible amounts of energy from an input electromagnetic signal for driving a low impedance load” | “an element that stores a non-negligible amount of energy from an input electromagnetic (EM) signal” |
| “energy storage device”<br>’673 patent, claim 13                               | “a device of an energy transfer system that stores non-negligible amounts of energy from an input electromagnetic signal for driving a low impedance load”   | “a device that stores a non-negligible amount of energy from an input electromagnetic (EM) signal”   |
| “storage element”<br>’444 patent, claim 3                                      | “an element of an energy transfer system that stores non-negligible amounts of energy                                                                        | “an element that stores a non-negligible amount of energy from an input electromagnetic (EM)         |

|                                          |                                                                                                                                                            |                                                                                                    |
|------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------|
| '474 patent, claim 1                     | from an input electromagnetic signal for driving a low impedance load”                                                                                     | signal”                                                                                            |
| “storage module”<br>'725 patent, claim 1 | “a module of an energy transfer system that stores non-negligible amounts of energy from an input electromagnetic signal for driving a low impedance load” | “a module that stores a non-negligible amount of energy from an input electromagnetic (EM) signal” |

The specification specifically distinguishes “storage” modules from “holding” modules.

FIG. 82A illustrates an exemplary energy transfer system 8202 for down-converting an input EM signal 8204. The energy transfer system 8202 includes a switching module 8206 and a storage module illustrated as a storage capacitance 8208. The terms storage module and storage capacitance, as used herein, are distinguishable from the terms holding module and holding capacitance, respectively. Holding modules and holding capacitances, as used above, identify systems that store negligible amounts of energy from an under-sampled input EM signal with the intent of ‘holding’ a voltage value. **Storage modules and storage capacitances, on the other hand, refer to systems that store non-negligible amounts of energy from an input EM signal.**

'518 patent, 66:11-23.

Intel continues to focus improperly on a *single* sentence (red above) while ignoring the other relevant language in that same paragraph. By doing so, Intel is trying to omit key distinguishing features. See ParkerVision Op. Br. at 14-17; ParkerVision Resp. Br. at 6-10.

Tellingly, Intel’s opening brief provides no substantive reason based on the intrinsic evidence as to why “energy transfer system” should not be included in the construction of “storage” terms. Yet now in its responsive brief, Intel asserts that “insert[ing] the requirement that the storage terms be part of an ‘energy transfer system’ is not supported by the intrinsic evidence.” Intel Resp. Br. at 36. Not only has Intel now *changed* its position, but that assertion is a gross misrepresentation of the specification’s disclosures.

In fact, Intel’s own statements in its opening brief demonstrate why the inclusion of “energy transfer system” in the “storage” terms is appropriate. *First*, Intel admitted there are only

two systems disclosed in the patent (1) energy transfer and (2) under-sampling. Intel Op. Br. at 8-9. *Second*, Intel acknowledged that “the specifications state that the ‘energy transfer’ mode uses ‘a storage module’ . . . whereas the ‘under-sampling’ [sample and hold] mode utilizes a ‘holding module’ . . . .” *Id.* at 35-36. Logically, if there are only two systems and a “storage” module is only used in an energy transfer system, then, consistent with ParkerVision’s construction, a “storage” module must necessarily be a module of an energy transfer system.

Indeed, the specification, as ParkerVision previously discussed, makes it clear that “storage” modules/elements/devices are inseparably intertwined with energy transfer systems. *See ParkerVision Op. Br.* at 5-15.

With regard to ParkerVision’s language “for driving a low impedance load,” Intel has not raised any new issues that ParkerVision’s briefs have not already addressed. For the foregoing reasons, ParkerVision’s construction should be adopted.

**B. “modulated carrier signal” (’528 patent, claims 1, 5, 14)**

| <b>ParkerVision’s Construction</b>                                                                                                 | <b>Intel’s Construction</b>                               |
|------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------|
| “electromagnetic signal at transmission frequency having at least one characteristic that has been modulated by a baseband signal” | “a carrier signal that is modulated by a baseband signal” |

Intel does not (and cannot) dispute that ParkerVision’s construction is technically accurate. Indeed, in July 2019, the Jacksonville court expressly adopted this construction, which both Qualcomm and ParkerVision had agreed to. D.I. 51-1 at 28-29. As such, the construction became the Jacksonville court’s construction – a fact that Intel ignores in its brief. Though not binding on this Court, the Jacksonville court’s construction demonstrates another court’s thinking on this term and provides yet another data point for this Court to consider.

Tellingly, Intel avoids any technical discussion to assist the Court’s understanding of this term. Instead, Intel paints broad brush strokes. In particular, Intel asserts that its construction is correct because it “tracks the patents’ express definition of the term.” Intel Resp. Br. at 37. But this is incorrect. Intel’s construction is incomplete because it ignores the fact that “carrier signal” is nested within the definition of “modulated carrier signal” and expressly defined in the patent: “The term carrier signal, when used herein, refers to an EM wave having at least one characteristic that may be varied by modulation, that is capable of carrying information via modulation.” ’528 patent, 21:36-39. ParkerVision’s construction simply marries the definition of these two terms. And, given that there are a number of signals involved in the process of down-converting, ParkerVision also includes “at a transmission frequency” to clarify for a jury that a carrier signal is the electromagnetic signal that is transmitted over the air. *See* ParkerVision Op. Br. at 17-19; ParkerVision Resp. Br. at 10-11. For the foregoing reasons, ParkerVision’s construction should be adopted.

- C. **“switch” (’528 patent, claims 1, 5, 17; ’444 patent, claim 3; ’474 patent, claim 1; ’513 patent, claim 19; ’518 patent, claim 50; ’736 patent, claims 1, 11; ’673 patent, claims 1, 13); “switching device” (’725 patent, claim 1; ’528 patent, claim 8); “switching module” (’902 patent, claim 1)**

| <b>ParkerVision’s Construction</b>                                                                   | <b>Intel’s Construction</b>                              |
|------------------------------------------------------------------------------------------------------|----------------------------------------------------------|
| “an electronic device for opening and closing a circuit as dictated by an independent control input” | “an electronic device for opening and closing a circuit” |

Not only has ParkerVision explained why the intrinsic evidence supports its language “as dictated by an independent control input,” but the Orlando court considered and rejected the same types of arguments that Intel raises here for omitting this language. *See* D.I. 51-3 at 24-32. And, in April 2019, the Orlando court construed “switch” and “switching module” as a “device with an input and output that can take two states, open and closed, *as dictated by an independent*

*control input.*”<sup>7</sup> D.I. 51-3 at 32. Though Intel attempts to dismiss the Orlando court’s construction, Intel provides no reasons demonstrating that the Orlando court got it wrong. Indeed, Intel has not raised any new arguments regarding these terms. For the foregoing reasons, ParkerVision’s construction or the Orlando court’s construction which include “as dictated by an independent control input” should be adopted.

**D. “sampling aperture” (’528 patent, claim 1)**

| <b>ParkerVision’s Construction</b>                                                                                                                  | <b>Intel’s Construction</b>                                                                                                                                        |
|-----------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| “a period of time during which the claimed switch is in its closed (on) state, thereby reducing a continuous-time signal to a discrete-time signal” | “a period of time during which the switch is in its closed (i.e., on) state as part of the process of reducing a continuous-time signal to a discrete-time signal” |

At bottom, Intel’s only argument is that its construction is more technically accurate than ParkerVision’s construction. Intel Resp. Br. at 39. ParkerVision disagrees. Intel’s language injects substantial ambiguity into the term as to what steps constitute “part” of the process. ParkerVision Op. Br. at 23; ParkerVision Resp. Br. at 15. Notably, the Jacksonville court *expressly adopted* ParkerVision’s construction.<sup>8</sup> See D.I. 51-1 at 28-29. ParkerVision’s construction here merely adopts the Jacksonville court’s construction. Though not binding on this Court, the Jacksonville court’s construction demonstrates another court’s thinking on this term and provides yet another data point for this Court to consider. Moreover, as ParkerVision previously stated, “it is the occurrence of an aperture that causes the switch to reduce a continuous-time signal to a discrete-time signal.” ParkerVision Op. Br. at 22. For the foregoing reasons, ParkerVision’s construction should be adopted.

---

<sup>7</sup> ParkerVision’s construction is consistent with the Orlando court’s construction. As such, either of these constructions are proper constructions.

<sup>8</sup> Intel misleadingly asserts that no court ever ruled on the construction of “sampling aperture.” Intel Resp. Br. at 40 n. 15. By expressly *adopting* the parties’ construction of “sampling aperture,” the Jacksonville court ruled on this construction.

**E. “a down-converted signal being generated from said sampled energy” (’902 patent, claim 1)**

| <b>ParkerVision’s Construction</b>                                                                                                                                                                                           | <b>Intel’s Construction</b>                                                                                                                      |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| “a lower frequency signal formed from sampled energy transferred from the electromagnetic signal when the switch module is closed and from sampled energy discharged from the storage module when the switch module is open” | Plain and ordinary meaning<br><br>Alternatively, “a down-converted signal being created from sampled energy stored in the energy storage module” |

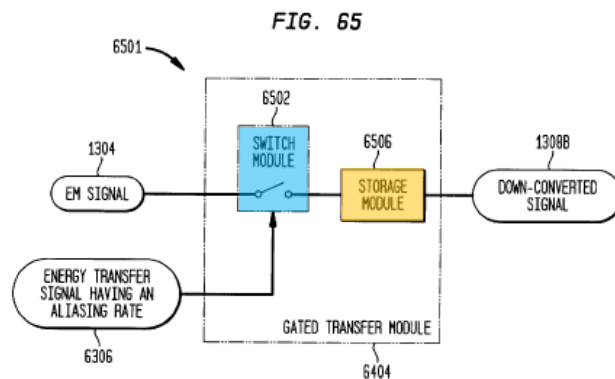
Intel continues to twist the language of the claim and again avoids any discussion of how the technology actually works. The claim language, however, makes it clear that a down-converted signal is generated from the sampled energy from the energy transfer module *as a whole*, not just its storage module component as Intel’s construction suggests.

In particular, claim 1 recites “an energy transfer module having a *switch module* and an *energy storage module*.” Claim 1 then recites “said *energy transfer module sampling the electromagnetic signal* at an energy transfer rate... to obtain sampled energy” and “a down-converted signal being generated from said sampled energy.” As such, consistent with how the technology is described in the specification, the down-converted signal is generated with energy from *both* the switch and the storage module. See ParkerVision Op. Br. at 23-26; ParkerVision Resp. Br. at 16-17. That the claim language *also* recites that “said sampled energy” is stored in a storage module does not change this fact. Indeed, that language is entirely consistent with how the technology works. Energy stored in a storage module is discharged when the switch is OFF (open) and forms *part of* a down-converted signal. See ParkerVision Op. Br. at 7-9.

Indeed, the use of “said” in “said sampled energy” with reference to the storage module demonstrates that the sampled energy had already been recited in the claims i.e., it is the *second* instance of the use of “sampled energy.” As such, the claim’s reference of the down-converted

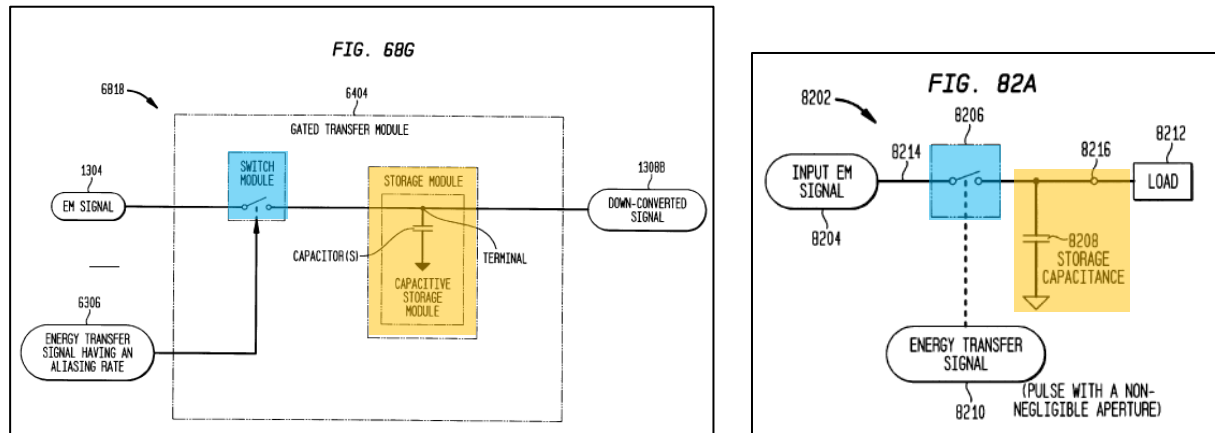
signal being generated from “said sampled energy” is referring back to the sampled energy from the energy transfer module, not the storage module contained therein.<sup>9</sup>

Recognizing the weakness of its position and hoping to sway the Court, Intel asserts that ParkerVision’s construction excludes the embodiment of Figure 65. Intel Resp. Br. at 43-44. This is *false*. Intel’s analysis of Figure 65 is purposefully devoid of any details because even the most cursory analysis of the specification’s disclosure regarding Figure 65 would reveal how Intel is misleading the Court.



As shown above, the system of Figure 65 includes a switch module 6502 (blue) and a storage module 6506 (orange). The storage module is simply represented by a box. In making its argument, Intel glosses over the fact that there is a circuit configuration inside the box and ignores the specification’s discussion of Figure 65.

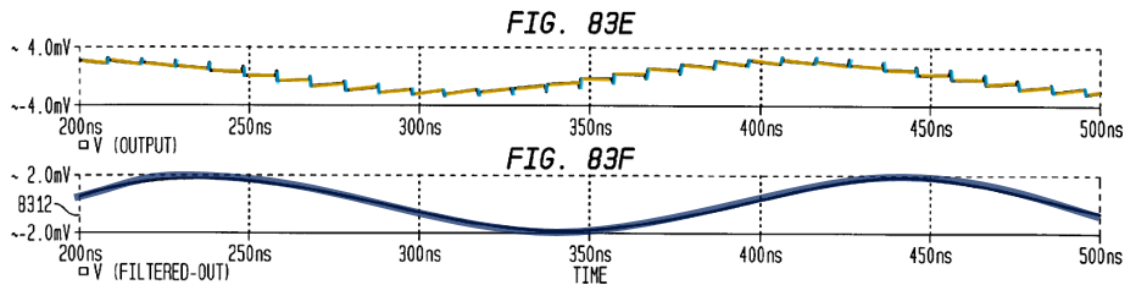
<sup>9</sup> Intel reads the claim as if “sampled energy” was first discussed with regard to the energy storage module. In particular, Intel reads the claim as if it read: “the energy storage module storing sampled energy” and “a down-converted signal being generated from said sampled energy.” That is not how the claim is written.



In particular, Figures 68G and 82A illustrate the circuit configuration inside of the storage module (orange). Indeed, the specification states that Figure 65 is using the timing diagram of Figures 83A-F: “For example, operation of the switch module 6502 and the storage module 6506 is now described for down-converting the EM signal 1304 to an intermediate signal, with reference to the flowchart 4607 and the example *timing diagrams in FIGS. 83A–F.*” ’902 patent, 102:40-44. By no coincidence, Figures 83A-F is the same timing diagram that is used for the storage module (orange) in Figure 82A (above right). *Id.* at 70:55-56. This is because the system of Figures 65 works similarly to Figure 82A, which generates a down-converted signal from energy from the switch *and* the capacitor. *See ParkerVision Op. Br.* at 6-9.

Indeed, the specification states that the switch module and storage module cooperate to transfer energy from the EM signal and down-convert the energy: “*the switch module 6502 and the storage module 6506 cooperate to transfer energy from the EM signal 1304 and down-convert it to an intermediate signal.*” *Id.* at 102:47-50. Similar to Figure 82A, “the switch module 6502 closes during each energy transfer pulse to couple the EM signal 1304 to the storage module 6506. . . . While the EM signal 1304 is coupled to the storage module 6506, non-negligible amounts of energy are transferred from the EM signal 1304 to the storage module 6506.” *Id.* at 102:51-59. And, similar to Figure 82A, “[t]he storage module 6506 outputs the

*transferred* energy as the down-converted signal 1308B.” *Id.* at 102:62-64. Notably, the specification does not say that the down-converted signal is just from the *stored* energy in the storage module (i.e., in the capacitor). Instead, the specification states that the down-converted signal is generated from the *transferred* energy from the storage module. Such *transferred* energy includes (1) energy that passes through the storage module from the switch when the switch is ON (closed) *and* (2) energy stored in the storage module (in the capacitor) and discharged when the switch is OFF (open). The specification further states that “[t]he storage module 6506 can output the down-converted signal 1308B as an unfiltered signal such as signal shown in FIG. 83E, or as a filtered down-converted signal (FIG. 83F).” *Id.* at 102:64-67.



As shown above, Figure 83E illustrates that the down-converted signal is made up of (1) energy (blue) from the switch module that passes through the storage module when the switch module is ON (closed) *and* (2) energy (orange) stored in and subsequently discharged from the storage module when the switch module is OFF (open). See ParkerVision Resp. Br. at 16-17. Indeed, if the down-converted signal did not include energy that passes through the storage module when the switch is ON (closed), the down-converted signal would not be continuous, as shown in FIG. 83E-F. If, as Intel asserts, the down-converted signal only contains energy (orange) from the storage module (i.e., discharged when the switch is OFF (open)) and no energy (blue) from the input when the switch is ON (closed), the down-converted signal would be filled with gaps or *incomplete*.

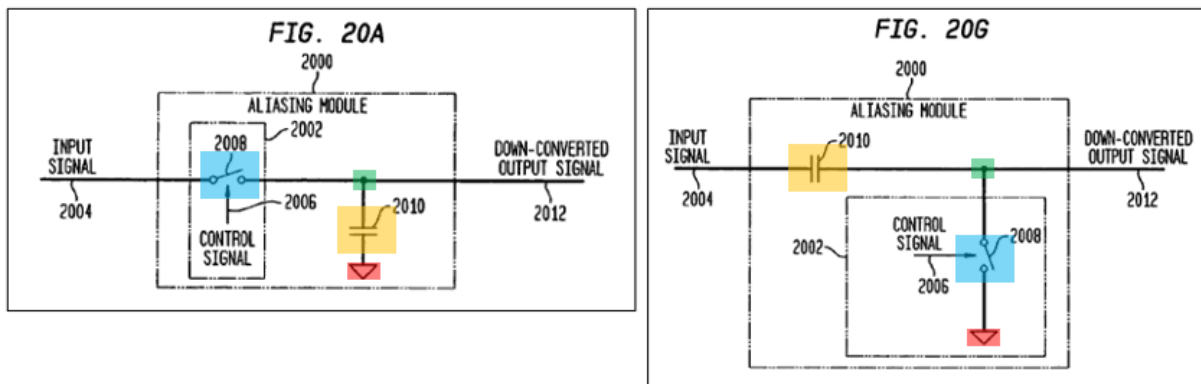
For the foregoing reasons, ParkerVision’s construction should be adopted.

**F. “the [] switch is coupled to the [] storage element at a [] node and coupled to a [] reference potential” (’474 patent, claim 1)**

| ParkerVision’s Construction | Intel’s Construction                                                                        |
|-----------------------------|---------------------------------------------------------------------------------------------|
| Plain and ordinary meaning  | “the switch shunts (i.e., diverts) current to a point held at a constant reference voltage” |

Intel seeks to change the meaning of the term, which simply requires that a switch is coupled to (1) a storage element and (2) a reference potential.

In particular, Intel’s construction seeks to limit claim 1 to the embodiment of Figure 20G and *exclude* the embodiments of Figures 20A, 90, 91, 92B, 93, 94A, 97, 99, 100, 105, 107. For simplicity, ParkerVision’s argument will focus on Figure 20A.



As shown above, Figures 20A and 20B illustrate an aliasing module (frequency down-conversion module) having different configurations of a switch 2008 (blue), a capacitor 2010 (orange), a reference potential (e.g., ground) (red). A node (green) connects the switch and capacitor.

According to Intel, the language of claim 1 as written could cover any configuration of a switch, storage element and reference potential. Intel Resp. Br. at 22. So Intel tries to limit the claims to the embodiment of Figure 20G. To do so, Intel incorrectly asserts that the language “the [] switch is . . . coupled to a reference potential” means that the switch must be *directly*

coupled to a reference potential (as shown in Figure 20G), not *indirectly* coupled to a reference potential (as shown in Figure 20A). Intel then crafted its construction to only encompass the configuration of Figure 20G.

Intel's position is flawed. *First*, with regard to Figures 20A and 20G, the specification makes it clear that the term "coupled" can refer to an *indirect* connection/coupling. Tellingly, Intel ignores this relevant portion of the specification. In particular, with regard to Figures 20A and 20G, the specification states that the input signal is "coupled" to the capacitor through another component – the switch: "When the switch 2008 is closed, the input signal 2004 is coupled to the capacitor 2010." '474 patent, 12:10-11, 43-44. This is an *indirect* connection/coupling. Tellingly, to support its position, Intel does not cite to the disclosure of Figures 20A and 20G, but instead points to other figures in the specification and asserts that "every time the specification identifies any electrical component as being 'coupled to a reference potential,' the specification refers to the type of direct connection . . . not to a connection through another element." Intel Resp. Br. at 26. But that disclosure does *not* negate the disclosure related to Figures 20A and 20G regarding "coupled" being an *indirect* connection/coupling.

*Second*, Figures 20A and 20G do *not* refer to either the switch or capacitor "coupled to a reference potential." The specification refers to these components relative to the input signal 2004 (i.e., being in series with the input signal) or being shunted to ground.

FIG. 20A illustrates an aliasing module 2000 for down-conversion using a universal frequency translation (UFT) module 2002 which down-converts an EM input signal 2004. . . . [I]n one implementation, the switch 2008 is in series with input signal 2004 and capacitor 2010 is shunted to ground (although it may be other than ground in configurations such as differential mode). In a second implementation (see FIG. 20G), the capacitor 2010 is in series with the input signal 2004 and the switch 2008 is shunted to ground (although it may be other than ground in configurations such as differential mode).

*Id.* at 11:38-50.

*Third*, contrary to Intel’s assertion (Intel Resp. Br. at 22), the specification makes it clear that the switch, capacitor and reference potential of the frequency down-conversion module can be in any number of different configurations. With regard to the frequency down-conversion module (e.g., aliasing module of Figures 20A and 20G), the specification states that “[t]he electronic alignment of the circuit components is *flexible*.” ’474 patent, 11:42-43. Moreover, the specification discloses that Figures 20A and 20G are “implementation[s]” of the aliasing module. *Id.* at 11:43-50.

*Fourth*, Intel ignores the language of dependent claim 3 (below), which specifically recites the configuration of Figure 20G.

3. The apparatus of claim 1, wherein:  
the first storage element is coupled in series between the  
input signal and the first node; and  
the second storage element is coupled in series between the  
input signal and the second node.

As such, independent claim 1 is necessarily broader than claim 3 and, thus, should include the embodiment of Figure 20A.

*Finally*, Intel’s argument that its construction will help a jury is of no moment. Intel Resp. Br. at 24-25. An expert can explain the plain and ordinary meaning of the disputed term to the jury. For the foregoing reasons, Intel’s construction should be rejected and the term should be given its plain and ordinary meaning.

**G. “under-samples” (’444 patent, claim 2; ’474 patent, claim 6)**

| <b>ParkerVision’s Construction</b>                                          | <b>Intel’s Construction</b>                                                                                                                                        |
|-----------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| “sampling at an aliasing rate”                                              | “samples at less than or equal to twice the frequency of the input signal using negligible apertures (i.e., pulse widths) that tend towards zero time in duration” |
| “sampling at less than or equal to twice the frequency of the input signal” |                                                                                                                                                                    |

Intel’s position is that “under-sampling” / “under-samples” is synonymous with sample/hold systems and the use of negligible apertures. As such, according to Intel, “under-

samples” should be construed to include sampling “using negligible apertures (i.e., pulse widths) that tend towards zero time in duration.” Though Intel cites numerous passages from the specification to support its position, it conveniently *omits* the other portions of the specification demonstrating that Intel is wrong. In particular, the specification makes it clear that under-sampling is performed by energy transfer system using non-negligible apertures.

FIGS. 83A-F illustrate example timing diagrams for the energy transfer system 8202 in FIG. 82. . . . FIG. 83C illustrates an example under-sampling signal 8304, including energy transfer pulses 8306 having non-negligible apertures . . .

’518 patent, 67:5-10. *See also* ParkerVision Resp. Br. at 20-21. As such, it is no surprise that the Jacksonville court *rejected* the same argument that Intel makes here. D.I. 51-2 at 7-8.

Indeed, Intel’s position regarding “under-samples” is contradicted by its *own* statements earlier in its responsive brief where Intel admits that a “sample and hold” system is merely an *example* of a system that performs “under-sampling.” According to Intel, “the term ‘sample and hold’ is used only as an example of ‘under-sampling.’” Intel Br. at 2 (emphasis in original). Intel also recognized that the patents “disclos[e] ‘sample and hold’ as an ‘example’ of ‘under-sampling’ for ‘purposes of illustration, and not limitation.’” *Id.* For the foregoing reasons, ParkerVision’s construction should be adopted.

#### **H. The six terms (11 claims) into which Intel seeks to inject “aliasing rate”**

At bottom, Intel’s argument is that sampling an EM signal at an “aliasing rate” is “the” invention and, thus, the six disputed terms<sup>10</sup> (and all of the independent claims) must include Intel’s specific aliasing rate language. But Intel’s argument rests on the *false* premise that the concept of “aliasing rate” is not already in the claims that include these terms. As shown in the

---

<sup>10</sup> The terms are “system for frequency down-converting,” “apparatus for down-converting,” “frequency down-conversion module,” “universal frequency down-converter,” “energy transfer module,” and “aliasing module.”

chart below, the concept of “aliasing rate” is *already* in the claims.<sup>11</sup> Intel just does not like where the language is found in the claims. See ParkerVision Resp. Br. at 23.

| <b>Claim</b>          | <b>Aliasing rate language already recited in the claim</b>                                                                                                                                                                                                                                                                                                                           |
|-----------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| '725 patent, claim 1  | “wherein said control signal operates at an <u>aliasing rate</u> selected so that energy of the RF information signal is <i>sampled and applied</i> to the storage module at a <u>frequency</u> that is equal to or less than twice the frequency of the RF information signal”                                                                                                      |
| '518 patent, claim 50 | “wherein said pulse generator outputs pulses to said switch at an <u>aliasing rate</u> that is determined according to: (a <u>frequency</u> of the carrier signal +/— a frequency of the lower frequency signal) divided by N”                                                                                                                                                       |
| '673 patent, claim 1  | “said pulse generator outputting pulses to said switch at a <u>rate</u> that is a function of a frequency of the modulated carrier signal and a frequency of the demodulated baseband signal determined according to: (the <u>frequency</u> of the modulated carrier signal +/— a frequency of the demodulated baseband signal) divided by N, where N is any integer including 1”    |
| '902 patent, claim 1  | “said energy transfer module <i>sampling</i> the electromagnetic signal at an <u>energy transfer rate</u> , according to an energy transfer signal, . . . said energy transfer signal having a control <u>frequency</u> that is substantially equal to said energy transfer rate”                                                                                                    |
| '513 patent, claim 19 | “a first switch, a first control signal which comprises a <i>sampling aperture</i> with a specified <u>frequency</u> ”<br><br>“a second switch, a second control signal which comprises a <i>sampling aperture</i> with a specified <u>frequency</u> ”<br><br>“a third switch, a third control signal which comprises a <i>sampling aperture</i> with a specified <u>frequency</u> ” |
| '528 patent, claim 1  | “a first switch coupled to a first control signal which comprises a <i>sampling aperture</i> with a specified <u>frequency</u> ”<br><br>“a second switch coupled to a second control signal which comprises a <i>sampling aperture</i> with a specified <u>frequency</u> ”                                                                                                           |
| '736 patent, claim 1  | “a first switch coupled to a first control signal which comprises a first <i>sampling aperture</i> with a specified <u>frequency</u> ”<br><br>“a second switch coupled to a second control signal which comprises a second <i>sampling aperture</i> with a specified <u>frequency</u> ”                                                                                              |
| '673 patent, claim 13 | “a controller coupled to a switch, the controller providing a <i>control signal</i> with a specified <u>frequency</u> that controls when the switch is on and when                                                                                                                                                                                                                   |

<sup>11</sup> Claim 3 of the '444 patent does not expressly include the concept of an aliasing rate. But the claim recites “control signals.” Consistent with the other claims in the chart, the aliasing rate would be tied to the term “control signal,” not to the term “frequency down-conversion module” as Intel suggests.

|                                    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                    | the switch is off”                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| ’474 patent, claim 1               | <p>Claim 6, which depends from claim 1, recites:</p> <p>“the first switch <i>under-samples</i> the input signal according to the first control signal; and the second switch <i>under-samples</i> the input signal according to the second control signal.”</p> <p><u>NOTE</u>: While the parties’ constructions of “under-samples” are different, the parties agree that “under-samples” is sampling at an aliasing rate, which is less than or equal to twice the frequency of the input signal.</p>             |
| ’444 patent, claim 2 <sup>12</sup> | <p>“wherein said first frequency down-conversion module <i>under-samples</i> said input signal according to said first control signal, and said second frequency down-conversion module <i>under-samples</i> said input signal according to said second control signal”</p> <p><u>NOTE</u>: While the parties’ constructions of “under-samples” are different, the parties agree that “under-samples” is sampling at an aliasing rate, which is less than or equal to twice the frequency of the input signal.</p> |

Ironically, Intel concludes its brief by asserting that when drafting the patents-in-suit, “ParkerVision had the power of the pen” (Intel Resp. Br. at 45), yet Intel seeks to rewrite the claims and ignore how the patentees chose to write its claims. *See ParkerVision Resp. Br. at 23-30*. In particular, since the claims as written do not work for Intel’s non-infringement case, Intel seeks to inject *additional* instances of aliasing rate in the claims – into the broader system, apparatus, module and down-converter terms. There is no reason to do so.

Indeed, Intel and its expert admit that the concept of aliasing rate is *already* included in the claims. With regard to claim 1 of the ’725 patent, while recognizing that the claim recites the exact aliasing rate language, Intel’s only argument is that Intel’s construction is consistent with the existing language, which is more specific. Intel Resp. Br. at 13. As to claim 1 of the ’902

---

<sup>12</sup> For the first time in its responsive brief, Intel now asserts that “frequency down-conversion module” in claim 2 of the ’444 patent is a means-plus-function term. Intel Resp. Br. at 10 n. 6. Intel is incorrect. *First*, the term does not use the term “means.” *Second*, the term does not merely recite any type of module but, rather, recites a specific type of module – *frequency down-conversion* module. Such modules have known structural components – switches and capacitors.

patent, Intel admits that “the ‘energy transfer rate’ in the claim *is an aliasing rate that aliases the signal.*” *Id.* at 16. Moreover, Intel and its expert acknowledge that claim 50 of the ’518 patent and claim 1 of the ’673 patent recite a specific aliasing rate (see table above). *See id.* at 14-15 (citing D.I. 58-5 at ¶¶10-35). Intel’s expert states that these rates are *less than* twice the input frequency and, thus, fall within the range of Intel’s aliasing rate – “less than or equal to twice the frequency” of the input signal. Even assuming Intel’s expert is correct, that is no reason to change how the patentees wrote the claim to recite an aliasing rate that is *equal to* twice the frequency. For the foregoing reasons, there is no reason why the claim language would have to include Intel’s specific “aliasing rate” in an *additional* portion of the claim. Accordingly, Intel’s constructions should be rejected and the terms should be given their plain and ordinary meaning.<sup>13</sup>

**I. “a capacitor that reduces a DC offset voltage in said first down-converted signal and said second down-converted signal” (’444 patent, claim 4)**

| <b>ParkerVision’s Construction</b> | <b>Intel’s Construction</b>                                                                                                   |
|------------------------------------|-------------------------------------------------------------------------------------------------------------------------------|
| Plain and ordinary meaning         | “a capacitor that reduces a DC offset voltage in both said first down-converted signal and said second down-converted signal” |

As with so many other terms, Intel is attempting to change the meaning of the claim language. Indeed, Intel continues to read the claim language in the abstract, isolated from the specification. As ParkerVision pointed out in its briefs, the claim language aligns with the description of Figure 70A. ParkerVision Op. Br. at 36; ParkerVision Resp. Br. at 30. Tellingly, after two rounds of briefing Intel is still unable to point to a single embodiment that supports its

---

<sup>13</sup> Though ParkerVision proposed a construction of “universal frequency down-converter,” it only did so because Intel sought a construction and the Jacksonville court already construed the term. D.I. 51-2 at 38. An expert, however, can explain to a jury that what makes a frequency down-converter a “universal” frequency down-converter is that it can down-convert multiple frequencies. *See* ParkerVision Op. Br. at 31. As such, ParkerVision believes that plain and ordinary meaning for this term would also be appropriate.

reading of the claim. There is none. And an expert can explain the plain and ordinary meaning of the disputed term to the jury. For the foregoing reasons, Intel's construction should be rejected and the term should be given its plain and ordinary meaning.

**J. "DC offset voltage" ('444 patent, claim 4)**

| <b>ParkerVision's Construction</b>                   | <b>Intel's Construction</b>                                                     |
|------------------------------------------------------|---------------------------------------------------------------------------------|
| "a deviation of DC voltage from a reference voltage" | "a DC voltage level that is added to a signal of interest by related circuitry" |

Intel has not raised any new arguments regarding this term. For the reasons set forth in ParkerVision's opening and responsive claim construction briefs, ParkerVision's construction should be adopted.

**K. Terms alleged to be indefinite.**

Intel's responsive brief does not raise any new issues regarding indefiniteness. For the reasons set forth in ParkerVision's responsive claim construction brief (ParkerVision Resp. Br. at 32-39) and the attached declaration, the terms are not indefinite and should be given their plain and ordinary meaning. *See* Steer Decl. ¶¶17-39.

Dated: December 11, 2020

/s/ Raymond W. Mort, III  
Raymond W. Mort, III  
Texas State Bar No. 00791308

THE MORT LAW FIRM, PLLC  
100 Congress Avenue, Suite 2000  
Austin, Texas 78701  
Tel/Fax: 512-865-7950

*Of Counsel:*  
Ronald M. Daignault (*pro hac vice*)  
Chandran B. Iyer (*pro hac vice*)  
Jason S. Charkow (*pro hac vice*)  
Stephanie R. Mandir (*pro hac vice*)  
rdaignault@goldbergsegalla.com

ciyer@goldbergsegalla.com  
jcharkow@goldbergsegalla.com  
smandir@goldbergsegalla.com  
GOLDBERG SEGALLA LLP  
711 Third Avenue, Suite 1900  
New York, New York 10017  
Telephone: (646) 292-8700

*Attorneys for ParkerVision, Inc.*