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- [54] **INTEGRATED FREQUENCY TRANSLATION AND SELECTIVITY**
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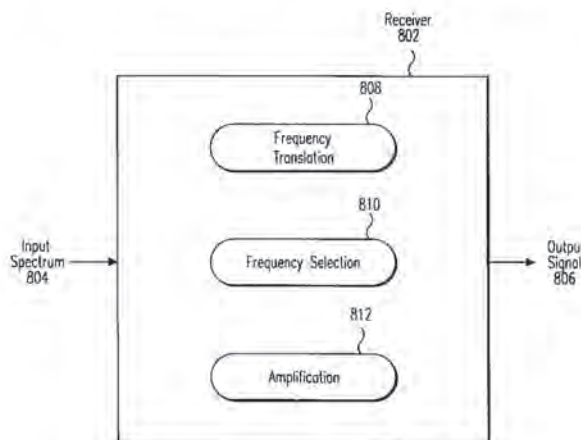
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[57] ABSTRACT

Methods and apparatuses for frequency selectivity and frequency translation, and applications for such methods and apparatuses, are described herein. The method includes steps of filtering an input signal, and down-converting the filtered input signal. The filtering and the down-conversion operations are performed in an integrated, unified manner. The apparatus described herein can be implemented as an integrated circuit (IC).

194 Claims, 55 Drawing Sheets



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- Copy of Declaration of Alex Holtz filed in patent application Ser. No. 09/176,022, which is directed to related subject matter.
- Copy of Declaration of Richard C. Looke filed in patent application Ser. No. 09/176,022, which is directed to related subject matter.
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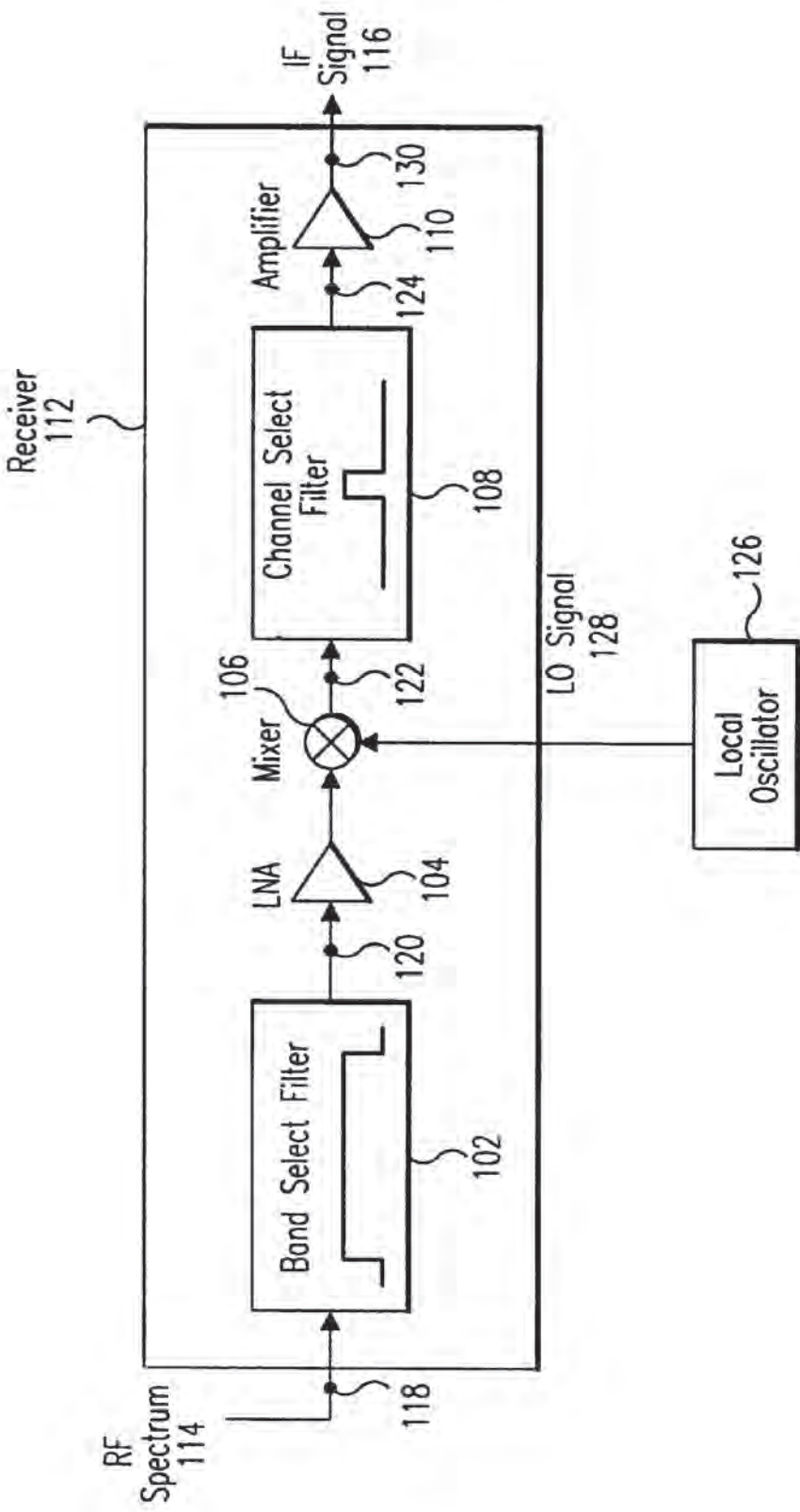


FIG. 1
Related Art

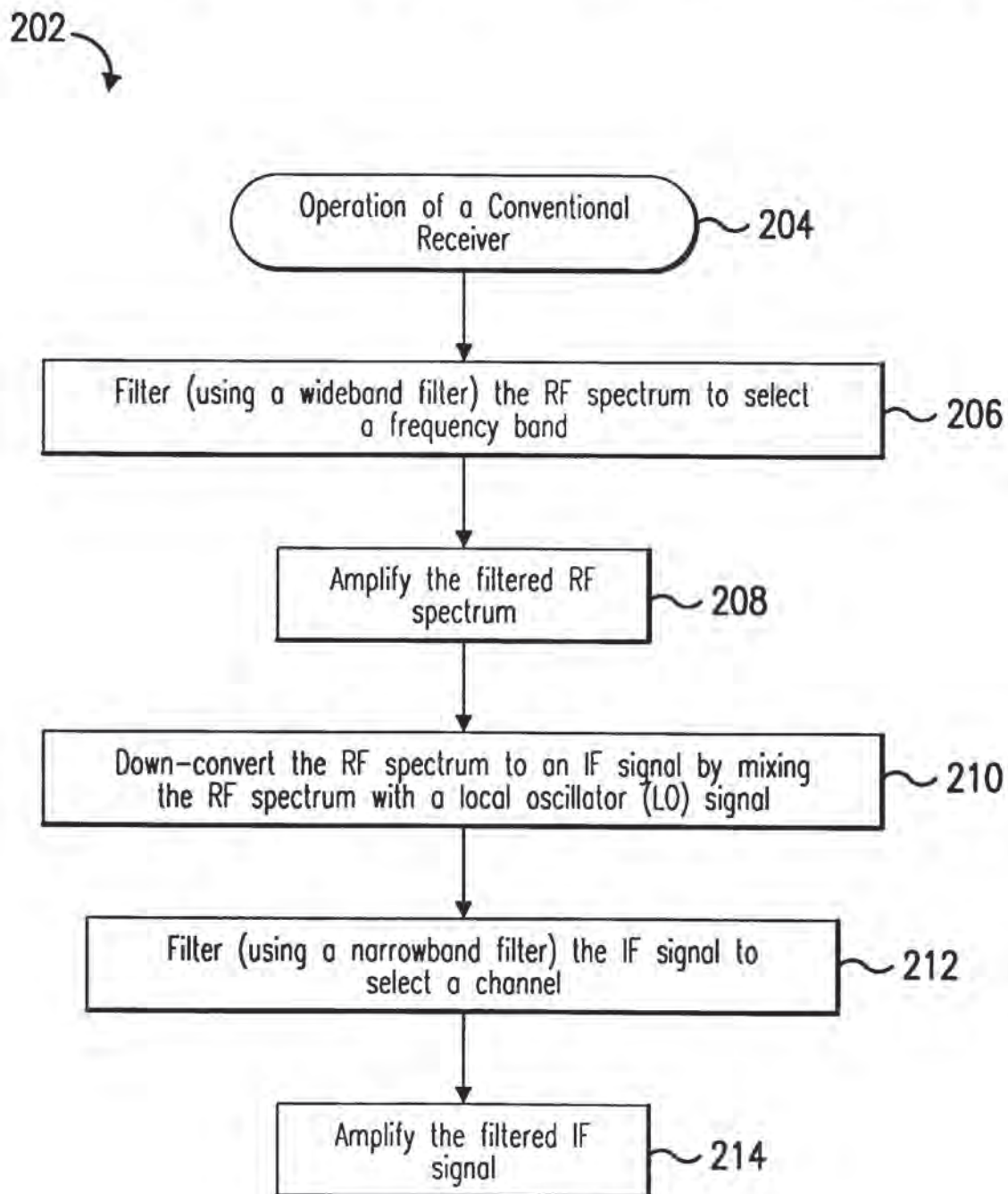


FIG.2
Related Art

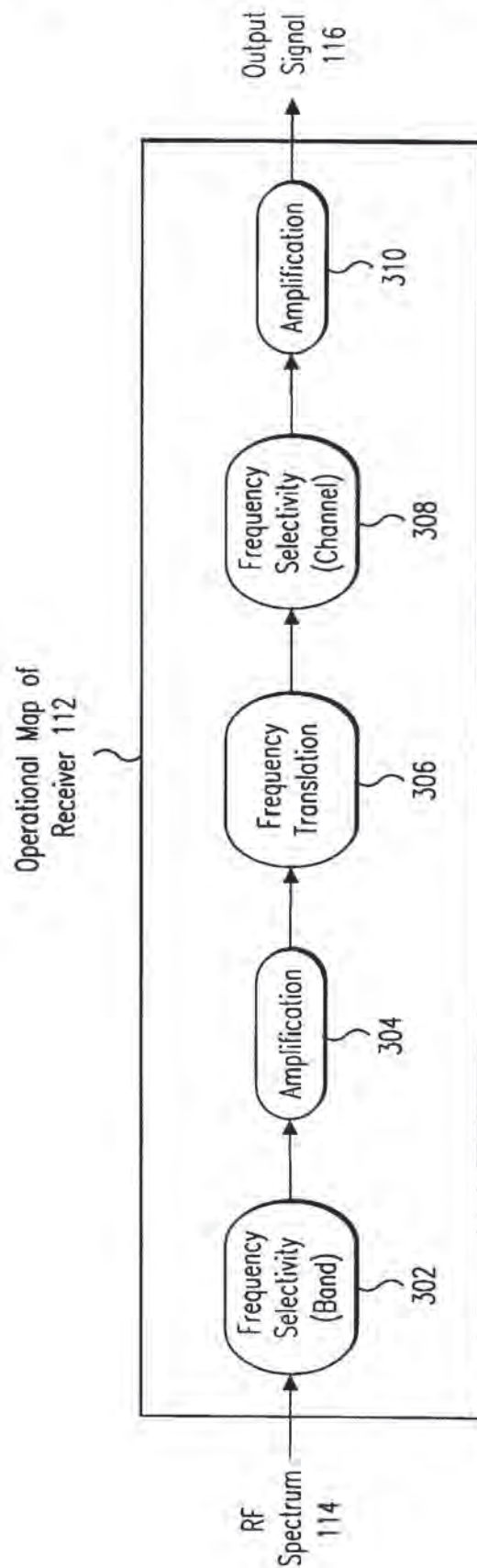


FIG. 3
Related Art

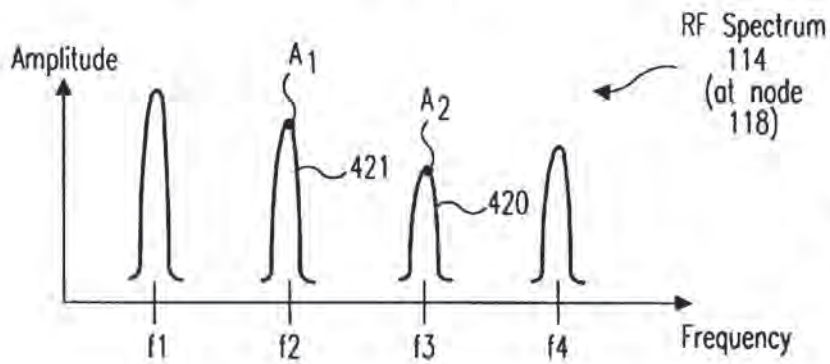


FIG. 4A
Related Art

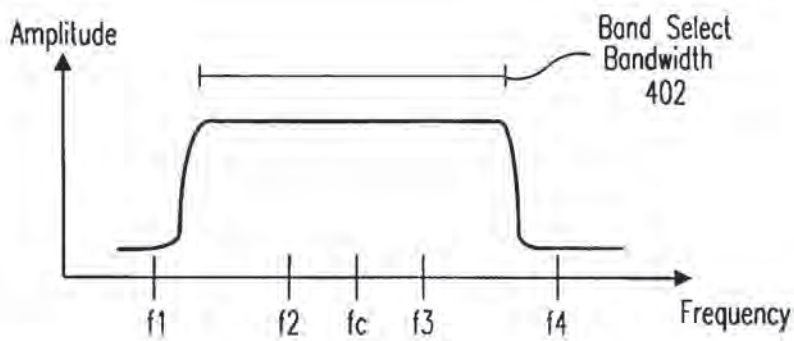


FIG. 4B
Related Art

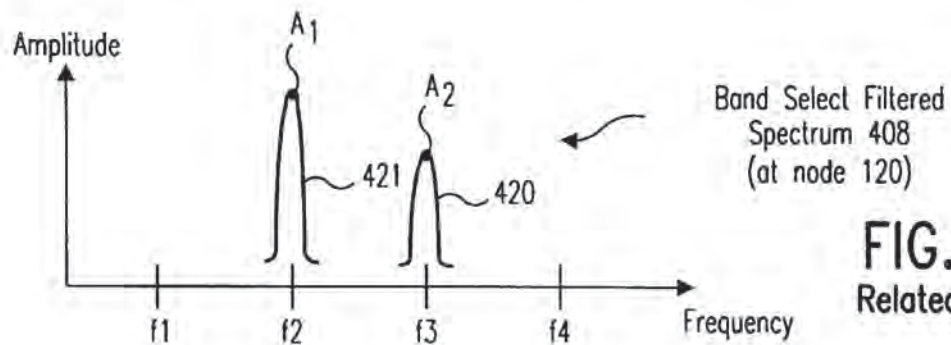


FIG. 4C
Related Art

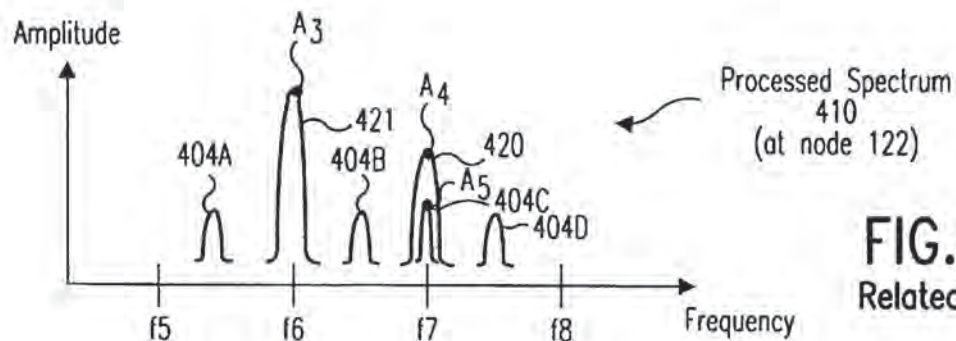


FIG. 4D
Related Art

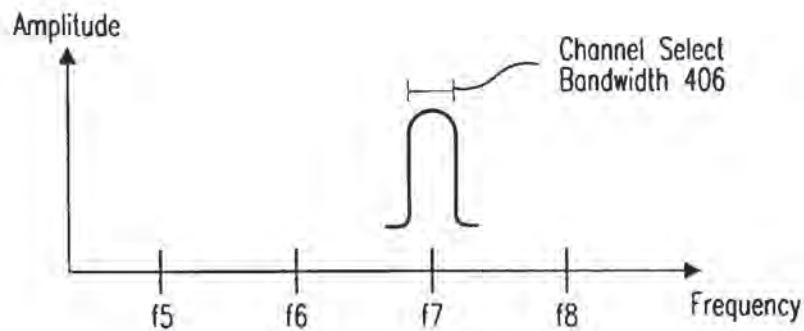


FIG. 4E
Related Art

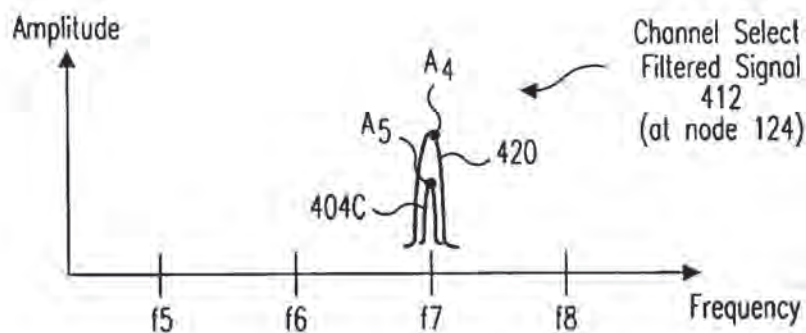


FIG. 4F
Related Art

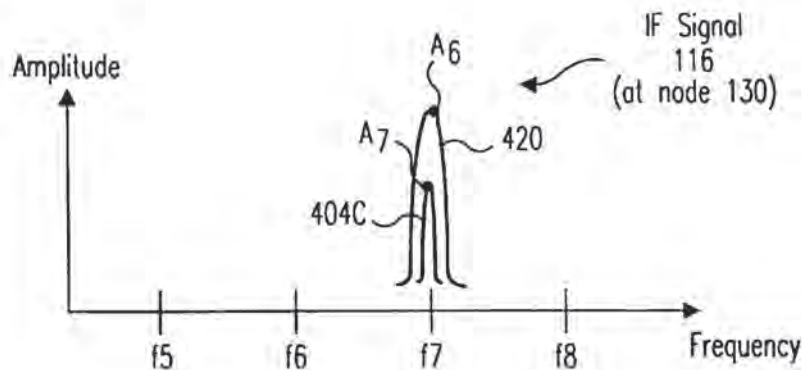
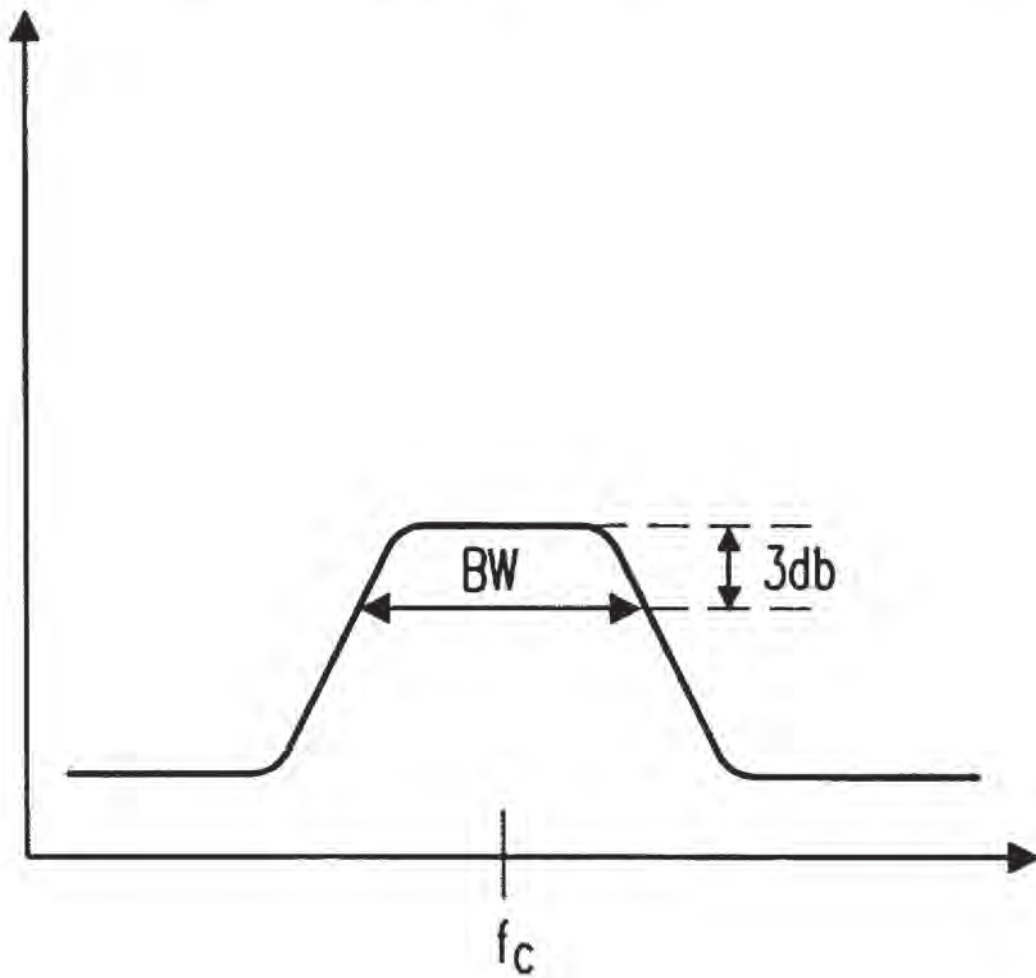


FIG. 4G
Related Art



$$Q = \text{Quality Factor} = \frac{f_c}{BW}$$

FIG.5
Related Art

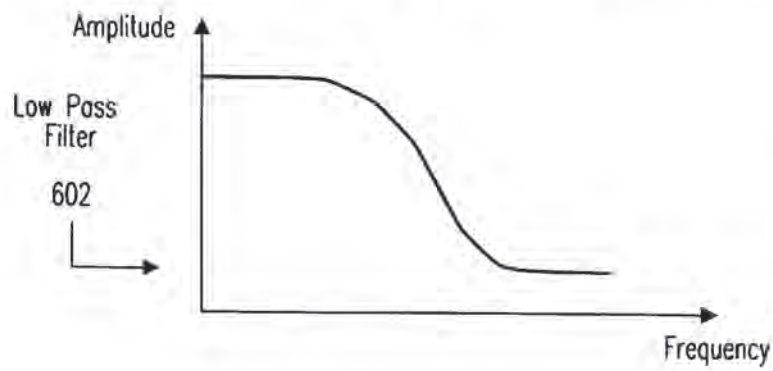


FIG. 6A
Related Art

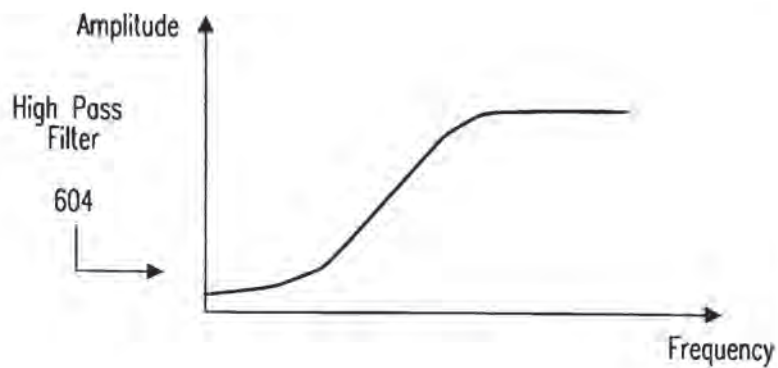


FIG. 6B
Related Art

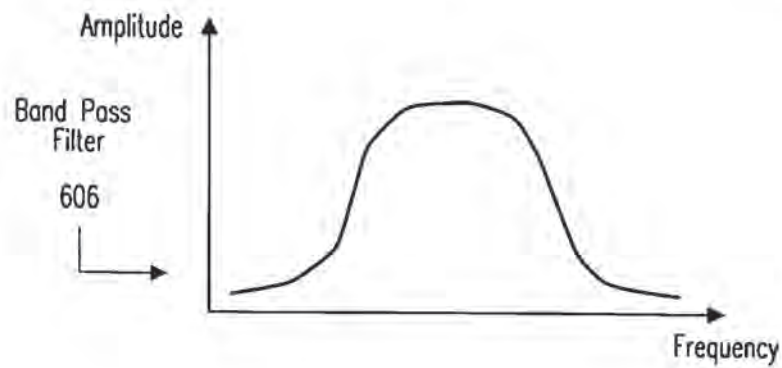


FIG. 6C
Related Art

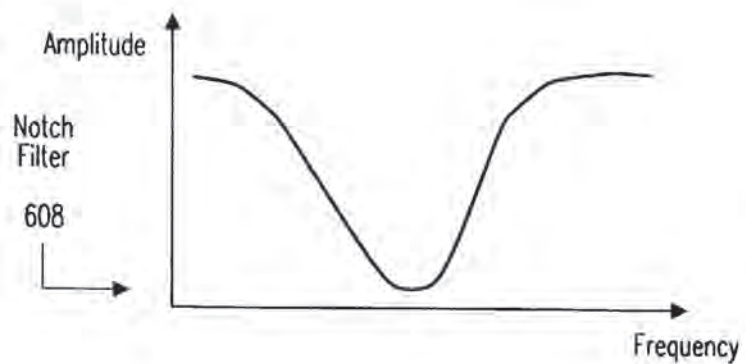


FIG. 6D
Related Art

Example 702
Phase Modulation

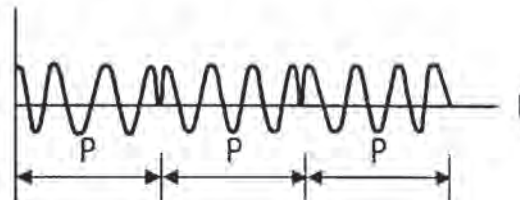


FIG. 7A
Related Art

Example 704
Frequency Modulation

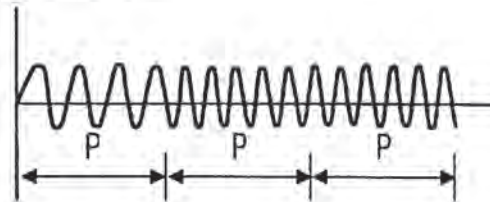


FIG. 7B
Related Art

Example 706
Amplitude Modulation

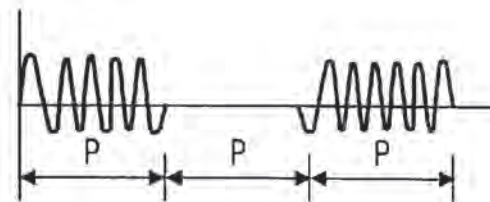


FIG. 7C
Related Art

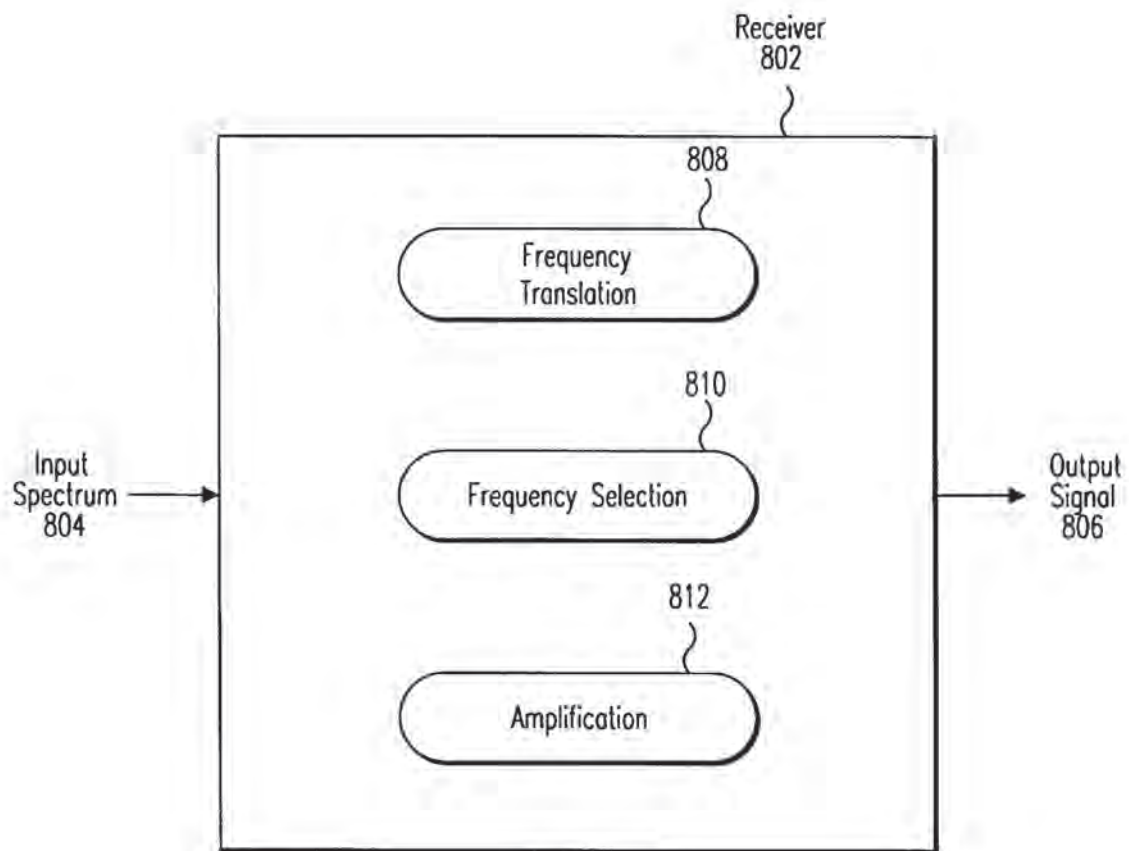


FIG.8

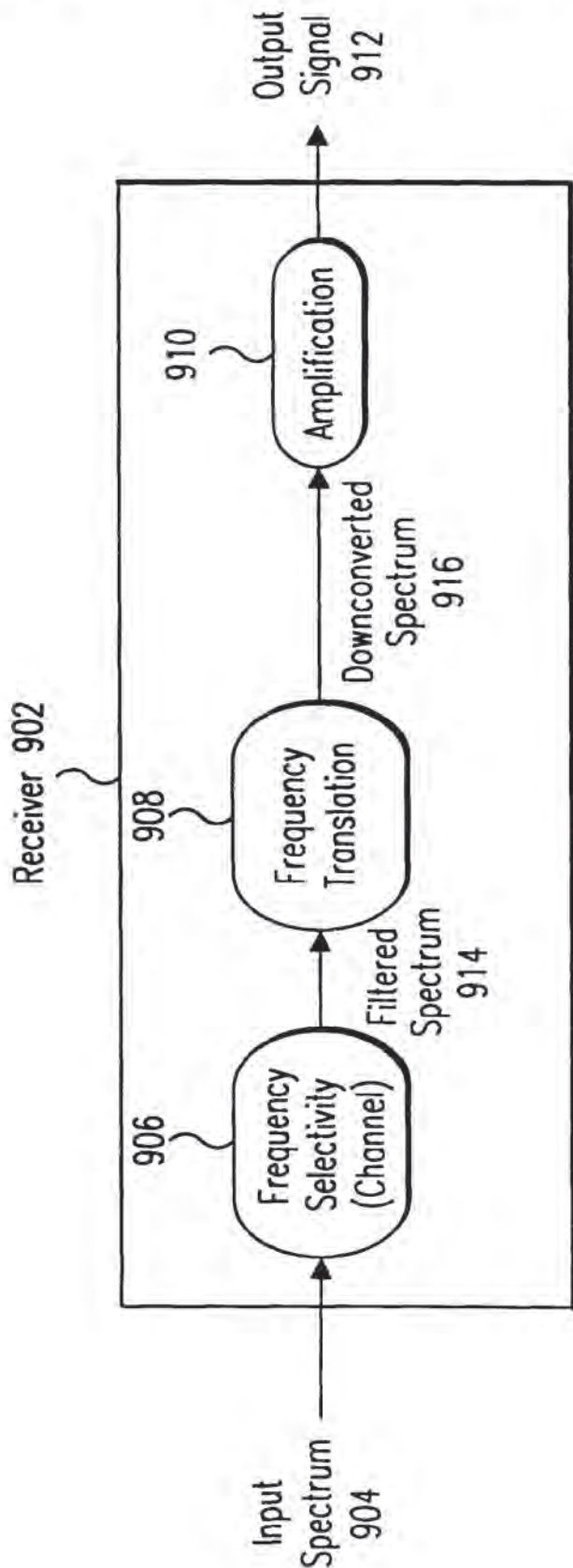


FIG. 9

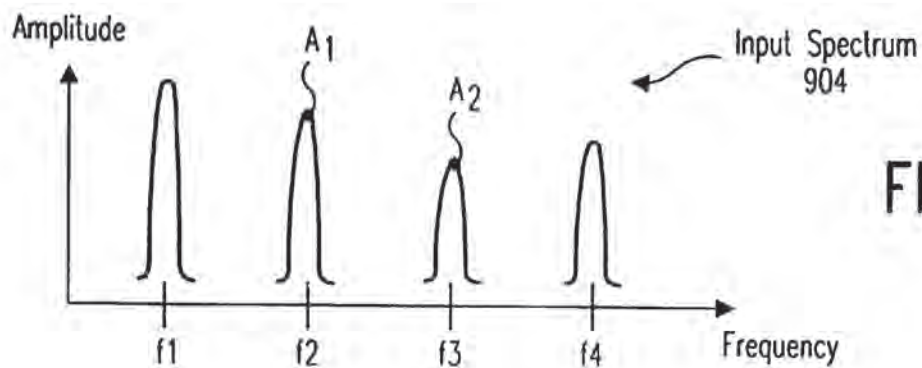


FIG. 10A

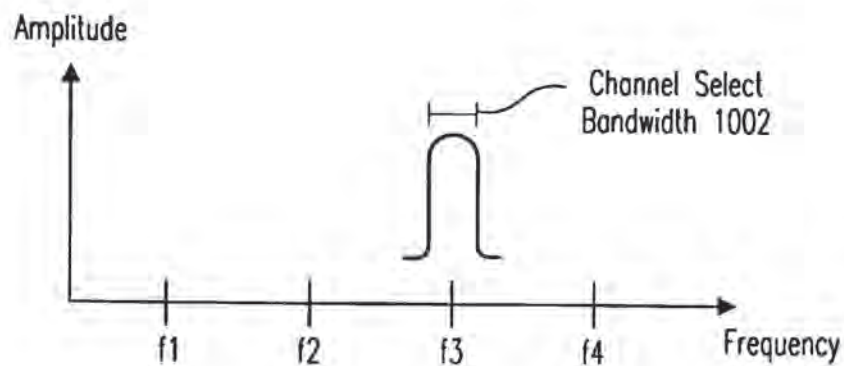


FIG. 10B

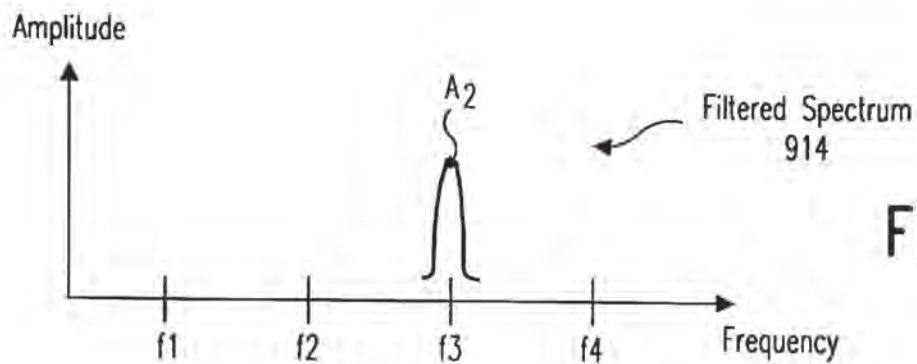


FIG. 10C

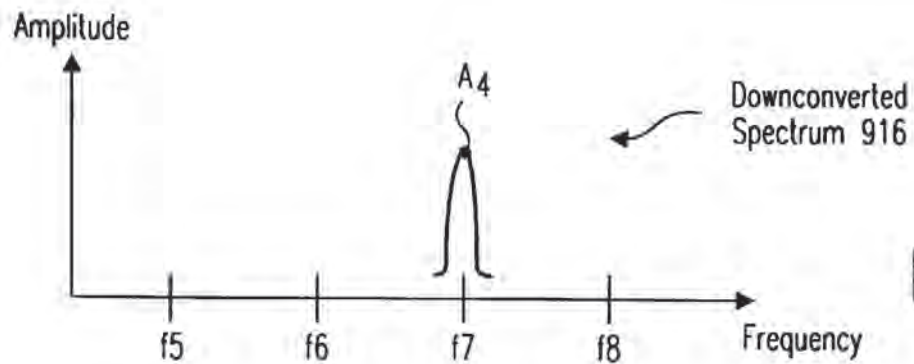


FIG. 10D

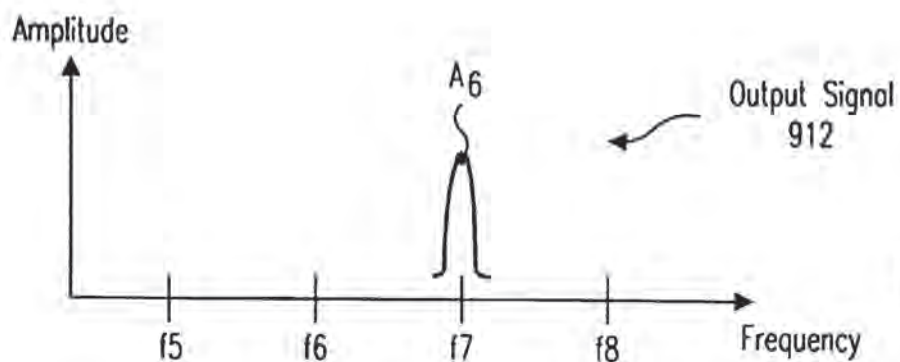


FIG. 10E

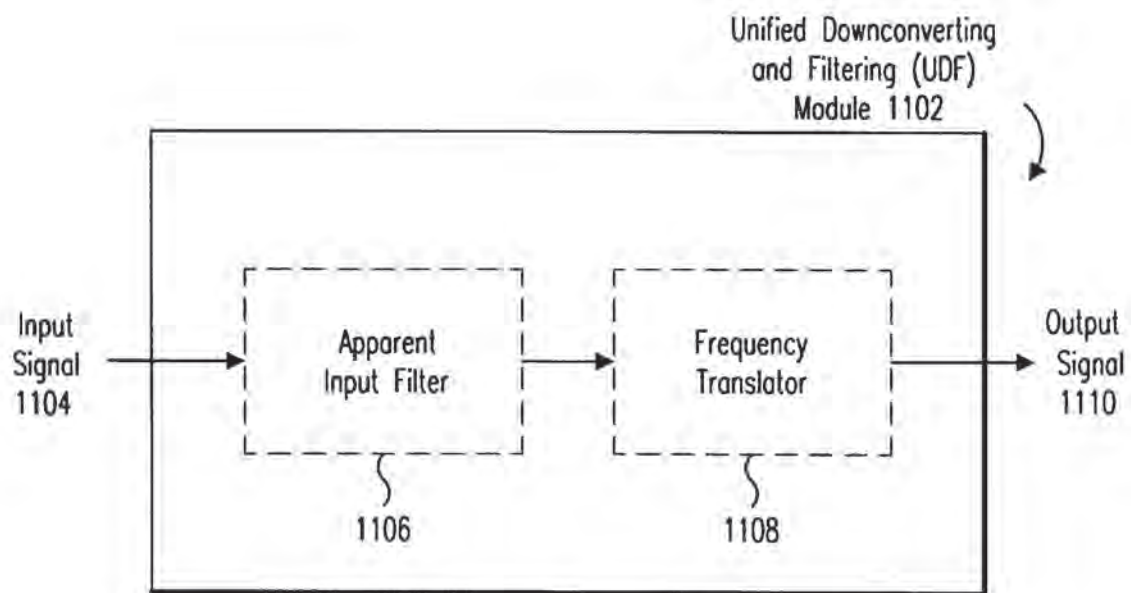


FIG. 11

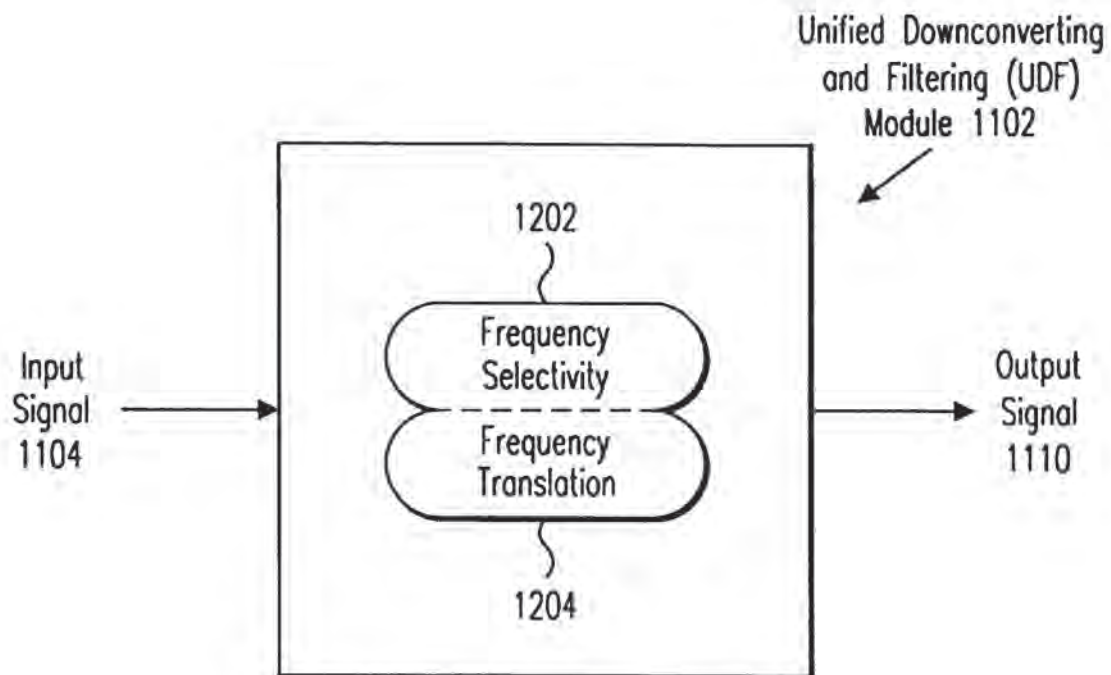


FIG.12

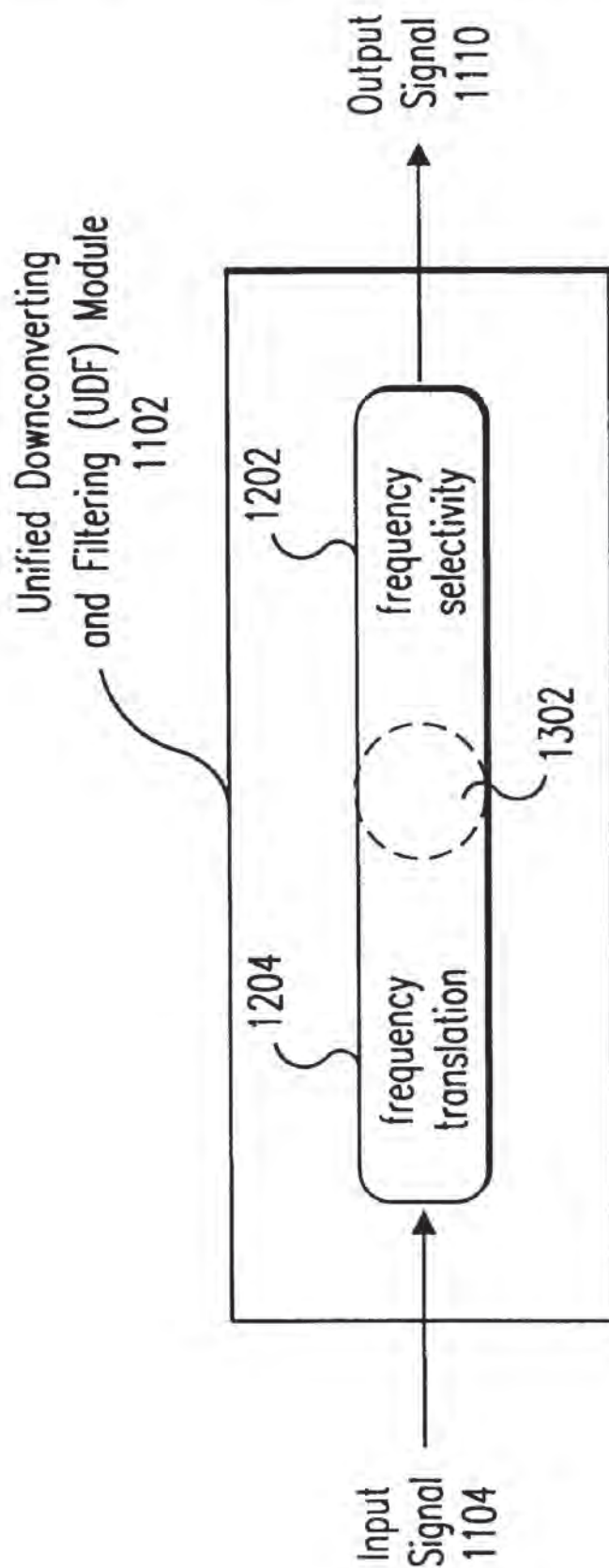


FIG.13

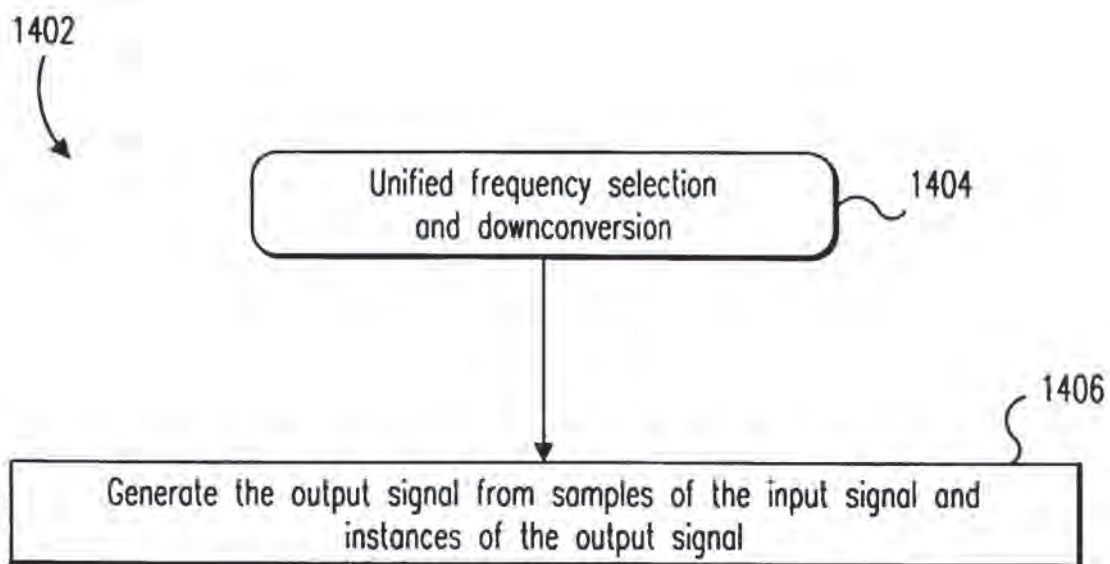


FIG.14

1502



Time Node	t (rising edge of ϕ_1)	$t-1$ (rising edge of ϕ_2)	t (rising edge of ϕ_1)	t (rising edge of ϕ_2)	$t+1$ (rising edge of ϕ_1)
2602	V_{t-1} 1504	V_{t-1} 1508	V_t 1516	V_t 1526	V_{t+1} 1538
2604	—	V_{t-1} 1510	V_{t-1} 1518	V_t 1528	V_t 1540
2606	V_{0t-1} 1506	V_{0t-1} 1512	V_{0t} 1520	V_{0t} 1530	V_{0t+1} 1542
2608	—	V_{0t-1} 1514	V_{0t-1} 1522	V_{0t} 1532	V_{0t} 1544
2610	— 1507	—	V_{0t-1} 1524	V_{0t-1} 1534	V_{0t} 1546
2612	—	— 1515	—	V_{0t-1} 1536	V_{0t-1} 1548
2618	—	—	—	—	$V_t - \frac{1550}{0.1 * V_{0t} - 0.8 * V_{0t-1}}$

FIG.15

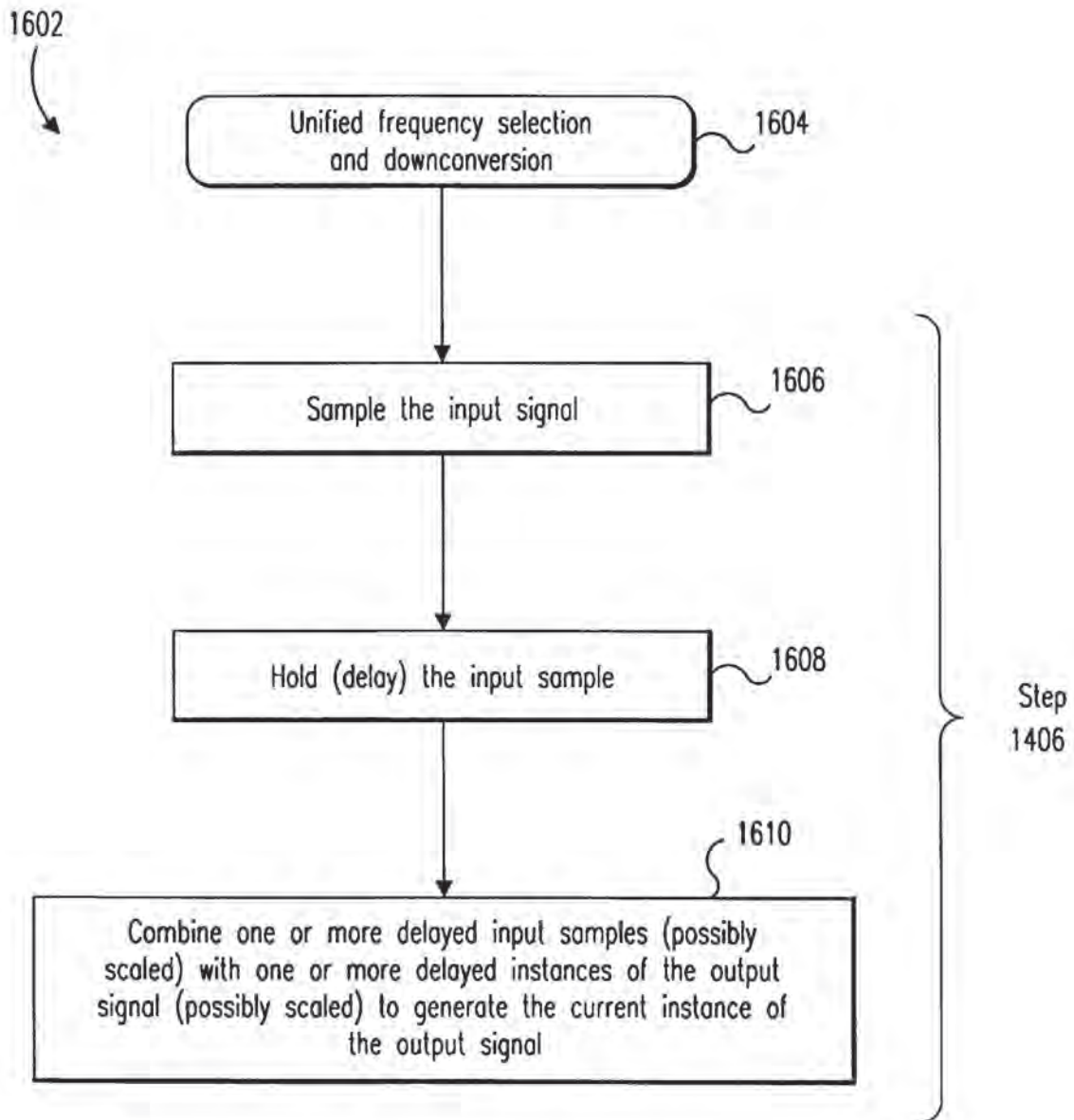


FIG.16

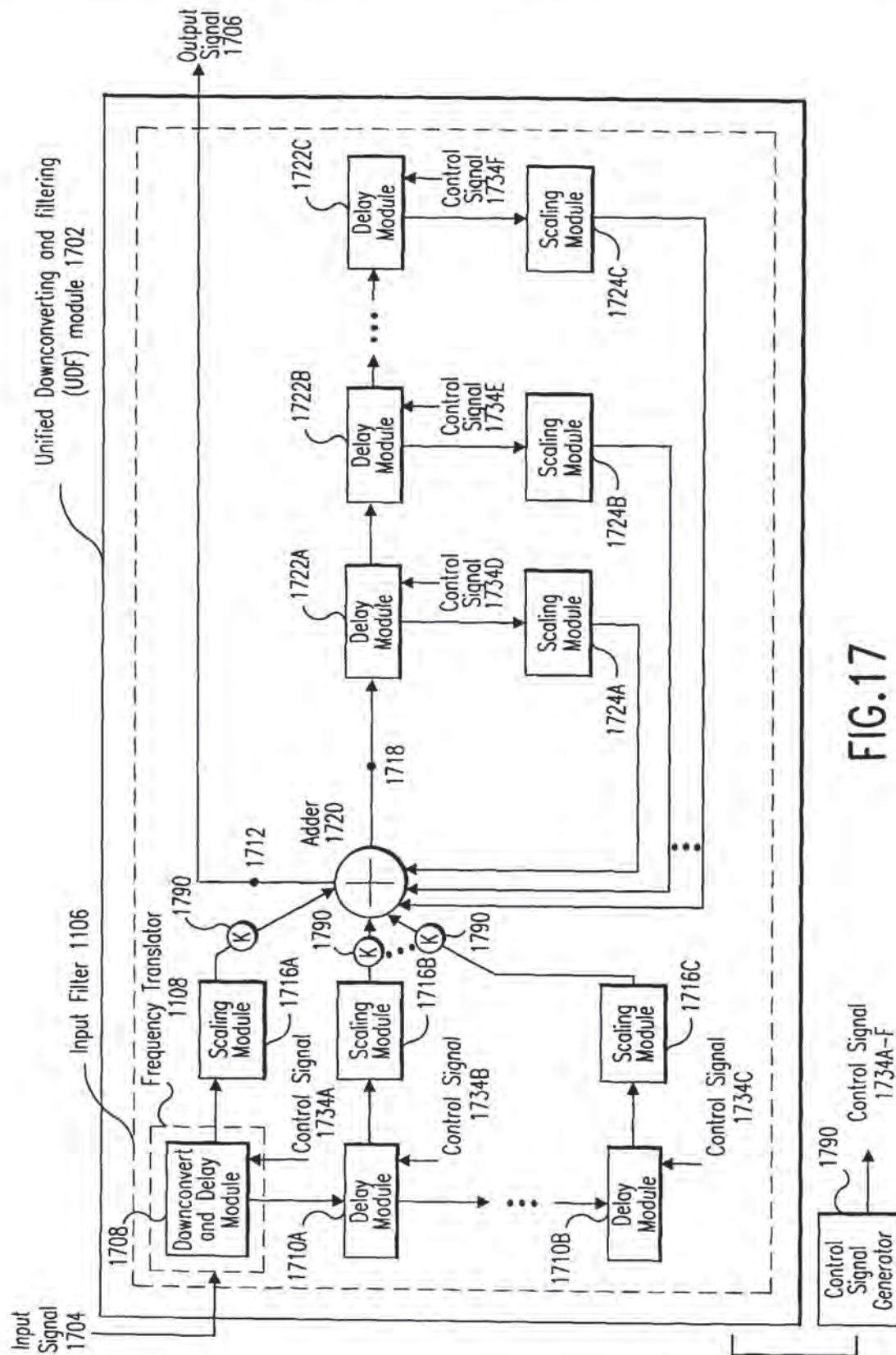


FIG.17

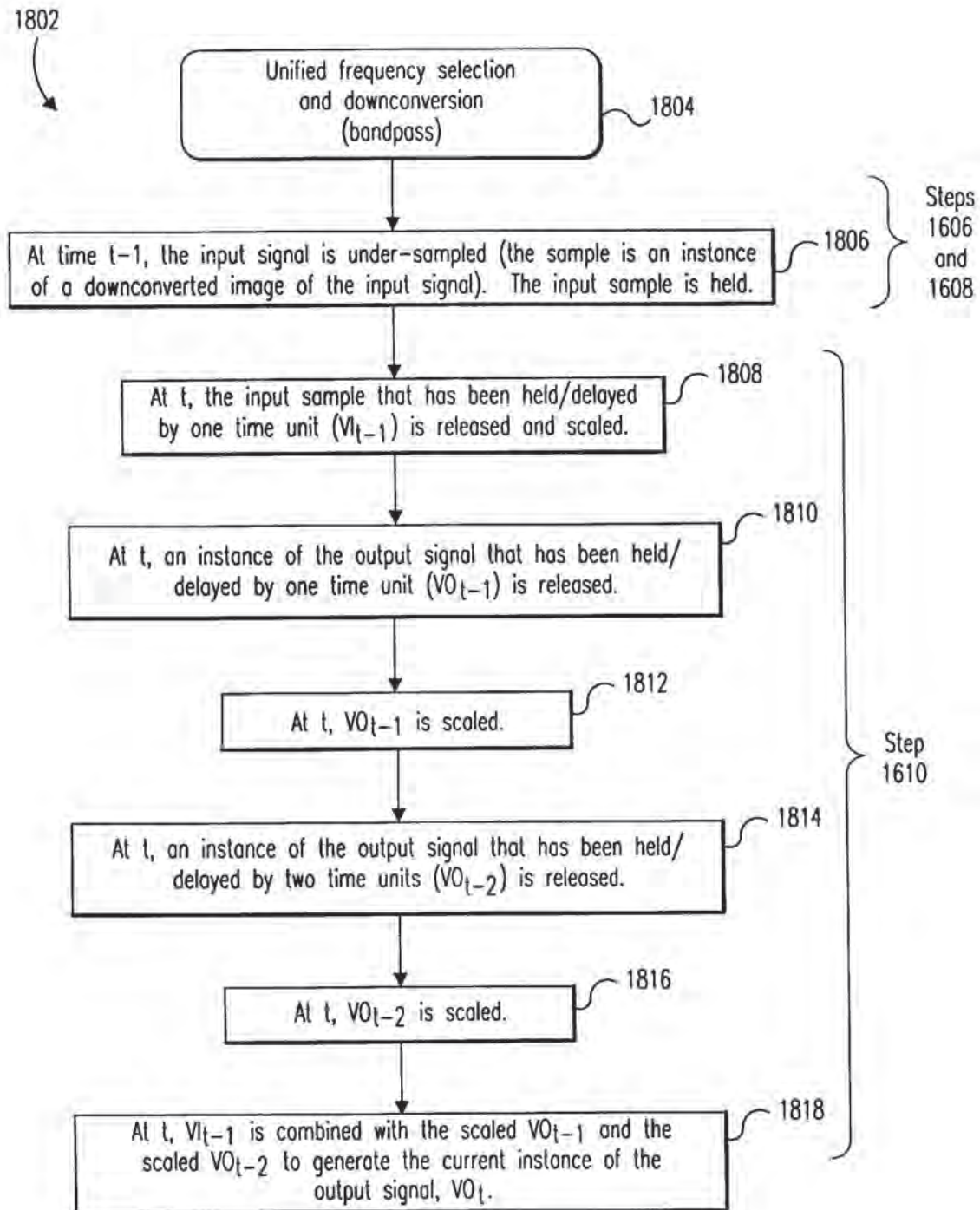


FIG.18

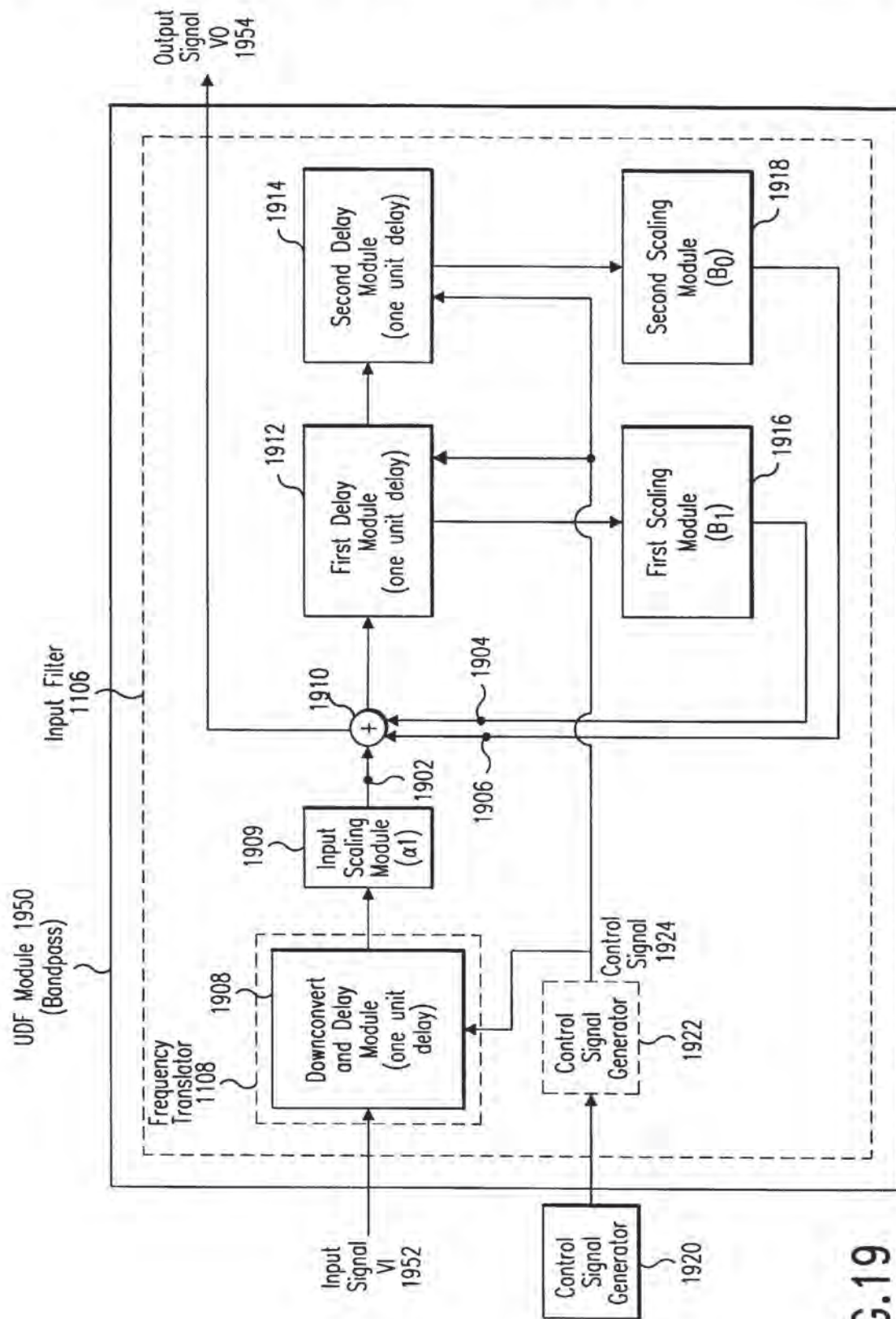


FIG. 19

2002



Time Value	t-2	t-1	t	t+1
Value held in Downconvert and Delay Module	VI_{t-2}	VI_{t-1} <u>2004</u>	VI_t	VI_{t+1}
Value at node 1902	$\alpha_1 * VI_{t-3}$	$\alpha_1 * VI_{t-2}$	$\alpha_1 * VI_{t-1}$ <u>2006</u>	$\alpha_1 * VI_t$
Value of Output Signal VO	$VO_{t-2} = \alpha_1 * VI_{t-3} - B_1 * VO_{t-3} - B_0 * VO_{t-4}$	$VO_{t-1} = \alpha_1 * VI_{t-2} - B_1 * VO_{t-2} - B_0 * VO_{t-3}$	$VO_t = \alpha_1 * VI_{t-1} - B_1 * VO_{t-1} - B_0 * VO_{t-2}$ <u>2008</u>	$VO_{t+1} = \alpha_1 * VI_t - B_1 * VO_t - B_0 * VO_{t-1}$
Value held in First Delay Module	VO_{t-2}	VO_{t-1}	VO_t <u>2010</u>	VO_{t+1}
Value at node 1904	$-B_1 \cdot VO_{t-3}$	$-B_1 \cdot VO_{t-2}$	$-B_1 \cdot VO_{t-1}$ <u>2012</u>	$-B_1 \cdot VO_t$
Value held in Second Delay Module	VO_{t-3}	VO_{t-2}	VO_{t-1} <u>2014</u>	VO_t
Value at node 1906	$-B_0 \cdot VO_{t-4}$	$-B_0 \cdot VO_{t-3}$	$-B_0 \cdot VO_{t-2}$ <u>2016</u>	$-B_0 \cdot VO_{t-1}$

FIG.20

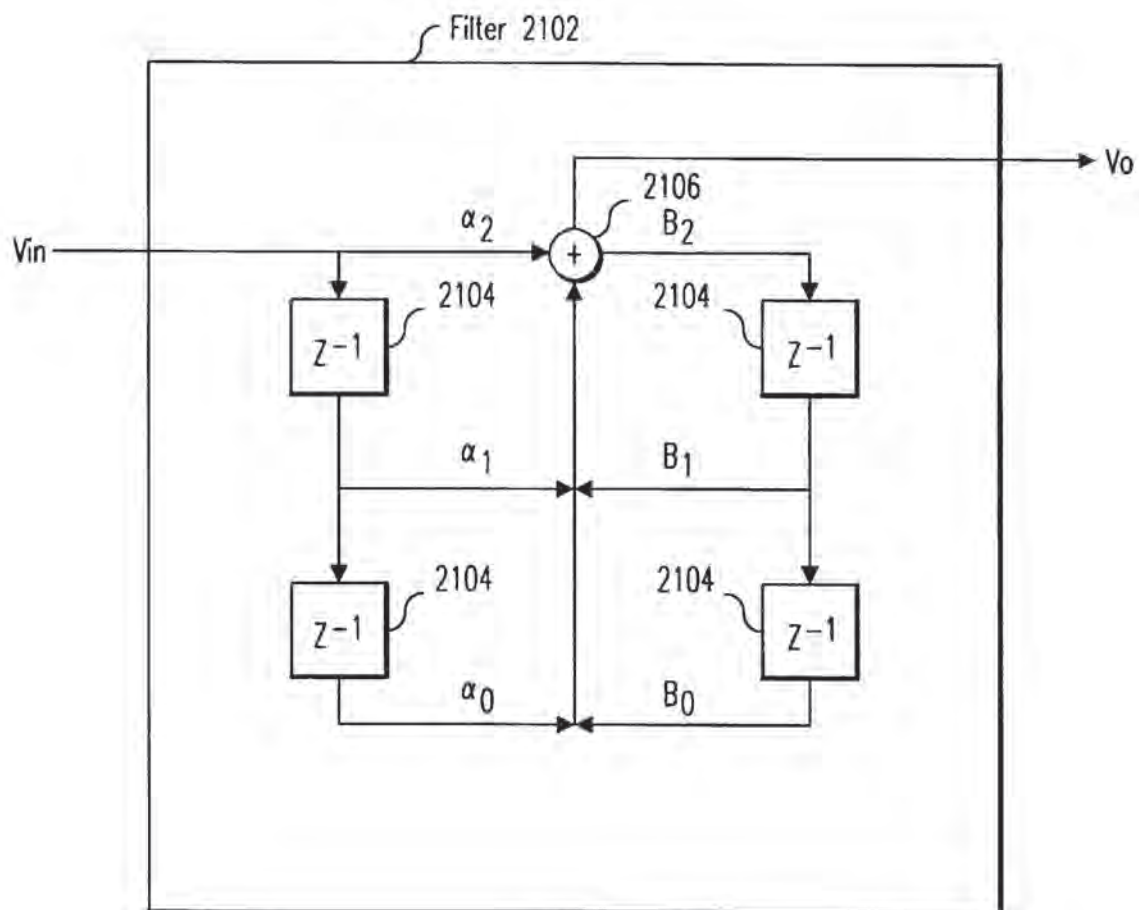


FIG. 21
Related Art

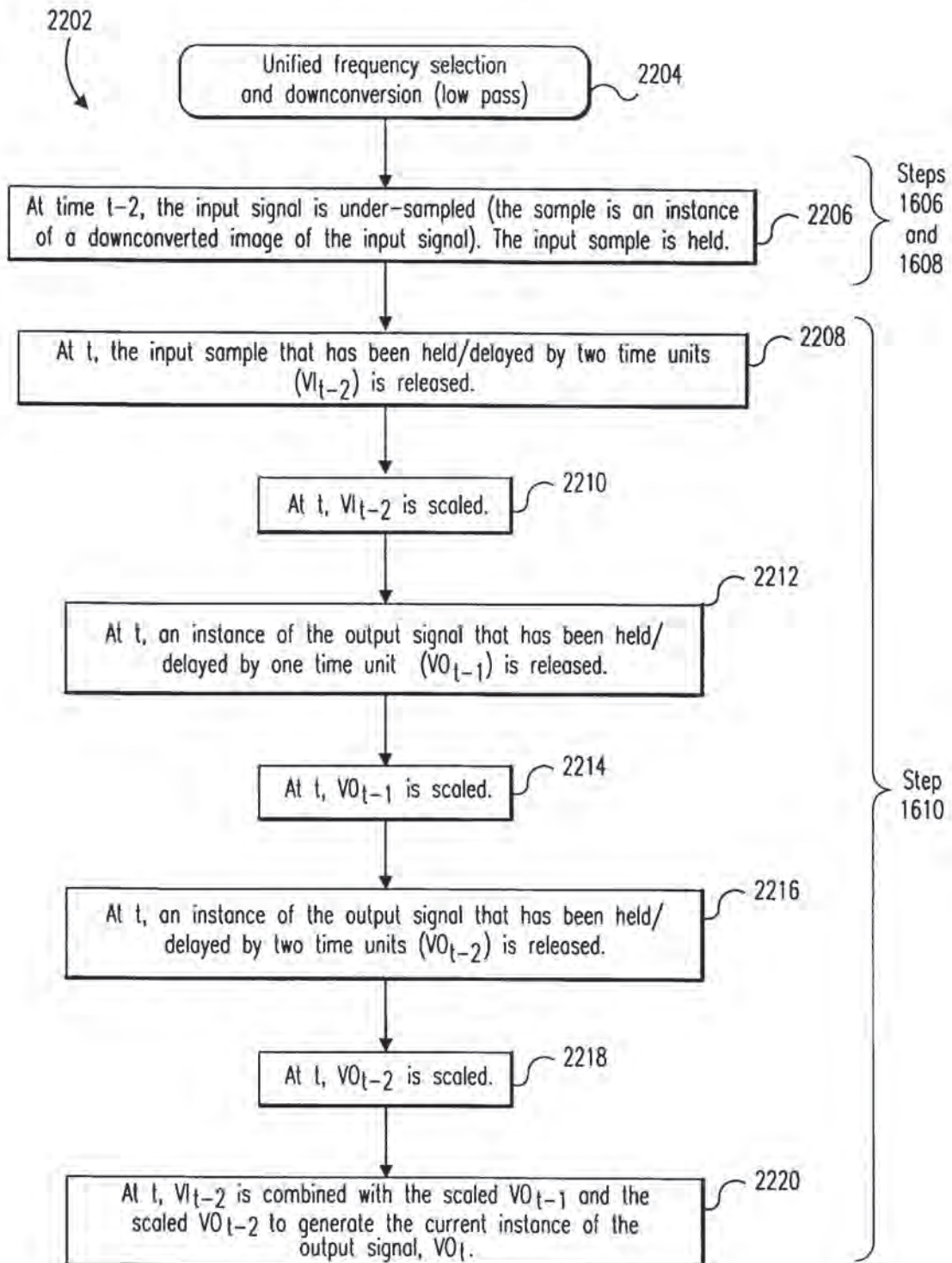


FIG. 22

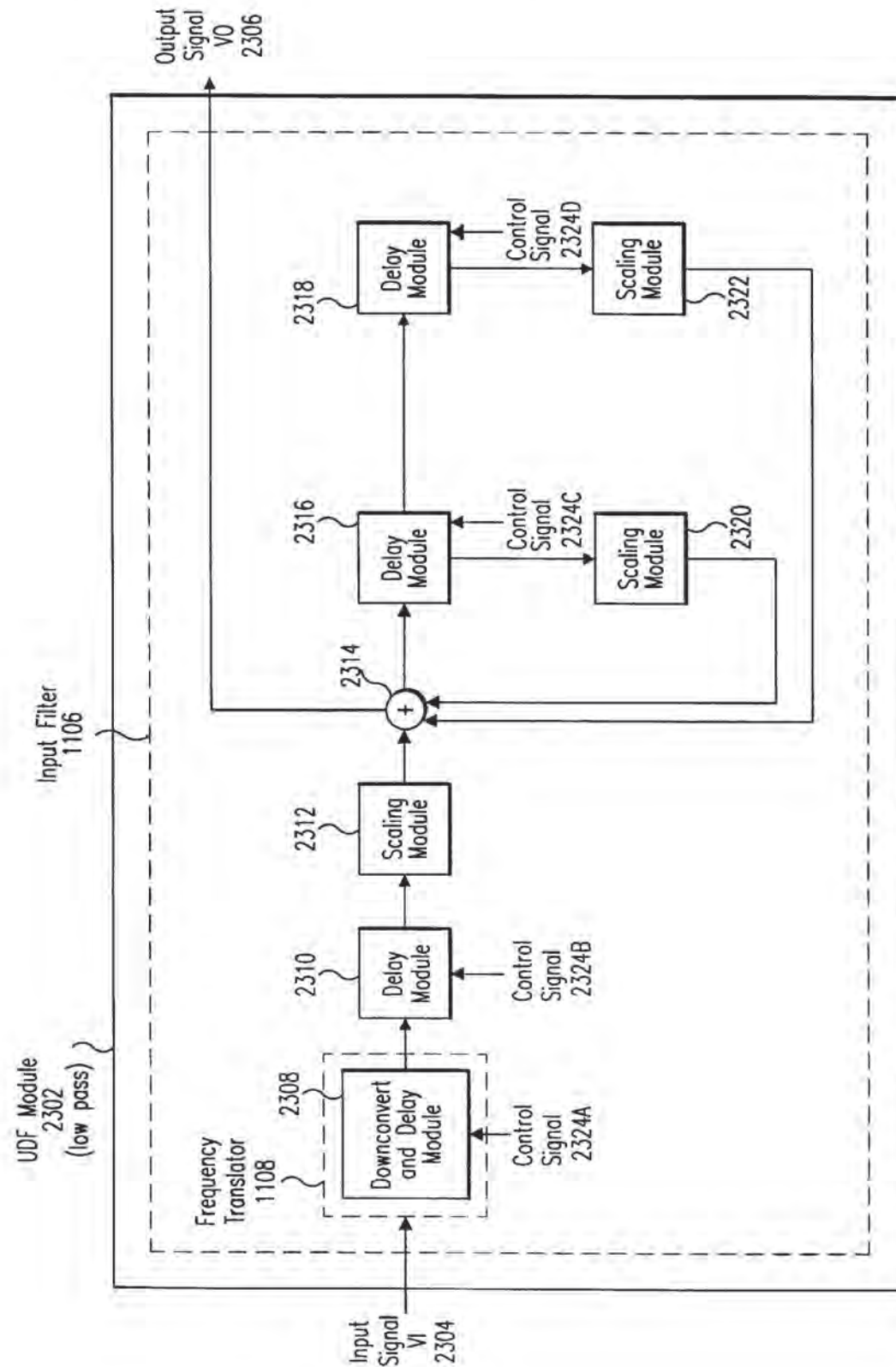


FIG. 23

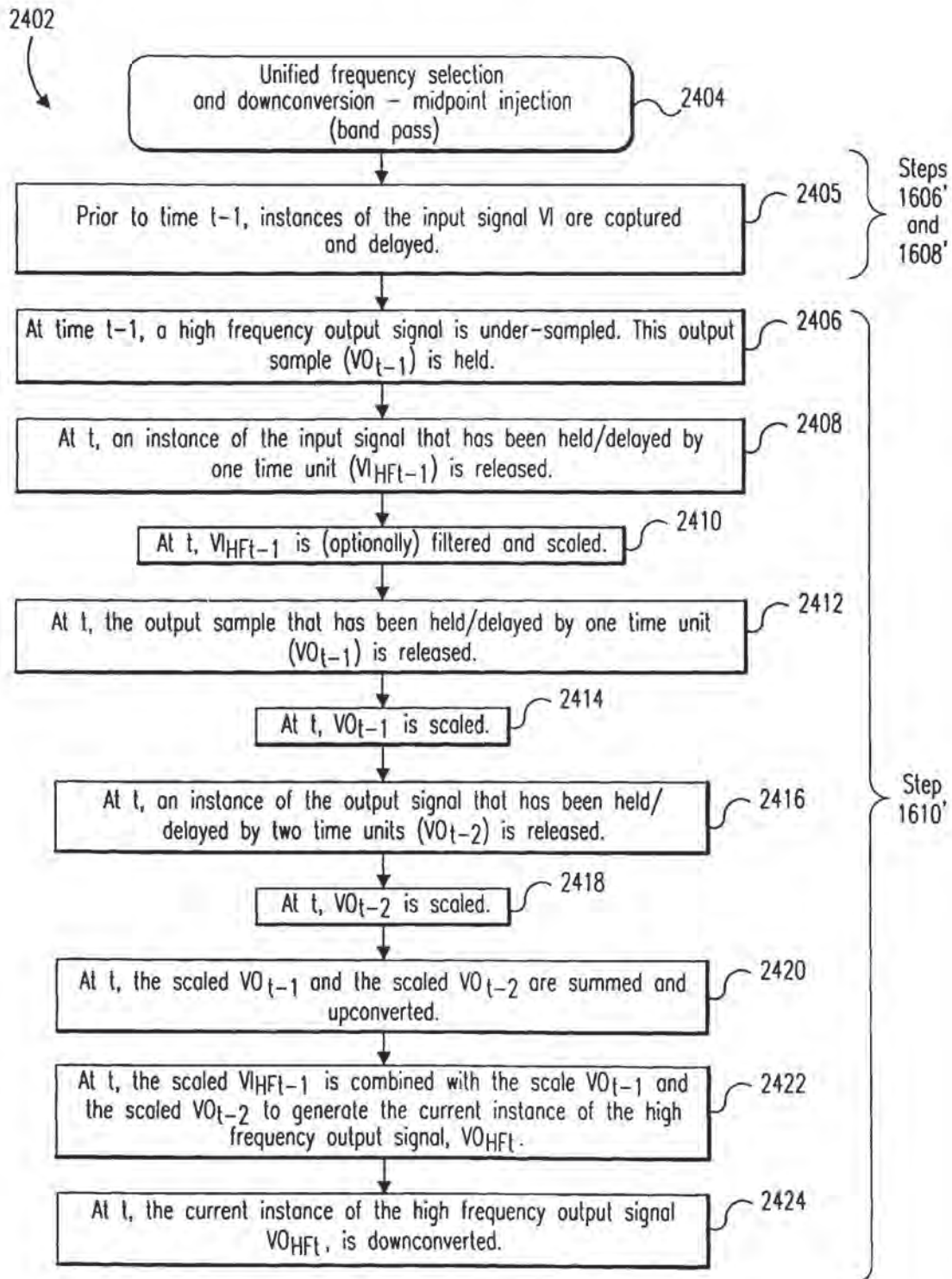


FIG. 24

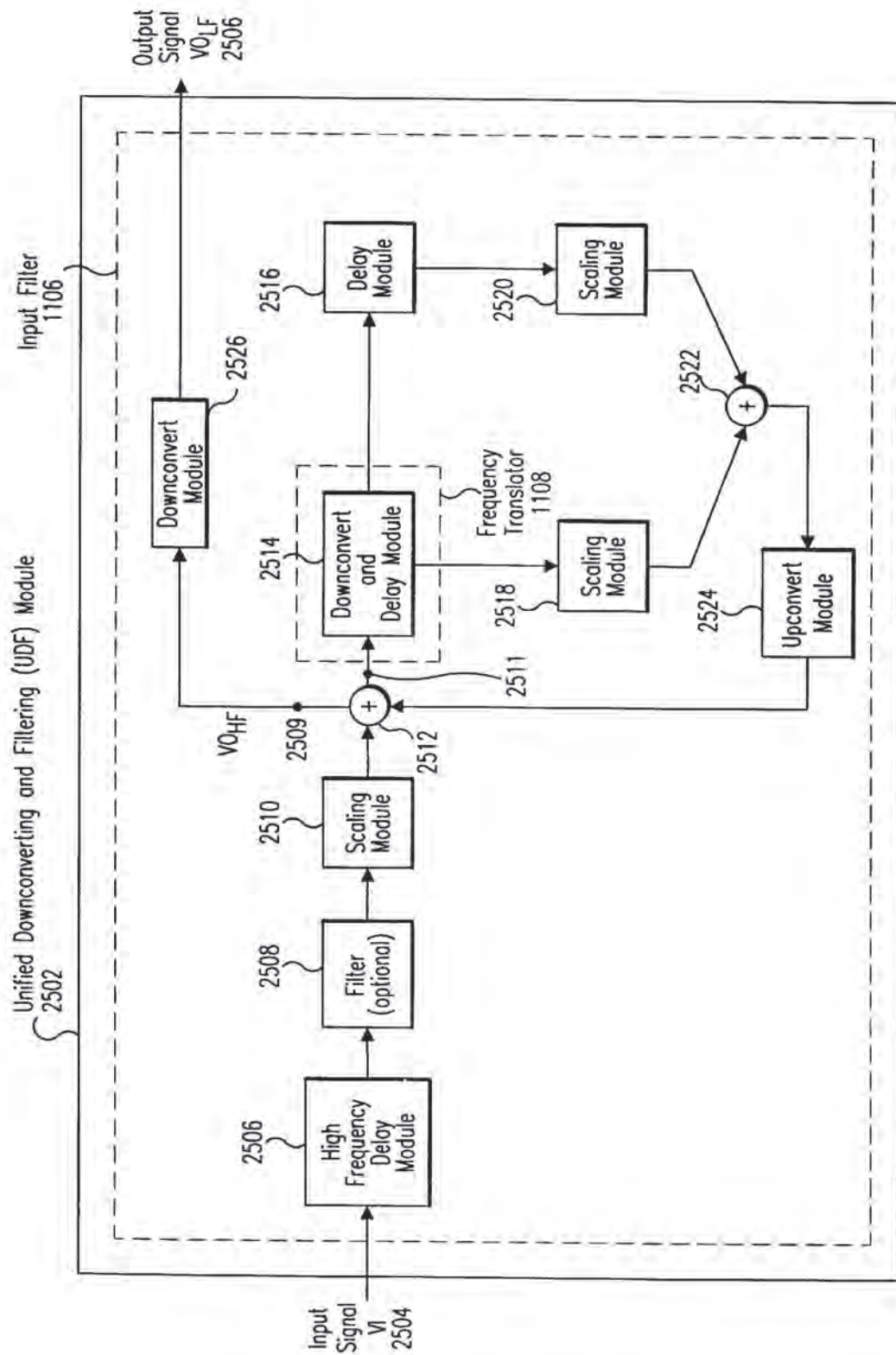


FIG.25

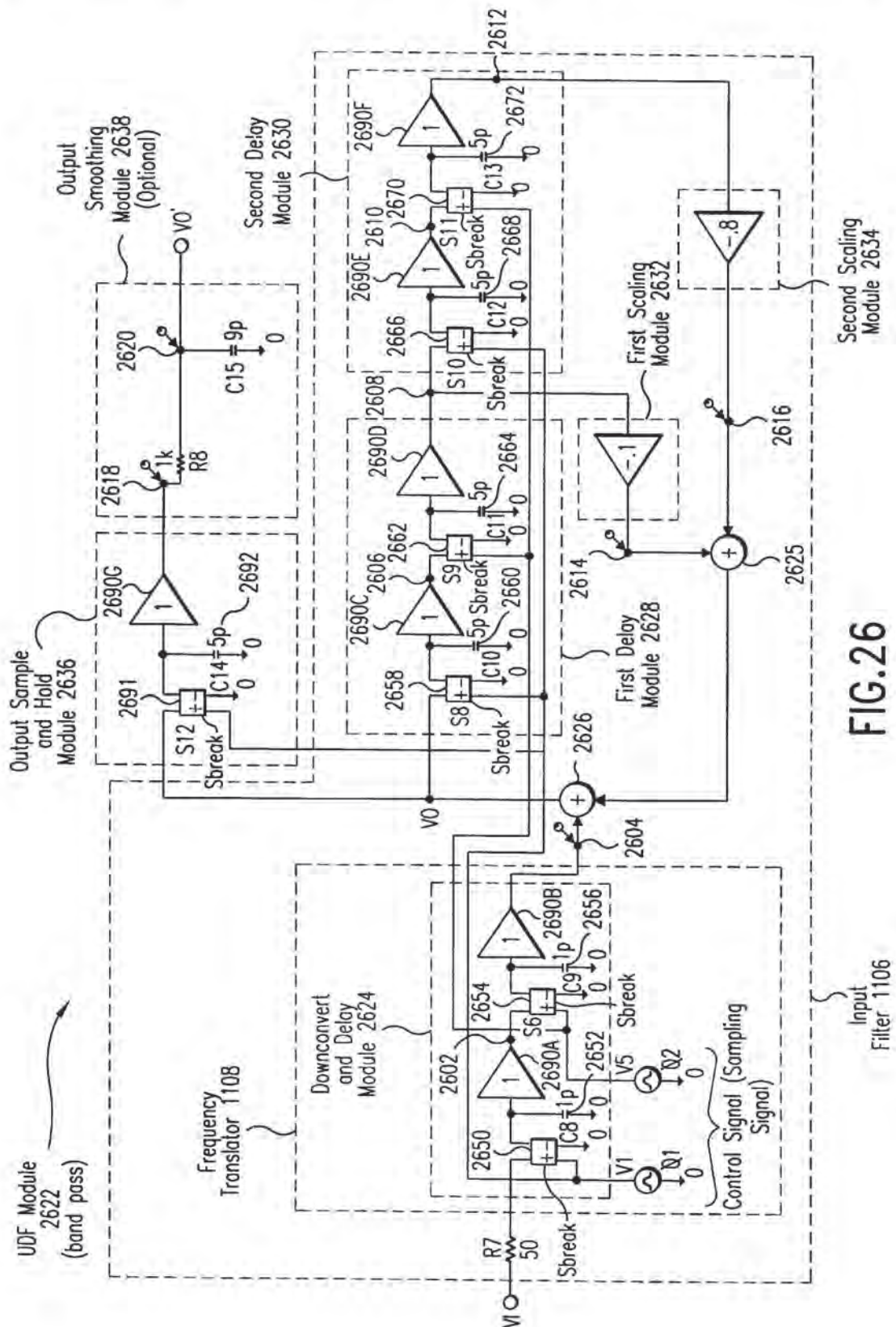


FIG. 26

2702

$$\begin{aligned}t &:= 1..16000 \\ \omega_s &:= 2 \cdot \pi \\ Z_p(t) &:= \cos\left(\frac{t \cdot \omega_s}{16000}\right) + i \cdot \sin\left(\frac{t \cdot \omega_s}{16000}\right) \\ H_z(t) &:= \frac{Z_p(t)}{Z_p(t)^2 + (.1 \cdot Z_p(t)) + .8}\end{aligned}$$

FIG.27A

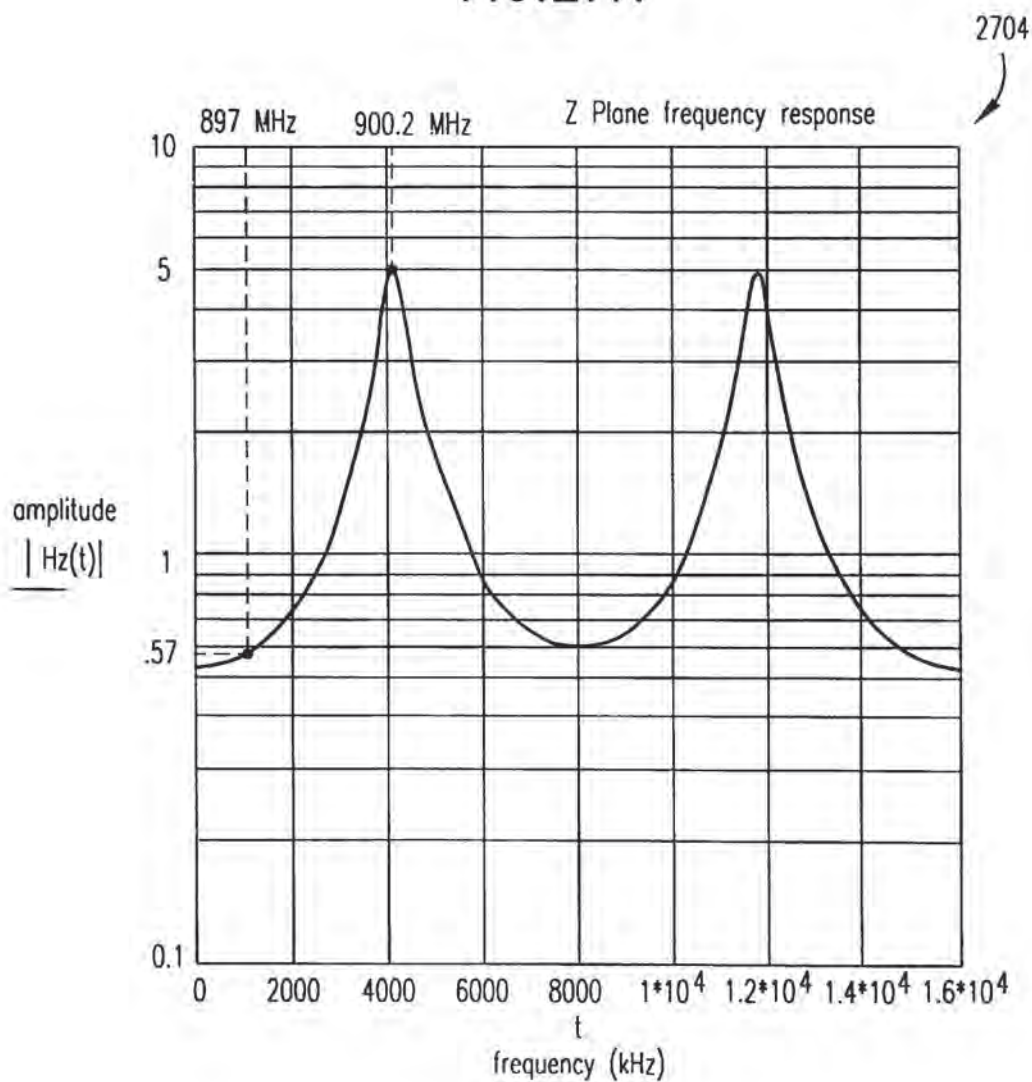
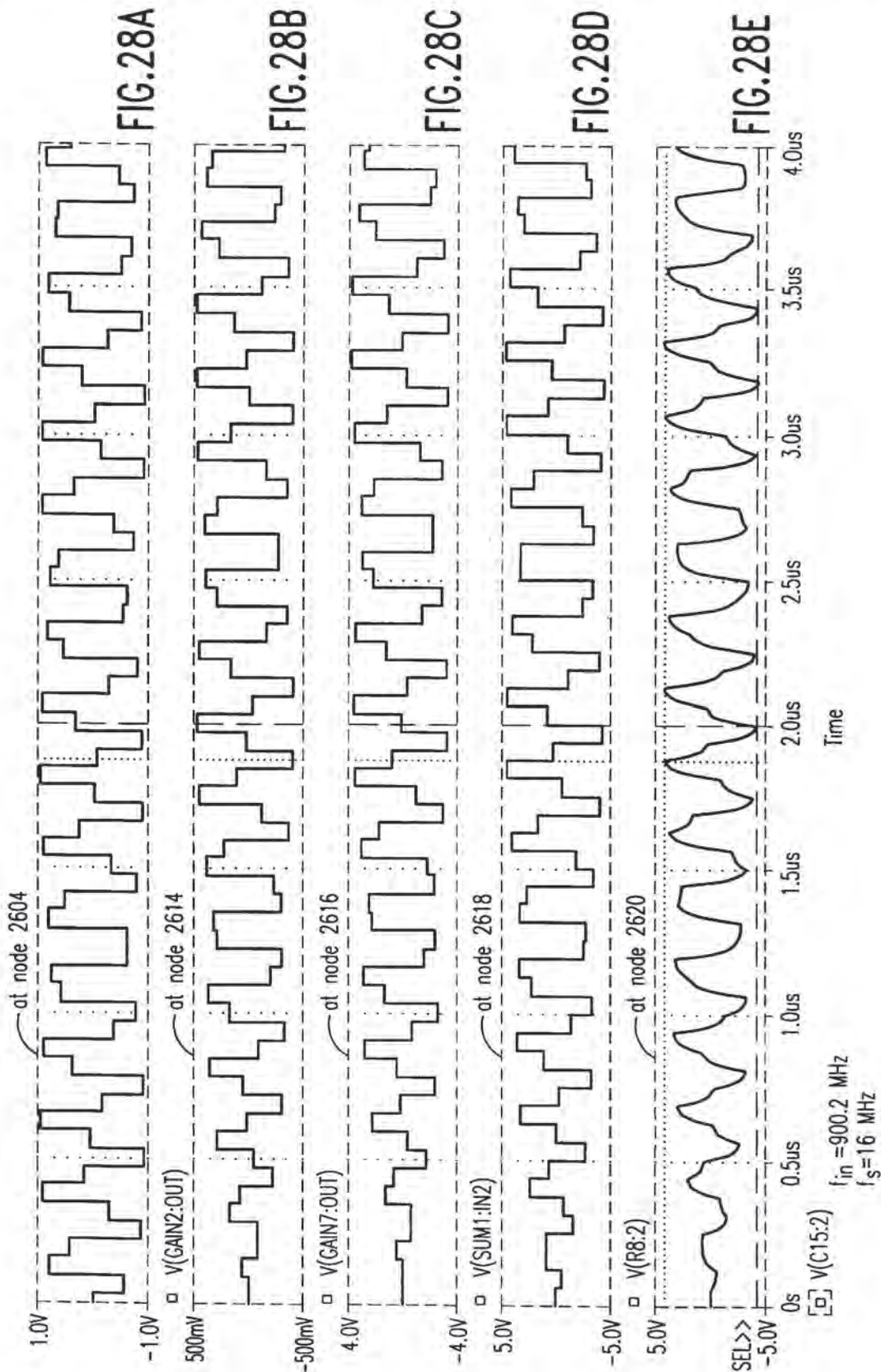
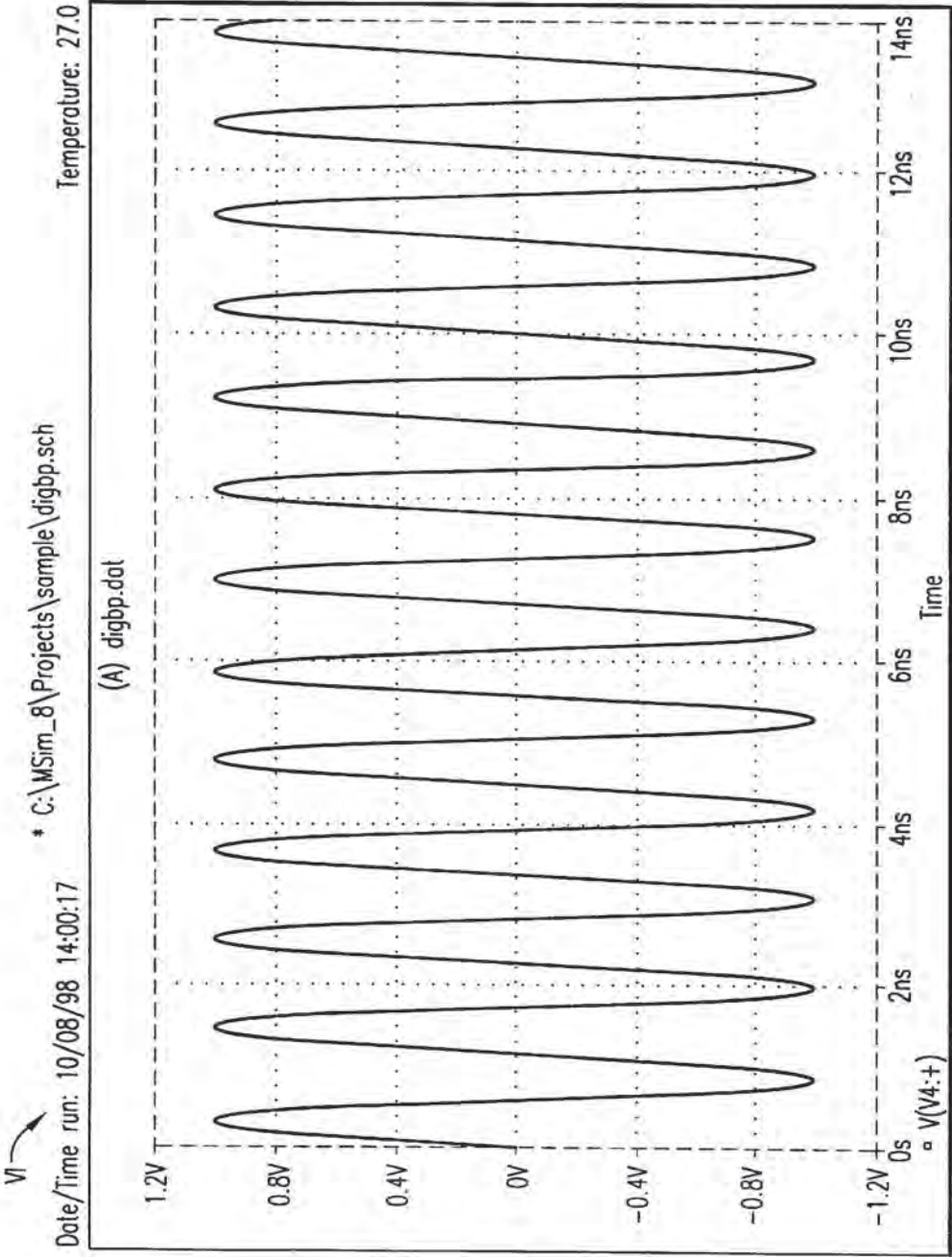


FIG.27B





Date: October 08, 1998

Page 1

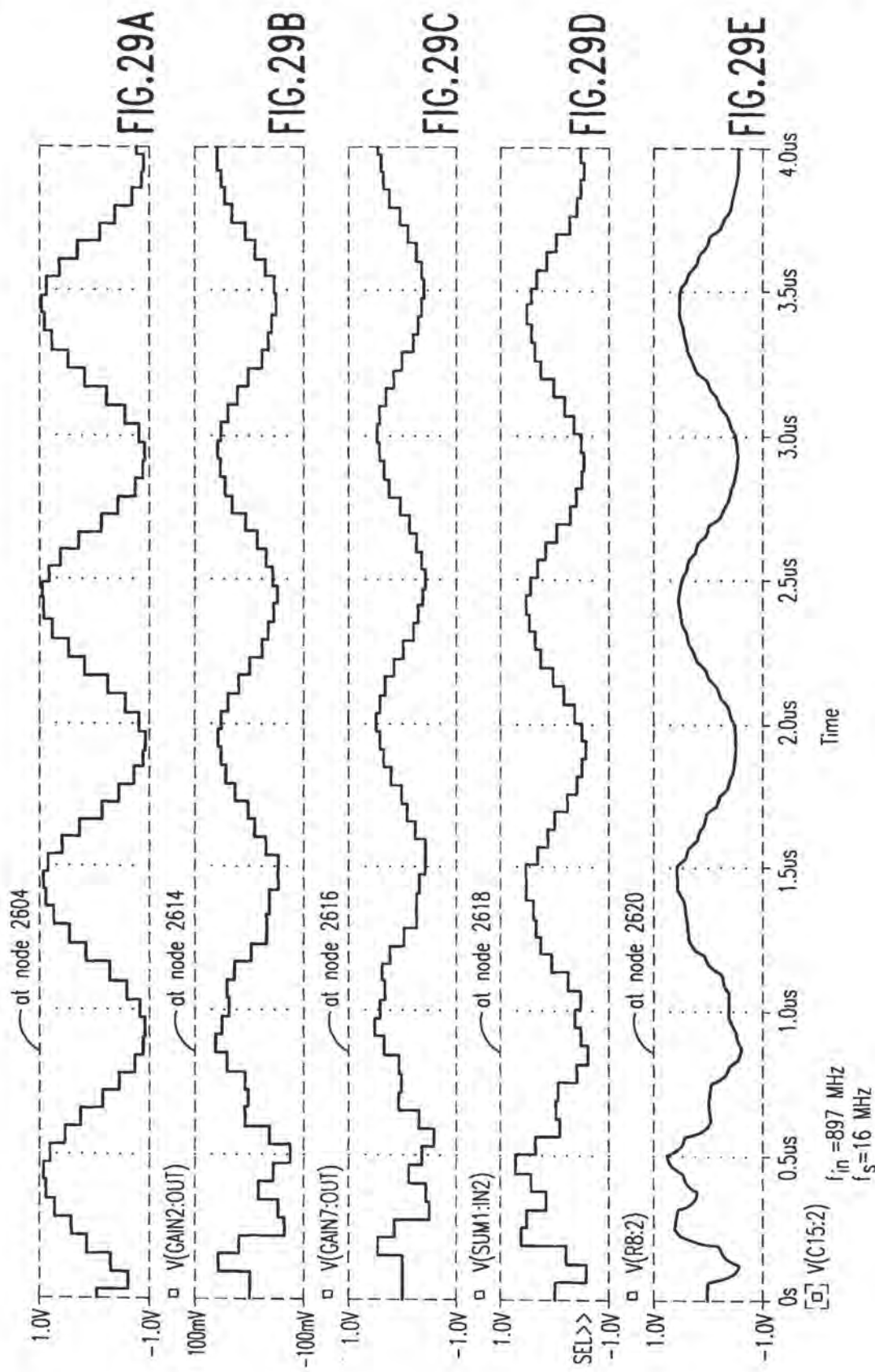
900.2 MHz

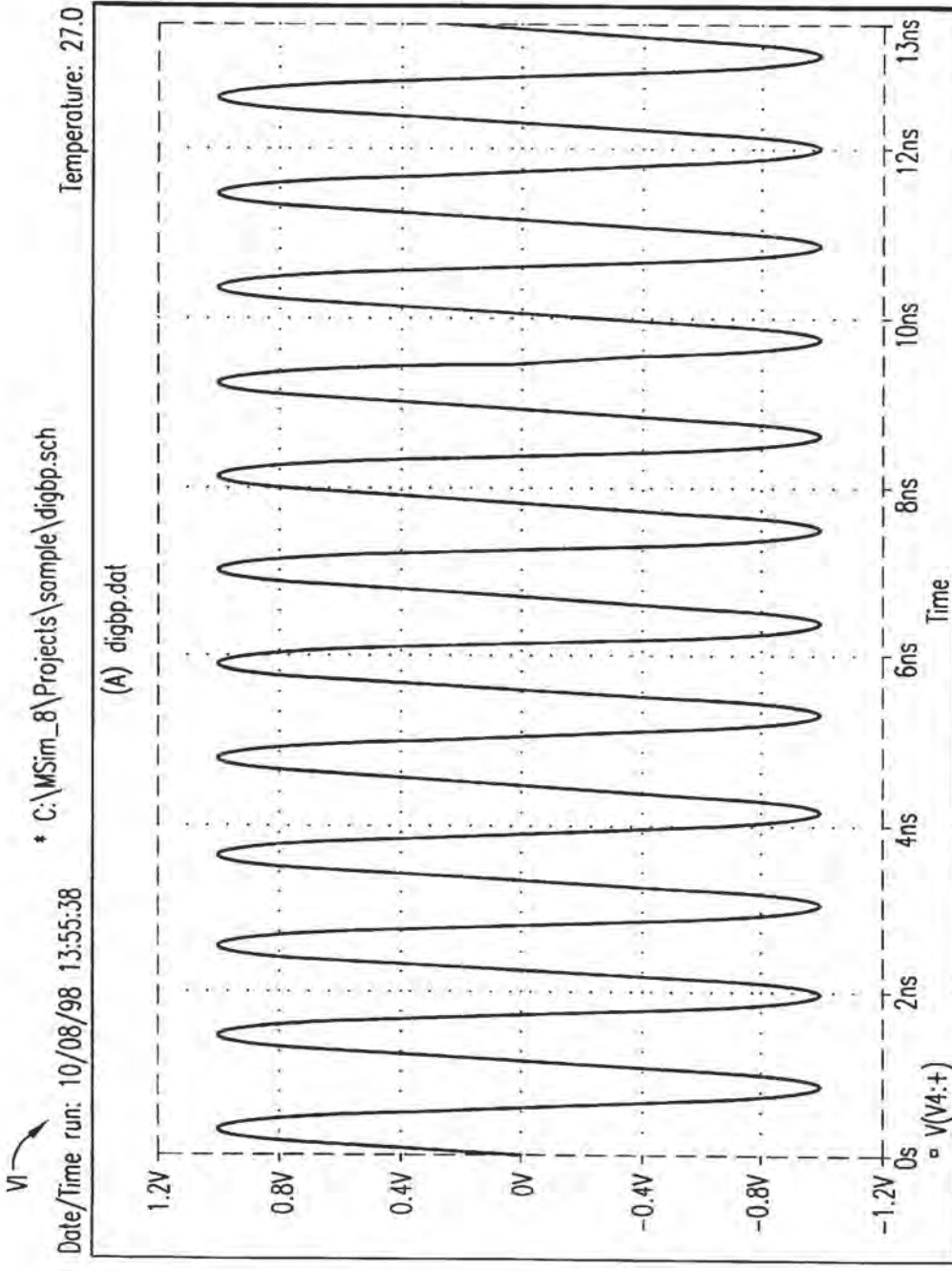
2 volts peak-to-peak

1 volt amplitude

Time: 14:01:11

FIG. 28F





Date: October 08, 1998

Page 1

Time: 13:58:34

897 MHz

2 volts peak-to-peak

1 volt amplitude

FIG. 29F

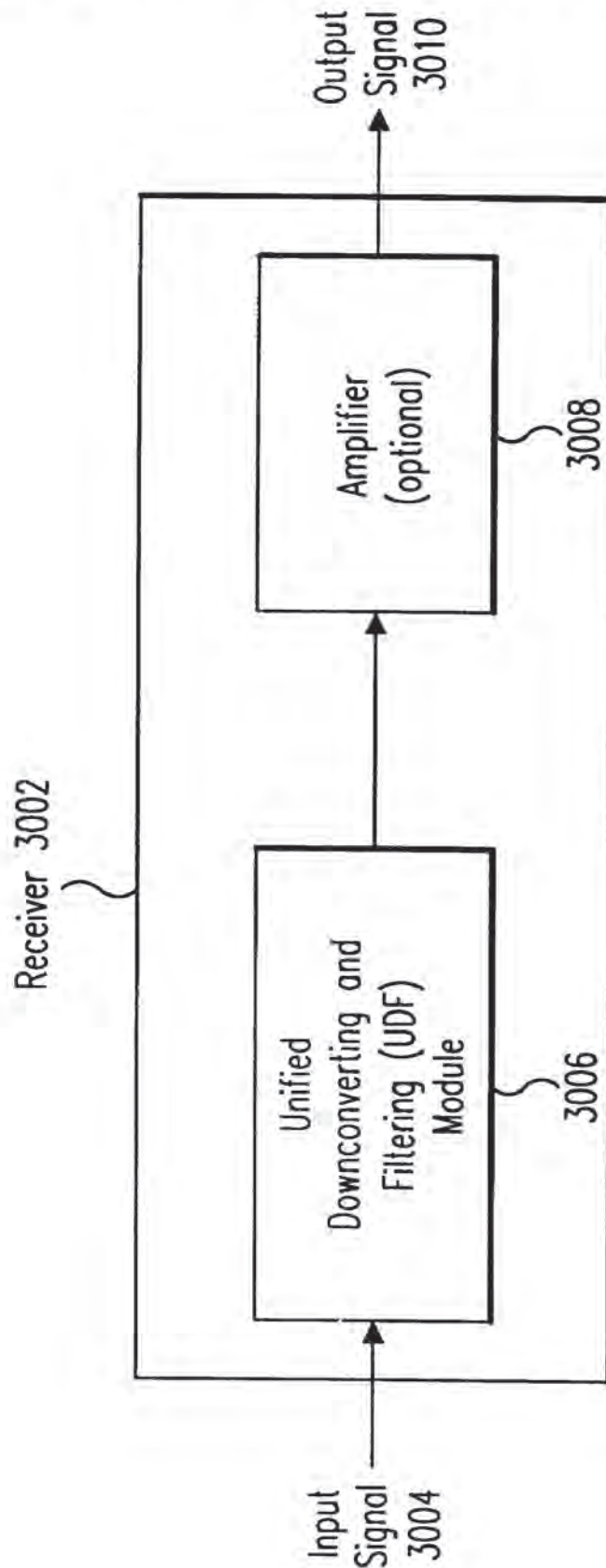


FIG.30

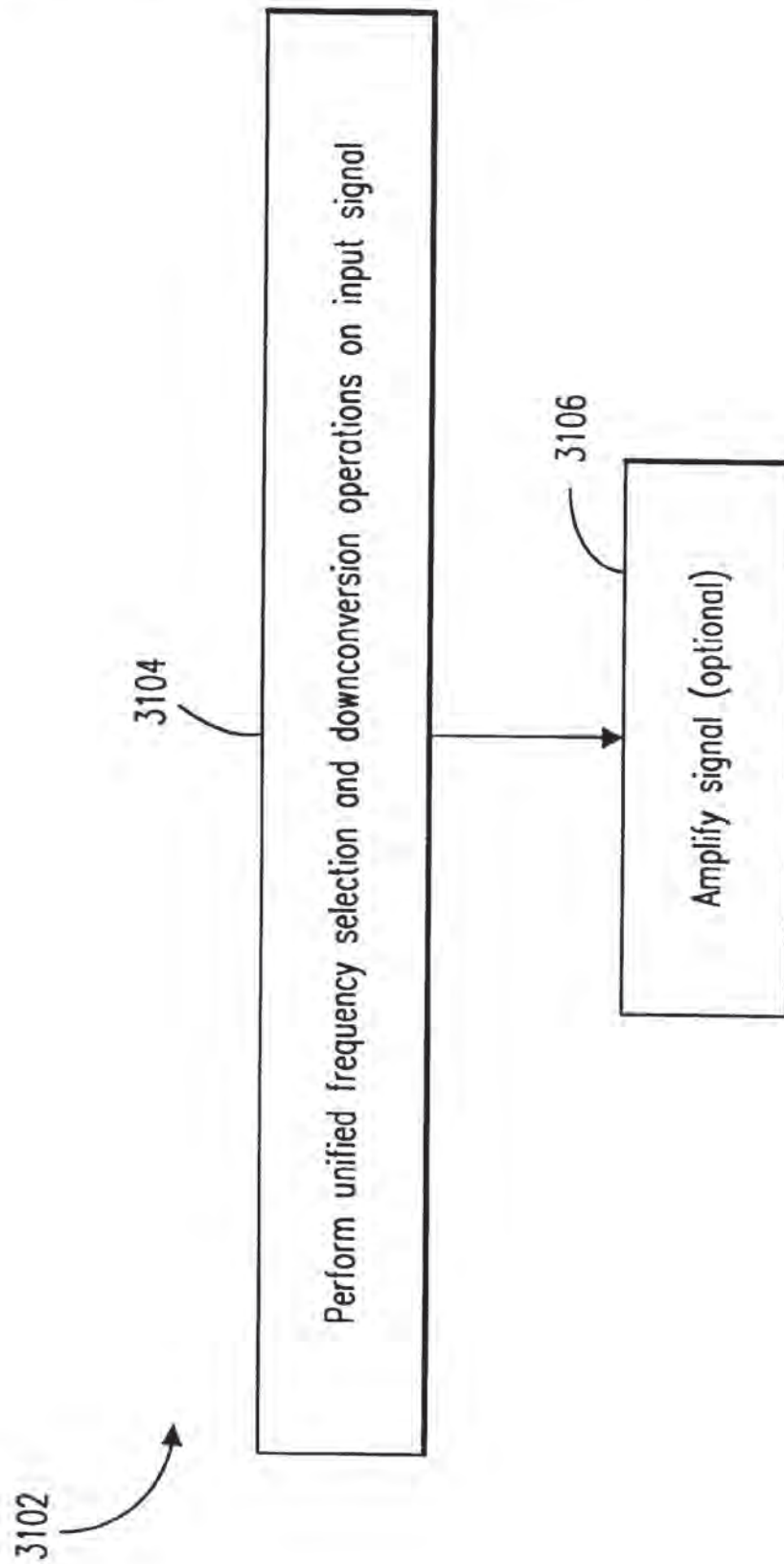


FIG. 31

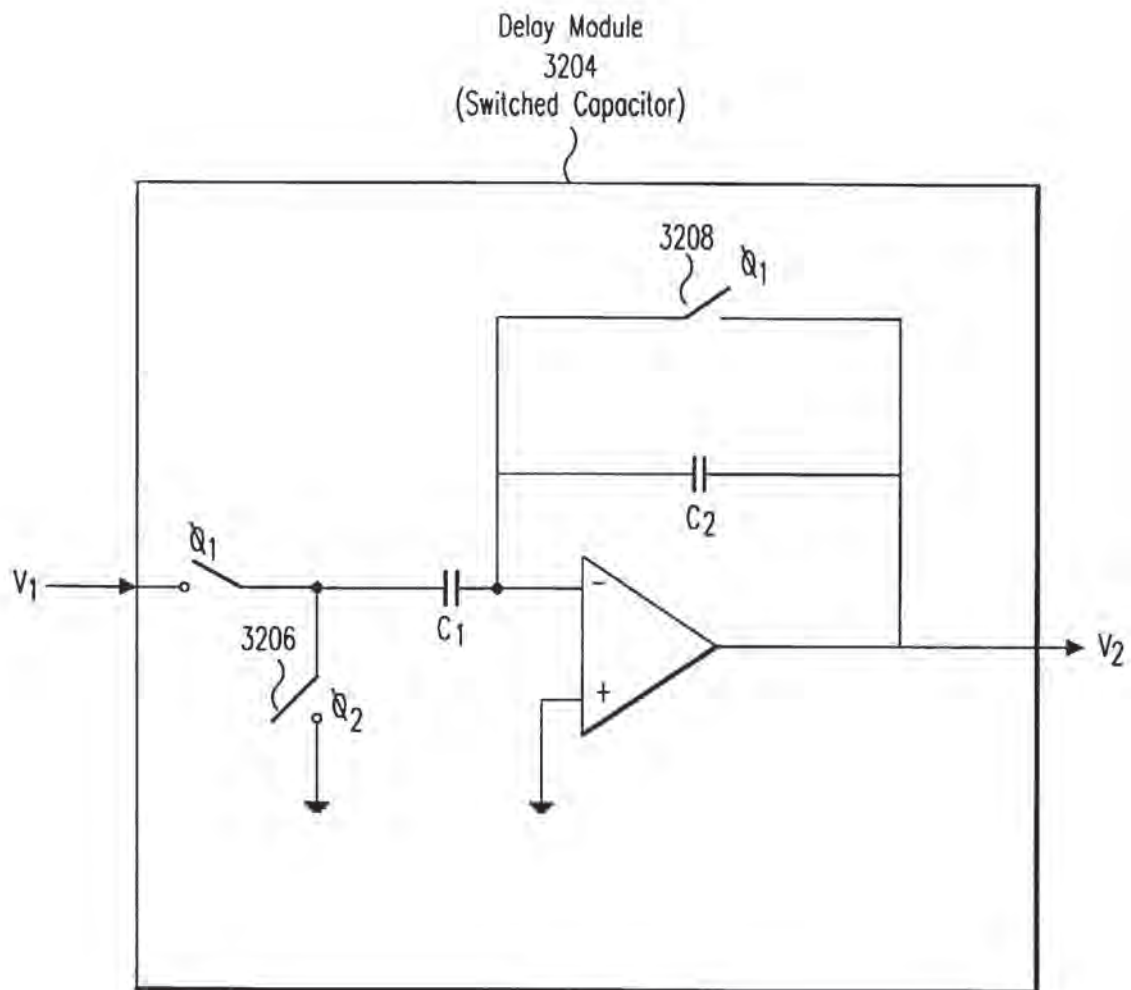
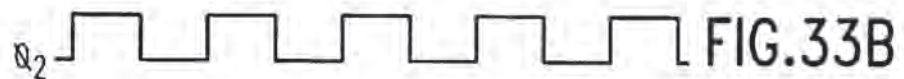
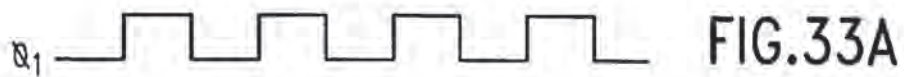


FIG.32

$$V_2 = \frac{C_1}{C_2} \cdot V_1$$



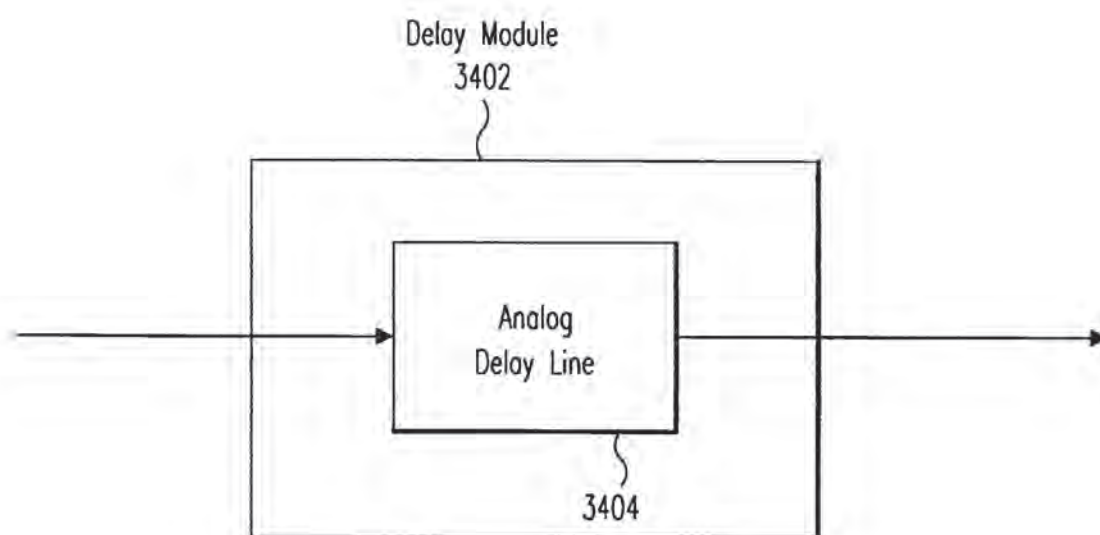


FIG.34

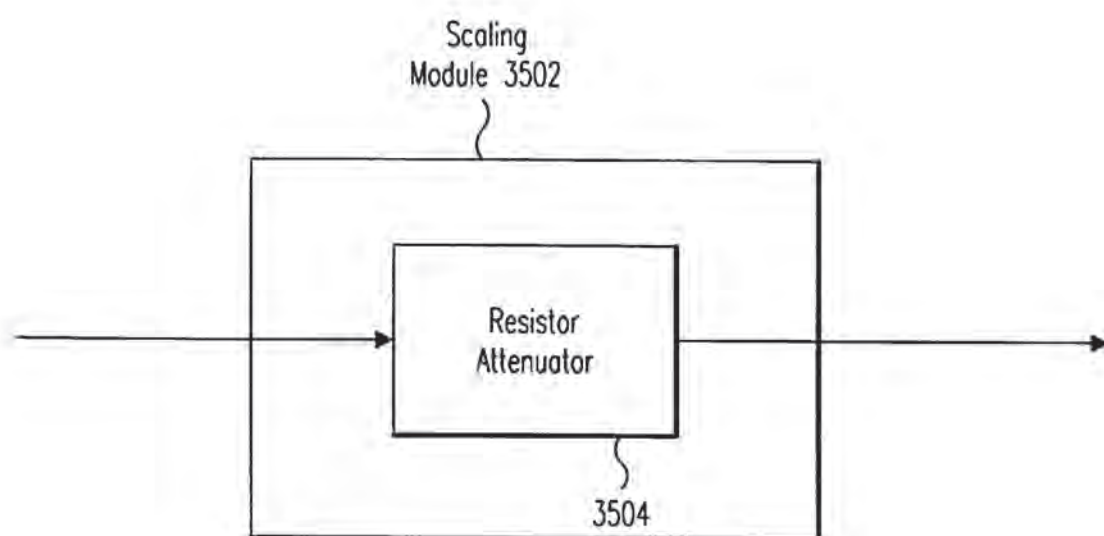


FIG.35

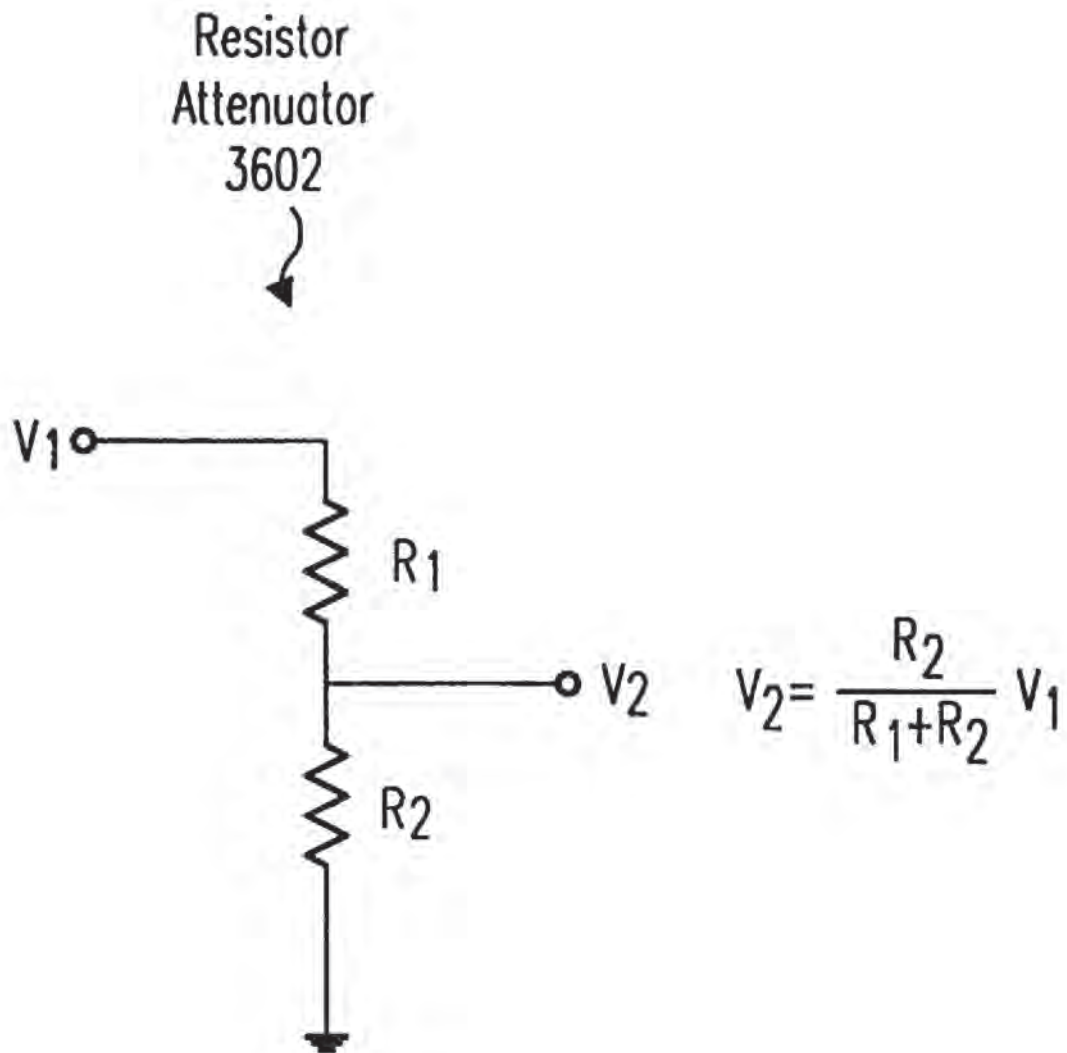


FIG.36

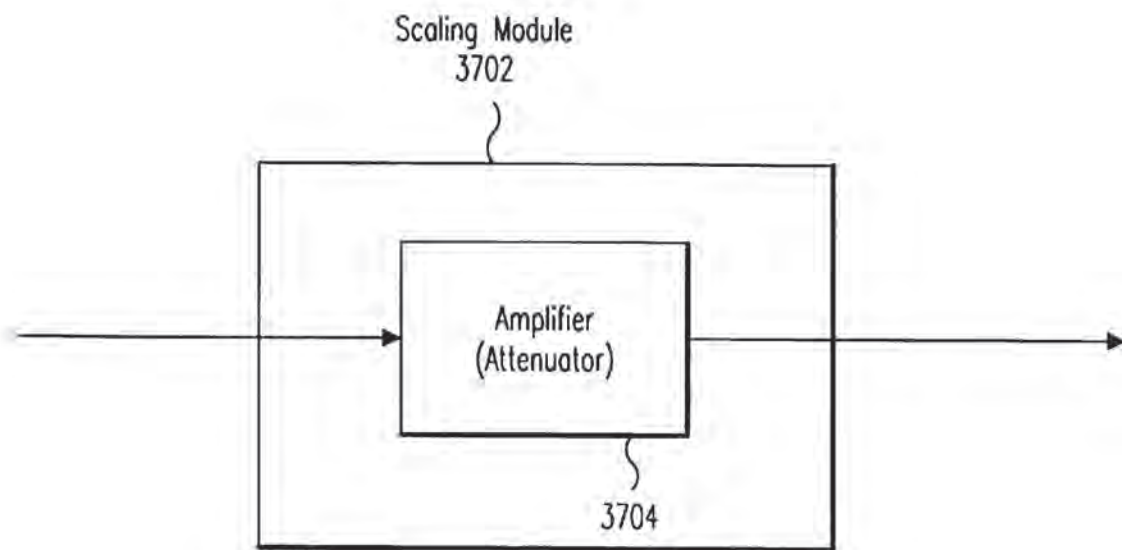


FIG.37

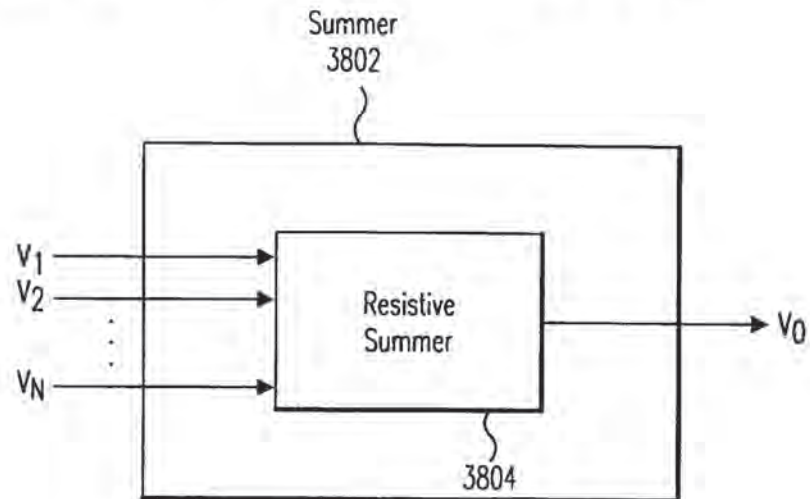


FIG.38

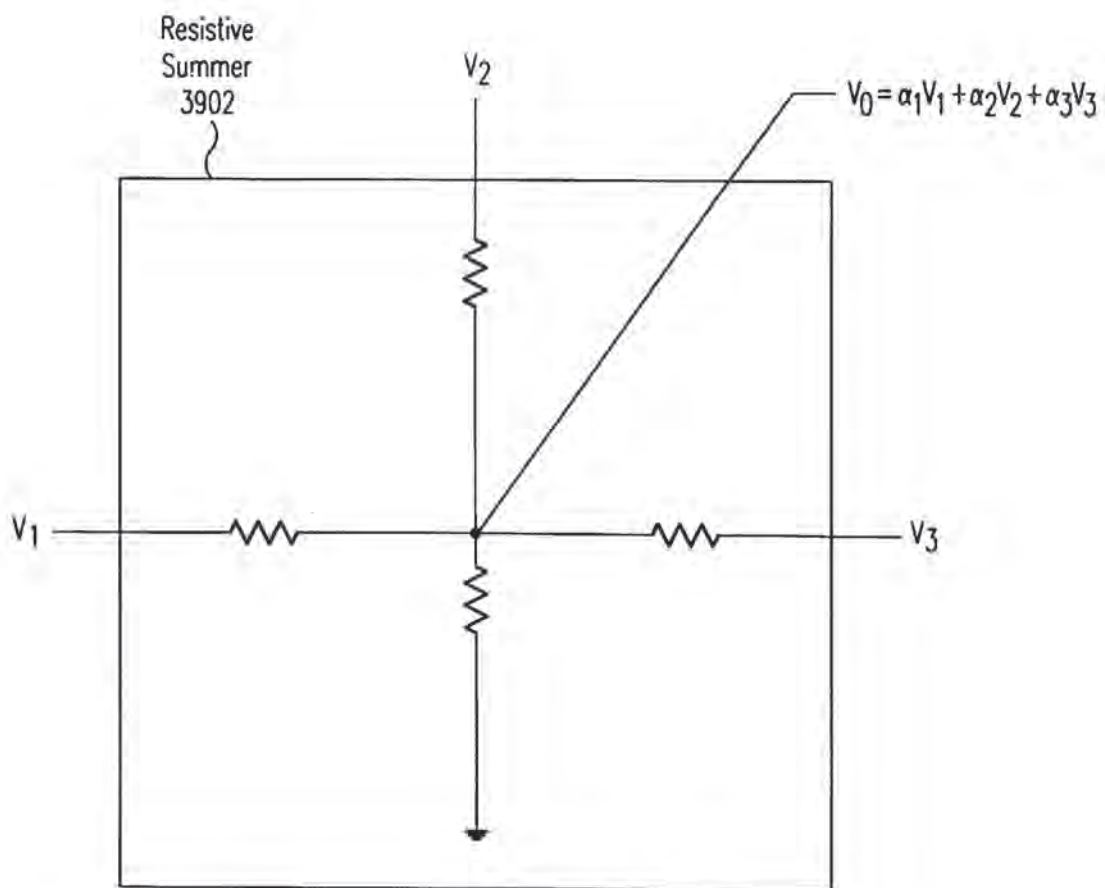


FIG.39

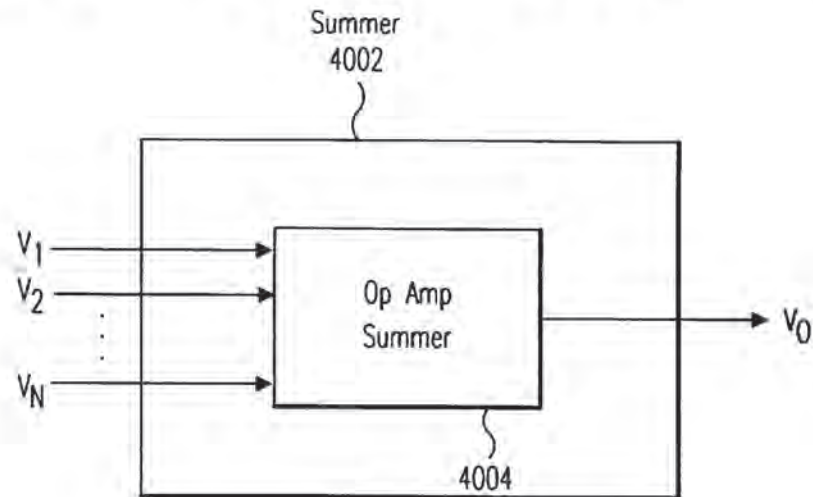


FIG.40

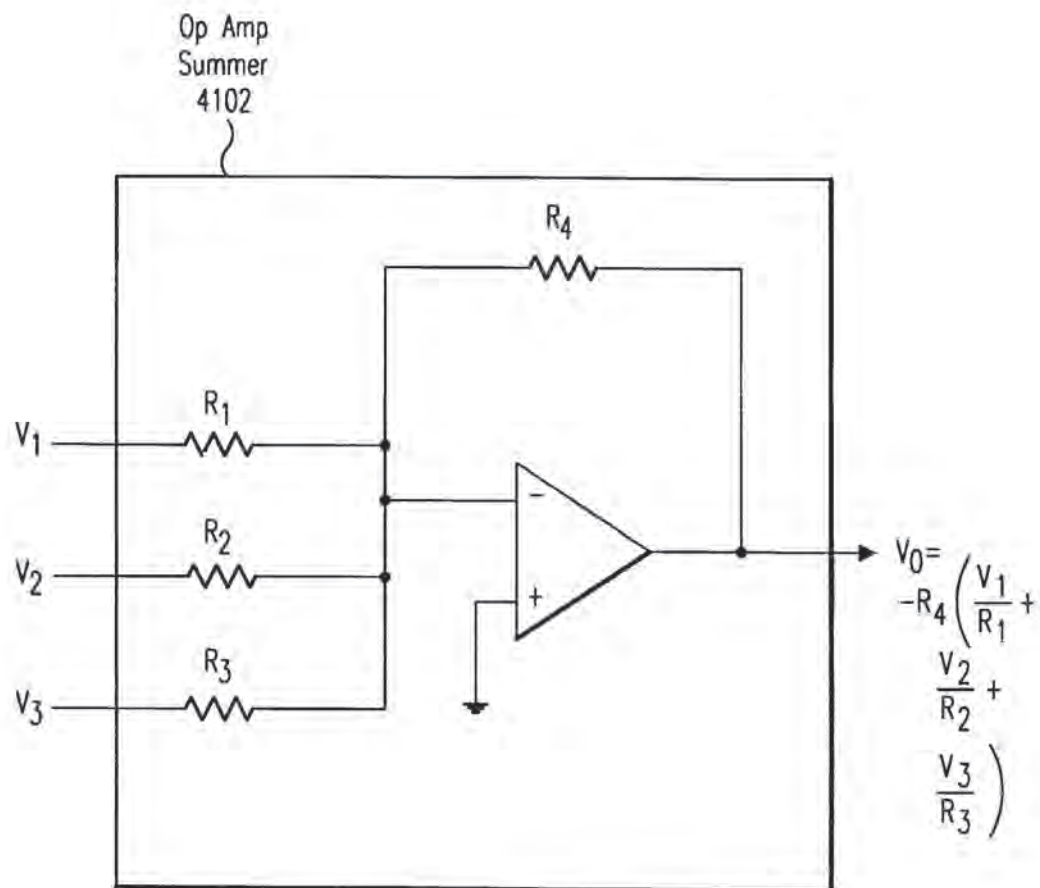


FIG.41

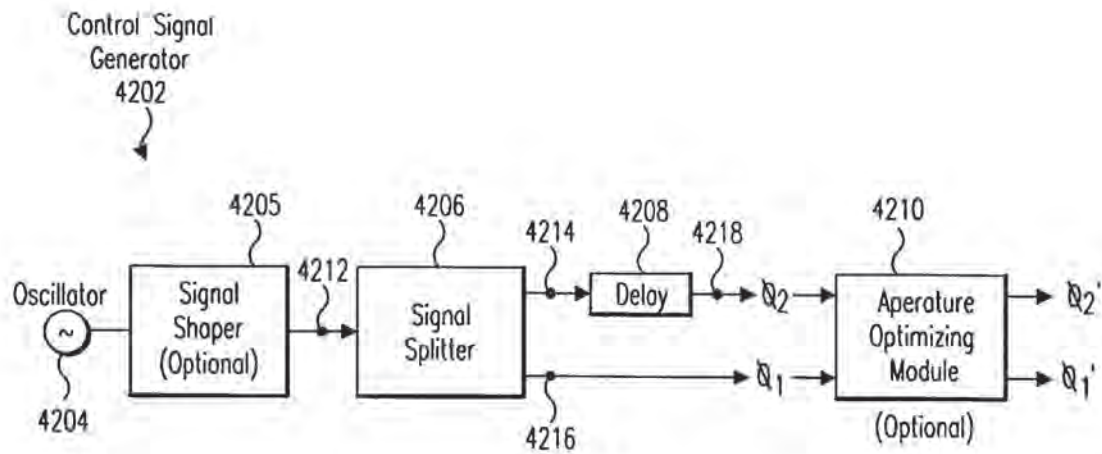


FIG. 42

At node
4212



FIG. 43A

At node
4216



FIG. 43B

At node
4214



FIG. 43C

At node
4218



FIG. 43D

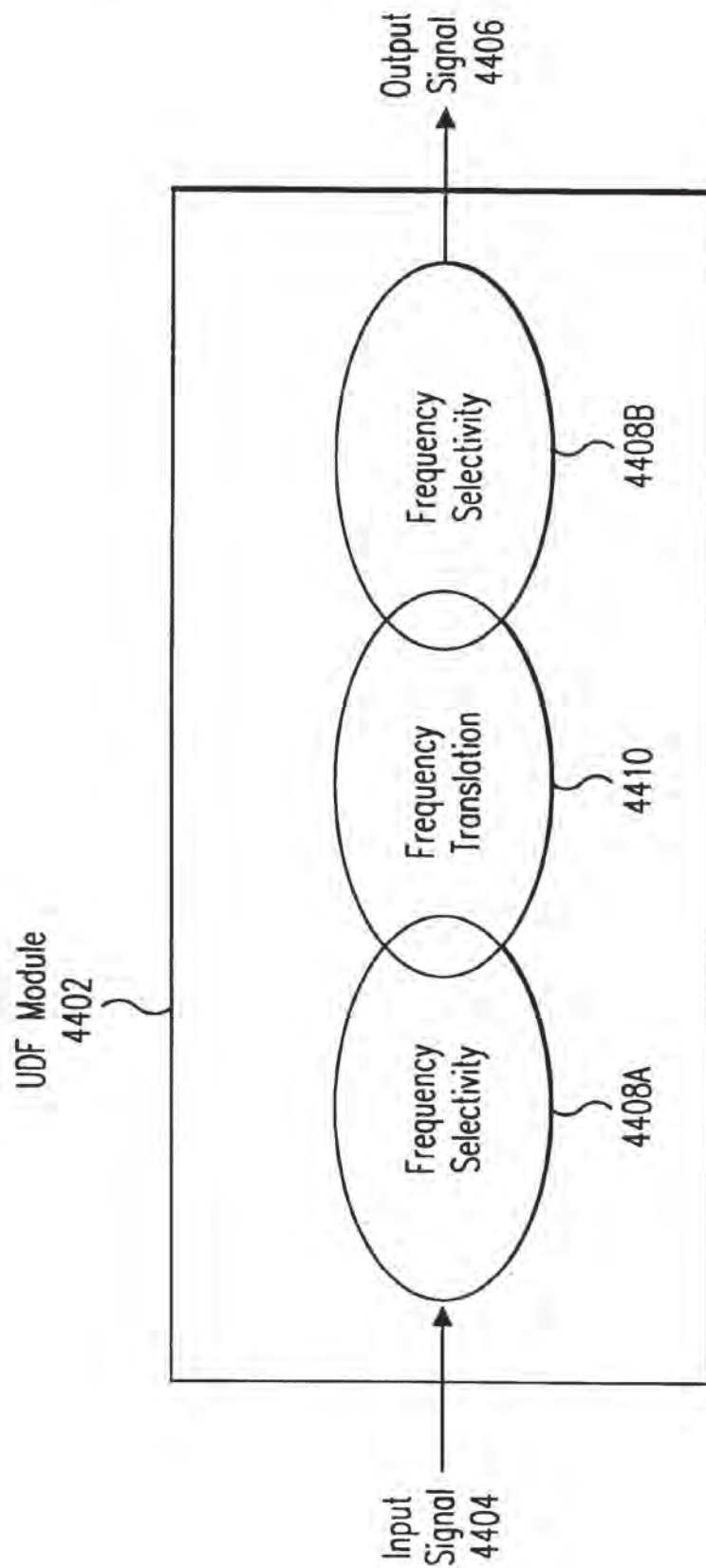


FIG. 44

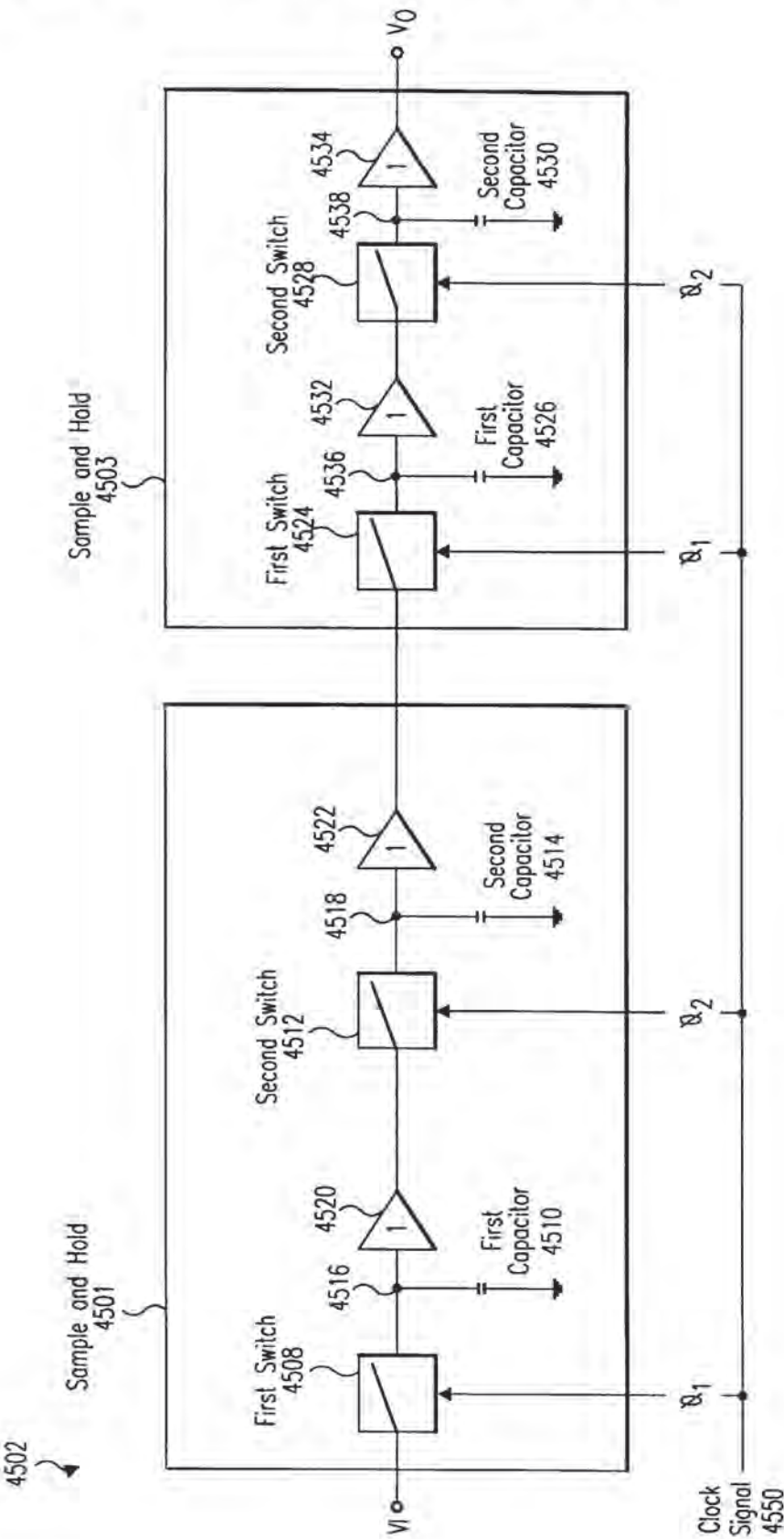


FIG. 45

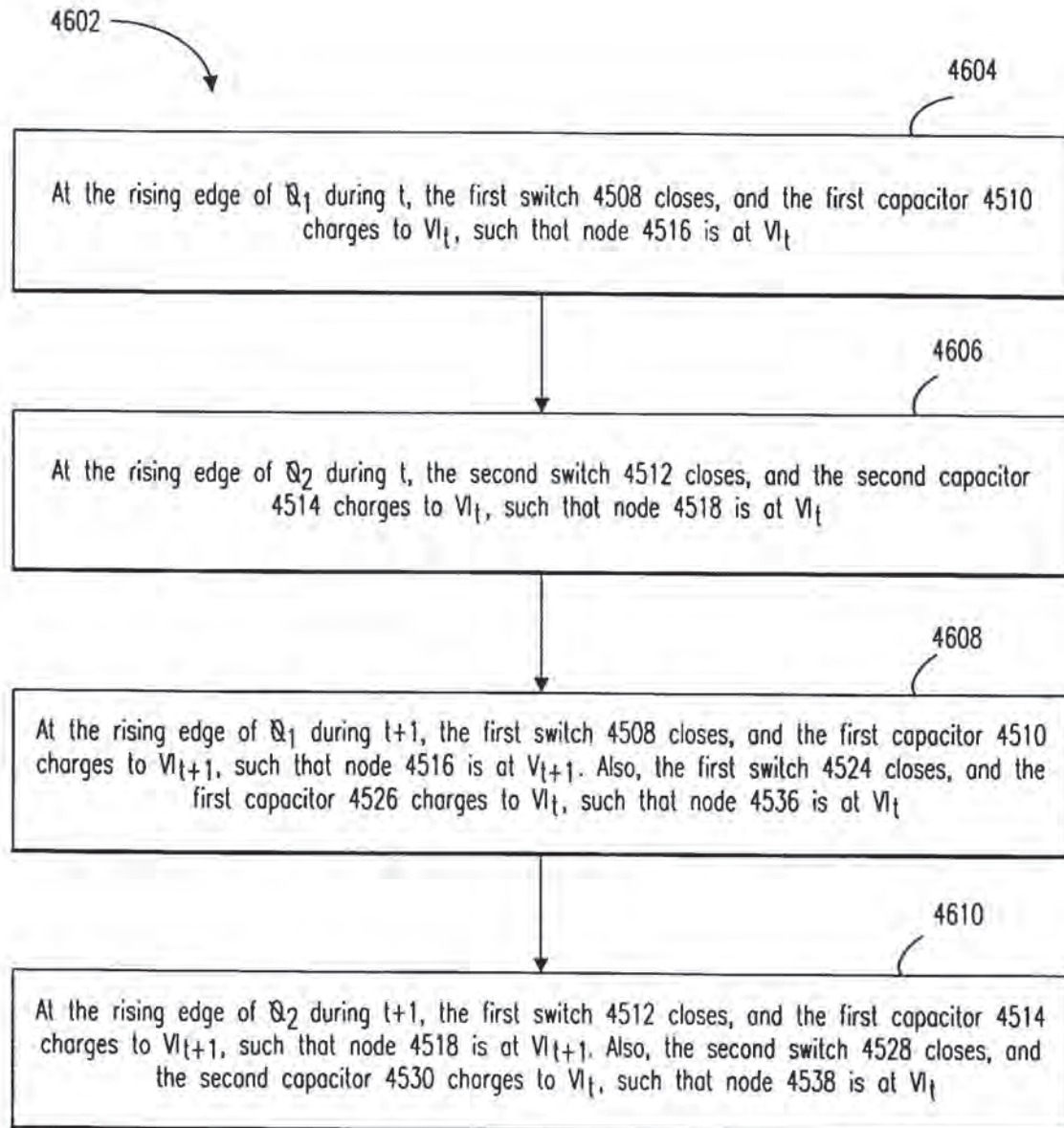


FIG. 46

4702



Time Node	^t (rising edge of Φ_1)	^t (rising edge of Φ_2)	^{t+1} (rising edge of Φ_1)	^{t+1} (rising edge of Φ_2)
4516	V_{I_t} <u>4704</u>	V_{I_t} <u>4706</u>	$V_{I_{t+1}}$ <u>4710</u>	$V_{I_{t+1}}$ <u>4716</u>
4518	—	V_{I_t} <u>4708</u>	V_{I_t} <u>4712</u>	$V_{I_{t+1}}$ <u>4718</u>
4536	— <u>4705</u>	—	V_{I_t} <u>4714</u>	V_{I_t} <u>4720</u>
4538	—	— <u>4709</u>	—	V_{I_t} <u>4722</u>

FIG. 47

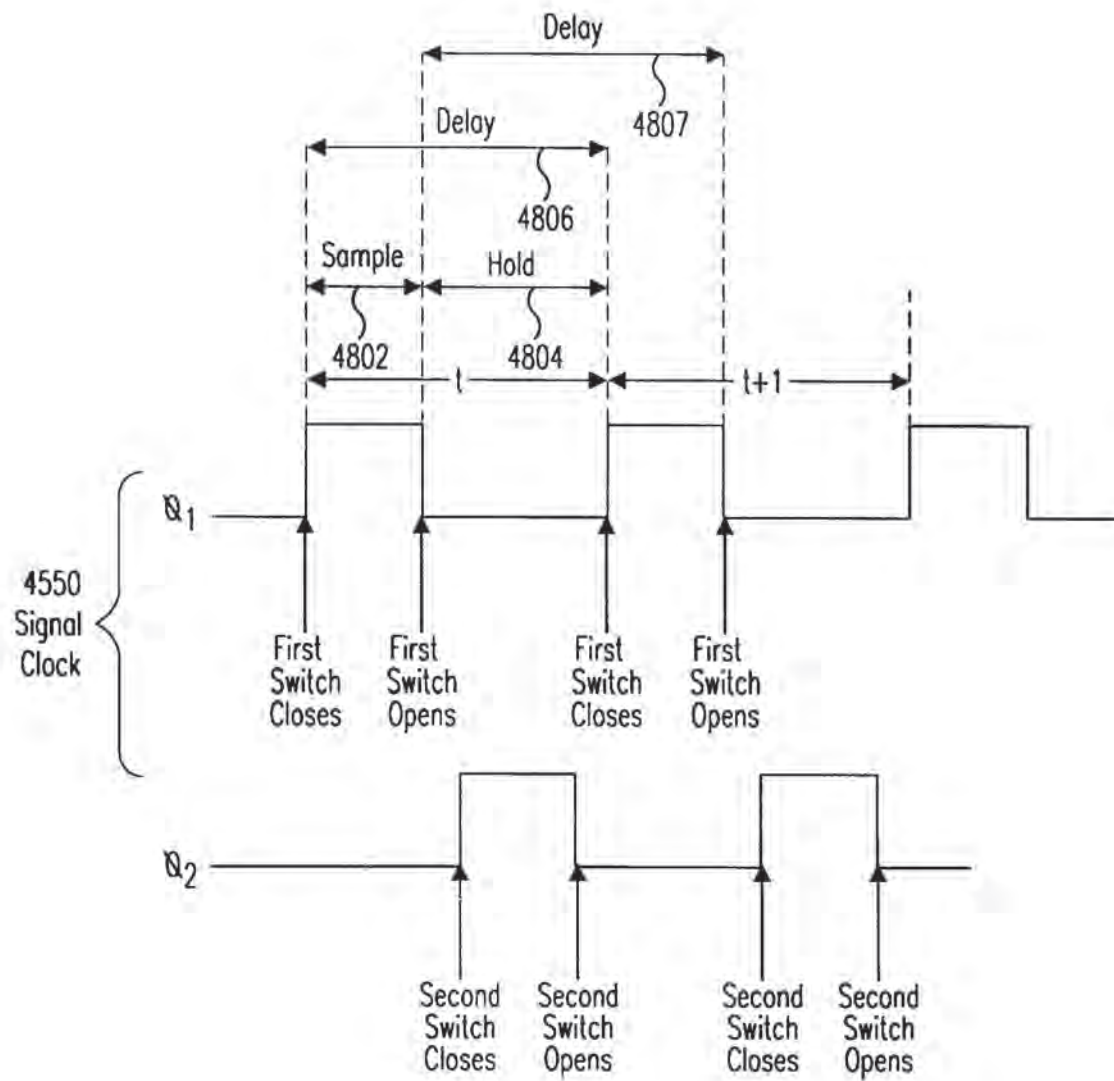


FIG. 48

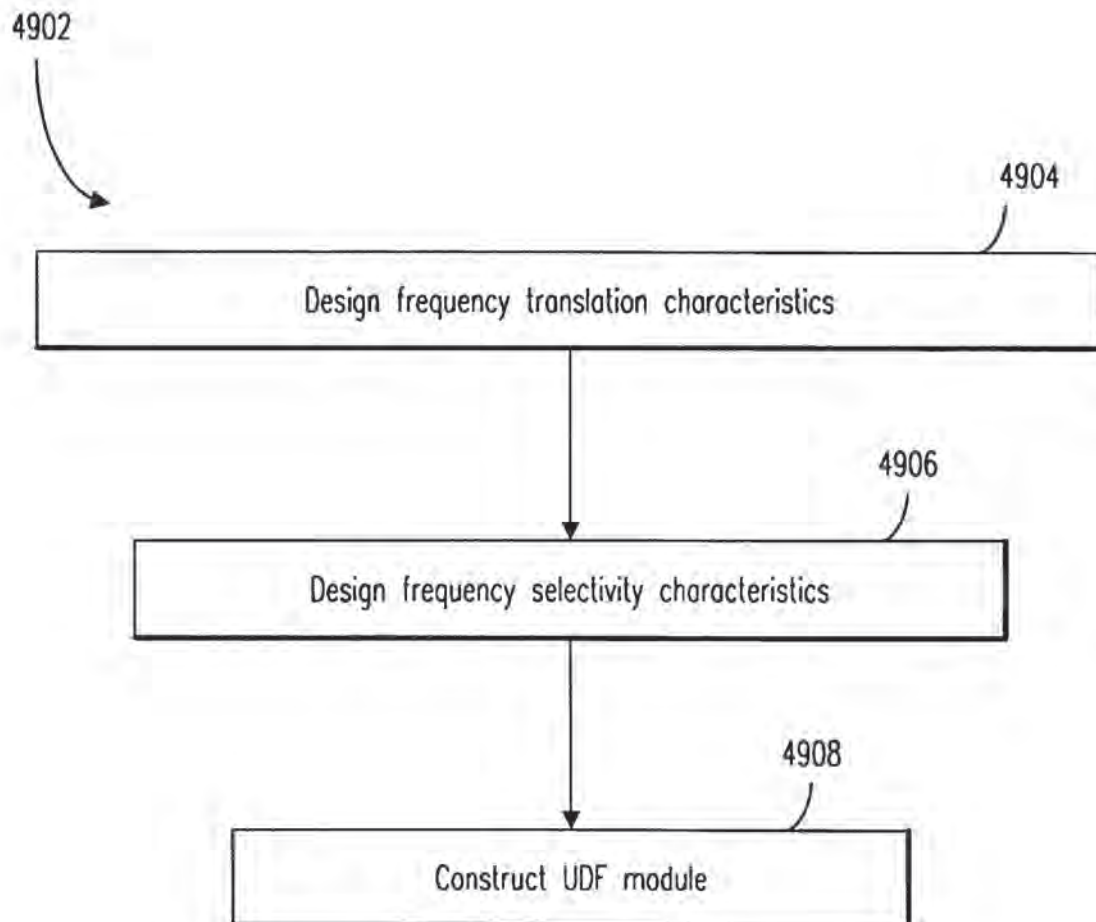


FIG. 49

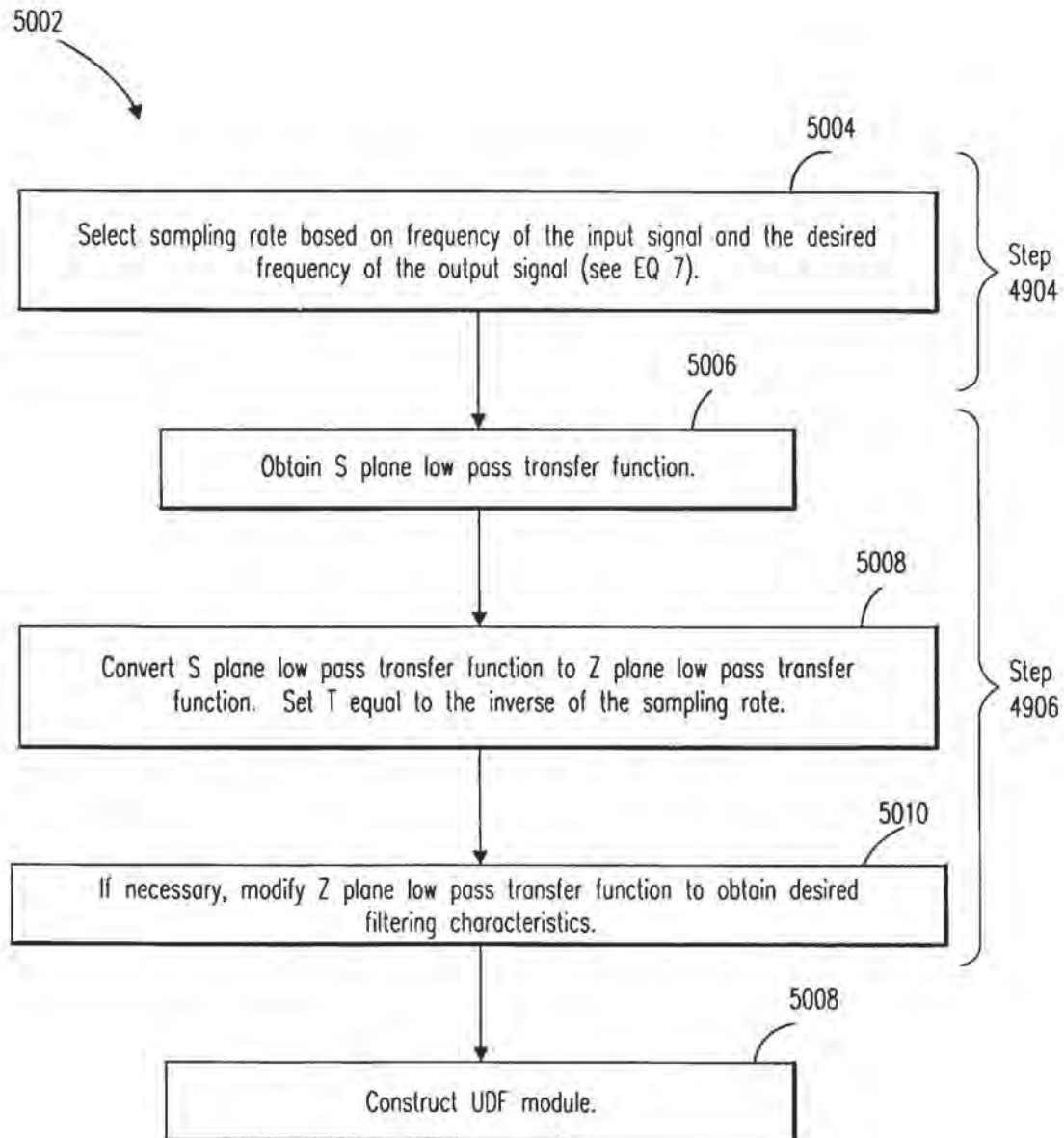


FIG. 50

5102

Filter Type	Transformation	Associated Design Formulas
Lowpass	$z^{-1} = \frac{Z^{-1} - \alpha}{1 - \alpha Z^{-1}}$	$\alpha = \frac{\sin\left(\frac{\theta_p - \omega_p}{2}\right)}{\sin\left(\frac{\theta_p + \omega_p}{2}\right)} \quad \underline{5112}$ $\omega_p = \text{desired cutoff frequency}$
Highpass	$-\frac{Z^{-1} + \alpha}{1 + \alpha Z^{-1}}$	$\alpha = -\frac{\cos\left(\frac{\omega_p + \theta_p}{2}\right)}{\cos\left(\frac{\omega_p - \theta_p}{2}\right)} \quad \underline{5114}$ $\omega_p = \text{desired cutoff frequency}$
Bandpass	$-\frac{Z^{-2} - \frac{2\alpha k}{k+1} Z^{-1} + \frac{k-1}{k+1}}{\frac{k-1}{k+1} Z^{-2} - \frac{2\alpha k}{k+1} Z^{-1} + 1}$	$\alpha = \frac{\cos\left(\frac{\omega_2 + \omega_1}{2}\right)}{\cos\left(\frac{\omega_2 - \omega_1}{2}\right)} \quad \underline{5116}$ $k = \cot\left(\frac{\omega_2 - \omega_1}{2}\right) \tan \frac{\theta_p}{2}$ $\omega_2, \omega_1 = \text{desired upper and lower cutoff frequencies}$
Bandstop	$\frac{Z^{-2} - \frac{2\alpha}{1+k} Z^{-1} + \frac{1-k}{1+k}}{\frac{1-k}{1+k} Z^{-2} - \frac{2\alpha}{1+k} Z^{-1} + 1}$	$\alpha = \frac{\cos\left(\frac{\omega_2 + \omega_1}{2}\right)}{\cos\left(\frac{\omega_2 - \omega_1}{2}\right)} \quad \underline{5118}$ $k = \tan\left(\frac{\omega_2 - \omega_1}{2}\right) \tan \frac{\theta_p}{2}$ $\omega_2, \omega_1 = \text{desired upper and lower cutoff frequencies}$

FIG. 51



FIG. 52A

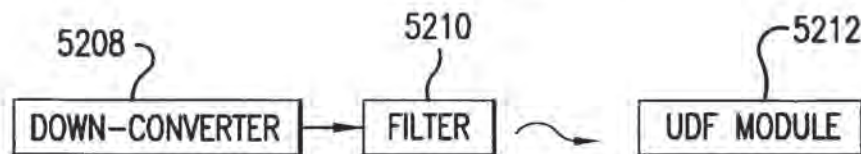


FIG. 52B

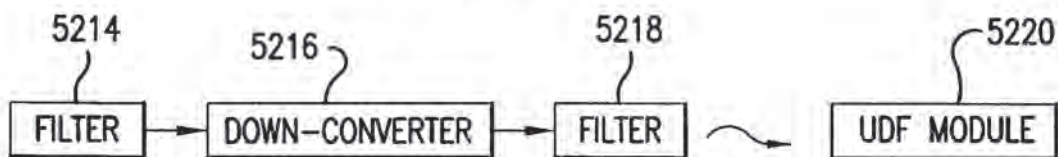


FIG. 52C



FIG. 52D



FIG. 52E



FIG. 52F

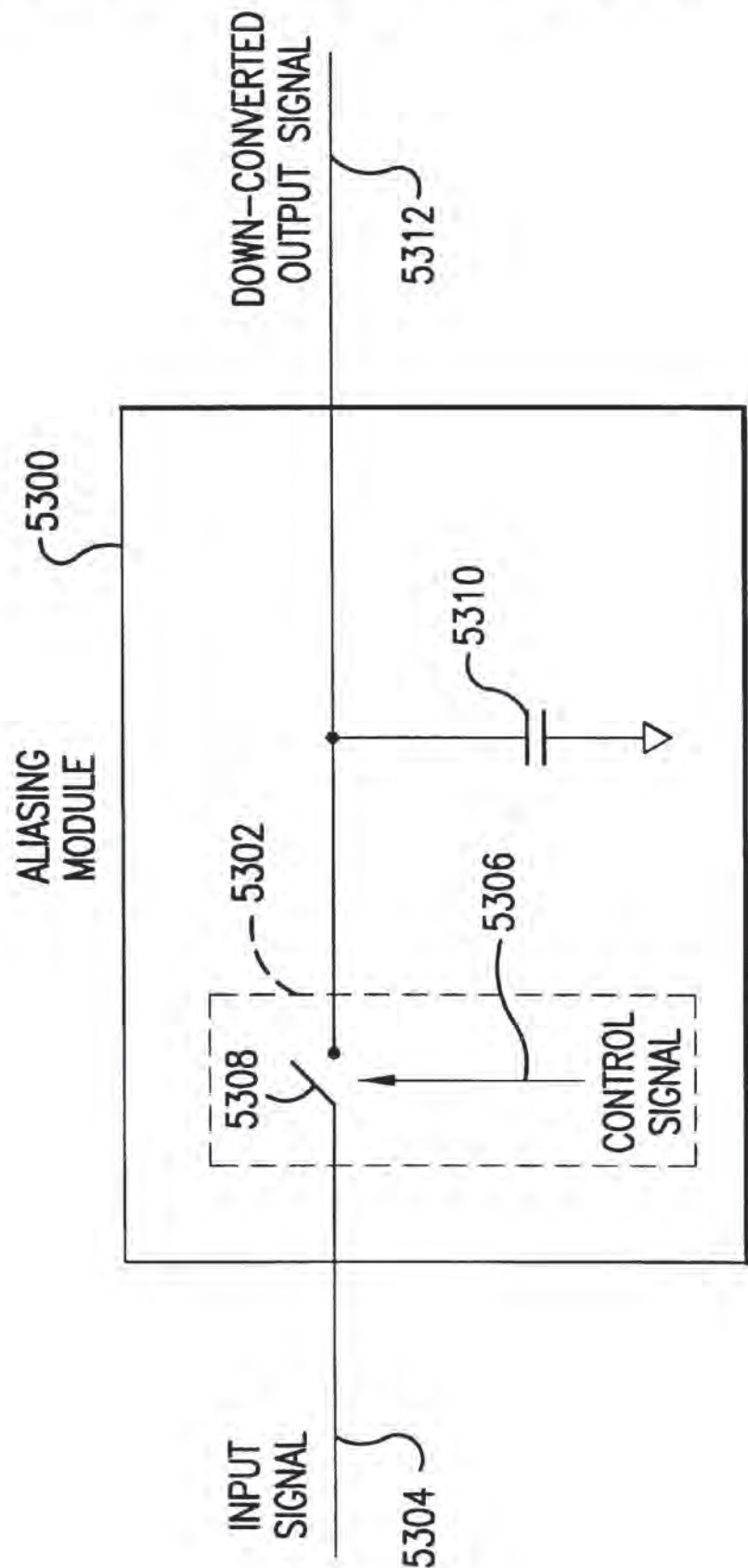


FIG. 53A

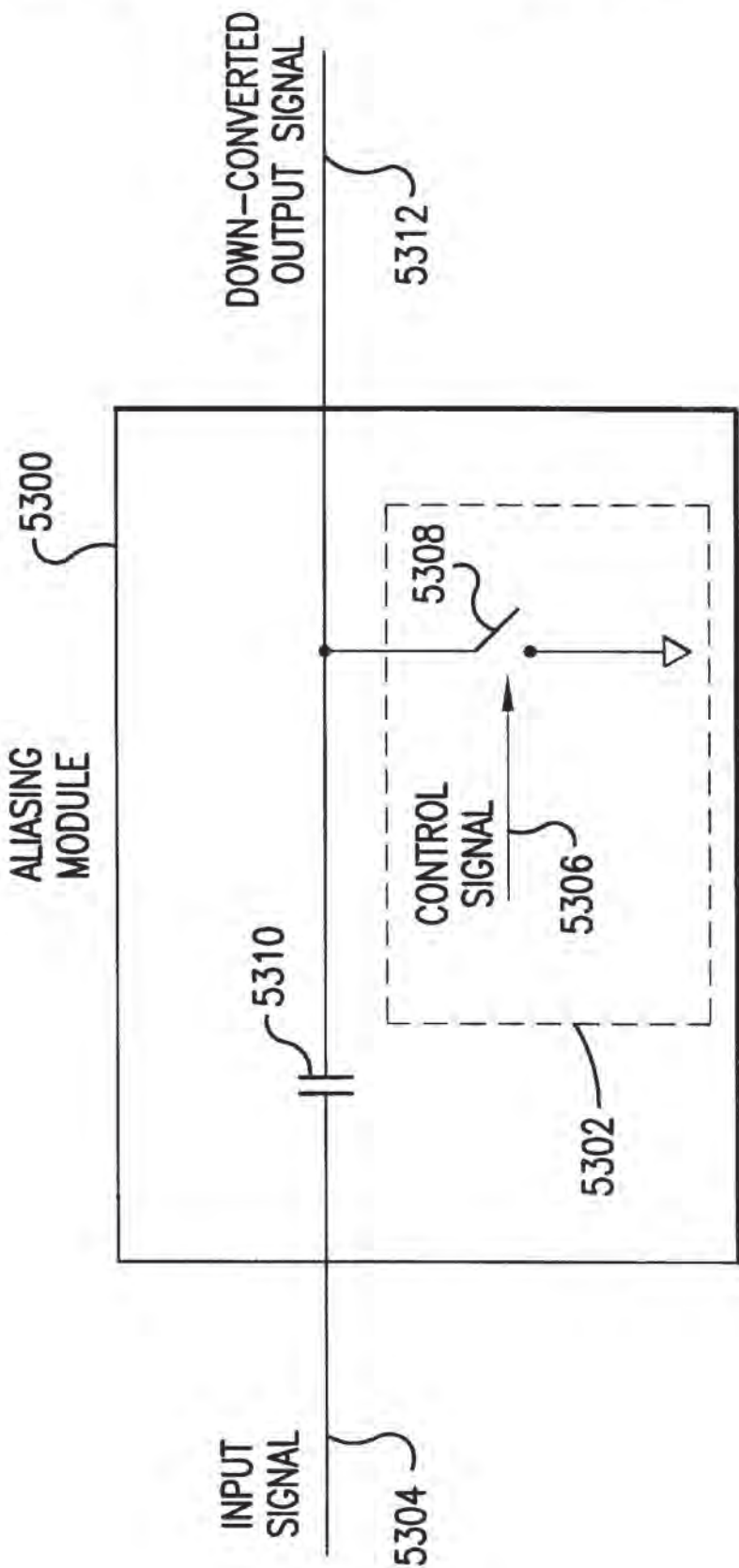


FIG. 53A-1

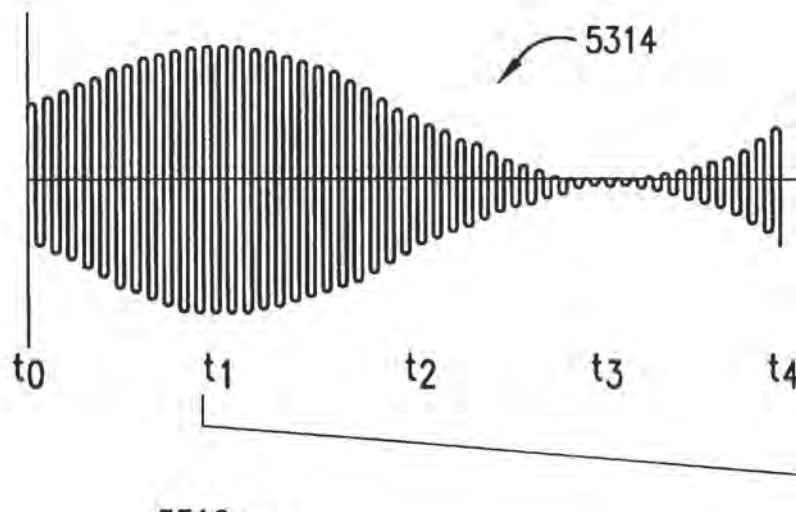


FIG. 53B

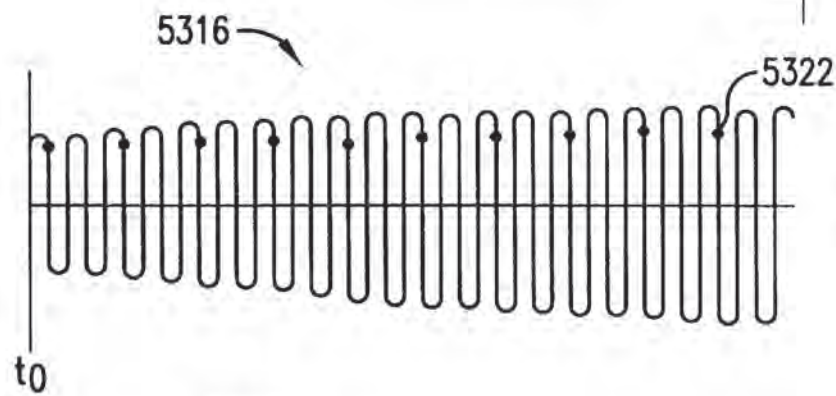


FIG. 53C

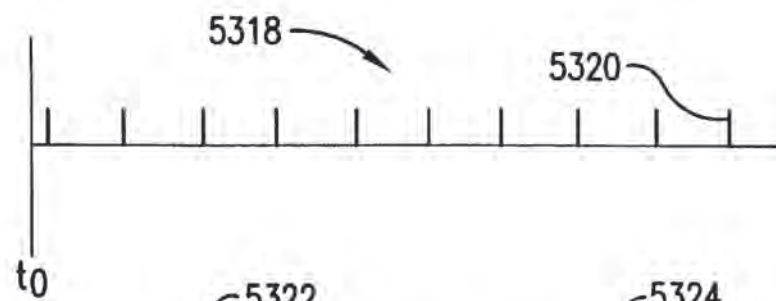


FIG. 53D

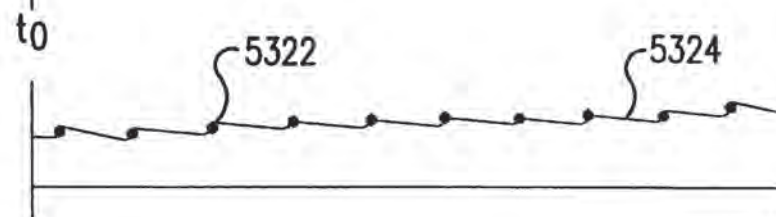


FIG. 53E

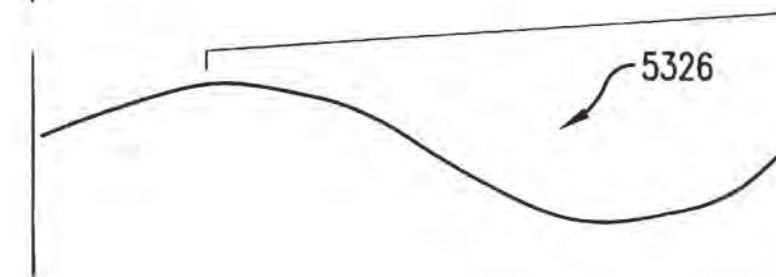


FIG. 53F

INTEGRATED FREQUENCY TRANSLATION AND SELECTIVITY

CROSS-REFERENCE TO OTHER APPLICATIONS

The following applications of common assignee are related to the present application, have the same filing date as the present application, and are herein incorporated by reference in their entireties:

"Method and System for Down-Converting Electromagnetic Signals," Attorney Docket No. 1744.0010000.

"Method and System for Frequency Up-Conversion," Attorney Docket No. 1744.0020000.

"Method and System for Ensuring Reception of a Communications Signal," Attorney Docket No. 1744.0030000.

"Universal Frequency Translation, and Applications of Same," Attorney Docket No. 1744.0140000.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention is generally related to methods and apparatuses for frequency translation and frequency selectivity.

2. Related Art

FIG. 1 is a block diagram of an example conventional receiver 112. FIG. 2 is a flowchart representing the operation of the receiver 112.

In step 206, a band-select filter 102 filters an RF (radio frequency) spectrum 114. An example RF spectrum 114 is shown in FIG. 4A. The RF spectrum 114 includes signal components at frequencies f_1 , f_2 , f_3 , and f_4 . Assume, for purposes of example, that the receiver 112 is configured to receive signals at frequency f_3 .

Typically, the band-select filter 102 is a wide-band filter. The characteristics of the band-select filter 102 are generally illustrated in FIG. 4B. The band-select filter 102 has a center frequency f_c , and a band-select bandwidth 402. In the example shown in FIG. 1, where the receiver 112 is receiving an RF spectrum 114, the center frequency f_c of the band-select filter 102 is within the RF range. For example, the center frequency f_c may be 900 MHz. Depending on the application, the band-select bandwidth 402 may be as much as 50 MHz, or greater. In the example where the center frequency f_c is 900 MHz and the band-select bandwidth 402 is 50 MHz, the passband (i.e., the band of frequencies that pass through a filter with little loss, relative to frequencies outside of the band) of the band-select filter 102 is 875 MHz to 925 MHz. According to these specifications, the quality factor of the band-select filter 102, or Q, is equal to 18 (as described further below, Q is equal to the center frequency divided by the bandwidth, or 900 MHz/50 MHz in this example). This Q factor is typical for a band-pass filter operating at RF. In fact, generally, high Q factors at high frequencies are difficult to realize using conventional filter techniques, and have at best limited tuning capabilities.

The band-select filter 102 in step 206 operates to filter out signals outside its passband. For example purposes, assume that f_1 and f_4 are outside the passband of the band-select filter 102, and f_2 and f_3 are inside the passband of the band-select filter 102 (this is the case in the example of FIGS. 4A and 4B). Accordingly, in this example, the band-select filter 102 operates to filter out the signal components at frequencies f_1 and f_4 . The band-select filter 102 passes the signal components at frequencies f_2 and f_3 . The result of the operation of the band-select filter 102 is shown in FIG. 4C.

In steps 208 and 210, the signal output by the band-select filter 102 (herein called the band-select filtered spectrum 408 for reference purposes) is processed by a low-noise amplifier (LNA) 104 and a mixer 106. The LNA 104 operates to amplify the band-select filtered spectrum 408, and the mixer 106 operates to down-convert the band-select filtered spectrum 408 in a well known manner.

Both the LNA 104 and the mixer 106 have limited dynamic ranges over which their operation is linear. Outside of these ranges, the LNA 104 and the mixer 106 exhibit non-linear operation. The broader the band select filter 102 (i.e., the wider the pass band), the more energy is able to reach the LNA 104 and the mixer 106. Consequently, the broader the band select filter 102, the greater the chance that the respective dynamic ranges of the LNA 104 and the mixer 106 will be exceeded. For purposes of example, assume that the signal component 420 at frequency f_3 combined with the undesired signal component 421 at frequency f_2 exceed the linear ranges of the LNA 104 and the mixer 106 (this is a common practical example).

When operating on a signal that is outside their linear ranges (i.e., when operating in a non-linear manner), the LNA 104 and/or the mixer 106 generate spurious signal components. In the given example, when operating on the signal components 420 and 421, the LNA 104 and/or the mixer 106 generate spurious signal components 404. See FIG. 4D. Some of these spurious components 404 may coincide and interfere with signals at desired frequencies. For example, as noted above, the receiver 112 is tuned to receive signals at frequency f_3 (in the example of FIGS. 4A-4G, frequency f_7 corresponds to f_3 after downconversion; similarly, frequency f_6 corresponds to f_2 after downconversion).

In the process of operating on the signal components 420 and 421, the LNA 104 and/or the mixer 106 generate a spurious signal component 404C at frequency f_7 . This spurious component 404C coincides with the desired signal component 420 at frequency f_7 . This spurious component 404C interferes with the desired signal component 420.

In step 212, a channel-select filter 108 filters the signal generated by the LNA 104 and the mixer 106 (this signal is herein called the processed spectrum 410 for reference purposes). The characteristics of the channel-select filter 108 are generally shown in FIG. 4E. The channel-select filter 108 has a center frequency at frequency f_7 and a channel-select bandwidth 406. The center frequency f_7 of the channel select filter 108 is at a lower frequency than the center frequency of the band select filter 102. For example, the center frequency f_7 of the channel select filter 108 may be 10 MHz. Depending on the application, the channel-select bandwidth 406 may be, for example, 50 KHz. According to these specifications, the quality factor of the channel-select filter 108, or Q, is equal to 200 (as indicated above, and described further below, Q is equal to the center frequency divided by the bandwidth, or 10 MHz/50 KHz in this example). This Q factor is typical for a narrowband band-pass filter operating at IF (intermediate frequency). As this example illustrates, it is possible to realize higher Q factors at lower frequencies using conventional filter techniques.

As shown in FIG. 4F, the effect of the channel-select filter 108 in step 212 is to filter-out the signal component at frequency f_6 and spurious components 404A, 404B, and 404D, but to pass any signals at frequency f_7 . Both the desired signal component 420 and the spurious component 404C exist at frequency f_7 , and are within the passband of the channel-select filter 108. Thus, both the desired signal

component 420 and the spurious component 404C are passed by the channel-select filter 108.

In step 214, an amplifier 110 amplifies the signal output from the channel-select filter 108 (this signal is called the channel select filtered signal 412 for reference purposes). The channel select filtered signal 412 includes both the desired signal component 420 and the spurious component 404C. Consequently, the amplifier 110 amplifies both the desired signal component 420 and the spurious component 404C.

In other words, once the spurious component 404C is generated, it follows the desired signal component 420 in all downstream processing.

As noted above, the spurious signal component 404C may make it difficult if not impossible to properly receive the desired signal component 420. Accordingly, because the receiver 112 utilized a wide-band, band-select filter 102 prior to amplification and frequency translation by non-linear components (i.e., by the LNA 104 and the mixer 106, respectively), the receiver 112 suffers from potentially degraded performance. The potential for signal interference as described above limits the receiver 112's applicability.

SUMMARY OF THE INVENTION

The present invention is directed to methods and apparatuses for frequency selectivity and frequency translation. The invention is also directed to applications for such methods and apparatuses.

Briefly stated, the invention operates to filter an input signal, and to down-convert the filtered input signal. According to embodiments of the present invention, the filtering operation and the down-conversion operation are performed in an integrated, unified manner.

According to embodiments of the invention, the filtering operation is effectively performed prior to the down-conversion operation. Thus, the frequency selectivity operation performed by the present invention represents input filtering, such as but not limited to front end filtering.

In embodiments of the invention, a relatively high Q factor can be realized regardless of center frequency.

In embodiments of the invention, the input signal is an RF signal. Thus, the frequency selectivity operation performed by the present invention represents relatively high Q RF filtering.

Thus, embodiments of the present invention preferably perform front end, narrowband filtering at RF, followed by frequency down-conversion.

In other words, embodiments of the invention provide precise frequency selectivity at high frequencies. Also, the invention provides for frequency down-conversion.

It is noted that the invention is not limited to the embodiments summarized in this section. The embodiments summarized in this section, as well as other embodiments, are described below.

Further features and advantages of the invention, as well as the structure and operation of various embodiments of the invention, are described in detail below with reference to the accompanying drawings. The drawing in which an element first appears is typically indicated by the leftmost digit(s) in the corresponding reference number.

BRIEF DESCRIPTION OF THE FIGURES

The present invention will be described with reference to the accompanying drawings, wherein:

FIG. 1 is a block diagram of a conventional receiver;

FIG. 2 is a flowchart representing the operation of the conventional receiver of FIG. 1;

FIG. 3 illustrates an operational map of the conventional receiver of FIG. 1;

FIGS. 4A-4G are waveforms used to illustrate the operation of the conventional receiver of FIG. 1;

FIG. 5 is used to illustrate the manner in which a filter's quality factor is calculated;

FIGS. 6A-6D illustrate characteristics of different types of filters;

FIGS. 7A-7C illustrate different types of modulation schemes;

FIG. 8 is a block diagram of a receiver and functions that are performed by the receiver;

FIG. 9 is an operational map of a receiver according to a preferred embodiment of the present invention;

FIGS. 10A-10E are waveforms used to describe the operational map of FIG. 9;

FIG. 11 is a block diagram of a unified downconverting and filtering (UDF) module according to an embodiment of the invention;

FIG. 12 is a block diagram of the UDF module of FIG. 11, wherein the unified performance of the frequency selectivity operation and the frequency translation operation according to the present invention is depicted;

FIG. 13 is a block diagram of the UDF module of FIG. 11, wherein it is illustrated that operations related to the frequency translation operation are performed prior to operations relating to the frequency selectivity operation, according to an embodiment of the invention;

FIG. 14 is a flowchart depicting the operation of the unified downconverting and filtering (UDF) module according to an embodiment of the invention;

FIG. 15 is a table illustrating example values at nodes within an example UDF module (shown in FIG. 26) at consecutive time increments;

FIG. 16 is a more detailed operational flowchart of the unified downconverting and filtering (UDF) operations performed by embodiments of the invention;

FIG. 17 is a more detailed block diagram of an example UDF module according to an embodiment of the invention;

FIG. 18 is an operational flowchart of the unified downconverting and filtering (UDF) operations performed by embodiments of the invention, wherein the filtering operation comprises a band-pass filtering operation;

FIG. 19 is an example implementation of the operational steps of FIG. 18;

FIG. 20 is a table representing example values in nodes of the UDF module of FIG. 19 at consecutive time increments;

FIG. 21 is an example block diagram of an example filter;

FIG. 22 is an operational flowchart of the unified downconverting and filtering (UDF) operations performed by embodiments of the invention, wherein the filtering operation comprises a low-pass filtering operation;

FIG. 23 is an example UDF module useful for implementing the steps of the flowchart in FIG. 22;

FIG. 24 is a flowchart illustrating the operation of an example midpoint injection embodiment of the present invention;

FIG. 25 is an example UDF module useful for performing the operational steps of the flowchart of FIG. 24;

FIG. 26 is an example implementation of the UDF module according to an embodiment of the invention;

FIGS. 27A and 27B are used to illustrate the filter characteristics of the UDF module of FIG. 26;

FIGS. 28A–28F and 29A–29F are waveforms used to illustrate the operation of the UDF module of FIG. 26;

FIG. 30 is a block diagram of an example receiver according to an embodiment of the invention;

FIG. 31 is a flowchart representing the operation of the receiver of FIG. 30 according to an embodiment of the invention;

FIG. 32 illustrates an example switched capacitor used to implement the delay modules in an example UDF module according to an embodiment of the invention;

FIGS. 33A and 33B illustrate a clock signal having two phases, ϕ_1 and ϕ_2 ;

FIG. 34 illustrates an example analog delay line used to implement the delay modules of an example UDF module according to an embodiment of the invention;

FIG. 35 illustrates a resistor attenuator used to implement the scaling modules in an example UDF module according to an embodiment of the invention;

FIG. 36 illustrates an example resistor attenuator;

FIG. 37 illustrates an example amplifier capable of implementing the scaling module in an example UDF module according to an embodiment of the invention;

FIG. 38 illustrates an example resistive summer capable of implementing the summer/adder in an example UDF module according to an embodiment of the invention;

FIG. 39 illustrates an example resistive summer;

FIG. 40 illustrates an example OPAMP (operational amplifier) summer capable of implementing the summer/adder in an example UDF module according to an embodiment of the invention;

FIG. 41 illustrates an example OPAMP summer;

FIG. 42 illustrates an example control signal generator according to an embodiment of the invention;

FIGS. 43A–43D illustrate signals present at nodes in the control signal generator of FIG. 42;

FIG. 44 illustrates an operational map of an example UDF module according to an alternate embodiment of the invention;

FIG. 45 is used to illustrate the operation of a sample and hold circuit according to an embodiment of the invention;

FIG. 46 is a flowchart representing an example operation of the sample and hold circuits shown in FIG. 45;

FIG. 47 is a table indicating example values present at nodes in the sample and hold circuits of FIG. 45;

FIG. 48 illustrates an example bi-phase clock signal used to control switches in the sample and hold circuits of FIG. 45;

FIG. 49 is a flowchart depicting the manner in which a UDF module is designed according to an embodiment of the invention;

FIG. 50 is a more detailed flowchart depicting the manner in which a UDF module is designed according to an embodiment of the invention;

FIG. 51 illustrates an example table of transform expressions that can be used when designing a UDF module according to embodiments of the invention;

FIGS. 52A–52F illustrate example applications of the UDF module according to embodiments of the invention;

FIGS. 53A and 53A–1 illustrate example aliasing modules according to an embodiment of the invention; and

FIGS. 53B–53F illustrate example waveforms used to describe the operation of the aliasing modules of FIGS. 53A and 53A–1.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

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1	Terminology

Various terms and concepts used in this application are generally described in this section. The description in this section is provided for illustrative and convenience purposes only, and is not limiting. The meaning of these terms and concepts will be apparent to persons skilled in the relevant art(s) based on the entirety of the teachings provided herein.

1.1 Filters

A filter is a device that allows electromagnetic signals of specific frequencies to pass with little attenuation. More particularly, a filter passes signals inside a frequency range (called a passband) with little attenuation. The filter does not pass signals outside of the passband (i.e., the filter attenuates signals outside of the passband).

There are a number of different types of filters. These include, for example, low-pass filters, high-pass filters, band-pass filters, notch filters, etc. The characteristics of these filters are generally illustrated in FIGS. 6A-6D.

There are many transfer functions for characterizing the operation of filters. For example, and without limitation, the following biquadratic equation represents the transfer function of a second order filter.

$$\frac{VO}{VI} = \frac{a_2 z^2 + a_1 z + a_0}{\beta_2 z^2 + \beta_1 z + \beta_0} \quad \text{EQ. 1}$$

Often, the β_2 coefficient is factored out in order to solve for z^2 . As will be appreciated, doing so merely results in changing the values of other coefficients. Without any loss of generality, EQ. 1 is re-written below with β_2 factored out (for ease of illustration, the effect of filtering out β_2 on the other coefficients of EQ. 1 is not explicitly indicated in the following):

$$\frac{VO}{VI} = \frac{a_2 z^2 + a_1 z + a_0}{z^2 + \beta_1 z + \beta_0}$$

It is noted that the invention is not limited to second order filters (the invention is applicable to filters of other orders), or to EQ. 1 for second order filters.

A well known conceptual block diagram implementation of this biquadratic equation is shown in FIG. 21. The z^{-1} designation in FIG. 21 designates a unit delay operation (that is, a z^{-1} module delays an input signal by one time unit).

The biquadratic equation of EQ. 1 applies to second order filter types. The transfer function for a particular type of second order filter (low-pass, high-pass, band-pass, notch, etc.) can be obtained from the biquadratic equation of EQ. 1 by appropriately setting the values of the coefficients. For example, a transfer function of a band-pass filter can be obtained from the biquadratic equation of EQ. 1 by setting α_2 and α_0 to zero. The resulting transfer function, representing the operation of a band-pass filter, is as follows:

$$\frac{VO}{VI} = \frac{\alpha_1 z}{z^2 + \beta_1 z + \beta_0} \quad \text{EQ. 2}$$

Solving for VO yields the following:

$$VO = \alpha_1 z^{-1} VI - \beta_1 z^{-1} VO - \beta_0 z^{-2} VO \quad \text{EQ. 3}$$

In the above, the value z equals the following:

$$z = \sin\left(\frac{f}{F_s}\right) + j\cos\left(\frac{f}{F_s}\right) \quad \text{EQ. 4}$$

In EQ. 4, f is the frequency, and F_s is the sample frequency of the system.

An example transfer function of a low-pass filter can be obtained from the biquadratic equation of EQ. 1 by setting α_2 and α_1 equal to zero. The resulting transfer function, corresponding to a low-pass filter, is as follows:

$$\frac{VO}{VI} = \frac{\alpha_0}{z^2 + \beta_1 z + \beta_0} \quad \text{EQ. 5}$$

Solving for VO yields the following:

$$VO = \alpha_0 z^{-2} VI - \beta_1 z^{-1} VO - \beta_0 z^{-2} VO \quad \text{EQ. 6}$$

Transfer functions for other types of filters, such as (and without limitation) high-pass filters and notch filters, can be obtained in a similar manner from the biquadratic equation of EQ. 1.

It should be noted that the transfer functions provided above are not the only representations of a band-pass filter and a low-pass filter. Multiple transfer functions for filter types can be obtained via different combinations of coefficient values in the biquadratic of EQ. 1, or via use of base equations other than the biquadratic of EQ. 1.

There are a number of measures for characterizing the performance of a filter. For example, and without limitation, the performance of a second order band-pass filter is often measured by its quality factor, or Q. FIG. 5 illustrates the manner in which Q is calculated for a second order filter. Q is equal to the center frequency f_c of the filter divided by the bandwidth BW of the filter. The bandwidth BW is measured at a point 3 DB below the maximum amplitude of the filter. Therefore, if a filter operates at a center frequency f_c of 1 MHz, and has a bandwidth BW of 50 KHz, the Q of the filter is

$$\frac{1,000,000}{50,000} = 20$$

1.2 Other Terms

Various terms used in this application are generally described in this section. The description in this section is provided for illustrative and convenience purposes only, and is not limiting. The meaning of these terms will be apparent to persons skilled in the relevant art(s) based on the entirety of the teachings provided herein. These terms may be discussed throughout the specification with additional detail.

Amplitude Modulation (AM): A modulation technique wherein the amplitude of the carrier signal is shifted (i.e., varied) as a function of the information signal. A subset of AM is referred to as "amplitude shift keying" which is used primarily for digital communications where the amplitude of the carrier signal shifts between discrete states rather than varying continuously as it does for analog information.

Analog signal: A signal that is constant or continuously variable as contrasted to changes between discrete states.

Baseband: A frequency band occupied by any generic information signal desired for transmission and/or reception.

Baseband signal: Any generic information signal desired for transmission and/or reception.

Carrier frequency: The frequency of a carrier signal. Typically, it is the center frequency of a transmission signal that is generally modulated.

Carrier signal: An EM wave having at least one characteristic that may be varied by modulation, that is capable of carrying information via modulation.

Control a switch: Causing a switch to open and close. The switch may be, without limitation, mechanical, electrical, electronic, optical, etc., or any combination thereof.

Demodulation: The process of removing or extracting information from a carrier signal.

Digital signal: A signal in which the information contained therein is discrete as contrasted to continuous.

Direct down conversion: A down conversion technique wherein a transmitted signal is directly down converted from the transmitted frequency (i.e., a carrier frequency) to the baseband signal without having an intermediate frequency.

Down conversion: A process for performing frequency translation in which the final frequency is lower than the initial frequency.

Electromagnetic spectrum: A spectrum comprising waves characterized by variations in electric and magnetic fields. Such waves may be propagated in any communication medium, both natural and manmade, including but not limited to air, space, wire, cable, liquid, waveguide, microstrip, stripline, optical fiber, etc. The EM spectrum includes all frequencies greater than zero hertz.

EM signal: A signal in the EM spectrum. Also generally called an EM wave. Unless stated otherwise, all signals discussed herein are EM signals, even when not explicitly designated as such.

Frequency Modulation (FM): A modulation technique wherein the frequency of the carrier signal is shifted (i.e., varied) as a function of the information signal. A subset of FM is referred to as "frequency shift keying" which is used primarily for digital communications where the frequency of the carrier signal shifts between discrete states rather than varying continuously as it does for analog information.

Harmonic: A harmonic is a sinusoidal component of a periodic wave. It has a frequency that is an integer multiple of the fundamental frequency of the periodic wave. In other words, if the periodic waveform has a fundamental frequency of "f" (also called the first harmonic), then it has harmonics at frequencies of "n-f," where "n" is 2, 3, 4, etc. The harmonic corresponding to n=2 is referred to as the second harmonic, the harmonic corresponding to n=3 is referred to as the third harmonic, and so on.

Information signal: The signal that contains the information that is to be transmitted. As used herein, it refers to the original baseband signal at the source. When it is intended that the information signal modulate a carrier signal, it is also referred to as the "modulating baseband signal." It may be voice or data, analog or digital, or any other signal or combination thereof.

Intermediate frequency (IF) signal: A signal that is at a frequency between the frequency of the baseband signal and the frequency of the transmitted signal.

Modulation: The process of varying one or more physical characteristics of a signal to represent the information to be transmitted. Three commonly used modulation techniques are frequency modulation, phase modulation, and amplitude modulation. There are also variations, subsets, and combinations of these three techniques.

Phase Modulation (PM): A modulation technique wherein the phase of the carrier signal is shifted (i.e., varied) as a function of the information signal. A subset of PM is referred to as "phase shift keying" which is used primarily for digital

communications where the phase of the carrier signal shifts between discrete states rather than varying continuously as it does for analog information.

Subharmonic: A subharmonic of a periodic waveform is a sinusoidal wave having a frequency that is an integer submultiple of the fundamental frequency of that periodic waveform. That is, a subharmonic frequency is the quotient obtained by dividing the fundamental frequency by an integer. For example, if the periodic waveform has a frequency of "f" (also called the fundamental), then its subharmonics have frequencies of "f/n," where n is 2, 3, 4, etc. The subharmonic corresponding to n=2 is referred to as the second subharmonic, the subharmonic corresponding to n=3 is referred to as the third subharmonic, and so on. A subharmonic itself has harmonics, and the ith harmonic of the ith subharmonic will be at the fundamental frequency of the original periodic waveform. For example, the third subharmonic (which has a frequency of "f/3"), has harmonics at integer multiples of itself (i.e., a second harmonic at "2-f/3," a third harmonic at "3-f/3," and so on). The third harmonic of the third subharmonic of the original signal (i.e., "3-f/3") is at the frequency of the original signal.

Up conversion: A process for performing frequency translation in which the final frequency is higher than the initial frequency.

2 Overview of the Invention

The present invention is directed to methods and apparatuses for frequency selectivity and frequency translation. The invention is also directed to applications for such methods and apparatuses.

According to the present invention, frequency selectivity and frequency translation are performed as a single unified (i.e., integrated) operation. By performing frequency selectivity and translation as a single unified operation, the invention achieves high frequency selectivity prior to frequency translation. The invention achieves high frequency selectivity at any input frequency (the input frequency refers to the frequency of the input spectrum being filtered and translated), including but not limited to RF (radio frequency) and greater frequencies. It should be understood that the invention is not limited to this example of RF and greater frequencies. The invention is intended, adapted, and capable of working with lower than radio frequencies.

Understanding of the invention may be facilitated by considering the operation of a receiver. Generally, a receiver performs three primary functions: frequency translation, frequency selection, and amplification. See FIG. 8. In the conventional receiver 112 of FIG. 1, for example, the mixer 106 performs the frequency translation operation; the band select filter 102 and the channel select filter 108 collectively perform the frequency selection operation; and the LNA 104 and the amplifier 110 collectively perform the amplification operation.

In the conventional receiver 112, note that the band select filter 102 is positioned prior to the mixer 106, and the channel select filter 108 is positioned after the mixer 106. Thus, in the conventional receiver 112, only a portion of the frequency selection operation 810 is performed prior to the frequency translation operation 808. Specifically, only band select filtering (i.e., wideband or image reject filtering) is performed prior to the frequency translation operation 810; channel select filtering (i.e., narrowband filtering) is performed after the frequency translation operation 808. This operational map of the conventional receiver 112 is illustrated in FIG. 3.

As described above, in the conventional receiver 112, signal components at frequencies near the desired frequency

are not filtered out by the band select filter 102. This is because the bandwidth of the band select filter 102 is wide (specifically, the bandwidth of the band select filter 102 is greater than the bandwidth of the channel select filter 108). These signal components can exceed the dynamic range of the system and cause the LNA 104 and/or the mixer 106 to generate spurious signal components that may interfere with other signal components at desired frequencies (see FIGS. 4A–4G). Thus, the conventional receiver 112 suffers from potentially degraded performance because only band select or wideband filtering is performed prior to the frequency translation operation 808 or other operations (such as the amplification operation 812) that involve components having a limited linear range (such as the mixer 106 and the LNA 104).

What would be desired is a receiver 902 having an operational map as shown in FIG. 9. In the receiver 902 of FIG. 9, preferably filtering (shown as the frequency selectivity operation 906 in FIG. 9) with a relatively narrow bandwidth (such as channel select filtering) is performed prior to the frequency translation operation 908 and the amplification operation 910. The advantages of the functional arrangement of the receiver 902 shall be considered with reference to FIGS. 10A–10E.

FIG. 10A illustrates an example input spectrum 904 having signal components at frequencies f_1 , f_2 , f_3 , and f_4 . Input spectrum 904 is, for example, an RF spectrum. Assume, for purposes of example, that the receiver 902 is tuned to receive signals at frequency f_3 . In the receiver 902, the frequency selectivity operation 906 is first performed on the input spectrum 904. In the example receiver 902, this frequency selectivity operation 906 comprises channel select filtering. The characteristics of such filtering is generally illustrated in FIG. 10B, where the filter (that is performing the frequency selectivity operation 906) is centered at frequency f_3 and has a channel select bandwidth 1002.

In the case where the input spectrum 904 is an RF spectrum, the center frequency f_3 is also an RF frequency. For purposes of example, assume that the center frequency f_3 is 900 MHz. Preferably, the channel select bandwidth 1002 is consistent with that of a narrow band filter. For example and without limitation, the channel select bandwidth 1002 may be 50 KHz, such that the passband associated with the frequency selectivity operation 906 is 899.95 MHz to 900.05 MHz. Accordingly, the frequency selectivity operation 906 of the receiver 902 represents a front end, narrow band filtering operation operating at RF. The Q of this filter is 900 MHz divided by 50 KHz, or 18,000. Thus, with the present invention, filters with high Q factors at high frequencies are realizable.

The frequency selectivity operation 906 operates to filter out signal components not falling within the passband associated with the frequency selectivity operation 906. For purposes of example, assume that the signal component at frequency f_3 falls within this passband, but the signal components at f_1 , f_2 , and f_4 fall outside this passband (this is the example shown in FIGS. 10A and 10B). Accordingly, only the signal component at frequency f_3 is passed by the frequency selectivity operation 906. This signal component at frequency f_3 is referred to as the filtered spectrum 914 for reference purposes.

In the receiver 902 of FIG. 9, the frequency translation operation 908 and the amplification operation 910 follow the frequency selectivity operation 906. Because of the operation of the frequency selectivity operation 906, these operations 908, 910 operate on only the signal component at

frequency f_3 . Other signal components (that is, the signal components at frequencies f_1 , f_2 , and f_4) were filtered out by the frequency selectivity operation 906 and, thus, these signal components are not processed by the frequency translation operation 908 or the amplification operation 910.

When the frequency translation operation 908 and the amplification operation 910 operate on the filtered signal 914, spurious components due to other than the filtered signal 914 are not generated. The result of the frequency translation operation 908 is depicted in FIG. 10D, and the result of the amplification operation 910 is depicted in FIG. 10E. Note that the desired output signal 912 shown in FIG. 10E is not compromised by spurious signal components.

The present invention is directed to methods and apparatuses for unified down-converting and filtering (UDF). The invention preferably performs at least the frequency selectivity operation 906 and the frequency translation operation 908. According to embodiments of the present invention, the frequency selectivity operation 906 performed by the present invention comprises filtering at any frequency, such as RF or greater. Such filtering is effectively performed prior to performance of the frequency translation operation 908, as shown in FIG. 9. Accordingly, the present invention exhibits the advantages described above with reference to FIGS. 10A–10E.

In some embodiments, the filter bandwidth of the present invention is consistent with narrow band filtering. Thus, the present invention can be accurately characterized as performing a narrow band filtering operation. In other embodiments, depending on the application, the filter bandwidth of the present invention is consistent with wide band filtering. Thus, the present invention can be accurately characterized as performing a wide band filtering operation. However, it should be understood that such characterizations of the invention are provided herein for illustrative purposes only. The filtering capabilities of the invention are not limited to those filter bandwidths typically associated with “narrow band filtering” and “wide band filtering.” Instead, the unified down-converting and filtering (UDF) functionality of the present invention can be designed with substantially any filter bandwidth. The present invention is intended, adapted, and capable of filtering using substantially any filter bandwidth.

As noted above, the invention is capable of operating with input electromagnetic signals having frequencies equal to RF and above. In these embodiments, the invention operates to filter and downconvert at RF and greater frequencies. However, it should be understood that the invention is not limited to operation at RF and above. Instead, the invention is intended, adapted, and capable of working with substantially any frequency.

The invention is operable with any communication medium, including but not limited to wireless, optical, wire, etc., and variations and combinations thereof.

Signals referred to herein may be modulated or unmodulated. Modulated signals may have been generated using any modulation scheme, such as AM, FM, PM, etc., or combinations thereof. See, for example and without limitation, various modulation examples shown in FIGS. 7A–7C.

The invention is described in detail below.

3 Unified Downconverting and Filtering

The following sections describe operational methods for unified down-converting and filtering (UDF) according to embodiments of the invention. Structural exemplary embodiments for achieving these methods are also described. It should be understood that the invention is not limited to the particular embodiments described below.

Equivalents, extensions, variations, deviations, etc., of the following will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such equivalents, extensions, variations, deviations, etc., are within the scope and spirit of the present invention.

3.1 Conceptual Description

The present invention is conceptually described in this section.

FIG. 11 is a conceptual block diagram of a unified down-converting and filtering (UDF) module 1102 according to an embodiment of the present invention. The UDF module 1102 performs at least the frequency translation operation 908 and the frequency selectivity operation 906 (FIG. 9).

The effect achieved by the UDF module 1102 is to perform the frequency selectivity operation 906 prior to the performance of the frequency translation operation 908. Thus, the UDF module 1102 effectively performs input filtering.

According to embodiments of the present invention, such input filtering involves a relatively narrow bandwidth. For example, such input filtering may represent channel select filtering, where the filter bandwidth may be, for example, 50 KHz to 150 KHz. It should be understood, however, that the invention is not limited to these frequencies. The invention is intended, adapted, and capable of achieving filter bandwidths of less than and greater than these values.

In embodiments of the invention, input signals 1104 received by the UDF module 1102 are at radio frequencies. The UDF module 1102 effectively operates to input filter these RF input signals 1104. Specifically, in these embodiments, the UDF module 1102 effectively performs input, channel select filtering of the RF input signal 1104. Accordingly, the invention achieves high selectivity at high frequencies.

The UDF module 1102 effectively performs various types of filtering, including but not limited to bandpass filtering, low pass filtering, high pass filtering, notch filtering, all pass filtering, band stop filtering, etc., and combinations thereof.

Conceptually, the UDF module 1102 includes a frequency translator 1108. The frequency translator 1108 conceptually represents that portion of the UDF module 1102 that performs frequency translation (down conversion).

The UDF module 1102 also conceptually includes an apparent input filter 1106 (also sometimes called an input filtering emulator). Conceptually, the apparent input filter 1106 represents that portion of the UDF module 1102 that performs input filtering.

In practice, the input filtering operation performed by the UDF module 1102 is integrated with the frequency translation operation. The input filtering operation can be viewed as being performed concurrently with the frequency translation operation. This is a reason why the input filter 1106 is herein referred to as an "apparent" input filter 1106.

The UDF module 1102 of the present invention includes a number of advantages. For example, high selectivity at high frequencies is realizable using the UDF module 1102. This feature of the invention is evident by the high Q factors that are attainable. For example, and without limitation, the UDF module 1102 can be designed with a filter center frequency f_c on the order of 900 MHz, and a filter bandwidth on the order of 50 KHz. This represents a Q of 18,000, as indicated below.

$$\frac{900 \cdot 10^6}{50 \cdot 10^3} = 18,000$$

It should be understood that the invention is not limited to filters with high Q factors. The filters contemplated by the present invention may have lesser or greater Qs, depending on the application, design, and/or implementation. Also, the scope of the invention includes filters where Q factor as described herein is not applicable.

The invention exhibits additional advantages. For example, the filtering center frequency f_c of the UDF module 1102 can be electrically adjusted, either statically or dynamically.

Also, the UDF module 1102 can be designed to amplify input signals.

Further, the UDF module 1102 can be implemented without large resistors, capacitors, or inductors. Also, the UDF module 1102 does not require that high tolerances be maintained on its individual components, i.e., its resistors, capacitors, inductors, etc. As a result, the architecture of the UDF module 1102 is friendly to integrated circuit design techniques and processes.

These and other advantages of the UDF module 1102 of the present invention will be apparent to persons skilled in the relevant art(s) based on the discussion contained herein.

Further understanding of the UDF module 1102 may be facilitated by making a comparison with the conventional receiver 112 (FIGS. 1 and 3). The frequency selectivity operations 302, 308 performed by the conventional receiver 112 are distinct from the frequency translation operation 306 (see FIG. 3). More particularly, the components which perform the frequency selectivity operation 302, 308 (that is, the band-select filter 102 and the channel-select filter 108) are different from the component that performs the frequency translation operation 306 (that is, the mixer 106).

The features and advantages exhibited by the UDF module 1102 are achieved at least in part by adopting a new technological paradigm with respect to frequency selectivity and translation. Specifically, according to the present invention, the UDF module 1102 performs the frequency selectivity operation and the frequency translation operation as a single, unified (integrated) operation. This is conceptually represented in FIG. 12, where the selectivity operation 1202 is shown as being combined or integrated with the frequency translation operation 1204. This is also indicated via the dotted line representations of the apparent input filter 1106 and the frequency translator 1108 in FIG. 11.

Referring to FIG. 13, as described above, the UDF module 1102 preferably performs frequency translation 1204 prior to frequency selectivity 1202 (in other embodiments, the reverse is true). The overlapping area 1302 depicted in FIG. 13 indicates that the operations relating to frequency translation 1204 also contribute to the performance of frequency selectivity 1202, and/or vice versa.

3.2 High Level Description

This section (including its subsections) provides a high-level description of unified down-converting and filtering (UDF) according to the present invention. In particular, an operational process of down-converting and filtering is described at a high-level. Also, a structural implementation for achieving this process is described at a high-level. This structural implementation is described herein for illustrative purposes, and is not limiting. In particular, the process described in this section can be achieved using any number of structural implementations, one of which is described in

this section. The details of such structural implementations will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

3.2.1 Operational Description

According to embodiments of the present invention, the UDF module generates an output signal from an input signal using samples/instances of the input signal and samples/instances of the output signal. This operation is represented by step 1406 in a flowchart 1402 (FIG. 14). By operating in this manner, the UDF module preferably performs input filtering and frequency down-conversion in a unified manner.

For illustrative purposes, the operation of the invention is often represented by flowcharts, such as flowchart 1402 in FIG. 14. It should be understood, however, that the use of flowcharts is for illustrative purposes only, and is not limiting. For example, the invention is not limited to the operational embodiment(s) represented by the flowcharts. Instead, alternative operational embodiments will be apparent to persons skilled in the relevant art(s) based on the discussion contained herein. Also, the use of flowcharts should not be interpreted as limiting the invention to discrete or digital operation. In practice, as will be appreciated by persons skilled in the relevant art(s) based on the herein discussion, the invention can be achieved via discrete or continuous operation, or a combination thereof. Further, the flow of control represented by the flowcharts is provided for illustrative purposes only. As will be appreciated by persons skilled in the relevant art(s), other operational control flows are within the scope and spirit of the present invention. Also, the ordering of steps may differ in various embodiments.

The operation of embodiments of the invention shall now be described in greater detail with reference to a flowchart 1602 shown in FIG. 16. The steps of flowchart 1602 generally represent step 1406 in FIG. 14.

In step 1606, the input signal is sampled. This input sample includes information (such as amplitude, phase, etc.) representative of the input signal existing at the time the sample was taken.

As described further below, the effect of repetitively performing step 1606 is to translate the frequency (that is, down-convert) of the input signal to a desired lower frequency, such as an intermediate frequency (IF) or baseband.

In step 1608, the input sample is held (that is, delayed).

In step 1610, one or more delayed input samples (some of which may have been scaled), such as the delayed input sample of step 1608, are combined with one or more delayed instances of the output signal (some of which may have been scaled) to generate a current instance of the output signal.

Thus, according to a preferred embodiment of the invention, the output signal is generated from prior samples/instances of the input signal and/or the output signal. (It is noted that, in some embodiments of the invention, current samples/instances of the input signal and/or the output signal may be used to generate current instances of the output signal.)

As noted above, this operation of the present invention supports multiple filtering types, including but not limited to bandpass, low pass, high pass, notch, all pass, etc., and combinations thereof.

3.2.2 Structural Description

FIG. 17 illustrates a UDF module 1702 according to an embodiment of the invention. The UDF module 1702 includes a portion that generally corresponds to the frequency translator 1108 (FIG. 11). The UDF module 1702 includes another portion that generally corresponds to the

input filter 1106. Note that the portion of the UDF module 1702 that corresponds to the frequency translator 1108 also forms a part of the input filter 1106. This further highlights the preferred aspect of the invention that the frequency selectivity operation 1202 and the frequency translation operation 1204 are performed as an integrated and unified operation.

Note that the UDF module 1702 includes scaling elements 1790. These elements are optional, and are used for amplification. The scaling elements 1790 are discussed in a section below. In the present discussion, the scaling elements 1790 are not considered.

The operation of the UDF module 1702 shall now be described with reference to flowchart 1602 in FIG. 16.

In step 1606, a down-convert and delay module 1708 samples the input signal 1704. This sampling operation is performed in accordance with a control signal 1734A. The down-convert and delay module 1708, when repetitively performing step 1606, results in translating the frequency of the input signal 1704 to a desired lower frequency, such as IF or baseband. Accordingly, the down-convert and delay module 1708 down-converts the input signal 1704 to a desired lower frequency.

In step 1608, the down-convert and delay module 1708 holds (delays) the input sample. This delaying operation by the down-convert and delay module 1708 contributes to the performance of the frequency selectivity operation 1202.

In step 1610, components of the UDF module 1702 operate to combine one or more delayed input samples (some of which may have been scaled) with one or more delayed instances of the output signal 1706 (some of which may have been scaled) to generate a current instance of the output signal 1706. More particularly, delay modules 1710A, 1710B, etc., operate to delay samples of the input signal 1704 taken by the down-convert and delay module 1708 (although two delay modules 1710A, 1710B are shown in the example of FIG. 17, the invention is not limited to this embodiment). Scaling modules 1716A, 1716B, 1716C, etc., operate to scale these delayed input samples from the down-convert and delay module 1708 and the delay modules 1710A, 1710B, etc.

Delay modules 1722A, 1722B, 1722C, etc., operate to delay instances of the output signal 1706 (note that the output signal 1706 is present at both nodes 1712 and 1718). (Although three delay modules 1722A–1722C are shown in the example of FIG. 17, the invention is not limited to this embodiment.) Scaling modules 1724A, 1724B, 1724C, etc., operate to scale these delayed instances of the output signal 1706 from the delay modules 1722A, 1722B, 1722C, etc.

An adder 1720 operates to combine the delayed and scaled input samples and the delayed and scaled instances of the output signal 1706 to generate instances of the output signal 1706.

As noted above, different embodiments of the UDF module utilize different numbers and/or configurations of delay modules 1710, 1722, and different numbers and/or configurations of scaling modules 1716 and 1724. Also, the operation of the delay modules 1710, 1722 and the scaling modules 1716, 1724 will vary among embodiments of the UDF module. For example, the amount of delay introduced by each delay module 1710, 1722 will vary among embodiments of the UDF module. Also, the scale factors of scaling modules 1716, 1724 will vary among embodiments of the UDF module (generally, the scale factor of each scaling module 1716, 1724 may be any real number). For example, and without limitation, the scale factor of one or more scaling modules in some embodiments may be zero.

Accordingly, it should be understood that the embodiments of the UDF module shown and discussed herein are provided for illustrative purposes only. The present invention is not limited to the embodiments of the UDF module shown and discussed herein. Alternate embodiments of the UDF module, differing slightly or greatly from those shown and discussed herein, will be apparent to persons skilled in the relevant art(s) based on the discussion contained herein.

3.3 Example Embodiments

Various embodiments related to the method(s) and structure(s) described above are presented in this section (and its subsections). These embodiments are described herein for purposes of illustration, and not limitation. The invention is not limited to these embodiments. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

3.3.1 First Embodiment: Band Pass Filtering and Frequency Translation

An example embodiment of the invention, wherein band-pass filtering and frequency translation are performed, is described in the following sections.

3.3.1.1 Operational Description

A representation of a transfer function for a band-pass filter is shown in EQ. 3, which was discussed above and presented below for convenience. As indicated above, EQ. 3 is described herein for illustrative purposes only, and is not limiting.

$$VO = \alpha_1 z^{-1} VI - \beta_1 z^{-1} VO - \beta_0 z^{-2} VO \quad \text{EQ. 3}$$

As evidenced by EQ. 3, the output signal VO is formed from a summation of scaled delayed values of the input signal VI and scaled delayed values of the output signal VO. More particularly, at any given time t, the value of the output signal VO is equal to a scaled value of the input signal VI from time t-1, minus a scaled value of the output signal VO from time t-1, minus a scaled value of the output signal VO from a time t-2.

It is noted that EQ. 3 is a transfer function for band-pass filtering the input signal VI. EQ. 3 is not in any way related to translating the frequency of the input signal VI. That is, EQ. 3 is not in any way related to down-converting the input signal VI. However, the invention preferably operates such that frequency translation is performed at substantially the same time that band-pass filtering is performed in accordance with EQ. 3. Such operation of the present invention shall now be described with reference to a flowchart 1802 presented in FIG. 18.

In step 1806, at a time t-1, the input signal VI is under-sampled. According to the present invention and as further described below, this under-sampling of the input signal results in translating the frequency of the input signal VI to a desired lower frequency (such as IF or baseband), such that the input sample is an instance of a down-converted image of the input signal VI. As described below, this input sample is used in the frequency selectivity operation. This further indicates the integrated operation of the present invention.

In step 1808, at a time t, the input sample that was held from step 1806 is released and scaled. The scaling value can be any real number, including but not limited to zero.

In steps 1810 and 1812, at time t, an instance of the output signal VO that was previously captured at time t-1, and that was held until this time, is released and scaled. The scaling value can be any real number, including but not limited to zero.

In steps 1814 and 1816, at time t, an instance of the output signal that was previously captured at time t-2, and that was held until this time, is released and scaled. The scaling value can be any real number, including but not limited to zero.

In step 1818, at time t, a current instance of the output signal, VO_t , is generated by combining the scaled and delayed sample of the input signal VI_{t-1} with the scaled and delayed instances of the output signal VO_{t-1} and VO_{t-2} .

3.3.1.2 Structural Description

FIG. 19 is a block diagram of a UDF module 1950 according to an embodiment of the invention. The UDF module 1950 includes a portion that corresponds to the frequency translator 1108 (FIG. 11), and a portion that corresponds to the input filter 1106. Note that the portion corresponding to the frequency translator 1108, that is, the down-convert and delay module 1908, also forms a part of the input filter 1106. This is indicative of the preferred aspect of the invention wherein the frequency selectivity operation 1202 and the frequency translation operation 1208 are performed as a single unified operation.

The UDF module 1950 of FIG. 19 is a structural embodiment for performing the operational steps of flowchart 1802 (FIG. 18). However, it should be understood that the scope and spirit of the present invention includes other structural embodiments for performing the steps of flowchart 1802. The specifics of these other structural embodiments will be apparent to persons skilled in the relevant art(s) based on the discussion contained herein.

The operation of the UDF module 1950 is now described in detail with reference to the flowchart 1802 of FIG. 18. Reference also will be made to a table 2002 in FIG. 20 that indicates example values at nodes in the UDF module 1950 at a number of consecutive time increments.

In step 1806, at time t-1, the down-convert and delay module 1908 under-samples the input signal VI. This input sample is denoted as VI_{t-1} . As noted above, in performing step 1806, the down-convert and delay module 1908 operates to translate the frequency of the input signal VI to a desired lower frequency, such as IF or baseband. Accordingly, the input sample VI_{t-1} represents an instance of a down-converted image of the input signal VI. This operation of the down-convert and delay module 1908 is further described below.

Also in step 1806, the down-convert and delay module 1908 holds the input sample VI_{t-1} for preferably one time unit. See cell 2004 in Table 2002. As apparent from EQ. 3, above, the band-pass filtering transfer function requires that the input sample be held for one time unit. Accordingly, when performing this portion of step 1806, the down-convert and delay module 1908 is performing a portion of the frequency selectivity operation 1202. Accordingly, as should be apparent by this description, the down-convert and delay module 1908 contributes to both the frequency translation operation 1204 and the frequency selectivity operation 1202.

In step 1808, at time t, the input sample that was held for one time unit (that is, VI_{t-1}) is released by the down-convert and delay module 1908, and scaled by the input scaling module 1909. Accordingly, the signal present at node 1902 is (see cell 2006 in Table 2002): $\alpha_1 \cdot VI_{t-1}$.

Previously, at time t-1, the first delay module 1912 captured an instance of the output signal VO. This instance of the output signal VO is denoted as VO_{t-1} . In step 1810, at time t, the first delay module 1912 releases this instance of the output signal VO_{t-1} . In step 1812, this instance of the output signal VO_{t-1} is scaled by the first scaling module 1916. The value present at node 1904 after operation of the first scaling module 1916 is (see cell 2012 in Table 2002): $-\beta_1 \cdot VO_{t-1}$.

Previously, at time $t-1$, the second delay module 1914 captured an instance of the output signal VO stored in the first delay module 1912 (note that the first delay module 1912 sampled the output signal VO to obtain this instance at time $t-2$). This instance of the output signal VO is denoted as VO_{t-2} . At time t , this instance of the output signal VO_{t-2} is released by the second delay module 1914.

In step 1816, the second scaling module scales this instance of the output signal VO_{t-2} . After operation of the second scaling module 1918, the following value is present at node 1906 (see cell 2016 in Table 2002): $-\beta_0 \cdot VO_{t-2}$.

In step 1818, at time t , a summer 1910 adds the values present at nodes 1902, 1904, and 1906. The sum represents the current instance of the output signal VO. This output signal instance is denoted as VO_t , and is equal to the following (see field 2008 in Table 2002): $\alpha_1 \cdot VI_{t-1} - \beta_1 \cdot VO_{t-1} - \beta_0 \cdot VO_{t-2}$.

3.3.2 Second Embodiment: Low Pass Filtering and Frequency Translation

An example embodiment of the invention, wherein low-pass filtering and frequency translation are performed, is described in the following sections.

3.3.2.1 Operational Description

EQ. 6 is a representation of a transfer function for a low-pass filter. EQ. 6, first introduced above, is presented below for convenience. As indicated above, EQ. 6 is described herein for illustrative purposes only, and is not limiting.

$$VO = \alpha_0 z^{-2} VI - \beta_1 z^{-1} VO - \beta_0 z^{-2} VO \quad \text{EQ. 6}$$

As evidenced by EQ. 6, a low-pass filtering operation can be achieved by adding a scaled instance of the input signal VI that has been delayed by two time units to two scaled instances of the output signal VO that had been delayed by one and two time units, respectively.

Note that the low-pass transfer function of EQ. 6 is not in any way related to the frequency translation operation 1204. However, the invention preferably operates such that frequency translation is performed at substantially the same time that low-pass filtering is performed in accordance with EQ. 6. Such operation of the present invention shall now be described with reference to a flowchart 2202 presented in FIG. 22.

In step 2206, at a time $t-2$, the input signal VI is under-sampled. The input sample is denoted as VI_{t-2} . According to the present invention and as further described below, this under-sampling of the input signal results in translating the frequency of the input signal VI to a desired lower frequency (such as IF or baseband), such that the input sample is an instance of a down-converted image of the input signal VI. The input sample is preferably held for two time periods.

Also in step 2206, the input sample VI_{t-2} is held for two time units. As evident from EQ. 6, in order to achieve a low-pass filtering operation, it is necessary to hold an instance of the input signal VI by two time units. Accordingly, this aspect of step 2206 constitutes a portion of the frequency selectivity operation 1202. Thus, in performing step 2206, the present invention is performing aspects of the frequency selectivity operation 1202. Thus, the down-convert and delay module 2308 contributes to both the frequency translation operation and the frequency selectivity operation.

In step 2208, at time t , the input sample VI_{t-2} that had been held by two time units is released. This input sample VI_{t-2} is scaled in step 2210.

In steps 2212 and 2214, at time t , an instance of the output signal VO_{t-1} that has been held by one time unit is released and scaled.

In steps 2216 and 2218, at time t , an instance of the output signal VO_{t-2} that has been held by two time units is released and scaled.

In step 2220, at time t , the current instance of the output signal, VO_t , is generated by combining the scaled input sample VI_{t-2} with the scaled instances of the output signal VO_{t-1} and VO_{t-2} .

3.3.2.2 Structural Description

FIG. 23 is a block diagram of a UDF module 2302 according to an embodiment of the invention. The UDF module 2302 includes a portion that corresponds to the frequency translator 1108, and a portion that corresponds to the input filter 1106. Note that the portion of the UDF module 2302 that corresponds to the frequency translator 1108 also forms a part of the input filter 1106.

The UDF module 2302 is a structural embodiment for performing the operational steps of flowchart 2202. However, it should be understood that the scope and spirit of the present invention includes other structural embodiments for performing the steps of flowchart 2202. The specifics of these other structural embodiments will be apparent to persons skilled in the relevant art(s) based on the discussion contained herein.

The operation of the UDF module 2302 shall now be described in detail with reference to the flowchart 2202 of FIG. 22.

At a time $t-2$, the down-convert and delay module 2308 under-samples the input signal VI. This input sample is denoted as VI_{t-2} . The down-convert and delay module 2308 under-samples the input signal VI to obtain input sample VI_{t-2} in accordance with a control signal 2324A. As further described below, the down-convert and delay module 2308 performs such sampling in a manner that operates to translate the frequency of the input signal VI to a desired lower frequency, such as IF or baseband. Accordingly, the input sample VI_{t-2} represents an instance of a down-converted image of the input signal VI.

Also in step 2206, the down-convert and delay module 2308 holds the input sample VI_{t-2} for one time unit. At time $t-1$, the input sample VI_{t-2} is captured by a delay module 2310, and held for an additional time unit. As evident from the low-pass filtering transfer function of EQ. 6, in order to perform the low-pass filtering operation, it is necessary to hold or delay the input signal VI by two time units. As just described, this delaying operation is performed collectively by the down-convert and delay module 2308 and the delay module 2310. Therefore, in performing this aspect of step 2206, the down-convert and delay module 2308 contributes to the performance of the frequency selectivity operation 1202, as well as the frequency translation operation 1204.

In step 2208, at time t , the input sample VI_{t-2} that has been held/delayed by two time units is released by the delay module 2310.

In step 2210, at time t , the input sample VI_{t-2} is scaled by the scaling module 2312.

Previously, at time $t-1$, the delay module 2316 captured an instance of the output signal VO. This instance of the output signal VO is denoted as VO_{t-1} . In step 2212, at time t , this instance of the output signal VO_{t-1} is released by the delay module 2316.

In step 2214, at time t , this instance of the output signal VO_{t-1} is scaled by the scaling module 2320.

Previously, at time $t-1$, the delay module 2318 captured an instance of the output signal VO stored in the delay

module 2316. This instance of the output signal VO is denoted as VO_{t-2} . At time t, in step 2216, this instance of the output signal VO_{t-2} is released by the delay module 2318.

In step 2218, at time t, this instance of the output signal VO_{t-2} is scaled by the scaling module 2322.

In step 2220, at time t, the current instance of the output signal, VO_t , is generated by combining the scaled input sample VI_{t-2} with the scaled instances of the output signal, VO_{t-1} and VO_{t-2} .

3.3.3 Third Embodiment: Filtering With Mid-Point Injection and Frequency Translation

The UDF embodiments described above are provided for illustrative purposes only. The invention is not limited to these embodiments.

For example, as will be appreciated by persons skilled in the relevant art(s), it is possible to achieve a given set of filter characteristics using a variety of transfer functions. The elements of such transfer functions can be arranged and configured to satisfy particular goals and/or requirements.

In a similar manner, a variety of UDF embodiments are possible. In such embodiments, components contained therein are selected and arranged to satisfy particular goals and/or requirements.

For example, and without limitation, it is possible to construct a UDF module 4402 having the operational map illustrated in FIG. 44. Such operation is herein characterized as filtering with mid-point injection, in combination with frequency translation. These embodiments are described in the following sections.

It is noted that the mid-point injection embodiment is presented to illustrate the great flexibility of the invention. In particular, UDF embodiments according to the invention can be constructed with a great variety of components and component configurations. Additional UDF embodiments will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

3.3.3.1 Operational Description

EQ. 3, discussed above, is a representation of a transfer function for a band-pass filter. EQ. 3 is reproduced below for convenience. As indicated above, EQ. 3 is described herein for illustrative purposes only, and is not limiting.

$$VO = \alpha_1 z^{-1} VI - \beta_1 z^{-1} VO - \beta_2 z^{-2} VO \quad \text{EQ. 3}$$

An embodiment of the UDF module for performing, in a unified manner, the frequency translation operation 1204 and the frequency selectivity operation 1202 according to the band-pass filtering transfer function of EQ. 3 was described above. See, for example, FIGS. 18 and 19.

An alternate embodiment of the present invention, wherein frequency translation is performed in an integrated manner with frequency selectivity per the band-pass filtering transfer function of EQ. 3, shall now be described with reference to a flowchart 2402 presented in FIG. 24. In flowchart 2402, step 2405 generally corresponds to steps 1606 and 1608 of FIG. 16, and steps 2406–2424 generally correspond to step 1610.

In step 2405, prior to and including time t–1, instances of the input signal VI are captured and delayed, as required by the band-pass filtering transfer function of EQ. 3. These delayed instances of the input signal VI are used in conjunction with other values (described below) to generate instances of the output signal VO.

For example, at time t–1, an instance of the input signal VI is captured. This capturing of the input signal VI is performed prior to any frequency translation of the input signal VI. Accordingly, the resulting instance of the input

signal VI is representative of the input signal VI prior to down-conversion. This instance of the input signal VI is denoted as $VI_{HF,t-1}$, where HF stands for “high frequency.”

In step 2406, at a time t–1, the output signal is under-sampled. The output signal being sampled has a relatively high frequency. In particular, the frequency of the output signal is generally equal to the frequency of the input signal VI before down-conversion. Accordingly, the output signal being sampled in step 2406 is denoted as VO_{HF} , where HF stands for “high frequency.”

According to the present invention, the under-sampling performed in step 2406 operates to translate the frequency of the high-frequency output signal VO_{HF} to a desired lower frequency, such as IF or baseband. Accordingly, the output sample VO_{t-1} represents an instance of a down-converted image of the high-frequency output signal VO_{HF} . As apparent from this discussion, this aspect of step 2406 relates to the frequency translation operation 4410.

Also in step 2406, the output sample VO_{t-1} is held for one time period. As evident from EQ. 3, the bandpass filtering transfer function requires that the output signal be held, as is being done in step 2406. Therefore, this aspect of step 2406 relates to the frequency selectivity operation 4408.

Accordingly, in step 2406, operations related to both the frequency translation operation 4410 and the frequency selectivity operation 4408 are performed in a single, unified (integrated) manner.

In steps 2408 and 2410, at time t, the high-frequency instance of the input signal $VI_{HF,t-1}$ that has been held by one time unit is released and optionally filtered and scaled. Preferably, the filtering done at this point involves relatively wide filter bandwidths (for example, wideband filtering as opposed to narrowband filtering).

In steps 2412 and 2414, at time t, the output sample VO_{t-1} from step 2406 that has been held for one time unit is released, and scaled.

In steps 2416 and 2418, at time t, an instance of the output signal VO that has been held by two time units is released and scaled. This instance of the output signal VO is denoted as VO_{t-2} .

In step 2420, at time t, the scaled VO_{t-1} and the scaled VO_{t-2} are summed. Note that VO_{t-1} and VO_{t-2} are at a frequency that is lower than the frequency of the input signal 2504. This is due to the fact that VO_{t-1} was obtained from an under-sampling operation that involved frequency down-conversion (as described above in step 2406), and the fact that VO_{t-2} was obtained from VO_{t-1} .

Also in step 2420, the sum of the scaled VO_{t-1} and the scaled VO_{t-2} is upconverted to a frequency substantially equal to the frequency of the input signal VI.

In step 2422, at time t, the scaled instance of the input signal $VI_{HF,t-1}$ is combined with the upconverted sum of the scaled VO_{t-1} and the scaled VO_{t-2} . This results in generating the current instance of the high-frequency output signal, $VO_{HF,t}$.

In step 2424, at time t, this current instance of the high-frequency output signal, $VO_{HF,t}$, is down-converted to the desired lower frequency, for example, IF or baseband. The result is an instance of the low-frequency output signal, $VO_{LF,t}$, where LF stands for “low frequency.”

3.3.3.2 Structural Description

FIG. 25 is a block diagram of a UDF module 2502 according to an embodiment of the invention. The UDF module 2502 includes a portion that corresponds to the frequency translator 1108, and a portion that corresponds to the input filter 1106. Note that the portion of the UDF module 2502 that corresponds to the frequency translator

1108 also forms a part of the portion of the UDF module 2502 that corresponds to the input filter 1106.

The UDF module 2502 is a structural embodiment for performing the operational steps of flowchart 2402. However, it should be understood that the scope and spirit of the present invention includes other structural embodiments for performing the steps of flowchart 2402. The specifics of these other structural embodiments will be apparent to persons skilled in the relevant art(s) based on the discussion contained herein.

The operation of the UDF module 2502 shall now be described in detail with reference to the flowchart 2402 of FIG. 24.

In step 2405, prior to and including time $t-1$, a high frequency delay module 2506 captures instances of the input signal VI. For example, at time $t-1$, an instance of the input signal VI is captured by the high frequency delay module 2506. This instance of the input signal VI is noted as $VI_{HF,t-1}$.

In step 2406, at a time $t-1$, the down-convert and delay module 2514 under-samples a high-frequency representation of the output signal VO_{HF} . This high-frequency output signal VO_{HF} is at a frequency substantially equal to the frequency of the input signal VI. As discussed in further detail below, the down-convert and delay module 2514 under-samples the high frequency output signal VO_{HF} in a manner so as to translate the frequency of the high-frequency output signal VO_{HF} to a desired lower frequency, such as IF or baseband. Accordingly, the output sample VO_{t-1} represents an instance of a down-converted image of the high frequency output signal VO_{HF} .

Also in step 2406, the output sample VO_{t-1} is held by the down-convert and delay module 2514.

In step 2408, at time t , the instance of the input signal $VI_{HF,t-1}$, that was previously captured by the high-frequency delay module 2506 at time $t-1$, is released.

In step 2410, at time t , the instance of the input signal $VI_{HF,t-1}$ is optionally filtered by a filter 2508, and scaled by a scaling module 2510.

In step 2412, at time t , the output sample VO_{t-1} from step 2406 is released by the down-convert and delay module 2514.

In step 2414, at time t , the output sample VO_{t-1} is scaled by the scaling module 2518.

Previously, at time $t-1$, a low frequency delay module 2516 captured an instance of the output sample VO_{t-2} stored in the down-convert and delay module 2514. In step 2416, at time t , this instance of the output signal VO_{t-2} is released by the low frequency delay module 2516.

In step 2418, at time t , the instance of the output signal VO_{t-2} is scaled by the scaling module 2520.

In step 2420, at time t , an adder 2522 sums the scaled sample of the output signal VO_{t-1} and the scaled instance of the output signal VO_{t-2} . Recall that VO_{t-1} and VO_{t-2} are at a frequency that is lower than the frequency of the input signal 2504. This is due to the fact that VO_{t-1} was obtained from an under-sampling operation that involved frequency down-conversion (as described above in step 2406), and the fact that VO_{t-2} was obtained from VO_{t-1} (as described above in step 2416).

Also in step 2420, the sum of the scaled VO_{t-1} and the scaled VO_{t-2} is upconverted by an upconvert module 2524 to a frequency substantially equal to the frequency of the input signal VI.

In step 2422, at time t , the scaled instance of the input signal $VI_{HF,t-1}$, is combined with the upconverted sum of the scaled sample of the output signal VO_{t-1} and the scaled

instance of the output signal VO_{t-2} . The result is the current instance of the high-frequency output signal, $VO_{HF,t}$. Note that this instance of the high-frequency output signal $VO_{HF,t}$ is at a frequency generally equal to the frequency of the input signal VI.

In step 2424, at time t , a down-convert module 2526 down-converts the current instance of the high-frequency output signal, $VO_{HF,t}$, to a desired lower frequency, such as IF or baseband. The result is an instance of the low-frequency output signal, VO_{LFr} .

3.3.4 Other Embodiments

The embodiments described above are provided for purposes of illustration. These embodiments are not intended to limit the invention. Alternate embodiments, differing slightly or substantially from those described herein, will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such alternate embodiments include, but are not limited to, embodiments of the UDF module where the filtering function is performed according to transfer functions differing from those utilized above. Such alternate embodiments also include, but are not limited to, embodiments of the UDF module where the frequency selectivity operation comprises filtering types not discussed above, such as, but not limited to, high pass filtering, notch filtering, etc. Such alternate embodiments fall within the scope and spirit of the present invention.

3.4 Implementation Examples

Exemplary operational and/or structural implementations related to the method(s), structure(s), and/or embodiments described above are presented in this section (and its subsections). These implementations are presented herein for purposes of illustration, and not limitation. The invention is not limited to the particular implementation examples described herein. Alternate implementations (including equivalents, extensions, variations, deviations, etc., of those described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such alternate implementations fall within the scope and spirit of the present invention.

3.4.1 Implementation Example of a Unified Downconverting and Filtering (UDF) Module

FIG. 26 illustrates an example implementation of the unified down-converting and filtering (UDF) module 2622. The UDF module 2622 performs the frequency translation operation 1204 and the frequency selectivity operation 1202 in an integrated, unified manner as described above, and as further described below.

In the example of FIG. 26, the frequency selectivity operation 1202 performed by the UDF module 2622 comprises a band-pass filtering operation. As noted above, EQ. 3 is an example representation of a band-pass filtering transfer function. EQ. 3 is presented below for convenience. As indicated above, EQ. 3 is described herein for illustrative purposes only, and is not limiting.

$$VO = \alpha_3 z^{-1} VI - \beta_1 z^{-1} VO - \beta_2 z^{-2} VO \quad \text{EQ. 3}$$

In the example of FIG. 26, the UDF module 2622 performs band-pass filtering in accordance with the example band-pass filtering transfer function of EQ. 3.

The UDF module 2622 includes a down-convert and delay module 2624, first and second delay modules 2628 and 2630, first and second scaling modules 2632 and 2634, an output sample and hold module 2636, and an (optional) output smoothing module 2638. Other embodiments of the UDF module will have these components in different configurations, and/or a subset of these components, and/or

additional components. For example, and without limitation, in the configuration shown in FIG. 26, the output smoothing module 2638 is optional. Alternate embodiments of the UDF module will be apparent to persons skilled in the relevant art(s) based on the discussion contained herein.

As further described below, in the example of FIG. 26, the down-convert and delay module 2624 and the first and second delay modules 2628 and 2630 include switches that are controlled by a clock having two phases, ϕ_1 and ϕ_2 . ϕ_1 and ϕ_2 preferably have the same frequency, and are non-overlapping (alternatively, a plurality such as two clock signals having these characteristics could be used). As used herein, the term "non-overlapping" is defined as two or more signals where only one of the signals is active at any given time. In some embodiments, signals are "active" when they are high. In other embodiments, signals are active when they are low. See, for example, FIGS. 33A and 33B.

Preferably, each of these switches closes on a rising edge of ϕ_1 or ϕ_2 , and opens on the next corresponding falling edge of ϕ_1 or ϕ_2 . However, the invention is not limited to this example. As will be apparent to persons skilled in the relevant art(s), other clock conventions can be used to control the switches.

In the example of FIG. 26, it is assumed that α_1 is equal to one. Thus, the output of the down-convert and delay module 2624 is not scaled. As evident from the embodiments described above, however, the invention is not limited to this example.

The filter characteristics of the example UDF module 2622 are presented in FIGS. 27A and 27B. The example UDF module 2622 has a filter center frequency of 900.2 MHz and a filter bandwidth of 570 KHz. The pass band of the UDF module 2622 is on the order of 899.915 MHz to 900.485 MHz. The Q factor of the UDF module 2622 is approximately 1579 (i.e., 900.2 MHz divided by 570 KHz).

Example waveforms present at nodes in the UDF module 2622 according to an example where the frequency of the input signal VI is 900.2 MHz and the frequency of the control or sample signal is 16 MHz, are presented in FIGS. 28A–28E. FIG. 28F illustrates VI corresponding to the example of FIGS. 28A–28E. FIGS. 28A–28F represent an in-band example, since the frequency of the input signal VI (i.e., 900.2 MHz) is within the passband of the example UDF module 2622. As such, the UDF module 2622 amplifies the input signal by a factor of approximately 5, as predicted by the frequency response of FIG. 27B.

Another series of example waveforms present in the UDF module 2622 where the frequency of the input signal VI is 897 MHz and the frequency of the control or sampling signal is 16 MHz, are presented in FIGS. 29A–29E. FIG. 29F illustrates VI corresponding to the example of FIGS. 29A–29E. FIGS. 29A–29F represent an out-of-band example, since the frequency of the input signal VI (i.e., 897 MHz) is not within the passband of the example UDF module 2622. As such, the UDF module 2622 attenuates the input signal by a factor of approximately 0.57, as predicted by the frequency response of FIG. 27B.

The operation of the UDF module 2622 shall now be described with reference to a Table 1502 (FIG. 15) that indicates example values at nodes in the UDF module 2622 at a number of consecutive time increments. It is assumed in Table 1502 that the UDF module 2622 begins operating at time $t-1$. As indicated below, the UDF module 2622 reaches steady state a few time units after operation begins. The number of time units necessary for a given UDF module to reach steady state depends on the configuration of the UDF module, and will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

At the rising edge of ϕ_1 at time $t-1$, a switch 2650 in the down-convert and delay module 2624 closes. This allows a capacitor 2652 to charge to the current value of an input signal, VI_{t-1} , such that node 2602 is at V_{t-1} . This is indicated by cell 1504 in FIG. 15. In effect, the combination of the switch 2650 and the capacitor 2652 in the down-convert and delay module 2624 operates to translate the frequency of the input signal VI to a desired lower frequency, such as IF or baseband. Thus, the value stored in the capacitor 2652 represents an instance of a down-converted image of the input signal VI. This operation of the down-convert and delay module 2624 is further described below.

Also at the rising edge of ϕ_1 at time $t-1$, a switch 2658 in the first delay module 2628 closes, allowing a capacitor 2660 to charge to VO_{t-1} , such that node 2606 is at VO_{t-1} . This is indicated by cell 1506 in Table 1502. (In practice, VO_{t-1} is undefined at this point. However, for ease of understanding, VO_{t-1} shall continue to be used for purposes of explanation.)

Also at the rising edge of ϕ_1 at time $t-1$, a switch 2666 in the second delay module 2630 closes, allowing a capacitor 2668 to charge to a value stored in a capacitor 2664. At this time, however, the value in capacitor 2664 is undefined, so the value in capacitor 2668 is undefined. This is indicated by cell 1507 in table 1502.

At the rising edge of ϕ_2 at time $t-1$, a switch 2654 in the down-convert and delay module 2624 closes, allowing a capacitor 2656 to charge to the level of the capacitor 2652. Accordingly, the capacitor 2656 charges to VI_{t-1} , such that node 2604 is at VI_{t-1} . This is indicated by cell 1510 in Table 1502.

The UDF module 2622 may optionally include a unity gain module 2690A between capacitors 2652 and 2656. The unity gain module 2690A operates as a current source to enable capacitor 2656 to charge without draining the charge from capacitor 2652. For a similar reason, the UDF module 2622 may include other unity gain modules 2690B–2690G. It should be understood that, for many embodiments and applications of the invention, these unity gain modules 2690A–2690G are optional. The structure and operation of the unity gain modules 2690 will be apparent to persons skilled in the relevant art(s).

Also at the rising edge of ϕ_2 at time $t-1$, a switch 2662 in the first delay module 2628 closes, allowing a capacitor 2664 to charge to the level of the capacitor 2660. Accordingly, the capacitor 2664 charges to VO_{t-1} , such that node 2608 is at VO_{t-1} . This is indicated by cell 1514 in Table 1502.

Also at the rising edge of ϕ_2 at time $t-1$, a switch 2670 in the second delay module 2630 closes, allowing a capacitor 2672 to charge to a value stored in a capacitor 2668. At this time, however, the value in capacitor 2668 is undefined, so the value in capacitor 2672 is undefined. This is indicated by cell 1515 in table 1502.

At time t , at the rising edge of ϕ_1 , the switch 2650 in the down-convert and delay module 2624 closes. This allows the capacitor 2652 to charge to VI_t , such that node 2602 is at VI_t . This is indicated in cell 1516 of Table 1502.

Also at the rising edge of ϕ_1 at time t , the switch 2658 in the first delay module 2628 closes, thereby allowing the capacitor 2660 to charge to VO_t . Accordingly, node 2606 is at VO_t . This is indicated in cell 1520 in Table 1502.

Further at the rising edge of ϕ_1 at time t , the switch 2666 in the second delay module 2630 closes, allowing a capacitor 2668 to charge to the level of the capacitor 2664. Therefore, the capacitor 2668 charges to VO_{t-1} , such that node 2610 is at VO_{t-1} . This is indicated by cell 1524 in Table 1502.

At the rising edge of ϕ_2 at time t , the switch **2654** in the down-convert and delay module **2624** closes, allowing the capacitor **2656** to charge to the level of the capacitor **2652**. Accordingly, the capacitor **2656** charges to VI_n such that node **2604** is at VI_n . This is indicated by cell **1528** in Table **1502**.

Also at the rising edge of ϕ_2 at time t , the switch **2662** in the first delay module **2628** closes, allowing the capacitor **2664** to charge to the level in the capacitor **2660**. Therefore, the capacitor **2664** charges to VO_n such that node **2608** is at VO_n . This is indicated by cell **1532** in Table **1502**.

Further at the rising edge of ϕ_2 at time t , the switch **2670** in the second delay module **2630** closes, allowing the capacitor **2672** in the second delay module **2630** to charge to the level of the capacitor **2668** in the second delay module **2630**. Therefore, the capacitor **2672** charges to VO_{t-1} , such that node **2612** is at VO_{t-1} . This is indicated in cell **1536** of FIG. **15**.

At time $t+1$, at the rising edge of ϕ_1 , the switch **2650** in the down-convert and delay module **2624** closes, allowing the capacitor **2652** to charge to VI_{t+1} . Therefore, node **2602** is at VI_{t+1} , as indicated by cell **1538** of Table **1502**.

Also at the rising edge of ϕ_1 at time $t+1$, the switch **2658** in the first delay module **2628** closes, allowing the capacitor **2660** to charge to VO_{t+1} . Accordingly, node **2606** is at VO_{t+1} , as indicated by cell **1542** in Table **1502**.

Further at the rising edge of ϕ_1 at time $t+1$, the switch **2666** in the second delay module **2630** closes, allowing the capacitor **2668** to charge to the level of the capacitor **2664**. Accordingly, the capacitor **2668** charges to VO_n as indicated by cell **1546** of Table **1502**.

In the example of FIG. **26**, the first scaling module **2632** scales the value at node **2608** (i.e., the output of the first delay module **2628**) by a scaling factor of -0.1 . Accordingly, the value present at node **2614** at time $t+1$ is $-0.1 \cdot VO_n$. Similarly, the second scaling module **2634** scales the value present at node **2612** (i.e., the output of the second scaling module **2630**) by a scaling factor of -0.8 . Accordingly, the value present at node **2616** is $-0.8 \cdot VO_{t-1}$ at time $t+1$.

At time $t+1$, the values at the inputs of the summer **2626** are: VI_t at node **2604**, $-0.1 \cdot VO_t$ at node **2614**, and $-0.8 \cdot VO_{t-1}$ at node **2616** (in the example of FIG. **26**, the values at nodes **2614** and **2616** are summed by a second summer **2625**, and this sum is presented to the summer **2626**). Accordingly, at time $t+1$, the summer generates a signal equal to $VI_t - 0.1 \cdot VO_t - 0.8 \cdot VO_{t-1}$.

At the rising edge of ϕ_1 at time $t+1$, a switch **2691** in the output sample and hold module **2636** closes, thereby allowing a capacitor **2692** to charge to VO_{t+1} . Accordingly, the capacitor **2692** charges to VO_{t+1} , which is equal to the sum generated by the adder **2626**. As just noted, this value is equal to: $VI_t - 0.1 \cdot VO_t - 0.8 \cdot VO_{t-1}$. This is indicated in cell **1550** of Table **1502**. This value is presented to the output smoothing module **2638**, which smooths the signal to thereby generate the instance of the output signal VO_{t+1} . It is apparent from inspection that this value of VO_{t+1} is consistent with the band pass filter transfer function of EQ. **3**.

3.4.2 Implementation Examples of Components of the UDF Module

Implementation examples of the components of the UDF module according to embodiments of the present invention are described in the following sections. These example implementations are provided for purposes of illustration only, and are not limiting.

3.4.2.1 Downconvert and Delay Module

Referring to FIG. **17** only for illustrative purposes, the down-convert and delay module **1708** performs the fre-

quency translation operation. In an embodiment, the down-convert and delay module **1708** under-samples the input signal **VI** such that the input under-samples form a down-converted signal. In an example implementation, the down-converted signal is an intermediate frequency (IF) representation of the input signal **VI**. In another example implementation, the down-converted signal is a demodulated baseband signal. The invention is not limited to these implementation examples.

In addition to performing the frequency translation operation, the down-convert and delay module **1708** also delays the input samples for the frequency selectivity (filtering) operation. Thus, the down-convert and delay module **1708** contributes to both the frequency translation operation and the frequency selectivity operation.

The down-convert and delay module is further described below.

3.4.2.1.1 Universal frequency down-conversion (UFD) Module

In FIG. **26**, the downconvert and delay module **2624** represents an example implementation of the down-convert and delay modules described herein, such as **1708** in FIG. **17**, **1908** in FIG. **19**, **2308** in FIG. **23**, and **2514** in FIG. **25**. The downconvert and delay module **2624** preferably includes the switch **2650** and the capacitor **2652**. The switch **2650** and the capacitor **2652** operate to down-convert the input signal **VI**. This aspect of the invention is described in this section.

In particular, the following discussion describes down-converting using a Universal Frequency Translation (UFT) Module. The down-conversion of an EM signal by aliasing the EM signal at an aliasing rate is fully described in co-pending U.S. Patent Application entitled "Methods and Systems for Down-converting an Electromagnetic Signal," Application No. (to be assigned). Attorney Docket Number 1744.0010000, the full disclosure of which is incorporated herein by reference. A relevant portion of the above mentioned patent application is summarized below to describe down-converting an input signal to produce a down-converted signal that exists at a lower frequency or a baseband signal.

FIG. **53A** illustrates an aliasing module **5300** (also called in this context a universal frequency down-conversion module) for down-conversion using a universal frequency translation (UFT) module **5302** which down-converts an EM input signal **5304**. In particular embodiments, aliasing module **5300** includes a switch **5308** and a capacitor **5310**. The electronic alignment of the circuit components is flexible. That is, in one implementation, the switch **5308** is in series with input signal **5304** and capacitor **5310** is shunted to ground (although it may be other than ground in configurations such as differential mode). In a second implementation (see FIG. **53A-1**), the capacitor **5310** is in series with the input signal **5304** and the switch **5308** is shunted to ground (although it may be other than ground in configurations such as differential mode). Aliasing module **5300** with UFT module **5302** can be easily tailored to down-convert a wide variety of electromagnetic signals using aliasing frequencies that are well below the frequencies of the EM input signal **5304**.

In one implementation, aliasing module **5300** down-converts the input signal **5304** to an intermediate frequency (IF) signal. In another implementation, the aliasing module **5300** down-converts the input signal **5304** to a demodulated baseband signal. In yet another implementation, the input signal **5304** is a frequency modulated (FM) signal, and the aliasing module **5300** down-converts it to a non-FM signal,

such as a phase modulated (PM) signal or an amplitude modulated (AM) signal. Each of the above implementations is described below.

In an embodiment, the control signal 5306 (which is an example of control signal ϕ_1 that controls switch 2650 in FIG. 26) includes a train of pulses that repeat at an aliasing rate that is equal to, or less than, twice the frequency of the input signal 5304. In this embodiment, the control signal 5306 is referred to herein as an aliasing signal because it is below the Nyquist rate for the frequency of the input signal 5304. Preferably, the frequency of control signal 5306 is much less than the input signal 5304.

The train of pulses 5318 of FIG. 53D controls the switch 5308 to alias the input signal 5304 with the control signal 5306 to generate a down-converted output signal 5312. More specifically in an embodiment, switch 5308 closes on a first edge of each pulse 5320 of FIG. 53D and opens on a second edge of each pulse. When the switch 5308 is closed, the input signal 5304 is coupled to the capacitor 5310, and charge is transferred from the input signal to the capacitor 5310. The charge stored during successive pulses forms down-converted output signal 5312.

Exemplary waveforms are shown in FIGS. 53B–53F.

FIG. 53B illustrates an analog amplitude modulated (AM) carrier signal 5314 that is an example of input signal 5304. For illustrative purposes, in FIG. 53C, an analog AM carrier signal portion 5316 illustrates a portion of the analog AM carrier signal 5314 on an expanded time scale. The analog AM carrier signal portion 5316 illustrates the analog AM carrier signal 5314 from time t_0 to time t_1 .

FIG. 53D illustrates an exemplary aliasing signal 5318 that is an example of control signal 5306. Aliasing signal 5318 is on approximately the same time scale as the analog AM carrier signal portion 5316. In the example shown in FIG. 53D, the aliasing signal 5318 includes a train of pulses 5320 having negligible apertures that tend towards zero (the invention is not limited to this embodiment, as discussed below). The pulse aperture may also be referred to as the pulse width as will be understood by those skilled in the art(s). The pulses 5320 repeat at an aliasing rate, or pulse repetition rate of aliasing signal 5318. The aliasing rate is determined as described below, and further described in co-pending U.S. Patent Application entitled “Method and System for Down-converting an Electromagnetic Signal,” Application No. (to be assigned), Attorney Docket Number 1744.0010000.

As noted above, the train of pulses 5320 (i.e., control signal 5306) control the switch 5308 to alias the analog AM carrier signal 5316 (i.e., input signal 5304) at the aliasing rate of the aliasing signal 5318. Specifically, in this embodiment, the switch 5308 closes on a first edge of each pulse and opens on a second edge of each pulse. When the switch 5308 is closed, input signal 5304 is coupled to the capacitor 5310, and charge is transferred from the input signal 5304 to the capacitor 5310. The charge transferred during a pulse is referred to herein as an under-sample. Exemplary under-samples 5322 form down-converted signal portion 5324 (FIG. 53E) that corresponds to the analog AM carrier signal portion 5316 (FIG. 53C) and the train of pulses 5320 (FIG. 53D). The charge stored during successive under-samples of AM carrier signal 5314 forms a down-converted signal 5324 (FIG. 53E) that is an example of down-converted output signal 5312 (FIG. 53A). In FIG. 53F a demodulated baseband signal 5326 represents the demodulated baseband signal 5324 after filtering on a compressed time scale. As illustrated, down-converted signal 5326 has substantially the same “amplitude envelope” as

AM carrier signal 5314. Therefore, FIGS. 53B–53F illustrate down-conversion of AM carrier signal 5314.

The waveforms shown in FIGS. 53B–53F are discussed herein for illustrative purposes only, and are not limiting. Additional exemplary time domain and frequency domain drawings, and exemplary methods and systems of the invention relating thereto, are disclosed in co-pending U.S. Patent Application entitled “Method and System for Down-converting an Electromagnetic Signal,” Application No. (to be assigned), Attorney Docket Number 1744.0010000.

As indicated above, the aliasing rate of control signal 5306 determines whether the input signal 5304 is down-converted to an IF signal, down-converted to a demodulated baseband signal, or down-converted from an FM signal to a PM or an AM signal. Generally, relationships between the input signal 5304, the aliasing rate of the control signal 5306, and the down-converted output signal 5312 are illustrated below:

$$\begin{aligned} (\text{Freq. of input signal } 5304) - n(\text{Freq. of control signal } 5306) &= \text{Freq. of down-converted output signal } 5312 \end{aligned}$$

For the examples contained herein, only the “+” condition will be discussed. The value of n represents a harmonic or sub-harmonic of input signal 5304 (e.g., $n=0.5, 1, 2, 3, \dots$).

When the aliasing rate of control signal 5306 is off-set from the frequency of input signal 5304, or off-set from a harmonic or sub-harmonic thereof, input signal 5304 is down-converted to an IF signal. This is because the under-sampling pulses occur at different phases of subsequent cycles of input signal 5304. As a result, the under-samples form a lower frequency oscillating pattern. If the input signal 5304 includes lower frequency changes, such as amplitude, frequency, phase, etc., or any combination thereof, the charge stored during associated under-samples reflects the lower frequency changes, resulting in similar changes on the down-converted IF signal. For example, to down-convert a 901 MHz input signal to a 1 MHz IF signal, the frequency of the control signal 5306 would be calculated as follows:

$$(\text{Freq}_{\text{input}} - \text{Freq}_{\text{IF}}) / n = \text{Freq}_{\text{control}} (901 \text{ MHz} - 1 \text{ MHz}) / n = 900 / n$$

For $n=0.5, 1, 2, 3, 4$, etc., the frequency of the control signal 5306 would be substantially equal to 1.8 GHz, 900 MHz, 450 MHz, 300 MHz, 225 MHz, etc.

Exemplary time domain and frequency domain drawings, illustrating down-conversion of analog and digital AM, PM and FM signals to IF signal, and exemplary methods and systems thereof, are disclosed in co-pending U.S. Patent Application entitled “Method and System for Down-converting an Electromagnetic Signal,” Application No. (to be assigned), Attorney Docket Number 1744.0010000.

Alternatively, when the aliasing rate of the control signal 5306 is substantially equal to the frequency of the input signal 5304, or substantially equal to a harmonic or sub-harmonic thereof, input signal 5304 is directly down-converted to a demodulated baseband signal. This is because, without modulation, the under-sampling pulses occur at substantially the same point of subsequent cycles of the input signal 5304. As a result, the under-samples form a constant output baseband signal. If the input signal 5304 includes lower frequency changes, such as amplitude, frequency, phase, etc., or any combination thereof, the charge stored during associated under-samples reflects the lower frequency changes, resulting in similar changes on the demodulated baseband signal. For example, to directly down-convert a 900 MHz input signal to a demodulated baseband signal (i.e., zero IF), the frequency of the control signal 5306 would be calculated as follows:

$$(Freq_{input}-Freq_{IF})/n=Freq_{control}(900\text{ MHz}-0\text{ MHz})/n=900\text{ MHz}/n$$

For $n=0.5, 1, 2, 3, 4$, etc., the frequency of the control signal **5306** should be substantially equal to 1.8 GHz, 900 MHz, 450 MHz, 300 MHz, 225 MHz, etc.

Exemplary time domain and frequency domain drawings, illustrating direct down-conversion of analog and digital AM and PM signals to demodulated baseband signals, and exemplary methods and systems thereof, are disclosed in the co-pending U.S. Patent Application entitled "Method and System for Down-converting an Electromagnetic Signal," Application No. (to be assigned), Attorney Docket Number 1744.0010000.

Alternatively, to down-convert an input FM signal to a non-FM signal, a frequency within the FM bandwidth must be down-converted to baseband (i.e., zero IF). As an example, to down-convert a frequency shift keying (FSK) signal (a sub-set of FM) to a phase shift keying (PSK) signal (a subset of PM), the mid-point between a lower frequency F_1 and an upper frequency F_2 (that is, $[(F_1+F_2)/2]$) of the FSK signal is down-converted to zero IF. For example, to down-convert an FSK signal having F_1 equal to 899 MHz and F_2 equal to 901 MHz, to a PSK signal, the aliasing rate of the control signal **5306** would be calculated as follows:

$$\begin{aligned}\text{Frequency of the input} &= (F_1 + F_2) \div 2 \\ &= (899\text{ MHz} + 901\text{ MHz}) \div 2 \\ &= 900\text{ MHz}\end{aligned}$$

Frequency of the down-converted signal=0 (i.e., baseband)

$$(Freq_{input}-Freq_{IF})/n=Freq_{control}(900\text{ MHz}-0\text{ MHz})/n=900\text{ MHz}/n$$

For $n=0.5, 1, 2, 3$, etc., the frequency of the control signal **5306** should be substantially equal to 1.8 GHz, 900 MHz, 450 MHz, 300 MHz, 225 MHz, etc. The frequency of the down-converted PSK signal is substantially equal to one half the difference between the lower frequency F_1 and the upper frequency F_2 .

As another example, to down-convert a FSK signal to an amplitude shift keying (ASK) signal (a subset of AM), either the lower frequency F_1 or the upper frequency F_2 of the FSK signal is down-converted to zero IF. For example, to down-convert an FSK signal having F_1 equal to 900 MHz and F_2 equal to 901 MHz, to an ASK signal, the aliasing rate of the control signal **5306** should be substantially equal to:

$$(900\text{ MHz}-0\text{ MHz})/n=900\text{ MHz}/n,$$

or

$$(901\text{ MHz}-0\text{ MHz})/n=901\text{ MHz}/n.$$

For the former case of 900 MHz/n, and for $n=0.5, 1, 2, 3, 4$, etc., the frequency of the control signal **5306** should be substantially equal to 1.8 GHz, 900 MHz, 450 MHz, 300 MHz, 225 MHz, etc. For the latter case of 901 MHz/n, and for $n=0.5, 1, 2, 3, 4$, etc., the frequency of the control signal **5306** should be substantially equal to 1.802 GHz, 901 MHz, 450.5 MHz, 300.333 MHz, 225.25 MHz, etc. The frequency of the down-converted AM signal is substantially equal to the difference between the lower frequency F_1 and the upper frequency F_2 (i.e., 1 MHz).

Exemplary time domain and frequency domain drawings, illustrating down-conversion of FM signals to non-FM signals, and exemplary methods and systems thereof, are disclosed in the co-pending U.S. Patent Application entitled

"Method and System for Down-converting an Electromagnetic Signal," Application No. (to be assigned), Attorney Docket Number 1744.0010000.

In an embodiment, the pulses of the control signal **5306** have negligible apertures that tend towards zero. This makes the UFT module **5302** a high input impedance device. This configuration is useful for situations where minimal disturbance of the input signal may be desired.

In another embodiment, the pulses of the control signal **5306** have non-negligible apertures that tend away from zero. This makes the UFT module **5302** a lower input impedance device. This allows the lower input impedance of the UFT module **5302** to be substantially matched with a source impedance of the input signal **5304**. This also improves the energy transfer from the input signal **5304** to the down-converted output signal **5312**, and hence the efficiency and signal to noise (sin) ratio of UFT module **5302**.

Exemplary systems and methods for generating and optimizing the control signal **5306** and for otherwise improving energy transfer and s/n ratio, are disclosed in the co-pending U.S. Patent Application entitled "Method and System for Down-converting an Electromagnetic Signal," Application No. (to be assigned), Attorney Docket Number 1744.0010000.

3.4.2.2 Delay Modules

As indicated above, a delay module operates to delay samples/instances of a signal presented at its input by a known amount.

For example, in the embodiment of the UDF module **2622** shown in FIG. 26, the first and second delay modules **2628** and **2630** operate to delay instances of the output signal VO. Specifically, the first delay module **2628** delays instances of the output signal VO by one time unit. The second delay module **2630** also delays instances of the output signal VO by one time unit. However, the second delay module **2630** receives its input from the first delay module **2628**. Accordingly, the effect of the second delay module **2630** (in combination with the first delay module **2628**) is to delay instances of the output signal VO by two time units. This is required, for example, by the second and third components of the example band-pass filtering transfer function of EQ. 3.

In the embodiment of the UDF module **2622** shown in FIG. 26, the first delay module **2628** and the second delay module **2630** are each implemented using a sample and hold circuit. For ease of presentation and illustration, such sample and hold circuits are depicted in FIG. 45. (As apparent from the discussion contained herein, other embodiments of the UDF module include delay modules. Such delay modules can also be implemented using sample and hold circuits. Alternatively, well known delay circuits or processors/software can be utilized, as will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.)

More particularly, FIG. 45 shows two sample and hold circuits **4501** and **4503**. The sample and holds **4501** and **4503** are similar in structure and operation. Generally, the first delay module **2628** and the second delay module **2630** can each be implemented using either the sample and hold **4501** or the sample and hold **4503**. Preferably, the first delay module **2628** and the second delay module **2630** are generally implemented in the example configuration shown in FIG. 45.

Each sample and hold **4501**, **4503** includes a first switch **4508**, **4524** and a second switch **4512**, **4528**, respectively. The first switches **4508**, **4524**, and the second switches **4512**,

4528 are controlled by a clock signal 4550. Preferably, the clock signal 4550 has two phases, ϕ_1 and ϕ_2 . Preferably, ϕ_1 and ϕ_2 have the same frequency, but are non-overlapping. The first switches 4508, 4524 are controlled by ϕ_1 . Preferably, the first switches 4508 and 4524 close on rising edges of ϕ_1 , and open on the following falling edges of ϕ_1 . The second switches 4512, 4528 are controlled by ϕ_2 . Preferably, the second switches 4512 and 4528 close on rising edges of ϕ_2 , and open on the following falling edges of ϕ_2 . Example representations of ϕ_1 and ϕ_2 are shown in FIG. 48. It is noted that the invention is not limited to this switching convention. In other embodiments, other switching conventions are used. Further, other circuit configurations could be used.

The sample and holds 4501, 4503 also each include a first capacitor 4510, 4526 and a second capacitor 4514, 4530, respectively. The sample and holds 4501, 4503 optionally include unity gain modules 4520, 4522, 4532, 4534 which operate in the manner described above.

The operation of the sample and holds 4501, 4503 is now described with reference to a flowchart 4602 shown in FIG. 46. Reference shall also be made to a Table 4702 that indicates example values at particular nodes in the sample and holds 4501 and 4503 at a number of consecutive time increments. In the example of Table 4702, it is assumed that operation of the sample and holds 4501, 4503 begins at time t . One or more cycles are required for the sample and holds 4501, 4503 to reach steady state. The number of cycles required to reach steady state will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

In step 4604, at the rising edge of ϕ_1 during a time t , the switch 4508 closes. Upon the closing of the first switch 4508, the first capacitor 4510 charges to V_i , such that node 4516 is at V_i . This is indicated in cell 4704 of Table 4702.

Note that the first switch 4524 in the sample and hold 4503 also closes upon the rising edge of ϕ_1 during t . This causes the first capacitor 4526 in the sample and hold 4503 to charge to the level stored in the second capacitor 4514 in the sample and hold 4501. However, in the example currently being discussed, the value of the second capacitor 4514 at the rising edge of ϕ_1 during time t is undefined. Accordingly, the charge in the first capacitor 4526 at this time t is undefined, as indicated in cell 4705 in Table 4702.

In step 4606, at the rising edge of ϕ_2 during time t , the second switch 4512 in the sample and hold 4501 closes. This causes the second capacitor 4514 to charge to the level of the first capacitor 4510. Accordingly, the second capacitor 4514 charges to V_i . This causes the value at node 4518 to become V_i . This is indicated in cell 4708 of table 4702.

Also upon the rising edge of ϕ_2 during time t , the second switch 4528 in the sample and hold 4503 closes, such that the second capacitor 4530 charges to the level of the first capacitor 4526 in the sample and hold 4503. However, as described above, the charge in the first capacitor 4526 at this time is undefined. Accordingly, the charge in the second capacitor 4530 at this time is undefined, as indicated by cell 4709 in Table 4702.

In step 4608, at the rising edge of ϕ_1 during time $t+1$, the first switch 4508 in the sample and hold 4501 closes. This causes the first capacitor 4510 to charge to $V_{i,t+1}$, such that node 4516 is at $V_{i,t+1}$. This is indicated in cell 4710 in Table 4702.

Also on the rising edge of ϕ_1 during time $t+1$, the first switch 4524 in the sample and hold 4503 closes. This causes the first capacitor 4526 in the sample and hold 4503 to charge to the level of the second capacitor 4514 in the

sample and hold 4501. Accordingly, the first capacitor 4526 charges to V_i , such that node 4536 is at V_i . This is indicated in cell 4714 of Table 4702.

In step 4610, at the rising edge of ϕ_2 during time $t+1$, the second switch 4512 in the sample and hold 4501 closes. This causes the second capacitor 4514 in the sample and hold 4501 to charge to the level of the first capacitor 4510. In other words, the second capacitor 4514 charges to $V_{i,t+1}$, such that node 4518 is at $V_{i,t+1}$. This is indicated by cell 4718 in Table 4702.

Also at the rising edge of ϕ_2 during time $t+1$, the second switch 4528 in the sample and hold 4503 closes. This causes the second capacitor 4530 to charge to the level of the first capacitor 4526 in the sample and hold 4503. In other words, the second capacitor 4530 charges to V_i , such that node 4538 is at V_i . This is indicated in cell 4722 of Table 4702.

FIG. 48 illustrates another representation of the operation of the sample and holds 4501, 4503. FIG. 48 illustrates ϕ_1 and ϕ_2 of the clock signal 4550. As discussed above, the first switches 4508, 4524 close at rising edges of ϕ_1 , and open at falling edges of ϕ_1 . The second switches 4512, 4528 close at rising edges of ϕ_2 , and open at falling edges of ϕ_2 .

Consider now the sample and hold 4501. When the first switch 4508 closes, the first capacitor 4510 begins to charge to the input signal V_i and continues to charge until the first switch 4508 opens. The first switch 4508 is closed while ϕ_1 is high. Accordingly, while ϕ_1 is high, the sample and hold 4501 samples the input signal V_i . This is indicated in FIG. 48 by a sample period 4802. FIG. 48 also indicates a hold period 4804. During this hold period 4804, the sample of the input signal V_i that is stored in the first capacitor 4510 is held in the sample and hold 4501. Specifically, this input sample is held in the first capacitor 4510 until the next rising edge of ϕ_1 (during time $t+1$). Also, at the rising edge of ϕ_2 during time t , the second switch 4512 closes and the second capacitor 4514 charges to this input sample. This value is held in the second capacitor 4514 until the next rising edge of ϕ_2 at time $t+1$.

Accordingly, in sample and hold 4501, V_i is sampled at the beginning of t , and is held in the sample and hold 4501 until after time period t expires (i.e., for greater than a full period of the clock signal 4550). Note, however, that the next sample and hold 4503 does not sample the output of the first sample and hold 4501 until the next rising edge of ϕ_1 (that is, the rising edge of ϕ_1 during time $t+1$). Thus, the first sample and hold 4501 samples V_i at time t ; this sample V_i does not propagate to the next sample and hold 4503 until time $t+1$. Accordingly, the sample and hold 4501 effectively holds or delays the sample of the input signal V_i for one time period. This delay period is denoted as 4806 in FIG. 48.

In practice, the charge in the first capacitor 4510 tracks the input signal V_i while the first switch 4508 is closed (i.e., during the sample period 4802 of time t). The charge stored in the first capacitor 4510 at the falling edge of ϕ_1 of time t constitutes the input sample V_i . In other words, the input sample V_i is defined in the sample and hold 4501 at the falling edge of ϕ_1 of time t . The input sample in the sample and hold 4501 is not re-defined until the next falling edge of ϕ_1 (i.e., the falling edge of ϕ_1 of time $t+1$). Accordingly, the delay of the sample and hold 4501 can be considered to be delay 4807 shown in FIG. 48.

The discussion in this section has thus far focused on the delay modules 2628, 2630 implemented using sample and hold circuits, as in the example UDF module 2622 of FIG. 26. However, the invention is not limited to this implementation example. Instead, the delay modules in the UDF module can be implemented using any apparatus or circuit that operates to delay an incoming signal by a predetermined amount.

For example, referring for illustrative purposes only to FIG. 17, the delay modules 1710, 1722 can each be implemented using a switched capacitor topology 3204, such as that shown in FIG. 32. The switch capacitor topology 3204 includes two switches 3208 and 3206 which operate according to ϕ_1 and ϕ_2 of a clock signal. An example representation of ϕ_1 and ϕ_2 is shown in FIGS. 33A and 33B.

In addition to delaying an input signal VI, the particular switch capacitor shown in FIG. 32 also scales the input signal as follows:

$$V2 = \frac{C1}{C2} * VI$$

Accordingly, when using a switched capacitor such as that shown in FIG. 32, the switch capacitor performs the function of both the delay module 1710, 1722 and the associated scaling module 1716, 1724.

The delay modules 1710, 1722 can also each be implemented using an analog delay line, such as the analog delay line 3404 in FIG. 34, for example. As will be apparent to persons skilled in the relevant art(s), an analog delay line 3404 is constructed using a combination of capacitors, inductors, and/or resistors. The analog delay line 3404 operates to delay an input signal by a known amount. In some embodiments, the analog delay line 3404 is combined with other components to achieve this function, such as samplers.

The above implementation examples are provided for illustrative purposes only, and are not limiting. Other implementation examples will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

3.4.2.3 Scaling Modules

The scaling modules in the UDF module operate to scale signals present at their respective inputs. Such scaling contributes to the filter characteristics (such as the filter center frequency and bandwidth) of the UDF module.

Referring for illustrative purposes only to the UDF module 1702 in FIG. 17, the scaling modules 1716, 1724 can be implemented using any apparatus or circuit that scales an input signal by a known amount. The scaling factor may be less than 1 (in the case of attenuation) or greater than 1 (in the case of amplification). More generally, the scaling factor may be any real number, including but not limited to zero.

For example, each scaling module 1716, 1724 can be implemented using a resistor attenuator 3504, as shown in FIG. 35. As will be appreciated by persons skilled in the relevant art(s), there are many types and configurations of resistor attenuators. FIG. 36 illustrates an example resistor attenuator 3602. This example resistor attenuator 3602 scales an input VI by:

$$V2 = \frac{R_2}{R_1 + R_2} * VI$$

Other circuit diagrams for resistor attenuators suitable for use as the scaling modules 1716, 1724 in the UDF module 1702 will be apparent to persons skilled in the relevant art(s).

An amplifier/attenuator 3704 can also be used to implement the scaling modules 1716, 1724. An example amplifier 3704 is shown in FIG. 37. As will be appreciated by persons skilled in the relevant art(s), amplifiers suitable for use as scaling modules 1716, 1724 in the UDF module 1702 can be implemented using a variety of circuit components, such as, but not limited to, operational amplifiers (OP AMPS), transistors, FETS, etc.

The above implementation examples are provided for illustrative purposes only, and are not limiting. Other implementation examples will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

3.4.2.4 Adder

Referring for illustrative purposes only to FIG. 17, the adder 1720 (also called the summer herein) sums the signals presented at its inputs. The adder 1720 can be implemented using any apparatus or circuit that sums a plurality of input signals.

For example, the adder 1720 can be implemented using a resistive summer 3804 (FIG. 38). As will be appreciated by persons skilled in the relevant art(s), there are many configurations of resistive summers. FIG. 39 illustrates an example resistive summer 3902 that can be used to implement the adder 1720. However, the invention is not limited by this example.

The adder 1720 could also be implemented using an OP AMP summer 4004 (FIG. 40). As will be appreciated by persons skilled in the relevant art(s), there are many types and configurations of OP AMP summers. For illustrative purposes, an example OP AMP summer 4102 is provided in FIG. 41. The structure and operation of the OP AMP summer 4102 will be apparent to persons skilled in the relevant art(s). It should be understood that the invention is not limited by the example OP AMP summer 4102 provided in FIG. 41.

The adder 1720 can also be implemented using a combination of summer components. This is shown, for example, in the embodiment of FIG. 26.

The above implementation examples are provided for illustrative purposes only, and are not limiting. Other implementation examples will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

3.4.2.5 Control Signal Generator

Referring for illustrative purposes only to the UDF module 1702 in FIG. 17, the down-convert and delay module 1708 and the delay modules 1710, 1722 preferably operate according to control signals 1734A–1734F. Preferably, the control signals 1734A–1734F represent a bi-phase control signal, that is, a control signal with two phases, ϕ_1 and ϕ_2 . Preferably, ϕ_1 and ϕ_2 have the same frequency and are not overlapping.

An example representation of ϕ_1 and ϕ_2 is shown in FIGS. 43B and 43D. Any apparatus and circuit for generating such a bi-phase control signal can be utilized with the present invention. An example implementation of a control signal generator 1790 is presented in FIG. 42.

The control signal generator 1790 includes an oscillator 4204 and optionally a signal shaper 4205 that generate a series of pulses at a sampling frequency f_s . This is represented in FIG. 43A. A signal splitter 4206 splits this oscillating signal into two identical signals. An example representation of these two signals is shown in FIGS. 43B and 43C. These two signals are present at nodes 4216 and 4214, respectively, in the control signal generator 4202.

The signal splitter 4206 may cause some attenuation in the signals. Consequently, some embodiments of the invention may include amplifiers.

A delay module 4208 operates to delay one of the signals so as to generate ϕ_2 present at node 4218. This is shown in FIG. 43D.

As noted above, in some embodiments, it is useful to adjust the aperture (width) of the pulses in one or more of the control signals ϕ_1 and/or ϕ_2 . In such embodiments, an optional aperture optimizing module 4210 performs the task of adjusting the aperture (width) of the pulses of the control

signals ϕ_1 and/or ϕ_2 . The structure and operation of an embodiment of the aperture optimizing module 4210 is described in detail in co-pending U.S. Patent Application titled, "Methods and Systems for Down-Converting Electromagnetic Signals," referenced above.

The above implementation examples are provided for illustrative purposes only, and are not limiting. Other implementation examples will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

3.4.2.6 Output Sample and Hold Module

Some embodiments of the UDF module may include an output sample and hold module. For example, the example UDF module 2622 in FIG. 26 includes an output sample and hold module 2636. Preferably, the output sample and hold module 2636 is positioned at the output of the adder 2626.

As evident from the embodiments discussed above, the output signal VO generated by the UDF module is typically represented by the output of the adder (although there are some embodiments and applications where this is not the case). See, for example, the UDF module 1702 in FIG. 17. In some implementations of the UDF module, such as that shown in FIG. 26, the value present at the output of the adder 2626 may not always represent a valid instance of the output signal VO. This is due, for example, to the propagation of signals through the UDF module. The output sample and hold module 2636 ensures that only valid values of the output of the adder 2626 (i.e., only valid instances of the output signal VO) are presented to downstream devices external to the UDF module.

In the example of FIG. 26, the value at the output of the adder 2626 is guaranteed to be valid only at rising edges of ϕ_1 . Accordingly, a switch 2691 in the output sample and hold module 2636 closes upon rising edges of ϕ_1 , thereby allowing the capacitor 2692 in the output sample and hold module 2636 to charge to the value at the output of the adder 2626. This value in the capacitor 2692 is presented to an output smoothing module 2638. The signal generated by the output smoothing module 2638 represents the output signal VO. See, for example, cell 1550 in Table 1502, and the accompanying description provided above.

The above implementation examples are provided for illustrative purposes only, and are not limiting. Other implementation examples will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

3.4.2.7 Output Smoothing Module

Some embodiments of the UDF module may include an output smoothing module. For example, the example UDF module 2622 of FIG. 26 includes an output smoothing module 2636. The output smoothing module 2638 operates to smooth the signal generated by the output sample and hold module 2636. It is noted that the output smoothing module is an optional component.

The above implementation example is provided for illustrative purposes only, and is not limiting. Other implementation examples will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

3.4.2.8 Mid-Point Injection Embodiment: High Frequency Delay Module

Referring to FIG. 25, the high frequency delay module 2506 utilized in the UDF module 2502 of the mid-point injection embodiments of the present invention can be implemented using any apparatus that delays a relatively high frequency signal, or instances of the signal, for a given amount of time. The frequency of the signal may be, for example, RF or greater (but the invention is not limited to these frequencies—the frequency of the signal may be less than RF).

Any well known delay lines and/or transmission structures can be used to implement the high frequency delay module 2506. For example, a transmission line of known length can be used to implement the high frequency delay module 2506. As will be apparent to persons skilled in the relevant art(s), a particular delay can be obtained using a transmission line of known length.

Other apparatuses or structures for implementing the high frequency delay module 2506 will be apparent to persons skilled in the relevant art(s) based on the discussion contained herein.

3.4.2.9 Mid-Point Injection Embodiment: Optional Filter

Referring to FIG. 25, the filter 2508 optionally utilized in the UDF module 2502 of the mid-point injection embodiments of the present invention can be implemented using any appropriate filtering apparatus. Preferably, the filter 2508 represents a high frequency, wideband filter. Any appropriate known filter topology can be employed, such as an LC configuration, strip lines, and/or a saw filter. Many apparatuses or structures for implementing the filter 2508 will be apparent to persons skilled in the relevant art(s) based on the discussion contained herein.

3.4.2.10 Mid-Point Injection Embodiment Downconvert Module

Referring to FIG. 25, the downconvert module 2526 utilized in the UDF module 2502 of the mid-point injection embodiments of the present invention can be implemented using any apparatus that performs frequency down-conversion. For example, any well known frequency down-conversion apparatus employing a mixer and an oscillator can be used. Other well known apparatuses that perform frequency down-conversion suitable for use with the present invention will be apparent to persons skilled in the relevant art(s) based on the discussion contained herein.

According to embodiments of the invention, the downconvert module 2526 is alternatively implemented using the universal frequency down-conversion (UFD) module. The UFD module is described above.

3.4.2.11 Mid-Point Injection Embodiment: Upconvert Module

Referring to FIG. 25, the upconvert module 2524 utilized in the UDF module 2502 of the mid-point injection embodiments of the present invention can be implemented using any apparatus that performs frequency upconversion that retains amplitude and phase information. For example, any well known frequency upconversion apparatus employing a mixer and an oscillator can be used. Other well known apparatuses that perform frequency upconversion suitable for use with the present invention will be apparent to persons skilled in the relevant art(s) based on the discussion contained herein.

The reader is directed to co-pending U.S. application "Method and System for Frequency Up-Conversion," Attorney Docket No. 1744.0020000, incorporated herein by reference in its entirety. Teachings relating to frequency up-conversion contained in that U.S. application may be applicable to this and other aspects of the present invention.

3.4.3 Implementing the UDF Module as an Integrated Circuit (IC)

The invention is direct to the UDF module implemented on an integrated circuit (IC).

Understanding of this aspect of the invention may be facilitated by considering IC fabrication technology.

The fabrication of filters typically requires very tight tolerances on component parts of the filters, such as capacitors, inductors, resistors, etc. In contrast, the UDF module of the present invention does not require a high

degree of accuracy on the values of elements used therein. More particularly, the UDF module does not require a high degree of accuracy on the value of any given individual circuit element used therein.

Instead, according to the invention, the parameters of the filters depend on the ratio of element values. This is illustrated, for example, by the above description of the switched capacitor of FIG. 32, where the scaling factor depended on the ratio of C1 to C2.

As will be appreciated by persons skilled in the relevant art(s), it is difficult with present day fabrication technology to achieve tight tolerances on individual circuit component values, especially when operating at high frequencies (such as RF and above). However, current technology allows for tight tolerances on the ratios of circuit component values. This is generally the case for all operating frequencies. Thus, the invention facilitates the IC fabrication process.

This aspect of the present invention is one factor that enables the UDF module to be implemented as an IC.

There are a number of additional aspects of the UDF module that enable it to be implemented as an IC.

For example, the component of the UDF module that preferably performs the frequency translation operation, i.e., the universal frequency down-conversion module, is achieved using a limited number of components. See, for example, the embodiment of FIG. 26, where the frequency down-conversion operation is being performed essentially by a switch 2650 and a capacitor 2652.

Also, according to the present invention, input filtering is preferably achieved using a limited number of components. Again, for example, see the example UDF module 2622 of FIG. 26.

Further, the goals of the invention (input filtering and frequency translation) are preferably achieved without the use of large capacitors, inductors, or resistors. These aspects of the invention are discussed above.

Thus, the architecture of the invention is friendly to integrated circuit design techniques and processes. Consequently, as will be appreciated by persons skilled in the relevant art(s) based on the teachings contained herein, any of the embodiments of the UDF module can be implemented on an integrated circuit using existing fabrication technology.

3.4.4 Other Implementations

The implementations described above are provided for purposes of illustration. These implementations are not intended to limit the invention. Alternate implementations, differing slightly or substantially from those described herein, will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such alternate implementations fall within the scope and spirit of the present invention.

4 Designing a Unified Downconverting and Filtering (UDF) Module

A methodology for designing a unified downconverting and filtering (UDF) module according to an embodiment of the invention shall now be described. This methodology is applicable to any of the embodiments of the UDF module discussed or contemplated herein.

It should be understood that this methodology is provided for purposes of illustration, and is not intended to limited the invention. Alternate design methodologies, differing slightly or substantially from those described herein, will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such alternate design methodologies fall within the scope and spirit of the present invention.

Referring now to a flowchart 4902 in FIG. 49, in step 4904, the UDF module is designed so as to exhibit desired frequency translation characteristics. Such characteristics may include, for example and without limitation, the expected frequency of the input signal and the desired frequency of the output signal. Such characteristics may also include, for example and without limitation, whether the input signal is down-converted to an IF signal, down-converted to a demodulated baseband signal, down-converted from an FM signal to a PM or an AM signal, etc. Such characteristic may also include, for example and without limitation, whether energy transfer should be augmented during the frequency translation process.

In step 4906, the UDF module is designed so as to exhibit desired frequency selectivity characteristics. Such characteristics may include, for example and without limitation, the type of filtering to be performed by the UDF module (low pass, high pass, band pass, all pass, band stop, notch, etc.), the filtering center frequency, the filtering bandwidth, the filtering passband, etc.

It is noted that steps 4904 and 4906 may be performed in any order.

In step 4908, the UDF module is constructed in accordance with the design considerations of steps 4904 and 4906.

The operation of the steps of flowchart 4902 shall now be described in greater detail with reference to a flowchart 5002 in FIG. 50.

Step 4904 (designing the UDF module so as to exhibit desired frequency translation characteristics) is represented by step 5004 in FIG. 50. Preferably, the desired frequency translation characteristics of the UDF module is established by selecting the sampling rate. There may be other considerations, as described above, and further described in co-pending U.S. Patent Application titled, "Methods and Systems for Down-Converting Electromagnetic Signals," referenced above.

Step 4906 (designing the UDF module so as to exhibit desired frequency selectivity characteristics) is represented by steps 5006-5010 in FIG. 50, which are now described.

In step 5006, a low pass transfer function in the S plane is obtained/selected. As will be appreciated by persons skilled in the relevant art(s), it is common practice to design a filter by starting with a lowpass filter at a desired cutoff frequency. As will be further appreciated by persons skilled in the relevant art(s), there are numerous formulas and/or design tables for low pass transfer functions, including Butterworth, Chebyshev, elliptic filters, etc. Any of these may be utilized as the S plane low pass transfer function obtained/selected in step 5006.

In step 5008, the S plane low pass transfer function obtained in step 5006 is converted to a Z plane low pass transfer function. Step 5008 is preferably performed by substituting S variables in the S plane low pass transfer function with the expression provided in EQ. 8. As will be appreciated by persons skilled in the relevant art(s), other S plane to Z plane transformations exist. Any of these transformations may be used in the present invention.

$$S = \frac{2(1 - z^{-1})}{T(1 + z^{-1})} \quad \text{EQ. 8}$$

In EQ. 8, T represents the inverse of the sampling rate (determined in step 5004). In other words, T is equal to 1/(sampling rate).

In step 5010, if necessary, the Z plane low pass transfer function is modified to obtain desired filtering characteristics.

tics. Preferably, the modifications of step 5010 are performed using any well known transformation expressions. Examples of such well known transformation expressions are provided, without limitation, in FIG. 51 (the transformation expressions of FIG. 51 are independent of the manner in which the S plane to Z plane conversion was performed in step 5008). In these expressions, θ_p represents the cutoff frequency of the S low pass transfer function obtained and modified in steps 5006 and 5008.

The table 5102 in FIG. 51 is from Oppenheim and Schafer, *Digital Signal Processing*, Prentice-Hall, New Jersey, 1975, page 230. This entire publication is herein incorporated by reference.

As will be appreciated by persons skilled in the relevant art(s), other transformation expressions exist. Any such transformations can be used by the present invention.

When using the example transformations of table 5102, it is possible to obtain a Z plane high pass transfer function from the Z plane low pass transfer function of step 5008 by using the transformation and formulas of cells 5106 and 5114. It is possible to obtain a Z plane bandpass transfer function from the Z plane low pass transfer function of step 5008 by using the transformation and formulas of cells 5108 and 5116. It is possible to obtain a Z plane bandstop transfer function from the Z plane low pass transfer function of step 5008 by using the transformation and formulas of cells 5110 and 5118. It is possible to obtain a modified Z plane lowpass transfer function from the Z plane low pass transfer function of step 5008 by using the transformation and formulas of cells 5104 and 5112.

The equations and transformations of FIG. 51 establish filtering characteristics such as the center frequency and the passband. For example, with regard to the bandpass filter, once the transformation in cell 5108 has been applied to the Z plane low pass transfer function generated in step 5008, the original low pass cutoff frequency θ_p represents the center frequency of the band pass filter. The passband of the band pass filter is defined by ω_1 and ω_2 .

It is noted that Z plane transfer functions generated as described above with reference to steps 5006, 5008, and 5010 may differ in form and/or content from the transfer functions of EQS. 1-6. This illustrates the great flexibility, broad scope, and wide applicability of the present invention. In particular, the present invention is operable according to (i.e., the invention can be implemented in accord with) any or at least a large number of filtering transfer functions generated using any or at least a large number of procedures, as will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

Still referring to FIG. 50, in step 4908, the UDF module is constructed in accordance with the design considerations of steps 5004-5010. Consider, for example, the UDF module 1702 in FIG. 17. The number of delay elements and the arrangement of the delay elements in the UDF module 1702 (such as the downconvert and delay module 1708 and the delay modules 1710, 1722) are dictated by the delay factors in the filter transfer function produced after operation of steps 5006, 5008, and 5010. This is apparent from the discussion in prior sections. The sampling rate selected in step 5004 corresponds to the control signal 1734. The constants in the filter transfer function (produced after operation of steps 5006, 5008, and 5010) are achieved by the scaling modules 1716, 1724 (and optionally 1790).

5 Adjustable UDF Module

As noted above, and referring to FIG. 17 for illustrative purposes only, the frequency translation and selectivity characteristics of the UDF module 1702 are established in

large part by the control signal 1734 (including the sample clock) and the scaling modules 1716, 1724. In embodiments of the UDF module, various parameters are adjustable, including but not limited to the control signal 1734 and the scaling modules 1716, 1724. Accordingly, frequency translation and selectivity characteristics of the UDF module that depend on the control signal 1734 and the scaling modules 1716, 1724 are adjustable. In some embodiments, such characteristics (and perhaps others) are electronically adjustable.

Frequency translation characteristics, including but not limited to the desired frequency of the output signal, whether the input signal is down-converted to an IF signal, down-converted to a demodulated baseband signal, down-converted from an FM signal to a PM or an AM signal, etc., and whether energy transfer should be augmented during the frequency translation process, can be adjusted by adjusting, for example and without limitation, characteristics of the control signal 1734 (such as rate and/or pulse aperture).

Frequency selectivity characteristics, including but not limited to the filter center frequency, the filter bandwidth, the filter passband, the filter type, etc., can be adjusted by adjusting, for example and without limitation, the scaling factors of the scaling modules 1716, 1722 and/or the control signal 1734 (such as rate and/or pulse aperture).

The control signal can be adjusted, for example, by implementing the control signal generator 4202 (FIG. 42) using a tunable oscillator, and implementing the aperture optimizing module 4210 using tunable components (such as tunable resistors, capacitors, inductors, etc.). Such tunable elements may be electrically tunable.

The scaling factors can be adjusted by implementing the scaling modules 1716, 1722 using adjustable components, such as tunable resistors, capacitors, inductors, etc. Such tunable elements may be electrically tunable.

The tunable devices may be manually controlled. Alternatively, embodiments of the UDF module include control modules to automatically control such tunable devices (in some embodiments, the control modules operate according to user input and/or commands). The control modules may operate in real time, such that the UDF module is dynamically tunable. The control modules may be implemented as a software controlled processor, a state machine, etc., or combinations thereof.

6 Amplification

As described above, unified down-converting and filtering according to embodiments of the present invention involves both frequency down-conversion and filtering. According to embodiments of the invention, unified down-converting and filtering of the present invention also includes signal amplification. This feature of the invention is discussed in this section.

Recall, for example purposes only, EQ. 2 that represents an example transfer function of a band-pass filter. (It is noted that EQ. 2 is referred to for illustrative purposes. This aspect of the invention is applicable to other transfer functions and other filter types.)

$$\frac{VO}{VI} = \frac{\alpha_1 z}{z^2 + \beta_1 z + \beta_0} \quad \text{EQ. 2}$$

It is possible to achieve amplification or attenuation by a factor K by scaling the numerator by K. K is a real number. Doing this for EQ. 2 yields the following:

$$\frac{VO}{VI} = \frac{K\alpha_1 z}{z^2 + \beta_1 z + \beta_0} \quad \text{EQ. 9}$$

Solving for VO yields the following:

$$VO = K\alpha_1 z^{-1} VI - \beta_1 z^{-1} VO - \beta_0 z^{-2} VO \quad \text{EQ. 10}$$

In embodiments of the invention, such amplification is achieved as specified by EQS. 9 and 10 by inserting a scaling module having a scale factor K in each feedforward path of the UDF module. Consider, for example, UDF module 1702 in FIG. 17. A scaling module 1790 having scale factor K is inserted into each feedforward path to thereby achieve an amplification or attenuation factor of K. The scaling modules 1790 may be electrically adjustable/tunable.

Alternatively, the scale factors of scaling modules 1716 are adjusted to incorporate the amplification/attenuation scale factor K. In such embodiments, the scale factors of the scaling modules 1716 affect both the filtering operation and the amplification/attenuation operation.

It is noted that this feature of the invention is optional. Where amplification is not required, the scaling modules 1790 can be omitted (or their scale factors can be set to 1).

The invention supports amplification adjustment. That is, the amplification achieved by the UDF module 1702 can be adjusted by adjusting the scale factors of the scaling modules 1716. Such amplification adjustment can be performed statically or dynamically, and can also be performed electronically.

Such adjustment can be manually controlled, or can be automatically controlled using a processor operating according to control modules that comprise software, a hardware state machine, etc., or a combination thereof. In some embodiments, the control modules operate according to user input and/or commands.

This amplification feature of the invention has been described in the context of the example UDF module 1702 of FIG. 17 for illustrative purposes only. The amplification feature as described herein is equally applicable to other UDF modules.

7 Example Applications

The following sections describe applications involving the UDF module of the present invention. The invention includes these applications. It should be understood that the invention is not limited to the particular applications described below. Equivalents, extensions, variations, deviations, etc., of the following will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. In particular, any application requiring the performance of at least a frequency translation operation and a frequency selectivity operation may utilize the UDF module described herein. Such applications are within the scope and spirit of the present invention.

7.1 Receiver

As noted above with reference to FIG. 8, a receiver performs three primary functions: frequency translation 808, frequency selection 810, and amplification 812.

Embodiments of the unified down-converting and filtering (UDF) module perform the frequency translation operation 808 and the frequency selection module 810. In some embodiments, the frequency selection operation 810 performed by the UDF module represents input filtering at any frequency, including RF and greater frequencies. Accordingly, such embodiments of the UDF module perform the primary functions of a receiver, except for amplification.

Therefore, it is possible to form a receiver in accordance with the present invention by combining the UDF module 1102 with an amplifier. This is shown in FIG. 30.

According to this receiver 3002, the UDF module 3006 performs unified frequency selection and conversion operations on an input signal 3004 in the manner described herein. The amplifier 3008 amplifies the output of the UDF module 1102 to thereby generate an output signal 3010. This operation of the receiver 3002 is represented in a flowchart 3102 in FIG. 31.

In some applications, the level of the output signal generated by the UDF module 3006 is sufficient for downstream processing. In such cases, an amplifier is not necessary. In this case, the embodiment of the UDF module 3006 shown in FIG. 30 (that performs frequency selection and translation, but not amplification) is sufficient to act as a receiver.

As noted above, some UDF embodiments also perform amplification. In such embodiments, the UDF module performs the primary functions of a receiver, i.e., frequency translation 808, frequency selection 810, and amplification 812. In such embodiments, the UDF module alone is sufficient to act as a receiver.

As will be apparent to persons skilled in the relevant art(s), the receiver 3002 can be implemented on an integrated circuit (IC). As discussed above, the UDF module can be implemented on an IC. Depending on the application, the UDF module performs most, if not all, of the functions required of a receiver. Accordingly, it follows that any receiver implemented using an embodiment of the UDF module can be implemented on an IC. Embodiments of the present invention are directed to such receivers implemented on an IC.

7.2 Other Application Examples

The applications described above are provided for purposes of illustration. These applications are not intended to limit the invention. Alternate applications, differing slightly or substantially from those described herein, will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such alternate applications fall within the scope and spirit of the present invention.

For example, and without limitation, UDF embodiments can be utilized in applications that involve filtering and frequency translation (in any combination or order), as illustrated in FIGS. 52A–52C. Also, UDF embodiments can be utilized in applications that involve filtering with or without down-conversion (in the latter case, the extent of frequency down-conversion by such UDF embodiments is minimized), as shown in FIG. 52D. Further, UDF embodiments can be utilized in applications that involve down-conversion with or without filtering (in the latter case, such UDF embodiments pass substantially all frequencies), as shown in FIG. 52E. Additionally, UDF embodiments can be utilized in applications that involve amplification or attenuation, as shown in FIG. 52F. It is noted that these features of the invention can be combined. Specifically, depending on the application, one or more of filtering, frequency translation, and amplification/attenuation can be arranged in desired combinations.

8 Conclusion

Example implementations of the systems and components of the invention have been described herein. As noted elsewhere, these example implementations have been described for illustrative purposes only, and are not limiting. Other implementation embodiments are possible and covered by the invention, such as but not limited to software and software/hardware implementations of the systems and

components of the invention. Such implementation embodiments will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

While various application embodiments of the present invention have been described above, it should be understood that they have been presented by way of example only, and not limitation. Thus, the breadth and scope of the present invention should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.

What is claimed is:

1. An apparatus for filtering and down-converting, comprising:

- (1) a frequency translator, comprising a down-convert and delay module to under-sample an input signal to produce an input sample of a down-converted image of said input signal, and to delay said input sample; and
- (2) a filter, comprising:
 - (a) at least a portion of said down-convert and delay module;
 - (b) at least one delay module to delay instances of an output signal; and
 - (c) an adder to combine at least said delayed input sample with at least one of said delayed instances of said output signal to generate an instance of said output signal;

wherein said down-convert and delay module under-samples said input signal according to a control signal, wherein a frequency of said control signal is equal to a frequency of said input signal plus or minus a frequency of said down-converted image, divided by n , where n represents a harmonic or sub-harmonic of said input signal.

2. The apparatus of claim 1, wherein said control signal comprises a train of pulses having pulse widths that are established to improve energy transfer from said input signal to said down-converted image.

3. The apparatus of claim 1, wherein said down-convert and delay module comprises a switch and a storage element, wherein a first node of said storage element is coupled to a node of said switch, and a second node of said storage element is coupled to a reference potential.

4. The apparatus of claim 1, wherein said down-convert and delay module comprises a switch and a storage element, wherein a first node of said switch is coupled to a node of said storage element, and a second node of said switch is coupled to a reference potential.

5. The apparatus of claim 1, wherein said frequency translator is at least partially integral with said filter.

6. An apparatus for filtering and down-converting, comprising:

- (1) a frequency translator, comprising:
 - (a) means for under-sampling an input signal to produce an input sample of a down-converted image of said input signal; and
 - (b) first delaying means for delaying said input sample; and
- (2) a filter, comprising:
 - (a) said first delaying means;
 - (b) second delaying means for delaying instances of an output signal; and
 - (c) means for combining at least said delayed input sample with at least one of said delayed instances of said output signal to generate an instance of said output signal;

wherein said under-sampling means under-samples said input signal according to a control signal, wherein a frequency of said control signal is equal to a frequency of said input signal plus or minus a frequency of said down-converted image, divided by n , where n represents a harmonic or sub-harmonic of said input signal.

7. An apparatus for filtering and down-converting, comprising:

a down-convert and delay module to under-sample an input signal to produce an input sample of a down-converted image of said input signal, and to delay said input sample;

at least one delay module to delay instances of an output signal; and

an adder to combine at least said delayed input sample with at least one of said delayed instances of said output signal to generate an instance of said output signal;

wherein said down-convert and delay module under-samples said input signal according to a control signal, wherein a frequency of said control signal is equal to a frequency of said input signal plus or minus a frequency of said down-converted image, divided by n , where n represents a harmonic or sub-harmonic of said input signal.

8. A method of filtering and down-converting, comprising the steps of:

- (1) under-sampling an input signal to produce input samples of a down-converted image of said input signal;
- (2) delaying said down-converted input samples; and
- (3) generating a down-converted and filtered output signal from at least said delayed and down-converted input samples and delayed instances of the output signal;

wherein step (1) comprises the step of:

under-sampling said input signal according to a control signal, wherein a frequency of said control signal is equal to a frequency of said input signal plus or minus a frequency of said down-converted image, divided by n , where n represents a harmonic or sub-harmonic of said input signal.

9. The method of claim 8, wherein step (1) comprises the step of:

under-sampling said input signal according to a control signal to produce said down-converted input samples.

10. The method of claim 9, further comprising the step of:

- (4) scaling said delayed and down-converted input samples and said delayed instances of the output signal; wherein step (3) comprises the step of generating said down-converted and filtered output signal from said scaled, delayed, and down-converted input samples and said scaled and delayed instances of the output signal.

11. The method of claim 10, further comprising the step of:

- (5) tuning one or more filter parameters.

12. The method of claim 11, wherein step (5) comprises the step of:

tuning at least one of a filter center frequency, a filter bandwidth, and a filter passband.

13. The method of claim 11, wherein step (5) comprises the step of:

performing at least one of steps (i) and (ii) to tune said one or more filter parameters:

- (i) adjusting at least one scale factor; and
- (ii) adjusting one or more characteristics of said control signal.

14. The method of claim 8, further comprising the step of:
 (4) tuning at least one frequency translation parameters.
15. The method of claim 8, further comprising the step of:
 (4) amplifying said output signal.
16. The method of claim 15, wherein step (4) comprises the step of:
 scaling at least one of said delayed and down-converted input samples and delayed instances of the output signal to achieve amplification.
17. The method of claim 8, wherein step (2) is at least partially integral with step (1).
18. The method of claim 8, wherein said control signal comprises a train of pulses having pulse widths that are established to improve energy transfer from said input signal to said down-converted image.
19. A method of filtering and down-converting, comprising the steps of:
 (1) filtering and down-converting an input signal in an integrated manner, and
 (2) tuning at least one of said filtering operation and said down-converting operation of step (1);
 wherein step (1) comprises the step of:
 under-sampling said input signal according to a control signal, wherein a frequency of said control signal is equal to a frequency of said input signal plus or minus a frequency of a down-converted image, divided by n , where n represents a harmonic or sub-harmonic of said input signal.
20. The method of claim 19, wherein step (2) comprises the step of:
 tuning at least one of a filter center frequency, a filter bandwidth, and a filter passband.
21. The method of claim 19, wherein step (2) comprises the step of:
 performing at least one of steps (i) and (ii) to tune said one or more filtering parameters:
 (i) adjusting at least one scale factor; and
 (ii) adjusting one or more characteristics of a control signal.
22. The method of claim 21, further comprising the step of:
 (3) amplifying an output signal resulting from said filtering and down-converting operations of step (1), comprising the step of modifying said at least one scale factor.
23. The method of claim 19, wherein step (2) comprises the step of:
 dynamically tuning said one or more parameters of said filtering operation of step (1).
24. The method of claim 19, further comprising the step of:
 (3) tuning at least one frequency translation parameter.
25. The method of claim 24, wherein step (3) comprises the step of:
 adjusting one or more characteristics of a control signal.
26. The method of claim 19, wherein said down-converting operation is performed so as to improve energy transfer from said input signal to a down-converted image.
27. The method of claim 19, wherein said filtering operation effectively represents input filtering, and said input signal is a radio frequency (RF) signal.
28. An apparatus to filter and down-convert, comprising:
 an integral filter/frequency translator to filter and down-convert an input signal; and
 a module to tune at least one of said filtering operation and said down-conversion operations;

- wherein said integral filter/frequency translator under-samples said input signal according to a control signal, wherein a frequency of said control signal is equal to a frequency of said input signal plus or minus a frequency of a down-converted image, divided by n , where n represents a harmonic or sub-harmonic of said input signal.
29. The apparatus of claim 28, wherein said filtering operation effectively represents input filtering, and said input signal is a radio frequency (RF) signal.
30. A method of filtering and down-converting, comprising the steps of:
 (1) filtering and down-converting an input signal in an integrated manner, comprising at least adjusting scale factors; and
 (2) amplifying an output signal resulting from said filtering and down-converting operations of step (1), comprising the step of modifying said scale factors to achieve a desired amplification level;
 wherein step (1) comprises the step of:
 under-sampling said input signal according to a control signal, wherein a frequency of said control signal is equal to a frequency of said input signal plus or minus a frequency of a down-converted image, divided by n , where n represents a harmonic or sub-harmonic of said input signal.
31. The method of claim 30, wherein step (1) comprises the steps of:
 (a) under-sampling said input signal to produce input samples of a down-converted image of said input signal;
 (b) delaying said down-converted input samples; and
 (c) generating a down-converted and filtered output signal from said delayed and down-converted input samples and delayed instances of the output signal.
32. The method of claim 31, wherein step (a) comprises the step of:
 under-sampling said input signal according to a control signal to produce said down-converted input samples.
33. The method of claim 32, wherein said control signal is established to improve energy transfer from said input signal to said down-converted image.
34. An apparatus to filter and down-convert, comprising:
 (1) a frequency translator to produce a sample of a down-converted image of an input signal, and to delay said sample; and
 (2) a filter, comprising:
 (a) at least a portion of said frequency translator;
 (b) at least one delay module to delay an output signal; and
 (c) an adder to combine at least said delayed sample with at least a portion of said delayed output signal to generate at least a part of said output signal;
 wherein said frequency translator under-samples said input signal according to a control signal, wherein a frequency of said control signal is equal to a frequency of said input signal plus or minus a frequency of said down-converted image, divided by n , where n represents a harmonic or sub-harmonic of said input signal.
35. The method of claim 8 wherein filtering of steps (1)–(3) comprises narrow band filtering.
36. The method of claim 35, wherein filtering of steps (1)–(3) comprises channel select filtering.
37. The method of claim 36, wherein said input signal is a radio frequency (RF) signal.

38. The method of claim 36, wherein said input signal comprises a frequency greater than a radio frequency (RF).
39. The method of claim 36, wherein said input signal comprises a frequency less than a radio frequency (RF).
40. The method of claim 8, wherein filtering of steps (1)-(3) comprises wide band filtering.
41. The method of claim 8, wherein said input signal comprises a frequency greater than or equal to a radio frequency (RF).
42. The method of claim 8, further comprising the step of: receiving said input signal via a communication medium.
43. The method of claim 42, wherein said communication medium comprises a wired medium.
44. The method of claim 42, wherein said communication medium comprises a wireless medium.
45. The method of claim 8, wherein said input signal is an unmodulated signal.
46. The method of claim 8, wherein said input signal is a modulated signal.
47. The method of claim 46, wherein said input signal is one of an amplitude modulated signal, a frequency modulated signal, or a phase modulated signal.
48. The method of claim 8 wherein filtering of steps (1)-(3) comprises at least one of: (a) band pass filtering; (b) low pass filtering; (c) high pass filtering; (d) notch filtering; (e) all pass filtering; and (f) band stop filtering.
49. The method of claim 8, wherein steps (1)-(3) are performed such that said input signal is effectively filtered prior to being down-converted.
50. The method of claim 49, wherein filtering of steps (1)-(3) comprises narrow band filtering.
51. The method of claim 50, wherein filtering of steps (1)-(3) comprises channel select filtering.
52. The method of claim 50, wherein said input signal comprises a frequency greater than or equal to a radio frequency (RF).
53. The method of claim 8, further comprising the step of: (4) tuning one or more filter parameters.
54. The method of claim 53, wherein said filter parameters are statically or dynamically tuned.
55. The method of claim 53, wherein said filter parameters are electrically tuned.
56. The method of claim 53, wherein step (4) comprises the step of: tuning at least one of a filter center frequency, a filter bandwidth, and a filter passband.
57. The method of claim 53, wherein step (4) comprises the step of: performing at least one of steps (i) and (ii) to tune said one or more filter parameters: (i) adjusting at least one scale factor; and (ii) adjusting one or more characteristics of said control signal.
58. The method of claim 8, further comprising the step of: (4) tuning one or more frequency translation parameters.
59. The method of claim 8, wherein in step (1) each input sample represents a portion of said down-converted image of said input signal, wherein step (2) comprises delaying said each input sample, and step (3) comprises combining said delayed each input sample with at least one delayed instance of the output signal, at least steps (1) and (2) operating to down-convert said input signal, and at least steps (2) and (3) operating to filter said input signal.
60. The method of claim 8, further comprising the steps of: (4) further delaying one or more of said delayed and down-converted input samples;

- wherein step (3) comprises the step of generating a down-converted and filtered output signal from at least one or more of said delayed and down-converted input samples, said further delayed and down-converted input samples, and delayed instances of the output signal.
61. The method of claim 8, further comprising the steps of: (4) delaying instances of the output signal; (5) further delaying one or more of said delayed output signal instances; wherein step (3) comprises the step of generating a down-converted and filtered output signal from at least one or more of said delayed and down-converted input samples, said delayed instances of the output signal, and said further delayed output signal instances.
62. The method of claim 8, further comprising the steps of: (4) scaling one or more of said delayed and down-converted input samples; wherein step (3) comprises the step of generating a down-converted and filtered output signal from at least one or more of said delayed and down-converted input samples, said scaled, delayed and down-converted input samples, and delayed instances of the output signal.
63. The method of claim 8, further comprising the steps of: (4) scaling one or more of said delayed instance of the output signal; wherein step (3) comprises the step of generating a down-converted and filtered output signal from at least one or more of said delayed and down-converted input samples, said delayed instances of the output signal, and said scaled and delayed instances of the output signal.
64. The method of claim 8, further comprising the steps of: (4) further delaying one or more of said delayed and down-converted input samples; (5) scaling one or more of said delayed and down-converted input samples and one or more of said further delayed and down-converted input samples; (6) delaying instances of the output signal; (7) further delaying one or more of said delayed output signal instances; (8) scaling one or more of said delayed instances of the output signal and one or more of said further delayed instances of the output signal; wherein step (3) comprises the step of generating a down-converted and filtered output signal from at least a plurality of said delayed and down-converted input samples, said scaled, delayed and down-converted input samples, said scaled further delayed and down-converted input samples, said delayed instances of the output signal, said scaled delayed instances of the output signal, said further delayed instances of the output signal, and said scaled further delayed instances of the output signal.
65. The method of claim 66, wherein step (3) comprises the step of generating a down-converted and filtered output signal by combining at least said delayed and down-converted input samples, said scaled, delayed and down-converted input samples, said further delayed and down-

converted input samples, said scaled further delayed and down-converted input samples, said delayed instances of the output signal, said scaled delayed instances of the output signal, said further delayed instances of the output signal, and said scaled further delayed instances of the output signal.

66. The method of claim 64, wherein scale factors of steps (5) and (8) are real numbers.

67. The method of claim 66, wherein said scale factors are established to provide amplification.

68. The method of claim 66, wherein said scale factors are established to at least assist in setting at least one of: a filter parameter, and a frequency translation parameter.

69. The method of claim 68, wherein characteristics of said control signal are established to at least assist in setting at least one of: a filter parameter; and a frequency translation parameter.

70. The method of claim 69, wherein at least one of said scale factors and characteristics of said control signal are electrically tuned.

71. The method of claim 69, wherein at least one of said scale factors and characteristics of said control signal are dynamically adjusted.

72. The method of claim 69, wherein at least one of said scale factors and characteristics of said control signal are statically adjusted.

73. The method of claim 8, wherein delay factors are established according to a selected filter transfer function.

74. The method of claim 8, wherein step (2) comprises the step of delaying an input sample by one time unit, and further comprising the steps of:

(4) delaying an instance of the output signal by one time unit; and

(5) delaying said one time unit delayed output signal instance by an additional time unit;

wherein step (3) comprises the step of generating a portion of a down-converted and filtered output signal from at least said one time unit delayed input sample, said one time unit delayed output signal instance, and said additional time unit delayed output signal instance.

75. The method of claim 74, further comprising the step of:

(6) scaling said one time unit delayed input sample, said one time unit delayed output signal instance, and said additional time unit delayed output signal instance;

wherein step (3) comprises the step of generating a portion of a down-converted and filtered output signal from at least one or more of said scaled one time unit delayed input sample, said scaled one time unit delayed output signal instance, and said scaled additional time unit delayed output signal instance.

76. The method of claim 75, wherein scale factors of step (6) are real numbers.

77. The method of claim 76, wherein steps (1)–(5) operate to band pass filter said input signal.

78. The method of claim 76, further comprising the step of:

(6) sampling and holding said output signal.

79. The method of claim 76, further comprising the step of:

(6) smoothing said output signal.

80. The method of claim 8, wherein step (2) comprises the step of delaying an input sample by one time unit, and further comprising the steps of:

(4) delaying said one time unit delayed input sample by an additional time unit;

(5) delaying an instance of the output signal by one time unit; and

(6) delaying said one time unit delayed output signal instance by an additional time unit;

wherein step (3) comprises the step of generating a portion of a down-converted and filtered output signal from at least one or more of said additional time unit delayed input sample, said one time unit delayed output signal instance, and said additional time unit delayed output signal instance.

81. The method of claim 80, further comprising the step of:

(7) scaling one or more of said additional time unit delayed input sample, said one time unit delayed output signal instance, and said additional time unit delayed output signal instance;

wherein step (3) comprises the step of generating a portion of a down-converted and filtered output signal from at least said scaled additional time unit delayed input sample, said scaled one time unit delayed output signal instance, and said scaled additional time unit delayed output signal instance.

82. The method of claim 81, wherein scale factors of step (7) are real numbers.

83. The method of claim 80, wherein steps (1)–(6) operate to low pass filter said input signal.

84. The method of claim 8, wherein said frequency of said down-converted image is substantially equal to zero.

85. The method of claim 8, wherein said frequency of said down-converted image is equal to an intermediate frequency.

86. The method of claim 8, wherein step (1) comprises the step of:

(a) generating an energy transfer signal comprising a train of pulses, said pulses controlling opening and closing of a switch to transfer energy from said input signal.

87. The method of claim 86, wherein step (a) comprises the step of establishing apertures of said pulses to increase the time that said switch is closed for a purpose of reducing an impedance of said switch.

88. The method of claim 86, wherein step (a) comprises the step of widening apertures of said pulses of said energy transfer signal by a non-negligible amount that tends away from zero time in duration to extend the time that said switch is closed for a purpose of increasing energy transferred from said input signal.

89. The method of claim 88, wherein said apertures of said pulses of said energy transfer signal are one of (I) or (II):

(I) a non-zero fraction of a period of said input signal; or
(II) one or more periods of said input signal plus or minus a non-zero fraction of a period of said input signal.

90. The method of claim 88, wherein energy transferred from said input signal is sufficient to drive loads without additional buffering or amplification, including high impedance loads and low impedance loads.

91. The method of claim 88, wherein widening of said apertures of said pulses by a non-negligible amount that tends away from zero time in duration to extend the time that said switch is closed for a purpose of increasing energy transferred from said input signal prevents substantial voltage reproduction of said input signal.

92. The method of claim 8, further comprising the step of: matching an impedance of said switch to a source impedance to increase energy transferred from said input signal.

93. The method of claim 8, further comprising the step of: matching an impedance of said switch to a load impedance to increase energy transferred from said input signal.
94. The method of claim 8, further comprising the step of: 5
transferring said input signal to said switch via a resonant circuit, said resonant circuit storing energy from components of said input signal while said switch is open, and wherein energy stored in said resonant circuit is discharged via said switch while said switch is closed, 10
to thereby increase energy transfer from said input signal.
95. The method of claim 94, wherein said resonant circuit is configured to appear as high impedance to a first range of frequencies including a frequency of said input signal, and configured to appear as a low impedance to a second range of frequencies including a frequency of said output signal, such that passage of components of said input signal in said first range of frequencies is impeded through said resonant circuit, and such that passage of components of said input signal in said second range of frequencies is not so impeded through said resonant circuit.
96. The method of claim 8, wherein step (1) comprises the step of: 15
(a) generating an energy transfer signal comprising a train of pulses, said pulses controlling opening and closing of a switch to transfer energy from said input signal; wherein step (a) comprises the step of establishing apertures of said pulses to increase the time that said switch is closed for a purpose of reducing an impedance of said switch; 20
wherein step (a) comprises the step of widening apertures of said pulses of said energy transfer signal by a non-negligible amount that tends away from zero time in duration to extend the time that said switch is closed for a purpose of increasing energy transferred from said input signal; 25
wherein said apertures of said pulses of said energy transfer signal are one of (I) or (II):
(I) a non-zero fraction of a period of said input signal; or
(II) one or more periods of said input signal plus or minus a non-zero fraction of a period of said input signal; 30
wherein energy transferred from said input signal is sufficient to drive loads without additional buffering or amplification, including high impedance loads and low impedance loads; and
wherein widening of said apertures of said pulses by a non-negligible amount that tends away from zero time in duration to extend the time that said switch is closed for a purpose of increasing energy transferred from said input signal prevents substantial voltage reproduction of said input signal.
97. The method of claim 96, further comprising the step of: 35
matching an impedance of said switch to a source impedance to increase energy transferred from said input signal.
98. The method of claim 96, further comprising the step of: 40
matching an impedance of said switch to a load impedance to increase energy transferred from said input signal.
99. The method of claim 96, further comprising the step of: 45

- transferring said input signal to said switch via a resonant circuit, said resonant circuit storing energy from components of said input signal while said switch is open, and wherein energy stored in said resonant circuit is discharged via said switch while said switch is closed, to thereby increase energy transfer from said input signal.
100. The method of claim 99, wherein said resonant circuit is configured to appear as high impedance to a first range of frequencies including a frequency of said input signal, and configured to appear as a low impedance to a second range of frequencies including a frequency of said output signal, such that passage of components of said input signal in said first range of frequencies is impeded through said resonant circuit, and such that passage of components of said input signal in said second range of frequencies is not so impeded through said resonant circuit.
101. The apparatus of claim 1, wherein said down-convert and delay module comprises a universal frequency translation (UFT) module.
102. The apparatus of claim 1, wherein said down-convert and delay module comprises an aliasing module.
103. The apparatus of claim 1, wherein said frequency of said down-converted image is substantially equal to zero.
104. The apparatus of claim 1, wherein said frequency of said down-converted image is equal to an intermediate frequency.
105. The apparatus of claim 1, wherein said down-convert and delay module comprises: 50
a switch; and
a storage module electrically coupled to said switch.
106. The apparatus of claim 105, further comprising: 55
an energy transfer signal generator that generates an energy transfer signal comprising a train of pulses.
107. The apparatus of claim 106, wherein said energy transfer signal generator establishes apertures of said pulses to increase the time that said switch is closed for a purpose of reducing an impedance of said switch.
108. The apparatus of claim 106, wherein said energy transfer signal generator establishes apertures of said pulses, said apertures being one of (I) or (II): 60
(I) a non-zero fraction of a period of said input signal; or
(II) one or more periods of said input signal plus or minus a non-zero fraction of a period of said input signal.
109. The apparatus of claim 106, wherein said energy transfer signal generator widens apertures of said pulses of said energy transfer signal by a non-negligible amount that tends away from zero time in duration to extend the time that said switch is closed for a purpose of increasing energy transferred from said input signal.
110. The apparatus of claim 109, wherein energy transferred from said input signal is sufficient to drive loads without additional buffering or amplification, including high impedance loads and low impedance loads.
111. The apparatus of claim 109, wherein said energy transfer signal generator in widening said apertures of said pulses by a non-negligible amount that tends away from zero time in duration to extend the time that said switch is closed for the purpose of increasing energy transferred from said input signal does so at the expense of reproducing said input signal, such that said increased energy transferred from said input signal when said switch is closed in response to said energy transfer signal prevents substantial voltage reproduction of said input signal.
112. The apparatus of claim 105, further comprising energy transfer optimization circuitry comprising one or more of (i), (ii), and (iii): 65

- (i) an input impedance matching circuit, electrically coupled to said switch, that matches a source impedance to an impedance of said switch so as to increase energy transferred from said input signal to said storage module via said switch when said switch is closed in response to said energy transfer signal;
 - (ii) an output impedance matching circuit, electrically coupled to said switch, that matches a load impedance to an impedance of said switch so as to increase energy discharged from said storage module to a load when said switch is open in response to said energy transfer signal; and
 - (iii) a resonant circuit coupled between said switch and a source of said input signal, wherein said resonant circuit stores energy from components of said input signal while said switch is open in response to said energy transfer signal, and wherein energy stored in said resonant circuit is discharged to said storage module via said switch while said switch is closed in response to said energy transfer signal, said storage module being of a size sufficient to accommodate energy transferred via said switch including energy discharged from said resonant circuit.
113. The apparatus of claim 112, wherein said resonant circuit is configured to appear as high impedance to a first range of frequencies including a frequency of said input signal, and configured to appear as a low impedance to a second range of frequencies including a frequency of said output signal, such that passage of components of said input signal in said first range of frequencies is impeded through said resonant circuit, and such that passage of components of said input signal in said second range of frequencies is not so impeded through said resonant circuit.
114. The apparatus of claim 105, wherein said storage module stores energy transferred via said switch, including energy transferred from said input signal via said switch when said switch is closed in response to said energy transfer signal.
115. The apparatus of claim 114, wherein said storage module is of a size sufficient to accommodate energy transferred via said switch, including energy transferred from said input signal via said switch when said switch is closed in response to said energy transfer signal.
116. The apparatus of claim 1, wherein said filter performs narrow band filtering.
117. The apparatus of claim 1, wherein said filter performs channel select filtering.
118. The apparatus of claim 1, wherein said input signal is a radio frequency (RF) signal.
119. The apparatus of claim 117, wherein said input signal comprises a frequency greater than a radio frequency (RF).
120. The apparatus of claim 117, wherein said input signal comprises a frequency less than a radio frequency (RF).
121. The apparatus of claim 1, wherein said filter performs wide band filtering.
122. The apparatus of claim 1, wherein said input signal comprises a frequency greater than or equal to a radio frequency (RF).
123. The apparatus of claim 1, wherein said input signal is received via a communication medium.
124. The apparatus of claim 123, wherein said communication medium comprises a wired medium.
125. The apparatus of claim 123, wherein said communication medium comprises a wireless medium.
126. The apparatus of claim 1, wherein said input signal is an unmodulated signal.
127. The apparatus of claim 1, wherein said input signal is a modulated signal.

128. The apparatus of claim 127, wherein said input signal is one of an amplitude modulated signal, a frequency modulated signal, or a phase modulated signal.
129. The apparatus of claim 1, wherein said filter performs at least one of: (a) band pass filtering; (b) low pass filtering; (c) high pass filtering; (d) notch filtering; (e) all pass filtering; and (f) band stop filtering.
130. The apparatus of claim 1, wherein said frequency translator and said filter operate such that said input signal is effectively filtered prior to being down-converted.
131. The apparatus of claim 130, wherein said filter performs narrow band filtering.
132. The apparatus of claim 131, wherein said filter performs channel select filtering.
133. The apparatus of claim 131, wherein said input signal comprises a frequency greater than or equal to a radio frequency (RF).
134. The apparatus of claim 1, further comprising: filter tuning means for tuning one or more filter parameters.
135. The apparatus of claim 134, wherein said filter parameters are statically or dynamically tuned.
136. The apparatus of claim 134, wherein said filter parameters are electrically tuned.
137. The apparatus of claim 134, wherein at least one of a filter center frequency, a filter bandwidth, and a filter passband is tuned.
138. The apparatus of claim 134, wherein said filter tuning means comprises:
- means for adjusting at least one scale factor or one or more characteristics of said control signal.
139. The apparatus of claim 1, further comprising: means for tuning one or more frequency translation parameters.
140. The apparatus of claim 1, further comprising: one or more additional delay modules to further delay one or more of said delayed and down-converted input samples;
- wherein said adder generates a portion of an output signal from at least said delayed and down-converted input samples, said further delayed and down-converted input samples, and delayed instances of the output signal.
141. The apparatus of claim 1, further comprising the steps of:
- one or more additional delay modules to further delay one or more of said delayed output signal instances;
 - wherein said adder generates a portion of an output signal from at least said delayed and down-converted input samples, said delayed instances of the output signal, and said further delayed output signal instances.
142. The apparatus of claim 1, further comprising: one or more scale modules to scale one or more of said delayed and down-converted input samples;
- wherein said adder generates a portion of an output signal from at least said delayed and down-converted input samples, said scaled, delayed and down-converted input samples, and delayed instances of the output signal.
143. The apparatus of claim 1, further comprising: one or more scale modules to scale one or more of said delayed instances of the output signal;
- wherein said adder generates a portion of an output signal from at least said delayed and down-converted input samples, said delayed instances of the output signal, and said scaled and delayed instances of the output signal.

144. The apparatus of claim 1, further comprising:
 one or more additional delay modules to further delay at
 least one of said delayed and down-converted input
 samples and said delayed output signal instances;
 one or more scale modules to scale at least one of said
 delayed and down-converted input samples, said further
 delayed and down-converted input samples, said
 delayed instances of the output signal, and said further
 delayed instances of the output signal;
 wherein said adder generates a portion of an output signal
 from at least a plurality of said delayed and down-
 converted input samples, said scaled, delayed and
 down-converted input samples, said further delayed
 and down-converted input samples, said scaled further
 delayed and down-converted input samples, said
 delayed instances of the output signal, said scaled
 delayed instances of the output signal, said further
 delayed instances of the output signal, and said scaled
 further delayed instances of the output signal.

145. The apparatus of claim 144, wherein scale factors of
 said scale modules are real numbers.

146. The apparatus of claim 145, wherein said scale
 factors are established to provide amplification.

147. The apparatus of claim 145, wherein said scale
 factors are established to at least assist in setting at least one
 of: a filter parameter; and a frequency translation parameter.

148. The apparatus of claim 147, wherein characteristics
 of said control signal are established to at least assist in
 setting at least one of: a filter parameter, and a frequency
 translation parameter.

149. The apparatus of claim 148, wherein at least one of
 said scale factors and characteristics of said control signal
 are electrically tuned.

150. The apparatus of claim 148, wherein at least one of
 said scale factors and characteristics of said control signal
 are dynamically adjusted.

151. The apparatus of claim 148, wherein at least one of
 said scale factors and characteristics of said control signal
 are statically adjusted.

152. The apparatus of claim 1, wherein delay factors are
 established according to a selected filter transfer function.

153. The apparatus of claim 1, wherein said down-convert
 and delay module delays an input sample by one time unit,
 and wherein said delay module delays an output signal
 instance by one time unit, and further comprising:

at least one additional delay module to delay said one time
 unit delayed output signal instance by an additional
 time unit;

wherein said adder generates a portion of an output signal
 from at least said one time unit delayed input sample,
 said one time unit delayed output signal instance, and
 said additional time unit delayed output signal instance.

154. The apparatus of claim 153, further comprising:
 at least one scale module to scale at least one of said one
 time unit delayed input sample, said one time unit
 delayed output signal instance, and said additional time
 unit delayed output signal instance;

wherein said adder generates a portion of an output signal
 from at least said scaled one time unit delayed input
 sample, said scaled one time unit delayed output signal
 instance, and said scaled additional time unit delayed
 output signal instance.

155. The apparatus of claim 154, wherein scale factors of
 said scale module are real numbers.

156. The apparatus of claim 153, wherein said filter
 operates to band pass filter said input signal.

157. The apparatus of claim 153, further comprising:
 an output smoothing module.

158. The apparatus of claim 1, wherein said down-convert
 and delay module delays an input sample by one time unit,
 and wherein said delay module delays an output signal
 instance by one time unit, and further comprising:

a first additional delay module to delay said one time unit
 delayed input sample by an additional time unit;

a second additional delay module to delay said one time
 unit delayed output signal instance by an additional
 time unit;

wherein said adder generates a portion of an output signal
 from at least said additional time unit delayed input
 sample, said one time unit delayed output signal
 instance, and said additional time unit delayed output
 signal instance.

159. The apparatus of claim 158, further comprising:

at least one scale module to scale at least one of said
 additional time unit delayed input sample, said one
 time unit delayed output signal instance, and said
 additional time unit delayed output signal instance;

wherein said adder generates a portion of an output signal
 from at least said scaled additional time unit delayed
 input sample, said scaled one time unit delayed output
 signal instance, and said scaled additional time unit
 delayed output signal instance.

160. The apparatus of claim 159, wherein scale factors of
 said scale module are real numbers.

161. The apparatus of claim 158, wherein said filter
 operates to low pass filter said input signal.

162. The apparatus of claim 6, wherein said frequency
 translator comprises a universal frequency translation (UFT)
 module.

163. The apparatus of claim 6, wherein said frequency of
 said down-converted image is one of: (i) substantially equal
 to zero; or (ii) equal to an intermediate frequency.

164. The apparatus of claim 6, wherein said frequency
 translator comprises:

a switch; and

a storage module electrically coupled to said switch.

165. The apparatus of claim 164, further comprising:

an energy transfer signal generator that generates an
 energy transfer signal comprising a train of pulses, said
 pulses controlling opening and closing of said switch,
 said energy transfer signal generator establishing aper-
 tures of said pulses to increase the time that said switch
 is closed to reduce an impedance of said switch, and to
 increase energy transferred from said input signal.

166. The apparatus of claim 164, further comprising
 energy transfer optimization circuitry that increases energy
 transferred from said input signal, said energy transfer
 optimization circuitry comprising one or more of (i), (ii),
 and (iii):

(i) an input impedance matching circuit, electrically
 coupled to said switch, that matches a source imped-
 ance to an impedance of said switch so as to increase
 energy transferred from said input signal to said storage
 module via said switch when said switch is closed in
 response to said energy transfer signal;

(ii) an output impedance matching circuit, electrically
 coupled to said switch, that matches a load impedance
 to an impedance of said switch so as to increase energy
 discharged from said storage module to a load when
 said switch is open in response to said energy transfer
 signal; and

(iii) a resonant circuit coupled between said switch and a source of said input signal, wherein said resonant circuit stores energy from components of said input signal while said switch is open in response to said energy transfer signal, and wherein energy stored in said resonant circuit is discharged to said storage module via said switch while said switch is closed in response to said energy transfer signal, said storage module being of a size sufficient to accommodate energy transferred via said switch including energy discharged from said resonant circuit.

167. The apparatus of claim 166, wherein said resonant circuit is configured to appear as high impedance to a first range of frequencies including a frequency of said input signal, and configured to appear as a low impedance to a second range of frequencies including a frequency of said output signal, such that passage of components of said input signal in said first range of frequencies is impeded through said resonant circuit, and such that passage of components of said input signal in said second range of frequencies is not so impeded through said resonant circuit.

168. The apparatus of claim 164, wherein said storage module is of a size sufficient to accommodate energy transferred via said switch, including said increased energy transferred from said input signal via said switch when said switch is closed in response to said energy transfer signal.

169. The apparatus of claim 6, wherein said frequency translator and said filter operate such that said input signal is effectively filtered prior to being down-converted.

170. The apparatus of claim 169, wherein said filter performs narrow band filtering.

171. The apparatus of claim 170, wherein said input signal comprises a frequency greater than or equal to a radio frequency (RF).

172. The apparatus of claim 6, further including means for tuning one or more filter and frequency translation parameters.

173. The apparatus of claim 7, wherein said down-convert and delay module comprises a universal frequency translation (UFT) module.

174. The apparatus of claim 7, wherein said frequency of said down-converted image is one of: (i) substantially equal to zero; or (ii) equal to an intermediate frequency.

175. The apparatus of claim 7, wherein said down-convert and delay module comprises:

a switch; and

a storage module electrically coupled to said switch.

176. The apparatus of claim 175, further comprising:

an energy transfer signal generator that generates an energy transfer signal comprising a train of pulses, said pulses controlling opening and closing of said switch, said energy transfer signal generator establishing apertures of said pulses to increase the time that said switch is closed to reduce an impedance of said switch, and to increase energy transferred from said input signal.

177. The apparatus of claim 175, further comprising energy transfer optimization circuitry that increases energy transferred from said input signal, said energy transfer optimization circuitry comprising one or more of (i), (ii), and (iii):

(i) an input impedance matching circuit, electrically coupled to said switch, that matches a source impedance to an impedance of said switch so as to increase energy transferred from said input signal to said storage module via said switch when said switch is closed in response to said energy transfer signal;

(ii) an output impedance matching circuit, electrically coupled to said switch, that matches a load impedance

to an impedance of said switch so as to increase energy discharged from said storage module to a load when said switch is open in response to said energy transfer signal; and

(iii) a resonant circuit coupled between said switch and a source of said input signal, wherein said resonant circuit stores energy from components of said input signal while said switch is open in response to said energy transfer signal, and wherein energy stored in said resonant circuit is discharged to said storage module via said switch while said switch is closed in response to said energy transfer signal, said storage module being of a size sufficient to accommodate energy transferred via said switch including energy discharged from said resonant circuit.

178. The apparatus of claim 177, wherein said resonant circuit is configured to appear as high impedance to a first range of frequencies including a frequency of said input signal, and configured to appear as a low impedance to a second range of frequencies including a frequency of said output signal, such that passage of components of said input signal in said first range of frequencies is impeded through said resonant circuit, and such that passage of components of said input signal in said second range of frequencies is not so impeded through said resonant circuit.

179. The apparatus of claim 175, wherein said storage module is of a size sufficient to accommodate energy transferred via said switch, including said increased energy transferred from said input signal via said switch when said switch is closed in response to said energy transfer signal.

180. The apparatus of claim 7, wherein said down-convert and delay module, said at least one delay module, and said adder operate such that said input signal is effectively filtered prior to being down-converted.

181. The apparatus of claim 180, wherein said down-convert and delay module, said at least one delay module, and said adder perform narrow band filtering.

182. The apparatus of claim 181, wherein said input signal comprises a frequency greater than or equal to a radio frequency (RF).

183. The apparatus of claim 7, further including means for tuning one or more filter and frequency translation parameters.

184. The apparatus of claim 34, wherein said frequency translator comprises a universal frequency translation (UFT) module.

185. The apparatus of claim 34, wherein said frequency of said down-converted image is one of: (i) substantially equal to zero; or (ii) equal to an intermediate frequency.

186. The apparatus of claim 34, wherein said frequency translator comprises:

a switch; and

a storage module electrically coupled to said switch.

187. The apparatus of claim 183, further comprising:

an energy transfer signal generator that generates an energy transfer signal comprising a train of pulses, said pulses controlling opening and closing of said switch, said energy transfer signal generator establishing apertures of said pulses to increase the time that said switch is closed to reduce an impedance of said switch, and to increase energy transferred from said input signal.

188. The apparatus of claim 186, further comprising energy transfer optimization circuitry that increases energy transferred from said input signal, said energy transfer optimization circuitry comprising one or more of (i), (ii), and (iii):

(i) an input impedance matching circuit, electrically coupled to said switch, that matches a source imped-

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ance to an impedance of said switch so as to increase energy transferred from said input signal to said storage module via said switch when said switch is closed in response to said energy transfer signal;

- (ii) an output impedance matching circuit, electrically coupled to said switch, that matches a load impedance to an impedance of said switch so as to increase energy discharged from said storage module to a load when said switch is open in response to said energy transfer signal; and
- (iii) a resonant circuit coupled between said switch and a source of said input signal, wherein said resonant circuit stores energy from components of said input signal while said switch is open in response to said energy transfer signal, and wherein energy stored in said resonant circuit is discharged to said storage module via said switch while said switch is closed in response to said energy transfer signal, said storage module being of a size sufficient to accommodate energy transferred via said switch including energy discharged from said resonant circuit.

189. The apparatus of claim **188**, wherein said resonant circuit is configured to appear as high impedance to a first range of frequencies including a frequency of said input signal, and configured to appear as a low impedance to a

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second range of frequencies including a frequency of said output signal, such that passage of components of said input signal in said first range of frequencies is impeded through said resonant circuit, and such that passage of components of said input signal in said second range of frequencies is not so impeded through said resonant circuit.

190. The apparatus of claim **186**, wherein said storage module is of a size sufficient to accommodate energy transferred via said switch, including said increased energy transferred from said input signal via said switch when said switch is closed in response to said energy transfer signal.

191. The apparatus of claim **34**, wherein said frequency translator and said filter operate such that said input signal is effectively filtered prior to being down-converted.

192. The apparatus of claim **191**, wherein said filter performs narrow band filtering.

193. The apparatus of claim **192**, wherein said input signal comprises a frequency greater than or equal to a radio frequency (RF).

194. The apparatus of claim **34**, further including means for tuning one or more filter and frequency translation parameters.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,049,706
DATED : April 11, 2000
INVENTOR(S) : Cook et al.

Page 1 of 4

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 1,

Line 6, please replace "applications" with -- patents and patent applications --.

Lines 10-17, please replace with the following:

-- "Method and System for Down-Converting Electromagnetic Signals," Ser. No. 09/176,022, Attorney Docket No. 1744.0010000, now U.S. Patent No. 6,061,551, issued May 9, 2000.

"Method and System for Frequency Up-Conversion," Ser. No. 09/176,154, Attorney Docket No. 1744.0020000, now allowed.

"Method and System for Ensuring Reception of a Communications Signal," Ser. No. 09/176,415, Attorney Docket No. 1744.0030000, now U.S. Patent No. 6,061,555, issued May 9, 2000.

"Universal Frequency Translation, and Applications of Same," Ser. No. 09/176,027, Attorney Docket No. 1744.0140000, now abandoned. --

Column 28,

Lines 33-35, please replace with -- "Method and System for Down-Converting Electromagnetic Signals," Ser. No. 09/176,022, filed October 21, 1998, Attorney Docket No. 1744.0010000, now U.S. Patent No. 6,061,551, issued May 9, 2000, --.

Line 36, please delete "1744.0010000,".

Line 38, please delete "application".

Column 29,

Lines 43-46, please replace with -- "Method and System for Down-Converting Electromagnetic Signals," Ser. No. 09/176,022, filed October 21, 1998, Attorney Docket No. 1744.0010000, now U.S. Patent No. 6,061,551, issued May 9, 2000. --.

Column 30,

Line 7, please delete "co-pending U.S. Patent".

Lines 8-10, please replace with -- "Method and System for Down-Converting Electromagnetic Signals," Ser. No. 09/176,022, filed October 21, 1998, Attorney Docket No. 1744.0010000, now U.S. Patent No. 6,061,551, issued May 9, 2000. --.

Line 47, please delete "co-pending U.S. Patent".

Lines 48-50, please replace with -- "Method and System for Down-Converting Electromagnetic Signals," Ser. No. 09/176,022, filed October 21, 1998, Attorney Docket No. 1744.0010000, now U.S. Patent No. 6,061,551, issued May 9, 2000. --

Column 31,

Line 9, at the end please delete "the".

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,049,706
DATED : April 11, 2000
INVENTOR(S) : Cook et al.

Page 2 of 4

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 31,

Lines 1-2, please replace with the following:

-- $(\text{Freq}_{\text{input}} - \text{Freq}_{\text{IF}})/n = \text{Freq}_{\text{control}}$
(900 MHz - 0 MHz)/n = 900 MHz/n --.

Lines 10-13, please replace with -- "Method and System for Down-Converting Electromagnetic Signals," Ser. No. 09/176,022, filed October 21, 1998, Attorney Docket No. 1744.0010000, now U.S. Patent No. 6,061,551, issued May 9, 2000. --

Lines 33-34, please replace with the following:

-- $(\text{Freq}_{\text{input}} - \text{Freq}_{\text{IF}})/n = \text{Freq}_{\text{control}}$
(900 MHz - 0 MHz)/n = 900 MHz/n --.

Line 67, please delete "the co-pending U.S. Patent Application entitled".

Column 32,

Lines 1-3, please replace with -- "Method and System for Down-Converting Electromagnetic Signals," Ser. No. 09/176,022, filed October 21, 1998, Attorney Docket No. 1744.0010000, now U.S. Patent No. 6,061,551, issued May 9, 2000. --
Line 21, please delete " the co-pending".

Lines 22-25, please replace with -- "Method and System for Down-Converting Electromagnetic Signals," Ser. No. 09/176,022, filed October 21, 1998, Attorney Docket No. 1744.0010000, now U.S. Patent No. 6,061,551, issued May 9, 2000. --

Column 37,

Line 3, please delete "co-pending U.S. Patent Application".

Lines 4-5, please replace with -- "Method and System for Down-Converting Electromagnetic Signals," Ser. No. 09/176,022, filed October 21, 1998, Attorney Docket No. 1744.0010000, now U.S. Patent No. 6,061,551, issued May 9, 2000. --

Column 38,

Lines 52-54, please replace with -- The reader is directed to "Method and System for Frequency Up-Conversion," Ser. No. 09/176,154, filed October 21, 1998, Attorney Docket No. 1744.0020000, now allowed, incorporated herein by reference in its entirety. --

Line 55, please delete "erence in its entirety.".

Column 40,

Lines 34-36, please replace with -- "Method and System for Down-Converting Electromagnetic Signals," Ser. No. 09/176,022, filed October 21, 1998, Attorney Docket No. 1744.0010000, now U.S. Patent No. 6,061,551, issued May 9, 2000. --

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,049,706
DATED : April 11, 2000
INVENTOR(S) : Cook et al.

Page 3 of 4

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 47,

Lines 35-36, please replace "said one or more filtering parameters:" with -- said at least one of said filtering operation and said down-converting operation: --.

Lines 49-50, please replace "one or more parameters of said filtering operation" with -- at least one of said filtering operation and said down-converting operation --.

Line 56, please replace "of a control" with -- of said control --.

Line 59, please replace "to a down-converted" with -- to said down-converted --.

Column 48,

Line 31, please replace "of a down-converted" with -- of said down-converted --.

Line 39, please replace "to a control" with -- to said control --.

Column 52,

Line 64, please replace "8" with -- 86 --.

Column 53,

Line 1, please replace "8" with -- 86 --.

Line 5, please replace "8" with -- 86 --.

Column 54,

Line 65, please replace "105" with -- 106 --.

Column 55,

Line 33, please replace "105" with -- 106 --.

Column 58,

Line 51, please replace "164" with -- 165 --.

Column 59,

Line 21, please replace "164" with -- 165 --.

Line 55, please replace "175" with -- 176 --.

Column 60,

Line 25, please replace "175" with -- 176 --.

Line 61, please replace "186" with -- 187 --.

Column 62,

Line 7, please replace "186" with -- 187 --.

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,049,706
DATED : April 11, 2000
INVENTOR(S) : Cook et al.

Page 4 of 4

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 46,

Line 53, please replace "farther" with -- further --.

Column 47,

Line 2, please replace "parameters" with -- parameter --.

Line 67, please replace "operations" with -- operation --.

Column 51,

Line 55, please replace "76" with -- 74 --.

Line 57, please replace "76" with -- 74 --.

Line 60, please replace "76" with -- 74 --.

Signed and Sealed this

Twenty-seventh Day of November, 2001

Attest:

Nicholas P. Godici

Attesting Officer

NICHOLAS P. GODICI
Acting Director of the United States Patent and Trademark Office