

Basic Principles and New Solutions for Analog Sampled-Data Image Rejection Mixers

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Abstract—This paper briefly reviews basic principles of image rejection (IR) receivers, and then proposes a new architecture which is suitable for CMOS technology. The critical issue in the IR receiver is the phase accuracy and magnitude balance of the 90° phase shifting network. The proposed IR receiver employs a 3rd order IIR switched-capacitor (SC) quasi-Hilbert filter to act as a broad band 90° phase shifter. This SC phase shifter generates only 0.1° phase error and has a capacitor-ratio insensitive magnitude response. The simulated overall image rejection ratio is over 40dB in a bandwidth equal to 25% of the sampling frequency of the SC circuit.

I. INTRODUCTION

TRENDS in wireless IC design go towards higher integration level, lower power consumption and lower cost. Among wireless ICs, RF receivers are very important. Traditional RF receivers employ the super-heterodyne (super-het) architecture. However, superhet has poor integration level. Recently, much research effort has been put into receiver architectures for single chip integration. Some new architectures have been proposed, for example, low IF receiver [1], and some existing architectures have been studied, for example, direct conversion receiver [2], [3]

The image rejection (IR) receiver, originally proposed by Hartley [4], has also drawn attention again. This architecture has two big advantages. First, it eliminates the need of high-Q high-frequency image rejection filters which must be implemented with external passive components in the superhet. Therefore, the power consumption can be greatly reduced because there is no need to drive the low input impedance off-chip passive filters anymore. Second, intermediate frequency (IF) can be very low because the performance of image rejection does not depend on IF anymore. Therefore, selectivity is sufficient with integrated filters with a Q factor of only 10 to 20, typically. The IR receiver has found applications in radio receivers [5], mobile phone transceivers [6] and video systems [7]. However, it has not become very popular. The critical problem of IR receiver is the phase error and magnitude imbalance generated by the 90° phase shifting network (PSN) [8], which limits the image rejection ratio (IRR) to only 35dB, as shown in Table I. All existing implementations of this PSN are based on the RC/CR networks where it is difficult to achieve high magnitude balance in a broad frequency band. Fortunately, we found that this PSN can be implemented with extremely high accuracy by using switched-capacitor(SC) technology to emulate the operation of a sampled-data Hilbert transformer. With this method, a very high IRR can be achieved in a wide bandwidth without external tuning or trimming.

TABLE I
REPORTED IRR OF INTEGRATED IMAGE REJECTION RECEIVER.

Authors	IRR(dB)	90° Phase Shifter
Mcdonald, 93 [9]	14.1	RC/CR
Baumberger, 94 [8]	34	RC/CR
Pache, 95 [10]	35	RC/CR
Okanobu, 92 [5]	30*	Active RC/CR

*Contribution from MW ferrite bar antenna is not taken into account.

In section 2, the basic principles and practical issues of IR receivers will be briefly reviewed. In section 3, the proposed architecture will be described and simulation results will be given. Lastly, concluding remarks will be presented.

II. BASIC PRINCIPLES AND PRACTICAL ISSUES

There are a few variations of IR receiver topology. However, all are similar to the one shown in Figure 1. It consists of two matched mixers, a 90° PSN, a quadrature local oscillator (LO), and a summing circuit.

Figure 1 also illustrates the operation principle of the IR receiver. Here, the quadrature signal is defined to lead in-phase signal by 90° , and phase shifting is defined to shift phase in advance. The image signal lies at $2LO - RF$ for systems having LO lower than RF. In this receiver, the desired and image signals are mixed down together in both signal paths. However, the desired signal at the end of the upper and the lower paths are in-phase, while image signals are 180° out of phase. When the upper path and the lower path are recombined, the image signal will be canceled out and the desired signal left. This is explained in time domain in the following paragraphs.

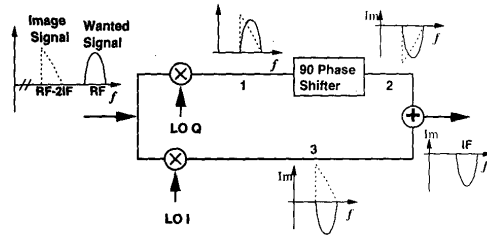


Fig. 1. Principle of an image rejection receiver.

Assume that the input wanted signal and image signal are $A \cos(\omega_s t)$ and $B \cos(\omega_i t)$, respectively, and that the LO Q and LO I are $\cos(\omega_{LO} t)$ and $\sin(\omega_{LO} t)$, respectively.

where $\omega_s - \omega_{LO} = \omega_{LO} - \omega_i$. For a perfectly matched circuit, the signal at node 1 is

$$\begin{aligned} & A \cos(\omega_s t) \cos(\omega_{LO} t) + B \cos(\omega_i t) \cos(\omega_{LO} t) \\ &= \frac{A}{2} \cos(\omega_{IF} t) + \frac{B}{2} \cos(\omega_{IF} t) \quad (\text{low passed}), \end{aligned}$$

at node 2 is

$$\begin{aligned} & \frac{A}{2} \cos(\omega_{IF} t + 90^\circ) + \frac{B}{2} \cos(\omega_{IF} t + 90^\circ) \\ &= -\frac{A}{2} \sin(\omega_{IF} t) - \frac{B}{2} \sin(\omega_{IF} t), \end{aligned}$$

and at node 3 is

$$\begin{aligned} & A \cos(\omega_s t) \sin(\omega_{LO} t) + B \cos(\omega_i t) \sin(\omega_{LO} t) \\ &= -\frac{A}{2} \sin(\omega_{IF} t) + \frac{B}{2} \sin(\omega_{IF} t) \quad (\text{low passed}). \end{aligned}$$

Therefore, the output signal is $-A \sin(\omega_{IF} t)$, and the image signal is cancelled out.

Now, let us consider the non-ideal case. Suppose the total gain mismatch (or ratio of gains) and phase error in the two paths of the IR receiver are e_g and θ degree, respectively. It can be proven that the IRR is given by:

$$IRR = \frac{1 + 2e_g \cos \theta + e_g^2}{1 - 2e_g \cos \theta + e_g^2}. \quad (1)$$

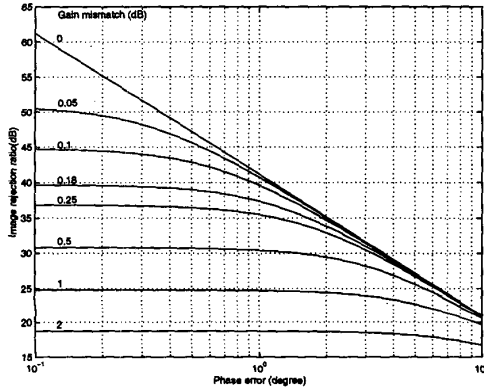


Fig. 2. IRR versus gain and phase error.

Figure 2 shows a graph of the IRR versus the gain and phase error. From this figure, we observe that if the gain (phase) accuracy remains unchanged, once the phase (gain) accuracy reaches a threshold value, further increase of the gain (phase) accuracy will not improve the IRR.

Factors which limit the IRR in the real IC systems are: (1) gain difference between two mixers; (2) magnitude imbalance and phase error between the quadrature outputs of LO; (3) magnitude imbalance and phase error of the PSN in the signal path.

An important specification of mixer specification is linearity. To improve linearity, double-balanced mixers which show no even-harmonic distortion are preferred. In the IR receiver, the source of mixer gain mismatching between its two paths comes from local variations and alignment errors in the fabrication. Careful layout is necessary. To achieve

higher gain matching, external tunable mixer could be employed [5]. However, this method is not favorable because an additional output pin is required and the additional tuning procedure increases the production cost.

Quadrature output of LO can be generated by three methods: (1) use of oscillators with inherent quadrature outputs; (2) use of frequency divider with one output triggered by the rising edge and another by the falling edge; (3) use of PSN. The first method is most favorable. A phase error of 0.5° and magnitude imbalance of 0.1dB [11] (corresponding to 45dB IRR) can be easily achieved by this method. The performance of the second method is limited by the duty cycle of the clock signal [5]. Besides, this method is not suitable for frequencies higher than 1GHz , because it needs a clock signal with doubled frequency. The third method is suitable only for systems with a narrow tuning range of the LO, because of the limitation of the PSN [12], [13].

A more critical problem is the magnitude imbalance and phase error of the PSN in the signal path. In the following subsection, existing methods of PSN design will be briefly reviewed.

Phase Shifting Network (PSN)

The PSN is not only required in an IR receiver, but is also widely used in other quadrature modulation/demodulation applications. There are many types of PSNs in the literature: delay lines, distributed couplers, lumped LC couplers, digital frequency dividers and RC/CR allpass network. However, as shown in Table I, only RC/CR allpass networks are commonly used in IR receivers, because the other methods are not suitable for monolithic integrated circuits.

In an RC/CR network, the output of an RC low pass section has always a 90° phase lag from a CR high pass section. The phase error comes from the RC relative value variance which can be well controlled. The major drawback is that its magnitude response is only matched at $f = 1/RC$, and this frequency depends on the absolute RC value which may have up to 50% variance for a typical IC technology. Thus, the achieved IRR is limited to about 20dB only. A solution to the problem of center frequency variance is to use tunable RC/CR circuit where the value of R or C is controlled by an external voltage [14]. A 1.6° phase error (corresponding to 37dB IRR) has been reported using this technique.

Recently, the sequence asymmetric cascaded RC polyphase network was proposed, which yielding a phase error of 0.5° and a magnitude imbalance of 0.5dB [15] (corresponding to 31dB IRR) in a wide frequency range. In this circuit, a signal and its inverse are applied to one pair of input pins, with the other two pins grounded. Due to its asymmetric structure, the magnitude error in RC section will be compensated in the next CR section. Therefore, with quite mild tolerances on its components, it is possible to have an order-of-magnitude improvement in magnitude response over the RC/CR network. The RC polyphase network is suitable for frequencies higher than 10MHz for

There is also a proposal of a PSN with electronic phase correction. The reported phase error is less than 1° and the magnitude imbalance is less than 0.1dB [16], [13]. However, it applies only for the quadrature generation of LO signal and not for the PSN in signal path, because clipping is necessary while the received signal can not be clipped to avoid distortion.

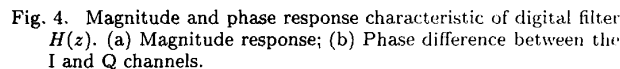
A. Architecture

$$H(jw) = \begin{cases} -j, & w \geq 0; \\ j, & w < 0. \end{cases} \quad (2)$$

Figure 3 shows the architecture of the proposed IR receiver, which consists of two matched mixers, two matched anti-aliasing filters and the Q and I branches of an SC Hilbert filter where the summing circuit is embedded (the sampling frequency is $4f_{IF}$ as will be discussed in next subsection). Filter Q has the same magnitude response as filter I but with 90° phase difference. Anti-aliasing filters are employed to relax the dynamic range requirement of the Hilbert filter. The IRR can of this architecture can be quite high because in general, the accuracy of SC circuits depends on the capacitor-ratio which can be well controlled in integrated circuits. We'll discuss the SC Hilbert filter in the next subsection.



Discrete-time Hilbert transform is usually approximated by an FIR filter. To have enough accuracy, a very large filter order is required (for example, 43rd order [17]). A such large order filter is infeasible for our application. However,

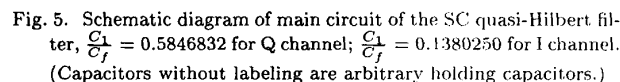


we do not need to perform 90° phase shift for the entire frequency band, only in a limited bandwidth. To design such a filter is much easier and IIR technique could be used.

$$H_Q = z^{-1} \frac{z^{-2} - a^2}{1 - a^2 z^{-2}}, \quad a^2 = 0.5846832 \quad (3)$$

$$H_I = -\frac{z^{-2}-b^2}{1-b^2z^{-2}}, \quad b^2 = 0.1380250 \quad (4)$$

The magnitude response of $H(z) = H_Q(z) + iH_I(z)$ is shown in figure 4(a), and the phase difference between the Q and I channels ($\angle H_Q - \angle H_I$) is shown in figure 4(b). Figure 4(b) shows that the I and Q channels have 90° phase difference in the frequency band ($\frac{1}{8}f_s, \frac{3}{8}f_s$), where f_s is the sampling frequency. Within this frequency band, this filter acts as a Hilbert transformer. Thus we call it “quasi-Hilbert filter”. For proper operation, the sampling frequency f_s should be 4 times the center frequency of IF signal (f_{IF}). As shown in Figure 4(a), within ($\frac{1}{8}f_s, \frac{3}{8}f_s$), the IRR is greater than 60dB.



The main component of equation (3) and (4), $\frac{z^{-2}-c^2}{1-z^2-c^2}$ where $c^2 = 0.5846832$ for Q channel, $c^2 = 0.1380250$ for I channel, can be implemented by a SC delay line circuit shown in Figure 5. The I and Q sub-filters have similar structure, except that filter Q has one more unit-delay element (not shown in Figure 5). The label 1 and 2 in Figure 5 denote two non-overlap clock signals with frequency $4f_{IF}$.

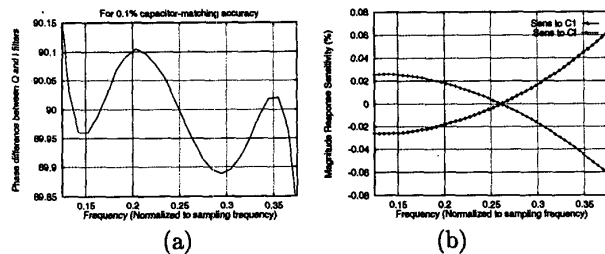


Fig. 6. (a) Phase response of quasi-Hilbert filter for 0.1% capacitor-matching accuracy; (b) Sensitivity of magnitude response to the capacitor C_f and C_1 .

C. Simulation results

For the quasi-Hilbert filter, the capacitor-matching between C_f and C_1 determines the phase accuracy. A matching accuracy of 0.1% typically achievable with proper layout method provides a phase error below 0.1° within $(\frac{1}{8}f_s, \frac{3}{8}f_s)$, as shown in Figure 6(a). Note that the required capacitor ratios can be represented as rational numbers: $\frac{7}{12}$ for Q channels (error is -0.0013), $\frac{4}{29}$ for I channel (error is -0.0001), where the capacitance spread is small. Two common-centroid capacitor arrays, one with 36 unit capacitors, the other with 25, can be used.

One important property of the circuit shown in Figure 5 is that its magnitude response is insensitive to capacitor-mismatch. Figure 6(b) shows the sensitivity of magnitude response to the capacitance C_f and C_1 . From this figure we observe that the sensitivity is less than 0.06% within $(\frac{1}{8}f_s, \frac{3}{8}f_s)$.

As a summary, the SC quasi-Hilbert filter can achieve more than 60dB IRR. However, the overall IRR of the proposed receiver depends also on the matching of mixers and the accuracy of quadrature LO.

The proposed architecture is designed primarily for the second frequency down converter in a cordless phone receiver, in which the IF is 200kHz. For more than 40dB overall IRR, LO must generate less than 0.1dB magnitude error and 0.5° phase error, mixers must generate less than 0.05dB magnitude error. These are not stringent requirements. The behavioral simulation result under these conditions is shown in Figure 7, from which we verify that 40dB IRR can be achieved.

IV. CONCLUSION

In this paper, the IR receiver has been reviewed and a new architecture which is suitable for CMOS technology has been proposed. This new receiver employs a SC phase shifting network which has a simple structure and achieves only 0.1° phase error (corresponds to 60dB IRR). This architecture is designed primarily for the use in the second frequency down converter in a cordless phone receiver. Better than 40dB IRR can be obtained without external tuning or trimming.

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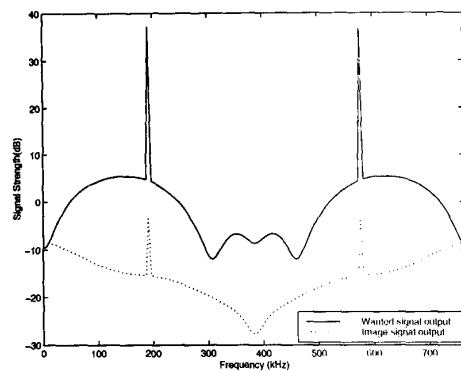


Fig. 7. Simulated output of IR receiver, with totally 0.15dB gain error between LO, Mixers and AA Filters, 0.5° phase error for quadrature LO, and 0.1% capacitor-mismatch of Hilbert filter.

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