

An improved 3V 2GHz BICMOS Image Reject Mixer IC

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ABSTRACT

A 2GHz BICMOS image reject mixer is described in this paper. A novel combination of 90° phase shifter networks and a gain control system are used to obtain high image rejection despite local oscillator frequency variation due to channel selection, intermediate frequency (IF) adjustment and process fluctuations. A 35 dB min. image rejection is obtained in a 200 MHz RF bandwidth centered at 2GHz and a 200MHz IF. Furthermore, the gain control system allows a 25 dB min. image rejection for IF adjustment from 100MHz to 300MHz. The conversion gain of the mixer is 10 dB and the IP3 is -4,5 dBm referenced to the input. The overall current consumption is 15 mA from a +3V supply. The mixer has been integrated in a front end IC including an antenna preamplifier in a silicon BICMOS process.

I Introduction

Future portable communication transceivers will need low cost high performance front end RF ICs in terms of, respectively, low power and high (GHz) frequency range. In the receiver path, the critical RF functions are the Low Noise Amplifier (LNA) and the UHF mixer. After preamplification in the LNA, the mixer converts both the RF signal and the unwanted image signal to the same fixed IF (intermediate frequency). To achieve good receiver selectivity, a low IF can be chosen, allowing the use of low Q IF filters which can be integrated. On the other hand, the image signal (RF-2IF) is then close to the RF frequency band and is difficult to eliminate. Usually the image signal is attenuated prior to the mixer by expensive high Q SAW filters which cannot be integrated. To eliminate the SAW filter, an image reject mixer must be used. An image reject system basically consists of two mixers, 90° phase shifters for the LO and IF, and a combiner. In this paper, a novel arrangement between RC/CR 90° phase shifter networks and a gain control system is used to obtain good image rejection despite LO frequency variation, IF adjustment and process fluctuations. The mixer has been integrated in a front end IC including an antenna preamplifier in a silicon BICMOS process.

II Conventional image cancelling architecture and previous realisations

Fig. 1 shows a classical image rejection system. A phase shifter (D_{LO}) supplies from local oscillator LO two quadrature signals (LO1 and LO2) to balanced mixers M1 and M2. The resulting transposed RF signals are available on two paths IF1 and IF2. After a second 90° phase shifter D_{IF} inserted into one of the IF paths, the resulting phase shifts are in opposite directions for the IF and image signals. After appropriate combination of IF1 and IF2 in the combiner C, the resulting image signal is reduced.

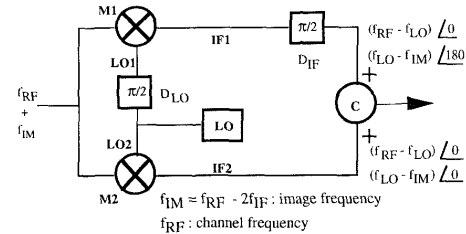


Fig.1 Classical image rejection mixer

The phase shifters are a critical part of the system. The image rejection is greatly dependent on the phase shift accuracy and the gain matching in the two paths LO1 - IF1 and LO2 - IF2 [1]. In FM applications, 90° phase shifts are achieved by frequency doubling in the LO part and by an active network in IF part [2]. These methods are not applicable in GHz range because the LO must run at two times the RF frequency and the IF is too high for active phase shifters. Furthermore, this approach is rather power consuming for use in portable RF systems.

Recent image rejection realisations [3], [4] use a combination of an RC integrator and a CR differentiator for the D_{LO} phase shifter (see fig. 2).

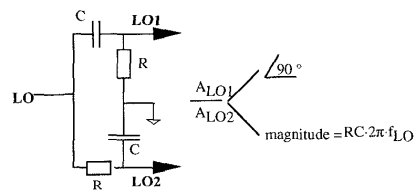


Fig. 2 D_{LO} phase shifter

In this network combination, the phase accuracy between the two signals LO1 and LO2 is only due to local R and C matching. On the other hand, the magnitude difference between the two signals is sensitive to LO frequency variation and to process fluctuations. This magnitude difference is given by :

$$A_{LO1} - A_{LO2} = A_{LO} [\Delta R/R + \Delta C/C + \Delta f_{LO}/f_{LO}] \quad (1)$$

process effect LO effect

Where A_{LO1} , A_{LO2} are the magnitudes of the two oscillator signals and f_{LO} is the variable LO frequency. R and C are the nominal values of resistance and capacitance chosen to center the pole in the f_{LO} range.

In ref. [3], D_{IF} is implemented as a differential R'C/C'R' bridge between the differential output of one of the mixers and the corresponding differential input of the combiner (see fig4). The other differential path is connected directly to the combiner.

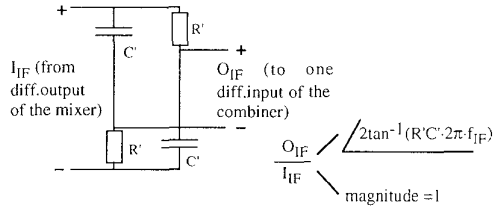


Fig. 4 .Differential D_{IF} phase shifter (from [3])

Contrary to the previous D_{LO} architecture, this network introduces no magnitude difference between differential input and output signals, but the phase shift error is greatly dependent on the IF frequency and technology fluctuations. This phase error is given by :

$$(\theta_O - \theta_I) = \pi/2 \cdot [\Delta R'/R' + \Delta C'/C' + \Delta f_{IF}/f_{IF}] \quad (2)$$

process effect IF effect

Where θ_I and θ_O are the phases of the input and output differential signals and IF is the intermediate frequency. R' and C' are the nominal values of resistance and capacitance chosen to center the pole at a fixed IF.

In conclusion, the cumulated amplitude error due to D_{LO} and phase error due to D_{IF} makes the image rejection greatly dependent on the LO frequency variation in the RF bandwidth, the IF adjustment and process fluctuations.

III Proposed architecture

Fig. 5 shows the proposed new mixer architecture. With regard to the previous conclusion, two main improvements have been performed :

- a- the R'C/C'R' phase shifter D_{IF} was distributed among the IF1 and IF2 paths. As shown previously for

the D_{LO} phase shifter, this network arrangement introduces a constant 90° phase difference between the two IF paths. So, the D_{IF} and D_{LO} phase shifters achieve the appropriate phase shift between the two paths LO1 - IF1 and LO2 - IF2 independently of the LO frequency variation, the IF adjustment and process fluctuations.

- b- Only the magnitudes of the signals between the two paths remain to be matched to obtain good image rejection.

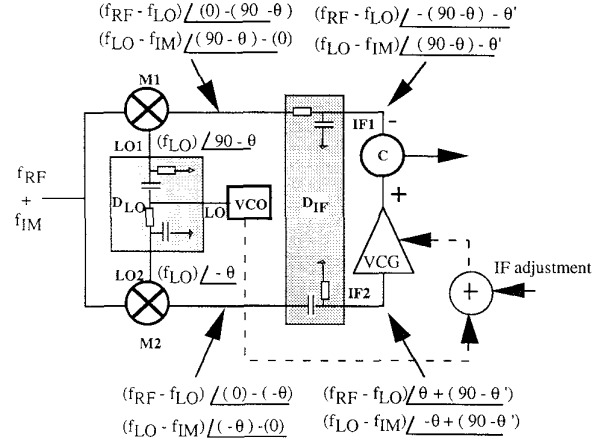


Fig.5 The proposed new architecture of the mixer. ($-\theta$ and $-\theta'$ are the respective phase shift due to the RC networks in D_{LO} and D_{IF} phase shifters).

This is realized in two ways as shown in figure 5. First, an RC (CR) LO network is connected to a CR (RC) IF network in each LO-IF path so that the attenuation in each of the networks is compensated. Second, a voltage controlled gain (VCG) is introduced into the combiner. A feedforward loop can be used between the VCO and the VCG to compensate the gain variation due to D_{LO} over the VCO frequency range. In the same way, the VCG can be trimmed to compensate the gain variation due to D_{IF} over the IF adjustment range.

The improvement can be quantified by writing the amplitude ratio of the signals A_{IF1} and A_{IF2} at the inputs of the combiner :

$$A_{IF1}/A_{IF2} = RC \cdot f_{LO}/R'C' \cdot f_{IF} \quad (3)$$

from which the amplitude difference of the two signals is deduced :

$$(A_{IF1} - A_{IF2}) = A_{IF} \cdot [\Delta R/R - \Delta R'/R' + \Delta C/C - \Delta C'/C' + \Delta f_{LO}/f_{LO} - \Delta f_{IF}/f_{IF}] \quad (4)$$

$\Delta R/R - \Delta R'/R' = \Delta C/C - \Delta C'/C'$ is nulled due to the new distributed phase shifters, while $\Delta f_{LO}/f_{LO}$ and $\Delta f_{IF}/f_{IF}$ are nulled due to the VCG

IV Circuit implementation

Fig. 6 shows the schematic diagram of the circuit. To obtain a complete image rejection front end, an antenna preamplifier was integrated before the image reject mixer (IR). The multipliers M1 and M2 are classical differential Gilbert cells and are not detailed. The RC/CR phase shifter D_{LO} is connected between the external LO input and the two multipliers. The common mode bias is set by an external voltage and the 10 pF internal decoupling capacitance C_1 . The R'C/C'R' phase shifter D_{IF} is implemented as differential stages between the mixers and the combiner. Two internal systems B1 and B2 are used to mirror the common mode bias to the preamplifier-multipliers connection and to the C'R' network-combiner connection.

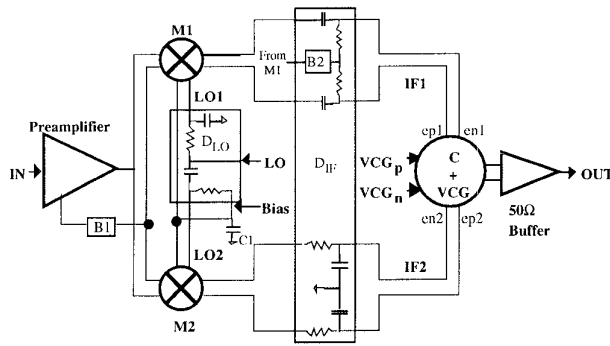


Fig. 6 Complete schematic diagram

Fig. 7 shows the schematic of the bandpass antenna preamplifier. It is composed of large area transistor Q1 designed for low noise and of an integrated LC load. The cascode transistor Qc eliminates the Miller effect multiplication of the capacitance C_{bc} of Q1. C is a double poly capacitor. L and L' are integrated metal inductors [5]. Inductor L' is used to achieve a 50Ω real part input impedance for the preamplifier. The current mirror $Q_m - Q_d$ and the 40 pF internal decoupling capacitance C_2 form a low noise bias scheme for Q1. Transistor Q_s acts as source follower and level shifter.

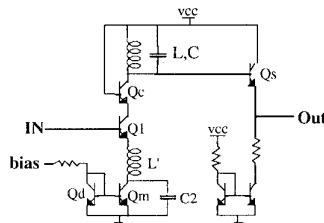


Fig. 7 Preamplifier schematic

Fig. 8 shows the schematic of the combiner including the VCG. The VCG voltage is applied to the inputs of the source coupled pair $M_1 - M_2$, biased by the current I_0 . The current mirrors $M_3 - M_{m3}$ and M_4

- M_{m4} control the transconductances g_m and g_m' of the differential pairs Q1 - Q2 and Q'1 - Q'2 so that $g_m = \alpha \cdot g_{m0}$ and $g_m' = (1 - \alpha) \cdot g_{m0}$. α depends on the VCG input voltage and g_{m0} is the common transconductance for $\alpha = 0.5$. Resulting from the cross - coupling between the two differential pairs, the output voltage is given by:

$$v_{out} = g_{m0} \cdot R [\alpha \cdot v_1 + (1 - \alpha) \cdot v_2] \quad (5)$$

Where v_1 and v_2 are the input signals from the IF1 and IF2 paths and v_{out} is the output signal of the combiner. Furthermore, (see Fig. 8), the common mode output voltage $V_{cm} = R (I_{cQ1} + I_{cQ'1}) = (K/2) R I_0$ is held constant independently of the α variation. A buffer amplifier was integrated for test purposes to drive a 50Ω system load.

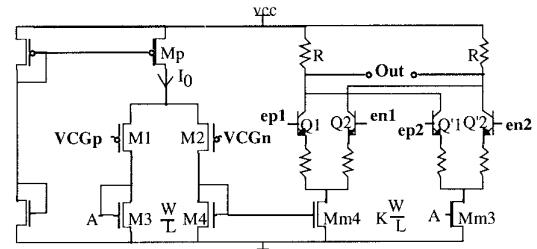


Fig. 8 Combiner schematic

V Experimental results

The overall circuit was implemented in a silicon BICMOS process with typical f_T (n-p-n) = 10 GHz and 0.8 μm MOSFET channel length. All precise capacitors (in the LC load of the preamplifier and in the RC/CR networks in the phase shifters) were fabricated using two poly layers. All decoupling capacitors were fabricated using gate poly and well diffusion. Figs. 9 and 10 show the image rejection and conversion gain performances of the front end circuit. The image rejection results reported here were obtained despite two minor design errors :

First, the decoupling capacitance C_1 (10 pF) in Fig. 6 with the bonding wire connected to the external common mode bias of D_{LO} phase shifter makes a parasitic resonant circuit. The insufficient value of C_1 results in a high resonance frequency, introducing a 2 degree phase error in D_{LO} .

Second, the RC network in D_{IF} , loaded by the capacitance due to the Miller effect at the input of the combiner, adds approximately 1 degree to the previous phase error.

The first problem can be solved easily by increasing the value of capacitance C_1 (up to 50 pF) or by working in a differential mode for the local oscillator. The solution for solving the second problem is to insulate D_{IF} from the combiner by using a follower stage. Simulated image rejection in a revised circuit currently in fabrication is better than 50dB.

Performances of the mixer and the overall front end circuit are summarized in Table 1.

Parameter	Measurement
Supply voltage	3 V
Mixer supply current	15 mA
LNA supply current	5 mA
S11 (front end)	-10 dB
Conv. Gain (front end)	17 dB
Conv. Gain (mixer)	8,5 dB
Image Rejection (mixer)	25-35 dB
Input IP3 (front end)	-15 dBm
Input IP3 (mixer)	-4,5 dBm
LO-RF isolation (front end)	27 dB
LO-IF isolation (front end)	34 dB

Table 1 Summary of measured results.

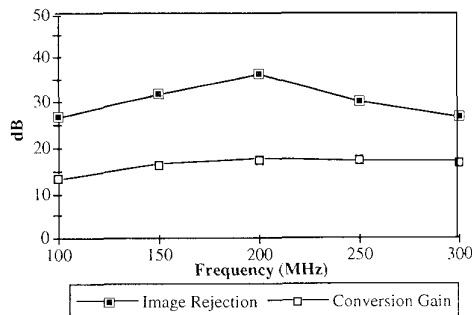


Fig. 9 Image rejection and Conversion Gain versus Intermediate Frequency (after VCG trimming).

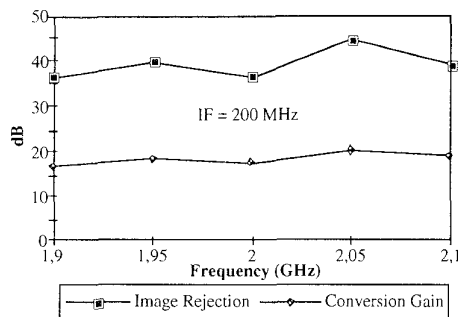


Fig. 10 Image rejection and Conversion Gain versus RF channel (after VCG trimming).

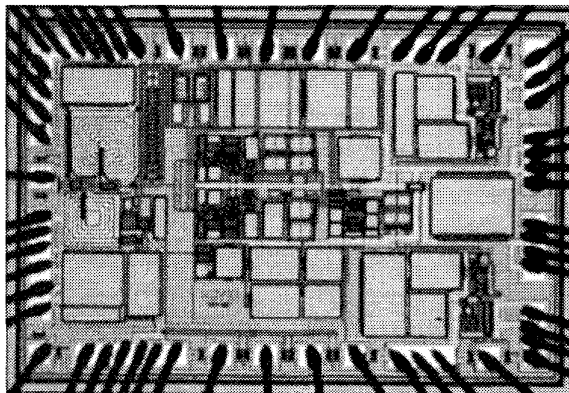


Fig. 11 Front end chip microphotograph

Fig. 11 shows a microphotograph of the front end circuit. Separate ground pads for input and output stages are used to overcome feedback coupling. Multiple bonding wires are used for lowering the self inductance on the ground and Vcc pins. The die size of the circuit is 2mm x 1mm.

VI Conclusion

A 2GHz, 3V image reject mixer is described in this paper. A novel combination of phase shifter networks and a gain control system are used to obtain high image rejection despite LO frequency variation, IF adjustment and process fluctuations. The measured results are lower than expected (50 dB for IR) because of two minor errors which have been corrected in a new circuit in fabrication. The concept is particularly suited for application in low cost and low power radio terminals.

Acknowledgement

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