

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ELMOS SEMICONDUCTOR SE
Petitioner

v.

TEXAS INSTRUMENTS INCORPORATION
Patent Owner

Patent No. 11,653,432
Filing Date: Nov. 30, 2021
Issue Date: May 16, 2023

LIGHT-EMITTING DIODE (LED) DRIVER SYSTEM WITH SLEW-RATE
CONTROL

**DECLARATION OF PETER GLÖSEKÖTTER IN SUPPORT OF PETITION
FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 11,653,432**

Inter Partes Review No. _____

1. I, PETER GLÖSEKÖTTER, declare as follows:
2. I have personal knowledge of the facts stated in this declaration, and could and would testify to these facts under oath if called upon to do so.

I. INTRODUCTION

a. Engagement Overview

3. I have been retained by counsel for Petitioners in this case as an expert in the relevant art. I am being compensated for my work as part of an engagement with ELMOS Semiconductor SE. No part of my compensation is contingent upon the outcome of this petition.
4. I was asked to study U.S. Pat. No. 11,653,432 (“the ‘432 Patent”), its prosecution history, and the prior art, and to render opinions on the anticipation and/or obviousness or non-anticipation and/or non-obviousness of the claims of the ‘432 Patent in light of the teachings of the prior art, as understood by a person of ordinary skill in the art in the November 2021 time frame. I understand that the claims being challenged in the Petition are Claims 1-20 (“the challenged claims”).

b. Summary of Opinions

5. After studying the ‘432 Patent, its file history, and the prior art, and considering the subject matter of the claims of the ‘432 Patent in light of the

state of technical advancement in the area of light-emitting (LED) driver systems prior to and approaching the November, 2021 timeframe, I reached the conclusions discussed herein.

6. In light of these general conclusions, and as explained in more detail throughout this declaration, it is my opinion that each of the challenged claims are obvious in light of the knowledge of skill in the art in the November 2021 timeframe and the teachings, suggestions, and motivations present in the prior art and commercially.
7. This Declaration, and the conclusions and opinions herein, provide support for the Petition for *inter partes* review (“IPR”) of the ‘432 Patent filed by Petitioner. I have reviewed the Petition in its entirety as well as its corresponding exhibits.

c. Qualifications and Experience

8. My educational background includes a Master’s Degree in Electrical Engineering from the University of Dortmund, Germany including the Graduate Thesis “Learning Methods for an Adaptive Neuro-Fuzzy Network, December, 1997,” and a Ph. D. in Electrical Engineering from the University of Dortmund, Germany, including the Dissertation: “Resonant Tunnel Diodes and Heterobipolar Transistors in Dynamic Digital Circuits,” July, 2002. I worked as a Design Engineer for Intel from January 2003 to

September 2006. Since September 2006, I have been in my current role of Professor in the Department of Electrical Engineering and Computer Science for the Münster University of Applied Sciences.

9. I am knowledgeable and familiar with electrical regulated drivers for light-emitting diodes LEDs and more generally with electrical regulated driver systems for electrical loads of which LED driver circuits are a subset. I have received multiple awards and research grants, as listed on my curriculum vitae, provided attached to this Petition as Ex1004.

d. Materials Considered

10. My analysis is based on my education and experience as set out above and in my CV, including the documents I have read and electrical circuits and systems I have developed and or studied.
11. I reviewed the various relevant publications from the art at the time of the alleged invention and the claim analysis that is included in the Petition for IPR of the '432 Patent, to which this declaration relates. I have also reviewed the Petition in its entirety. Based on my experience as a person having ordinary skill in the art ("POSITA") at the time of the alleged invention, the references accurately characterize the state of the art at the relevant time. More specifically, I have reviewed at least the following references for the preparation of this Declaration:

Ex. No.	Description
1001	U.S. Patent 11,653,432 to Meng et al. (“the ‘432 Patent”)
1002	App. Ser. No. 17/537,694 for U.S. Pat. 11,653,432 File Wrapper History (“File History”)
1003	Declaration of Peter Glösekötter in Support of Petition for Inter Partes Review of U.S. Patent No. 11,653,432 (“Glösekötter Decl.”)
1004	Curriculum Vitae of Peter Glösekötter (“Glösekötter Curriculum Vitae”)
1005	U.S. Patent 10,136,496 to Sudhaus (Sudhaus)
1006	Japanese Patent JP 2012160287 A to Ryoichi (Ryoichi) with English translation
1007	Certification of Translation for Ryoichi
1008	Article published in October 2016 edition of Elektronik Praxis by Sudhaus 2016 entitled <i>Die Verlustleistung in linearen Regelsystemen günstig verteilen</i> (Praxis) with English translation
1009	U.S. Patent 11,599,132 B2 to Wu et al. (Wu)
1010	Article published in IEEE Journal of Solid-State Circuits – March 2003 entitled <i>On-chip ramp generators for mixed-signal BIST and ADS self-test</i> by Provost (Provost)
1011	White paper by Texas Instruments entitled <i>Voltage-to-current (V-I) converter circuit with MOSFET</i> – document number SBOA327A – December 2019 – Revised August 2021 (TI Paper)
1012	White paper entitled “ <i>The MOSFET Current Mirror</i> ” by the University of Kansas, dated April 25, 2011 (UK Paper). Chrome-extension://efaidnbmnnnibpcajpcglclefindmkaj/https://www.ittc.ku.edu/~jstiles/412/handouts/4.5%20Biasing%20in%20MOS%20Amp%20Circuits/The%20MOSFET%20Current%20Mirror.pdf
1013	ELMOS presentation at the International CAR Symposium of February 4, 2015 by Burchard entitled “Wärmemanagement mit intelligenten Linearreglerkonzepten” (the Burchard presentation) with English translation.

II. LEGAL PRINCIPLES USED IN THE ANALYSIS

12. I am not a patent attorney, nor have I independently researched the law on patent validity. Attorneys for the Petitioner explained certain legal principles to me that I have relied upon in forming my opinions set forth in this report.

a. Person Having Ordinary Skill in the Art (“POSITA”)

13. I understand that I must undertake my assessment of the claims of the ‘432 Patent from the perspective of what would have been known or understood by a POSITA as of the earliest-claimed priority date of the patent claim, which I understand is November 30, 2021. The opinions and statements that I provide herein regarding the ‘432 Patent and the references that I discuss are made from the perspective of a person of ordinary skill in the art in the November 2021 time frame.

14. Counsel has advised me that, to determine the appropriate level of one of ordinary skill in the art, I may consider the following factors: (a) the types of problems encountered by those working in the field and prior art solutions thereto; (b) the sophistication of the technology in question, and the rapidity with which innovations occur in the field; (c) the educational level of active workers in the field’ and (d) the educational level of the inventor.

15. I believe the relevant technology field for the ‘432 Patent has to do with light-emitting diode (LED) driver systems. Based on this, a POSITA at the

time of the '432 Patent filing would have been an engineer with at least a bachelor's degree in electrical engineering, or a related field, or equivalent experience of at least two years of working in the field of developing LED driver systems.

16. Unless otherwise specified, when I mention a POSITA or someone of ordinary skill, I am referring to someone with at least the above level of knowledge and understanding.
17. Based on my experiences, I have a good understanding of the capabilities of a person of ordinary skill in the relevant field. Indeed, in addition to being a person of at least ordinary skill in the art, I have worked closely with many such persons over the course of my career.
18. Although my qualifications and experience exceed those of the hypothetical person having ordinary skill in the art defined above, my analysis and opinions regarding the '432 Patent have been based on the perspective of a person of ordinary skill in the art in the 2010's through the 2020-2021 time frame.
19. My opinions regarding the level of ordinary skill in the art are based on, among other things, the content of the '432 Patent, my years of experience in the field of design and development of electrical circuits, and in particular, my knowledge and experience regarding regulated electrical driver systems,

acquired through my education, work experience, research experience and teaching experience as a Professor, my understanding of the basic qualifications that would be relevant to POSITA in the relevant area, and my familiarity with the backgrounds of colleagues and co-workers, both past and present.

20. My opinions herein regarding the person of ordinary skill in the art and my other opinions set forth herein would remain the same if the person of ordinary skill in the art were determined to have somewhat more or less education and/or experience than I have identified above.

b. Prior Art

21. I understand that the law provides categories of information that constitute prior art that may be used to anticipate or render obvious patent claims. To be prior art to a particular patent under the relevant law, a reference must have been made, known, used, published, or patented, or be the subject of a patent application by another, before the priority or invention dates of the patent. I also understand that the POSITA is presumed to have knowledge of the relevant prior art.

22. As discussed below, I understand that the Petitioner has determined, for purposes of this proceeding, that the challenged claims of the '432 Patent may be entitled to a November 30 , 2021 priority date.

c. Claim Interpretation

23. I understand that, in an IPR, the claims are to be construed to have “the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art in and the prosecution history pertaining to the patent.” See 37 C.F.R. §42.100(b). I applied the plain and ordinary meaning of the petitioned Claims to the asserted prior art references. In support of grounds 1-5, which involve terms that are basic in the industry, and readily understood by a POSITA upon review of the specification and file history. In performing my analysis and rendering my opinions, I have interpreted the claim terms by giving the terms the ordinary meaning they would have had to a POSITA reading the ‘432 Patent around the time of its earliest priority filing date November 30, 2021 and in light of the ‘432 specification and file history.

d. Legal Standards of Anticipation & Obviousness

24. I have been provided the following instructions from the Federal Circuit Bar Association Model Instructions regarding anticipation and obviousness, which is reproduced in part below. I apply this understanding in my analysis, with the caveat that I have been informed that the Patent Office will find a patent claim invalid in an IPR if it concludes that it is more likely than not that the claim is invalid (i.e., a preponderance-of-the-evidence

standard), which is a lower standard than the “clear-and-convincing” burden of proof that is applied in United States District Courts (and described in the jury instruction below):

4.3b-1 ANTICIPATION

To anticipate the invention, the prior art does not have to use the same words as the claim, but all of the requirements of the claim must have been disclosed and arranged as in the claim. The claim requirements may either be disclosed expressly or inherently that is, necessarily implied such that a person having ordinary skill in the art in the technology of the invention, looking at that one reference, could make and use the claimed invention..

Here is a list of the ways that a person may show that a patent claim in the “432 Patent is not new:

- if the claimed invention was already publicly known or was used, on sale, or otherwise made available to the public before November 30, 2021;
- if the claimed invention was already patented or described in a printed publication anywhere in the world before November 30, 2021. A reference is a “printed publication” if it is accessible to those interested in the field, even if it is difficult to find;
- if the claimed invention was already made by someone else in the United States before November 30, 2021, if that other person had not kept it secret;

- if the claimed invention was already described in another issued U.S. patent or published U.S. patent application that was based on a patent application filed before November 30, 2021;

25. Where Petitioner is relying on prior art that was not considered by the PTO during examination, you may consider whether that prior art is significantly different and more relevant than the prior art that the PTO did consider. If you decide it is different and more relevant, you may weigh that prior art more heavily when considering whether the challenger has met its burden of proof in showing the claims are invalid (Federal Circuit Bar Association Model Patent Jury Instructions (May 2020)).

26. Furthermore, it is my understanding that “[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.” *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

27. (Model Patent Jury Instructions for the Northern District of California at 32, § 4.3a2 (July 16, 2015)).

4.3c OBVIOUSNESS

Even though an invention may not have been identically disclosed or described before it was made by an inventor, in order to be patentable, the

invention must also not have been obvious to a person of ordinary skill in the field of technology of the patent at the time the invention was made. Petitioner may establish that a patent claim is invalid by showing, by clear and convincing evidence, that the claimed invention would have been obvious to persons having ordinary skill in the art at the time the invention was made in the design and development of electrical regulated driver systems.

In determining whether a claimed invention is obvious, you must consider the level of ordinary skill in the field [of the invention] that someone would have had at the time the patent was filed, the scope and content of the prior art, and any differences between the prior art and the claimed invention.

Keep in mind that the existence of each and every element of the claimed invention in the prior art does not necessarily prove obviousness. Most, if not all, inventions rely on building blocks of prior art. In considering whether a claimed invention is obvious, you may but are not required to find obviousness if you find that at the time of the claimed invention there was a reason that would have prompted a person having ordinary skill in the field of design and development of electrical

regulated driver systems to combine the known elements in a way the claimed invention does, taking into account such factors as (1) whether the claimed invention was merely the predictable result of using prior art elements according to their known function(s); (2) whether the claimed invention provides an obvious solution to a known problem in the relevant field; (3) whether the prior art teaches or suggests the desirability of combining elements claimed in the invention; (4) whether the prior art teaches away from combining elements in the claimed invention; (5) whether it would have been obvious to try the combinations of elements, such as when there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions; and (6) whether the change resulted more from design incentives or other market forces. To find it rendered the invention obvious, you must find that the prior art provided a reasonable expectation of success. Obvious to try is not sufficient in unpredictable technologies.

In determining whether the claimed invention was obvious, consider each claim separately. Do not use hindsight, i.e., consider only what was known at the patent's filing date.

In making these assessments, you should take into account any objective evidence (sometimes called “secondary considerations”) that may shed light on the obviousness or not of the claimed invention, such as:

- (a) Whether the invention was commercially successful as a result of the merits of the claimed invention (rather than the result of design needs or market-pressure advertising or similar activities);
- (b) Whether the invention satisfied a long-felt need;
- (c) Whether others had tried and failed to make the invention;
- (d) Whether others invented the invention at roughly the same time;
- (e) Whether others copied the invention;
- (f) Whether there were changes or related technologies or market needs contemporaneous with the invention;
- (g) Whether the invention achieved unexpected results;
- (h) Whether others in the field praised the invention;
- (i) Whether persons having ordinary skill in the art of the invention expressed surprise or disbelief regarding the invention;

- (j) Whether others sought or obtained rights to the patent from the patent holder; and
- (k) Whether the inventor proceeded contrary to accepted wisdom in the field.

28. Federal Circuit Bar Association Model Jury Instructions §4.3c (2020);
MPEP §§ 2141-43.

29. I am also informed that the United States Patent Office supplies its examining corps with a Manual of Patent Examining Procedure that provides exemplary rationales that may support a conclusion of obviousness, including:

- (a) Combining prior art elements according to known methods to yield predictable results;
- (b) Simple substitution of one known element for another to obtain predictable results;
- (c) Use of known technique to improve similar devices (methods, or products) in the same way;
- (d) Applying a known technique to a known device (method, or product) ready for improvement to yield predictable results;
- (e) “Obvious to try” – choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;
- (f) Known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives

or other market forces if the variations are predictable to one of ordinary skill in the art; or
(g) Some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

30.MPEP § 2143. I apply these principles in my analysis below.

III. BACKGROUND OF THE TECHNOLOGY RELATED TO THE ‘432 PATENT

31.The ‘432 Patent relates to a driver system to supply energy to light-emitting diodes (LEDs). LEDs have taken on a primary role for automobile lighting, and other applications. Power to LEDs is commonly controlled via integrated circuits (ICs) with driver circuits and driver transistors controlling electrical energy delivered to the LEDs.

32.In automotive applications, supply voltage conditions for LED driver circuits can vary significantly. As supply voltage increases, heat dissipated by driver transistors can increase to a critical point at which driver circuits can be damaged by overheating.

33.Known approaches for protecting LED driver circuits, pioneered by Petitioner, include using an IC with an error amplifier, driver outputs (integrated in an IC) and an external shunt resistor to drive an LED load. Dependent on the supply voltage, a portion of power to the LED load is

delivered through a second driver and associated external shunt resistor. The external resistor dissipates some of the excess heat, thereby extending a voltage range under which an LED driver system can operate without suffering damage due to overheating.

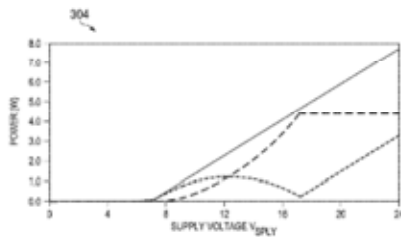
34. The '432 Patent purportedly relates to such a driver system for LEDs. The '432 Patent includes two current driver paths for an LED load, with one current path including an external shunt resistor. As supply voltage increases, a portion of the total current supplied to the LED load is purportedly shifted to the current path including the shunt resistor, with the intent of transferring heat losses to the shunt resistor. Ex1001, 2:27-31, 2:40-49.

35. Prior art disclosing such LED drivers was publicly available at the time of filing of the '432 Patent. For example, Sudhaus, issued on Nov. 20, 2018, discloses a driver system including two or more current paths for supply power to an LED load. Ex1005, 2:25-53. Praxis appeared in the October 2016 edition of Elektronik Praxis, Ex1008, Section entitled "Modern linear regulators with a power distribution," second and third paragraphs, Figure 1 describing such drivers. Further, the Burchard presentation at the International CAR Symposium of February 4, 2015 entitled "Wärmemanagement mit intelligenten Linearreglerkonzepten" described

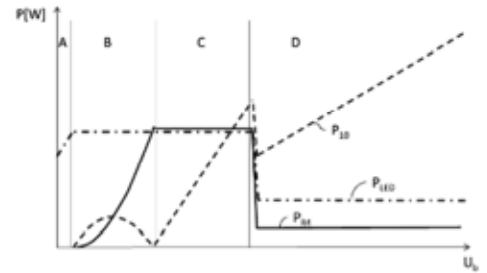
these concepts. Ex1013, slides 6 and 7.

36. Independent claim 1 of the '432 Patent is an apparatus claim with only two claim elements listing basic electronic components: an error amplifier, and an amplifier output stage comprising a slew rate controller, a shunt resistor, current paths, and an LED string. The '432 claims are to be construed with functional limitations in view of the basic electronic components consisting of: an error amplifier, and an amplifier output stage comprising a slew rate controller, a shunt resistor, current paths, and an LED string.
37. In my opinion, the '432 patent is modeled after, and is nothing more than an implementation of Sudhaus, using well known and basic circuit constructs such as error amplifiers (including amplifier output stages), slew rate controllers, current paths, current mirrors, and shunt resistors. Sudhaus discloses an LED driver system including two or more current paths for supply power to an LED load. Ex1005, 2:25-53. Sudhaus further includes controlling a total current delivered to the LED load based on a reference value. Ex1005, 4:46-50. Sudhaus further includes gradually transitioning a part of a total current delivered to an LED load from a first current path without the external resistor to a second current path with the external resistor as supply voltage increases (slew rate control). Ex1005, 5:40-46, 6:18-26.

38.I further observed in reviewing the '432 patent and Sudhaus, that the '432 Patent includes in Fig. 3, a graph similar to Fig. 5 of Sudhaus, with the '432 Patent essentially replicating the point of the Sudhaus graph.



'432 Patent, Fig. 3 (second graph)



Sudhaus Fig. 5

39.Applicants of the '432 Patent, did not, however, identify Sudhaus as relevant prior art in their filing. Although Applicants, are a sophisticated supplier of integrated circuits, with multiple published slew rate circuits (see www.ti.com), Applicants did not disclose any prior art with the application of the '432 Patent.

IV. INTERPRETATION OF CLAIM LIMITATIONS IN THE '432 PATENT

40.Claim terms in *inter partes* review proceedings are construed to have “the meaning that the term would have to a person of ordinary skill in the art in

question at the time of the invention.”¹ Petitioner applies the plain and ordinary meaning of the petitioned claims to the asserted prior art references in support of grounds 1-5², which involve terms that are readily understood by a POSITA upon review of the specification and file history. Petitioner proposes claim term constructions according to their plain and ordinary meaning to a POSITA in view of the ‘432 Patent’s specification.

Accordingly, the plain and ordinary meaning of:

- 41. **“amplifier output stage”** means an electrical circuit that receives at least one input and outputs a signal based on the at least one input.
- 42. **“control voltage”** means an electrical signal used as an input to an electrical device that can influence an operation of the electrical device.
- 43. **“current path”** is a means for conveying electrical current along a controlled pathway.
- 44. **“error amplifier”** means an electrical circuit that detects a difference between two electrical input signals and outputs a signal based on the

¹ Petitioner reserves the right to present different constructions and/or challenge the patentability of any claim under 35 U.S.C. § 112 in another forum where a different claim construction standard applies. Thus, the proposed constructions do not constitute an admission that the claims are valid under 35 U.S.C. § 112.

² See Phillips v. AWH Corp., 415 F.3d 1303 (Fed. Cir. 2005) (en banc)

difference.

45. **“reference voltage”** means a voltage representing a desired level of an electrical parameter in a circuit.

46. **“slew rate”** means a rate of change of an electrical signal over time.

47. **“slew-rate controller”** means an electrical circuit that controls a rate of change of an electrical signal over time.

V. THE ASSERTED PRIOR ART REFERENCES ARE ANALOGOUS ART

48. A POSITA would understand the asserted prior art references are analogous to the ‘432 Patent and are combinable in the ways explained below.

a. A POSITA’s Level of ordinary skill in the art.

49. As discussed above, based on the disclosure of the ‘432 Patent, a person having ordinary skill in the art (“POSITA”) at the relevant time, would have had at least a bachelor’s degree in electrical engineering or related field, or equivalent experience of at least two years working in the field of design and development of electrical regulated driver systems.

VI. THE PRIORITY OF CLAIMS OF THE ‘432 PATENT

50. I understand that the ‘432 Patent has a filing date and priority date of November 30, 2021.

VII. OVERVIEW OF THE PRIOR ART

51. The prior art references included in the grounds of unpatentability pre-date

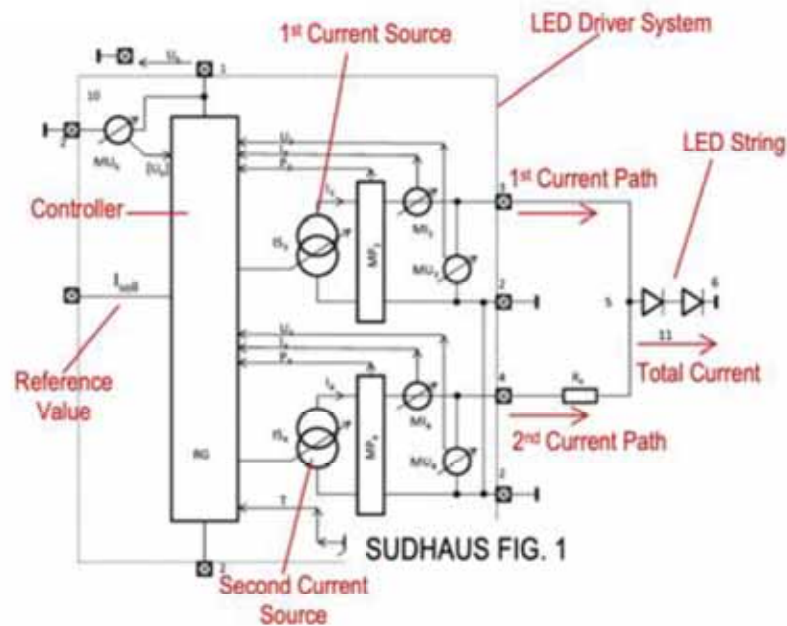
Nov. 30, 2021.

52. The prior art references Sudhaus, Praxis, Ryoichi, Wu, Provost, TI Paper, and UK paper all relate to the design of electrical regulated driver systems.

53. Sudhaus, Praxis and Wu teach regulated supplies that provide source current (from a positive supply) to a load, Ryoichi is configured to provide a sink current (to ground) to a load. It would have been obvious to POSITA that the concepts and circuits presented in Ryoichi are applicable and easily adapted to the regulated supplies presented in Sudhaus, Praxis and Wu.

A. Overview of U.S. Pat. No. 10,136,496 B2 to Sudhaus (“Sudhaus”) (Ex. 1005)

54. I have reviewed Sudhaus, U.S. Pat. No. 10,136,496 B2 to Sudhaus, and found it teaches, in reference to Fig. 1, a Controller RG operative to control a total current delivered to an LED load through two current paths, based on a desired value for I_{soll} . Ex1005, 4:46-50, Fig. 1. The two current paths include a first current path including a current source IS_3 and a second current path including a current source IS_4 in series with an external resistor R_4 .



55. Sudhaus further teaches to manage power dissipation, gradually shifting a portion of the total current from the first current path to the second current path as the system supply voltage increases. Ex1005, 5:40-46, 6:18-26.

56. In my opinion, a POSITA would recognize that the claimed features of the '432 Patent, i.e., an error amplifier, amplifier output stage including slew rate controller, two current paths, and an external shunt resistor are no more than a specific realization of the teaching of Sudhaus.

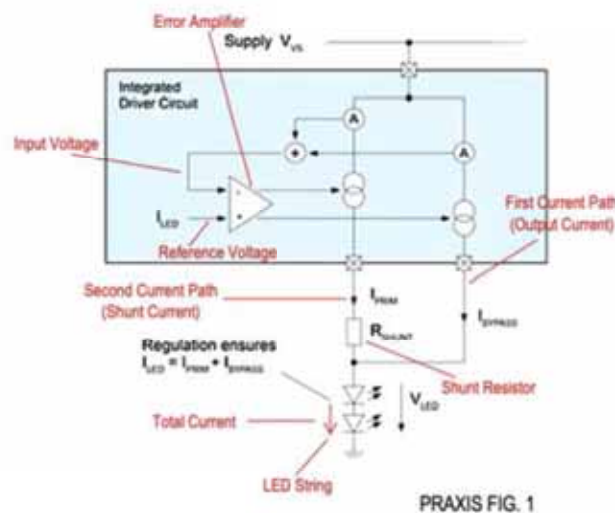
B. Overview of JP 2012160287 A to Ryoichi ("Ryoichi") (Ex1006)

57. Ryoichi is directed to a regulated LED driving circuit that supplies driving current to LEDs through a driving transistor. Ex1006, ¶ [0017]. The integrated circuit is characterized by supplying the driving transistor with driving signals whose rise time and fall time are controllable, thus making it

60. In my opinion, Ryoichi, discloses multiple transistor level implementations of the basic building blocks (error amplifier, amplifier output stage, slew rate control, current source output), as used to supply a controlled current to an LED load. A POSITA would have found it obvious to include these basic circuit structures in the LED driver system of Sudhaus.

C. Overview of Article by Sudhaus, published in the October 2016 Edition of Elektronik Praxis entitled “Die Verlustleistung in linearen Regelsystemen günstig verteilen” – English translation (Praxis) (Ex1008)

61. Praxis discloses a system to deliver a controlled total current to an LED load. Ex1008, page 1:1-2. Praxis includes distributing total current delivered to the LED load over two outputs, including one in series with an external resistor. Ex1008, page 3:5-16.

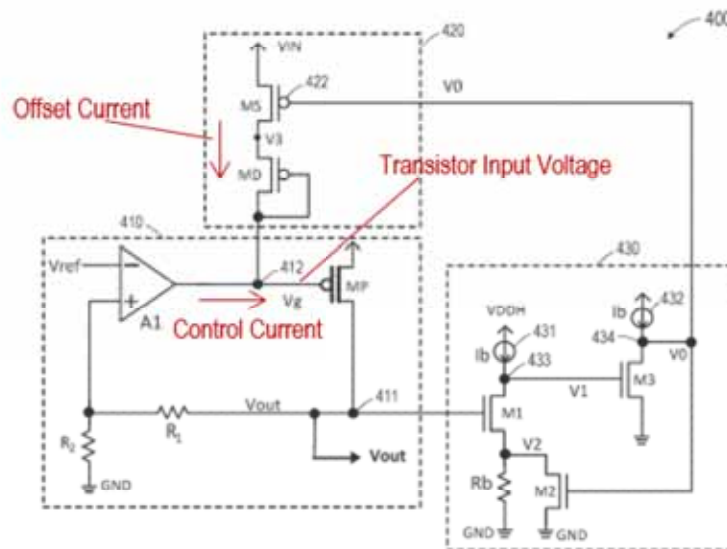


62. Praxis provides examples of error amplifiers including an amplifier output stage having two outputs for controlling two separate current sources. A

POSITA would have found it obvious to realize a portion of the controller of Sudhaus with the error amplifier of Praxis providing two outputs to control two current paths, and further found it obvious to base the amplifier output stage on the amplifier output stage presented in Ryoichi, thereby adding an additional output to control the second current path.

D. Overview of U.S. 11,599,132 B2 to Wu et al. (“Wu”) (Ex. 1009)

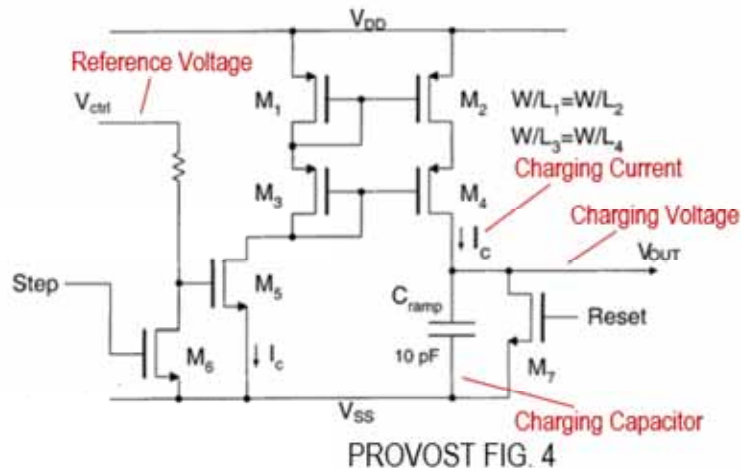
63. Wu is directed to a regulator circuit including an error amplifier that controls an output transistor and a slew rate control circuit coupled to a gate of the output transistor. Wu provides an alternate approach for implementing slew rate control, based on a supply voltage level.



WU FIG. 4

E. Overview of Article published in IEEE Journal of Solid-State Circuits – March 2003 entitled *On-chip ramp generators for mixed-signal BIST and ADS self-test* by Provost (Provost) (Ex1010)

64. Provost discloses an on-chip ramp generator Ex1010, Fig. 4.

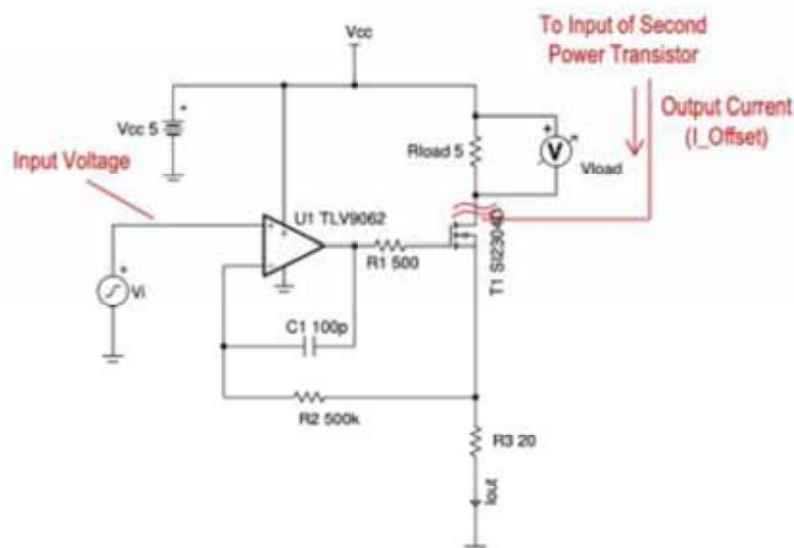


65. In the on-chip ramp driver of Provost, Fig. 4, transistor M5 is the current driver, M1-M4 form a cascode current mirror that delivers a current I_c (charging current) to a capacitor C_{ramp} (charging capacitor) to develop a voltage V_{out} (charging voltage).

F. Overview of White paper by Texas Instruments entitled *Voltage-to-current (V-I) converter circuit with MOSFET* – document number SBOA327A – December 2019 – Revised August 2021 (TI Paper) (Ex1011)

66. TI Paper discloses a voltage-to-current converter (V-I converter) in Fig. 1.

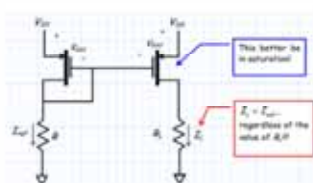
Ex1011, Fig. 1. The TI Paper V-I converter can be used to convert a charging voltage (applied to V_i) to generate an offset current. Ex1011, Fig. 1.



TI PAPER FIG. 1

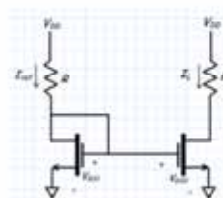
G. Overview of White paper entitled “*The MOSFET Current Mirror*” by the University of Kansas, dated April 25, 2011 (UK Paper) (EX1012)

67.UK Paper discloses NMOS and PMOS current mirrors. Ex1012, Figures on page 2 and page 6.



PMOS Current Mirror

Fig. page 6



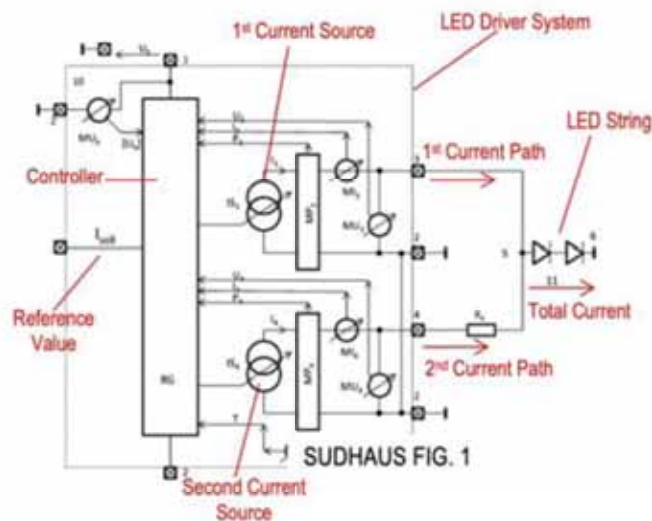
NMOS Current Mirror

Fig. page 2

H. Ground 1: Claims 1-3, 6, 10-11, and 16-17 are unpatentable under 35 U.S.C. § 103(a) as being obvious over Sudhaus

68. Claimed features of the LED driver system of the '432 Patent would have been obvious over Sudhaus to a POSITA at the time of filing.

69. Sudhaus discloses, in reference to Fig. 1, a Controller RG operative to control a total current delivered to an LED load through two current paths, based on a desired value for I_{sol} . Ex1005, 4:46-50, Fig. 1. The two current paths include a first current path including a current source IS_3 and a second current path including a current source IS_4 in series with an external resistor R_4 .



70. Sudhaus teaches to manage power dissipation, gradually shifting a portion of the total current from the first current path to the second current path as the system supply voltage increases. Ex1005, 5:40-46, 6:18-26.

71. POSITA would have found it obvious, based on Sudhaus, to supply an LED load through two current paths, one current path including an external

resistor, while controlling a sum of the currents delivered to the load with the motivation of managing power dissipation in the driver circuit to protect the circuit from thermal damage. POSITA would have further found it obvious to increase the portion of the current through the second current path including the external resistor as supply voltage increases. POSITA would further have found it obvious to *gradually* increase the current through the second current path (control the slew rate) with increasing supply voltage based on Sudhaus.

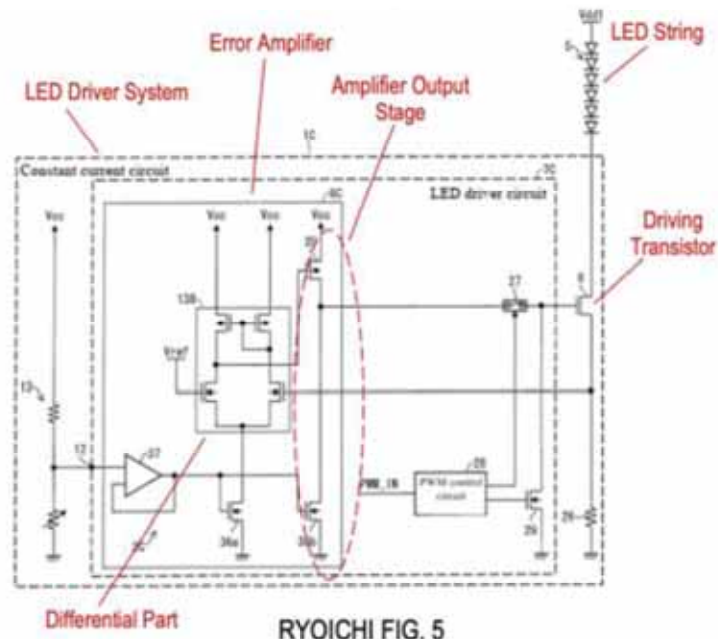
I. Ground 2: Claims 1-4, 6-7, 10-12 and 15-18 are unpatentable under 35 U.S.C. § 103(a) as being obvious over Sudhaus in view of Ryoichi.

72.Claimed features of the LED driver system of the '432 Patent would have been obvious over Sudhaus as discussed above, in view of Ryoichi.

73.Sudhaus discloses an LED driver system that delivers a controlled total current to an LED load via two current paths, a first current path including a current source, and a second current path including a current source and external shunt resistor. The system further includes provisions to gradually shift a portion of total current from the first current path to the second current path with increasing supply voltage.

74.Ryoichi is directed to an LED driving system with a driving transistor (as part of a current source) that controls driving current for an LED load.

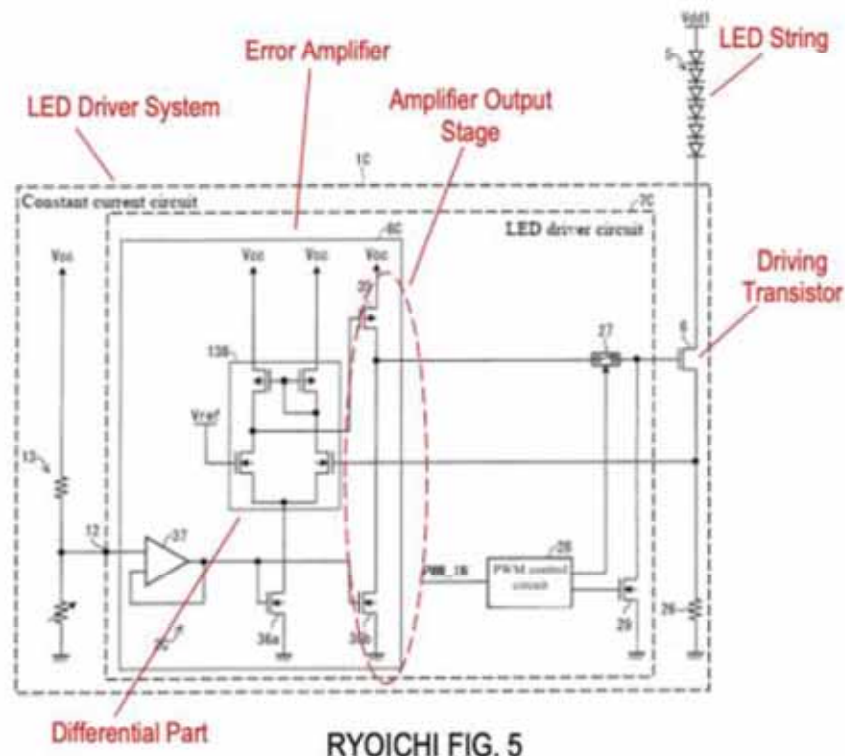
Ryoichi's driving system includes control of rise and fall times (slew rate control) of a control signal controlling the driving transistor. Ex1006, ¶ [0017].



75. As shown in Fig. 5, Ryoichi's LED driver circuit 10 includes operational amplifier 8C (error amplifier) that compares reference voltage V_REF with voltage corresponding to LED load current, Ex1006, ¶ [0083]. Operational amplifier 8C includes differential part 138, and an amplifier output stage comprising transistors 35 and 36b. Differential part 138 generates control voltage to control one or more control transistors 35 in the amplifier output stage. Ex1006, ¶ [0083]. The amplifier output stage controls power transistor 6 that delivers current to LED string 5. Ex1006, ¶ [0083].

76. Ryoichi discloses multiple approaches to controlling the slew rate of the driving signal controlling the driving transistor, of which three approaches will be discussed herein.

77. As a first example, Ryoichi, in Fig. 5, discloses controlling a slew rate of a driving signal controlling the driving transistor by adjusting a bias current provided to an error amplifier and amplifier output stage. Ex1006, Fig. 5.

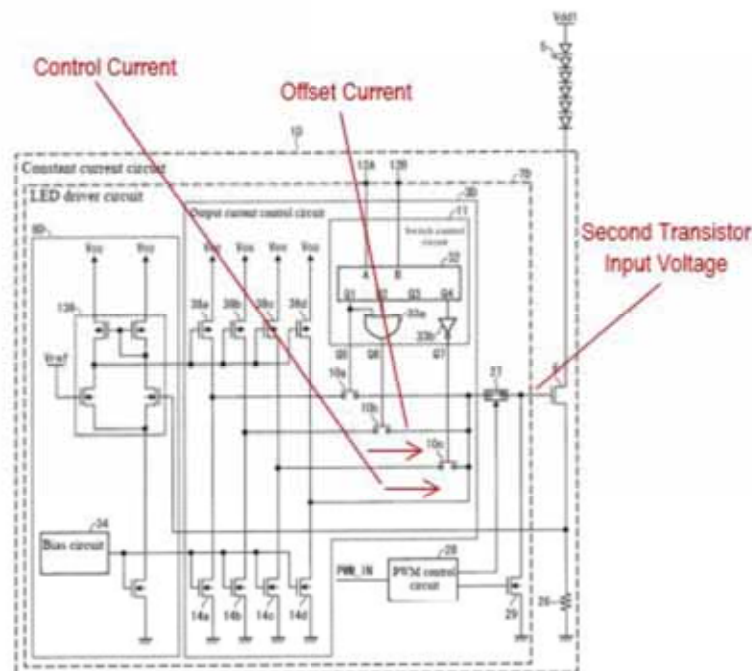


RYOICHI FIG. 5

78. Ryoichi's LED driver circuit includes operational amplifier 8C (error amplifier) that compares reference voltage V_{REF} with a voltage corresponding to a current to the LED load 5. to control a current delivered

to the LED load 5. Ex. 1006, ¶ [0083]. Drive capability of operational amplifier 8C can be adjusted by changing voltage applied to input 12 with the resistive divider 13, to change a bias current delivered to the differential part 138 by transistor 36a and a bias current delivered to the amplifier output stage by transistor 36b, effectively adjusting a rise time and fall time of a driving signal driving transistor 6. Ex1006, ¶ [0085].

79.As a second approach to controlling slew rate, Ryoichi Fig. 6 illustrates controlling of rise and fall time of the control signal controlling the driving transistor 6 by switching pairs of transistors into and out of the amplifier output stage. E1006, Fig. 6.



RYOICHI FIG. 6

80.In Fig. 6, the amplifier output stage of Fig. 5 (transistors 35 and 36b), has

82. Ryoichi discloses at a transistor level an error amplifier and an amplifier output stage, e.g. Ex1006, [0083], Fig. 5. Ryoichi discloses a slew rate controller e.g. Ex1006, ¶¶ [0085], [0089]-[0092], [0104]. Ryoichi further discloses functional limitations of controlling a slew rate and providing a regulated current to an LED load. Ex1006, [0083]-[0085].

83. It would have been obvious to POSITA to include the error amplifier (including the amplifier output stage) of Ryoichi in the controller of Sudhaus as a method to regulate the total current to the LED load. It would further have been obvious to POSITA to include the slew rate control of Ryoichi to control the slew rate of the second current path in Sudhaus to accomplish gradual transition from first current path to second current path.

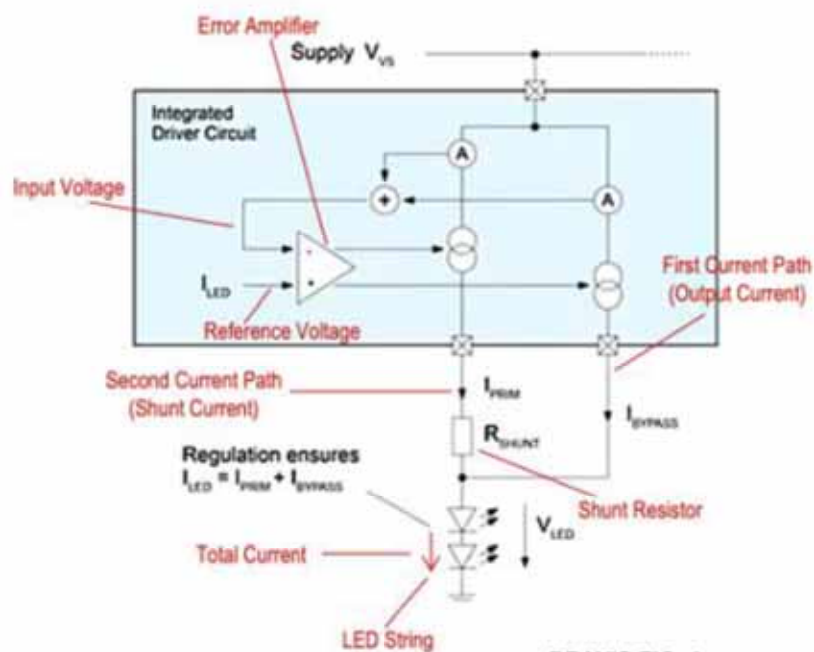
J. Ground 3: Claims 1-4, 6-7, 10-12 and 15-18 are unpatentable under 35 U.S.C. § 103(a) as being obvious over Sudhaus in view of Ryoichi in view of Praxis

84. The LED driver system of the '432 Patent would have been obvious over Sudhaus in view of Ryoichi, in further view of Praxis.

85. Sudhaus discloses an LED driver system that delivers a total controlled current to an LED load via two current paths, a first current path including a current source, and a second current path including a current source and [IC] external shunt resistor. The system further includes provisions to gradually transition current from the first current path to the second current path.

86. Ryoichi discloses an LED driver system that further discloses multiple variations of slew rate control. Ryoichi further discloses transistor level realizations of an error amplifier, amplifier output stage and current source.

87. Praxis discloses a system to deliver controlled total current to an LED load. Ex1008, page 1:1-2. Praxis includes distributing the total current delivered to the LED load over two outputs, one of which is in series with an external resistor. Ex1008, page 3:5-17.



PRAXIS FIG. 1

88. Analogously to the '432 Patent, Praxis includes an error amplifier with an amplifier output stage having two outputs to independently control two driver outputs. Ex1008, 3:5-16. A primary driver output together with a resistor R_{SHUNT} provide a first current path for providing current I_{PRIM}

to the LED load. A bypass driver provides a second current path for providing current I_{BYPASS} . EX1008, Page 3:13 to Page 4:7, Fig. 2.

89. Praxis provides a total current to the LED load through the two current paths (primary and bypass). Ex1008, e.g., page 3;15-17.

90. Praxis' error amplifier includes two outputs to control two current sources. It would have been obvious to include the error amplifier of Praxis including an output stage have two outputs to control two current sources in the LED driver system of Sudhaus.

91. Based on the combination of Sudhaus and Praxis, it would have further been obvious to POSITA to include Ryoichi's differential part and amplifier output stage and slew rate control in the error amplifier of Praxis, to control a transition of a current to the second current path of Sudhaus.

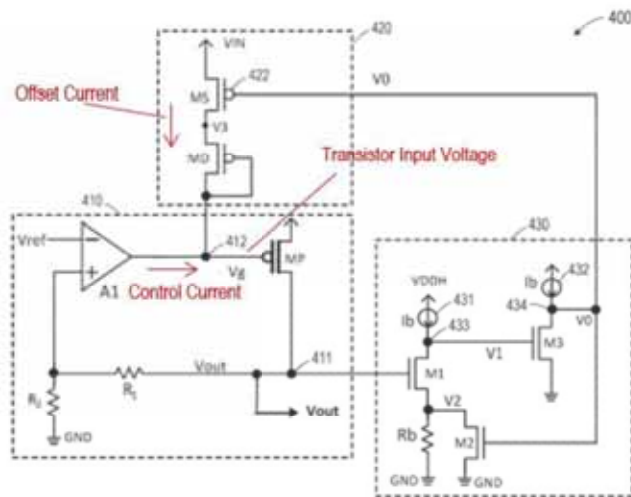
K. Ground 4: Claims 1-4, 6-7, 10-12, 15-18 are unpatentable under 35 U.S.C. § 103(a) as being obvious over Sudhaus in view of Ryoichi in view of Praxis in view of Wu

92. Wu is directed to a regulator circuit including an error amplifier that controls an output transistor and a slew rate control circuit coupled to a gate of the output transistor and is presented as an alternative to the slew rate control of Sudhaus and/or Ryoichi for controlling a slew rate of an input to a power transistor in a regulated system.

93. As described in reference to Grounds 1, 2, and 3, Sudhaus in view of

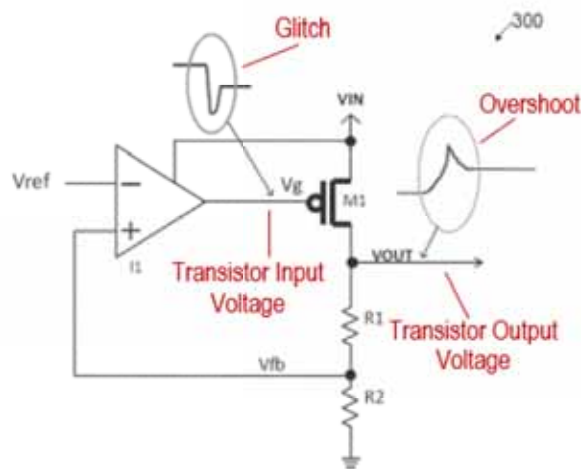
Ryoichi in view of Praxis disclose an LED driver system supplying current to an LED load via two current paths: a first current path including a power transistor, and a second current path including a power transistor in series with a resistor. The LED driver system includes slew rate control to gradually transition a portion of a total current delivered to an LED load from a first current path to a second current path with increasing supply voltage.

94. Figure 4 of Wu describes linear regulator circuit 400 including linear regulator 410. Linear regulator 410 includes error amplifier A1, the output of error amplifier A1 is connected to control the gate of output transistor MP. Error amplifier A1 is configured to regulate output voltage V_OUT at the output of output transistor MP, based on feedback of resistor pair R1 and R2. Ex1009, 6:14-19. Linear regulator circuit 400 includes slew-rate control circuit 420 coupled to gate node 412 of output transistor M1. Slew-rate control circuit 420 is configured to control voltage rise of gate node 412 during power-up to reduce output voltage overshoot. Ex1009, 6:24-28.



WU FIG. 4

95. Figure 3 of Wu illustrates overshoot that the slew-rate circuit addresses.



WU FIG. 3

96. During power-up, a glitch on the gate of M1 can cause the full rail voltage to appear on the output V_{OUT} . Ex1009, 5:47-48. The slew rate controller of Wu includes an output voltage level detection 430 that turns the slew rate control off when the output voltage V_{OUT} reaches a preset level. Ex1009,

7:6-14.

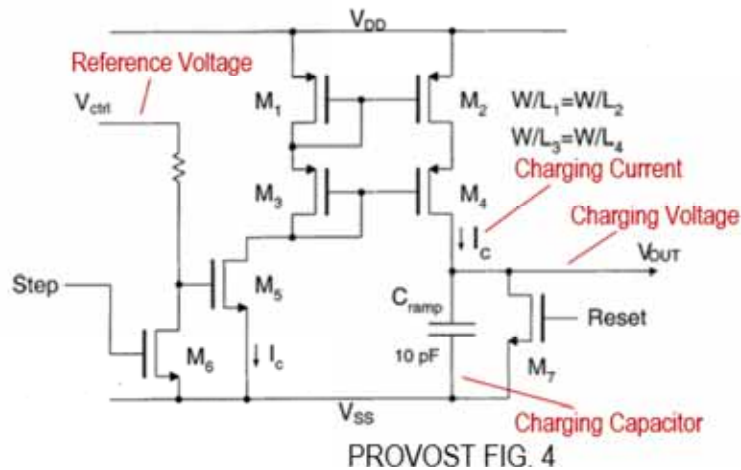
97. POSITA would have found it obvious at the time of the invention to include Wu with Sudhaus, to implement the gradual transition of current from the first current path to the second current path, as described in Sudhaus.

L. Ground 5: Claims 1-20 are unpatentable under 35 U.S.C. § 103(a) as being obvious over Sudhaus in view of Ryoichi in view of Praxis in view of Provost in view of TI Paper in view of UK Paper

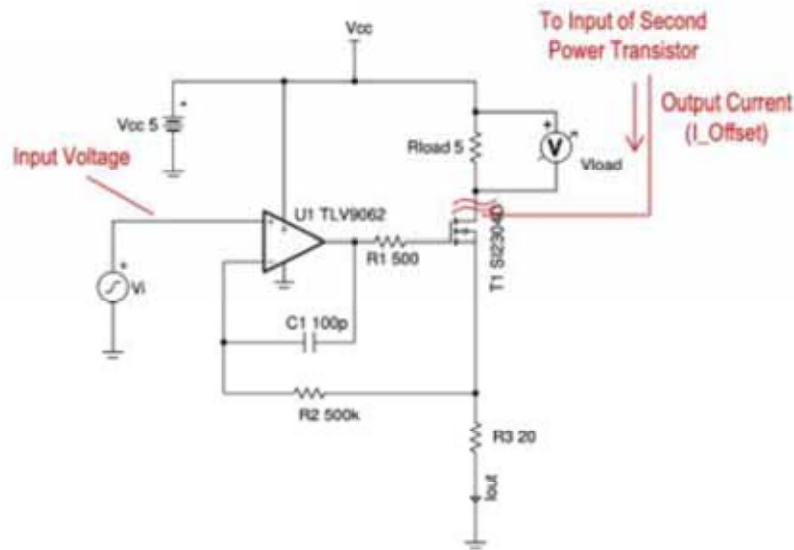
98. As described in reference to Ground 3, Sudhaus in view of Ryoichi in view of Praxis disclose an LED driver system supplying current to an LED load via two current paths: a first current path including a power transistor, and a second current path including a power transistor in series with a resistor. Slew rate control is described to gradually transition a portion of a total current delivered to an LED load from a first current path to a second current path with increasing supply voltage.

99. The combination of Provost, the TI Paper and the UK Paper are presented as an alternative method of slew rate control.

100. Provost discloses an on-chip ramp generator in Fig. 4. Ex1010, Fig. 4.



101. Provost transistor M5 is a current driver, M1-M4 form a cascode current mirror delivering current I_c (charging current) to capacitor C_{ramp} (charging capacitor). M6 is used for stopping the current source when Step is at logic 1. M7 is used to reset C_{ramp} . Ex1010, Section II (C), page 265-266. When turned on, charging current charges the charging capacitor to generate a ramp (charging voltage). Ex1010, Section II (C), page 265-266.
102. It would have been obvious to POSITA to combine the ramp generator of Provost with the combination of Sudhaus, Ryoichi and Praxis to generate a charging current, and to use a charging capacitor together with the charging current to generate a charging voltage.
103. TI Paper discloses a voltage-to-current converter (V-I converter) in Fig. 1. Ex1011, Fig. 1.



TI PAPER FIG. 1

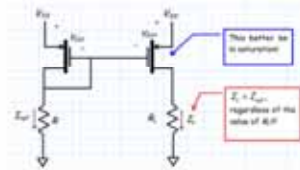
104. The voltage-to-current converter converts an input voltage to an output current. In the example of Fig. 1, the output current is given by:

$$I_o = \frac{V_i}{R_3}$$

105. Ex1011, page 2:1-2. The V-I converter of TI Paper can be used to convert a charging voltage (applied to V_i) to generate an offset current (output current delivered to the load R_{load_5} in Fig. 1). Ex1011, Fig. 1. It would have been obvious to POSITA to use the basic circuit building block of a voltage-to-current converter to convert a ramp voltage (charging voltage) of Provost to an offset current to control the slew rate of an input signal applied to a driving transistor.

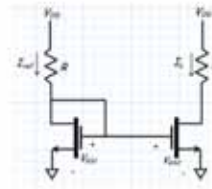
106. UK Paper discloses NMOS and PMOS current mirrors. Ex1012,

Figures on page 2 and page 6.



PMOS Current Mirror

Fig. page 6



NMOS Current Mirror

Fig. page 2

107. When the transistors in transistor pairs are dimensioned the same, I_{ref} will equal I_L for both the NMOS Current Mirror and the PMOS Current Mirror. Ex1012, page 3.
108. UK Paper is included for completeness. PMOS and NMOS current mirrors are common, well known building blocks in MOSFET circuits. Although current I_{offset} generated by the voltage-to-current converter of TI paper could, under at least some circumstances, be applied directly to an input of a driving transistor to control a slew rate, Claims 5, 8, 13 and 19 of the '432 Patent include current mirrors to apply the current I_{offset} to the driving transistor input. It would be an obvious choice for POSITA, in order, for example, to adjust a current magnitude of current I_{offset} (by varying transistor sizes in the current mirrors), or in some cases, to reconcile voltage levels of the output of the voltage-to-current converter to the voltage level of the input to the driving transistor.

VIII. THE PETITIONED CLAIMS ARE UNPATENTABLE UNDER GROUNDS 1 -5

109. Ground 1: It is my opinion that Claims 1-3, 6, 10-11, and 16-17 are unpatentable under 35 U.S.C. §103(a) as being obvious over Sudhaus.
110. Ground 2: It is my opinion that Claims 1-4, 6-7, 10-12 and 15-18 are unpatentable under 35 U.S.C. §103(a) as being obvious over Sudhaus in view of Ryoichi.
111. Ground 3: It is my opinion that Claims 1-4, 6-7, 10-12 and 15-18 are unpatentable under 35 U.S.C. §103(a) as being obvious over Sudhaus in view of Ryoichi in view of Praxis.
112. Ground 4: It is my opinion that Claims 1-4, 6-7, 10-12, and 15-18 are unpatentable under 35 U.S.C. §103(a) as being obvious over Sudhaus in view of Ryoichi in view of Praxis in view of Wu.
113. Ground 5: It is my opinion that Claims 1-20 are unpatentable under 35 U.S.C. §103(a) as being obvious over Sudhaus in view of Ryoichi in view of Praxis in view of Provost in view of TI paper in view of UK paper.
114. It is my understanding that none of: Sudhaus, Ryoichi, Praxis, Provost, TI Paper, or UK paper were considered during the prosecution of the application for the '432 patent.
115. I used the following table to help me keep the references and grounds organized:

CLAIM	GROUND 1 Sudhaus 103	GROUND 2 Sudhaus, Ryoichi 103	GROUND 3 Sudhaus, Praxis & Ryoichi	GROUND 4 Sudhaus, Praxis, Ryoichi & Wu	GROUND 5 Sudhaus, Ryoichi
CLAIM 1 [1.PRE-1.4]	✓	✓	✓	✓	✓
CLAIM 2 [2.1-2.2]	✓	✓	✓	✓	✓
CLAIM 3 [3.1-3.2]	✓	✓	✓	✓	✓
CLAIM 4 [4.1-4.2]	-	✓	✓	✓	✓
CLAIM 5 [5.1-5.3]	-	-	-	-	✓
CLAIM 6	✓	✓	✓	✓	✓
CLAIM 7	✓	✓	✓	✓	✓
CLAIM 8 [8.1-8.3]	-	-	-	-	✓
CLAIM 9 [9.1-9.3]	-	-	-	-	✓
CLAIM 10	✓	✓	✓	✓	✓
CLAIM 11 [11.PRE-11.6]	✓	✓	✓	✓	✓
CLAIM 12	-	✓	✓	✓	✓
CLAIM 13 [13.1-13.3]	-	-	-	-	✓
CLAIM 14 [14.1-14.3]	-	-	-	-	✓
CLAIM 15 [15.1-15.6]	-	✓	✓	✓	✓
CLAIM 16 [16.PRE-16.7]	✓	✓	✓	✓	✓
CLAIM 17 [17.1-17.2]	✓	✓	✓	✓	✓
CLAIM 18	-	✓	✓	✓	✓
CLAIM 19 [19.1-19.3]	-	-	-	-	✓
CLAIM 20 [20.1-20.3]	-	-	-	-	✓
Notes:					

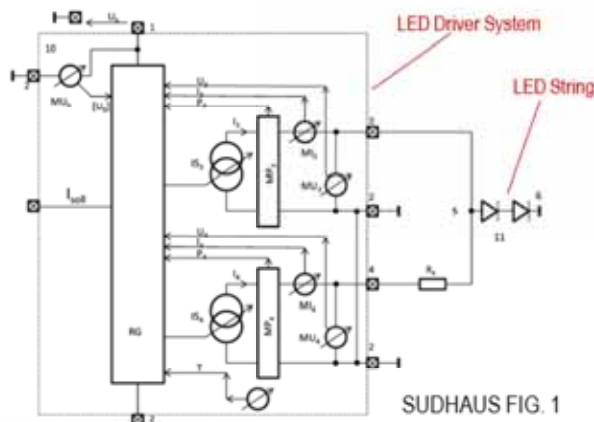
A. Claim 1 (broken into elements [1.pre – 1.4] presented below) is unpatentable under Grounds 1-5

[1.pre]	A light-emitting diode (LED) driver system comprising:
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a) Grounds 1–5: Claim [1.pre]

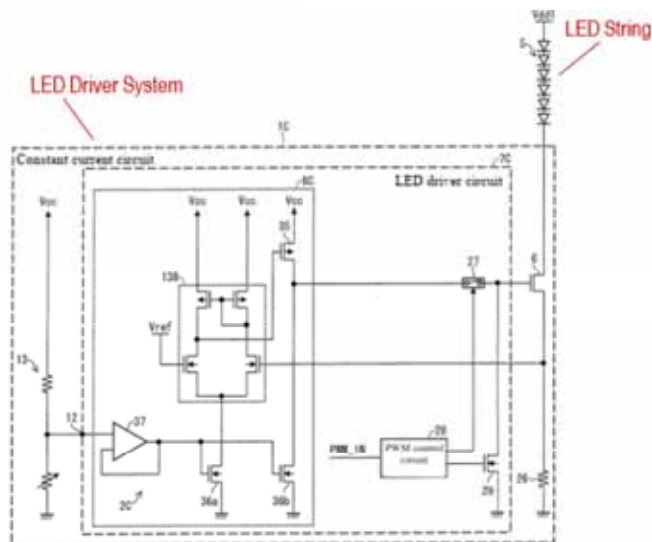
116. Sudhaus discloses apparatus for supplying electrical consumer (load) with electrical energy. Ex1005, 2:25-27, Figure 1. Sudhaus further discloses,

the electrical consumer can be chain of LEDs. Ex1005, 4:29-30.



b) Grounds 2-5: Claim [1.pre]

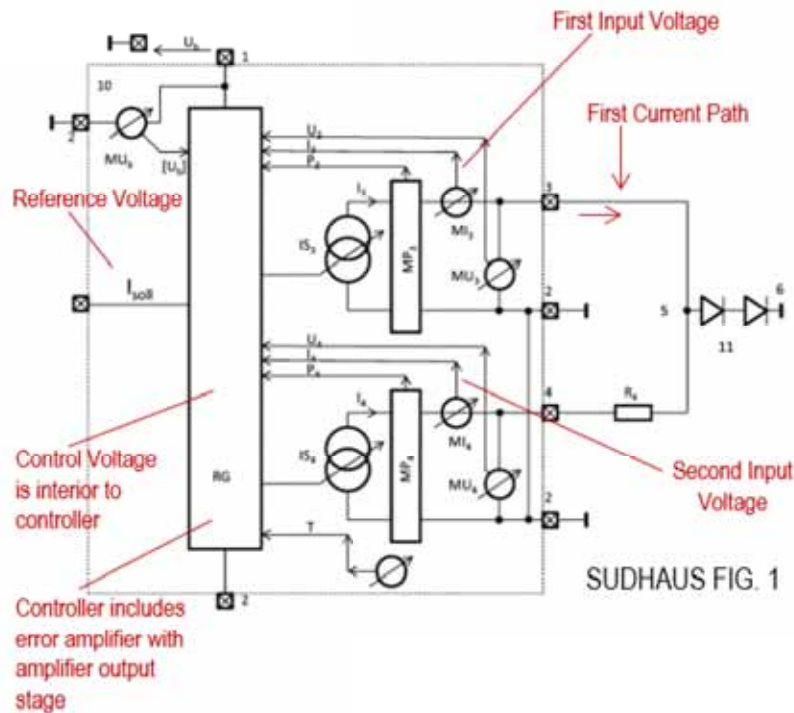
117. In addition to Sudhaus, Ryoichi discloses light-emitting diode (LED) driver system (e.g., “light-emitting-diode actuation circuitry,” Ex1006 ¶ [0082], Fig. 5.



[1.1]	an error amplifier configured to compare an input voltage with a reference voltage to generate a control voltage; and an amplifier output stage configured to control an output current through a first current path
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c) **Grounds 1–5:** Claim [1.1]

118. An error amplifier is an electrical circuit that detects a difference between two electrical signals and outputs a signal based on the difference.
119. Sudhaus discloses a controller RG that performs the functions of an error amplifier and amplifier output stage.
120. Sudhaus discloses control circuits to control two outputs supplying current to consumer (LED load). Ex1005, 2:32-33. Controller RG is operative to control two currents based on a desired value for I_{soll} . Ex. 1005, 4:46-50, Fig. 1. Sudhaus: “[a] controller RG is operative to control the current sources IS_3 and IS_4 with the aid of these measurement values and optionally with the aid of control instructions received from external sources, here a desired value I_{soll} ...” Ex1005, 4:46-50, Fig. 1.



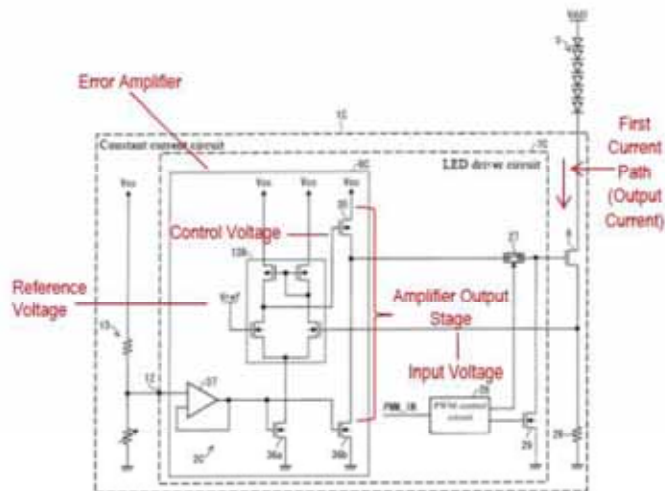
121. Controller RG may be implemented by either analog or digital circuits. Ex. 1005, 8:47-55. Controller RG has output signals to control currents IS_3 and IS_4. Ex1005, 4:25-28, Fig. 1.
122. First output (labeled 3) from controller RG controls current source IS_3 and accordingly current through first current path. (analogous to Claim 1.1 amplifier output stage).

d) Grounds 2–5: Claim [1.1]

123. In addition to Sudhaus, and alternatively, Ryoichi discloses a transistor level circuit diagram of an operational amplifier including an amplifier output stage, used for controlling current for an LED.

124. Ryoichi discloses an operational amplifier that controls a driving transistor current based on a reference value. Ex1006, ¶ [0019]. The operational amplifier includes “[a]n output control circuit, which is disposed between the aforementioned comparator-amplifier circuit and the aforementioned driving transistor so as to control the aforementioned driving signals.” *Id.*

125. Ryoichi discloses operational amplifier 8C in Fig 5. Ex1006 ¶ [0083].



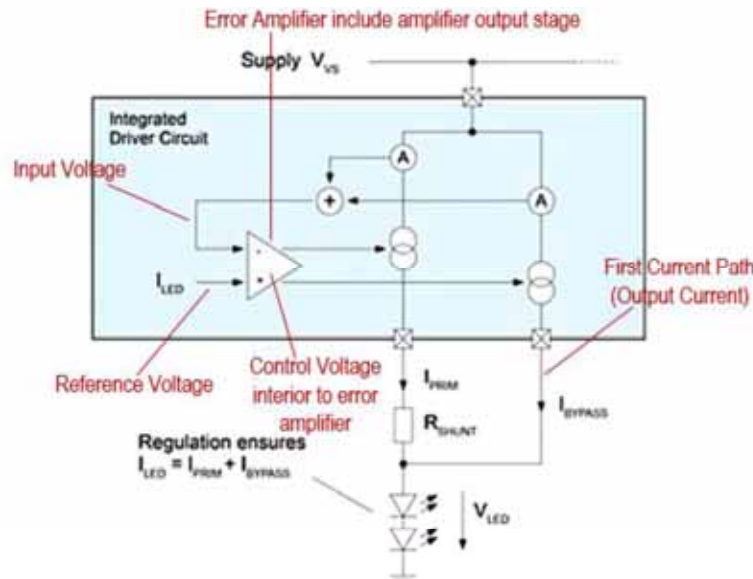
RYOICHI FIG. 5

126. Ryoichi Fig. 5 describes: operational amplifier 8C includes amplifier output stage consisting of transistors 35 and 36b. Ex1006; ¶ [0083]. Transistor 35 is controlled by output of differential part 138 (control voltage); the amplifier output stage (transistors 35/36b) controls first current path (transistor 6/resistor 26), providing current to LED load 5. *Id.*

e) **Grounds 3–5**: Claim [1.1]

127. In addition and alternatively to Sudhaus and Ryoichi, Praxis discloses an analog error amplifier including two outputs to respectively control two current sources. The error amplifier controls a total current from the two current sources delivered to an LED load based on a reference value.

Ex1008, page 3, Section titled “Modern linear regulators with a power distribution,” lines 7-14; and Fig. 1. First output controls first current path.



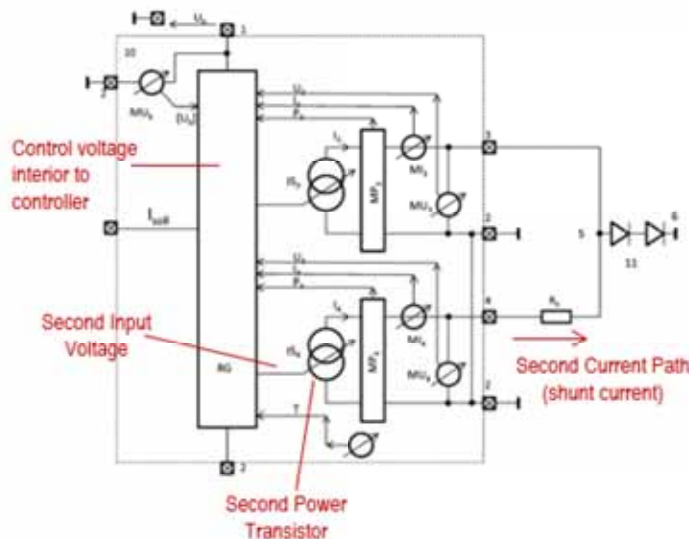
PRAXIS FIG. 1

[1.2]

and a shunt current through a second current path based on the control voltage,

f) **Grounds 2–5**: Claim [1.2]

128. Fig. 1 of Sudhaus discloses a second output 4, driven by current source IS_4 that supplies a shunt current through a second current path based on the control voltage. Ex1005, 4:46-50, Fig. 1.



SUDHAUS FIG. 1

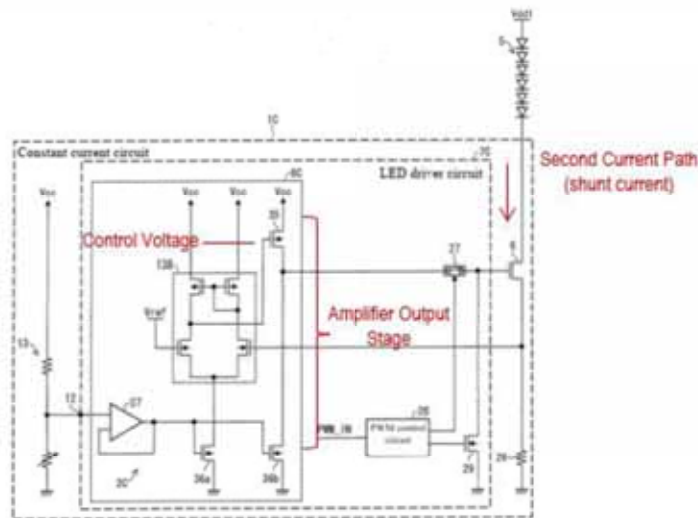
129. The controller RG is operative to control a sum of the currents through the first and second current paths based on a reference value I_{sol}. Ex1005, 4:46-50, Fig. 1. The control voltage is an internal signal to the Controller RG.

g) Grounds 2–5: Claim [1.2]

130. In addition to Sudhaus, and alternatively, Ryoichi Fig. 5 shows a controller for regulating a current through a current path based on a control voltage. Ex1006, Fig. 5, ¶ [0083]. For example, operational amplifier 8C, includes an amplifier output stage including transistors 35 and 36b, amplifier

output stage controlling current source (e.g., transistor 6 and resistor 26).

Transistor 35 in amplifier output stage is controlled by the output of differential part 138 (the control voltage). Ryoichi Fig. 5 shows: amplifier output stage (transistors 35/36b) controls current path (e.g., transistor 6/resistor 26, providing current to LED load 5. Ex1006, Fig. 5.

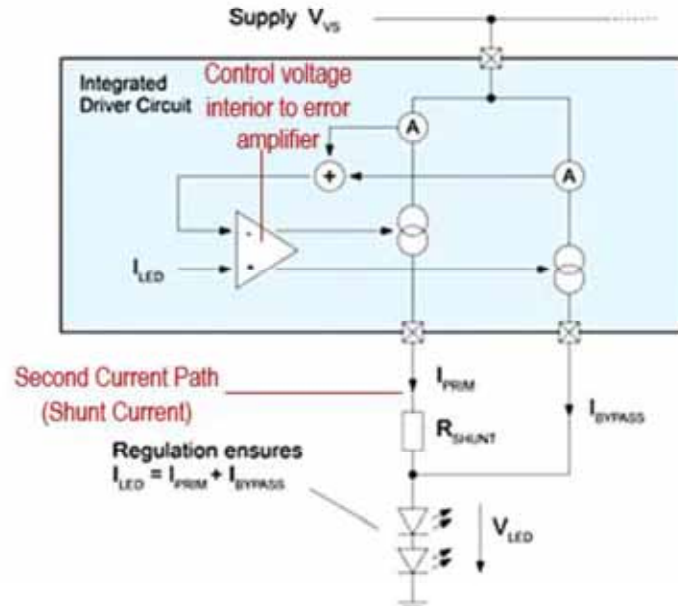


RYOICHI FIG. 5

h) Grounds 3–5: Claim [1.2]

131. In addition to Sudhaus and Ryoichi, alternatively, Praxis discloses an error amplifier having two outputs to control two current sources providing current to LED load. Ex1008, page 3, Section titled “Modern linear regulators with a power distribution,” (lines 7-14; Fig. 1). The second output controls a shunt current through the second current path. Two stage

amplifiers, as shown in Ryoichi above, are well known. The control voltage is an internal signal that controls an internal amplifier output stage in Praxis.



PRAXIS FIG. 1

[1.3]	the amplifier output stage comprising a slew-rate controller configured to control a slew-rate of a shunt current,
-------	--

233. Slew-rate is a rate of change of an electrical signal over time. A slew-rate controller is an electrical circuit that controls a rate of change of an electrical signal over time.

i) **Grounds 1–5:** Claim [1.3]

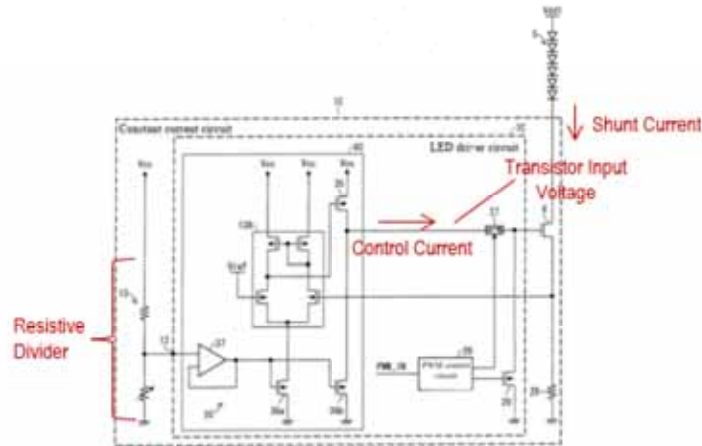
133. Sudhaus discloses slew rate control of the second current output.

Sudhaus discloses that as supply voltage increases, a portion of the total current of the two current paths is gradually taken over by the second current

path at the second connector 4 [the current path including current source IS_4 and external shunt resistor R_4]. Ex. 1005, 5:43-46. This is further emphasized: “Therefore, the second output will only *gradually* take over a part of the sum current $I_3 + I_4$. This is effected e.g. in that the first output voltage U_3 of control circuit 10 and, therefore, the voltage that decreases [is dropped] across LEDs ... is kept constant.” Ex. 1005, 6:24-29, emphasis added.

j) Grounds 2–5: Claim [1.3]

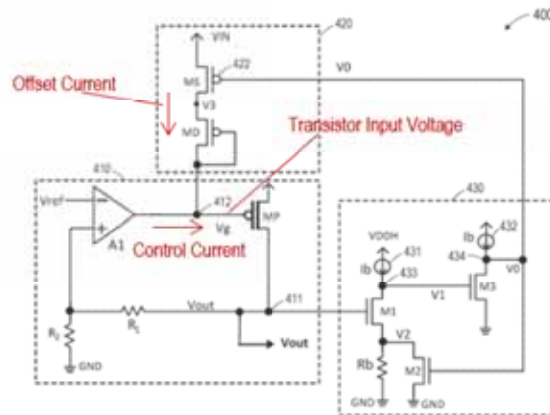
134. In addition to Sudhaus, and alternatively, Ryoichi includes slew rate control: e.g. “[t]he aforementioned integrated circuit is characterized by supplying the driving transistor with driving signals whose rise time and fall times are controllable.” Ex1006, [0017]; in reference to Fig. 5, Ryoichi shows changing constant current provided to differential stage 138 via transistor 36a and constant current provided to amplifier output stage via 36b by adjusting control voltage of transistors 36a/36b. Ex1006 ¶[0083]-[0085]. The constant current provided by transistors 35a/36b is adjusted by adjusting voltage at node 12 using resistive divider circuit 13 “thereby changing drive capability of operational amplifier 8C.” Ex1006, [0085].



RYOICHI FIG. 5

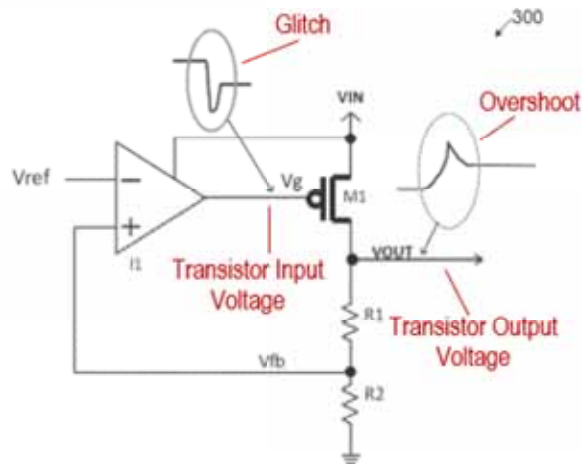
k) **Ground 4:** Claim [1.3]

135. Additionally to Sudhaus, Ryoichi and Praxis, and alternatively, Wu includes a slew-rate controller to control an output that supplies current to a load. Fig. 4 shows a slew-rate controller 420 that controls a voltage rise on the gate of an output transistor MP. Ex1009, 6:24-28.



WU FIG. 4

136. Wu illustrates a glitch that can occur on the gate of an output transistor (here, M1), and a resulting peak that can occur at the output V_OUT. Ex1009, 5:47-48.



WU FIG. 3

137. Wu's slew-rate controller prevents glitches on the output transistor gate and consequently the output peak. Ex1009, 8:33-40.

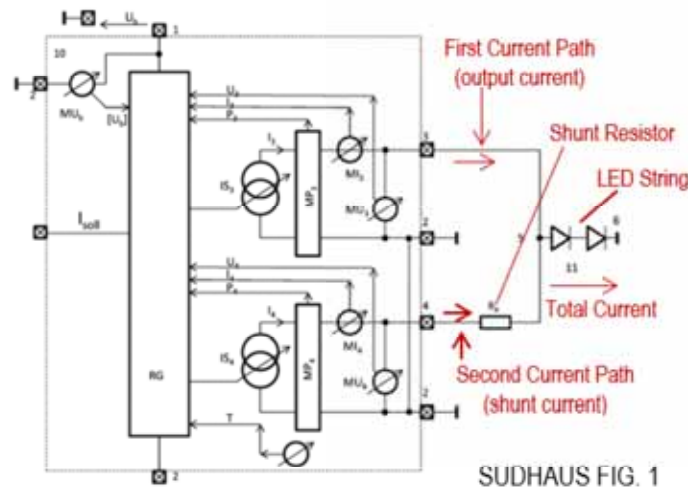
l) Ground 5: Claim [1.3]

138. Alternatively, the combination of Provost, TI Paper and UK Paper provide a slew-rate controller as described in detail in reference to claim 5.

[1.4]	the shunt current provided through a shunt resistor in the second current path and added to the output current to provide a total current through an LED string.
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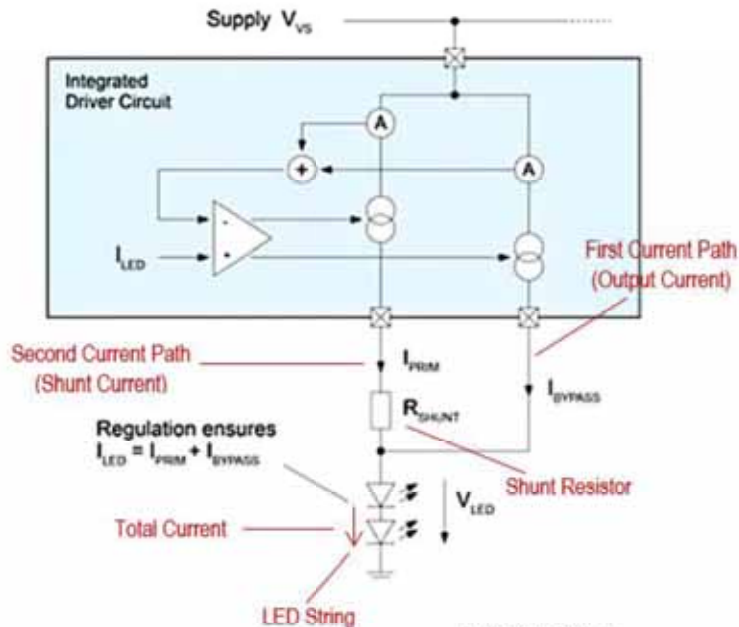
m) Grounds 1-5: Claim [1.4]

139. Sudhaus discloses, in reference to Fig. 1, providing an output current through a first current path and a shunt current that a second current including an external resistor. Ex1005, 4:25-32. The second current path includes the current source IS_4 and resistor R_4 . Ex1005, 4:30-32. Sudhaus further discloses that controller RG is operative to control the total of the two output currents based on a desired value I_soll . Ex1005, 4:46-50, Fig. 1. The total current is delivered to an LED string 11.



n) Grounds 3–5: Claim [1.4]

140. Additionally to Sudhaus and Ryoichi, and alternatively, Praxis discloses an error amplifier having two outputs to control two current sources providing current to LED load. Ex1008, page 3, Section titled “Modern linear regulators with a power distribution,” lines 7-14; and Fig. 1. Second output controls second current path.



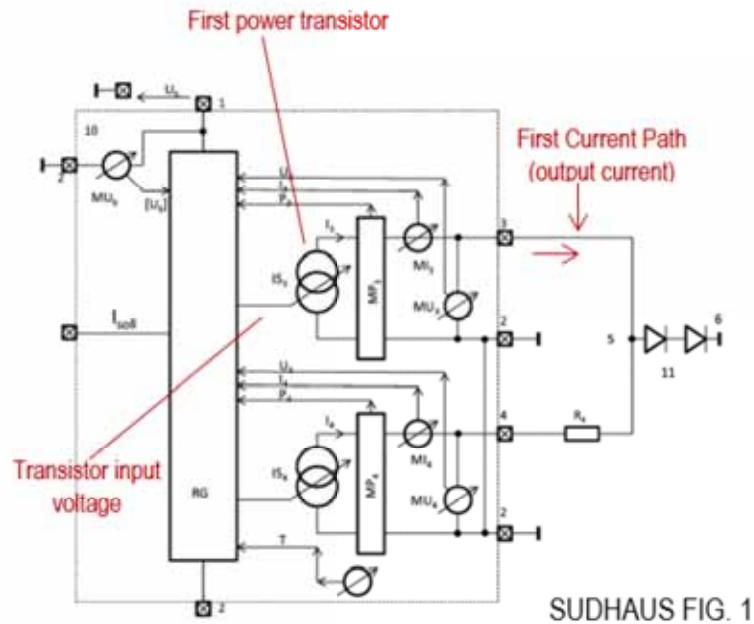
PRAXIS FIG. 1

B. Claims 2 (broken into elements [2.1] and [2.2] presented below) are unpatentable under Grounds 1-5

[2.1]	The system of claim 1, further comprising: a first power transistor configured to conduct the output current in the first path based on a first transistor input voltage; and
-------	---

a) Grounds 1–5: Claim [2.1]

141. Sudhaus discloses: a power transistor to conduct output current based upon a first input voltage.



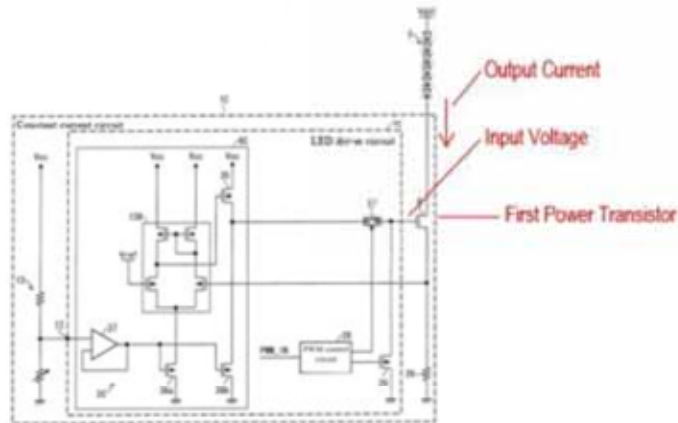
142. First output (3) driven by current source IS_3 is configured to conduct current in first current path based on current source IS_3 input voltage (signal from RG controlling IS_3). Ex1005, 4:46-50, Fig. 1. “[a] controller RG is operative to control the current sources IS_3 and IS_4 with the aid of these measurement values and optionally with the aid of control instructions received from external sources, here a desired value I_{soll} ... Ex1005, 4:46-50, Fig. 1.

143. Sudhaus’ current sources (such as IS_3 and IS_4) include “controlling transistor(s).” Ex1005, 1:65-2:14; “controlling transistor” can be understood to be output transistors (power transistors) of current source. e.g., “[t]he disclosure (Sudhaus) is founded on the recognition that, basically, a transistor which is the controlling transistor of a current source,

can in the broadest sense be considered as an adjustable resistor. If this transistor has a medium resistance value, a maximum of power will drop across the transistor.” Ex1005, 1:65-2:2.

b) Grounds 2–5: Claim [2.1]

144. In addition to Sudhaus, and alternatively, Ryoichi discloses driving transistor 6. Ex1006, ¶[0083], Fig. 5.



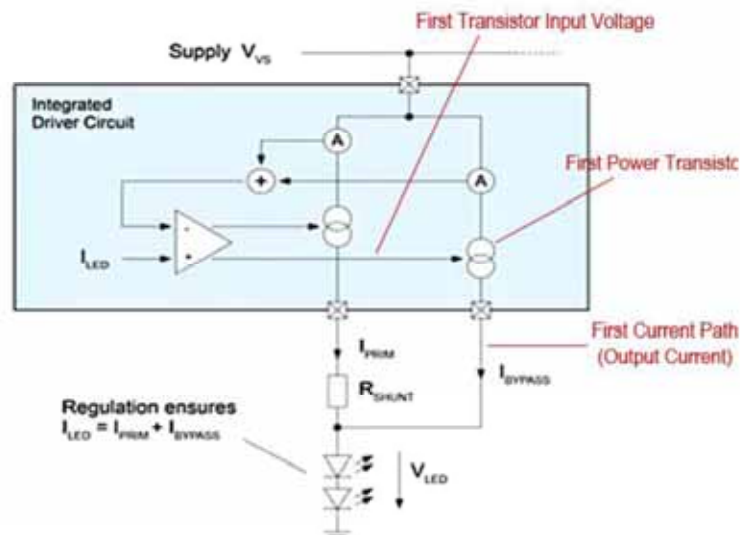
RYOICHI FIG. 5

145. Ryoichi Fig. 5 shows: first transistor 6 receives input voltage on gate input of transistor 6, input voltage being provided by amplifier output stage (transistors 35/36b). Current through transistor 6 (current in first path) is based on this input voltage. Ex. 1006, ¶[0083], Fig. 5.

c) Grounds 3–5: Claim [2.1]

146. In addition to Sudhaus and Ryoichi, and alternatively, Praxis discloses an error amplifier having two outputs to control two current sources

providing current to LED loads. Ex1008, page 3, Section titled “Modern linear regulators with a power distribution,” lines 7-14; and Fig. 1. Two current sources include first current source to conduct current through first current path.

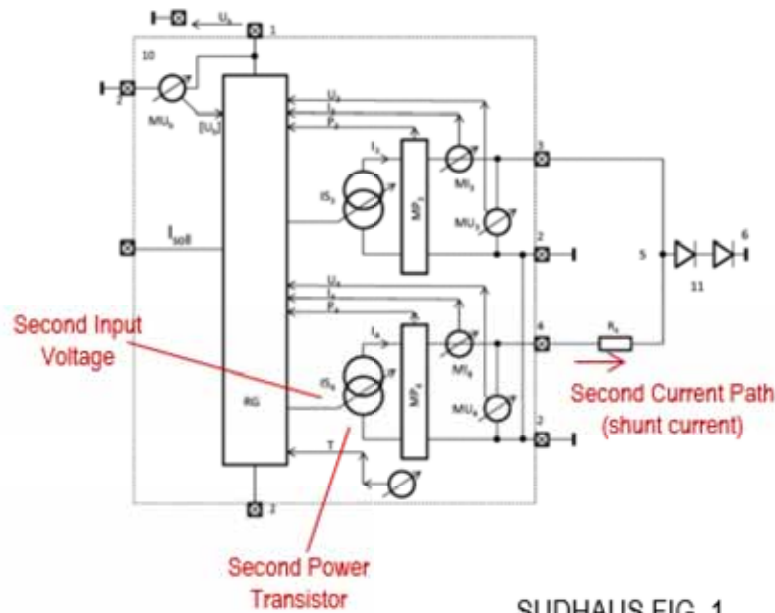


PRAXIS FIG. 1

[2.2]	a second power transistor, configured to conduct the shunt current in the second current path based on a second transistor input voltage,
-------	---

d) Grounds 1–5: Claim [2.2]

147. Sudhaus discloses first and second current sources IS_3 and IS_4 to drive respectively first and second current paths. Ex1005, 4:46-47, Fig. 1.



SUDHAUS FIG. 1

148. Sudhaus discloses, controller RG controlling second current path IS_4 and resistor R_4 based on input voltage to second current source IS_4.

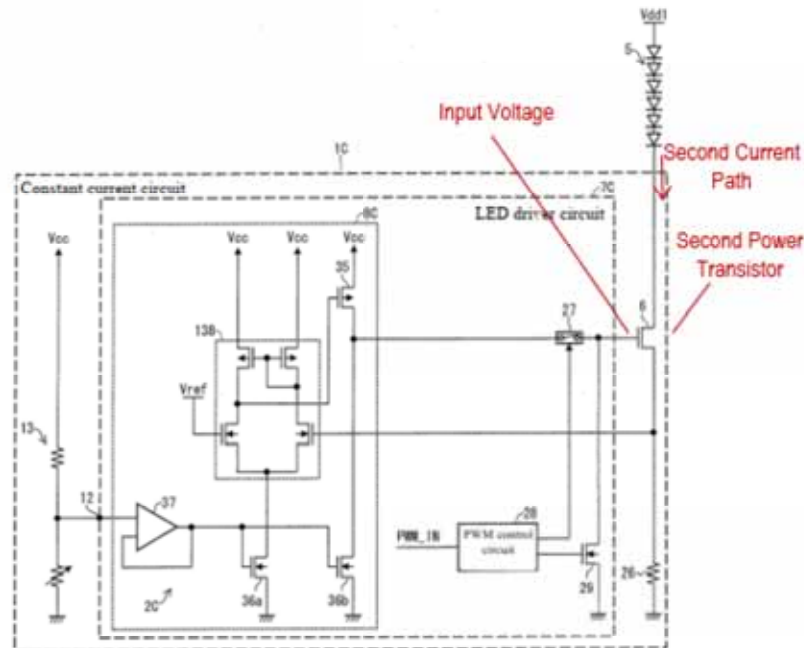
Ex1005, 4:46-47. E.g., Sudhaus states: “Fig. 1 shows an exemplary control circuit 10. Said control circuit comprises two outputs 3, 4, and for each of these outputs 3, 4, an associated current source IS_3 and IS_4.” Ex1005, 4:25-26, Fig. 1. Sudhaus teaches: controller RG is operative to control two current sources. Ex1005, 4:46-47.

149. Current sources (such as IS_3 and IS_4) in Sudhaus include a “controlling transistor.” Ex1005, 1:65-2:2.

e) **Grounds 2–5:** Claim [2.2]

150. In addition to Sudhaus, and alternatively, Ryoichi Fig. 5 shows: transistor 6 (power transistor) receives input voltage on gate input of

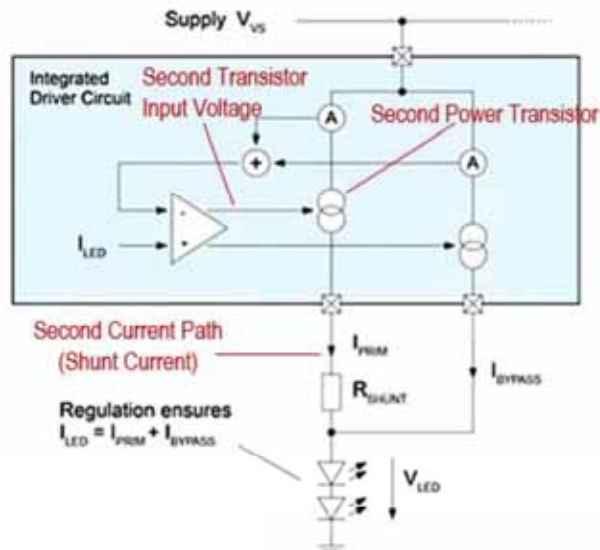
transistor 6, input voltage being provided by amplifier output stage (transistors 35/36b). Current through transistor 6 is based on this input voltage. Ex. 1006, Fig. 5.



RYOICHI FIG. 5

f) Grounds 3–5: Claim [2.2]

151. In addition to Sudhaus and Ryoichi, Praxis discloses an error amplifier having two outputs to control two current sources providing current to an LED load. Ex1008, page 3, Section titled “Modern linear regulators with a power distribution,” lines 7-14; and Fig. 1. Two current sources include a second current source to conduct current through a second current path including a shunt resistor.



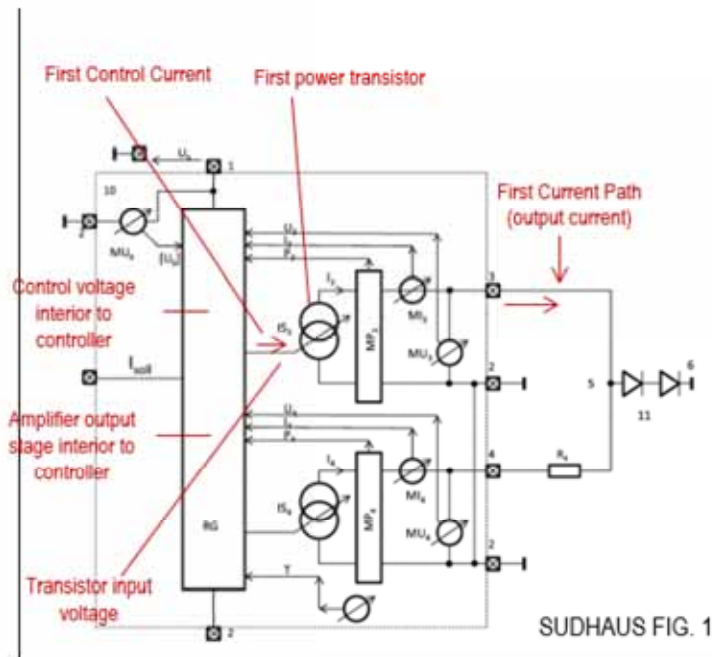
PRAXIS FIG. 1

C. Claim 3 (broken into elements [3.1] and [3.2] presented below) is unpatentable under Grounds 1-5

[3.1]	The system of claim 2, wherein the amplifier output stage comprises: a first control transistor configured to conduct a first control current based on the control voltage to generate the first transistor input voltage, and
-------	--

a) Grounds 1–5: Claim [3.1]

152. Sudhaus Fig. 1 discloses controller RG controlling first current path IS_3. Ex1005, 4:46-47, e.g., Sudhaus states: “Fig. 1 shows exemplary control circuit 10. Control circuit comprises two outputs 3, 4, and for each output 3, 4, associated current source IS_3 and IS_4.” Ex1005, 4:25-26, Fig. 1. Controller RG is operative to control two current sources. Ex1005, 4:46-47. Controller RG includes an output that generates first control current to generate voltage to control input of first current source IS_3.

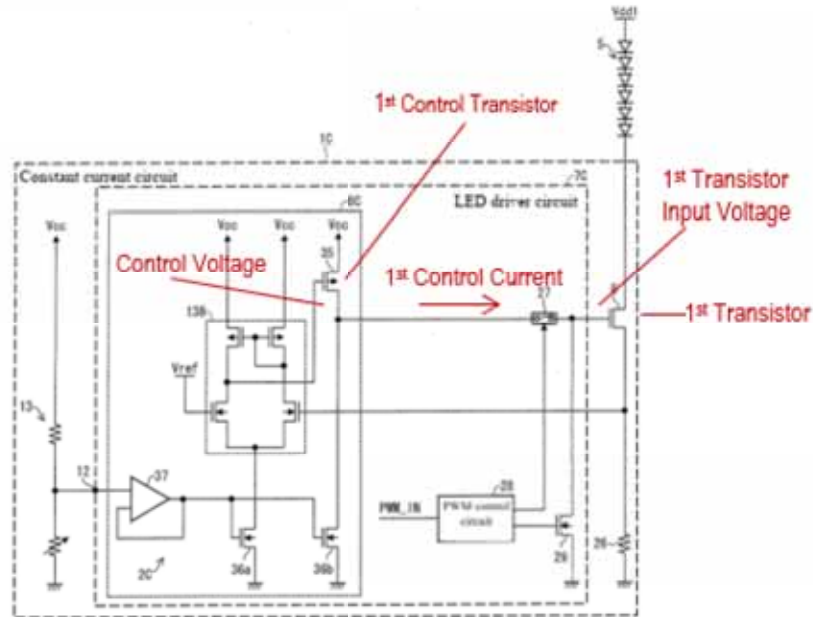


153. Sudhaus discloses that current sources (such as IS_3 and IS_4) include a power transistor referred to as a controlling transistor. Ex1005, 1:65-2:14. The controller RG of Sudhaus includes an output stage that generates the current used to drive the power transistor in IS_3. This output stage includes at least one control transistor.

b) Grounds 2–5: Claim [3.1]

154. In addition to Sudhaus, and alternatively, Ryoichi Fig. 5 shows: operational amplifier 8C includes amplifier output stage consisting of transistors 35/36b. Ex1006, Fig. 5. Transistor 35 (control transistor) is controlled by output of differential part 138 (control voltage). Ex1006, Fig. 5. First control transistor 35 is configured to conduct current (control

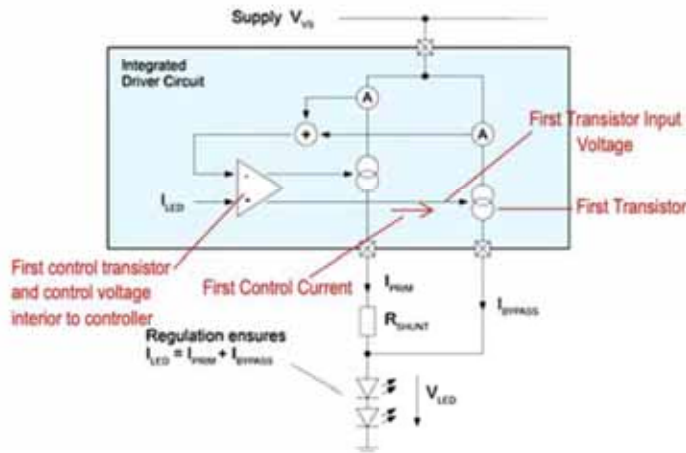
current) to drive control input of driving transistor 6 (generate first transistor input voltage).



RYOICHI FIG. 5

c) **Grounds 3–5:** Claim [3.1]

155. In addition to Sudhaus and Ryoichi, and alternatively, Praxis discloses error amplifier having two outputs to control two current sources providing current to LED load. Ex1008, page 3, Section titled “Modern linear regulators with a power distribution,” lines 7-14; and Fig. 1. The error amplifier includes first output to control first current source.

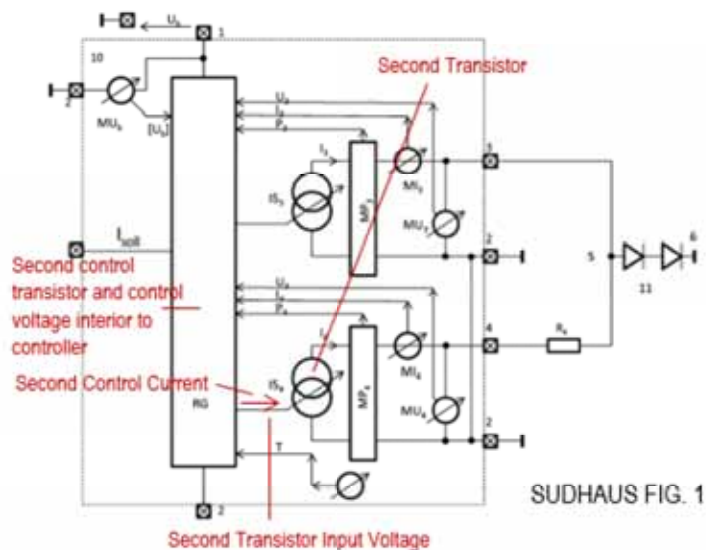


PRAXIS FIG. 1

[3.2]	a second control transistor to conduct a second control current based on the control voltage to generate the second transistor input voltage.
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d) Grounds 1–5: Claim [3.2]

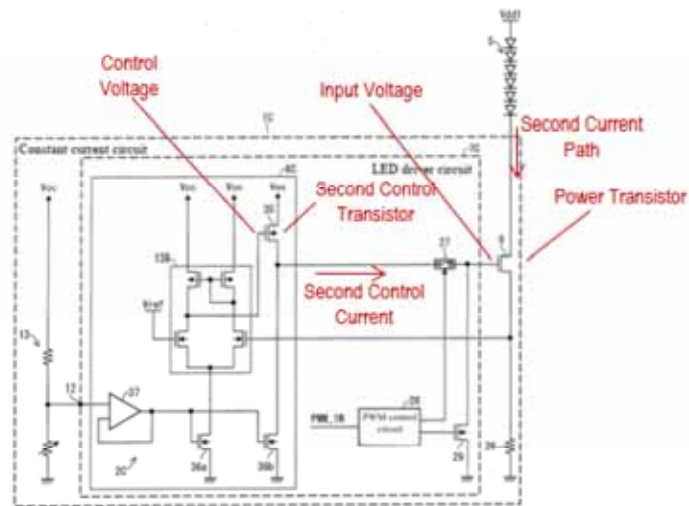
156. Sudhaus Fig. 1 discloses, controller RG controlling second current path IS_4 and R_4. Ex1005, 4:46-47. Sudhaus teaches: controller RG is operative to control two current sources. Ex1005, 4:46-47. Control current from second RG output generates voltage to control input of second current source IS_4.



157. Sudhaus discloses that current sources (such as IS_3 and IS_4) include a power transistor referred to as a controlling transistor. Ex1005, 1:65-2:14. The controller RG of Sudhaus includes an output stage that generates current used to drive the power transistor in IS_4. The output stage includes at least one transistor.

e) **Grounds 2-5: Claim [3.2]**

158. In addition to Sudhaus, and alternatively, Ryoichi Fig. 5 shows: operational amplifier 8C includes amplifier output stage including transistors 35/36b. Ex1006, Fig. 5. Transistor 35 (control transistor) is controlled by output of differential part 138 (control voltage). Ex1006, Fig. 5. First control transistor 35 is configured to conduct current (control current) to drive control input of driving transistor 6 (generate first transistor input voltage).

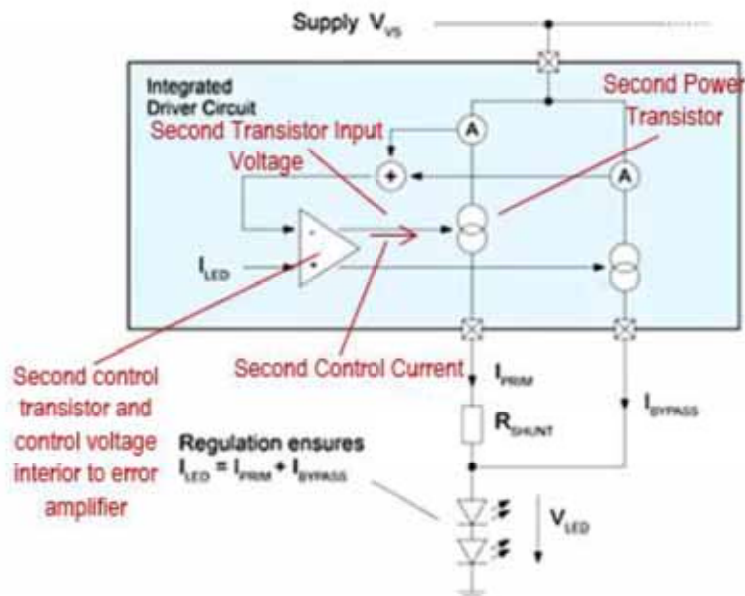


RYOICHI FIG. 5

f) Grounds 3–5: Claim [3.2]

159. In addition to Sudhaus, Praxis discloses an error amplifier having two outputs to control two current sources providing current to LED load.

Ex1008, page 3, Section titled “Modern linear regulators with a power distribution,” lines 7-14; and Fig. 1. Error amplifier includes first output to control first current source.



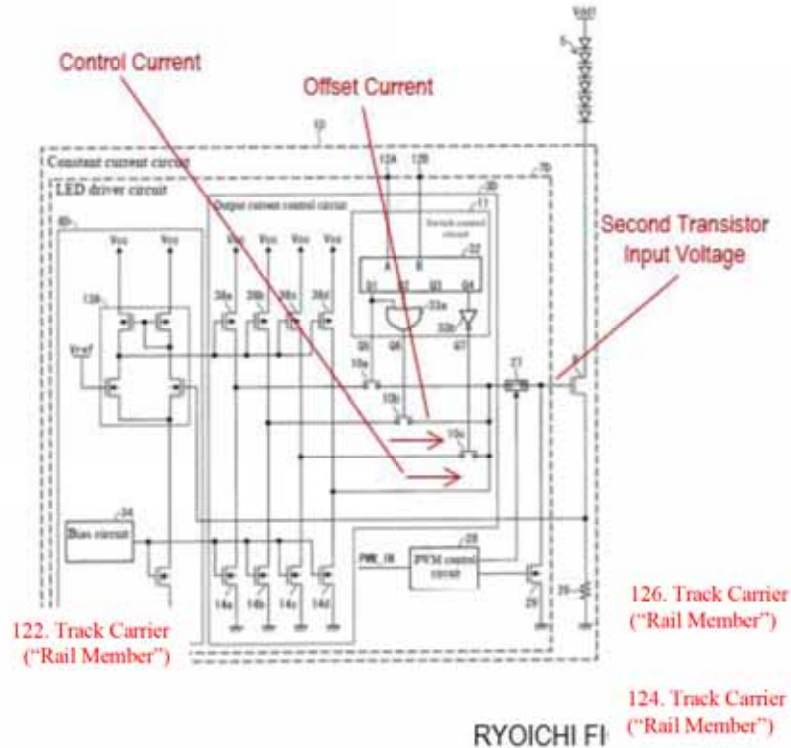
PRAXIS FIG. 1

D. Claim 4 (broken into elements [4.1] and [4.2] presented below) is unpatentable under Grounds 2-5

[4.1]	The system of claim 3, wherein the slew-rate controller is configured to conduct an offset current in parallel with the second control current to generate the second transistor input voltage,
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a) Grounds 2–5: Claim [4.1]

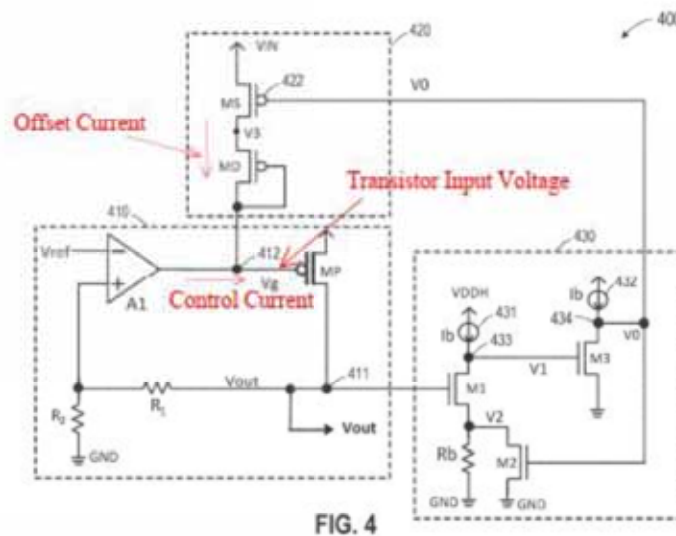
160. Fig. 6 of Ryoichi discloses a slew-rate controller including multiple parallel paths to generate control current and offset current for first transistor input voltage.



161. In Fig. 6, the amplifier output stage of Ryoichi Fig. 5 (essentially transistors 35/36b), has been replaced by transistors 38a, 38b, 38c, 38d (corresponding to transistor 35 of Fig. 5) combined with transistors 14a, 14b, 14c, 14d (corresponding to transistor 36b of Fig. 5. ¶¶ [0087]-[0088]. The drive capability of the amplifier output stage can be adjusted by selecting how many of transistors 38a, 38b, 38c, 38d and corresponding transistors 14a, 14b, 14c, 14d are coupled via switches 10a, 10b, 10c to drive driving transistor 6, effectively switching in (or out) an offset current by the switching in or out of a transistor pair (e.g., 14c and 38c as shown above). This allows adjusting rise time and fall time of the driving signal applied to the driving transistor 6. Ex. 1006, ¶¶ [0089]-[0092].

b) Ground 4: Claim [4.1]

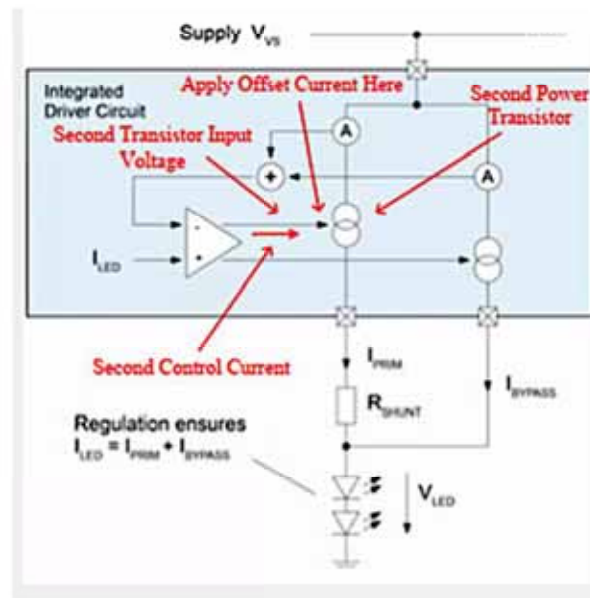
162. As another alternative, Wu teaches sourcing a negative offset current (current reducing slew rate of transistor MP) from a positive supply voltage. e.g., Wu Fig. 4 discloses a slew rate control circuit 420 that introduces offset into a control node of power transistor MP. Ex. 1009, 6:24-28.



Wu Fig. 4

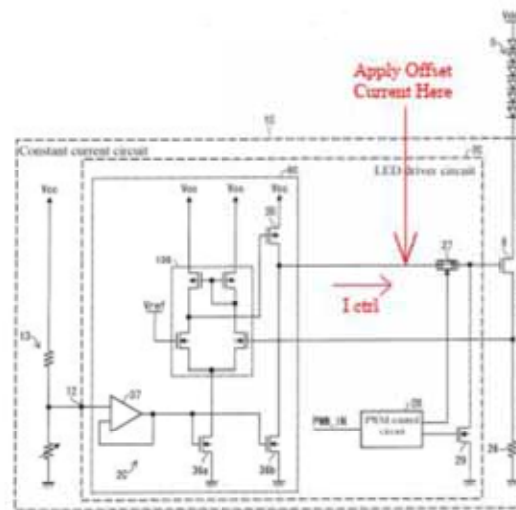
163. This is intended to avoid a glitch on input of M1 and resulting overshoot at the output of power transistor MP shown in Wu, Fig. 3.

168. Alternatively, the output of Wu can be applied, for example, to an input of a second power transistor of Praxis, as shown below. Ex1008, page 3, Section titled “Modern linear regulators with a power distribution,” lines 7-14; and Fig. 1.



Praxis Fig. 1

169. Alternatively, output of Wu can be applied, e.g., to input of transistor 6 of Ryoichi, Fig. 5. Ex1006, Fig. 5.



Ryoichi Fig. 5

c) **Ground 5:** Claim [4.1]

170. The combination of Provost and TI Paper provide an offset current controlled by a ramp voltage. Provost discloses on-chip ramp generator in Fig. 4. Ex1010, Fig. 4.

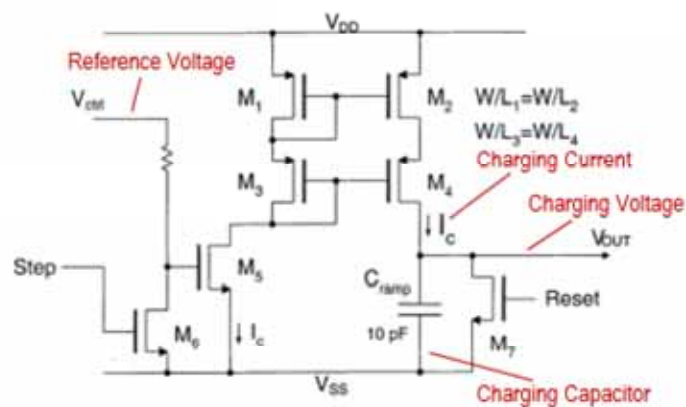


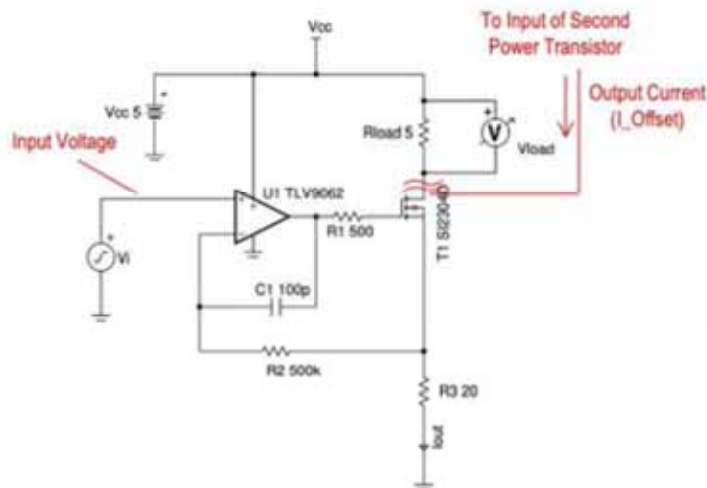
Fig. 4. Schematic of the basic current source of first analog ramp generator.

PROVOST FIG. 4

171. In the on-chip ramp driver of Provost, Fig. 4, transistor M5 is a current driver, M1-M4 form a cascode current mirror, and C_ramp is

charging capacitor. M6 is used for stopping current source when Step is at logic 1. M7 is used to reset C_ramp. I_c is the charging current that charges C_ramp to generate charging voltage V_OUT. Ex1010, page 264, Adaptive Scheme, line 23 – page 265, Adaptive Scheme, line 32.

172. Based on ramp generated by the on-chip ramp generator, offset current can be generated using voltage-to-current converter, such as disclosed in TI Paper, Ex1011. TI Paper, in Fig. 1, discloses voltage-to-current converter.



TI PAPER FIG. 1

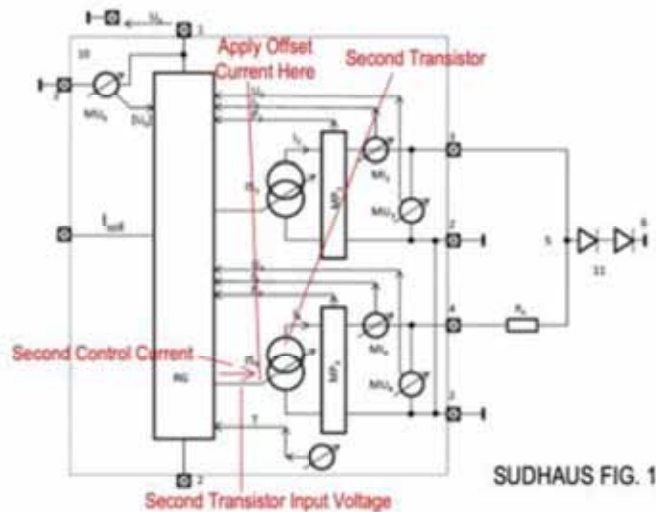
173. Ex1011, page 1. Here, the output current is given by:

$$I_o = \frac{V_i}{R_3}$$

Ex1011, page 2, lines 1-2.

174. To generate offset current for current application, output of on-chip ramp generator V_{outf} can be applied as V_i to voltage-to-current converter of TI Paper.

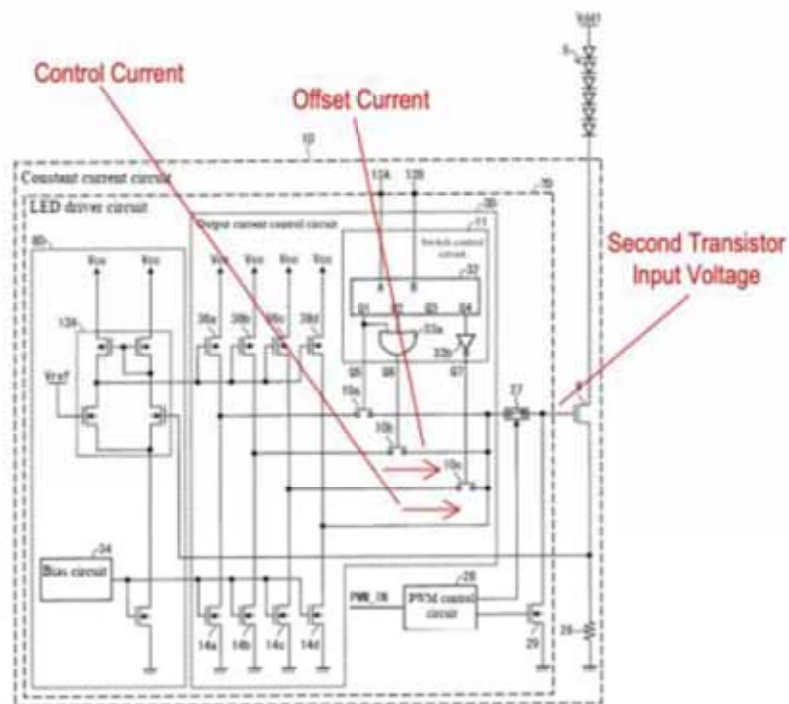
175. Output current I_o of voltage-to-current converter can be applied as current I_{offset} , for example, to the second transistor of Sudhaus. Ex1005, Fig. 1.



176. Alternatively, offset current I_{offset} can be applied to input of second current source of Praxis. Ex1008, page 3, Section titled “Modern linear regulators with a power distribution,” lines 7-14.

d) **Ground 2-5:** Claim [4.2]

178. Referring to Fig. 6 of Ryoichi, slew rate will be at lower level, e.g., if only one pair of transistors, for example transistors 38d/14d are connected to the gate of driver transistor 6, and will be at another, higher level (faster) if one or more pair of transistors, e.g., 38c/14c is switched in. Accordingly, offset current (current introduced by current pair 38c/14c) increases as slew rate increases. 6. Ex1006, ¶¶ [0089]-[0092].



RYOICHI FIG. 6

e) **Ground 4:** Claim [4.2]

179. Alternatively, a controlled slew rate of Wu can be applied, for example, to second power transistor of Sudhaus (Ex1005, Fig. 1), to second power transistor input of Praxis (Ex1008, page 3, Section titled “Modern linear regulators with a power distribution,” lines 7-14, and Fig. 1), or to input of transistor 6 of Ryoichi, Fig. 5, EX1006, Fig. 5) until slew-rate control circuit 420 is turned off. Ex1009, 7:52-63. Adding negative offset current (i.e., source current) to a control gate of a power transistor as it is turning on to control a slew rate, and then turning it off at preset voltage, causes an effective increase in sink current (current increasing slew rate) applied to a gate.

f) Ground 5: Claim [4.2]

180. Alternatively, based on Provost and TI Paper, applying the ramp voltage V_{out} of Provost to an input of voltage-to-current converter of the TI Paper generates an offset current (I_{out} of V-I converter) that changes with slew rate of ramp.

E. Claim 5 (broken into elements [5.1 – 5.3] presented below) is unpatentable under Ground 5

[5.1]	The system of claim 4, wherein the slew-rate controller comprises: a charging current generator configured to generate a charging current;
-------	--

a) Ground 5: Claim [5.1]

181. Provost discloses on-chip ramp generator in Fig. 4 including charging current generator.

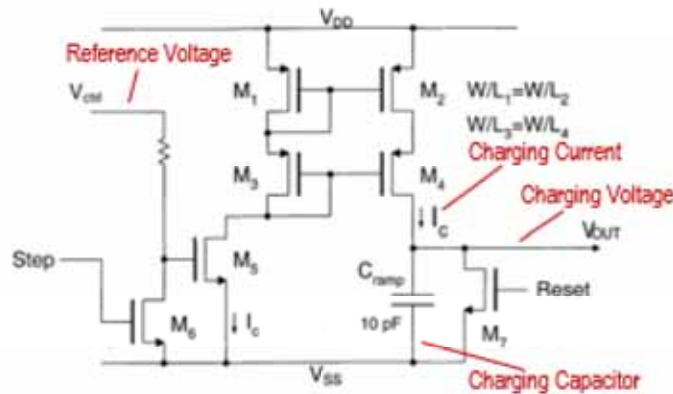


Fig. 4. Schematic of the basic current source of first analog ramp generator.

PROVOST FIG. 4

182. In on-chip ramp driver of Provost, Fig. 4, transistor M5 together with M1-M4 form charging current generator. Charging current I_c charges C_{ramp} to generate charging voltage V_{OUT} . Ex1010, page 264, Adaptive Scheme, line 23 – page 265, Adaptive Scheme, line 32.

[5.2]	a charging capacitor that is charged by a charging current to generate a charging voltage;
-------	--

b) Ground 5: Claim [5.2]

183. Provost Fig. 4 shows charging a charging capacitor C_{ramp} with charging current I_c to generate a charging voltage. Ex1010, page 264, Adaptive Scheme, line 23 – page 265, Adaptive Scheme, line 32.

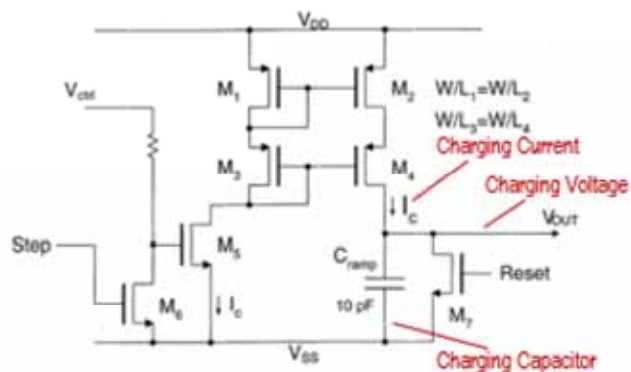


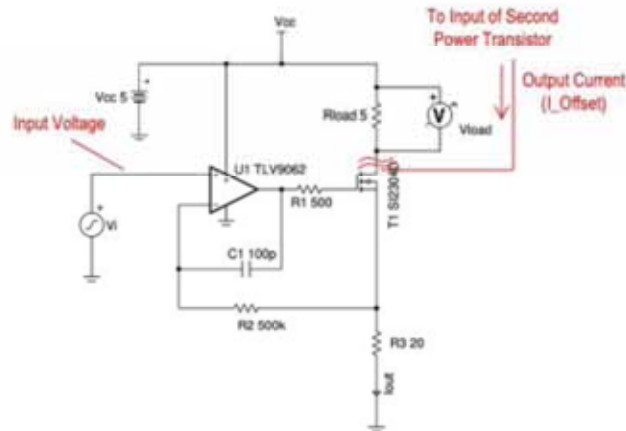
Fig. 4. Schematic of the basic current source of first analog ramp generator.

PROVOST FIG. 4

[5.3]	a current mirror configured to conduct the offset current based on the charging voltage.
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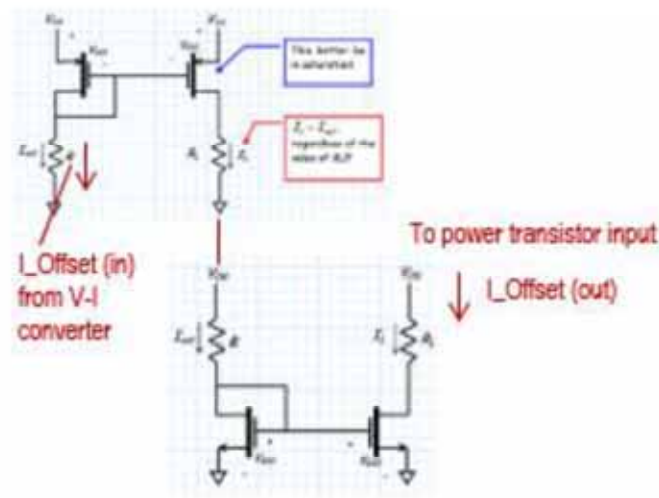
c) **Ground 5:** Claim [5.3]

184. Based on ramp (Charging Voltage) generated by on-chip ramp generator, offset current can be generated using voltage-to-current converter, such as disclosed in TI Paper, Ex1011. TI Paper, in Fig. 1, discloses voltage-to-current converter.



TI PAPER FIG. 1

185. To generate offset current for current application, output of on-chip ramp generator V_{outf} can be applied as V_i to voltage-to-current converter of TI Paper.
186. Current I_{Offset} from voltage-to-current converter can be delivered to input of second power transistor via current mirrors if necessary.
187. UK Paper, Ex1012, discloses NMOS/PMOS current mirrors. Ex1012, Fig. page 2, Fig. page 6.
188. PMOS Current Mirror (Fig. page 6)



NMOS Current Mirror (Fig. page 2)

189. Where, if transistors in transistor pairs are dimensioned similarly, I_{ref} will equal I_L for both NMOS Current Mirror and the PMOS Current Mirror. Ex1012, page 3. One PMOS current mirror together with one NMOS current mirror can be used to conduct offset current based on charging voltage as shown above.

F. Claim 6 is unpatentable under Grounds 1-5

6	The system of claim 1, wherein the amplifier output stage is configured to increase an amplitude of the shunt current and decrease an amplitude of the output current as the supply voltage increases.
---	--

a) Grounds 1-5: Claim 6

190. Sudhaus discloses: as supply voltage increases, portion of total current of two current paths is gradually taken over by second current path [current

path including external shunt resistor]. Ex1005, 5:43-46. Sudhaus states:

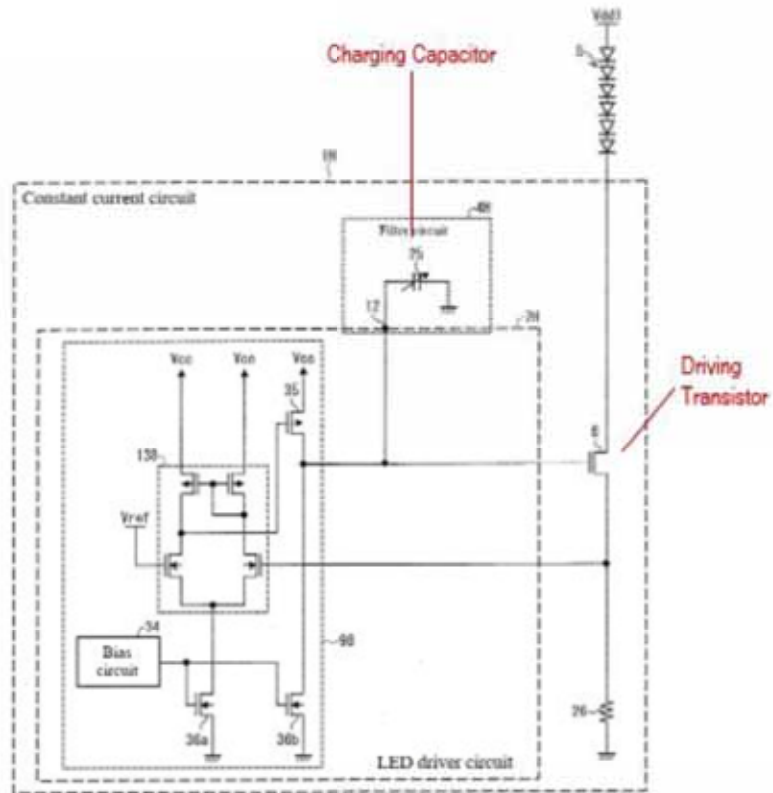
“[i]n a second operating current range B, the current is gradually taken over by the second current path at the second connector 4 with the second resistor R4.” Ex1005, 5:43-46.” That is, with increasing supply voltage, amplitude of shunt current increases and amplitude of output current (current path without shunt resistor) decreases.

G. Claim 7 is unpatentable under Grounds 2-5

7	The system of claim 1, wherein the slew-rate controller comprises a charging capacitor having a capacitance that defines the slew-rate of the shunt current.
---	--

a) Grounds 2–5: Claim 7

191. Ryoichi teaches slew-rate controller comprising charging capacitor having capacitance that defines slew rate of control signal to driving transistor in reference to Fig. 10. Ex1006, Fig. 10.



RYOICHI FIG. 10

192. In Ryoichi Fig. 10, variable capacitor 25 can be adjusted to adjust rise/fall time of output stage of operational amplifier 98. Ex1006, ¶ [0104].

b) Ground 5: Claim 7

193. Provost Fig. 4 discloses on-chip ramp generator including charging capacitor C_{ramp}. Ex1010, Adaptive Scheme, page 264 line 23 – page 265 line 32.

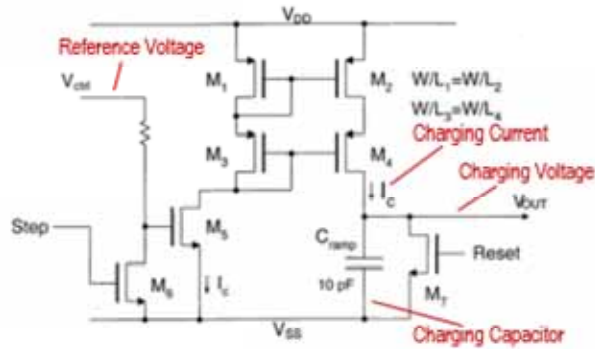
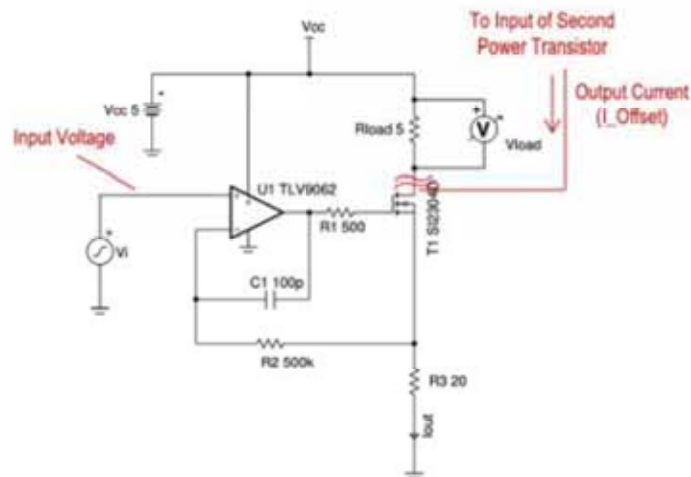


Fig. 4. Schematic of the basic current source of first analog ramp generator.

PROVOST FIG. 4

194. Based on ramp generated by on-chip ramp generator, offset current can be generated using voltage-to-current converter, such as disclosed in TI Paper, Ex1011. TI Paper, in Fig. 1, discloses voltage-to-current converter.



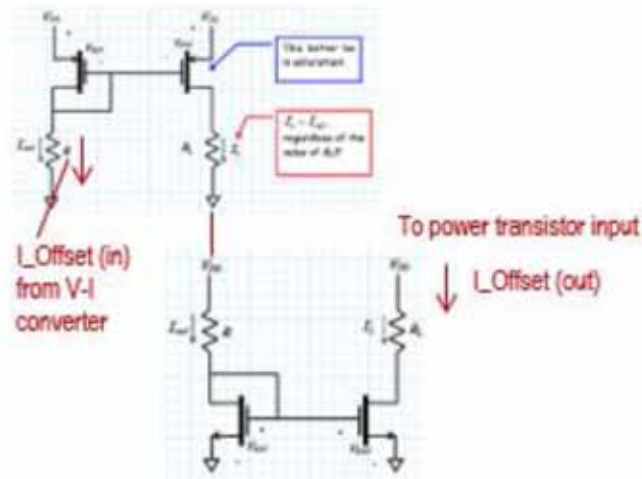
TI PAPER FIG. 1

195. Ex1011, page 1. Here, the output current is given by:

$$I_o = \frac{V_i}{R_3}$$

Ex1011, page 2, lines 1-2.

196. To generate offset current for current application, output of on-chip ramp generator V_{out} can be applied as V_i to voltage-to-current converter of TI Paper, and output current I_{out} [I_o] of voltage-to-current converter can be applied as current I_{offset} to gate of power transistor, e.g., transistor 6 in Ryoichi Fig. 5, either directly, or via a current mirror, if required.
197. The UK Paper, Ex1012, discloses NMOS and PMOS current mirrors.



198. Converting voltage V_{out} at output of Provost to current I_{offset} at output of voltage-to-current converter of TI Paper and delivering the current I_{offset} via current mirrors as in UK Paper results in charging voltage of Provost controlling offset current via current mirror.

H. Claim 8 is unpatentable under Ground 5

[8.1]	The system of claim 7, further comprising a power transistor configured to conduct the shunt current in the second current path based on a transistor input voltage,
-------	--

a) **Ground 5:** Claim [8.1]

199. This recitation is invalid for reasons cited in reference to recitation [2.2] in claim 2.

[8.2]	wherein the charging capacitor is configured to generate a charging voltage to control an amplitude of an offset current via a current mirror,
-------	--

b) **Ground 5:** Claim [8.2]

200. Provost discloses on-chip ramp generator in Fig. 4 including charging current generator M5 and M1-M4. The charging current generates a voltage V_OUT (charging voltage) on a capacitor C_ramp (charging capacitor).

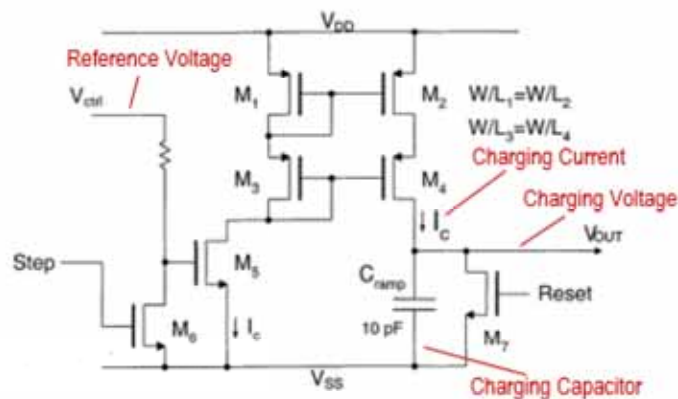
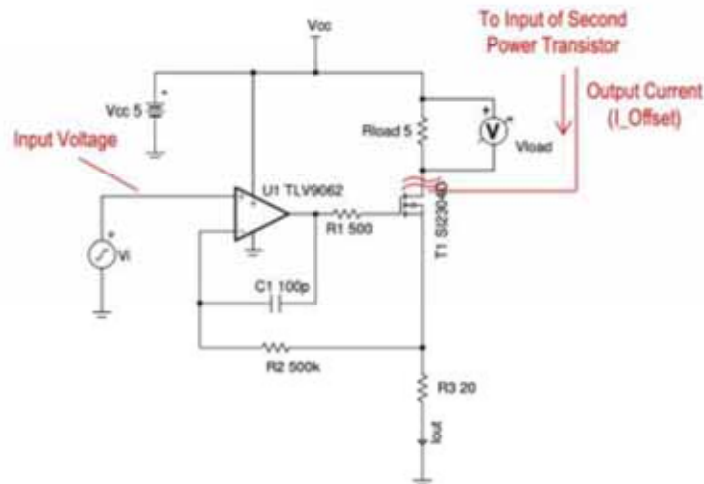


Fig. 4. Schematic of the basic current source of first analog ramp generator.

PROVOST FIG. 4

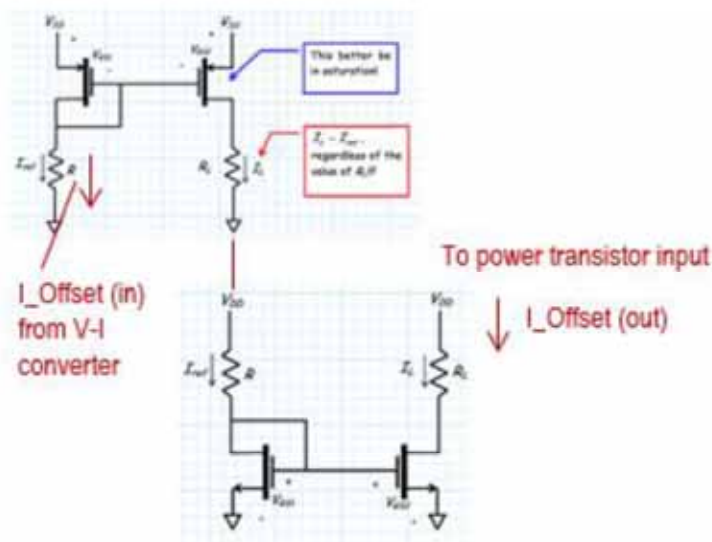
201. Ex1010, Adaptive Scheme, page 264 line 23 - page 265 line 32.

202. Based on ramp generated by on-chip ramp generator, offset current can be generated using voltage-to-current converter, such as disclosed in TI Paper, Ex1011, page 1, Fig. 1.



TI PAPER FIG. 1

203. To generate offset current for current application, output of on-chip ramp generator V_{outf} can be applied as V_i to voltage-to-current converter of TI Paper, and output current I_{out} [I_o] of voltage-to-current converter can be applied as current I_{offset} to an input to a current mirror, as shown in UK Paper.
204. UK Paper discloses NMOS/PMOS current mirrors. Ex1012, page 2, page 6.



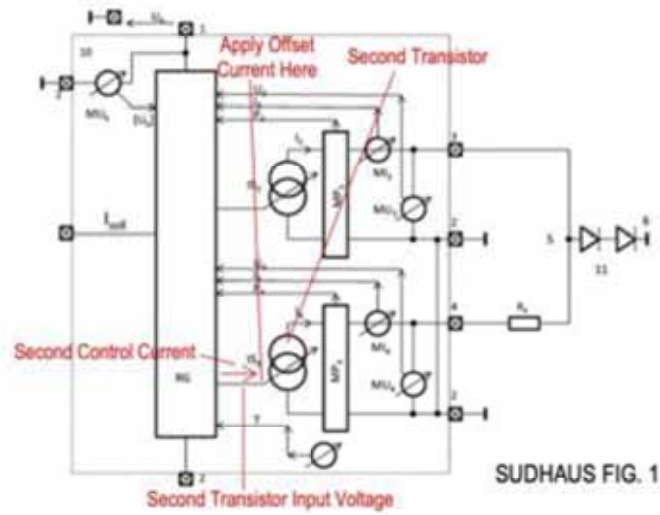
205. One PMOS current mirror together with one NMOS current mirror can be used to conduct offset current based on charging voltage, as shown above.

206. The amplitude of the offset current delivered by the current mirror will be based on the charging voltage generated by Provost.

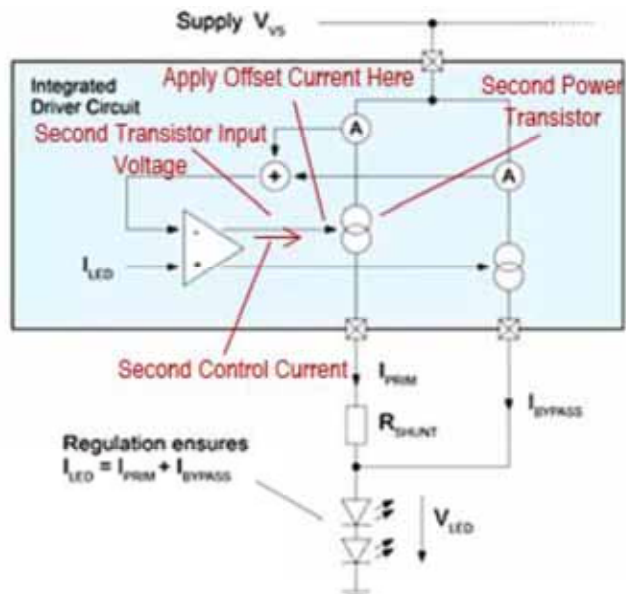
[8.3]	wherein the offset current is configured to control the transistor input voltage.
-------	---

c) **Ground 5:** Claim [8.3]

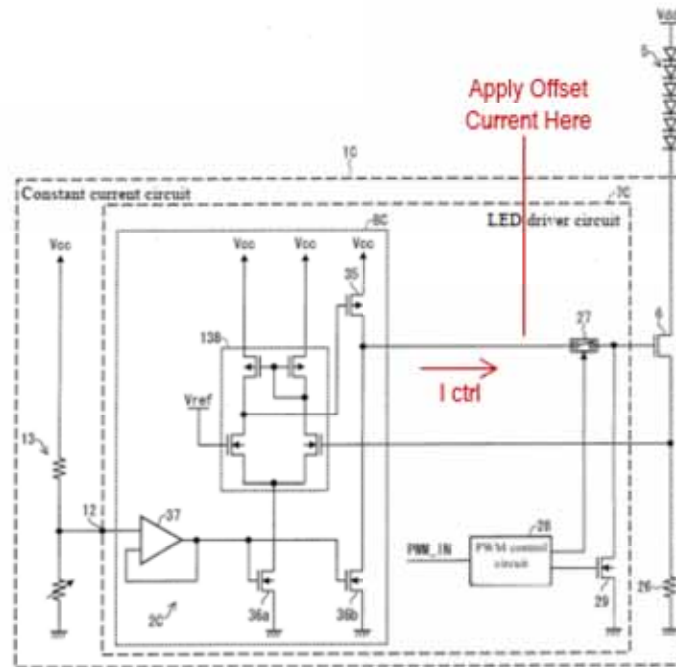
207. Output current (I_{offset}) can be applied, e.g., to input of second transistor of Sudhaus, as shown below. Ex1005, Fig. 1.



208. Alternatively, offset current I_{offset} can be applied to input of second power transistor of Praxis, as shown below.



209. Alternatively, offset current (I_{offset}) can be applied to input of power transistor 6 of Ryoichi to control transistor input voltage.



RYOICHI FIG. 5

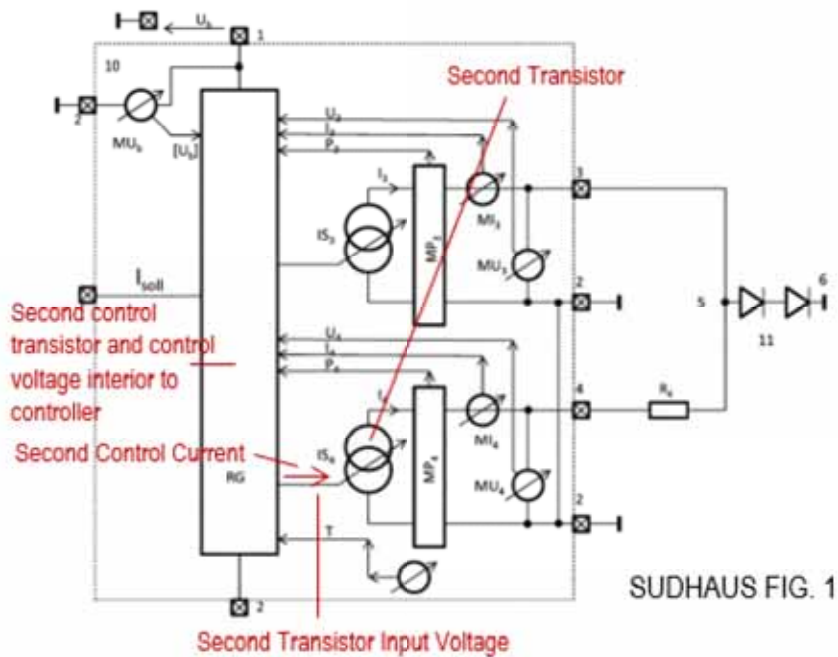
I. Claim 9 is unpatentable under Ground 5

[9.1]	The system of claim 8, wherein the amplifier output stage comprises a control transistor that is controlled by the control voltage,
-------	---

a) Ground 5: Claim [9.1]

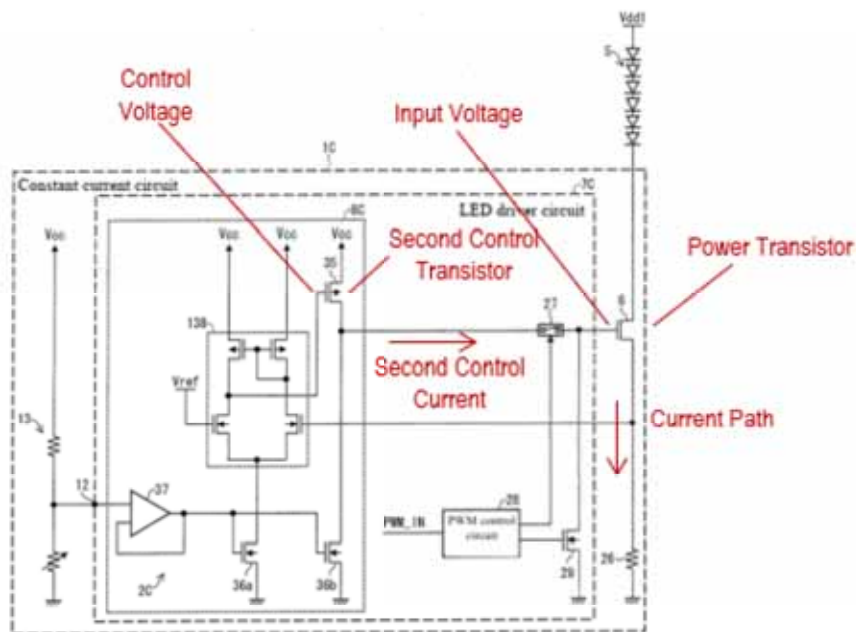
210. Claim 9, in dependence from claims 7 and 8, refers to control of the second current path.

211. Sudhaus Fig. 1 discloses, controller RG controlling second current path IS₄ and R4. Ex1005, 4:46-47. Sudhaus teaches: controller RG is operative to control two current sources. Ex1005, 4:46-47. Control current



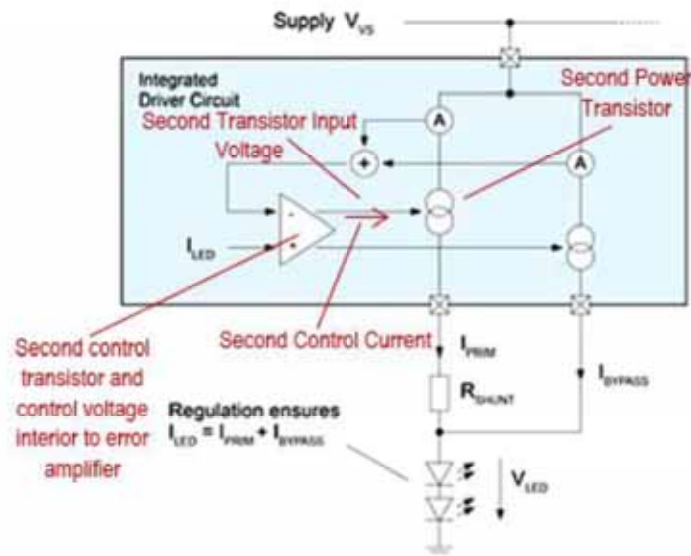
212. Sudhaus discloses that current sources (such as IS_3 and IS_4) include a power transistor referred to as a controlling transistor. Ex1005, 1:65-2:14.

213. In addition to Sudhaus, Ryoichi Fig. 5 shows: operational amplifier 8C includes amplifier output stage including transistors 35/36b. Ex1006, Fig. 5. Transistor 35 (control transistor) is controlled by output of differential part 138 (control voltage). Ex1006, Fig. 5. First control transistor 35 conducts current (control current) to drive control input of driving transistor 6 (generate first transistor input voltage).



RYOICHI FIG. 5

214. In addition to Sudhaus, and Ryoichi, Praxis discloses error amplifier having two outputs to control two current sources providing current to LED load. Ex1008, page 3, Section titled “Modern linear regulators with a power distribution,” lines 7-14; and Fig. 1. Error amplifier includes second output to control second current source.

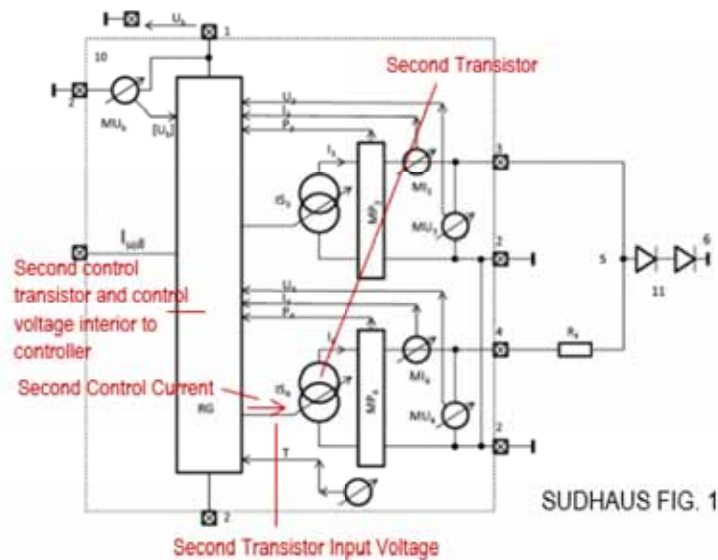


PRAXIS FIG. 1

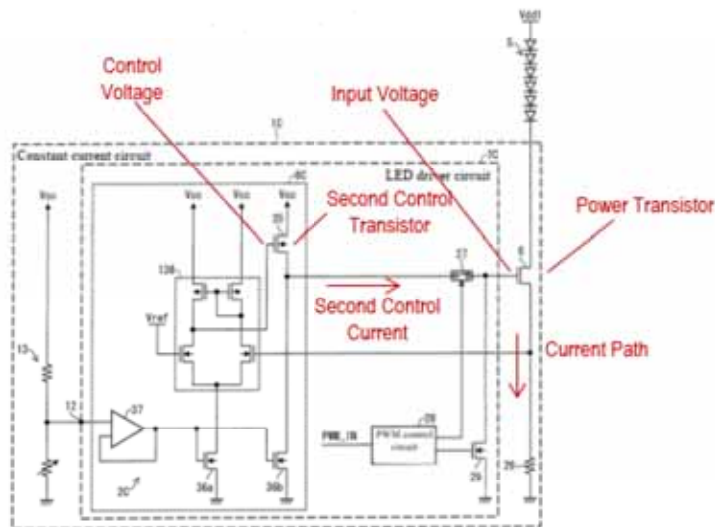
[9.2]	wherein the control transistor is coupled to an input of the power transistor to set an initial amplitude of the transistor input voltage,
-------	--

b) Ground 5: Claim [9.2]

215. Sudhaus shows the control transistor (internal to controller RG) connected to an input of the power transistor. Ex1005, 4:46-47.

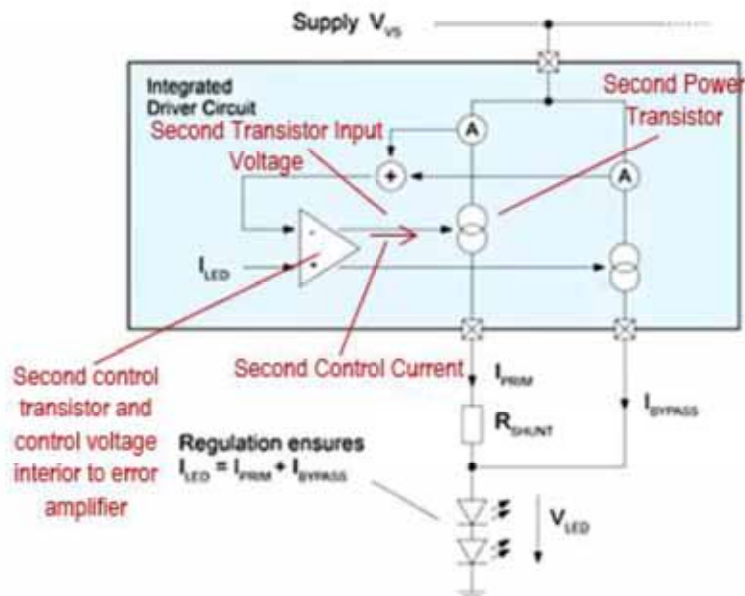


216. Absent an offset current, the power transistor input voltage will be determined by the control transistor.
217. Alternatively, Ryoichi Fig. 5 shows amplifier output stage coupled to input of power transistor 6. Ex1006, Fig. 5. Amplifier output stage sets initial amplitude of transistor input voltage.



RYOICHI FIG. 5

218. Alternatively, Praxis discloses an error amplifier having two outputs to control two current sources providing current to LED load. Ex1008, page 3, Section titled “Modern linear regulators with a power distribution,” lines 7-14; and Fig. 1. As shown in Fig. 1 of Praxis, each of the outputs of the error amplifier is connected to a respective input of a current source (power transistor) and will set an initial amplitude of the input voltage before an offset current is applied.

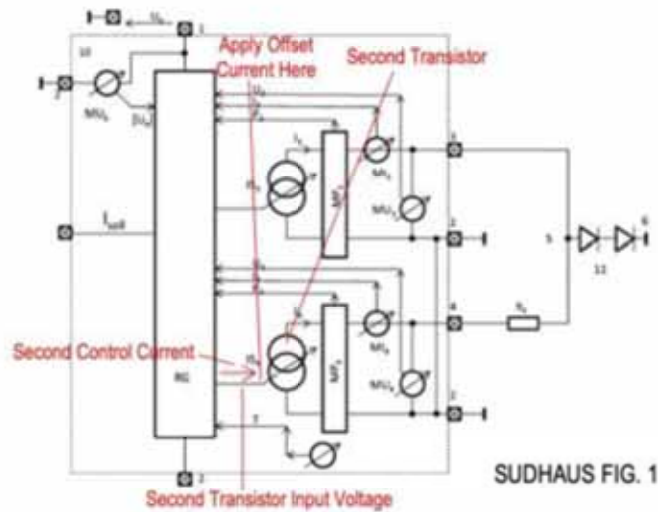


PRAXIS FIG. 1

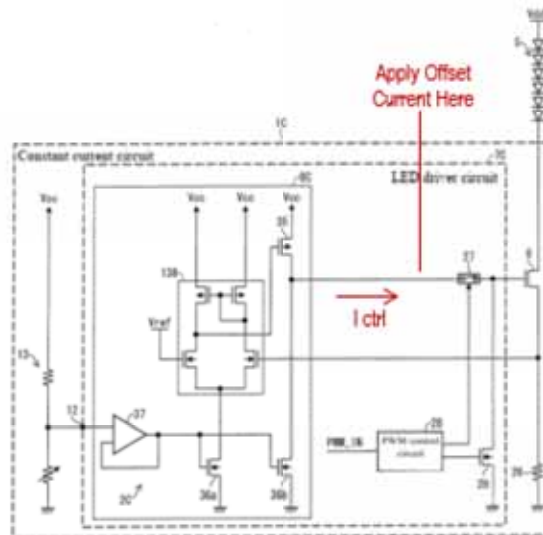
[9.3]	wherein the offset current is subtracted from the initial amplitude to control the power transistor based on the slew-rate.
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c) **Ground 5:** Claim [9.3]

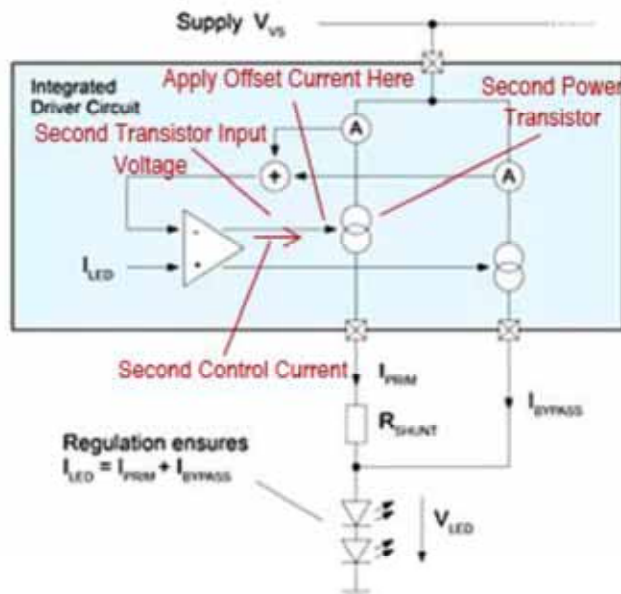
219. As described in reference to claim 7, the combination of Provost, TI Paper and UK Paper generate an offset current that varies with the slew rate. The offset current I_{offset} can be applied, for example, to the input of the second transistor of Sudhaus, Ex1005, Fig. 1.



220. Alternatively, the offset current can be applied for example to power transistor 6 of Ryoichi to control the power transistor based on the slew rate.



221. Alternatively, the offset current can be applied to the input of the second power transistor shown in Praxis, Fig. 1.



PRAXIS FIG. 1

J. Claim 10 is unpatentable under Grounds 1-5

10	An integrated circuit (IC) chip comprising the LED driver system of claim 1.
----	--

a) Grounds 1–5: Claim 10

222. Sudhaus discloses that control circuit is designed as integrated circuit (IC), e.g., Sudhaus states: [t]hus, according to the disclosure, the apparatus for supplying at least one consumer with electrical energy ... is provided with a control circuit designed as an integrated circuit (IC) and having a control circuit ... having at least a first output and a second output, wherein the consumer can be powered with electrical energy ... wherein the desired value for the electrical power of the consumer , which electrical power can

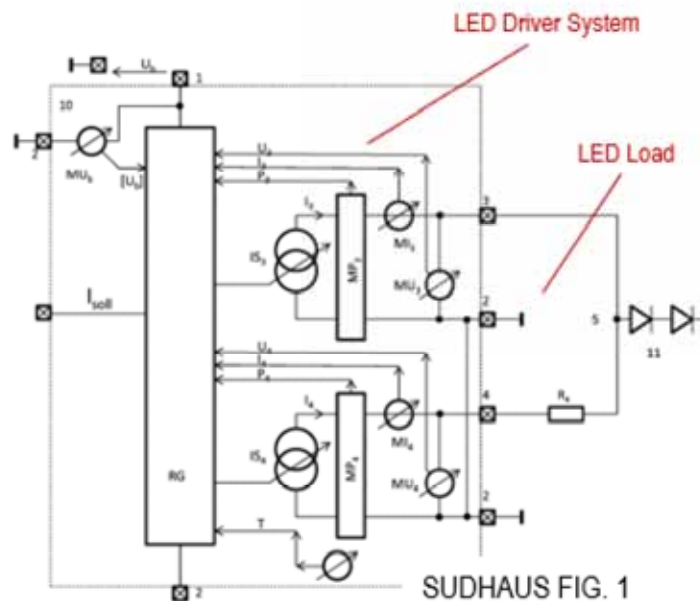
be controlled by the control circuit, can be specified, and ... wherein the distribution of the electrical current for the consumer ... between the at least two outputs ... can be controlled by said control circuit ...” Ex1005, 2: 25-50.

K. Claim 11 (broken into elements [11.pre – 11.5] presented below) is unpatentable under Grounds 1-5

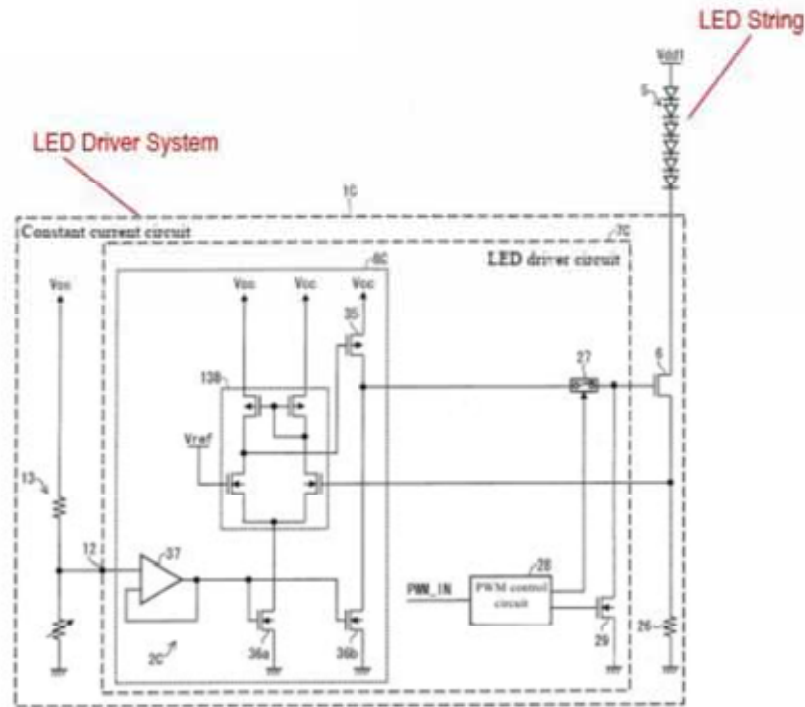
[11.pre]	A light-emitting diode (LED) system comprising:
----------	---

a) Grounds 1–5: Claim [11.pre]

223. Claim 11, [11.pre] is the same as claim 1, except that the light-emitting diode system of claim 11 includes the LED string. Please reference claim 1 [1.pre] above.



224. [Ground 2–5] Please reference claim 1, [1.pre] above.



RYOICHI FIG. 5

[11.1]	an error amplifier configured to compare an input voltage with a reference voltage to generate a control voltage; and an amplifier output stage configured to control an output current through a first current path
--------	--

b) Grounds 1–5: Claim [11.1]

225. This recitation is equivalent to, and invalid for the reasons cited in reference to claim 1, recitation [1.1] above.

[11.2]	and a shunt current through a second current path based on the control voltage,
--------	---

c) Grounds 1–5: Claim [11.2]

226. This recitation is equivalent to, and invalid for the reasons cited in reference to claim 1, recitation [1.2] above.

[11.3]	the amplifier output stage comprising a slew-rate controller configured to control slew-rate of the shunt current;
--------	--

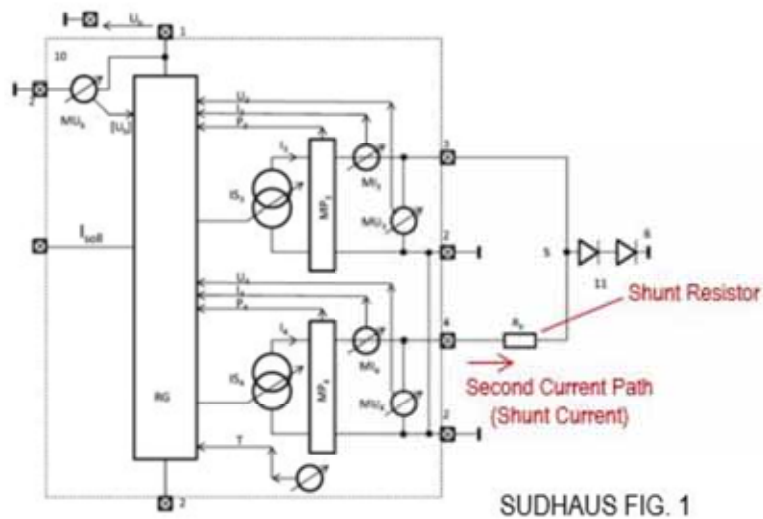
d) Grounds 1–5: Claim [11.3]

227. This recitation is equivalent to, and invalid for the reasons cited in reference to claim 1, recitation [1.3] above.

[11.4]	a shunt resistor in the second current path to conduct the shunt current; and
--------	---

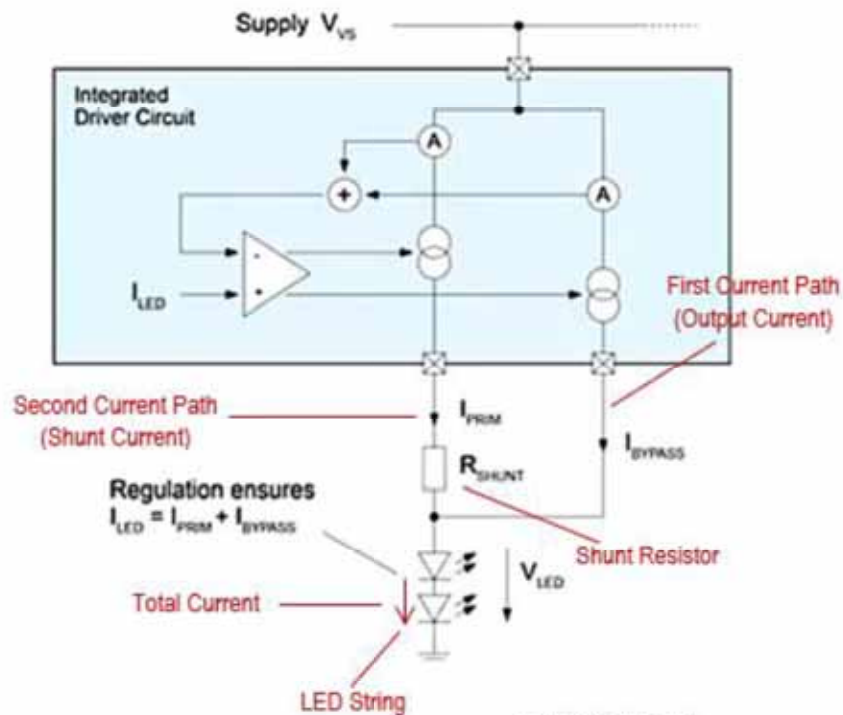
e) Grounds 1 – 5: Claim [11.4]

228. Sudhaus further discloses that one of current paths includes external resistor, e.g., Sudhaus states: “[t]he current of the second current source IS_4 is conducted via the resistor R_4 ...” Ex1005, 4:30-33. This is shown in Sudhaus, Fig. 1.



f) **Grounds 3 – 5:** Claim [11.4]

229. In addition to Sudhaus, and alternatively, Praxis discloses error amplifier having two outputs to control two current sources providing current to LED load. Ex1008, page 3, Section titled “Modern linear regulators with a power distribution,” lines 7-14; and Fig. 1. The second output current path includes a shunt resistor.

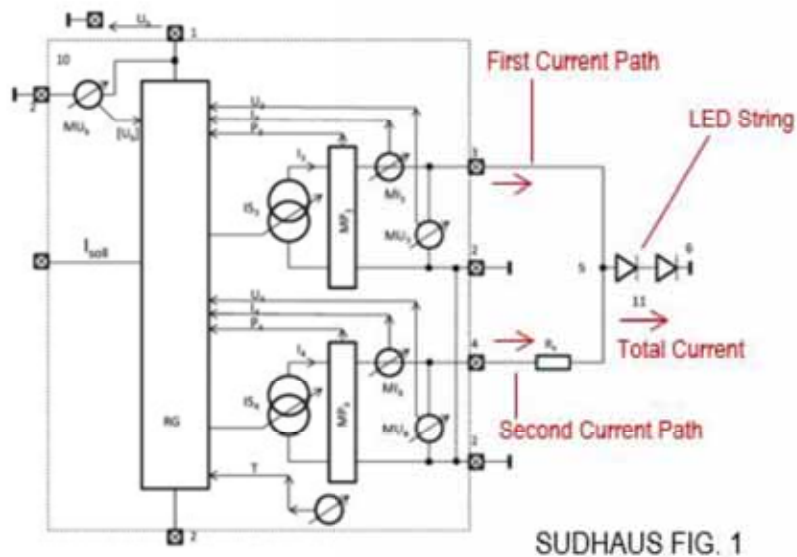


PRAXIS FIG. 1

[11.5]	an LED string arranged at an output of the first current path and the second current path to illuminate in response to a total current comprising a sum of the output current and the shunt current.
--------	--

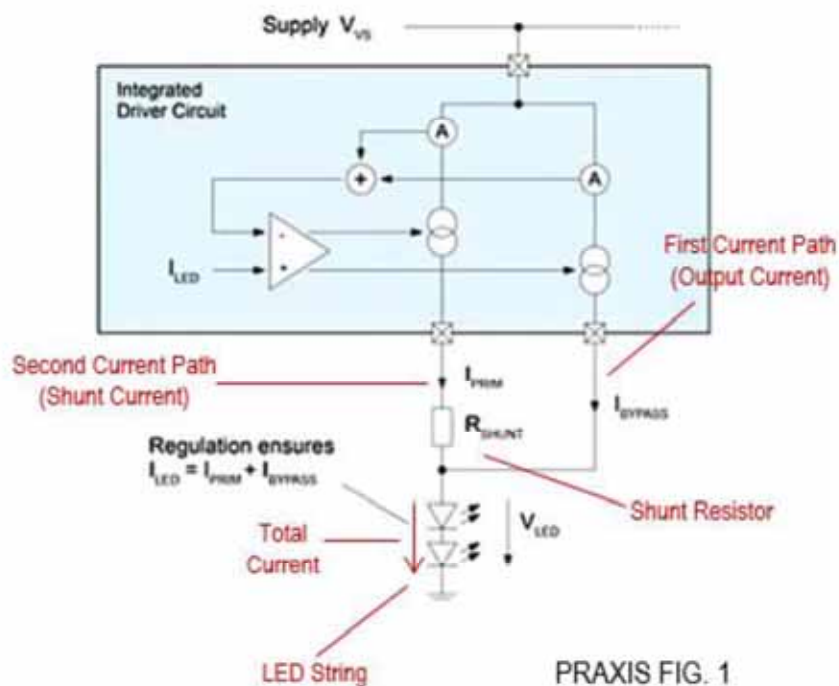
g) Grounds 1–5: Claim [11.5]

230. Sudhaus further discloses that the controller is operative to control the total of the two output currents based on a desired value I_{soll} . Ex1005, 4:46-50, Fig. 1. The total current is delivered to an LED string.



h) Grounds 3–5: Claim [11.5]

231. In addition to Sudhaus, and alternatively, Praxis discloses error amplifier having two outputs to control two current sources providing current to LED load. Ex1008, page 3, Section titled “Modern linear regulators with a power distribution,” lines 7-14; and Fig. 1.



L. Claim 12 is unpatentable under Grounds 2-5

12	The system of claim 11, wherein the slew-rate controller comprises a charging capacitor having a capacitance that defines the slew-rate of the shunt current.
----	---

a) Grounds 2-5: Claim 12

232. Claim 12 is equivalent to claim 7, addressed above.

M. Claim 13 (broken into elements [13.1-13.3] presented below) is unpatentable under Ground 5

[13.1]	The system of claim 12, further comprising a power transistor configured to conduct the shunt current in the second current path based on a transistor input voltage,
--------	---

a) **Ground 5:** Claim [13.1]

233. This recitation is equivalent to, and invalid for the reasons cited in reference to claim 8, recitation [8.1] above.

[13.2]	wherein the charging capacitor is configured to generate a charging voltage to control an amplitude of an offset current via a current mirror,
--------	--

b) **Ground 5:** Claim [13.2]

234. This recitation is equivalent to, and invalid for the reasons cited in reference to claim 8, recitation [8.2] above.

[13.3]	wherein the offset current is configured to control the transistor input voltage.
--------	---

c) **Ground 5:** Claim [13.3]

235. This recitation is equivalent to, and invalid for the reasons cited in reference to claim 8, recitation [8.3] above.

N. Claim 14 (broken into elements [14.1 – 14.3] presented below) is unpatentable under Ground 5

[14.1]	The system of claim 13, wherein the amplifier output stage comprises a control transistor that is controlled by the control voltage,
--------	--

a) **Ground 5:** Claim [14.1]

236. This recitation is equivalent to, and invalid for the reasons cited in reference to claim 9, recitation [9.1] above.

[14.2]	wherein the control transistor is coupled to an input of the power transistor to set an initial amplitude of the transistor input voltage,
--------	--

b) Ground 5: Claim [14.2]

237. This recitation is equivalent to, and invalid for the reasons cited in reference to claim 9, recitation [9.2] above.

[14.3]	wherein the offset current is subtracted from the initial amplitude to control the power transistor based on the slew-rate.
--------	---

c) Ground 5: Claim [14.3]

238. This recitation is equivalent to, and invalid for the reasons cited in reference to claim 9, recitation [9.3] above.

O. Claim 15 (broken into elements [15.1 – 15.6] presented below) is unpatentable under Grounds 2-5

[15.1]	The system of claim 11, further comprising: a first power transistor configured to conduct the output current in the first current path based on a first transistor
--------	---

a) Grounds 2–5: Claim [15.1]

239. This recitation is equivalent to, and invalid for the reasons cited in reference to claim 2, recitation [2.1] above.

[15.2]	a second power transistor configured to conduct the shunt current in the second current path based on a second transistor input voltage;
--------	--

b) Grounds 2–5: Claim [15.2]

240. This recitation is equivalent to, and invalid for the reasons cited in reference to claim 2, recitation [2.2] above.

[15.3]	wherein the amplifier output stage comprises: a first control transistor configured to conduct a first control current based on the control voltage to generate the first transistor input voltage; and
--------	---

c) Grounds 2–5: Claim [15.3]

241. This recitation is equivalent to, and invalid for the reasons cited in reference to claim 3, recitation [3.1] above.

[15.4]	a second control transistor configured to conduct a second control current based on the control voltage to generate the second transistor input voltage,
--------	--

d) Grounds 2–5: Claim [15.4]

242. This recitation is equivalent to, and invalid for the reasons cited in reference to claim 3, recitation [3.2] above.

[15.5]	wherein the slew-rate controller is configured to conduct an offset current in parallel with the second control current to generate the second
--------	--

e) Grounds 2–5: Claim [15.5]

243. This recitation is equivalent to, and invalid for the reasons cited in reference to claim 4, recitation [4.1] above.

[15.6]	the offset current increasing at the slew-rate.
--------	---

f) Grounds 2–5: Claim [15.6]

244. This recitation is equivalent to, and invalid for the reasons cited in reference to claim 4, recitation [4.2] above.

P. Claim 16 (broken into elements [16.pre – 16.6] presented below) is unpatentable under Grounds 1-5

[16.pre]	A light-emitting diode (LED) driver system comprising:
----------	--

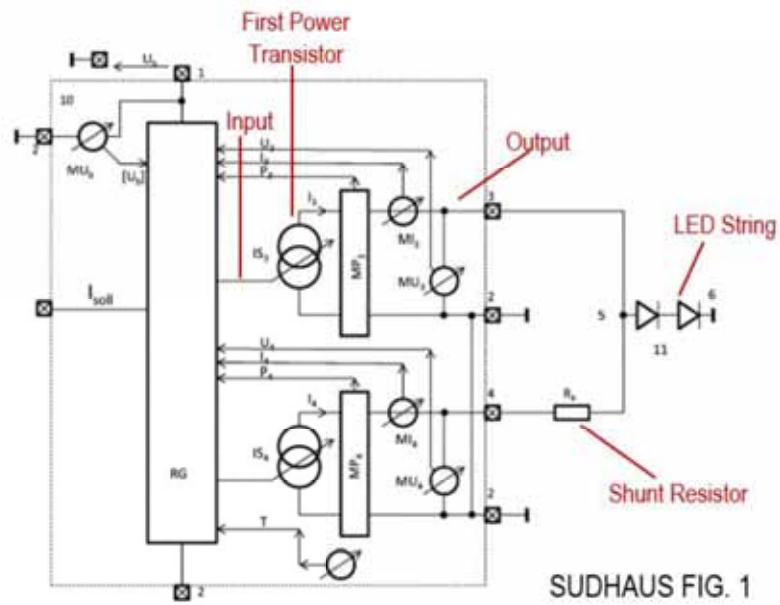
a) Grounds 1–5: Claim [16.pre]

245. The preamble to claim 16 is equivalent to, and invalid, for the same reasons as the preamble to claim 1.

[16.1]	a first power transistor comprising an input and an output coupled to an LED string and a shunt resistor;
--------	---

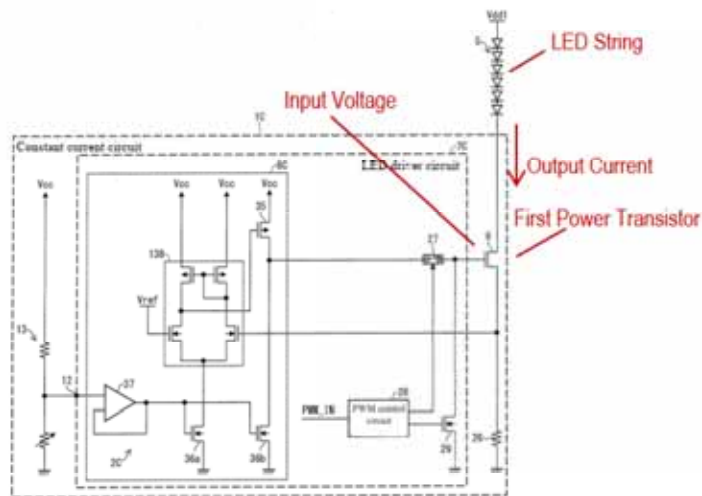
b) Grounds 1–5: Claim [16.1]

246. Sudhaus FIG 1 discloses output 3 coupled to LED load 11 and shunt resistor R_4 and driven by current source IS_3. Ex1005, 4:46-50, Fig. 1.



c) **Grounds 2–5:** Claim [16.1]

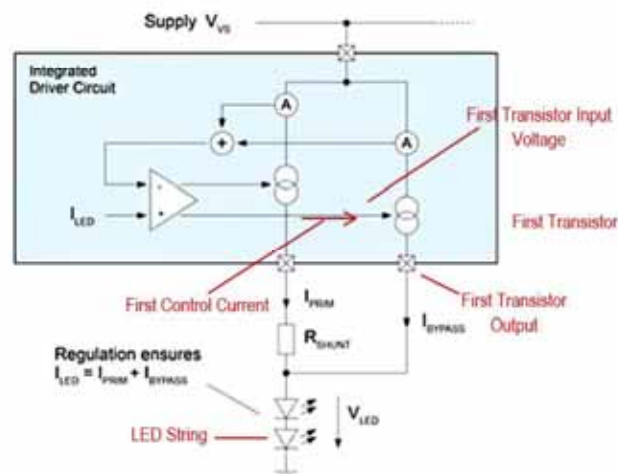
247. In addition to Sudhaus, and alternatively, Ryoichi discloses, in Fig. 5, driving transistor 6. Ex1006, Fig. 5.



248. Ryoichi Fig. 5 shows: first transistor 6 receives input voltage on gate input of transistor 6, input voltage being provided by amplifier output stage (transistors 35/36b). Current through transistor 6 (current in first path) is based on input voltage. Ex1006, Fig. 5. Output is coupled to LED string 5.

d) **Grounds 3–5:** Claim [16.1]

249. In addition to Sudhaus and Ryoichi, and alternatively, Praxis discloses error amplifier having two outputs, one output driving an input to a first current source, the current source having a first input and a output coupled to the LED load and to resistor R_SHUNT Ex1008, page 3, Section entitled “Modern linear regulators with a power distribution,” lines 5-14; and Fig. 1. Praxis discloses first current source having first input and being coupled to LED load and to resistor R_SHUNT.

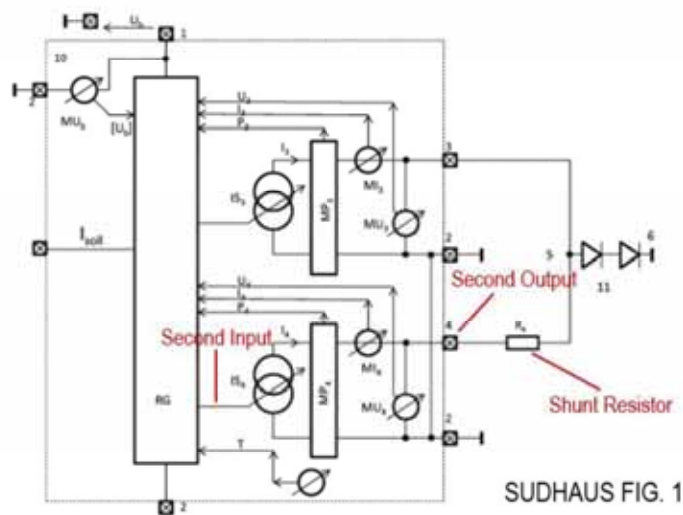


PRAXIS FIG. 1

[16.2]	a second power transistor comprising an input and an output coupled to the shunt resistor;
--------	--

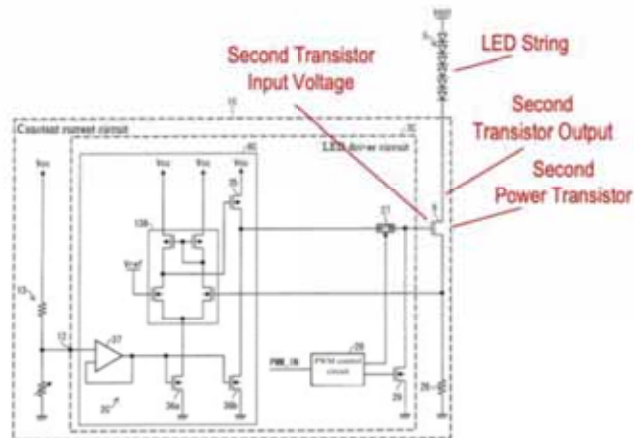
e) **Grounds 1–5:** Claim [16.2]

250. Sudhaus FIG 1 discloses output 4 driven by IS_4. IS_4 includes a power transistor driven by the controller RG and an output coupled to the shunt resistor R_4. Ex. 1005, 4:46-50, Fig. 1.



f) **Grounds 2–5:** Claim [16.2]

251. In addition to Sudhaus, and alternatively, Ryoichi discloses, in Fig. 5, driving transistor 6. Ex1006, Fig. 5.

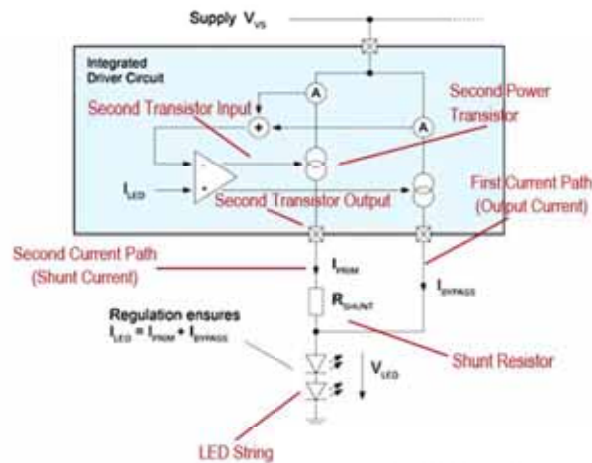


RYOICHI FIG. 5

252. Ryoichi Fig. 5 shows that a current source includes a first transistor 6 having an input and an output and being driven by amplifier output stage (transistors 35 and 36b). Ex1006, Fig. 5. It would have been obvious to POSITA to include the transistor 6 in the current source IS_4 of Sudhaus.

g) Grounds 3–5: Claim [16.2]

253. In addition to Sudhaus and Ryoichi, Praxis discloses error amplifier having a second output to control a current source coupled with a shunt resistor R_{shunt}. Ex1008, page 3, Section titled “Modern linear regulators with a power distribution,” lines 5-14; and Fig. 1.

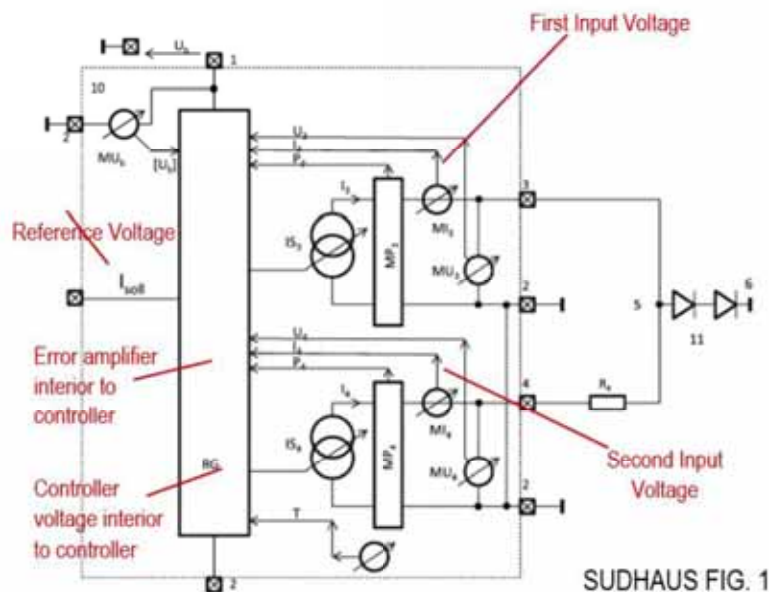


PRAXIS FIG. 1

[16.3]	an error amplifier, comprising a first input to receive an input voltage, a second input to receive a reference voltage, and an output to provide a control voltage; and
--------	--

h) Grounds 1–5: Claim [16.3]

254. Sudhaus discloses control circuit to control two outputs supplying current to consumer. Ex1005, 2:32-33. The controller is operative to control the total of two currents based on desired value I_{soll} . Ex1005, 4:46-50.

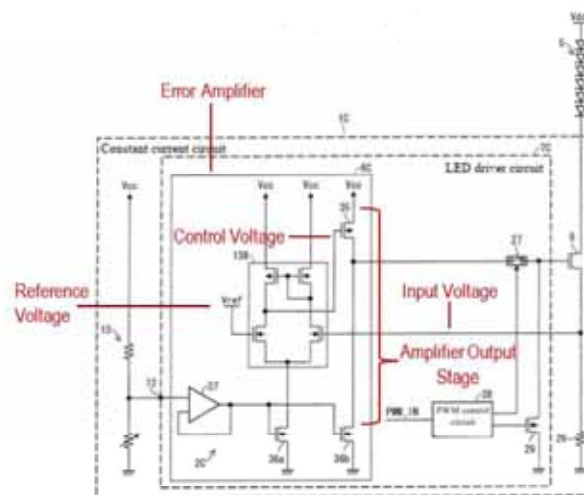


255. The controller may be implemented by either analog or digital circuits. Ex1005, 8:47-55.

256. Sudhaus FIG 1, the controller RG receives first and second input voltages (combined to form input voltage), and further receives a reference voltage I_{soll} . Based on these signals, the controller RG generates a necessary correction (control voltage) used to generate signals to control currents IS_3 and IS_4 . Ex1005, 4:25-28, Fig. 1.

i) **Grounds 2–5:** Claim [16.3]

257. In addition to Sudhaus, and alternatively, Ryoichi discloses operational amplifier 8C in Fig 5. Ex1006 ¶ [0019].



RYOICHI FIG. 5

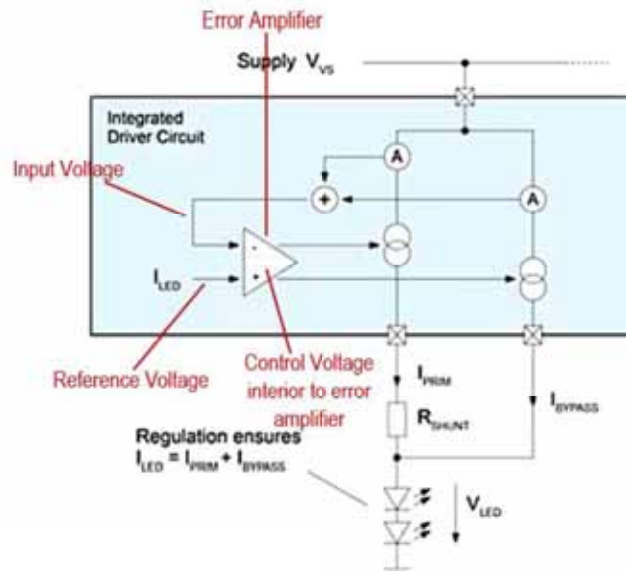
258. Ryoichi Fig. 5 shows: operational amplifier 8C includes a differential part 138 and amplifier output stage consisting of transistors 35/36b.

Ex1006, Fig. 5. The differential part receives an input voltage and a reference voltage and generates an output (control voltage). Ex1006, ¶ [0083].

j) **Grounds 3–5:** Claim [16.3]

259. In addition to Sudhaus and Ryoichi, and alternatively, Praxis discloses error amplifier having two outputs to control two current sources providing current to LED load. Ex1008, page 3, Section titled “Modern linear regulators with a power distribution,” lines 7-14; and Fig. 1. Error amplifier has first input to receive input voltage and second input to receive reference voltage. The error amplifier generates an internal signal

(control voltage) based on the inputs provides first and second outputs to control first and second current sources based on the internal signal.

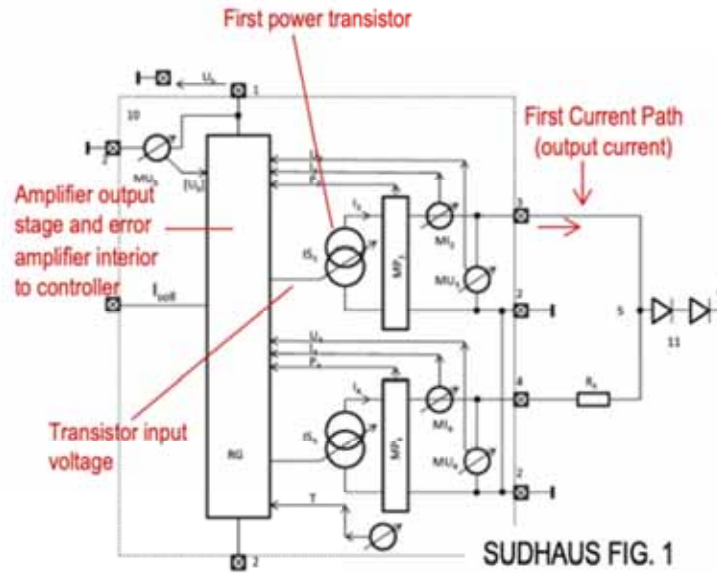


PRAXIS FIG. 1

[16.4]	an amplifier output stage comprising an input coupled to the output of the error amplifier, a first output coupled to the input of the first power transistor,
--------	--

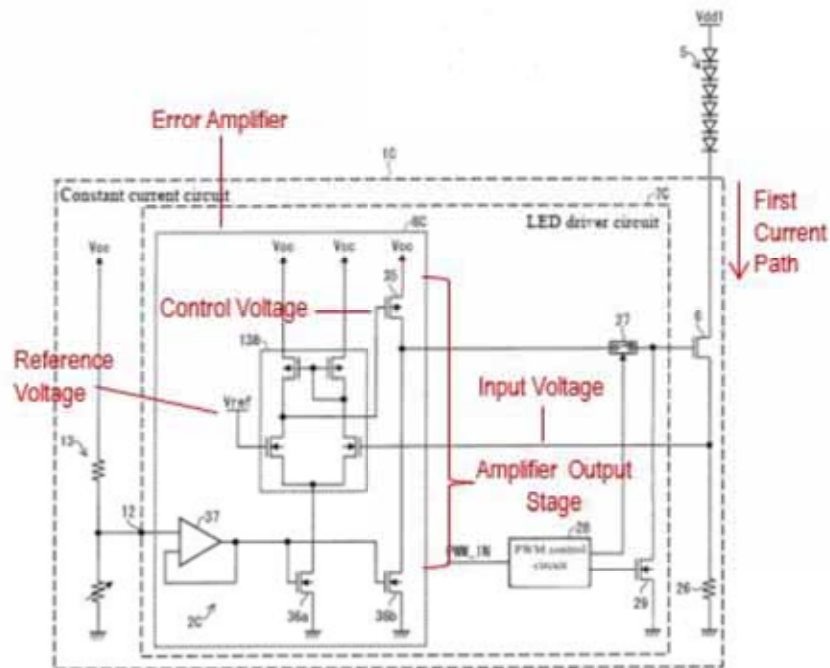
k) Grounds 1–5: Claim [16.4]

260. Sudhaus discloses a controller RG operative to control total of two currents based on desired value I_{soll} . Ex. 1005, 4:46-50, Fig. 1. The controller RG includes a first output coupled to the input of IS_3 (the first power transistor). The first output of the controller RG is controlled internally to the controller RG at its input. Ex. 1005, 4:25-28, Fig. 1.



I) **Grounds 2–5:** Claim [16.4]

261. In addition to Sudhaus, and alternatively, Ryoichi FIG 5 discloses operational amplifier 8C. Ex1006 ¶ [0019].

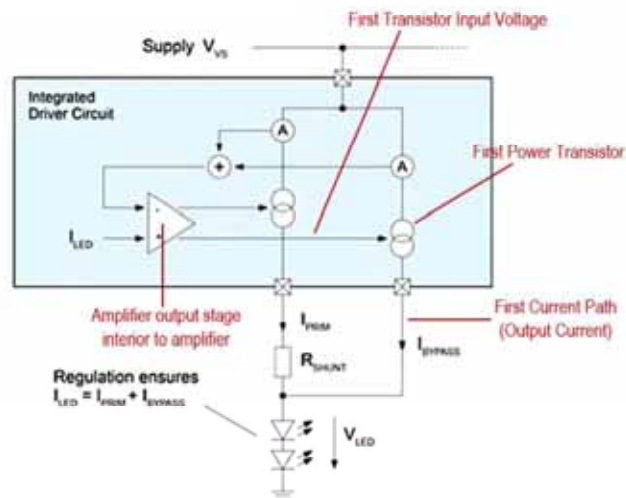


RYOICHI FIG. 5

262. Ryoichi Fig. 5 shows: operational amplifier 8C includes amplifier output stage consisting of transistors 35 and 36b. Ex1006, Fig. 5. The input of transistor 35 is coupled to the output of differential part 138 (control voltage). The output of transistor 35 is coupled to the input of power transistor 6. Ryoichi Fig. 5, ¶ [0083].

m) Grounds 3–5: Claim [16.4]

263. In addition to Sudhaus and Ryoichi, and alternatively, Praxis discloses an error amplifier having two outputs to control two current sources providing current to an LED load. Ex1008, page 3, Section titled “Modern linear regulators with a power distribution,” lines 7-14; and Fig. 1. The error amplifier includes a first output (amplifier output stage) coupled to an input of the first current source. It would have been obvious to POSITA to include the amplifier structure of Ryoichi in the error amplifier of Praxis, such that an input of the output stage is driven by the differential stage.

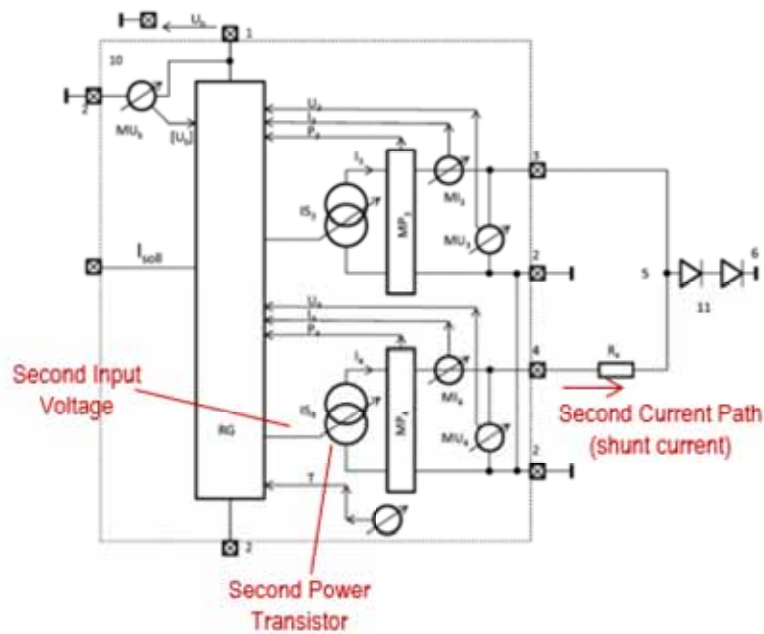


PRAXIS FIG. 1

[16.5]	and a second output coupled to the input of the second power transistor,
--------	--

n) Grounds 1–5: Claim [16.5]

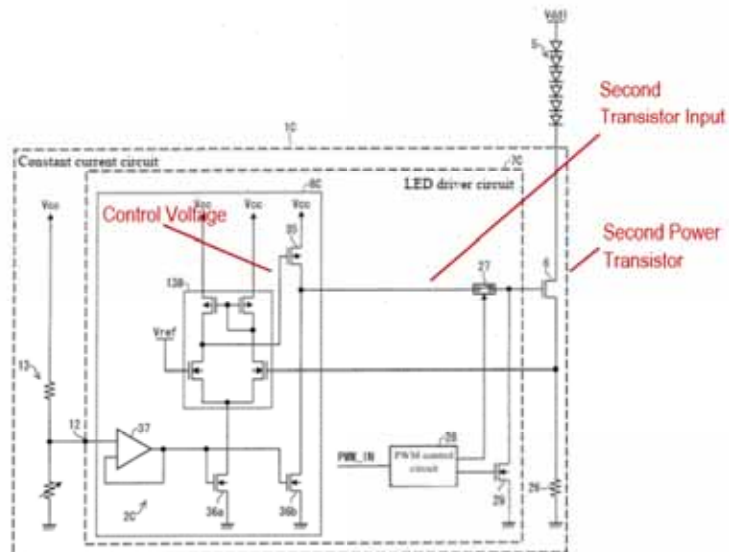
264. Sudhaus discloses a controller RG operative to control total of two currents based on desired value I_{soll} . Ex. 1005, 4:46-50, Fig. 1. The controller RG includes a second output 4 coupled to the input of IS_4 (the second power transistor). The second output of the controller RG is controlled internally to the controller RG. Ex. 1005, 4:25-28, Fig. 1.



SUDHAUS FIG. 1

o) **Grounds 2–5:** Claim [16.5]

265. Ryoichi FIG 5 discloses operational amplifier 8C. Ex1006 ¶ [0019].

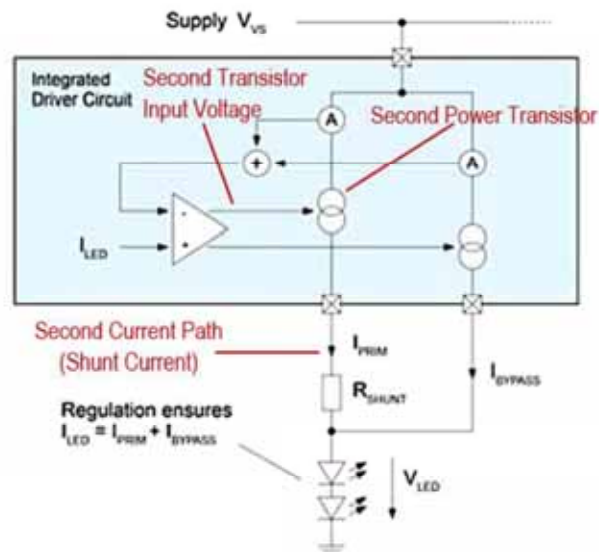


RYOICHI FIG. 5

266. Ryoichi Fig. 5 shows: operational amplifier 8C includes amplifier output stage consisting of transistors 35 and 36b. Ex1006, Fig. 5. The input of transistor 35 is coupled to the output of differential part 138 (control voltage). The output of transistor 35 is coupled to the input of power transistor 6. Ryoichi Fig. 5, ¶ [0083]. It would have been obvious to POSITA to include the differential amplifier and amplifier output structure of Ryoichi to control the second output (output 4) of Sudhaus to control IS_4.

p) Grounds 3–5: Claim [16.5]

267. In addition to Sudhaus and Ryoichi, and alternatively, Praxis discloses an error amplifier having two outputs to control two current sources providing current to an LED load. Ex1008, page 3, Section titled “Modern linear regulators with a power distribution,” lines 7-14; and Fig. 1. The error amplifier includes a second output (amplifier output stage) coupled to an input of the second current source. It would have been obvious to POSITA to include the amplifier structure of Ryoichi in the error amplifier of Praxis, such that an input of the output stage is driven by the differential stage.

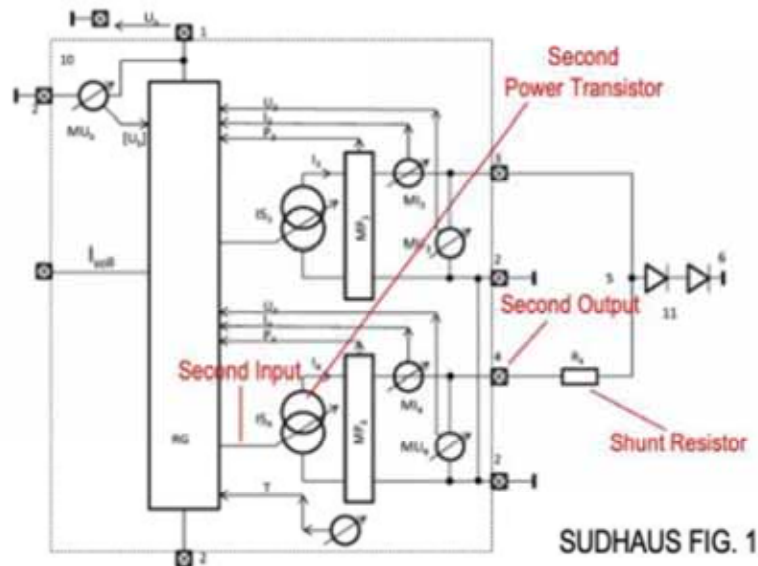


PRAXIS FIG. 1

[16.6]	the amplifier output stage comprising a slew-rate controller, the slew rate controller comprising an output coupled to the input of the second power transistor.
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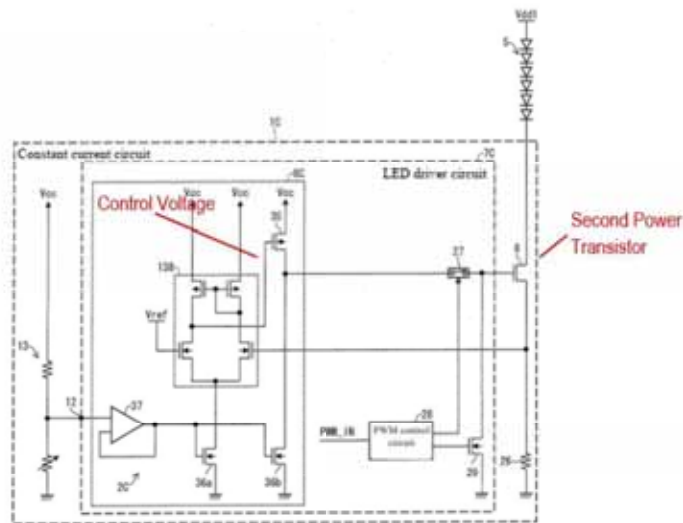
q) Grounds 1–5: Claim [16.6]

268. Sudhaus includes a slew rate controller for the second power transistor as described in reference to claim 1, recitation [1.3]. Sudhaus Fig. 1 shows output 4 of the controller RG connected to the input (power transistor IS_4). Ex. 1005, 4:25-28, Fig. 1.



r) Grounds 2–5: Claim [16.6]

269. In addition to Sudhaus, and alternatively, Ryoichi includes slew rate control as described in reference to claim 1, recitation [1.3]. The slew rate control is included in the operational amplifier 8C. Ex1006, ¶¶ [0083]-[0085]. As shown in Fig. 5, the output of the operational amplifier 8C is coupled to the input of power transistor 6.



RYOICHI FIG. 5

s) **Ground 4:** Claim [16.6]

270. Alternatively to the slew rate control of Sudhaus, and Ryoichi, Wu discloses a slew rate controller, as described in reference to claim 1, recitation [1.3].

t) **Ground 5:** Claim [16.6]

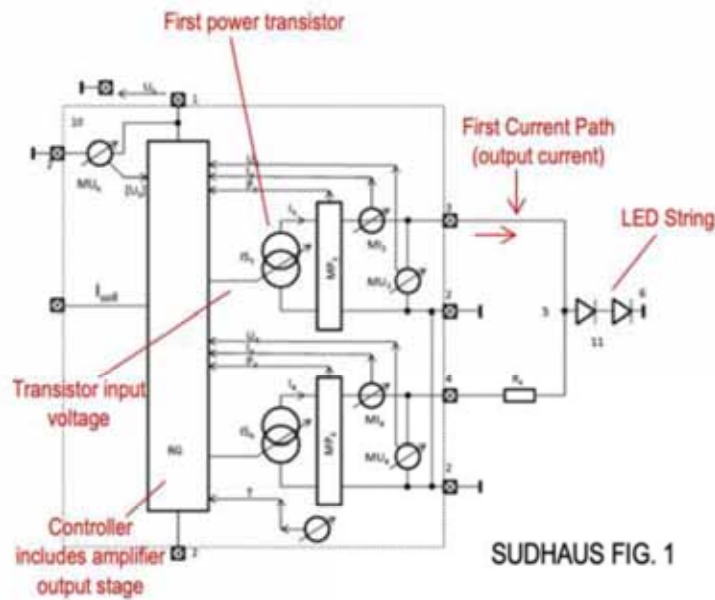
271. Alternatively to the slew rate control of Sudhaus, Ryoichi, and Wu, the combination of Provost, TI Paper and UK Paper discloses a slew rate controller, as described in reference to claim 5.

Q. Claim 17 (broken into elements [17.1 – 17.2] presented below) is unpatentable under Grounds 1-5

[17.1]	The system of claim 16, wherein the amplifier output stage is configured to control an amplitude of an output current through a first current path that includes the LED string and
--------	---

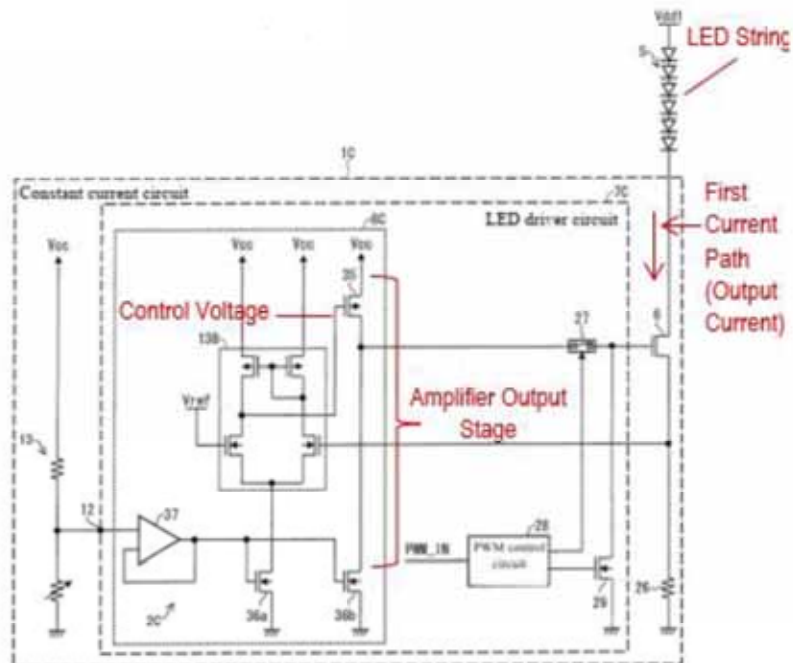
a) **Grounds 1–5:** Claim [17.1]

272. Sudhaus, FIG 1, shows the controller RG outputs a signal to control current from current source IS_3 (output current). Ex1005, 4:25-28, Fig. 1. The first output of controller RG is applied to first current source IS_3 and controls amplitude of current through first current path to the LED string 11.



b) **Grounds 2–5:** Claim 17.1

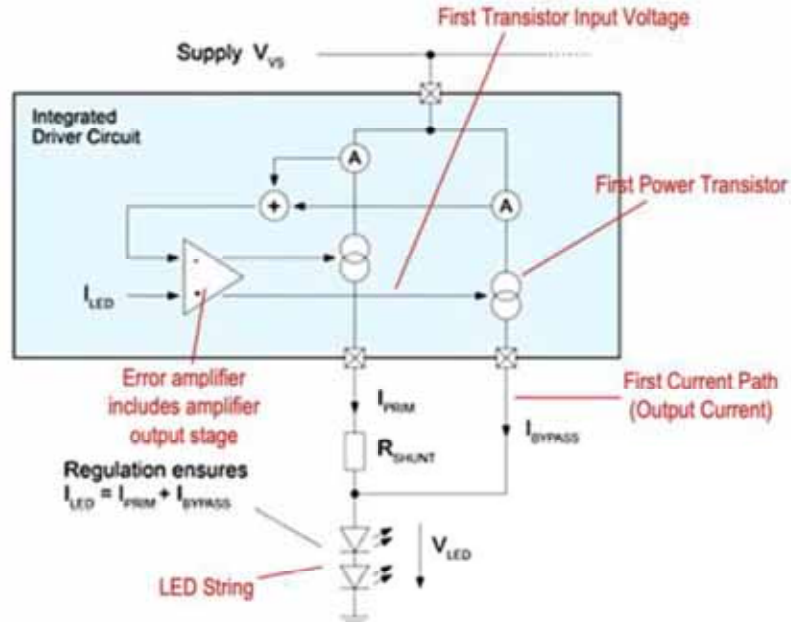
273. In addition to Sudhaus, and alternatively, Ryoichi Fig. 5 shows: amplifier output stage (transistors 35/36b) controls first current path (transistor 6/resistor 26), providing current to LED load 5. Ex1006, Fig. 5.



RYOICHI FIG. 5

c) **Grounds 3–5:** Claim 17.1

274. In addition to Sudhaus and Ryoichi, Praxis discloses error amplifier having two outputs to control two current sources providing current to LED load. Ex1008, page 3, Section titled “Modern linear regulators with a power distribution,” lines 7-14; and Fig. 1. Error amplifier is configured to control output current through first current path that includes LED string.

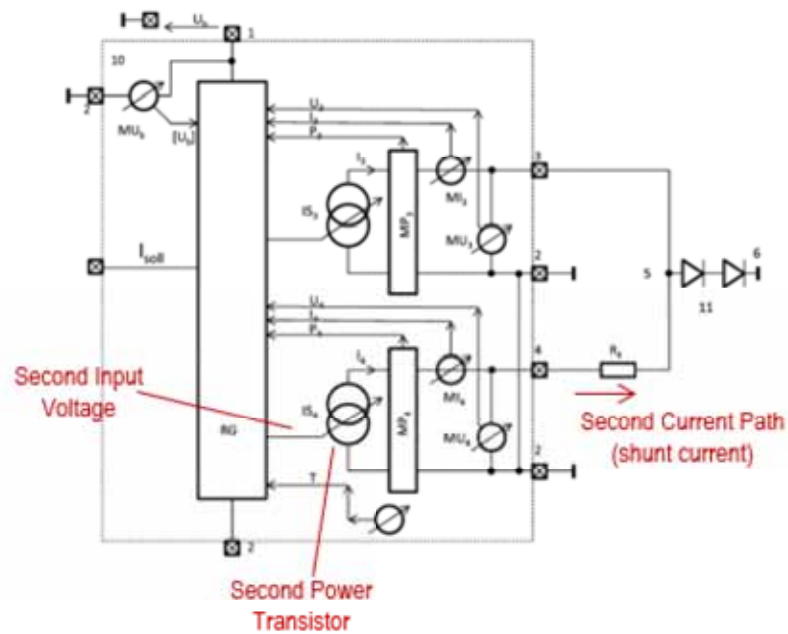


PRAXIS FIG. 1

[17.2]	a shunt current through a second current path that includes the shunt resistor based on the control voltage.
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d) Grounds 1–5: Claim [17.2]

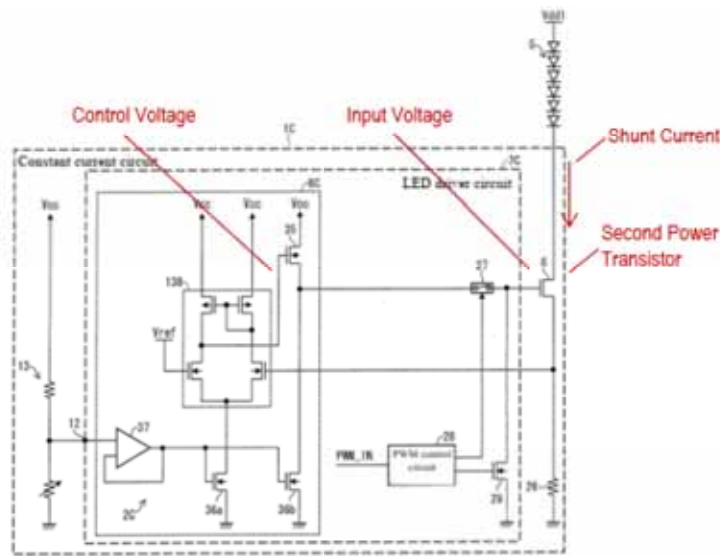
275. This recitation is the same as recitation [1.2] with the addition that the second current path includes the shunt resistor. Sudhaus Fig. 1 shows that the second current path includes the shunt resistor. Ex1005, 4:46-50, Fig. 1.



SUDHAUS FIG. 1

e) **Grounds 2–5:** Claim [17.2]

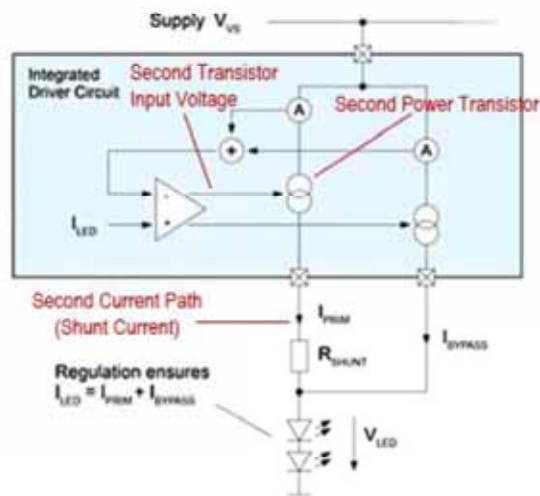
276. This recitation is the same as recitation [1.2] with the addition that this recitation includes that the second current path includes the shunt resistor. It would have been obvious to POSITA to include the amplifier 8C of Fig. 5 of Ryoichi in the controller of Sudhaus to control the current through the second current path as shown in Sudhaus above. Ex1006, ¶ [0083], Fig. 5.



RYOICHI FIG. 5

f) Grounds 3–5: Claim [17.2]

277. This recitation is the same as recitation [1.2] with the addition that the second current path includes the shunt resistor. Praxis Fig. 1 shows that the second current path includes the shunt resistor.



PRAXIS FIG. 1

R. Claim 18 is unpatentable under Grounds 2-5

18	The system of claim 17, wherein the slew-rate controller comprises a charging capacitor having a capacitance that defines the slew-rate of the shunt current.
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a) Grounds 2-5: Claim 18

278. Claim 18 is equivalent to, and invalid for the same reasons as claim 7, above.

S. Claim 19 (broken into elements [19.1 – 19.3] presented below) is unpatentable under Ground 5

[19.1]	The system of claim 18, further comprising a power transistor configured to conduct the shunt current in the second current path based on a transistor input voltage,
--------	---

a) Ground 5: Claim [19.1]

279. This recitation is equivalent to, and invalid for the same reasons as claim 8, recitation [8.1].

[19.2]	wherein the charging capacitor is configured to generate a charging voltage to control an amplitude of an offset current via a current mirror,
--------	--

b) Ground 5: Claim [19.2]

280. This recitation equivalent to, and invalid for, the same reasons as claim 8, recitation 8.2.

[19.3]	wherein the offset current is configured to control the transistor input
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	voltage.
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c) Ground 5: Claim [19.3]

281. This recitation is equivalent to, and invalid for the same reasons as claim 8, recitation 8.3.

T. Claim 20 (broken into elements [20.1 – 20.3] presented below) is unpatentable under Ground 5

[20.1]	The system of claim 19, wherein the amplifier output stage comprises a control transistor that is controlled by the control voltage,
--------	--

a) Ground 5: Claim [20.1]

282. This recitation is equivalent to, and invalid for the same reasons as claim 9, recitation [9.1], above.

[20.2]	wherein the control transistor is coupled to an input of the power transistor to set an initial amplitude of the transistor input voltage,
--------	--

b) Ground 5: Claim [20.2]

283. This recitation is equivalent to, and invalid for the same reasons as claim 9, recitation [9.2], above.

[20.3]	wherein the offset current is subtracted from the initial amplitude to control the power transistor based on the slew-rate.
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c) Ground 5: Claim [20.3]

284. This recitation is equivalent to, and invalid for the same reasons as claim 9, recitation [9.3], above.

IX. CONCLUSION

285. I reserve the right to offer opinions relevant to the invalidity of the '432 Patent claims at issue and/or offer testimony in support of this Declaration.

286. In signing this Declaration, I recognize that the Declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be subject to cross-examination in the case. If required, I will appear for cross-examination at the appropriate time.

287. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true and, further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001.

Dated: April 11, 2024

Respectfully submitted,

Peter Glösekötter
PETER GLÖSEKÖTTER