

On-Chip Ramp Generators for Mixed-Signal BIST and ADC Self-Test

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Abstract—A practical approach to generate on-chip precise and slow analog ramps, intended for time-domain analog testing, monotonicity and histogram-based tests of ADCs is proposed. The technique uses an analog discrete-time adaptive scheme to calibrate the ramp generator. The lowest slope is 0.4 V/ms. Three implementations are presented for different levels of accuracy and complexity. Measurement results show excellent accuracy and programmability, up to only 0.6% of slope error and maximum integral nonlinearity error of $\pm 175 \mu\text{V}$. Experimental and theoretical results are in good agreement.

Index Terms—ADC self-test, built-in self-test (BIST), linearity, ramp generation, time-domain test.

I. INTRODUCTION

BUILT-IN self-test (BIST) and design for testability (DFT) of analog circuits are important and necessary to produce highly reliable mixed-signal systems [1]. Due to the constant increase of analog circuit density, the nature of analog faults, and the embedding of analog functions within large digital systems, the detection and isolation of faults in these circuits is becoming more difficult.

Many research groups have suggested techniques to make on-chip frequency-domain testing of mixed-signal circuits and on-chip testing of analog–digital converters (ADCs). The goal of these techniques is to overcome the complexity of integrating a traditional ac characterization approach [2]. Well-defined techniques for reducing the size of the test set while maintaining high fault coverage have been reported [3], [4]. Some ac BIST techniques inject optimized digital inputs to a linear device under test (DUT) and extract a dc signature [5], [6]. These approaches are simple, but their precision is limited. On the other hand, Toner and Roberts [7] have proposed several methods to make frequency-domain tests on sigma–delta converters by generating precise on-chip sine waves and analyzing the results with an on-chip digital signal processor (DSP), but the area overhead is large. Several techniques have been published to generate on-chip linear ramps and perform ADC BIST [8]–[11], but the results either depend largely on the accuracy of the additional components in the test circuitry, or have not been proven experimentally. In [12], the

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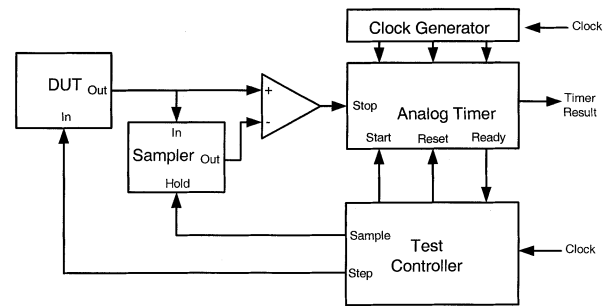


Fig. 1. Conceptual system for time-domain testing.

authors present a self-calibration scheme for linear ramps, but the linearity is not high enough for linearity test of ADCs. A technique very similar to ours is presented in [13], following a previous publication from our group [14]. However, the former does not provide measurement results.

An on-chip ramp generator (OCRG) is desirable to perform monotonicity and histogram tests of ADCs. A novel application of the OCRG is proposed in [15], which allows the ac test of a linear circuit in time-domain using the ramp generator.

In this paper, we propose a unified approach at designing OCRGs using a discrete-time (DT) adaptive approach. Section II describes the adaptive scheme used in all the implementations. Section III gives the details of two low-complexity implementations. Section IV describes the third OCRG version. Section V presents the measurement results and Section VI gives the conclusions.

II. ADAPTIVE SCHEME FOR ON-CHIP RAMP GENERATION

A. Application of the OCRG to Time-Domain and ADC BIST

Fig. 1 illustrates a conceptual system where an OCRG can be used to perform time-domain ac BIST [15]. The goal is to extract several rise or fall time delay values from the DUT. A first step signal is sent to the DUT and the sampler is used to generate the target thresholds (for example, 10% and 90%) from the steady-state value of the DUT. When a second step is sent to the DUT and the response crosses the threshold, the timer is started or stopped, depending on the test (rise or fall delays) being performed. An analog timer is used instead of a digital timer because the latter would require the clock frequency to be too high for the same order of accuracy. For example, if the DUT has a rise time of $10 \mu\text{s}$ (for a second-order low-pass filter with a cutoff frequency of approximately 52 kHz) and an accuracy of 1% is needed, the clock frequency would need to be 10 MHz. If the whole system operates in the range of 52 kHz, the need

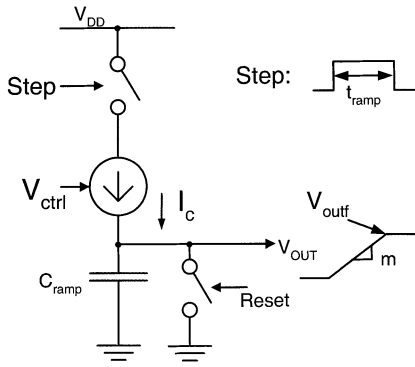


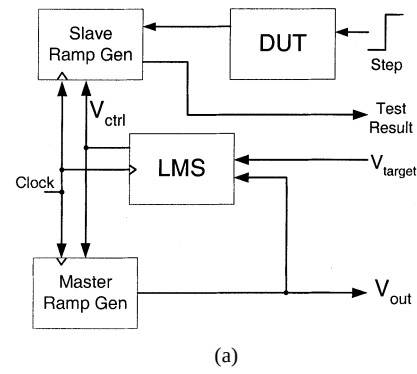
Fig. 2. Basic principle of the ramp generation used in the analog timer.

for a 10-MHz clock only to test the system would not be an acceptable solution. The analog timer is, in fact, a ramp generator for which the start and stop times are controlled by the delay to be measured. Once the ramp is stopped, the final analog value (V_{outf}) is directly proportional to the delay to be measured. Therefore, an accurate OCRG is desirable. In the case where the DUT can be approximated by a first- or second-order system, simple relations between time-domain and frequency-domain can be used by an external computer or tester to compute the frequency-domain characteristics (ω_0 , Q , ω_0/Q) [16] and/or diagnose a fault. Further arbitrary rise and fall delay tests can also be performed that do not necessarily have a frequency-domain relation. These test results can be used as signature of the DUT, be compared to a predefined signature of a fault-free circuit, and a go/no-go signal can be generated. The measurements can also be sent to an external diagnosis system.

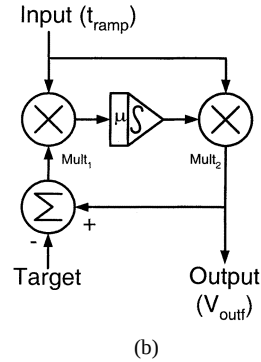
In the case of ADC testing, the practical implementation of the monotonicity test [17] is usually complicated by the presence of digital noise on the ADC output codes. However, simple digital signal processing can be used to reduce the effect of that noise and extract the monotonicity behavior of the ADC. If a very linear ramp is available on chip, linearity measurements based on histogram testing can be computed on chip with digital circuitry. Simple self-testing mechanisms to trace a calibration failure can be added to the technique to ensure that the OCRG is functioning properly before using it.

B. Inaccuracies in the Basic Ramp Generator

The principle of the basic ramp generator is to charge a capacitor with a constant current source. In the circuit of Fig. 2, $V_{outf} = t_{ramp}(I_c/C_{ramp}) = m_{ramp}t_{ramp}$ and is directly proportional to the pulsewidth of the step signal. In the case of time-domain testing as shown in Fig. 1, t_{ramp} would be the delay under test. To achieve the required performance (small slope and linear ramp in the case of ADC testing, and precisely known slope in the case of time-domain testing), we need a current source with a near-infinite output impedance that sources a very small current and a very large capacitor. Both have to be precise and constant. For most ADC tests, we have $t_{TEST} = 2^N T_S HPC$, where t_{TEST} is the ramping time and represents the longest portion of the ADC test. HPC is the number of hits per code used for the histogram, N is the number of bits of the ADC, and T_S is the ADC sampling period. If we want to use an on-chip ramping capacitor in the range of 10 pF, the design



(a)



(b)

Fig. 3. Block diagram of the adaptive approach. (a) Conceptual block diagram. (b) Details of a typical LMS block.

of the extremely small current source required to test a typical ADC becomes a challenge. Moreover, the process variation affecting the absolute value of the current source and on-chip capacitor ($\pm 20\%$) would result in significant slope errors.

C. Adaptive Scheme

The proposed solution is an adaptive scheme [14]. The advantage of this approach is that a precise and process-independent current reference is not needed since the adaptive scheme will generate the proper value automatically to satisfy the least square (LMS) condition [18]. Fig. 3(a) shows the general block diagram of the adaptive scheme.

The discrete adaptive calibration procedure is based on two reference values: the *clock* signal and a reference voltage used as a target. The calibration procedure consists of letting the output ramp during a constant delay t_{ramp} (which, in this case, is derived from the clock, and is not the delay under test) then comparing V_{outf} with the target dc level (V_{target}). The LMS block uses this information to vary the control voltage V_{ctrl} of the current source. This process of ramping and adjusting the control voltage is repeated until V_{outf} becomes exactly the same as V_{target} . Once the calibration is completed, we can use the slave ramp generator to measure delays in the DUT. In the case of ADC testing, we can discard the slave ramp generator and use V_{out} as the Ramp output. Referring to a typical LMS block [Fig. 3(b)], our input signal is t_{ramp} and the output is V_{outf} . Mult₂ is the ramp generator. As will be seen, Mult₁ is not necessary in our case.

Fig. 4 illustrates the basic current source used in the first implementation. Modifications will be made to this current source in the following implementations, but its characteristics, as far as the adaptive scheme is concerned, remain the same. M_5 is

TABLE I
IMPORTANCE OF PERFORMANCE CRITERIA FOR DIFFERENT APPLICATIONS

Application	Slope stability	Calibration time	Start/Stop offsets	Linearity	Programmability of the slope
Low frequency time-domain BIST (several KHz range)	high	medium	medium	low	high
Medium frequency time-domain BIST (100K-1MHz range)	high	Low (fast slope= fast calibration)	high	low	high
Monotonicity BIST for ADC	low	low	low	Medium (less than ADC)	low
Linearity BIST for ADC	medium	medium	low	High (larger than ADC)	low

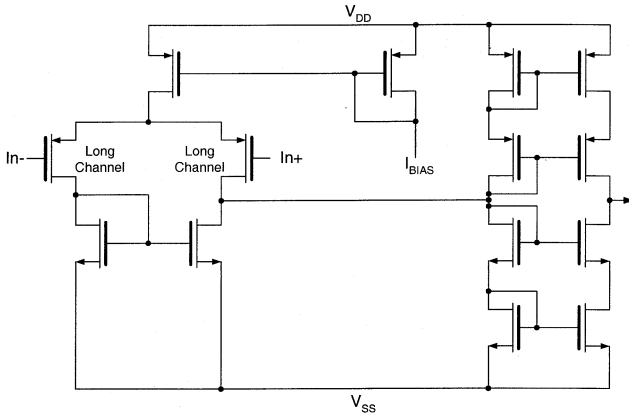


Fig. 6. Detailed schematic of the OTA.

not discharge through the output impedance of OTA1 while the timers are ramping. Because V_{outf} is not a continuous function, we have to use a DT implementation of the adaptive scheme

$$V_{ctrl} \cong G \sum_{i=1}^{\infty} \left[\int_{t-\Delta t}^t (V_{target} - V_{outfi}) dt \right] + V_{ctrl0} \quad (5)$$

where Δt defines the delay during which the integration of the error is performed by the OTA-C (controlled by S_1). Switches S_2 and S_3 limit the leakage of C_{integr} into the resistor and M_6 in Fig. 4. The gain G must be set so that the feedback gain is low enough to guarantee stability. The delay Δt must be set in such a way that the rise or fall on V_{ctrl} from one time step to the other are converging. In order to guarantee convergence, each OTA is made of a differential input stage with long channel length pMOS drivers to ensure low g_m ($0.7 \mu A/V$) and a cascode current-mirror output stage to ensure high output impedance (see Fig. 6). Δt was set to $1 \mu s$.

B. Second Implementation: Error-Cancellation LMS Integrator

When the calibration delay t_{ramp} becomes large (for monotonicity or histogram tests of ADCs) and the ramping capacitor is on chip, the control voltage has to be very precise. The second implementation of the LMS integrator (Fig. 7) uses an error-cancellation approach with two single-ended integrators to reduce the effect of charge injection. Also, the basic ramp generator

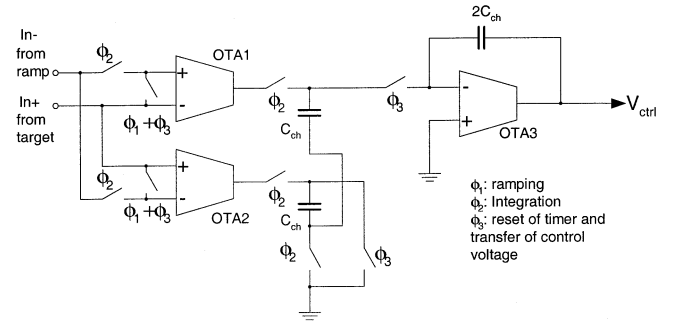


Fig. 7. Second implementation of the LMS integrator.

(Fig. 4) was modified by removing M_6 and placing it as a switch between the drain of M_4 and C_{ramp} . This allows the elimination of the resistor in Fig. 4 and the switches S_2 and S_3 in Fig. 5. The OTAs are identical to the one used in the first OCRG version. The charging capacitor C_{ch} is 14.9 pF . Leakage current in the switches [20] causes the stored voltage on the capacitor to decrease as

$$V_{cap}(t) = V_{cap0} - \frac{I_{leak}}{C} t \quad (6)$$

where $V_{cap}(t)$ is the capacitor voltage, V_{cap0} is the initial capacitor voltage, I_{leak} is the leakage current of the switch, and C is the capacitor used to store the control voltage of the adaptive loop. The leakage current of a wide ($20/0.6$) transistor in the AMI $0.5\text{-}\mu m$ technology is less than $2.5 \text{ pA}/\mu m$, which is a very conservative value for our small switches. The use of transmission gates and the fact that some capacitors are connected to two switches (Fig. 7) raises the leakage current to $10 \text{ pA}/\mu m$. Using a 15-pF capacitor and a 1-ms delay results in a maximum voltage drop of 0.67 mV . This has virtually no effect on the output current charging the ramping capacitor, and is smaller than the clock feedthrough and charge injection error sources.

The second OCRG implementation shows significant improvement on the precision of long ramps with on-chip capacitors. Fig. 8 shows a simulation of the calibration process for a ramp ranging from 0 to 2 V within 1 ms . Fig. 9 shows a more detailed view (zoom) of the ramp once calibrated, along with the integral nonlinearity (INL) of the ramp.

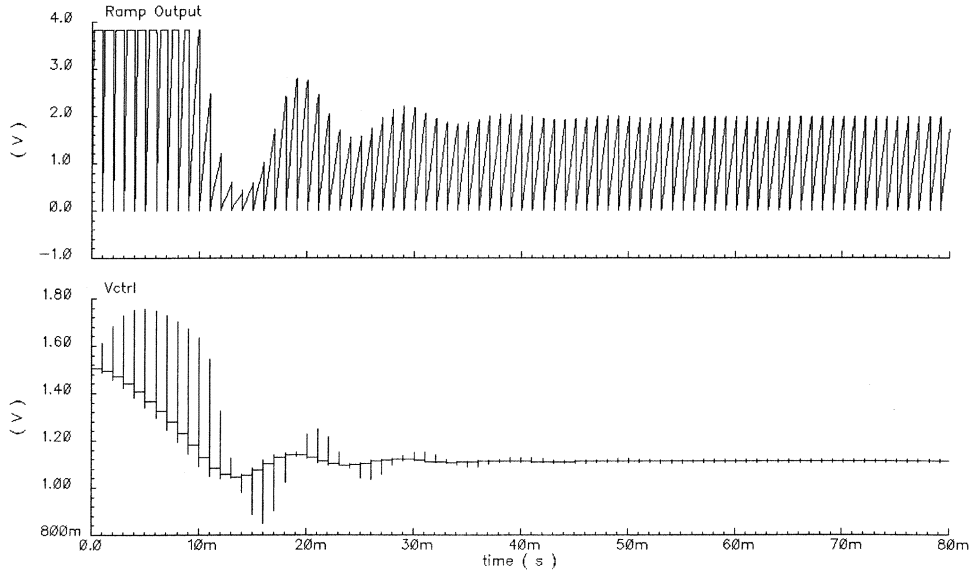


Fig. 8. Simulation of the calibration process. Upper trace shows the ramp being calibrated. Lower trace shows the control voltage.

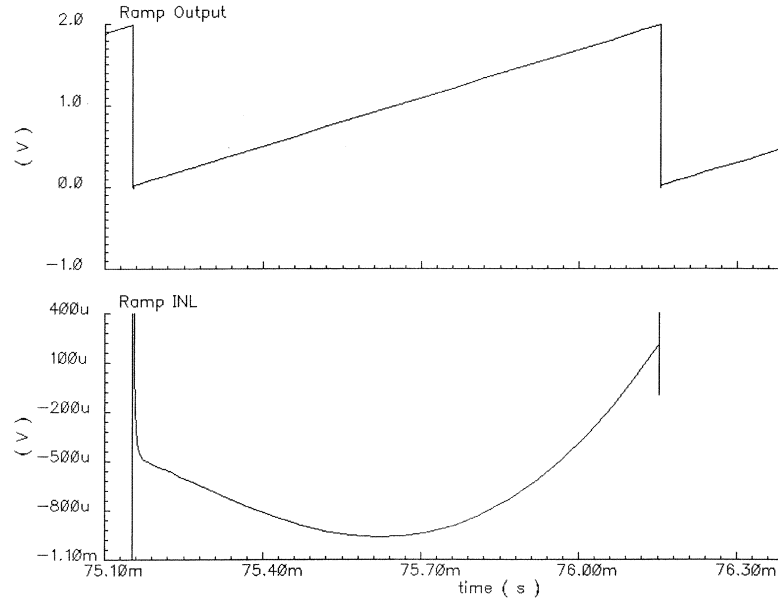


Fig. 9. Detailed view of a calibrated ramp and INL. Upper trace shows the calibrated ramp. Lower trace shows the ramp INL.

IV. THIRD IMPLEMENTATION: SC FULLY DIFFERENTIAL LMS INTEGRATOR

The purpose of the third version of the OCRG was to assemble a BIST scheme for pipeline ADCs. The design constraints were to improve the linearity and stability of the ramp at the cost of a slightly more complex circuitry, as well as to convert it to a fully differential topology. In the case of an ADC histogram test, the maximum INL of the input ramp should be $INL_{max} < FSR/(2^N HPC)$, where FSR is the full-scale range of the ADC under test, N is the number of bits of the ADC, and HPC is the number of desired hits per code. The linearity provided by the previous implementations is insufficient for typical ADC histogram tests.

A. Improvement of Ramp Stability

In order to perform ADC histogram testing, a very stable low-current source with high power-supply rejection ratio (PSRR) is needed. We decided to use the self-biased Widlar current source [21] shown in Fig. 10. M_3 , operating in triode region, is added to control the current. Also, by using additional design variables (such as the relative sizes of M_1 and M_2 , as well as the sizes of M_3 and R_1), the G_m of the current source can be lowered, which reduces the OCRG loop gain and, thus, decreases the sensitivity to noise and leakage on the charging capacitor. By using the change of variable $x^2 = I_2$, we have $I_1 = I_2 = I_{out} = 0$ and (7), shown at the bottom of the next page, where α and β are the current mirror ratios $I_1 - I_2$ and $I_{out} - I_2$, respectively. When $(V_{ctrl} - V_{TN})$ becomes large, the whole equation becomes a constant. Fig. 11 shows a plot of this function for typical component

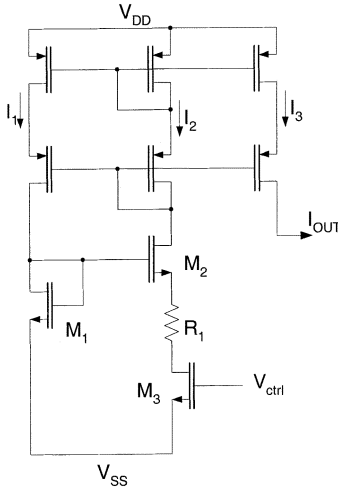


Fig. 10. Self-biased Widlar current source.

values. Proving that this current source can be used in an adaptive scheme such as Fig. 3(a) involves solving (2) and (7), which is quite complex. Instead, we will take advantage of the fact that with the proper choice of components, the shape (curvature) of the relation described by (7) becomes fairly linear in the range of interest. In that case, we have $I_{out} \approx K(V_{ctrl} - V_{TN})$, where K incorporates the effect of the choice of components. It is now easy to show that the control voltage is given, according to the LMS algorithm, by the same equation as (4). Moreover, it has been found from behavioral and transistor-level simulations that the adaptive scheme gives very good results in the case where the I_{out} versus V_{ctrl} relation of the current source is not linear.

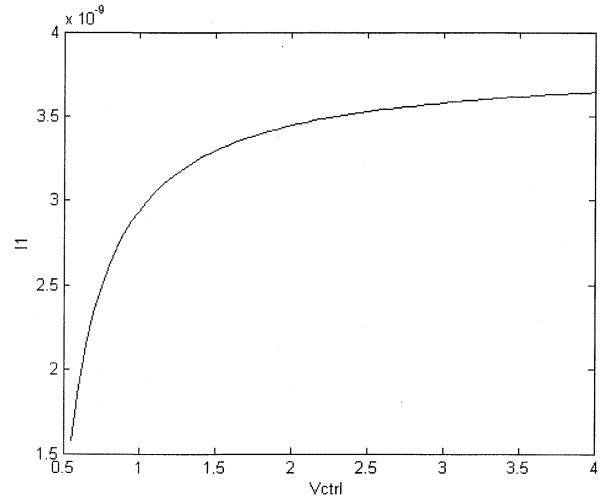
B. Improvement on Ramp Linearity

In the simplified ramp generator Fig. 12(a)], $V_{c,real}$ represents the real capacitor voltage, including the effect of the output impedance R_o of the current source. An output-dependent offset current will flow through R_o and add to the nominal current I causing nonlinearity on the output ramp. The capacitor is reset to V_{cs} on ϕ_2 (which corresponds to $t = 0$ in the following analysis). Fig. 12(b) shows the Thevenin equivalent, which simplifies the analysis. It can be shown that the maximum error in the ramp is given by

$$e_{max} = INL_{max} = \frac{(V_{cf} - V_{cs})t_{e\max}}{t_{ramp}} + V_{cs} - V_a + (V_a - V_{cs})e^{-t_{e\max}/R_oC} \quad (8)$$

where

$$t_{e\max} = \ln \left(\frac{R_oC(V_{cf} - V_{cs})}{t_{ramp}(V_a - V_{cs})} \right)^{-R_oC}. \quad (9)$$

Fig. 11. Typical output current from the self-biased Widlar current source in function of V_{ctrl} .

V_{cf} is the final voltage of the ideal ramp (with $R_o = \infty$) and $V_a = V_{DD} + IR_o$. If we want to test a 12-b ADC with FSR = 2 V and make a 16 hits per code histogram, (8) predicts that we need an output impedance of about 300 G Ω . Note that this is dc output impedance. Still, this is a very large value and it is unlikely that we can achieve such a high value in a low-voltage process. The present current source (Fig. 10) has a dc output impedance of 19 G Ω , based on simulation results.

A reduction on the effect of R_o can be achieved by keeping the capacitor node constant, which is done by using an operational amplifier (opamp) in feedback of the charging capacitor as shown in Fig. 13. It can be shown that for an opamp gain of A , the maximum error is now given by

$$e_{max} = INL_{max} = \frac{(V_{cf} - V_{cs})t_{e\max}}{t_{ramp}} + V_{cs} - A \left[\left(V_a + \frac{V_{cs}}{A} \right) e^{-t_{e\max}/R_oC(A+1)} - V_a \right] \quad (10)$$

$$t_{e\max} = \ln \left[\frac{R_oC(A+1)(V_{cs} - V_{cf})}{t_{ramp}(V_{cs} + AV_a)} \right]^{-R_oC(A+1)}. \quad (11)$$

The linearity improvement is in the order of A . The slope of the curve is given by the derivative of $V_{c,real}$ with respect to time and is

$$m(t) = \frac{dV_{c,real}}{dt} = \frac{-e^{-t/R_oC(A+1)}}{R_oC(A+1)} [AV_a - V_{cs}]. \quad (12)$$

$$I_{out} = \frac{2\beta\alpha K p_N (W_3/L_3)^2 (V_{ctrl} - V_{TN})^2 \left(\alpha L_1/W_1 - 2\sqrt{\frac{\alpha L_1 L_2}{W_1 W_2}} + L_2/W_2 \right)}{\left[R_1 K p_N \frac{W_3}{L_3} (V_{ctrl} - V_{TN}) + 1 \right]^2}. \quad (7)$$

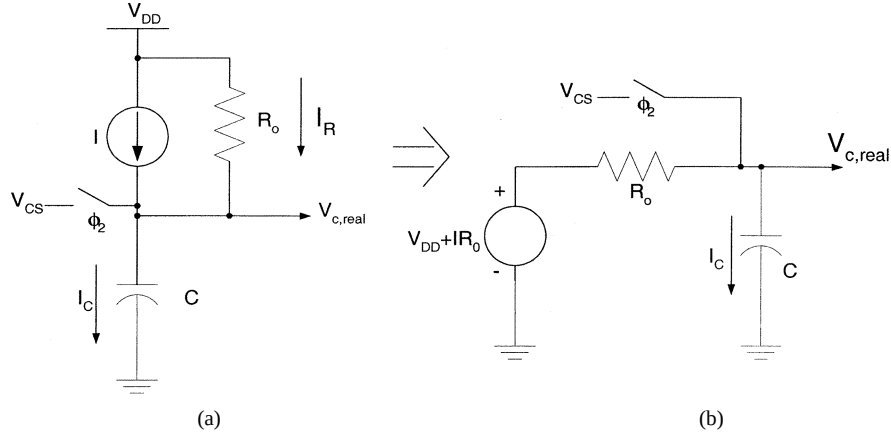


Fig. 12. Simplified circuit of the ramp generator with current source output impedance. (a) Original circuit. (b) Thevenin equivalent to simplify the calculations.

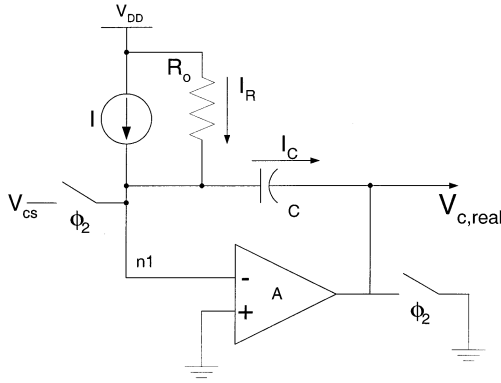


Fig. 13. New circuit to decrease the effect of R_o .

When A becomes large, the slope becomes (using L'Hopital's rule)

$$m(t)|_{A \rightarrow \infty} = \frac{-V_{DD} - IR_o}{R_o C} \quad (13)$$

which is a constant for a given current I . This proves that the slope is constant at all times and, thus, that the curve is linear. Also, when A becomes large, the end point of the curve becomes independent of A . We can set V_{cs} and V_{cf} and find the required nominal value for I in Fig. 13

$$I = \frac{1}{R_o} \left[\frac{1}{A} \left(\frac{V_{cf} - V_{cs} e^{-t_{\text{ramp}}/R_o C(A+1)}}{e^{-t_{\text{ramp}}/R_o C(A+1)} - 1} \right) - V_{DD} \right]. \quad (14)$$

A systematic methodology can now be used to define the value of A needed for a particular application where a ramp is needed to go from V_{cs} to V_{cf} in a delay of t_{ramp} , with a maximum $\text{INL} = \text{INL}_{\text{test}}$.

- 1) Start with a small value of A . For example, $A = 10$.
- 2) Choose a design value for R_o such that its associated offset current will never get higher than the total $I_{\text{total}} = I + I_R$ needed. We already know that we need $I_{\text{ideal}} = C(V_{cf} - V_{cs})/t_{\text{ramp}}$, therefore, $R_o > V_{DD}/I_{\text{ideal}} = V_{DD}t_{\text{ramp}}/C(V_{cf} - V_{cs})$. This will set a design constraint on the current source.
- 3) Find the nominal value of I needed with (14).
- 4) Find the resulting INL_{max} with (10). $\text{INL}_{\text{max}} > \text{INL}_{\text{test}}$ means that A is too low. In that case, increase A and repeat the procedure from step 3.

The simulation result from a transistor-level implementation of the current source with the feedback opamp is shown in Fig. 14. The INL error is now only $\pm 27 \mu\text{V}$. This precision is sufficient to test the 12-b ADC with a 2-V input range and 16 HPC described earlier.

C. Implementation of the Third Version

All the internal signals of the third version, except for the control signal, are fully differential in order to reduce the effect of offsets and the noise in the system and because the ADC under test has a differential input. We now have one target voltage for each ramp. The input range of the ADC is from 0.75 to 1.25 V and the power supply is 1.8 V (see Fig. 15).

The fully differential opamp is a two-stage topology with a telescopic cascode input stage (see Fig. 16). It was decided not to put the cascode on the output stage so that the output swing would be large enough. Since the ramping phase is long, the opamp contains a continuous-time common-mode feedback circuit in addition to the reset of its input nodes to V_{cm} at every clock cycle. The common-mode feedback circuit is a simple differential pair with diode-connected loads. The dc gain of the opamp is 104 dB and the gain bandwidth is 46 MHz. The phase margin is 75° . The linear-gain output swing is 0.55–1.5 V. The input and feedback capacitors of the LMS integrator are 0.5 and 4 pF, respectively (gain of 1/8). The differential-to-single-ended block is used to convert the differential output of the LMS integrator to the single-ended input of the current source in the ramp generator. The topology is a simple differential stage with diode-connected active loads and a gain around unity.

The clocking necessary for this system is made of three nonoverlapping phases. The first phase ϕ_1 is the ramping phase and lasts for 1.024 ms. The two other phases, ϕ_2 and ϕ_3 (integration and reset phases, respectively), last for $1 \mu\text{s}$ each. In addition to these basic phases, we also need their inverse and their delayed version for bottom-plate sampling. The clock generator is a three-flip-flop state machine and a counter to create the 1.024-ms delay on ϕ_1 .

V. MEASUREMENT RESULTS

All three versions of the OCRG implementations have been fabricated and tested. The first implementation was fabricated on an ORBIT 2- μm process from MOSIS (see Fig. 17). The

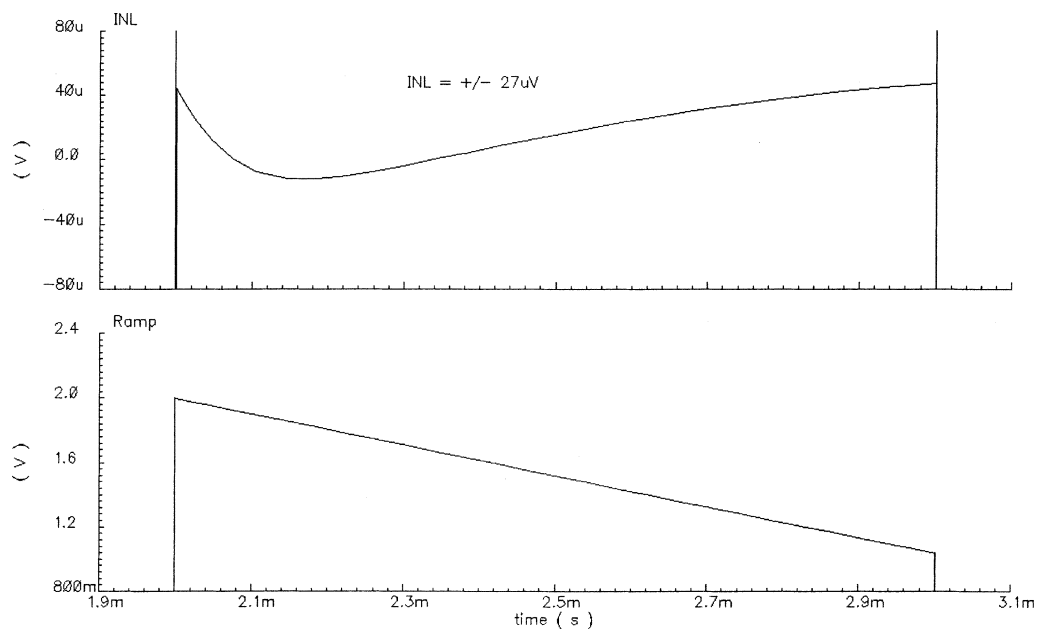


Fig. 14. Transistor-level simulation of the OCRG with opamp in feedback. Upper trace shows the ramp INL. Lower trace shows the calibrated ramp.

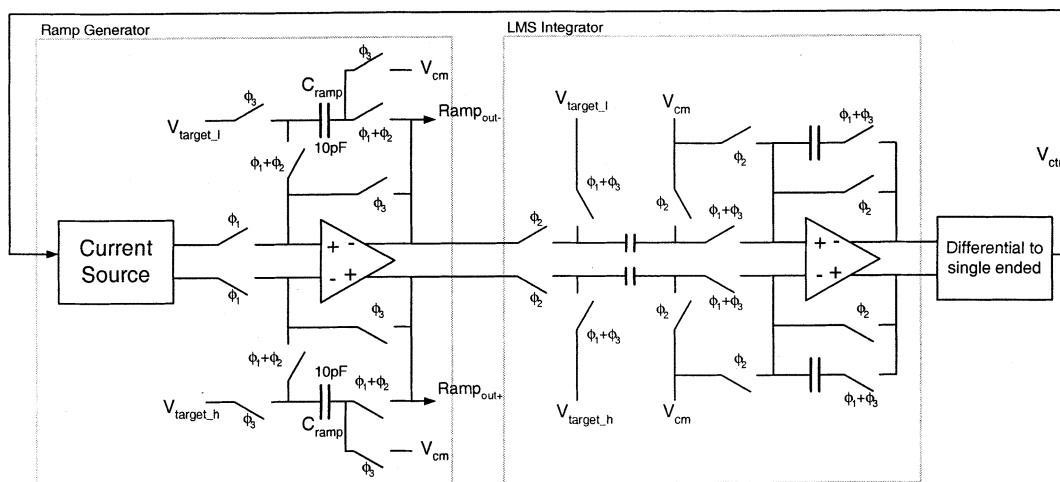


Fig. 15. Detailed view of the third version of the adaptive OCRG.

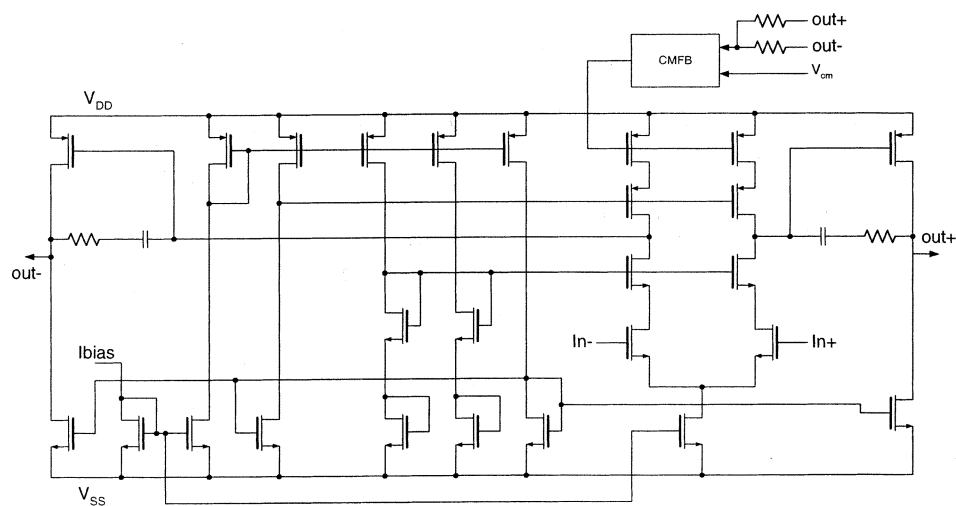


Fig. 16. Detailed schematic of the opamp.

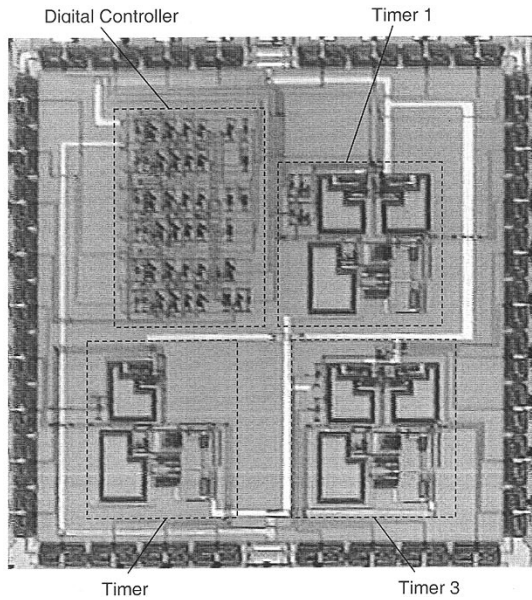


Fig. 17. Microphotograph of the first implementation of the OCRG.

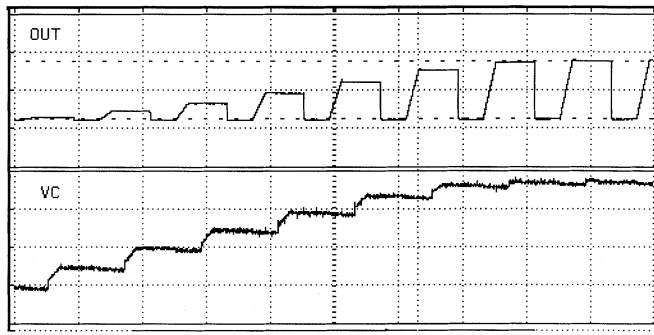


Fig. 18. Chip test results from the first OCRG implementation. Upper trace shows the ramp being calibrated. Lower trace shows the control voltage.

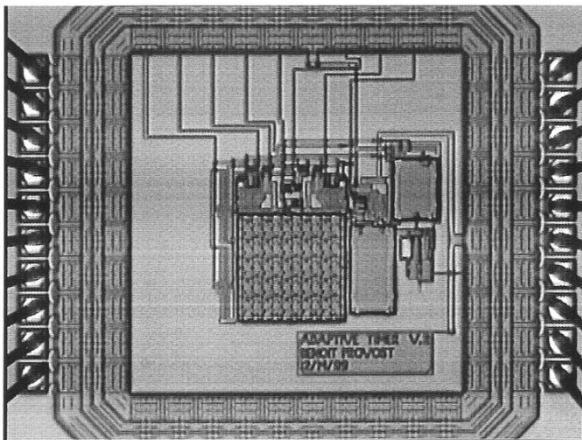


Fig. 19. Chip microphotograph of the second version of the OCRG.

chip contains two master/slave pairs (different implementations of the timer), a finite-state machine (FSM) to generate the clocks and a slave to be controlled externally for test purposes. The entire circuit measures 3.2 mm^2 and a single master/slave pair with FSM measures 1 mm^2 . The measurement results are shown in Fig. 18. This version was designed for an operation frequency

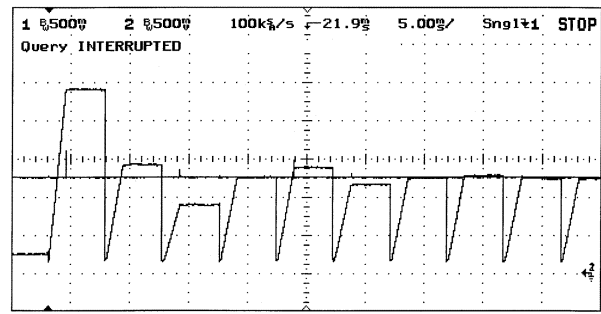


Fig. 20. Calibration process for the second version of the OCRG. The calibration process requires approximately nine iterations.

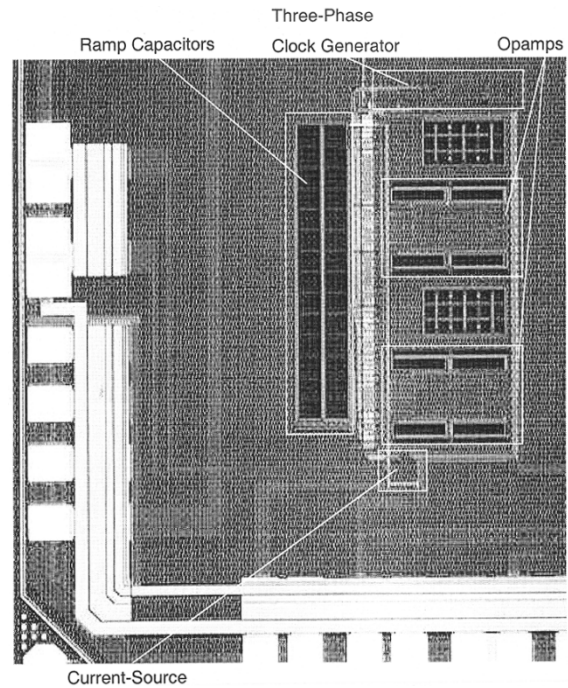


Fig. 21. Chip microphotograph of the third version of the adaptive OCRG.

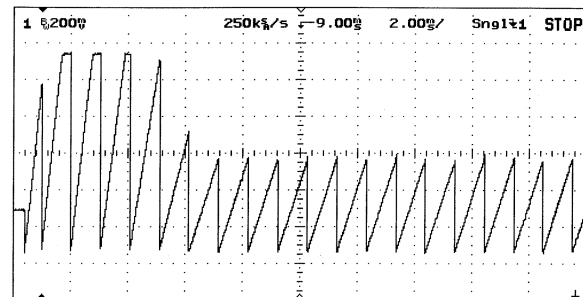


Fig. 22. Calibration process for the third version of the OCRG.

of 10 kHz. Extra capacitance was added externally to the ramping and LMS capacitors. We can see that the output ramp (OUT) gets precisely calibrated to the target final value. This shows the validity of the adaptive scheme. The measured transconductance of the OTA is $0.7 \mu\text{A/V}$, and the error on the final value of the ramp is 20 mV, which translates into a slope error of 0.6%.

The second version of the OCRG has been fabricated on an AMI $0.5\text{-}\mu\text{m}$ process from MOSIS (see Fig. 19). Post-layout

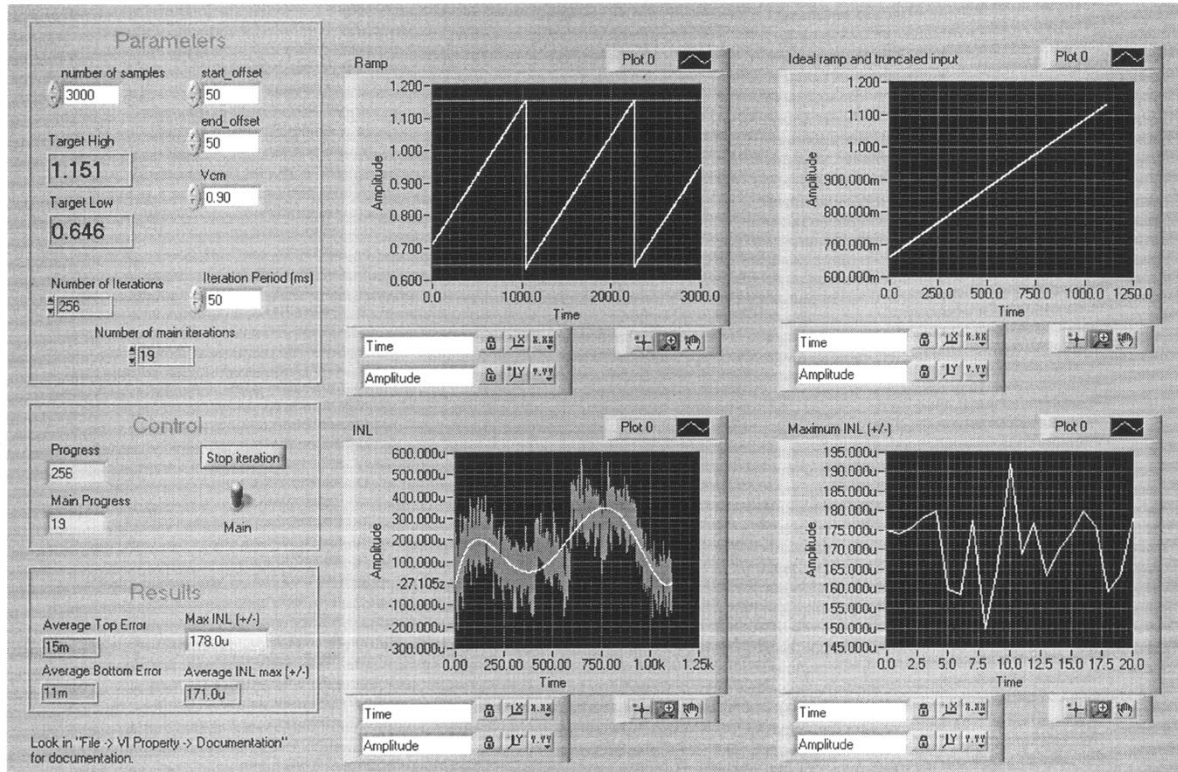


Fig. 23. Measurement interface for the third version of the OCRG.

TABLE II
PERFORMANCE RESULTS, APPLICABILITY, AND COMPARISON

Name	Complexity	Linearity (bits)		Slope Error	Start/Stop errors	Calib. Time	Program-mability	Typical Application
		Simul.	Meas.					
Ver. 1	Very Low	N/A	N/A	0.6%	20mV	9 iter.	Low	TDBIST
Ver. 2	Low	11	10	1.5 %	14mV	9 iter.	Low	TDBIST & ADCMT
Ver. 3	High	15	11	0.6%	12mV	12 iter.	Med.	ADCMT & ADCLT
Wen & Lee	Low	12*	N/A	N/A	N/A	N/A	N/A	ADCLT (not self-calibrating)
Huang et al	High	14**	N/A	N/A	N/A	N/A	N/A	ADCLT (not self-calibrating)
Jansson et al	Medium	N/A	8	N/A	N/A	10	High	TDBIST & ADCMT
Bernard et al	Low	14	N/A	0.4%	12mV	10	N/A	ADCLT

*Not mentioned in the paper; assumed 12 bits accuracy.

**Not mentioned in the paper; assumed 8 bits ADC. Linearity results are based on a -0.5 LSB INL limit.

simulations show that the errors on the starting and final voltages are 14 mV, which translates in an average slope error of 1.5%. The post-layout simulations show a ramp INL of $\pm 570 \mu\text{V}$ (11 b) and a slope distortion of 0.2%. We can see in Fig. 20 that the ramp calibrates itself within nine iterations. After analysis of the measurements, the ramp INL was found to be approximately ± 1 mV (10 b), which translates into a slope distortion of approximately 0.4%.

The third version of the OCRG was fabricated on a $0.18\text{-}\mu\text{m}$ process from Texas Instruments Inc. (see Fig. 21). Dimensions are $0.6 \times 0.3 \text{ mm}^2$. In measurements, the ramp goes from 0.7 to 1.3 V within 1.024 ms with a start and stop error of 12 mV. The average slope error is 0.6%. The calibration process is shown in Fig. 22. The INL of the ramp was measured with a test setup using a PXI6071E multifunction data acquisition card

from National Instruments. A LabView program was written to perform several tasks such as curve fitting to extract the INL shape from the noise generated by the digital signals. It also computes the best-fit straight line from the acquired ramp in order to calculate the INL (see Fig. 23). The measured average ramp INL is $\pm 175 \mu\text{V}$ (11 b), with a maximum of $\pm 190 \mu\text{V}$ and a minimum of $\pm 150 \mu\text{V}$. The ramp slope can be adjusted by varying the global clock frequency. The lowest slope attainable was 0.4 V/ms, and the highest was 2 V/ms. A lower slope results in unstable ramps and a higher slope results in excessive errors on the start and stop values. The start and stop targets are also widely adjustable. The maximum differential slope amplitude is 1.6 V (limited by the linear output range of the opamps). Larger amplitudes are possible, but the INL becomes excessive. Amplitudes as small as $0.2V_{\text{pp}}$ were measured with

good linearity. Smaller amplitude would result in instability. The typical number of iterations required for calibration is 12.

VI. CONCLUSION

This paper presented three versions of on-chip adaptive ramp generator designs to be used in time-domain BIST for analog circuits and ADC testing. The adaptive approach allows the generation of very long on-chip ramps without the need for manual fine tuning and makes the system process independent. The technique needs only the system clock and a reliable reference voltage, which, in the case of time-domain testing, can be almost any voltage reference already present in the system. Table II provides the applicability of each implementation in consideration of its performance and complexity. It also compares the obtained performance with other published implementations. Many performance results were unavailable since the performance metrics for on-chip ramp generation are application dependent and not well established. It is clear that we can trade complexity with performance, depending on the application we are considering. The third version of the OCRG is currently being used in a pipeline ADC BIST technique.

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