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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ELMOS SEMICONDUCTOR SE
Petitioner

v.

TEXAS INSTRUMENTS INCORPORATION
Patent Owner

Patent No. 11,653,432
Filing Date: Nov. 30, 2021
Issue Date: May 16, 2023

LIGHT-EMITTING DIODE (LED) DRIVER SYSTEM WITH SLEW-RATE
CONTROL

**PETITION FOR *INTER PARTES*
REVIEW OF U.S. PATENT NO. 11,653,432
AIA review number: IPR2024-00802**

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Patent Trial and Appeal Board
U.S. Patent & Trademark Office
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EXHIBIT LIST

Ex. No.	Description
1001	U.S. Patent 11,653,432 to Meng et al. (“the ‘432 Patent”)
1002	App. Ser. No. 17/537,694 for U.S. Pat. 11,653,432 File Wrapper History (“File History”)
1003	Declaration of Peter Glösekötter in Support of Petition for <i>Inter Partes</i> Review of U.S. Patent No. 11,653,432 (“Glösekötter Decl.”)
1004	Curriculum Vitae of Peter Glösekötter (“Glösekötter Curriculum Vitae”)
1005	U.S. Patent 10,136,496 to Sudhaus (Sudhaus)
1006	Japanese Patent JP 2012160287 A to Ryoichi (Ryoichi) with English translation
1007	Certification of Translation for Ryoichi
1008	Article published in October 2016 edition of Elektronik Praxis by Sudhaus 2016 entitled <i>Die Verlustleistung in linearen Regelsystemen günstig verteilen</i> (Praxis) with English translation
1009	U.S. Patent 11,599,132 B2 to Wu et al. (Wu)
1010	Article published in IEEE Journal of Solid-State Circuits – March 2003 entitled <i>On-chip ramp generators for mixed-signal BIST and ADS</i> self-test by Provost (Provost)
1011	White paper by Texas Instruments entitled <i>Voltage-to-current (V-I) converter circuit with MOSFET</i> – document number SBOA327A – December 2019 – Revised August 2021 (TI Paper)
1012	White paper entitled “ <i>The MOSFET Current Mirror</i> ” by the University of Kansas, dated April 25, 2011 (UK Paper). Chrome-extension://efaidnbmnnnibpcajpcglclefindmkaj/https://www.ittc.ku.edu/~jstiles/412/handouts/4.5%20Biasing%20in%20MOS%20Amp%20Circuits/The%20MOSFET%20Current%20Mirror.pdf
1013	ELMOS presentation at the International CAR Symposium of February 4, 2015, by Burchard entitled “Wärmemanagement mit intelligenten Linearreglerkonzepten” (the Burchard presentation) with English translation.

I. INTRODUCTION

Elmos Semiconductor SE petitions for *inter partes* review of Claims 1-20 of United States Patent 11,653,432 to Meng (the “’432 Patent”). The challenged Claims of the ‘432 Patent recite a minimal number of basic electronic components (i.e. one error amplifier, one slew rate controller, and one shunt resistor in independent Claim 1, with the addition of one LED string in independent Claim 11; and two power transistors, one error amplifier, and one slew rate controller in independent Claim 16). The ‘432 Claims simply claim that such minimal basic components be arranged (“configured”) for a proposed purpose. Electronic circuits including these three (or four) basic components were well known before the priority date of the ‘432 Patent and configured for many purposes, including the claimed purpose of the ‘432 Patent.

The ‘432 Patent Claims are written with no limitation regarding the arrangement of their basic components, so long as their proposed purpose is accomplished.

Accordingly, prior art references, that include the recited components, and are capable of bringing about the proposed purpose, anticipate and/or render obvious the issued Claims of the ‘432 Patent.

The Applicant provided no references in an Information Disclosure Statement. This petition includes representative prior art, including competitor’s products, and one of many relevant circuits published by the Applicant.

The Examiner cites only two patents of mild interest and no non-patent literature references. The Reasons for Allowance merely repeat the claim limitations and provide no insight into what the Examiner considered novel.

II. MANDATORY NOTICES (37 C.F.R. § 42.8(a)(1)).

A. Real Party-In-Interest under 37 C.F.R. § 42.8(b)(1)

Petitioner ELMOS SEMICONDUCTOR SE (“Elmos”) is the real party-in-interest for this Petition.

B. Related Matters under 37 C.F.R. § 42.8(b)(2)

None.

C. Lead and Back-Up Counsel under 37 C.F.R. § 42.8(b)(3), 37 C.F.R. § 42.10(a)

Lead Counsel: Michael McCandlish (Reg. No. 68,668)	MINDFUL IP PLLC 28175 Haggerty Rd. Novi, MI 48377 mmccandlish@mindfuliplaw.com T: (248) 444-0470
Back-up Counsel: Joseph P. Kincart (Reg. No. 43,716)	TRACNIK LAW, PLLC 5923 Saxony Woods Lane Jacksonville, FL 32211 jkincart@tracnik.com T: (904) 305-4809

D. Service Information

As identified in the attached Certificate of Service, an entire copy of the present Petition, including Exhibits and power of attorney, is being served by U.S.P.S. Priority Express, costs prepaid, to the address of Cynthia Hoff Trochu, Texas Instruments Senior

Vice President, Secretary and General Counsel, P.O. Box 660199, Dallas, TX 75266-0199, United States, with a courtesy copy to the attorney of record. Petitioner may be served at the lead counsel address in Sect. II. C. of this Petition. Petitioner consents to service by e-mail at the e-mail addresses provided above.

E. Power of Attorney

A power of attorney is being filed with this Petition in accordance with 37 C.F.R. § 42.10(b).

III. PAYMENT OF FEES – 37 C.F.R. § 42.103

This Petition for *inter partes* review requests review of Claims 1-20 of the '432 Patent and is accompanied by a payment of \$41,500. See 37 C.F.R. § 42.15. Thus, this Petition meets the fee requirements under 35 U.S.C. § 312(a)(1). Payment is authorized for any additional fees due in connection with this Petition to be charged to Deposit Account No. 603732.

IV. REQUIREMENTS FOR INTER PARTES REVIEW UNDER 37 C.F.R. § 42.104

A. Grounds for Standing under 37 C.F.R. § 42.104(a)

Petitioner certifies that the '432 patent is available for *inter partes* review and further certifies that Petitioner is not barred or estopped from requesting this *inter partes* review on the grounds identified herein.

B. Identification of Challenge under 37 C.F.R. § 42.104(b) and Statement of Precise Relief Requested

Petitioner requests *inter partes* review of the petitioned Claims under the

statutory grounds set forth in the table below. Petitioner asks that each of the Claims be found unpatentable. An explanation of how the petitioned Claims are unpatentable is included in Sects. IX and X of this Petition. Additional explanation and support for specific grounds of rejection is set forth in the Declaration of a technical expert, Dr. Peter Glösekötter (Glösekötter Decl.) (Ex1003.)

Ground	‘432 Patent Claims	Basis for Challenge
1	1-3, 6, 10-11, 16-17	Obvious under 35 U.S.C. § 103 (“§ 103”) over Sudhaus*
2	1-4, 6-7, 10-12, 15-18	Obvious under § 103 over Sudhaus* in view of Ryoichi*
3	1-4, 6-7, 10-12, 15-18	Obvious under § 103 over Sudhaus* in view of Ryoichi* and further in view of Praxis*
4	1-4, 6-7, 10-12, 15-18	Obvious under § 103 over Sudhaus* in view of Ryoichi* in view of Praxis*, and further in view of Wu*
5	1-20	Obvious under § 103 over Sudhaus* in view of Ryoichi* in view of Praxis* and further in view of Provost*, TI Paper*, and UK Paper*
*Prior art reference not considered during the prosecution of the ‘432 Patent.		

Praxis, Sudhaus, Wu, Ryoichi, Provost, TI Paper, and UK Paper are prior art under at least one of 35 U.S.C. § 102(a)(1) or 35 U.S.C. § 102(a)(2). This Petition and the Glösekötter Decl. cite prior art materials not disclosed by the ‘432 Applicant, and not considered by the USPTO during prosecution of the ‘432 Patent.

Grounds 1-5 are not duplicative under 35 U.S.C. §§ 315(d), 325(d). Petitioner requests institution on all grounds, but to the extent that the Board determines to institute on less than all grounds, the Petitioner requests that the Board institute on Ground 3, Ground 4, and Ground 5.

C. Threshold Requirement for *Inter Partes* Review under 37 C.F.R. § 42.108(c)

Inter partes review of the petitioned Claims should be instituted because this Petition establishes a reasonable likelihood that Petitioner will prevail with respect to at least one of the Claims challenged. See U.S.C. § 314(a). Each limitation of each challenged Claim is disclosed by and/or obvious in light of the prior art as shown in detail in Sections VI, IX, and X below.

V. BACKGROUND OF TECHNOLOGY RELATED TO THE ‘432 PATENT

The ‘432 Patent relates to a driver system to supply energy to light-emitting diodes (LEDs). LEDs have taken on a primary role for automobile lighting, and other applications. Power to LEDs is commonly controlled via integrated circuits (ICs) with driver circuits and driver transistors controlling electrical energy delivered to the LEDs.

In automotive applications, supply voltage conditions for LED driver circuits can vary significantly. As supply voltage increases, heat dissipated by driver transistors can increase to a critical point at which driver circuits can be damaged by overheating.

Known approaches for protecting LED driver circuits, pioneered by Petitioner, include using an IC with an error amplifier, driver outputs (integrated in an IC) and an

external shunt resistor to drive an LED load. Dependent on the supply voltage, a portion of power to the LED load is delivered through a second driver and associated external shunt resistor. The external resistor dissipates some of the excess heat, thereby extending a voltage range under which an LED driver system can operate without suffering damage due to overheating.

The ‘432 Patent purportedly relates to such a driver system for LEDs. The ‘432 Patent includes two current driver paths for an LED load, with one current path including an external shunt resistor. As supply voltage increases, a portion of the total current supplied to the LED load is purportedly shifted to the current path including the shunt resistor, with the intent of transferring heat losses to the shunt resistor. Ex1001, 2:27-31, 2:40-49.

Prior art disclosing such LED drivers was publicly available at the time of filing of the ‘432 Patent. For example, Sudhaus, issued on Nov. 20, 2018, discloses a driver system including two or more current paths for supply power to an LED load. Ex1005, 2:25-53. Praxis appeared in the October 2016 edition of Elektronik Praxis, Ex1008, Section entitled “Modern linear regulators with a power distribution,” second and third paragraphs, Figure 1 describing such drivers. Further, the Burchard presentation at the International CAR Symposium of February 4, 2015, entitled “Wärmemanagement mit intelligenten Linearreglerkonzepten” described these concepts. Ex1013, slides 6 and 7.

Independent Claim 1 of the ‘432 Patent is an apparatus claim with only two

claim elements listing basic electronic components: an error amplifier, and an amplifier output stage comprising a slew rate controller, a shunt resistor, current paths, and an LED string. All other limitations are functional limitations (e.g. “configured to” “control a slew rate” and “provide a total current through”). Functional limitations without corresponding structure cannot be afforded patentable weight, and limiting the scope of the Claims solely to overcome prior art without corresponding structural element limitations is contrary to the law and to public policy.¹ Therefore, the ‘432 Claims must be construed with functional limitations only in view of the basic electronic components consisting of: an error amplifier, and an amplifier output stage comprising a slew rate controller, a shunt resistor, current paths, and an LED string.

VI. THE PRIOR ART RELIED ON FOR GROUNDS 1-5

The ‘432 Patent was filed on Nov. 30, 2021. The prior art references included in the grounds of unpatentability pre-date Nov. 30, 2021.

Sudhaus, Praxis and Wu teach regulated supplies that provide source current

¹In re Schreiber, 128 F.3d 1473, 1477 (Fed. Cir. 2011);

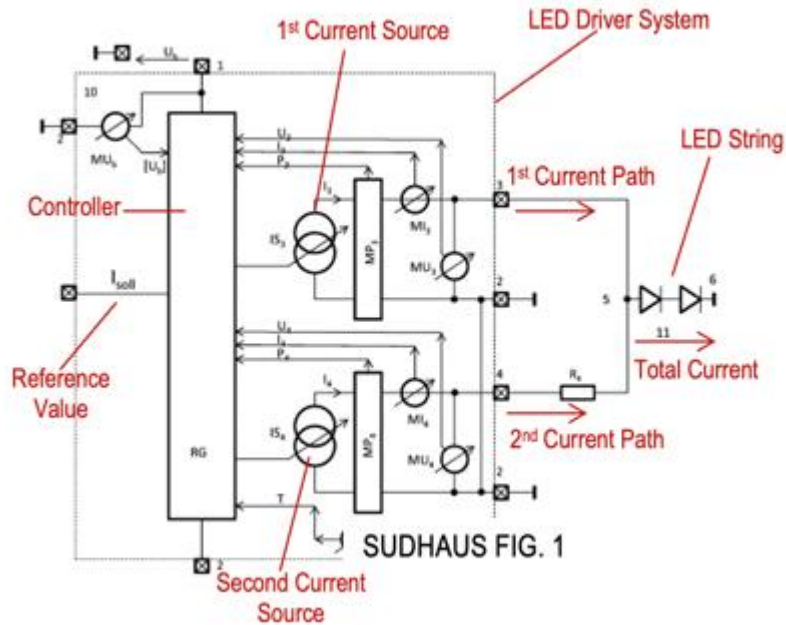
see also Bettcher Indus., Inc. v. Bunzi USA, Inc., 661 F.3d 629, 654 (Fed. Cir. 2011); Marrin v. Griffin, 599 F.3d 1290, 1294 (Fed. Cir. 2010) (“For apparatus claims, ..., generally patentability depends on the claimed structure, not on the use or purpose of that structure.”)

(from a positive supply) to a load, Ryoichi is configured to provide a sink current (to ground) to a load. It would have been obvious to POSITA that the concepts and circuits presented in Ryoichi are applicable and easily adapted to the regulated supplies presented in Sudhaus, Praxis and Wu.

A. U.S. Pat. No. 10,136,496 B2 to Sudhaus (“Sudhaus”) (Ex. 1005)

Sudhaus, titled “Apparatus for Supplying Electrical Energy to a Consumer” issued on November 20, 2018, and therefore qualifies as prior art under 35 U.S.C. § 102(a)(1).

Sudhaus discloses, in reference to Fig. 1, a Controller RG operative to control a total current delivered to an LED load through two current paths, based on a desired value for I_{soll} . Ex1005, 4:46-50, Fig. 1. The two current paths include a first current path including a current source IS_3 and a second current path including a current source IS_4 in series with an external resistor R_4 .



Sudhaus further teaches to manage power dissipation, gradually shifting a portion of the total current from the first current path to the second current path as the system supply voltage increases. Ex1005, 5:40-46, 6:18-26.

B. JP 2012160287 A to Ryoichi (“Ryoichi”) (Ex1006)

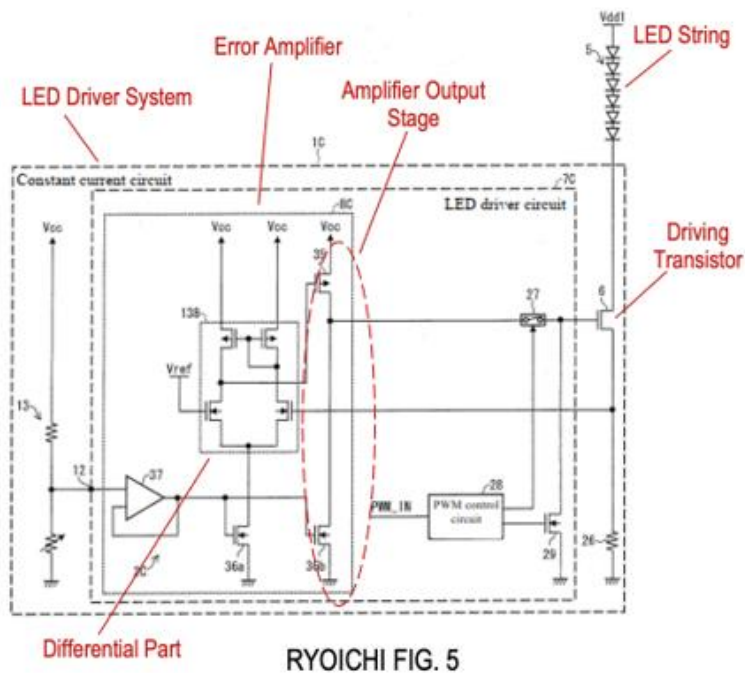
Ryoichi, entitled “Light-Emitting Diode Lighting Actuation Circuitry” was published on August 23, 2012, and is therefore prior art under 35 U.S.C. § 102(a)(1).

References to Ex1006 in this document refer to the certified English translation included as part of the exhibit. Ryoichi figures shown are translated from the translation for readability.

Ryoichi is directed to a regulated LED driving circuit that supplies driving current to LEDs through a driving transistor. Ex1006, ¶ [0017]. The integrated circuit is

characterized by supplying the driving transistor with driving signals whose rise time and fall time are controllable, thus making it possible to reduce a differential velocity (dv/dt) of the driving signals by controlling rise and fall times of the driving signals to be longer [slew rate control]. Ex1006, ¶ [0017].

Ryoichi, in Fig. 5, discloses, at a transistor level, an error amplifier and amplifier output stage for controlling a driving transistor in a current source. Ex1006, Fig. 5.

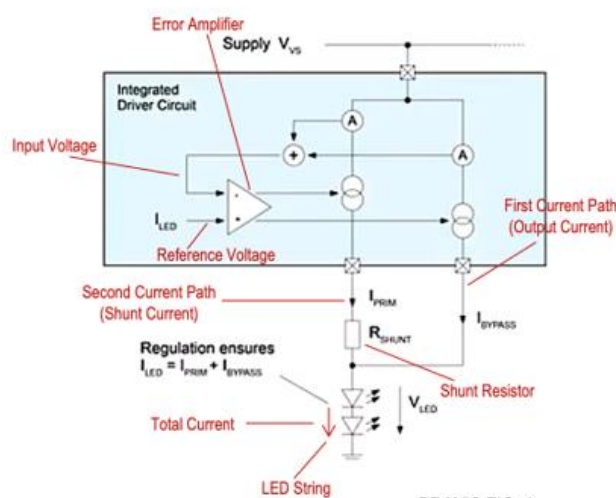


Ryoichi describes multiple approaches to controlling a slew rate of the driving signal controlling the driver transistor 6 including adjusting bias currents ¶¶ [0083]-[0085], switching in and out of transistor pairs in the amplifier output stage [parallel offset currents] [0089]-[0092], and use of a capacitor [104].

C. Article by Sudhaus, published in the October 2016 Edition of Elektronik Praxis entitled “Die Verlustleistung in linearen Regelsystemen günstig verteilen” – English translation (Praxis) (Ex1008)

The Elektronik Praxis Article (Praxis), by Sudhaus, was published in the October 2016 edition of Elektronik Praxis and is prior art under 35 U.S.C. § 102(a)(1).

Praxis discloses a system to deliver a controlled total current to an LED load. Ex1008, page 1:1-2. Praxis includes distributing total current delivered to the LED load over two outputs, including one in series with an external resistor. Ex1008, page 3:5-16.



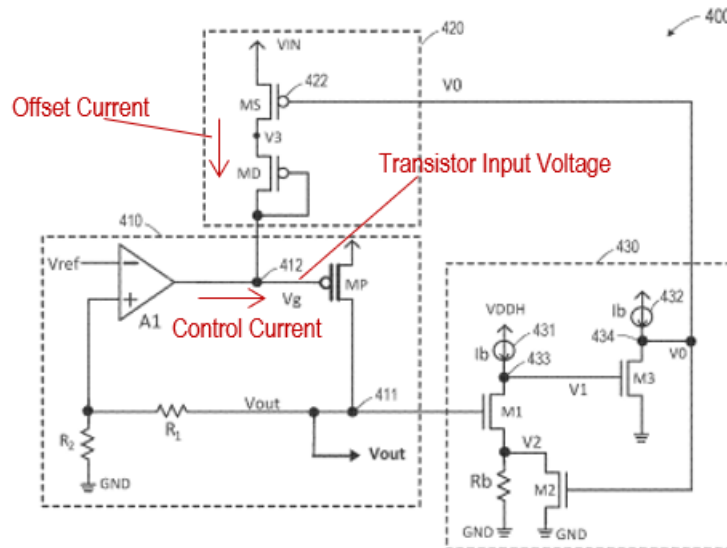
PRAXIS FIG. 1

D. U.S. 11,599,132 B2 to Wu et al. (“Wu”) (Ex. 1009)

Wu, titled “Method and Apparatus for Reducing Power-Up Overstress of Capacitor-less Regulating Circuits,” was filed on February 26, 2021, and issued on March 7, 2023, and is therefore prior art under 35 U.S.C. § 102(a)(2).

Wu is directed to a regulator circuit including an error amplifier that controls an

output transistor and a slew rate control circuit coupled to a gate of the output transistor.

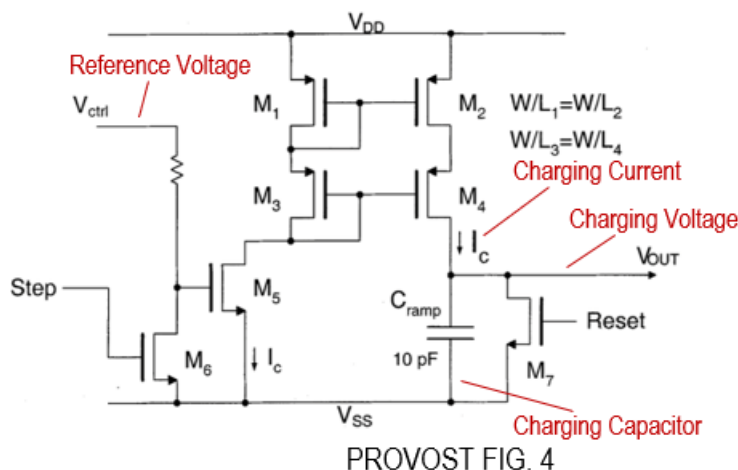


WU FIG. 4

E. Article published in IEEE Journal of Solid-State Circuits – March 2003 entitled *On-chip ramp generators for mixed-signal BIST and ADS self-test* by Provost (Provost) (Ex1010)

The Provost Article published in IEEE Journal of Solid-State Circuits – March 2003 entitled *On-chip ramp generators for mixed-signal BIST and ADS self-test* by Provost published in Vol. 38, No. 2 February 2003 and therefore is prior art under 35 U.S.C. § 102(a)(1).

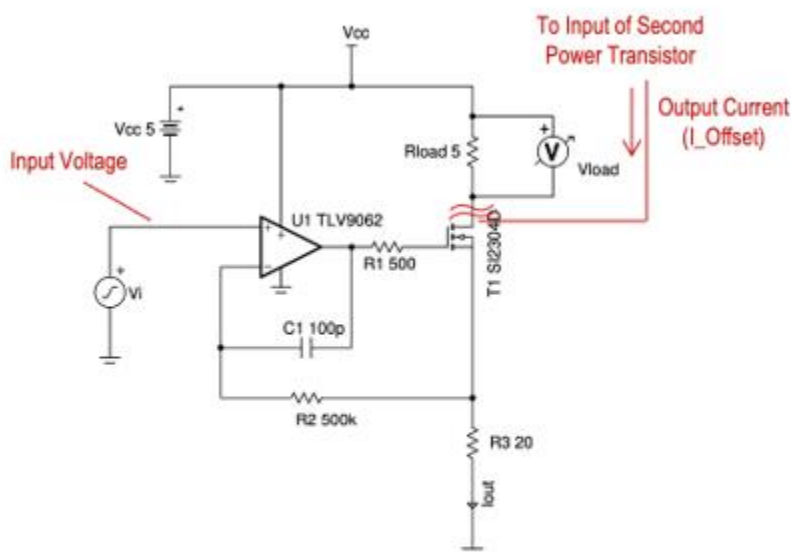
Provost discloses an on-chip ramp generator Ex1010, Fig. 4.



In the on-chip ramp driver of Provost, Fig. 4, transistor M5 is the current driver, M1-M4 form a cascode current mirror that delivers a current I_c (charging current) to a capacitor C_{ramp} (charging capacitor) to develop a voltage V_{out} (charging voltage).

F. White paper by Texas Instruments entitled *Voltage-to-current (V-I) converter circuit with MOSFET* – document number SBOA327A – December 2019 – Revised August 2021 (TI Paper) (Ex1011)

TI Paper, entitled *Voltage-to-current (V-I) converter circuit with MOSFET* is dated December 2019 – Revised August 2021, and is therefore prior art under 35 U.S.C. § 102(a)(1).



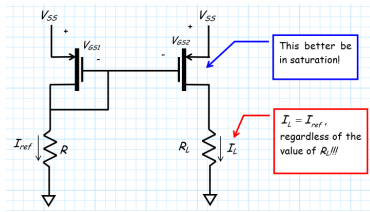
TI PAPER FIG. 1

TI Paper discloses a voltage-to-current converter (V-I converter) in Fig. 1. Ex1011, Fig. 1. The TI Paper V-I converter can be used to convert a charging voltage (applied to V_i) to generate an offset current. Ex1011, Fig. 1.

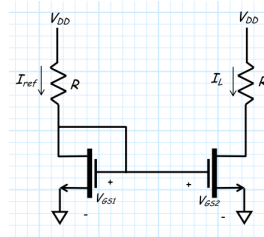
G. White paper entitled “*The MOSFET Current Mirror*” by the University of Kansas, dated April 25, 2011 (UK Paper) (EX1012)

UK Paper, entitled *The MOSFET Current Mirror*, published by the University of Kansas, is dated April 25, 2011, and is therefore prior art under 35 U.S.C. § 102(a)(1).

UK Paper discloses NMOS and PMOS current mirrors. Ex1012, Figures on page 2 and page 6.



PMOS Current Mirror
Fig. page 6

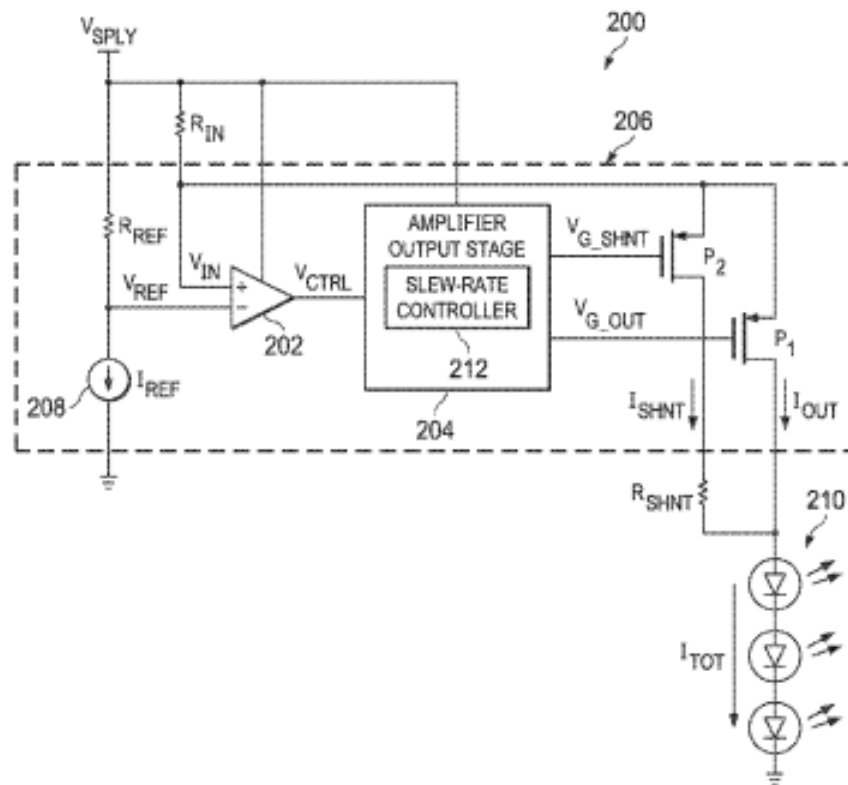


NMOS Current Mirror
Fig. page 2

VII. The '432 Patent.

A. Generally

The '432 Patent relates generally to electronic regulator circuits, and more particularly to an LED driver system with slew-rate control. Ex1001 at Fig. 1, 2:16-18. Referencing Fig. 2, the '432 LED driver system includes an LED string driven by a first current path that includes a power transistor that drives the LED directly and a second current path that drives the LED string with a power transistor connected in series with a shunt resistor.



Ex1001, Figure 2

The '432 driver system includes a control circuit comprising well known components: an error amplifier 202, an amplifier output stage 204 including a slew-rate controller 212 that controls the current through the first and second current paths. Purportedly, the current through the two current paths is controlled such that: a) total output current through the two current paths remains approximately constant over a range of supply voltages, and b) such that the portion of the total output current through the second path including the shunt resistor increases as the supply voltage increases. In this manner, a portion of power that is dissipated as heat by the driver system purportedly will be dissipated by the shunt resistor, purportedly protecting the power transistors from overheating.

To prevent overshoot of the total current in a phase when the second current path including the shunt resistor begins to conduct (due to increasing supply voltage), a slew-rate is implemented for the second current path that purportedly slows down the ramp up of the current through this second current path.

According to the Notice of Allowance for the '432 Patent, the alleged novelty of Claim 1 of the '432 Patent was:

“... a light-emitting diode (LED) driver system comprising: an error amplifier configured to compare an input voltage with a reference voltage to generate a control voltage; and an amplifier output stage configured to control an output current through a first current path and a shunt current through a second current path based on the control voltage, the amplifier output stage comprising a slew-rate controller configured to control a slew-rate of the shunt current, the shunt current provided through a shunt resistor in the second current path and added to the output current to provide a total current through an LED string.”

Ex1002, Notice of Allowance, mailed on January 20, 2023, Examiner's Statement of Reasons for Allowance, page 2.

B. Prosecution History

Patent application 17/537,694 was filed on November 30, 2021, by Texas Instruments Incorporated (the Applicant). The 17/537,694 application included 20 Claims of which Claims 1, 11, and 16 were independent. No Information Disclosure

Statement (IDS) was filed by the Applicant at the time of filing, nor at any time during the prosecution of the patent application.

A notice that the application did not include an inventor oath or declaration of inventorship was mailed on December 10, 2021. Subsequently, on February 10, 2023, declarations of inventorship were filed for the two inventors Xianghao Meng and Shangquan Liang.

The United States Patent and Trademark Office (USPTO) issued a Notice of Allowance for all 20 Claims on January 20, 2023.

The '432 Patent issued on May 16, 2023, and published June 2, 2023.

VIII. CLAIM CONSTRUCTION UNDER 37 C.F.R. § 42.204(B)(3)

A. Legal Overview

Claim terms in *inter partes* review proceedings are construed to have “the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention.”² Petitioner applies the plain and ordinary meaning of the petitioned Claims to the asserted prior art references in support of grounds 1-5³, which

² Petitioner reserves the right to present different constructions and/or challenge the patentability of any claim under 35 U.S.C. § 112 in another forum where a different claim construction standard applies. Thus, the proposed constructions do not constitute an admission that the claims are valid under 35 U.S.C. § 112.

³ See *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc)

involve terms that are readily understood by a POSITA upon review of the specification and file history. Petitioner proposes Claim term constructions according to their plain and ordinary meaning to a POSITA in view of the ‘432 Patent’s specification. Accordingly, the plain and ordinary meaning of:

1. **“amplifier output stage”** means an electrical circuit that receives at least one input and outputs a signal based on the at least one input.

2. **“control voltage”** means an electrical signal used as an input to an electrical device that can influence an operation of the electrical device.

3. **“current path”** is a means for conveying electrical current along a controlled pathway.

4. **“error amplifier”** means an electrical circuit that detects a difference between two electrical input signals and outputs a signal based on the difference.

5. **“reference voltage”** means a voltage representing a desired level of an electrical parameter in a circuit.

6. **“slew rate”** means a rate of change of an electrical signal over time.

7. **“slew-rate controller”** means an electrical circuit that controls a rate of change of an electrical signal over time.

IX. THE ASSERTED PRIOR ART REFERENCES ARE ANALOGOUS ART

A POSITA would understand the asserted prior art references are analogous to the ‘432 Patent and are combinable in the ways set out below.

A. A POSITA's Level of ordinary skill in the art.

Based on the disclosure of the '432 Patent, a person having ordinary skill in the art ("POSITA") at the relevant time, would have had at least a bachelor's degree in electrical engineering, or equivalent experience of at least two years working in the field of the design electrical driver systems for Light Emitting Diodes (LEDs).

B. Sudhaus, Praxis, Ryoichi, Wu, Provost, TI Paper and UK Paper Are Analogous Art

To be considered proper prior art in an obviousness analysis, a reference must be analogous to the claimed invention. A reference is analogous if: (1) it is from the same field of endeavor as the claimed invention (even if it addresses a different problem); or (2) it is reasonably pertinent to the problem faced by the inventor (even if it is not in the same field of endeavor). MPEP § 2141.01(a) I.

Here, Sudhaus, Praxis, Ryoichi, and Wu are in the same field of endeavor as the '432 Patent; namely, the field of providing a regulated power supply to an electrical load. Provost, TI Paper, and UK Paper are in the same field of endeavor in as much as they disclose subcircuits used in the field of providing a regulated power supply to an electrical load and are reasonably pertinent to the problem faced by the inventor.

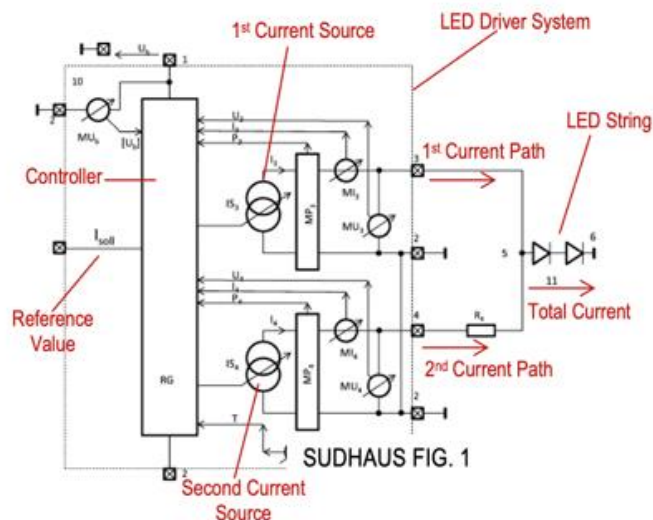
A POSITA would have recognized that Sudhaus, Praxis, Ryoichi, Wu, Provost, TI Paper, and UK Paper disclose or could have been modified based on well-known principles to provide each limitation of the petitioned Claims as set out below. Multiple *KSR* obviousness rationales support the modifications set out in Sections IX-

X. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 415-421 (2007); MPEP § 2141. A POSITA would have been motivated to combine Sudhaus and Ryoichi as Ryoichi discloses transistor level detail of a portion of a controller, such as the Sudhaus controller, including current control (the error amplifier and amplifier output stage) and gradual transitioning between current outputs (amplifier output stage and slew rate control). POSITA would have been motivated to combine Sudhaus and Praxis as Praxis discloses an analog approach to the design need of controlling a sum of two currents. Each of Wu, and the combination of Provost with the TI Paper and the UK Paper, provide alternatives for slew rate control and a POSITA would be motivated to combine any of these references to accommodate a particular design need.

C. GROUND 1: CLAIMS 1-3, 6, 10-11, AND 16-17 ARE UNPATENTABLE UNDER 35 U.S.C. § 103(a) AS BEING OBVIOUS OVER SUDHAUS

Systems of Claims 1-3, 6, 10-11, 16-17 are obvious over Sudhaus to a POSITA at the time of filing.

Sudhaus Fig. 1 discloses Controller RG operative to control a total current delivered to an LED load through two current paths, based on a desired value for I_{soll} . Ex1005, 4:46-50, Fig. 1. Sudhaus' two current paths include: first current path with current source IS_3; and second current path with current source IS_4 in series with external resistor R_4.



Sudhaus teaches managing power dissipation, gradually shifting a portion of a total current from a first current path to a second current path, as supply voltage increases. Ex1005, 5:40-46, 6:18-26.

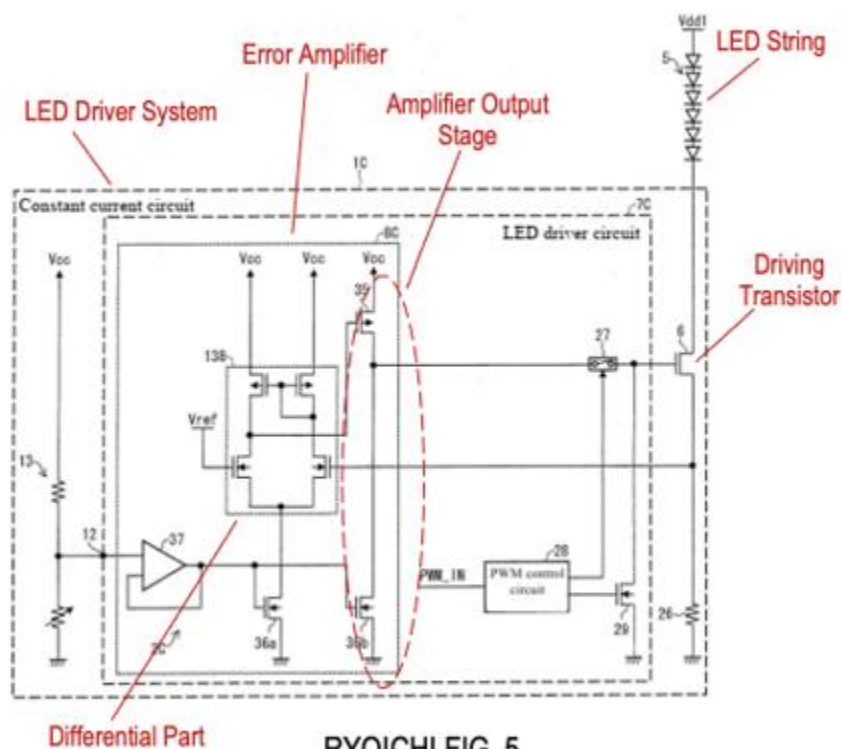
POSITA would find it obvious, based on Sudhaus, to supply an LED load through two current paths, one current path including an external resistor, while controlling a sum of currents delivered to the load. Sudhaus describes increasing the portion of current through the second current path including the external resistor as supply voltage increases, and *gradually* increasing current through the second current path (control the slew rate) with increasing supply voltage.

D. GROUND 2: CLAIMS 1-4, 6-7, 10-12 AND 15-18 ARE UNPATENTABLE UNDER 35 U.S.C. § 103(a) AS BEING OBVIOUS OVER SUDHAUS IN VIEW OF RYOICHI.

The '432 Patent claimed LED driver system is obvious over Sudhaus, in view of Ryoichi.

Sudhaus teaches LED driver systems that deliver controlled total current to an LED load via two current paths, a first current path including a current source, and a second current path including a current source and external shunt resistor. Sudhaus further teaches gradually shifting a portion of total current from the first current path to the second current path with increasing supply voltage.

Ryoichi describes an LED driving system with a driving transistor (as part of a current source) that controls driving current for an LED load. Ryoichi's driving system includes control of rise and fall times (slew rate control) of a control signal controlling the driving transistor. Ex1006, [0017].

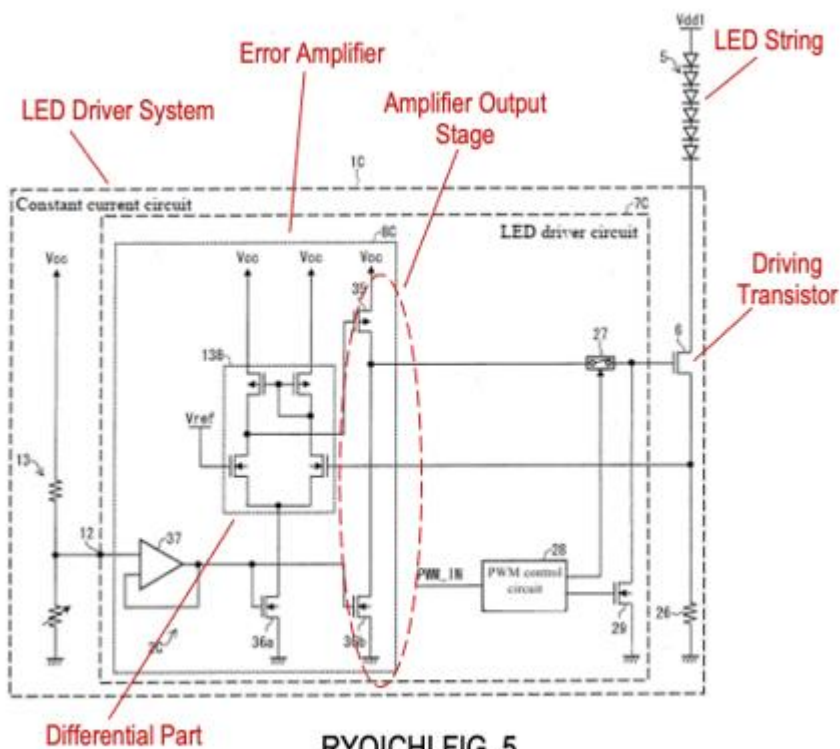


RYOICHI FIG. 5

Ryoichi's Fig. 5 illustrates LED driver circuit 10 with operational amplifier 8C (error amplifier) that compares reference voltage V_{REF} with voltage corresponding to LED load current, Ex1006, [0083]. Operational amplifier 8C includes differential part 138, and an amplifier output stage comprising transistors 35 and 36b. Differential part 138 generates control voltage to control transistors 35 in the amplifier output stage. Ex1006, [0083]. Ryoichi's amplifier output stage controls power transistor 6 that delivers current to LED string 5. Ex1006, [0083].

Ryoichi discloses multiple approaches to controlling slew rate of a driving signal controlling a driving transistor. Three Ryoichi approaches are discussed herein.

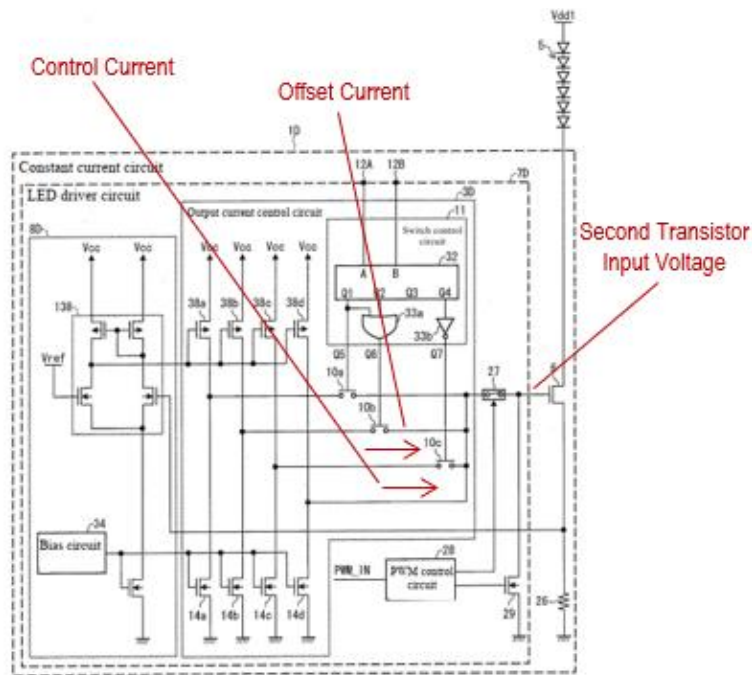
First, Ryoichi discloses controlling slew rate of a driving signal controlling a driving transistor by adjusting bias current provided to an error amplifier and amplifier output stage. Ex1006, Fig. 5.



Ryoichi's LED driver circuit includes operational amplifier 8C (error amplifier) that compares reference voltage V_{REF} with a voltage corresponding to a current to the LED load 5 to control a current delivered to LED load 5. Ex1006, [0083]. Drive capability of operational amplifier 8C is adjustable via changing voltage applied to input 12 with the resistive divider 13, to change a bias currents delivered respectively to the differential part 138 by transistor 36a, and to an amplifier output stage via transistor

36b, effectively adjusting rise and fall time of a signal driving transistor 6. Ex1006, [0085].

Secondly, Ryoichi illustrates controlling rise and fall time of a control signal controlling driving transistor 6 by switching pairs of transistors into and out of an amplifier output stage. E1006, Fig. 6.

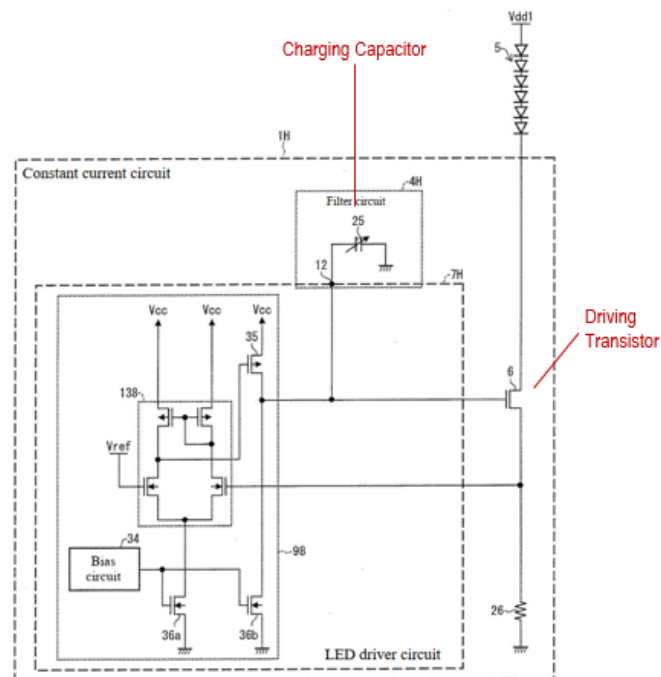


RYOICHI FIG. 6

Ryoichi teaches replacing the amplifier output stage of Fig. 5 (transistors 35 and 36b), with transistors 38a, 38b, 38c, 38d (corresponding to Fig. 5 transistor 35) combined with transistors 14a, 14b, 14c, 14d (corresponding to Fig. 5 transistor 36b). Ex1006, [0087]-[0088]. Drive capability of Ryoichi's amplifier output stage is adjustable by selecting how many of transistors 38a, 38b, 38c, 38d and corresponding transistors 14a, 14b, 14c, 14d are coupled via switches 10a, 10b, 10c to drive Ryoichi's

driving transistor 6, thereby adjusting rise time and fall time of the driving signal applied to driving transistor 6. Ex1006, [0089]-[0092].

Ryoichi's third example of slew-rate control uses variable capacitor 25 (charging capacitor) for adjusting slew rate of a driving signal applied to a driving transistor. Ex1006, [0104], Fig. 10.



RYOICHI FIG. 10

Ryoichi provides transistor level detail of an error amplifier and an amplifier output stage, e.g. Ex1006, [0083], and slew rate controller e.g. Ex1006, Fig. 5, [0085], [0089]-[0092], [0104]. Ryoichi further discloses functional limitations of controlling slew rate and providing regulated current to an LED load. Ex1006, [0083]-[0085].

POSITA would find it obvious to include Ryoichi's error amplifier (including the amplifier output stage) in the Sudhaus controller. POSITA would further find it obvious

to include Ryoichi's slew rate control to Sudhaus' second current path to accomplish gradual transition from the first current path to the second current path.

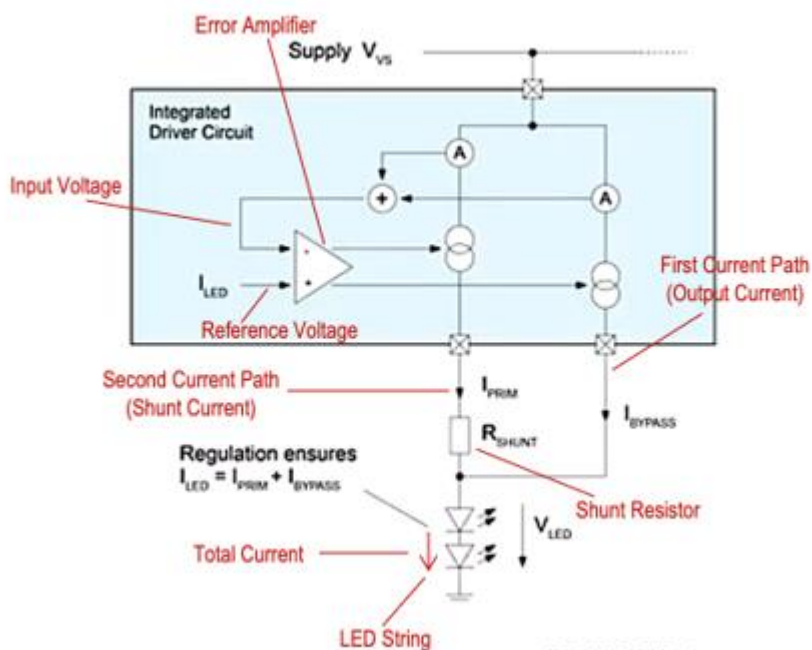
E. GROUND 3: CLAIMS 1-4, 6-7, 10-12 AND 15-18 ARE UNPATENTABLE UNDER 35 U.S.C. § 103(a) AS BEING OBVIOUS OVER SUDHAUS IN VIEW OF RYOICHI IN VIEW OF PRAXIS

Claims of the '432 Patent are obvious over Sudhaus in view of Ryoichi, in further view of Praxis.

Sudhaus discloses an LED driver system that delivers a total controlled current to an LED load via two current paths, a first current path including a current source, and a second current path including a current source and [IC] external shunt resistor. Sudhaus further teaches gradually transferring current from a first current path to a second current path.

Praxis discloses controlled delivery of total current to an LED load. Ex1008, page 1:1-2, combinable with Sudhaus' controlled current to an LED load via two current paths, and Ryoichi's multiple variations of slew rate control and transistor level realizations of error amplifiers, amplifier output stages and current sources.

Praxis describes distributing a total current to an LED load over two outputs, one output in series with an external resistor. Ex1008, p.3:5-17.



Analogous to the '432 Patent, Praxis describes error amplifiers with amplifier output stages having two outputs independently controlling two driver outputs. Ex1008, 3:5-16. Praxis' primary driver output together with resistor R_SHUNT provide a first current path providing current I_PRIM to an LED load. Praxis bypass driver provides a second current path providing current I_BYPASS. EX1008, p. 3:13 - 4:7, Fig. 2.

Praxis provides total current to an LED load through two current paths (primary and bypass). Ex1008, e.g., page 3;15-17.

Praxis' error amplifier includes two outputs to control two current sources. A POSITA would find it obvious to include Praxis' error amplifier with an output stage have two outputs, to control two current sources in Sudhaus' LED driver system.

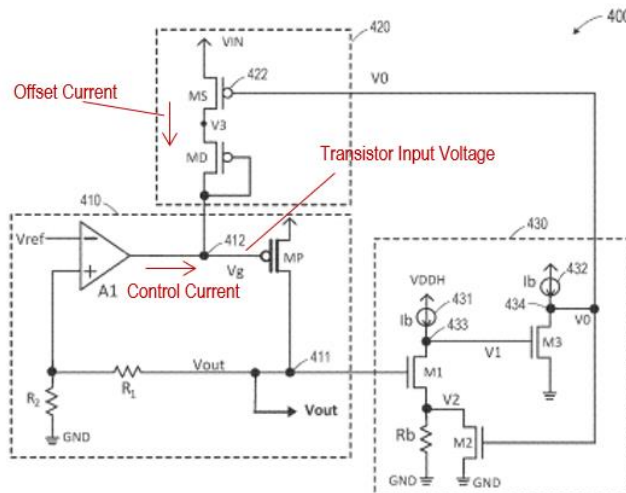
Sudhaus and Praxis, make it obvious for POSITA to include Ryoichi's

differential part amplifier output stage and slew rate control in the error amplifier of Praxis, to control a transition of a current to Sudhaus, second current path.

F. GROUND 4: CLAIMS 1-4, 6-7, 10-12, 15-18 ARE UNPATENTABLE UNDER 35 U.S.C. § 103(a) AS BEING OBVIOUS OVER SUDHAUS IN VIEW RYOICHI IN VIEW OF PRAXIS IN VIEW OF WU

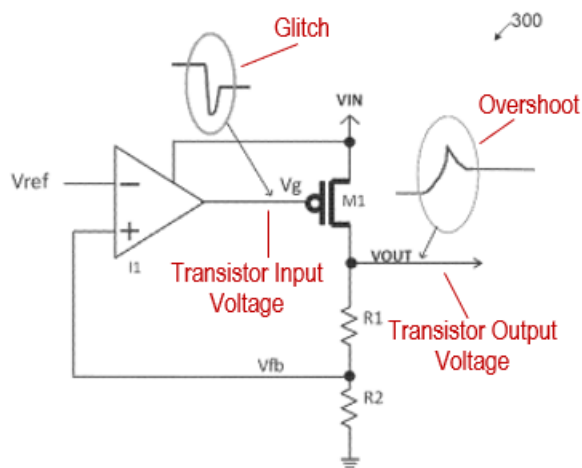
Wu is presented as an alternative to the slew rate control of Sudhaus and/or Ryoichi for controlling the slew rate of an input to a power transistor in a regulated system. Wu teaches a regulator circuit including an error amplifier that controls an output transistor and a slew rate control circuit, coupled to a gate of an output transistor.

In addition to Sudhaus, Ryoichi and Praxis disclosing LED drivers supplying current to an LED load via two current paths, Wu describes linear regulator circuit 400 including linear regulator 410 with error amplifier A1. Error amplifier A1's output is connected to control the gate of output transistor MP. Error amplifier A1 is configured to regulate output voltage V_OUT at output transistor MP's output, based on feedback of resistor pair R1, R2. Ex1009, 6:14-19. Linear regulator circuit 400 includes slew-rate control circuit 420 coupled to gate node 412 of output transistor M1. Slew-rate control circuit 420 is configured to control voltage rise of gate node 412 during power-up to reduce output voltage overshoot. Ex1009, 6:24-28.



WU FIG. 4

Figure 3 of Wu illustrates overshoot that Wu's slew-rate circuit addresses.



WU FIG. 3

During power-up, a glitch on M1's gate can cause full rail voltage to appear on output VOUT. Ex1009, 5:47-48. Wu's slew rate controller includes an output voltage level detection 430 that turns slew rate control off when output voltage VOUT reaches a preset level. Ex1009, 7:6-14.

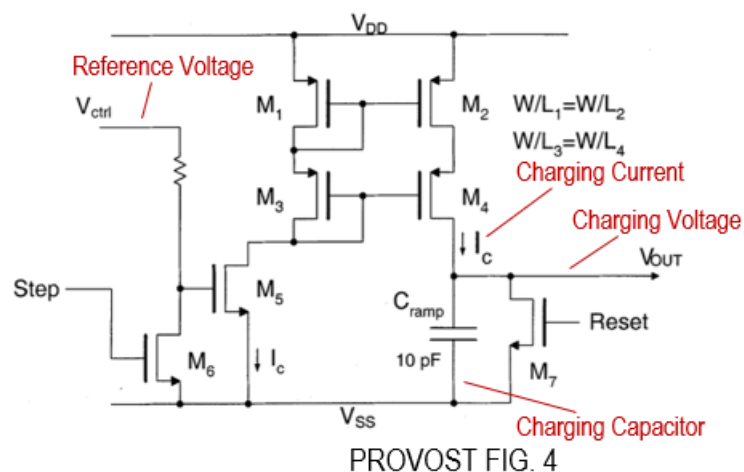
At the time of the invention, POSITA would find it obvious to combine Wu with Sudhaus, to implement gradual transition of current from a first current path to a second current path.

G. GROUND 5: CLAIMS 1-20 ARE UNPATENTABLE UNDER 35 U.S.C. § 103(a) AS BEING OBVIOUS OVER SUDHAUS IN VIEW OF RYOICHI IN VIEW OF PRAXIS IN VIEW OF PROVOST IN VIEW OF TI PAPER IN VIEW OF UK PAPER.

As described in reference to Ground 3, Sudhaus, Ryoichi and Praxis disclose supplying current to an LED load via two current paths. Slew rate control gradually transitions a portion of a total current from a first current path to a second current path.

Combinations of Provost, the TI Paper and the UK Paper are presented as alternative methods of slew rate control.

Provost discloses an on-chip ramp generator. Ex1010, Fig. 4.

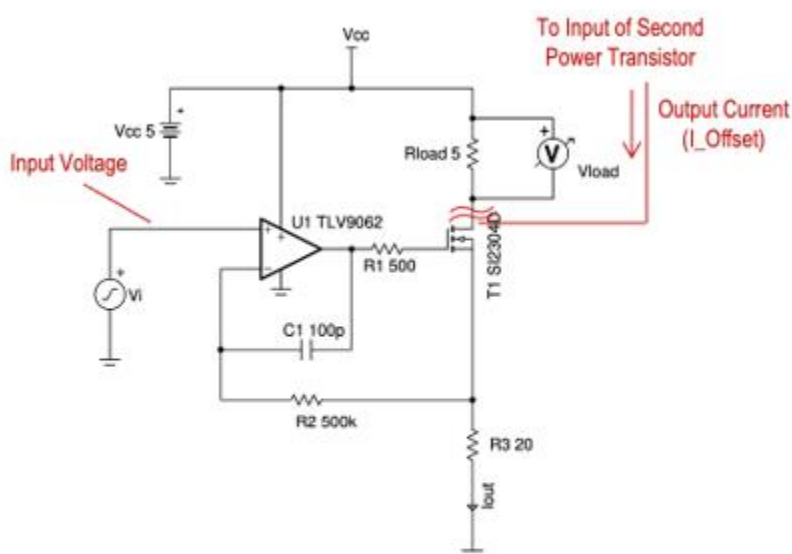


Provost includes current driver transistor M5. M1-M4 form a cascode current

mirror delivering current I_c (charging current) to capacitor C_{ramp} (charging capacitor). M6 is for stopping a current source when Step is at logic 1. M7 is used to reset C_{ramp} . Ex1010, Section II (C), page 265-266. When turned on, charging current charges the charging capacitor to generate a ramp (charging voltage). Ex1010, Section II (C), page 265-266.

A POSITA would find it obvious to combine Provost's ramp generator with one or more of Sudhaus, Ryoichi and Praxis to generate a charging current, and to use a charging capacitor with a charging current to generate charging voltage.

TI Paper's discloses a voltage-to-current converter (V-I converter). Ex1011 Fig. 1.



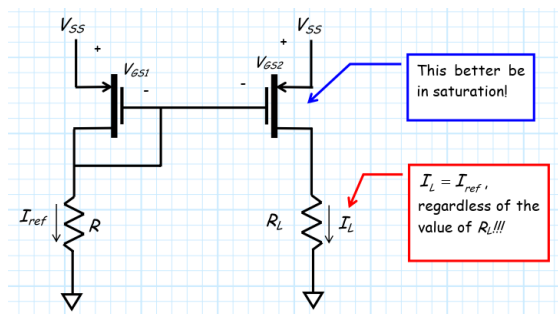
TI PAPER FIG. 1

The voltage-to-current converter converts input voltage to output current. TI Paper's Fig. 1, describes output current as:

$$I_o = \frac{V_i}{R_3}$$

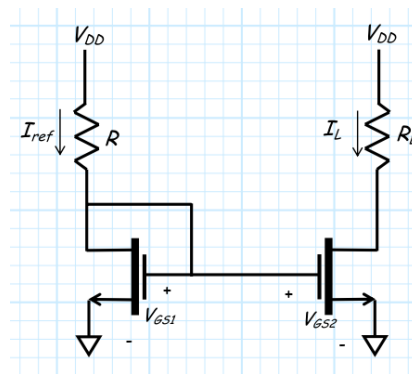
Ex1011, page 2:1-2. TI Paper's V-I converter converts charging voltage (applied to V_i) to generate offset current (output current delivered to load R_{load_5}). Ex1011, Fig. 1. It would have been obvious to POSITA to use the basic circuit building blocks of Provost's voltage-to-current converter to convert ramp voltage (charging voltage) to offset current to control slew rate of an input signal applied to a driving transistor.

UK Paper is included for completeness, disclosing NMOS and PMOS current mirrors. Ex1012, Figs. p. 2, 6.



PMOS Current Mirror

P. 6



NMOS Current Mirror

P. 2

With transistors in pairs dimensioned the same, I_{ref} equals I_L for both the NMOS Current Mirror and the PMOS Current Mirror. Ex1012, p. 3.

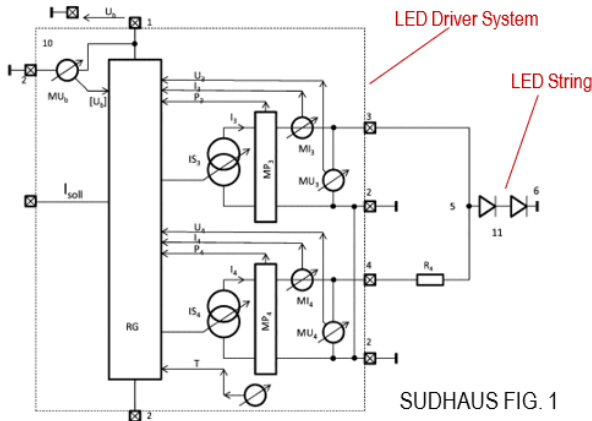
PMOS and NMOS current mirrors are common, well known building blocks in MOSFET circuits. Although current I_{offset} generated by the voltage-to-current converter of TI paper may be applied directly to an input of a driving transistor to control a slew rate, Claims 5, 8, 13 and 19 of the '432 Patent include current mirrors to apply current I_{offset} to a driving transistor input. It would be obvious for POSITA to use current mirrors to adjust a current magnitude of current I_{offset} (by varying transistor sizes in the current mirrors), or to reconcile output voltage levels of the voltage-to-current converter to the voltage level of the input to the driving transistor.

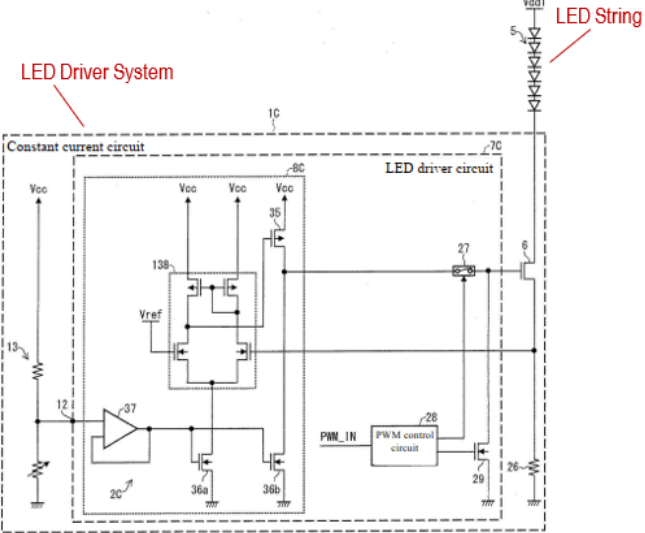
X. THE PETITIONED CLAIMS ARE UNPATENTABLE UNDER GROUNDS 1-5

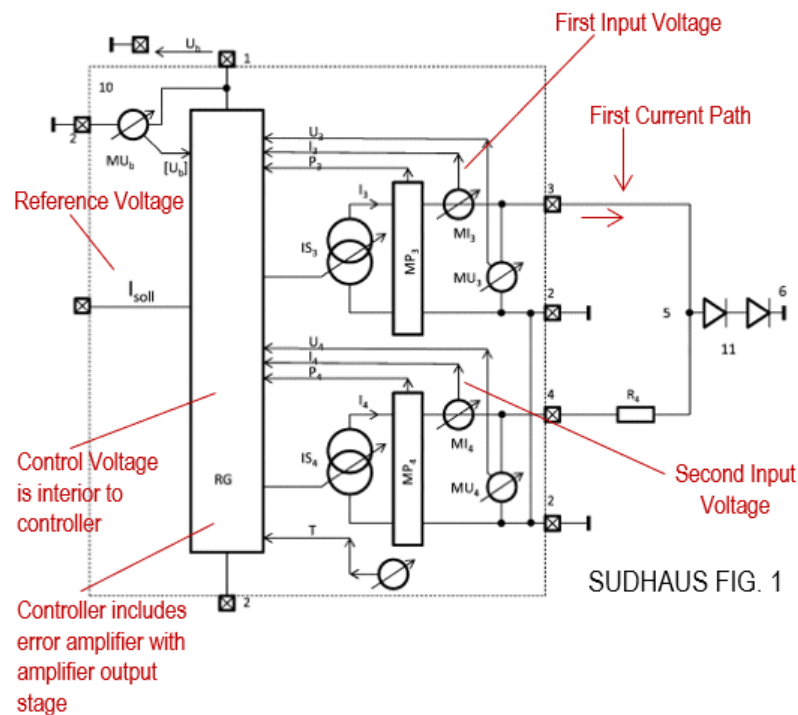
Grounds 1-5 render obvious each of the limitations of the petitioned claims. Sudhaus discloses or renders obvious LED driver systems including controlling total current to LED loads (error amplifier and amplifier output stage), two current paths for supplying the total current with one current path including an external shunt resistor, and gradually transitioning from a first current path to a second current path with increasing supply voltage (slew rate control) (Claims 1-3, 6, 10-11, 16-17). To the extent the Board finds that Sudhaus does not disclose an error amplifier and amplifier output stage, Praxis discloses an error amplifier for controlling two current paths, and Ryoichi discloses a transistor level realization of an error amplifier and amplifier output stage for controlling a current to an LED load. (Claims 1-3, 6, 10-11, 16-17). To the extent the Board finds that Sudhaus does not disclose slew rate control, Ryoichi discloses

multiple variations of slew rate control of which three are presented here, and Wu presents a fourth alternative to slew rate control (Claims 1-4, 6-7, 10-12, 15-18). Further, the combination of Provost, TI Paper and UK Paper discloses a fifth approach to slew rate control (Claims 1-20).

A. Claim 1 is unpatentable under Grounds 1-5

Claim 1	Grounds
[1.pre] A light-emitting diode (LED) driver system comprising:	[Grounds 1–5] Sudhaus discloses apparatus for supplying electrical consumer (load) with electrical energy. Ex1005, 2:25-27, Figure 1. Sudhaus further discloses, the electrical consumer can include LEDs. Ex1005, 4:29-30.  SUDHAUS FIG. 1 Sudhaus Fig.1 [Grounds 2–5] Ryoichi discloses LED driver systems Ex1006 [0082], Fig. 5.

	 RYOICHI FIG. 5
[1.1] an error amplifier configured to compare an input voltage with a reference voltage to generate a control voltage; and an amplifier output stage configured to control an output current through a first current path	[Grounds 1-5] Error amplifiers are electrical circuits that detect a difference between two electrical signals and output a signal based on the difference. See supra, Sect. VIII. A. 4. Phrases such as: “to compare”, “to generate” and “configured to control” are functional limitations. Sudhaus discloses a controller RG that performs the functions of an error amplifier and amplifier output stage. Sudhaus discloses control circuits to control two outputs supplying current to consumer (LED load). Ex1005, 2:32-33. Controller RG is operative to control two currents based on a desired value for I_{soll}. Ex. 1005, 4:46-50, Fig. 1. Sudhaus: “[a] controller RG is operative to control the current sources IS_3 and IS_4 with the aid of these measurement values and optionally with the aid of control instructions received from external sources, here a desired value I_{soll} ...” Ex1005, 4:46-50, Fig. 1.



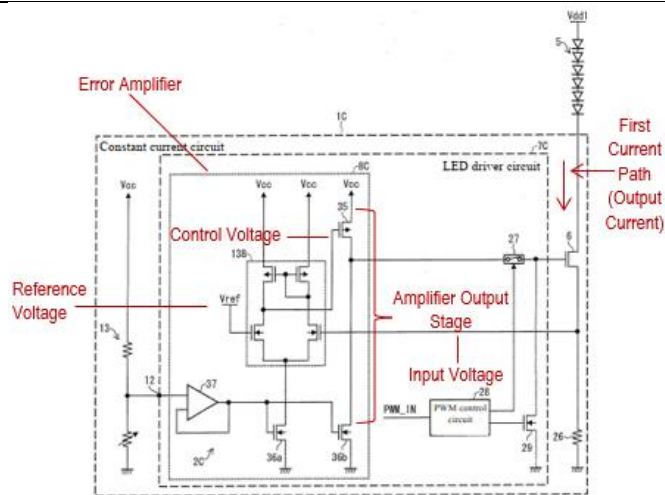
ControllerRG may comprise analog or digital circuits. Ex1005, 8:47-55. ControllerRG has output signals to control currents IS_3, IS_4. Ex1005, 4:25-28, Fig. 1.

First output (labeled 3) from Controller RG controls current source IS_3 and accordingly current through the first current path. (analogous to Claim 1.1 amplifier output stage).

[Grounds 2-5] Additionally (and alternatively) to Sudhaus, Ryoichi discloses transistor level circuits of operational amplifiers including an amplifier output stage, used for controlling current for LEDs.

Ryoichi's operational amplifier controls driving transistor current based on a reference value. Ex1006, [0019]. Ryoichi's operational amplifier includes "[a]n output control circuit, which is disposed between the aforementioned comparator-amplifier circuit and the aforementioned driving transistor so as to control the aforementioned driving signals." *Id.*

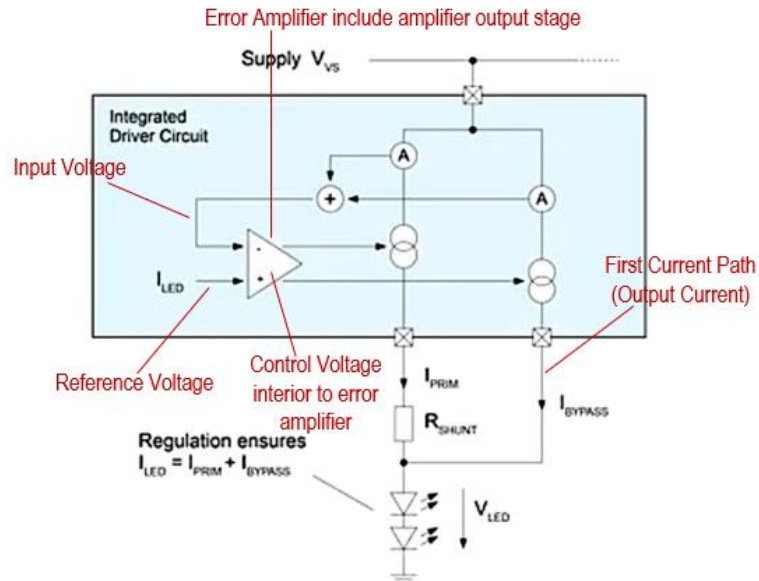
Ryoichi operational amplifier 8C Ex1006 [0083],



RYOICHI FIG. 5

teaches amplifier output stages of transistors 35/36b. Ex1006; [0083]. Transistor 35 is controlled by output of differential part 138 (control voltage); Ryoichi's amplifier output stage (transistors 35/36b) controls first current path (transistor 6/resistor 26), providing current to LED load 5. *Id.*

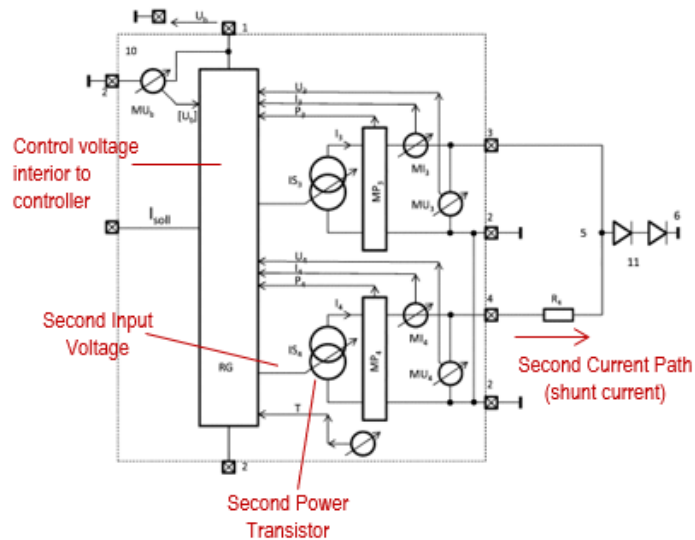
[Grounds 3–5] Additionally (and alternatively) to Sudhaus/Ryoichi, Praxis discloses analog error amplifiers including two outputs to respectively control two current sources. Praxis' error amplifier controls total current from two current sources delivered to an LED load based on a reference value. Ex1008, page 3, Section entitled "Modern linear regulators with a power distribution," lines 7-14; Fig. 1. Praxis' first output controls first current path.



PRAXIS FIG. 1

[1.2] and a shunt current through a second current path based on the control voltage,

[Grounds [1–5] Sudhaus discloses a second output 4, driven by current source IS₄ that supplies shunt current through a second current path based upon control voltage. Ex1005, 4:46-50, Fig. 1.

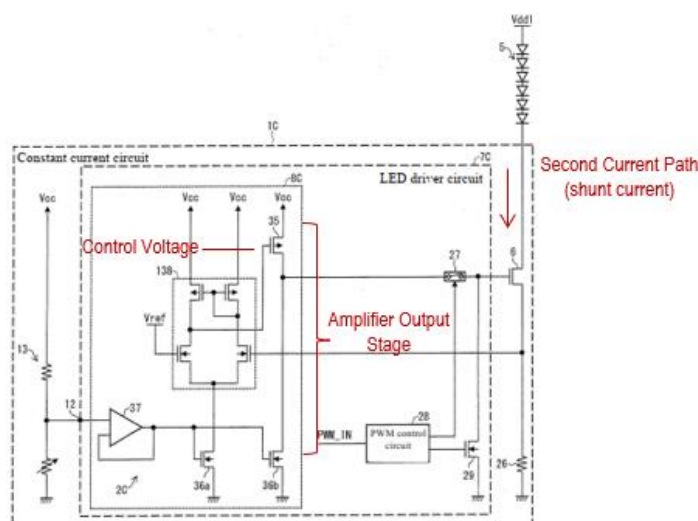


SUDHAUS FIG. 1

Controller RG is operative to control a sum of currents

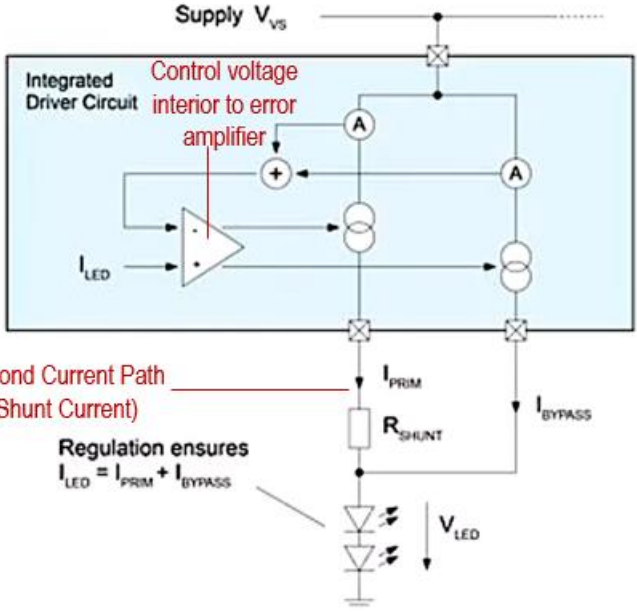
through first and second current paths based upon reference value I_{soll} . Ex1005, 4:46-50, Fig. 1. Sudhaus' control voltage is an internal signal to Controller RG.

[Grounds 2-5] Additionally (and alternatively) to Sudhaus, Ryoichi shows a controller for regulating current through a current path based upon control voltage. Ex1006, Fig. 5, [0083]. Operational amplifier 8C, includes an amplifier output stage including transistors 35 and 36b, amplifier output stage controlling current source (e.g., transistor 6 and resistor 26). Transistor 35 in amplifier output stage is controlled by the output of differential part 138 (the control voltage). Ryoichi's amplifier output stage (transistors 35/36b) controls a current path (e.g., transistor 6/resistor 26), providing current to LED load 5. Ex1006, Fig. 5.

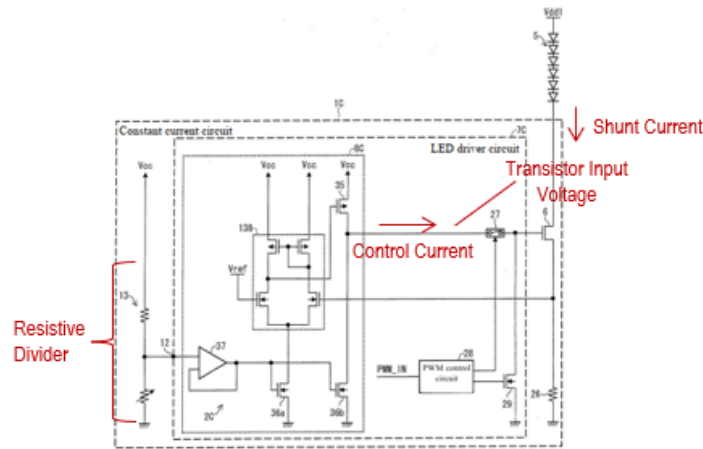


RYOICHI FIG. 5

[Ground 3-5] Additionally (and alternatively) to Sudhaus/Ryoichi, Praxis discloses error amplifiers having two outputs to control two current sources providing current to LED loads. Ex1008, page 3, "Modern linear regulators with a power distribution," (lines 7-14; Fig. 1). The second output controls a shunt current through the second current path. Two stage amplifiers, (see Ryoichi above), are well known. The control voltage is an internal signal that controls Praxis' internal amplifier output stage.

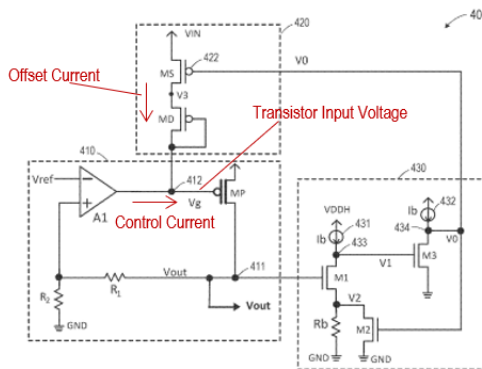
	 PRAXIS FIG. 1
[1.3] the amplifier output stage comprising a slew-rate controller configured to control a slew-rate of a shunt current,	Slew-rate is a rate of change of an electrical signal over time. A slew-rate controller is an electrical circuit that controls a rate of change of an electrical signal over time. Supra, Section VIII. A. 4-5. [Grounds 1-5] Sudhaus discloses slew rate control of the second current output. In Sudhaus, as supply voltage increases, a portion of a total current of two current paths is gradually taken over by the second current path at second connector 4 [the current path including current source IS_4 and external shunt resistor R_4]. Ex. 1005, 5:43-46. Sudhaus further emphasizes this: “Therefore, the second output will only <i>gradually</i> take over a part of the sum current $I_3 + I_4$. This is effected e.g. in that the first output voltage U_3 of control circuit 10 and, therefore, the voltage that decreases [is dropped] across LEDs ... is kept constant.” Ex1005, 6:24-29, emphasis added. [Grounds 2–5] Additionally (and alternatively) Sudhaus, Ryoichi includes slew rate control: e.g. “[t]he aforementioned integrated circuit is characterized by supplying the driving transistor with driving signals whose

rise time and fall times are controllable.” Ex1006, [0017]; Fig. 5, Ryoichi shows changing constant current provided to differential stage 138 via transistor 36a and constant current provided to amplifier output stage via 36b by adjusting control voltage of transistors 36a/36b. Ex1006 [0083]-[0085]. Constant current provided by transistors 35a/36b is adjusted by adjusting voltage at node 12 using resistive divider circuit 13 “thereby changing drive capability of operational amplifier 8C.” Ex1006, [0085].



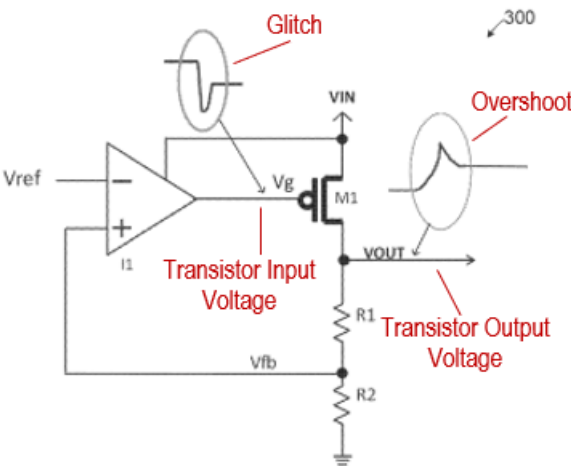
RYOICHI FIG. 5

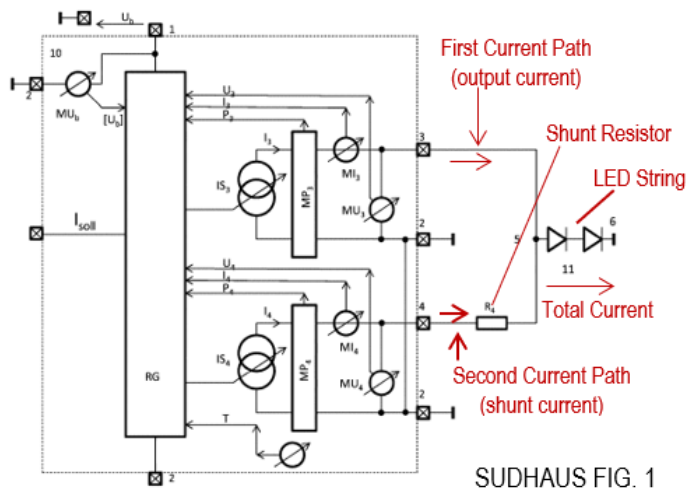
[Ground 4] Additionally (and alternatively), to Sudhaus/Ryoichi/Praxis, Wu includes a slew-rate controller to control an output supplying current to a load. Slew-rate controller 420 controls a voltage rise on the gate of an output transistor MP. Ex1009, 6:24-28.



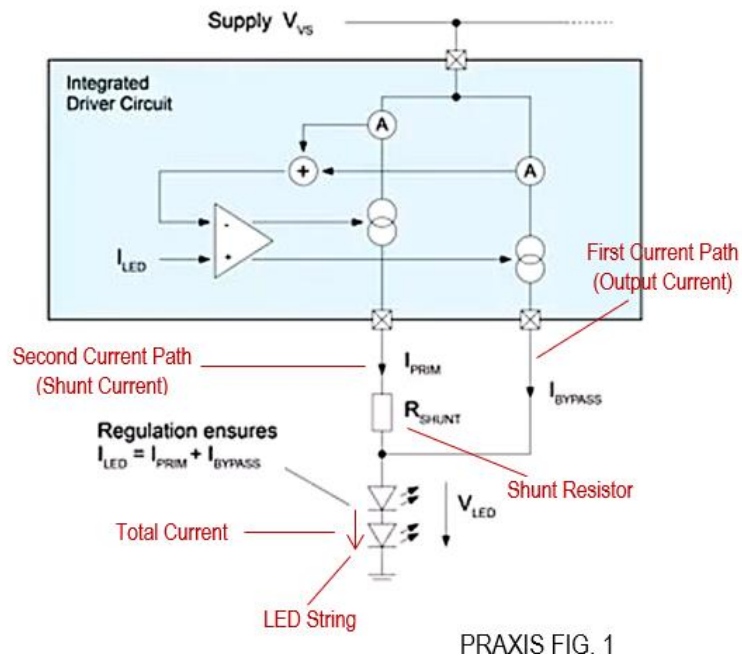
WU FIG. 4

Wu illustrates a glitch that can occur on the gate of an output transistor (M1), and a resulting peak that can occur at output

	V_OUT. Ex1009, 5:47-48.  WU FIG. 3 Wu's slew-rate controller prevents glitches on the output transistor gate and consequently the output peak. Ex1009, 8:33-40. [Ground 5] Alternatively, the combination of Provost, TI Paper and UK Paper provide a slew-rate controller as described in reference to Claim 5, below.
[1.4] the shunt current provided through a shunt resistor in the second current path and added to the output current to provide a total current through an LED string.	[Grounds 1–5] Sudhaus discloses providing output current through a first current path and a shunt current in a second current path including an external resistor. Ex1005, Fig. 1, 4:25-32. Sudhaus' second current path includes current source IS_4 and resistor R_4. Ex1005, 4:30-32. Sudhaus discloses controller RG is operative to control a total of the two output currents based on a desired value I_soll. Ex1005, 4:46-50, Fig. 1. The total current is delivered to LED string 11.



[Grounds 3–5] Additionally (and alternatively) to Sudhaus/Ryoichi, Praxis discloses error amplifiers having two outputs to control two current sources providing current LED loads. Ex1008, page 3, Section titled “Modern linear regulators with a power distribution,” lines 7-14; and Fig. 1. The second output controls the second current path.



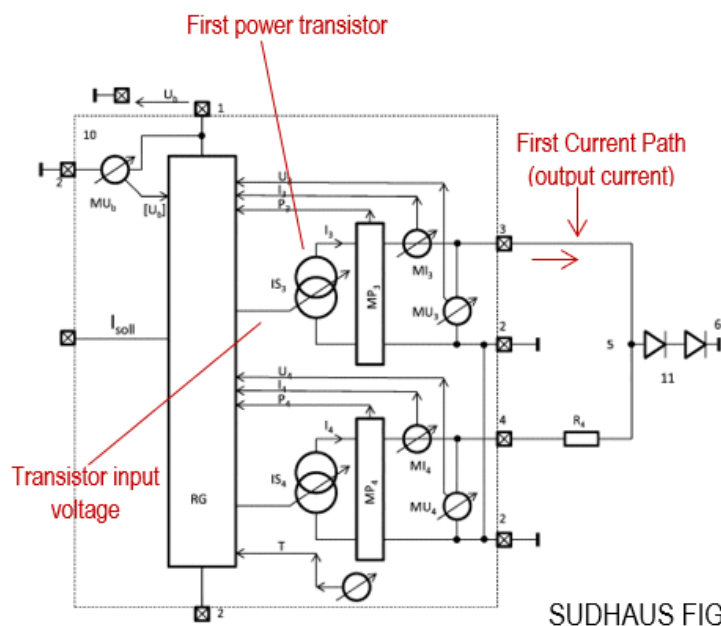
B. Claim 2 (elements [2.1] - [2.2]) is unpatentable under Grounds 1-5

Claim 2

[2.1] The system of claim 1, further comprising: a first power transistor configured to conduct the output current in the first path based on a first transistor input voltage; and

Grounds

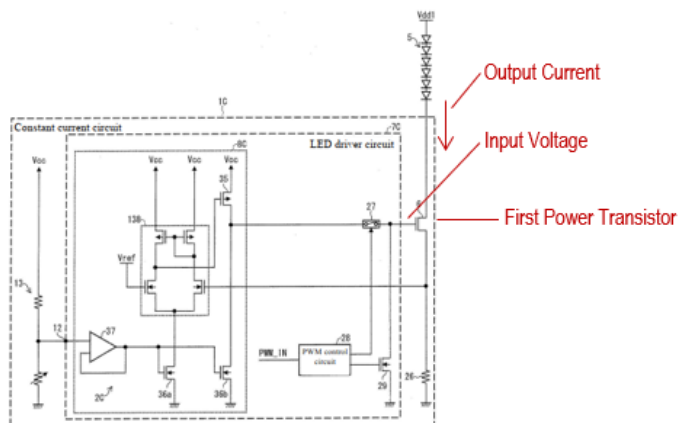
[Grounds 1–5] Sudhaus discloses: a power transistor to conduct output current based upon a first input voltage.



First output (3) driven by current source IS_3 is configured to conduct current in a first current path based on current source IS_3 input voltage (signal from RG controlling IS_3): “[a] controller RG is operative to control the current sources IS_3 and IS_4 with the aid of these measurement values and optionally with the aid of control instructions received from external sources, here a desired value I_{soll} ... Ex1005, 4:46-50, Fig. 1.

Sudhaus' current sources (e.g. IS_3 - IS_4) include "controlling transistor(s)." Ex1005, 1:65-2:14; "controlling transistor" can be understood to be output transistors (power transistors) of a current source: "[t]he disclosure (Sudhaus) is founded on the recognition that, basically, a transistor which is the controlling transistor of a current source, can in the broadest sense be considered as an adjustable resistor. If this transistor has a medium resistance value, a maximum of power will drop across the transistor." Ex1005, 1:65-2:2.

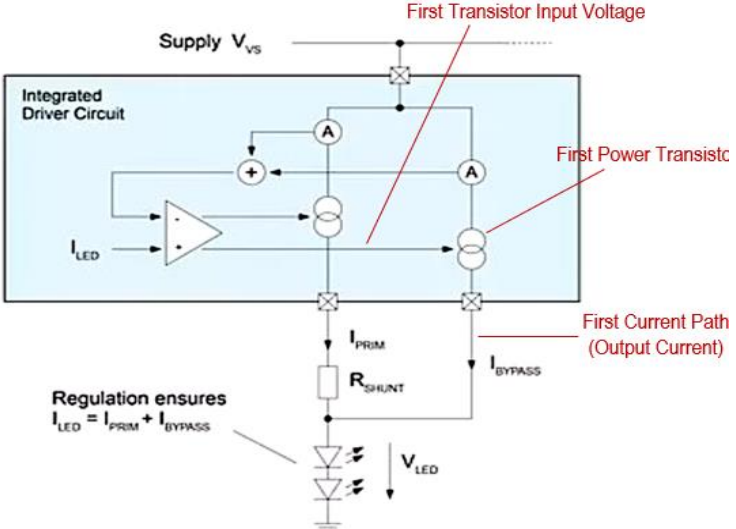
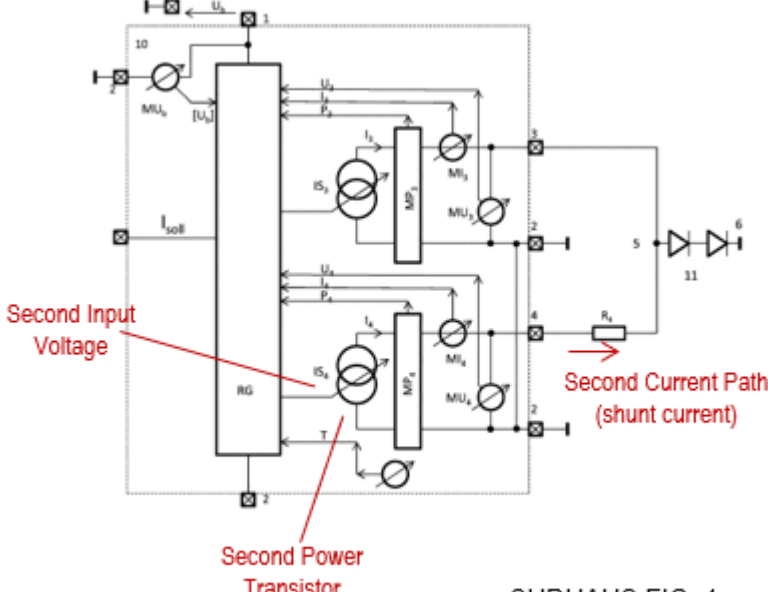
[Grounds 2-5] Additionally (and alternatively) to Sudhaus, Ryoichi discloses driving transistor 6. Ex1006, [0083], Fig. 5.



RYOICHI FIG. 5

Ryoichi Fig. 5 shows: first transistor 6 receives input voltage on gate inputs of transistor 6, input voltage being provided by amplifier output stage (transistors 35/36b). Current through transistor 6 (current in first path) is based on this input voltage. Ex. 1006, [0083], Fig. 5.

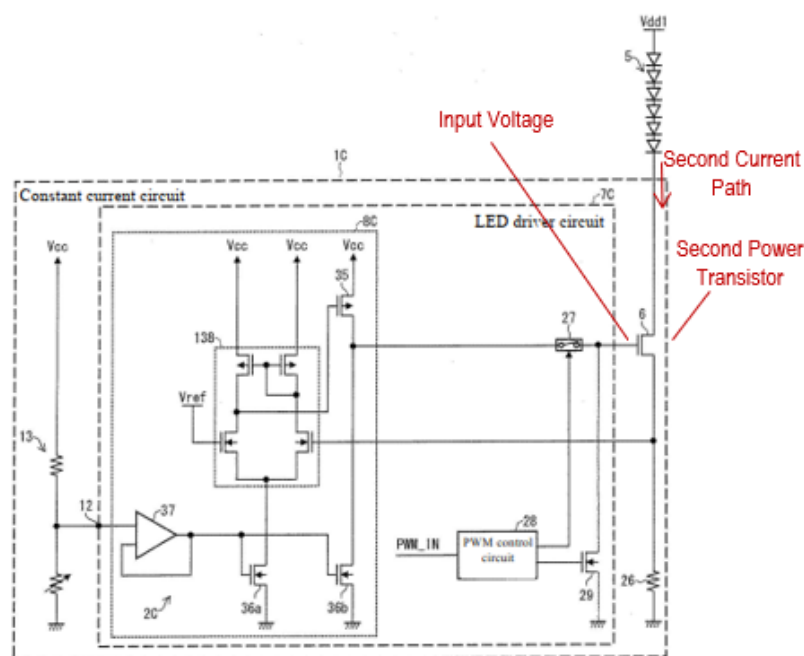
[Grounds 3–5] Additionally (and alternatively) to Sudhaus/Ryoichi, Praxis discloses error amplifiers having two outputs to control two current sources providing current to LED loads. Ex1008, page 3, Section titled “Modern linear regulators with a power distribution,” lines 7-14; and Fig. 1. Two current sources include the first current source to conduct current through first current path.

	 PRAXIS FIG. 1
[2.2] a second power transistor, configured to conduct the shunt current in the second current path based on a second transistor input voltage.	[Grounds 1–5] Sudhaus discloses first and second current sources IS₃ and IS₄ to drive respectively first and second current paths. Ex1005, 4:46-47, Fig. 1.  SUDHAUS FIG. 1 Sudhaus discloses, controller RG controlling second current path IS₄ and resistor R₄ based on input voltage to second current source IS₄. Ex1005, 4:46-47. E.g., Sudhaus states: “Fig. 1 shows an exemplary control circuit 10. Said control circuit comprises two outputs 3, 4, and for

each of these outputs 3, 4, an associated current source IS_3 and IS_4.” Ex1005, 4:25-26, Fig. 1. Sudhaus teaches: controller RG is operative to control two current sources. Ex1005, 4:46-47.

Current sources (such as IS_3 and IS_4) in Sudhaus include a “controlling transistor.” Ex1005, 1:65-2:2.

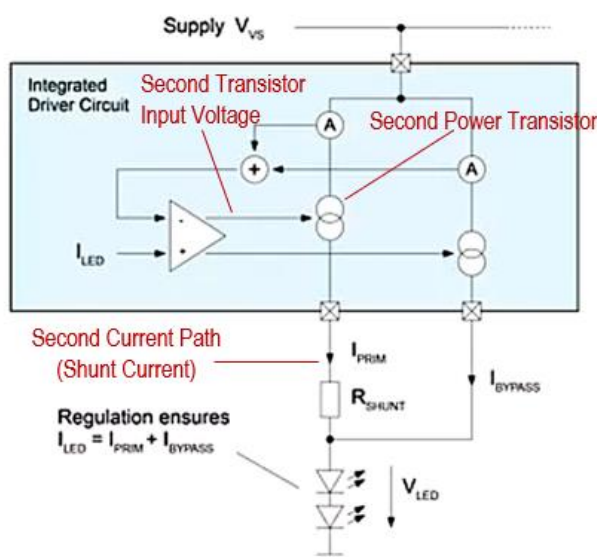
[Grounds 2-5] Additionally (and alternatively) to Sudhaus, Ryoichi shows: transistor 6 (power transistor) receives input voltage on gate input of transistor 6, input voltage being provided by amplifier output stage (transistors 35/36b). Current through transistor 6 is based on this input voltage. Ex1006, Fig. 5.



RYOICHI FIG. 5

[Grounds 3–5] Additionally (and alternatively) to Sudhaus/Ryoichi, Praxis discloses error amplifiers having two outputs to control two current sources providing current to LED loads. Ex1008, page 3, Section titled “Modern linear regulators with a power distribution,” lines 7-14; Fig. 1. Praxis’ two current sources include a second

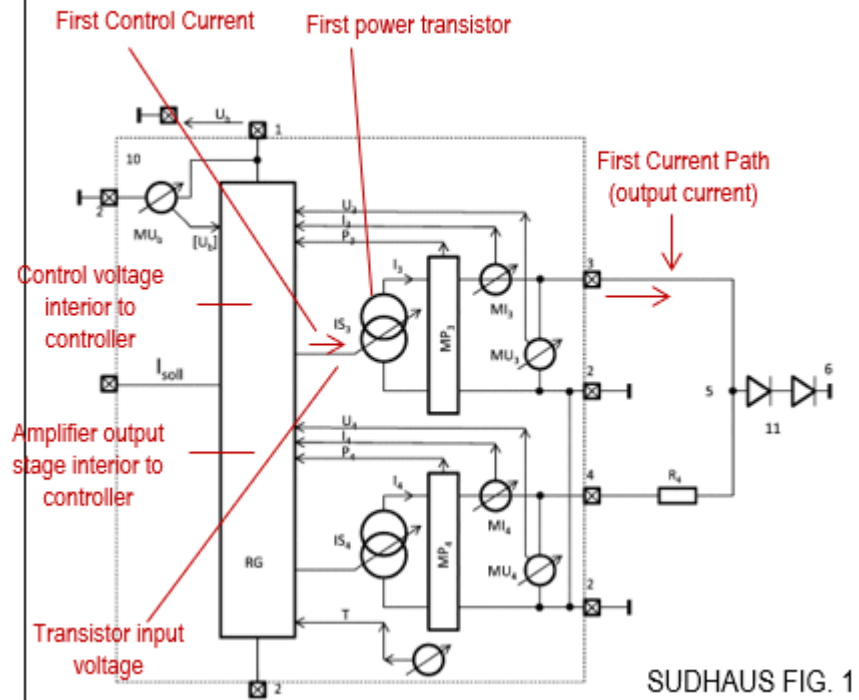
current source that conducts current through a second current path including a shunt resistor.

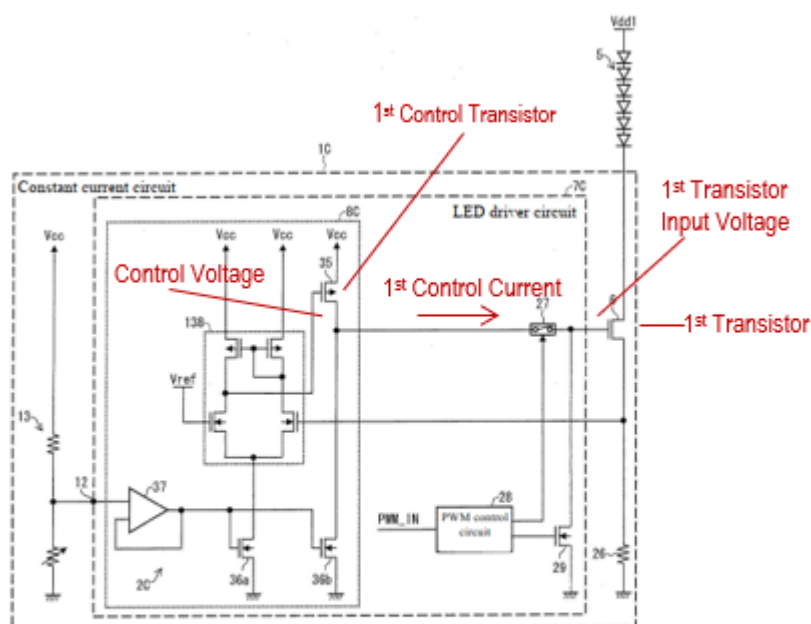


PRAXIS FIG. 1

C. Claim 3 is unpatentable under Grounds 1-5

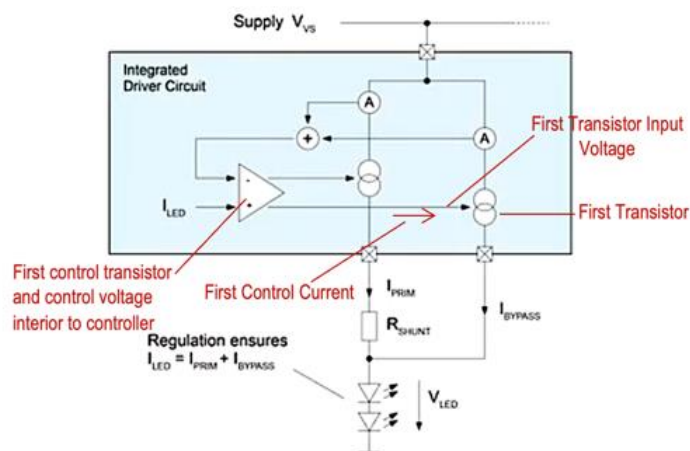
Claim 3	Grounds
[3.1] The system of claim 2, wherein the amplifier output stage comprises: a first control transistor configured to conduct a first control current based on the control voltage to generate the first transistor input voltage, and	[Grounds 1–5] Sudhaus discloses controller RG controlling first current path IS_3. Ex1005, 4:46-47. Control circuit 10 comprises two outputs 3, 4, with associated current source IS_3, IS_4. Ex1005, 4:25-26, Fig. 1. Controller RG is operative to control two current sources. Ex1005, 4:46-47. Controller RG includes an output that generates first control current to generate voltage to control input of first current source IS_3.





RYOICHI FIG. 5

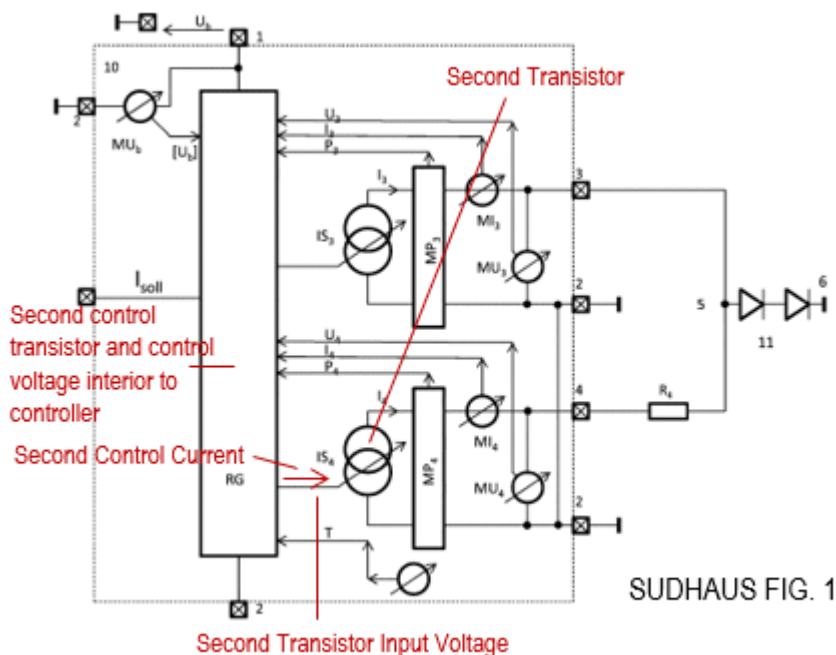
[Grounds 3–5 Additionally (and alternatively) to Sudhaus/Ryoichi, Praxis discloses error amplifiers having two outputs to control two current sources providing current to LED loads. Ex1008, page 3, Section titled “Modern linear regulators with a power distribution,” lines 7-14; Fig. 1. Praxis’ error amplifier includes a first output to control a first current source.



PRAXIS FIG. 1

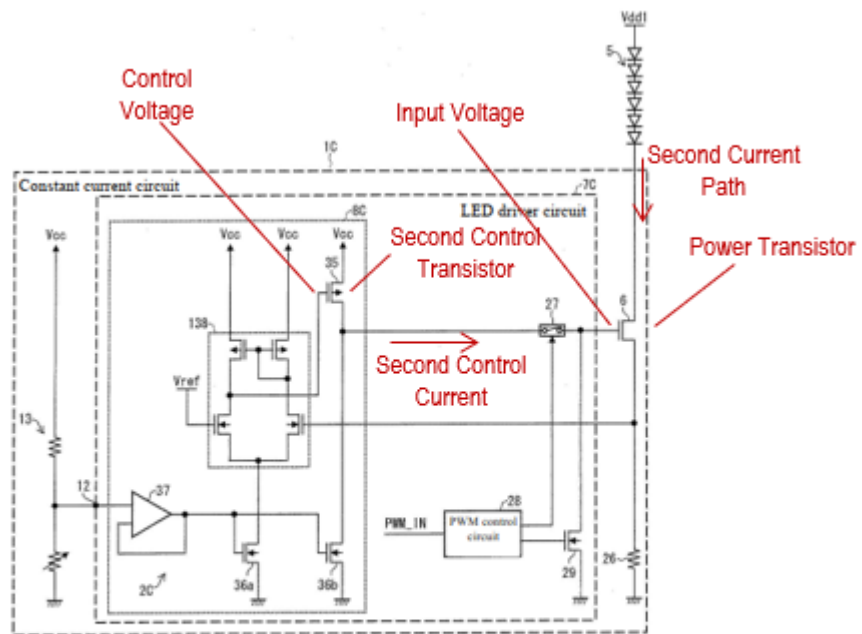
[3.2] a second control transistor to conduct a second control current based on the control voltage to generate the second transistor input voltage.

[Grounds 1–5] Sudhaus discloses Controller RG controlling second current path IS_4 and R_4. Ex1005, 4:46-47. Sudhaus teaches: Controller RG is operative to control two current sources. Ex1005, 4:46-47. Control current from the second RG output generates voltage to control input of second current source IS_4.



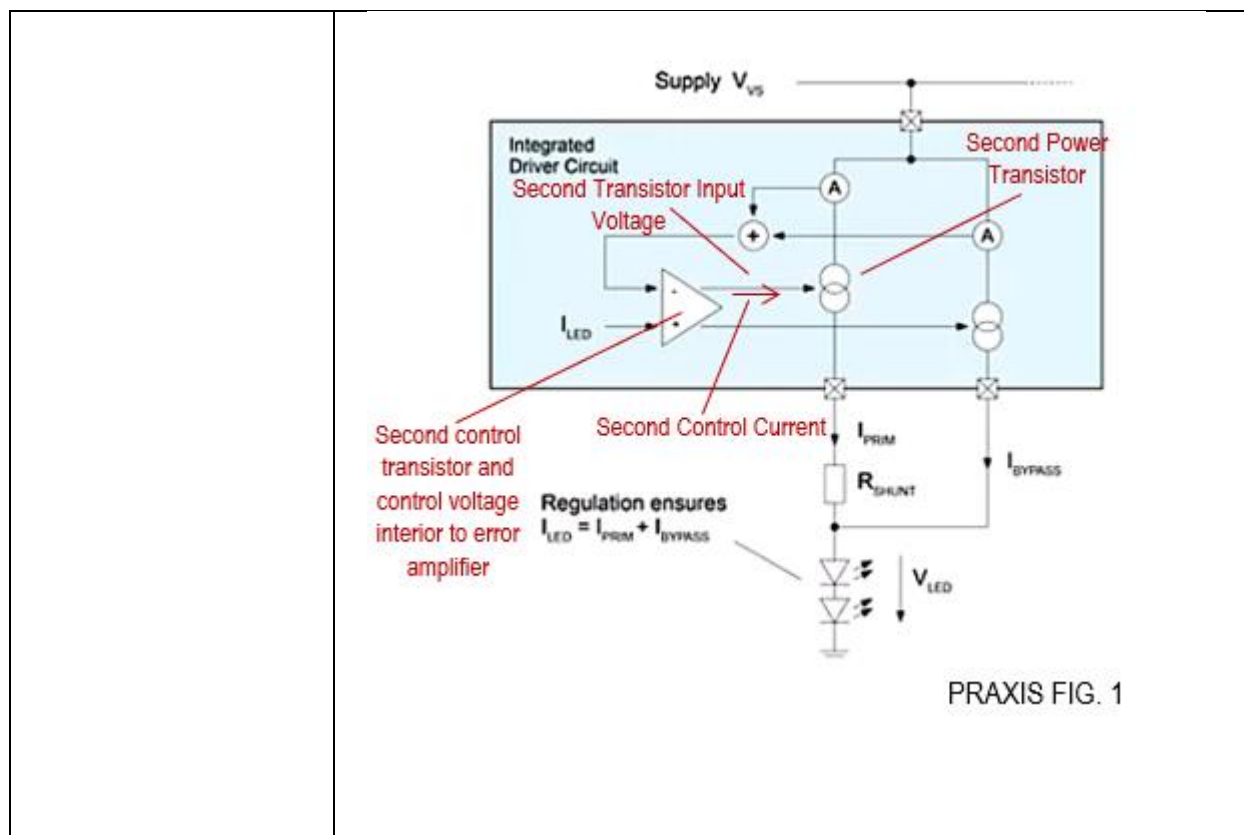
Sudhaus discloses that current sources (such as IS_3 and IS_4) include a power transistor referred to as a controlling transistor. Ex1005, 1:65-2:14. Sudhaus' controller RG includes an output stage that generates current used to drive the power transistor in IS_4. The output stage includes at least one transistor.

[Grounds 2-5] Additionally (and alternatively) to Sudhaus, Ryoichi shows: operational amplifier 8C includes amplifier output stage including transistors 35/36b. Transistor 35 (control transistor) is controlled by output of differential part 138 (control voltage). Ex1006, Fig. 5. First control transistor 35 is configured to conduct current (control current) to drive control input of driving transistor 6 (generate first transistor input voltage).



RYOICHI FIG. 5

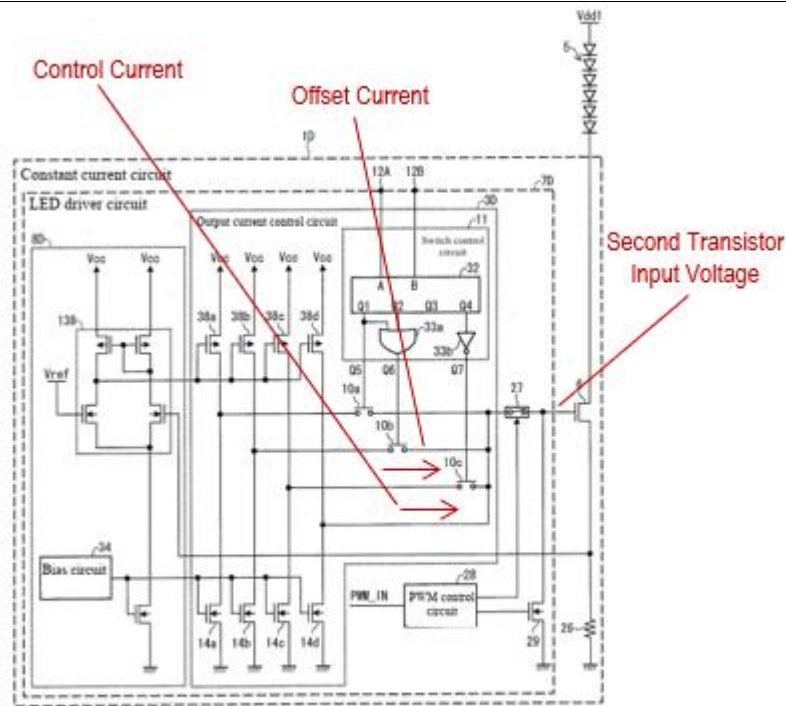
[Grounds 3–5] In addition to Sudhaus, Praxis discloses an error amplifier having two outputs to control two current sources providing current to LED load. Ex1008, page 3, Section titled “Modern linear regulators with a power distribution,” lines 7-14; and Fig. 1. Error amplifier includes second output to control second current source.



D. Claim 4 is unpatentable under Grounds 1-5

[4.1] The system of claim 3, wherein the slew-rate controller is configured to conduct an offset current in parallel with the second control	[Grounds 2–5] Ryoichi discloses a slew-rate controller including multiple parallel paths to generate control current and offset current for first transistor input voltage. Ex1006 Fig.5.
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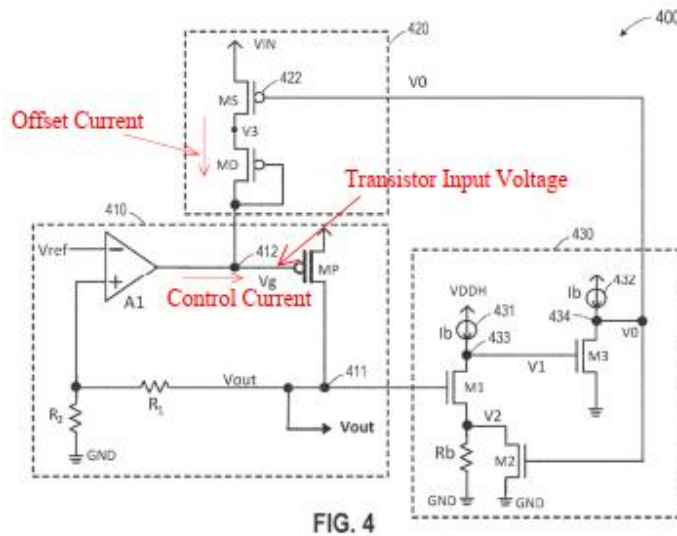
current to
generate
the second
transistor
input
voltage,



RYOICHI FIG. 6

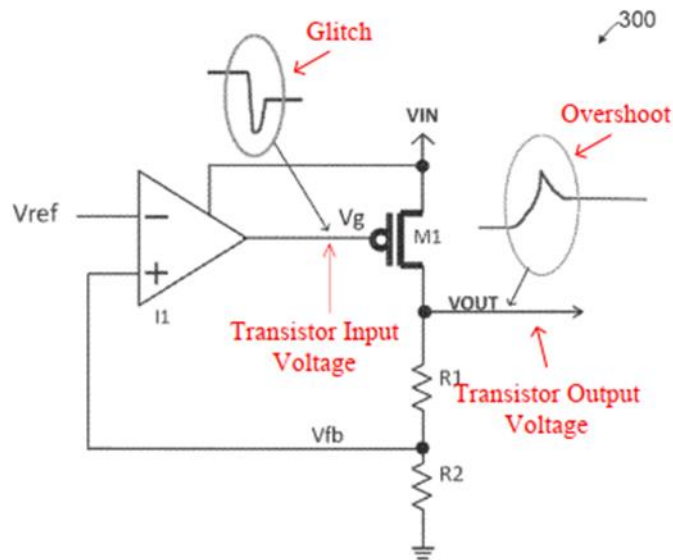
In Ryoichi's Fig. 6, the amplifier output stage of Fig. 5 (transistors 35/36b), has been replaced by transistors 38a, 38b, 38c, 38d (corresponding to transistor 35 of Fig. 5) combined with transistors 14a, 14b, 14c, 14d (corresponding to transistor 36b of Fig. 5. [0087]-[0088]. Drive capability of amplifier output stage can be adjusted by selecting how many of transistors 38a, 38b, 38c, 38d and corresponding transistors 14a, 14b, 14c, 14d are coupled via switches 10a, 10b, 10c to drive driving transistor 6, effectively switching in (or out) an offset current by the switching in or out of a transistor pair (e.g., 14c and 38c as shown above). This allows adjusting rise time and fall time of driving signal applied to driving transistor 6. Ex`006, ¶¶ [0089]-[0092].

[Ground 4] As another alternative, Wu teaches sourcing negative offset current (current reducing slew rate of transistor MP) from positive supply voltage. e.g., Wu Fig. 4 discloses slew rate control circuit 420 that introduces offset into control node of power transistor MP. Ex1009, 6:24-28.



Wu Fig. 4

This is intended to avoid glitch on input of M1 and resulting overshoot at output of power transistor MP shown in Wu, Fig. 3.

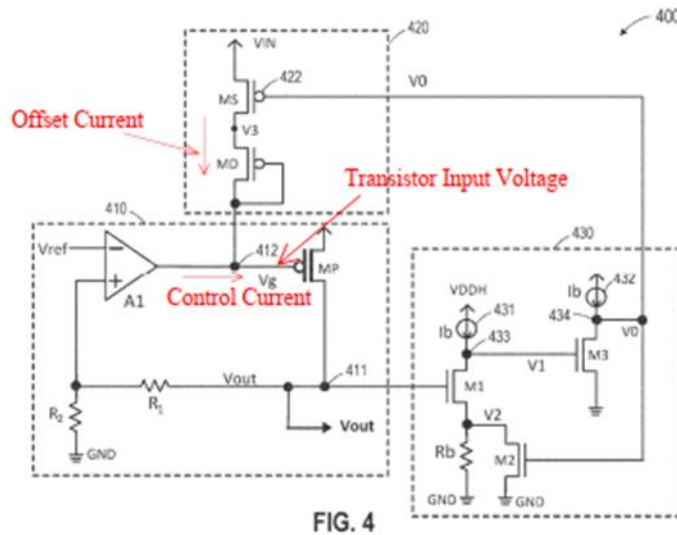


Wu Fig. 3

During power-up, glitch on gate of M1 can cause full rail voltage to appear on output VOUT. Ex1009, 5:47-48.

System of Wu is configured to turn off slew rate control circuit when VOUT reaches preset value. Ex1009, 7:6-9. Preset value is determined

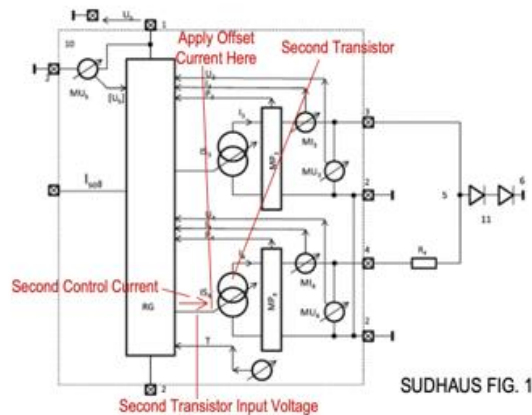
by bias current I_b of first current source, resistance of bias resistor R_b , and threshold voltage on resistor M2. Ex1009, 7:9-11.



Wu Fig. 4

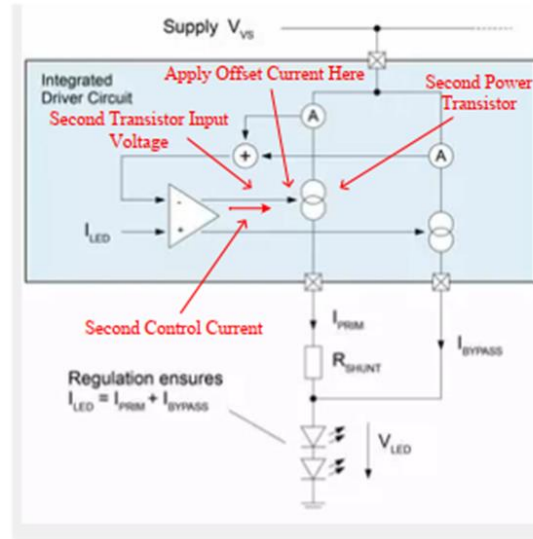
Wu adds source current to control gate of a power transistor in parallel with current from op-amp A1.

Output of Wu can be applied, e.g., to input of second power transistor of Sudhaus, Ex1005, Fig. 1.



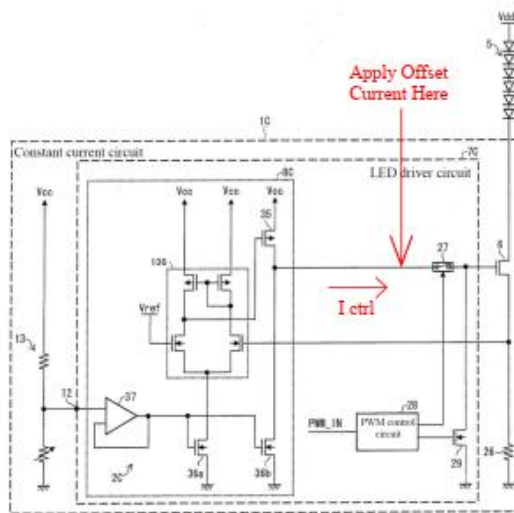
Alternatively, output of Wu can be applied, e.g., to input of second power transistor of Praxis, as shown below. Ex1008, page 3, Section titled "Modern linear regulators with a power distribution," lines 7-14;

and Fig. 1.



Praxis Fig. 1

Alternatively, output of Wu can be applied, e.g., to input of transistor 6 of Ryoichi, Fig. 5. Ex1006, Fig. 5.



Ryoichi Fig. 5

[Ground 5] The combination of Provost and TI Paper provide an offset current controlled by a ramp voltage. Provost discloses on-chip ramp generator in Fig. 4. Ex1010, Fig. 4.

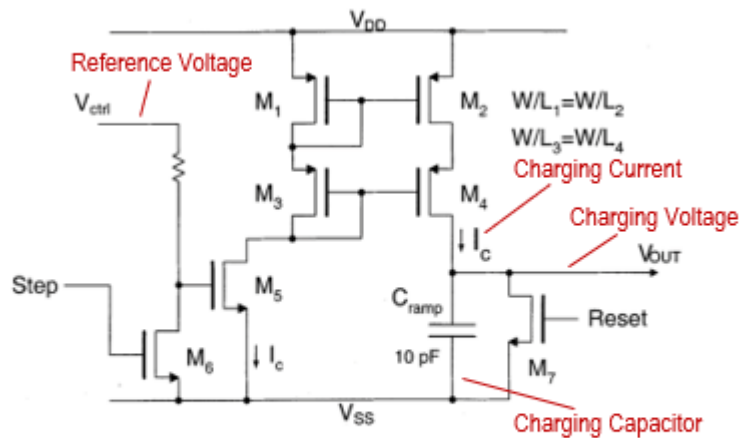
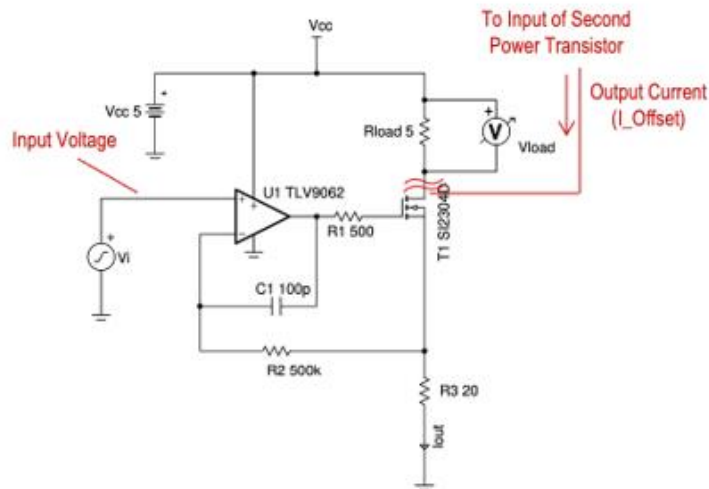


Fig. 4. Schematic of the basic current source of first analog ramp generator.

PROVOST FIG. 4

Provost's on-chip ramp driver transistor M5 is current driver, M1-M4 form a cascode current mirror and C_ramp is charging capacitor. M6 is used for stopping current source when Step is at logic 1. M7 is used to reset C_ramp. I_c is the charging current that charges C_ramp to generate charging voltage V_OUT. Ex1010, page 264, Adaptive Scheme, line 23 – page 265, Adaptive Scheme, line 32.

Based on ramp generated by on-chip ramp generator, offset current can be generated using voltage-to-current converter, such as disclosed in TI Paper, Ex1011. TI Paper, in Fig. 1, discloses voltage-to-current converter.



TI PAPER FIG. 1

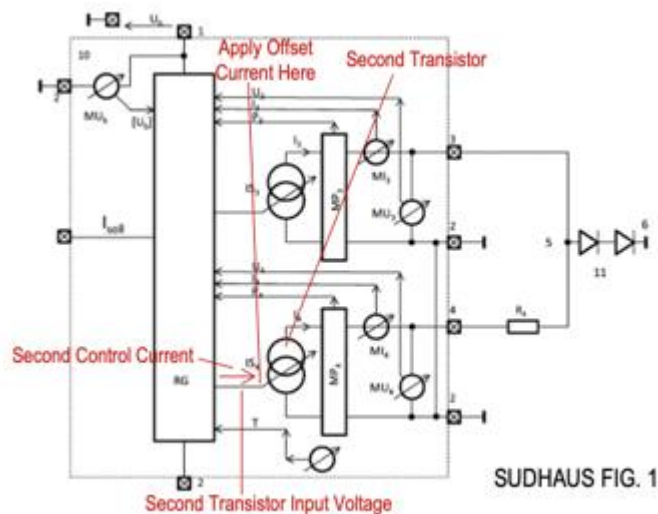
Ex1011, page 1. the output current is given by:

$$I_o = \frac{V_i}{R_3}$$

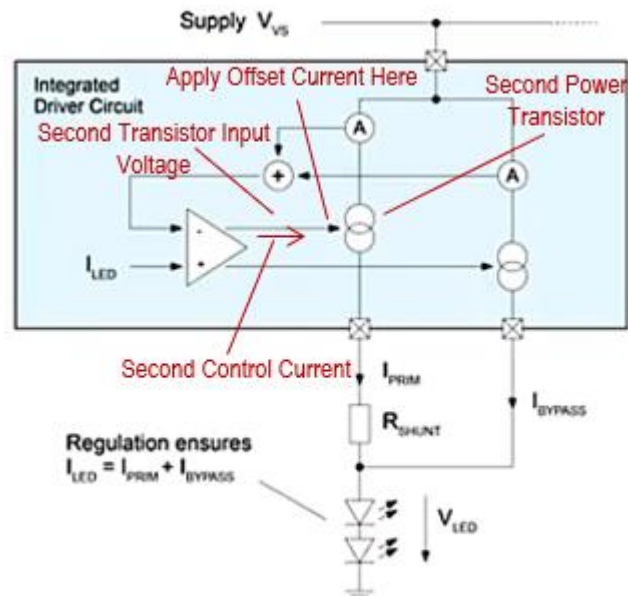
Ex1011, page 2, lines 1-2.

To generate offset current for current application, output of on-chip ramp generator V_{outf} can be applied as V_i to voltage-to-current converter of TI Paper.

Output current I_o of voltage-to-current converter can be applied as current I_{offset} , for example, to the second transistor of Sudhaus.
Ex1005, Fig. 1.

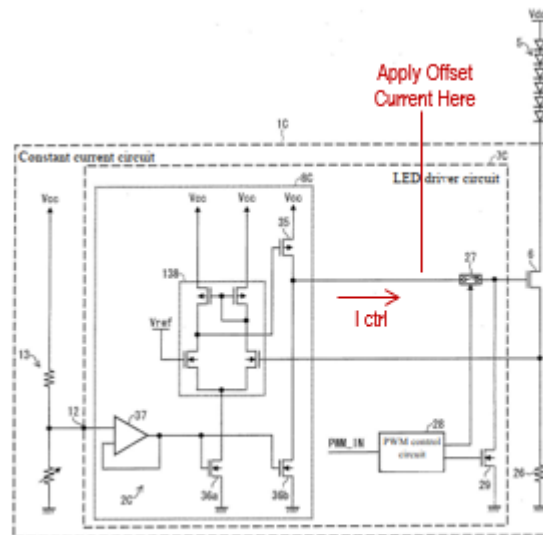


Alternatively, offset current I_{offset} can be applied to input of second current source of Praxis. Ex1008, page 3, Section titled "Modern linear regulators with a power distribution," lines 7-14.



PRAXIS FIG. 1

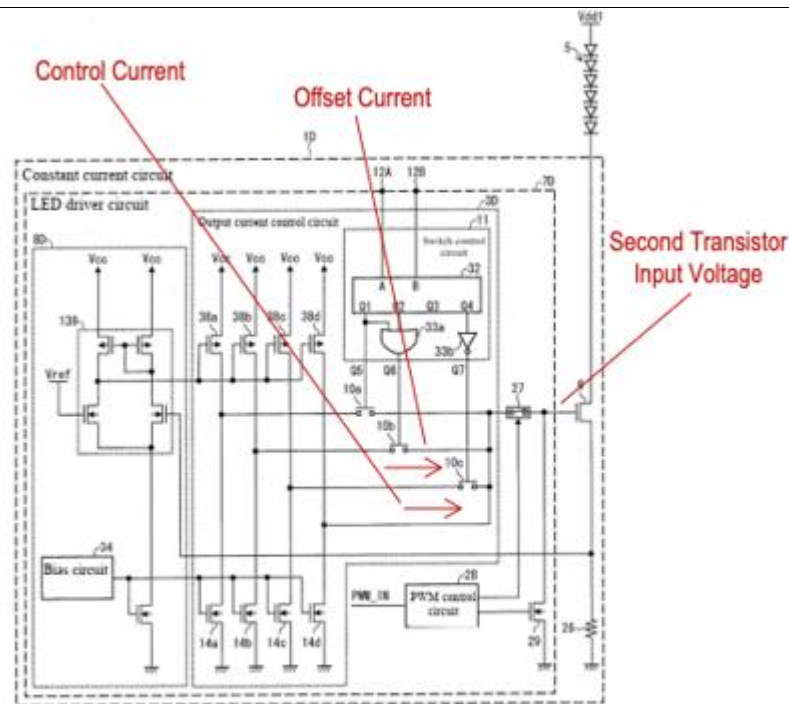
Alternatively, offset current I_{offset} can be applied to gate of power transistor, for example, transistor 6 in Ryoichi Fig. 5. Ex1006, Fig. 5.



RYOICHI FIG. 5

[4.2] the offset current increasing at the slew-rate.

[Grounds 2–5] Ryoichi describes a slew rate at a lower level, e.g., if only one pair of transistors, for example transistors 38d/14d are connected to the gate of driver transistor 6, and will be at another, higher level (faster) if one or more pair of transistors, e.g., 38c/14c is switched in. Accordingly, offset current (current introduced by current pair 38c/14c) increases as slew rate increases. 6. Ex1006, [0089]-[0092].

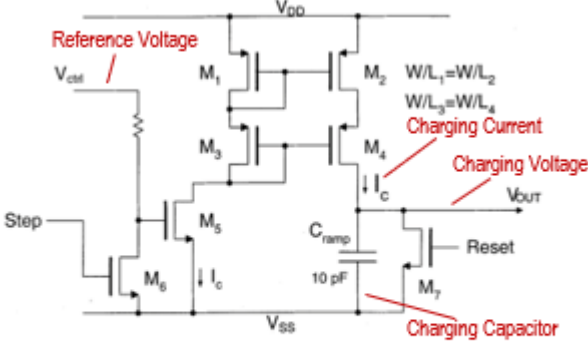
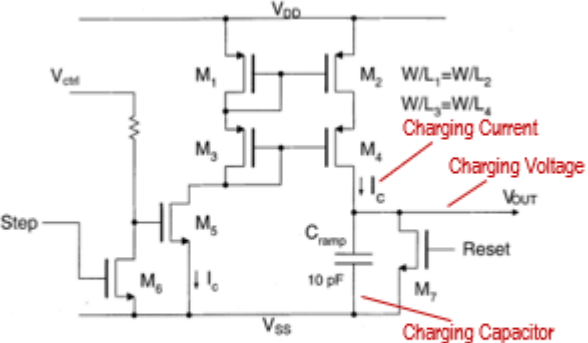


RYOICHI FIG. 6

[Ground 4] Alternatively, controlled slew rate of Wu can be applied, e.g., to second power transistor of Sudhaus (Ex1005, Fig. 1), to second power transistor input of Praxis (Ex1008, page 3, Section titled “Modern linear regulators with a power distribution,” lines 7-14, and Fig. 1), or to input of transistor 6 of Ryoichi, Fig. 5, EX1006, Fig. 5) until slew-rate control circuit 420 is turned off. Ex1009, 7:52-63. Adding negative offset current (i.e., source current) to control gate of power transistor as it is turning on to control slew rate and then turning it off at preset voltage causes an effective increase in sink current (current increasing slew rate) applied to gate.

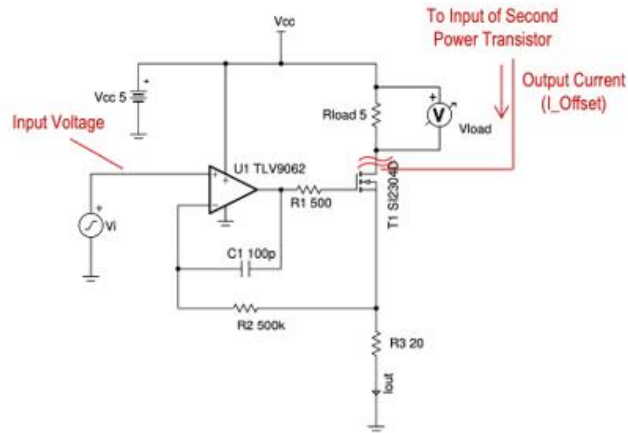
[Ground 5] Alternatively, based on Provost and TI Paper, applying ramp voltage V_{out} of Provost to input of voltage-to-current converter of TI Paper generates an offset current (I_{out} of V-I converter) that changes with slew rate of ramp.

E. Claim 5 is unpatentable under Ground 5

Claim 5 [5.1] The system of claim 4, wherein the slew-rate controller comprises: a charging current generator configured to generate a charging current;	Grounds [Ground 5] Provost discloses on-chip ramp generator in Fig. 4 including charging current generator.  Fig. 4. Schematic of the basic current source of first analog ramp generator. PROVOST FIG. 4 Provost's on-chip ramp driver (Fig. 4_, transistor M5 together with M1-M4 form charging current generator. Charging current I_c charges C_{ramp} to generate charging voltage V_{OUT}. Ex1010, page 264, Adaptive Scheme, line 23 – page 265, Adaptive Scheme, line 32.
[5.2] a charging capacitor that is charged by a charging current to generate a charging voltage;	[Ground 5] Provost Fig. 4 shows charging a charging capacitor C_{ramp} with charging current I_c to generate a charging voltage. Ex1010, page 264, Adaptive Scheme, line 23 – page 265, Adaptive Scheme, line 32.  Fig. 4. Schematic of the basic current source of first analog ramp generator. PROVOST FIG. 4

[5.3] a current mirror configured to conduct the offset current based on the charging voltage.

[Ground 5] Based on ramp (Charging Voltage) generated by on-chip ramp generator, offset current can be generated using voltage-to-current converter, such as disclosed in TI Paper, Ex1011. TI Paper, in Fig. 1, discloses voltage-to-current converter.



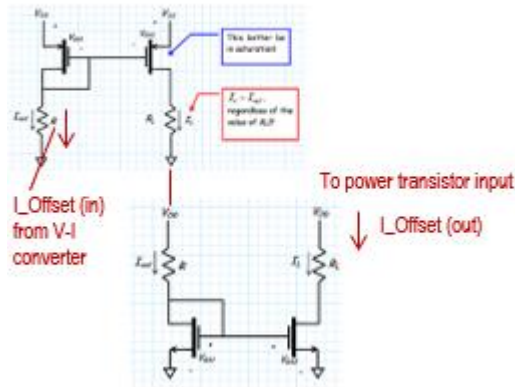
TI PAPER FIG. 1

To generate offset current for current application, output of on-chip ramp generator V_{outf} can be applied as V_i to voltage-to-current converter of TI Paper.

Current I_{Offset} from voltage-to-current converter can be delivered to input of second power transistor via current mirrors if necessary.

UK Paper, Ex1012, discloses NMOS/PMOS current mirrors. Ex1012, Fig. page 2, Fig. page 6.

PMOS Current Mirror (Fig. page 6)



NMOS Current Mirror (Fig. page 2)

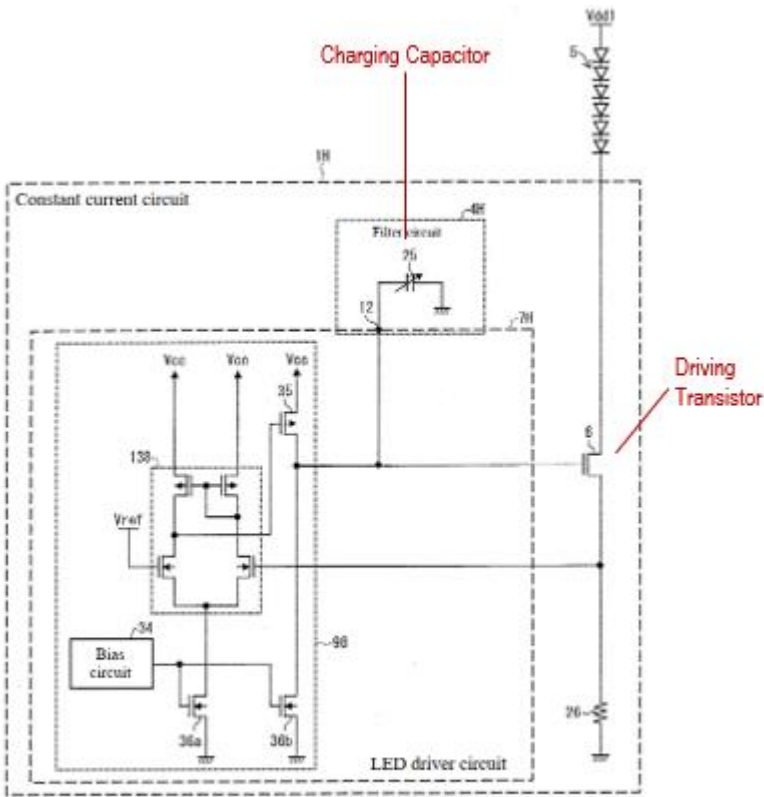
Where, if transistors in transistor pairs are dimensioned similarly, I_{ref} will equal I_L for both NMOS Current Mirror and the PMOS Current Mirror. Ex1012, page 3. One PMOS current mirror together with one NMOS current mirror can be used to conduct offset current based on charging voltage as shown above.

F. Claim 6 is unpatentable under Grounds 1-5

<u>Claim 6</u>	<u>Grounds</u>
The system of claim 1, wherein the amplifier output stage is configured to increase an amplitude of the shunt current and decrease an amplitude of the	[Grounds 1–5] Sudhaus discloses: as supply voltage increases, a portion of total current of two current paths is gradually taken over by second current path [current path including external shunt resistor]. Ex1005, 5:43-46. Sudhaus states: “[i]n a second operating current range B, the current is gradually taken over by the second current path at the second connector 4 with the second resistor R4.” Ex1005, 5:43-46.” That is, with increasing supply voltage, amplitude of shunt current increases and

output current as the supply voltage increases.	amplitude of output current (current path without shunt resistor) decreases.
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G. Claim 7 is unpatentable under Grounds 2-5

Claim 7	Grounds
The system of claim 1, wherein the slew-rate controller comprises a charging capacitor having a capacitance that defines the slew-rate of the shunt current.	[Grounds 2-5] Ryoichi teaches slew-rate controllers comprising charging capacitors having capacitance that defines slew rate of control signals to driving transistors in reference to Fig. 10. Ex1006, Fig. 10.  RYOICHI FIG. 10 Ryoichi's variable capacitor 25 can be adjusted to adjust rise/fall time of output stage of operational amplifier 98. Ex1006, Fig. 10, [0104].

[Ground 5] Provost Fig. 4 discloses on-chip ramp generators including charging capacitors C_{ramp} . Ex1010, Adaptive Scheme, page 264 line 23 – page 265 line 32.

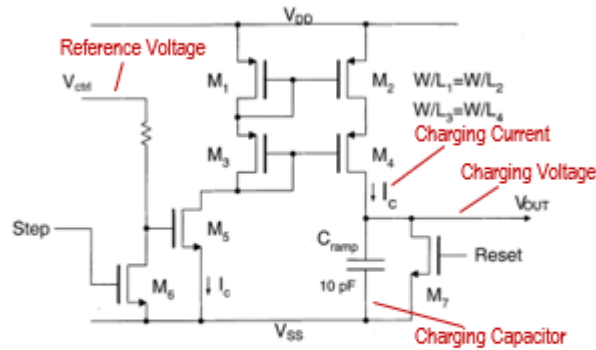
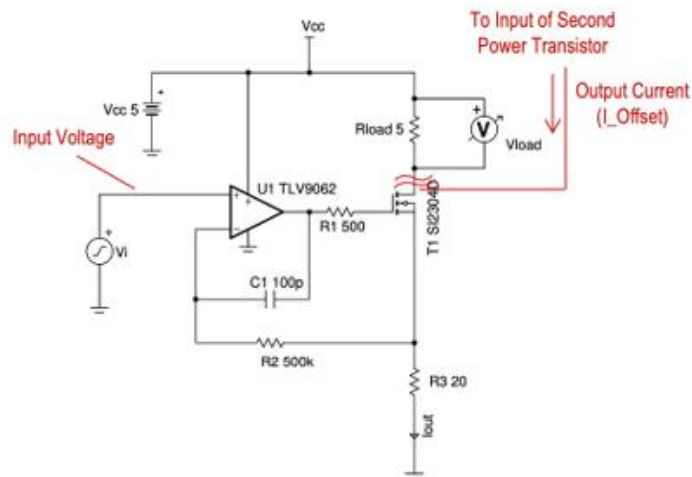


Fig. 4. Schematic of the basic current source of first analog ramp generator.

PROVOST FIG. 4

Based on ramp, generated by on-chip ramp generator, offset current can be generated using voltage-to-current converter, such as disclosed in TI Paper, Ex1011. TI Paper, in Fig. 1, discloses voltage-to-current converter.

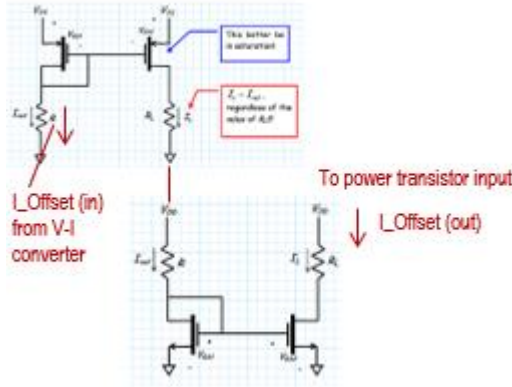


TI PAPER FIG. 1

Ex1011, page 1. The output current is given by:

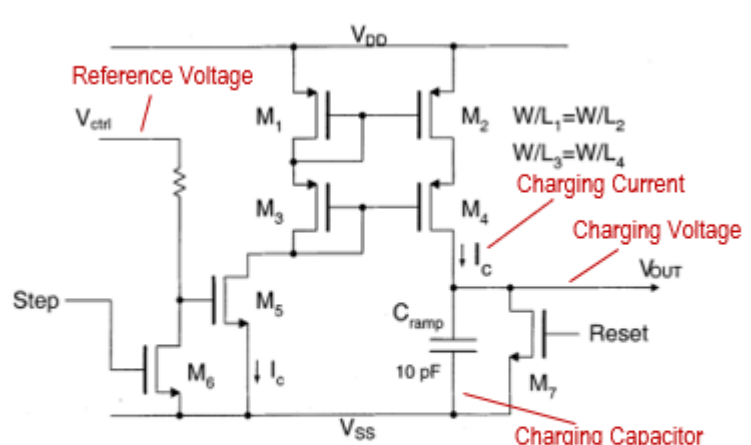
$$I_o = \frac{V_i}{R_3}$$

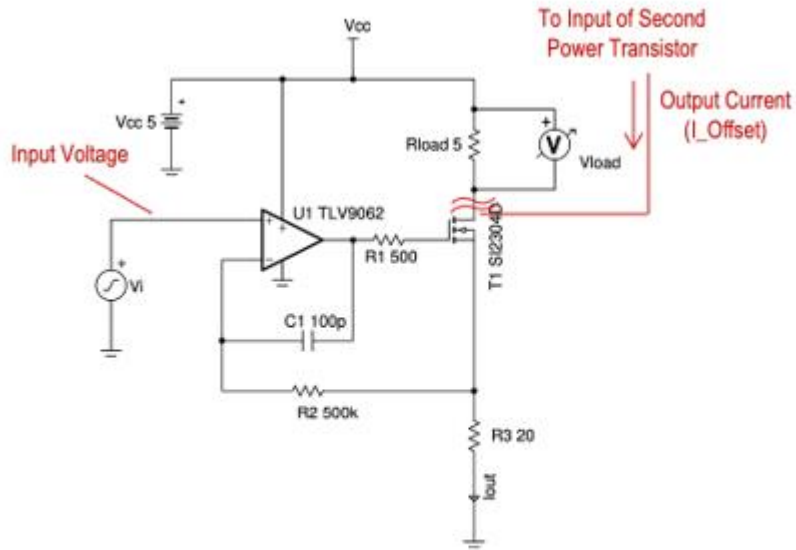
Ex1011, page 2, lines 1-2.

	To generate offset current for current application, output of on-chip ramp generator V_{out} can be applied as V_i to voltage-to-current converter of TI Paper, and output current I_{out} [I_o] of voltage-to-current converter can be applied as current I_{offset} to gate of power transistor, e.g., transistor 6 in Ryoichi Fig. 5, either directly, or via a current mirror, if required. UK Paper, Ex1012, discloses NMOS and PMOS current mirrors.  Converting voltage V_{out} at output of Provost to current I_{offset} at output of voltage-to-current converter of TI Paper and delivering the current I_{offset} via current mirror as in UK Paper results in charging voltage of Provost controlling offset current via current mirror.
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H. Claim 8 is unpatentable under Ground 5

<u>Claim 8</u>	<u>Grounds</u>
[8.1] The system of claim 7, further comprising a power transistor configured to	[Ground 5] Element 8.1 is invalid for the same reasons cited in reference to claim element [2.2].

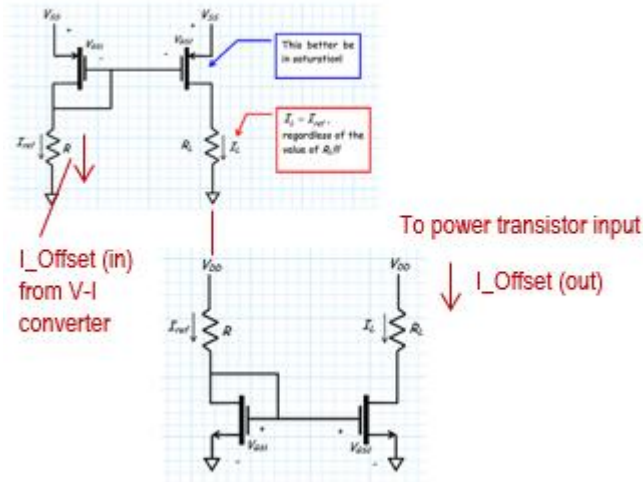
conduct the shunt current in the second current path based on a transistor input voltage,	
[8.2] wherein the charging capacitor is configured to generate a charging voltage to control an amplitude of an offset current via a current mirror,	[Ground 5] Provost discloses on-chip ramp generator in Fig. 4 including charging current generator M5 and M1-M4. The charging current generates a voltage V_{OUT} (charging voltage) on a capacitor C_{ramp} (charging capacitor).  Fig. 4. Schematic of the basic current source of first analog ramp generator. PROVOST FIG. 4 Ex1010, Adaptive Scheme, page 264 line 23 - page 265 line 32. Based on ramp generated by on-chip ramp generator, offset current can be generated using voltage-to-current converter, such as disclosed in TI Paper, Ex1011, page 1, Fig. 1.



TI PAPER FIG. 1

To generate offset current for current application, output of on-chip ramp generator V_{outf} can be applied as V_i to voltage-to-current converter of TI Paper, and output current I_{out} [I_o] of voltage-to-current converter can be applied as current I_{offset} to an input to a current mirror, as shown in UK Paper.

UK Paper discloses NMOS/PMOS current mirrors. Ex1012, page 2, page 6.

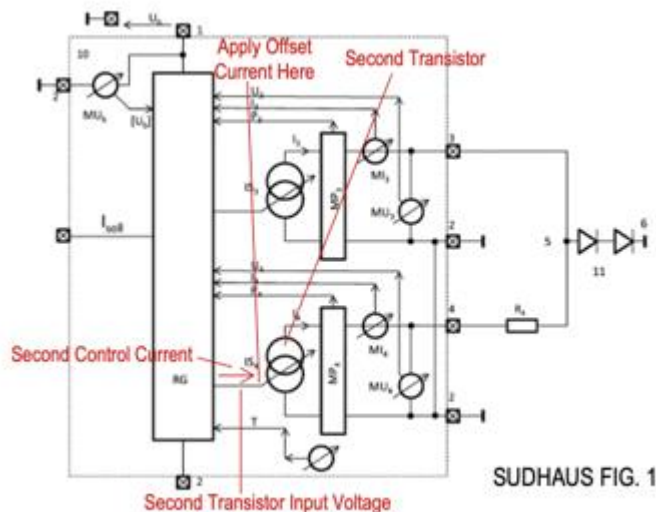


One PMOS current mirror together with one NMOS current mirror can be used to conduct offset current based on charging voltage.

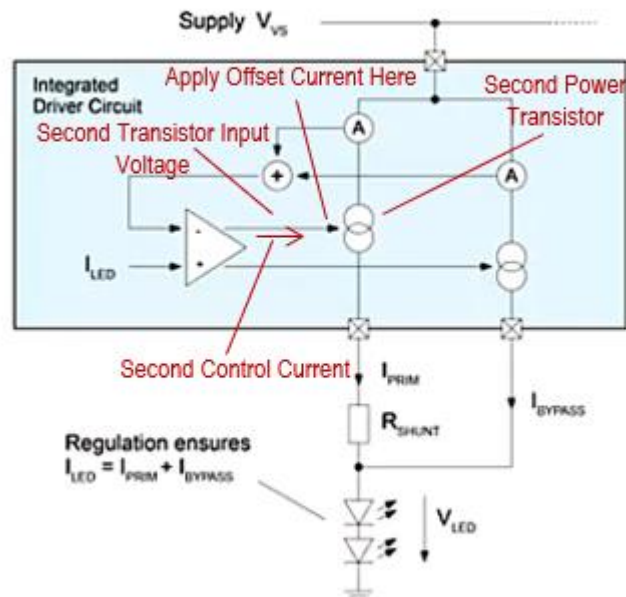
Amplitude of the offset current delivered by the current mirror may be based on a charging voltage generated by Provost.

[8.3] wherein the offset current is configured to control the transistor input voltage.

[Ground 5] Output current (I_{offset}) can be applied, e.g., to input of second transistor of Sudhaus, as shown below. Ex1005, Fig. 1.

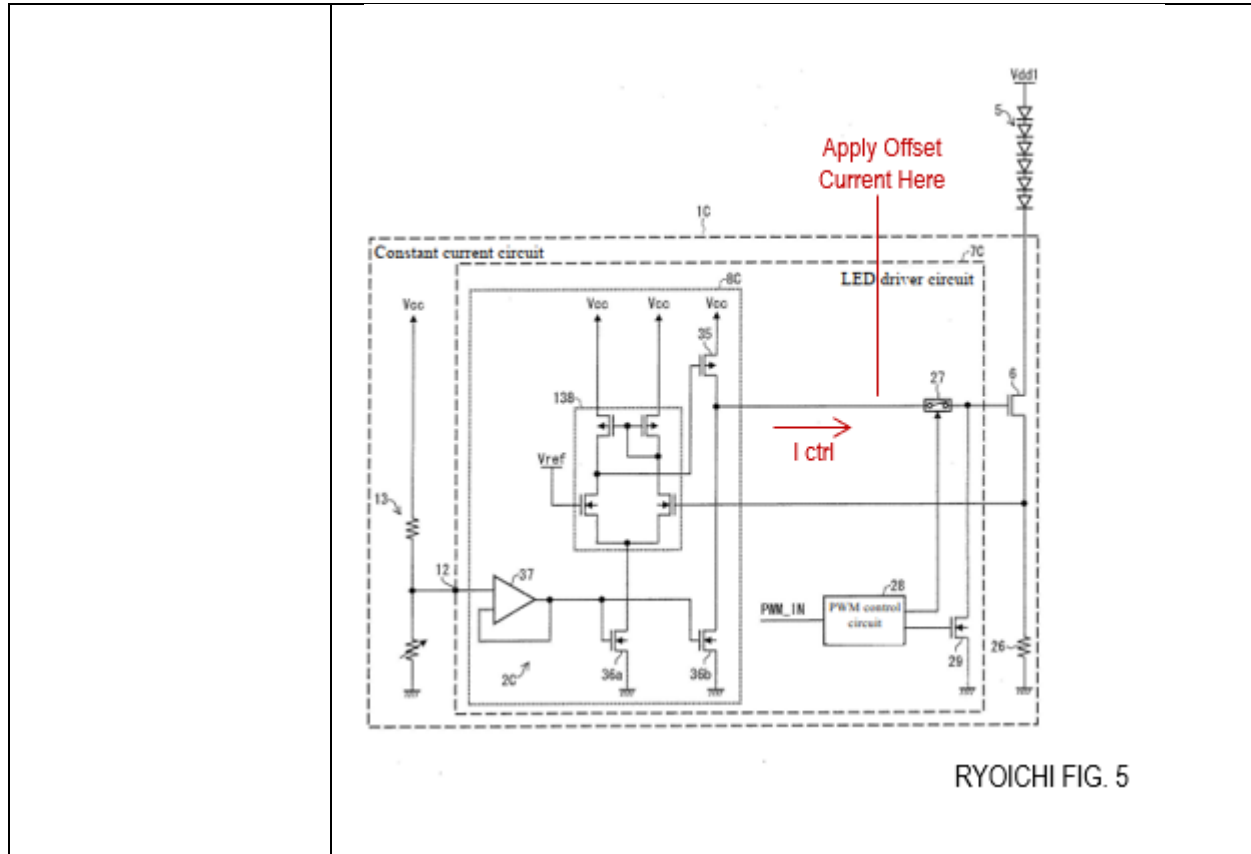


Alternatively, offset current I_{offset} can be applied to input of second power transistor of Praxis, (see below).



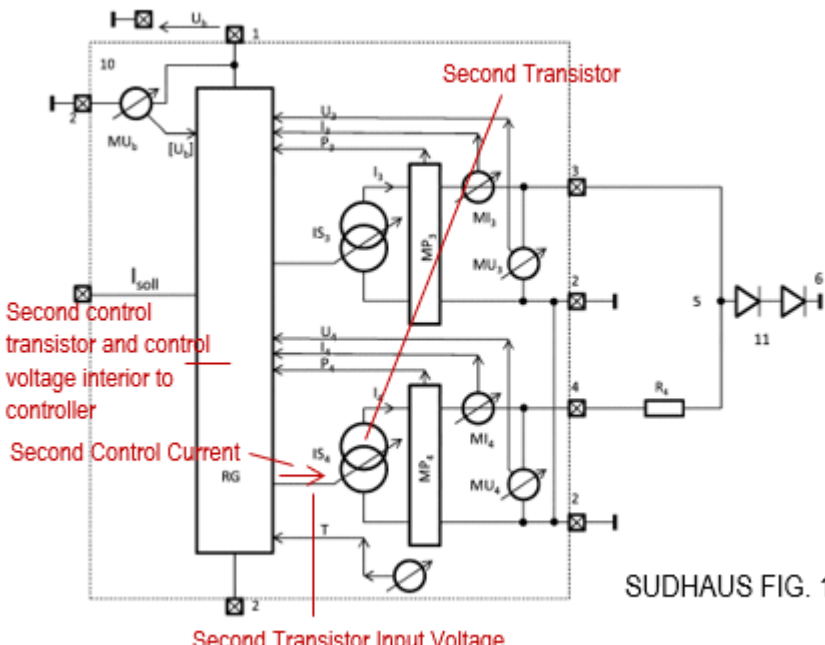
PRAXIS FIG. 1

Alternatively, offset current (I_{offset}) can be applied to input of power transistor 6 of Ryoichi to control transistor input voltage.



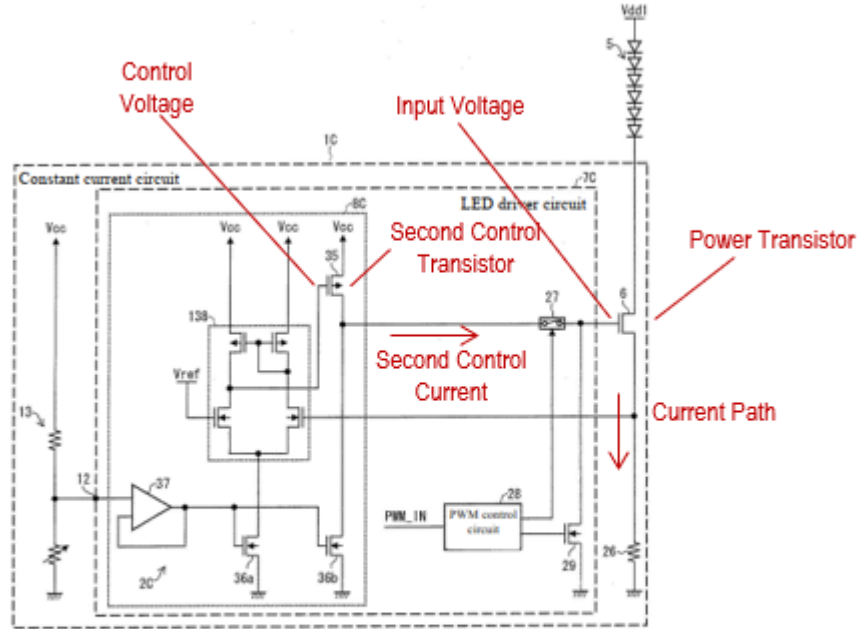
I. Claim 9 is unpatentable under Ground 5

Claim 9	Ground 5
[9.1] The system of claim 8, wherein the amplifier output stage comprises a control transistor that is controlled by the control voltage,	[Ground 5] Claim 9 claims control of the second current path. Sudhaus Fig. 1 discloses, controller RG controlling second current path IS_4 and R4. Ex1005, 4:46-47. Sudhaus teaches: controller RG operative to control two current sources. Ex1005, 4:46-47. Control current from second RG output generates voltage to control input of second current source IS_4.



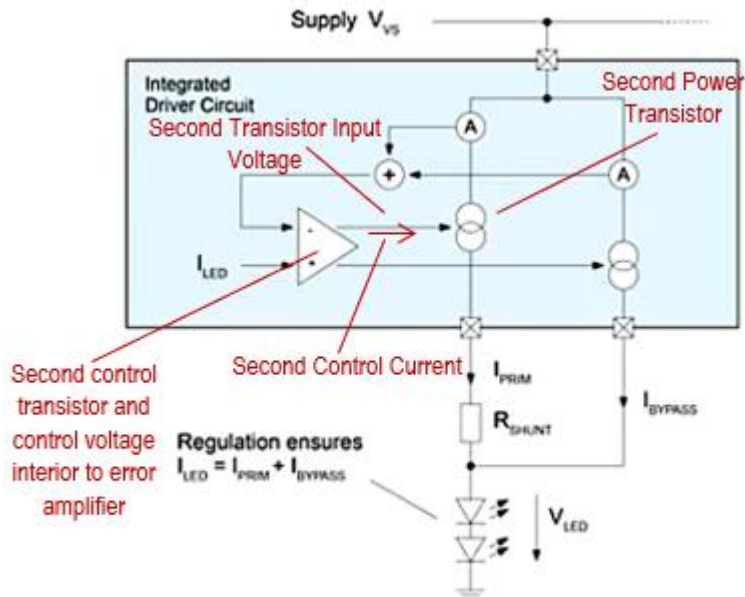
Sudhaus discloses current sources (e.g., IS_4) including a power transistor referred to as a controlling transistor.
Ex1005, 1:65-2:14.

In addition to Sudhaus, Ryoichi shows: operational amplifier 8C includes amplifier output stage including transistors 35/36b. Transistor 35 (control transistor) is controlled by output of differential part 138 (control voltage). Ex1006, Fig. 5. First control transistor 35 conducts current (control current) to drive control input of driving transistor 6 (generate first transistor input voltage).



RYOICHI FIG. 5

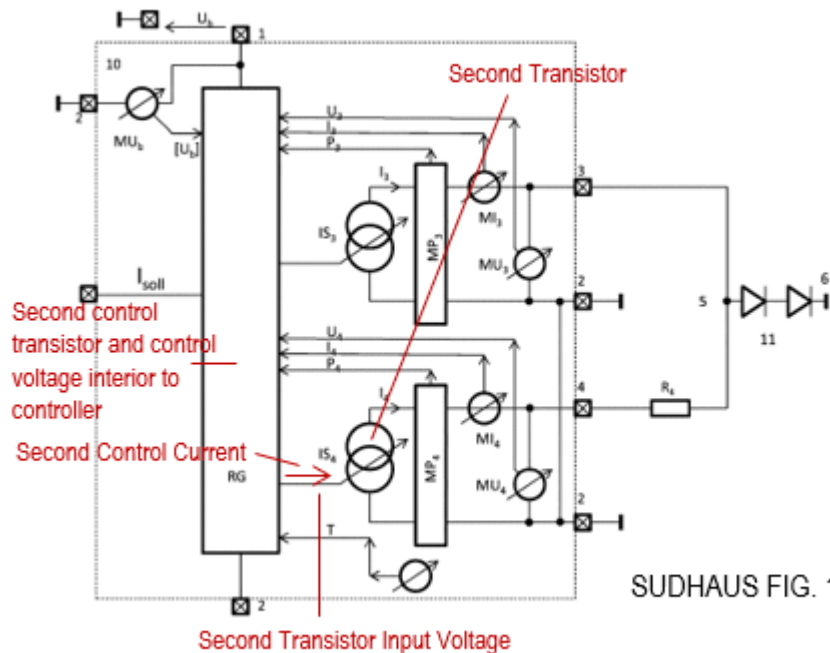
In addition to Sudhaus/Ryoichi, Praxis discloses error amplifiers having two outputs to control two current sources providing current to LED loads. Ex1008, page 3, Section titled “Modern linear regulators with a power distribution,” lines 7-14; and Fig. 1. Praxis’ error amplifier includes second output to control second current source.



PRAXIS FIG. 1

[9.2] wherein the control transistor is coupled to an input of the power transistor to set an initial amplitude of the transistor input voltage,

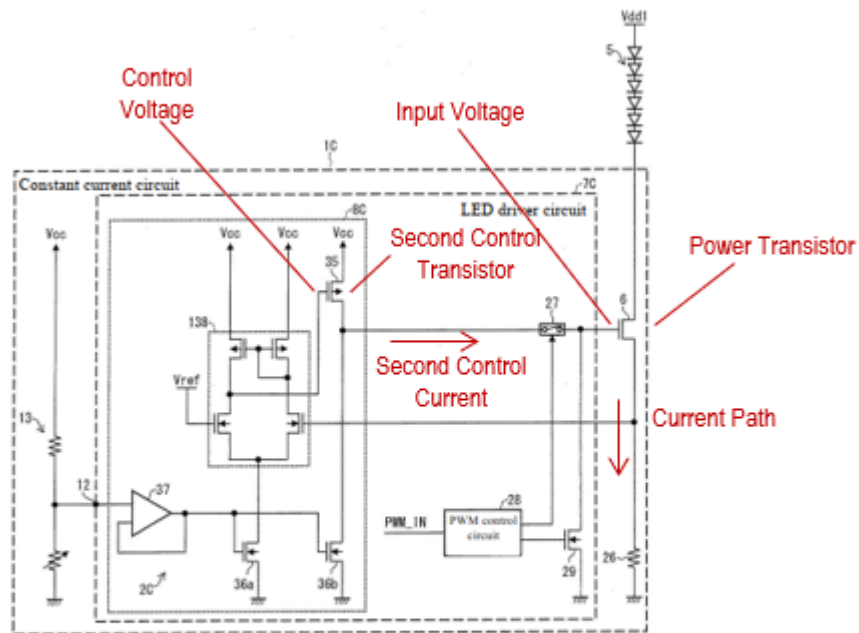
[Ground 5] Sudhaus shows control transistors (internal to controller RG) connected to an input of the power transistor. Ex1005, 4:46-47.



SUDHAUS FIG. 1

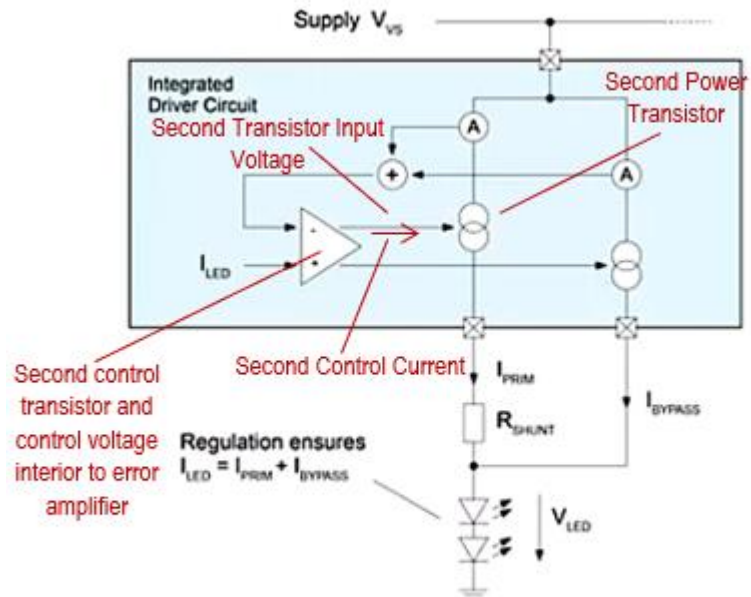
The power transistor initial amplitude of the input voltage is determined by the control transistor.

Alternatively, Ryoichi shows amplifier output stages coupled to input of power transistors 6. Ex1006, Fig. 5. Ryoichi's amplifier output stage sets initial amplitude of transistor input voltage.



RYOICHI FIG. 5

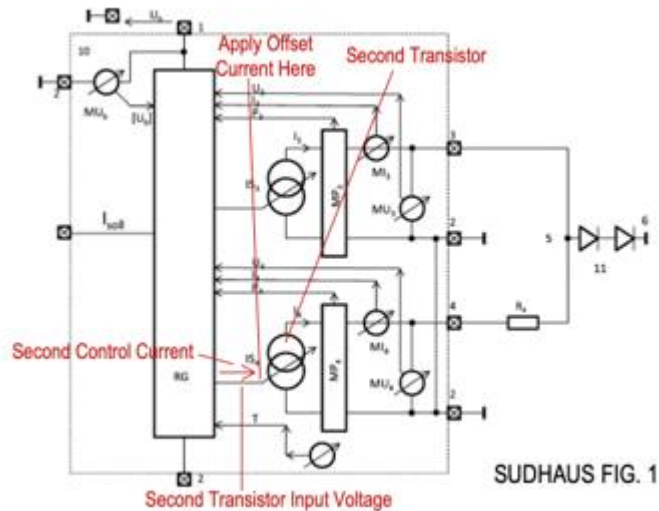
Alternatively, Praxis discloses error amplifiers having two outputs to control two current sources providing current to LED loads. Ex1008, page 3, Section titled “Modern linear regulators with a power distribution,” lines 7-14; and Fig. 1. Praxis Fig.1 shows outputs of the error amplifier connected to respective inputs of a current source (power transistor) which set an initial amplitude of the input voltage before an offset current is applied.



PRAXIS FIG. 1

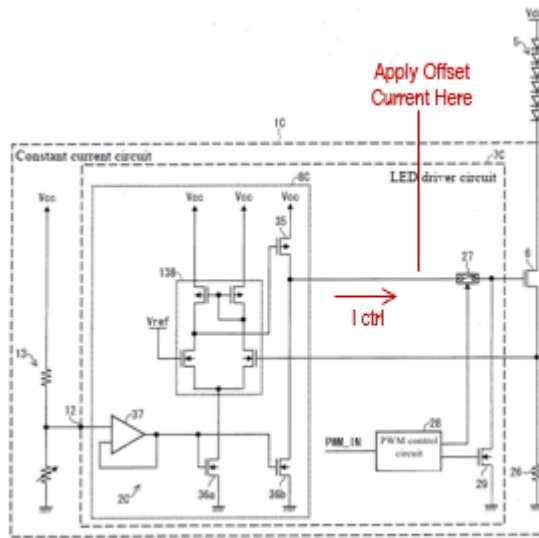
[9.3] wherein the offset current is subtracted from the initial amplitude to control the power transistor based on the slew-rate.

[Ground 5] As per Claim 7, Provost, TI Paper and UK Paper show generating an offset current that varies with the slew rate. The offset current I_{offset} can be applied, for example, to the input of the second transistor of Sudhaus, Ex1005, Fig. 1.



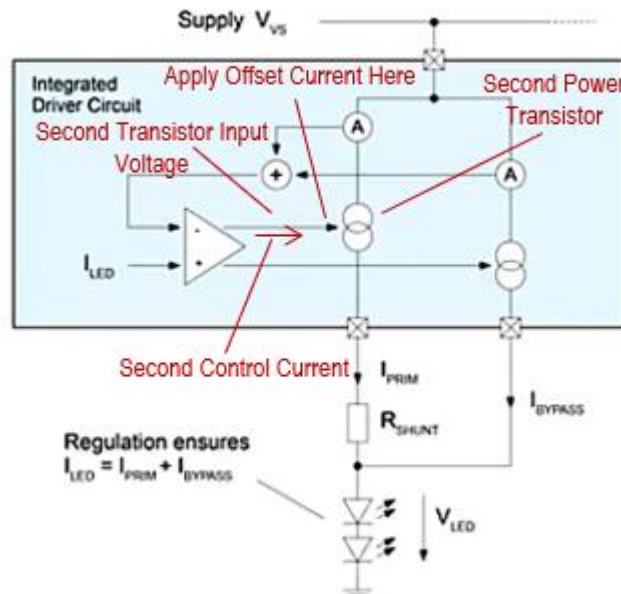
SUDHAUS FIG. 1

Alternatively, offset current can be applied e.g. to Ryoichi's power transistor 6 to control the power transistor based on slew rate.



RYOICHI FIG. 5

Alternatively, offset current can be applied to the input of the second power transistor (Praxis, Fig. 1).



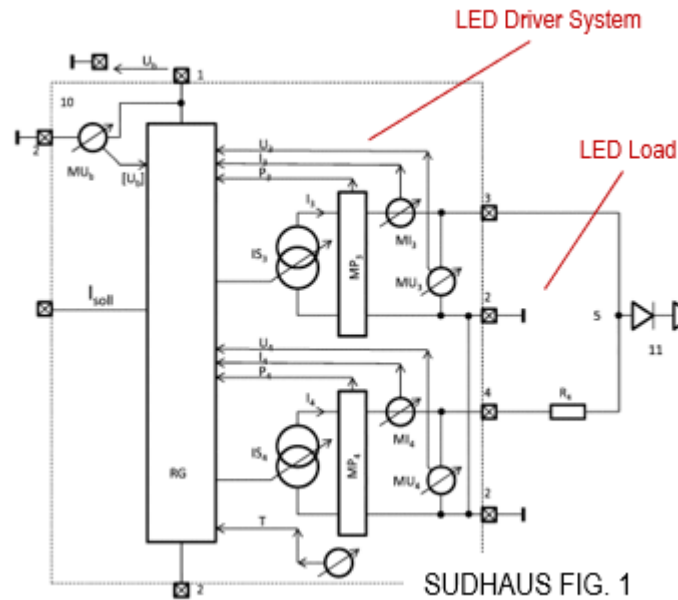
PRAXIS FIG. 1

J. Claim 10 is unpatentable under Grounds 1-5

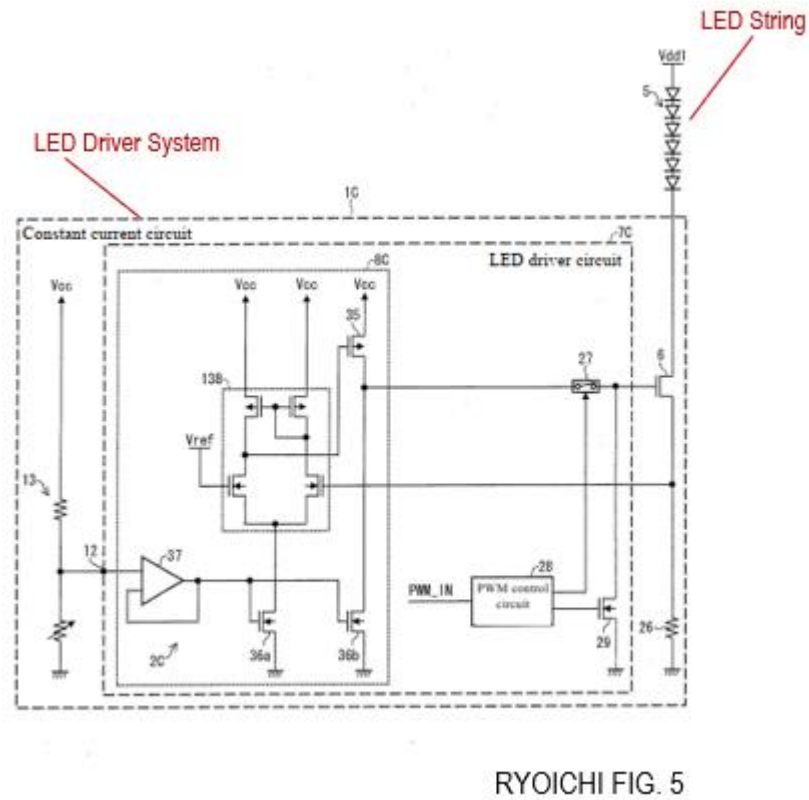
<u>Claim 10</u>	<u>Grounds</u>
An integrated circuit (IC) chip comprising the LED driver system of claim 1.	[Grounds 1–5] Sudhaus discloses a control circuit designed as integrated circuit (IC), e.g., Sudhaus states: [t]hus, according to the disclosure, the apparatus for supplying at least one consumer with electrical energy ... is provided with a control circuit designed as an integrated circuit (IC) and having a control circuit ... having at least a first output and a second output, wherein the consumer can be powered with electrical energy ... wherein the desired value for the electrical power of the consumer , which electrical power can be controlled by the control circuit, can be specified, and ... wherein the distribution of the electrical current for the consumer ... between the at least two outputs ... can be controlled by said control circuit ...” Ex1005, 2: 25-50.

K. Claim 11 is unpatentable under Grounds 1-5

<u>Claim 11</u>	<u>Grounds</u>
[11.pre] A light-emitting diode (LED) system comprising:	[Grounds 1–5] Claim 11, [11.pre] is equivalent to Claim 1, [1.pre], additionally including an LED string.



[Ground 2–5] See Claim 1, [1.pre].



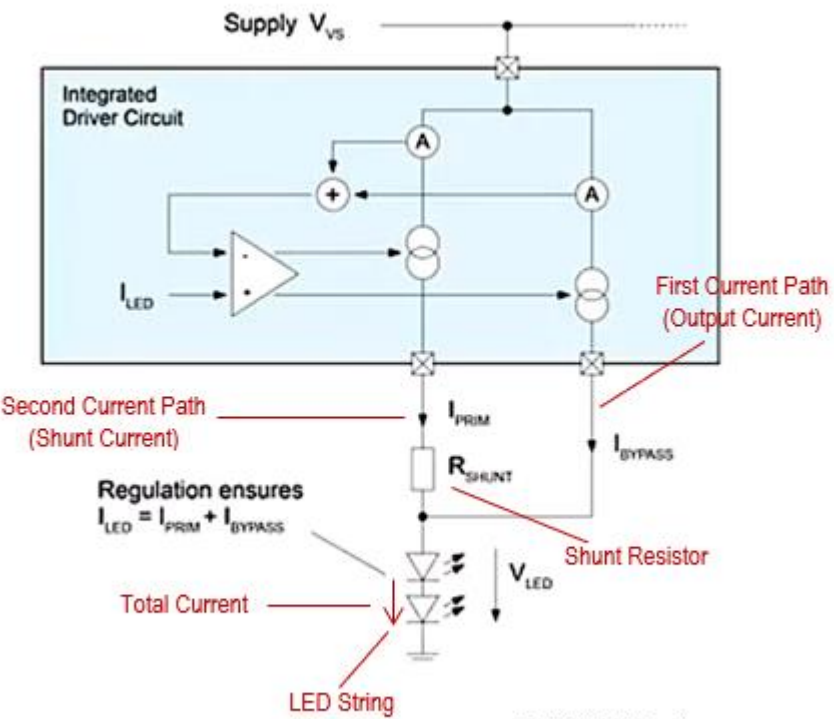
[11.1] an error

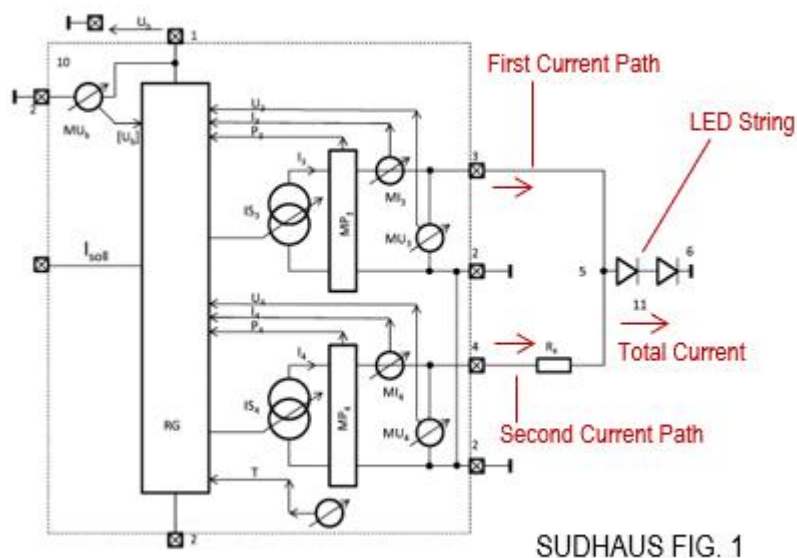
Equivalent to Claim 1 [1.1].

amplifier configured to compare an input voltage with a reference voltage to generate a control voltage; and an amplifier output stage configured to control an output current through a first current path	
[11.2] and a shunt current through a second current path based on the control voltage,	Equivalent to Claim 1, [1.2].
[11.3] the amplifier output stage comprising a slew-rate controller configured to control slew-rate of the shunt current;	Equivalent to Claim 1, [1.3].
[11.4] a shunt resistor in the second current path to conduct the shunt current; and	[Grounds 1–5] Sudhaus discloses current paths includes external resistors, e.g., Sudhaus states: “[t]he current of the second current source IS_4 is conducted via the resistor R_4 ...” Ex1005, 4:30-33, Fig. 1.

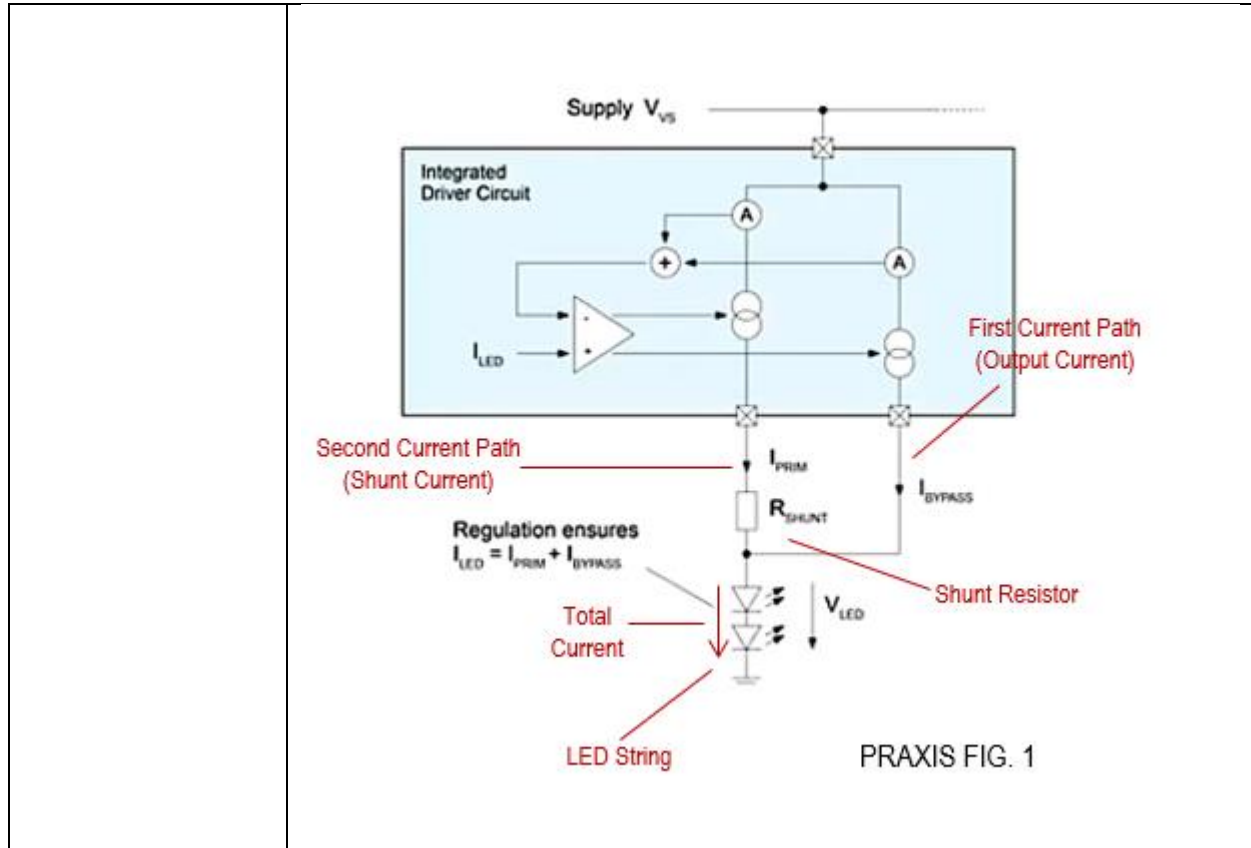


- 84 -

	 PRAXIS FIG. 1
[11.5] an LED string arranged at an output of the first current path and the second current path to illuminate in response to a total current comprising a sum of the output current and the shunt current.	[Grounds 1-5] Sudhaus discloses that the controller is operative to control the total of the two output currents based on a desired value I_{soll}. Ex1005, 4:46-50, Fig. 1. The total current is delivered to an LED string.



Grounds [3–5] In addition to Sudhaus, and alternatively, Praxis discloses error amplifiers having two outputs to control two current sources providing current to LED load. Ex1008, page 3, Section titled “Modern linear regulators with a power distribution,” lines 7-14; and Fig. 1.



L. Claim 12 is unpatentable under Grounds 2-5

<u>Claim 12</u>	<u>Grounds</u>
The system of claim 11, wherein the slew-rate controller comprises a charging capacitor having a capacitance that defines the slew-rate of the shunt current.	Supra Claim 7 Grounds (Claim 12 is equivalent to, and unpatentable for the same reasons as Claim 7).

M. Claim 13 is unpatentable under Ground 5

<u>Claim 13</u>	<u>Grounds</u>
[13.1] The system of claim 12, further comprising a power transistor configured to conduct the shunt current in the second current path based on a transistor input voltage,	Supra Claim 8 Grounds (Claim 13 is equivalent to, and unpatentable for the same reasons as Claim 8).
[13.2] wherein the charging capacitor is configured to generate a charging voltage to control an amplitude of an offset current via a current mirror,	<i>Supra 8.2.</i>
[13.3] wherein the offset current is configured to control the transistor input voltage.	<i>Supra 8.3.</i>

N. Claim 14 is unpatentable under Ground 5

<u>Claim 14</u>	<u>Grounds</u>
[14.1] The system	Claim 14 includes elements equivalent to Claim 9, e.g.

of claim 13, wherein the amplifier output stage comprises a control transistor that is controlled by the control voltage,	[14.1] is equivalent to [9.1]
[14.2] wherein the control transistor is coupled to an input of the power transistor to set an initial amplitude of the transistor input voltage,	Supra [9.2].
[14.3] wherein the offset current is subtracted from the initial amplitude to control the power transistor based on the slew-rate.	Supra [9.3].

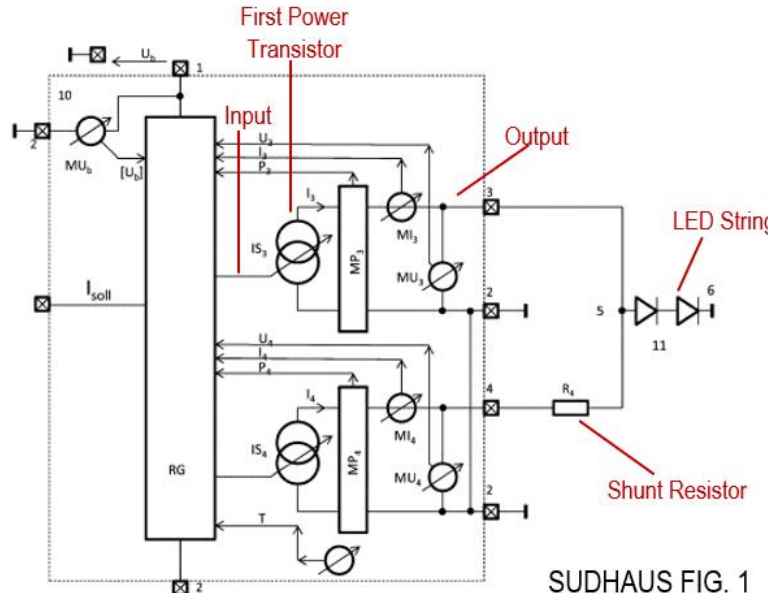
O. Claim 15 is unpatentable under Grounds 2-5

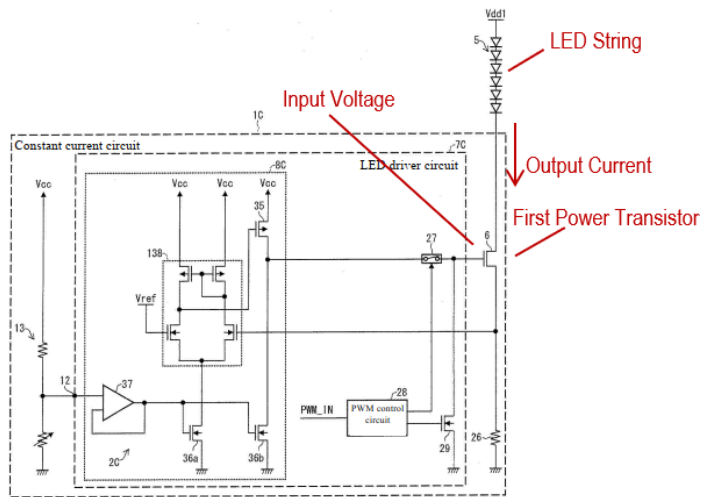
Claim 15	<u>Grounds</u>
[15.1] The system of claim 11, further comprising: a first power transistor configured to conduct the output current in the first current path based on a first transistor input voltage; and	Claim 15 includes elements equivalent to earlier claim elements, e.g. [15.1] is equivalent to [2.1]
[15.2] a second	Supra [2.2].

power transistor configured to conduct the shunt current in the second current path based on a second transistor input voltage;	
[15.3] wherein the amplifier output stage comprises: a first control transistor configured to conduct a first control current based on the control voltage to generate the first transistor input voltage; and	Supra [3.1].
[15.4] a second control transistor configured to conduct a second control current based on the control voltage to generate the second transistor input voltage,	Supra [3.2].
[15.5] wherein the slew-rate controller is configured to conduct an offset current in parallel with the second control current to generate the second transistor input voltage,	Supra [4.1].

[15.6] the offset current increasing at the slew-rate.	Supra [4.2].
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P. Claim 16 is unpatentable under Grounds 1-5.

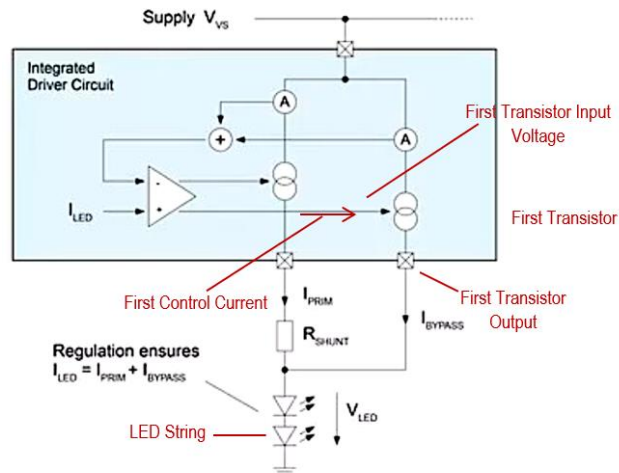
<u>Claim 16</u>	<u>Grounds</u>
[16.pre] A light-emitting diode (LED) driver system comprising:	Supra [1.pre] [16.pre] is equivalent to [1.pre].
[16.1] a first power transistor comprising an input and an output coupled to an LED string and a shunt resistor;	[Grounds 1-5] Sudhaus FIG 1 discloses output 3 coupled to LED load 11 and shunt resistor R_4 and driven by current source IS_3. Ex1005, 4:46-50, Fig. 1.  SUDHAUS FIG. 1 [Grounds 2-5] In addition to Sudhaus, and alternatively, Ryoichi discloses, in Fig. 5, driving transistor 6. Ex1006, Fig. 5.



RYOICHI FIG. 5

Ryoichi Fig. 5 shows: first transistor 6 receives input voltage on gate input of transistor 6, input voltage being provided by amplifier output stage (transistors 35/36b). Current through transistor 6 (current in first path) is based on input voltage. Ex1006, Fig. 5. Output is coupled to LED string 5.

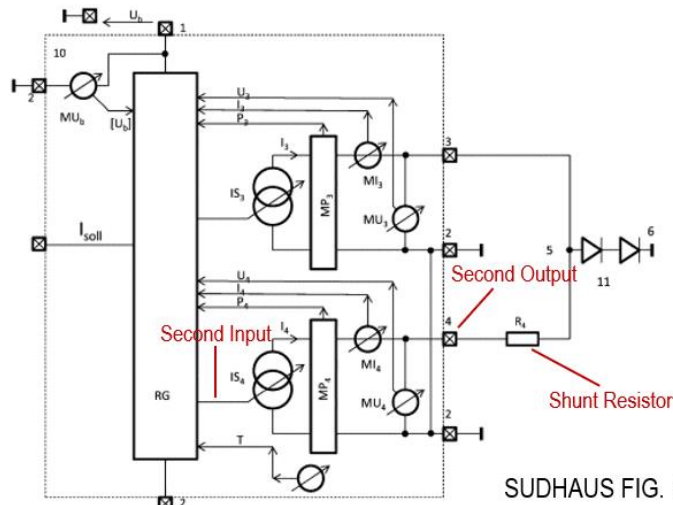
[Grounds 3-5] In addition to Sudhaus and Ryoichi, and alternatively, Praxis discloses error amplifiers having two outputs, one output driving an input to a first current source, the current source having a first input and an output coupled to the LED load and to resistor R_SHUNT Ex1008, page 3, Section entitled “Modern linear regulators with a power distribution,” lines 5-14; and Fig. 1. Praxis discloses first current source having first input and being coupled to LED load and to resistor R_SHUNT.



PRAXIS FIG. 1

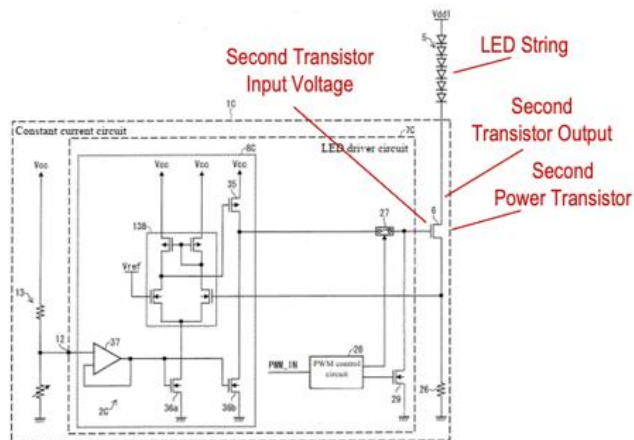
[16.2] a second power transistor comprising an input and an output coupled to the shunt resistor;

[Grounds 1-5] Sudhaus FIG 1 discloses output 4 driven by IS_4. IS_4 includes a power transistor driven by the controller RG and an output coupled to the shunt resistor R_4. Ex1005, 4:46-50, Fig. 1.



SUDHAUS FIG. 1

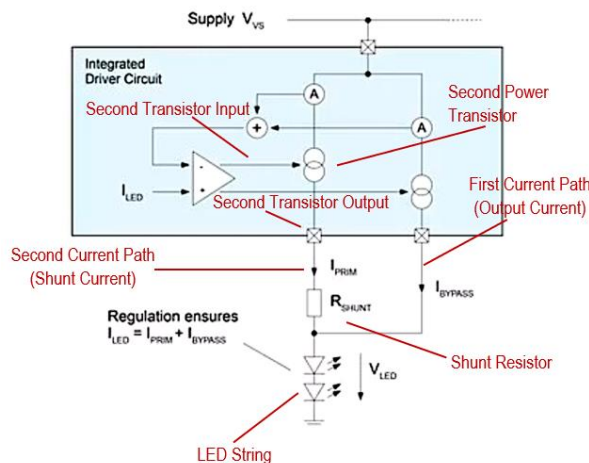
[Grounds 2-5] In addition to Sudhaus, and alternatively, Ryoichi discloses, in Fig. 5, driving transistor 6. Ex1006, Fig. 5.



RYOICHI FIG. 5

Ryoichi shows a current source including a first transistor 6 having an input and an output and driven by amplifier output stage (transistors 35 and 36b). Ex. 1006, Fig. 5. It would have been obvious to POSITA to include the transistor 6 in the current source IS_4 of Sudhaus.

[Grounds 3-5] In addition to Sudhaus and Ryoichi, Praxis discloses error amplifiers having a second output to control a current source coupled with a shunt resistor R_shunt. Ex1008, page 3, Section titled “Modern linear regulators with a power distribution,” lines 5-14; and Fig. 1.



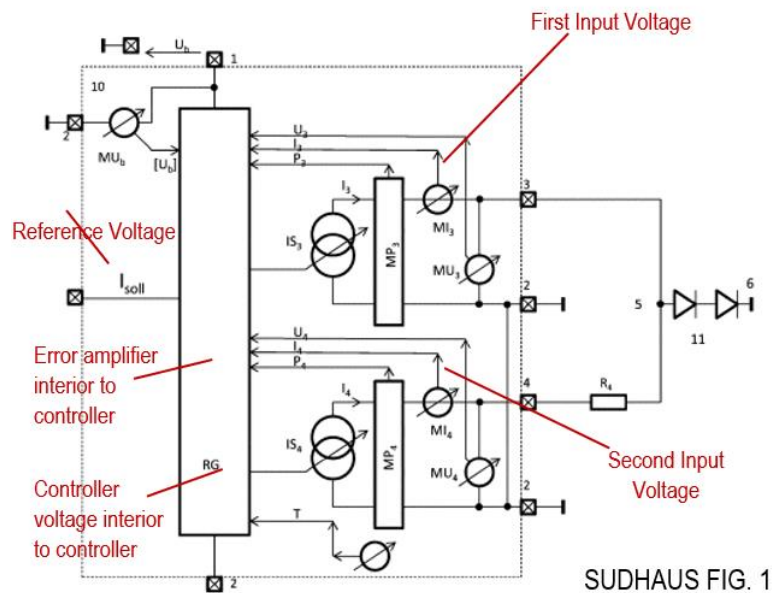
PRAXIS FIG. 1

[16.3] an error amplifier, comprising a first input to receive an

[Grounds 1-5] Sudhaus discloses control circuits to control two outputs supplying current to consumers (loads). Ex1005, 2:32-33. Sudhaus’s controller is operative to control the total of two currents based on desired value

input voltage, a second input to receive a reference voltage, and an output to provide a control voltage; and

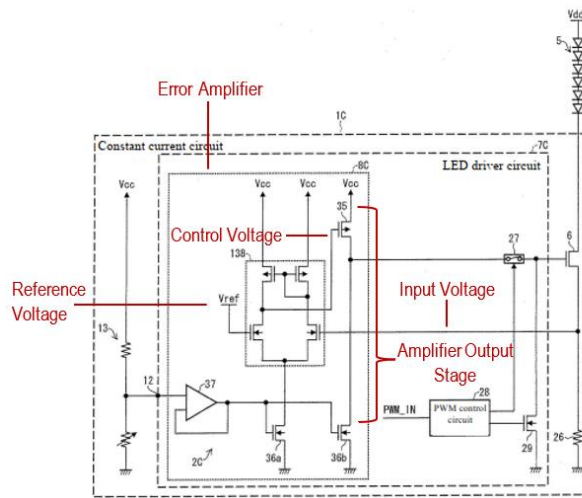
I_{soll} . Ex1005, 4:46-50.



Sudhaus' controller may be implemented with analog or digital circuits. Ex1005, 8:47-55.

Sudhaus' controller_RG receives first and second input voltages (combined to form input voltage), and further receives a reference voltage I_{soll} . Based on these signals, controller RG generates a necessary correction (control voltage) used to generate signals to control currents IS_3 and IS_4 . Ex1005, 4:25-28, Fig. 1.

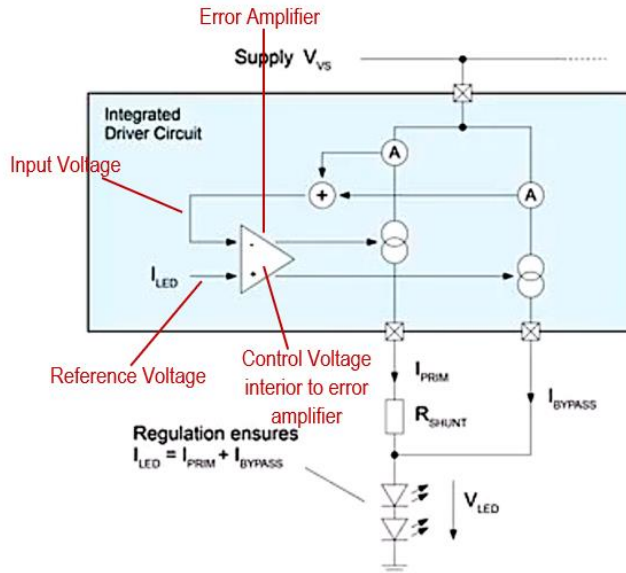
[Grounds 2-5] In addition to Sudhaus, and alternatively, Ryoichi discloses operational amplifier 8C. Ex1006, Fig.5, [0019].



RYOICHI FIG. 5

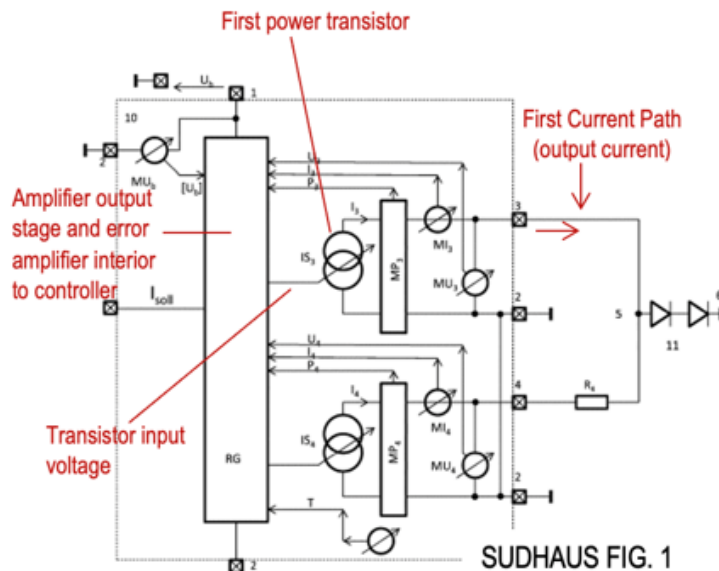
Ryoichi shows: operational amplifier 8C includes a differential part 138 and amplifier output stage consisting of transistors 35/36b. Ex1006, Fig. 5. The differential part receives an input voltage and a reference voltage and generates an output (control voltage). Ex1006, ¶ [0083].

[Grounds 3–5] In addition to Sudhaus and Ryoichi, and alternatively, Praxis discloses error amplifiers having two outputs to control two current sources providing current to LED load. Ex1008, page 3, Section titled “Modern linear regulators with a power distribution,” lines 7-14; and Fig. 1. Error amplifier has first input to receive input voltage and second input to receive reference voltage. The error amplifier generates an internal signal (control voltage) based on the inputs provides first and second outputs to control first and second current sources based on the internal signal.

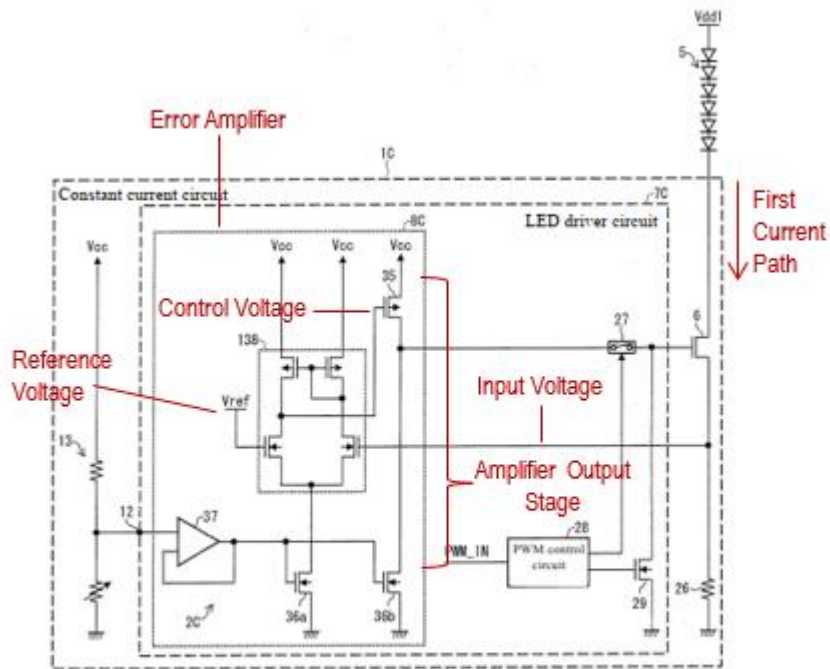


[16.4] an amplifier output stage comprising an input coupled to the output of the error amplifier, a first output coupled to the input of the first power transistor,

[Ground 1–5] Sudhaus discloses controller_RG operative to control two currents based on desired value I_{soll} . Ex. 1005, 4:46-50, Fig. 1. Sudhaus controller_RG includes a first output coupled to the input of IS_3 (the first power transistor). The first output of controller_RG is controllable internally via the controller_RG input. Ex1005, 4:25-28, Fig. 1.



[Grounds 2-5] In addition to Sudhaus, and alternatively, Ryoichi discloses operational amplifier 8C. Ex1006 ¶ [0019] FIG 5.

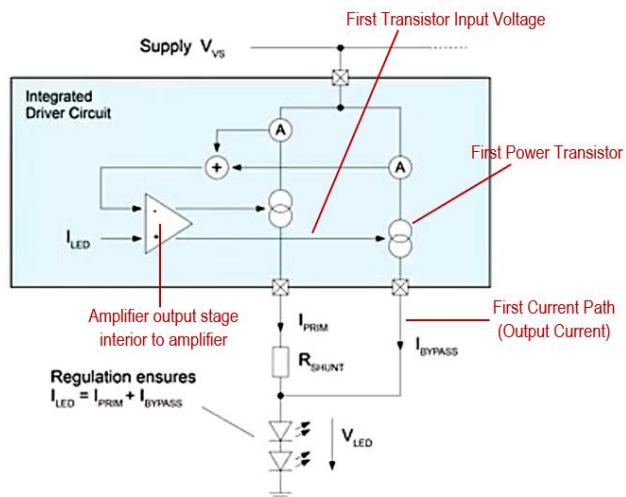


RYOICHI FIG. 5

Ryoichi shows: operational amplifier 8C includes amplifier output stages consisting of transistors 35 and 36b. The input of transistor 35 is coupled to the output of differential part 138 (control voltage). The output of transistor 35 is coupled to the input of power transistor 6. Ex1006, Fig. 5, [0083].

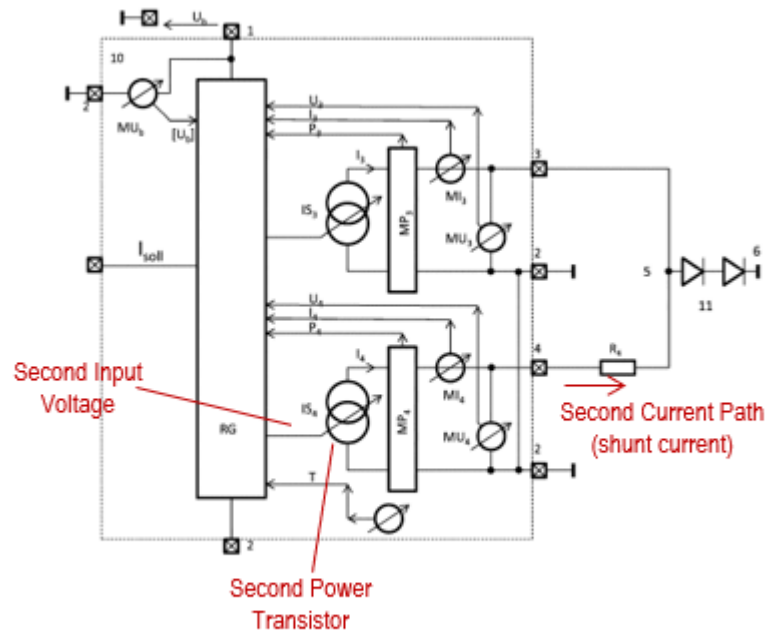
[Grounds 3-5] Additionally (and alternatively) to Sudhaus/Ryoichi, Praxis discloses error amplifiers having two outputs to control two current sources providing current to an LED load. Ex1008, page 3, Section titled “Modern linear regulators with a power distribution,” lines 7-14; and Fig. 1. Praxis’ error amplifier includes a first output (amplifier output stage) coupled to an input of the first current source. It would have been obvious to POSITA to include the amplifier structure of Ryoichi in the error amplifier of Praxis, such that an input of the

output stage is driven by the differential stage.



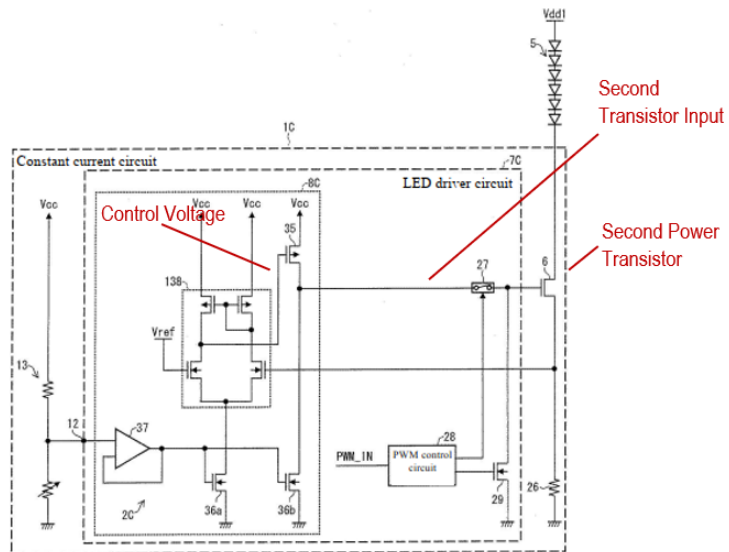
[16.5] and a second output coupled to the input of the second power transistor,

[Grounds 1–5] Sudhaus discloses a controller RG operative to control total of two currents based on desired value I_{soll} . Ex1005, 4:46-50, Fig. 1. The controller RG includes a second output 4 coupled to the input of IS_4 (the second power transistor). The second output of the controller RG is controlled internally to the controller RG. Ex1005, 4:25-28, Fig. 1.



SUDHAUS FIG. 1

[Grounds 2–5] Ryoichi discloses operational amplifier 8C.

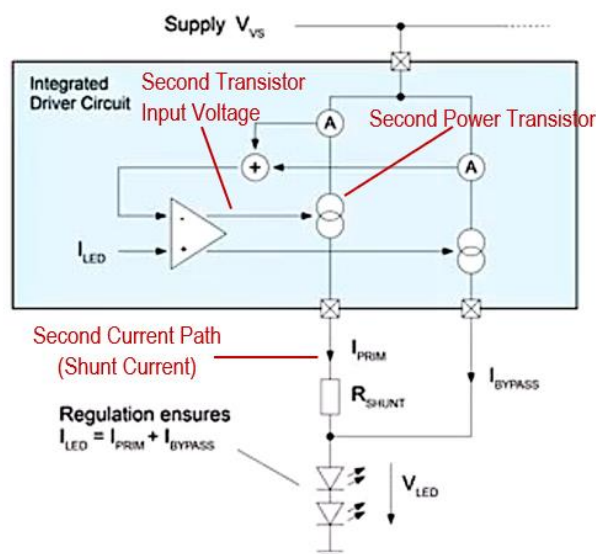


RYOICHI FIG. 5

Including an amplifier output stage (transistors 35 and 36b). Ex1006, Fig. 5. The input of transistor 35 is coupled to the output of differential part 138 (control voltage). The output of transistor 35 is coupled to the input of power transistor 6. Ryoichi Fig. 5, [0083]. It would have been

obvious to POSITA to include the differential amplifier and amplifier output structure of Ryoichi to control the second output (output 4) of Sudhaus to control IS_4. Ex1006 ¶ [0019].

[Grounds 3-5] Additionally (and alternatively) to Sudhaus/Ryoichi, Praxis discloses error amplifiers having two outputs to control two current sources providing current to an LED load. Ex1008, page 3, Section titled “Modern linear regulators with a power distribution,” lines 7-14; and Fig. 1. The error amplifier includes a second output (amplifier output stage) coupled to an input of the second current source. It would have been obvious to POSITA to include the amplifier structure of Ryoichi in the error amplifier of Praxis, such that an input of the output stage is driven by the differential stage.

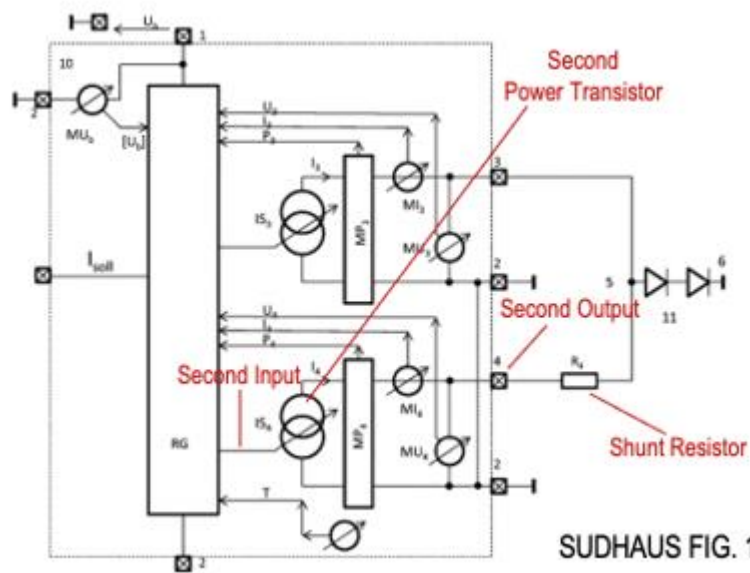


PRAXIS FIG. 1

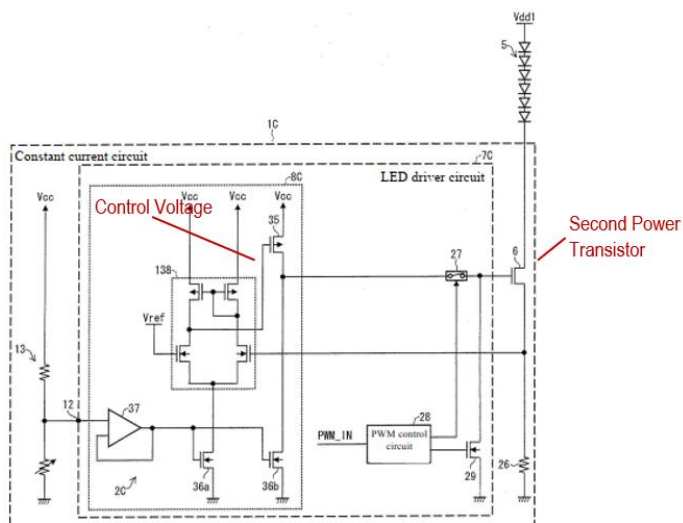
[16.6] the amplifier output stage comprising a slew-rate controller, the slew rate controller comprising an output coupled to

[Grounds 1-5] Sudhaus includes a slew rate controller for the second power transistor as described in reference to Claim 1, recitation [1.3]. Sudhaus Fig. 1 shows output 4 of the controller RG connected to the input (power transistor IS_4). Ex. 1005, 4:25-28, Fig. 1.

the input of the second power transistor.



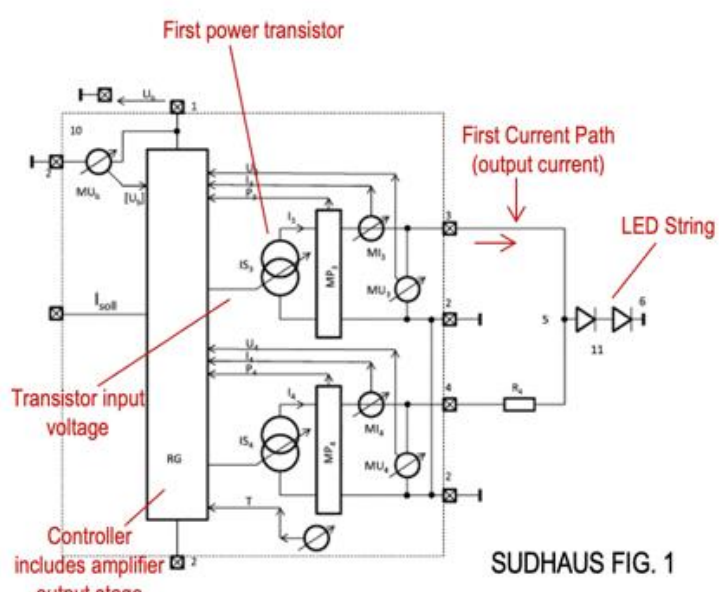
[Grounds 2-5] Additionally (and alternatively) to Sudhaus, Ryoichi includes slew rate control as described in reference to Claim 1, recitation [1.3]. The slew rate control is included in the operational amplifier 8C. Ex1006, ¶¶ [0083]-[0085]. Ryoichi Fig. 5 shows the output of operational amplifier 8C coupled to the input of power transistor 6.

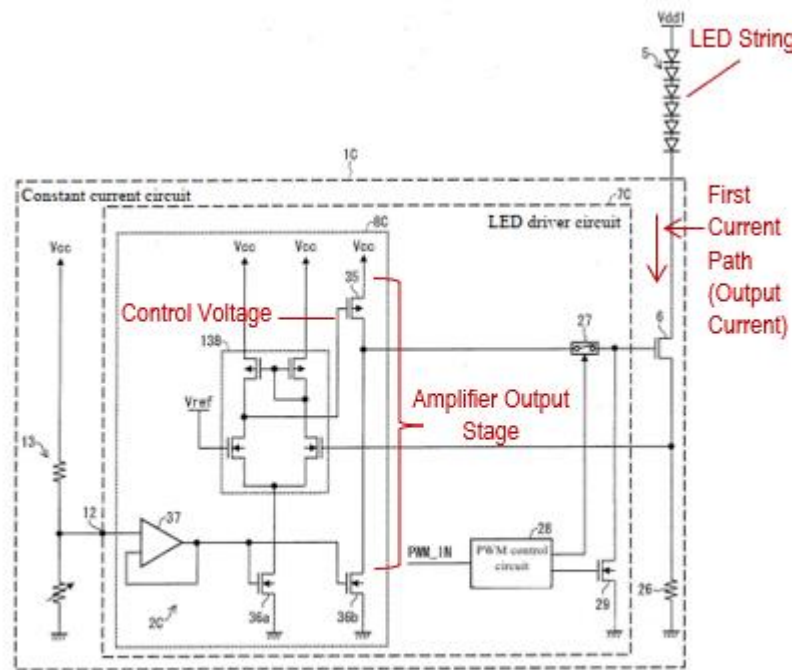


[Ground 4] Additionally (and alternatively) to Sudhaus,

	Ryoichi, Wu discloses a slew rate controller, as described in reference to Claim 1, Supra [1.3]. [Ground 5] Additionally (and alternatively) to Sudhaus, Ryoichi, and Wu, the combination of Provost, TI Paper and UK Paper discloses a slew rate controller, Supra Claim 5.
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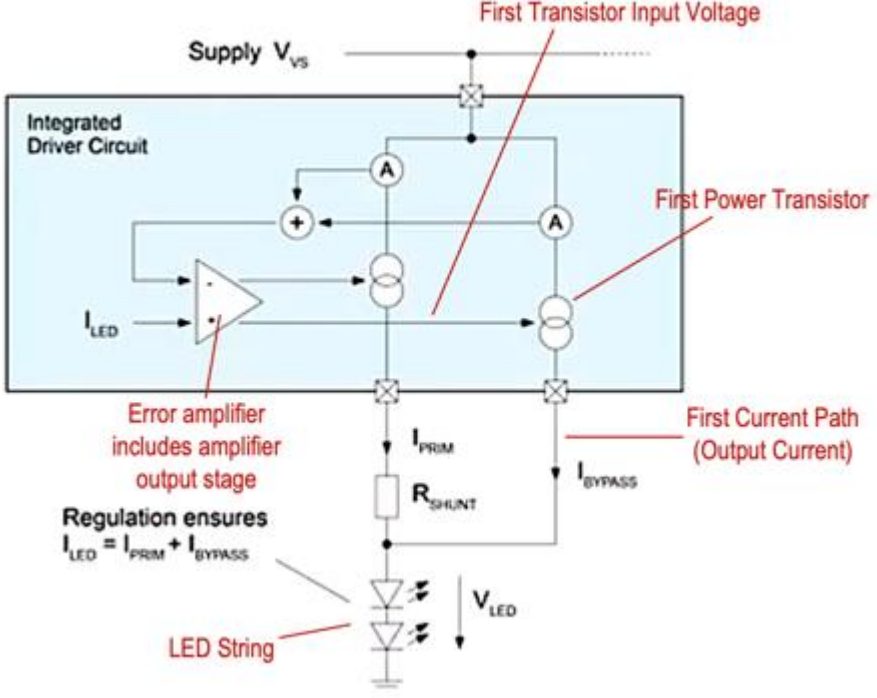
Q. Claim 17 is unpatentable under Grounds 1-5

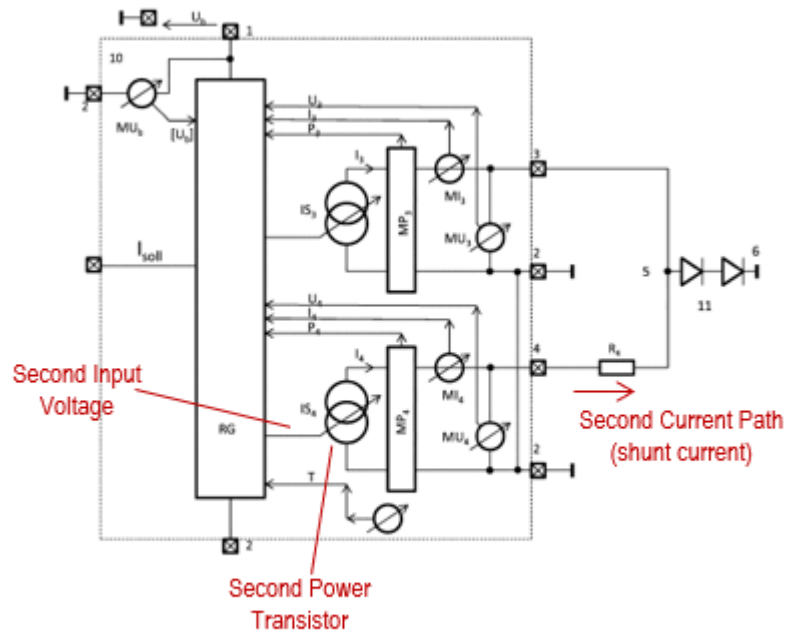
<u>Claim 17</u>	<u>Grounds</u>
[17.1] The system of claim 16, wherein the amplifier output stage is configured to control an amplitude of an output current through a first current path that includes the LED string and	[Grounds 1–5] Sudhaus, FIG 1, shows controller_RG outputs a signal to control current from current source IS_3 (output current). Ex1005, 4:25-28, Fig. 1. The first output of controller_RG is applied to first current source IS_3 and controls amplitude of current through first current path to LED string 11.  The diagram shows a circuit with a controller block labeled 'RG' (labeled 'Controller includes amplifier output stage' in red). The controller has two outputs. One output is connected to a current source 'IS_3' (labeled 'First power transistor' in red). The other output is connected to a transistor 'MP_3' (labeled 'First Current Path (output current)' in red). The transistor 'MP_3' is connected to a resistor 'R_4' (labeled 'LED String' in red). The current source 'IS_3' is also connected to the resistor 'R_4'. The circuit is powered by a supply 'U_1' and ground. Various other components like 'MU_1', 'MU_2', 'MU_3', 'MU_4', 'MU_5', 'MU_6', 'MU_7', 'MU_8', 'MU_9', 'MU_10', 'MU_11', 'MU_12', 'MU_13', 'MU_14', 'MU_15', 'MU_16', 'MU_17', 'MU_18', 'MU_19', 'MU_20' are shown. The diagram is labeled 'SUDHAUS FIG. 1'. [Ground 2–5] Additionally (and alternatively) to Sudhaus, Ryoichi shows: amplifier output stages (transistors 35/36b) control first current path (transistor 6/resistor 26), providing current to LED load 5. Ex1006, Fig. 5.



RYOICHI FIG. 5

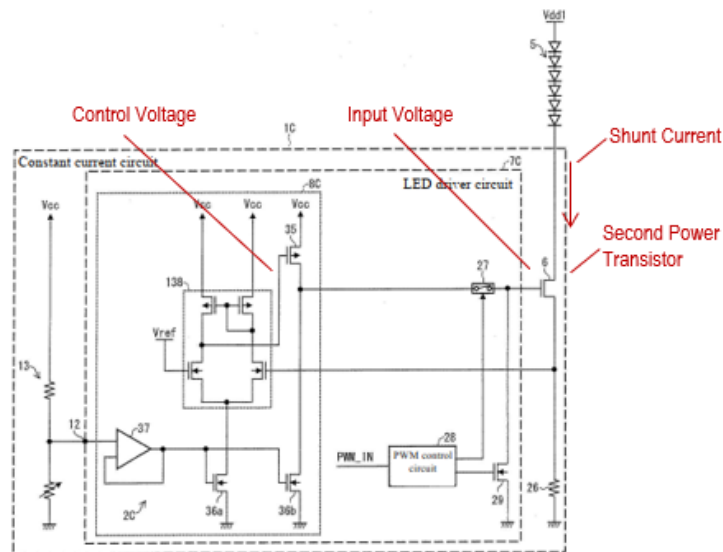
[Grounds 3–5] Additionally (and alternatively) to Sudhaus, Ryoichi, Praxis discloses error amplifiers having two outputs to control two current sources providing current to LED load. Ex1008, page 3, Section titled “Modern linear regulators with a power distribution,” lines 7-14; and Fig. 1. Error amplifier is configured to control output current through first current path that includes LED string.

	 PRAXIS FIG. 1
[17.2] a shunt current through a second current path that includes the shunt resistor based on the control voltage.	[Grounds 1-5] [17.2] is equivalent to [1.2] with the addition that the second current path includes a shunt resistor. Sudhaus shows a second current path including a shunt resistor. Ex1005, 4:46-50, Fig. 1.



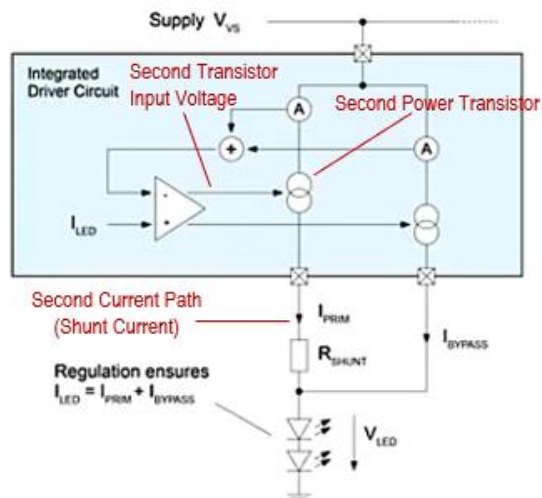
SUDHAUS FIG. 1

[Grounds 2–5] This recitation is the same as recitation [1.2] with the addition that this recitation includes that the second current path includes the shunt resistor. It would have been obvious to POSITA to include the amplifier 8C of Fig. 5 of Ryoichi in the controller of Sudhaus to control the current through the second current path as shown in Sudhaus above. Ex1006, ¶ [0083], Fig. 5.



RYOICHI FIG. 5

[Ground 3-5] This recitation is the same as recitation [1.2] with the addition that the second current path includes the shunt resistor. Praxis Fig. 1 shows that the second current path includes the shunt resistor.



PRAXIS FIG. 1

R. Claim 18 is unpatentable under Grounds 2-5

Claim 18	<u>Grounds</u>
[18] The system of claim 17, wherein the slew-rate controller comprises a charging capacitor having a capacitance that defines the slew-rate of the shunt current.	Claim 18 is equivalent to Claim 7.

S. Claim 19 is unpatentable under Ground 5.

Claim 19	<u>Ground</u>
[19.1] The system of claim 18, further comprising a power transistor configured to conduct the shunt current in the second current path based on a transistor input voltage,	Claim 19 elements are equivalent to Claim 8 elements, e.g. Supra[8.1].
[19.2] wherein the charging capacitor is configured to generate a charging voltage to control an amplitude of an offset current via a current mirror,	Supra [8.2].
[19.3] wherein the offset current is	Supra [8.3].

configured to control the transistor input voltage.	
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T. Claim 20 is unpatentable under Ground 5.

<u>Claim 20</u>	<u>Grounds</u>
[20.1] The system of claim 19, wherein the amplifier output stage comprises a control transistor that is controlled by the control voltage,	Claim 20 elements are equivalent to Claim 9 elements, e.g. Supra [9.1].
[20.2] wherein the control transistor is coupled to an input of the power transistor to set an initial amplitude of the transistor input voltage,	Supra [9.2].
[20.3] wherein the offset current is subtracted from the initial amplitude to control the power transistor based on the slew-rate.	Supra [9.3].

XI. Conclusion.

For the reasons provided above, *inter partes* review of Claims 1-20 is requested.

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Respectfully submitted,

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APPENDIX A- LISTING OF CHALLENGED CLAIMS

CLAIM	LIMITATION
1.pre	A light-emitting diode (LED) driver system comprising:
1.1	an error amplifier configured to compare an input voltage with a reference voltage to generate a control voltage; and an amplifier output stage configured to control an output current through a first current path
1.2	and a shunt current through a second current path based on the control voltage,
1.3	the amplifier output stage comprising a slew-rate controller configured to control a slew-rate of a shunt current,
1.4	the shunt current provided through a shunt resistor in the second current path and added to the output current to provide a total current through an LED string.
2.1	The system of claim 1, further comprising: a first power transistor configured to conduct the output current in the first current path based on a first transistor input voltage; and
2.2	a second power transistor configured to conduct the shunt current in the second current path based on a second transistor input voltage.
3.1	The system of claim 2, wherein the amplifier output stage comprises: a first control transistor configured to conduct a first control current based on the control voltage to generate the first transistor input voltage; and
3.2	a second control transistor configured to conduct a second control current based on the control voltage to generate the second transistor input voltage.
4.1	The system of claim 4, wherein the slew-rate controller is configured to conduct an offset current in parallel with the second control current to generate the second transistor input voltage,
4.2	the offset current increasing at the slew rate.
5.1	The system of claim 4, wherein the slew-rate controller comprises: a charging current generator configured to generate a charging current;
5.2	a charging capacitor that is charged by a charging current to generate a charging voltage;
5.3	a current mirror configured to conduct the offset current based on the charging voltage.
6	The system of claim 1, wherein the amplifier output stage is configured to increase an amplitude of the shunt current and decrease an amplitude of the output current as the supply voltage increases.
7	The system of claim 1, wherein the slew-rate controller comprises a charging capacitor having a capacitance that defines the slew-rate of the shunt current.

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8.1	The system of claim 7, further comprising a power transistor configured to conduct the shunt current in the second current path based on a transistor input voltage,
8.2	wherein the charging capacitor is configured to generate a charging voltage to control an amplitude of an offset current via a current mirror,
8.3	wherein the offset current is configured to control the transistor input voltage.
9.1	The system of claim 8, wherein the amplifier output stage comprises a control transistor that is controlled by the control voltage,
9.2	wherein the control transistor is coupled to an input of the power transistor to set an initial amplitude of the transistor input voltage,
9.3	wherein the offset current is subtracted from the initial amplitude to control the power transistor based on the slew-rate.
10	An integrated circuit (IC) chip comprising the LED driver system of claim 1.
11[pre]	A light-emitting diode (LED) system comprising:
11.1	an error amplifier configured to compare an input voltage with a reference voltage to generate a control voltage; and
11.2	an amplifier output stage configured to control an output current through a first current path and a shunt current through a second current path based on the control voltage,
11.3	the amplifier output stage comprising a slew-rate controller configured to control a slew-rate of the shunt current;
11.4	a shunt resistor in the second current path to conduct the shunt current; and
11.5	an LED string arranged at an output of the first current path and the second current path to illuminate in response to a total current comprising a sum of the output current and the shunt current.
12	The system of claim 11, wherein the slew-rate controller comprises a charging capacitor having a capacitance that defines the slew-rate of the shunt current.
13.1	The system of claim 12, further comprising a power transistor configured to conduct the shunt current in the second current path based on a transistor input voltage,
13.2	wherein the charging capacitor is configured to generate a charging voltage to control an amplitude of an offset current via a current mirror,
13.3	wherein the offset current is configured to control the transistor input voltage.
14.1	The system of claim 13, wherein the amplifier output stage comprises a control transistor that is controlled by the control voltage,
14.2	wherein the control transistor is coupled to an input of the power transistor to set an initial amplitude of the transistor input voltage,

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14.3	wherein the offset current is subtracted from the initial amplitude to control the power transistor based on the slew-rate.
15.1	The system of claim 11, further comprising: a first power transistor configured to conduct the output current in the first current path based on a first transistor input voltage; and
15.2	a second power transistor configured to conduct the shunt current in the second current path based on a second transistor input voltage;
15.3	wherein the amplifier output stage comprises: a first control transistor configured to conduct a first control current based on the control voltage to generate the first transistor input voltage; and
15.4	a second control transistor configured to conduct a second control current based on the control voltage to generate the second transistor input voltage,
15.5	wherein the slew-rate controller is configured to conduct an offset current in parallel with the second control current to generate the second transistor input voltage,
15.6	the offset current increasing at the slew-rate.
16.pre	A light-emitting diode (LED) driver system comprising:
16.1	a first power transistor comprising an input and an output coupled to an LED string and a shunt resistor;
16.2	a second power transistor comprising an input and an output coupled to the shunt resistor;
16.3	an error amplifier comprising a first input to receive an input voltage, a second input to receive a reference voltage, and an output to provide a control voltage; and
16.4	an amplifier output stage comprising an input coupled to the output of the error amplifier, a first output coupled to the input of the first power transistor, and
16.5	a second output coupled to the input of the second power transistor,
16.6	the amplifier output stage comprising a slew-rate controller, the slew-rate controller comprising an output coupled to the input of the second power transistor.
17.1	The system of claim 16, wherein the amplifier output stage is configured to control an amplitude of an output current through a first current path that includes the LED string and
17.2	and a shunt current through a second current path that includes the shunt resistor based on the control voltage.
18	The system of claim 17, wherein the slew-rate controller comprises a charging capacitor having a capacitance that defines the slew-rate of the shunt current.
19.1	The system of claim 18, further comprising a power transistor configured to conduct the shunt current in the second current path based on a transistor

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	input voltage,
19.2	wherein the charging capacitor is configured to generate a charging voltage to control an amplitude of an offset current via a current mirror,
19.3	wherein the offset current is configured to control the transistor input voltage.
20.1	The system of claim 19, wherein the amplifier output stage comprises a control transistor that is controlled by the control voltage,
20.2	wherein the control transistor is coupled to an input of the power transistor to set an initial amplitude of the transistor input voltage,
20.3	wherein the offset current is subtracted from the initial amplitude to control the power transistor based on the slew-rate.

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CERTIFICATION OF SERVICE (37 C.F.R. §§ 42.6(e))

The undersigned hereby certifies that on April 24, 2024, true and correct copies of the foregoing **PETITION FOR *Inter Partes* Review of U.S. Patent NO. 11,653,432**, the accompanying Power of Attorney, and all associated exhibits were served in their entirety on the following parties via U.S.P.S. Priority Express:

Correspondence Address:	Texas Instruments Incorporated Attention: Cynthia Hoff Trochu Senior Vice President, Secretary and General Counsel P.O. Box 660199, Dallas, Texas 75266-0199;
Correspondence Address:	Texas Instruments Incorporated Attention: Frank Cimino P.O. Box 655474, M/S 3999 Dallas, Texas 75265-5474

via U.S.P.S. Priority Mail Express:

Respectfully submitted,

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Date: April 24, 2024

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**CERTIFICATE OF COMPLIANCE WITH TYPE-VOLUME LIMITATION,
TYPEFACE REQUIREMENTS, AND TYPE STYLE REQUIREMENTS**

1. This Petition complies with the type-volume limitation of 14,000 words, comprising 13,188 words, excluding the parts exempted by 37 C.F.R. § 42.24(a).

2. This Petition complies with the general format requirements of 37 C.F.R. § 42.6(a) and has been prepared using Microsoft® Word 365 in 14-point Times New Roman.

Respectfully submitted,

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