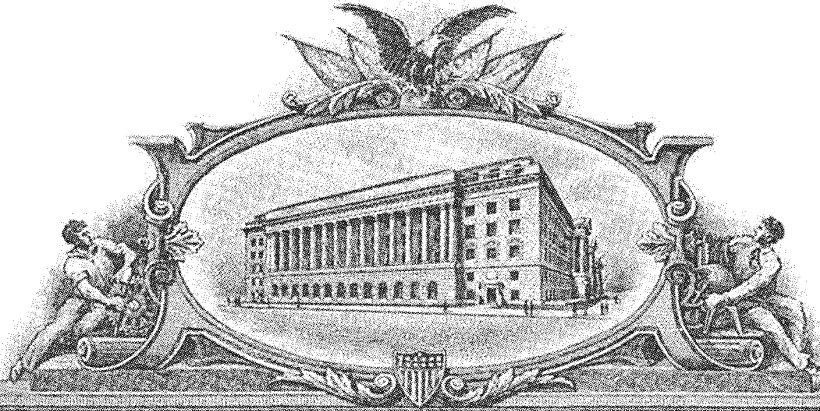


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**PATENT
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SMSC**

Pad ESD Spreading Technique

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BACKGROUND OF THE INVENTION

Field of the Invention

[0001] This invention relates generally to the field of integrated circuit design and, more particularly, to the design of protection circuitry for providing protection against damaging effects of Electrostatic Discharge (ESD).

Description of the Related Art

[0002] Integrated circuits (ICs) are typically manufactured with external connections - most commonly pins - for coupling to external devices, systems, signals and/or power supply voltages. More recently, IC design and manufacturing has been trending towards an increase in the density of internal components, most commonly transistors and device interconnects, with a concurrent decrease in the power supply voltage levels used in operating the ICs. As IC devices increase in density and operating supply voltage levels decrease, the IC devices may become more sensitive to the effects of electrostatic discharge (ESD).

[0003] ESD many times originates from build up of static charge near the IC or on a human handling the IC, leading to extremely high voltages developed near the IC, and typically results in an electrical discharge of very high current for a short duration. Therefore, ESD poses a serious problem for semiconductor devices as it can potentially lead to malfunction and/or the destruction of an entire IC. In addition, the physical dimensions of circuit elements in many ICs, for example in microprocessors, have seen a decrease with each new generation of manufacturing process. Although smaller dimensions lead to an increase in IC operating speeds, they also have an adverse impact by increasing the sensitivity of circuit elements, such as field effect transistors (FETs), to high electric fields. One technique employed in overcoming this increased sensitivity has been to reduce the operating voltage of an IC. However, as supply voltages are scaled down (from 5.0 volts, to 3.3 volts, to 2.5, to 1.8 volts, for example), there is typically a need to maintain backward compatibility with the higher voltage requirements of older ICs.

[0004] In order to maintain compatibility with previous generations of semiconductor products and devices, it has been necessary to provide ICs with interface circuits that are interoperable with older generation ICs requiring higher supply voltages. One result of this has been the practice of designing ICs having a core operated using a first power supply voltage, and Input/Output (I/O) circuitry, typically around the physical periphery of the IC, operated using a higher power supply voltage. Since ESD events often occur across the silicon circuits attached to the package terminals, or pins, of an IC, circuit designers have concentrated their efforts on developing adequate protection mechanisms for these sensitive circuits. Often the design of ESD protection circuits has to satisfy high performance requirements. For example, one of the primary industry standards for measuring ESD robustness (MIL-STD-883C method 3015.7 Notice 8 (1989), and the subsequent Human Body Model (HBM) standard No. 5.1 (1993) from the EOS/ESD Association) requires ESD zapping for what can be a large number of pin and power supply combinations.

[0005] Generally formulated, protection against effects of ESD requires sensing either a predetermined voltage level, or the fast rate of voltage change resulting from an ESD pulse that might affect an integrated circuit component or an entire chip. The pins that require the ESD protection must generally be tolerant to voltages above the highest voltage tolerance of the typical FETs used in the fabrication process. Trigger circuits that may be used to turn on a clamp in response to any incoming ESD pulse would therefore have to be high voltage tolerant. In the past, ESD protection circuits have had difficulty meeting these stringent requirements while maintaining adequate noise immunity and without increasing the required silicon area.

[0006] In general, various techniques for improving ESD performance, including the use of semiconductor controlled rectifiers (SCRs), snapback devices, and rail clamps, have been devised, published and/or patented.

[0007] Other corresponding issues related to the prior art will become apparent to one skilled in the art after comparing such prior art with the present invention as described herein.

SUMMARY OF THE INVENTION

[0009] In one set of embodiments, a robust electrostatic discharge (ESD) structure for a variety of digital input/output (I/O) pads may be achieved. Output PMOS devices comprised in the output buffer of the pad and coupled between an I/O pad supply rail and the output pad may be enabled in response to an ESD event, to charge a pad capacitance (which, in some cases, may be approximately 3pF) corresponding to the physical pad or pad cell, to spread out the energy generated by the ESD event, resulting in a lower peak voltage and therefore better ESD performance. By configuring all of the pads comprised within the system, (e.g. integrated circuit or part), to operate this way, the ESD energy may be shared by the respective pad capacitances corresponding to all the pads, thereby reducing the maximum voltage that may develop in the system as a result of the ESD event. This method may be employed as an additional technique to be used in conjunction with other established solutions, such as various clamp devices and clamp circuits, for example, allowing improved ESD performance over the established solutions used alone.

[0010] In one set of embodiments, an I/O pad circuit associated with a physical pad may comprise three main sections: an output buffer that may also include an ESD clamp device, a clamp control circuit, and a functional control block. The clamp control circuit may be supplied power by an ESD power rail that is activated by the energy of the ESD event, and may be triggered/enabled according to an RC time constant associated with a slope, or rise time, of a voltage pulse that may activate the ESD power rail. In an ESD event, the clamp control circuit may perform at least two different operations. It may turn on the clamp device in the output buffer, where the clamp device is coupled between the ESD power rail and a low supply rail, and may also send a signal to the functional control block, to instruct the functional control block to turn on the p-channel output device(s) – e.g. PMOS device(s) – comprised in the output buffer. By turning on the p-channel devices, while disabling n-channel devices – e.g. NMOS devices – that may also be comprised in the output buffer, and coupled to the PMOS device(s), the functional control block may operate to couple the high supply rail (i.e. the pad power rail) and its

associated capacitance (such as all the other pad cells) to the pad affected by the ESD event, thus charge sharing the ESD pulse, thereby reducing the maximum voltage developed in the part comprising the pads. The reduced voltage correlates to improved part reliability. This technique may be used in conjunction with other established solutions, such as clamp devices and active clamp circuits, allowing improved ESD performance over other established solutions being used alone.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] The foregoing, as well as other objects, features, and advantages of this invention may be more completely understood by reference to the following detailed description when read together with the accompanying drawings in which:

[0012] Fig. 1 shows the partial block diagram of one embodiment of a system in which pads have been configured to share a charge developed as a result of an electrostatic discharge (ESD) event, to reduce the maximum voltage developed in the system as a result of the ESD event; and

[0013] Fig. 2 shows a partial circuit diagram of one embodiment of a pad circuit configured to turn on PMOS devices in its output buffer to charge a corresponding pad capacitance to reduce the maximum voltage developed in the system as a result of the ESD event.

[0014] While the invention is susceptible to various modifications and alternative forms, specific embodiments thereof are shown by way of example in the drawings and will herein be described in detail. It should be understood, however, that the drawings and detailed description thereto are not intended to limit the invention to the particular form disclosed, but on the contrary, the intention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the present invention as defined by the appended claims. Note, the headings are for organizational purposes only and are not meant to be used to limit or interpret the description or claims. Furthermore, note that the word “may” is used throughout this application in a permissive sense (i.e., having the potential to, being able to), not a mandatory sense (i.e., must).” The term “include”, and derivations thereof, mean “including, but not limited to”. The term “coupled” means “directly or indirectly connected”.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0015] In one set of embodiments, a more robust electrostatic discharge (ESD) structure for a variety of variable input/output (I/O) pads may be realized. In one set of embodiments, output PMOS devices comprised in the output buffer of a pad, for example a digital I/O pad, may be enabled in response to an ESD event, to charge a pad capacitance (which may be approximately 3pF) corresponding to the physical pad or pad cell, to spread out the ESD energy, which may result in a lower peak voltage and therefore better ESD performance. By configuring all of the pads comprised within the system, or integrated circuit, to operate this way, the ESD energy may be shared by the respective pad capacitances corresponding to all the pads, thereby reducing the maximum voltage that may develop in the system as a result of the ESD event (or of the energy of the ESD event). This method may be employed as an additional technique to be used in conjunction with other established solutions, such as various clamp devices and clamp circuits, for example, allowing improved ESD performance over the established solutions used alone.

[0016] Fig. 1 shows the partial block diagram of pads comprised in a system 100, for example an integrated circuit, and configured to share a charge developed as a result of an electrostatic discharge (ESD) event, to reduce the maximum voltage developed in the system as a result of the ESD event. Each pad may comprise a physical pad (114a and 114b) and a corresponding pad circuit (102a and 102b, respectively). Each physical pad may have an associated pad capacitance, shown in Fig. 1 only for pad 114b, where capacitor 120 symbolizes the pad capacitance associated with pad 114b. The pads may be coupled between an I/O supply/voltage pad rail (VDDIO) 122, which may be a variable I/O pad rail in some embodiments, and low supply/voltage (VSSIO) rail 124, where VSSIO rail 124 has a lower value than VDDIO rail 124. Pad circuit 102a may be configured such that in case of an ESD event 126 affecting pad 114a, pad circuit 102a may turn on PMOS devices 110a in response to the energy of the ESD event, while keeping NMOS devices 112a and 112b turned off, resulting in charge flowing from pad 114a to pad capacitance 120 through PMOS devices 110a and 110b. Although only two

pads are shown in Fig. 1, any and all pads similarly configured between VDDIO rail 122 and VSSIO rail 124 may have their respective PMOS devices turned on (including pad circuit 102a), resulting in the charge being shared across all pads (pads 114a and 114b shown in Fig. 1), that is, across the respective pad capacitances associated with all the pads. This may effectively reduce the maximum, or peak, voltage developed in the circuit, or system, as a result of ESD event 126.

[0017] Fig. 2 shows a partial circuit diagram of one embodiment of a pad circuit 102 (which may be an embodiment of pad circuit 102a and/or 102b, for example) configured to turn on PMOS devices 110 in its output buffer 206 to charge a corresponding pad capacitance to reduce the maximum voltage developed in the system as a result of ESD event 126. It should be noted that the terms “buffer” and “output buffer” are used herein in the context of electrical and/or integrated circuits to denote signal driver circuits, as opposed to a programming/data transmission context, where the terms are commonly used to denote data structures or memory elements used to hold data/and or information. In pad circuit 102, PMOS device 110 represents one or more PMOS devices coupled between VDDIO rail 122 and PAD 114. In case of multiple PMOS devices 110, the PMOS devices may be coupled in parallel, that is, their respective drain terminals coupled together and their respective source terminals coupled together. Control block 202 may contain logic circuitry to perform various functions associated with pad circuit 102, for example receiving I/O data, address information, and various system control signals 201 in order to perform I/O functions for the system. It should be noted that control block 202 may contain digital, analog, and/or mixed-mode circuitry configured to perform the various functions assigned to control block 202 as set forth herein and further described below. Those skilled in the art will appreciate that control block 202 may be implemented in a variety of ways to achieve the functionality of control block 202 as set forth herein, and the embodiment shown in Fig. 2 is meant to be exemplary and in no way limiting.

[0018] One of the functions that may be performed by control block 202 is the control of output buffer 206 to drive an output signal at pad 114. In one embodiment, control block 202 uses control signal 234 (which may be a control signal bus comprising multiple signal lines in case of multiple PMOS devices) to control the gate (or gates) of PMOS

device(s) 110 to enable/disable PMOS device(s) 110. Similarly, control block 202 may use control signal(s) 236 to control the gate of NMOS device(s) 212b to enable/disable NMOS device(s) 212b. NMOS device(s) 212b may be coupled between PAD 114 and VSSIO rail 124, operating together with PMOS device(s) 110 to drive the output signal at PAD 114 as per the function of output buffer 206. An internal high supply rail VDDCR 242 may be configured to provide power to various functional blocks within the system, including at least a portion of the circuitry inside control block 202, and in addition to enabling NMOS device 212a. Pad circuit 102 may also include a supply rail (VIOESD) 244 used to power up clamp control circuit 204. In one embodiment, clamp control circuit 204 comprises inverters 220 and 222 coupled in series, and is operable to provide an ESD control signal 230 to control block 202. ESD control signal 230 may be asserted in response to the ESD event to instruct control block 202 to turn on PMOS devices 110.

[0019] When an ESD event occurs, the fast ramp rate of a voltage spike on VIOESD rail 244 may result in VIOESD rail 244 providing increased power to clamp control circuit 204, thereby facilitating clamp control circuit 204 asserting ESD control signal 230. Based on the asserted ESD control signal 230, clamp control circuit 204 may also turn on clamp device 214 configured to shunt VIOESD rail 244 and VISSIO rail 124, thereby absorbing at least a portion of the energy generated by the ESD event. Those skilled in the art will appreciate that while the clamp device shown in Fig. 2 is a PMOS device, in alternate embodiments clamp device 214 may be an NMOS device or any other device configurable to absorb at least a portion of the energy generated by the ESD event, and clamp device 214 is not limited to the use of a PMOS device. Clamp control circuit 204 may also include capacitor 216 configured to aid in turning on clamp device 214. As mentioned above, in response to being powered by the ESD event, clamp control circuit 204 may assert ESD control signal 230 to instruct control block 202 to enable PMOS device(s) 110, while disabling or keeping disabled NMOS device(s) 212b. By enabling (i.e. turning on) PMOS device(s) 110, control block 202 effectively connects VDDIO rail 122 and its associated capacitance (which may comprise all the other pads or pad cells) to the physical pad affected by the ESD event, thereby sharing the charge generated by the ESD event, reducing the maximum voltage developed in the system as the result of the ESD event. The reduced maximum voltage correlates to improved part reliability.

[0020] In one embodiment, clamp control circuit 204 may also be configured to receive a control signal (RC) 240. RC signal 240 may correspond to an RC time constant, and may serve as a trigger (enable) signal to clamp control circuit 204. In case there is a power surge on VIOESD rail 244 resulting from normal operation, for example from powering up the system/part, which may not have the harmful effects of an ESD pulse, RC signal 240 may operate to keep clamp control circuit 204 disabled even if VIOESD rail 244 provides enough power to clamp control circuit 204 for clamp control circuit 204 to assert ESD control signal 230. Thus, the RC time constant to which RC signal 240 corresponds may correlate to a specified slope of an energy pulse that may result in VIOESD rail 244 providing enough power to clamp control circuit 204 for clamp control circuit 204 to enable ESD control signal 230. Generally, an ESD event generates a voltage spike having a steep slope, in which case RC signal 240 would operate to enable clamp control circuit 204, while a lower slope present during a routine powering up of the system/part would result in RC signal 240 keeping clamp control circuit 204 disabled. It should also be noted that VIOESD 244 and VDDIO 122 may in fact be the same power/supply rail, and alternate embodiments may be configured with a single power rail providing power to the circuit and/or system components that are powered by VIOESD 244 and VDDIO 122 in the embodiment shown in Fig. 2. In general, the ESD rail and the power supply rail can be the same supply rail, and separate supply rails (e.g. VIOESD 244 and a distinct VDDIO 122) may not be required.

[0021] In one set of embodiments, a system, e.g. an integrated circuit or part, may include a plurality of physical pads and associated pad circuits (e.g. pad circuit 102) together operating as digital I/O pads. In case of an ESD event affecting one or more of the digital I/O pads, the PMOS devices configured between the I/O supply rail and the output pad –within their respective pad circuits in the affected digital I/O pads – may all be turned on. This may allow the capacitance of each pad, in some embodiments approximately 3pF capacitance per pad, to charge up, absorbing the energy of the ESD event and reducing the peak voltage the integrated circuit or part experiences as a result of the ESD event. The reduced peak voltage may be directly correlated with improved ESD performance of the product.

[0022] Further modifications and alternative embodiments of various aspects of the invention may be apparent to those skilled in the art in view of this description. Accordingly, this description is to be construed as illustrative only and is for the purpose of teaching those skilled in the art the general manner of carrying out the invention. It is to be understood that the forms of the invention shown and described herein are to be taken as embodiments. Elements and materials may be substituted for those illustrated and described herein, parts and processes may be reversed, and certain features of the invention may be utilized independently, all as would be apparent to one skilled in the art after having the benefit of this description of the invention. Changes may be made in the elements described herein without departing from the spirit and scope of the invention as described in the following claims.

We claim:

1. A pad circuit configured to provide protection against electrostatic discharge (ESD) in a system comprising the pad circuit, the pad circuit comprising:

a first node coupled to a first voltage rail;

a second node coupled to a physical pad having capacitance;

one or more output transistor devices coupled between the first node and the second node, and operable to at least partially drive an output signal at the second node; and

a control block operable to turn on at least one of the one or more output transistor devices in response to an ESD event to charge the pad capacitance, thereby reducing a maximum voltage developed in the system as a result of the ESD event.

2. The pad circuit of claim 1, wherein in turning on the at least one of the one or more output transistor devices in response to the ESD event, the control block is further operable to couple the first voltage rail and its associated capacitance to the physical pad to share a charge developed in the system in response to the ESD event, thereby reducing the maximum voltage developed in the system as the result of the ESD event.

3. The pad circuit of claim 1, further comprising enable circuitry operable to send a control signal to the control block in response to the ESD event to instruct the control block to turn on the at least one of the one or more output transistor devices.

4. The pad circuit of claim 3, further comprising:

a clamp device coupled between a second voltage rail and a third voltage rail, wherein the second voltage rail is configured to provide power to the enable circuitry, and wherein the third voltage rail has a value below the first voltage rail;

wherein the enable circuitry is operable to turn on the clamp device to reduce the maximum voltage developed in the system as the result of the ESD event.

5. The pad circuit of claim 1, wherein the one or more output transistor devices are PMOS devices, wherein the at least one of the one or more transistor devices comprises:

a subset of the PMOS devices; or
the PMOS devices.

6. The pad circuit of claim 5, further comprising one or more NMOS devices coupled between the second node and a second voltage rail that has a value below the first voltage rail, wherein the NMOS devices and the PMOS devices are operable to operate together to drive the output signal at the second node, wherein the logic circuit is operable to have the NMOS devices turned off during the ESD event.

7. The pad circuit of claim 1, wherein the pad circuit and the physical pad are comprised in a digital input/output pad.

8. A method for protecting a system against electrostatic discharge (ESD), the method comprising:

turning on at least one of one or more output transistor devices in response to an ESD event to charge a pad capacitance, to thereby reduce a maximum voltage developed in the system as a result of the ESD event;

wherein the one or more output transistor devices are configured in the system, and are coupled to a physical pad having the pad capacitance, and wherein the one or more output transistor devices are operable to drive an output signal at the physical pad.

9. The method of claim 8, further comprising:

turning on a clamp device in response to the ESD event, wherein the clamp device is configured to absorb, when turned on, a portion of an energy generated by the ESD

event, to thereby reduce the maximum voltage developed in the system as the result of the ESD event.

10. The method of claim 8;
wherein the one or more transistor devices comprise one or more PMOS devices;
wherein said turning on the at least one of the one or more output transistor devices comprises:

turning on at least one of the one or more PMOS devices; or
turning on the one or more PMOS devices.

11. The method of claim 10;
wherein the one or more transistor devices further comprise one or more NMOS devices;
wherein the method further comprises disabling the one or more NMOS devices during the ESD event.

12. The method of claim 11, wherein the physical pad is an input/output pad.

13. A circuit configured to provide protection against electrostatic discharge (ESD) in a system comprising the circuit, the circuit comprising:
an output buffer configured to couple to a physical pad having capacitance, and operable to drive at least one output signal at the physical pad;
a control block configured to control the output buffer; and
a control circuit configured to instruct the control block to activate at least a portion of the output buffer when an ESD event occurs, thereby charging the pad capacitance to reduce a maximum voltage developed in the system as a result of the ESD event.

14. The circuit of claim 13, wherein the output buffer comprises:
one or more PMOS devices coupled between a first supply rail and the physical pad; and

one or more NMOS devices coupled between the physical pad and a second supply rail having a value less than the first supply rail;

wherein in activating at least a portion of the output buffer when the ESD event occurs, the control block is operable to:

enable at least one of the one or more PMOS devices; or
enable the one or more PMOS devices.

15. The circuit of claim 14, wherein in activating at least a portion of the output buffer when the ESD event occurs, the control block is operable to:

disable at least one of the one or more NMOS devices; or
disable the one or more NMOS devices.

16. The circuit of claim 14, wherein the one or more PMOS devices are coupled in parallel between the first supply rail and the physical pad, and the NMOS devices are coupled in series between the physical pad and the second supply rail.

17. The circuit of claim 13, further comprising a clamp device coupled between a first supply rail configured to provide power to the control circuit, and a low supply rail;

wherein the clamp device is configured to absorb, when turned on, a portion of an energy generated by the ESD event, to thereby reduce the maximum voltage developed in the system as the result of the ESD event;

wherein the control circuit is operable to turn on the clamp device in response to the ESD event.

18. The circuit of claim 17, wherein the clamp device is one of:

a PMOS device having its source terminal coupled to the first supply rail, its drain terminal coupled to the low supply rail, and its gate terminal coupled to the control circuit; or

an NMOS device having its drain terminal coupled to the first supply rail, its source terminal coupled to the low supply rail, and its gate terminal coupled the control circuit.

19. The circuit of claim 13, wherein the control circuit is configured to be powered by a first supply rail operable to provide increased power during the ESD event.

20. The control circuit of claim 13, wherein in instructing the control block to activate at least a portion of the output buffer when an ESD event occurs, the control circuit is operable to provide a control signal to the control block in response to the ESD event.

21. The circuit of claim 13, wherein the control circuit is configured to receive a control signal corresponding to a time constant, wherein the time constant corresponds to a specified slope, wherein the control signal is configured to trigger the control circuit if a slope of a voltage pulse developed in the system as a result of the ESD event is greater than or equal to the specified slope.

22. A system comprising:
one or more pads, each pad comprising:
a respective physical pad having respective capacitance; and
a respective pad circuit comprising:
a respective output buffer coupled to the respective physical pad,
and operable to drive at least one respective output signal at the respective physical pad;
and
respective control circuitry operable to activate at least a portion of
the respective output buffer in response to an ESD event to charge the respective pad
capacitance to reduce a maximum voltage developed in the system as a result of the ESD
event.

23. The system of claim 22, further comprising functional circuitry coupled to the respective pad circuit of at least one of the one or more pads, wherein the functional circuitry is operable to generate the at least one respective output signal driven by the respective pad circuit of the at least one of the one or more pads.

24. The system of claim 22, wherein each pad further comprises a respective clamp device configured to absorb, when turned on, a portion of an energy generated by the ESD event, to thereby further reduce the maximum voltage developed in the system as the result of the ESD event;

wherein the respective control circuitry of the respective pad circuit of each pad is operable to turn on the clamp device in response to the ESD event.

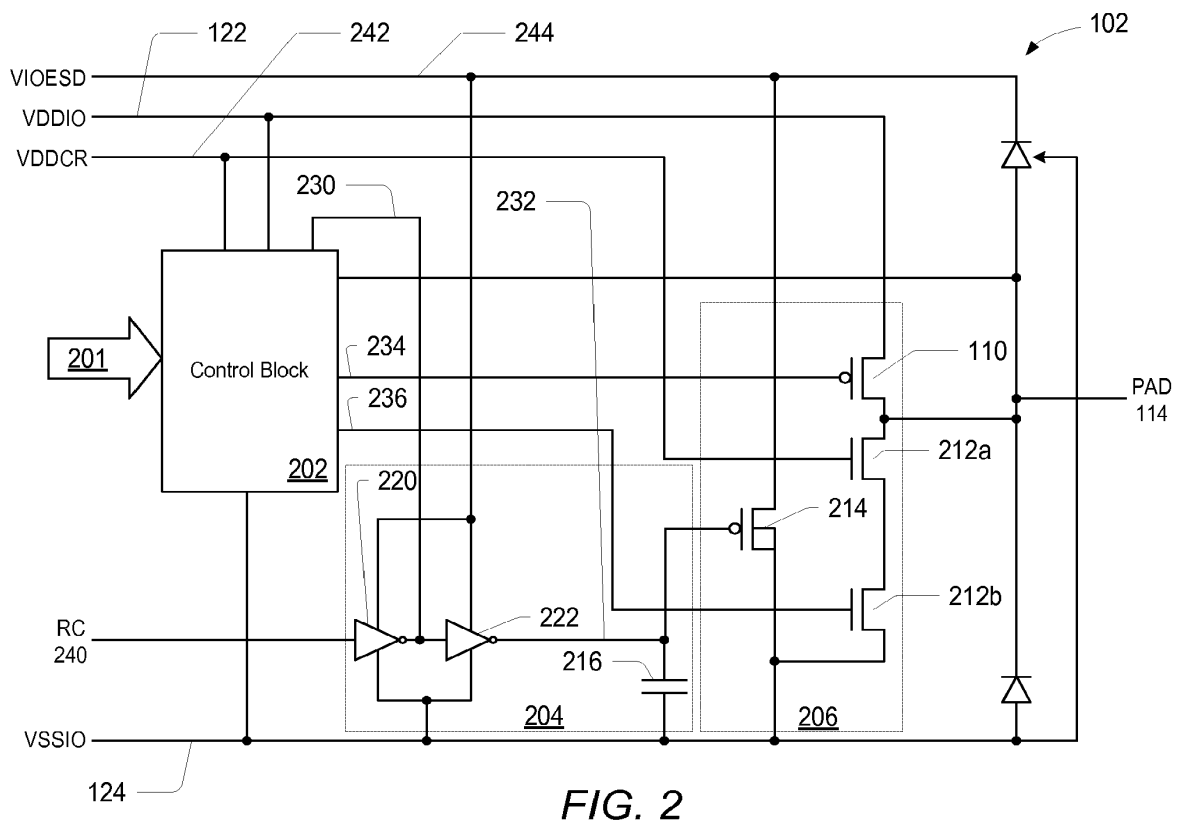
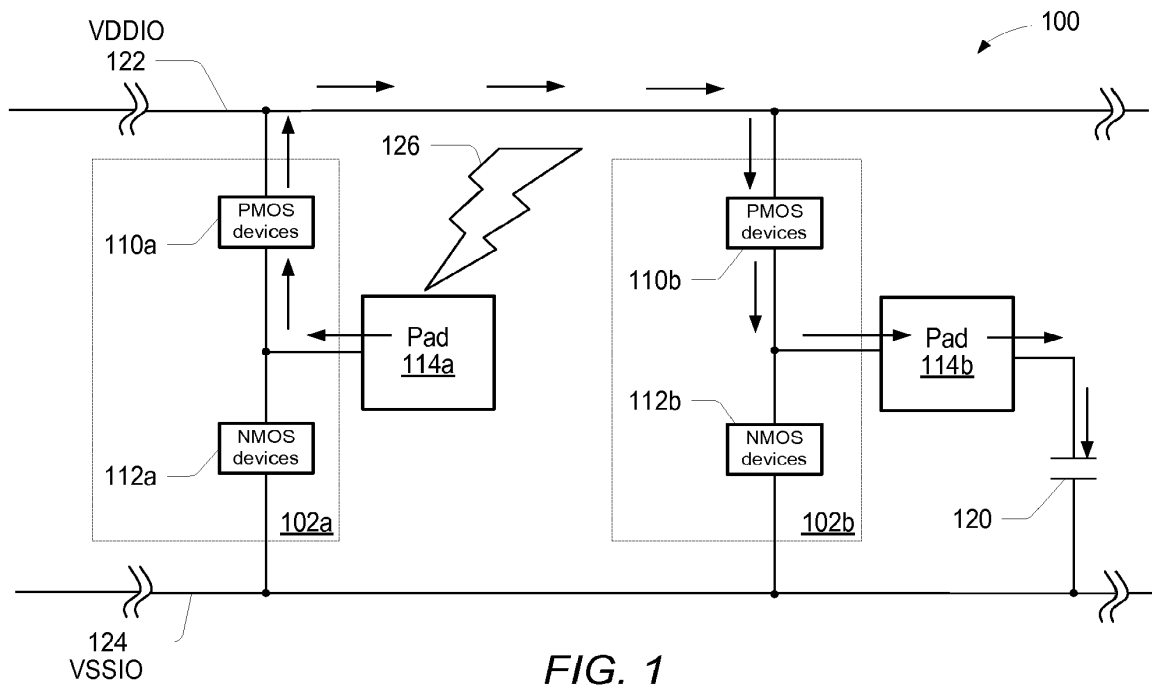
25. The system of claim 22, further comprising a first supply rail configured to provide increased power in accordance with the ESD event, and further configured to power the respective control circuitry of the respective pad circuit of each pad.

26. The system of claim 25, further comprising a second supply rail configured to power the respective output buffer of the respective pad circuit of each pad.

27. The system of claim 25, wherein the respective control circuitry of the respective pad circuit of each pad is configured to receive a respective control signal corresponding to a time constant, wherein the time constant corresponds to a specified slope, wherein the respective control signal is configured to trigger the respective control circuitry if a slope of a voltage pulse developed in the system as a result of the ESD event is greater than or equal to the specified slope.

ABSTRACT OF THE DISCLOSURE

[0023] A system, e.g. an integrated circuit or part, may include a plurality of pads, e.g. digital I/O pads, each comprising a physical pad and associated pad circuit. In case of an ESD event affecting one or more of the digital I/O pads, PMOS devices configured in an output buffer section between an I/O pad supply rail and the physical output pad – within their respective pad circuits in the affected digital I/O pads – may all be turned on in response to the ESD event. This may allow the capacitance of each pad, in some cases approximately 3pF capacitance per pad, to charge up, absorbing the energy of the ESD event and reducing the peak voltage the integrated circuit or part experiences as a result of the ESD event. The reduced peak voltage may be directly correlated with improved ESD performance of the product.



DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name.

I believe the inventor(s) named below to be the original and first inventor(s) of the subject matter which is claimed and for which a patent is sought on the invention entitled "PAD ESD SPREADING TECHNIQUE," the specification of which:

☒ is attached hereto.
☐ was filed on _____ as Application Serial No. _____
 and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the Patent and Trademark Office all information known to me to be material to patentability of the subject matter claimed in this application, as "materiality" is defined in 37 C.F.R. § 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate listed below, or under § 365(a) of any PCT international application listed below designating at least one country other than the United States of America, and have identified below any foreign application for patent or inventor's certificate, or of any PCT international application, having a filing date before that of the application on which priority is claimed.

<u>Prior Foreign Application No.</u>	<u>Country</u>	<u>Filing Date</u> <u>(mm/dd/yy)</u>	<u>Priority</u> <u>Claimed</u>	<u>Cert. copy</u> <u>Attached</u>
N/A				

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below.

<u>Provisional Application No.</u>	<u>Filing Date</u> <u>(mm/dd/yy)</u>
N/A	

I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s) listed below, or under § 365(c) of any PCT international application listed below designating the United States of America, and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose all information known to me to be material to the patentability of the subject matter claimed in this application, as "materiality" is defined in 37 C.F.R. § 1.56, which became available between the filing date of the prior application and the national or PCT international filing date of this application.

<u>Parent Application No.</u>	<u>Filing Date</u> <u>(mm/dd/yy)</u>	<u>Parent Patent No. (if applicable) or Status</u>
N/A		

I hereby revoke any previous Powers of Attorney and appoint the practitioners at Customer Number 35690, which currently includes Jeffrey C. Hood, Reg. No. 35,198; B. Noël Kivlin, Reg. No. 33,929; Robert C. Kowert Reg. No. 39,255; Eric B. Meyertons, Reg. No. 34,876; Mark S. Williams, Reg. No. 50,658; Mark K. Brightwell, Reg. No. 47,446; Russell E. Henrichs, Reg. No. 50,354; and Mario J. Lewin, Reg. No. 54,268; with full power of substitution and revocation, to prosecute the application, to make alterations and amendments therein, to transact all business in the Patent and Trademark Office in connection therewith, and to receive the Letters Patent.

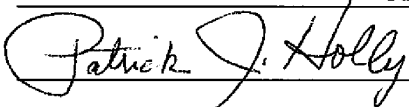
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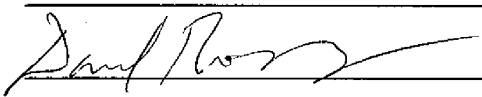
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Phone: (512) 853-8800

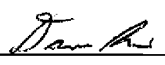
I hereby declare that all statements made herein of my own knowledge are true and that all statements made herein on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

PJH

J.

Inventor's Full Name: Patrick Holly
Inventor's Signature:  Date: 1/9/07
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(Include number, street name, city, state and zip code)

Inventor's Full Name: David Rodriguez
Inventor's Signature:  Date: 1/9/07
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Inventor's Full Name: David R. Rice
Inventor's Signature:  Date: 1/9/07
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Post Office and Residence Address: 3930 E. Ray Rd., Ste. 200, Phoenix, AZ 85044
(Include number, street name, city, state and zip code)

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		Pad ESD Spreading Technique		
First Named Inventor/Applicant Name:		Patrick J. Holly		
Filer:		Jeffrey C Hood/Jeannie Miranda		
Attorney Docket Number:		5707-12800		
Filed as Large Entity				
Utility Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility application filing	1011	1	300	300
Utility Search Fee	1111	1	500	500
Utility Examination Fee	1311	1	200	200
Pages:				
Claims:				
Claims in excess of 20	1202	7	50	350
Independent claims in excess of 3	1201	1	200	200
Miscellaneous-Filing:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1550

Electronic Acknowledgement Receipt

EFS ID:	1429131
Application Number:	11621724
International Application Number:	
Confirmation Number:	1652
Title of Invention:	Pad ESD Spreading Technique
First Named Inventor/Applicant Name:	Patrick J. Holly
Customer Number:	35690
Filer:	Jeffrey C Hood/Jeannie Miranda
Filer Authorized By:	Jeffrey C Hood
Attorney Docket Number:	5707-12800
Receipt Date:	10-JAN-2007
Filing Date:	
Time Stamp:	14:47:02
Application Type:	Utility

Payment information:

Submitted with Payment	yes
Payment was successfully received in RAM	\$1550
RAM confirmation Number	15
Deposit Account	501505
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 and 1.17	

File Listing:

MCHP_00000033

Document Number	Document Description	File Name	File Size(Bytes)	Multi Part /.zip	Pages (if appl.)		
1		5707-12800_patent_app.pdf	114220	yes	18		
	Multipart Description/PDF files in .zip description						
	Document Description		Start	End			
	Specification		1	11			
	Claims		12	17			
	Abstract		18	18			
Warnings:							
Information:							
2	Drawings	5707-12800_formal_drawing s.pdf	31590	no	1		
Warnings:							
Information:							
3	Oath or Declaration filed	5707-12800_signed_dec_po a.pdf	66830	no	2		
Warnings:							
Information:							
4	Fee Worksheet (PTO-06)	fee-info.pdf	8526	no	2		
Warnings:							
Information:							
Total Files Size (in bytes):			221166				
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.							

Electronic Acknowledgement Receipt

EFS ID:	1429131
Application Number:	11621724
International Application Number:	
Confirmation Number:	1652
Title of Invention:	Pad ESD Spreading Technique
First Named Inventor/Applicant Name:	Patrick J. Holly
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Filer Authorized By:	Jeffrey C Hood
Attorney Docket Number:	5707-12800
Receipt Date:	10-JAN-2007
Filing Date:	
Time Stamp:	14:47:02
Application Type:	Utility

Payment information:

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Payment was successfully received in RAM	\$1550
RAM confirmation Number	15
Deposit Account	501505
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 and 1.17	

File Listing:

MCHP_00000035

Document Number	Document Description	File Name	File Size(Bytes)	Multi Part /.zip	Pages (if appl.)				
1		5707-12800_patent_app.pdf	114220	yes	18				
	Multipart Description/PDF files in .zip description								
	Document Description		Start	End					
	Specification		1	11					
	Claims		12	17					
	Abstract		18	18					
Warnings:									
Information:									
2	Drawings	5707-12800_formal_drawing s.pdf	31590	no	1				
Warnings:									
Information:									
3	Oath or Declaration filed	5707-12800_signed_dec_po a.pdf	66830	no	2				
Warnings:									
Information:									
4	Fee Worksheet (PTO-06)	fee-info.pdf	8526	no	2				
Warnings:									
Information:									
Total Files Size (in bytes):			221166						
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.									



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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	DRAWINGS	TOT CLAIMS	IND CLAIMS
11/621,724	01/10/2007	2836	1550	5707-12800	1	27	4

CONFIRMATION NO. 1652

35690
MEYERTONS, HOOD, KIVLIN, KOWERT & GOETZEL, P.C.
700 LAVACA, SUITE 800
AUSTIN, TX78701

FILING RECEIPT

Date Mailed: 02/08/2007

Receipt is acknowledged of this regular Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please mail to the Commissioner for Patents P.O. Box 1450 Alexandria Va 22313-1450. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).**

Applicant(s)

Patrick J. Holly, Tempe, AZ;
David Rodriguez, Phoenix, AZ;
David R. Rice, Phoenix, AZ;

Power of Attorney: The patent practitioners associated with Customer Number 35690

Domestic Priority data as claimed by applicant

Foreign Applications

If Required, Foreign Filing License Granted: 02/08/2007

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is
US11/621,724

Projected Publication Date: 07/10/2008

Non-Publication Request: No

Early Publication Request: No

Title

Pad ESD Spreading Technique

Preliminary Class

361

MCHP_00000037

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

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Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD					11/621,724	
Substitute for Form PTO-875						
APPLICATION AS FILED – PART I						
		(Column 1)	(Column 2)			
FOR	NUMBER FILED	NUMBER EXTRA		SMALL ENTITY		OTHER THAN SMALL ENTITY
BASIC FEE (37 CFR 1.16(a), (b), or (c))				RATE (\$)	FEE (\$)	RATE (\$)
SEARCH FEE (37 CFR 1.16(k), (l), or (m))						300
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))						500
TOTAL CLAIMS (37 CFR 1.16(i))	24	minus 20 =		X\$25=		200
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3	minus 3 =		X\$100=		200
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR					X\$50
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))						X\$200=
				N/A		N/A
				TOTAL		TOTAL
						1200
APPLICATION AS AMENDED – PART II						
		(Column 1)	(Column 2)	(Column 3)		
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	SMALL ENTITY	
	Total (37 CFR 1.16(i))	*	Minus **	=	RATE (\$)	ADDITIONAL FEE (\$)
	Independent (37 CFR 1.16(h))	*	Minus ***	=	X =	
	Application Size Fee (37 CFR 1.16(s))				X =	
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))				N/A	
					TOTAL	
					ADD'T FEE	
					OR	
					OTHER THAN SMALL ENTITY	
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	SMALL ENTITY	
	Total (37 CFR 1.16(i))	*	Minus **	=	RATE (\$)	ADDITIONAL FEE (\$)
	Independent (37 CFR 1.16(h))	*	Minus ***	=	X =	
	Application Size Fee (37 CFR 1.16(s))				X =	
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))				N/A	
					TOTAL	
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					OTHER THAN SMALL ENTITY	
					RATE (\$)	ADDITIONAL FEE (\$)
					X =	
					X =	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		11621724
	Filing Date		2007-01-10
	First Named Inventor	Patrick J. Holly	
	Art Unit	2836	
	Examiner Name	Unknown	
	Attorney Docket Number	5707-12800	

U.S. PATENTS						Remove
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
	1	5717560		1998-02-10	Doyle, et al.	
	2	5907464		1999-05-25	Maloney, et al.	
	3	5956219		1999-09-21	Timothy J. Maloney	
	4	6008970		1999-12-28	Maloney, et al.	
	5	6577481	B2	2003-06-10	Steinhoff, et al.	
	6	6690555	B1	2004-02-10	Ronald Pasqualini	
	7	6744610	B2	2004-06-01	Chang, et al.	
	8	6747501	B2	2004-06-08	Ker, et al.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		11621724	
	Filing Date		2007-01-10	
	First Named Inventor	Patrick J. Holly		
	Art Unit	2836		
	Examiner Name	Unknown		
	Attorney Docket Number	5707-12800		

	9	6760209	B1	2004-06-07	Bradley A. Sharpe-Geisler	
	10	6768176	B1	2004-07-27	David D. Litfin	
	11	6788507	B2	2004-09-07	Chen, et al.	
	12	6800906	B2	2004-10-05	Jyh-Nan Cheng	
	13	6829126	B2	2004-12-07	Lee, et al.	
	14	6838775	B2	2005-01-04	Makoto Takahashi	
	15	6844595	B2	2005-01-18	Wei-Fan Chen	
	16	6864536	B2	2005-03-08	Lin, et al.	
	17	6876529	B2	2005-04-05	Larry B. Li	
	18	7106563	B2	2006-09-12	Lai, et al.	
	19	7019366	B1	2006-03-28	Yang, et al.	

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	First Named Inventor	Patrick J. Holly		
	Art Unit	2836		
	Examiner Name	Unknown		
	Attorney Docket Number	5707-12800		

	20	6157065		2000-12-05	Huang, et al.	
	21	5707886		1998-01-13	Consiglio, et al.	
	22	5223737		1993-06-12	Athos Canclini	
	23	5208719		1993-05-04	Yi-Hen Wei	

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	Examiner Name	Unknown	
	Attorney Docket Number	5707-12800	

	1	TIMOTHY J. MALONEY, STEVEN S. POON and LAWRENCE T. CLARK; "Methods for Designing Low-leakage Power Supply Clamps"; Proceedings of Electrical Overstress Electrostatic Discharge Symposium; 2003, 7 pages; Intel Corporation.	☐
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Methods for Designing Low-leakage Power Supply Clamps

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Abstract - Low power semiconductor components require minimizing leakage currents including those from ESD protection circuits. Here, MOSFET ESD power clamps with substantial leakage reduction over previous approaches are presented. Designs are described for core logic circuits and for I/O applications where supply voltages exceed what single gate oxides can reliably sustain.

I. Introduction and rationale

Integrated circuits powered by small batteries, e.g., hand-held and cell phone applications, must meet stringent power usage requirements that are, in turn, demanded by limited battery capacity. Process scaling, which requires lower threshold voltages to maintain gate overdrive as V_{cc} is scaled, exponentially increases transistor drain to source leakage currents. Long device idle times increasingly make standby power a limiting factor in battery lifetime. This has made MTCMOS [1], and reverse-body bias (RBB) [2,3] techniques attractive on 0.25 μ m process generations and beyond. While the leakage reduction techniques can be applied to reduce core logic circuit leakage currents successfully, other leakage contributions due to I/O or ESD protection circuits are unaffected and can consequently become the limiting case during standby operation.

In the IC described in [3], the reverse-body bias "drowsy" mode allows a leakage reduction of over 25x compared with the active bias condition. One of the power supply clamps described here utilizes reverse body bias to limit the I_{off} contribution to a negligible fraction of the total standby current, while judicious circuit design retains high clamping performance. Another clamp design is amenable to high-voltage I/O operation using only low voltage transistors. It is useful for providing compatibility with 3.3V or 5V I/O standards, while using thin-oxide low voltage logic transistors as in [4,5].

II. Power supply clamps for a single thin gate oxide voltage

A typical power supply clamp for a low voltage core has a very wide PMOS device [6,7] that provides the primary ESD clamping function. Figure 1 illustrates a PMOS clamp that body biases the large clamp device to lower the I_{off} contribution, commensurate with that in the core logic circuits. Unlike the core circuits, this RBB is applied continuously in operation. Thus, the leakage of the ESD clamp is lessened during both active and standby operation. Referring to Fig. 1, operation resembles that of the standard PMOS clamp with a few important differences. An additional inverter follows the RC timer and is used to drive the gate of N1, which pulls up the nwell of the main clamp transistor P1 to the V_{cc} supply (approved for a single gate oxide) during an ESD zap and before the clamp times out. However, once the timeout happens, N1 turns off and P1's nwell defaults to an NMOS threshold voltage below the high voltage node V_{cchi} as pulled up by device N2. In this way the high voltage supply V_{cchi} (typically 2.5 or 3.3V vs. V_{cc} of 1.3V or less) applies RBB to the clamp transistor P1. V_{cchi} itself is clamped by a high voltage clamp, resembling those discussed below.

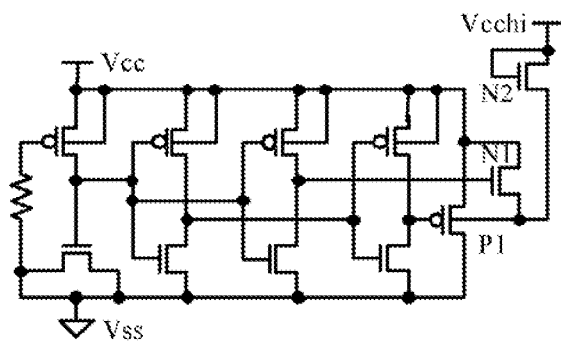


Figure 1. Backgated low leakage PMOS ESD clamp

The transistor V_T is affected by back-bias in such a way that over 1V is required to increase V_T by 100mV, corresponding to roughly a decade in I_{off} improvement for the PMOS transistor as given by

$$I_{off} \propto \exp \left(\frac{V_T}{S/1610} \right) \quad (1)$$

where the subthreshold swing factor S is typically between 85 and 100mV. Consequently, raising V_T by S will lower I_{off} by one decade, but at the cost of transistor performance. RBB allows electrical adjustment of V_T while maintaining logic circuit speed. Figure 2 shows that application of reverse body bias V_b is worthwhile, with nearly two orders of magnitude of leakage reduction for about 2V of reverse body bias at $V_{cc} = 1V$. Depending on the process, the I_{off} may be driven below a gate leakage value of approximately 5-8pA/ μm of gate width (typical for a 0.13 μm process), depending on the drain bias. This takes the total clamp leakage to a low level, so that it no longer dominates the core leakage. Simulations have shown that the circuit performs acceptably at all temperature and process corners. The low standby power is accomplished without significantly increasing the layout area since the circuitry to perform the reverse body biasing need only supply the well leakage current. A small, low current circuit to apply the body bias incidentally allows the ESD event to provide forward body bias, thereby increasing the transistor drive current when clamping.

It is well known that subthreshold leakage is typically the dominant leakage component of the minimum-length, non-back biased device [8]. But there are other contributors to the off-state leakage of a MOS device. Device scaling has encouraged process developers to reduce oxide thickness and to increase doping levels in the channel and/or in halo implants [9]. These innovations, while successful in controlling

short-channel effects, have caused significant increases in gate tunneling and junction band-to-band tunneling currents [10-11]; e.g., the gate-to-drain component of the gate oxide leakage does not decrease through backgating. And while subthreshold current decreases with increased body bias, junction leakage increases with body bias due to the higher junction voltages. Thus the influence of backgating will be limited in newer process generations as these other leakage mechanisms grow in their influence [12]. Nonetheless, the circuit in Fig. 1 significantly reduces leakage current in the 0.18 μm and 0.13 μm generations, especially at high temperatures and fast process corners, at which substantially higher levels of subthreshold leakage exist.

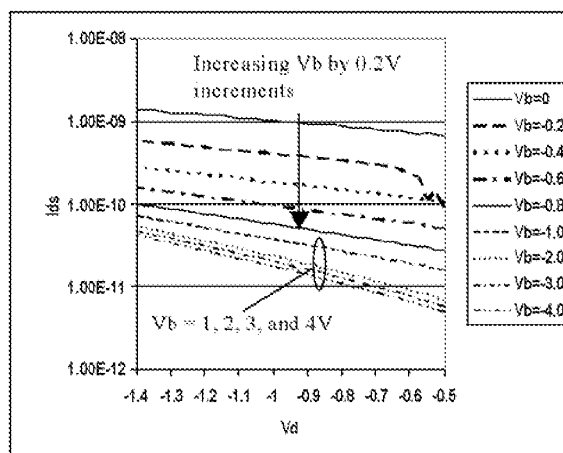


Figure 2. Drain to source leakage (I_{off}) of PMOS transistors on a 0.18 μm process at room temperature

A. Lowering leakage in a clamp for single gate oxide through stand-alone backgating

Sometimes a higher supply voltage will not be available for backgating the n-well as described above. In that event, some reduction of the standby leakage can still be achieved by building a small amount of backgating into the clamp design, at the expense of some area. Figure 3 shows a design that uses the same drive circuitry as described in [6,7], only it drives a double-gate FET stack for which both devices P1 and P2 are in the same n-well. Accordingly, the lower FET P2 will have its n-well approximately one threshold voltage V_{tp} above its source, where it is effectively back-gated. Leakage is lower than for a single gate clamp because the backgating of the series FET P2 limits the current. Additionally, the slightly positive gate to source voltage further decreases the P2 I_{off} . P1

I_{off} is reduced due to lower V_{ds} . Informally, this design is sometimes known as “one for the price of two”, but the actual area increase is only about 50% because of the efficiency of layout of a double gate. Table 1 (see section IV) shows how, in a 0.18 μ m process, the leakage of this kind of clamp (pmoslwk, Figure 3) is cut to about 30% of the leakage of a standard PMOS clamp device (pmos1, designed as in [6,7]).

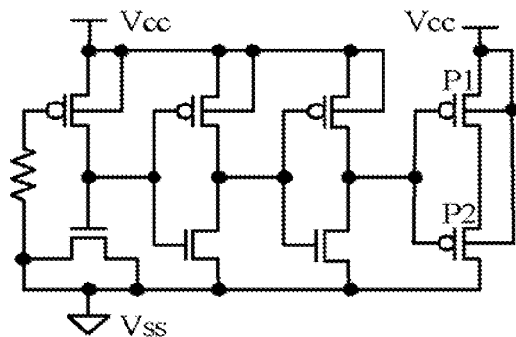


Figure 3. Low-leakage PMOS clamp with double gate on large device and built-in back bias for P2

III. Lowering leakage in stacked-gate clamps for higher voltages

Contemporary product designs often have multiple voltage supplies. When the voltage exceeds the allowed voltage for a single thin gate oxide, we need new methods for protecting the supply itself. For low power products we must improve on the 2-stack and multi-stack clamps in [13-16], which commonly require at least 0.5 to 1 μ A of standby current. These stacked clamps have their midpoint V_{mid} biased by resistive long-channel devices Pbias1 and Pbias2 as in Figure 4 [15]. The following methods are aimed at stacked-gate clamps for high voltages, using bias circuits with much lower standby current.

Figure 5 shows an example of a two-stack voltage tolerant clamp with low bias current. Rather than use a resistive voltage divider to establish the midpoint voltage V_{mid} between V_{cc} and V_{ss} , we now use a long string of slightly-on subthreshold devices to establish the midpoint voltage. These devices need only drive the small gates of two follower FETs Pfl and Nfl in Fig. 5. Pfl and Nfl in Fig. 5 are a voltage buffer that turns the weak voltage V_{ref} into a fairly strong voltage source for V_{mid} , such that $V_{ref} - V_{tp} < V_{mid} < V_{ref} + V_{tn}$. The buffer Pfl and Nfl then sources or sinks just enough current to supply the

subthreshold currents of the bias circuitry, a fairly small requirement. In practice, it is Nfl that nearly always turns on to supply extra current to the lower half of the circuit, since its NMOS FETs have no substrate back bias. The subthreshold current of the wide PMOS clamp FETs P1 and P2 then dominates the standby leakage of the entire circuit, as shown in Table 1 the improvement is over 50%. The remainder of the bias circuitry in Fig. 5 for the stacked clamp is exactly as in [13-16]. The devices in the subthreshold string are small in size (0.4/2) so that a long string will not use much area or consume much current. The transistors are tied identically, providing good consistency across process corners. The area impact of the extra bias circuitry required for these designs can be held to less than 10% (and one must carefully optimize the layout of both designs to see any impact at all). This method of supplying bias for low leakage stacked clamps can be generalized to stacks of three or more clamping devices and bias circuits, thus raising the voltage that can be clamped.

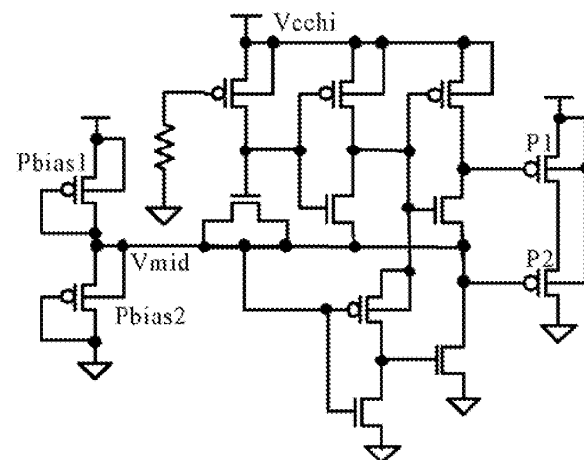


Figure 4. Standard stacked PMOS clamp with resistive bias through Pbias1 and Pbias2, fixing midpoint V_{mid} at about half of V_{cchi}

IV. Leakage Results

Table 1 summarizes the standby leakage results for the designs discussed herein and shows the kind of improvement over existing design practices that can be achieved. The back-gated value temperature dependence is taken from experimental data on a 0.18 μ m process. These designs have been described in [17] and are used in low-power Intel products such as XScale Microarchitecture™ processors [3, 18].

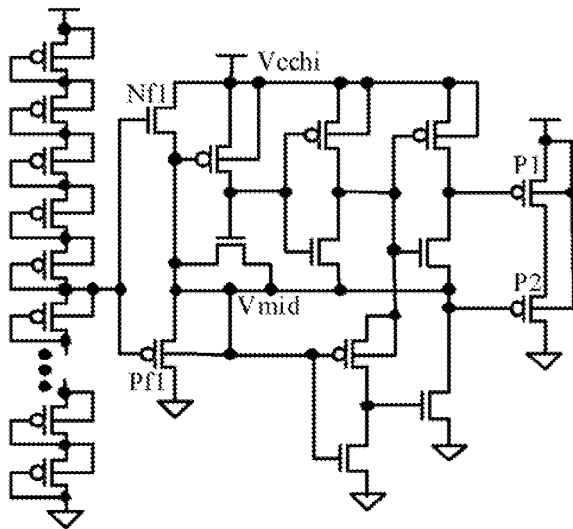


Figure 5. 2-stack voltage-tolerant clamp with reduced bias current

Table 1. Thin gate oxide clamp designs compared for leakage on a 0.18 μ m process

PMOS Clamp design, 0.18 μ m	Leakage, 27C (μ A)	Leakage, 110C (μ A)
pmos1, regular clamp cell	0.413	11
back-gated pmos1, Fig. 1	0.064	3.52
pmos1wk, Fig. 3	0.132	2.83
2-stack cell, Fig. 4, from [13-15]	0.650	17.3
2-stack low-leak clamp, Fig. 5	0.300	8.65

Now we turn to the same kind of designs on the 0.13 μ m process [19]. This process introduced substantial gate leakage and had an effect on total leakage as well as the circuits used in ESD power supply clamps [15-16]. As shown in Table 2, leakage was always in the microamp range, and moving to the new circuits such as in Figs. 3 and 5 was not very effective. There was some effect at high temperature with backgating as in Figs. 1 and 3. As expected, backgating was most effective at reducing leakage for the low- V_T end of the process and at high temperature. As discussed earlier, increased gate oxide and junction leakage puts some limits on the effectiveness of backgating at this process node. Fortunately, the products intended for low leakage applications in the 0.13 μ m process are typically

implemented in a process version supporting two oxide thicknesses, so there is also a far less leaky thick gate oxide, tolerant of 2.5V and intended for I/O, which can be used for power supply clamps.

Table 2. Thin gate oxide clamp designs compared for leakage on a 0.13 μ m process. Typical results are shown; at the low- V_T or "fast" end of the process, there is more leakage and more effect due to backgating

PMOS Clamp design, 0.13 μ m	Leakage, 25C (μ A)	Leakage, 125C (μ A)
latched regular clamp cell, [15]	6.8	22.9
back-gated pmos1, Fig. 1*	6.7	11.7
pmos1wk, Fig. 3*	6.7	12.3
2-stack cell, Fig. 4, from [13-15]*	5.1	19.0
2-stack low-leak clamp, Fig. 5*	5.7	20.6

*with latch circuit as in [15]

Table 3 shows the typical leakage results for ESD power clamps made with thick gate oxide devices in the 0.13 μ m process. Using a familiar design for non-leaky gate oxides [7], essentially Fig. 1 without the backgating, standby leakage is fairly low. Adding backgating to this design as in Fig. 1 does not reduce the low-temperature leakage by much, but does reduce high-temperature leakage to about one microamp at typical and fast (i.e., typical and low V_T) process corners.

Table 3. Thick gate oxide clamp leakage results on a 0.13 μ m process

PMOS Clamp design, 0.13 μ m	Leakage, 25C (μ A)	Leakage, 125C (μ A)
regular thick gate clamp cell, [7], 2.5V	0.63	10.2
thick gate clamp cell, [7], 1.3V	0.19	5.9
2-stack cell, Fig. 4, 3.3V, from [13-15]	1.7	9.8
2-stack low-leak clamp, 3.3V, Fig. 5	0.35	9.5
2-stack cell, Fig. 4, 5V, from [13-15]	4.0	17.1
2-stack low-leak clamp, 5V, Fig. 5	0.93	13.7

Table 3 also shows that using the low-leakage circuits as in Fig. 5 provides substantial improvement in standby leakage at lower temperatures, over Fig. 4 for the 2-stack thick oxide clamp in the 0.13 μ m process. But it is at these lower temperatures where the low standby current is most desired, when the component is idling. Since the high temperature leakage is mostly temperature-dependent subthreshold leakage in the main clamping FETs, backgating would be available for reducing that leakage if it were desired.

V. Discussion and Conclusions

The theme of this work is to arrive at ESD power clamp designs which will have the same performance as traditional clamp designs [6-7,13-16] yet will have lower standby leakage current. All the designs discussed herein have virtually the same Human Body Model (HBM), Charged Device Model (CDM), and transmission line pulse (TLP) results as discussed in those earlier references. The intention is for HBM and CDM to be high enough (e.g., over 4kV HBM and over 1kV CDM on the KeyTek Zapmaster) to prove self-protection of the clamps, and enough pulsed TLP current at low voltage (e.g., 2A at about 4V as in [15]) to protect other circuitry on the power supply. In short, the ESD performance impact of the low-leakage circuitry discussed herein was negligible. This is because the ESD current is sunk through the large FETs, which are unchanged. We made sure the gate drive and timing would be unaffected by the low leakage circuitry, through circuit simulation.

In recent times there has been renewed interest in the power-up transient associated with these RC-timed clamps. The fastest anticipated ramp times (slew rates) are getting faster, and there is more frequent dynamic power-up and power-down of circuits. The increase in battery-powered applications motivates us to look at total charge consumption on power-up, and to put bounds on how weak a power supply (i.e., how high an output impedance) might have to power up these clamps. The good news about the low-leakage circuits in this paper is that there was little if any impact on the basic behavior of the ESD clamps' power-up transient. Again, the reason is that the clamp FETs are unchanged, and the gate drive timing of those FETs is also largely unchanged.

As we investigate power-up transients in the light of broader applications, it is useful to reflect on a basic fact brought out in our early work on the subject of ESD power clamps [20,21], the fact that the total

amount of charge needed to power up these clamps is a few microcoulombs. This makes sense based on amps of current for RC-timed microseconds, of course. The fast (nanosecond scale) ramp requires the most charge, and the required charge declines from there, with a 100 μ s power ramp's charge pulse down by a factor of ten to a few hundred nanocoulombs. But note how these quantities of charge compare with battery charges, which are measured on the scale of ampere-hours. 3.6 μ C is a billionth of an ampere-hour! This illustrates a fundamental principle of electrostatic phenomena that we should all know, which is that the currents and voltages in ESD can be high, but the amount of charge is small.

If total charge for power-up is of any concern, it can still be reduced for the longer times common to power-up of the supply by a voltage source. Table 4 shows the charge quantities associated with ramp times from fast to slow, and how they are influenced by adding a simple pullup resistor of a few hundred ohms, R1, as in Figure 6. For ramp times of 100 μ s and above, note that total charge required drops by over two orders of magnitude. The transient for an ESD-like fast ramp, and the total charge pulse, is not affected.

Table 4. Charge quantities, in microcoulombs, for power-up of a simple ESD clamp using 2.5V gate oxide, designed as in Fig. 6, with and without pullup resistor R1

Voltage ramp time	Charge, no pullup (μ C)	Charge, with pullup (μ C)
1 nsec	3.54	3.56
10 μ sec	2.96	2.84
100 μ sec	0.43	0.002
1 msec	0.089	0.00028

In addition, the R1 in Fig. 6 adds a threshold-free device between clamp FET gate and source, and largely removes any concern about V_T effects on the quasi-static I-V curve of the power clamp as voltage varies from 0V to nominal V_{CC} . If this curve intercepts the load line of a weak voltage supply, then the power-up could stall out at a low voltage. Resistor R1 vastly reduces any such difficulties by pulling up the gate of the clamp FET at any voltage, independent of the V_{tp} of the PMOS drive device. It is beyond the scope of this paper to further discuss process corners and power sources which could cause concern about

powering up the clamp and associated circuitry in normal operation, but suffice it to say that the pullup resistor R1 of a few hundred ohms has relieved those concerns without compromising ESD performance.

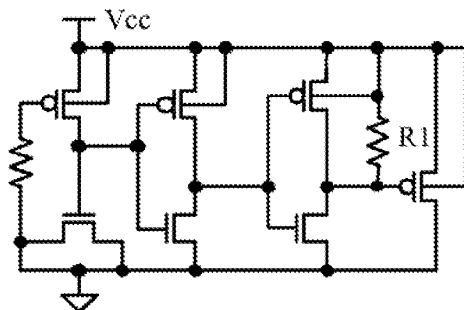


Figure 6. Regular PMOS single oxide clamp with pullup resistor R1 (several hundred ohms) that reduces the power-up transient for ramp rates slower than ESD

In conclusion, we have presented circuits for reducing leakage in a variety of MOS ESD power supply clamps in 0.18 μ m and 0.13 μ m processes. The circuits have enabled substantial reduction of leakage without compromising ESD performance. A large payoff in leakage reduction comes with various backgating schemes to reduce the subthreshold leakage of the clamping MOSFETs (PMOS in our case, but the same principles would apply to NMOS). These effects are most pronounced when that subthreshold leakage dominates the total leakage, and are less noticeable when gate oxide leakage is substantial. In addition, stacked voltage-tolerant ESD clamps benefit from improving on the resistive voltage divider as a way to establish internal bias in the clamp. An active circuit targets the bias current distribution in a more efficient way and reduces leakage current in these clamps for all processes, whether or not gate oxide leakage is substantial. Finally, the total charge required for power-up of the supply clamp at ordinary supply ramp rates can be reduced by adding a single resistive element to the circuit, but this has no appreciable effect on the circuit's behavior at the ESD time scale.

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References

- [1] S. Mutoh, et al., "1-V Power Supply High-Speed Digital Circuit Technology with Multithreshold-Voltage CMOS," *IEEE J. of Solid-State Circuits*, **30**, pp. 847-854 (1995).
- [2] H. Mizuno, et al., "An 18- μ A Standby Current 1.8V, 200MHz Microprocessor with Self-Substrate-Biased Data-Retention Mode," *IEEE J. Solid-State Circuits*, **34**, pp. 1492-1500 (1999).
- [3] L. T. Clark, et al., "Standby Power Management for a 0.18 μ m Microprocessor," *Proc. 2002 International Symposium on Low Power Electronics and Design*, pp. 7-12.
- [4] L. T. Clark, "A High-Voltage Output Buffer Fabricated on a 2V CMOS Technology," *Proc. 1999 IEEE Symposium on VLSI Circuits*, pp. 61-62.
- [5] G. B. Singh and R. B. Salem, "High-Voltage-Tolerant I/O Buffers with Low-Voltage CMOS Process," *IEEE J. of Solid-State Circuits*, **34**, pp. 1512-1525 (1999).
- [6] T.J. Maloney and T.M. Eiles, US Patent 5,907,464; issued May 25, 1999, assigned to Intel Corp.
- [7] T.J. Maloney, "Designing Power Supply Clamps for Electrostatic Discharge Protection of Integrated Circuits", *Microelectronics Reliability* **38**, No. 11, pp. 1691-1703 (November, 1998).
- [8] B. Doyle et al., "Transistor Elements for 30nm Physical Gate Lengths and Beyond." *Intel Technology Journal*. <http://developer.intel.com/technology/itj/2002/volume06issue02/> (May 2002).
- [9] R. Chau et al., "30 nm physical gate length CMOS transistors with 1.0 ps n-MOS and 1.7 ps p-MOS gate delays," *IEDM Tech. Digest*, 2000, pp. 45-48.
- [10] T. Ghani et al., "Scaling challenges and device design requirements for high-performance sub-50 nm gate length planar CMOS transistors," *VLSI Symposium Tech. Digest*, 2000, pp. 174-175.
- [11] B. Yu et al., "50nm Gate-Length CMOS Transistor with Super-Halo: Design, Process, and Reliability," *IEDM Tech. Digest*, 1999, pp.653-655.
- [12] A. Keshavarzi, S. Narendra, S. Borkar, C. Hawkins, K. Roy and V. De, "Technology Scaling Behavior of Optimum Reverse Body Bias

- for Standby Leakage Power Reduction in CMOS IC's", Proceedings of 1999 International Symposium on Low Power Electronics and Design, pp. 252-254.
- [13] T.J. Maloney, US Patent 5,956,219, issued Sept. 21, 1999, assigned to Intel.
 - [14] T.J. Maloney and W. Kan, "Stacked PMOS Clamps for High Voltage Power Supply Protection", 1999 EOS/ESD Symposium Proceedings, pp. 70-77. Also published in *Microelectronics Reliability* 41, No. 3, pp. 335-348 (March, 2001).
 - [15] S.S. Poon and T.J. Maloney, "New Considerations for MOSFET Power Clamps", 2002 EOS/ESD Symposium Proceedings, pp. 1-5.
 - [16] T.J. Maloney and W. Kan, "RC Timer Scheme", US Patent 6,510,033, issued Jan. 21, 2003, assigned to Intel.
 - [17] L.T. Clark, P. Elamanchili, T. Maloney, "Electrostatic Discharge Protection Device and Method Therefor", US Patent application, filed Dec. 22, 2000.
 - [18] L.T. Clark, et al., "An Embedded 32-b Microprocessor Core for Low-Power and High-Performance Applications", *IEEE J. Solid-State Circuits*, 36, pp. 1599-1608 (2001).
 - [19] S. Tyagi et al., "A 130 nm Generation Logic Technology Featuring 70 nm Transistors, Dual Vt Transistors and 6 Layers of Cu Interconnects", *IEDM Tech. Digest*, 2000, pp. 567-570.
 - [20] T.J. Maloney and S. Dabral, "Novel Clamp Circuits for IC Power Supply Protection", 1995 EOS/ESD Symposium Proceedings, pp. 1-12. Revised version published in *IEEE Trans. on Components, Packaging, and Manufacturing Technology--Part C*, 19, 150-161, July 1996.
 - [21] S. Dabral and T.J. Maloney, *Basic ESD and I/O Design*, published by Wiley Interscience, November 1998, 302 pages. <http://www.amazon.com/exec/obidos/ASIN/0471253596/>.

Electronic Acknowledgement Receipt

EFS ID:	1541401
Application Number:	11621724
International Application Number:	
Confirmation Number:	1652
Title of Invention:	Pad ESD Spreading Technique
First Named Inventor/Applicant Name:	Patrick J. Holly
Customer Number:	35690
Filer:	Jeffrey C Hood/James Candelas
Filer Authorized By:	Jeffrey C Hood
Attorney Docket Number:	5707-12800
Receipt Date:	23-FEB-2007
Filing Date:	10-JAN-2007
Time Stamp:	17:51:56
Application Type:	Utility

Payment information:

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Filed	5707-12800_IDS_01.pdf	1005098	no	6

Warnings:

MCHP_00000054

Information:					
2	NPL Documents	Maloney_Methods_for_Designing_Low-leakage_Power_Supply_Clamps.pdf	1656098	no	7
Warnings:					
Information:					
Total Files Size (in bytes):			2661196		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD					Application or Docket Number 11/621 724	
Substitute for Form PTO-875						
1/10/07 CLAIMS AS FILED – PART I SMALL ENTITY						
(Column 1)		(Column 2)		(Column 3)		(Column 4)
FOR	NUMBER FILED	NUMBER EXTRA	RATE	FEE		
BASIC FEE (37 CFR 1.16(a))						
TOTAL CLAIMS (37 CFR 1.16(c))						
INDEPENDENT CLAIMS (37 CFR 1.16(b))						
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(d))						
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			
CLAIMS AS AMENDED – PART II OTHER THAN SMALL ENTITY						
(Column 1)		(Column 2)		(Column 3)		(Column 4)
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE	ADDITIONAL FEE	
Total (37 CFR 1.16(c))						
Independent (37 CFR 1.16(b))						
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(d))						
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.			TOTAL ADD'L FEE			
AMENDMENT B OTHER THAN SMALL ENTITY						
(Column 1)		(Column 2)		(Column 3)		(Column 4)
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE	ADDITIONAL FEE	
Total (37 CFR 1.16(c))						
Independent (37 CFR 1.16(b))						
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(d))						
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.			TOTAL ADD'L FEE			
AMENDMENT C OTHER THAN SMALL ENTITY						
(Column 1)		(Column 2)		(Column 3)		(Column 4)
AMENDMENT C	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE	ADDITIONAL FEE	
Total (37 CFR 1.16(c))						
Independent (37 CFR 1.16(b))						
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(d))						
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.			TOTAL ADD'L FEE			

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/621,724	01/10/2007	Patrick J. Holly	5707-12800	1652
35690 7590 04/04/2008 MEYERTONS, HOOD, KIVLIN, KOWERT & GOETZEL, P.C. P.O. BOX 398 AUSTIN, TX 78767-0398			EXAMINER CLARK, CHRISTOPHER JAY	
			ART UNIT 2836	PAPER NUMBER
			MAIL DATE 04/04/2008	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	11/621,724	HOLLY ET AL.	
	Examiner	Art Unit	
	CHRISTOPHER J. CLARK	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on 10 January 2007.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) 1-27 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) 1-3, 8-16, 19-23 and 25-27 is/are rejected.

7) ☒ Claim(s) 4, 17, 18 and 24 is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on 10 January 2007 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)	4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) ☐ Notice of Informal Patent Application
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date <u>2/23/2007</u> .	6) ☐ Other: _____

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on February 23, 2007 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-3, 5-8, 10-15, 19, 20, 22, 23, 25, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Allen et al (U. S. Patent 5,168,178) in view of Loh et al (U. S. Patent Publication 2007/0019345).
4. In re Claim 1, Allen teaches a pad circuit as seen in Figure 2 comprising:
 - A first node coupled to a first voltage rail (the source of FET 22)
 - A second node coupled to a physical pad having capacitance (20)
 - One or more output transistor devices coupled between the first node and the second node and operable to at least partially drive an output signal at the second node (22)
5. Allen does not teach a control block operable to turn on at least one of the one or more output transistor devices in response to an ESD event to charge the pad capacitance to reduce a maximum voltage developed as a result of an ESD.

6. Loh teaches an ESD protection circuit that utilizes existing circuitry of an IC, particularly an inverter and capacitor (as seen in Figure 3) in order to shunt ESD current [Paragraph 20-22]. Loh relies on a control block (606) to send a signal to the inverter in order to shunt ESD current to the capacitor when an ESD event is detected [Paragraph 24-28].

7. It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the control block of Loh in the existing inverter/capacitor circuitry of Allen in order to provide protection from ESD events.

8. In re Claim 2, Allen teaches that first voltage rail is coupled to the capacitance to share a charge developed in the system in response to the ESD event and reducing maximum voltage developed in the system as a result of the ESD (Paragraph 20). Upon being modified by Loh as discussed above, it is to be understood that the capacitance is associated with the pad as taught by Loh.

9. In re Claim 3, Loh teaches enable circuitry (610) that sends a control signal to the control block in response to the ESD event to instruct the control block to turn on the one or more output transistors (Paragraphs 25-28).

10. In re Claim 5, both Loh and Allen teach that the output transistors are PMOS as seen in the Figures discussed above.

11. In re Claim 6, both Loh and Allen teach that the output transistors are also NMOS as seen in the Figures discussed above. Loh teaches in Paragraph 20 that ESD current is shunted to the capacitor. In order for this to occur, the NMOS transistor as seen in Figure 3 would have to be in a "turned off" state in order for ESD current to flow from the high voltage supply line to the capacitor during a high voltage ESD event.

12. In re Claim 7, Allen teaches that the pad is an output pad that receives digital outputs (Column 1 Lines 25-33).

13. In re Claim 8, Allen teaches as seen in Figure 2, one or more output transistors (22 and 24) coupled to a physical pad (20) having a pad capacitance (19) wherein the one or more output transistor devices are operable to drive an output signal at the physical pad.

14. Allen does not teach turning on at least one of the one or more output transistor devices in response to an ESD event to charge the pad capacitance to reduce a maximum voltage developed as a result of an ESD.

15. Loh teaches an ESD protection circuit that utilizes existing circuitry of an IC, particularly an inverter and capacitor (as seen in Figure 3) in order to shunt ESD current [Paragraph 20-22]. Loh relies on a control block (606) to send a signal to the inverter in order to shunt ESD current to the capacitor when an ESD event is detected [Paragraph 24-28].

16. It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the control block of Loh in the existing inverter/capacitor circuitry of Allen in order to provide protection from ESD events.

17. In re Claim 10, both Loh and Allen teach that the output transistors are PMOS as seen in the Figures discussed above.

18. In re Claim 11, both Loh and Allen teach that the output transistors are also NMOS as seen in the Figures discussed above. Loh teaches in Paragraph 20 that ESD current is shunted to the capacitor. In order for this to occur, the NMOS transistor as seen in Figure 3 would have to

be in a "turned off" state in order for ESD current to flow from the high voltage supply line to the capacitor during a high voltage ESD event.

19. In re Claim 12, Allen teaches that the pad is an output pad that receives digital outputs (Column 1 Lines 25-33).

20. In re Claim 13, Allen teaches a circuit in a system as seen in Figure 2 comprising:

- an output buffer (18B) configured to couple to a physical pad (19) having capacitance (20) and operable to drive at least one output signal at the physical pad
- a control block (18A) configured to control the output buffer

21. Allen does not teach a control circuit configured to instruct the control block to activate a portion of the output buffer when an ESD event occurs to charge the pad capacitance to reduce a maximum voltage developed as a result of an ESD.

22. Loh teaches an ESD protection circuit that utilizes existing circuitry of an IC, particularly an inverter and capacitor (as seen in Figure 3) in order to shunt ESD current [Paragraph 20-22].

Loh relies on a control block (606) to send a signal to the inverter in order to shunt ESD current to the capacitor when an ESD event is detected [Paragraph 24-28].

23. It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the control circuit of Loh in the existing inverter/capacitor circuitry of Allen in order to provide protection from ESD events.

24. In re Claims 14 and 15, Allen and Loh teach that one or more PMOS devices are coupled between a first supply rail and the physical pad and one or more NMOS devices are coupled between the physical pad and a second supply rail having a value less than the first supply rail as seen in the respective Figures discussed above. Loh teaches in Paragraph 20 that the ESD

current is shunted to the capacitor. In order for this to occur, the PMOS as seen in Figure 3 would have to be enabled while the NMOS transistor as seen would have to be disabled in order for ESD current to flow from the high voltage supply line to the capacitor during a high voltage ESD event.

25. In re Claim 19, it should be understood that the electronic control circuit as taught by Loh requires some form of voltage supply to function and is therefore considered to be powered by a first supply rail.

26. In re Claim 20, Loh teaches that the control circuit sends a signal to the control block to activate a portion of the output buffer during an ESD event (Paragraphs 24-28).

27. In re Claim 22, Allen teaches a system as seen in Figure 2 comprising:

- A physical pad (19) having a capacitance (20)
- An output buffer (18B) coupled to the physical pad and operable to drive at least one output signal at the respective physical pad

28. Allen does not teach a control circuitry operable to activate at least a portion of the respective output buffer in response to an ESD event to charge the pad capacitance to reduce a maximum voltage developed as a result of an ESD.

29. Loh teaches an ESD protection circuit that utilizes existing circuitry of an IC, particularly an inverter and capacitor (as seen in Figure 3) in order to shunt ESD current [Paragraph 20-22].

Loh relies on a control block (606) to send a signal to the inverter in order to shunt ESD current to the capacitor when an ESD event is detected [Paragraph 24-28].

30. It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the control block of Loh in the existing inverter/capacitor circuitry of Allen in order to provide protection from ESD events.

31. In re Claim 23, Allen teaches functional circuitry (10A, 12A, 14A) coupled to the pad circuit operable to generate an output signal.

32. In re Claim 25, it should be understood that the electronic control circuit as taught by Loh requires some form of voltage supply to function and is therefore considered to be powered by a first supply rail.

33. In re Claim 26, the examiner considers the ground terminal disclosed in each reference as the second supply rail since it is required as a return path to provide power to the output buffer.

34. Claims 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Allen in view Loh as applied to claims 14 above, and further in view of Seo et al (U. S. Patent Publication 2006/0001448).

35. In re Claim 16, the teaching of Allen as modified by Loh has been discussed above. Furthermore, it is noted that Allen teaches a buffer circuit 18B that does not have one or more PMOS devices connected in parallel between a first voltage supply and pad and NMOS devices connected in series between a pad and second voltage supply.

36. Seo teaches placing the PMOS devices (301 and 302) in parallel and NMOS devices in series (305 and 304) in a buffer circuit as seen in Figure 3. The advantage of the buffer of Seo is to reduce signal slew and faulty logic level determination (Paragraphs 8 and 9).

37. It would have been obvious to one having ordinary skill in the art at the time the invention was made to replace the output buffer of Allen with the buffer circuit of Seo, since Seo teaches that including such an output buffer would reduce signal slew and faulty logic level determination.

38. Claims 9, 21 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Allen in view Loh as applied to claims 13 and 25 above, and further in view of Lien et al (U. S. Patent 7,102,862).

39. In re Claim 9, the teaching of Allen as modified by Loh has been discussed above, but does not teach turning on a clamp device in response to an ESD event.

40. Lien teaches that it is known to provide a clamp device between power rails in order to shunt excess energy (Column 1 Lines 10-67).

41. It would have been obvious to one having ordinary skill in the art at the time the invention was made to include a clamp device that responds to ESD events as taught by Lien in the invention of Allen as modified by Loh in order to provide further protection against ESD events.

42. In re Claims 21 and 27, the teaching of Allen as modified by Loh has been discussed above. Furthermore, Loh teaches a control circuit that outputs an ESD clock signal upon detecting an ESD event from a trigger circuit (610, Paragraph 25-28). Loh however does not specifically define how the ESD event is detected.

43. Lien teaches that it is known in the art to rely on a resistor/capacitor ESD detection circuit as seen in Figure 1A. Based on the values of the resistor and capacitor, a voltage having a specific slope and value is detected as being an ESD event.

44. It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the resistor/capacitor ESD detection circuit as taught by Lien as the ESD detecting circuit in Loh since Lien teaches that it is a known method in the art of providing indication of an ESD event.

Allowable Subject Matter

45. Claims 4, 17, 18, and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

46. Claim 4 recites a pad circuit that includes among other components a clamp device coupled between a second and third voltage rail wherein the enable circuitry is operable to turn on the clamp device. The featured limitations discussed above in combination with the other limitations of the claims is not anticipated by the prior art of record, nor would it have been obvious to one having ordinary skill in the art to modify the prior art of record in order to make the aforementioned limitations unpatentable.

47. Claims 17 and 18 recite a circuit configured to provide protection against ESD that includes among other components a clamp device configured to absorb, when turned on, a portion of an energy generated by the ESD event, wherein the control circuit is operable to turn on the clamp device in response to the ESD event. The featured limitations discussed above in combination with the other limitations of the claims is not anticipated by the prior art of record,

nor would it have been obvious to one having ordinary skill in the art to modify the prior art of record in order to make the aforementioned limitations unpatentable.

48. Claim 24 recites a system that includes among other components a clamp device configured to absorb, when turned on, a portion of an energy generated by the ESD event, wherein the control circuitry is operable to turn on the clamp device in response to the ESD event. The featured limitations discussed above in combination with the other limitations of the claims is not anticipated by the prior art of record, nor would it have been obvious to one having ordinary skill in the art to modify the prior art of record in order to make the aforementioned limitations unpatentable.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHRISTOPHER J. CLARK whose telephone number is (571)270-1427. The examiner can normally be reached on M-F, 7:30-5:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on 571-272-2084. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Michael J Sherry/
Supervisory Patent Examiner, Art Unit 2836

CJC
03/26/2008

Notice of References Cited	Application/Control No. 11/621,724		Applicant(s)/Patent Under Reexamination HOLLY ET AL.	
	Examiner CHRISTOPHER J. CLARK		Art Unit 2836	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2007/0019345	01-2007	Loh et al.	361/056
*	B	US-5,168,178	12-1992	Allen et al.	326/49
*	C	US-2006/0001448	01-2006	Seo et al.	326/080
*	D	US-7,102,862	09-2006	Lien et al.	361/56
	E	US-			
	F	US-			
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

<i>Index of Claims</i> 	Application/Control No. 11621724	Applicant(s)/Patent Under Reexamination HOLLY ET AL.
	Examiner CHRISTOPHER J CLARK	Art Unit 2836

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant										☐ CPA										☐ T.D.										☐ R.1.47									
CLAIM			DATE																																				
Final	Original	03/26/2008																																					
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Search Notes 	Application/Control No. 11621724	Applicant(s)/Patent Under Reexamination HOLLY ET AL.
	Examiner CHRISTOPHER J CLARK	Art Unit 2836

SEARCHED			
Class	Subclass	Date	Examiner
361	56	3/26/2008	CJC

SEARCH NOTES		
Search Notes	Date	Examiner

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner



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CONFIRMATION NO. 1652

SERIAL NUMBER 11/621,724	FILING or 371(c) DATE 01/10/2007 RULE	CLASS 361	GROUP ART UNIT 2836	ATTORNEY DOCKET NO. 5707-12800		
APPLICANTS Patrick J. Holly, Tempe, AZ; David Rodriguez, Phoenix, AZ; David R. Rice, Phoenix, AZ; ** CONTINUING DATA ***** ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 02/08/2007						
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and /Christopher Jay Clark/ Acknowledged Examiner's Signature		☐ Met after Allowance CJC Initials	STATE OR COUNTRY AZ	SHEETS DRAWINGS 1	TOTAL CLAIMS 27	INDEPENDENT CLAIMS 4
ADDRESS MEYERTONS, HOOD, KIVLIN, KOWERT & GOETZEL, P.C. P.O. BOX 398 AUSTIN, TX 78767-0398 UNITED STATES						
TITLE Pad ESD Spreading Technique						
FILING FEE RECEIVED 1550	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit			

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L3	520	trigger\$4 same slope same (time adj constant)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/26 13:53
L4	0	3 same esd	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/26 13:53
L5	2244	esd same trigger\$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/26 13:54
L6	116	5 same (time adj constant)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/26 13:54
L7	272	buffer with (nmos near4 series)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/26 14:45
L8	179	buffer with (nmos near4 series) with pmos	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/26 14:46
S1	6710	pad with capacitance	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/20 14:55
S2	936	S1 same transistor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/20 14:55

S3	127	S2 same control\$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/20 14:56
S4	52	S3 same output	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/20 14:57
S5	32	S3 same (esd electrostatic)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/20 14:57
S6	697	S1 same (esd electrostatic)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/20 15:14
S7	544	S1 with (esd electrostatic)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/20 15:15
S8	49	S7 same buffer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/20 15:15
S9	2885	361/56.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/20 15:24
S10	1392	S9 and (pad pin port)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/20 15:25

S11	411	S9 and ((pad pin port) with (capacitor capacitance))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/20 15:26
S12	16	S9 and ((pad pin port) with (capacitor capacitance) with buffer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/20 15:26
S15	0	(esd electrostatic) same (disipat\$4 with (pad pin))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/20 15:36
S16	2935	(esd electrostatic) same (output with (pad pin))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/20 15:37
S17	1540	(esd electrostatic) same (output near (pad pin))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/20 15:37
S18	177	(esd electrostatic) same ((output near (pad pin)) with buffer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/20 15:37
S19	670	(output near (pad pin)) with capacitance	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/20 16:31
S20	52	S19 same (esd electrostatic)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/20 16:31

S21	95	charg\$4 with parasitic with capacit\$4 with (pin pad)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/20 18:05
S22	8	S21 same (esd electrostatic)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/20 18:06
S23	3827	charg\$4 with capacit\$4 with (pin pad)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/20 18:10
S24	274	S23 same (esd electrostatic)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/20 18:24
S25	13421	discharg\$4 near4 (pin pad)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/20 18:33
S26	430	discharg\$4 near4 (output adj (pin pad))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/20 18:33
S27	223	S26 same (esd electrostatic)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/20 18:33
S28	2364	pad with spreading	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/20 19:13

S29	6	S28 with (esd electrostatic)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/20 19:14
S30	41	S27 same buffer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/20 19:42
S31	2885	361/56.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/21 14:48
S32	2885	S31	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/21 14:48
S33	30	S31 and (capacit\$4 near absorb\$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/21 14:49
S34	144	S31 and (capacit\$4 near transistor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/21 14:51
S35	84	S31 and (capacitor near transistor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/21 14:52
S36	191749	transistor with capacitor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/21 15:52

S37	121089	capacitor near4 ((discharg \$4 absorb\$4))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/21 15:53
S38	21	esd with transistor with (capacitor near4 ((discharg \$4 absorb\$4)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/21 15:54
S39	0	("2007/0019345").URPN.	USPAT	OR	ON	2008/03/21 15:57
S40	1	"5907464".pn.	USPAT	OR	ON	2008/03/21 15:59
S41	31	("5400202" "5530612" "5543650" "5654862"). PN. OR ("5907464"). URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2008/03/21 16:00
S42	518	capacitor near3 esd	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/21 16:03
S43	29	(capacitor near3 esd) with (buffer inverter)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/21 16:11
S44	16	(capacitor near3 esd) with shunt\$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/21 16:42
S45	252	(output adj pad) with capacitance	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/21 16:58
S46	56	S45 same (buffer inverter)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/21 16:58

S47	13	S46 same esd	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/21 16:59
S48	25	(output adj pad) near capacitance	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/21 17:02
S49	125	(output adj pad) near buffer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/21 17:28
S50	0	(output adj pad) near ((inherent intrinsic) adj capacitance)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/21 17:58
S51	1	(output adj pad) with ((inherent intrinsic) adj capacitance)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/21 17:58
S52	252	(output adj pad) with (capacitance)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/21 17:59
S53	25	(output adj pad) near (capacitance)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/21 17:59
S54	47	("5208719" "5223737" "5707886" "5717560" "5907464" "5956219" "6008970" "6157065" "6577481" "6690555" "6744610" "6747501" "6760209" "6768176" "6788507" "6800906" "6829126" "6838775" "6844595" "6864536" "6876529" "7019366" "7106563").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/21 19:41

S55	23	("5208719" "5223737" "5707886" "5717560" "5907464" "5956219" "6008970" "6157065" "6577481" "6690555" "6744610" "6747501" "6760209" "6768176" "6788507" "6800906" "6829126" "6838775" "6844595" "6864536" "6876529" "7019366" "7106563").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2008/03/21 19:41
S56	1	"6552583".pn.	US-PGPUB; USPAT; USOCR	OR	ON	2008/03/25 20:58
S57	23	("4678950" "4855620" "5208719" "5287241" "5442217" "5537067" "5631793" "5686751" "5710682" "5729419" "5959488" "5982217" "5986867" "5990723" "6064556" "6118323" "6118640" "6249410"). PN. OR ("6552583"). URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2008/03/25 21:01
S58	1	"5907464".pn.	US-PGPUB; USPAT; USOCR	OR	ON	2008/03/25 21:23

3/ 26/ 2008 3:59:02 PM

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		11621724
	Filing Date		2007-01-10
	First Named Inventor	Patrick J. Holly	
	Art Unit	2836	
	Examiner Name	Unknown	
	Attorney Docket Number	5707-12800	

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Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
/CC/ 	1	5717560		1998-02-10	Doyle, et al.	
	2	5907464		1999-05-25	Maloney, et al.	
	3	5956219		1999-09-21	Timothy J. Maloney	
	4	6008970		1999-12-28	Maloney, et al.	
	5	6577481	B2	2003-06-10	Steinhoff, et al.	
	6	6690555	B1	2004-02-10	Ronald Pasqualini	
	7	6744610	B2	2004-06-01	Chang, et al.	
	8	6747501	B2	2004-06-08	Ker, et al.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	11621724	11621724 - GAU: 2836
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	First Named Inventor	Patrick J. Holly	
	Art Unit	2836	
	Examiner Name	Unknown	
	Attorney Docket Number	5707-12800	

/CC/	9	6760209	B1	2004-06-07	Bradley A. Sharpe-Geisler	
	10	6768176	B1	2004-07-27	David D. Litfin	
	11	6788507	B2	2004-09-07	Chen, et al.	
	12	6800906	B2	2004-10-05	Jyh-Nan Cheng	
	13	6829126	B2	2004-12-07	Lee, et al.	
	14	6838775	B2	2005-01-04	Makoto Takahashi	
	15	6844595	B2	2005-01-18	Wei-Fan Chen	
	16	6864536	B2	2005-03-08	Lin, et al.	
	17	6876529	B2	2005-04-05	Larry B. Li	
	18	7106563	B2	2006-09-12	Lai, et al.	
	19	7019366	B1	2006-03-28	Yang, et al.	

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	Filing Date		2007-01-10	
	First Named Inventor	Patrick J. Holly		
	Art Unit	2836		
	Examiner Name	Unknown		
	Attorney Docket Number	5707-12800		

/CC/	20	6157065		2000-12-05	Huang, et al.	
/CC/	21	5707886		1998-01-13	Consiglio, et al.	
/CC/	22	5223737		1993-06-12	Athos Canciani	
/CC/	23	5208719		1993-05-04	Yi-Hen Wei	

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	Filing Date		2007-01-10	
	First Named Inventor	Patrick J. Holly		
	Art Unit	2836		
	Examiner Name	Unknown		
	Attorney Docket Number	5707-12800		

/CC/	1	TIMOTHY J. MALONEY, STEVEN S. POON and LAWRENCE T. CLARK; "Methods for Designing Low-leakage Power Supply Clamps"; Proceedings of Electrical Overstress Electrostatic Discharge Symposium; 2003, 7 pages; Intel Corporation.	☐
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Examiner Signature	/Christopher Clark/	Date Considered	/Christopher Clark/
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¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	11621724	11621724 - GAU: 2836
	Filing Date	2007-01-10	
	First Named Inventor	Patrick J. Holly	
	Art Unit	2836	
	Examiner Name	Unknown	
	Attorney Docket Number	5707-12800	

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Jeffrey C. Hood/	Date (YYYY-MM-DD)	2007-02-23
Name/Print	Jeffrey C. Hood	Registration Number	35,198

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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

~~ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /CC/~~

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.:	11/621,724	§	Examiner:	Clark, Christopher
Filed:	January 10, 2007	§		Jay
Inventor(s):		§	Group/Art Unit:	2836
	Patrick J. Holly, David	§	Atty. Dkt. No:	5707-12800
	Rodriguez, David R. Rice	§		
Title:	PAD ESD TECHNIQUE	§		
		§		
		§		
		§		
		§		
		§		

**RESPONSE TO OFFICE ACTION OF
APRIL 4, 2008**

Dear Sir or Madam:

This paper is submitted in response to the Office Action of April 4, 2008, to further highlight why the application is in condition for allowance.

Please amend the case as listed below.

IN THE CLAIMS:

The following listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Original) A pad circuit configured to provide protection against electrostatic discharge (ESD) in a system comprising the pad circuit, the pad circuit comprising:

a first node coupled to a first voltage rail;

a second node coupled to a physical pad having capacitance;

one or more output transistor devices coupled between the first node and the second node, and operable to at least partially drive an output signal at the second node; and

a control block operable to turn on at least one of the one or more output transistor devices in response to an ESD event to charge the pad capacitance, thereby reducing a maximum voltage developed in the system as a result of the ESD event.

2. (Original) The pad circuit of claim 1, wherein in turning on the at least one of the one or more output transistor devices in response to the ESD event, the control block is further operable to couple the first voltage rail and its associated capacitance to the physical pad to share a charge developed in the system in response to the ESD event, thereby reducing the maximum voltage developed in the system as the result of the ESD event.

3. (Original) The pad circuit of claim 1, further comprising enable circuitry operable to send a control signal to the control block in response to the ESD event to instruct the control block to turn on the at least one of the one or more output transistor devices.

4. (Original) The pad circuit of claim 3, further comprising:

a clamp device coupled between a second voltage rail and a third voltage rail, wherein the second voltage rail is configured to provide power to the enable circuitry, and wherein the third voltage rail has a value below the first voltage rail;

wherein the enable circuitry is operable to turn on the clamp device to reduce the maximum voltage developed in the system as the result of the ESD event.

5. (Original) The pad circuit of claim 1, wherein the one or more output transistor devices are PMOS devices, wherein the at least one of the one or more transistor devices comprises:

a subset of the PMOS devices; or
the PMOS devices.

6. (Original) The pad circuit of claim 5, further comprising one or more NMOS devices coupled between the second node and a second voltage rail that has a value below the first voltage rail, wherein the NMOS devices and the PMOS devices are operable to operate together to drive the output signal at the second node, wherein the logic circuit is operable to have the NMOS devices turned off during the ESD event.

7. (Original) The pad circuit of claim 1, wherein the pad circuit and the physical pad are comprised in a digital input/output pad.

8. (Original) A method for protecting a system against electrostatic discharge (ESD), the method comprising:

turning on at least one of one or more output transistor devices in response to an ESD event to charge a pad capacitance, to thereby reduce a maximum voltage developed in the system as a result of the ESD event;

wherein the one or more output transistor devices are configured in the system, and are coupled to a physical pad having the pad capacitance, and wherein the one or more output transistor devices are operable to drive an output signal at the physical pad.

9. (Original) The method of claim 8, further comprising:

turning on a clamp device in response to the ESD event, wherein the clamp device is configured to absorb, when turned on, a portion of an energy generated by the ESD event, to thereby reduce the maximum voltage developed in the system as the result of the ESD event.

10. (Original) The method of claim 8;
wherein the one or more transistor devices comprise one or more PMOS devices;
wherein said turning on the at least one of the one or more output transistor devices comprises:

turning on at least one of the one or more PMOS devices; or
turning on the one or more PMOS devices.

11. (Original) The method of claim 10;
wherein the one or more transistor devices further comprise one or more NMOS devices;
wherein the method further comprises disabling the one or more NMOS devices during the ESD event.

12. (Original) The method of claim 11, wherein the physical pad is an input/output pad.

13. (Original) A circuit configured to provide protection against electrostatic discharge (ESD) in a system comprising the circuit, the circuit comprising:
an output buffer configured to couple to a physical pad having capacitance, and operable to drive at least one output signal at the physical pad;
a control block configured to control the output buffer; and
a control circuit configured to instruct the control block to activate at least a portion of the output buffer when an ESD event occurs, thereby charging the pad capacitance to reduce a maximum voltage developed in the system as a result of the ESD event.

14. (Original) The circuit of claim 13, wherein the output buffer comprises:
one or more PMOS devices coupled between a first supply rail and the physical pad; and
one or more NMOS devices coupled between the physical pad and a second supply rail having a value less than the first supply rail;
wherein in activating at least a portion of the output buffer when the ESD event occurs, the control block is operable to:
enable at least one of the one or more PMOS devices; or
enable the one or more PMOS devices.

15. (Original) The circuit of claim 14, wherein in activating at least a portion of the output buffer when the ESD event occurs, the control block is operable to:
disable at least one of the one or more NMOS devices; or
disable the one or more NMOS devices.

16. (Original) The circuit of claim 14, wherein the one or more PMOS devices are coupled in parallel between the first supply rail and the physical pad, and the NMOS devices are coupled in series between the physical pad and the second supply rail.

17. (Original) The circuit of claim 13, further comprising a clamp device coupled between a first supply rail configured to provide power to the control circuit, and a low supply rail;
wherein the clamp device is configured to absorb, when turned on, a portion of an energy generated by the ESD event, to thereby reduce the maximum voltage developed in the system as the result of the ESD event;
wherein the control circuit is operable to turn on the clamp device in response to the ESD event.

18. (Original) The circuit of claim 17, wherein the clamp device is one of:

a PMOS device having its source terminal coupled to the first supply rail, its drain terminal coupled to the low supply rail, and its gate terminal coupled to the control circuit; or

an NMOS device having its drain terminal coupled to the first supply rail, its source terminal coupled to the low supply rail, and its gate terminal coupled the control circuit.

19. (Original) The circuit of claim 13, wherein the control circuit is configured to be powered by a first supply rail operable to provide increased power during the ESD event.

20. (Original) The control circuit of claim 13, wherein in instructing the control block to activate at least a portion of the output buffer when an ESD event occurs, the control circuit is operable to provide a control signal to the control block in response to the ESD event.

21. (Original) The circuit of claim 13, wherein the control circuit is configured to receive a control signal corresponding to a time constant, wherein the time constant corresponds to a specified slope, wherein the control signal is configured to trigger the control circuit if a slope of a voltage pulse developed in the system as a result of the ESD event is greater than or equal to the specified slope.

22. (Original) A system comprising:

one or more pads, each pad comprising:

a respective physical pad having respective capacitance; and

a respective pad circuit comprising:

a respective output buffer coupled to the respective physical pad, and operable to drive at least one respective output signal at the respective physical pad; and

respective control circuitry operable to activate at least a portion of the respective output buffer in response to an ESD event to charge the respective pad

capacitance to reduce a maximum voltage developed in the system as a result of the ESD event.

23. (Original) The system of claim 22, further comprising functional circuitry coupled to the respective pad circuit of at least one of the one or more pads, wherein the functional circuitry is operable to generate the at least one respective output signal driven by the respective pad circuit of the at least one of the one or more pads.

24. (Original) The system of claim 22, wherein each pad further comprises a respective clamp device configured to absorb, when turned on, a portion of an energy generated by the ESD event, to thereby further reduce the maximum voltage developed in the system as the result of the ESD event;

wherein the respective control circuitry of the respective pad circuit of each pad is operable to turn on the clamp device in response to the ESD event.

25. (Original) The system of claim 22, further comprising a first supply rail configured to provide increased power in accordance with the ESD event, and further configured to power the respective control circuitry of the respective pad circuit of each pad.

26. (Original) The system of claim 25, further comprising a second supply rail configured to power the respective output buffer of the respective pad circuit of each pad.

27. (Original) The system of claim 25, wherein the respective control circuitry of the respective pad circuit of each pad is configured to receive a respective control signal corresponding to a time constant, wherein the time constant corresponds to a specified slope, wherein the respective control signal is configured to trigger the respective control circuitry if a slope of a voltage pulse developed in the system as a result of the ESD event is greater than or equal to the specified slope.

REMARKS

Applicant is in receipt of the Office Action mailed April 4, 2008.

Applicant notes that an information disclosure statement was submitted electronically on February 23, 2007. Applicant notes that all references have been initialed and signed but that Examiner did not date the information disclosure statement. Applicant respectfully requests a correctly dated information disclosure statement.

35 U.S.C. § 103 Rejection:

Claims 1-3, 5-8, 10-15, 19, 20, 22, 23, 25, and 26 were rejected under 35 U.S.C. 103(a) as being unpatentable over Allen et al (U. S. Patent 5,168,178) in view of Loh et al (U. S. Patent Publication 2007/0019345). Claim 16 was rejected under 35 U.S.C. 103(a) as being unpatentable over Allen in view Loh as applied to claims 14 above, and further in view of Seo et al (U. S. Patent Publication 2006/0001448). Claims 9, 21 and 27 were rejected under 35 U.S.C. 103(a) as being unpatentable over Allen in view Loh as applied to claims 13 and 25 above, and further in view of Lien et al (U. S. Patent 7,102,862). With respect to these claims, Applicant respectfully traverses this rejection.

The cited references taken singly or in combination do not teach or suggest all of the elements of the independent claims.

For example, independent claim 1 recites:

A pad circuit configured to provide protection against electrostatic discharge (ESD) in a system comprising the pad circuit, the pad circuit comprising:

- a first node coupled to a first voltage rail;
- a second node coupled to a physical pad having capacitance;

one or more output transistor devices coupled between the first node and the second node, and operable to at least partially drive an output signal at the second node; and

a control block operable to turn on at least one of the one or more output transistor devices in response to an ESD event to charge the pad capacitance, thereby reducing a maximum voltage developed in the system as a result of the ESD event.

Allen and Loh, taken singly or in combination, do not teach, suggest, or render obvious at least a control block operable to turn on at least one of one or more output transistor devices [operable to at least partially drive an output signal at the second node coupled to a physical pad having capacitance] in response to an ESD event to charge the pad capacitance, thereby reducing a maximum voltage developed in the system as a result of the ESD event. The Office Action acknowledges that Allen does not teach a control block operable to turn on at least one of the one or more output transistor devices in response to an ESD event to charge the pad capacitance to reduce a maximum voltage developed as a result of an ESD. The Office Action however argues that Loh teaches an ESD protection circuit that utilizes existing circuitry of an IC, particularly an inverter and capacitor (as seen in Figure 3) in order to shunt ESD current [Paragraph 20-22]. The Office Action further states that Loh relies on a control block (606) to send a signal to the inverter in order to shunt ESD current to the capacitor when an ESD event is detected [Paragraph 24-28]. The Office Action subsequently argues that it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the control block of Loh in the existing inverter/capacitor circuitry of Allen in order to provide protection from ESD events.

Applicant, however, respectfully submits that combining the control block of Loh in the existing circuitry of Allen does not result in the combination of features recited in the claims, because such a combination would still fail to *turn on at least one of the one or more output transistor devices [that are operable to at least partially drive an output signal at the pad] in response to an ESD event to charge the pad capacitance, thereby reducing a maximum voltage developed in the system as a result of the ESD event.*

Applicant also notes that the reference to “control block (606)” in Loh as presented in the Office Action is unclear, as none of the figures of Loh feature such an element. Applicant has however identified in the File History of Loh a replacement sheet submitted for the Application of Loh, which features a revised Fig. 6. Applicant therefore assumes that all references to element 606 and Fig. 6 of Loh that were made in the Office Action were in reference to that replacement figure.

With regards to Loh, Applicant respectfully submits that Loh teaches a specific protection circuit that requires specific elements, namely transistors 304 and 306, and capacitor 308 to perform the necessary protection against ESD events. Because Loh only teaches how the control circuit it discloses may control the specific inverter and capacitor circuit also disclosed by Loh, there is no indication how this control circuit may be used to control any other type of circuit in general, or more specifically, any other type of circuit configured to protect against ESD events. Therefore, it is neither obvious nor inherent in Loh, how the control circuit of Loh may be combined with Allen to obtain the combination of features recited in Applicant’s claims, more specifically, how the control circuit of Loh may be adapted to control one or more transistors that are configured as part of a pad circuit, operable to drive an output signal at the second node (pad). The operation of pad circuits is different from that of an inverter, thus the control circuit disclosed by Loh as specifically controlling an inverter circuit coupled to a capacitor, cannot be automatically or obviously used to control output transistors in a pad circuit, without also affecting normal operation of the pad circuit.

Loh discloses various circuits that comprise a pad, but no mention, suggestion, or teaching is provided in Loh regarding the use of any of these pads in protecting against ESD events. As a matter of fact, by explicitly teaching the additional capacitor as a required element in the protection circuit (disclosed in Fig. 3) that may be controlled by the trigger circuit (disclosed in Figs. 6 and 7), Loh teaches away from any use of the pad and corresponding I/O circuit in providing ESD protection. In Fig. 8, Loh provides a schematic diagram of an I/O circuit with which the protection circuit of FIG. 3 can be implemented, and Fig. 8 clearly discloses a pad 802, where the I/O circuit 800 couples between an input/output (I/O) pad 802 and the circuit core 400, which includes the protection circuits 300 [see paragraph 0034]. Because the control circuit disclosed by

Loh is configured to control the protection circuit 300, and not the output at the pad, such a control circuit cannot be combined with Allen to control an output transistor configured within the I/O (pad) circuit and expect the pad (I/O) circuit to continue operating as desired and/or required.

Claim 1 recites one or more output transistor devices coupled between the first node and the second node, operable to at least partially drive an output signal at the second node, which is coupled to a physical pad having pad capacitance, and a control block operable to turn on at least one of the one or more output transistor devices in response to an ESD event to charge the pad capacitance. Applicant respectfully submits that if using the pad and/or pad circuit in providing ESD protection was in any way obvious or anticipated, Loh would have been expected to provide at least some teaching to that effect, and would not have specified using an additional capacitor (as shown in Fig. 3), considering the presence of pads and pad circuits in many of the embodiments and prior art systems disclosed in Loh (see Figs. 1, 6, 7, and 8). Loh would also have expected to provide at least some teaching suggesting adapting such a control circuit to operate with output transistors within a pad circuit, if such a solution was obvious, yet Loh fails to suggest, and is completely silent regarding any such possibility.

Applicant therefore submits that combining Loh with Allen does not result in the combination of features recited in the claims, since the control circuit in Loh is not adapted to turn on at least one of the one or more output transistor devices (operable to at least partially drive an output signal at the second node [pad]) in response to an ESD event to charge the pad capacitance, thereby reducing a maximum voltage developed in the system as a result of the ESD event. None of the embodiments of Loh comprise a control block operable to activate at least a portion of an output transistor or buffer when an ESD event occurs, thereby charging the pad capacitance to reduce a maximum voltage developed in the system as a result of the ESD event, where the output transistor or buffer is operable to drive at least one output signal at the physical pad. The control circuit of Loh can therefore not be combined with Allen to produce the combination of features recited in the claims, because the operation of a pad circuit is different from that of an inverter, and Applicant's claims explicitly recite charging a pad capacitance.

The same arguments also apply to claims 8, 13, and 22.

For at least these reasons, Applicant submits that the combinations of features recited in independent claims 1, 8, 13, and 22 are patentably distinct over Allen and Loh, whether taken singly or in combination. Applicant also submits that since independent claims 1, 8, 13, and 22 have been shown to be patentably distinct, their respective dependent claims are also patentably distinct for at least the same reasons. Accordingly, Applicant respectfully requests removal of the 35 U.S.C. § 103(a) rejection.

Allowable Subject Matter:

Claims 4, 17, 18, and 24 were objected to as being dependent upon a rejected base claim, but were deemed to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicant appreciates and acknowledges the allowable subject matter, and submits that these claims are also allowable for at least the reasons shown above, in addition to the reasons cited in the Office Action.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above-referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. The Commissioner is hereby authorized to charge any fees which may be required or credit any overpayment to Meyertons, Hood, Kivlin, Kowert & Goetzel P.C., Deposit Account No. 50-1505/5707-12800/JCH.

Also filed herewith are the following items:

- ☐ Request for Continued Examination
- ☐ Terminal Disclaimer
- ☐ Power of Attorney By Assignee and Revocation of Previous Powers
- ☐ Notice of Change of Address
- ☐ Other:

Respectfully submitted,

/Jeffrey C. Hood/

Jeffrey C. Hood, Reg. #35198
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Date: 2008-07-03 JCH/TAK

Electronic Acknowledgement Receipt

EFS ID:	3568401
Application Number:	11621724
International Application Number:	
Confirmation Number:	1652
Title of Invention:	Pad ESD Spreading Technique
First Named Inventor/Applicant Name:	Patrick J. Holly
Customer Number:	35690
Filer:	Jeffrey C Hood/Jeannie Miranda
Filer Authorized By:	Jeffrey C Hood
Attorney Docket Number:	5707-12800
Receipt Date:	03-JUL-2008
Filing Date:	10-JAN-2007
Time Stamp:	18:28:16
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1		5707-12800_Resp_OA_2008-04-04.pdf	131482 d9cc55c591845023f0e04c127efc7eabb0931108	yes	13

MCHP_00000100

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Amendment - After Non-Final Rejection	1	1
	Claims	2	7
	Applicant Arguments/Remarks Made in an Amendment	8	13
Warnings:			
Information:			
Total Files Size (in bytes):		131482	
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/621,724	01/10/2007	Patrick J. Holly	5707-12800

CONFIRMATION NO. 1652

PUBLICATION NOTICE

35690
MEYERTONS, HOOD, KIVLIN, KOWERT & GOETZEL, P.C.
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OC000000030893461

Date Mailed: 07/10/2008

Title: Pad ESD Spreading Technique

Publication No. US-2008-0165459-A1

Publication Date: 07/10/2008

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publicly available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently <http://www.uspto.gov/patft/>.

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 11/621,724		Filing Date 01/10/2007		☐ To be Mailed		
APPLICATION AS FILED – PART I											
(Column 1)			(Column 2)		SMALL ENTITY ☐		OR		OTHER THAN SMALL ENTITY		
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)			RATE (\$)	FEE (\$)			
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A				N/A				
☐ SEARCH FEE (37 CFR 1.16(k), (j), or (m))	N/A	N/A	N/A				N/A				
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A				N/A				
TOTAL CLAIMS (37 CFR 1.16(j))	minus 20 =	*	X \$	=			OR	X \$	=		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$	=				X \$	=		
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).										
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))											
* If the difference in column 1 is less than zero, enter "0" in column 2.											
APPLICATION AS AMENDED – PART II										TOTAL	
(Column 1)			(Column 2)		(Column 3)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY		
AMENDMENT	07/03/2008	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)		RATE (\$)	ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	* 27	Minus	** 27	= 0	X \$	=	OR	X \$50=	0	
	Independent (37 CFR 1.16(h))	* 4	Minus	***4	= 0	X \$	=	OR	X \$210=	0	
	☐ Application Size Fee (37 CFR 1.16(s))										
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
	TOTAL ADD'L FEE										
(Column 1)										TOTAL ADD'L FEE	0
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)		RATE (\$)	ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$	=	OR	X \$	=	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$	=	OR	X \$	=	
	☐ Application Size Fee (37 CFR 1.16(s))										
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
	TOTAL ADD'L FEE										
TOTAL ADD'L FEE										TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.											

Legal Instrument Examiner:
/Trina Steptoe/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/621,724	01/10/2007	Patrick J. Holly	5707-12800	1652

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EXAMINER	
CLARK, CHRISTOPHER JAY	

ART UNIT	PAPER NUMBER
2836	

MAIL DATE	DELIVERY MODE
11/13/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	11/621,724	HOLLY ET AL.	
	Examiner	Art Unit	
	CHRISTOPHER J. CLARK	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on 03 July 2008.

2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) 1-27 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) 1-3, 8-16, 19-23 and 25-27 is/are rejected.

7) ☒ Claim(s) 4, 17, 18, and 24 is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) ☐ All b) ☐ Some * c) ☐ None of:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892) 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.	4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____. 5) ☐ Notice of Informal Patent Application 6) ☐ Other: _____.
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DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed July 3, 2008 have been fully considered but they are not persuasive. The previous rejection has been updated to provide clarification and address arguments of the applicant below.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-3, 5-8, 10-15, 19, 20, 22, 23, 25, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Loh et al (U. S. Patent Publication 2007/0019345) in view of Allen et al (U. S. Patent 5,168,178).

3. In re Claim 1, Loh teaches a pad circuit as seen in Figure 3 comprising:

- A first node coupled to a first voltage rail (the source of FET 304)
- A second node coupled to a physical pad having capacitance (308)
- One or more output transistor devices (304 and 306) coupled between the first node and the second node and operable to at least partially drive an output signal at the second node ("V(t)")
- a control block (606) operable to turn on at least one of the one or more output transistor devices in response to an ESD event to charge the pad capacitance to reduce a maximum voltage developed as a result of an ESD (Paragraph 24-28)

4. Loh further teaches an ESD protection circuit that utilizes existing circuitry of an IC, particularly an inverter and capacitor (as seen in Figure 3) which drive an output signal to a load inside of the core circuitry, in order to shunt ESD current [Paragraph 20-22].

5. Loh does not teach the capacitor being a capacitance of a physical pad.

6. Allen teaches that it is known in the art to provide the same circuit setup consisting of two output transistors (22 and 24) and a capacitor [via pad (20) with a parasitic capacitance (19)] as seen in Figure 2. The circuit of Allen demonstrates that a capacitance is available to an inverter circuit of an internal circuit in the form of a pad when the core circuitry is providing an output to a load that is external to the core circuitry.

7. It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the protection scheme of Loh using an inverter of the core circuitry which was providing an output signal external to the core circuitry and connected to an output pad, since Allen teaches that it is known in the art to connect an inverter circuit to an external load via a pad with parasitic capacitance.

8. In re Claim 2, Loh teaches that first voltage rail is coupled to the capacitance to share a charge developed in the system in response to the ESD event and reducing maximum voltage developed in the system as a result of the ESD (Paragraph 20). Upon being modified by Loh as discussed above, it is to be understood that the capacitance is associated with the pad as taught by Allen.

9. In re Claim 3, Loh teaches enable circuitry (610) that sends a control signal to the control block in response to the ESD event to instruct the control block to turn on the one or more output transistors (Paragraphs 25-28).

10. In re Claim 5, both Loh and Allen teach that the output transistors are PMOS as seen in the Figures discussed above.

11. In re Claim 6, both Loh and Allen teach that the output transistors are also NMOS as seen in the Figures discussed above. Loh teaches in Paragraph 20 that ESD current is shunted to the capacitor. In order for this to occur, the NMOS transistor as seen in Figure 3 would have to be in a "turned off" state in order for ESD current to flow from the high voltage supply line to the capacitor during a high voltage ESD event.

12. In re Claim 7, Allen teaches that the pad is an output pad that receives digital outputs (Column 1 Lines 25-33).

13. In re Claim 8, Loh teaches as seen in Figure 3, turning on one or more output transistors (304 and 306) in response to an ESD event to charge a capacitance (308) to thereby reduce a maximum voltage developed in the system as a result of the ESD event [Paragraphs 20-28], wherein the one or more output transistor devices are operable to drive an output signal at the physical pad as well turning on ("V(t)")

14. Loh further teaches an ESD protection circuit that utilizes existing circuitry of an IC, particularly an inverter and capacitor (as seen in Figure 3) which drive an output signal to a load inside of the core circuitry, in order to shunt ESD current [Paragraph 20-22].

15. Loh does not teach the capacitor being a capacitance of a physical pad.

16. Allen teaches that it is known in the art to provide the same circuit setup consisting of two output transistors (22 and 24) and a capacitor [via pad (20) with a parasitic capacitance (19)] as seen in Figure 2. The circuit of Allen demonstrates that a capacitance is available to an

inverter circuit of an internal circuit in the form of a pad when the core circuitry is providing an output to a load that is external to the core circuitry.

17. It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the protection scheme of Loh using an inverter of the core circuitry which was providing an output signal external to the core circuitry and connected to an output pad, since Allen teaches that it is known in the art to connect an inverter circuit to an external load via a pad with parasitic capacitance.

18. In re Claim 10, both Loh and Allen teach that the output transistors are PMOS as seen in the Figures discussed above.

19. In re Claim 11, both Loh and Allen teach that the output transistors are also NMOS as seen in the Figures discussed above. Loh teaches in Paragraph 20 that ESD current is shunted to the capacitor. In order for this to occur, the NMOS transistor as seen in Figure 3 would have to be in a "turned off" state in order for ESD current to flow from the high voltage supply line to the capacitor during a high voltage ESD event.

20. In re Claim 12, Allen teaches that the pad is an output pad that receives digital outputs (Column 1 Lines 25-33).

21. In re Claim 13, Loh teaches a circuit in a system as seen in Figure 3 comprising:

- an output buffer (302) configured to couple to a capacitance (308) and operable to drive at least one output signal at output
- a control block (606) configured to control the output buffer
- a control circuit (610 as seen in the revised Figure 6 correctly recognized by the Applicant) configured to instruct the control block to activate at least a portion of the

output buffer when an ESD event occurs, thereby charging the capacitance to reduce a maximum voltage developed in the system as a result of the ESD event [paragraphs 20-28)

22. Loh further teaches an ESD protection circuit that utilizes existing circuitry of an IC, particularly an inverter and capacitor (as seen in Figure 3) which drive an output signal to a load inside of the core circuitry, in order to shunt ESD current [Paragraph 20-22].

23. Loh does not teach the capacitor being a capacitance of a physical pad.

24. Allen teaches that it is known in the art to provide the same circuit setup consisting of two output transistors (22 and 24) and a capacitor [via pad (20) with a parasitic capacitance (19)] as seen in Figure 2. The circuit of Allen demonstrates that a capacitance is available to an inverter circuit of an internal circuit in the form of a pad when the core circuitry is providing an output to a load that is external to the core circuitry.

25. It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the protection scheme of Loh using an inverter of the core circuitry which was providing an output signal external to the core circuitry and connected to an output pad, since Allen teaches that it is known in the art to connect an inverter circuit to an external load via a pad with parasitic capacitance.

26. In re Claims 14 and 15, Allen and Loh teach that one or more PMOS devices are coupled between a first supply rail and the physical pad and one or more NMOS devices are coupled between the physical pad and a second supply rail having a value less than the first supply rail as seen in the respective Figures discussed above. Loh teaches in Paragraph 20 that the ESD current is shunted to the capacitor. In order for this to occur, the PMOS as seen in Figure 3

would have to be enabled while the NMOS transistor as seen would have to be disabled in order for ESD current to flow from the high voltage supply line to the capacitor during a high voltage ESD event.

27. In re Claim 19, it should be understood that the electronic control circuit as taught by Loh requires some form of voltage supply to function and is therefore considered to be powered by a first supply rail.

28. In re Claim 20, Loh teaches that the control circuit sends a signal to the control block to activate a portion of the output buffer during an ESD event (Paragraphs 24-28).

29. In re Claim 22, Loh teaches a system as seen in Figure 3 comprising:

- A capacitance (308)
- An output buffer (302) coupled to the physical pad and operable to drive at least one output signal at output
- Control circuitry (606) operable to activate a portion of the output buffer in response to an ESD event to charge the capacitance to reduce a maximum voltage developed in the system as a result of the ESD event [Paragraphs 20-28]

30. Loh further teaches an ESD protection circuit that utilizes existing circuitry of an IC, particularly an inverter and capacitor (as seen in Figure 3) which drive an output signal to a load inside of the core circuitry, in order to shunt ESD current [Paragraph 20-22].

31. Loh does not teach the capacitor being a capacitance of a physical pad.

32. Allen teaches that it is known in the art to provide the same circuit setup consisting of two output transistors (22 and 24) and a capacitor [via pad (20) with a parasitic capacitance (19)]

as seen in Figure 2. The circuit of Allen demonstrates that a capacitance is available to an inverter circuit of an internal circuit in the form of a pad when the core circuitry is providing an output to a load that is external to the core circuitry.

33. It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the protection scheme of Loh using an inverter of the core circuitry which was providing an output signal external to the core circuitry and connected to an output pad, since Allen teaches that it is known in the art to connect an inverter circuit to an external load via a pad with parasitic capacitance.

34. In re Claim 23, Allen teaches functional circuitry (10A, 12A, 14A) coupled to the pad circuit operable to generate an output signal.

35. In re Claim 25, it should be understood that the electronic control circuit as taught by Loh requires some form of voltage supply to function and is therefore considered to be powered by a first supply rail.

36. In re Claim 26, the examiner considers the ground terminal disclosed in each reference as the second supply rail since it is required as a return path to provide power to the output buffer.

37. Claims 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Loh in view of Allen as applied to claims 14 above, and further in view of Seo et al (U. S. Patent Publication 2006/0001448).

38. In re Claim 16, the teaching of Loh as modified by Allen has been discussed above. Furthermore, it is noted that Allen teaches a buffer circuit 18B that does not have one or more

PMOS devices connected in parallel between a first voltage supply and pad and NMOS devices connected in series between a pad and second voltage supply.

39. Seo teaches placing the PMOS devices (301 and 302) in parallel and NMOS devices in series (305 and 304) in a buffer circuit as seen in Figure 3. The advantage of the buffer of Seo is to reduce signal slew and faulty logic level determination (Paragraphs 8 and 9).

40. It would have been obvious to one having ordinary skill in the art at the time the invention was made to replace the output buffer of Allen with the buffer circuit of Seo, since Seo teaches that including such an output buffer would reduce signal slew and faulty logic level determination.

41. Claims 9, 21 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Loh in view of Allen as applied to claims 13 and 25 above, and further in view of Lien et al (U. S. Patent 7,102,862).

42. In re Claim 9, the teaching of Loh as modified by Allen has been discussed above, but does not teach turning on a clamp device in response to an ESD event.

43. Lien teaches that it is known to provide a clamp device between power rails in order to shunt excess energy (Column 1 Lines 10-67).

44. It would have been obvious to one having ordinary skill in the art at the time the invention was made to include a clamp device that responds to ESD events as taught by Lien in the invention of Allen as modified by Loh in order to provide further protection against ESD events.

45. In re Claims 21 and 27, the teaching of Loh as modified by Allen has been discussed above. Furthermore, Loh teaches a control circuit that outputs an ESD clock signal upon detecting an ESD event from a trigger circuit (610, Paragraph 25-28). Loh however does not specifically define how the ESD event is detected.

46. Lien teaches that it is known in the art to rely on a resistor/capacitor ESD detection circuit as seen in Figure 1A. Based on the values of the resistor and capacitor, a voltage having a specific slope and value is detected as being an ESD event.

47. It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the resistor/capacitor ESD detection circuit as taught by Lien as the ESD detecting circuit in Loh since Lien teaches that it is a known method in the art of providing indication of an ESD event.

Allowable Subject Matter

48. Claims 4, 17, 18, and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

49. Claim 4 recites a pad circuit that includes among other components a clamp device coupled between a second and third voltage rail wherein the enable circuitry is operable to turn on the clamp device. The featured limitations discussed above in combination with the other limitations of the claims is not anticipated by the prior art of record, nor would it have been obvious to one having ordinary skill in the art to modify the prior art of record in order to make the aforementioned limitations unpatentable.

50. Claims 17 and 18 recite a circuit configured to provide protection against ESD that includes among other components a clamp device configured to absorb, when turned on, a portion of an energy generated by the ESD event, wherein the control circuit is operable to turn on the clamp device in response to the ESD event. The featured limitations discussed above in combination with the other limitations of the claims is not anticipated by the prior art of record, nor would it have been obvious to one having ordinary skill in the art to modify the prior art of record in order to make the aforementioned limitations unpatentable.

51. Claim 24 recites a system that includes among other components a clamp device configured to absorb, when turned on, a portion of an energy generated by the ESD event, wherein the control circuitry is operable to turn on the clamp device in response to the ESD event. The featured limitations discussed above in combination with the other limitations of the claims is not anticipated by the prior art of record, nor would it have been obvious to one having ordinary skill in the art to modify the prior art of record in order to make the aforementioned limitations unpatentable.

Conclusion

52. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHRISTOPHER J. CLARK whose telephone number is (571)270-1427. The examiner can normally be reached on M-F, 10:00-6:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-727-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

CJC
11/6/2008

/Stephen W Jackson/
Primary Examiner, Art Unit 2836

<i>Index of Claims</i> 	Application/Control No. 11621724	Applicant(s)/Patent Under Reexamination HOLLY ET AL.
	Examiner CHRISTOPHER J CLARK	Art Unit 2836

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant				☐ CPA				☐ T.D.				☐ R.1.47			
CLAIM		DATE													
Final	Original	03/26/2008	11/06/2008												
	1	✓	✓												
	2	✓	✓												
	3	✓	✓												
	4	O	O												
	5	✓	✓												
	6	✓	✓												
	7	✓	✓												
	8	✓	✓												
	9	✓	✓												
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	16	✓	✓												
	17	O	O												
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	19	✓	✓												
	20	✓	✓												
	21	✓	✓												
	22	✓	✓												
	23	✓	✓												
	24	O	O												
	25	✓	✓												
	26	✓	✓												
	27	✓	✓												

**RESPONSE UNDER 37 C.F.R. § 1.116
EXPEDITED PROCEDURE
GROUP ART UNIT 2836**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application. No:	11/621,724	§	Examiner:	Clark,
Filed:	January 10, 2007	§		Christopher Jay
Inventor(s):		§	Group/Art Unit:	2836
	Patrick J. Holly, David	§	Atty. Dkt. No:	5707-12800
	Rodriguez, David R. Rice	§		
		§		
Title:	PAD ESD TECHNIQUE	§		
		§		
		§		
		§		
		§		
		§		

**RESPONSE TO FINAL OFFICE ACTION OF
NOVEMBER 13, 2008**

Dear Sir or Madam:

This paper is submitted in response to the Office Action of November 13, 2008, to further highlight why the application is in condition for allowance.

Please amend the case as listed below.

IN THE CLAIMS:

The following listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) A pad circuit configured to provide protection against electrostatic discharge (ESD) in a system comprising the pad circuit, the pad circuit comprising:

a first node coupled to a first voltage rail;

a second node coupled to a physical pad having capacitance;

one or more output transistor devices coupled between the first node and the second node, and operable to at least partially drive an output signal at the second node; ~~and~~

a control block configured, operable to turn on, when instructed, at least one of the one or more output transistor devices ~~in response to an ESD event to charge the pad capacitance, thereby reducing to reduce~~ a maximum voltage developed in the system as a result of the ESD event;

a clamp device configured between a second voltage rail and a third voltage rail to reduce, when turned on, the maximum voltage developed in the system as the result of the ESD event;

enable circuitry configured to turn on the clamp device and instruct the control block to turn on the at least one of the one or more output transistor devices, in response to the ESD event;

wherein the second voltage rail is configured to provide power to the enable circuitry, and wherein the third voltage rail has a value below the first voltage rail.

2. (Original) The pad circuit of claim 1, wherein in turning on the at least one of the one or more output transistor devices in response to the ESD event, the control block is further operable to couple the first voltage rail and its associated capacitance to the physical pad to share a charge developed in the system in response to the ESD event,

thereby reducing the maximum voltage developed in the system as the result of the ESD event.

3. (Cancelled)

4. (Cancelled)

5. (Original) The pad circuit of claim 1, wherein the one or more output transistor devices are PMOS devices, wherein the at least one of the one or more transistor devices comprises:

a subset of the PMOS devices; or
the PMOS devices.

6. (Original) The pad circuit of claim 5, further comprising one or more NMOS devices coupled between the second node and a second voltage rail that has a value below the first voltage rail, wherein the NMOS devices and the PMOS devices are operable to operate together to drive the output signal at the second node, wherein the logic circuit is operable to have the NMOS devices turned off during the ESD event.

7. (Original) The pad circuit of claim 1, wherein the pad circuit and the physical pad are comprised in a digital input/output pad.

8. (Currently Amended) A method for protecting a system against electrostatic discharge (ESD), the method comprising:

asserting a control signal in response to an ESD event;

turning on at least one of one or more output transistor devices in response to ~~an ESD event~~ said asserting the control signal to charge a pad capacitance, to thereby reduce a maximum voltage developed in the system as a result of the ESD event; and

turning on a clamp device in response to said asserting the control signal, wherein the clamp device is configured to absorb, when turned on, a portion of an energy

generated by the ESD event, to reduce the maximum voltage developed in the system as the result of the ESD event;

wherein the one or more output transistor devices are configured in the system, and are coupled to a physical pad having the pad capacitance, and wherein the one or more output transistor devices are operable to drive an output signal at the physical pad.

9. (Cancelled)

10. (Original) The method of claim 8;

wherein the one or more transistor devices comprise one or more PMOS devices;

wherein said turning on the at least one of the one or more output transistor devices comprises:

turning on at least one of the one or more PMOS devices; or

turning on the one or more PMOS devices.

11. (Original) The method of claim 10;

wherein the one or more transistor devices further comprise one or more NMOS devices;

wherein the method further comprises disabling the one or more NMOS devices during the ESD event.

12. (Original) The method of claim 11, wherein the physical pad is an input/output pad.

13. (Currently Amended) A circuit configured to provide protection against electrostatic discharge (ESD) in a system comprising the circuit, the circuit comprising:

an output buffer configured to couple to a physical pad having capacitance, and operable to drive at least one output signal at the physical pad;

a control block configured to control the output buffer; ~~and~~

a clamp device coupled between a first supply rail configured to provide power to the control circuit, and a low supply rail, wherein the clamp device is configured to

absorb, when turned on, a portion of an energy generated by the ESD event, to reduce the maximum voltage developed in the system as the result of the ESD event; and

a control circuit configured to instruct the control block to activate at least a portion of the output buffer when an ESD event occurs, ~~thereby charging~~ to charge the pad capacitance to reduce a maximum voltage developed in the system as a result of the ESD event, wherein the control circuit is further configured to turn on the clamp device in response to the ESD event.

14. (Original) The circuit of claim 13, wherein the output buffer comprises:

one or more PMOS devices coupled between a first supply rail and the physical pad; and

one or more NMOS devices coupled between the physical pad and a second supply rail having a value less than the first supply rail;

wherein in activating at least a portion of the output buffer when the ESD event occurs, the control block is operable to:

enable at least one of the one or more PMOS devices; or

enable the one or more PMOS devices.

15. (Original) The circuit of claim 14, wherein in activating at least a portion of the output buffer when the ESD event occurs, the control block is operable to:

disable at least one of the one or more NMOS devices; or

disable the one or more NMOS devices.

16. (Original) The circuit of claim 14, wherein the one or more PMOS devices are coupled in parallel between the first supply rail and the physical pad, and the NMOS devices are coupled in series between the physical pad and the second supply rail.

17. (Cancelled)

18. (Currently Amended) The circuit of claim ~~17~~ 13, wherein the clamp device is one of:

a PMOS device having its source terminal coupled to the first supply rail, its drain terminal coupled to the low supply rail, and its gate terminal coupled to the control circuit; or

an NMOS device having its drain terminal coupled to the first supply rail, its source terminal coupled to the low supply rail, and its gate terminal coupled to the control circuit.

19. (Original) The circuit of claim 13, wherein the control circuit is configured to be powered by a first supply rail operable to provide increased power during the ESD event.

20. (Original) The control circuit of claim 13, wherein in instructing the control block to activate at least a portion of the output buffer when an ESD event occurs, the control circuit is operable to provide a control signal to the control block in response to the ESD event.

21. (Original) The circuit of claim 13, wherein the control circuit is configured to receive a control signal corresponding to a time constant, wherein the time constant corresponds to a specified slope, wherein the control signal is configured to trigger the control circuit if a slope of a voltage pulse developed in the system as a result of the ESD event is greater than or equal to the specified slope.

22. (Currently Amended) A system comprising:

one or more pads, each pad comprising:

a respective physical pad having respective capacitance;

a respective clamp device configured to absorb, when turned on, a portion of an energy generated by the ESD event, to thereby further reduce the maximum voltage developed in the system as the result of the ESD event; and

a respective pad circuit comprising:

a respective output buffer coupled to the respective physical pad,
and operable to drive at least one respective output signal at the respective physical pad;
and

respective control circuitry operable to:

activate at least a portion of the respective output buffer in
response to an ESD event to charge the respective pad capacitance to reduce a maximum
voltage developed in the system as a result of the ESD event; and

turn on the clamp device in response to the ESD event.

23. (Original) The system of claim 22, further comprising functional circuitry
coupled to the respective pad circuit of at least one of the one or more pads, wherein the
functional circuitry is operable to generate the at least one respective output signal driven
by the respective pad circuit of the at least one of the one or more pads.

24. (Cancelled)

25. (Original) The system of claim 22, further comprising a first supply rail
configured to provide increased power in accordance with the ESD event, and further
configured to power the respective control circuitry of the respective pad circuit of each
pad.

26. (Original) The system of claim 25, further comprising a second supply rail
configured to power the respective output buffer of the respective pad circuit of each pad.

27. (Original) The system of claim 25, wherein the respective control circuitry of
the respective pad circuit of each pad is configured to receive a respective control signal
corresponding to a time constant, wherein the time constant corresponds to a specified
slope, wherein the respective control signal is configured to trigger the respective control
circuitry if a slope of a voltage pulse developed in the system as a result of the ESD event
is greater than or equal to the specified slope.

REMARKS

Applicant is in receipt of the Office Action mailed November 13, 2008. Claims 3-4, 9, 17, and 24 have been cancelled. Claims 1, 8, 13, 18, and 22 have been amended. Claims 1-2, 5-8, 10-16, 18-23, and 25-27 are currently pending in the application.

35 U.S.C. § 103 Rejection:

Claims 1-3, 5-8, 10-15, 19, 20, 22, 23, 25, and 26 were rejected under 35 U.S.C. 103(a) as being unpatentable over Allen et al (U. S. Patent 5,168,178) in view of Loh et al (U. S. Patent Publication 2007/0019345). Claim 16 was rejected under 35 U.S.C. 103(a) as being unpatentable over Allen in view Loh as applied to claims 14 above, and further in view of Seo et al (U. S. Patent Publication 2006/0001448). Claims 9, 21 and 27 were rejected under 35 U.S.C. 103(a) as being unpatentable over Allen in view Loh as applied to claims 13 and 25 above, and further in view of Lien et al (U. S. Patent 7,102,862).

Applicant respectfully disagrees with the rejection of these claims. However, in order to expedite prosecution, Applicant has elected to accept the allowable subject matter as set forth below. Applicant reserves the right to file a continuation application directed to the rejected claims.

With regards to claims 8-12, Applicant has amended claim 8 to include all the limitations of claim 9, and the additional feature of asserting a control signal in response to the ESD event. Applicant therefore submits that amended claim 8 and all claims that depend thereon are also allowable for at least the reasons provided in the Office Action with regards to the allowable subject matter indicated in claims 4, 17, 18, and 24.

Applicant therefore respectfully requests removal of the 35 U.S.C. 103(a) rejection of claims 8-12.

Allowable Subject Matter:

Claims 4, 17, 18, and 24 were objected to as being dependent upon a rejected base claim, but were deemed to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicant has amended claim 1 to also include all of the limitations of claim 3 and claim 4, has amended claim 13 to also include the limitations of claim 17, and has amended claim 22 to also include the limitations of claim 24.

Applicant therefore submits that all currently amended claims and all non-canceled original claims dependent thereon are allowable for at least the reasons provided in the Office Action, and respectfully requests removal of the objection of claims 4, 17, 18, and 24.

CONCLUSION

In light of the foregoing amendments and remarks, Applicant submits the application is now in condition for allowance, and an early notice to that effect is requested.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above-referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. The Commissioner is hereby authorized to charge any fees which may be required or credit any overpayment to Meyertons, Hood, Kivlin, Kowert & Goetzel P.C., Deposit Account No. 50-1505/5707-12800/JCH.

Also filed herewith are the following items:

- ☐ Request for Continued Examination
- ☐ Terminal Disclaimer
- ☐ Power of Attorney By Assignee and Revocation of Previous Powers
- ☐ Notice of Change of Address
- ☐ Other:

Respectfully submitted,

/Jeffrey C. Hood/

Jeffrey C. Hood, Reg. #35198
ATTORNEY FOR APPLICANT(S)

Meyertons, Hood, Kivlin, Kowert & Goetzel PC
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Date: 2009-02-13 JCH/TAK

Electronic Acknowledgement Receipt

EFS ID:	4791386
Application Number:	11621724
International Application Number:	
Confirmation Number:	1652
Title of Invention:	Pad ESD Spreading Technique
First Named Inventor/Applicant Name:	Patrick J. Holly
Customer Number:	35690
Filer:	Jeffrey C Hood/Jeannie Miranda
Filer Authorized By:	Jeffrey C Hood
Attorney Docket Number:	5707-12800
Receipt Date:	13-FEB-2009
Filing Date:	10-JAN-2007
Time Stamp:	14:41:33
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		5707-12800_Final_OA_2008-11-13.pdf	88851 2c071b729e294d901d17eb212d15ac165bf e247f	yes	10

MCHP_00000128

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Amendment After Final	1	1
	Claims	2	7
	Applicant Arguments/Remarks Made in an Amendment	8	10
Warnings:			
Information:			
Total Files Size (in bytes):		88851	
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.			

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 11/621,724		Filing Date 01/10/2007		☐ To be Mailed		
APPLICATION AS FILED – PART I											
(Column 1)			(Column 2)			SMALL ENTITY ☐		OR		OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	RATE (\$)	FEE (\$)	RATE (\$)	FEE (\$)	RATE (\$)	FEE (\$)	
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A		N/A		N/A		N/A		
☐ SEARCH FEE (37 CFR 1.16(k), (j), or (m))	N/A	N/A	N/A		N/A		N/A		N/A		
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A		N/A		N/A		N/A		
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$	=	OR	X \$	=	X \$	=	X \$	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$	=	OR	X \$	=	X \$	=	X \$	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).										
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))											
* If the difference in column 1 is less than zero, enter "0" in column 2.											
APPLICATION AS AMENDED – PART II										TOTAL	TOTAL
(Column 1)			(Column 2)			SMALL ENTITY		OR		OTHER THAN SMALL ENTITY	
AMENDMENT	02/13/2009	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	* 22	Minus	** 27	= 0	X \$	=	OR	X \$52=	0	
	Independent (37 CFR 1.16(h))	* 4	Minus	***4	= 0	X \$	=	OR	X \$220=	0	
	☐ Application Size Fee (37 CFR 1.16(s))										
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
	TOTAL ADD'L FEE										TOTAL ADD'L FEE
(Column 1)			(Column 2)			SMALL ENTITY		OR		OTHER THAN SMALL ENTITY	
AMENDMENT	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)	ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$	=	OR	X \$	=	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$	=	OR	X \$	=	
	☐ Application Size Fee (37 CFR 1.16(s))										
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
	TOTAL ADD'L FEE										TOTAL ADD'L FEE
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.											

Legal Instrument Examiner:
/APRIL WALKER/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/621,724	01/10/2007	Patrick J. Holly	5707-12800	1652

35690 7590 03/19/2009
MEYERTONS, HOOD, KIVLIN, KOWERT & GOETZEL, P.C.
P.O. BOX 398
AUSTIN, TX 78767-0398

EXAMINER

CLARK, CHRISTOPHER JAY

ART UNIT	PAPER NUMBER
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2836

MAIL DATE	DELIVERY MODE
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03/19/2009

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Advisory Action Before the Filing of an Appeal Brief	Application No. 11/621,724	Applicant(s) HOLLY ET AL.	
	Examiner CHRISTOPHER J. CLARK	Art Unit 2836	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 13 February 2009 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:

a) ☐ The period for reply expires _____ months from the mailing date of the final rejection.

b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☒ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because

(a) ☒ They raise new issues that would require further consideration and/or search (see NOTE below);

(b) ☐ They raise the issue of new matter (see NOTE below);

(c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or

(d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

NOTE: See Continuation Sheet. (See 37 CFR 1.116 and 41.33(a)).

4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).

5. ☒ Applicant's reply has overcome the following rejection(s): See Continuation Sheet.

6. ☒ Newly proposed or amended claim(s) 1, 2, 5-7, 13-16, 18-23 and 25-27 would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).

7. ☒ For purposes of appeal, the proposed amendment(s): a) ☒ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

The status of the claim(s) is (or will be) as follows:
 Claim(s) allowed: _____
 Claim(s) objected to: 4, 17, 18 and 24.
 Claim(s) rejected: 1-3, 5-16, 19-23 and 25-27.
 Claim(s) withdrawn from consideration: _____

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).

9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing of a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).

10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☐ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: _____

12. ☐ Note the attached Information *Disclosure Statement*(s). (PTO/SB/08) Paper No(s). _____

13. ☐ Other: _____

3/16/2009

/Ronald W Leja/
Primary Examiner, Art Unit 2836

Continuation of 3. NOTE: Claim 8 has been amended to include the limitation "asserting a control signal in response to an ESD event" which was not previously found in Claim 8 or any dependent claims thereof and would therefore require further consideration.

Continuation of 5. Applicant's reply has overcome the following rejection(s): 35 U.S.C. 103 Rejection of Claims 1-3, 5-7, 13-15, 19-23, and 25-27 .

**RESPONSE UNDER 37 C.F.R. § 1.116
EXPEDITED PROCEDURE
GROUP ART UNIT 2836**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application. No:	11/621,724	§	Examiner:	Clark,
Filed:	January 10, 2007	§		Christopher Jay
Inventor(s):		§	Group/Art Unit:	2836
	Patrick J. Holly, David	§	Atty. Dkt. No:	5707-12800
	Rodriguez, David R. Rice	§		
		§		
Title:	PAD ESD TECHNIQUE	§		
		§		
		§		
		§		
		§		

**RESPONSE TO FINAL OFFICE ACTION OF
NOVEMBER 13, 2008**

Dear Sir or Madam:

Applicant's proposed amendments filed on February 13, 2009 in response to the Office Action of November 13, 2008 have not been entered by the Examiner. This paper is therefore submitted in response to the Office Action of November 13, 2008, and further in response to the Advisory Action of mailed on March 13, 2009, to further highlight why the application is in condition for allowance.

Please amend the case as listed below.

IN THE CLAIMS:

The following listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) A pad circuit configured to provide protection against electrostatic discharge (ESD) in a system comprising the pad circuit, the pad circuit comprising:

a first node coupled to a first voltage rail;

a second node coupled to a physical pad having capacitance;

one or more output transistor devices coupled between the first node and the second node, and operable to at least partially drive an output signal at the second node;
~~and~~

a control block configured, operable to turn on, when instructed, at least one of the one or more output transistor devices ~~in response to an ESD event~~ to charge the pad capacitance, ~~thereby reducing to reduce~~ a maximum voltage developed in the system as a result of the ESD event;

a clamp device configured between a second voltage rail and a third voltage rail to reduce, when turned on, the maximum voltage developed in the system as the result of the ESD event;

enable circuitry configured to turn on the clamp device and instruct the control block to turn on the at least one of the one or more output transistor devices, in response to the ESD event;

wherein the second voltage rail is configured to provide power to the enable circuitry, and wherein the third voltage rail has a value below the first voltage rail.

2. (Original) The pad circuit of claim 1, wherein in turning on the at least one of the one or more output transistor devices in response to the ESD event, the control block is further operable to couple the first voltage rail and its associated capacitance to the physical pad to share a charge developed in the system in response to the ESD event,

thereby reducing the maximum voltage developed in the system as the result of the ESD event.

3. (Cancelled)

4. (Cancelled)

5. (Original) The pad circuit of claim 1, wherein the one or more output transistor devices are PMOS devices, wherein the at least one of the one or more transistor devices comprises:

a subset of the PMOS devices; or
the PMOS devices.

6. (Original) The pad circuit of claim 5, further comprising one or more NMOS devices coupled between the second node and a second voltage rail that has a value below the first voltage rail, wherein the NMOS devices and the PMOS devices are operable to operate together to drive the output signal at the second node, wherein the logic circuit is operable to have the NMOS devices turned off during the ESD event.

7. (Original) The pad circuit of claim 1, wherein the pad circuit and the physical pad are comprised in a digital input/output pad.

8. – 12. (Cancelled)

13. (Currently Amended) A circuit configured to provide protection against electrostatic discharge (ESD) in a system comprising the circuit, the circuit comprising:

an output buffer configured to couple to a physical pad having capacitance, and operable to drive at least one output signal at the physical pad;

a control block configured to control the output buffer; ~~and~~

a clamp device coupled between a first supply rail configured to provide power to the control circuit, and a low supply rail, wherein the clamp device is configured to

absorb, when turned on, a portion of an energy generated by the ESD event, to reduce the maximum voltage developed in the system as the result of the ESD event; and

a control circuit configured to instruct the control block to activate at least a portion of the output buffer when an ESD event occurs, ~~thereby charging~~ to charge the pad capacitance to reduce a maximum voltage developed in the system as a result of the ESD event, wherein the control circuit is further configured to turn on the clamp device in response to the ESD event.

14. (Original) The circuit of claim 13, wherein the output buffer comprises:

one or more PMOS devices coupled between a first supply rail and the physical pad; and

one or more NMOS devices coupled between the physical pad and a second supply rail having a value less than the first supply rail;

wherein in activating at least a portion of the output buffer when the ESD event occurs, the control block is operable to:

enable at least one of the one or more PMOS devices; or

enable the one or more PMOS devices.

15. (Original) The circuit of claim 14, wherein in activating at least a portion of the output buffer when the ESD event occurs, the control block is operable to:

disable at least one of the one or more NMOS devices; or

disable the one or more NMOS devices.

16. (Original) The circuit of claim 14, wherein the one or more PMOS devices are coupled in parallel between the first supply rail and the physical pad, and the NMOS devices are coupled in series between the physical pad and the second supply rail.

17. (Cancelled)

18. (Currently Amended) The circuit of claim ~~17~~ 13, wherein the clamp device is one of:

a PMOS device having its source terminal coupled to the first supply rail, its drain terminal coupled to the low supply rail, and its gate terminal coupled to the control circuit; or

an NMOS device having its drain terminal coupled to the first supply rail, its source terminal coupled to the low supply rail, and its gate terminal coupled the control circuit.

19. (Original) The circuit of claim 13, wherein the control circuit is configured to be powered by a first supply rail operable to provide increased power during the ESD event.

20. (Original) The control circuit of claim 13, wherein in instructing the control block to activate at least a portion of the output buffer when an ESD event occurs, the control circuit is operable to provide a control signal to the control block in response to the ESD event.

21. (Original) The circuit of claim 13, wherein the control circuit is configured to receive a control signal corresponding to a time constant, wherein the time constant corresponds to a specified slope, wherein the control signal is configured to trigger the control circuit if a slope of a voltage pulse developed in the system as a result of the ESD event is greater than or equal to the specified slope.

22. (Currently Amended) A system comprising:

one or more pads, each pad comprising:

a respective physical pad having respective capacitance;

a respective clamp device configured to absorb, when turned on, a portion of an energy generated by the ESD event, to thereby further reduce the maximum voltage developed in the system as the result of the ESD event; and

a respective pad circuit comprising:

a respective output buffer coupled to the respective physical pad,
and operable to drive at least one respective output signal at the respective physical pad;
and

respective control circuitry operable to:

activate at least a portion of the respective output buffer in
response to an ESD event to charge the respective pad capacitance to reduce a maximum
voltage developed in the system as a result of the ESD event; and

turn on the clamp device in response to the ESD event.

23. (Original) The system of claim 22, further comprising functional circuitry
coupled to the respective pad circuit of at least one of the one or more pads, wherein the
functional circuitry is operable to generate the at least one respective output signal driven
by the respective pad circuit of the at least one of the one or more pads.

24. (Cancelled)

25. (Original) The system of claim 22, further comprising a first supply rail
configured to provide increased power in accordance with the ESD event, and further
configured to power the respective control circuitry of the respective pad circuit of each
pad.

26. (Original) The system of claim 25, further comprising a second supply rail
configured to power the respective output buffer of the respective pad circuit of each pad.

27. (Original) The system of claim 25, wherein the respective control circuitry of
the respective pad circuit of each pad is configured to receive a respective control signal
corresponding to a time constant, wherein the time constant corresponds to a specified
slope, wherein the respective control signal is configured to trigger the respective control
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REMARKS

Applicant is in receipt of the Office Action mailed November 13, 2008. Claims 3-4, 8-12, 17, and 24 have been cancelled. Claims 1, 13, 18, and 22 have been amended. Claims 1-2, 5-7, 13-16, 18-23, and 25-27 are currently pending in the application.

35 U.S.C. § 103 Rejection:

Claims 1-3, 5-8, 10-15, 19, 20, 22, 23, 25, and 26 were rejected under 35 U.S.C. 103(a) as being unpatentable over Allen et al (U. S. Patent 5,168,178) in view of Loh et al (U. S. Patent Publication 2007/0019345). Claim 16 was rejected under 35 U.S.C. 103(a) as being unpatentable over Allen in view Loh as applied to claims 14 above, and further in view of Seo et al (U. S. Patent Publication 2006/0001448). Claims 9, 21 and 27 were rejected under 35 U.S.C. 103(a) as being unpatentable over Allen in view Loh as applied to claims 13 and 25 above, and further in view of Lien et al (U. S. Patent 7,102,862).

Applicant respectfully disagrees with the rejection of these claims. However, in order to expedite prosecution, Applicant has elected to accept the allowable subject matter as set forth below. Applicant reserves the right to file a continuation application directed to the rejected claims.

Allowable Subject Matter:

Claims 4, 17, 18, and 24 were objected to as being dependent upon a rejected base claim, but were deemed to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicant has amended claim 1 to also include all of the limitations of claim 3 and claim 4, has amended claim 13 to also include the limitations of claim 17, and has amended claim 22 to also include the limitations of claim 24.

Applicant therefore submits that all currently amended claims and all non-canceled original claims dependent thereon are allowable for at least the reasons provided in the Office Action, and respectfully requests removal of the objection of claims 4, 17, 18, and 24.

CONCLUSION

In light of the foregoing amendments and remarks, Applicant submits the application is now in condition for allowance, and an early notice to that effect is requested.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above-referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. The Commissioner is hereby authorized to charge any fees which may be required or credit any overpayment to Meyertons, Hood, Kivlin, Kowert & Goetzel P.C., Deposit Account No. 50-1505/5707-12800/JCH.

Also filed herewith are the following items:

- ☐ Request for Continued Examination
- ☐ Terminal Disclaimer
- ☐ Power of Attorney By Assignee and Revocation of Previous Powers
- ☐ Notice of Change of Address
- ☐ Other:

Respectfully submitted,

/Jeffrey C. Hood/

Jeffrey C. Hood, Reg. #35198
ATTORNEY FOR APPLICANT(S)

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Date: 2009-04-03 JCH/TAK

Electronic Acknowledgement Receipt

EFS ID:	5095442
Application Number:	11621724
International Application Number:	
Confirmation Number:	1652
Title of Invention:	Pad ESD Spreading Technique
First Named Inventor/Applicant Name:	Patrick J. Holly
Customer Number:	35690
Filer:	Jeffrey C Hood/Jeannie Miranda
Filer Authorized By:	Jeffrey C Hood
Attorney Docket Number:	5707-12800
Receipt Date:	03-APR-2009
Filing Date:	10-JAN-2007
Time Stamp:	17:19:11
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		5707-12800_Final_OA_2008-11-13_resp-to-advisory.pdf	83026 b938e61852097a89350612032b9472398ce72676	yes	9

MCHP_00000143

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Amendment After Final	1	1
	Claims	2	6
	Applicant Arguments/Remarks Made in an Amendment	7	9
Warnings:			
Information:			
Total Files Size (in bytes):		83026	
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 11/621,724		Filing Date 01/10/2007		☐ To be Mailed			
APPLICATION AS FILED – PART I												
(Column 1)			(Column 2)		SMALL ENTITY ☐		OR		OTHER THAN SMALL ENTITY			
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)			RATE (\$)	FEE (\$)				
☒ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A				N/A	300				
☒ SEARCH FEE (37 CFR 1.16(k), (j), or (m))	N/A	N/A	N/A				N/A	500				
☒ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A				N/A	200				
TOTAL CLAIMS (37 CFR 1.16(j))	27 minus 20 =	* 7	X \$ =		OR		X \$50 =	350				
INDEPENDENT CLAIMS (37 CFR 1.16(h))	4 minus 3 =	* 1	X \$ =		OR		X \$200 =	200				
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))			If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).									
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))												
* If the difference in column 1 is less than zero, enter "0" in column 2.												
			TOTAL					TOTAL		1550		
APPLICATION AS AMENDED – PART II												
(Column 1)			(Column 2)		(Column 3)		SMALL ENTITY		OR		OTHER THAN SMALL ENTITY	
AMENDMENT	04/03/2009	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)		RATE (\$)	ADDITIONAL FEE (\$)		
	Total (37 CFR 1.16(o))	* 18	Minus	** 27	= 0	X \$ =		OR	X \$52=	0		
	Independent (37 CFR 1.16(h))	* 3	Minus	***4	= 0	X \$ =		OR	X \$220=	0		
	☐ Application Size Fee (37 CFR 1.16(s))											
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))											
						TOTAL ADD'L FEE			OR	TOTAL ADD'L FEE		0
(Column 1)			(Column 2)		(Column 3)							
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)		RATE (\$)	ADDITIONAL FEE (\$)		
	Total (37 CFR 1.16(o))	*	Minus	**	=	X \$ =		OR	X \$ =			
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =		OR	X \$ =			
	☐ Application Size Fee (37 CFR 1.16(s))											
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))											
						TOTAL ADD'L FEE			OR	TOTAL ADD'L FEE		
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.												

Legal Instrument Examiner:
/AJAY R. DAVID/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Document code: WFEE

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UNITED STATES PATENT AND TRADEMARK OFFICE

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NOTICE OF ALLOWANCE AND FEE(S) DUE

35690 7590 05/06/2009

MEYERTONS, HOOD, KIVLIN, KOWERT & GOETZEL, P.C.
P.O. BOX 398
AUSTIN, TX 78767-0398

EXAMINER

CLARK, CHRISTOPHER JAY

ART UNIT

PAPER NUMBER

2836

DATE MAILED: 05/06/2009

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/621,724	01/10/2007	Patrick J. Holly	5707-12800	1652

TITLE OF INVENTION: PAD ESD SPREADING TECHNIQUE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	08/06/2009

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

35690 7590 05/06/2009

MEYERTONS, HOOD, KIVLIN, KOWERT & GOETZEL, P.C.
P.O. BOX 398
AUSTIN, TX 78767-0398

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/621,724	01/10/2007	Patrick J. Holly	5707-12800	1652

TITLE OF INVENTION: PAD ESD SPREADING TECHNIQUE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	08/06/2009

EXAMINER	ART UNIT	CLASS-SUBCLASS
CLARK, CHRISTOPHER JAY	2836	361-056000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____
Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/621,724	01/10/2007	Patrick J. Holly	5707-12800	1652
35690	7590	05/06/2009		
MEYERTONS, HOOD, KIVLIN, KOWERT & GOETZEL, P.C. P.O. BOX 398 AUSTIN, TX 78767-0398			EXAMINER CLARK, CHRISTOPHER JAY	
			ART UNIT	PAPER NUMBER
			2836	
DATE MAILED: 05/06/2009				

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)

(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Notice of Allowability	Application No.	Applicant(s)	
	11/621,724	HOLLY ET AL.	
	Examiner	Art Unit	
	CHRISTOPHER J. CLARK	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 3 April 2009.

2. ☒ The allowed claim(s) is/are 1,2,5-7,13-16,18-23 and 25-27.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some* c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
(a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
(b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892) 2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____ 4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material	5. ☐ Notice of Informal Patent Application 6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ 7. ☒ Examiner's Amendment/Comment 8. ☒ Examiner's Statement of Reasons for Allowance 9. ☐ Other _____.
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/Ronald W Leja/ Primary Examiner, Art Unit 2836	4/26/2009
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EXAMINER'S AMENDMENT

This action is in response to Applicant's filing on April 3, 2009.

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Jeff Hood on April 15, 2009 and April 21, 2009.

The application has been amended as follows:

CLAIM 2: In Line 2, replace "in response to the ESD event" with --when instructed--.

In Line 3, replace "is further operable to couple" with --couples an associated capacitance of--.

In Line 3, delete "and its associated capacitance".

In Line 5, replace "thereby reducing" with --to reduce--.

CLAIM 5: In Line 2, replace " , wherein the at least one of the one or more transistor devices" with --,--.

Delete Lines 3-5.

CLAIM 6: In Line 2, replace "a second" with --the third--.

In Lines 2 and 3, delete "that has a value below the first voltage rail".

In Line 5, replace “logic circuit is operable” with --control block operates--.

In Line 5, replace “have” with --turn off--.

In Line 5, delete "turned off".

CLAIM 13: In Lines 3 and 4, delete "and operable".

In Lines 6-7, delete “configured to provide power to the control circuit,”.

In Line 14, replace “.” with --;--.

On a new Line 15, insert --wherein the first supply rail is configured to provide power to the control circuit.--.

CLAIM 14: In Line 2, replace “first” with --second--.

In Line 4, replace “a second” with --the low--.

In Line 5, replace “having” with --, wherein the low supply rail has--.

In Line 5, “first” with --second--.

In Line 7, replace “is operable to:” with --enables one or more of the one or more PMOS devices.--.

Delete Lines 8 and 9.

CLAIM 15: In Line 2, delete “is operable to:”.

In Line 3, replace “disable at least” with --disables--.

In Line 3, insert prior to “of the one” --or more--.

In Lines 3 and 4, delete “; or disable the one or more NMOS devices”

CLAIM 16: In Line 2, replace "are" with --comprise a plurality of PMOS devices--.

In Line 2, replace "first" with --second--.

In Line 2, prior to "NMOS" insert --one or more--.

In Line 3, replace "are" with --comprise a plurality of NMOS devices--.

CLAIM 19: In Lines 1 and 2, delete "control circuit is configured to be powered by a".

In Line 2, replace "operable" with --is configured--.

CLAIM 22: In Line 5, replace "the ESD event" with --an ESD event--.

Allowable Subject Matter

2. Claims 1, 2, 5-7, 13-16, 18-23, and 25-27 are allowed.
3. Claims 1, 2, and 5-7 recite a pad circuit that includes among other components a clamp device coupled between a second and third voltage rail wherein the enable circuitry is operable to turn on the clamp device and instruct the control block to turn on at least one of the one or more output transistor devices, in response to the ESD event. The featured limitations discussed above in combination with the other limitations of the claims is not anticipated by the prior art of record, nor would it have been obvious to one having ordinary skill in the art to modify the prior art of record in order to make the aforementioned limitations unpatentable.

4. Claims 13-16 and 18-21, recite a circuit configured to provide protection against ESD that includes among other components a clamp device configured to absorb, when turned on, a portion of an energy generated by the ESD event, and a control circuit configured to instruct the control block to activate at least a portion of the output buffer when an ESD event occurs and further configured to turn on the clamp device in response to the ESD event. The featured limitations discussed above in combination with the other limitations of the claims is not anticipated by the prior art of record, nor would it have been obvious to one having ordinary skill in the art to modify the prior art of record in order to make the aforementioned limitations unpatentable.

5. Claims 22, 23, and 25-27 recite a system that includes among other components a clamp device configured to absorb, when turned on, a portion of an energy generated by the ESD event, wherein the control circuitry is operable to activate at least a portion of the respective output buffer and turn on the clamp device in response to the ESD event. The featured limitations discussed above in combination with the other limitations of the claims is not anticipated by the prior art of record, nor would it have been obvious to one having ordinary skill in the art to modify the prior art of record in order to make the aforementioned limitations unpatentable.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHRISTOPHER J. CLARK whose telephone number is (571)270-1427. The examiner can normally be reached on M-F, 10:00-6:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-727-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

April 26, 2009

/Ronald W Leja/
Primary Examiner, Art Unit 2836

CJC
4/21/2009

<i>Index of Claims</i> 	Application/Control No. 11621724	Applicant(s)/Patent Under Reexamination HOLLY ET AL.
	Examiner CHRISTOPHER J CLARK	Art Unit 2836

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant		☐ CPA		☐ T.D.		☐ R.1.47			
CLAIM		DATE							
Final	Original	03/26/2008	11/06/2008	04/11/2009					
1	1	✓	✓	=					
2	2	✓	✓	=					
	3	✓	✓	-					
	4	O	O	-					
3	5	✓	✓	=					
4	6	✓	✓	=					
5	7	✓	✓	=					
	8	✓	✓	-					
	9	✓	✓	-					
	10	✓	✓	-					
	11	✓	✓	-					
	12	✓	✓	-					
6	13	✓	✓	=					
7	14	✓	✓	=					
8	15	✓	✓	=					
9	16	✓	✓	=					
	17	O	O	-					
10	18	O	O	=					
11	19	✓	✓	=					
12	20	✓	✓	=					
13	21	✓	✓	=					
14	22	✓	✓	=					
15	23	✓	✓	=					
	24	O	O	-					
16	25	✓	✓	=					
17	26	✓	✓	=					
18	27	✓	✓	=					

Search Notes 	Application/Control No. 11621724	Applicant(s)/Patent Under Reexamination HOLLY ET AL.
	Examiner CHRISTOPHER J CLARK	Art Unit 2836

SEARCHED			
Class	Subclass	Date	Examiner
361	56	3/26/2008	CJC

SEARCH NOTES		
Search Notes	Date	Examiner

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
	See L1 of attached Search History	4/11/2009	CJC

/CHRISTOPHER J CLARK/ Examiner.Art Unit 2836	
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Issue Classification 	Application/Control No. 11621724	Applicant(s)/Patent Under Reexamination HOLLY ET AL.
	Examiner CHRISTOPHER J CLARK	Art Unit 2836

ORIGINAL						INTERNATIONAL CLASSIFICATION												
CLASS			SUBCLASS			CLAIMED					NON-CLAIMED							
361			56			H	0	2	H	9 / 00 (2006.01.01)								
CROSS REFERENCE(S)																		
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)																	
	NONE																	

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1		17												
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	3	11	19												
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9	16														

/CHRISTOPHER J CLARK/ Examiner.Art Unit 2836 (Assistant Examiner)	4/11/2009 (Date)	Total Claims Allowed: 18	
/Ronald W Leja/ Primary Examiner.Art Unit 2836 (Primary Examiner)	04/26/2009 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 1



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CONFIRMATION NO. 1652

SERIAL NUMBER 11/621,724	FILING or 371(c) DATE 01/10/2007 RULE	CLASS 361	GROUP ART UNIT 2836	ATTORNEY DOCKET NO. 5707-12800		
APPLICANTS Patrick J. Holly, Tempe, AZ; David Rodriguez, Phoenix, AZ; David R. Rice, Phoenix, AZ; ** CONTINUING DATA ***** ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 02/08/2007						
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and /Christopher Jay Clark/ Acknowledged Examiner's Signature		☐ Met after Allowance CJC Initials	STATE OR COUNTRY AZ	SHEETS DRAWINGS 1	TOTAL CLAIMS 27	INDEPENDENT CLAIMS 4
ADDRESS MEYERTONS, HOOD, KIVLIN, KOWERT & GOETZEL, P.C. P.O. BOX 398 AUSTIN, TX 78767-0398 UNITED STATES						
TITLE Pad ESD Spreading Technique						
FILING FEE RECEIVED 1550	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit			

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	(pad capacitance ESD clamp control rail).clm.	US-PGPUB; USPAT; USOCR	AND	ON	2009/04/11 16:32
S1	6710	pad with capacitance	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/20 14:55
S2	936	S1 same transistor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/20 14:55
S3	127	S2 same control\$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/20 14:56
S4	52	S3 same output	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/20 14:57
S5	32	S3 same (esd electrostatic)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/20 14:57
S6	697	S1 same (esd electrostatic)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/20 15:14
S7	544	S1 with (esd electrostatic)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/20 15:15

S8	49	S7 same buffer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/20 15:15
S9	2885	361/56.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/20 15:24
S10	1392	S9 and (pad pin port)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/20 15:25
S11	411	S9 and ((pad pin port) with (capacitor capacitance))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/20 15:26
S12	16	S9 and ((pad pin port) with (capacitor capacitance) with buffer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/20 15:26
S15	0	(esd electrostatic) same (disipat\$4 with (pad pin))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/20 15:36
S16	2935	(esd electrostatic) same (output with (pad pin))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/20 15:37
S17	1540	(esd electrostatic) same (output near (pad pin))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/20 15:37

S18	177	(esd electrostatic) same ((output near (pad pin)) with buffer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/20 15:37
S19	670	(output near (pad pin)) with capacitance	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/20 16:31
S20	52	S19 same (esd electrostatic)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/20 16:31
S21	95	charg\$4 with parasitic with capacit\$4 with (pin pad)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/20 18:05
S22	8	S21 same (esd electrostatic)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/20 18:06
S23	3827	charg\$4 with capacit\$4 with (pin pad)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/20 18:10
S24	274	S23 same (esd electrostatic)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/20 18:24
S25	13421	discharg\$4 near4 (pin pad)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/20 18:33

S26	430	discharg\$4 near4 (output adj (pin pad))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/20 18:33
S27	223	S26 same (esd electrostatic)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/20 18:33
S28	2364	pad with spreading	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/20 19:13
S29	6	S28 with (esd electrostatic)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/20 19:14
S30	41	S27 same buffer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/20 19:42
S31	2885	361/56.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/21 14:48
S32	2885	S31	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/21 14:48
S33	30	S31 and (capacit\$4 near absorb\$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/21 14:49

S34	144	S31 and (capacit\$4 near transistor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/21 14:51
S35	84	S31 and (capacitor near transistor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/21 14:52
S36	191749	transistor with capacitor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/21 15:52
S37	121089	capacitor near4 ((discharg \$4 absorb\$4))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/21 15:53
S38	21	esd with transistor with (capacitor near4 ((discharg \$4 absorb\$4)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/21 15:54
S39	0	("2007/0019345").URPN.	USPAT	OR	ON	2008/03/21 15:57
S40	1	"5907464".pn.	USPAT	OR	ON	2008/03/21 15:59
S41	31	("5400202" "5530612" "5543650" "5654862"). PN. OR ("5907464"). URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2008/03/21 16:00
S42	518	capacitor near3 esd	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/21 16:03
S43	29	(capacitor near3 esd) with (buffer inverter)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/21 16:11

S44	16	(capacitor near3 esd) with shunt\$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/21 16:42
S45	252	(output adj pad) with capacitance	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/21 16:58
S46	56	S45 same (buffer inverter)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/21 16:58
S47	13	S46 same esd	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/21 16:59
S48	25	(output adj pad) near capacitance	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/21 17:02
S49	125	(output adj pad) near buffer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/21 17:28
S50	0	(output adj pad) near ((inherent intrinsic) adj capacitance)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/21 17:58
S51	1	(output adj pad) with ((inherent intrinsic) adj capacitance)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/21 17:58

S52	252	(output adj pad) with (capacitance)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/21 17:59
S53	25	(output adj pad) near (capacitance)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/21 17:59
S54	47	("5208719" "5223737" "5707886" "5717560" "5907464" "5956219" "6008970" "6157065" "6577481" "6690555" "6744610" "6747501" "6760209" "6768176" "6788507" "6800906" "6829126" "6838775" "6844595" "6864536" "6876529" "7019366" "7106563").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/21 19:41
S55	23	("5208719" "5223737" "5707886" "5717560" "5907464" "5956219" "6008970" "6157065" "6577481" "6690555" "6744610" "6747501" "6760209" "6768176" "6788507" "6800906" "6829126" "6838775" "6844595" "6864536" "6876529" "7019366" "7106563").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2008/03/21 19:41
S56	1	"6552583".pn.	US-PGPUB; USPAT; USOCR	OR	ON	2008/03/25 20:58
S57	23	("4678950" "4855620" "5208719" "5287241" "5442217" "5537067" "5631793" "5686751" "5710682" "5729419" "5959488" "5982217" "5986867" "5990723" "6064556" "6118323" "6118640" "6249410"). PN. OR ("6552583"). URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2008/03/25 21:01
S58	1	"5907464".pn.	US-PGPUB; USPAT; USOCR	OR	ON	2008/03/25 21:23

S59	520	trigger\$4 same slope same (time adj constant)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/26 13:53
S60	0	S59 same esd	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/26 13:53
S61	2244	esd same trigger\$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/26 13:54
S62	116	S61 same (time adj constant)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/26 13:54
S63	272	buffer with (nmos near4 series)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/26 14:45
S64	179	buffer with (nmos near4 series) with pmos	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/26 14:46
S65	458	discharg\$4 near4 (output adj (pin pad))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/06 13:57
S66	9	S65 with dissipat\$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/06 13:57

S67	1989	pad near2 capacitance	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/06 14:03
S68	2	S67 with dissipat\$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/06 14:03
S69	39	S67 near4 charg\$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/06 14:03

4/ 11/ 2009 4:57:06 PM

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**RESPONSE UNDER 37 C.F.R. § 1.116
EXPEDITED PROCEDURE
GROUP ART UNIT 2836**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application. No: 11/621,724

Filed: January 10, 2007

Inventor(s):

Patrick J. Holly, David

Rodriguez, David R. Rice

Title: PAD ESD TECHNIQUE

§
§
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§
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§
§
§

Examiner: Clark,
Christopher Jay

Group/Art Unit: 2836

Atty. Dkt. No: 5707-12800

**RESPONSE TO FINAL OFFICE ACTION OF
NOVEMBER 13, 2008**

Dear Sir or Madam:

Applicant's proposed amendments filed on February 13, 2009 in response to the Office Action of November 13, 2008 have not been entered by the Examiner. This paper is therefore submitted in response to the Office Action of November 13, 2008, and further in response to the Advisory Action of mailed on March 13, 2009, to further highlight why the application is in condition for allowance.

Please amend the case as listed below.

DO NOT ENTER: /CC/

**RESPONSE UNDER 37 C.F.R. § 1.116
EXPEDITED PROCEDURE
GROUP ART UNIT 2836**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application. No:	11/621,724	§	Examiner:	Clark,
Filed:	January 10, 2007	§		Christopher Jay
Inventor(s):		§	Group/Art Unit:	2836
	Patrick J. Holly, David	§	Atty. Dkt. No:	5707-12800
	Rodriguez, David R. Rice	§		
		§		
Title:	PAD ESD TECHNIQUE	§		
		§		
		§		
		§		
		§		
		§		

**RESPONSE TO FINAL OFFICE ACTION OF
NOVEMBER 13, 2008**

Dear Sir or Madam:

This paper is submitted in response to the Office Action of November 13, 2008, to further highlight why the application is in condition for allowance.

Please amend the case as listed below.

To: patent_docketing@intprop.com,ptomhkk@gmail.com,
From: PAIR_eOfficeAction@uspto.gov
Cc: PAIR_eOfficeAction@uspto.gov
Subject: Private PAIR Correspondence Notification for Customer Number 35690

May 06, 2009 05:43:22 AM

Dear PAIR Customer:

MEYERTONS, HOOD, KIVLIN, KOWERT & GOETZEL, P.C.
P.O. BOX 398
AUSTIN, TX 78767-0398
UNITED STATES

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The official date of notification of the outgoing correspondence will be indicated on the form PTOL-90 accompanying the correspondence.

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Application	Document	Mailroom Date	Attorney Docket No.
11621724	NOA	05/06/2009	5707-12800
	NOA	05/06/2009	5707-12800

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Thank you for prompt attention to this notice,

UNITED STATES PATENT AND TRADEMARK OFFICE
PATENT APPLICATION INFORMATION RETRIEVAL SYSTEM

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		11621724	11621724 - GAU: 2836
	Filing Date		2007-01-10	
	First Named Inventor	Patrick J. Holly		
	Art Unit	2836		
	Examiner Name	Unknown		
	Attorney Docket Number	5707-12800		

TS
5/28/09

/CC/	9	6760209	B1	7/2004 ~~2004-06-07~~	Bradley A. Sharpe-Geisler	
	10	6768176	B1	2004-07-27	David D. Litfin	
	11	6788507	B2	2004-09-07	Chen, et al.	
	12	6800906	B2	2004-10-05	Jyh-Nan Cheng	
	13	6829126	B2	2004-12-07	Lee, et al.	
	14	6838775	B2	2005-01-04	Makoto Takahashi	
	15	6844595	B2	2005-01-18	Wei-Fan Chen	
	16	6864536	B2	2005-03-08	Lin, et al.	
	17	6876529	B2	2005-04-05	Larry B. Li	
	18	7106563	B2	2006-09-12	Lai, et al.	
↓	19	7019366	B1	2006-03-28	Yang, et al.	

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /CC/

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PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** **Mail Stop ISSUE FEE**
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35690 7590 05/06/2009

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P.O. BOX 398
AUSTIN, TX 78767-0398

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(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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11/621,724 01/10/2007 Patrick J. Holly 5707-12800 1652

TITLE OF INVENTION: PAD ESD SPREADING TECHNIQUE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
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nonprovisional NO \$1510 \$300 \$0 \$1810 08/06/2009

EXAMINER	ART UNIT	CLASS-SUBCLASS
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CLARK, CHRISTOPHER JAY 2836 361-056000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1. Meyertons Hood Kivlin Kowert & Goetzel, P.C.
2. Jeffrey C. Hood
3.

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Standard Microsystems Corporation

Hauppauge, New York

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
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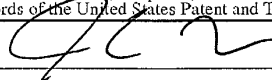
- ☐ A check is enclosed.
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5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

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Authorized Signature



Date

2009-06-18

Typed or printed name

Jeffrey C. Hood

Registration No.

PTO # 35,198

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Electronic Patent Application Fee Transmittal				
Application Number:		11621724		
Filing Date:		10-Jan-2007		
Title of Invention:		PAD ESD SPREADING TECHNIQUE		
First Named Inventor/Applicant Name:		Patrick J. Holly		
Filer:		Jeffrey C Hood/Jeanne Miranda		
Attorney Docket Number:		5707-12800		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	1501	1	1510	1510
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Printed copy of patent - no color	8001	2	3	6
Total in USD (\$)				1816

Electronic Acknowledgement Receipt	
EFS ID:	5545779
Application Number:	11621724
International Application Number:	
Confirmation Number:	1652
Title of Invention:	PAD ESD SPREADING TECHNIQUE
First Named Inventor/Applicant Name:	Patrick J. Holly
Customer Number:	35690
Filer:	Jeffrey C Hood/Jeannie Miranda
Filer Authorized By:	Jeffrey C Hood
Attorney Docket Number:	5707-12800
Receipt Date:	18-JUN-2009
Filing Date:	10-JAN-2007
Time Stamp:	17:27:09
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$1816
RAM confirmation Number	3704
Deposit Account	501505
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	5707-12800_issue_fee.pdf	90926	no	1
			a65037b481020cff668a1baedeb21757&fd5e74		
Warnings:					
Information:					
2	Fee Worksheet (PTO-875)	fee-info.pdf	33504	no	2
			1f1c62de5584e0fc3d5ee09bc66e74f062b71019		
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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/621,724	07/21/2009	7564665	5707-12800	1652

35690 7590 07/01/2009
MEYERTONS, HOOD, KIVLIN, KOWERT & GOETZEL, P.C.
P.O. BOX 398
AUSTIN, TX 78767-0398

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

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APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Patrick J. Holly, Tempe, AZ;
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David R. Rice, Phoenix, AZ;

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Application	Document	Mailroom Date	Attorney Docket No.
11621724	ISSUE.NTF	07/01/2009	5707-12800

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