

Patent No. 7,564,665
Petition For *Inter Partes* Review

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APTIV SERVICES US, LLC
Petitioner,

v.

MICROCHIP TECHNOLOGY, INC.
Patent Owner.

Patent No. 7,564,665

Case No. IPR2024-00803

DECLARATION OF DR. MICHAEL S. CHEN

I, Dr. Michael S. Chen, make this declaration in connection with the proceeding identified above.

I. BACKGROUND

1. I have been retained by counsel for Aptiv Services US, LLC (“Aptiv”) as a technical expert in connection with the proceeding identified above. I submit this declaration in support of Aptiv’s Petition for *Inter Partes* Review of United States Patent No. 7,564,665 (the “’665 patent”).

2. I have personal knowledge of the facts and opinions set forth in this declaration and believe them to be true. If called upon to do so, I would testify competently thereto. I have been warned that willful false statements and the like are punishable by fine or imprisonment, or both.

3. I am being paid at an hourly rate for my work on this matter. I have no personal or financial stake or interest in the outcome of the present proceeding.

4. I have reviewed and am familiar with the ’665 patent. I understand that claims 1-18 (“the challenged claims”) of the ’665 patent are being challenged.

5. In this declaration, I present certain opinions regarding the knowledge and skill of a person of ordinary skill in the art (“POSITA”), and regarding whether such a person would have found the challenged claims of the ’665 patent obvious in view of the prior art as of the patent’s claimed priority date of January 10, 2007. I

conclude that a POSITA would have found each claim obvious under each of the petitioned grounds.

6. I note that some of my opinions assume specific interpretations of claim elements with which I do not necessarily agree. I present these opinions because I have been asked to consider whether a POSITA would find the claims obvious over the petitioned grounds if these interpretations applied. I will identify these opinions as they arise below.

II. QUALIFICATIONS

7. I am a tenured full professor of Electrical Engineering at the University of Southern California, where I have been a faculty member since 2011. As a professor, I research and teach electrical circuit design. My research focuses on analog mixed-signal and RF circuit architectures for data converters (both ADC and DAC), clock generation (such as PLL and DLL), digital VLSI, SoC, mostly-digital circuits, artificial intelligence (AI) and machine learning (ML) accelerators, analog CAD, and power amplification (PA). My research has been applied to wireless, wireline communications, computing, IoT systems, autonomous vehicles, etc.

8. I earned my Ph.D. and M.Sc. in Electrical Engineering and Computer Science from the University of California, Berkeley in 2006 and 2002 respectively. I received my B.S. degree from National Taiwan University, where I graduated as the top student in the upper division.

9. My work has been recognized by both academic and commercial entities. I have published over 90 conference, journal, magazine articles, including multiple publications in the IEEE International Solid State Circuits Conference (ISSCC), IEEE Symposium on VLSI Circuits (VLSIC), IEEE Custom Integrated Circuits Conference (CICC), IEEE European Conference on Solid-State Circuit (ESSCIRC), IEEE Radio Frequency Integrated Circuits Symposium (RFIC), IEEE Journal of Solid-State Circuits (JSSC), and Transactions on Circuit and System I (TCAS-I). My research has been funded by the National Science Foundation (NSF), ONR, IARPA, SRC, DARPA and various industry companies. I have also served as a technical consultant for companies including Qualcomm, Tetramem, BAE Systems and Samsung.

10. I have received recognition for my work and research. In 2024, I was honored with the grade of IEEE Fellow to recognize my technical contributions in solid-state circuit society. This grade is reserved for 0.1% of IEEE members. In 2023, I was the co-recipient of the ISSCC Jack Kilby Award for significant advances in analog mixed-signal circuits. In 2022, I was a co-recipient for the RFIC 2022 Best Student Paper Award for my work with students in my laboratory on a circuit prototype. From 2021 to 2023, I was the IEEE Solid-State Circuit Society (SSCS) Distinguished Lecturer. I have been invited to offer seminars, workshops, keynote talks, and panel discussions in major IEEE conferences, IEEE SSCS chapters, and

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universities on a range of topics covering fundamental to advanced integrated circuit design and how to improve the performance and/or reduce cost of a circuit or system. In 2019, I was also the recipient of Qualcomm Faculty Award, and in 2014 both the NSF Faculty Early Career Development (CAREER) Award and DARPA Young Faculty Award (YFA). As a student, I was the recipient of a UC Regents' Fellowship at Berkeley in 2000 and the Analog Devices Outstanding Student Award for IC design in 2006.

11. ESD protection is ubiquitous in modern integrated circuits. Thus, I have used ESD protection extensively throughout my career. More importantly, I am familiar with the underlying technologies used to facilitate ESD protection—such as transistors and RC circuits—as well as the design considerations used by integrated circuit designers and electrical engineers.

12. A copy of my curriculum vitae is attached as Appendix A.

III. MATERIALS CONSIDERED

13. In preparing this declaration, I have reviewed, among other things, the following materials:

Document	Exhibit #
U.S. Patent No. 7,564,665 to Holly et al.	1001
Prosecution History of U.S. Patent No. 7,564,665	1003

Inter Partes Review of U.S. Patent No. 7,564,665

U.S. Pat. No. 6,529,359 to Verhaege et al.	1004
U.S. Pat. No. 6,249,410 to Ker et al.	1005
U.S. Pat. No. 7,589,945 to Miller et al.	1006

14. I have also reviewed the Petition for *Inter Partes* Review of the '665 patent, to which my declaration relates.

IV. DEFINITIONS AND STANDARDS

15. I have been informed and understand that claims are construed from the perspective of a POSITA at the time of the claimed invention, and that during *inter partes* review, the same claim construction standard is applied as in a district court proceeding.

16. I have been informed and understand that the subject matter of a patent claim is obvious if the differences between the subject matter of the claim and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains.

17. I have been informed that the framework for determining obviousness involves considering the following factors: (i) the scope and content of the prior art; (ii) the differences between the prior art and the claimed subject matter; (iii) the level of ordinary skill in the art; and (iv) any objective evidence of non-obviousness.

18. I understand that the claimed subject matter would have been obvious to one of ordinary skill in the art if, for example, it results from the combination of known elements according to known methods to yield predictable results, the simple substitution of one known element for another to obtain predictable results, use of a known technique to improve similar devices in the same way or applying a known technique to a known device ready for improvement to yield predictable results. I have also been informed that the analysis of obviousness may include recourse to logic, judgment and common sense available to the person of ordinary skill in the art that does not necessarily require explication in any reference.

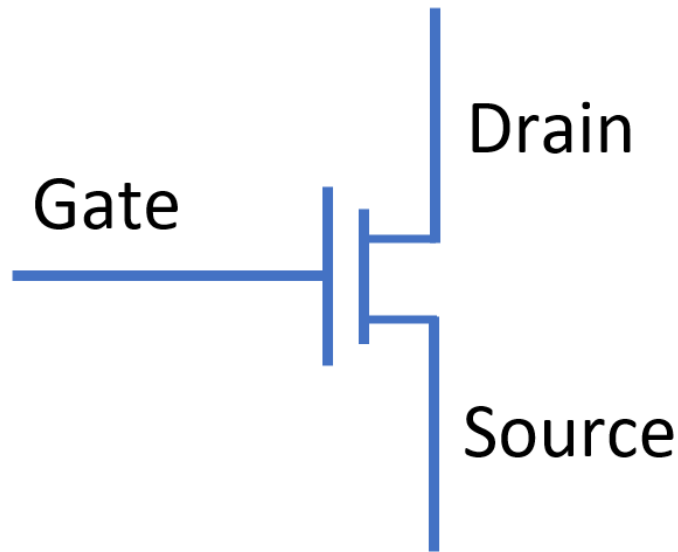
V. TECHNICAL BACKGROUND

19. In the following sections, I present some background principles from analog circuit design that would have been known to a POSITA on Jan. 10, 2007.

A. Transistors

20. A transistor is a basic electrical component that acts as a switch. A MOS transistor (a.k.a MOSFET) is a type of transistor that is controlled by voltage signals.

21. A MOS transistor has three key parts: a gate, a drain, and a source. In electrical schematics, the gate, drain, and source are commonly depicted as shown below.



22. When the MOS transistor is turned off, the drain and source are not electrically connected. In other words, there is an “open circuit” between them. But when the MOS transistor is turned on, the drain and source are electrically connected and current can flow through the device.

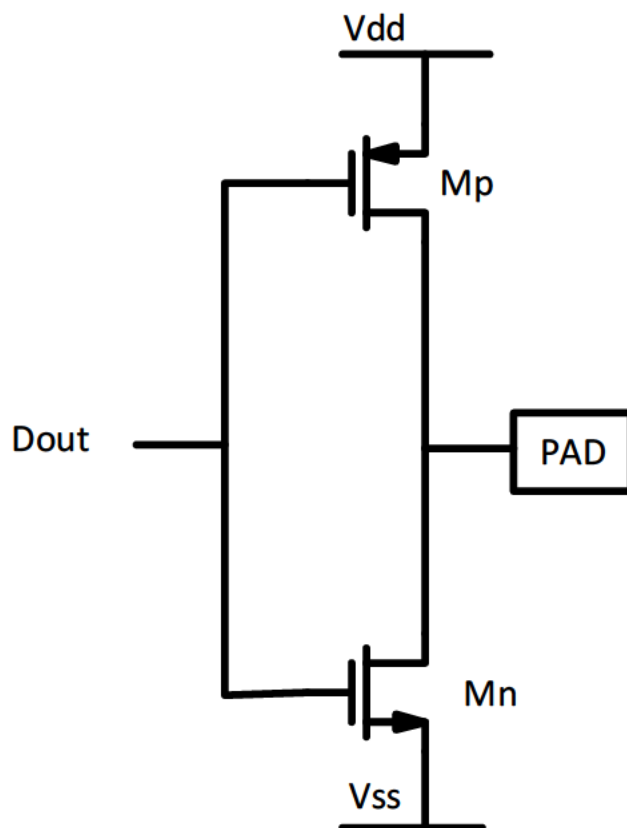
23. The gate controls whether the MOS transistor is on or off. Specifically, a voltage signal is placed at the gate. This is commonly referred to as the “gate voltage.” The gate voltage is compared to a “threshold voltage” at which the switch changes state (i.e., switches from on to off or vice versa).

24. There are two types of MOS transistors, P type and N type. A P type device may also be referred to as a P channel device, PMOS, or PMOS transistor.

Similarly, an N type device may be called an N channel device, NMOS or NMOS transistor.

25. For our purposes, the difference is simple: a PMOS device activates when the gate voltage is *less* than the source voltage minus the threshold voltage. An NMOS device, on the other hand, activates when the gate voltage is *greater* than the source voltage plus the threshold voltage.

26. Transistors are commonly used to drive a signal at a digital I/O pad with an inverter driver configuration. A typical implementation is shown below.



27. The source voltage of the NMOS (Mn) is ground and the source voltage of the PMOS (Mp) is Vdd. The devices receive the same gate voltage via the signal line Dout. Thus, a low gate voltage will turn on the PMOS device and turn off the NMOS device. Conversely, a high gate voltage will turn off the PMOS device and turn on the NMOS device.

B. Electrostatic Discharge

28. Prior to the priority date of the '665 patent, Jan. 10, 2007, electrostatic discharge was a well-known problem in the art of integrated circuit design. (*See e.g.*, EX-1005.)

29. An electrostatic discharge (“ESD”) is the sudden flow of electricity between two objects and “one of the main reliability concerns” for integrated circuits. (EX-1005, 1:13-1:14.) During an ESD event (e.g., static charge flows from a human body to an integrated circuit chip), an integrated circuit with a low operating voltage (i.e., 5 volts) might be subjected to thousands of volts of electricity. (*Id.*, 1:20-1:24.) Without precautionary measures, this extreme voltage can damage electrical components in the integrated circuit chip. (*Id.*, 1:15-1:20.)

C. ESD Protection

30. Solutions to prevent ESD damage were equally well known before the '665 patent. (*See e.g.*, EX-1005.)

31. By the early 2000's it was standard practice to include ESD protection in integrated circuits. (*Id.*) In general, an ESD protection circuit protects sensitive components by providing an alternative path for ESD energy. Most commonly, a transistor is connected between a power rail and ground in parallel to sensitive components. (*E.g.*, EX-1004, 2:45-2:58) During normal operation, the transistor remains off and has no effect on the circuit. But when an ESD occurs, the transistor activates and allows the excess energy to flow harmlessly from the power rail to ground. The transistor is known as an ESD protection clamp, clamp transistor, or clamp. (EX-1006, 1:24-1:25.)

32. In addition to ESD protection clamps, POSITAs understood that any means of dissipating and/or storing ESD energy would help reduce the peak voltage developed in the system. For example, the art teaches that diodes, Zener diodes, various ESD dissipation circuits, and capacitors can reduce voltage spikes during ESD events. (EX-1005, 12:9-12:11, 12:20-12:26, 12:39-12:56, 14:42-47; EX-1006, 1:16-1:20; EX-1004, 3:56-3:66, 4:14-4:20.)

33. To activate these various protective devices, a circuit to detect an ESD event was also required. This circuit had to distinguish between a normal rise in voltage (i.e., circuit power-up) and a voltage rise due to an ESD event. Because voltage spikes from ESD occur so quickly, the RC circuit emerged as the preferred ESD detection device.

34. An RC circuit is a low-pass filter, meaning only low frequency voltage changes can pass through. In other words, when the input to an RC circuit changes slowly, the output of the RC circuit tracks the signal closely. But when the input changes suddenly, the output can no longer keep up. Thus, POSITAs understood that an ESD event could be detected by comparing the voltage of the entire circuit (i.e., the input) to the voltage of the RC circuit (i.e., the output). During an ESD event, there would be a large difference between the two voltages.

35. RC circuits, and their ability to detect ESD events, were well-known prior to the '665 patent. (EX-1004, 3:1-3:13, Figure 2; EX-1005, 19:37-19:58, Figure 29; EX-1006, 12:47-12:52.)

36. One challenge of implementing ESD protection is that the magnitude and polarity of ESD events vary. Nor is it known what operating state the circuit will be in when an ESD event occurs. As such, the performance of the protection circuit may vary based on the ESD event. Nevertheless, designers include protection circuits because even a solution that might only work during some ESD events, or provide imperfect protection, reduces the overall risk of damage to sensitive components.

D. Design Considerations

37. As the prior art makes clear, a POSITA must balance several considerations when designing an ESD protection circuit.

38. First, ESD events are most likely to originate where the integrated circuit is exposed to the outside world. For many circuits, the most exposed elements are the input/output (“I/O”) pins—used to connect with other devices—and their associated circuitry. Consequently, much of the prior art concerns ESD protection for I/O pins, pads, and circuits. (*E.g.*, EX-1006; EX-1005; EX-1004.)

39. Second, ESD protection is generally most effective when it is close to the I/O circuitry. Most ESD protection circuits work by providing ESD energy with an alternative path to ground. (*E.g.*, EX-1005, 2:45-2:58.) If there is high resistance along that path, then the system will experience a higher voltage spike during an ESD, risking damage to components. (EX-1006, 1:36-1:44.) Keeping ESD protection close to the I/O circuitry minimizes resistance. To that end, the prior art suggests including an ESD protection circuit at every I/O pad. (EX-1006, 1:16-1:23, 1:36-1:39.)

40. Third, space on an integrated circuit chip is limited. This is particularly true near the I/O circuitry of chips with many I/O pins. (EX-1006, 1:29-39.) Size constraints incentivize POSITAs to minimize the footprint of ESD protection circuitry and, to the extent possible, use components for multiple purposes to maximize efficiency. (EX-1006, 7:48-7:52; 7:63-7:67.)

41. Fourth, the components used for ESD protection are not immune to damage from high voltage and/or current that can occur during an ESD event. Larger

ESD clamps can withstand higher currents, but also cost more and occupy more space. Thus, engineers may use multiple protective circuits in parallel to dissipate ESD energy, allowing them to dissipate greater ESD events with smaller, less expensive components. (EX-1006, 2:44-2:52, 7:48-7:52; 7:63-7:67.)

VI. THE '665 PATENT

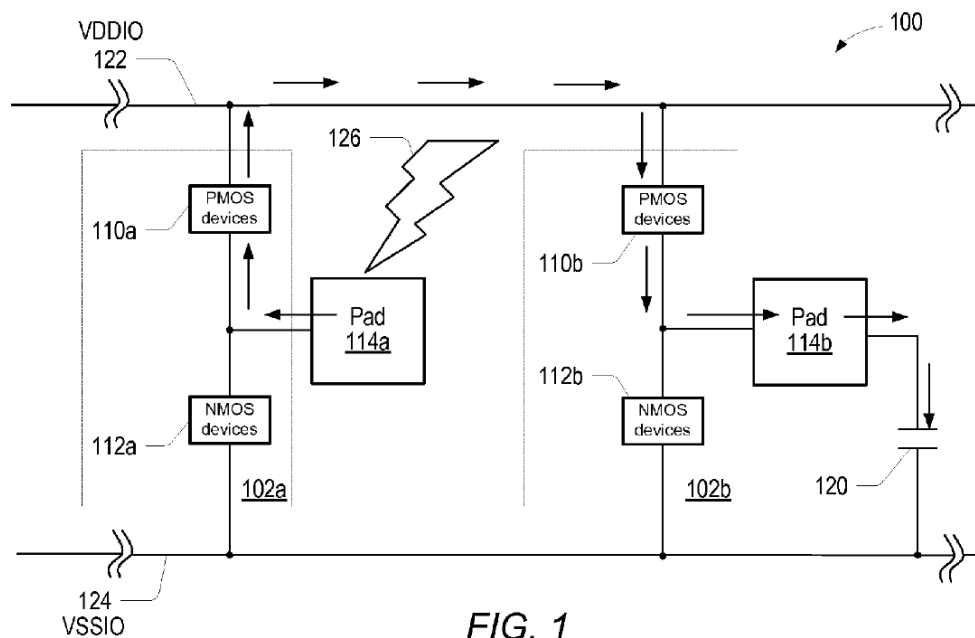
42. The '665 patent is titled “Pad ESD Spreading Technique.” It purports to mitigate an ESD event by charging the capacitance of one or more I/O pads. (EX-1001, Abstract.)

43. As discussed in the technical background section, integrated circuits require ESD protection, but space is limited. (EX-1006, 1:29-39.) The '665 patent identifies the same problem, noting the difficulty of providing robust ESD protection “without increasing the required silicon area.” (EX-1001, 2:3-2:6.)

44. In addition to “established solutions, such as various clamp devices and clamp circuits,” the '665 patent proposes storing ESD energy in the I/O pads themselves. (EX-1001, 2:21-29.) This is possible because, as physical, conductive objects, I/O pads have capacitance. Specifically, each pad is a physical, conductive component near or above other conductive components and/or substrate, so it acts like a capacitor because there are multiple conductive devices separated by an

insulator. In some embodiments of the '665 patent, each I/O pad has a capacitance of approximately 3 pF.¹ (EX-1001, 3:44-3:50.)

45. Figure 1 of the '665 patent, reproduced below, shows a partial block diagram of one embodiment. (EX-1001, 3:11-3:15.)



(EX-1001 Figure 1)

46. In Figure 1, ESD event 126 occurs at I/O pad 114a. (*Id.*, 4:7-4:9.) In response, pad circuit 102a turns on PMOS devices 110a, allowing energy to flow to VDDIO rail 122. (*Id.*, 4:7-4:13.) If PMOS devices 110b are also on, charge will flow to I/O pad 114b. (*Id.*) Because I/O pad 114b has capacitance (signified by capacitor

¹ A farad is SI unit of capacitance: the ability of a body to hold electrical charge. The pico-prefix means that the base unit is multiplied by 1.0E-12. Therefore, a capacitance of 3 pF is 0.000000000003 farads.

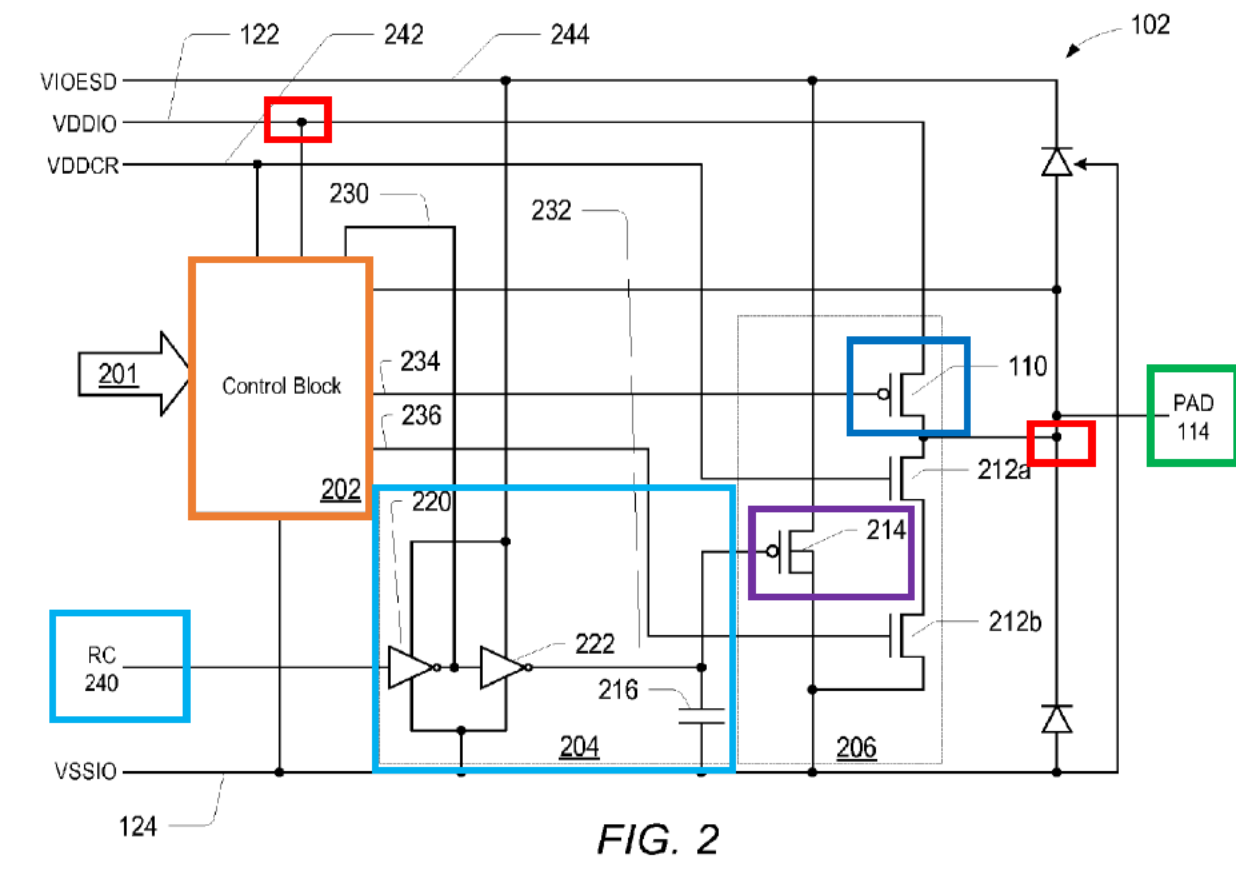
FIG. 2

(EX-1001, Figure 2)

48. During an ESD event, the rapid change in voltage activates clamp control circuit 204. (*Id.*, 5:9-5:13.) Clamp control circuit 204 turns on clamp device 214, thereby shunting energy from a voltage rail to ground. (*Id.*, 5:13-5:17.) In other words, the '665 patent uses an “established solution[], such as various clamp devices and clamp circuits.” (EX-1001, 2:21-29.)

49. Meanwhile, control block 202 also sends signals to output buffer 206: a signal driver circuit including PMOS and NMOS devices. (*Id.*, 4:27-4:33, 4:54-4:64.) Specifically, control block 202 enables PMOS device 110. (*Id.*, 5:6-5:8.) This “connects VDDIO rail 122 and its associated capacitance (which may comprise all the other pads or pad cells) to the physical pad affected by the ESD event.” (*Id.*, 5:30-5:32.) The capacitance associated with rail 122 will absorb some of the ESD energy, thereby reducing the peak voltage developed in the system. (*Id.*, 5:33-5:35.)

50. Many of the claims of the '665 patent are directed to the configuration of various components—including nodes, a control block, enable circuitry, a clamp device, an output transistor, and an I/O pad—shown in Figure 2. These components are identified in the annotated figure below based on a POSITA's reading of the '665 patent.



(EX-1001, Figure 2 (annotated).)

Component	Exemplary Limitation	Color
First and second nodes	[1a], [1b]	Red
Control block	[1d]	Orange
Enable circuitry	[1f]	Light Blue
Clamp device	[1e]	Purple
Output transistor	[1c]	Dark Blue
I/O pad	[1b]	Green

VII. LEVEL OF ORDINARY SKILL IN THE ART

51. In my opinion, a POSITA in the field of the '665 patent in 2007 would have had at least a Master's Degree in Electrical Engineering, or a Bachelor's Degree

in Electrical Engineering plus two years of experience working on analog circuit design.

VIII. ANALYSIS OF THE PETITIONED GROUNDS

52. I understand that Aptiv challenges all claims of the '665 patent based on a first ground of obviousness based on Verhaege; and a second ground of obviousness based on Verhaege in view of Miller; and a third ground of obviousness based on Ker.

IX. GROUNDS OF UNPATENTABILITY

A. Ground 1 (Verhaege)

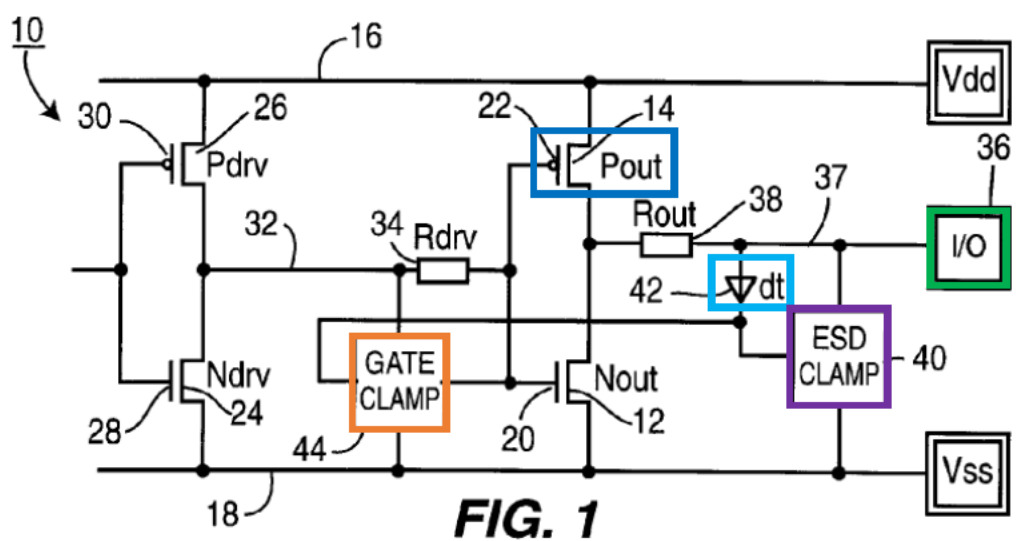
53. I have reviewed Exhibit 1004 to the Petition, which is U.S. Patent No. 6,529,359 to Verhaege et al. ("Verhaege"). Having compared Verhaege's disclosures to the '665 patent's claims, it is my opinion that the claims are obvious over Verhaege in view of the background knowledge of a POSITA.

1. Summary of Verhaege

54. Verhaege discloses a circuit to protect an output driver transistor during an ESD event or electrical overstress ("EOS"). (EX-1004, 1:9-1:13.) Verhaege uses a conventional ESD clamp to shunt excess voltage during an ESD event. But like the '665 patent, Verhaege recognizes that a clamp is a partial but imperfect solution: "when an electrical EOS/ESD is clamp is added, a problem can arise when the EOS or ESD stress is applied to the I/O pad." (*Id.*, 1:22-1:24.) Namely, "the circuit or part

of the circuit gets powered up dynamically” and “the pre-drive circuits will force either a high or low state at the gate of the final output drivers which is undesirable.” (*Id.*, 1:26-1:27, 1:28-1:30.)

55. To address this issue, Verhaege teaches a gate clamp connected to the gates of the output transistors. (EX-1004, 1:48-1:50.) In addition, an ESD clamp is attached in parallel to the NMOS transistor between the input/output (“I/O”) pad and the Vss line. (*Id.*, 1:48-1:50.) Finally, Verhaege discloses circuitry to activate both clamps during an ESD event. (EX-1004, 2:20-2:22, 2:29-2:30.) Verhaege’s Figure 1, included below, shows one embodiment of the resulting circuit.



(EX-1004, Figure 1 (annotated).)

56. Verhaege explains that dynamic trigger device 42 (light blue) detects an ESD event and sends a signal to gate clamp 44 (orange) and ESD clamp 40 (purple). ESD clamp 40 connects I/O pad 36 (green) to the Vss rail, thereby diverting

some ESD energy. (*Id.*, 2:29-2:30, 2:37-2:39.) But in addition, gate clamp 44 grounds the gates of NMOS output transistor 12 and PMOS output transistor 14 (dark blue). (*Id.*, 2:32-2:34.) This activates PMOS transistor 14 and allows ESD energy to flow to the Vdd rail. From there, the ESD energy charges the capacitance of the rail and/or the capacitance of any devices connected to the rail.

2. Claim-by-Claim Analysis

57. As detailed below, Verhaege renders every limitation of the challenged claims obvious.

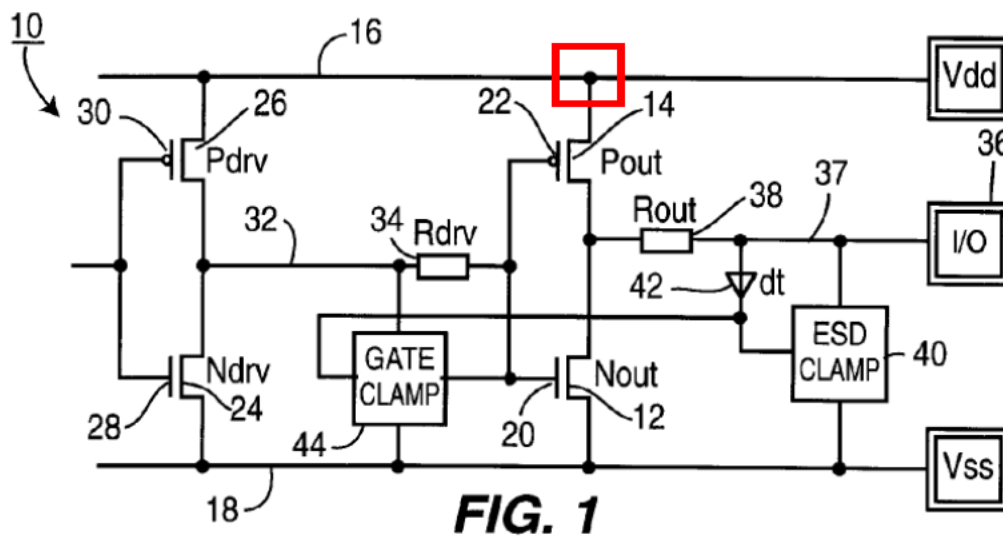
Claim 1 A pad circuit configured to provide protection against electrostatic discharge (ESD) in a system comprising the pad circuit, the pad circuit comprising:

58. Verhaege teaches *a pad circuit*² because in Verhaege, “[a]n I/O pad is connected to the junction of the output driver transistors.” (EX-1004 at Abstract.) The pad circuit is also *configured to provide protection against electrostatic discharge (ESD) in a system* because the Verhaege invention is a “circuit for the protection of an output driver NMOS transistor during EOS/ESD stress.” (EX-1004 at Abstract.)

² For ease of reference, I will identify claim language from the '665 patent using *italics*.

[a] a first node coupled to a first voltage rail;

59. In Figure 1, Verhaege teaches that output driver transistors 14 and 12 are coupled in series between a Vdd rail and a Vss rail. (EX-. Verhaege, 1:66-2:3.) The *first node coupled to a first voltage rail* is where output PMOS transistor 14 meets the Vdd rail, as indicated in red below.

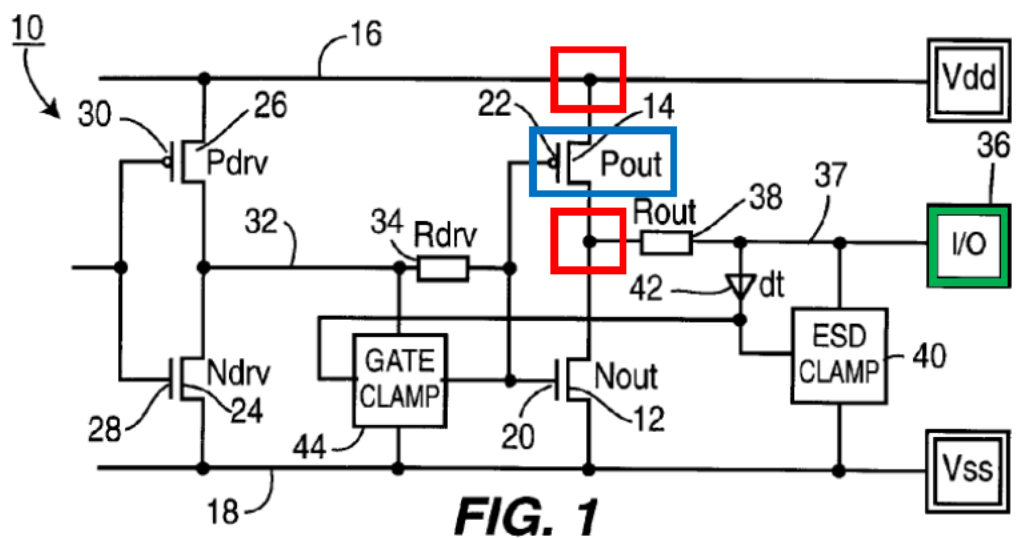


(EX-1004, Figure 1 (annotated).)

[b] [the pad circuit comprising] a second node coupled to a physical pad having capacitance;

60. First, Verhaege teaches *a second node coupled to a physical pad* because “[a]n I/O pad is connected to the junction of the output driver transistors.” (EX-1004 Abstract, 2:16-8.) In Figure 1, for example, “I/O pad 36 is electrically connected to the junction between the output driver NMOS transistor 12 and the output driver PMOS transistor 14 by line 37 and through an output resistor 38.” (EX-

transistor 14 (dark blue) is coupled to the VDD rail at the first node (red) and to the I/O pad 36 (green) at a second node (red) via an output resistor. (EX-1004 1:66-2:2, 2:16-2:19.) Thus, PMOS transistor 14 is an *output transistor device[] coupled between the first node and the second node.*



(EX-1004, Figure 1 (annotated).)

63. PMOS transistor 14 is *operable to at least partially drive an output signal at the second node.* Verhaege explicitly describes PMOS transistor 14 and NMOS transistor 12 as output drivers. (EX-1004 1:66-2:2.) A POSITA would understand that the primary function of output driver transistors is to drive a signal at an I/O pad. Here, pre-driver NMOS transistor 24 and pre-driver PMOS transistor 26 send a signal to the gates of PMOS transistor 14 and NMOS transistor 12 via line 32. The signal activates one transistor, connecting I/O pad 36 to either Vdd or Vss and thereby creating a “high” or “low” output signal. As discussed above, in Figure

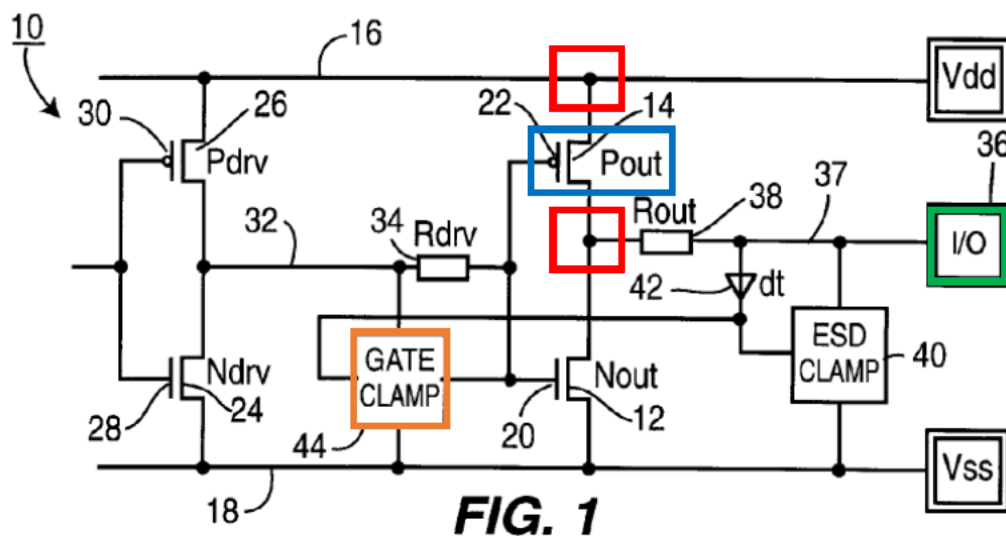
1 the second node is coupled to I/O pad 36. Thus, PMOS transistor 14 is *operable to at least partially drive an output signal at the second node.*

[d] a control block configured, to turn on, when instructed, at least one of the one or more output transistor devices to charge the pad capacitance to reduce a maximum voltage developed in the system as a result of the ESD event;

64. I understand that, within the '665 patent, a “control block” may contain “any digital, analog, and/or mixed mode circuitry configured to perform the functions assigned to the control block.” (EX-1001, 4:43-4:46.) Here, the function of the control block is to “turn on, when instructed, at least one of the one or more output transistor devices to charge the pad capacitance to reduce a maximum voltage developed in the system as a result of the ESD event.” (EX-1001, Claim 1.)

65. Verhaege teaches analog circuitry for this same purpose. Verhaege discloses *a control block configured to turn on, when instructed, at least one of the one or more output transistor devices* in the form of gate clamp 44. In Figure 1, gate clamp 44 (orange) is connected to the gates of output transistor 12 and output transistor 14 (dark blue). (EX-1004, 2:23-2:25.) As discussed above, PMOS transistor 14 is an output transistor device. During an ESD event, gate clamp 44 connects the gates of both output transistors to ground. (EX-1004, 2:23-2:25, 2:32-2:34.) This turns off NMOS transistor 12 and turns on PMOS transistor 14. (EX-

1004, 2:32-2:37.) Thus, gate clamp 44 is configured to turn on, when instructed, at least one of the output transistor devices (i.e., PMOS transistor 14.)

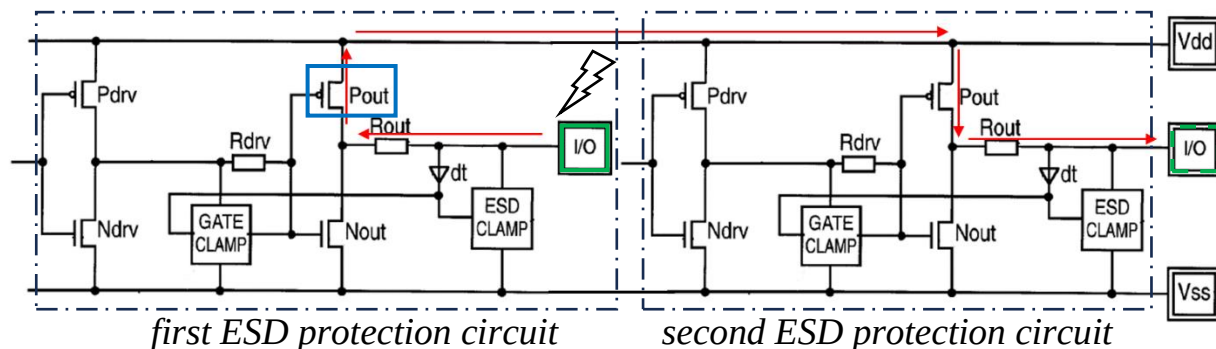


(EX-1004, Figure 1 (annotated).)

66. The limitation also requires *charg[ing] the pad capacitance to reduce a maximum voltage developed in the system as a result of the ESD event*. Verhaege renders this limitation obvious because, in practice, the Verhaege circuit also charges the pad capacitance.

67. Verhaege teaches an improved ESD protection circuit for an I/O pad. But most integrated circuits had multiple I/O pads by at least 2007, any of which could be exposed to an ESD event. A POSITA would understand that, to fully protect the integrated circuit, the Verhaege invention would be repeated at every I/O pad. The annotated figure below shows the ESD protection circuit of Verhaege's Figure 1 repeated for two I/O pads. When the PMOS transistor (dark blue) of the first circuit

connects the first I/O pad (solid green) to the Vdd rail, the first I/O pad becomes electrically connected to all other pads currently connected to the Vdd rail. The figure below shows a second circuit comprising a second I/O pad (dashed green) also connected to the Vdd rail. This allows the ESD energy to flow from the first I/O pad to other I/O pads (such as the second I/O pad (dashed green)), charging their capacitance and reducing the maximum voltage developed in the system.

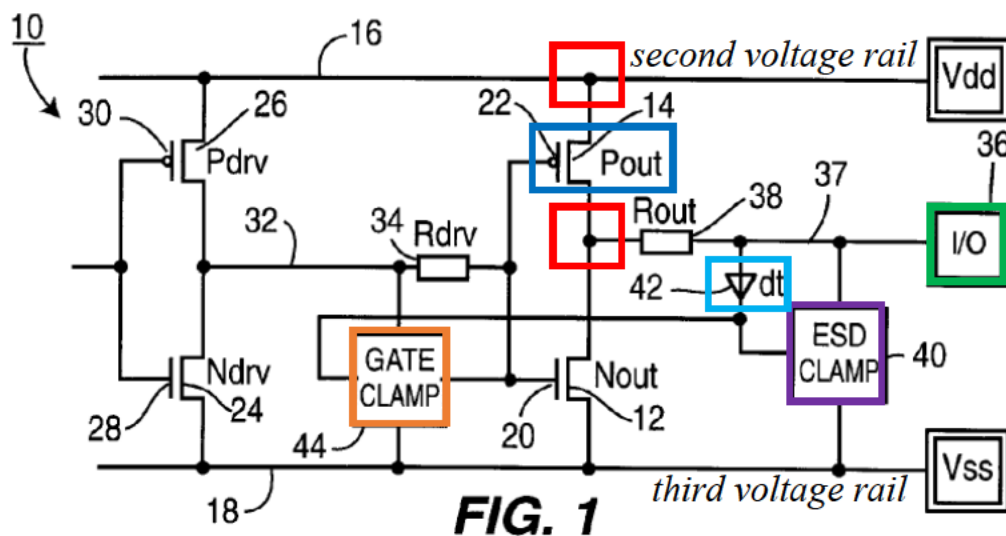


[e] a clamp device configured between a second voltage rail and a third voltage rail to reduce, when turned on, the maximum voltage developed in the system as the result of the ESD event;

68. At least under Microchip's apparent interpretation of this limitation as evidenced by its infringement contentions, Verhaege discloses this limitation.

69. I understand that Microchip's position is that the *first voltage rail* of claim 1[a] and *second voltage rail* of claim 1[e] can refer to the same voltage rail and/or be connected to each other. I further understand that, according to Microchip, the clamp need not be connected directly to both voltage rails to be *configured between* them. If so, Verhaege discloses a *second voltage rail* in the form of the Vdd

rail. Verhaege's *third voltage rail* is the Vss rail. Verhaege further discloses in Figure 1 a *clamp device configured between these rails*: ESD clamp 40 (purple).



(EX-1004, Figure 1 (annotated).)

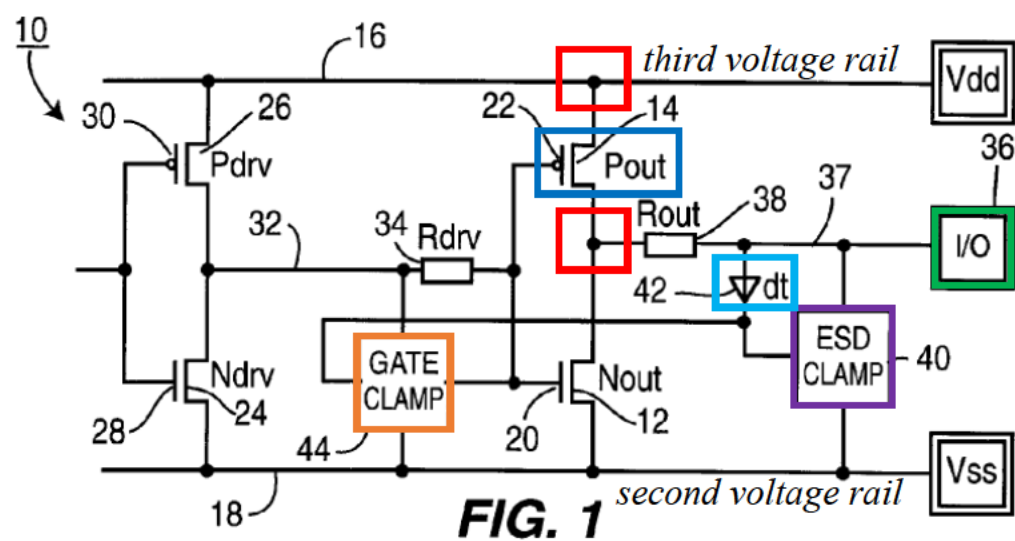
70. During an ESD event, ESD clamp 40 is *turned on* by the dynamic trigger device 42 (light blue). (EX-1004, 2:29-2:30.) This connects I/O pad 36 (green) to the Vss rail and *reduce[s] . . . the maximum voltage developed in the system as the result of the ESD event* because “the ESD stress can be diverted to the parallel ESD clamp and the EOS/ESD capability is achieved.” (EX-1004, 2:37-2:39.)

[f] enable circuitry configured to turn on the clamp device and instruct the control block to turn on the at least one of the one or more output transistor devices, in response to the ESD event;

71. As discussed previously, Verhaege discloses a clamp device in ESD clamp 40 and a control block in gate clamp 44. Verhaege also teaches enable

circuitry to (1) turn on the clamp device and (2) instruct the control block to turn on the at least one or more output transistor devices.

72. In Figure 1, for example, Verhaege discloses *enable circuitry* in the form of dynamic trigger device 42 (light blue). The input of dynamic trigger device 42 is connected to I/O pad 36 (green) where the ESD event originates. (EX-1004, 2:20-2:22.) The output of dynamic trigger device 42 is connected to the *clamp device* (i.e., ESD clamp 40 (purple)). (EX-1004, 2:21-2:23.) Dynamic trigger device 42 is *configured to turn on the clamp device* because “dynamic trigger device 42 is used to trigger the ESD clamp 40.” (EX-1004, 2:29-2:30.)



(EX-1004, Figure 1 (annotated).)

73. Meanwhile, dynamic trigger device 42 is also connected to the control block (i.e., gate clamp 44 (orange)). A POSITA would understand that dynamic trigger device 42 must *instruct* gate clamp 44 to turn on because “gate clamp 44

grounds the gate 20 of the output driver NMOS transistor 12 under transient over voltage stress conditions.” (EX-1004, 2:32-2:34.) As discussed above, the gate clamp 44 then *turn[s] on the at least one of the one or more output transistor devices* (i.e., PMOS transistor 14 (dark blue)) by grounding the gates of the output transistors. *Id.*

[g] wherein the second voltage rail is configured to provide power to the enable circuitry, and wherein the third voltage rail has a value below the first voltage rail.

74. At least under Microchip’s apparent interpretation of this limitation as evidenced by its infringement contentions, Verhaege discloses this limitation.

75. As discussed previously, Verhaege discloses a *second voltage rail* in the Vdd rail and a *third voltage rail* in the Vss rail based on Microchip’s apparent interpretations. A POSITA would understand that, by convention, the *second voltage rail*—Vdd—is *configured to provide power* to the circuit, which necessarily includes *the enable circuitry*. In Figure 1, for example, the enable circuitry is dynamic trigger device 42 as discussed in claim 1[f]. Dynamic trigger device 42 is powered by the second voltage rail when PMOS transistor 14 turns on.

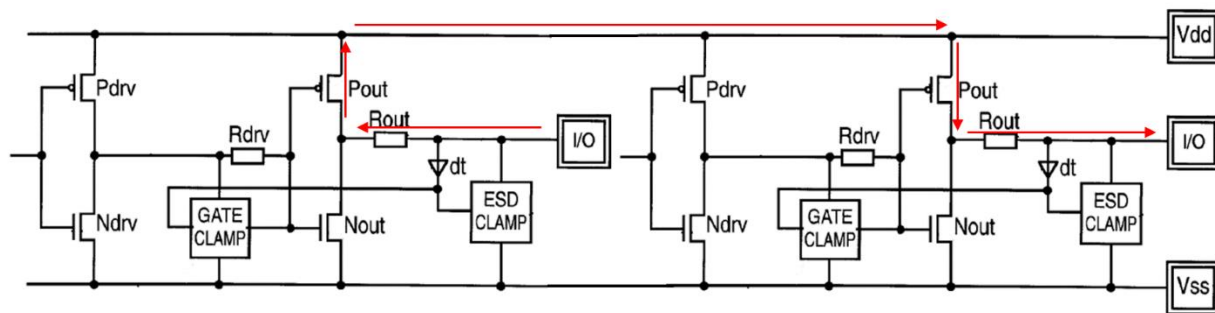


76. Based on Microchip's infringement contentions, I understand that Microchip interprets *wherein the third voltage rail has a value below the first voltage rail* to refer to voltage. If so, Verhaege discloses this limitation because, by definition, the first voltage rail (i.e., Vdd) has a positive voltage whereas the third voltage rail (i.e., Vss) is ground or a negative voltage rail. This means the third voltage rail *has a value below* the first voltage rail.

77. As discussed previously in claim 1[d], Verhaege teaches a *control block* (i.e., gate clamp 44) that turns on *at least one of the one or more output transistor*

devices (i.e., PMOS transistor 14.) By turning on PMOS transistor 14, gate clamp 44 couples the *first voltage rail* (i.e., Vdd) to the *physical pad* (i.e., I/O pad 36.) As a physical, conductive device, the Vdd rail has an *associated capacitance*. When I/O pad 36 is connected to the Vdd rail during an ESD event, the excess voltage charges the *associated capacitance* of the Vdd rail, thereby *reduc[ing] the maximum voltage developed in the system as a result of the ESD event*.

78. To the extent that the *associated capacitance of the first voltage rail* must be greater than its inherent capacitance (i.e., the capacitance of the rail itself), Verhaege still discloses the claim. As discussed in claim 1[e], integrated circuit devices typically had multiple I/O pads as of 2007, each of which required ESD protection. Thus, a POSITA would understand that the Verhaege invention is most effective applied at each I/O pad. As such, when the I/O pad 36 is coupled to the Vdd rail, the *associated capacitance* of the Vdd rail is equal to the sum of all other capacitive devices (i.e., I/O pads) currently connected to the Vdd rail plus the inherent capacitance of the rail itself. This further *reduce[s] the maximum voltage developed in the system by shar[ing] a charge* across a greater capacitance as shown below.

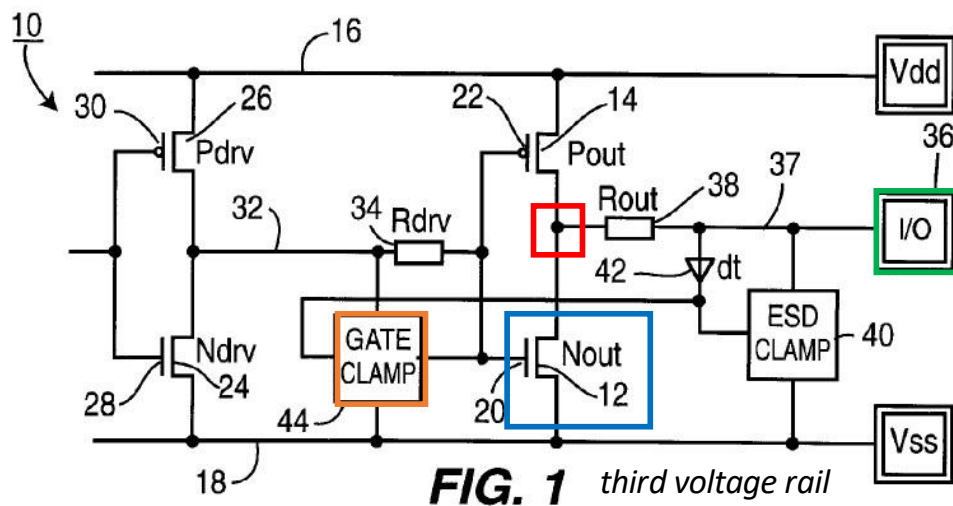


Claim 3 The pad circuit of claim 1, wherein the one or more output transistor devices are PMOS devices.

79. Verhaege discloses this claim because, as discussed in claim 1[c], the one or more output transistor devices (i.e., PMOS transistor 14) is a PMOS device. (EX-1004, 1:66-2:2.)

Claim 4 The pad circuit of claim 3, further comprising one or more NMOS devices coupled between the second node and the third voltage rail, wherein the NMOS devices and the PMOS devices are operable to operate together to drive the output signal at the second node, wherein the control block operates to turn off the NMOS devices during the ESD event.

80. Verhaege discloses an NMOS device coupled between the second node and third voltage rail because NMOS output transistor 12 (blue) is coupled between the second node (red) and Vss.



(EX-1004, Figure 1 (annotated).)

81. During normal operation, NMOS output transistor 12 works with PMOS output transistor 14 to drive a signal at the I/O pad (green) by connecting the pad to either Vdd or Vss. During an ESD event, the control block (i.e., gate clamp 44) (orange) turns off NMOS transistor 12 by connecting its gate to ground. (EX-1004, 2:32-2:36.)

Claim 5 The pad circuit of claim 1, wherein the pad circuit and the physical pad are comprised in a digital input/output pad.

82. As discussed above, Verhaege discloses both a pad circuit (circuit 10) and an associated physical pad (I/O pad 36). The pad is explicitly an input/output pad: “an I/O pad is connected to the junction between the output driver transistors.” (EX-1004, 1:38-1:39.) Moreover, a POSITA would understand that the disclosed I/O pad is digital, meaning that it outputs either a “high” or “low” logic signal. As

discussed in claim 1[c], Verhaege's I/O pad is connected to either Vdd or Vss by the output driver transistors 12 and 14, and therefore outputs a high or low signal.

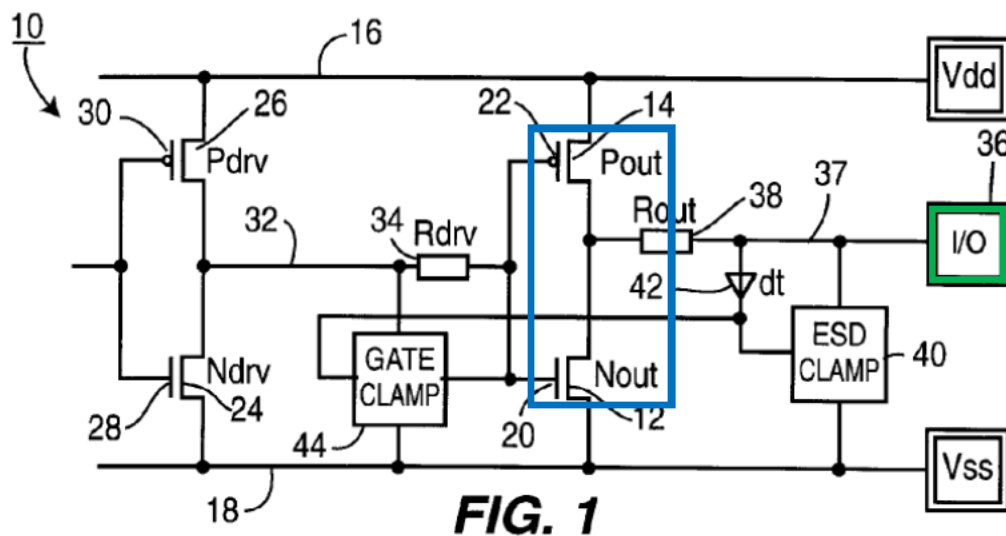
Claim 6 A circuit configured to provide protection against electrostatic discharge (ESD) in a system comprising the circuit, the circuit comprising:

83. See discussion of claim 1, Preamble.

[a] an output buffer configured to couple to a physical pad having capacitance, to drive at least one output signal at the physical pad

84. I understand that, in the context of the '665 patent, an output buffer is a signal driver circuit because "it should be noted that the terms 'buffer' and 'output buffer' are used herein in the context of electrical and/or integrated circuits to denote signal driver circuits." (EX-1001, 4:27-4:30.)

85. Verhaege discloses an *output buffer* because it teaches a CMOS output driver circuit (dark blue) that includes output driver NMOS transistor 12 and output driver PMOS transistor 14. (EX-1004, Abstract.) The output driver transistors are *configured to couple to a physical pad* because "an I/O pad is connected to the junction of the output driver transistors." (*Id.*) As a physical, conductive device, the I/O pad (green) [*has*] *capacitance*. Finally, as discussed in claim 1[c], the output driver transistors *drive at least one output signal at the physical pad* by connecting it to either the Vdd or Vss rail.



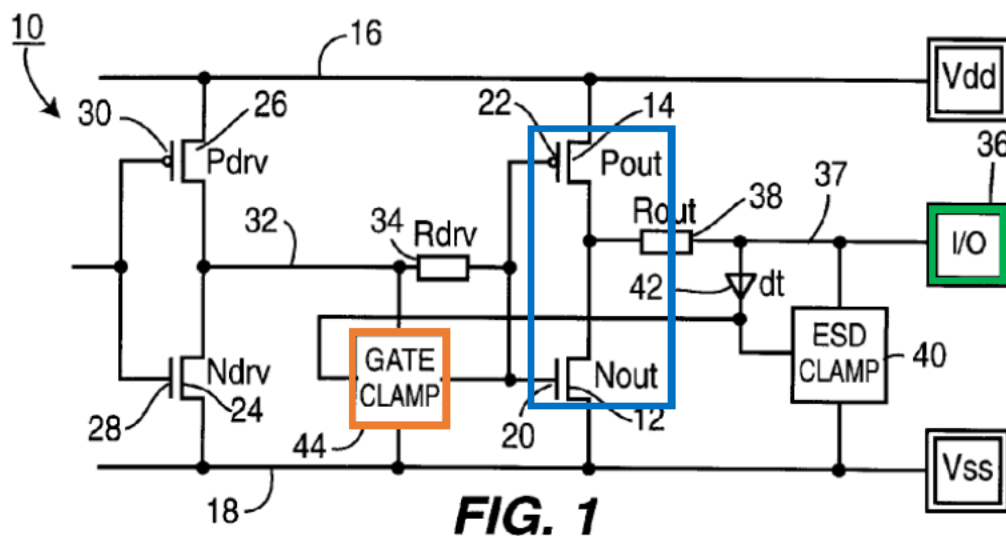
(EX-1004, Figure 1 (annotated).)

[b] a control block configured to control the output buffer;

86. I understand that, within the '665 patent, a “control block” may contain “any digital, analog, and/or mixed mode circuitry configured to perform the functions assigned to the control block.” (EX-1001, 4:43-4:46.) Here, the function of the control block is to “control the output buffer” (*Id.*, claim 6.)

87. Verhaege teaches analog circuitry for this same purpose. In the embodiment of Figure 1, for example, the control block is the gate clamp 44 (orange) and the output buffer is the CMOS output driver circuit (dark blue) that includes output driver NMOS transistor 12 and output driver PMOS transistor 14. During an ESD event gate, clamp 44 *control[s] the output buffer* because it “grounds the gate 20 of the output driver NMOS transistor 12,” thereby turning off NMOS transistor 12. (EX-1004, 2:32-2:35.) Conversely, grounding the gate 22 of PMOS transistor 14

(which is connected to gate 20 of NMOS transistor 12) turns on PMOS transistor 14.
(EX-1004, 2:23-2:25, 2:32-2:37)

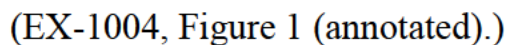


(EX-1004, Figure 1 (annotated).)

[c] a clamp device coupled between a first supply rail and a low supply rail, wherein the clamp device is configured to absorb, when turned on, a portion of an energy generated by the ESD event, to reduce the maximum voltage developed in the system as the result of the ESD event;

88. At least under Microchip's apparent interpretation of this limitation as evidenced by its infringement contentions, Verhaege discloses this limitation.

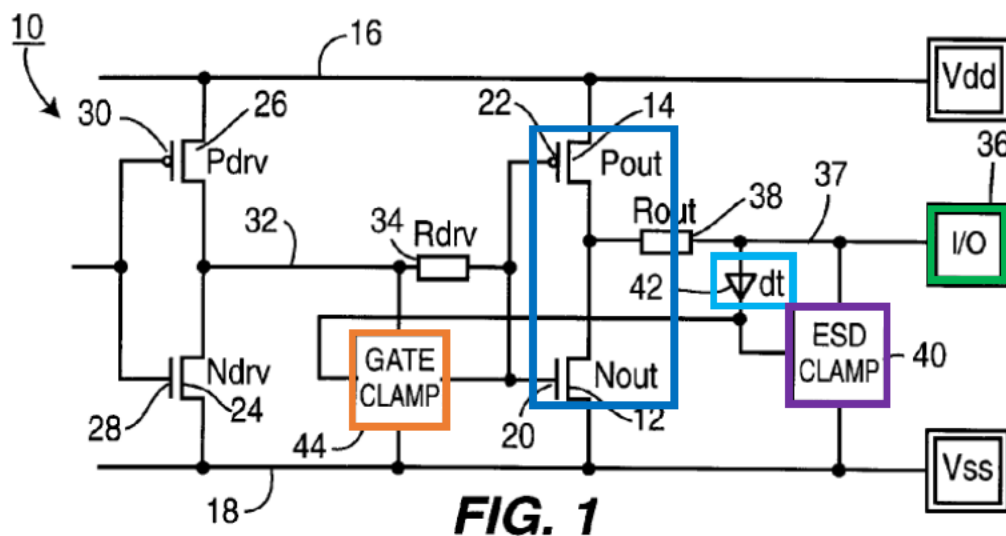
89. Based on Microchip's infringement contentions, I understand that Microchip's position is that the clamp need not be connected directly to the supply rails to be *coupled between* them. Thus, Verhaege discloses a *first voltage rail* in the form of the Vdd rail and a *low supply rail* in the form of the Vss rail. Verhaege further discloses in Figure 1 *a clamp device coupled between a first supply rail and*



[d] and a control circuit configured to instruct the control block to activate at least a portion of the output buffer when an ESD event occurs,

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Exhibit 1002 Page 38

to I/O pad 36 (green) where the ESD event originates. (EX-1004, 2:20-2:22.) The output of dynamic trigger device 42 is connected to gate clamp 44 (orange).

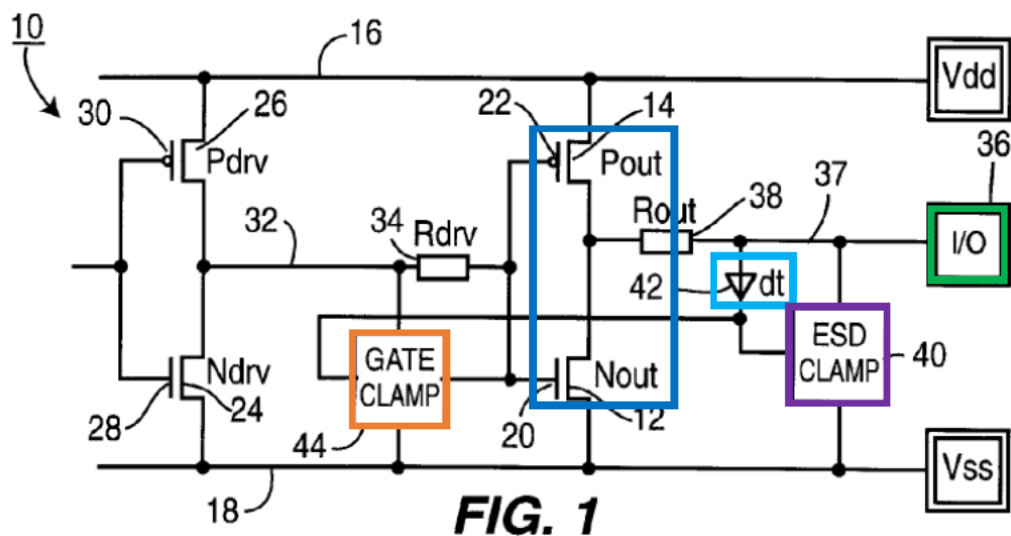


(EX-1004, Figure 1 (annotated).)

92. As discussed above in claim 6[b], gate clamp 44 is part of the control block. A POSITA would understand that dynamic trigger device 42 must instruct gate clamp 44 to turn on when an ESD event occurs because “gate clamp 44 grounds the gate 20 of the output driver NMOS transistor 12 under transient over voltage stress conditions.” (EX-1004, 2:32-2:34.) As discussed above, the gate clamp 44 also activates at least a portion of the output buffer (dark blue) by grounding the gate of PMOS transistor 14, thereby *instruct[ing]* it to turn on. (EX-1004, 2:4-2:6, Figure 1.)

[e] [the control circuit configured] to charge the pad capacitance to reduce a maximum voltage developed in the system as a result of the ESD event

93. In Verhaege, the control circuit in Figure 1 (i.e., dynamic trigger device 42 (light blue)) activates gate clamp 44 (orange) during an ESD event. In turn, the gate clamp grounds the gates of NMOS transistor 12 and PMOS transistor 14 (dark blue), thereby activating PMOS transistor 14. This connects I/O pad 36 (green) to the Vdd rail.



(EX-1004, Figure 1 (annotated).)

94. As discussed in claim 1[d], a POSITA would understand that the ESD protection circuit disclosed in Verhaege must be included at each I/O pad to provide comprehensive protection to the integrated circuit. Therefore, when PMOS transistor 14 connects I/O pad 36 to Vdd during an ESD event, the ESD energy flows to the Vdd rail. From there, the ESD energy *charge[s] the pad capacitance* of any other

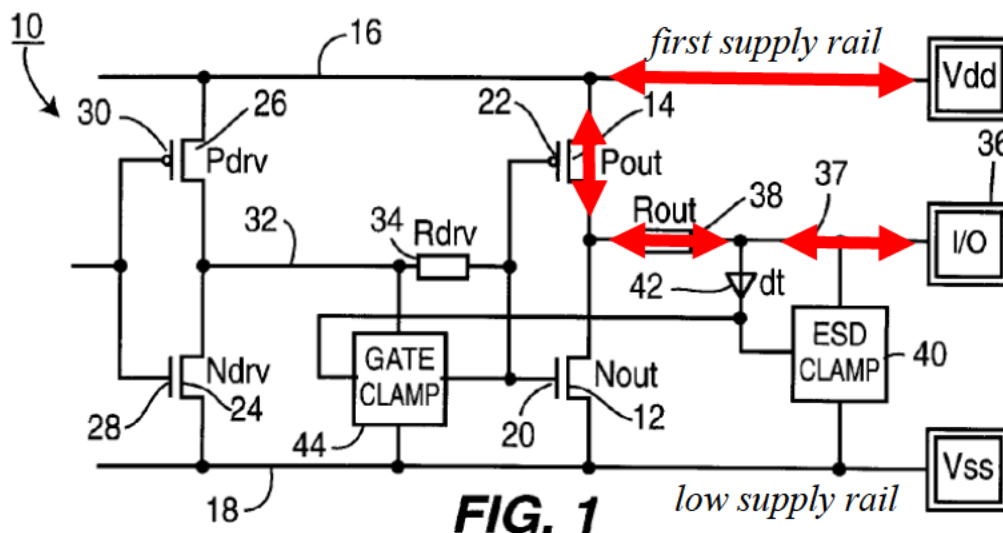
I/O pads connected to the rail, thereby reducing *the maximum voltage developed in the system* due to the ESD event.

[f] wherein the control circuit is further configured to turn on the clamp device in response to the ESD event;

95. As discussed in claim 6[d], the control circuit disclosed in Verhaege Figure 1 is dynamic trigger device 42. This control circuit is *further configured to turn on the clamp device in response to the ESD event* because “dynamic trigger device 42 is used to trigger the ESD clamp 40.” (EX-1004, 2:29-2:31.)

[g] wherein the first supply rail is configured to provide power to the control circuit

96. As discussed in claim 6[c], Verhaege discloses a *first supply rail* in the form of the Vdd rail. By convention, the Vdd rail is *configured to provide power* to the circuit, which necessarily includes *the control circuit*. In Figure 1, for example, the control circuit is dynamic trigger device 42. The dynamic trigger device 42 is powered by the first supply rail via PMOS transistor 14.



(EX-1004, Figure 1 (annotated).)

Claim 7 The circuit of claim 6,

[a] wherein the output buffer comprises one or more PMOS devices coupled between a second supply rail and the physical pad; and

97. At least under Microchip's apparent interpretation of this limitation as evidenced by its infringement contentions, Verhaege discloses this limitation.

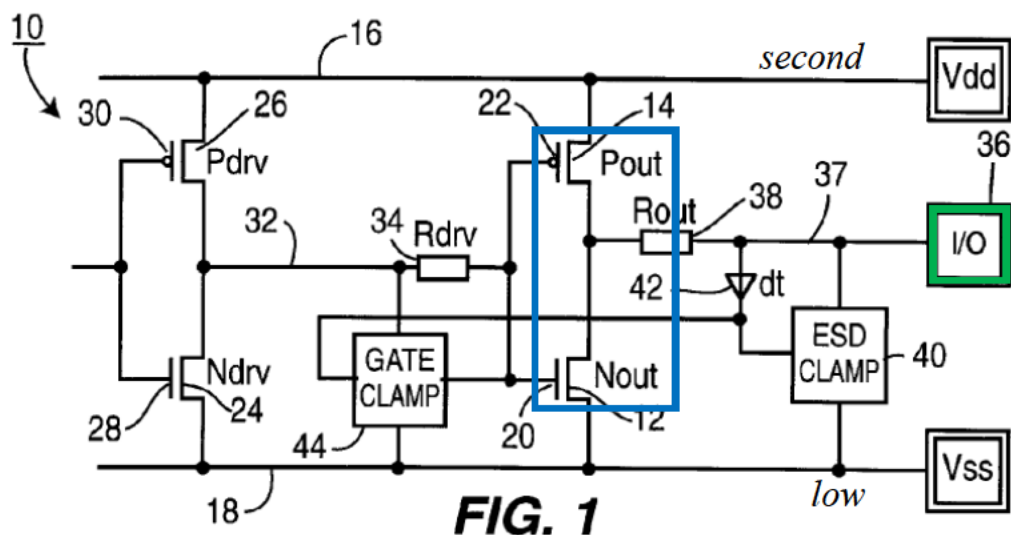
98. I understand that Microchip's position is that the *first supply rail* of claim 6[h] and *second supply rail* of claim [7a] can refer to the same voltage rail and/or be connected to each other. If so, Verhaege discloses a *second supply rail* in the form of the Vdd rail. As discussed in claim 6[a], Verhaege discloses an output buffer (dark blue) in Figure 1 comprising PMOS transistor 14 and NMOS transistor 12. This output buffer includes *one or more PMOS devices coupled between a second supply rail and the physical pad* because PMOS transistor 14 is connected to

Vdd and “is electrically connected” to I/O pad 36 (green) “by a line 37 and through an output resistor 38.” (EX-1004, 1:66-2:3, 2:16-2:19, Figure 1.)

[b] one or more NMOS devices coupled between the physical pad and the low supply rail wherein the low supply rail has a value less than the second supply rail

99. At least under Microchip’s apparent interpretation of this limitation as evidenced by its infringement contentions, Verhaege discloses this limitation.

100. As discussed in claim 6[a], Verhaege’s output buffer (dark blue) includes *one or more NMOS device* in the form of NMOS transistor 12. NMOS transistor 12 is connected to the low supply rail, Vss, and “is electrically connected” to I/O pad 36 (green) “by a line 37 and through an output resistor 38.” (EX-1004, 1:66-2:3, 2:16-2:19, Figure 1.)



(EX-1004, Figure 1 (annotated).)

101. I understand from its infringement contentions that Microchip interprets *a value less than* to refer to voltage. If so, Verhaege discloses a *low supply rail* that *has a value less than the second supply rail* because, by convention, the first supply rail (i.e., Vdd) has a positive voltage whereas the low supply rail (i.e., Vss) is ground or a negative voltage rail.

[c] wherein in activating at least a portion of the output buffer when the ESD event occurs, the control block enables one or more of the one or more PMOS devices.

102. Verhaege discloses this limitation because, as discussed in claim 6[d], the control block (i.e., gate clamp 44) *activat[es] at least a portion of the output buffer when the ESD event occurs* by enabl[ing] one or more of the one or more PMOS devices (i.e., PMOS transistor 14). (EX-1004, 2:4-6, 2:32-2:34.)

Claim 8 The circuit of claim 7, wherein in activating at least a portion of the output buffer when the ESD event occurs, the control block disables one or more of the one or more NMOS devices.

103. As discussed previously, the control block (i.e., gate clamp 44) grounds the gates of output transistors 12 and 14 during an ESD event. This activates at least a portion of the output buffer by turning on PMOS transistor 14. Conversely, NMOS transistor 12 is turned off. (EX-1004, 2:4-2:6, 2:32-2:36.)

Claim 9 The circuit of claim 7, wherein the one or more PMOS devices comprise a plurality of PMOS devices coupled in parallel between the second supply rail and the physical pad, and the one or more NMOS devices comprise a plurality of NMOS devices coupled in series between the physical pad and the second supply rail.

104. Verhaege renders this claim obvious. First, it would have been obvious to a POSITA that, instead of a single PMOS device, multiple PMOS devices could be used in parallel. Using parallel transistors is a common method for reducing the amount of current flowing through any one transistor, which in turn reduces the likelihood of damage due to over-current. Given the application—redirecting sudden ESD currents of unknown magnitude—it would have been obvious to use multiple transistors in parallel to reduce the risk of damage. A POSITA would have reasonably expected this improvement to succeed because the improvement is common and parallel transistors behave predictably.

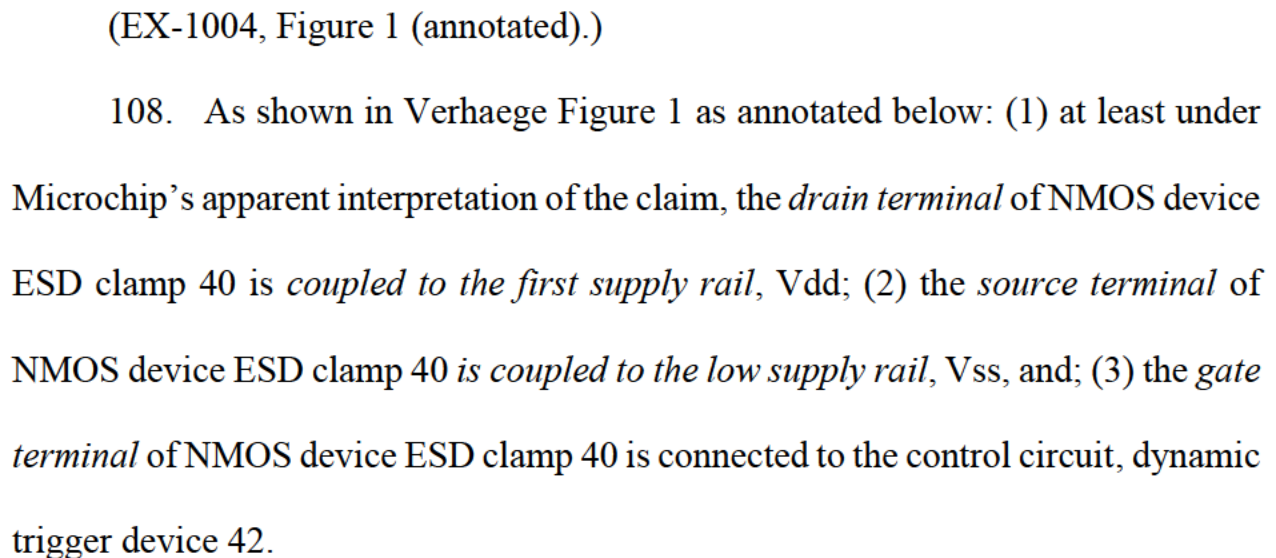
105. Placing multiple NMOS devices in series was also a common practice at the time of the '665 patent. This technique was used to protect sensitive NMOS devices from over-voltage. When enabled, there is a voltage drop across each NMOS transistor directly proportional to the current and resistance. Thus, having multiple enabled NMOS transistors in series reduces the voltage drop across subsequent transistors. Given that the pad could be subjected to extreme voltages during an ESD event, it would have been obvious to employ this technique to reduce the drain-

source voltage on the NMOS transistors and reduce the risk of damage. Here, too, a POSITA would have reasonably expected this improvement to succeed because this technique was common and predictable.

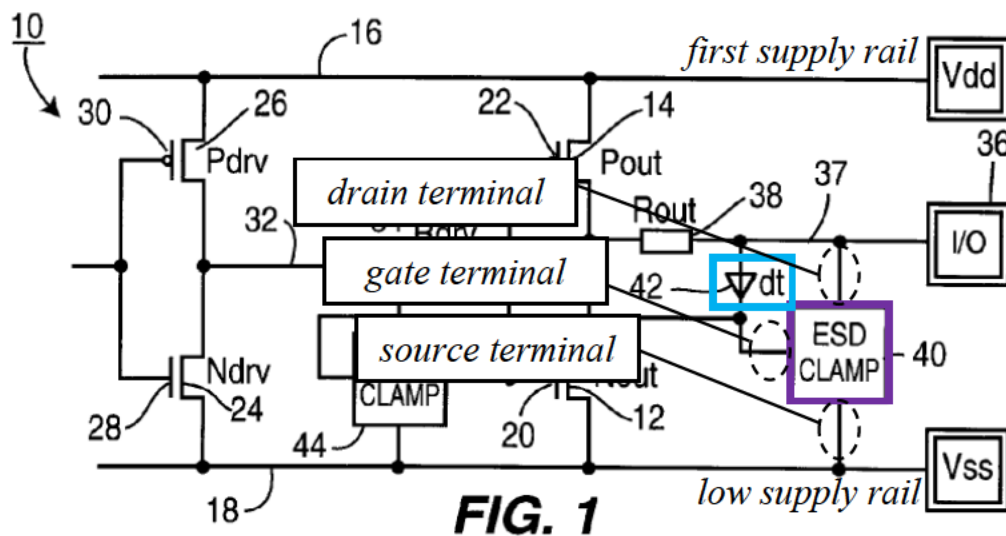
106. For the purposes of this petition, I have only been asked to consider whether claim 9 is obvious.

Claim 10 The circuit of claim 6, wherein the clamp device is one of: a PMOS device having its source terminal coupled to the first supply rail, its drain terminal coupled to the low supply rail, and its gate terminal coupled to the control circuit; or an NMOS device having its drain terminal coupled to the first supply rail, its source terminal coupled to the low supply rail, and its gate terminal coupled the control circuit.

107. Referring to Figure 1, the control circuit (i.e., dynamic trigger device 42 (light blue)) activates ESD clamp 40 (purple) during an ESD event. (EX-1004, 2:29-2:30.) At the time of the '665 patent, a conventional ESD clamp comprised a PMOS or NMOS transistor. Thus, a POSITA would conclude that ESD clamp 40 was a PMOS or NMOS device. Moreover, a POSITA would conclude that an NMOS could be used as ESD clamp device 40 because ESD clamp device 40 activates when given a high voltage signal by dynamic trigger 42. NMOS transistors are typically activated by high voltage signals (i.e., a signal greater than the source voltage plus the threshold voltage).



108. As shown in Verhaege Figure 1 as annotated below: (1) at least under Microchip's apparent interpretation of the claim, the *drain terminal* of NMOS device ESD clamp 40 is *coupled to the first supply rail, Vdd*; (2) the *source terminal* of NMOS device ESD clamp 40 is *coupled to the low supply rail, Vss*, and; (3) the *gate terminal* of NMOS device ESD clamp 40 is connected to the control circuit, dynamic trigger device 42.



(EX-1004, Figure 1 (annotated).)

Claim 11 The circuit of claim 6, wherein the first supply rail is configured to provide increased power during the ESD event.

109. As discussed in claim 6[c], Verhaege discloses a *first supply rail* in the Vdd rail. Verhaege teaches this claim because, during an ESD event, the Vdd rail is connected to I/O pad 36. Therefore, it carries the excess ESD voltage and *provide[s] increased power during the ESD event.*

Claim 12 The control circuit of claim 6, wherein in instructing the control block to activate at least a portion of the output buffer when an ESD event occurs, the control circuit is operable to provide a control signal to the control block in response to the ESD event.

110. As discussed above in claim 6[d], Verhaege Figure 1 discloses a control circuit in dynamic trigger device 42 and a control block comprising gate clamp 44. *In response to the ESD event, dynamic trigger device 42 provide[s] a control signal*

to the control block (i.e., gate clamp 44) in the form of a high voltage signal. This is readily apparent because dynamic trigger 42 sends a signal to activate ESD clamp 40 (EX-1004, 2:29-2:31) and the output of dynamic trigger 42 is also coupled to the input of gate clamp 44. (EX-1004, Figure 1.)

Claim 13 The circuit of claim 6, wherein the control circuit is configured to receive a control signal corresponding to a time constant, wherein the time constant corresponds to a specified slope, wherein the control signal is configured to trigger the control circuit if a slope of a Voltage pulse developed in the system as a result of the ESD event is greater than or equal to the specified slope.

111. First, it is my opinion that a POSITA would understand that this claim refers to the conventional means of activating an ESD protection device—the RC circuit—because an RC circuit generates a *control signal corresponding to a time constant*, triggering the system if the rate of voltage change exceeds a *specified slope*. In the art, these features are synonymous with an RC circuit. As discussed in claims 6[d] and 6[e], Verhaege Figure 1 uses dynamic trigger device 42 as its control circuit to detect an ESD event and respond accordingly, satisfying all applicable limitations. In Figures 2, 4 and 5, however, Verhaege discloses RC circuits for detecting ESD events. For example, Verhaege discloses a “trigger device” in Figure 2 wherein the trigger device “comprises a capacitor 48 in series with a resistor 50.”



(EX-1004, Figure 2.)

112. Given these disclosures, a POSITA would understand that the trigger device in Verhaege can take multiple forms. A POSITA would further understand that the trigger device of Figure 2 (i.e., an RC circuit) is interchangeable with the trigger device of Figure 1. A POSITA would reasonably expect the RC circuit to function as the trigger device in view of Verhaege's disclosures (EX-1004, Figure 2, 4, and 5) and because the RC circuit predictably acts as a low-pass filter.

113. When used in the Figure 1 configuration, the RC circuit trigger device meets all limitations of claim 13. Every RC circuit has a time constant that is proportional to the resistance and capacitance of the circuit. The time constant corresponds to how quickly the output voltage of the circuit can change. Thus, the output of an RC circuit is *a control signal corresponding to a time constant*.

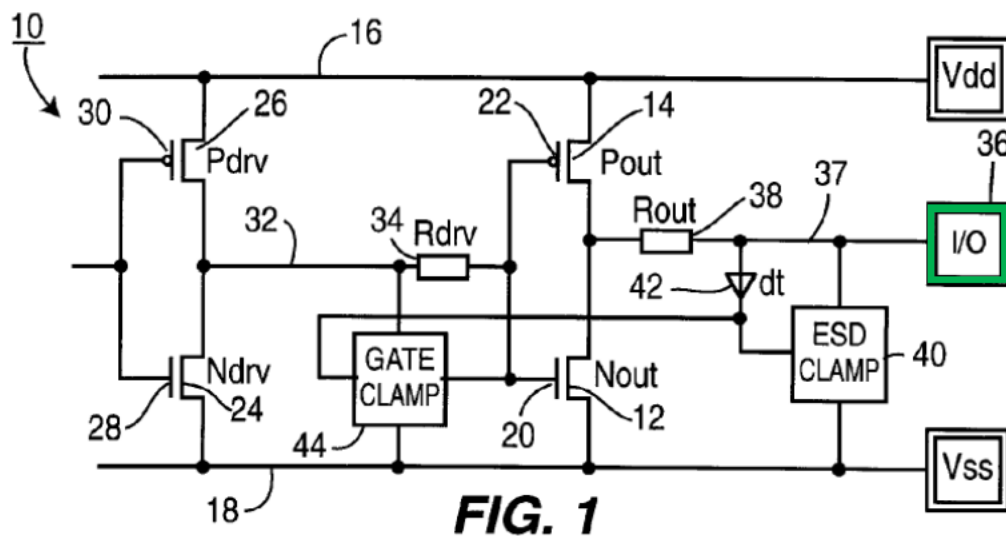
114. The RC circuit is the conventional means for detecting an ESD event because, during an ESD event, the *sudden voltage pulse developed in the system* exceeds the rate at which the output voltage of the RC circuit can change. In other words, the RC circuit determines if the slope of *[the] voltage pulse* is *greater than or equal to a specified slope* pre-set by the RC time constant. Unlike a voltage-based trigger, the RC circuit detects sudden changes in voltage: a superior indicator of ESD events. Moreover, a POSITA would reasonably expect an RC circuit to succeed as the trigger device because it is a well-known circuit with desirable features, and the art of circuit design is predictable.

Claim 14 A system comprising:

115. Verhaege teaches a “circuit for the protection of an output driver NMOS transistor during EOS/ESD stress,” and a circuit is a system. (EX-1004, Abstract.)

[a] one or more pads, each pad comprising: a respective physical pad having respective capacitance;

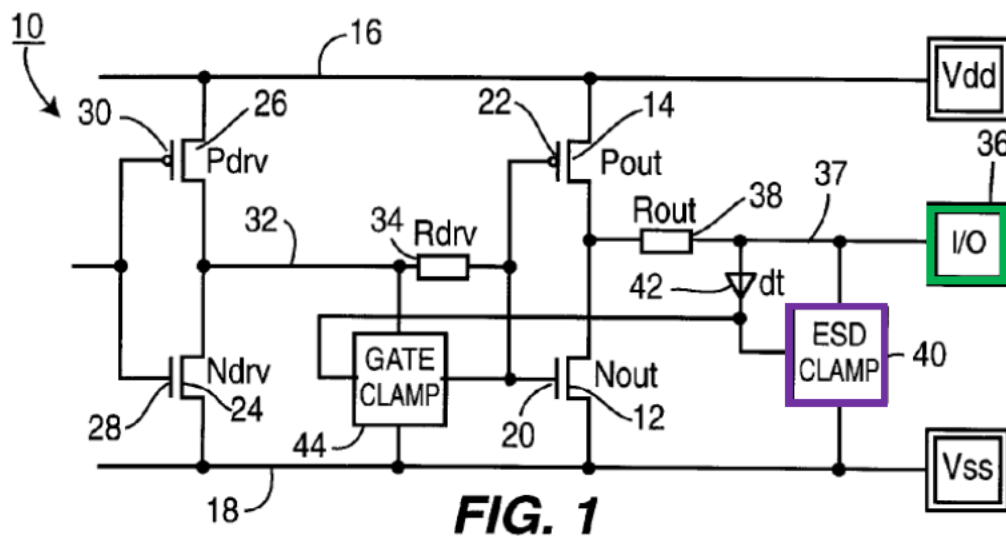
116. Verhaeghe teaches *one or more pads* because “[a]n I/O pad is connected to the junction between the output driver transistors.” (EX-1004, 1:38-1:39.) Moreover, a POSITA would understand that, in this context, the I/O pad (green in Figure 1, below) is a physical pad. As a physical, conductive device, each I/O pad *ha[s] respective capacitance*.



(EX-1004, Figure 1 (annotated).)

[b] [each pad comprising:] a respective clamp device configured to absorb, when turned on, a portion of an energy generated by an ESD event, to thereby further reduce the maximum voltage developed in the system as the result of the ESD event; and

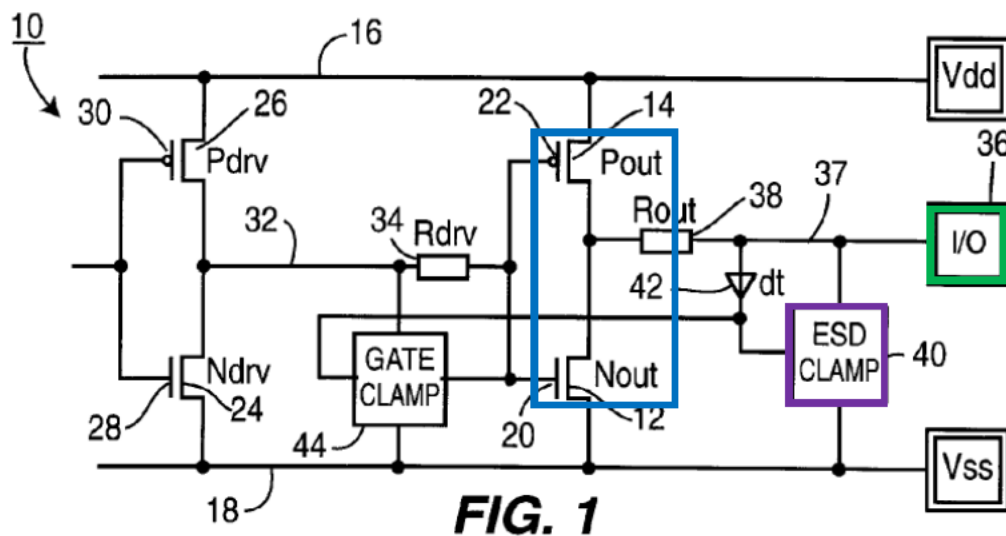
117. In the embodiment of Figure 1, for example, Verhaege discloses an I/O pad 36 (green) connected to its respective ESD clamp device 40 (purple). (EX-1004, 2:19-2:20.) When turned on, ESD clamp device 40 connects I/O pad 36 to the VSS rail. (EX-1004, 2:29-30, Figure 1.) Thus, “the ESD stress can be diverted to the parallel ESD clamp and the EOS/ESD capability is achieved.” (EX-1004, 2:37-2:39.) In other words, the clamp *absorb[s]* . . . a portion of the ESD energy by shunting it to ground to *reduce the maximum voltage developed in the system*.



(EX-1004, Figure 1 (annotated).)

[c] [each pad comprising:] a respective pad circuit comprising: a respective output buffer coupled to the respective physical pad, and operable to drive at least one respective output signal at the respective physical pad; and

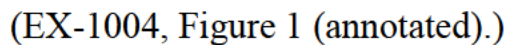
118. Verhaege teaches that the I/O pad 36 (green) comprises *a respective pad circuit* because the invention is directed to a “circuit for the protection of an output driver NMOS transistor.” (EX-1004, 1:1:33-1:34.) As discussed in claim 6[a], Verhaege also discloses an *output buffer* (dark blue) *coupled to the pad and operable to drive at least one output signal at the pad.*



(EX-1004, Figure 1 (annotated).)

[d] [the respective pad circuit comprising:] respective control circuitry operable to: activate at least a portion of the respective output buffer in response to an ESD event to charge the respective pad capacitance to reduce a maximum voltage developed in the system as a result of the ESD event; and

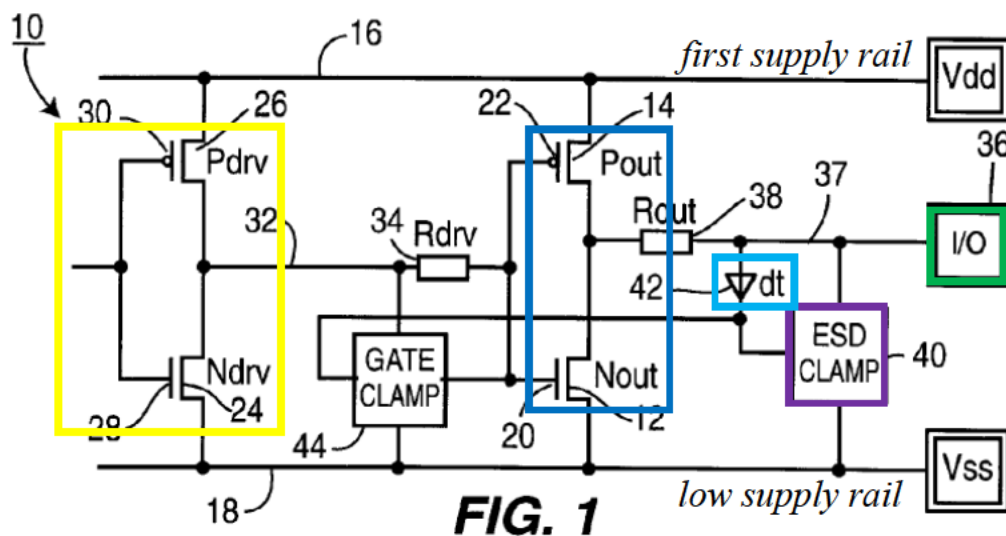
119. As discussed in claims 6[d] and 6[e], Verhaege discloses control circuitry (i.e., dynamic trigger device 42 (light blue)) operable to *activate at least a portion* (i.e., PMOS transistor 14) *of the output buffer* (dark blue) *in response to an ESD event*. In claims 6[d] and 6[e], I also explain why a POSITA would include the Verhaege circuit at every I/O pad (green). Thus, enabling PMOS transistor 14 allows the system to charge the capacitance of other pads connected to Vdd, *thereby reduc[ing] a maximum voltage developed in the system*.



120. Verhaege discloses this limitation because, as discussed in claim 6[d], Verhaege's control circuitry (i.e., dynamic trigger device 42) is operable to turn on the clamp device (i.e., ESD clamp 40) *in response to the ESD event*.

121. A POSITA would understand that pre-driver transistors 24 and 26 (yellow) require an output signal, as Verhaege indicates in Figure 1 by the wire from outside circuit 10. Various functional circuitries to create that signal, such as a

microcontroller, were well-known in the art. The output signal is then driven by the circuit 10 to create the final output signal at I/O pad 36 (green).



(EX-1004, Figure 1 (annotated).)

Claim 16 The system of claim 14, further comprising a first supply rail configured to provide increased power in accordance with the ESD event, and further configured to power the respective control circuitry of the respective pad circuit of each pad.

122. In Figure 1, Verhaege discloses a *first supply rail* in the form of the Vdd rail. (EX-1004, 1:65-2:3) The Vdd rail is *configured to provide increased power in accordance with the ESD event* because, as discussed in claim 1[d], the Vdd rail is connected to the source of the ESD energy during an ESD event by PMOS transistor 14. (EX-1004, Figure 1.) The Vdd rail is *further configured to power the respective control circuitry of the respective pad circuit of each pad* because, as discussed in

claim 14[d], the control circuitry is dynamic trigger device 42, which is connected to the Vdd rail via PMOS transistor 14. (EX-1004, Figure 1.)

Claim 17 The system of claim 16, further comprising a second supply rail configured to power the respective output buffer of the respective pad circuit of each pad.

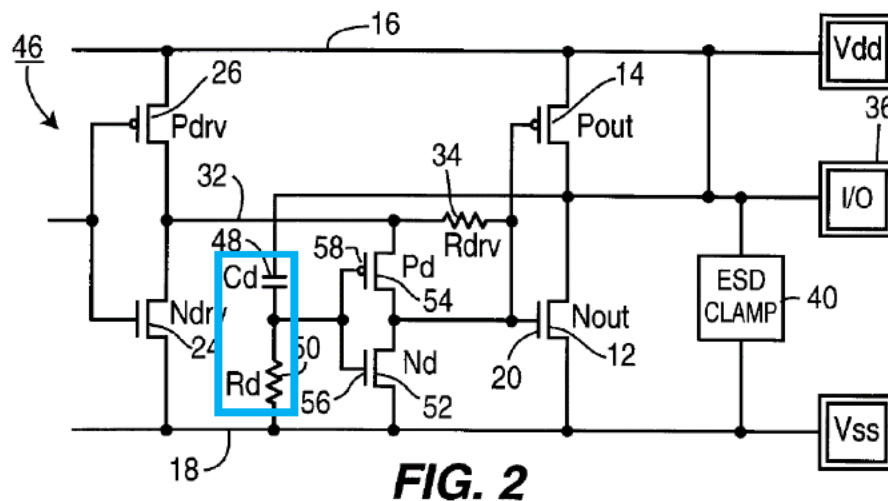
123. At least under Microchip's apparent interpretation of this limitation as evidenced by its infringement contentions, Verhaege discloses this limitation.

124. I understand that Microchip's position is that the *first supply rail* of claim 16 and *second supply rail* of claim 17 can refer to the same voltage rail and/or be connected to each other. If so, Verhaege discloses a *second supply rail* in the form of the Vdd rail. As discussed in claim 14[c], Verhaege discloses an output buffer in Figure 1 comprising PMOS transistor 14 and NMOS transistor 12. The Vdd rail is *configured to power the respective output buffer of the respective pad circuit of each pad* because it is connected to PMOS transistor 14. (EX-1004, 1:66-2:3.)

Claim 18 The system of claim 16, wherein the respective control circuitry of the respective pad circuit of each pad is configured to receive a respective control signal corresponding to a time constant, wherein the time constant corresponds to a specified slope, wherein the respective control signal is configured to trigger the respective control circuitry if a slope of a voltage pulse developed in the system as a result of the ESD event is greater than or equal to the specified slope.

125. Verhaege Figure 1 discloses *control circuitry* in the form of dynamic trigger device 42, which satisfies all applicable limitations. Alternatively, Figures 2,

4, and 5 disclose RC circuits for detecting ESD events. For example, Verhaege discloses a “trigger device” in Figure 2 wherein the trigger device “comprises a capacitor 48 in series with a resistor 50.” (EX1004, 2:45-2:47.)



(EX-1004, Figure 2.)

126. Given these disclosures, a POSITA would understand that the trigger device in Verhaege can take multiple forms. A POSITA would further understand that the trigger device (light blue) of Figure 2 (i.e., an RC circuit) is interchangeable with the trigger device of Figure 1.

127. When used in the Figure 1 configuration, the RC circuit trigger device meets all limitations of claim 18. Every RC circuit has a time constant that is proportional to the resistance and capacitance of the circuit. The time constant corresponds to how quickly the output voltage of the circuit can change. Thus, the output of an RC circuit is *a control signal corresponding to a time constant*.

128. The RC circuit is the conventional means for detecting an ESD event because, during an ESD event, the *sudden voltage pulse developed in the system* exceeds the rate at which the output voltage of the RC circuit can change. In other words, the RC circuit determines if the slope of *[the] voltage pulse* is *greater than or equal to a specified slope* pre-set by the RC time constant.

B. Ground 2 (Verhaege, Miller)

129. I have reviewed Exhibit 1006 to the Petition, which is U.S. Patent No. 7,589,945 to Miller et al. (“Miller”). Having compared the disclosures of Verhaege and Miller to the ’665 patent’s claims, it is my opinion that the claims are obvious over Verhaege in view of the background knowledge of a POSITA and/or Miller.

1. Summary of Miller

130. Miller discloses a distributed ESD protection system for I/O cells. (EX-1006, 1:7-1:10.) Miller notes that one conventional approach—including an ESD clamp at every I/O cell—can still result in current leakage during an ESD event. (*Id.*, 1:41-1:44.) Moreover, the location of the I/O pad within the integrated circuit can affect the efficacy of its ESD clamp due to resistance along the voltage rails. (*Id.*, 1:36-1:44.)

131. To address these problems, Miller teaches a circuit for distributing ESD energy across multiple I/O cells. In one embodiment, each I/O cell contains a P-channel output transistor and N-channel output transistor connected in series between a VDD rail and VSS rail. (*Id.*, 6:34-6:44.) Some cells include a clamp transistor device connected in parallel to the output transistors. (*Id.*, 6:44-6:49.) The I/O pad of each cell is connected to both the VDD rail and an optional third rail through diodes. (*Id.*, 4:18-4:19, 6:50-6:52.) The voltage of the optional third rail, or

“ESD boost bus,” is monitored by a transient detector circuit to detect an ESD event.

(*Id.*, 6:54-6:56.) The embodiment is illustrated in Miller’s Figure 3.

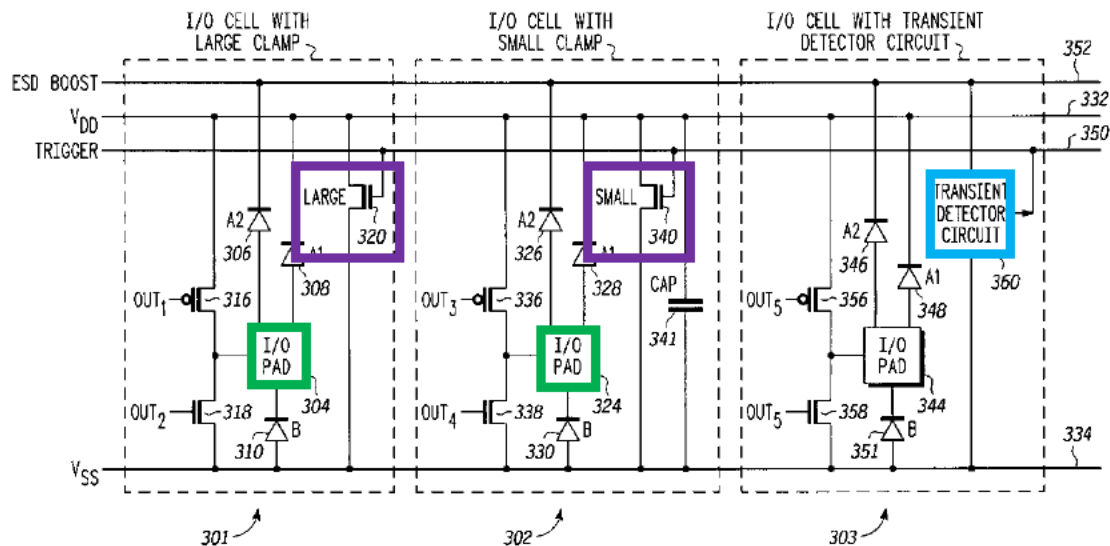


FIG. 3

(EX-1006, Figure 3 (annotated).)

132. During an ESD event at I/O pad 304 (green), current flows to the VDD rail 332 and optional ESD boost rail 352. (EX-1006., 7:14-7:17, 7:25-7:32.) In response to the sudden voltage change, the transient detector circuit 360 (light blue) sends a signal to the ESD protection clamps 320 and 340 (purple) via trigger rail 350. (*Id.*, 7:25-7:32.) Crucially, the signal activates not only the clamp transistor in the affected cell (i.e., clamp transistor 320), but all clamp transistors connected to the trigger rail 350. (*Id.*, 7:25-7:32, 7:49-7:50, 7:63-7:67.) This allows the excess

ESD energy to flow to all I/O circuits, wherein the clamp transistor devices of each cell “work together to dissipate the ESD currents.” (*Id.*, 7:63-7:67.)

2. Motivation to Combine Verhaege and Miller and Expectation of Success.

133. A POSITA would have been motivated to combine Verhaege and Miller because both concern the protection of I/O pads during ESD events. At the time, ESD was a well-known problem in integrated circuit design. In fact, the problem had become more pronounced due to densely-packed components with lower operating voltages, making them more susceptible to ESD damage. The specification of the ’665 patent acknowledged these challenges, as well as the “various techniques for improving ESD performance” that had already “been devised, published, and/or patented.” (EX-1001, 1:11-1:21.)

134. One such technique was disclosed in Verhaege, which improves on an ESD protection circuit by adding control circuitry to turn off one output transistor while using the other to connect the I/O pad to a voltage rail.

135. Another technique, disclosed in Miller, reflects the reality of integrated circuit design: most integrated circuits have multiple I/O pads. An express teaching of Miller is using the ESD protection circuit of every I/O pad, in parallel, to disperse an ESD event more effectively.

136. Therefore, a POSITA would have been motivated to use the improved protection circuit of Verhaege, apply it at every I/O pad, and share the ESD energy across multiple pad circuits as taught by Miller. This would require only a simple modification to the Verhaege circuit—connecting the trigger devices via a trigger line as shown in Miller—to activate multiple pad circuits during an ESD event. A POSITA would have been familiar with numerous other techniques to achieve the same effect; the trigger line is just one example.

137. A POSITA would reasonably expect this combination to succeed for at least three reasons. First, the components of both references—such as pads, transistors, clamp devices, and voltage rails—were well understood and behave in predictable ways when combined. Second, a POSITA would expect the modification to succeed because incorporating the ESD strategy of Miller requires only a small change to Verhaege. Third, the combination would foreseeably yield desirable results because an ESD protection circuit like Verhaege’s would benefit from sharing the ESD energy across multiple pad circuits as taught by Miller.

3. Claim-by-Claim Analysis

Claim 1 A pad circuit configured to provide protection against electrostatic discharge (ESD) in a system comprising the pad circuit,

138. See section A, claim 1, preamble.

[a] the pad circuit comprising: a first node coupled to a first voltage rail;

139. See section A, claim 1[a].

[b] [the pad circuit comprising] a second node coupled to a physical pad having capacitance;

140. See section A, claim 1[b].

[c] [the pad circuit comprising:] one or more output transistor devices coupled between the first node and the second node, and operable to at least partially drive an output signal at the second node;

141. See section A, claim 1[c].

[d] a control block configured, to turn on, when instructed, at least one of the one or more output transistor devices to charge the pad capacitance to reduce a maximum voltage developed in the system as a result of the ESD event;

142. As discussed in section A, claim 1[d], Verhaege discloses *a control block configured to turn on, when instructed, at least one of the one or more output transistor devices* in the form of gate clamp 44. Gate clamp 44 is connected to the gates of output transistors 12 and 14. (EX-1004, 2:23-2:25.) During an ESD event, gate clamp 44 connects the gates of both output transistors to ground. (EX-1004, 2:23-2:25, 2:32-2:34.) This turns off NMOS transistor 12 and turns on PMOS transistor 14. (EX-1004, 2:32-2:37.) Thus, gate clamp 44 is configured *to turn on, when instructed, at least one of the output transistor devices* (i.e., PMOS transistor 14.)

143. The limitation also requires *charg[ing] the pad capacitance to reduce a maximum voltage developed in the system as a result of the ESD event*. I understand from its infringement contentions that Microchip may interpret this limitation to require charging a pad other than the source of the ESD event. In addition to my opinions in section A, the combination of Verhaege over Miller also satisfies this limitation.

144. Miller discloses a distributed system for dissipating excess ESD energy wherein the protection circuit is repeated at each I/O pad then connected in parallel. (EX-1006, 7:63-7:67, Figure 3.) Figure 3, for example, shows an ESD protection circuit repeated at I/O cells 301 and 302, and connected in parallel via the Vdd rail and Vss rail.

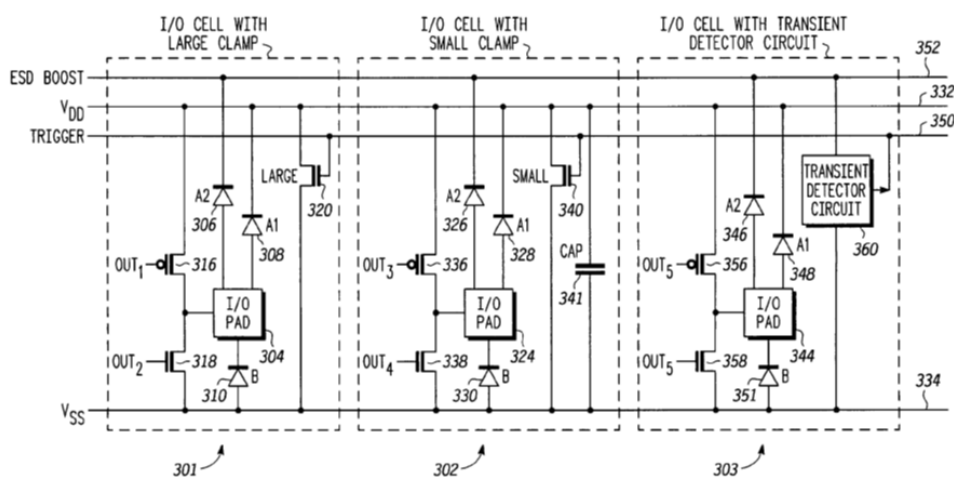
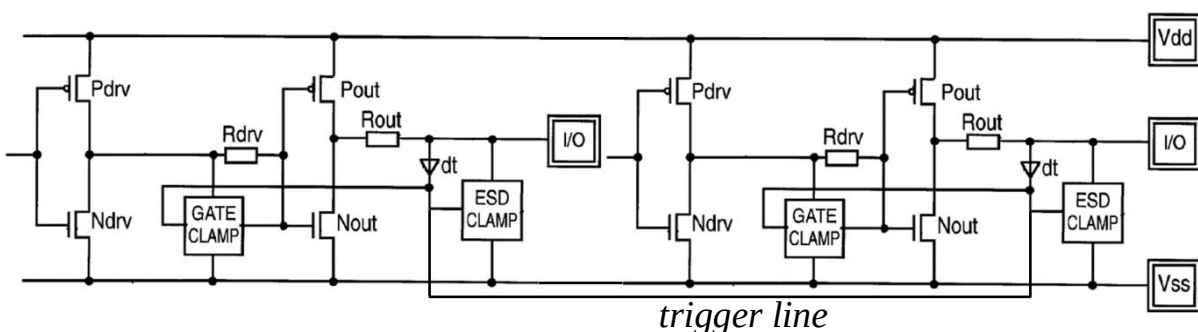


FIG. 3

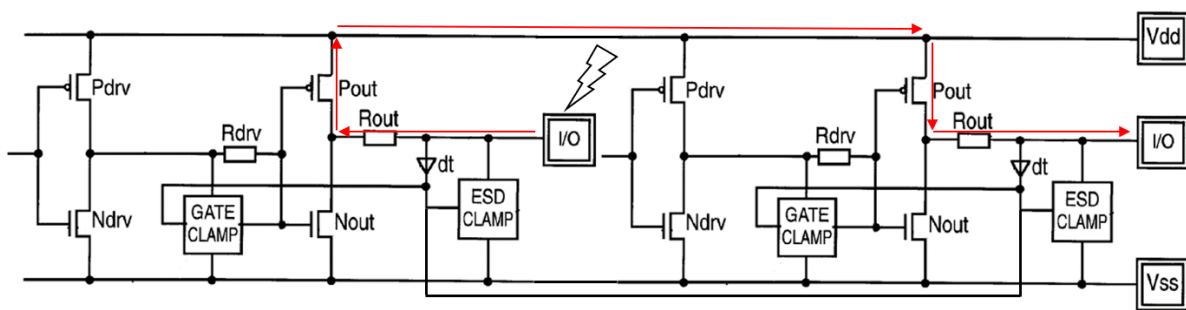
(EX-1006, Figure 3.)

145. Miller describes the advantages of this approach. “Distributing clamp transistor devices in the I/O cells of an I/O bank can provide efficient ESD protection since the clamp transistor devices, which are wired in parallel between a VDD bus and a Vss bus, can work together to dissipate the ESD currents.” (EX-1006, 7:63-7:67.)

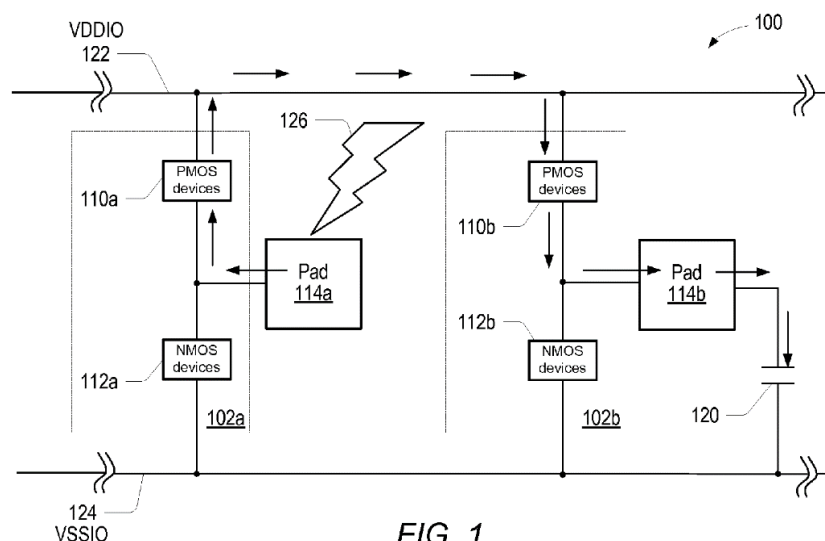
146. As discussed above, a POSITA would have been motivated to combine this approach with Verhaege, replacing the simple, ESD clamp devices 320 and 340 with the Verhaege circuit. In other words, a POSITA would include the Verhaege protection circuit at every I/O pad and connect them in parallel via the voltage rails. A POSITA would also understand that, to achieve the distributed ESD protection taught by Miller, the trigger devices of the protection circuit could be connected as shown in Miller Figure 3. One embodiment of the resulting circuit, shown below, can be drawn by simply connecting two of the protection circuits shown in Verhaege’s Figure 1.



147. During an ESD event, the control blocks (i.e., gate clamps 44) ground the gates of the PMOS output transistors 14, connecting both I/O pads to the Vdd rail. This allows excess ESD energy at one I/O pad to flow to the other I/O pad, *charg[ing] the pad capacitance to reduce a maximum voltage developed in the system.* For illustrative purposes, the ESD path is shown in the figure below, wherein the source of the ESD event is signified by a lightning bolt symbol.



148. For reference, Figure 1 of the '665 patent is included below.



(EX-1001, Figure 1.)

[e] a clamp device configured between a second voltage rail and a third voltage rail to reduce, when turned on, the maximum voltage developed in the system as the result of the ESD event;

149. As discussed in claim 1[e] of section A, Verhaege discloses this limitation if the first voltage rail of claim 1[a] and the second voltage rail of claim 1[e] can refer to the same rail and/or be connected together. To any extent that the first and second rails must be separate, this limitation would have been obvious to a POSITA because Miller, just like the '665 patent, teaches a separate, optional “ESD boost” rail. (EX-1006 4:15-4:19, Figure 3.) A dedicated ESD rail would improve Verhaege by segregating the ESD energy, thereby protecting sensitive components and increasing predictability of operation during ESD events. A POSITA would understand that, in a designated ESD rail configuration, the ESD *clamp device* would be configured between the *third voltage rail* (i.e., Vss) and the dedicated ESD rail to dissipate ESD energy. A POSITA would reasonably expect this combination to succeed because implementing a designated voltage rail predictably provides the benefits described above.

[f] enable circuitry configured to turn on the clamp device and instruct the control block to turn on the at least one of the one or more output transistor devices, in response to the ESD event;

150. See section A, claim 1[f].

[g] wherein the second voltage rail is configured to provide power to the enable circuitry, and wherein the third voltage rail has a value below the first voltage rail.

151. In addition to my opinions under claim 1[g] of section A, this limitation would have been obvious to a POSITA in view of Verhaege and Miller because Miller discloses *enable circuitry* in the form of transient detector circuit 360 used to turn on the clamp device during an ESD event. (EX-1006, 6:54-6:55.) Miller teaches that the ESD boost rail can be *configured to power* the transient detector circuit. (EX-1006, 6:56-6:57.) Like the addition of a designated voltage rail, this limitation is compatible with Verhaege.

Claim 2 The pad circuit of claim 1, wherein in turning on the at least one of the one or more output transistor devices when instructed, the control block couples an associated capacitance of the first voltage rail to the physical pad to share a charge developed in the system in response to the ESD event, to reduce the maximum voltage developed in the system as the result of the ESD event.

152. As discussed in section A, claim 1[d], Verhaege discloses a *control block* that couples the *first voltage rail to the physical pad*. To any extent that this claim requires that the voltage rail has associated capacitance other than its inherent capacitance, then it is obvious over Verhaege in view of Miller.

153. The combination of Verhaege in view of Miller satisfies this limitation because, during an ESD event, all I/O pads are coupled to the Vdd rail. As such, the *associated capacitance* of the Vdd rail is equal to capacitance of the rail itself plus

the sum of the other capacitive devices (i.e., I/O pads) connected to the Vdd rail. This further *reduce[s] the maximum voltage developed in the system by shar[ing] a charge* across a greater capacitance.

Claim 3 The pad circuit of claim 1, wherein the one or more output transistor devices are PMOS devices.

154. See section A, claim 3.

Claim 4 The pad circuit of claim 3, further comprising one or more NMOS devices coupled between the second node and the third voltage rail, wherein the NMOS devices and the PMOS devices are operable to operate together to drive the output signal at the second node, wherein the control block operates to turn off the NMOS devices during the ESD event.

155. See section A, claim 4.

Claim 5 The pad circuit of claim 1, wherein the pad circuit and the physical pad are comprised in a digital input/output pad.

156. See section A, claim 5.

Claim 6 A circuit configured to provide protection against electrostatic discharge (ESD) in a system comprising the circuit, the circuit comprising:

157. See section A, claim 6, preamble.

[a] an output buffer configured to couple to a physical pad having capacitance, to drive at least one output signal at the physical pad

158. See section A, claim 6[a].

[b] a control block configured to control the output buffer;

159. See section A, claim 6[b].

[c] a clamp device coupled between a first supply rail and a low supply rail, wherein the clamp device is configured to absorb, when turned on, a portion of an energy generated by the ESD event, to reduce the maximum voltage developed in the system as the result of the ESD event; and

160. As discussed in section A, claim 1[c], Verhaege discloses this limitation. But to any extent that this first supply rail and the second supply rail of dependent claim 7 (see below) must be separate rails, this limitation would have been obvious to a POSITA over Verhaege in view of Miller. Miller, just like the '665 patent, teaches a separate, optional "ESD boost" rail. (EX-1006, 4:15-4:19, Figure 3.) It would have been obvious to a POSITA that it would be necessary to attach the ESD clamp to this separate rail to dissipate the ESD energy.

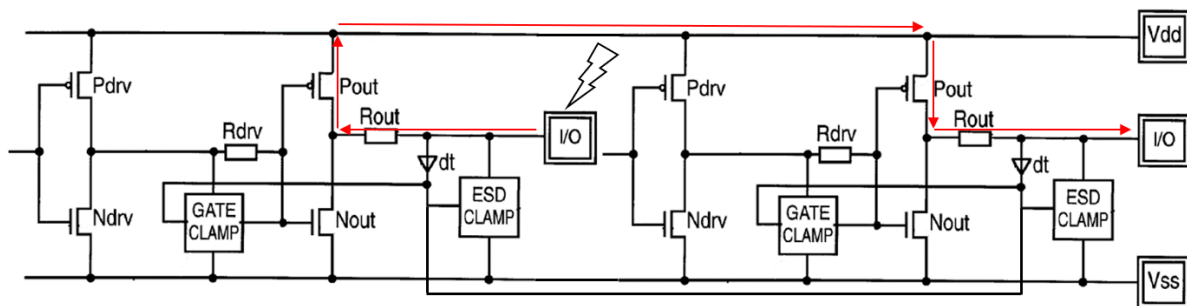
[d] a control circuit configured to instruct the control block to activate at least a portion of the output buffer when an ESD event occurs,

161. See section A, claim 6[d].

[e] [the control circuit configured] to charge the pad capacitance to reduce a maximum voltage developed in the system as a result of the ESD event

162. In addition to my opinions under section A, claim 6[e], this limitation also would have been obvious to a POSITA over Verhaege in view of Miller.

163. As discussed in claim 1[d], the combination of Verhaege and Miller would connect all I/O pads to the Vdd rail during an ESD event. Thus, the ESD charge at one I/O pad would flow to the other I/O pads in the system, *charg[ing] the pad capacitance and reduc[ing] a maximum voltage developed in the system as a result of the ESD event*, as shown below in one embodiment of the combination wherein the source of the ESD event is signified by a lightning bolt.



[f] wherein the control circuit is further configured to turn on the clamp device in response to the ESD event;

164. See section A, claim 6[f].

[g] wherein the first supply rail is configured to provide power to the control circuit

165. See section A, claim 6[g].

Claim 7 The circuit of claim 6,

[a] wherein the output buffer comprises one or more PMOS devices coupled between a second supply rail and the physical pad; and

166. As discussed in claim 1[e] of section A, Verhaege discloses this limitation if the first supply rail of claim 6[c] and the second supply rail of claim 6[e] can refer to the same rail and/or be connected together. To any extent that the first and second supply rails must be separate, the “first supply rail” of claim 6[c] would refer to the separate, “ESD boost” rail. (EX-1006 4:15-4:19, Figure 3.) Thus, this limitation would refer to Vdd and, as discussed above, the output buffer includes PMOS transistor 14 coupled between Vdd and I/O pad 36.

[b] one or more NMOS devices coupled between the physical pad and the low supply rail wherein the low supply rail has a value less than the second supply rail

167. See section A, claim 7[b].

[c] wherein in activating at least a portion of the output buffer when the ESD event occurs, the control block enables one or more of the one or more PMOS devices.

168. See section A, claim 7[c].

Claim 8 The circuit of claim 7, wherein in activating at least a portion of the output buffer when the ESD event occurs, the control block disables one or more of the one or more NMOS devices.

169. See section A, claim 8.

Claim 9 The circuit of claim 7, wherein the one or more PMOS devices comprise a plurality of PMOS devices coupled in parallel between the second supply rail and the physical pad, and the one or more NMOS devices comprise a plurality of NMOS devices coupled in series between the physical pad and the second supply rail.

170. See section A, claim 9.

Claim 10 The circuit of claim 6, wherein the clamp device is one of: a PMOS device having its source terminal coupled to the first supply rail, its drain terminal coupled to the low supply rail, and its gate terminal coupled to the control circuit; or an NMOS device having its drain terminal coupled to the first supply rail, its source terminal coupled to the low supply rail, and its gate terminal coupled the control circuit.

171. In addition to my opinions under section A, claim 10, this limitation would have been obvious to a POSITA over Verhaege in view of Miller because Miller explicitly discloses that the clamp devices are MOSFET transistors. (EX-1006, 3:8-3:16, Figure 3.)

Claim 11 The circuit of claim 6, wherein the first supply rail is configured to provide increased power during the ESD event.

172. See section A, claim 11.

Claim 12 The control circuit of claim 6, wherein in instructing the control block to activate at least a portion of the output buffer when an ESD event occurs, the control circuit is operable to provide a control signal to the control block in response to the ESD event.

173. See section A, claim 12.

Claim 13 The circuit of claim 6, wherein the control circuit is configured to receive a control signal corresponding to a time constant, wherein the time constant corresponds to a specified slope, wherein the control signal is configured to trigger the control circuit if a slope of a Voltage pulse developed in the system as a result of the ESD event is greater than or equal to the specified slope.

174. See section A, claim 13.

Claim 14 A system comprising:

175. See section A, claim 14, preamble.

[a] one or more pads, each pad comprising: a respective physical pad having respective capacitance

176. See section A, claim 14[a].

[b] [each pad comprising:] a respective clamp device configured to absorb, when turned on, a portion of an energy generated by an ESD event, to thereby further reduce the maximum voltage developed in the system as the result of the ESD event; and

177. See section A, claim 14[b].

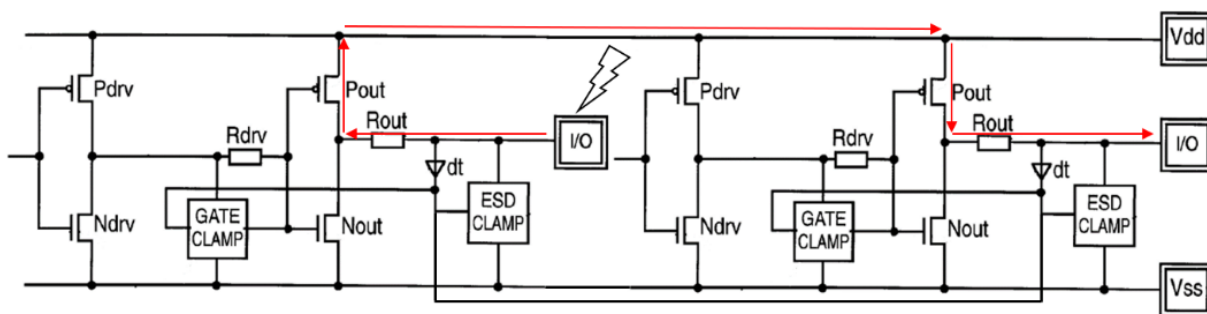
[c] [each pad comprising:] a respective pad circuit comprising: a respective output buffer coupled to the respective physical pad, and operable to drive at least one respective output signal at the respective physical pad; and

178. See section A, claim 14[c].

[d] [the respective pad circuit comprising:] respective control circuitry operable to: activate at least a portion of the respective output buffer in response to an ESD event to charge the respective pad capacitance to reduce a maximum voltage developed in the system as a result of the ESD event; and

179. In addition to my opinions under section A, claim 14[d], this limitation is rendered obvious by Verhaege in view of Miller.

180. As discussed in claim 1[d] and 6[e], in the combination of Verhaege and Miller the output buffer of each protection circuit (i.e., the PMOS output transistor) couples the I/O pad to the Vdd rail, allowing charge to flow from the source of the ESD event to other I/O pads. The ESD path is illustrated in the figure below, wherein the lightning bolt symbolizes the ESD event.



Thus, the capacitance of the I/O pads is charged, and the maximum voltage developed in the system is reduced.

[e] [the respective control circuitry operable to:] turn on the clamp device in response to the ESD event.

181. See section A, claim 14[e].

Claim 15 The system of claim 14, further comprising functional circuitry coupled to the respective pad circuit of at least one of the one or more pads, wherein the functional circuitry is operable to generate the at least one respective output signal driven by the respective pad circuit of the at least one of the one or more pads.

182. See section A, claim 15.

Claim 16 The system of claim 14, further comprising a first supply rail configured to provide increased power in accordance with the ESD event, and further configured to power the respective control circuitry of the respective pad circuit of each pad.

183. See section A, claim 16.

Claim 17 The system of claim 16, further comprising a second supply rail configured to power the respective output buffer of the respective pad circuit of each pad.

184. See section A, claim 17.

Claim 18 The system of claim 16, wherein the respective control circuitry of the respective pad circuit of each pad is configured to receive a respective control signal corresponding to a time constant, wherein the time constant corresponds to a specified slope, wherein the respective control signal is configured to trigger the respective control circuitry if a slope of a voltage pulse developed in the system as a result of the ESD event is greater than or equal to the specified slope.

185. See section A, claim 18.

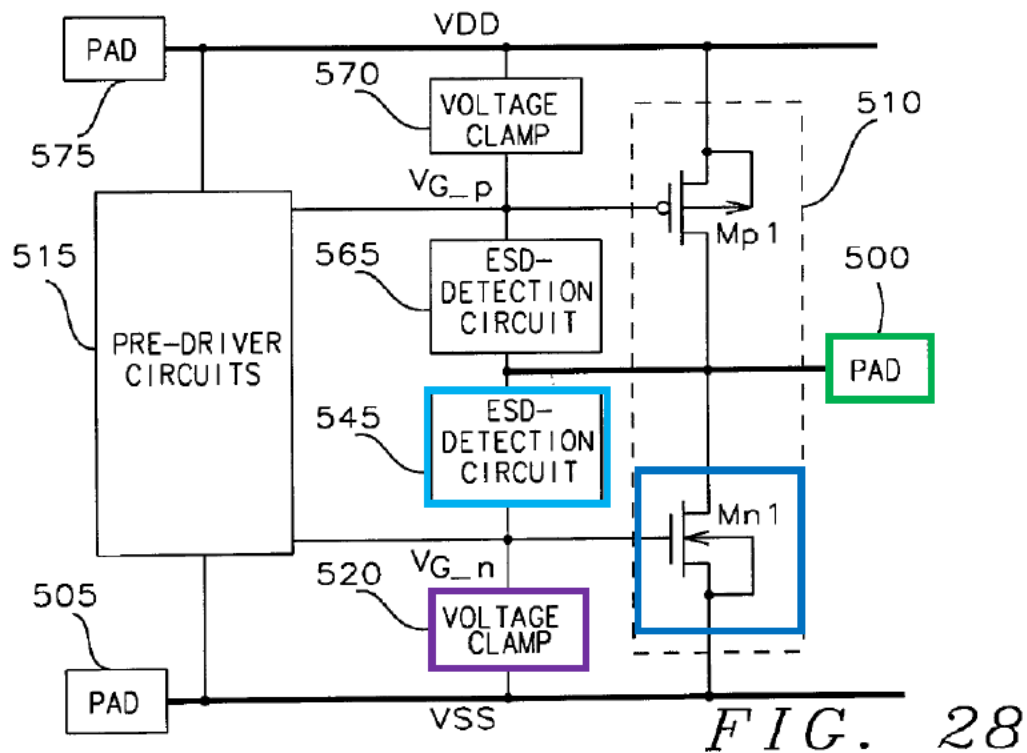
C. Ground 3 (Ker)

186. I have reviewed Exhibit 1005 to the Petition, which is U.S. Patent No. 6,249,410 to Ker et al. (“Ker”). Having compared Ker’s disclosures to the ’665 patent’s claims, it is my opinion that the claims are obvious over Ker in view of the background knowledge of a POSITA.

1. Summary of Ker

187. Ker teaches a circuit to protect sensitive components from ESD. (EX-1005, 1:7-1:9.) As Ker explains, the input and output pins of an integrated circuit can be exposed to 2000 volts during an ESD event. (*Id.*, 1:20-1:23.) Such extreme voltages can damage internal components like MOS devices. (*Id.*, 1:15-1:20.)

188. In one embodiment, Ker addresses this issue by connecting an ESD detection circuit to the gate of an output transistor. (*Id.*, 18:17-18:23.) A voltage clamp is placed between the ESD detection circuit and a voltage rail. (*Id.*, 18:43-18:51.) Ker mirrors this configuration for both output transistors, and each is relevant to the obviousness analysis as discussed below. Ker Figure 28 shows a block diagram of the protection circuit, with subsequent figures providing greater detail.



(EX-1005, Figure 28)

189. During a positive-voltage ESD event at I/O pad 500 (green), ESD detection circuit 545 (light blue) outputs a signal to signal port VG_n (orange). (*Id.*, 18:24-18:36.) Signal port VG_n then activates output transistor Mn1 (dark blue) which dissipates energy from the ESD event by connecting I/O pad 500 to the VSS rail. (*Id.*, 18:24-18:36.) Nevertheless, high voltage may accumulate at I/O pad 500 and ESD detection circuit 545 (light blue) during an ESD event. (*Id.*, 18:37-18:42.) If so, voltage clamp 520 (purple) activates to shunt excess voltage from pad 500 through ESD detection circuit 545 to the VSS rail. (*Id.*, 18:51-18:59.) From there,

the ESD energy charges the capacitance of the rail and/or the capacitance of any devices connected to the rail.

2. Claim-by-Claim Analysis

Claim 1 A pad circuit configured to provide protection against electrostatic discharge (ESD) in a system comprising the pad circuit,

190. Ker discloses a *pad circuit configured to provide protection against electrostatic discharge* because at least one embodiment of the invention “describes an integrated circuit output driver circuit for transferring digital signals from internal circuits to an output pad connected to a transmission medium and for dissipating electrostatic charge from an ESD Source connected to the output pad.” (EX-1005, 9:44-9:48.)

[a] the pad circuit comprising: a first node coupled to a first voltage rail;

191. Ker discloses a first node coupled to a first voltage rail. In Figure 29, for example, Ker discloses a *first node coupled to a first voltage rail* where output PMOS Mp1 meets the Vdd rail, as shown below in red.

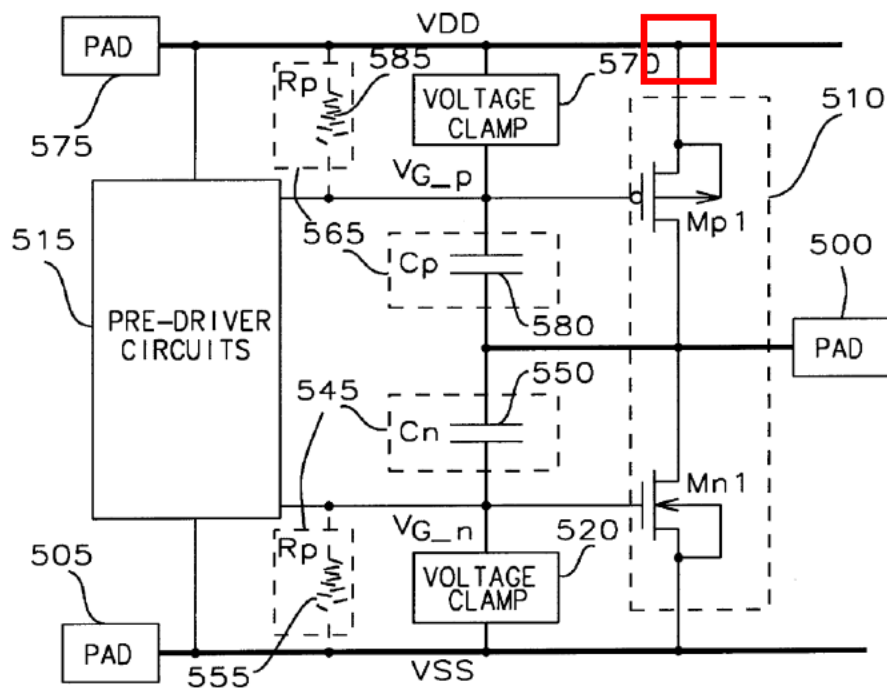


FIG. 29

(EX-1005, Figure 29 (annotated).)

[b] [the pad circuit comprising:] a second node coupled to a physical pad having capacitance;

192. Ker discloses this limitation.

193. First, Ker discloses a *second node* where PMOS Mp1 meets the output terminal pad 500, as shown below. (EX-1005, 19:20-19:24, Figure 29.)

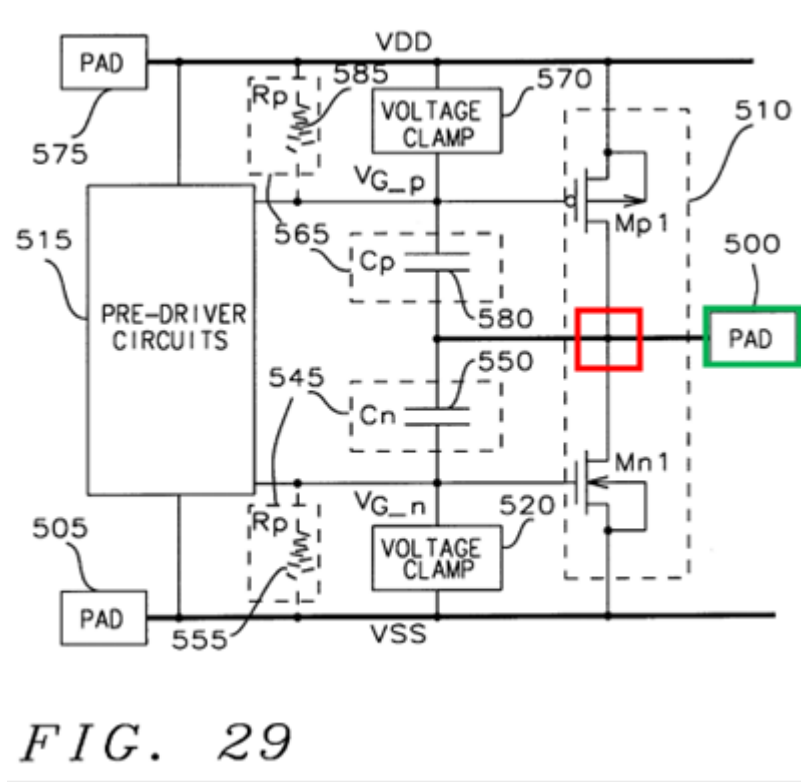


FIG. 29

(EX-1005, Figure 29 (annotated).)

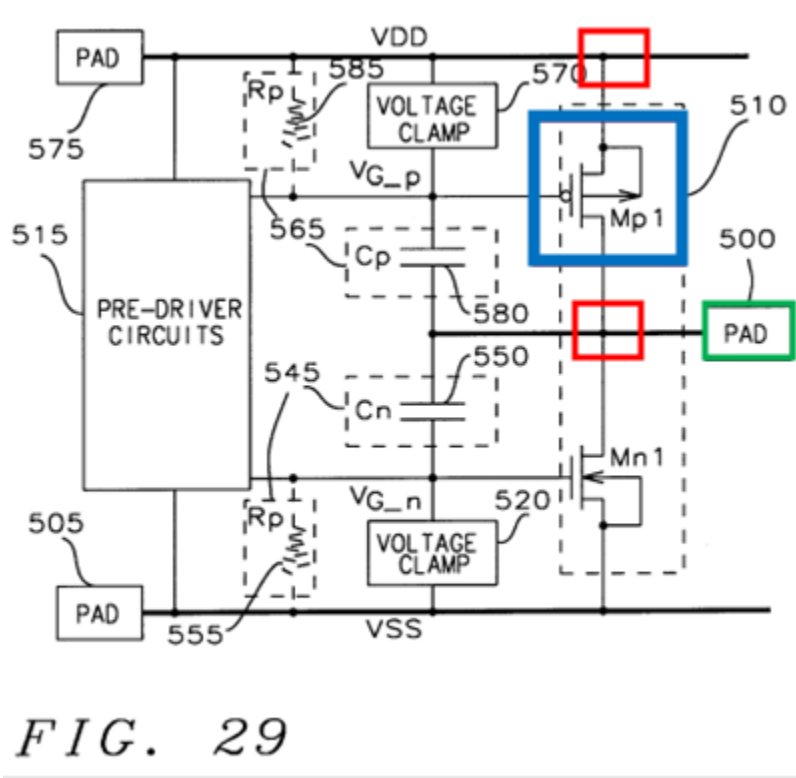
194. Second, the node is coupled to a *physical pad having capacitance* because output signal terminal 500 (green) is a physical pad. And as a physical, conductive device, pad 500 has capacitance.

[c] [the pad circuit comprising:] one or more output transistor devices coupled between the first node and the second node, and operable to at least partially drive an output signal at the second node;

195. Ker discloses this limitation.

196. Ker teaches *one or more output transistor devices coupled between the first node and second node* because a PMOS output transistor is connected between

the Vdd rail and the I/O pad. (EX-1005, 19:21-19:26.) In Figure 29, for example, PMOS device Mp1 (dark blue) is shown connected between the nodes.



(EX-1005, Figure 29 (annotated).)

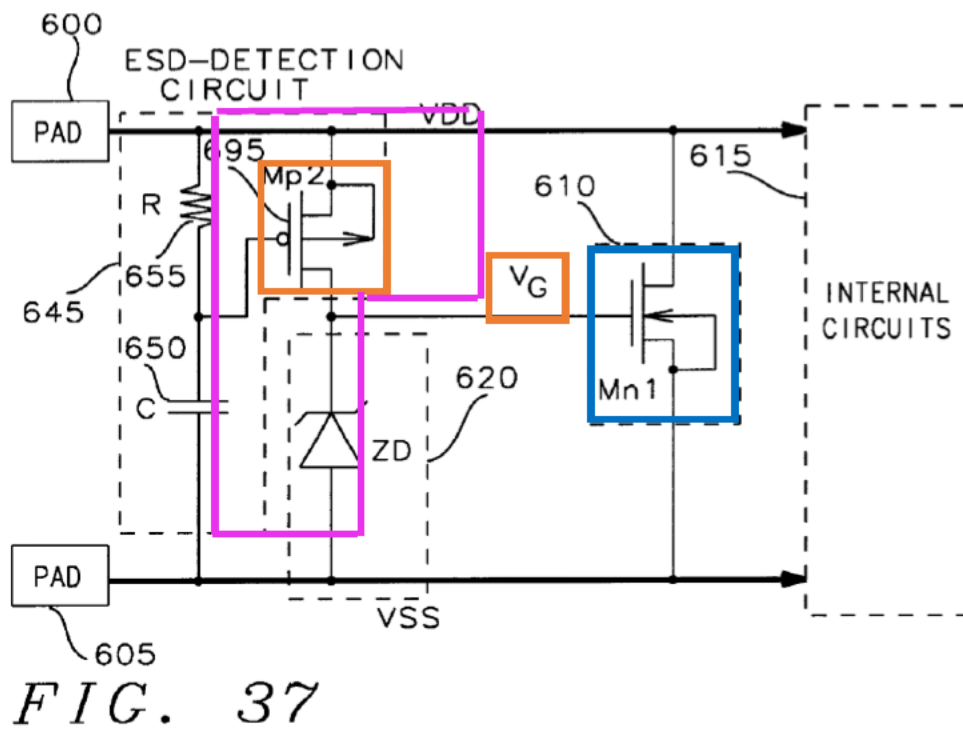
197. Mp1 is an output transistor because it is part of “driver circuit 510.” (EX-1005, 18:62-18:64.) This also means that Mp1 is *operable to at least partially drive an output signal at the second node* because it is the component of the driver circuit that connects pad 500 to Vdd to produce a “high” output signal. In other words, activating Mp1 during normal conditions connects the I/O pad to Vdd, creating a “high” logic signal.

[d] a control block configured, to turn on, when instructed, at least one of the one or more output transistor devices to charge the pad capacitance to reduce a maximum voltage developed in the system as a result of the ESD event;

198. At least under Microchip's apparent interpretation of the limitation as evidenced by its infringement contentions, Ker satisfies this limitation.

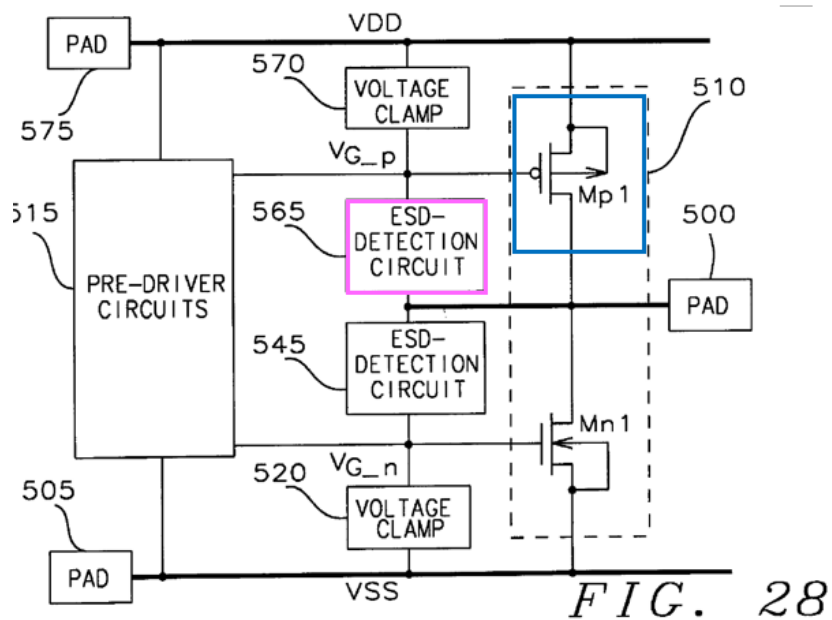
199. I understand that, within the '665 patent, a "control block" may contain "any digital, analog, and/or mixed mode circuitry configured to perform the functions assigned to the control block." (EX-1001, 4:43-4:46.) Here, the function of the control block is to "turn on, when instructed, at least one of the one or more output transistor devices to charge the pad capacitance to reduce a maximum voltage developed in the system as a result of the ESD event." (EX-1001, Claim 1.)

200. In my opinion, Ker renders this claim obvious because a POSITA would have already been familiar with a number of digital, analog, or mixed mode circuits for this same purpose. In fact, Ker itself discloses an analog control block (orange) in Figure 37 within an ESD detection circuit (pink) used to turn on and off a transistor (blue).



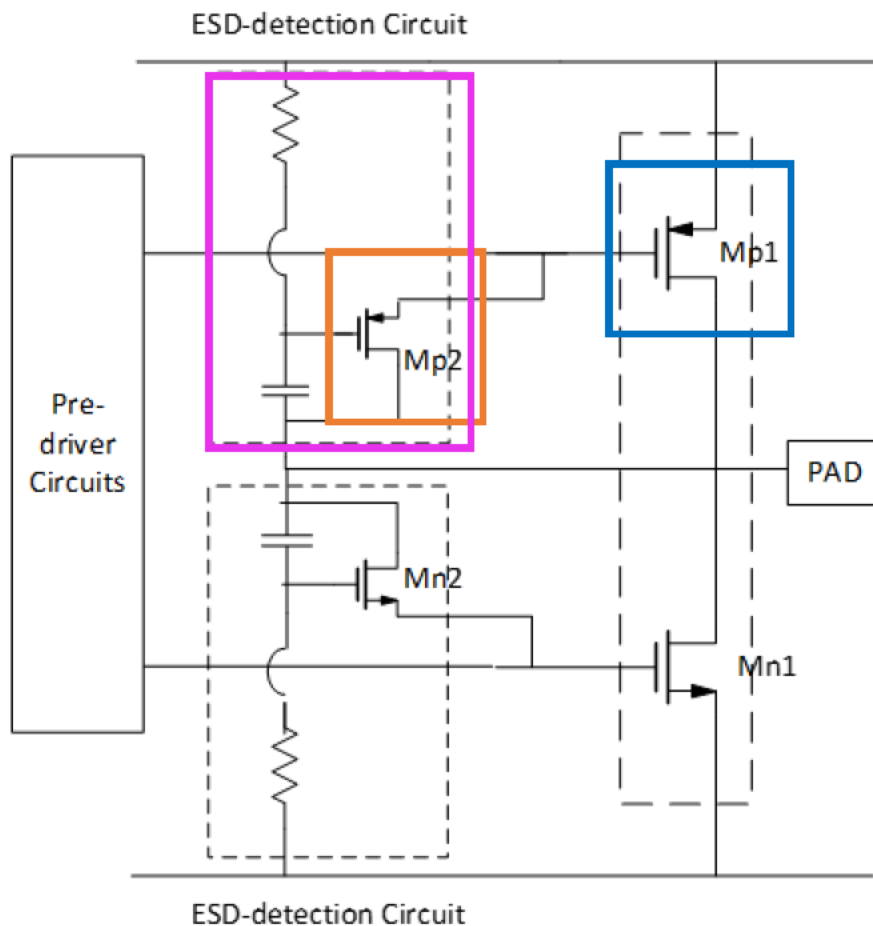
(EX-1005, Figure 37 (annotated).)

201. Figure 28, which shows a block diagram of the invention, indicates that the ESD detection circuit can take multiple forms.



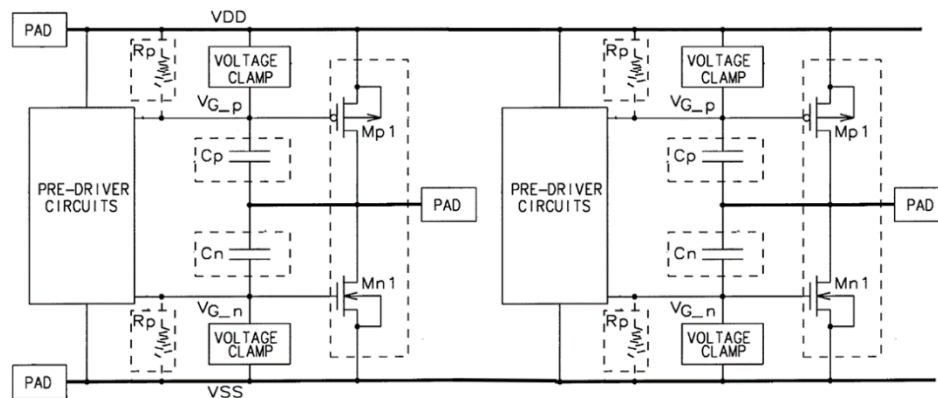
(EX-1005, Figure 28 (annotated).)

202. Accordingly, a POSITA would have understood that the ESD protection circuit shown in Figure 37 could be implemented as the ESD detection circuit in Figure 28. One possible embodiment of the resulting ESD detection circuit, control block, and output transistor is shown below.

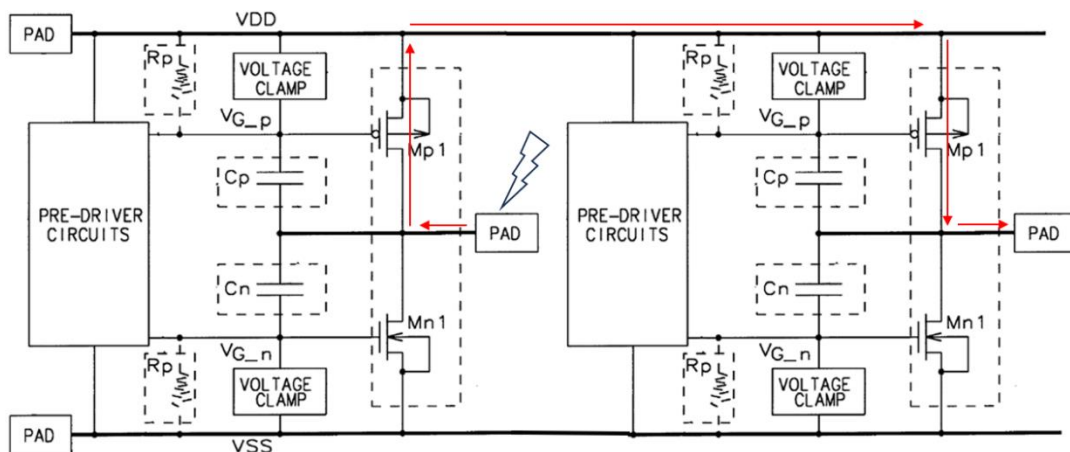


203. A POSITA would have been motivated to use the Figure 37 ESD detection circuit instead of other versions, such as the one shown in Figure 29. While the RC circuit is necessary for ESD detection, it creates a load on the output of the pre-driver circuits in the Figure 29 configuration. The Figure 37 version decouples the pre-driver circuits from the RC detection circuits during normal operating conditions, thereby reducing the load. A POSITA would expect this substitution to succeed because Ker itself discloses this alternate ESD detection circuit. Moreover,

205. Although Ker describes a single I/O pad, an individual Ker circuit would not be helpful. After all, by 2007 an integrated circuit typically contained multiple I/O pads, any of which could be subjected to an ESD event. Thus, a POSITA would understand that the ESD protection circuit disclosed in Ker is only effective if it is included at each I/O pad. Below, I provide an electrical schematic for a Ker circuit included at two I/O pads.



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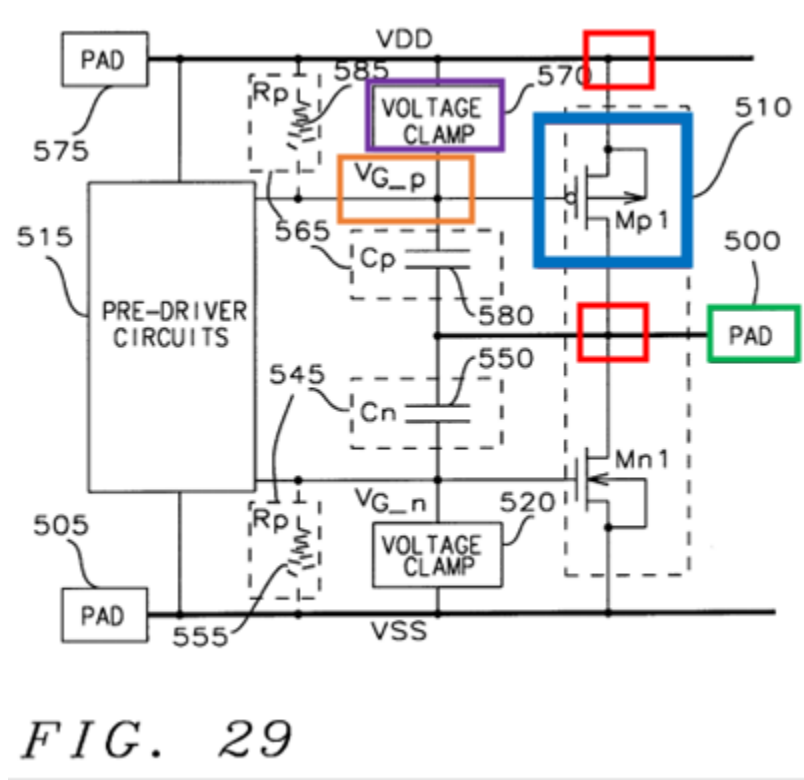
From there, the ESD energy charges the capacitance of any other I/O pads currently connected to the rail, thereby *reduc[ing] the maximum voltage developed in the system as a result of the ESD event.*

[e] a clamp device configured between a second voltage rail and a third voltage rail to reduce, when turned on, the maximum voltage developed in the system as the result of the ESD event;

207. At least under Microchip's apparent interpretation of this limitation as evidenced by its infringement contentions, Ker discloses this limitation.

208. I understand that Microchip's position is that the *first voltage rail* of claim 1[a] and *second voltage rail* of claim 1[e] can refer to the same voltage rail and/or be connected to each other. I further understand that, according to Microchip, the clamp need not be connected to both voltage rails to be *configured between* them. If so, Ker discloses a *second voltage rail* in the form of the Vdd rail. Ker's *third voltage rail* is Vss.

209. Ker further discloses a *clamp device* in the form of clamp circuit 570 (purple).



(EX-1005, Figure 29 (annotated).)

Clamp circuit 570 is configured between the second voltage rail (i.e., Vdd) and the third voltage rail (i.e., Vss.) (EX-1005, Figure 29.) When *turned on*, clamp circuit 570 *reduce[s] the maximum voltage developed in the system as the result of the ESD event* because it is “activated to prevent the voltage level attaining the voltage level that causes damage to the driver circuit 510.” (EX-1005, 18:58-18:60.) Basic principles of conservation dictate that the total voltage developed in the system is thereby reduced.

[f] enable circuitry configured to turn on the clamp device and instruct the control block to turn on the at least one of the one or more output transistor devices, in response to the ESD event;

210. Ker discloses this limitation.

211. In Figure 29, Ker teaches enable circuitry in the form of ESD detection circuit 565 (light blue).

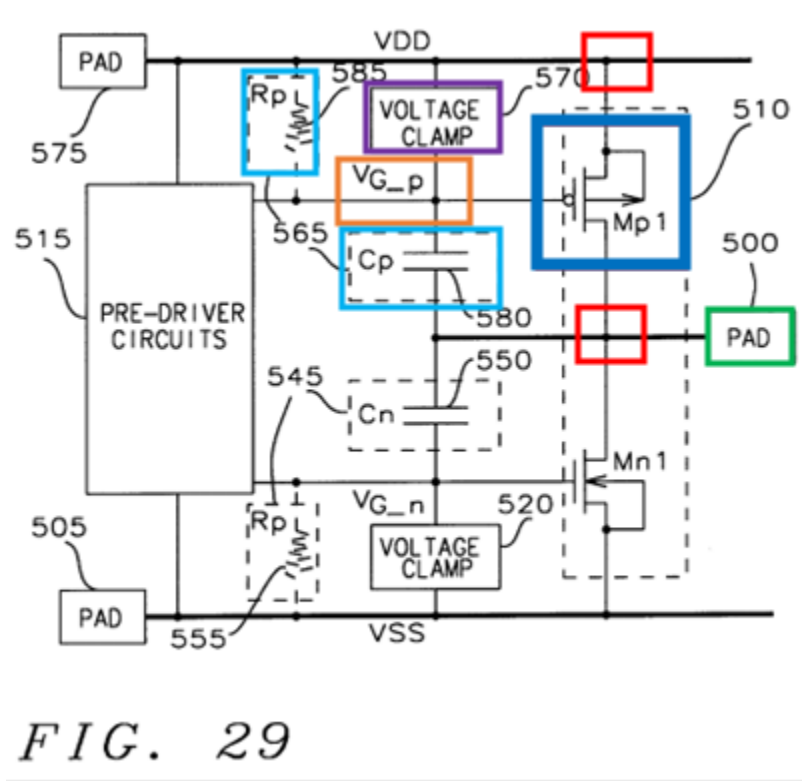


FIG. 29

(EX-1005, Figure 29 (annotated).)

ESD detection circuit 565 is “connected between the output signal terminal 500 and... output signal port VG_p of the pre-driver circuit 515.” (EX-1005, 18:20-18:23.) When an “ESD source having a negative polarity is coupled to... output signal terminal 500... ESD detection circuit 565 places [an] activation signal on...

signal port VG_p.” (EX-1005, 18:25-18:29.) As discussed above in claim 1[d], signal port VG_p, part of the *control block*, activates output transistor Mp1. Thus, the enable circuitry (i.e., ESD detection circuit 565) is configured to *instruct the control block to turn on the at least one of the one or more output transistor devices.*

212. ESD detection circuit 565 is also connected to the *clamp device* which, as discussed in claim 1[e], is clamp circuit 570. ESD detection circuit 565 is *configured to turn on the clamp device* because, when its output reaches a pre-defined voltage level, ESD detection circuit 565 turns on clamp device 570. Clamp circuit 570 then “activates and maintains the voltage level of... signal port VG_p.” (EX-1005, 19:33-19:35.)

213. Both actions are *in response to the ESD event* because the disclosed circuit is explicitly an “ESD detection circuit.” Moreover, Ker discloses that the circuit “senses the voltage level of the ESD source.” (EX-1005, 18:32-18:33.)

[g] wherein the second voltage rail is configured to provide power to the enable circuitry, and wherein the third voltage rail has a value below the first voltage rail.

214. At least under Microchip’s apparent interpretation of this limitation as evidenced by its infringement contentions, Ker discloses this limitation.

215. As discussed above in claim 1[e], Ker discloses a second voltage rail in Vdd. By convention, Vdd is *configured to provide power to* the entire circuit, including the *enable circuitry*. If the claim term *has a value below* refers to voltage,

then Ker's *third voltage rail* has a value below the *first voltage rail* because the first voltage rail (i.e., Vdd) has a positive voltage. The third voltage rail is Vss which, by convention, is ground.

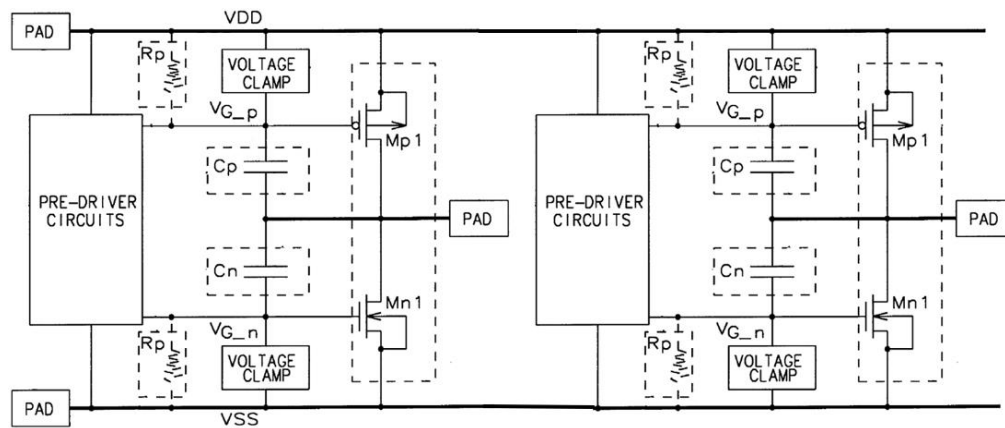
Claim 2 The pad circuit of claim 1, wherein in turning on the at least one of the one or more output transistor devices when instructed, the control block couples an associated capacitance of the first voltage rail to the physical pad to share a charge developed in the system in response to the ESD event, to reduce the maximum voltage developed in the system as the result of the ESD event.

216. At least under Microchip's apparent interpretation of this limitation as evidenced by its infringement contentions, Ker discloses this limitation.

217. As discussed previously in claim 1[d], Ker teaches a *control block* (i.e., output signal port VG_p and additional circuitry) that turns on *at least one of the one or more output transistor devices* (i.e., output transistor Mp1.) By turning on Mp1, output signal port VG_p *couples the first voltage rail* (i.e., Vdd) to the *physical pad* (i.e., pad 500.) As a physical, conductive device, the Vdd rail has an *associated capacitance*. When pad 500 is connected to the Vdd rail during an ESD event, the excess voltage charges the *associated capacitance* of the Vdd rail, thereby *reduc[ing] the maximum voltage developed in the system as a result of the ESD event*.

218. To the extent that the associated capacitance of the *first voltage rail* must be greater than its inherent capacitance, Ker renders the claim obvious. As

discussed in claim 1[e], by 2007 integrated circuit devices typically had multiple I/O pads, each of which required ESD protection. Thus, a POSITA would understand that the Ker invention is repeated at each I/O pad, like in the electrical schematic below.



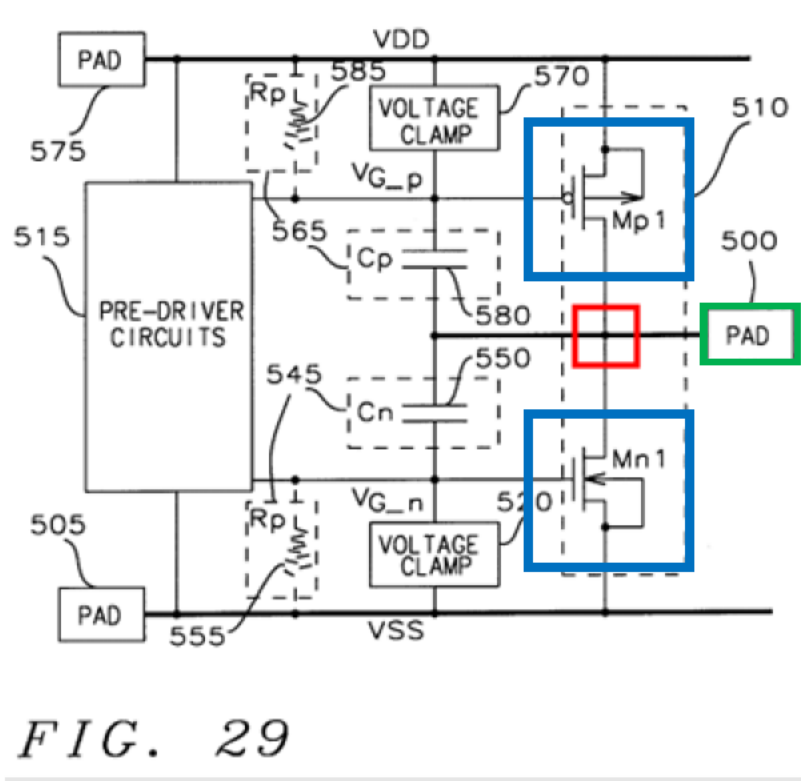
219. Thus, when pad 500 is coupled to the Vdd rail, the *associated capacitance* of the Vdd rail is equal to the capacitance of the rail and the sum of all other capacitive devices (i.e., I/O pads) currently connected to the Vdd rail. This further *reduce[s] the maximum voltage developed in the system by shar[ing] a charge* across a greater capacitance.

Claim 3 The pad circuit of claim 1, wherein the one or more output transistor devices are PMOS devices.

220. Ker discloses this limitation because output transistor Mp1 is a *PMOS device*. (EX-1005, 17:24.)

Claim 4 The pad circuit of claim 3, further comprising one or more NMOS devices coupled between the second node and the third voltage rail, wherein the NMOS devices and the PMOS devices are operable to operate together to drive the output signal at the second node, wherein the control block operates to turn off the NMOS devices during the ESD event.

221. Ker discloses this limitation because output transistor Mn1 (blue) is a NMOS device. (EX-1005, 17:24.) As shown below, it is coupled between the second node (red) and the third voltage rail (i.e., Vss).



222. Under normal operating conditions, output transistor Mp1 and Mn1 (blue) operate together to drive the output signal at the second node because they connect the node to either Vdd or Vss, creating a high or low output signal that goes

to pad 500 (green). But during a negative polarity ESD event, the control block (i.e., signal ports VG_p, VG_n, and additional circuitry) activates output transistor Mp1 as discussed above. (EX-1005, 18:24-18:34.) Conversely, the same signal turns off output transistor Mn1 because it is an N-type device.

Claim 5 The pad circuit of claim 1, wherein the pad circuit and the physical pad are comprised in a digital input/output pad.

223. At least under Microchip's apparent interpretation of this limitation as evidenced by its infringement contentions, Ker discloses this limitation.

224. For example, in one embodiment of the invention, "the ESD protection circuit is connected between a first power supply terminal, a second power supply terminal, and an input/output signal terminal of an integrated circuit formed on a semiconductor substrate." (EX-1005, 8:66-9:2.) Another embodiment is an integrated circuit output driver circuit for transferring digital signals from internal circuits to an output pad" (EX-1005, 9:44-9:46.) Thus, the *pad circuit and the physical pad are comprised in a digital input/output pad.*

Claim 6 A circuit configured to provide protection against electrostatic discharge (ESD) in a system comprising the circuit, the circuit comprising:

225. Ker discloses a *circuit configured to provide protection against electrostatic discharge (ESD) in a system comprising the circuit* because the invention is an "ESD protection circuit" that "dissipates an electrostatic charge from

an ESD source connected to the input/output signal terminal to protect the integrated circuit from damage caused by exposure to extreme voltage from the ESD Source.”

(EX-1005, 9:3-9:6.)

[a] an output buffer configured to couple to a physical pad having capacitance, to drive at least one output signal at the physical pad

226. Ker discloses this limitation.

227. I understand that, in context of the '665 patent, an output buffer is a signal driver circuit because “it should be noted that the terms ‘buffer’ and ‘output buffer’ are used herein in the context of electrical and/or integrated circuits to denote signal driver circuits.” (EX-1001, 4:27-4:30.)

228. In Figure 29, Ker discloses an output buffer (i.e., signal driver circuit) in the form of PMOS transistor Mp1 and NMOS transistor Mn1 (dark blue). Either transistor can *couple to a physical pad* because both are connected to pad 500 (green). (EX-1005, Figure 29.)

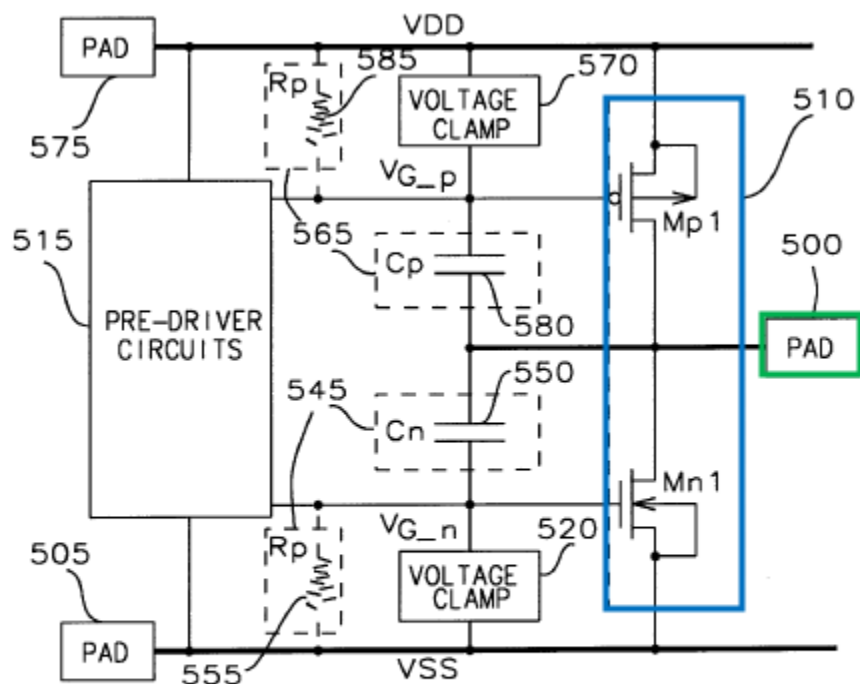


FIG. 29

(EX-1005, Figure 29 (annotated)).

229. Together, the transistors form driver circuit 510. (EX-1005, Figure 29.)

Driver circuit 510 can *drive at least one signal at the physical pad* because “driver circuit 510 will create the appropriate current and voltage levels from the electrical signals provided by the internal pre-driver circuits 515 to transfer the electrical signals to the external circuitry connected to the output signal terminal 500.” (EX-1005, 18:5-18:9.)

[b] a control block configured to control the output buffer;

230. In the discussion of claim 1[d], I describe a *control block* disclosed by Ker and the benefits of implementing it in the Figure 29 configuration. This control block is *configured to control the output buffer* (i.e., driver circuit 510) because ports VG_p and VG_N (orange), the outputs of the control block, are connected to the gates of PMOS transistor Mp1 and NMOS transistor Mn1, respectively. (EX-1005, 19:6-19:8, 19:24-19:26.)

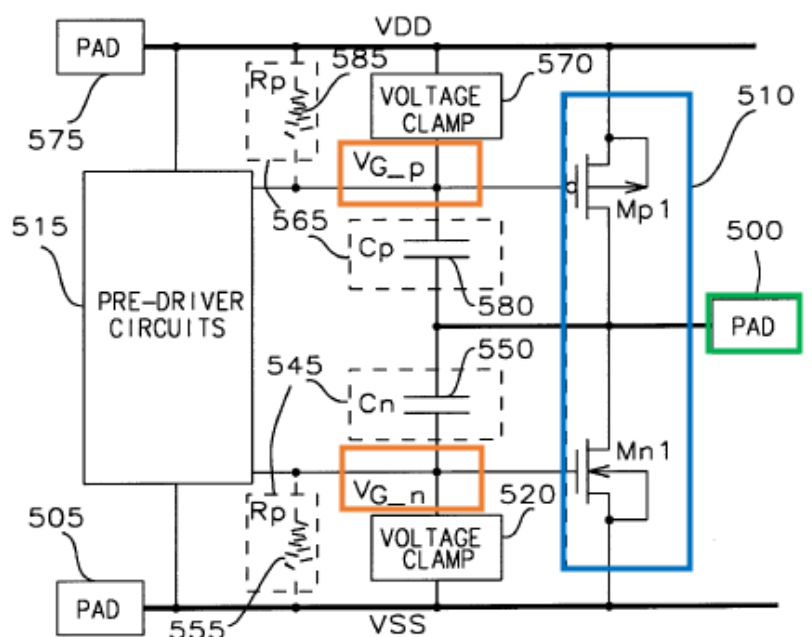


FIG. 29

(EX-1005, Figure 29 (annotated).).

[c] a clamp device coupled between a first supply rail and a low supply rail, wherein the clamp device is configured to absorb, when turned on, a portion of an energy generated by the ESD event, to reduce the maximum voltage developed in the system as the result of the ESD event; and

231. At least under Microchip's apparent interpretation of this limitation as evidenced by its infringement contentions, Ker discloses this limitation.

232. Based on Microchip's infringement contentions, I understand that Microchip's position is that the clamp need not be connected directly to the supply rails to be *coupled between* them. If so, Ker discloses a *first supply rail* in the form of the Vdd rail and a *low supply rail* in the form of the Vss rail. Ker discloses a clamp device in the form of voltage clamping circuit 520 (purple) *coupled between* the first and low supply rails as shown below.

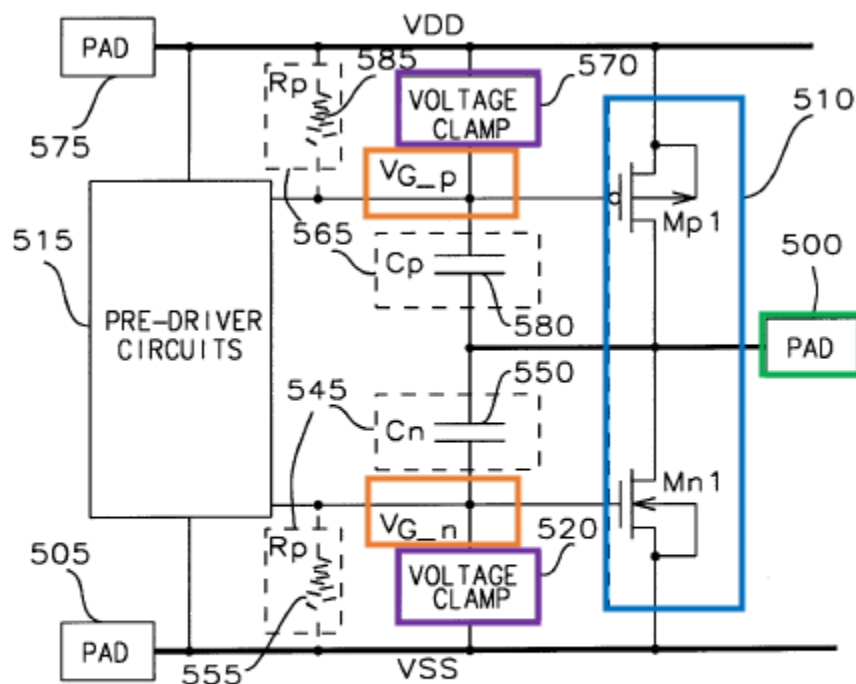


FIG. 29

(EX-1005, Figure 29 (annotated).).

233. Voltage clamping circuit 520 is *configured to absorb, when turned on, a portion of an energy generated by the ESD event* because when the voltage level at output signal port VG_n rises, voltage clamping circuit 520 is “activated to prevent the voltage level attaining the voltage level that causes damage to the driver circuit 510.” (EX-1005, 18:52-18:60.) Basic principles of conservation dictate that therefore, the *maximum voltage developed in the system as the result of the ESD event* is reduced.

[d] a control circuit configured to instruct the control block to activate at least a portion of the output buffer when an ESD event occurs,

234. Ker discloses this limitation.

235. As discussed above in claim 6[b], Ker discloses a *control block* comprising output ports VG_p and VG_n and additional circuitry. Ker further discloses a *control circuit* comprising ESD detection circuits 545 and 565 (light blue).

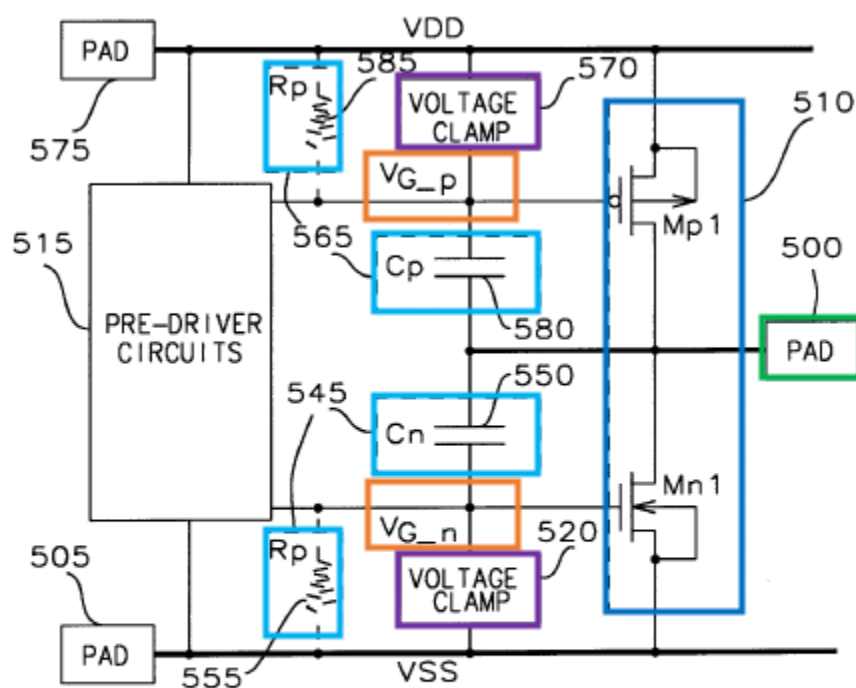


FIG. 29

(EX-1005, Figure 29 (annotated)).

236. These circuits are *configured to instruct the control block to activate at least a portion of the output buffer when an ESD event occurs* because “[i]f an ESD source having a voltage of a first polarity is coupled to the output signal terminal 500, the first ESD detection circuit 565 senses the voltage level of the first polarity and applies an activation signal to the first output signal port VG_n” or alternatively, “if the voltage level present on the ESD source has a polarity opposite the first polarity, the second ESD detection circuit 565 senses the voltage level of the ESD source and places a second activation signal at the second output signal port,” (i.e., VG_p.) (EX-1005, 18:24-18:34.)

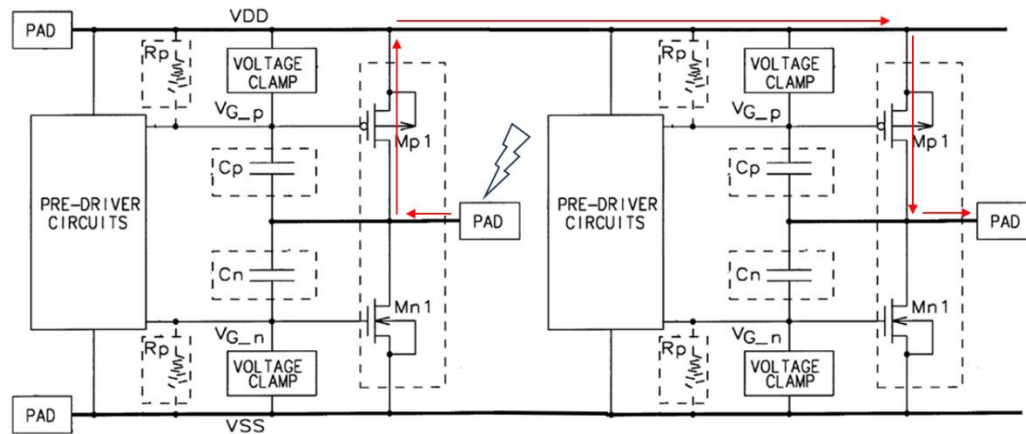
[e] [the control circuit configured] to charge the pad capacitance to reduce a maximum voltage developed in the system as a result of the ESD event

237. Ker discloses this limitation.

238. First, Ker teaches this limitation because *the control circuit* in Figure 29 (i.e., ESD detection circuits 545 and 565) sends an activation signal to VG_n or VG_p during an ESD event. In turn, VG_n and VG_p activate either output transistor Mn1 or Mp1. This connects pad 500 to the Vdd or Vss rail.

239. As discussed previously, a POSITA would understand that the Ker circuit must be repeated at every I/O pad to protect the integrated circuit. Therefore, when pad 500 is connected to the rail during an ESD event, the ESD energy flows to the rail. From there, the ESD energy *charge[s] the pad capacitance* of any other

I/O pads connected to the rail, thereby reducing *the maximum voltage developed in the system* due to the ESD event. The ESD path is show below.



[f] wherein the control circuit is further configured to turn on the clamp device in response to the ESD event;

240. Ker discloses this limitation.

241. Ker's control circuit is *further configured to turn on the clamp device in response to an ESD event* because one output of the control circuit (i.e., ESD detection circuits 545 and 565) is connected to voltage clamp 520. "When the voltage levels of the first and second output signal ports VG_n and VG_p begin to approach the voltage level at which the driver circuit 510 can be damaged, the appropriate voltage clamping circuits 520 and 570 are activated to prevent the voltage level attaining the voltage level that causes damage to the driver circuit 510." (EX-1005, 18:54-18:60.)

[g] wherein the first supply rail is configured to provide power to the control circuit

242. At least under Microchip's apparent interpretation of this limitation, as evidenced by its infringement contentions, Ker discloses this limitation. As discussed above in claim 6[c], Ker discloses a *first supply rail* Vdd. By convention, Vdd provides power to the entire circuit, including the control circuit. EX-

Claim 7 The circuit of claim 6,

[a] wherein the output buffer comprises one or more PMOS devices coupled between a second supply rail and the physical pad; and

243. At least under Microchip's apparent interpretation of this limitation as evidenced by its infringement contentions, Ker discloses this limitation.

244. I understand that Microchip's position is that the *first supply rail* of claim 6[c] and *second supply rail* of claim 7 can refer to the same voltage rail and/or be connected to each other. If so, Ker discloses a *second supply rail* in the form of the Vdd rail. As discussed in claim 6[a], Figure 29 discloses an *output buffer* in the form of driver circuit 510.

245. Ker further discloses an *output buffer comprising one or more PMOS devices* because output transistor Mp1—part of driver circuit 510—is a PMOS device. (EX-1005, 17:24, 18:62-18:64.) Output transistor Mp1 is *coupled between a*

second supply rail and the physical pad because it is connected between Vdd and pad 500, as shown below (dashed dark blue).

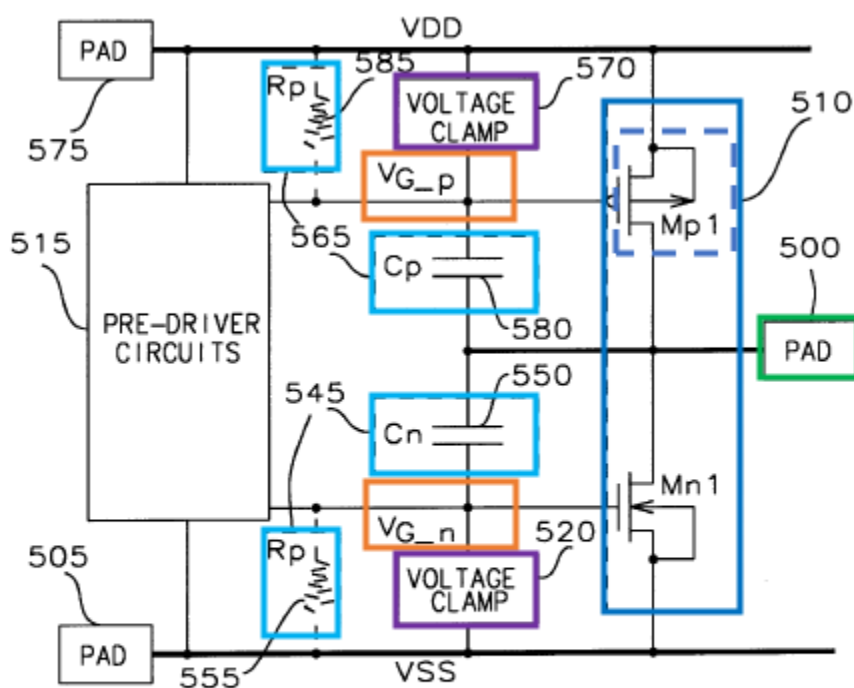


FIG. 29

(EX-1005, Figure 29 (annotated).).

[b] one or more NMOS devices coupled between the physical pad and the low supply rail wherein the low supply rail has a value less than the second supply rail

246. At least under Microchip's apparent interpretation of this limitation, as evidenced by its infringement contentions, Ker discloses this limitation.

247. Ker's output buffer (i.e., driver circuit 510) also comprises one or more NMOS devices because output transistor Mn1—part of driver circuit 510—is an

NMOS device. (EX-1005, 17:21-17:22, 18:62-18:64.) As discussed in claim 6[c], Ker discloses a low supply rail in the form of Vss, which has a value less than the second supply rail. Thus, output transistor Mp1 is *coupled between the physical pad and the low supply rail* because it is connected between pad 500 and Vss, as shown below (dashed dark blue).

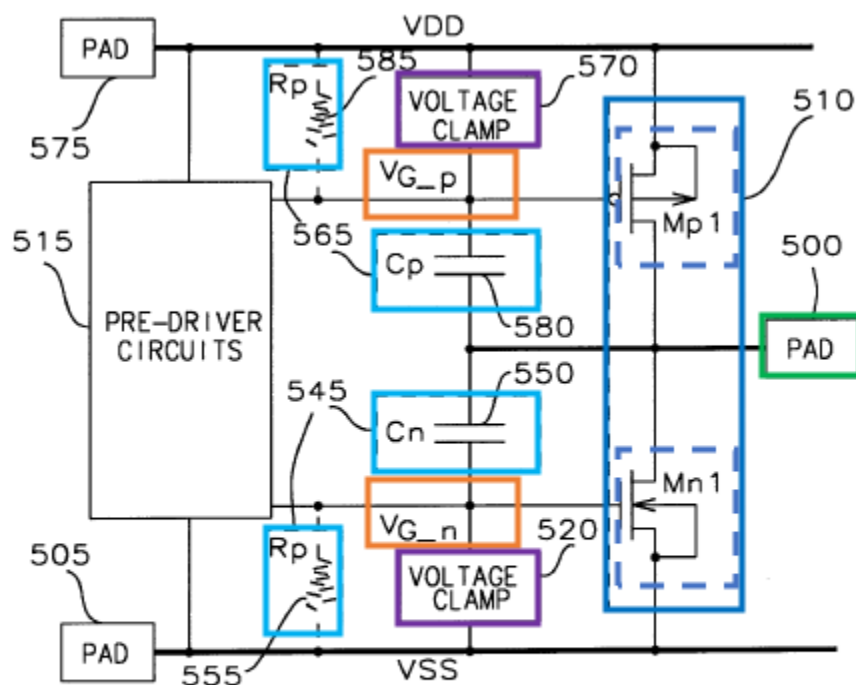


FIG. 29

(EX-1005, Figure 29 (annotated).)

[c] wherein in activating at least a portion of the output buffer when the ESD event occurs, the control block enables one or more of the one or more PMOS devices.

248. Ker discloses this limitation.

249. As discussed in claim 6[b]-6[e], in activating at least a portion of the output buffer (i.e., driver circuit 510) when the ESD event occurs, the control block (i.e., VG_p, VG_n, and other circuitry) enables one or more of the one or more PMOS devices (i.e., Mp1). For example:

250. “If an ESD source having a voltage level of a first polarity is coupled to the output signal terminal 500, the first ESD detection circuit 565 senses the voltage level of the first polarity and applies a first activation signal to the first output signal port VG_n. The driver circuit is activated and the charge present on the ESD source is dissipated preventing the damage. However, if the voltage level present on the ESD source has a polarity opposite the first polarity, the second ESD detection circuit 565 senses the voltage level of the ESD source and places a second activation signal at the second output signal port,” (i.e., VG_p), “of the internal pre-driver circuit 515. The driver circuit 510 is again activated to dissipate the charge from the ESD source.” (EX-1005, 18:24-18:36.)

Claim 8 The circuit of claim 7, wherein in activating at least a portion of the output buffer when the ESD event occurs, the control block disables one or more of the one or more NMOS devices.

251. Ker discloses a control block comprising VG_p, VG_n, and other circuitry. During an ESD event with a opposite (i.e., negative) polarity, ESD detection circuit 565 causes the control block to place an activation signal at VG_p,

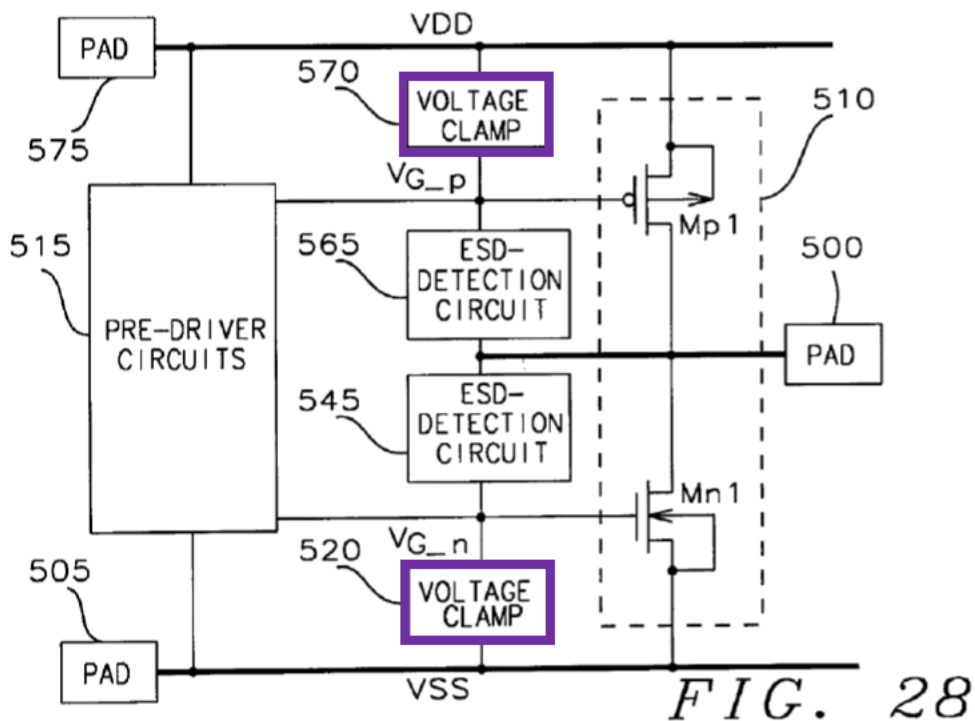
turning on output transistor Mp1. (EX-1005, 18:24-34.) Meanwhile, ESD detection circuit 545 causes the control block to put approximately the same signal at VG_n. This turns off output transistor Mn1 because it is an N-type device.

Claim 9 The circuit of claim 7, wherein the one or more PMOS devices comprise a plurality of PMOS devices coupled in parallel between the second supply rail and the physical pad, and the one or more NMOS devices comprise a plurality of NMOS devices coupled in series between the physical pad and the second supply rail.

252. Ker renders this limitation obvious for the same reasons described in the discussion of section A, claim 9.

Claim 10 The circuit of claim 6, wherein the clamp device is one of: a PMOS device having its source terminal coupled to the first supply rail, its drain terminal coupled to the low Supply rail, and its gate terminal coupled to the control circuit; or an NMOS device having its drain terminal coupled to the first supply rail, its source terminal coupled to the low supply rail, and its gate terminal coupled the control circuit.

253. Ker Figure 28 discloses two “voltage clamp device[s]” (purple). (EX-1005, Figure 28.)



(EX-1005, Figure 28 (annotated).)

254. A POSITA would understand that because Figure 28 does not show the exact components of the voltage clamps, the clamps can take multiple forms. This is confirmed by Figure 29, which shows that the clamps could comprise multiple diodes placed in series.

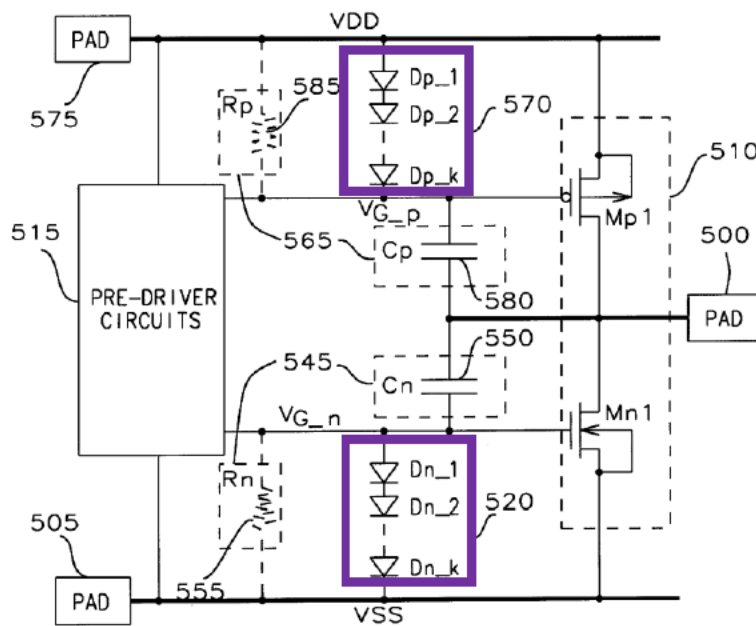


FIG. 30

(EX-1005, Figure 30 (annotated).)

255. At the time of the '665 patent, however, a conventional ESD clamp comprised a MOS transistor connected between the voltage rails. Ker discloses this type of voltage clamp in Figure 33.

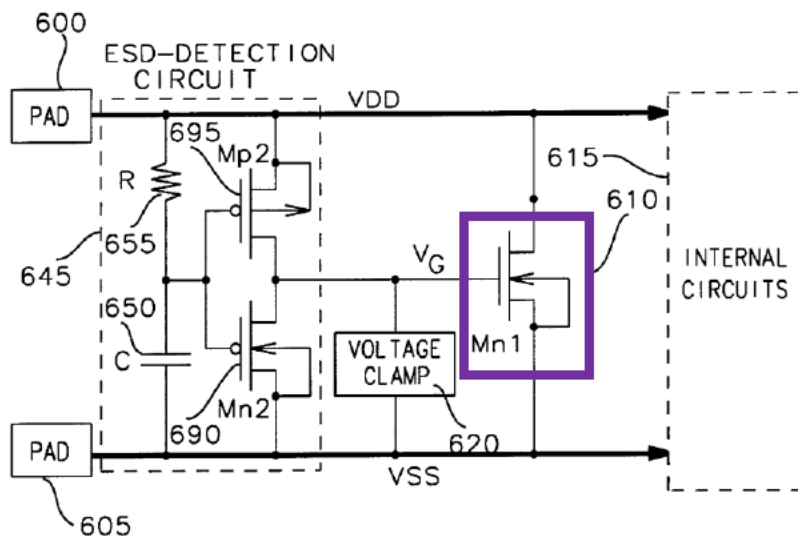


FIG. 33

(EX-1005, Figure 33 (annotated).)

256. A transistor-based voltage clamp is generally superior to a series of diodes because it allows for far greater power dissipation during an ESD event. A POSITA would understand that the transistor-based power clamp disclosed in Figure 33 could be added to the circuit of Figure 29. It would have been obvious to make this modification to allow for for superior power dissipation. After all, this type of power clamp was well-known in the art by 2007. Moreover, a POSITA would have had a reasonable expectation of success given that this method was common and transistors behave in predictable ways.

Claim 11 The circuit of claim 6, wherein the first supply rail is configured to provide increased power during the ESD event.

257. Ker discloses this limitation.

258. As discussed in claim 6, Ker Figure 29 discloses an embodiment that, during an ESD event, can connect pad 500 to the *first supply rail* (i.e., Vdd) via output transistor Mp1. This allows the excess ESD energy to flow to the Vdd rail, and thus the rail is *configured to provide increased power during the ESD event*.

Claim 12 The control circuit of claim 6, wherein in instructing the control block to activate at least a portion of the output buffer when an ESD event occurs, the control circuit is operable to provide a control signal to the control block in response to the ESD event.

259. As discussed in claim 6, Ker discloses a *control circuit* in the form of ESD detection circuits 545 and 565 that *instruct[s] the control block to activate at least a portion of the output buffer* (i.e., driver circuit 510.) This control circuit is *operable to provide a control signal to the control block* (i.e., output signal ports VG_n and VG_p and additional circuitry) *in response to the ESD event* because it “places the first activation signal” at VG_n or “the second activation signal” at VG_p depending on the polarity of the ESD event. (EX-1005, 19:8-19:12, 19:25-19:29.)

Claim 13 The circuit of claim 6, wherein the control circuit is configured to receive a control signal corresponding to a time constant, wherein the time constant corresponds to a specified slope, wherein the control signal is configured to trigger the control circuit if a slope of a Voltage pulse developed in the system as a result of the ESD event is greater than or equal to the specified slope.

260. At least under Microchip’s apparent interpretation of this limitation as evidenced by its infringement contentions, Ker discloses this limitation.

261. First, it is my opinion that a POSITA would understand that this claim refers to the conventional means of activating an ESD protection device: the RC circuit. As discussed in claims 6[d] and 6[e], Ker Figure 29 uses a control circuit in the form of ESD detection circuits 545 and 565. Both circuits are RC circuits. For example, capacitor Cn 550 and resistor Rn 555 “form the first ESD detection circuit.” (EX-1005, 19:40-19:41, Figure 29.)

262. This satisfies claim 13 because every RC circuit has a time constant that is proportional to the resistance and capacitance of the circuit. The time constant corresponds to how quickly the output voltage of the circuit can change. Thus, the output of the RC circuits 545 and 565 is *a control signal corresponding to a time constant*.

263. The RC circuit is the conventional means for detecting an ESD event because, during an ESD event, the *sudden voltage pulse developed in the system* exceeds the rate at which the output voltage of the RC circuit can change. In other words, the RC circuit determines if the slope of *[the] voltage pulse* is *greater than or equal to a specified slope* pre-set by the RC time constant. For example, Ker notes that, in a prior art ESD detection circuit, “the resistor R 80 and the capacitor C 85 have an RC time constant from approximately 0.1 μ sec to approximately 1.0 μ sec to detect the ESD transition across the power supply voltage source VDD and substrate biasing voltage source VSS.” (EX-1005, 4:39-4:44.)

264. Although Figure 29 shows the RC circuits connected directly to the output buffer, it would have been obvious to a POSITA that additional, intermediate circuitry could be used. As I explain in the discussion of claim 1[d], Ker itself discloses one such configuration where a transistor is added between the RC circuit and the output driver with desirable results. Thus, to any extent the control circuit cannot both generate and receive a control signal, the claim is rendered obvious because in such a configuration, the additional circuitry (i.e., the control circuit) receives a control signal from the RC circuit.

Claim 14 A system comprising:

265. To any extent the preamble is limiting, Ker discloses a system because it teaches an ESD protection circuit... to dissipate an electrostatic charge.” (EX-1005, Abstract.)

[a] one or more pads, each pad comprising: a respective physical pad having respective capacitance

266. Ker discloses this limitation.

267. Ker teaches *one or more pads* because one embodiment is “for dissipating electrostatic charge from an ESD source” in an “output driver circuit for transferring digital signals from internal circuits to an output pad.” (EX-1005, 9:44-9:46.) In Figure 29, for example, the *pad* is output signal terminal 500, labelled “pad 500” (green). (EX-1005, 18:5, Figure 29.)

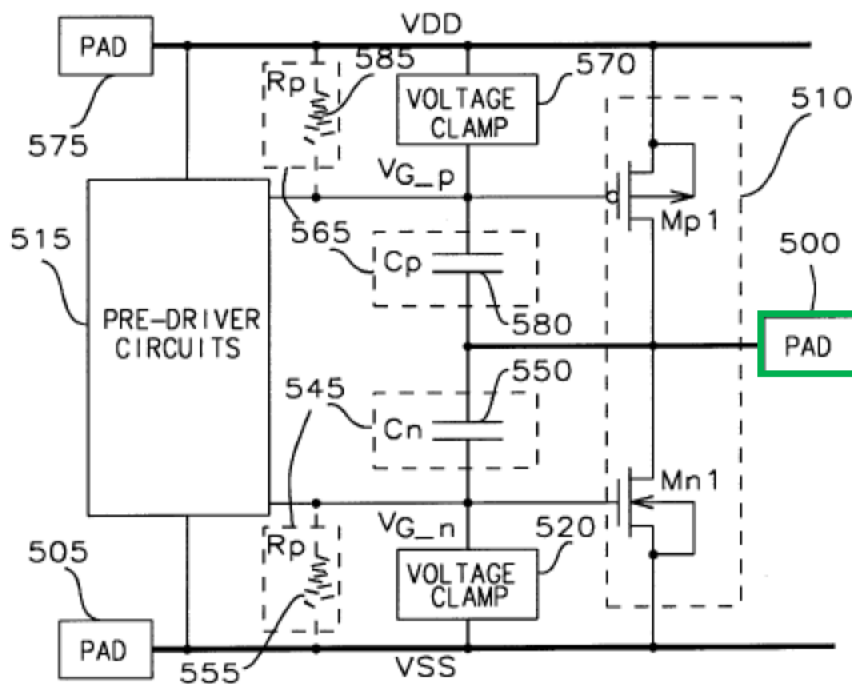


FIG. 29

(EX-1005, Figure 29 (annotated).)

268. A POSITA would understand that, in this context, pad 500 is a *physical pad*. And as a physical, conductive device, each pad *ha[s] respective capacitance*.

[b] [each pad comprising:] a respective clamp device configured to absorb, when turned on, a portion of an energy generated by an ESD event, to thereby further reduce the maximum voltage developed in the system as the result of the ESD event; and

269. Ker discloses this limitation.

270. In Figure 29, Ker discloses two *clamp device[s]* associated with pad 500: voltage clamp devices 520 and 570 (purple). (EX-1005, 18:43-18:50.)

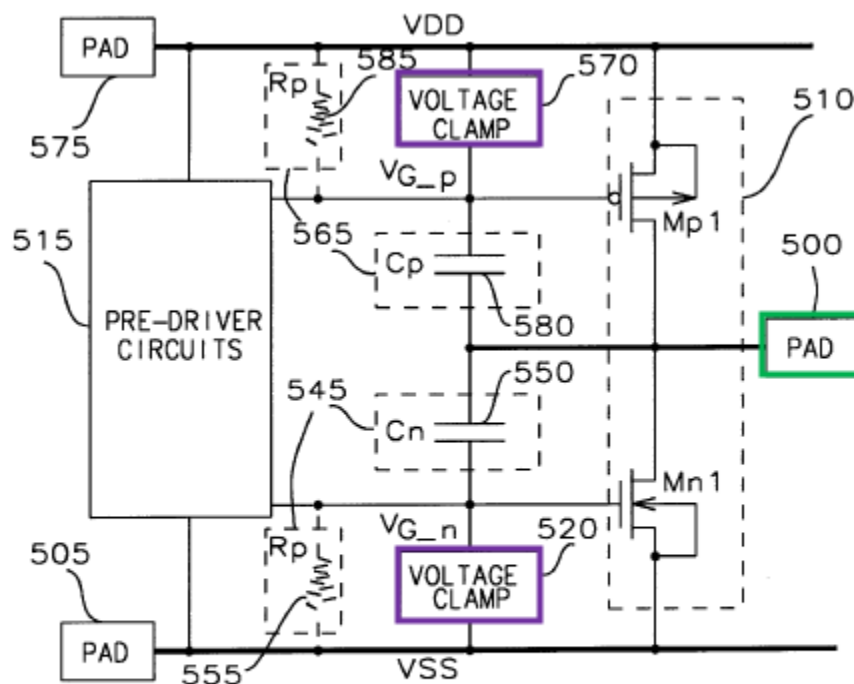


FIG. 29

(EX-1005, Figure 29 (annotated).)

271. These clamps are configured to absorb, when turned on, a portion of an energy generated by an ESD event because “when the voltage levels of the first and second output signal ports VG_n and VG_p begin to approach the voltage level at which the driver circuit 510 can be damaged, the appropriate voltage clamping circuits 520 and 570 are activated to prevent the voltage level attaining the voltage level that causes damage to the driver circuit 510.” (EX-1005, 18:54-18:60.) Basic principles of conservation dictate that therefore, the maximum voltage developed in the system is thereby reduced.

[c] [each pad comprising:] a respective pad circuit comprising: a respective output buffer coupled to the respective physical pad, and operable to drive at least one respective output signal at the respective physical pad; and

272. At least under Microchip's apparent interpretation of this limitation as evidenced by its infringement contentions, Ker discloses this limitation.

273. Ker teaches that the pad comprises *a respective pad circuit* because one embodiment of the invention "is an output driver circuit incorporating the ESD protection features of this invention." (EX-1005, 17:65-17:66.) As discussed in claim 6[a], Ker also discloses an *output buffer coupled to the pad* (dark blue) and *operable to drive at least one output signal at the pad*.

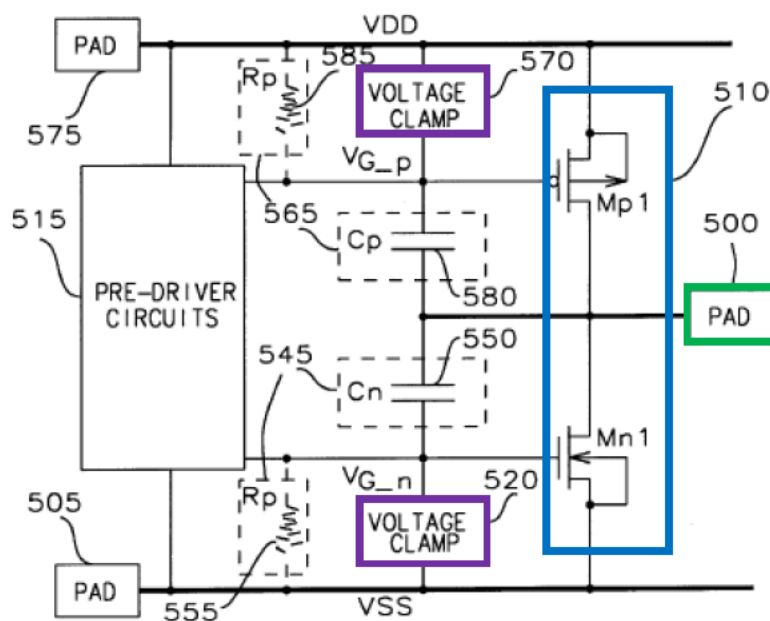


FIG. 29

(EX-1005, Figure 29 (annotated).)

[d] [the respective pad circuit comprising:] respective control circuitry operable to: activate at least a portion of the respective output buffer in response to an ESD event to charge the respective pad capacitance to reduce a maximum voltage developed in the system as a result of the ESD event; and

274. Ker discloses this limitation.

275. As discussed in claims 6[d] and 6[e], Ker discloses control circuitry (i.e., ESD detection circuits 545 and 565 (light blue)) operable to *activate at least a portion of the output buffer* (i.e., output transistor Mp1 or Mn1) in response to an ESD event.

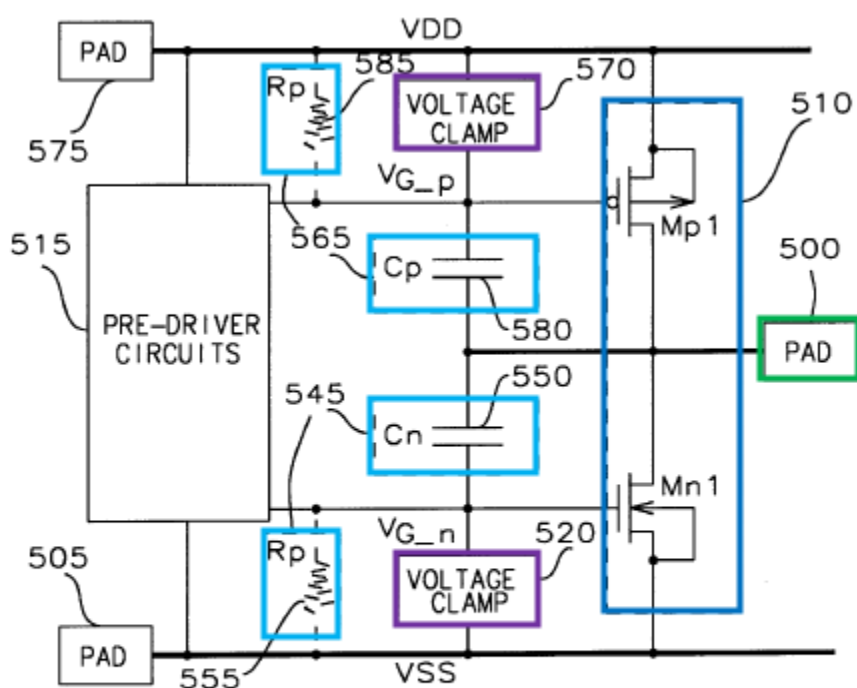
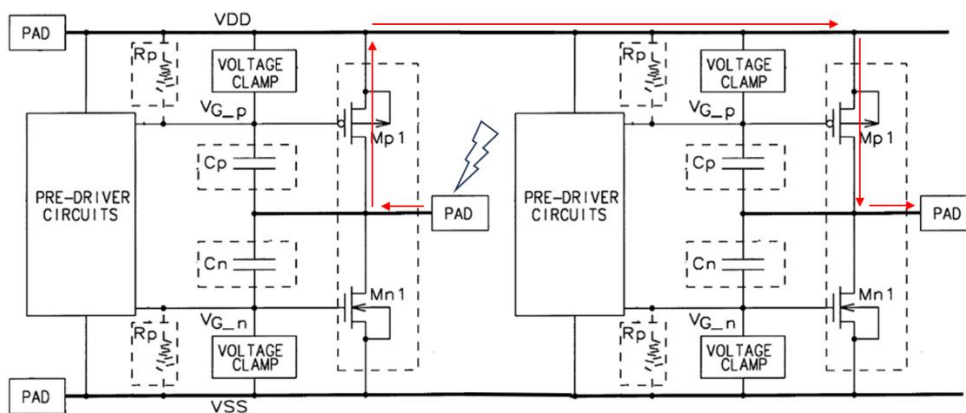


FIG. 29

(EX-1005, Figure 29 (annotated).)

276. In claims 6[d] and 6[e], I also explain why a POSITA would understand that the Ker circuit should be repeated at every I/O pad. Thus, enabling an output transistor allows the ESD energy to flow to adjacent pad circuits. This charges the capacitance of other pads connected to the voltage rail, as shown below, and reduces the maximum voltage developed in the system.



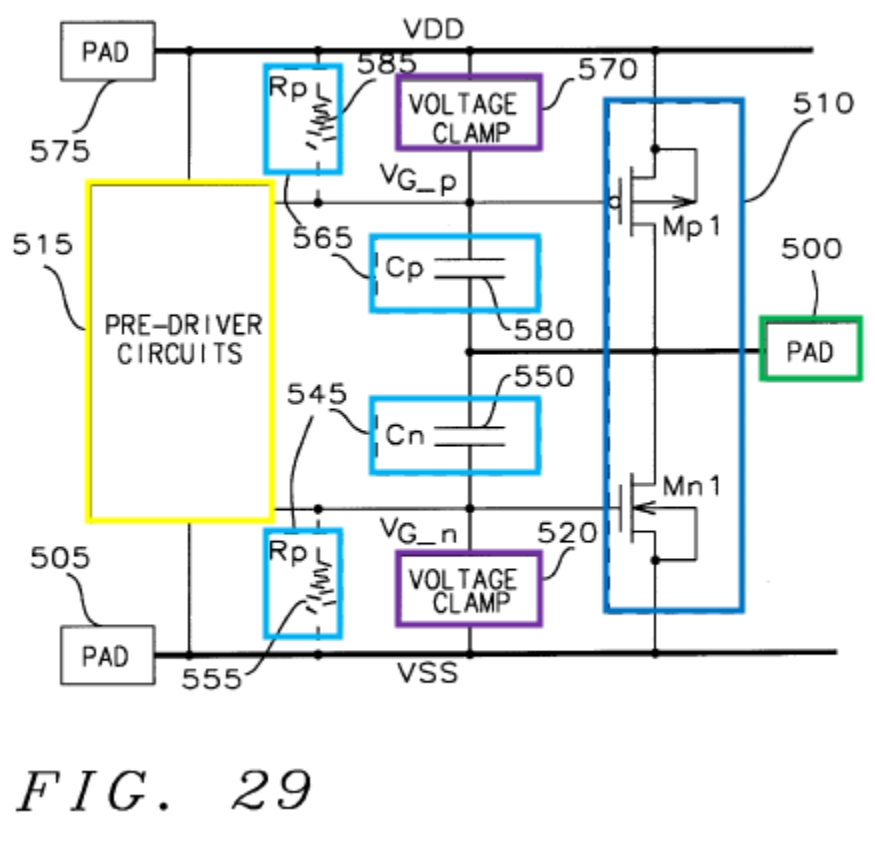
[e] [the respective control circuitry operable to:] turn on the clamp device in response to the ESD event.

277. Ker discloses this limitation because, as discussed in claim 6[d], Ker's control circuitry (i.e., ESD detection circuits 545 and 565) is operable to turn on the clamp device (i.e., voltage clamp 520 or 570) *in response to the ESD event*.

Claim 15 The system of claim 14, further comprising functional circuitry coupled to the respective pad circuit of at least one of the one or more pads, wherein the functional circuitry is operable to generate the at least one respective output signal driven by the respective pad circuit of the at least one of the one or more pads.

278. Ker renders obvious *functional circuitry coupled to the respective pad circuit to generate the output signal.*

279. Figure 29 discloses pre-driver circuits 515 (yellow).



(EX-1005, Figure 29 (annotated).)

The signal is then *driven by the pad circuit* of the pad 500 because “[t]he driver circuit 510 will create the appropriate current and voltage levels from the electrical

signals provided by the internal pre-driver circuits 515 to transfer the electrical signals to the external circuitry connected to the output signal terminal 500.” (EX-1005, 18:5-18:9.)

Claim 16 The system of claim 14, further comprising a first supply rail configured to provide increased power in accordance with the ESD event, and further configured to power the respective control circuitry of the respective pad circuit of each pad.

280. As discussed in claim 6, Ker Figure 29 discloses an embodiment that, during an ESD event, can connect pad 500 to the *first supply rail* (i.e., Vdd) via output transistor Mp1. This allows the excess ESD energy to flow to the Vdd rail, and thus the rail is *configured to provide increased power in accordance with the ESD event*. The Vdd rail is also *configured to power the respective control circuitry* because, by convention, it provides power to the circuit including the control circuitry.

Claim 17 The system of claim 16, further comprising a second supply rail configured to power the respective output buffer of the respective pad circuit of each pad.

281. At least under Microchip’s apparent interpretation of this limitation as evidenced by its infringement contentions, Ker discloses this limitation.

282. I understand that Microchip’s position is that the *first supply rail* of claim 16 and *second supply rail* of claim 17 can refer to the same voltage rail and/or be connected to each other. If so, Ker discloses a *second supply rail* in the form of

the Vdd rail. As discussed in claim 14[c], Ker discloses an output buffer in Figure 29 in the form of driver circuit 510. The Vdd rail is *configured to power the respective output buffer of the respective pad circuit of each pad* because “driver circuit 510” is “connected to the power supply voltage source Vdd.” (EX-1005, 17:66-18:1.)

Claim 18 The system of claim 16, wherein the respective control circuitry of the respective pad circuit of each pad is configured to receive a respective control signal corresponding to a time constant, wherein the time constant corresponds to a specified slope, wherein the respective control signal is configured to trigger the respective control circuitry if a slope of a voltage pulse developed in the system as a result of the ESD event is greater than or equal to the specified slope.

283. At least under Microchip’s apparent interpretation of this limitation as evidenced by its infringement contentions, Ker discloses this limitation.

284. As discussed in claim 13, a POSITA would understand that this claim describes using an RC circuit to detect an ESD event. In Figure 29, Ker discloses RC circuits for this same purpose. As described in claim 13, these RC circuits have a time constant and therefore the *control signal correspond[s] to a time constant*. The signal triggers the ESD protection measures when a *sudden voltage pulse developed in the system* exceeds the rate at which the output voltage of the RC circuit can change. In other words, the RC circuit determines if the slope of *[the] voltage pulse is greater than or equal to a specified slope* pre-set by the RC time constant.

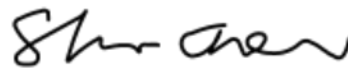
X. NO SECONDARY CONSIDERATIONS

285. I am not aware of any secondary considerations that may support the patentability of the challenged claims of the '665 patent set out above. To the extent Patent Owner, directly or through an expert, asserts that there are relevant secondary considerations of non-obviousness, I expressly reserve the right to respond and supplement my opinions herein.

* * *

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and that these statements were made with knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code.

Dated: April 12, 2024



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Curriculum Vitae

EDUCATION

University of California, Berkeley 2002 – 2006

- PhD in Electrical Engineering and Computer Science
- Dissertation: “High-Speed, Low-Power A/D Converter for a Low-Cost UWB Sub-sampling Radio”
- Advisor: Robert W. Brodersen

University of California, Berkeley 2000 – 2002

- Master of Science in Electrical Engineering and Computer Science
- Thesis: “Ultra Wideband Baseband Design and Implementation”

National Taiwan University 1994 – 1998

- Bachelor of Science in Electrical Engineering
- Top 1 student for upper division

ACADEMIC EXPERIENCE

- Professor, Department of Electrical Engineering, University of Southern California, 2021 – Present.
- Associate Professor, Department of Electrical Engineering, University of Southern California, 2017 – 2021.
- Colleen and Roberto Padovani Early Career Chair, USC, 2014 – 2021
- Assistant Professor, Department of Electrical Engineering, University of Southern California, 2011 – 2017.
- Graduate Student Researcher, Berkeley Wireless Research Center, Berkeley, CA, 2001 – 2006.

WORK EXPERIENCE

- Analog Senior Technical Staff, Atheros Communications, Santa Clara, CA, 2006–2010.
-Designed RF, analog mixed-signal circuits for various wireless products

CONSULTING EXPERIENCE

- Legal: Morrison & Foerster LLP (2019-2022): Xilinx-ADI litigation
Legal consultant, working with counselors to prepare/review legal documents, non-infringement arguments, deposition, source codes, PTAB, etc.

- Technical: Qualcomm, Samsung, BAE system, Tetramem

HONORS and AWARDS

- ISSCC 2022 Jack Kilby Award (co-recipient)
- RFIC 2022 Best Student Paper Award – First Place (co-recipient)
- IEEE Solid-State Circuit Society (SSCS) Distinguished Lecturer 2021-2023.
- Qualcomm Faculty Award, 2019.
- DARPA Young Faculty Award (YFA), 2014.
- NSF Faculty Early Career Development (CAREER) Award, 2014.
- Analog Devices Outstanding Student Award, 2006
- UC Regents Fellowship, UC Berkeley, 2000
- Lin's Foundation Award for Top 1 engineering college student over the academic year, 1996-1997
- Presidential Awards, National Taiwan University, 1996-1998
- Member of National Mathematics Team of Taiwan, awarded with Honourable Mention in Asian Pacific Mathematics Olympiad, 1994.

KEY TECHNICAL CONTRIBUTIONS

Analog Mixed-Signal and RF circuit architectures/techniques for data converters, clock generation and PA.

- Asynchronous SAR ADC (since 2006)
- Embedded TDC scheme for Digital PLL (since 2010)
- Nonuniform sampling (NUS) ADCs and NU DSP (since 2012)
- Direct spur/pulling cancellation for Digital PLL (since 2014)
- Dual-rate hybrid DAC (since 2014)
- Sub-harmonic switching (SHS) PA (since 2018)
- Time-Approximation Filter (TAF) for Transceiver (since 2019)
- Two-Point DTC Calibration scheme for Multiplying DLL (since 2021)
- Delay-tracking pipelined SAR TDC (since 2022)

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2. S. Su*, Q. Zhang*, and **M. S.-W. Chen**, "A 2GS/s 8.5-Bit Time-Based ADC Using a Segmented Stochastic Flash TDC," in 2023 IEEE Custom Integrated Circuits Conference (CICC), Apr. 2023 (* equal contribution)

3. Q. Zhang, H.-C. Cheng, S. Su, and **M. S.-W. Chen**, “A Fractional-N Digital MDLL with Injection Error Scrambling and Background Third-Order DTC Delay Equalizer Achieving -67dBc Fractional Spur,” in *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2023. (To appear)
4. Q. Zhang*, S. Su*, and **M. S.-W. Chen**, “A Cost-Efficient Fully Synthesizable Stochastic Time-to-Digital Converter Design Based on Integral Nonlinearity Scrambling,” in *2022 59th ACM/EDAC/IEEE Design Automation Conference (DAC)*, July 2022. (*contributed equally to this work)
5. C. Yang, S. Su and **Mike Chen**, “A Millimeter-Wave Mixer-First Receiver with Non-Uniform Time-Approximation Filter Achieving $>45\text{-dB}$ Blocker Rejection,” in *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, June 2022. (Best Student Paper Award – First Place)
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7. J. Liu, M. Hassanpourghadi, and **M. S.-W. Chen**, “A 10GS/s 8b 25fJ/c-s $2850\mu\text{m}^2$ Two-Step Time-domain ADC Using Delay-Tracking Pipelined-SAR TDC with 500fs Time Step in 14nm CMOS Technology“, *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2022.
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12. R.A. Rasul, and **M. S.-W. Chen**, “A 128×128 SRAM Macro with Embedded Matrix-Vector Multiplication Exploiting Passive Gain via MOS Capacitor for Machine Learning Application,” *IEEE Custom Integrated Circuits Conference (CICC)*, Apr. 2021.
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14. Q. Zhang, S. Su, C.-R. Ho, and **M. S.-W. Chen**, “A Fractional-N Digital MDLL with Background Two-Point DTC Calibration Achieving -60dBc Fractional Spur,” *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2021.

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7. S. Su, **M. S.-W. Chen**, "A Time-approximation Filter for Direct RF Transmitter," *IEEE J. Solid-State Circuits (JSSC)* 2021.
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10. A. Zhang, **M. S-W. Chen**, "A Subharmonic Switching Digital Power Amplifier for Power Back-Off Efficiency Enhancement," (Invited) *IEEE J. Solid-State Circuits (JSSC)* Feb., 2019.
11. T.F. Wu, **M. S.-W. Chen**, "A VCO-Based Nonuniform Sampling ADC with Phase-Domain Level Crossing," (Invited) *IEEE J. Solid-State Circuits (JSSC)* Mar., 2019.
12. S. Su, **M. S.-W. Chen**, "A 16-bit 12GS/s Single/Dual-Rate DAC with a Successive Bandpass Delta-Sigma Modulator Achieving <-67dBc IM3 within DC to 6GHz Tunable Passbands," (Invited) *IEEE J. Solid-State Circuits (JSSC)* Dec., 2018.
13. T.F. Wu, **M. S-W. Chen**, "A Subranging-Based Nonuniform Sampling ADC With Sampling Event Filtering," *IEEE Solid-State Circuits Letters (SSC-L)* April, 2018.
14. J.W. Nam, M. Hassanpourghadi, A. Zhang, **M.S-W Chen**, "A 12-bit 1.6/3.2/6.4 GS/s 4 b/cycle Time-interleaved SAR ADC with Dual Reference Shifting and Interpolation," *IEEE J. Solid-State Circuits (JSSC)*, June, 2018.
15. T.F. Wu, C.R. Ho, **M. S.-W. Chen**, "A Flash-Based Non-Uniform Sampling ADC With Hybrid Quantization Enabling Digital Anti-Aliasing Filter," *IEEE J. Solid-State Circuits (JSSC)* Sep., 2017.
16. M. Hassanpourghadi, P.K. Sharma, and **M. S.-W. Chen**, "A 6-bit Nyquist AC-coupled VCO Based ADC at 800MS/s," *IEEE Transactions on Circuits and Systems (TCAS-I)* 2017.

17. C.R. Ho, **M. S.-W. Chen**, "A Digital PLL with Feedforward Multi-Tone Spur Cancellation Loop Achieving <-73dBc Fractional Spur and <-110dBc Reference Spur in 65nm CMOS," (Invited) accepted for *IEEE J. Solid-State Circuits* (JSSC) Dec., 2016.
18. S. Su, **M. S.-W. Chen**, "A 12b 2GS/s Dual-Rate Hybrid DAC with Pulsed Timing-Error Pre-Distortion and In-Band Noise Cancellation Achieving >74dBc SFDR up to 1GHz in 65nm CMOS," (Invited) accepted for *IEEE J. Solid-State Circuits* (JSSC) Dec., 2016.
19. J.W. Nam, **M. S.-W. Chen**, "An Embedded Passive Gain Technique for Asynchronous SAR ADC Achieving >10 ENOB, 1.36 mW at 95MS/s in 65nm CMOS," accepted by *IEEE Transactions on Circuits and Systems (TCAS-I)* 2016
20. T.F. Wu, S. Dey, **M. S.-W. Chen**, "A Non-Uniform Sampling ADC Architecture with Reconfigurable Digital Anti-aliasing Filter," accepted by *IEEE Transactions on Circuits and Systems (TCAS-I)* 2016
21. C.R. Ho, **M. S.-W. Chen**, "A Fractional-N DPLL with Calibration-free Multi-phase Injection-locked TDC and Adaptive Single-tone Spur Cancellation Scheme," accepted by *IEEE Transactions on Circuits and Systems (TCAS-I)* 2016
22. S. Su, T. Tsai, P. Sharma, **M. S.W. Chen**, "A 12-bit 1GS/s Dual-Rate Hybrid DAC with an 8GS/s Unrolled Pipeline Delta-Sigma Modulator Achieving >75dB SFDR over the Nyquist Band," (Invited) *IEEE J. Solid-State Circuits*, April, 2015.
23. Y. Cao, J. Velamala, K. Sutaria, **M. S.W. Chen**, J. Ahlbin, I. Esqueda, M. Bajura, M. Fritze, "Cross-Layer Modeling and Simulation of Circuit Reliability", *IEEE Transactions on CAD of Integrated Circuits and Systems*, Jan. 2014.
24. **M.S.W. Chen**, D. Su, S. Mehta, "A Calibration-Free 800MHz Fractional-N Digital PLL with Embedded TDC," (Invited) *IEEE Journal of Solid-State Circuits*, Dec. 2010.
25. Zargari, M.; Nathawad, L.Y.; Samavati, H.; Mehta, S.S.; Kheirkhahi, A.; Chen, P.; Gong, K.; Vakili-Amini, B.; Hwang, J.A.; **Chen, S.-W.M.**; Terrovitis, M.; Kaczynski, B.J.; Limotyakis, S.; Mack, M.P.; Gan, H.; MeeLan Lee; Chang, R.T.; Dogan, H.; Abdollahi-Alibeik, S.; Baytekin, B.; Onodera, K.; Mendis, S.; Chang, A.; Rajavi, Y.; Jen, S.H.-M.; Su, D.K.; Wooley, B.A., "A Dual-Band CMOS MIMO Radio SoC for IEEE 802.11n Wireless LAN," *IEEE J. Solid-State Circuits*, Dec. 2008.
26. **M.S.W. Chen**, R. W. Brodersen, "A Subsampling Radio Architecture for Ultrawideband Communications," *IEEE Transactions on Signal Processing*, Oct. 2007.
27. **M.S.W. Chen**, R. W. Brodersen, "A 6-bit 600-MS/s 5.3-mW Asynchronous ADC in 0.13-um CMOS," *IEEE J. Solid-State Circuits*, Dec. 2006.
28. **M.S.W. Chen**, R. W. Brodersen, "A Subsampling UWB Impulse Radio Architecture Utilizing Analytic Signaling," (Invited Paper) *IEICE Trans. on Electronics*, June 2005.
29. D. Cabric, **M. S.-W. Chen**, D. Sobel, S. Wang, J. Yang, and R. W. Brodersen, "Novel Radio Architectures for UWB, 60GHz, and Cognitive Wireless Systems," *EURASIP J. on Wireless Communcations and Networking*, 2006.

1. **M. S.-W. Chen**, “Trend and New Opportunities in Digital PLL Design”, (Invited) IEEE Solid State Circuit Magazine, 2020 winter issue.
2. C.R. Ho, **M. S.-W. Chen**, “Clock Generation in the future with Digital Signal Processing Technique for Mitigating Spur and Interference,” IEEE Microwave Magazine 2019.
3. Sankaran, S.G.; Zargari, M.; Nathawad, L.Y.; Samavati, H.; Mehta, S.S.; Kheirkhahi, A.; Chen, P.; Ke Gong; Vakili-Amini, B.; Hwang, J.; **Chen, S.-W.M.**; Terrovitis, M.; Kaczynski, B.J.; Limotyakis, S.; Mack, M.P.; Gan, H.; Lee, M.; Chang, R.T.; Dogan, H.; Abdollahi-Alibeik, S.; Baytekin, B.; Onodera, K.; Mendis, S.; Chang, A.; Rajavi, Y.; Jen, S.H.-M.; Su, D.K.; Wooley, B., “Design and implementation of a CMOS 802.11n soc –[integrated circuits for communications],” *Communications Magazine*, April 2009.
4. D. Cabric, I. O’Donnell, **M. S.-W. Chen**, and R.W. Brodersen, “Spectrum Sharing Radios,” (Invited) *IEEE Circuits and Systems Magazine*, 2006.

Book Chapter

1. C.R. Ho, **M. S.-W. Chen**, “Fractional-N spur reduction techniques for DPLL,” *Phase-Locked Frequency Generation and Clocking: Architectures and Circuits for Modern Wireless and Wireline Systems*, IET 2019 (under preparation).
2. **M. S.-W. Chen**, “Challenges and Emerging Trend of DSP Enabled Frequency Synthesizer,” *Digitally-Assisted Analog and Analog-Assisted Digital IC Design*. Chapter4, 2015, Cambridge University Press.
3. **M. S.-W. Chen**, “Energy-Efficient ADC Topology Enabled with Asynchronous Techniques,” *Circuits for Nanoscale: Communications, Imaging, and Sensing*. Chapter14, Sep. 2008.

Patent

1. **M.S.W. Chen**, C.R. Ho, “Adaptive spur cancellation techniques and multi-phase injection locked TDC for digital phase locked loop circuit,” US patent #9941891, 2018.
2. **M. S.W. Chen**, “Non-uniform Sampling Analog to Digital Converter (ADC) Architecture with Digital Reconfigurable Anti-Aliasing Filter,” filed for provisional patent application, No. 61/911,261, Dec., 2013.
3. **M. S.W. Chen**, D. Su, “Fractional and Integer PLL Architectures,” US patent #8289086, 2012.

INVITED TALKS/TUTORIALS/WORKSHOPS

1. ITRI, Taiwan, “New Opportunities in Mixed-Signal ICs”, June, 2011.
2. UMC, Taiwan, “New Opportunities in Mixed-Signal ICs”, June, 2011.
3. HRL Laboratories, LLC: “Enhancing A-to-D Conversion Efficiency”. July 2nd, 2012
4. “Analog-to-Digital Interface: A Time Approach” 2013 CMOS Emerging Technologies Research Symposium, Whistler, July 2013.

5. "Path towards High-Speed High-Resolution Data Converters with Diminishing Cost", Sep. 2013, Broadcom.
6. "Analog-Digital Interface Research, really?" Sep. 2013, Qualcomm-Atheros.
7. "Re-shape Future Mixed-Signal IC Design" Oct. 2013, Qualcomm.
8. "Path towards High-Speed High-Resolution Data Converters with Diminishing Cost", Nov. 2013, UT Dallas.
9. "Path towards High-Speed High-Resolution Data Converters with Diminishing Cost", Nov. 2013, Texas Instrument.
10. "Power efficient ADC Topologies towards RF Sampling" 2014 RFIC Tutorial.
11. "Path Towards Direct RF Synthesis: A Hybrid Digital-to-Analog Converter Architecture" 2014 IEEE MWSCAS Conference, Distinguished Speaker Series.
12. "Asynchronous SAR ADC: Past, Present and Beyond" 2014 IEEE MWSCAS Conference Tutorial
13. "Exploring Limits of Mixed-Signal ICs" Sep. 2014, MaxLinear Corp.
14. "Rethinking Analog-Digital Interface Circuit Architectures" Oct. 2014, IC Seminar, Columbia University, NY.
15. "Rethinking Analog-Digital Interface Circuit Architectures" Mar. 2015, IC Seminar, UC Berkeley, CA.
16. "Rethinking Analog-Digital Interface Circuit Architectures" Dec. 2015, IC Seminar, National Taiwan University(NTU)/IEEE Chapter, Taipei, Taiwan.
17. "Rethinking Analog-Digital Interface Circuit Architectures" Feb. 2016, IC Seminar, UT Austin, Texas.
18. "Asynchronous SAR ADC: Past, Present and Beyond", Feb. 2016, EE department Colloquium, UT Austin/IEEE Chapter.
19. "Rethinking Analog-Digital Interface Circuit Architectures" Feb. 2016, IC Seminar, University of Michigan, Ann Arbor.
20. "Rethinking Analog-Digital Boundary from Circuit to System Level towards Reconfigurability of Everything" Mar. 2016, SystemX Seminar, Stanford
21. "Rethinking Analog-Digital Interface Circuit Architectures" April. 2016, EE department Colloquium. Carnegie Mellon University (CMU).
22. "Rethinking Analog-Digital Interface Circuit Architectures" April. 2016, IC Seminar, University of California, Los Angeles (UCLA).
23. "IC Research overview," TSMC, 2017
24. "IC Research overview," Intel Lab, 2017
25. "IC Research overview," InPhi, 2017
26. "Advancing Low-Power High-Speed Analog-to-Digital Converters: An Asynchronous Design Approach", VLSI DAT tutorial, 2017
27. "Generic spur cancellation for digital PLL," Qualcomm 2017
28. "Evolutions of SAR ADC: from High Resolution to High Speed Regime," IEEE CICC 2018 tutorial.
29. "Emerging Opportunities in Analog Mixed-Signal Circuit Design Automation," ACM/IEEE ICCAD 2018 workshop.
30. "Analog-to-Digital Converter Architecture Opportunities in Emerging Wireless Systems," RFIC 2018 workshop
31. "How can hardware designers reclaim the spotlight?" moderator/co-organizer of ISSCC 2019 evening panel.

32. “Fundamentals of Analog-to-digital conversion,” 2-day tutorial in Shanghai, China 2019.
33. “Digital Fractional-N Phase Locked Loop Design,” tutorial, ISSCC Feb 2020
34. “Digital Fractional-N Phase Locked Loop Design,” ISSCCedu Feb 2020
35. “Low Spur PLL architectures,” MEAD tutorial in EPFL, 2021 (to appear)
36. “Low Spur PLL architectures and techniques,” IEEE CICC 2020
37. “New Opportunities in Nonuniform Sampling,” IEEE SSCS Webinar Oct 2020.
38. “High-Performance Digital-to-Analog Converter Design: A Path towards Digital Transmitter,” ISESD Keynote June 2021
39. “ADC Evolution via Architectural Rethinking: from Asynchronous SAR to Non-uniform Sampling ADC,” IEEE SSCS Tainan Chapter, Oct 2021
40. “High-Performance Digital-to-Analog Converter Design: A Path towards Digital Transmitter,” IEEE SSCS Atlanta Chapter, Nov. 2021
41. “Asynchronous SAR ADC: Past, Present and Beyond,” IEEE Southern Alberta Chapter, Nov. 2021
42. “Non-Uniform Sampling Data Converters: A Journey to Uncharted Circuits and Systems” IEEE VLSI-DAT April 2022
43. “Asynchronous SAR ADC: Past, Present and Beyond,” IEEE Swiss Chapter, May 2022
44. “New Opportunities in Nonuniform Sampling,” IEEE Penang Chapter, July 2022
45. “Trend in Digital PLL Design and New Opportunities in Spur Cancellation,” IEEE Southern Alberta Chapter, Sep. 2022
46. “High-Performance Digital-to-Analog Converter Design: A Path towards Digital Transmitter,” IEEE Egypt Chapter Nov. 2022
47. “New Opportunities in Nonuniform Sampling,” IEEE Taipei Chapter, Dec. 2022
48. “Trend in Digital PLL Design and New Opportunities in Spur Cancellation,” IEEE Tainan Chapter, Dec. 2022

PROFESSIONAL SERVICES

Review Panel:

1. IEEE SSCS James D. Meindl Innovators Award
2. NSF Panelist
3. Samsung Research

Journal article review:

1. IEEE Journal of Solid-State Circuits
2. IEEE Solid-State Circuits Letters (SSC-L)
3. IEEE Transactions on Signal Processing
4. IEEE Transactions on Communications
5. IEEE Transactions on Circuits and Systems I
6. IEEE Transactions on Circuits and Systems II
7. IEEE Transactions on Vehicular Technology
8. IEEE Communications Letters
9. Journal of VLSI Signal Processing Systems

USC Department Services:

1. Munishian Series Committee
2. EFC
3. EE Festival reviewer

Conference TPC:

IEEE European Conference on Solid-State Circuits (ESSCIRC) (2022- present)
IEEE International Solid State Circuits Conference (ISSCC) (2018 - present)
IEEE Symposium on VLSI Circuits (VLSIC) (2017 - 2020)
IEEE Custom Integrated Circuits Conference (CICC) (2015 - 2019)
IEEE GlobalSIP (2014)

Organized/Participated Panel/Forum/Workshops for SSCS:

1. Forum: “Emerging Design Techniques for Data Converters” served as organizer at CICC 2017
2. Panel: “What can/should Circuit Designers do to Ride on the Wave of Machine Learning?” served as co-organizer and moderator at CICC 2018
3. Panel: “How can hardware designers reclaim the spotlight?” served as co-organizer and moderator at ISSCC 2019
4. Panel: “Favorite circuit design and testing mistakes of starting engineers?” served as co-organizer at ISSCC 2021
5. VLSI Symposia Mentoring Event June 2021
6. Panel: “How to choose career path, academia, industry, startups?” served as panelist at CICC 2022 (to appear)
7. Panel: “Open Source Systems, Circuits, and Design: Is It the Future?” served as panelist at CICC 2022 (to appear)

Associate Editor:

SSC-L, TCAS-II

Society Membership:

Senior Member of IEEE

CURRENT, PRIOR, AND PENDING RESEARCH GRANTS

Current Research Grants

Proposal Title: SpecEES: Switched-Capacitor Radiofrequency Signal Processing for Spectrally-Agile Low-Energy Wireless Transceivers
Source of Support: NSF: ECCS-1824442
Project Location: USC PI: Hossein Hashemi, Co-PI: Mike Chen
Total Award Amount: \$675,000 (Chen’s share: \$313,991)
Starting Date: 09/01/2018 Ending Date: 08/31/2023

Proposal Title: Bio-inspired hybrid computing platform for micro-unmanned vehicles

Source of Support: IARPA: 2021-21090200005
Project Location: USC PI: Wei Wu, Co-PIs: Mike Chen, Quan Nguyen
Total Award Amount: \$3,000,000 (Chen's share: \$1,100,000)
Starting Date: 09/27/2021 Ending Date: 10/26/2023

Proposal Title: High-Speed Multi-GS/s Time-based ADC
Source of Support: MediaTek Inc.
Project Location: USC PI: Mike Chen
Total Award Amount: \$160,000
Starting Date: 01/01/2022 Ending Date: 01/01/2024

Proposal Title: Center for Ubiquitous Connectivity (CUBiC)
Source of Support: Columbia University (Prime: SRC): 2023-JU-3132
Project Location: USC PI: Mike Chen
Total Award Amount: \$1,250,000
Starting Date: 01/01/2023 Ending Date: 12/31/2027

Proposal Title: High-Speed DAC with High Output Power and Linearity
Source of Support: University of Texas at Dallas (Prime: SRC): 2023-AM-3160
Project Location: USC PI: Mike Chen
Total Award Amount: \$270,000
Starting Date: 01/01/2023 Ending Date: 12/31/2025

Proposal Title: Machine-Learning Based Analog Mixed-signal Design Tool
Source of Support: University of Texas at Dallas (Prime: SRC): 2023-AM-3160
Project Location: USC PI: Mike Chen, Co-PIs: Sandeep Gupta, Anthony Levi
Total Award Amount: \$285,000 (Chen's share: \$259,568)
Starting Date: 01/01/2023 Ending Date: 12/31/2025

Proposal Title: Design Automation of Low Phase Noise PLL
Source of Support: University of Texas at Dallas (Prime: SRC): 2023-AM-3160
Project Location: USC PI: Mike Chen, Co-PIs: Sandeep Gupta, Anthony Levi
Total Award Amount: \$270,000 (Chen's share: \$244,568)
Starting Date: 01/01/2023 Ending Date: 12/31/2025

Prior Research Grants

Proposal Title: Techniques Estimating Reliability in COTS ICs (Phase 1)
Source of Support: DARPA: HR0011-11-C-0067 CLIN0001
Project Location: USC PI: Michael Fritze, Co-PI: Mike Chen
Total Award Amount: \$2,428,225 (Chen's share: \$299,153)
Starting Date: 07/21/2011 Ending Date: 03/07/2013

Proposal Title: Techniques Estimating Reliability in COTS ICs (Phase 2)
Source of Support: DARPA: HR0011-11-C-0067 CLIN0002
Project Location: USC PI: Michael Fritze, Co-PI: Mike Chen
Total Award Amount: \$1,787,093 (Chen's share: \$47,783)
Starting Date: 02/20/2013 Ending Date: 09/20/2014

Proposal Title: Silicon-Based Monolithic Digital RF Memory
Source of Support: ONR: N00014-11-1-0819
Project Location: USC PI: Hossein Hashemi, Co-PI: Mike Chen
Total Award Amount: \$1,200,000 (Chen's share: \$600,000)
Starting Date: 08/01/2011 Ending Date: 09/30/2015

Proposal Title: Multi-Tier Reconfigurable Transceivers for Hand-Portable Radio and
Micro Base Stations
Source of Support: DARPA: HR0011-12-C-0094
Project Location: USC PI: Hossein Hashemi, Co-PI: Mike Chen
Total Award Amount: \$3,257,252 (Chen's share: \$400,000)
Starting Date: 08/20/2012 Ending Date: 07/15/2017

Proposal Title: Computational Leverage Against Surveillance Systems (CLASS)
Source of Support: Itt Exelis (Prime: DARPA): 473685J
Project Location: USC PI: Mike Chen
Total Award Amount: \$287,125
Starting Date: 06/12/2013 Ending Date: 12/22/2014

Proposal Title: Design of Integrated Circuit for Intravascular Radial Arrays
Source of Support: Texas Instruments Inc.
Project Location: PI: K. Kirk Shung, Co-PI: Mike Chen
Total Award Amount: \$150,000 (Chen's share: \$29,332)
Starting Date: 02/01/2014 Ending Date: 01/31/2015

Proposal Title: Dual-Channel UWB Impulse-Based Interconnect Towards Large-Scale
Plastic Neural Network
Source of Support: DARPA YFA (SPANAVWAR): N66001-14-1-4049
Project Location: USC PI: Mike Chen
Total Award Amount: \$500,000
Starting Date: 09/04/2014 Ending Date: 09/03/2017

Proposal Title: Computational Leverage Against Surveillance Systems (CLASS) Phase 2
Source of Support: NexGen (Prime: DARPA): 004897-00001
Project Location: USC PI: Mike Chen

Total Award Amount: \$450,000
Starting Date: 10/01/2014 Ending Date: 03/31/2016

Proposal Title: R2 Transceiver Integration
Source of Support: Google: R2-USC-01
Project Location: USC PI: Mike Chen
Total Award Amount: \$800,000
Starting Date: 04/23/2015 Ending Date: 03/31/2016

Proposal Title: R2 2.0 Transceiver Integration - 2016 (Statement of Work #R2-USC-02)
Source of Support: Google: 349783
Project Location: USC PI: Mike Chen
Total Award Amount: \$600,000
Starting Date: 04/01/2016 Ending Date: 12/31/2016

Proposal Title: Wideband High-Dynamic Arbitrary Signal Generator for Electronic Warfare Integrated Systems Research
Source of Support: ONR (DURIP): N00014-15-1-2817
Project Location: USC PI: Hossein Hashemi, Co-PI: Mike Chen
Total Award Amount: \$189,500
Starting Date: 09/29/2015 Ending Date: 09/27/2017

Proposal Title: Calibration and Characterization of High-Speed Data Converter and Clock Generator
Source of Support: ONR: N00014-15-1-2864
Project Location: USC PI: Hossein Hashemi, Co-PI: Mike Chen
Total Award Amount: \$150,000 (Chen's share: \$100,383)
Starting Date: 09/30/2015 Ending Date: 06/30/2016

Proposal Title: Support for April 2017 Connectivity CDF
Source of Support: Airbus: SWLA00034
Project Location: USC PI: Mike Chen
Total Award Amount: \$20,000
Starting Date: 04/26/2017 Ending Date: 05/31/2017

Proposal Title: CAREER: Asynchronous Analog-to-Digital Converters with Non-Uniform Discrete-Time Signal Processing
Source of Support: NSF: ECCS-1351956
Project Location: USC PI: Mike Chen
Total Award Amount: \$400,000
Starting Date: 02/15/2014 Ending Date: 01/31/2020

Proposal Title: EARS: Enabling Opportunistic Environmental Monitoring with Non-Uniform Sampling and Processing Circuits
Source of Support: NSF: ECCS-1643004
Project Location: USC PI: Mike Chen, Co-PIs: Mahta Moghaddam, Keith Chugg
Total Award Amount: \$899,998 (Chen's share: \$300,000)
Starting Date: 10/01/2016 Ending Date: 09/30/2021

Proposal Title: Automated Analog Mixed-Signals (AMS) Intellectual Property Generator for Complementary Metal Oxide Semiconductor (CMOS) Technologies
Source of Support: DARPA (account managed by AFRL): FA8650-18-2-7853
Project Location: USC PI: Anthony Levi, Co-PIs: Mike Chen, Sandeep Gupta, Wes Hanford
Total Award Amount: \$6,028,731 (Chen's share: \$1,930,468)
Starting Date: 06/25/2018 Ending Date: 12/30/2022

Proposal Title: Discrete-time mm-wave Processors for Scalable Digital Arrays
Source of Support: DARPA (account managed by AFRL): FA8650-19-1-7996
Project Location: USC PI: Hossein Hashemi, Co-PI: Mike Chen
Total Award Amount: \$1,200,000 (Chen's share: \$600,000)
Starting Date: 10/09/2018 Ending Date: 01/10/2023

Pending Research Grants

Proposal Title: CMOS Integrated Warm Electronics for Large Format Far Infrared Detectors
Source of Support: Jet Propulsion Laboratory (Prime: NASA)
Project Location: USC PI: Mike Chen
Total Award Amount: \$393,294
Starting Date: 10/01/2023 Ending Date: 09/30/2026

Proposal Title: SHF: Medium: Transistors to Algorithm Hardware Acceleration of Boolean Satisfiability (SAT) and NP Complete Problems
Source of Support: NSF
Project Location: USC PI: Sandeep Gupta, Co-PIs: Pierluigi Nuzzo, Mike Chen, Tony Levi
Total Award Amount: \$1,199,994 (Chen's share: \$259,544)
Starting Date: 10/01/2023 Ending Date: 09/30/2026

Proposal Title: ACED Fab: 3D memristor/CMOS Hybrid Field-programmable Analog Arrays for Signal Processing from RF to Baseband
Source of Support: NSF
Project Location: USC PI: Mike Chen, Co-PIs: Joshua Yang, Qiangfei Xia
Total Award Amount: \$600,000 (Chen's share: \$420,000)
Starting Date: 07/01/2023 Ending Date: 06/30/2026

Mike Shuo-Wei Chen

Proposal Title: EFRI BRAID: Efficient learning in strongly-biased memristor-based
neural architectures
Source of Support: NSF
Project Location: USC PI: Bartlett Mel, Co-PIs: Joshua Yang, Mike Chen, Greg Ver Steeg
Total Award Amount: \$1,996,702 (Chen's share: \$94,202)
Starting Date: 08/16/2023 Ending Date: 08/15/2027