

Patent No. 7,564,665
Petition For *Inter Partes* Review

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APTIV SERVICES US, LLC
Petitioner,

v.

MICROCHIP TECHNOLOGY, INC.
Patent Owner.

Patent No. 7,564,665

Case No. IPR2024-00803

PETITION FOR *INTER PARTES* REVIEW

UNDER 35 U.S.C. §§ 311–319 AND 37 C.F.R. § 42.100 *et seq.*

TABLE OF CONTENTS

	Page
I. INTRODUCTION	1
II. THE STATE OF THE ART	2
III. THE '665 PATENT	3
A. Summary	3
B. Effective Filing Date	7
C. Prosecution History of the '665 Patent	7
D. Level of Ordinary Skill	10
IV. CLAIM CONSTRUCTION	10
V. PRECISE REASONS FOR RELIEF REQUESTED	10
A. Ground 1 — Obviousness based on Verhaege.....	11
1. Summary of Verhaege	11
2. Analysis.....	12
B. Ground 2 – Obviousness Based on Verhaege in View of Miller.....	47
1. Summary of Miller.....	47
2. The Combination.....	48
3. Analysis.....	49
C. Ground 3 – Obviousness Based on Ker	59
1. Summary of Ker.....	59
2. Analysis.....	60
VI. NOTICES AND STATEMENTS.....	96

Exhibit List for *Inter Partes* Review of U.S. Patent No. 7,564,665

Exhibit Description	Exhibit #
U.S. Patent No. 7,564,665 to Holly et al.	1001
Declaration of Dr. Mike Shuo-Wei Chen	1002
Prosecution History of U.S. Patent No. 7,564,665	1003
U.S. Pat. No. 6,529,359 to Verhaege et al.	1004
U.S. Pat. No. 6,249,410 to Ker et al.	1005
U.S. Pat. No. 7,589,945 to Miller et al.	1006
Microchip's Infringement Contentions — Redacted and Excerpted	1007
U.S. Patent No. 5,168,178 to Allen et al.	1008
U.S. Patent Publication No. 2007/0019345 to Loh et al.	1009
U.S. Patent Publication No. 2006/0001448 to Seo et al.	1010
U.S. Patent No. 7,102,862 to Lien et al.	1011

Petitioner Aptiv Services US, LLC (“Petitioner”) respectfully petitions for *inter partes* review of all claims of U.S. Patent No. 7,564,665 (“the ’665 patent” (Ex. 1001)) in accordance with 35 U.S.C. §§ 311–319 and 37 C.F.R. § 42.100 *et seq.*

I. INTRODUCTION

The ’665 patent is directed to a circuit for protection against electrostatic discharge (“ESD”), i.e., the sudden flow of electricity between differently-charged objects. The circuit of the ’665 patent connects input/output (“I/O”) pads to a voltage rail during an ESD event, which “may allow the capacitance of each pad, in some cases approximately 3pF capacitance per pad, to charge up, absorbing the energy of the ESD event and reducing the peak voltage the integrated circuit or part experiences as a result of the ESD event.” (EX-1001, Abstract.) In addition, the ESD energy may be shunted to a voltage rail via an ESD clamp. (EX-1001, 2:51-2:53.) But none of this was inventive. As explained below, U.S. Patent No. 6,529,359 to Verhaege (EX-1004) and U.S. Patent No. US 6,249,410 to Ker (EX-1005) include ESD clamps and connect the I/O pad to a voltage rail during an ESD event, allowing capacitive charging of other pads in the system.

Moreover, a POSITA would have been motivated to combine Verhaege with U.S. Pat. No. 7,589,945 to Miller. Miller teaches a high-level scheme for ESD protection wherein multiple pad-level ESD protection circuits are triggered

simultaneously, distributing the ESD charge across multiple pad circuits. This would have reinforced to a POSITA that the Verhaege and Ker circuits could share ESD charge between pad circuits, allowing capacitive charging.

Petitioner thus respectfully submits the challenged claims are unpatentable for the reasons set forth in this Petition. This Petition is supported by the Declaration of Dr. Mike Shuo-Wei Chen (Ex. 1002).

II. THE STATE OF THE ART

By 2007 (the earliest purported priority date of the '665 patent), ESD was a well-known problem in the art of integrated circuit design. (EX-1002 ¶ 28; see e.g., EX-1005.) As Ker explained about a decade earlier, ESD is “one of the main reliability concerns” for integrated circuits because it can subject a low-voltage circuit to thousands of volts of electricity. (EX-1005, 1:13-1:14, 1:20-1:24.) Thus, it was standard practice to include circuitry to protect sensitive components from high voltage. (EX-1002 ¶ 31.) These circuits were often located near an I/O pad, where ESD events are most likely to originate, to improve their efficacy. (EX-1002 ¶¶ 38-39.)

The prior art discloses a wide variety of protective circuits for this purpose. In general, these protective circuits (1) shunt excess ESD voltage to ground; (2) absorb the ESD energy; and/or (3) use capacitance to mitigate the impact on the circuit. (EX-1005, 12:9-12:11, 12:20-12:26, 12:39-12:56, 14:42-14:47; EX-1006,

1:16-1:20; EX-1004, 3:56-3:66, 4:14-4:20.) Circuit designers discovered that such protective circuits were most effective when placed near the source of the ESD event (i.e., the I/O pad). (EX-1002 ¶ 39.) Because any pad could be subjected to an ESD event, it was standard practice to include an ESD protection circuit at every I/O pad. (EX-1002 ¶ 39.)

Subsequent improvements—still before 2007—sought to reduce the strain on any one protective circuit by distributing the ESD energy across multiple I/O pad circuits. (E.g., EX-1006.) After all, if ESD protection devices are included at every I/O pad, there is plenty of protective circuitry to utilize. Connecting multiple protective circuits allowed engineers to use smaller, less expensive components while improving ESD protection. (*See* EX-1006, 2:44-2:52. EX-1002 ¶ 41.)

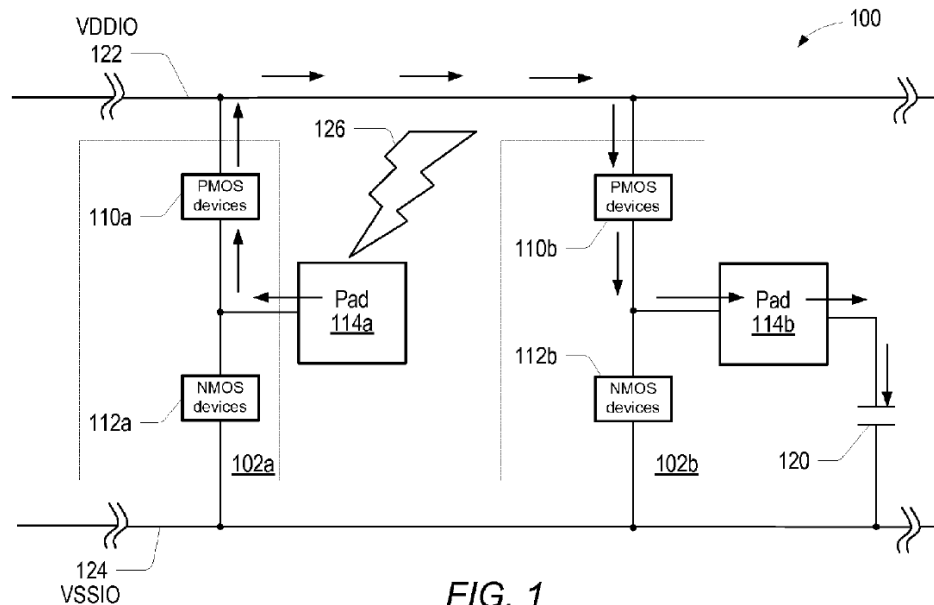
III. THE '665 PATENT

A. Summary

The application that matured into the '665 patent was filed on January 10, 2007. It issued with 18 claims, including independent claims 1, 6, and 14. The independent claims are largely similar, with claim 1 concerning a pad circuit, claim 6 concerning a circuit connected to a pad, and claim 14 concerning a system comprising a circuit and pad. (EX-1001, Claims 1, 6, 14.)

The purported innovation of the '665 patent is to use the capacitance of one or more I/O pads to store energy during an ESD event, thereby reducing the

maximum voltage developed in the system. (EX-1001, Abstract.) The patent only describes the circuitry for achieving this functionality—not an improvement to the pads themselves.¹ During an ESD event, PMOS devices may connect the I/O pads to the Vdd rail. This allows ESD energy to flow from the source of the ESD event to other pads in the system, charging their capacitance. Figure 1 of the '665 patent, reproduced below, shows a partial block diagram of one embodiment. (EX-1001, 3:11-3:15.)

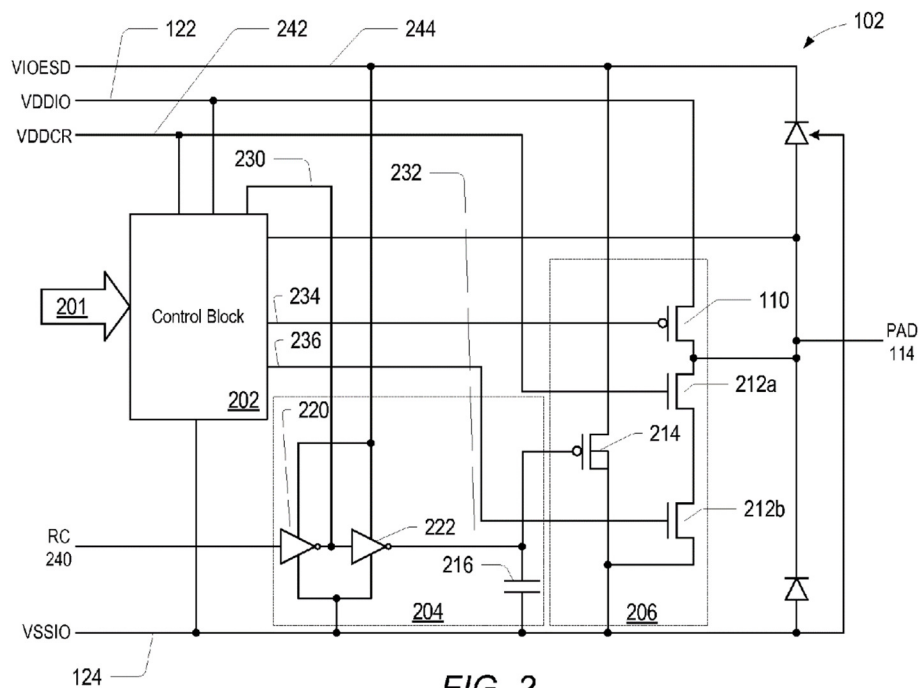


(EX-1001 Figure 1)

¹ All I/O pads have inherent capacitance based on being physical, conductive components in proximity to other conductive components and/or substrate, and the claims do not require any particular amount. (EX-1002 ¶ 44, EX-1001.)

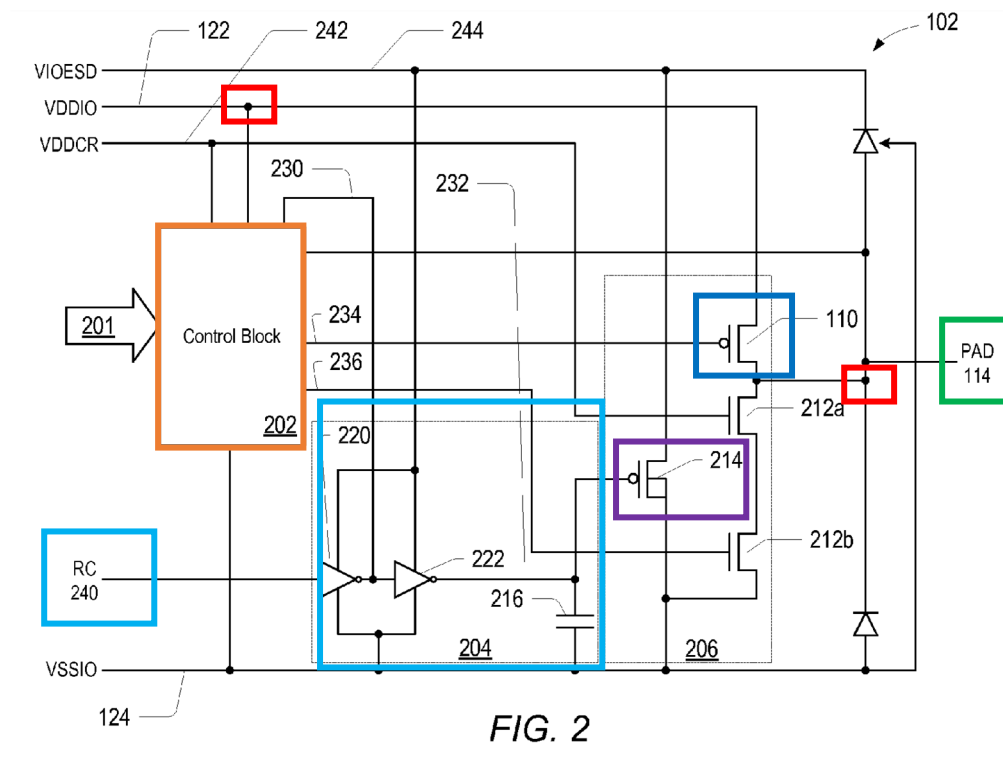
ESD event 126 occurs at I/O pad 114a as shown above. (*Id.*, 4:7-4:9.) In response, pad circuit 102a turns on PMOS devices 110a, allowing energy to flow to VDDIO rail 122. (*Id.*, 4:7-4:13.) Meanwhile, PMOS devices 110b are activated, allowing the charge to flow from the rail to I/O pad 114b. (*Id.*) Because I/O pad 114b has capacitance (signified by capacitor 120), I/O pad 114b may charge and store some amount of ESD energy. (*Id.*, 3:67-4:2, 3:7-3:13.)

Moreover, Figure 2 (below) of the '665 patent provides an exemplary electrical schematic for circuit 102a or circuit 102b in Figure 1.



(EX-1001, Figure 2.)

Many of the claims of the '665 patent are directed to the configuration of various components, including nodes, a control block, enable circuitry, a clamp device, an output transistor, and an I/O pad, as exemplarily shown in Figure 2. For reference, these components are identified in the annotated figure below.



(EX-1001, Figure 2 (annotated).)

Component	Color	
First and second nodes	Red	
Control block	Orange	
Enable circuitry	Light Blue	
Clamp device	Purple	
Output transistor	Dark Blue	
I/O pad	Green	

B. Effective Filing Date

As discussed above, the '665 patent was granted based on application No. 11/621,724, filed on January 10, 2007. Petitioner assumes—for this Petition only—that the challenged claims are entitled to a priority date of January 10, 2007.

C. Prosecution History of the '665 Patent

Office Action 1 / Response 1. On April 4, 2008, the Examiner rejected original claims 1-3, 5-16, 19-23, and 25-27 under 35 U.S.C. 103(a) based on combinations of U.S. Patent No. 5,168,178 (“Allen”) (EX-1008), U.S. Patent Publication No. 2007/0019345 (“Loh”) (EX-1009), U.S. Patent Publication No. 2006/0001448 (“Seo”) (EX-1010), and U.S. Patent No. 7,102,862 (“Lien”) (EX-1011) in a non-final Office Action. (EX-1003, 51-58.) The Examiner objected to claims 4, 17, 18, and 24 as being dependent upon rejected claims, but indicated that they would be allowable if rewritten in independent form. (*Id.*, 58-59.) The Examiner highlighted the “clamp device” and enabling circuitry of these dependent claims as the patentable feature. (*Id.*)

In response, Applicants argued that Allen and Loh were deficient because “Loh is not adapted to turn on at least one of the one or more output transistor devices . . . to charge the pad capacitance.” (EX-1003, 89.)

Office Action 2 / Response 2. In a final Office Action dated November 13, 2008, the Examiner stood firm. The Examiner stated that “[t]he circuit of Allen

demonstrates that a capacitance is available to an inverter circuit . . . comprising a pad when the core circuitry is providing an output to a load that is external to the core circuitry.” (EX-1003, 99.)

In response, Applicants amended claim 1 to include the features of allowable claim 4 and intervening claim 3. The added features included:

- a clamp device configured between a second voltage rail and a third voltage rail to reduce, when turned on, the maximum voltage developed in the system as the result of the ESD event;

- enable circuitry configured to turn on the clamp device and instruct the control block to turn on the at least one of the one or more output transistor devices, in response to the ESD event;

- wherein the second voltage rail is configured to provide power to the enable circuitry, and wherein the third voltage rail has a value below the first voltage rail.

Similarly, Applicants amended claim 13 to include the features of allowable claim 17. The added features included:

- a clamp device coupled between a first supply rail configured to provide power to the control circuit, and a low supply rail, wherein the clamp device is configured to absorb, when turned on, a portion of an energy generated by the ESD event, to reduce the maximum voltage developed in the system as the result of the ESD event;

- wherein the control circuit is further configured to turn on the clamp device in response to the ESD event.”

Likewise, Applicants amended claim 22 to include the allowable features of claim 24:

- a respective clamp device configured to absorb, when turned on, a portion of an energy generated by the ESD event, to thereby

further reduce the maximum voltage developed in the system as the result of the ESD event;

[respective control circuitry operable to] turn on the clamp device in response to the ESD event.

(EX-1003, 111-116.)

Applicants attempted to place independent method claim 8 in condition for allowance. But the Examiner issued an Advisory Action, stating that “Claim 8 has been amended to include the limitation ‘asserting a control signal in response to an ESD event’ which was not previously found in Claim 8 or any dependent claims thereof and would therefore require further consideration.” (EX-1003, 124-125.)

Applicants responded by canceling claim 8 and dependent claims 9-12. (EX-1003, 128.)

Allowance and Issuance. On May 6, 2009, the Examiner issued a Notice of Allowance. (EX-1003, 139.) The Examiner made minor amendments to claims 2, 5, 6 13-16, 19, and 22 via an Examiner’s Amendment. In the Reasons for Allowance, the Examiner indicated that the features of original claims 4, 7, and 24—which Applicants had incorporated into independent claims 1, 13, and 22—rendered the claims allowable. The ’665 patent issued on July 21, 2009 with 18 claims.

D. Level of Ordinary Skill

A person of ordinary skill in the art (“POSITA”) in the field of the ’665 patent in 2007 would have at least a Master’s degree in electrical engineering, computer engineering, or a related field and three to five years of experience in integrated circuit design. (EX-1002 ¶ 51.)

IV. CLAIM CONSTRUCTION

Petitioner has not proposed any terms for construction because no constructions are necessary to resolve any disputes identified in this Petition.

V. PRECISE REASONS FOR RELIEF REQUESTED

Pursuant to 37 C.F.R. § 42.104(b), Petitioner respectfully requests cancellation of all claims of the ’665 patent based on the following references:

Prior Art Reference	Abbreviation	Filing Date / Issue Date
U.S. Pat. No. 6,529,359 to Verhaege et al.	“Verhaege” (EX-1004)	Aug. 4, 2000 March 4, 2003
U.S. Pat. No. 6,249,410 to Ker et al.	“Ker” (EX-1005)	Aug. 23, 1999 June 19, 2001
U.S. Pat. No. 7,589,945 to Miller et al.	“Miller” (EX-1006)	Aug. 31, 2006 Sept. 15, 2009

The ’665 patent’s earliest purported filing date is January 10, 2007. Thus, Verhaege and Ker qualify as prior art under at least pre-AIA § 102(b), and Miller

qualifies as prior art under at least pre-AIA § 102(e) based on its filing date. None of the references was considered in the original examination. The statutory grounds for the challenge to each claim are set forth below.

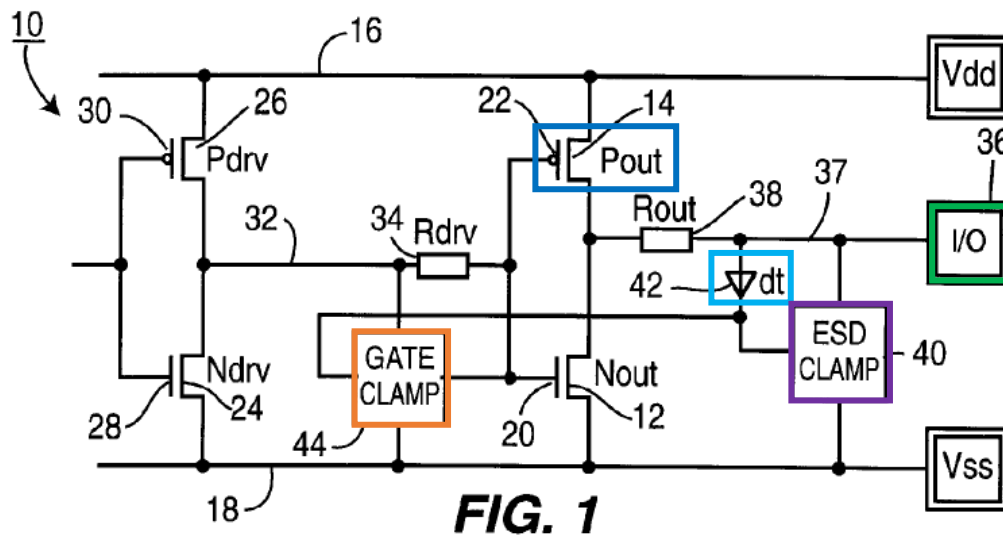
Ground	35 U.S.C. §	Claims	Prior Art References
1	103(a)	1-18	Verhaege
2	103(a)	1-18	Verhaege, Miller
3	103(a)	1-18	Ker

Below, Petitioner discusses why the challenged claims are unpatentable under the statutory grounds raised, including by specifying how and where the prior art satisfies each limitation of each challenged claim, as required by 37 C.F.R. § 42.104(b)(4). Petitioner’s showing establishes a reasonable likelihood that it will prevail on each ground of invalidity as to each challenged claim. Petitioner also provides the Declaration of Dr. Chen (Ex. 1002) to support its showing.

A. Ground 1 — Obviousness based on Verhaege

1. Summary of Verhaege

Verhaege discloses a circuit for protecting an output driver transistor from ESD stress or electrical overstress (“EOS”). (EX-1004, 1:9-1:13.)



(EX-1004, Figure 1 (annotated).)

When ESD stress is applied through I/O pad 36 (green), dynamic trigger device 42 (light blue) detects the stress and sends a signal to gate clamp 44 (orange) and ESD clamp 40 (purple). ESD clamp 40 diverts some ESD energy by connecting I/O pad 36 to the Vss rail. (*Id.*, 2:29-2:30, 2:37-2:39.) Meanwhile, gate clamp 44 grounds the gates of output driver transistors 12 and 14. (*Id.*, 2:32-2:34.) The grounding activates PMOS transistor 14, which allows ESD energy to flow to the Vdd rail. From there, the voltage charges the capacitance of the rail and any device connected to the rail. (EX-1002 ¶ 49.) This includes any I/O pads connected to the rail because, as a physical, conductive device, the pads have capacitance. (EX-1002 ¶ 44.)

2. Analysis

As set forth below, Verhaege renders the challenged claims obvious.

1) Claim 1

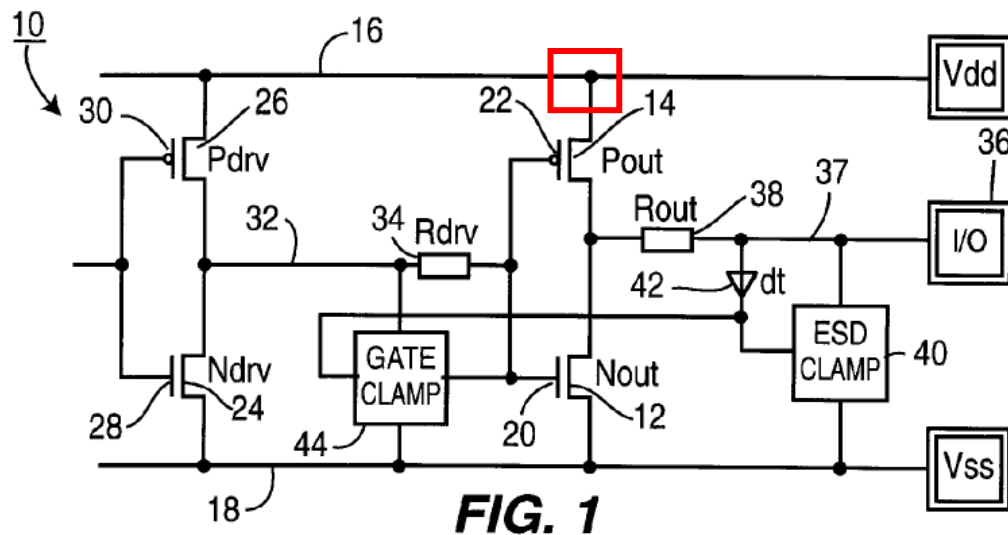
a. Preamble: “A pad circuit configured to provide protection against electrostatic discharge (ESD) in a system comprising the pad circuit,”

Verhaege discloses a circuit 10 comprising “[a]n I/O pad [that] is connected to the junction of the output driver transistors.” (EX-1004, Abstract.) Verhaege teaches that “[i]n the circuit 10, . . . ESD stress can be diverted to the parallel ESD clamp and the EOS/ESD capability is achieved.” (EX-1004, 2:35-2:39.) Thus, Verhaege discloses the preamble.²

b. [1a]: “the pad circuit comprising: a first node coupled to a first voltage rail;”

In Figure 1 (below), Verhaege discloses a first node coupled to a first voltage rail (red) where output driver PMOS transistor 14 meets the Vdd rail. (EX-1004, 1:66-2:3.)

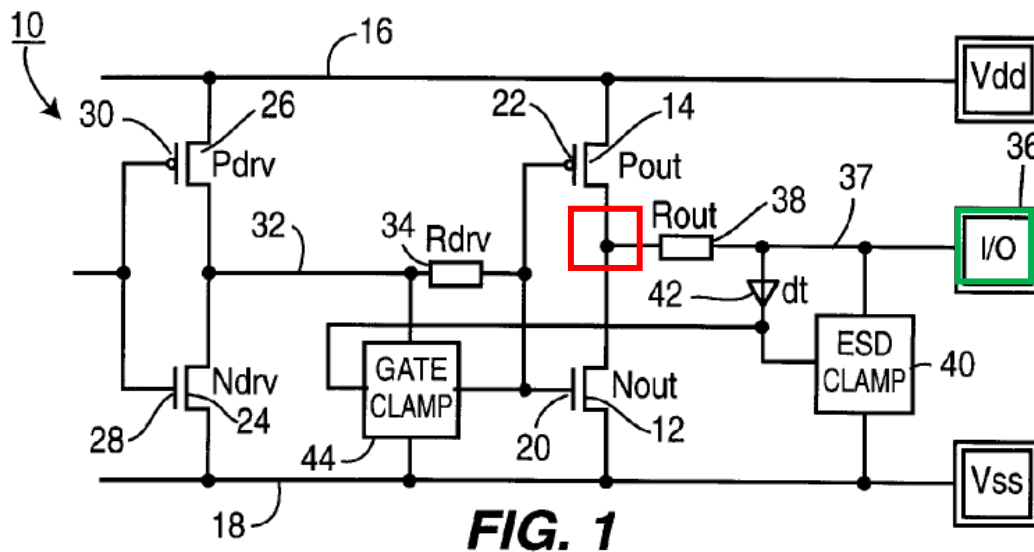
² Petitioner does not concede that the preamble of claim 1 or any other claim is limiting for the purposes of this Petition.



(EX-1004, Figure 1 (annotated).)

c. [1b]: “[the pad circuit comprising] a second node coupled to a physical pad having capacitance;”

In Verhaege’s circuit, “I/O pad 36 is electrically connected to the junction between the output driver NMOS transistor 12 and the output driver PMOS transistor 14 by line 37 and through an output resistor 38.” (EX-1004, 2:16-2:19.) The second node (red) is where PMOS transistor 14 connects to I/O pad 36 (green) through resistor 38.

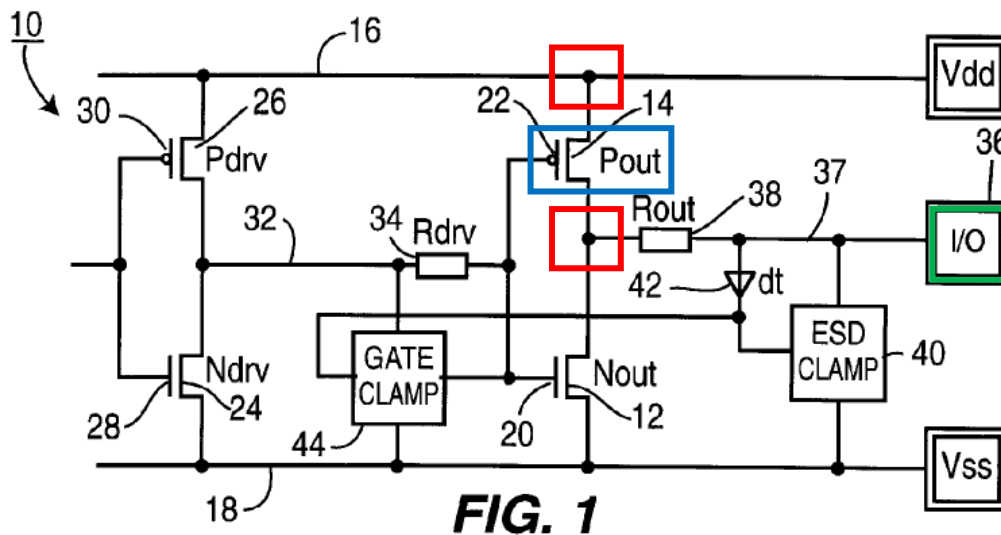


(EX-1004, Figure 1 (annotated).)

The second node is “coupled to a physical pad having capacitance” because I/O pad 36 is a physical, conductive device. It was well known in the art that physical, conductive devices have capacitance. (EX-1002 ¶ 61.)

d. [1c]: “[the pad circuit comprising:] one or more output transistor devices coupled between the first node and the second node, and operable to at least partially drive an output signal at the second node;”

Verhaege discloses an “output driver PMOS transistor 14” connected between the Vdd rail (first node) and the junction with resistor 38 (second node). (EX-1004, 1:66-2:2, 2:16-2:19.)



(EX-1004, Figure 1 (annotated).)

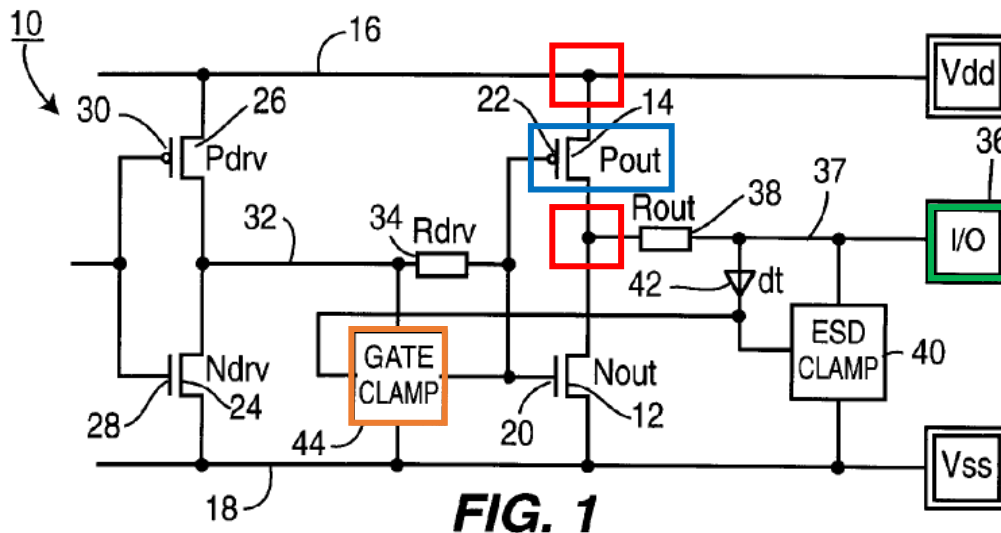
PMOS transistor 14 is “operable to at least partially drive an output signal at the second node” because it is “an output driver PMOS transistor.” (EX-1004, 1:66-2:2.) A POSITA would understand that the purpose of an output driver transistor is to drive a signal at an I/O pad. (EX-1002 ¶ 63.) In Verhaege’s circuit, transistors 12 and 14 receive a signal from pre-driver transistors 24 and 26. The signal activates one of the two transistors, creating a “high” or “low” output signal by connecting I/O pad 36 to either Vdd or Vss.

- e. [1d]: “a control block configured, to turn on, when instructed, at least one of the one or more output transistor devices to charge the pad capacitance to reduce a maximum voltage developed in the system as a result of the ESD event;”

According to the ’665 patent, a “control block” may contain “any digital, analog, and/or mixed mode circuitry configured to perform the functions assigned

to the control block.” (EX-1001, 4:43-4:46.) The function of the control block is to “turn on, when instructed, at least one of the one or more output transistor devices to charge the pad capacitance to reduce a maximum voltage developed in the system as a result of the ESD event.” (EX-1001, Claim 1.)

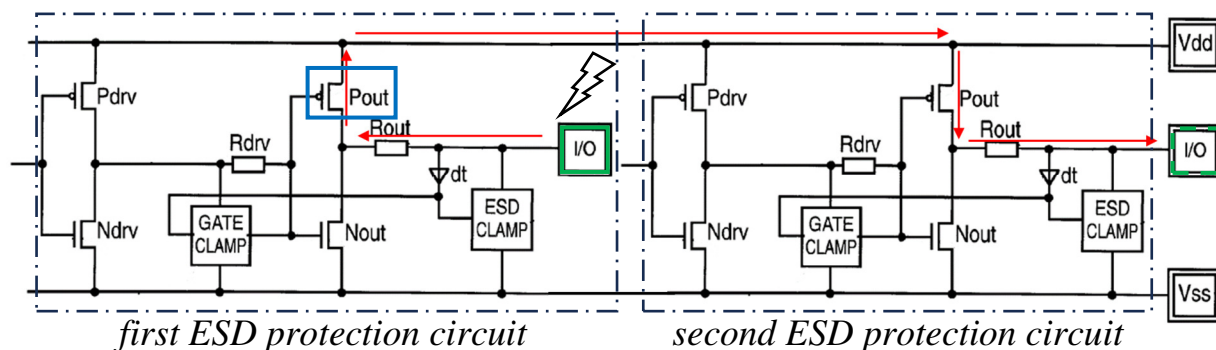
In Figure 1 of Verhaege, gate clamp 44 (orange) is connected to the gates of output transistor 12 and output transistor 14 (dark blue). (EX-1004, 2:23-2:25.) In response to an ESD event, gate clamp 44 connects the gates of both output transistors to ground, which turns off NMOS transistor 12 and turns on PMOS transistor 14. (EX-1004, 2:23-2:25, 2:32-2:37; EX-1002 ¶ 65.) Thus, gate clamp 44 is configured “to turn on, when instructed, at least one of the one or more output transistor devices” (i.e., PMOS transistor 14).



(EX-1004, Figure 1 (annotated).)

Verhaege renders obvious “charg[ing] the pad capacitance to reduce a maximum voltage developed in the system as a result of the ESD event.” Although Verhaege discloses a single pad circuit, most integrated circuits had multiple I/O pads by at least 2007. (EX-1002 ¶ 67.) It would have been obvious to a POSITA that, because an ESD event could occur at any I/O pad, the Verhaege invention should be repeated at every I/O pad. (EX-1002 ¶ 67.)

The annotated figure below shows the ESD protection circuit of Verhaege’s Figure 1 repeated for two I/O pads. When the PMOS transistor (dark blue) of the first circuit connects the first I/O pad (solid green) to the Vdd rail, the first I/O pad is electrically connected to all other pads currently connected to the Vdd rail. For example, the figure below shows a second circuit comprising a second I/O pad (dashed green) also connected to the Vdd rail. The ESD energy flows from the first I/O pad to the Vdd rail, increasing its voltage and charging the capacitance of the second I/O pad. Charging the capacitance of the second pad reduces the maximum voltage developed in the system. (EX-1002 ¶ 67.)



f. [1e]: “a clamp device configured between a second voltage rail and a third voltage rail to reduce, when turned on, the maximum voltage developed in the system as the result of the ESD event;”

At least under Microchip’s apparent interpretation of this limitation as evidenced by its infringement contentions, Verhaege discloses this limitation.³

Microchip’s apparent position is that the “first voltage rail” of claim [1a] and “second voltage rail” of claim [1e] can refer to the same voltage rail and/or be

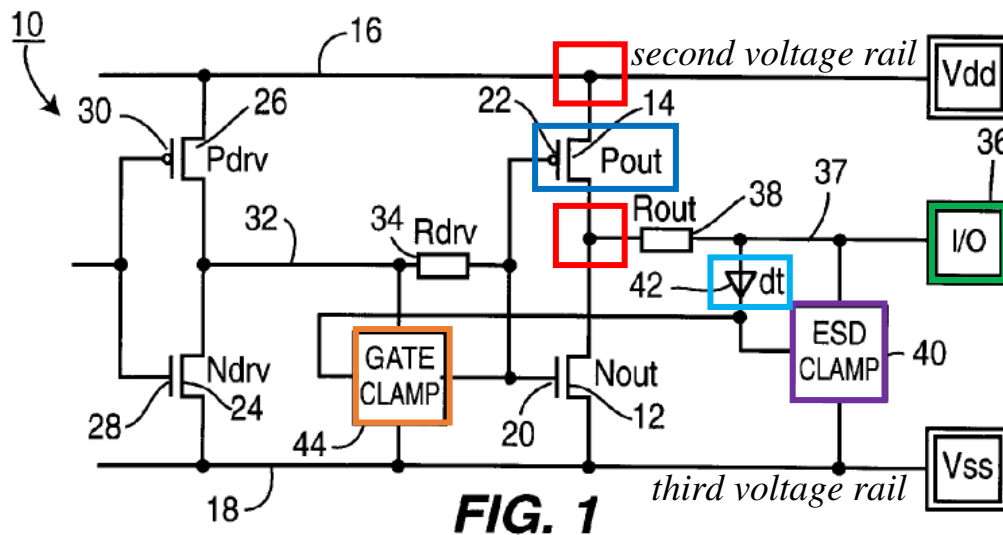
³ For some limitations, Aptiv will show why the challenged claims are unpatentable under Patent Owner’s expected claim constructions. The Board has repeatedly approved this approach. *See, e.g., 3Shape A/S v. Align Tech., Inc.*, Case IPR2020-00174, Paper 14, 11-12 (PTAB Jun. 12, 2020) (no requirement of “subjective belief of the correctness of the construction[s] asserted”); *Western Digital Corp. v. SPEX Techs., Inc.*, Case IPR2018-00084, Paper 14, 11 (PTAB Apr. 25, 2018) (an argument based on Patent Owner’s constructions in district court meets 37 C.F.R. § 104(b)(3)); *see also General Electric Co. v. Vestas Wind Systems A/S*, Case IPR2018-00928, Paper 9, 16 (PTAB Nov. 5, 2018) (petitioner can argue “more than one construction, including one that it believes is incorrect, such as patent owner’s”).

connected to each other. (EX-1007, 11.)⁴ Microchip does not represent that the clamp must be connected directly to both voltage rails to be “configured between” them. (EX-1007, 11.)⁵

Accordingly, Verhaege discloses a second voltage rail comprising the Vdd rail under Microchip’s understanding of the limitation. Verhaege’s Vss rail serves as a third voltage rail. Verhaege discloses ESD clamp 40 (purple) coupled between the Vdd and Vss rails.

⁴ Microchip cites EX-1001, 5:57-5:65: “[i]t should also be noted that VIOESD 244 [corresponding to the ‘second supply rail’ of claim 1] and VDDIO 122 [corresponding to the ‘first supply rail’ of claim 1] may in fact be the same power/supply rail” and “separate supply rails . . . may not be required.”

⁵ Microchip relies on a statement in the specification that “[t]he term ‘coupled’ means ‘directly or indirectly connected.’” (EX-1001, 3:36-3:37.)



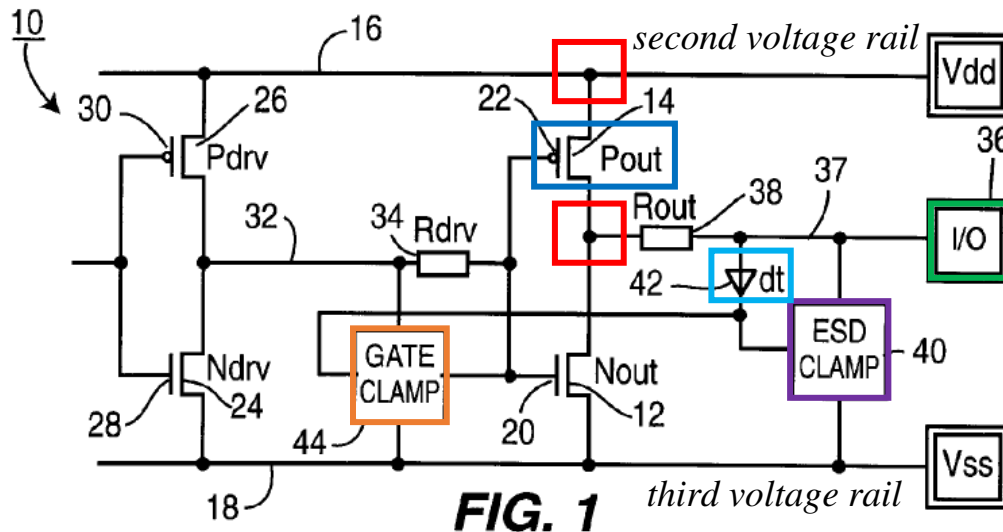
(EX-1004, Figure 1 (annotated).)

During an ESD event, dynamic trigger device 42 (light blue) activates ESD clamp 40. (EX-1004, 2:29-2:30.) ESD clamp 40 connects I/O pad 36 (green) to the Vss rail and reduces the maximum voltage developed in the system because “the ESD stress can be diverted to the parallel ESD clamp and the EOS/ESD capability is achieved.” (EX-1004, 2:37-2:39.)

g. [1f]: “enable circuitry configured to turn on the clamp device and instruct the control block to turn on the at least one of the one or more output transistor devices, in response to the ESD event;”

Verhaege discloses a “clamp device” in ESD clamp 40 and a “control block” in gate clamp 44, as discussed above. Verhaege further discloses enable circuitry to (1) turn on the clamp device and (2) instruct the control block to turn on the at least one or more output transistor devices.

Verhaege's Figure 1 shows enable circuitry comprising dynamic trigger device 42 (light blue). The input of dynamic trigger device 42 is connected to I/O pad 36 (green) where the ESD event originates. (*Id.*, 2:20-2:22.) "Dynamic trigger device 42 is used to trigger the ESD clamp 40." (*Id.*, 2:29-2:30.)



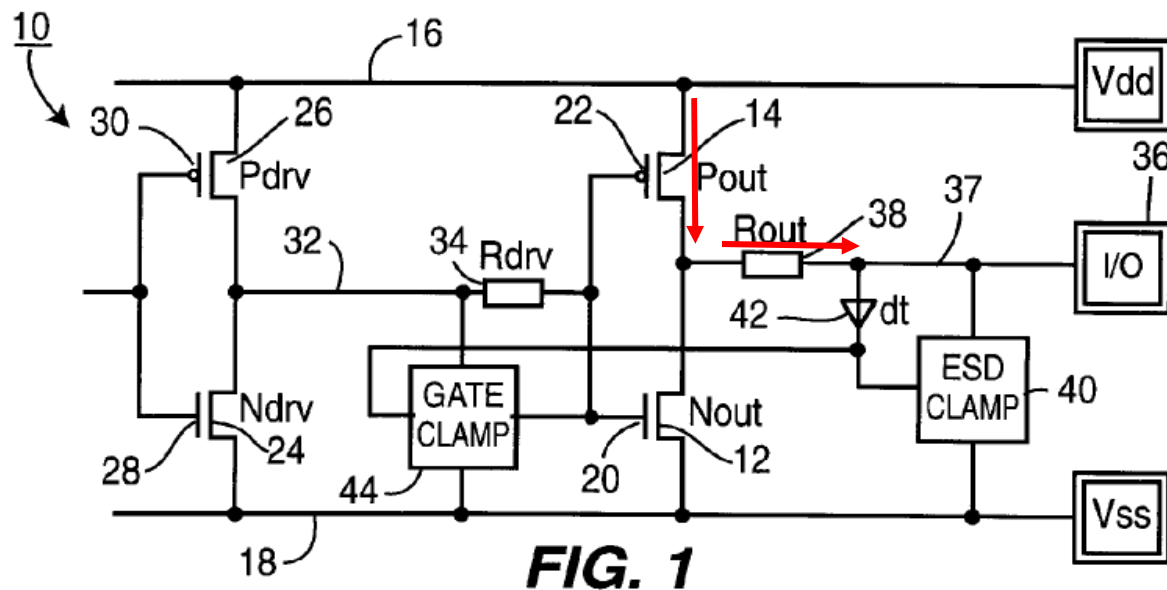
(EX-1004, Figure 1 (annotated).)

Dynamic trigger device 42 is also connected to the control block, i.e., gate clamp 44 (orange). Verhaege discloses that "gate clamp 44 grounds the gate 20 of the output driver NMOS transistor 12 under transient over voltage stress conditions." (*Id.*, 2:32-2:34.) A POSITA would understand that for gate clamp 44 to ground gate 20, dynamic trigger device 42 must "instruct" gate clamp 44. (*Id.*, 2:32-2:34, EX-1002 ¶ 73.) As discussed above, gate clamp 44 then "turn[s] on the at least one of the one or more output transistor devices," i.e., PMOS transistor 14 (dark blue), by grounding the gates of the output transistors. *Id.*

h. [1g]: “wherein the second voltage rail is configured to provide power to the enable circuitry, and wherein the third voltage rail has a value below the first voltage rail.”

At least under Microchip’s apparent interpretation of this limitation as evidenced by its infringement contentions, Verhaege discloses this limitation.

Verhaege discloses a “second voltage rail” in the Vdd rail and a “third voltage rail” in the Vss rail, as discussed above. Verhaege’s enable circuitry, dynamic trigger device 42, is powered by Vdd through PMOS transistor 14.



(EX-1004, Figure 1 (annotated).)

Microchip interprets “value” to refer to voltage. (EX-1007, 16.) Verhaege indicates that the “gate clamp 44 grounds the gate 20 of the output driver NMOS transistor 12 under transient over voltage stress conditions” by connecting it to Vss

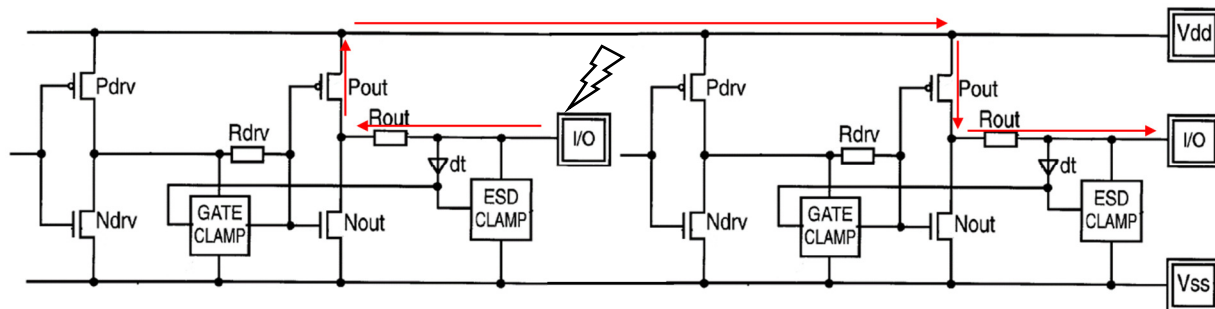
(EX-1004, 2:32-2:34, Figure 1.) Thus, a POSITA would understand that V_{ss} has a lower voltage than V_{dd} . (EX-1002 ¶ 76.)

2) Claim 2: “The pad circuit of claim 1, wherein in turning on the at least one of the one or more output transistor devices when instructed, the control block couples an associated capacitance of the first voltage rail to the physical pad to share a charge developed in the system in response to the ESD event, to reduce the maximum voltage developed in the system as the result of the ESD event.”

As discussed in claim [1d], Verhaege discloses a control block—gate clamp 44—connected to the gates of output transistors 12 and 14. During an ESD event, gate clamp 44 connects the gates of both output transistors to ground, which turns off NMOS transistor 12 and turns on PMOS transistor 14. (EX-1002 ¶¶ 65, 77.) By turning on PMOS transistor 14, gate clamp 44 couples an associated capacitance of the first voltage rail (i.e., V_{dd}) to the physical pad (i.e., I/O pad 36). The V_{dd} rail has an “associated capacitance” because it is a physical, conductive device. (EX-1002 ¶ 77.) When PMOS transistor 14 connects I/O pad 36 to the V_{dd} rail, the excess voltage from the ESD event charges the associated capacitance of the V_{dd} rail, thereby reducing the maximum voltage developed in the system as a result of the ESD event.

Even if “associated capacitance” refers to the capacitance of other pads connected to the rail, Verhaege renders the claim obvious. As discussed in claim

[1e], integrated circuit devices typically had multiple I/O pads by 2007. A POSITA would have understood that the ESD protection circuit disclosed in Verhaege would have been most effective if included at each I/O pad. (EX-1002 ¶ 78.) Thus, when I/O pad 36 is coupled to the Vdd rail, the associated capacitance of the Vdd rail will also include the sum of the capacitance of all I/O pads connected to the Vdd rail. (EX-1002 ¶ 78.) Distributing ESD energy to the Vdd rail and connected capacitive devices, as shown below, reduces the maximum voltage developed in the system by sharing a charge across a greater capacitance.



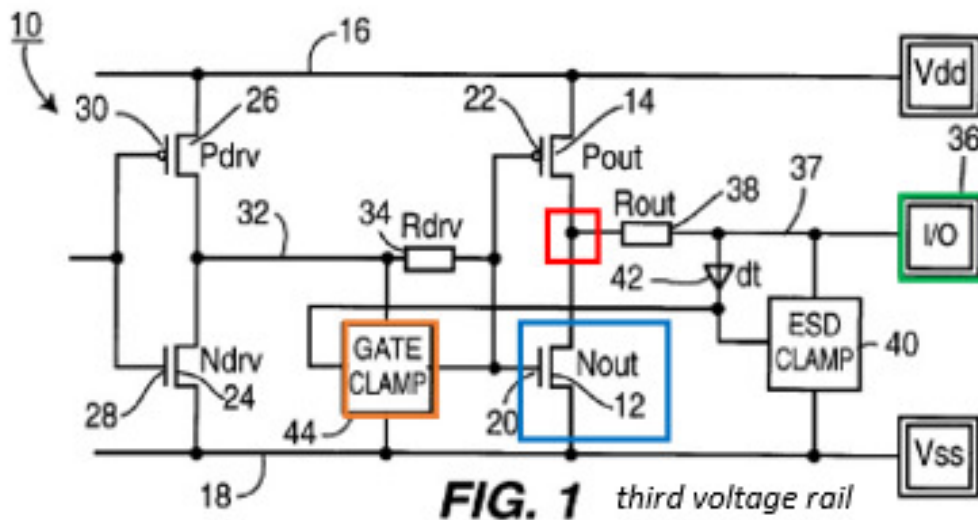
3) Claim 3: “The pad circuit of claim 1, wherein the one or more output transistor devices are PMOS devices.”

Verhaege discloses this claim because PMOS transistor 14 is a PMOS device. (EX-1004, 1:66-2:2.)

4) Claim 4: “The pad circuit of claim 3, further comprising one or more NMOS devices coupled between the second node and the third voltage rail, wherein the NMOS devices and the PMOS devices are operable to operate together to drive the output signal at the second node,

wherein the control block operates to turn off the NMOS devices during the ESD event.”

Verhaege discloses an NMOS output transistor 12 (blue) coupled between the second node (red) and the third voltage rail, Vss.



(EX-1004, Figure 1 (annotated).)

Together, transistors 12 and 14 operate to drive a signal at the I/O pad (green) by connecting it to Vdd or Vss during normal operation. During an ESD event, the control block—gate clamp 44 (orange)—grounds the gate of NMOS transistor 12, turning it off. (EX-1004, 2:32-2:36.)

5) Claim 5: “The pad circuit of claim 1, wherein the pad circuit and the physical pad are comprised in a digital input/output pad.”

Verhaege discloses a pad circuit (circuit 10 in Figure 1) and an associated physical pad (I/O pad 36). The pad is explicitly an input/output pad: “an I/O pad is connected to the junction between the output driver transistors.” (EX-1004, 1:38-1:39.) A POSITA would understand that the Verhaege invention is comprised in a digital input/output pad because pad 36 outputs a high or low signal, making it digital. (EX-1002 ¶ 82.)

6) Claim 6

a. Preamble: “A circuit configured to provide protection against electrostatic discharge (ESD) in a system comprising the circuit, the circuit comprising:”

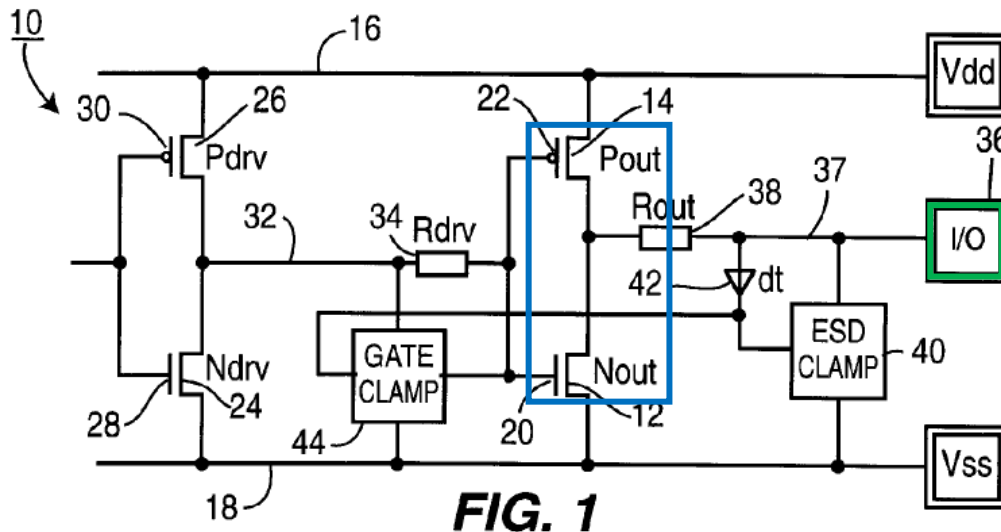
See discussion of claim 1, preamble.

b. [6a]: “an output buffer configured to couple to a physical pad having capacitance, to drive at least one output signal at the physical pad”

The '665 patent uses the term “output buffer” in the context of electrical circuits to denote signal driver circuits. (EX-1001, 4:27-4:33; EX-1002 ¶ 84.)

Verhaege discloses an output buffer comprising the output driver circuit (dark blue) comprising output driver NMOS transistor 12 and output driver PMOS transistor 14. (EX-1004, 2:26-2:28.) The output driver transistors are “configured to couple to a physical pad” because “an I/O pad is connected to the junction of the output driver transistors.” (*Id.*, Abstract.) Further, a POSITA would understand that

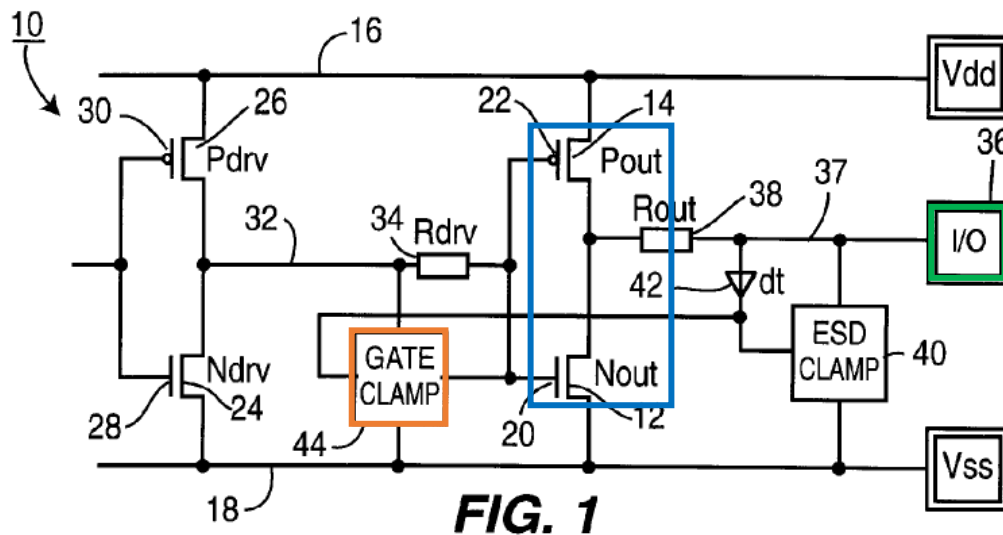
the I/O pad (green) is a physical, conductive device, and therefore has capacitance. (EX-1002 ¶ 85.) Finally, as discussed in claim [1c], the output driver transistors “drive at least one output signal at the physical pad” by connecting I/O pad 36 to either Vdd or Vss.



(EX-1004, Figure 1 (annotated).)

c. [6b]: “a control block configured to control the output buffer;”

In Figure 1, Verhaege teaches a control block comprising gate clamp 44 (orange) and an output buffer comprising the output driver circuit (dark blue) including output driver NMOS transistor 12 and output driver PMOS transistor 14. (EX-1004, 2:26-2:28.) In response to an ESD event, gate clamp 44 connects the gates of both transistors to ground, which turns off NMOS transistor 12 and turns on PMOS transistor 14. (EX-1004, 2:23-2:25, 2:32-2:37; EX-1002 ¶ 87.)

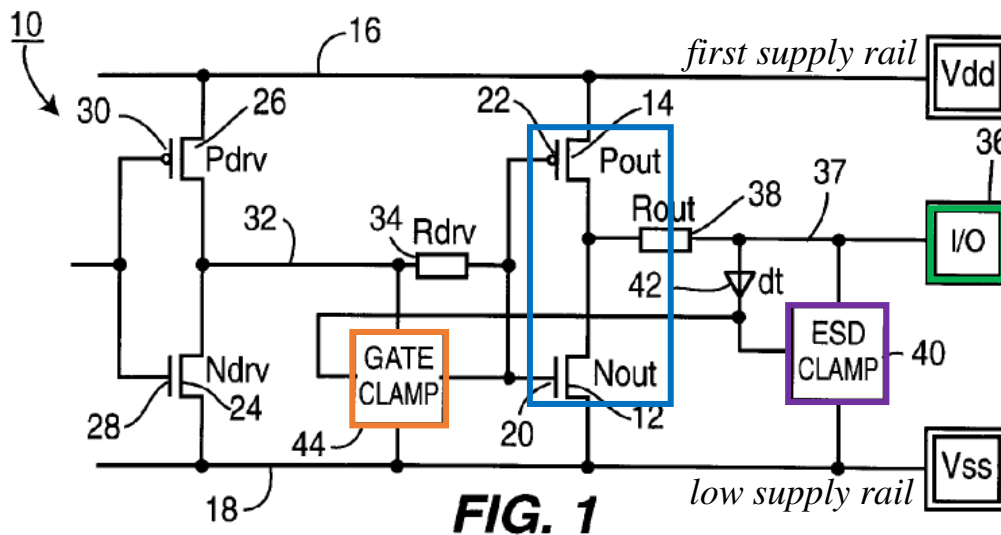


(EX-1004, Figure 1 (annotated).)

- d. [6c]: “a clamp device coupled between a first supply rail and a low supply rail, wherein the clamp device is configured to absorb, when turned on, a portion of an energy generated by the ESD event, to reduce the maximum voltage developed in the system as the result of the ESD event;”

At least under Microchip’s apparent interpretation of this limitation as evidenced by its infringement contentions, Verhaege discloses this limitation.

Verhaege discloses a first supply rail comprising the Vdd rail and a low supply rail comprising the Vss rail. Under Microchip’s apparent interpretation of the limitation, ESD clamp 40 (purple) is coupled between Vdd and Vss. (EX-1004, 2:19-2:20, Figure 1.) (EX-1007, 44-46.)

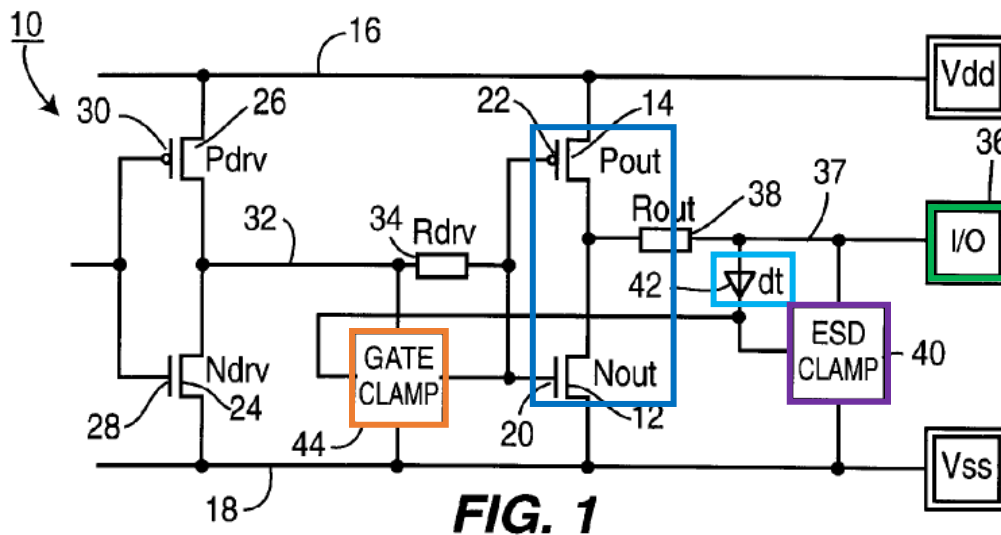


(EX-1004, Figure 1 (annotated).)

ESD clamp 40 connects I/O pad 36 to Vss during an ESD event. (EX-1004, 2:19-2:20, 2:29-2:30.) ESD clamp 40 is thus “configured to absorb, when turned on, a portion of an energy generated by the ESD event.” This reduces the maximum voltage developed in the system because “the ESD stress can be diverted to the parallel ESD clamp and the EOS/ESD capability is achieved.” (EX-1004, 2:37-2:39; EX-1002 ¶ 90.)

- e. [6d]: “and a control circuit configured to instruct the control block to activate at least a portion of the output buffer when an ESD event occurs,”

Verhaege discloses a control circuit comprising dynamic trigger device 42 (light blue) connected to the control block, i.e., gate clamp 44 (orange).



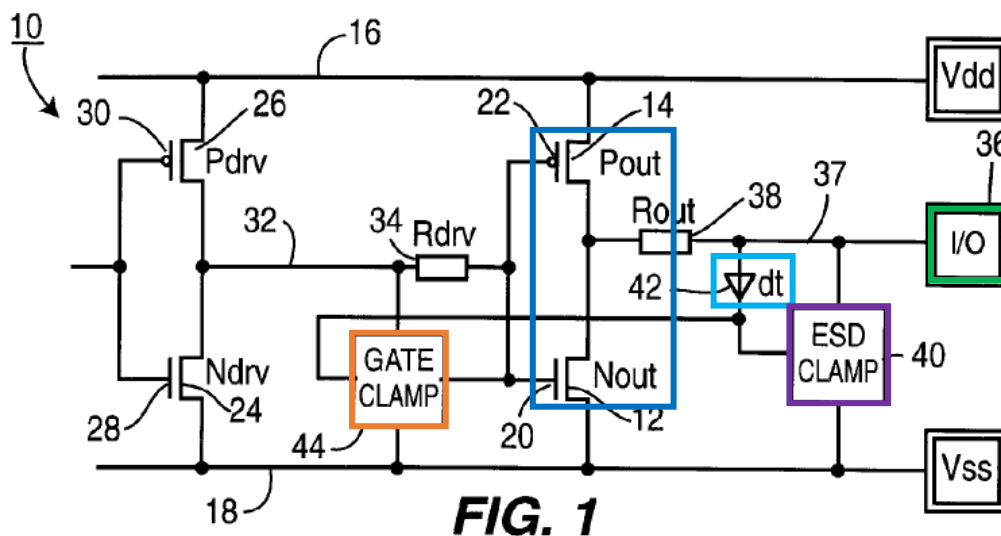
(EX-1004, Figure 1 (annotated).)

Verhaege discloses that “gate clamp 44 grounds the gate 20 of the output driver NMOS transistor 12 under transient over voltage stress conditions.” (*Id.*, 2:32-2:34.) A POSITA would understand that for gate clamp 44 to ground the gate 20, the dynamic trigger device 42 would *instruct* gate clamp 44 to do so. (EX-1002 ¶ 92.) As discussed above, the gate clamp 44 then activates at least a portion of the output buffer—PMOS transistor 14—when an ESD event occurs by grounding the gates of the output transistors (dark blue). (*Id.*)

- f. [6e]: “[the control circuit configured] to charge the pad capacitance to reduce a maximum voltage developed in the system as a result of the ESD event”**

As discussed above, a POSITA would repeat the Verhaege circuit at every I/O pad to protect the entire circuit from ESD. In Verhaege, the control circuit

(light blue) activates gate clamp 44 (orange) during an ESD event. (See discussion of claim [6d].) In turn, gate clamp 44 activates PMOS transistor 14, thereby connecting I/O pad 36 (green) to Vdd. The ESD energy flows to the Vdd rail and charges the capacitance of any connected I/O pads, thereby reducing the maximum voltage developed in the system due to the ESD event. (EX-1002 ¶ 94.)



(EX-1004, Figure 1 (annotated).)

g. [6f]: “wherein the control circuit is further configured to turn on the clamp device in response to the ESD event;”

Verhaege discloses that the control circuit—dynamic trigger device 42—is further configured to turn on the clamp device in response to the ESD event because “dynamic trigger device 42 is used to trigger the ESD clamp 40.” (EX-1004, 2:29-2:31.)

h. [6g]: “wherein the first supply rail is configured to provide power to the control circuit”

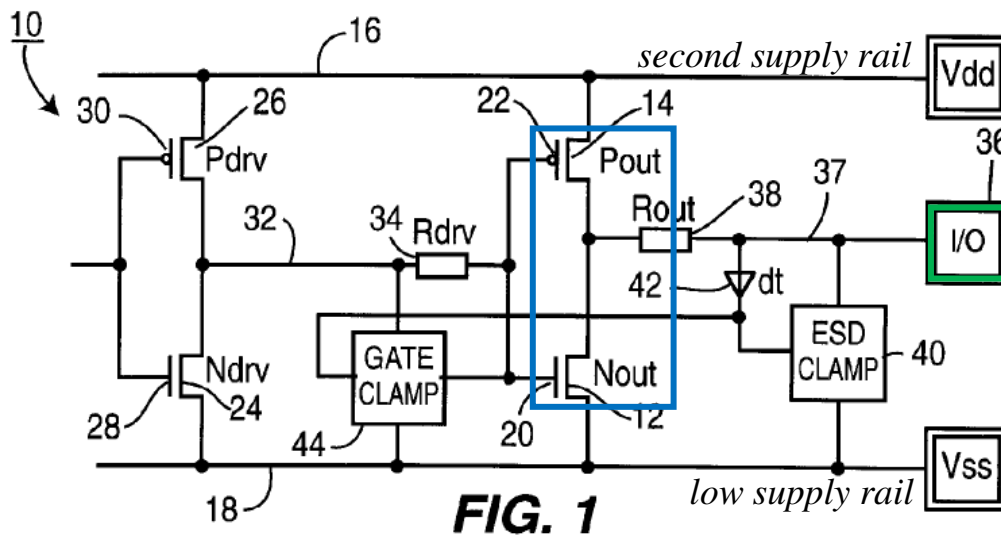
As discussed above in claim [6c], Verhaege’s first supply rail is Vdd. The Vdd rail provides power to the control circuit—dynamic trigger device 42—through PMOS transistor 14. (EX-1002 ¶ 96.)

7) Claim 7:

a. [7a]: “The circuit of claim 6, wherein the output buffer comprises one or more PMOS devices coupled between a second supply rail and the physical pad; and”

At least under Microchip’s apparent interpretation, wherein the first and second supply rail can be the same rail (EX-1007, 52, 67), Verhaege discloses this limitation.

Verhaege discloses an output buffer (dark blue) comprising NMOS transistor 12 and PMOS transistor 14. PMOS transistor 14 is connected to a second supply rail, Vdd, and is electrically connected to I/O pad 36 (green) “by a line 37 and through an output resistor 38.” (EX-1004, 1:66-2:3, 2:16-2:19.)



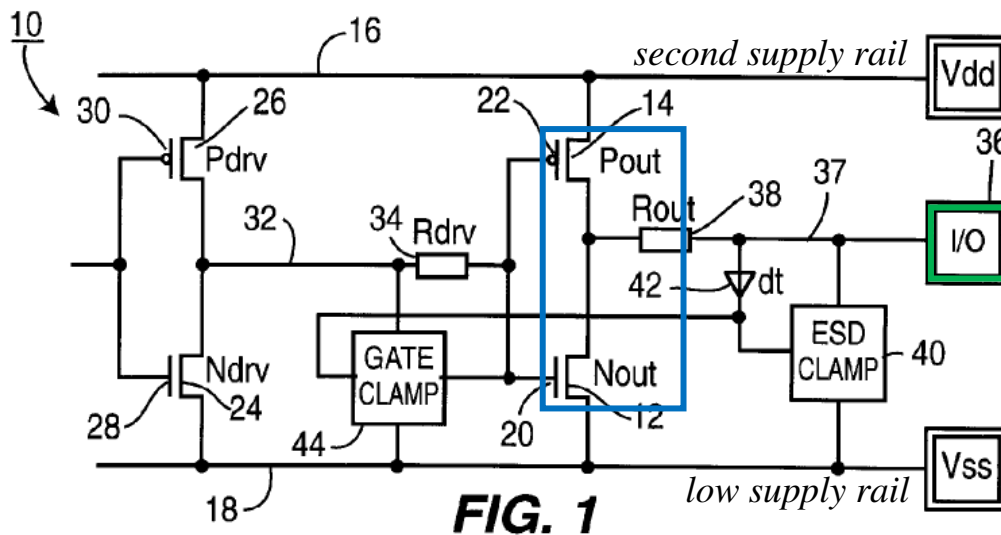
(EX-1004, Figure 1 (annotated).)

- b. [7b]: “one or more NMOS devices coupled between the physical pad and the low supply rail wherein the low supply rail has a value less than the second supply rail.”**

At least under Microchip’s apparent interpretation, Verhaege discloses this limitation.

Verhaege’s output buffer (dark blue) includes NMOS transistor 12, which is connected to the low supply rail, Vss, and I/O pad 36 (green) “by a line 37 and through an output resistor 38.” (EX-1004, 1:66-2:3, 2:16-2:19.)

As discussed in claim [7a], Verhaege discloses a second supply rail Vdd. By convention, the second supply rail Vdd has a positive voltage whereas the low supply rail Vss is ground. (*See also* discussion of claim [1g].) (EX-1002 ¶ 101.)



(EX-1004, Figure 1 (annotated).)

- c. [7c]: “wherein in activating at least a portion of the output buffer when the ESD event occurs, the control block enables one or more of the one or more PMOS devices.”

As discussed in claim [6d], the control block (i.e., gate clamp 44) enables PMOS transistor 14 when an ESD event occurs by grounding the gates of the output transistors. (EX-1004, 2:4-6, 2:32-2:34.)

- 8) **Claim 8:** “The circuit of claim 7, wherein in activating at least a portion of the output buffer when the ESD event occurs, the control block disables one or more of the one or more NMOS devices.”

Verhaege discloses that the control block (i.e., gate clamp 44) grounds the gates of transistors 12 and 14, disabling NMOS transistor 12. (EX-1004, 2:4-6, 2:32-2:36.)

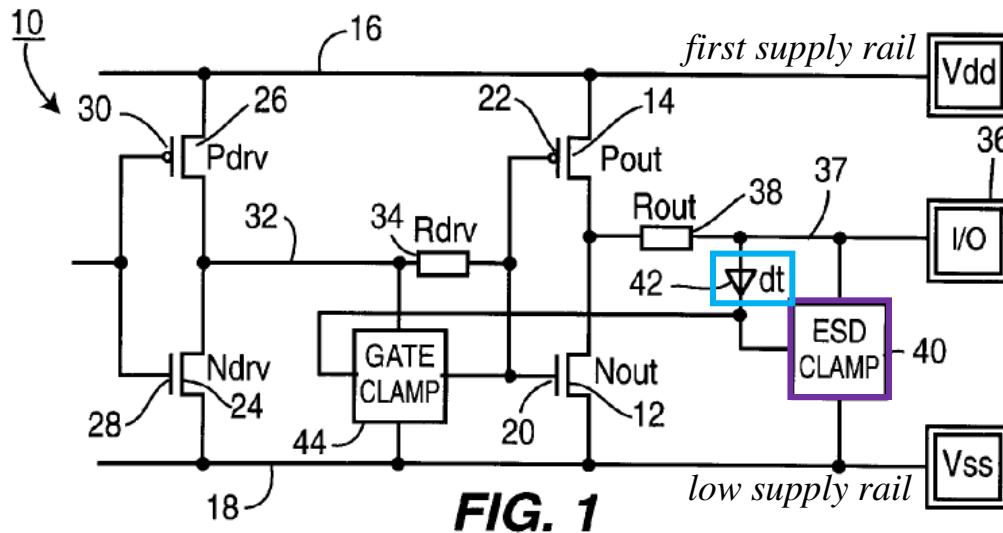
- 9) Claim 9: “The circuit of claim 7, wherein the one or more PMOS devices comprise a plurality of PMOS devices coupled in parallel between the second supply rail and the physical pad, and the one or more NMOS devices comprise a plurality of NMOS devices coupled in series between the physical pad and the second supply rail.**

Verhaege renders this claim obvious because it was well-known that a single PMOS transistor can be replaced with multiple PMOS transistors in parallel (with reasonable expectation of success) to reduce the current through any one transistor. (EX-1002 ¶ 104.) Similarly, it was common practice to include multiple NMOS devices in series (with reasonable expectation of success), which can protect sensitive NMOS devices by reducing the drain-source voltage.⁶ (EX-1002 ¶ 105.)

- 10) Claim 10: “The circuit of claim 6, wherein the clamp device is one of: a PMOS device having its source terminal coupled to the first supply rail, its drain terminal coupled to the low supply rail, and its gate terminal coupled to the control circuit; or an NMOS device having its drain terminal coupled to the first supply rail, its source terminal coupled to the low supply rail, and its gate terminal coupled the control circuit.”**

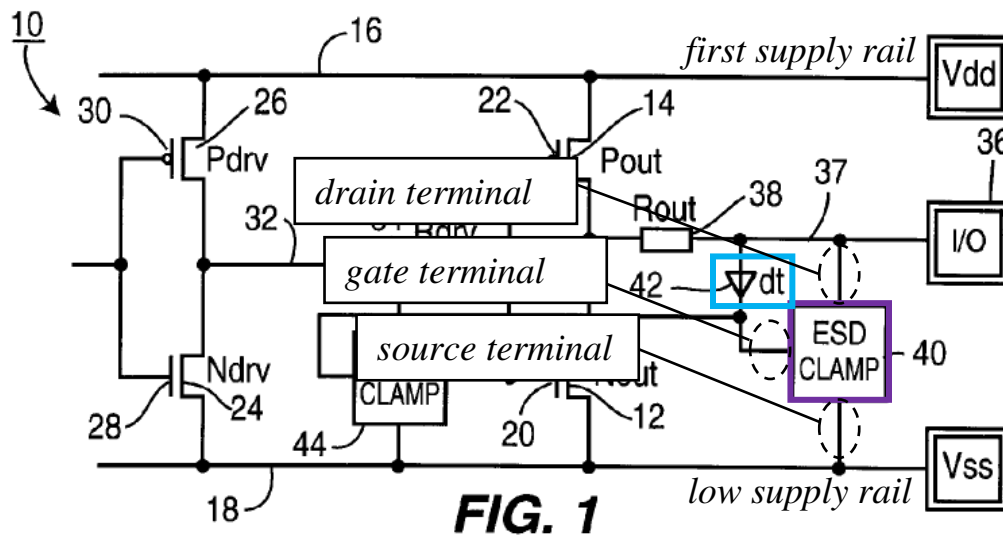
⁶ This remains true whether the NMOS devices are connected between the physical pad and the second supply rail, as claimed, or another location.

Verhaege's dynamic trigger device 42 (light blue) activates ESD clamp 40 (purple) during an ESD event. (EX-1004, 2:29-2:30.) At the time of the '665 patent, a conventional ESD clamp comprised a MOS transistor. (EX-1002 ¶ 107.) It would have been obvious to a POSITA that an NMOS could be used as ESD clamp device 40 because ESD clamp device 40 activates in response to a high voltage signal from dynamic trigger device 42. (EX-1002 ¶ 107.)



(EX-1004, Figure 1 (annotated).)

In Figure 1, the drain terminal of ESD clamp 40 is coupled to the first supply rail, Vdd, under Microchip's apparent interpretation. The source terminal of ESD clamp 40 is coupled to the low supply rail, Vss. The gate terminal of ESD clamp 40 is connected to the control circuit, dynamic trigger device 42.



(EX-1004, Figure 1 (annotated).)

- 11) **Claim 11: “The circuit of claim 6, wherein the first supply rail is configured to provide increased power during the ESD event.”**

Verhaege discloses a “first supply rail” in the Vdd rail. *See* discussion of claim [6c]. During an ESD event, Vdd is connected to I/O pad 36. The excess EDS energy flows to Vdd, providing increased power during the ESD event.

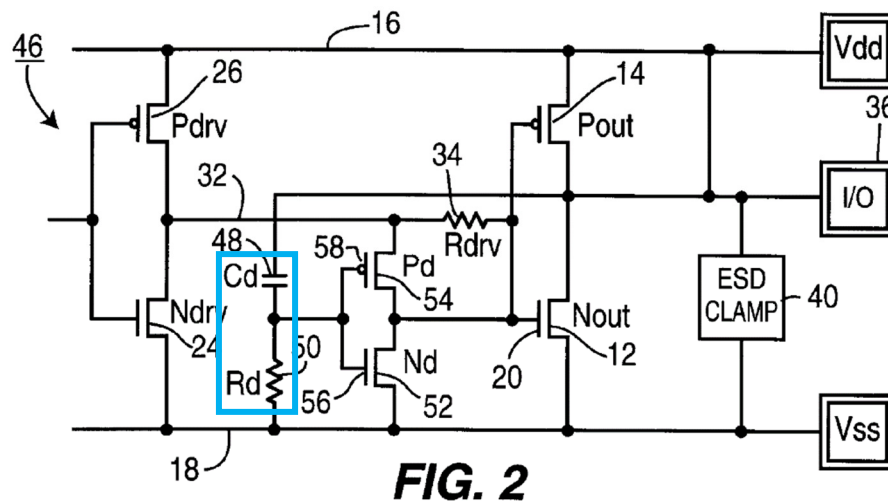
- 12) **Claim 12: “The control circuit of claim 6, wherein in instructing the control block to activate at least a portion of the output buffer when an ESD event occurs, the control circuit is operable to provide a control signal to the control block in response to the ESD event.”**

As discussed above in claim [6d], Verhaege discloses a control circuit in dynamic trigger device 42 and a control block comprising gate clamp 44. Dynamic trigger device 42 responds to an ESD event by providing a control signal to the

control block (i.e., gate clamp 44) comprising a high voltage signal. (EX-1002 ¶ 110.)

13) Claim 13: “The circuit of claim 6, wherein the control circuit is configured to receive a control signal corresponding to a time constant, wherein the time constant corresponds to a specified slope, wherein the control signal is configured to trigger the control circuit if a slope of a Voltage pulse developed in the system as a result of the ESD event is greater than or equal to the specified slope.”

A POSITA would understand the limitations of this claim to be directed to an RC circuit. (EX-1002 ¶ 111.) In Figure 1, Verhaege uses dynamic trigger device 42 as its control circuit, but in Figures 2, 4, and 5, Verhaege discloses RC circuits for detecting ESD events. In Figure 2, for example, Verhaege discloses a “trigger device compris[ing] a capacitor 48 in series with a resistor 50.” (EX-1004, 2:46-2:47.) A POSITA would understand that the trigger device (light blue) of Figure 2 (i.e., an RC circuit) is interchangeable with the trigger device of Figure 1. (EX-1002 ¶ 112.) A POSITA would be motivated to use the RC circuit to perform the same function as the dynamic trigger device in Figure 1 (with reasonable expectation of success) given the RC circuit’s superior ability to detect ESD events based on sudden voltage changes. (EX-1002 ¶¶ 112, 114.)



(EX-1004, Figure 2 (annotated).)

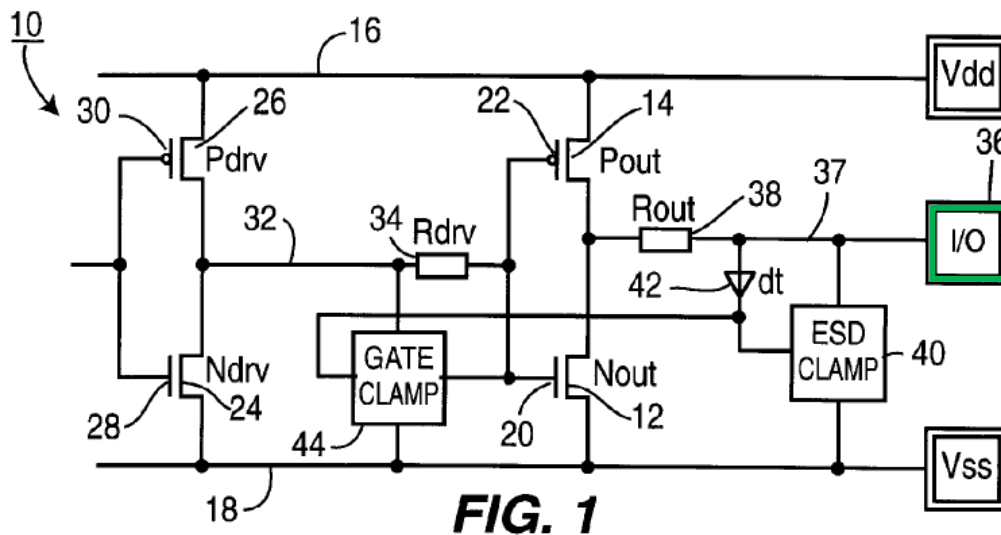
14) Claim 14

a. Preamble: “A system comprising:”

Verhaege discloses a system because Verhaege teaches a “circuit for the protection of an output driver NMOS transistor during EOS/ESD stress.” (EX-1004, Abstract.)

b. [14a]: “one or more pads, each pad comprising: a respective physical pad having respective capacitance;”

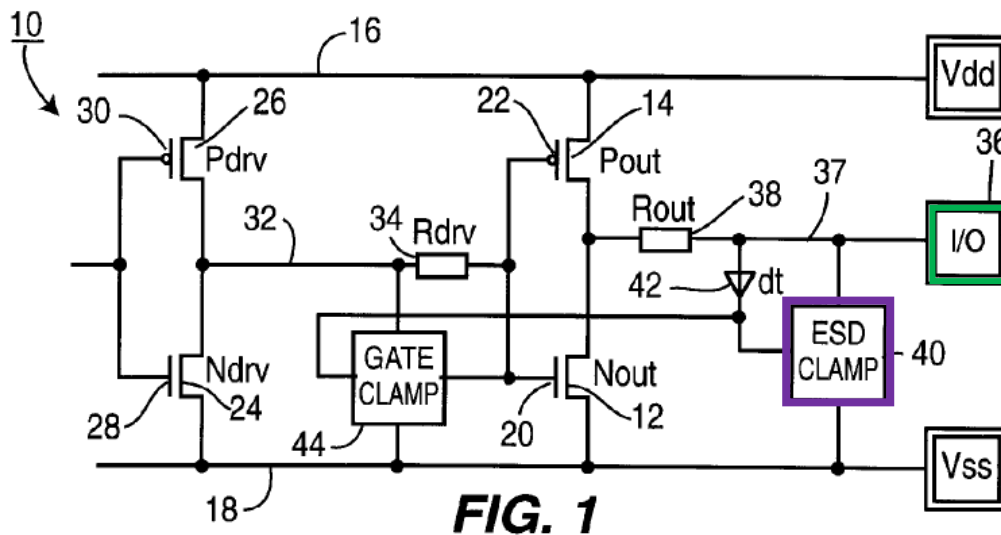
Verhaege discloses “[a]n I/O pad.” (EX-1004, 1:38-1:39.) In this context, a POSITA would understand that the I/O pad (green) is a physical pad. (EX-1002 ¶ 116.) As a physical, conductive device, the I/O pad has respective capacitance. (EX-1002 ¶ 116.)



(EX-1004, Figure 1 (annotated).)

- c. [14b]: “[each pad comprising:] a respective clamp device configured to absorb, when turned on, a portion of an energy generated by an ESD event, to thereby further reduce the maximum voltage developed in the system as the result of the ESD event; and”

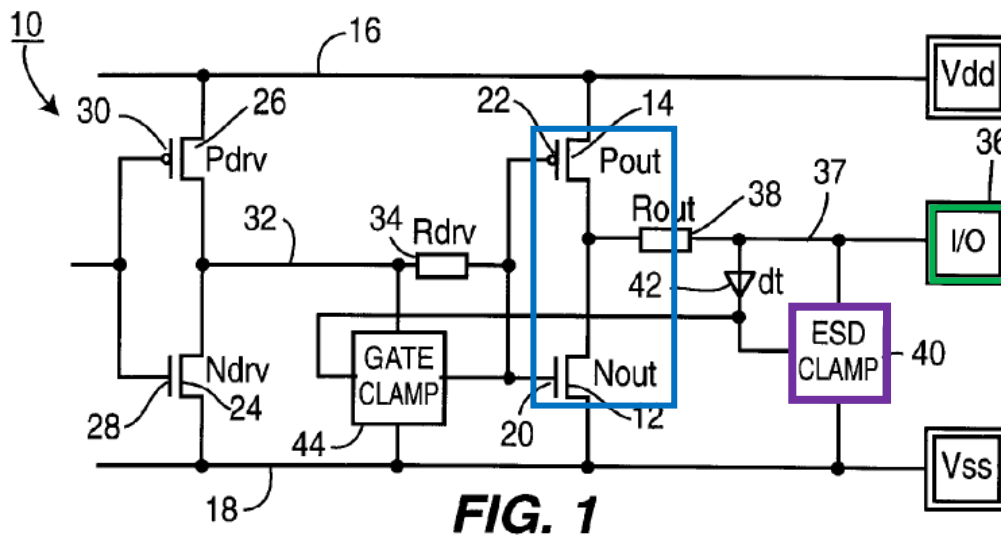
Verhaege’s Figure 1 (below) shows an I/O pad 36 (green) connected to its respective ESD clamp device 40 (purple). (EX-1004 2:19-2:20.) ESD clamp 40 connects I/O pad 36 to Vss during an ESD event. ESD clamp 40 is thus configured to absorb, when turned on, a portion of an energy generated by an ESD event. (EX-1004, 2:19-2:20, 2:29-2:30.) Verhaege’s ESD clamp 40 “reduce[s] the maximum voltage developed in the system as the result of the ESD event” because “the ESD stress can be diverted to the parallel ESD clamp and the EOS/ESD capability is achieved.” (EX-1004, 2:37-2:39.)



(EX-1004, Figure 1 (annotated).)

- d. [14c]: “[each pad comprising:] a respective pad circuit comprising: a respective output buffer coupled to the respective physical pad, and operable to drive at least one respective output signal at the respective physical pad; and”

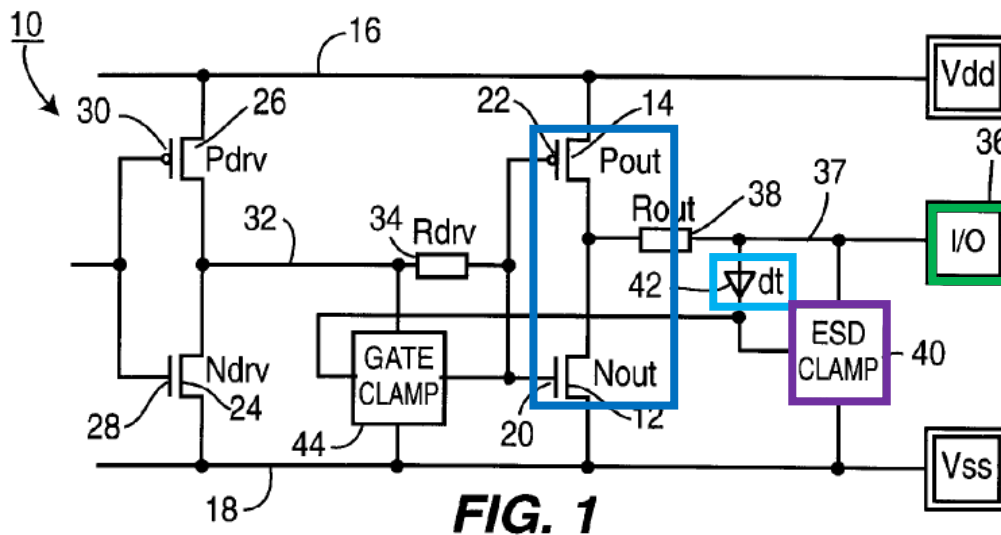
Verhaege discloses an I/O pad 36 (green) having a respective pad circuit—circuit 10. (EX-1004, 1:66-2:18.) As discussed in claim [6a], Verhaege also discloses an output buffer (dark blue) coupled to the pad and operable to drive at least one output signal at the pad.



(EX-1004, Figure 1 (annotated).)

- e. [14d]: “[the respective pad circuit comprising:]
respective control circuitry operable to: activate at
least a portion of the respective output buffer in
response to an ESD event to charge the respective
pad capacitance to reduce a maximum voltage
developed in the system as a result of the ESD
event; and”

As discussed in claims [6d] and [6e], Verhaege teaches control circuitry comprising dynamic trigger device 42 (light blue), which is operable to activate at least a portion (i.e., PMOS transistor 14) of the output buffer (dark blue) in response to an ESD event. As further discussed in claims [6d] and [6e], a POSITA would include the Verhaege circuit at every I/O pad (green). Activating PMOS transistor 14 allows ESD energy to flow to the Vdd rail and charge the capacitance of any connected I/O pads, thereby reducing a maximum voltage developed in the system due to the ESD event. (EX-1002 ¶ 119.)



(EX-1004, Figure 1 (annotated).)

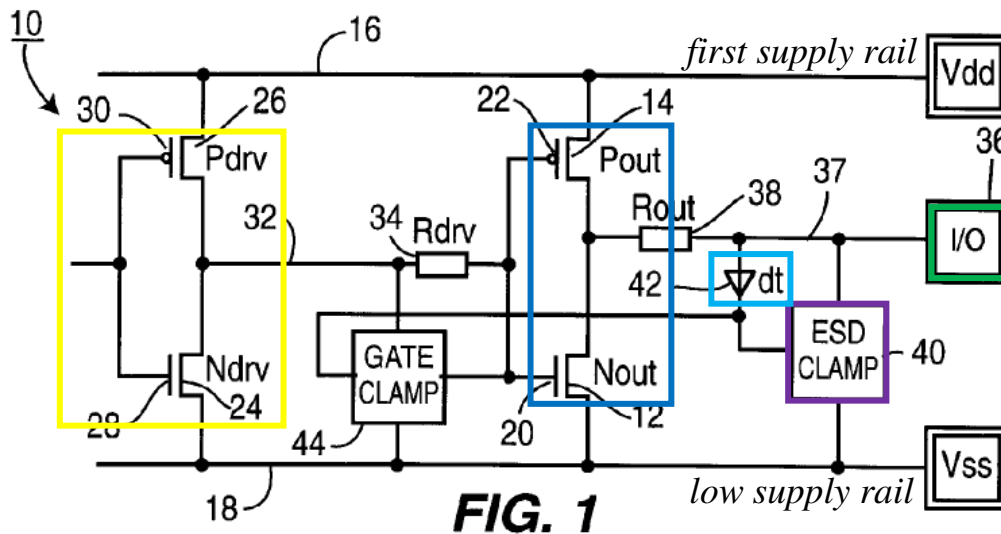
- f. [14e]: “[the respective control circuitry operable to:] turn on the clamp device in response to the ESD event.”

As discussed in claim [6f], in response to the ESD event, Verhaege’s “dynamic trigger device 42 is used to trigger the ESD clamp 40.” (EX-1004, 2:29-2:31.)

- 15) **Claim 15:** “The system of claim 14, further comprising functional circuitry coupled to the respective pad circuit of at least one of the one or more pads, wherein the functional circuitry is operable to generate the at least one respective output signal driven by the respective pad circuit of the at least one of the one or more pads.”

Verhaege renders this limitation obvious because a POSITA would understand that pre-driver transistors 24 and 26 (yellow) require an output signal, as indicated by the wire from outside circuit 10. Various functional circuitries to

create that signal, such as a microcontroller, were well-known in the art. (EX-1002 ¶ 121.). The output signal is then driven by the circuit 10 to create the final output signal at I/O pad 36 (green). (EX-1002 ¶ 121.)



(EX-1004, Figure 1 (annotated).)

- 16) Claim 16: “The system of claim 14, further comprising a first supply rail configured to provide increased power in accordance with the ESD event, and further configured to power the respective control circuitry of the respective pad circuit of each pad.”**

Verhaege discloses a “first supply rail” in the Vdd rail. (See discussion of claim [6c].) During an ESD event, Vdd is connected to I/O pad 36. The excess EDS energy flows to Vdd, providing increased power during the ESD event. Vdd also provides power to the respective control circuitry—dynamic trigger device 42—of the respective pad circuit 10 of each I/O pad 36 through PMOS transistor 14. (EX-1002 ¶ 122.)

17) Claim 17: “The system of claim 16, further comprising a second supply rail configured to power the respective output buffer of the respective pad circuit of each pad.”

Microchip’s apparent position is that the “first supply rail” of claim 16 and “second supply rail” of claim 17 can refer to the same voltage rail. (EX-1007, 96-97.) Under this interpretation, Verhaege discloses a second supply rail comprising the Vdd rail. (EX-1002 ¶ 124.) The Vdd rail provides power to the output buffer, including PMOS transistor 14. (EX-1002 ¶ 124.)

18) Claim 18: “The system of claim 16, wherein the respective control circuitry of the respective pad circuit of each pad is configured to receive a respective control signal corresponding to a time constant, wherein the time constant corresponds to a specified slope, wherein the respective control signal is configured to trigger the respective control circuitry if a slope of a voltage pulse developed in the system as a result of the ESD event is greater than or equal to the specified slope.”

See discussion of claim 13.

B. Ground 2 – Obviousness Based on Verhaege in View of Miller

1. Summary of Miller

Miller discloses an ESD protection system using multiple pad circuits. (EX-1006, 1:7-1:10.)

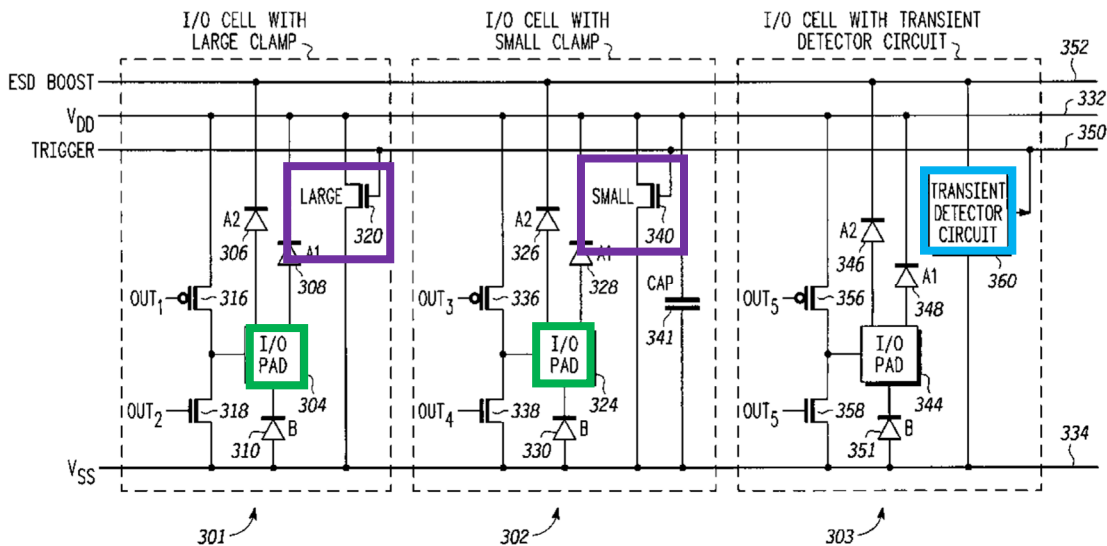


FIG. 3

(EX-1006, Figure 3)

During an ESD event at I/O pad 304 (green), current flows to the VDD rail 332 and optional ESD boost rail 352. (EX-1006, 7:14-7:17, 7:25-7:32.) In response to the sudden voltage change, transient detector circuit 360 (light blue) sends a signal to ESD protection clamps 320 and 340 (purple) via trigger rail 350. (*Id.*, 7:25-7:32.) The trigger rail activates *all* the ESD protection circuits, allowing the

clamp transistor devices of each cell to “work together to dissipate the ESD currents.” (*Id.*, 7:63-7:67.)

2. The Combination

A POSITA would have been motivated to combine Verhaege and Miller because both concern the protection of I/O pads during ESD events. (EX-1002 ¶ 133.) At the time, ESD was a well-known problem, particularly because integrated circuits with densely-packed components and lower operating voltages were susceptible to ESD damage. (EX-1002 ¶ 133.)

One solution was disclosed in Verhaege, which improves on an ESD protection circuit by adding control circuitry to turn off one output transistor while using the other to connect the I/O pad to a voltage rail.

Another technique, disclosed in Miller, reflects the reality of integrated circuit design as of 2007: most integrated circuits had multiple I/O pads. An express teaching of Miller is using the ESD protection circuit of every I/O pad, in parallel, to disperse an ESD event more effectively.

Therefore, a POSITA would have been motivated to use the improved protection circuit of Verhaege, apply it at every I/O pad, and share the ESD energy across multiple pad circuits as taught by Miller. This would require only a simple modification to the Verhaege circuit—connecting the trigger devices as shown in Miller—to activate multiple pad circuits during an ESD event. (EX-1002 ¶ 136.)

A POSITA would reasonably expect this combination to succeed. First, the building blocks of both references—such as pads, transistors, clamp devices, and voltage rails—were well understood and behave in predictable ways when combined. (EX-1002 ¶ 137.) Second, a POSITA would expect the modification to succeed because incorporating the ESD strategy of Miller requires only a small change to Verhaege. Finally, the combination would foreseeably yield desirable results because an ESD protection circuit like Verhaege’s would benefit from sharing the ESD energy across multiple pad circuits as taught by Miller. (*Id.*)

3. Analysis

As set forth below, the combination of Verhaege in view of Miller renders the challenged claims obvious.

1) Claim 1

a. Preamble, [1a]-[1c]

See Section V.A.

b. [1d]: “a control block configured, to turn on, when instructed, at least one of the one or more output transistor devices to charge the pad capacitance to reduce a maximum voltage developed in the system as a result of the ESD event;”

As discussed in Section V.A, Verhaege’s control block is gate clamp 44. The gate clamp turns on, when instructed, at least one of the output transistor devices—output transistor 14—by connecting its gate to ground. (EX-1002 ¶ 142.)

Miller discloses a distributed system for dissipating excess ESD energy wherein the protection circuit is repeated at each I/O pad then connected in parallel. (EX-1006, 7:63-7:67, Figure 3.) Figure 3, for example, shows an ESD protection circuit repeated at I/O cells 301 and 302, and connected in parallel via the Vdd rail and Vss rail.

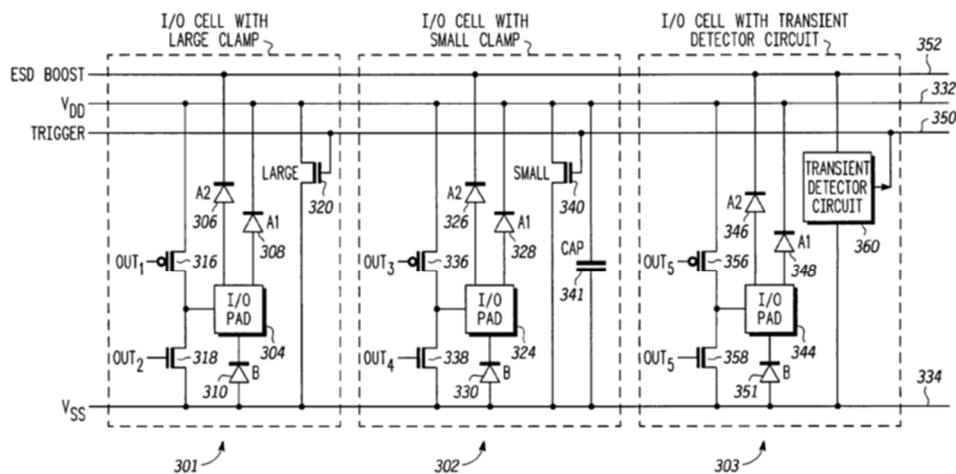


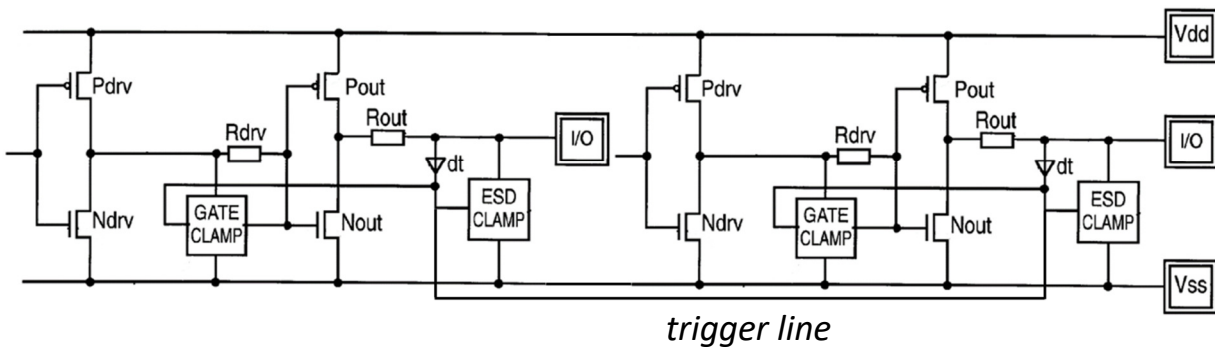
FIG. 3

(EX-1006, Figure 3.)

Miller teaches that this strategy provides superior ESD protection because “the clamp transistor devices . . . can work together to dissipate the ESD currents.” (EX-1006, 7:63-7:67.)

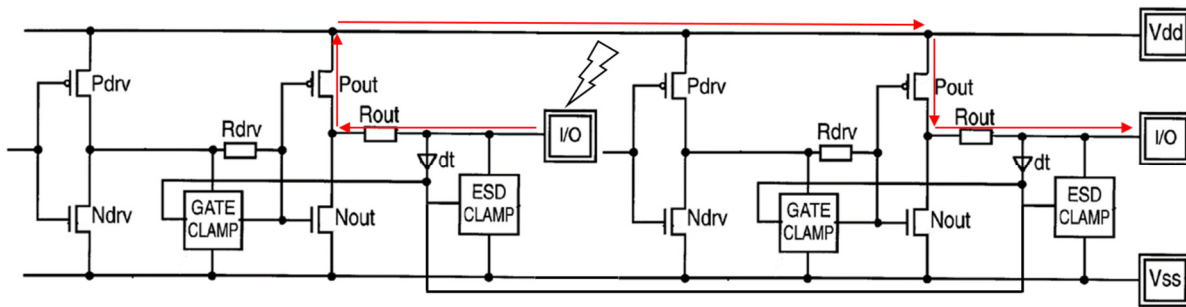
As discussed above, a POSITA would have been motivated to modify Verhaege to reap the benefits of distributing the ESD energy across multiple circuits. A POSITA would have included a Verhaege circuit at each I/O pad and

connected them via the voltage rails as shown in Miller. While there were many obvious ways to activate multiple circuits during an ESD event⁷, one approach taught by Miller is to use a single trigger line to carry the activation signal. One possible embodiment of the modified circuit is shown below. (EX-1002 ¶ 146.)

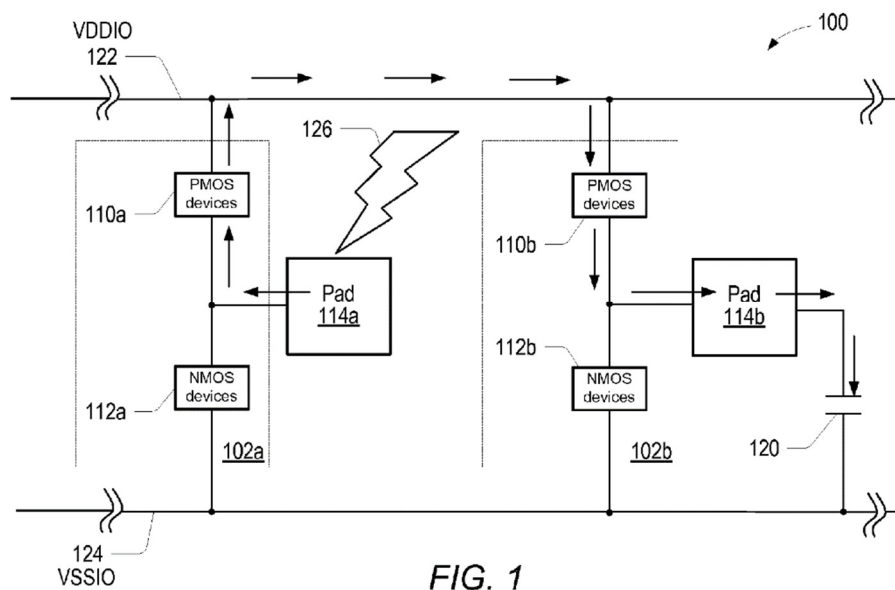


During an ESD event, both protection circuits are activated by the trigger line. The gate clamps ground the gates of the PMOS output transistors, turning them on and connecting the I/O pads to the Vdd rail. This allows excess ESD energy at one I/O pad to flow to the other I/O pad, thereby “charg[ing] the pad capacitance and reducing the maximum voltage developed in the system.” The ESD path is shown in the figure below, wherein the source of the ESD event is signified by a lightning bolt symbol. (EX-1002 ¶ 147.)

⁷ In fact, even the '665 patent does not disclose the exact mechanism that turns on multiple pad circuits during an ESD event.



For reference, Figure 1 of the '665 patent is included below.



(EX-1001, Figure 1.)

c. [1e]: “a clamp device configured between a second voltage rail and a third voltage rail to reduce, when turned on, the maximum voltage developed in the system as the result of the ESD event;”

To any extent that the first and second rails must be separate, this limitation would have been obvious to a POSITA because Miller, just like the '665 patent,

teaches a separate, optional “ESD boost” rail. (EX-1006 4:15-4:19, Figure 3.) A POSITA would understand that, to dissipate the ESD energy, the clamp device would necessarily be connected to the separate ESD rail. (EX-1002 ¶ 149.)

Moreover, a POSITA would have understood, with a reasonable expectation of success, that a separate ESD rail would improve Verhaege by segregating the ESD energy. (EX-1002 ¶ 149.)

- d. [1f]: “enable circuitry configured to turn on the clamp device and instruct the control block to turn on the at least one of the one or more output transistor devices, in response to the ESD event;”**

See Section V.A.

- e. [1g]: “wherein the second voltage rail is configured to provide power to the enable circuitry, and wherein the third voltage rail has a value below the first voltage rail.”**

If the rails must be separate, the second voltage rail disclosed by Miller is configured to provide power to the enable circuitry. Miller’s enable circuitry—transient detector circuit 360—is connected to the ESD voltage rail.

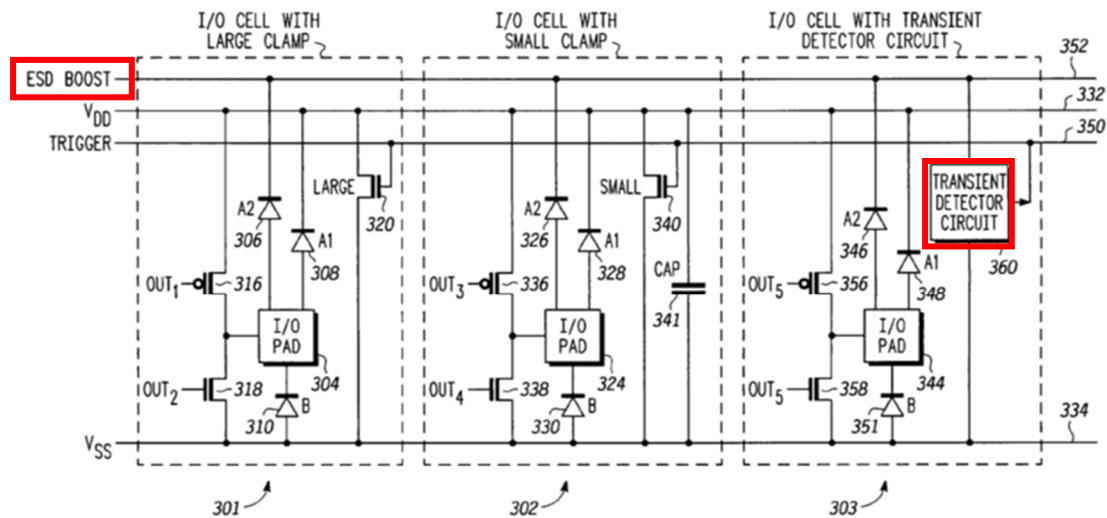


FIG. 3

(EX-1006, Figure 3 (annotated.))

A POSITA would have appreciated that this configuration was compatible with Verhaege. (EX-1002 ¶ 151.)

- 2) Claim 2: “The pad circuit of claim 1, wherein in turning on the at least one of the one or more output transistor devices when instructed, the control block couples an associated capacitance of the first voltage rail to the physical pad to share a charge developed in the system in response to the ESD event, to reduce the maximum voltage developed in the system as the result of the ESD event.”

The combination of Verhaege in view of Miller satisfies this limitation because, during an ESD event, all I/O pads are coupled to the Vdd rail as discussed in claim [1d]. Thus, the associated capacitance of the Vdd rail includes the sum of the capacitance of all I/O pads connected to the Vdd rail. This reduces the

maximum voltage developed in the system by sharing the charge across the pads.

(EX-1002 ¶ 153.)

3) Claims 3-5

See Section V.A.

4) Claim 6

a. Preamble, [6a], and [6b]

See Section V.A.

b. [6c]: “a clamp device coupled between a first supply rail and a low supply rail, wherein the clamp device is configured to absorb, when turned on, a portion of an energy generated by the ESD event, to reduce the maximum voltage developed in the system as the result of the ESD event;”

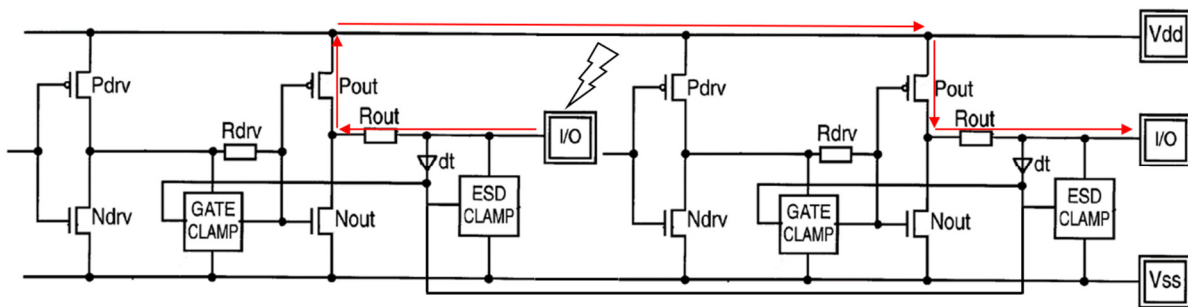
To any extent that the first supply rail of this claim and the second supply rail of dependent claim 7 must be separate, this limitation would have been obvious to a POSITA as explained in claim [1e].

c. [6d]: “and a control circuit configured to instruct the control block to activate at least a portion of the output buffer when an ESD event occurs,”

See Section V.A.

d. [6e]: “[the control circuit configured] to charge the pad capacitance to reduce a maximum voltage developed in the system as a result of the ESD event”

As discussed in claim [1d], the combination of Verhaege and Miller would connect all I/O pads to the Vdd rail during an ESD event. Thus, the ESD energy would charge the capacitance of the I/O pads and reduce the maximum voltage developed in the system. The ESD path is shown below in an embodiment of the combination wherein the lightning bolt signifies the ESD event.



- e. [6f] and [6g]: “wherein the control circuit is further configured to turn on the clamp device in response to the ESD event;”

See Section V.A.

5) Claim 7:

- a. [7a]: “The circuit of claim 6, wherein the output buffer comprises one or more PMOS devices coupled between a second supply rail and the physical pad; and”

To any extent that the first and second supply rails must be separate, the “first supply rail” of claim [6c] would refer to the separate, “ESD boost” rail taught by Miller. (EX-1006 4:15-4:19, Figure 3.) Thus, this limitation would refer to Vdd

and, as discussed above, the output buffer contains a PMOS device 14 coupled between Vdd and the I/O pad.

b. [7b] and [7c]

See Section V.A.

c. Claims 8 and 9

See Section V.A

- 6) Claim 10: “The circuit of claim 6, wherein the clamp device is one of: a PMOS device having its source terminal coupled to the first supply rail, its drain terminal coupled to the low Supply rail, and its gate terminal coupled to the control circuit; or an NMOS device having its drain terminal coupled to the first supply rail, its source terminal coupled to the low supply rail, and its gate terminal coupled the control circuit.”**

This limitation would have been obvious to a POSITA over Verhaege in view of Miller because Miller explicitly discloses that the clamp devices are MOSFET transistors configured as described. (EX-1006, 3:8-3:16, Figure 3.)

7) Claims 11-13

See Section V.A.

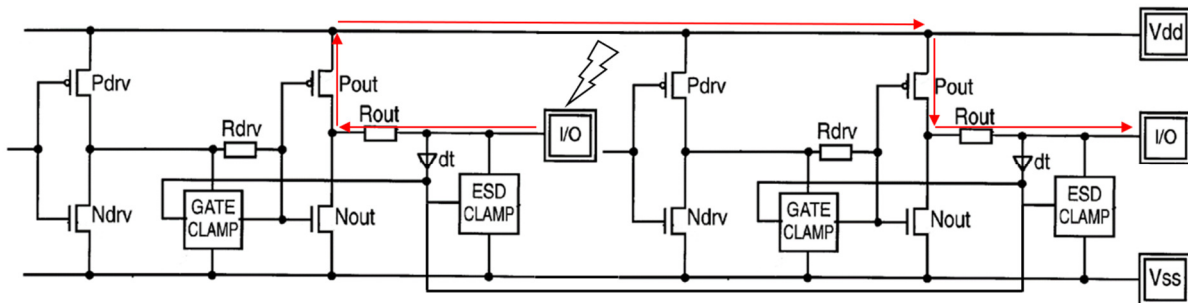
8) Claim 14

a. Preamble, [1a]-[1c]

See Section V.A.

- b. [14d]: “[the respective pad circuit comprising:] respective control circuitry operable to: activate at least a portion of the respective output buffer in response to an ESD event to charge the respective pad capacitance to reduce a maximum voltage developed in the system as a result of the ESD event; and”**

As discussed in claim [1d] and [6e], the output buffer of each protection circuit (i.e., the output transistors) couples the I/O pad to Vdd during an ESD event. As shown below, this allows ESD energy to flow to other pads in the system.



Thus, the ESD energy charges the capacitance of the I/O pads and the maximum voltage developed in the system is reduced. (EX-1002 ¶ 180.)

- c. [14e]: “[the respective control circuitry operable to:] turn on the clamp device in response to the ESD event.”**

See Section V.A.

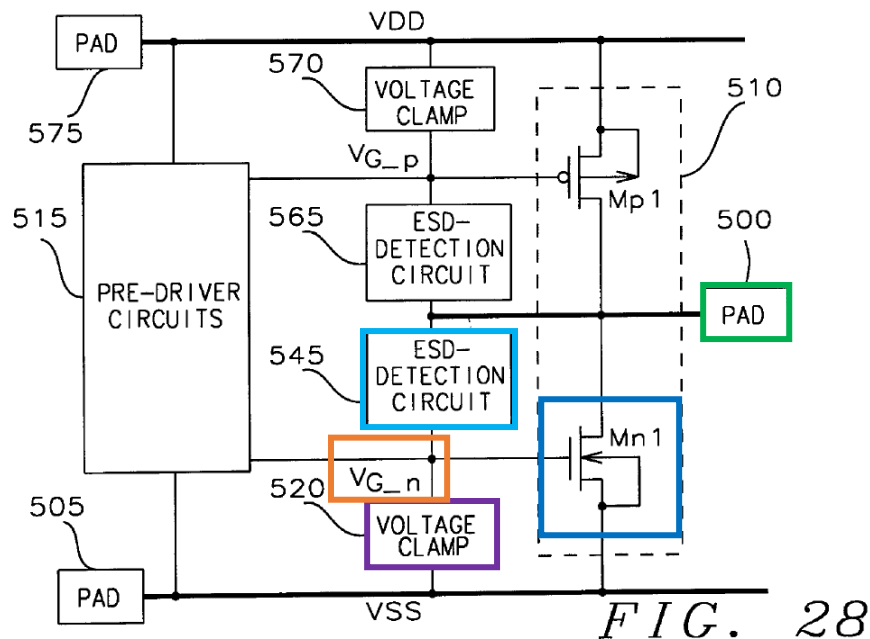
9) Claims 15-18

See Section V.A.

C. Ground 3 – Obviousness Based on Ker

1. Summary of Ker

Ker teaches a circuit to protect sensitive components from ESD events at an I/O pad. (EX-1005, 1:7-1:9.) Figure 28 (below) shows a generic block diagram of the invention, but subsequent figures provide further detail, such as Figure 29 which is particularly relevant.



(EX-1005, Figure 28 (annotated).)

During a positive-voltage ESD event at I/O pad 500 (green), ESD detection circuit 545 (light blue) sends a signal to signal port VG_n (orange). This activates N-type output driver Mn1 (dark blue). (*Id.*, 18:24-18:36.) In turn, Mn1 dissipates some energy from the ESD event by connecting I/O pad 500 to the VSS rail. (*Id.*,

18:24-18:36.) From the rail, the ESD energy charges the capacitance of any devices connected to the rail. (EX-1002 ¶ 189.) If the voltage at I/O pad 500 continues to climb, voltage clamp 520 (purple) activates to shunt excess voltage from pad 500 through ESD detection circuit 545 to the VSS rail. (*Id.*, 18:37-18:42, 18:51-18:59.)

Conversely, the ESD event can be directed to the positive voltage rail Vdd based on the polarity of the ESD using similar circuitry. Both the positive-ESD circuitry and negative-ESD circuitry are relevant to the obviousness analysis.

2. Analysis

As set forth below, Ker renders the challenged claims obvious.

1) Claim 1

a. Preamble: “A pad circuit configured to provide protection against electrostatic discharge (ESD) in a system comprising the pad circuit,”

At least one embodiment of the invention “describes an integrated circuit output driver circuit . . . for dissipating electrostatic charge from an ESD Source connected to the output pad.” (EX-1005, 9:44-9:48.)

b. [1a]: “the pad circuit comprising: a first node coupled to a first voltage rail;”

In Figure 29, Ker discloses a “first node coupled to a first voltage rail” (red) where output PMOS Mp1 meets the Vdd rail.

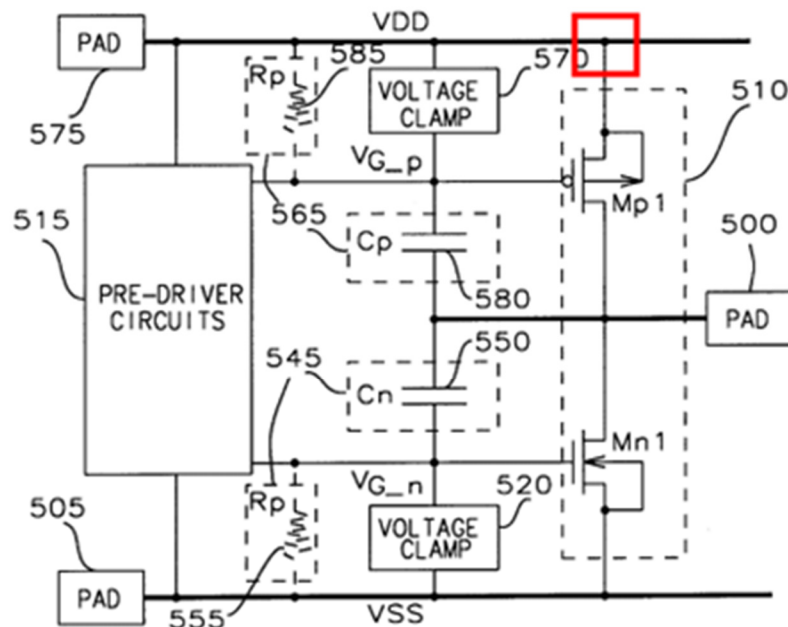
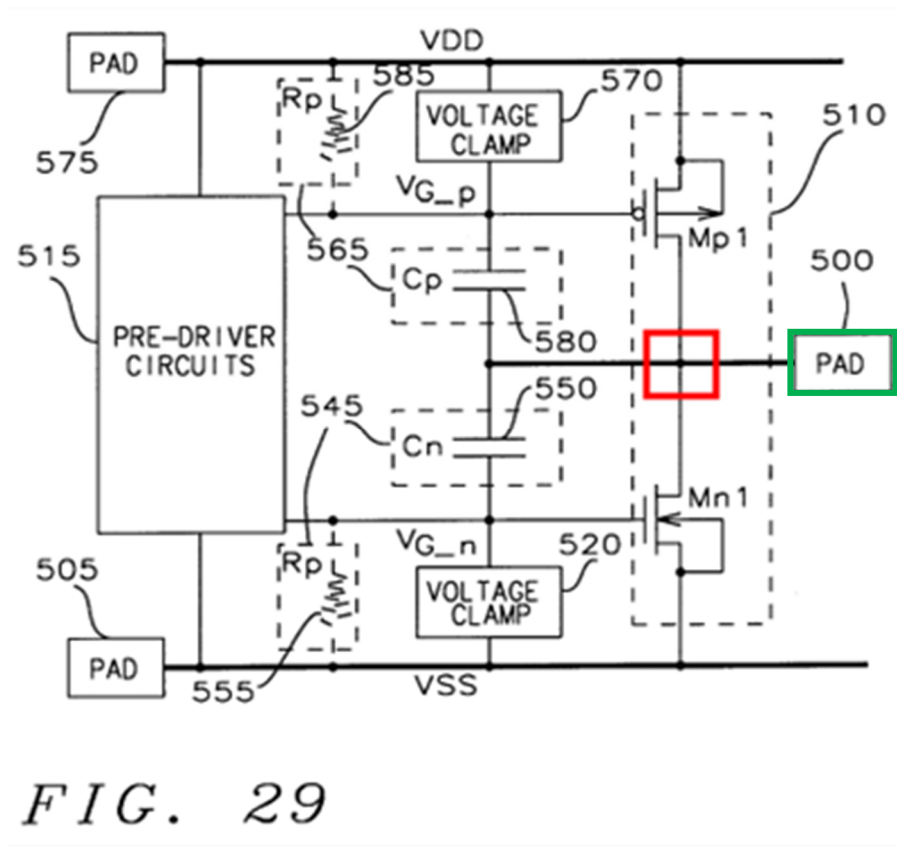


FIG. 29

(EX-1005, Figure 29 (annotated).)

- c. [1b]: “[the pad circuit comprising] a second node coupled to a physical pad having capacitance;”

Ker discloses a “second node coupled to a physical pad” (red) where PMOS Mp1 meets the output terminal pad 500 (green). (EX-1005, 19:20-19:24, Figure 29.)



(EX-1005, Figure 29 (annotated).)

Pad 500 is a physical pad. (EX-1002 ¶ 194.) As a physical, conductive device, it has capacitance. (EX-1002 ¶ 194.)

- d. [1c]: “[the pad circuit comprising:] one or more output transistor devices coupled between the first node and the second node, and operable to at least partially drive an output signal at the second node;”**

Ker teaches “one or more output transistor devices coupled between the first node and second node” because in Figure 29, PMOS output transistor Mp1 (blue) is connected between the two nodes (red). (EX-1005, 19:21-19:26.)

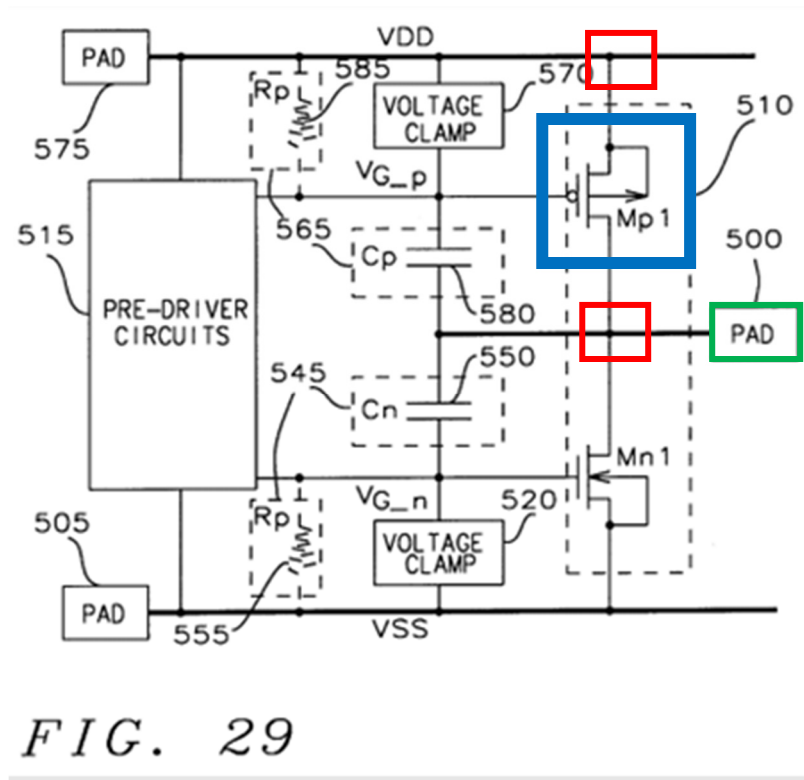


FIG. 29

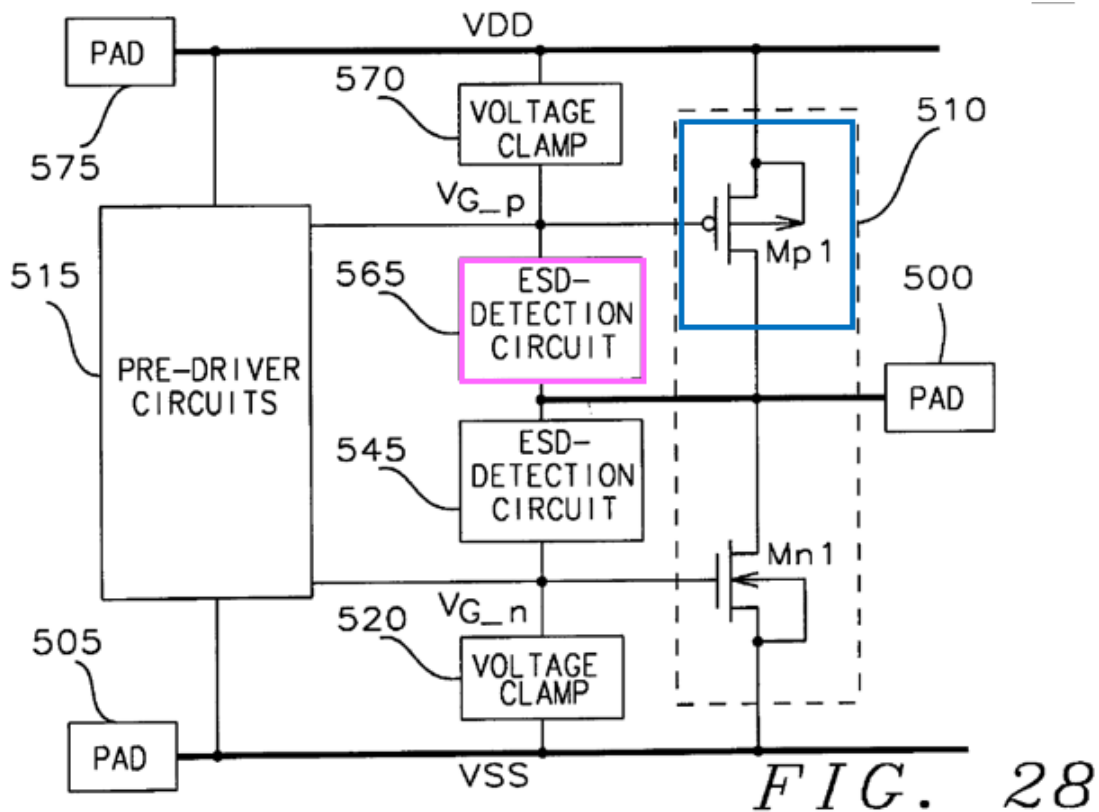
(EX-1005, Figure 29 (annotated).)

Mp1 is “operable to at least partially drive an output signal at the second node” because it is the component of the driver circuit that connects pad 500 to Vdd to produce a high output signal. (EX-1002 ¶ 197.)

- e. [1d]: “a control block configured, to turn on, when instructed, at least one of the one or more output transistor devices to charge the pad capacitance to reduce a maximum voltage developed in the system as a result of the ESD event;”

In the '665 patent, a “control block” may contain “any digital, analog, and/or mixed mode circuitry configured to perform the functions assigned to the control block,” namely, turning on the output transistor. (EX-1001, 4:43-4:46; EX-1002 ¶

199.) Ker renders the limitation obvious because, as indicated by the generic disclosure of Figure 28, the ESD detection circuit can take multiple forms.



(EX-1005, Figure 28 (annotated).)

Ker discloses numerous ESD detection circuits, including the one shown in Figure 37. This version discloses an ESD detection circuit comprising not only an RC circuit, but also a transistor Mp2 (orange).

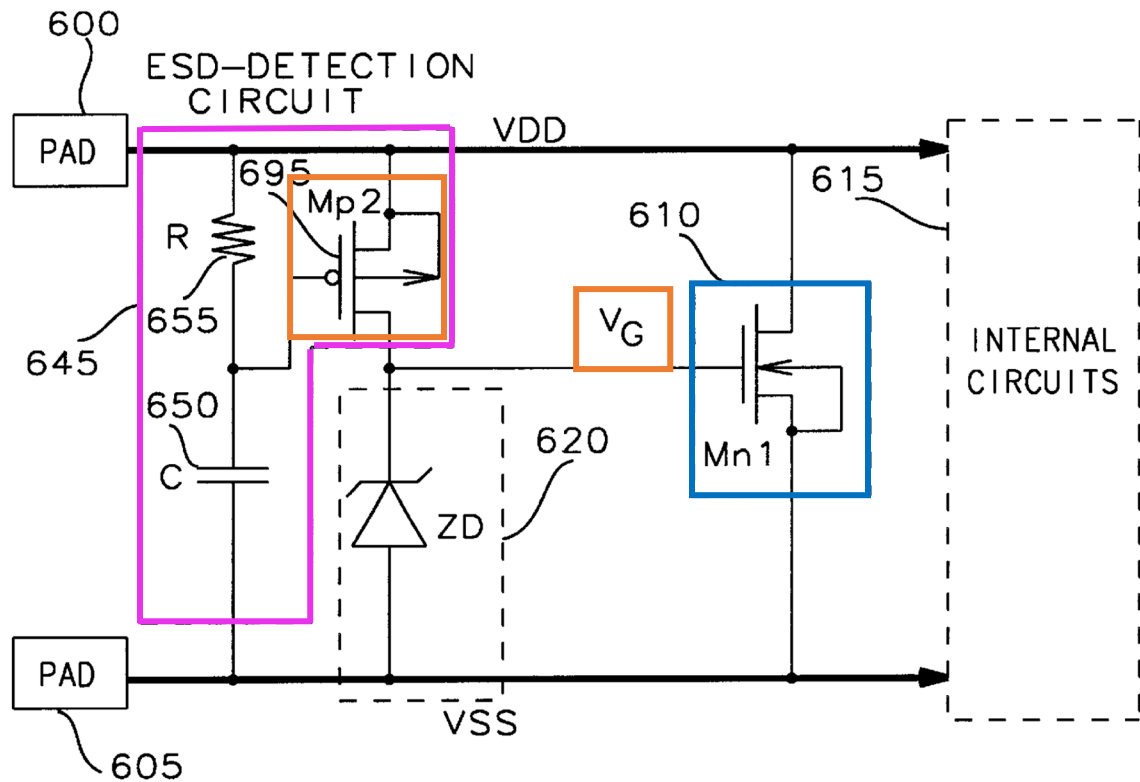


FIG. 37

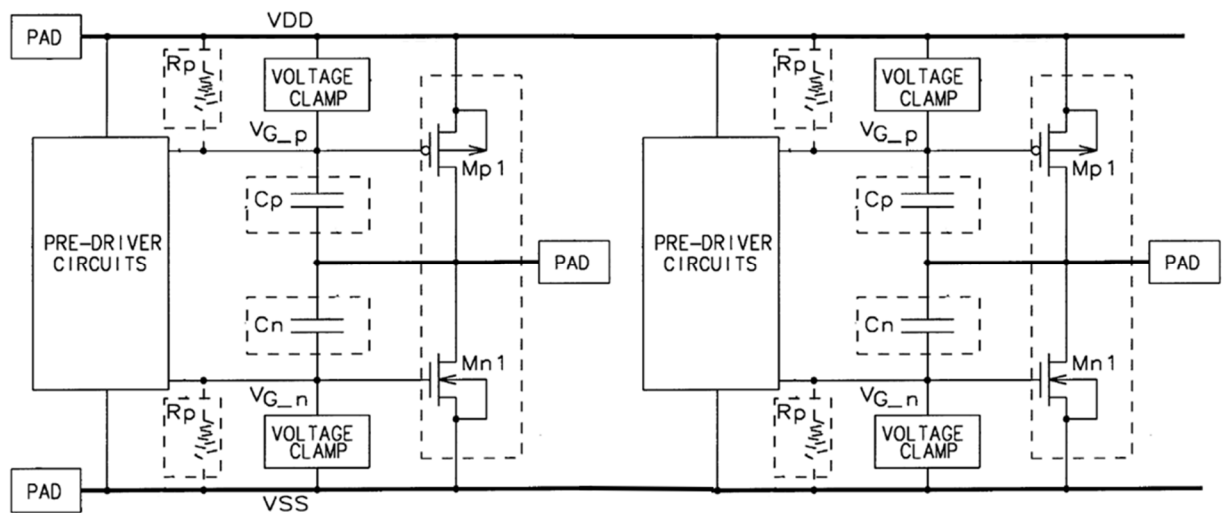
(EX-1005, Figure 37 (annotated).)

A POSITA would have appreciated that the ESD detection circuits were interchangeable and would have understood how to modify the Figure 28 circuit to use the more advanced detection circuit shown in Figure 37 as the control block⁸. (EX-1002 ¶¶ 199-202.) Including transistor Mp2 is beneficial because it decouples

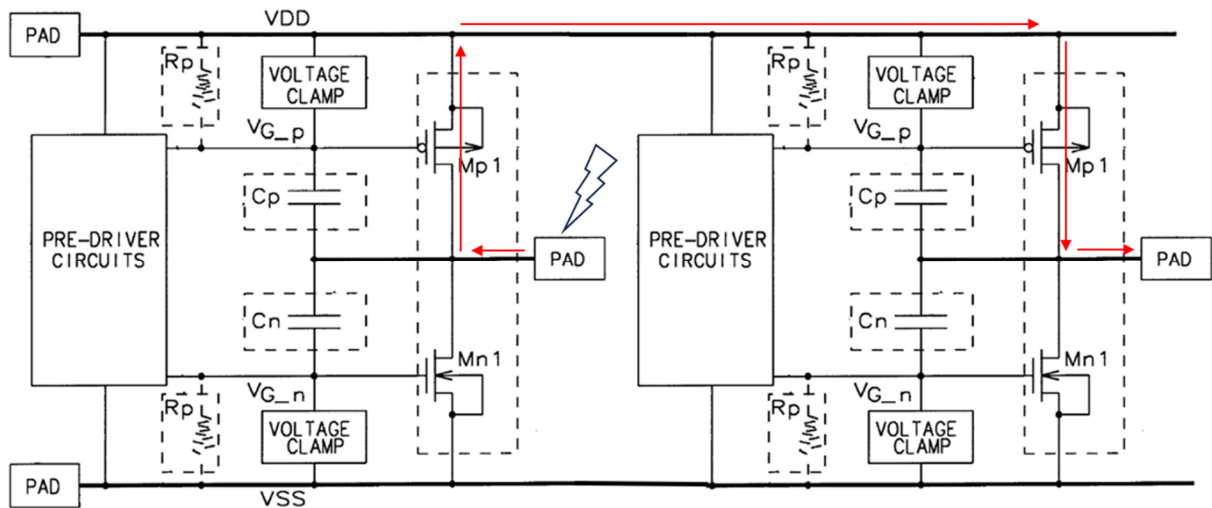
⁸ Hereafter, Figure 29 is still used for simplicity, but in addition to the signal ports Vg_n and VG_p, the control block comprises additional circuitry such as Mp2 in Figure 37. Without more, a signal port is not a control block.

the pre-driver signals from the RC circuits during normal operating conditions, reducing the load on the pre-driver. (EX-1002 ¶ 203.) A POSITA would have expected the substitution to succeed based on Ker's disclosures and because the components behave predictably when combined. (EX-1002 ¶ 203.)

Although Ker describes a single I/O pad circuit, a POSITA would have known that, by 2007, most devices had multiple I/O pads, any of which could be the source of an ESD event. (EX-1002 ¶ 205.) Thus, a POSITA would have been motivated to repeat the Ker circuit at each I/O pad. (EX-1002 ¶ 205.) The schematic below shows the Ker circuit repeated at two I/O pads.



Therefore, when output transistor Mp1 connects pad 500 to Vdd during an ESD event, allowing the ESD energy to flow to the Vdd rail, the ESD energy can flow to other pads connected to the rail as shown below.



This “charge[s] the pad capacitance” of the other I/O pads connected to the rail, thereby “reduc[ing] the maximum voltage developed in the system as a result of the ESD event.”

f. [1e]: “a clamp device configured between a second voltage rail and a third voltage rail to reduce, when turned on, the maximum voltage developed in the system as the result of the ESD event;”

At least under Microchip’s apparent interpretation of this limitation as evidenced by its infringement contentions, Ker discloses this limitation.

Microchip’s apparent position is that the “first voltage rail” of claim [1a] and “second voltage rail” of claim [1e] can refer to the same voltage rail and/or be connected to each other. (EX-1007, 11.) Thus, Ker discloses a “second voltage rail” comprising the Vdd rail and a “third voltage rail” in Vss. (EX-1002 ¶ 208.)

Ker also discloses a “clamp device”: clamp circuit 570. As shown below, clamp circuit 570 (purple) is “configured between” the second voltage rail (i.e., Vdd) and the third voltage rail (i.e., Vss) based on Microchip’s interpretation of the limitation as not requiring direct connections. (EX-1007, 11.)

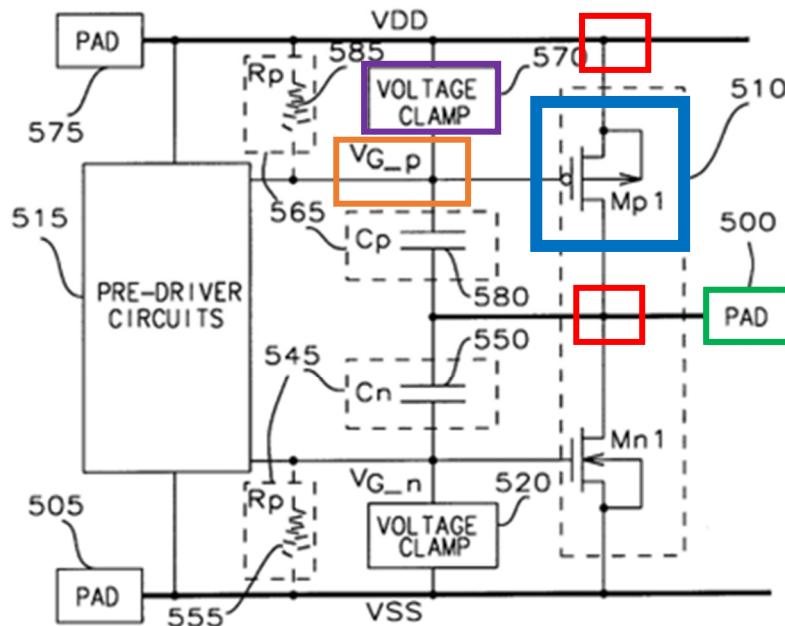


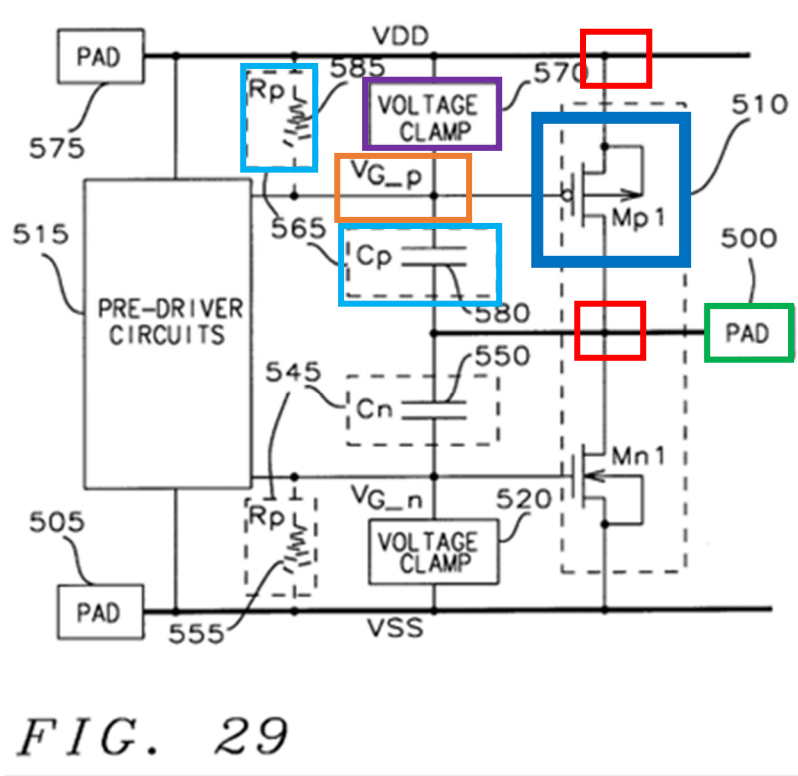
FIG. 29

(EX-1005, Figure 29 (annotated).)

Clamp 570 is configured to “reduce, when turned on, the maximum voltage developed in the system as the result of the ESD event” because it is “activated to prevent the voltage level attaining the voltage level that causes damage to the driver circuit 510.” (EX-1005, 18:58-18:60.) Because of conservation, reducing the magnitude of the voltage at VG_p reduces the total voltage developed in the system during an ESD event. (EX-1002 ¶ 209.)

g. [1f]: “enable circuitry configured to turn on the clamp device and instruct the control block to turn on the at least one of the one or more output transistor devices, in response to the ESD event;”

Ker Figure 29 teaches enable circuitry comprising ESD detection circuit 565. (EX-1002 ¶ 211.) ESD detection circuit 565 (light blue) is “connected between the output signal terminal 500 and... output signal port VG_p of the pre-driver circuit 515.” (EX-1005, 18:20-18:23.)



(EX-1005, Figure 29 (annotated).)

When an “ESD source having a negative polarity is coupled to... output signal terminal 500 [green] . . . ESD detection circuit 565 places [an] activation signal on... signal port VG_p” (orange), part of the control block. (EX-1005,

18:25-18:29.) The control block then activates output transistor Mp1 (dark blue). Thus, the enable circuitry (i.e., ESD detection circuit 565) is configured to “instruct the control block to turn on the at least one of the one or more output transistor devices.” (EX-1002 ¶ 211.)

ESD detection circuit 565 is also connected to the clamp device: clamp circuit 570 (purple). ESD detection circuit 565 is “configured to turn on the clamp device” because it turns on clamp device 570 at a certain voltage level. (EX-1002 ¶ 212.) Clamp circuit 570 then “activates and maintains the voltage level of... signal port VG_p.” (EX-1005, 19:33-19:35; EX-1002 ¶ 212.)

Both actions are “in response to the ESD event” because the disclosed circuit is explicitly an “ESD detection circuit” and it “senses the voltage level of the ESD source.” (EX-1005 Figure 28, 18:32-18:33; EX-1002 ¶ 213.)

h. [1g]: “wherein the second voltage rail is configured to provide power to the enable circuitry, and wherein the third voltage rail has a value below the first voltage rail.”

As explained in claim [1e], Ker discloses a second voltage rail, Vdd, under Microchip’s interpretation. By convention, Vdd powers the circuit, including the enable circuitry. (EX-1002 ¶ 215.)

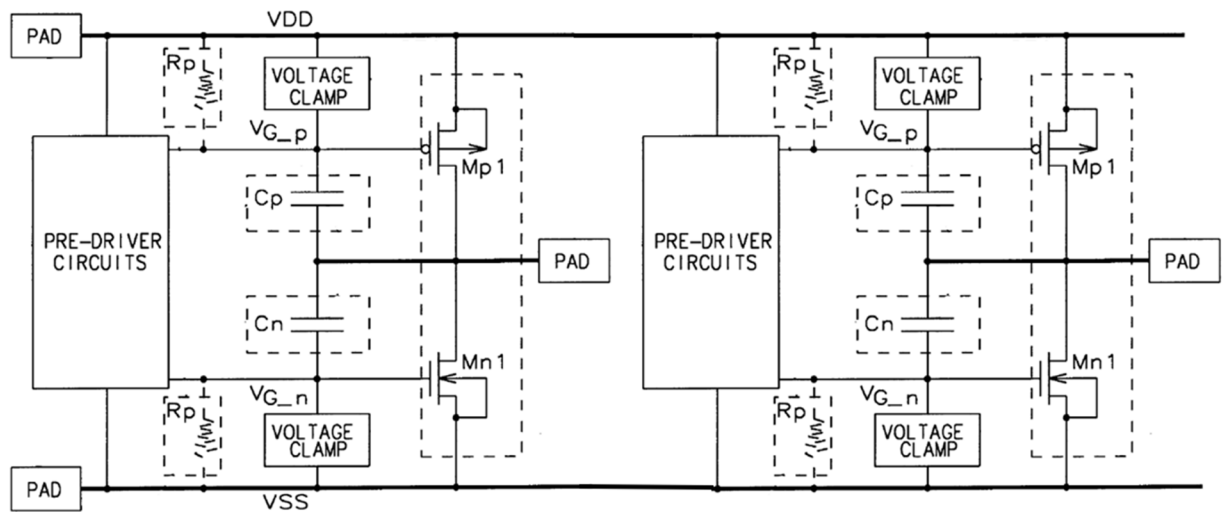
Ker also discloses a first and third voltage rail comprising Vdd and Vss, respectively. If the term “has a value below” refers to voltage, the limitation is

satisfied because the first voltage rail (i.e., Vdd) has a positive voltage whereas the Vss rail is ground. (EX-1002 ¶ 215.)

2) Claim 2: “The pad circuit of claim 1, wherein in turning on the at least one of the one or more output transistor devices when instructed, the control block couples an associated capacitance of the first voltage rail to the physical pad to share a charge developed in the system in response to the ESD event, to reduce the maximum voltage developed in the system as the result of the ESD event.”

As discussed in claim [1d], Ker’s control block—comprising signal port VG_p and other circuitry—turns on output transistor Mp1. Thus, Ker’s control block couples the first voltage rail, Vdd, to the physical pad 500. Because the voltage rail is a physical, conductive device, it has an associated capacitance. (EX-1002 ¶ 217.) This capacitance is then charged by the ESD energy, thereby reducing the maximum voltage developed in the system. (EX-1002 ¶ 217.)

Even if “associated capacitance” refers to the capacitance of other pads connected to the rail, Ker renders the claim obvious. As discussed in claim [1e], because integrated circuit devices typically had multiple I/O pads by 2007 (and each pad requires ESD protection), a POSITA would have included the Ker circuit at every I/O pad as shown below. (EX-1002 ¶ 218.)



Thus, during an ESD event, the “associated capacitance” of the Vdd rail is equal to the capacitance of the rail and all other I/O pads currently connected to the rail. (EX-1002 ¶ 219.)

3) Claim 3: “The pad circuit of claim 1, wherein the one or more output transistor devices are PMOS devices.”

Ker discloses that output transistor Mp1 is a PMOS device. (EX-1005, 17:24.)

4) Claim 4: “The pad circuit of claim 3, further comprising one or more NMOS devices coupled between the second node and the third voltage rail, wherein the NMOS devices and the PMOS devices are operable to operate together to drive the output signal at the second node, wherein the control block operates to turn off the NMOS devices during the ESD event.”

Ker discloses an NMOS output transistor Mn1 (blue) coupled between the second node (red) and the third voltage rail (i.e., Vss.)

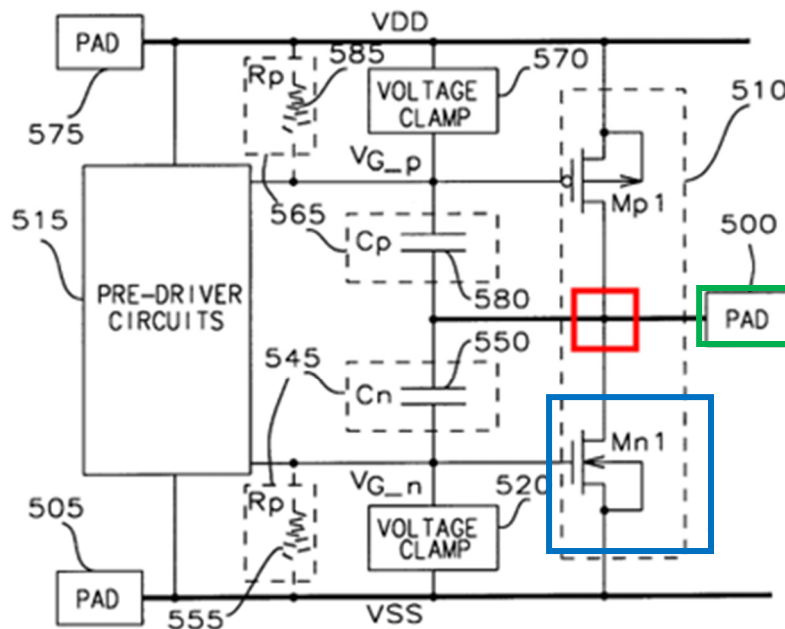


FIG. 29

(EX-1005, Figure 29 (annotated).)

Together, Mn1 and Mp1 drive an output signal by connecting the second node and pad 500 (green) to Vdd or Vss. During an ESD event of a certain polarity, the control block (i.e., VG_p, VG_n and other circuitry) turns on Mp1 and therefore turns off Mn1. (EX-1002 ¶ 222.)

5) Claim 5: “The pad circuit of claim 1, wherein the pad circuit and the physical pad are comprised in a digital input/output pad.”

A POSITA would understand that the Ker invention is comprised in a digital input/output pad. (EX-1002 ¶ 224.) Specifically, Ker discloses an input/output pad that is capable of outputting a high or low signal, making it digital.

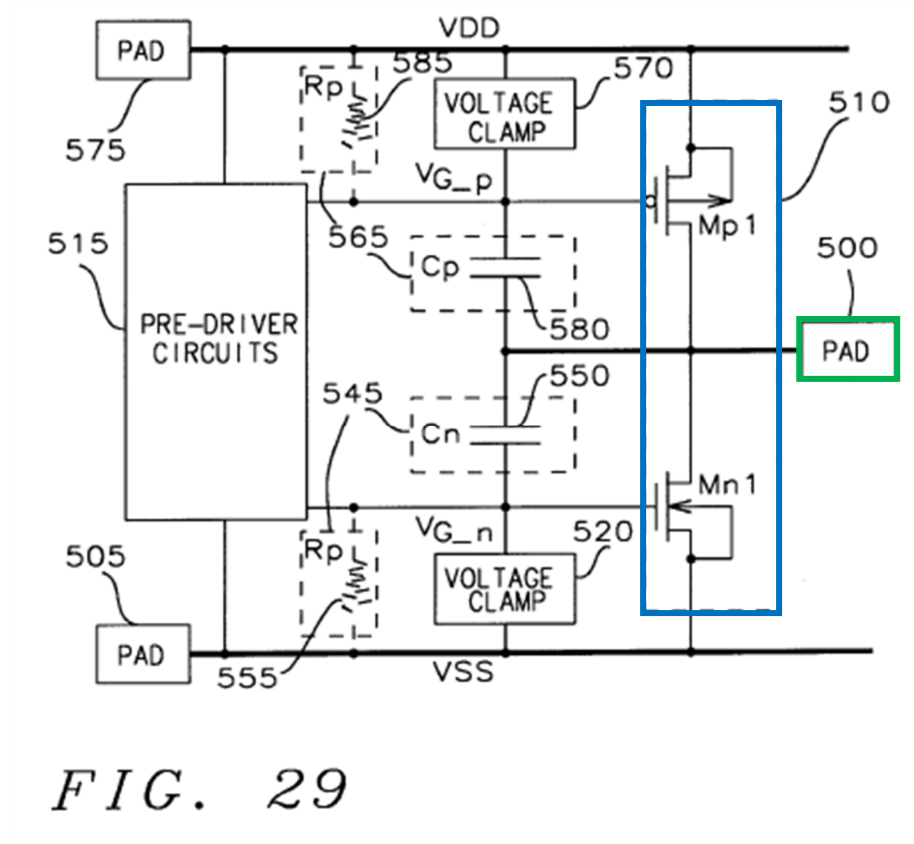
6) Claim 6

- a. Preamble: “A circuit configured to provide protection against electrostatic discharge (ESD) in a system comprising the circuit, the circuit comprising:”**

See discussion of claim 1, preamble.

- b. [6a]: “an output buffer configured to couple to a physical pad having capacitance, to drive at least one output signal at the physical pad”**

The '665 patent uses the term “output buffer” in the context of electrical circuits to denote signal driver circuits. (EX-1001, 4:27-4:30; EX-1002 ¶ 227.) Ker discloses a signal driver circuit in driver circuit 510 (dark blue). Driver circuit 510 is coupled to the physical pad 500 (green).

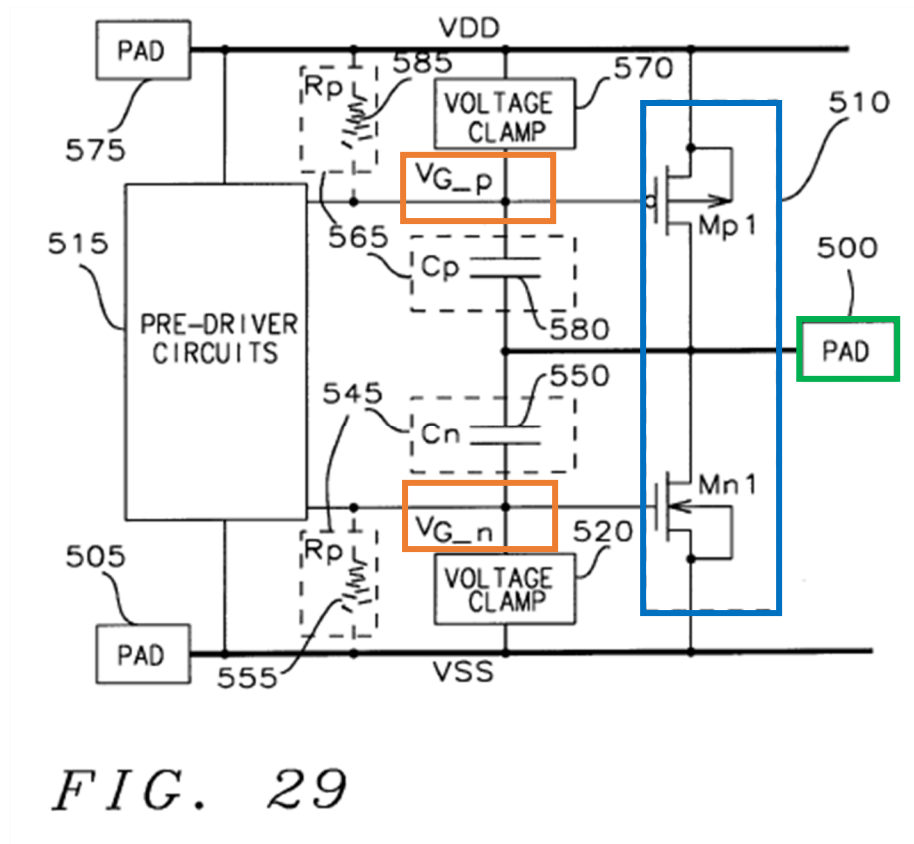


(EX-1005, Figure 29 (annotated).)

Driver circuit 510 is configured to drive at least one output signal at the physical pad it “create[s] the appropriate current and voltage levels from the electrical signals provided by the internal pre-driver circuits 515” and sends them to “output signal terminal 500.” (EX-1005, 18:5-18:9.)

c. [6b]: “a control block configured to control the output buffer;”

Ker teaches a control block comprising output signal ports VG_p and VG_n (orange) and other circuitry.



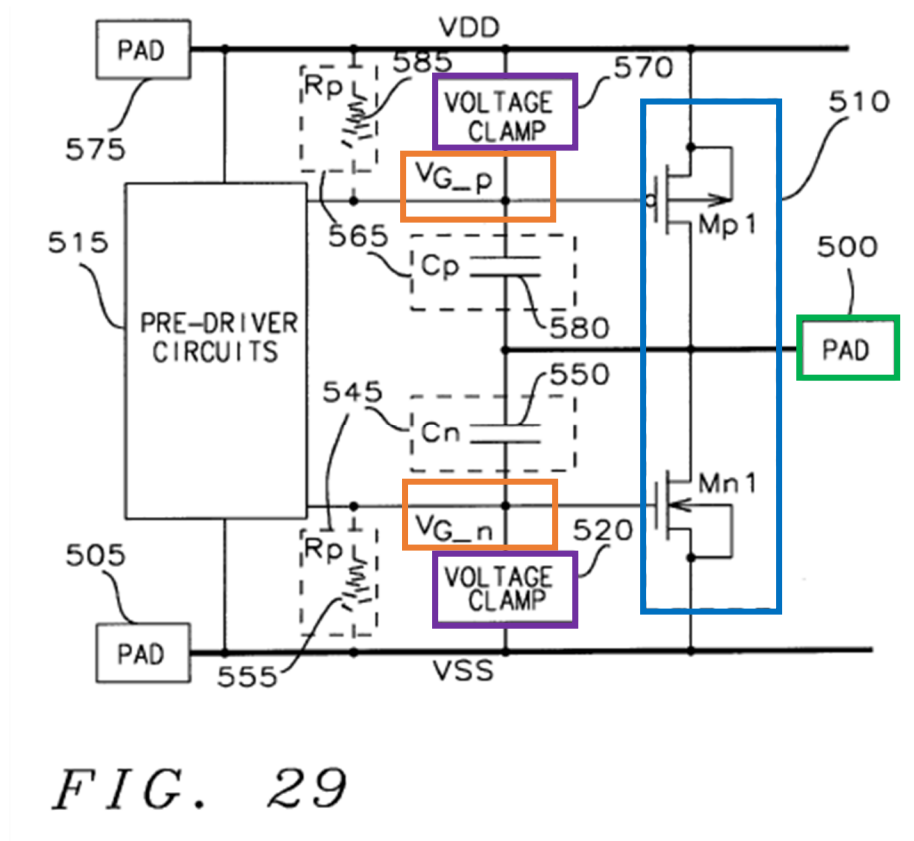
(EX-1005, Figure 29 (annotated).)

The output signal ports are connected to the gates of PMOS transistor Mp1 and NMOS transistor Mn1, respectively. (EX-1005, 19:6-19:8, 19:24-19:26.) Thus, they are configured to control the output buffer. (EX-1002 ¶ 230.)

d. [6c]: “a clamp device coupled between a first supply rail and a low supply rail, wherein the clamp device is configured to absorb, when turned on, a portion of an energy generated by the ESD event, to reduce the maximum voltage developed in the system as the result of the ESD event;”

Ker discloses a first supply rail comprising the Vdd rail and a low supply rail comprising the Vss rail. Under Microchip’s interpretation of coupled, which does

not require direct connections, voltage clamps 520 and 570 (purple) are coupled between these two rails. (EX-1002 ¶ 232; EX-1007, 44-46.)



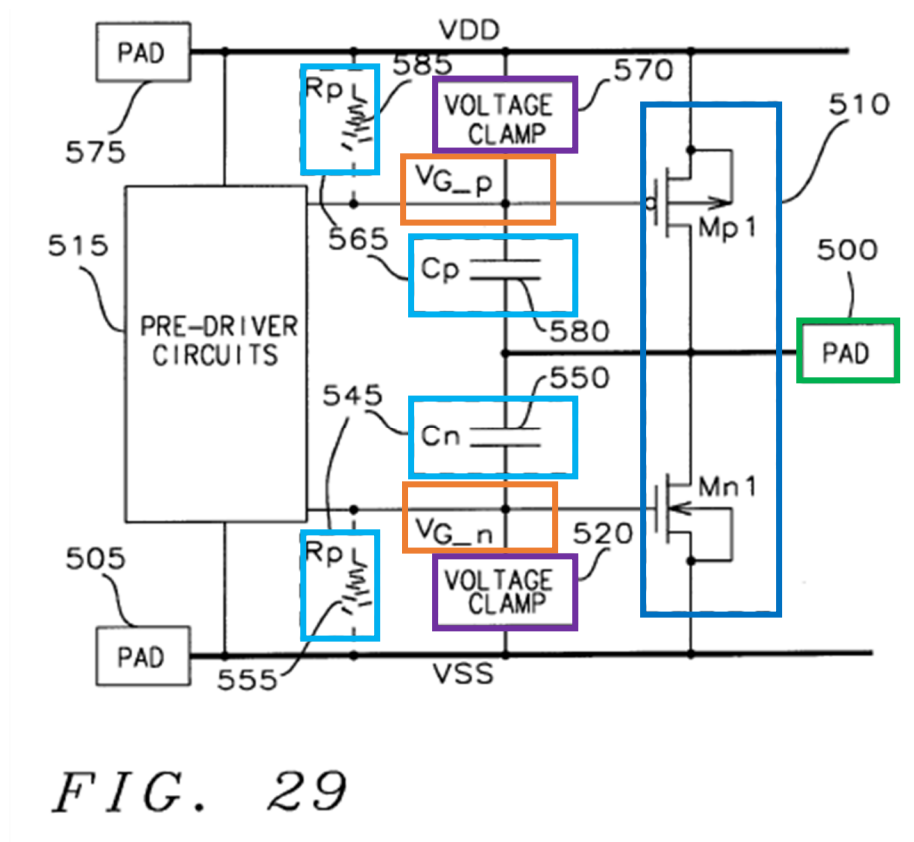
(EX-1005, Figure 29 (annotated).)

Voltage clamp 520 is “configured to absorb, when turned on, a portion of an energy generated by the ESD event” because when the voltage level at output signal port VG_n rises, voltage clamping circuit 520 is “activated to prevent the voltage level attaining the voltage level that causes damage to the driver circuit 510.” (EX-1005, 18:52-18:60.) Voltage clamp 570 behaves similarly. Thus, the

“maximum voltage developed in the system as the result of the ESD event” is reduced. (EX-1002 ¶ 233.)

- e. [6d]: “and a control circuit configured to instruct the control block to activate at least a portion of the output buffer when an ESD event occurs,”

Ker further discloses a control circuit comprising ESD detection circuits 545 and 565 (light blue).



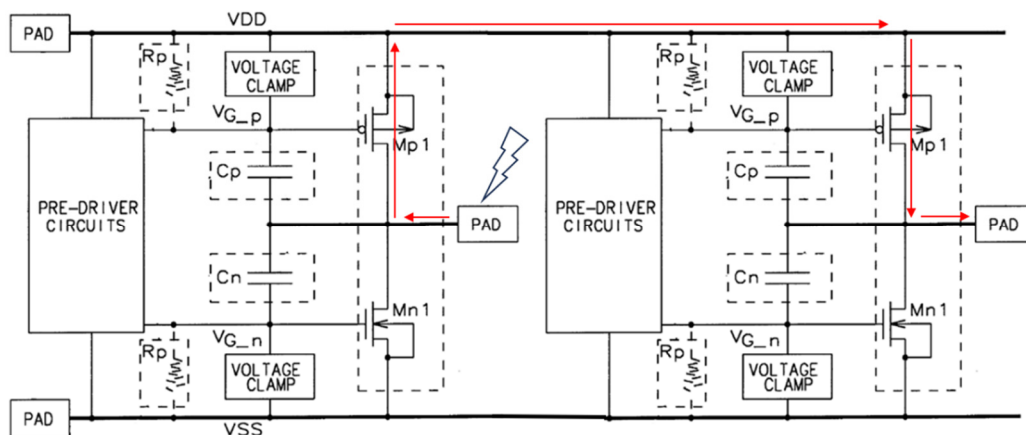
(EX-1005, Figure 29 (annotated).)

This control circuit instructs the control block—VG_p, VG_n, and other circuitry—to activate at least a portion of the output buffer (dark blue) during an

ESD event. “If an ESD source . . . is coupled to the output signal terminal 500 . . . ESD detection circuit 565 . . . applies an activation signal to the first output signal port VG_n.” Similarly, ESD detection circuit 565 places an activation signal at VG_p. Alternatively, “the second ESD detection circuit 565 . . . places a second activation signal at the second output signal port,” (i.e., VG_p.) (EX-1005, 18:24-18:34.)

f. [6e]: “[the control circuit configured] to charge the pad capacitance to reduce a maximum voltage developed in the system as a result of the ESD event”

As discussed above, a POSITA would repeat the Ker circuit at every I/O pad. When the control block activates a portion of the output buffer, pad 500 is connected to either Vdd or Vss through transistor Mp1 or Mn1, respectively. This causes the ESD energy to flow to the rail where it charges the pad capacitance of any connected I/O pad.



Because capacitors store energy, the maximum voltage developed in the system is reduced. (EX-1002 ¶ 239.)

g. [6f]: “wherein the control circuit is further configured to turn on the clamp device in response to the ESD event;”

Ker’s control circuit—ESD detection circuits 545 and 565—also turn on a voltage clamp during an ESD event. (EX-1002 ¶ 241.)

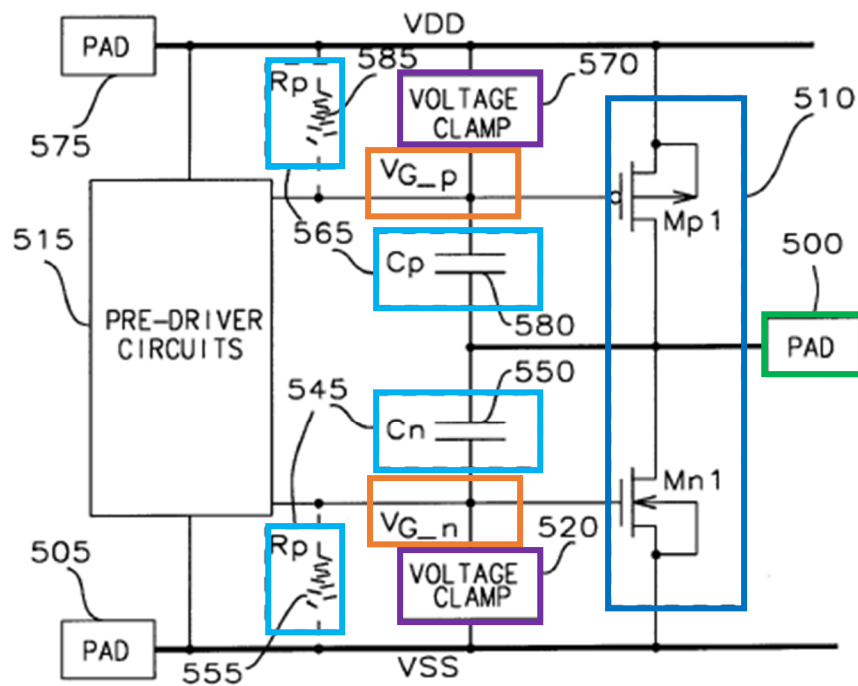


FIG. 29

(EX-1005, Figure 29 (annotated).)

Specifically, the ESD detection circuits (light blue) send a high voltage signal to the signal ports VG_n and VG_p (orange) when an ESD event occurs at pad 500 (green). “[W]hen the voltage levels of . . . VG_n and VG_p begin to

approach the voltage level at which the driver circuit 510 can be damaged, the appropriate voltage clamping circuits 520 and 570 are activated.” (EX-1005, 18:54-18-60.)

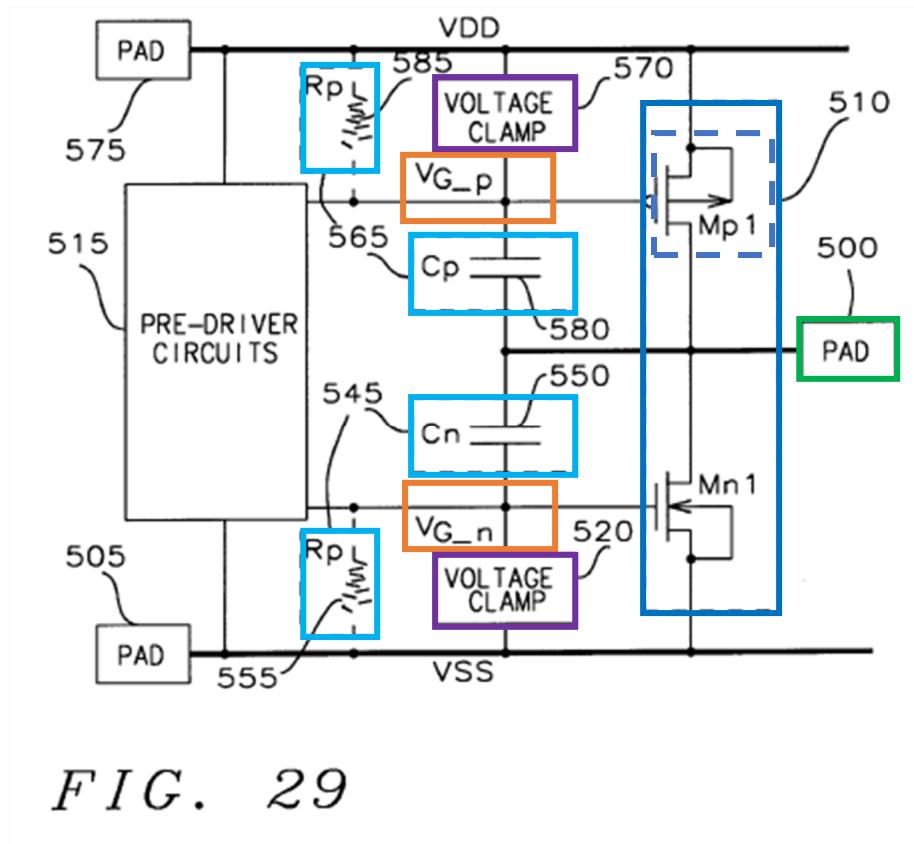
h. [6g]: “wherein the first supply rail is configured to provide power to the control circuit”

As discussed above in claim [6c], Ker’s first supply rail is Vdd. By convention, the Vdd rail provides power to the entire circuit, including the control circuit. (EX-1002 ¶ 242.)

7) Claim 7:

a. [7a]: “The circuit of claim 6, wherein the output buffer comprises one or more PMOS devices coupled between a second supply rail and the physical pad; and”

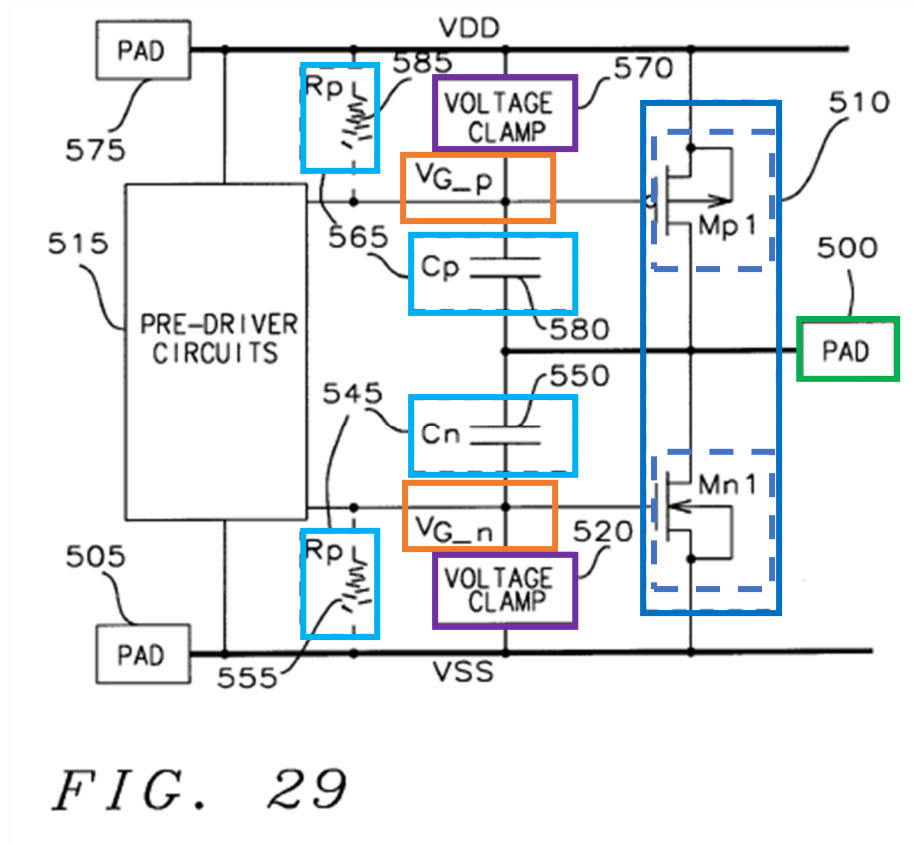
As discussed above, Ker discloses an output buffer in driver circuit 510. Applying Microchip’s interpretation, wherein the first and second rail can be the same rail, Vdd is also the second voltage rail. (EX-1007, 67.) The output buffer comprises one or more PMOS devices coupled between Vdd and the physical pad (green) because of output transistor Mp1 (dashed dark blue).



(EX-1005, Figure 29 (annotated).)

- b. [7b]: “one or more NMOS devices coupled between the physical pad and the low supply rail wherein the low supply rail has a value less than the second supply rail.”**

Ker’s output buffer, driver circuit 510 (dark blue) comprises one or more NMOS devices because output transistor Mn1 (dashed dark blue) is an NMOS device. As discussed in claim [6c], Ker discloses a low supply rail comprising Vss. Output transistor Mp1 (dashed dark blue) is connected between pad 500 (green) and Vss.



(EX-1005, Figure 29 (annotated).)

As discussed above, Ker discloses a second supply rail Vdd. By convention, Vss is ground and Vdd has positive voltage, so the low supply rail has a value “less than” the second supply rail. (EX-1002 ¶ 247.)

- c. [7c]: “wherein in activating at least a portion of the output buffer when the ESD event occurs, the control block enables one or more of the one or more PMOS devices.”**

As discussed in claim [6b]-[6e], the control block enables a portion of the output buffer. During some ESD events, this includes activating PMOS device Mp1. (EX-1005, 18:24-18:36; EX-1002 ¶¶ 249-250.)

- 8) Claim 8: “The circuit of claim 7, wherein in activating at least a portion of the output buffer when the ESD event occurs, the control block disables one or more of the one or more NMOS devices.”**

As discussed above, the control block activates Mp1 during some ESD events. Conversely, Mn1 is turned off because it is an N-type device (EX-1002 ¶ 251.)

- 9) Claim 9: “The circuit of claim 7, wherein the one or more PMOS devices comprise a plurality of PMOS devices coupled in parallel between the second supply rail and the physical pad, and the one or more NMOS devices comprise a plurality of NMOS devices coupled in series between the physical pad and the second supply rail.”**

Ker renders this claim obvious because it was well-known that a single PMOS transistor can be replaced with multiple PMOS transistors in parallel to reduce the current through any one transistor. (EX-1002 ¶¶ 252.) Similarly, it was common practice to include multiple NMOS devices in series, which can protect sensitive NMOS devices by reducing the drain-source voltage.⁹ (EX-1002 ¶ 252.)

⁹ This remains true whether the NMOS devices are connected between the physical pad and the second supply rail, as claimed, or the first supply rail, low supply rail, or another location.

10) Claim 10: “The circuit of claim 6, wherein the clamp device is one of: a PMOS device having its source terminal coupled to the first supply rail, its drain terminal coupled to the low Supply rail, and its gate terminal coupled to the control circuit; or an NMOS device having its drain terminal coupled to the first supply rail, its source terminal coupled to the low supply rail, and its gate terminal coupled the control circuit.”

As discussed above, Figure 29 discloses two “voltage clamp devices.” (EX-1005, Figure 29.) At the time, a conventional voltage clamp comprised of a MOS transistor. (EX-1002 ¶ 255.) In fact, another embodiment of Ker (shown in Figure 33), discloses an ESD clamp comprising an NMOS transistor configured between V_{dd} and V_{ss}.

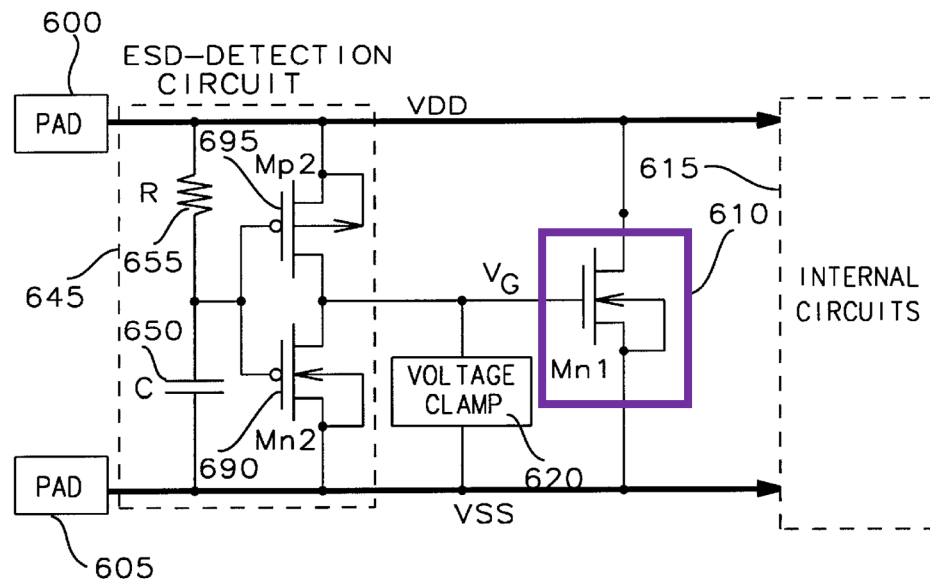


FIG. 33

(EX-1005, Figure 33 (annotated).)

Given the generic disclosure of Figure 29, a POSITA would have understood that the Ker ESD clamp can take multiple forms. (EX-1002 ¶ 254.) It would have been obvious to a POSITA (with a reasonable expectation of success) to use MOS transistors as the voltage clamps. In fact, a POSITA would have been motivated to connect the transistors between the pad and a rail for greater power dissipation, and the resulting configuration would satisfy claim 10. (EX-1002 ¶ 256.)

11) Claim 11: “The circuit of claim 6, wherein the first supply rail is configured to provide increased power during the ESD event.”

As discussed in claim 6, during an ESD event an output transistor connects pad 500 to a supply rail. This allows the excess ESD energy to flow to the rail, increasing the magnitude of the voltage and providing increased power. (EX-1002 ¶ 258.)

12) Claim 12: “The control circuit of claim 6, wherein in instructing the control block to activate at least a portion of the output buffer when an ESD event occurs, the control circuit is operable to provide a control signal to the control block in response to the ESD event.”

As discussed in claim 6, Ker discloses a control circuit that instructs the control block to activate at least a portion of the output buffer. This control circuit—ESD detection circuits 545 and 565—also provides a control signal to the

control block (i.e., VG_n, VG_p, and other circuitry) in response to the ESD event because the circuit “places the first activation signal” at VG_n or “the second activation signal” at VG_p depending on the polarity of the ESD event. (EX-1005, 19:8-19:12, 19:25-19:29.)

13) Claim 13: “The circuit of claim 6, wherein the control circuit is configured to receive a control signal corresponding to a time constant, wherein the time constant corresponds to a specified slope, wherein the control signal is configured to trigger the control circuit if a slope of a Voltage pulse developed in the system as a result of the ESD event is greater than or equal to the specified slope.”

A POSITA would understand the limitations of this claim to describe an RC circuit. (EX-1002 ¶ 261.) Ker's control circuit—ESD detection circuits 545 and 565—consists of two RC circuits. For example, capacitor Cn 550 and resistor Rn 555 “form the first ESD detection circuit.” (EX-1005, 19:40-41, Figure 29.) The RC circuit satisfies this claim because it triggers the control circuit when the slope of the ESD voltage exceeds the circuit's time constant. (EX-1002 ¶¶ 262-263.)

To any extent the claim does not allow the control circuit to both generate and receive the control signal, Ker still renders the claim obvious. It would have been obvious to a POSITA that any number of intermediate devices could be added between the RC circuit and the output transistor while still achieving the same result. (EX-1002 ¶ 264.) In fact, Ker discloses embodiments where additional

circuitry is placed between the RC circuit and the output buffer. In such a configuration, the additional circuitry is the control circuit, and it receives a control signal from the RC circuit. (EX-1002 ¶ 264.)

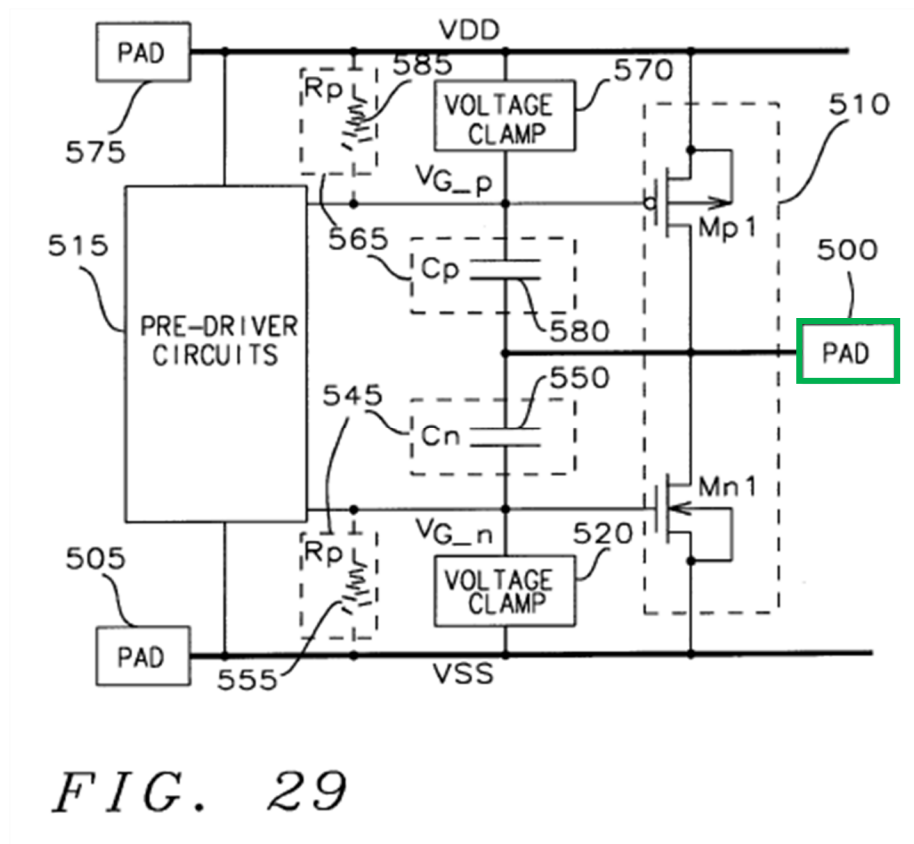
14) Claim 14

a. Preamble: “A system comprising:”

Ker discloses a system because it teaches an ESD protection circuit... to dissipate an electrostatic charge.” (EX-1005, Abstract.)

b. [14a]: “one or more pads, each pad comprising: a respective physical pad having respective capacitance;”

Ker discloses “pad 500,” an output signal terminal (green).



(EX-1005, Figure 29 (annotated).)

A POSITA would understand that, in the context of integrated circuits, pad 500 is a physical pad. (EX-1002 ¶ 268.) Because pad 500 is a physical, conductive device, it has capacitance. (EX-1002 ¶ 268.)

- c. [14b]: “[each pad comprising:] a respective clamp device configured to absorb, when turned on, a portion of an energy generated by an ESD event, to thereby further reduce the maximum voltage developed in the system as the result of the ESD event; and”

Ker discloses two clamp devices for each respective pad: voltage clamp devices 520 and 570 (purple). (EX-1005, 18:43-18:50.)

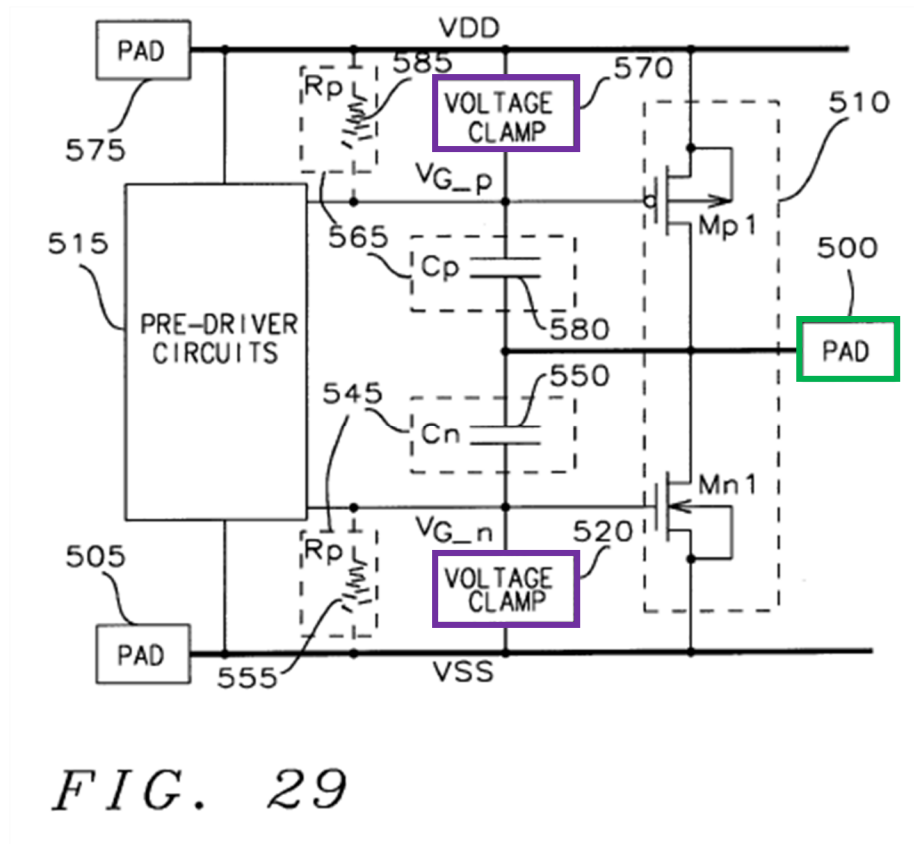


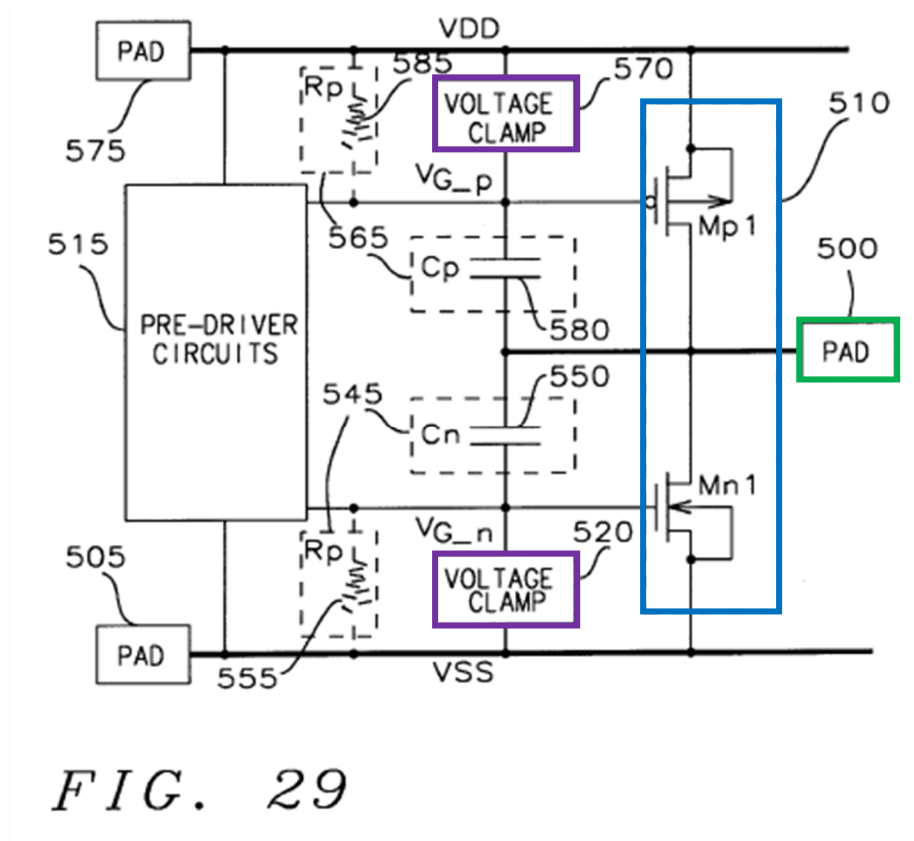
FIG. 29

(EX-1005, Figure 29 (annotated).)

These clamps are “configured to absorb, when turned on, a portion of an energy generated by an ESD event” because the clamps are activated when an ESD causes dangerous voltage levels, reducing the maximum voltage in the circuit. *See* discussion of claim [6c].

- d. [14c]: “[each pad comprising:] a respective pad circuit comprising: a respective output buffer coupled to the respective physical pad, and operable to drive at least one respective output signal at the respective physical pad; and”

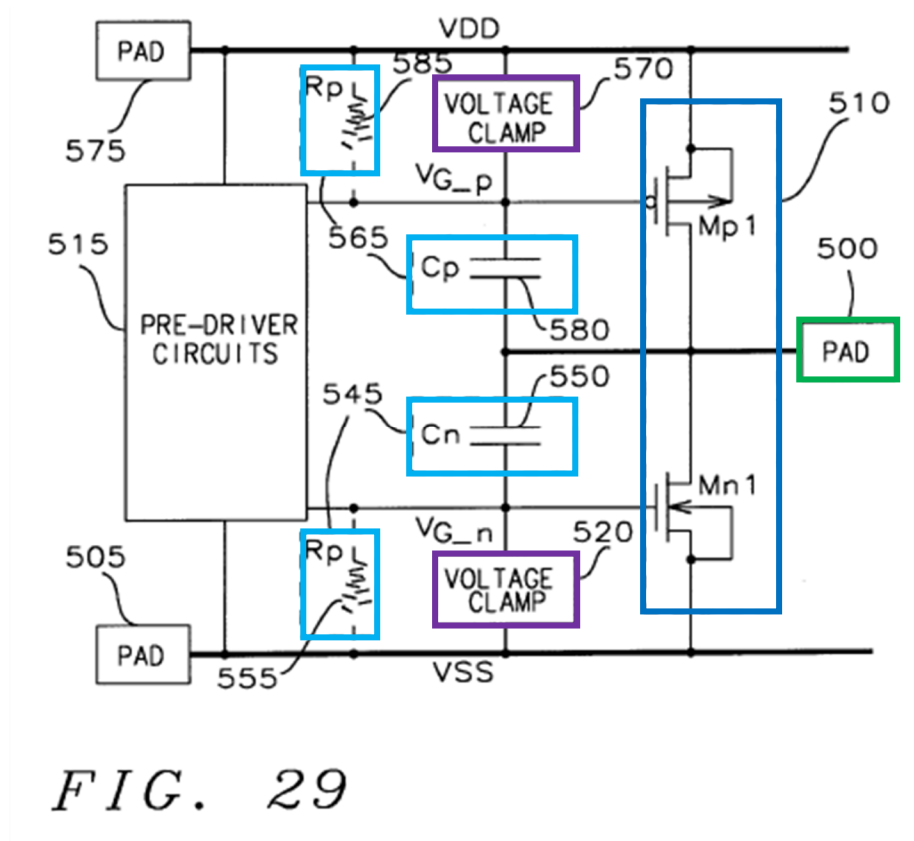
Ker teaches that the pad has “a respective pad circuit” as shown in Figure 29. The respective circuit includes an output buffer coupled to the pad as discussed in Claim [6a].



(EX-1005, Figure 29 (annotated).)

- e. [14d]: “[the respective pad circuit comprising:] respective control circuitry operable to: activate at least a portion of the respective output buffer in response to an ESD event to charge the respective pad capacitance to reduce a maximum voltage developed in the system as a result of the ESD event; and”**

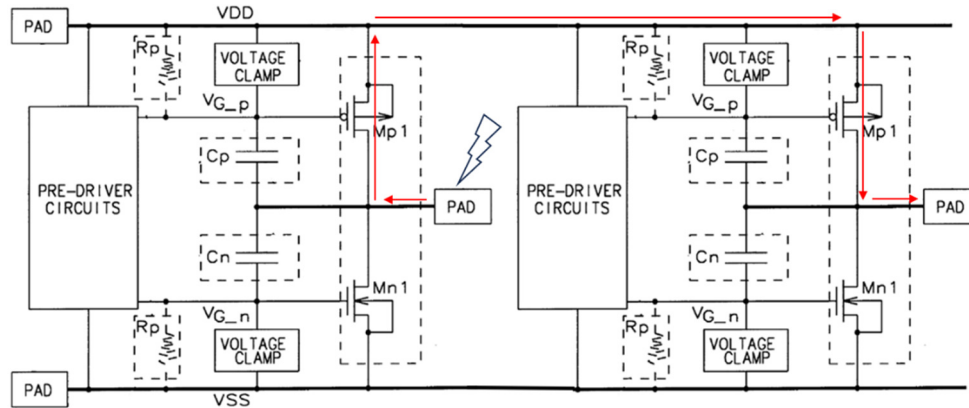
As discussed in claims [6d] and [6e], Ker discloses control circuitry—ESD detection circuits 545 and 565 (light blue)--operable to activate at least a portion of the output buffer in response to the ESD event.



(EX-1005, Figure 29 (annotated).)

When the control circuitry activates one of the output transistors Mp1 or Mn1, the ESD energy flows onto Vdd or Vss, respectively. Because a POSITA would repeat the Ker circuit at every I/O pad for ESD protection, the energy can then flow to other pad circuits. (EX-1002 ¶ 276.) This charges the pad capacitance

of any pad connected to the rail, thereby reducing the maximum voltage developed in the system due to the ESD event. (EX-1002 ¶ 276.)



f. [14e]: “[the respective control circuitry operable to:] turn on the clamp device in response to the ESD event.”

Ker discloses this limitation because, as discussed in claim [6d], Ker's control circuitry, ESD detection circuits 545 and 565 (light blue), is operable to turn on the clamp devices 520 or 570 (purple) in response to an ESD event.

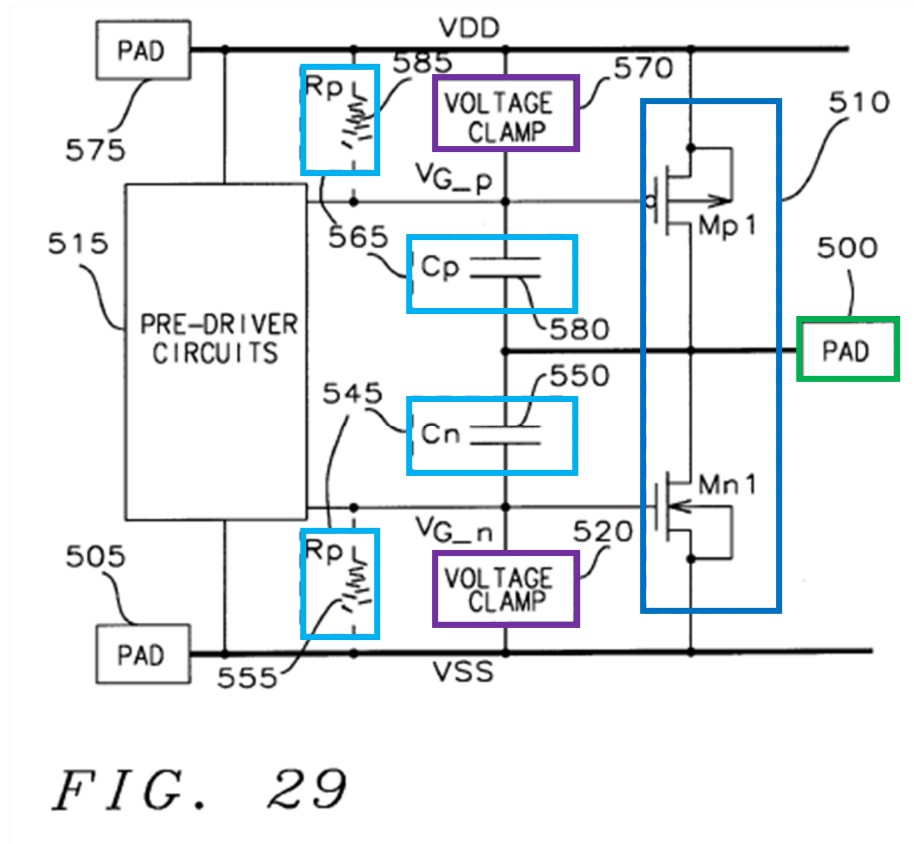


FIG. 29

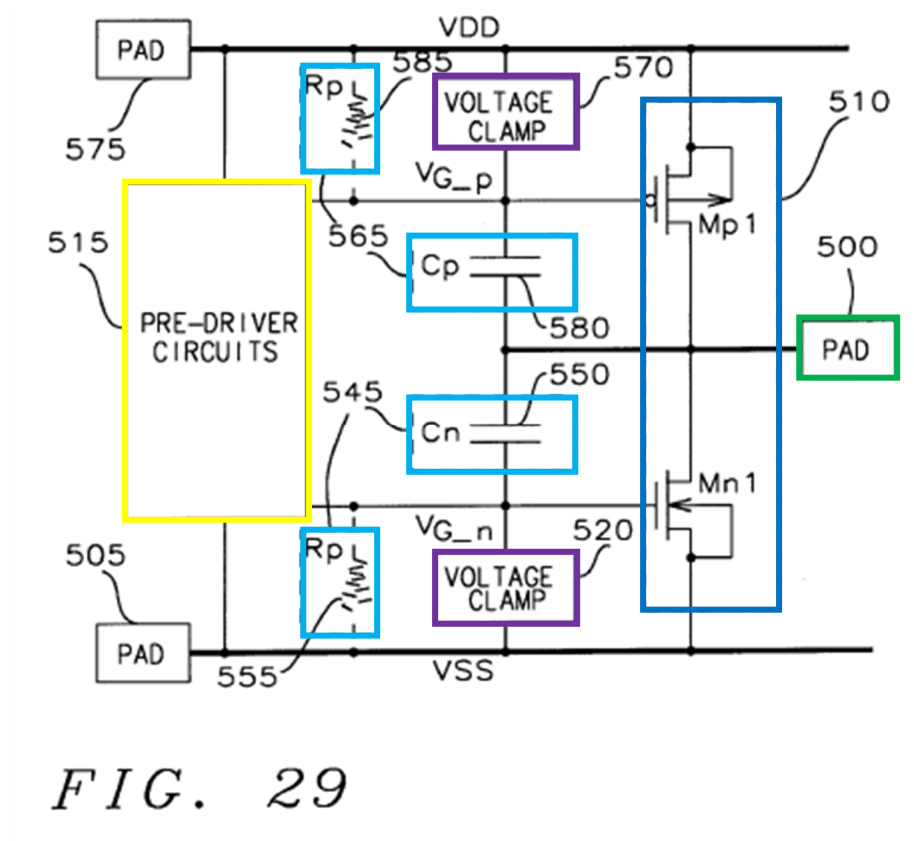
(EX-1005, Figure 29 (annotated).)

- 15) **Claim 15:** “The system of claim 14, further comprising functional circuitry coupled to the respective pad circuit of at least one of the one or more pads, wherein the functional circuitry is operable to generate the at least one respective output signal driven by the respective pad circuit of the at least one of the one or more pads.”

Ker renders this limitation obvious because a POSITA would understand that pre-driver circuits 515 (yellow) require an output signal. (EX-1002 ¶ 279.)

Various functional circuitries to create that signal, such as a microcontroller, were

well-known in the art. (EX-1002 ¶ 279.). The output signal is then driven by the pad circuit to create the final output signal at pad 500. (EX-1002 ¶ 279.)



(EX-1005, Figure 29 (annotated).)

- 16) Claim 16: “The system of claim 14, further comprising a first supply rail configured to provide increased power in accordance with the ESD event, and further configured to power the respective control circuitry of the respective pad circuit of each pad.”**

As discussed in claim 6, during some ESD events output transistor Mp1 connects pad 500 to the first supply rail: Vdd. This allows the excess ESD energy to flow to the Vdd rail, so the rail provides increased power during the ESD event.

- 17) Claim 17: “The system of claim 16, further comprising a second supply rail configured to power the respective output buffer of the respective pad circuit of each pad.”**

Under Microchip’s apparent interpretation, wherein the first and second supply rails can be the same rail, Ker discloses a second supply rail Vdd. (EX-1002 ¶ 282; EX-1007, 96-97) This rail provides power to the output buffer, driver circuit 510.

- 18) Claim 18: “The system of claim 16, wherein the respective control circuitry of the respective pad circuit of each pad is configured to receive a respective control signal corresponding to a time constant, wherein the time constant corresponds to a specified slope, wherein the respective control signal is configured to trigger the respective control circuitry if a slope of a voltage pulse developed in the system as a result of the ESD event is greater than or equal to the specified slope.”**

See claim 15.

VI. NOTICES AND STATEMENTS

Pursuant to 37 C.F.R. § 42.8(b)(1), Aptiv Services US, LLC, Aptiv Technologies AG, and Aptiv Technologies Limited are the real parties-in-interest for Petitioner.

Pursuant to 37 C.F.R. § 42.8(b)(2), Petitioner identifies the following related matter: the '665 patent is asserted in *Microchip Technology Inc. v. Aptiv Services US, LLC*, No. 23-cv-778-JDW (DED).

Pursuant to 37 C.F.R. § 42.8(b)(3), Petitioner identifies the following counsel (and a power of attorney accompanies this Petition).

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Pursuant to 37 C.F.R. § 42.8(b)(4), service information for lead and back-up counsel is provided above. Petitioner consents to electronic service by email to Aptiv-Microchip-PTAB@mofo.com.

Pursuant to 37 C.F.R. § 42.104(a), Petitioner certifies that the '665 patent is available for *inter partes* review and that Petitioner is not barred or estopped from requesting an *inter partes* review challenging the patent claims on the grounds identified in this Petition.

The USPTO is authorized to charge any required fees, including the fee as set forth in 37 C.F.R. § 42.15(a) and any excess claim fees, to Deposit Account No. **03-1952** referencing Docket No. **28640-00000.06**.

Dated: April 15, 2024

Respectfully submitted,

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Certification of Word Count (37 C.F.R. § 42.24)

I hereby certify that this Petition for *Inter Partes* Review has 13,992 words (as counted by the “Word Count” feature of the Microsoft Word™ word-processing system), exclusive of “a table of contents, a table of authorities, mandatory notices under § 42.8, a certificate of service or word count, or appendix of exhibits or claim listing.”

Dated: April 15, 2024

By /Mehran Arjomand/
Mehran Arjomand

Certificate of Service (37 C.F.R. § 42.6(e)(4) and 42.205(a))

I hereby certify that the attached Petition for *Inter Partes* Review and supporting materials were served as of the below date by UPS, which is a means at least as fast and reliable as U.S. Express Mail, on the Patent Owner at the correspondence address indicated for U.S. Patent No. 7,564,665.

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