

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APTIV SERVICES US, LLC,
Petitioner,

v.

MICROCHIP TECHNOLOGY INC.,
Patent Owner.

Case No. IPR2024-00803
U.S. Patent No. 7,564,665

PATENT OWNER'S PRELIMINARY RESPONSE

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LISTING OF EXHIBITS

Exhibit	Description
2001	Aptiv's District Court Invalidity Contentions (December 8, 2023)
2002	C. Ito, K. Banerjee, and R. Dutton, "Analysis and Design of ESD Protection Circuits for High-Frequency/RF Applications," Proceedings of the International Symposium on Quality of Electronic Design, pp. 117-122 (2001).
2003	Expert Declaration of Dr. Daniel Foty
2004	<i>Curriculum Vitae</i> of Dr. Daniel Foty

I. INTRODUCTION

Patent Owner Microchip Technology Inc. submits this Preliminary Response to Aptiv Services US, LLC's Petition for *Inter Partes* Review (Paper 1, the "Petition" or "Pet.") of U.S. Pat. 7,564,665 (the "'665 patent"). The Board should deny institution for two reasons, each of which alone warrants denial.

First, Petitioner fails to establish a reasonable likelihood of success that any Challenged Claim (*i.e.*, claims 1-18) is unpatentable as obvious. The '665 patent contains three independent claims (1, 6, and 14). Petitioner asserts three grounds of invalidity against all claims: (1) single-reference obviousness based on Verhaege (EX1004); (2) obviousness based on Verhaege combined with Miller (EX1006); and (3) single reference obviousness based on Ker (EX1005). Pet., 11. Notably, Petitioner's grounds are all obviousness. This is significant because the precise point of novelty—detecting an ESD event on another pad and activating circuitry in the claimed I/O cell to share ESD charge—is lacking in each of Verhaege, Miller, and Ker. Indeed, Petitioner makes no assertion that unmodified versions of Verhaege, Miller, or Ker disclose ESD charge-sharing among pads.

Rather, Petitioner modifies Verhage and Ker to construct multi-cell embodiments that still fail to meet the claims because, in each instance, the resulting I/O cells lack control circuitry that detect an ESD event *on a different pad* and turn on the necessary output transistor(s) to allow ESD charge-sharing

between pads. For Grounds 1 and 3, Petitioner simply assumes pad sharing occurs, but importantly, fatally overlooks that for such sharing to occur, circuitry must turn on a particular transistor, *viz.*, the output PMOS transistor. For Ground 2, Petitioner draws a made-up circuit to purportedly enable ESD charge-sharing, but fatally fails to show a POSITA would have had a reasonable expectation of success in implementing Petitioner's circuit.

What's more, a single claim construction (*see* §IV.B) confirming the claims require control circuitry that detects an ESD event on another pad and activates circuitry in its own I/O cell to share the ESD charge is separately dispositive of all Grounds. *See* §§V.A.2, V.B.2, and V.C.2. Because this fundamental concept is absent from all of Petitioner's grounds, the Board should deny institution. This Preliminary Response is supported by the expert declaration of Dr. Daniel Foty (EX2003).

Second, the Board should exercise its discretion to deny institution under 35 U.S.C. §314(a) because Petitioner is pursuing the same Verhaege, Miller, and Ker grounds in district court and offered no stipulation, thus teeing up the very type of duplicative litigation *inter partes* review was intended to avoid.

II. BACKGROUND¹

A. **Electrostatic Discharge (ESD)**

Before discussing the invention '665 patent's invention, it is helpful to have a basic understanding of electrostatic discharge (ESD). Petitioner defines ESD as “the sudden flow of electricity between differently-charged objects.” Pet., 1. But it is even more intuitive than that, as most lay persons have experienced ESD firsthand. For example, a common science experiment in many schools involves rubbing a balloon on one's hair or dragging one's feet across carpet to create an electrical charge. Then, when you touch another person (or a metal item such as a

¹ Petitioner states a POSITA “would have at least a Master's degree in electrical engineering, computer engineering, or a related field and three to five years of experience in integrated circuit design.” Pet., 10. Patent Owner disagrees with this excessively high level of ordinary skill in the art and maintains a POSITA would have had a bachelor's degree in electrical engineering or an equivalent technical degree and two years of experience in mixed-signal (*i.e.*, analog/digital) circuit design. EX2003, ¶¶30-34. Notably, the POSITA standard proffered by Petitioner's expert aligns more closely with Patent Owner's definition than Petitioner's. *See* EX1002, ¶51. But the Board need not resolve this dispute now as it should deny institution under either party's definition. EX2003, ¶35.

door knob), it provides an unpleasant “shock” when the electrical charge is discharged. EX2003, ¶42. This is shown below, on both a small scale (doorknob) and large scale (lightning).



That these two occurrences represent the same phenomenon but at two vastly different scales was first recognized—and then demonstrated—by Benjamin Franklin in 1752. In both cases, separate charge regions build up until the dielectric material (air) between them can no longer sustain the induced electric field, at which point the dielectric material breaks down and current flows through the breakdown path. In the case of “doorknob shock,” the electric field intensity increases as the distance between the hand and the doorknob decreases. At some point, the dielectric can no longer withstand the voltage difference, and a lightning-like spark will occur. EX2003, ¶42.

In 2007, integrated circuits in various shapes and sizes were well-known. Regardless of form factor, practically all packaged integrated circuits contained

metallic contacts, terminals, or pins used for interfacing with the outside world and/or other electronic components or chips. Some examples are shown below:



www.electronicsforu.com/resources/dip-smd-qfp-bga-ic-packages; see also

EX1001, 1:11-13 (“Integrated circuits (ICs) are typically manufactured with external connections—most commonly pins—for coupling to external devices, systems, signals and/or power supply voltages.”); *id.*, 1:49-51 (“ESD events often occur across the silicon circuits attached to the package terminals, or pins, of an IC”); EX2003, ¶¶43-44.

The ’665 specification explains that ESD often “originates from build up of static charge near the IC or on a human handling the IC.” EX1001, 1:22-23. ESD events are typically characterized by a high transient voltage (*e.g.*, thousands of volts) and high transient current (*e.g.*, several amperes). EX2003, ¶43. Though short-lived, ESD events are potentially destructive to sensitive electronics,

including integrated circuits which may be exposed to, *e.g.*, human touch. *See* EX1001, 1:23-25. As a result, “ESD poses a serious problem for semiconductor devices as it can potentially lead to malfunction and/or the destruction of an entire IC.” *Id.*, 1:26-28.

B. Conventional ESD Solutions

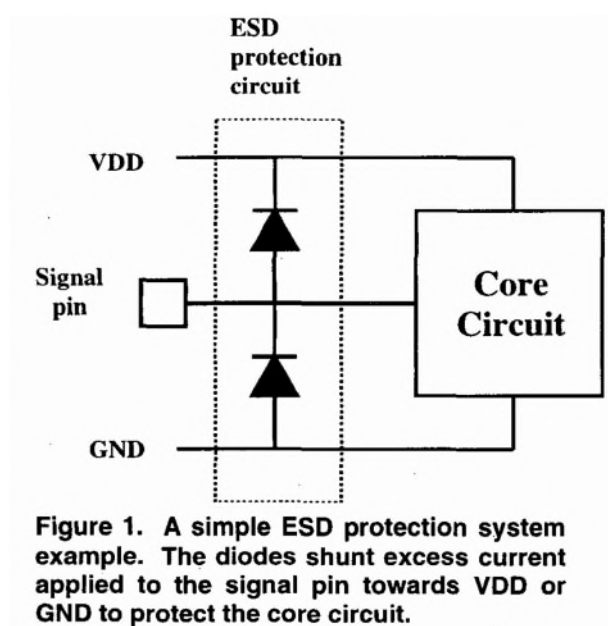
For the reasons noted above, it is important to protect integrated circuits against ESD events and a variety of techniques have been used. Various ESD protection circuits were known, such as those disclosed in Verhaege (EX1004), Miller (EX1006), and Ker (EX1005). *See* EX1001, 2:8-11 (“In general, various techniques for improving ESD performance, including the use of semiconductor controlled rectifiers (SCRs), snapback devices, and rail clamps, have been devised, published and/or patented.”). ESD protection circuitry should have minimal (if any) effect on the function, operation, speed, etc. of the underlying circuitry it protects. EX2003, ¶45. One commonly-used generalized method of ESD protection is to shunt² transient energy (*viz.*, current) from an ESD event away

² In the electrical context, the term “shunt” simply means “provid[ing] a low-resistance path for an electrical current in a circuit. It is typically used to divert current away from a system or component.”

[https://en.wikipedia.org/wiki/Shunt_\(electrical\)](https://en.wikipedia.org/wiki/Shunt_(electrical)).

from the protected circuitry to a power supply rail. *See, e.g.*, EX2002, 1 (“The protection circuit may be composed of various devices, such as diodes, transistors, or silicon controlled rectifiers (SCRs), but in all cases, these devices shunt ESD current coming from the signal pin to the power supply rails and away from the core circuit.”); EX2003, ¶¶46-47.

Power supply rails provide a readily available destination for ESD charge. EX2003, ¶46. Indeed, power rails are intended and designed to function as current sources (for providing current) and/or current sinks (for disposing of excess current). *Id.* A simple and commonly-known ESD protection mechanism (shown below) involves using two diodes, configured to shunt current as described above.



EX2002, 1; *see also* EX2003, ¶47.

For a positive-voltage ESD strike on the signal pin, the upper diode will turn

on and provide a shunt path to the VDD power supply rail. EX2003, ¶47.

Conversely, for a negative-voltage ESD strike on the signal pin, the lower diode turns on and provides a shunt path to the GND (or VSS) power supply rail. *Id.*

The core circuit is thus provided some protection from ESD damage. Notably, this ESD protection circuitry is added to protect a particular/individual I/O cell. *Id.*, ¶48.

C. The Problem to be Solved

The '665 patent generally relates to “the field of integrated circuit design,” and more particularly to “circuitry for providing protection against damaging effects of Electrostatic Discharge (ESD).” EX1001, 1:6-9.

The '665 specification explains that existing ESD techniques struggled to provide sufficient ESD protection. *See* EX1001, 2:3-6. This was due, in part, to the relentless advance of Moore’s law in which “the physical dimensions of circuit elements in many ICs ... have seen a decrease with each new generation of manufacturing process” that “adverse[ly] impact[ed]” ESD problems “by increasing the sensitivity of circuit elements, such as field effect transistors (FETs), to high electric fields.” *Id.*, 1:28-35; *see also id.*, 1:18-21 (“As IC devices increase in density and operating supply voltage levels decrease, the IC devices may become more sensitive to the effects of electrostatic discharge (ESD).”); 1:35-40. As transistor sizes shrink, gate dielectrics become thinner, making them more

susceptible to ESD damage. EX2003, ¶56. Additionally, industry standards also required ESD compliance for “a large number of pin and power supply combinations.” EX1001, 1:53-60.

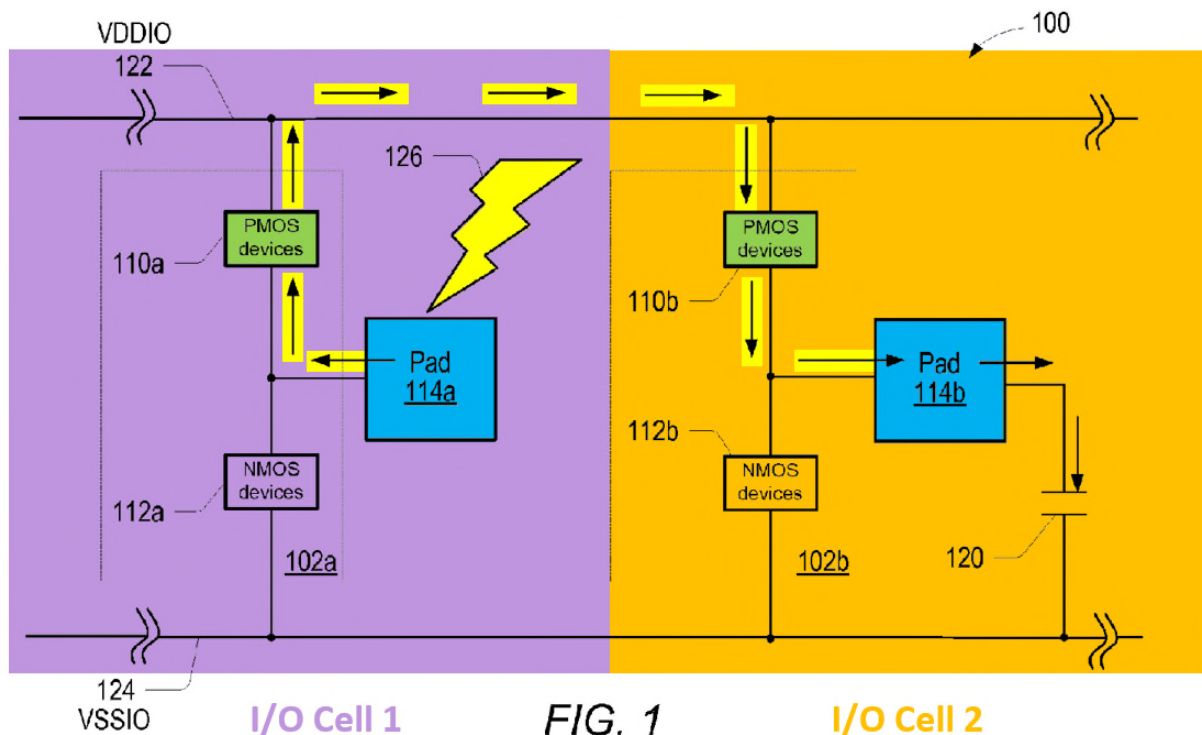
Against this backdrop, the ’665 patent presented novel and non-obvious advances in ESD circuitry to enhance ESD protection.

D. The ’665 Patent’s Solution

The ’665 patent’s solution for improved ESD performance is reflected in its title: “Pad ESD Spreading Technique.” EX1001, Title. As explained throughout the relatively short specification (consisting of two figures and six columns of text), this refers to spreading (*viz.*, sharing) charge from an ESD event on one pad to other pad(s) on the same chip. EX2003, ¶¶49-56. The ’665 patent explains that “[t]his method may be employed as an additional technique to be used in conjunction with other established solutions, such as various clamp devices and clamp circuits.” *Id.*, 2:35-39; *see also id.*, 2:66-3:3 (similar); 3:56-60 (similar). Doing so “reduc[es] the maximum voltage that may develop in the system as a result of the ESD event.” *Id.*, 2:29-34.

The ’665 patent teachings are most easily understood in connection with Figs. 1 and 2. Fig. 1 shows two I/O circuits (highlighted in purple and orange) that “have been configured to share a charge developed as a result of an electrostatic discharge (ESD) event, to reduce the maximum voltage developed in the system

[from] the ESD event.” EX1001, 3:11-15. Each I/O circuit has a “pad” (blue), labelled 114a and 114b, respectively. *Id.*, 3:65-67. And each pad has “an associated pad capacitance, shown in FIG. 1 only for pad 114b, where capacitor 120 symbolizes the pad capacitance associated with pad 114b.” *Id.*, 4:1-3. The lightning bolt (in yellow) indicates “an ESD event 126 affecting pad 114a.” *Id.*, 4:8-9. As reflected by the arrows (also highlighted in yellow), excess charge from an ESD event on pad 114a is shared with pad 114b by flowing through PMOS device 110a to the common/shared VDDIO supply rail and down through PMOS device 110b to pad 114b. *Id.*, 4:7-21.



Id., Fig. 1 (annotated).

Crucial to this charge-sharing operation is that “NMOS devices 112a and 112b [are] turned off” and that PMOS devices 110a and 110b are turned on “in response to the energy of the ESD event.” EX1001, 4:7-21. This “result[s] in charge flowing from pad 114a to pad capacitance 120 through PMOS devices 110a and 110b.” *Id.* The ’665 patent explains that “any and all pads similarly configured between VDDIO rail 122 and VSSIO rail 124 may have their respective PMOS devices turned on (including pad circuit 102a), resulting in the charge being shared ... across the respective pad capacitances associated with all the pads.”³ *Id.* Doing so “reduce[s] the maximum, or peak, voltage developed in the circuit, or system, as a result of ESD event 126.” *Id.*

This teaching—*viz.*, detecting ESD charge on another pad and sharing it to reduce peak voltage—is the primary purpose of the invention and is repeated throughout the specification. For example, the SUMMARY OF THE INVENTION explains that:

Output PMOS devices comprised in the output buffer of the pad and coupled between an I/O pad supply rail and the output pad may be

³ This modular approach—where each I/O cell contains all the circuitry necessary for ESD charge sharing—allows additional I/O cells to easily be added (or removed).

enabled in response to an ESD event, to *charge a pad capacitance ... to spread out the energy generated by the ESD event, resulting in a lower peak voltage* and therefore better ESD performance. By configuring all of the pads comprised within the system ... to operate this way, *the ESD energy may be shared* by the respective pad capacitances corresponding to all the pads, thereby *reducing the maximum voltage* that may develop in the system as a result of the ESD event.

See, e.g., EX1001, 2:21-35 (emphasis added). And the Abstract explains that:

A system, e.g. an integrated circuit or part, may include *a plurality of pads* In case of an ESD event affecting one or more of the digital I/O pads, *PMOS devices configured in an output buffer section ... may all be turned on in response to the ESD event*. This may allow the capacitance of each pad ... to charge up, absorbing the energy of the ESD event and *reducing the peak voltage* the integrated circuit or part experiences as a result of the ESD event.

Id., Abstract (emphasis added).

Fig. 2 (and its associated discussion) explain how this beneficial effect is achieved; in particular, how the output PMOS devices in the various pads are configured/controlled to turn on at the appropriate time in response to an ESD event. Fig. 2, reproduced below, is a circuit diagram “of a pad circuit configured to turn on PMOS devices in its output buffer to charge a corresponding pad capacitance to reduce the maximum voltage developed in the system as a result of

the ESD event.” EX1001, 3:16-20.

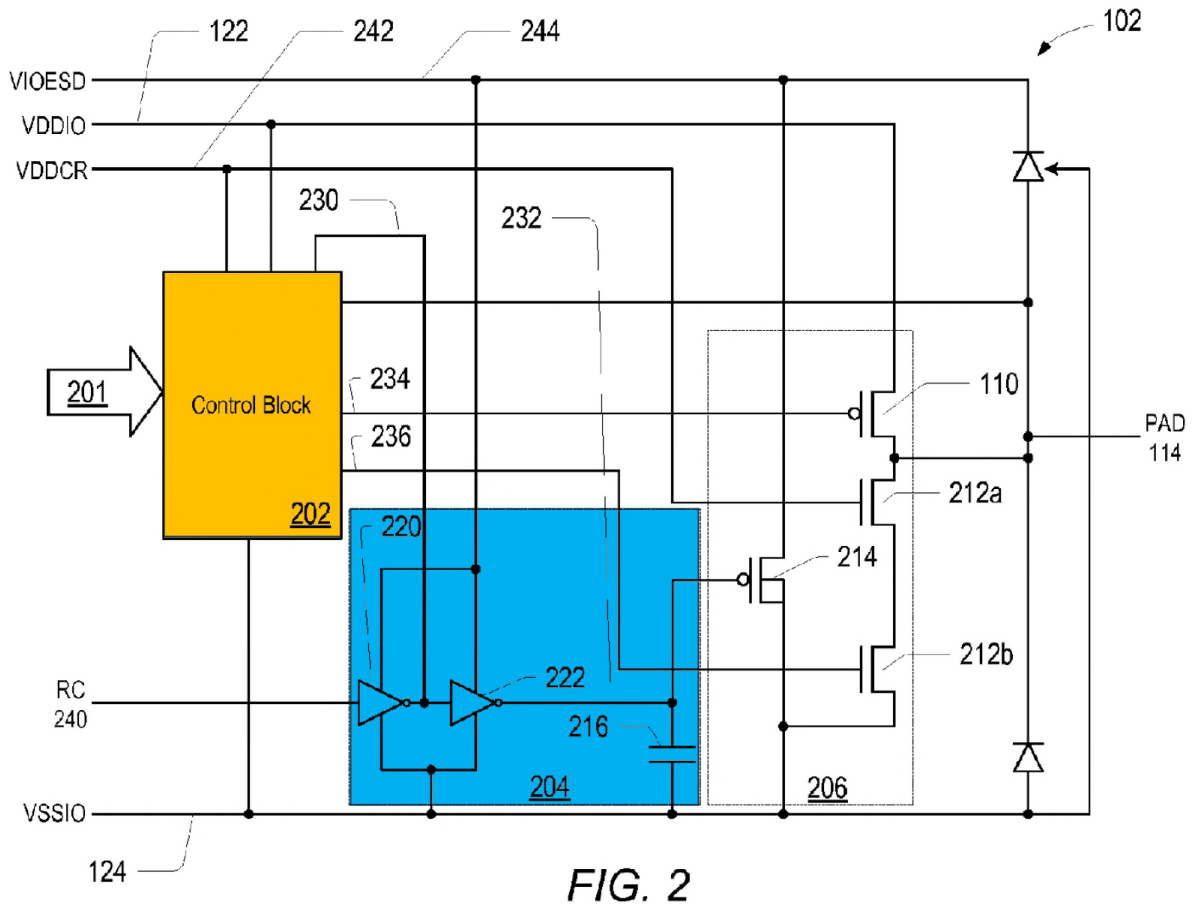


FIG. 2

Id., Fig. 2 (annotated); *see also* EX2003, ¶55.

Notably, each I/O cell includes its own control block 202 (orange) and control circuit 204 (blue) which, collectively, provide the logic for controlling PMOS device 110 during an ESD event. As the specification explains, “in response to being powered by the ESD event, clamp control circuit 204 may assert ESD control signal 230 to instruct control block 202 to enable PMOS device(s) 110, while disabling or keeping disabled NMOS device(s) 212b. By enabling (i.e. turning on) PMOS device(s) 110, control block 202 effectively connects VDDIO

rail 122 and its associated capacitance (which may comprise all the other pads or pad cells) to the physical pad affected by the ESD event, thereby sharing the charge generated by the ESD event, reducing the maximum voltage developed in the system [from] the ESD event.” EX1001, 5:24-36.

The ability of each I/O cell to detect an ESD event—on its own pad or any other pad—and “turn[] on” the PMOS device(s) connected to its respective physical pad in response thereto is essential to the operation of the invention and is repeated throughout the specification. For example, the SUMMARY OF THE INVENTION explains that during “*an ESD event, the clamp control circuit ... send[s] a signal to the functional control block, to instruct the functional control block to turn on the p-channel output device(s)—e.g. PMOS device(s)—* comprised in the output buffer. By turning on the p-channel devices, while disabling n-channel devices ... *the functional control block may operate to couple the high supply rail (i.e. the pad power rail) and its associated capacitance (such as all the other pad cells) to the pad affected by the ESD event*, thus charge sharing the ESD pulse.” EX1001, 2:49-65; *see also id.*, 3:44-50 (“output PMOS devices comprised in the output buffer of a pad ... may be enabled in response to an ESD event, to charge a pad capacitance ... corresponding to the physical pad or pad cell, to spread out the ESD energy.”); 4:22-27 (pad circuit is “*configured to turn on PMOS devices 110 in its output buffer 206 to charge a corresponding*

pad capacitance to reduce the maximum voltage developed in the system as a result of ESD event 126.”); 4:7-21 (“***any and all pads similarly configured between VDDIO rail 122 and VSSIO rail 124 may have their respective PMOS devices turned on (including pad circuit 102a), resulting in the charge being shared across all pads (pads 114a and 114b shown in FIG.1), that is, across the respective pad capacitances associated with all the pads.***”) (emphasis added).

Thus, it is central to the invention that each I/O cell has the ability to detect an ESD event and turn on the PMOS device(s) connected to the pad. Without this capability, excess ESD charge may not be shared with other pads.

III. THE ASSERTED PRIOR ART⁴

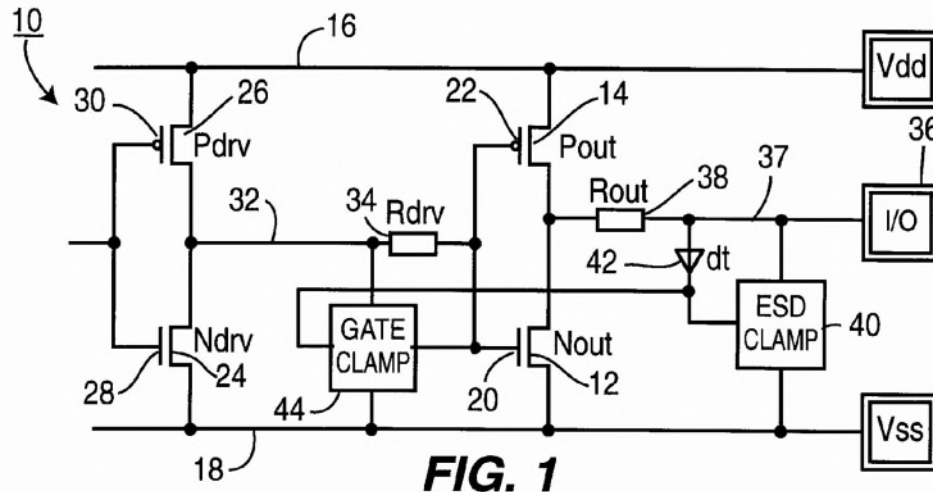
Patent Owner summarizes the two primary art references (Verhaege and Ker), both of which employ traditional ESD techniques designed to shunt current from a pad to the Vdd and/or Vss power rails. Neither reference discloses anything at all about sharing charge from an ESD event between I/O pads. *See generally* EX2003, ¶¶57-81.

⁴ Petitioner provides only the most rudimentary explanation of Ker and Verhaege. Pet., 11-12 (Verhaege), 59-60 (Ker). Patent Owner provides additional explanation here because a proper understanding of those references should result in denial of institution. *See also* EX2003, ¶¶57-75, 91-105.

A. Verhaege Summary

Verhaege is titled “Circuits for Dynamic Turn Off of NMOS Output Drivers During EOS/ESD Stress.” EX1004, Title. As the Abstract explains, Verhaege discloses “[a] circuit for the protection of an output driver NMOS transistor during EOS/ESD stress,” and “includes an output driver NMOS transistor and an output driver PMOS transistor connected in series between a Vss line and a Vdd line.” *Id.*, Abstract. As will be discussed below, Verhaege uses the conventional ESD approach that shunts current from an ESD event on an I/O pad to a power rail. EX2003, ¶¶58-62. It has nothing to do with sharing the ESD event’s charge with other I/O pads. *Id.*, ¶59. Instead, Verhaege relates to improving the conventional clamp by providing a “circuit for the protection of an output driver NMOS transistor during EOS/ESD stress.” EX1004, Abstract; *see also id.*, 4:39-47.

While Verhaege discloses several embodiments, all are variations on the same basic circuitry, so the relevant disclosures of Verhaege can be understood by examining the Fig. 1 embodiment.



EX1004, Fig. 1.

The functionality of this circuitry is explained in Verhaege's specification:

In the circuit 10, the CMOS output driver circuit (the output driver NMOS transistor 12 and the output driver PMOS transistor 14) is driven by the pre-driver transistors 24 and 26. The dynamic trigger device 42 is used to trigger the ESD clamp 40. The output resistor 38 is a decoupling resistor between the output drivers and the protection circuit (ESD clamp 40) and is optional in the circuit. The gate clamp 44 grounds the gate 20 of the output driver NMOS transistor 12 under transient over voltage stress conditions. In the circuit 10, the output driver NMOS transistor 12 is turned OFF during EOS/ESD stress, independent of the pre-driver state (high or low). As such, the ESD stress can be diverted to the parallel ESD clamp and the EOS/ESD capability is achieved.

Id., 2:26-40.

When a positive-voltage ESD event occurs on I/O pad (36), the “dynamic trigger circuit” (42) turns on, which activates the ESD clamp (40) and gate clamp (44). The gate clamp pulls the voltage on gates 20 and 22 (of Nout 12 and Pout 14,

respectively) low. This turns off the Nout transistor, which prevents any ESD current from flowing through it (thus protecting it from damage as Verhaege describes in the first sentence of its Abstract). At the same time, the activated ESD clamp 40 serves to shunt current from the ESD event on the I/O pad 36 to the Vss power supply rail (18)⁵ using the conventional approach discussed *supra* §II.B. EX2003, ¶¶60-61.

In summary, Verhaege discloses circuitry that, during a positive-voltage ESD event, will shunt ESD energy from the I/O pin to the Vss rail through the ESD clamp rather than through the Nout transistor. This is done as a means of protecting the Nout transistor from damage during an ESD event. Verhaege contains no disclosure or discussion of sharing ESD charge among multiple pads. EX2003, ¶¶61-62.

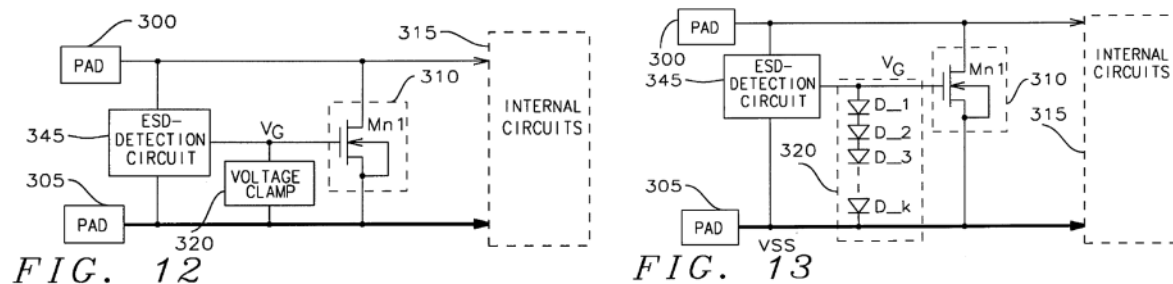
B. Ker Summary

Ker is titled “ESD Protection Circuit Without Overstress Gate-Driven Effect.” EX1005, Title. As will be discussed below, Ker uses the conventional ESD approach that shunts current from an ESD event on an I/O pad to a power rail. EX2003, ¶¶63-75. It has nothing to do with sharing ESD charge with other I/O

⁵ Verhaege contains no disclosure or discussion of using Pout to shunt ESD charge to the VDD rail. *See generally* EX1004; EX2003, ¶62.

pads. *Id.*, ¶64 et seq. Instead, Ker relates to improving the conventional shunting approach by protecting “the ESD protection MOS transistor” from “over-bias[ing its gate] with an extremely high voltage.” EX1005, 7:38-46.

Ker discloses various embodiments for an ESD protection circuit, many of which simply build on one another (*viz.*, by replacing block diagram components with actual circuitry). EX2003, ¶65. An example is seen in Figs. 12 and 13, where the generic “voltage clamp” black box in Fig. 12 is replaced with a series of diodes in Fig. 13. *Id.*

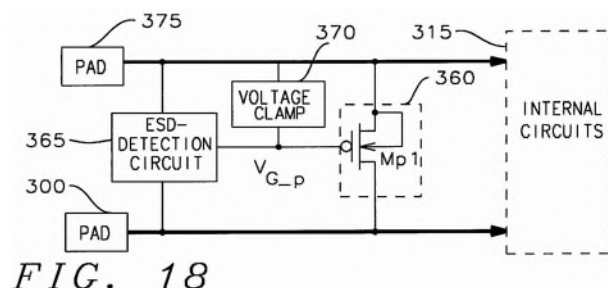
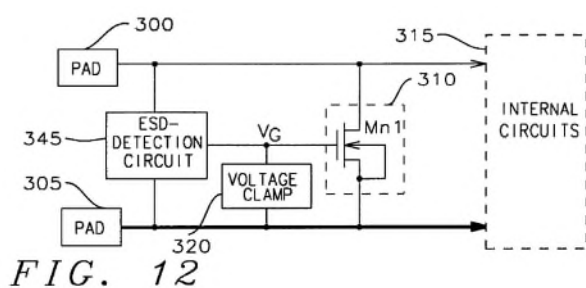


EX1005, Figs. 12-13.

Ker describes Figs. 1-10 as “Prior Art.” See EX1005, Figs. 1-10. Ker states Fig. 11 is “a first embodiment of an ESD protection circuit” and that Figs. 12-21 are “implementations” of that embodiment. *Id.*, 10:66-11:3. With respect to Fig. 12 (and applicable to similar figures), Ker explains pad 300 is an “input signal terminal to receive signals from external circuits” (*i.e.*, an I/O pad) and pad 305 is the associated “power supply terminal” (*viz.*, the Vss rail). *Id.*, 11:63-67.

If a positive-polarity ESD event strikes I/O pad 300, it is detected by ESD

detection circuit 345, which activates NMOS transistor 310 to shunt the ESD current to the VSS rail, just as described *supra* §II.B (“Conventional ESD Solutions”). EX1005, 12:1-6; EX2003, ¶¶67-69. Ker Fig. 18 provides an electrical mirror-image of Fig. 12, where the shunting transistor is a PMOS device (Mp1) instead of an NMOS device, and pad 375 represents the Vdd supply rail (instead of Vss rail 305). EX1005, 13:7-15; EX2003, ¶70.

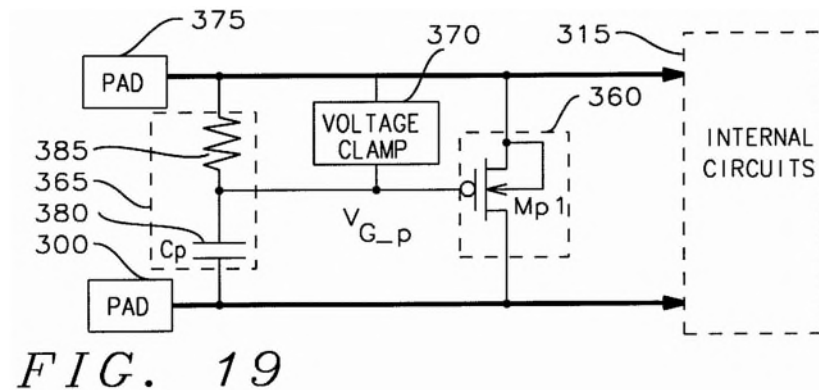


EX1005, Figs. 12 and 18.

Overall, operation of Fig. 18 is the inverse of Fig. 12. EX2003, ¶¶67-68. If a negative-polarity ESD event occurs on I/O pad 300, the ESD detection circuit 365 activates the “ESD protection PMOS transistor Mp1 360,” and the ESD event’s energy is shunted through Mp1 to the VDD rail. EX1005, 13:15; EX2003, ¶72. A negative-polarity ESD event is required in this implementation because transistor 360 is a PMOS device. *Id.*, ¶¶40-41. Again, this is conventional ESD shunting from an I/O pad to a power supply rail. *See supra* §II.B.

Ker Fig. 19 “illustrates an implementation of the ESD detection circuit 365.” EX1005, 13:29-30. As can be seen, the detection circuit comprises a resistor (385)

and a capacitor (380). *Id.*, 13:30-36.



Ker then pairs the two electrical-mirror-image embodiments together, with minor changes not relevant here, to form the combined embodiment of Fig. 29. See EX1005, 19:37-42 (“An implementation of the first ESD detection circuit 545 and the second ESD detection circuit 565 are shown in FIG. 29. The first capacitor C_n 550 and the optional first resistor R_n 555 form the first ESD detection circuit 545. The second capacitor C_p 580 and the optional second resistor R_p 585 form the second ESD detection circuit 565.”); see generally *id.*, 17:64-19:57.

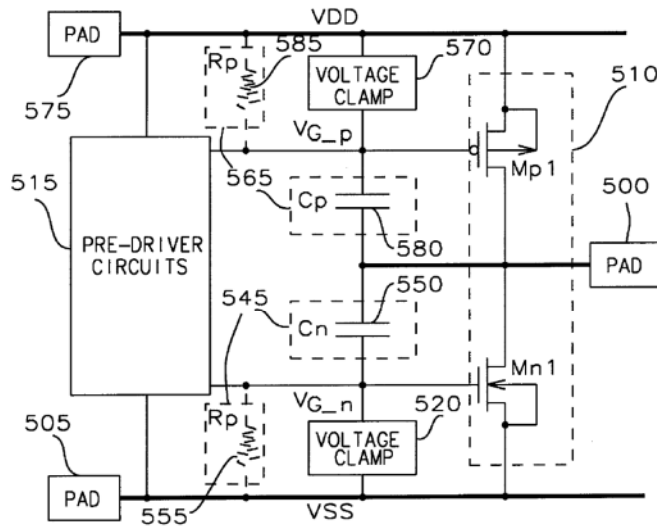


FIG. 29

Ker explains how this circuit operates in response to both positive- and negative-polarity ESD events on I/O pad 500. EX1005, 19:37-58. In particular, a positive-polarity ESD strike on pad 500 induces a transient voltage across the detection-circuit capacitor 550, which pulls the gate voltage on transistor Mn1 (*i.e.*, node V_{G_n}) high. *Id.*, 19:44-50; EX2003, ¶71. This turns on transistor Mn1 (because it is an NMOS device) to shunt ESD current to the Vss power supply rail. *Id.*, ¶¶40-41. The same positive-polarity ESD event will also turn off transistor Mp1 (because it is a PMOS device). *Id.*, *see also id.*, ¶71.

In contrast, a negative-polarity ESD strike on pad 500 induces a transient voltage across the detection-circuit capacitor 580 which pulls the voltage on the gate of transistor Mp1 (*i.e.*, node V_{G_p}) low. EX1005, 19:51-57; EX2003, ¶72. This turns on transistor Mp1 (which is a PMOS device) and provides ESD

protection by shunting excess current. *Id.*, ¶¶40-41. The same negative-polarity ESD event will also turn off transistor Mn1 (because it is an NMOS device). *Id.*, ¶72.

Like Verhaege, Ker teaches circuitry that shunts ESD charge on the I/O pad to a power supply rail, as described in the Technology Background (§II.B). Further, like Verhaege, Ker contains no disclosure or discussion of sharing ESD charge among multiple pads. EX2003, ¶¶63-75.

IV. CLAIM CONSTRUCTION

In IPR, claim terms are construed under *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc) and its progeny. 37 C.F.R. §42.100(b). The Board, however, only construes claim terms when necessary to resolve the controversy. *See, e.g., Toyota Motor Corp. v. Cellport Sys., Inc.*, IPR2015-00633, Paper 11 at 16 (PTAB Aug. 14, 2015).

After Petitioner filed the Petition, the district court issued a *Markman* ruling in which it construed two claim terms (“*second voltage rail*” and “*to charge the [respective] pad capacitance*”)⁶ in the ’665 patent. *See* EX1012 (*Markman* Order) and EX1013 (*Markman* Memorandum). Patent Owner includes those constructions here for completeness, but they have no bearing on Patent Owner’s

⁶ Claim language is indicated by *red italics*.

arguments in this Preliminary Response and need not be construed.

Petitioner asserts that “no constructions are necessary to resolve any disputes identified in [its] Petition” and did not propose any terms for construction. Pet., 10. Patent Owner submits that it is not necessary for the Board to construe any claims to deny institution based on the arguments in §§V.A.1 (Ground 1), V.B.1 (Ground 2), and V.C1 (Ground 3). However, resolving the claim construction dispute in §IV.B in Patent Owner’s favor provides an additional basis—dispositive as to all Grounds—to deny institution. See §§V.A.2, V.B.2, and V.C.2.

A. The Parties *AGREE* that an ESD Event on One I/O Pad Must Be Shared with a Different I/O Pad.

Before discussing the parties’ claim construction dispute (in §IV.B below), it is helpful to discuss one point—*i.e.*, charge-sharing between pads—on which the parties are in agreement. All three independent claims have a requirement “*to charge the [respective] pad capacitance to reduce a maximum voltage developed in the system as a result of the ESD event*” to “*reduce the maximum voltage developed in the system as the result of the ESD event.*” EX1001, cl. 1, 6, and 14. That “*the ESD event*” must occur on a different I/O pad follows from the pure logic of the claim language and teachings of the specification.

Regarding the claim language, the only way that “*charg[ing] the [respective] pad capacitance*” of an I/O pad can “*reduce a maximum voltage developed in the system as a result of the ESD event*” is if the ESD event occurs on

a *different I/O pad*. Otherwise, the claims would make no sense because they would require “*reduc[ing] a maximum voltage developed in the system as a result of the ESD event*” by charging the same I/O pad where the ESD event occurs. This is a logical impossibility and is not how a POSITA would understand the claim language. EX2003, ¶¶85-88.

Nor does the specification teach such an implausible interpretation. *See generally* EX1001. Rather, as the Abstract explains, “an integrated circuit or part, may include a plurality of pads, e.g. digital I/O pads, each comprising a physical pad and associated pad circuit.” *Id.*, Abstract. The Abstract further explains that “[i]n case of an ESD event affecting one or more of the digital I/O pads, PMOS devices configured in an output buffer section ... [of the respective pad circuits] ... may ***all be turned on in response to the ESD event.***” *Id.* (emphasis added). Doing so “charge[s] up” each pad and “reduce[s] the peak voltage” in the overall system. *Id.* Indeed, consistent with this concept, the ’665 patent’s title is “Pad ESD Spreading Technique.” *Id.*, Title.

This teaching is repeated throughout the specification. For example, Fig. 1 illustrates two I/O circuits “configured to share a charge developed as a result of an electrostatic discharge (ESD) event, to reduce the maximum voltage developed in the system [from] the ESD event.” EX1001, 3:11-15. The lightning bolt 126 indicates “an ESD event 126 affecting pad 114a.” *Id.*, 4:8-9. As reflected by the

arrows (highlighted in yellow), excess charge from an ESD event on pad 114a is shared with pad 114b by flowing through PMOS devices 110a to the common/shared VDDIO supply rail and down through PMOS devices 110b to pad 114b. *Id.*, 4:7-21.

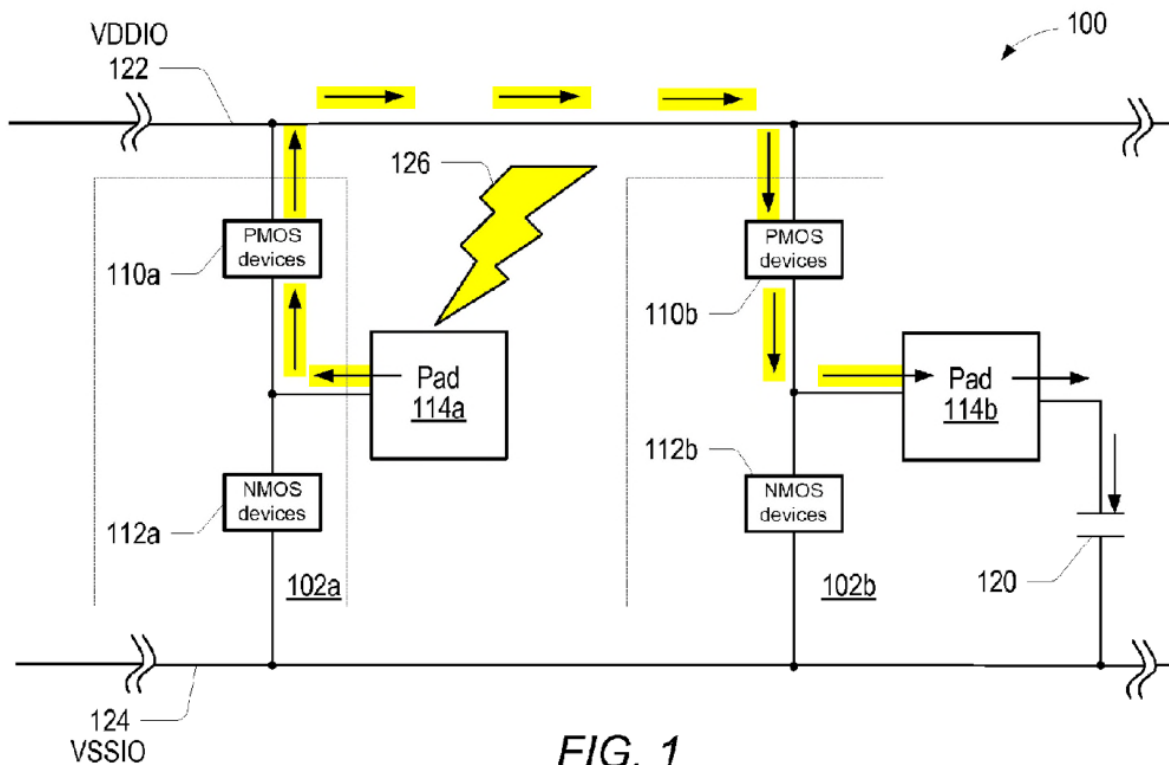


FIG. 1

Id., Fig. 1 (yellow highlights added); see EX2003, ¶¶85-88.

Petitioner agreed in district court—without construing the claims—with this analysis of the “charge-sharing” limitations. For example, when arguing invalidity in district court under §112, Petitioner stated “the [’665] specification does not describe a single pad with circuitry capable of activating a portion of the output buffers to charge the single pad’s capacitance. In each instance where the

specification discusses the reduction of voltage developed in a system as a result of an ESD event, it describes sharing the ESD voltage with adjacent pads and using the neighboring pad capacitance to absorb some ESD charge. *See e.g.*: [’665 patent at 2:19-35, 2:56-65; Fig. 1, 3:65-4:21, and 5:29-35].” EX2001, 25 (emphasis omitted).

Indeed, Patent Owner further asserted in district court that “[the ’665] specification does not describe any means by which a single pad may use its output buffer to charge its own pad capacitance to reduce the maximum voltage developed in the system as a result of an ESD event. Nor would a POSA reading the specification immediately envision such a system. The pad [struck by the ESD event] would already be fully saturated by the incoming ESD charge and activation of the control circuitry would not be able to charge the pad capacitance further.” EX2001, 27.

Accordingly, it should be beyond dispute that the claims require sharing ESD charge from one pad *with a different I/O pad*. As discussed *infra*, this alone is fatal to Ground 1 (*see* §V.A.1) and Ground 3 (§V.C.1).

B. The Parties *DISAGREE* on the Location of the “*Enable Circuitry*” (Claim 1) and “*Control Circuit[ry]*” (Claims 6 and 14)

The claims all require charge-sharing by “*turn[ing] on*” (claim 1) or “*activat[ing]*” (claims 6 and 14) “*one or more output transistor devices*” (claim 1) or a “*portion of the [respective] output buffer*” (claims 6 and 14). This is

accomplished by: “*control circuitry*” (claim 14); a “*control circuit*” and “*control block*” (claim 6); and “*enable circuitry*” and “*control block*” (claim 1). The disputed issue is whether the claimed “*enable circuitry*” (claim 1) and “*control circuit[ry]*” (claims 6 and 14) that turns on the “*output [buffer / transistor]*” (viz., PMOS output transistor) is located in the I/O cell where the ESD event occurs (Petitioner’s position) or the I/O cell with which the ESD charge is shared (Patent Owner’s position). In other words, the parties’ dispute which output PMOS device (110a or 110b in Fig. 1a) and accompanying enable/control circuitry are claimed (*i.e.*, in the lefthand I/O cell of ’665 patent Fig. 1 where lightning strikes or the righthand I/O cell).

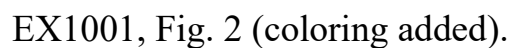
The answer lies with the claim language and specification, which indicate the claimed “*enable circuitry*” and “*control circuit[ry]*” reside in the I/O cell that receives the shared charge. *See* EX2003, ¶¶89-97. Otherwise, the claims cover nothing more than a traditional ESD circuit that shunts current to a supply rail through its own output transistor, a technique which the ’665 patent says was insufficient (EX1001, 2:3-6) and which the ’665 patent sought to improve upon (*id.*, 2:35-39 (“[the inventive] method may be employed as an additional technique to be used in conjunction with other established solutions, such as various clamp devices and clamp circuits.”)).

Taking claim 1, for example, the claim is directed to a “*pad circuit.*” The

parties agree that “*the maximum voltage developed in the system as the result of the ESD event*” refers to an ESD event on a different pad. Thus, when the claim recites “*enable circuitry*” of the “*pad circuit*” acting “*in response to the ESD event*,” the claim is plainly referring to that same pad’s enable circuitry acting in response to an ESD event on a different pad. Independent claims 6 and 14 include similar language. See EX1001, cl. 6 (“*A circuit configured to provide protection against electrostatic discharge (ESD) ... the circuit comprising: ... a control circuit configured to instruct the control block to activate at least a portion of the output buffer when an ESD event occurs*”), cl. 14 (“*a respective pad circuit comprising: ... respective control circuitry operable to[] activate at least a portion of the respective output buffer in response to an ESD event*”).

This teaching—viz., activating the output transistor upon detecting an ESD event in a different cell to enable charge-sharing between pads—is the primary purpose of the invention and is repeated throughout the specification. For example, the SUMMARY OF THE INVENTION explains that “[o]utput PMOS devices ... may be enabled in response to an ESD event, to charge a pad capacitance ... corresponding to the physical pad or pad cell, to spread out the energy generated by the ESD event, resulting in a lower peak voltage and therefore better ESD performance.” EX1001, 2:21-39. The construction of the claims should reflect this articulated purpose. See, e.g., *In re Abbott Diabetes Care, Inc.*,

The '665 specification goes on to explain in more detail how this is accomplished. In particular, the discussion of Fig. 2 explains how the output PMOS device(s) in each pad are configured/controlled to turn on at the appropriate time in response to an ESD event. For example, as shown in Fig. 2, each I/O cell includes its own control block 202 (orange) and control circuit 204 (light blue) which, collectively, provide the logic for controlling PMOS device 110.



As the specification explains, “in response to being powered by the ESD event, clamp control circuit 204 may assert ESD control signal 230 to instruct control block 202 to enable PMOS device(s) 110 By enabling (i.e. turning on) PMOS device(s) 110, control block 202 effectively connects VDDIO rail 122 and its associated capacitance (which may comprise all the other pads or pad cells) to the physical pad affected by the ESD event, thereby sharing the charge generated by the ESD event, reducing the maximum voltage developed in the system.” EX1001, 5:24-36; *see also id.*, 2:49-65 (“the functional control block may operate to couple the high supply rail (i.e. the pad power rail) and its associated capacitance (such as all the other pad cells) to the pad affected by the ESD event, thus charge-sharing the ESD pulse.”); 3:44-50 (“output PMOS devices comprised in the output buffer of a pad ... may be enabled in response to an ESD event, to charge a pad capacitance ... corresponding to the physical pad or pad cell, to spread out the ESD energy.”); 4:22-27 (pad circuit is “configured to turn on PMOS devices 110 *in its output buffer* 206 to charge a corresponding pad capacitance to reduce the maximum voltage developed in the system as a result of ESD event 126.”) (emphasis added); 4:7-21 (“any and all pads similarly configured between VDDIO rail 122 and VSSIO rail 124 may have their respective PMOS devices turned on (including pad circuit 102a), resulting in the charge being shared across all pads.”).

Thus, it is central to the '665 invention that each I/O cell can detect an ESD event on a different cell and turn on its own output transistor (*e.g.*, PMOS device) to enable charge-sharing between pads. It would be error to read the claims any other way (*i.e.*, as Petitioner does) to cover an I/O cell that does nothing more than shunt current to a power rail.⁷ EX2003, ¶¶85-97 (confirming how a POSITA would understand the claim language).

Patent Owner's construction reflects the patent's solution for improved ESD protection circuitry. Like the Federal Circuit in *In re Abbott*, which looked to the purpose of the patent to construe the disputed term, the Court's construction should reflect that the fundamental purpose of the '665 invention is to provide a cell that detects an ESD event on another I/O pad and turns on its own output transistor to share charge among pads. Patent Owner provides no answer for why it implicitly construes the claims in a manner unrelated to the purpose of the invention, and in an illogical manner contrary to the claim language itself.

Patent Owner's claim construction properly relies on the specification to inform the plain and ordinary meaning to a person of ordinary skill in the art ("POSITA") in the context of the '665 patent. Scores of appellate decisions rely

⁷ The Petition admits that it is necessary that the "PMOS devices 110b are activated," to "allow[] the charge to flow from the rail to I/O pad 114b." Pet., 5.

on similar types of information and clues in the specification to construe claim terms. *See, e.g., ICU Med., Inc. v. Alaris Med. Sys., Inc.*, 558 F.3d 1368, 1375 (Fed. Cir. 2009) (construing “spike” to require a pointed tip capable of piercing, based on repeated and uniform statements in the specification); *Alloc, Inc. v. ITC*, 342 F.3d 1361, 1369-70 (Fed. Cir. 2003) (construing claim to include limitation that the “very character of the invention” required); *Wang Labs., Inc. v. America Online, Inc.*, 197 F.3d 1377, 1382 (Fed. Cir. 1999) (construing “frame” as character based system, not bitmapped system, when specification consistently described it as such and mentioned bitmaps only in describing the prior art).⁸

C. “Second Voltage Rail” (claim 1)

For completeness, Patent Owner notes the district court construed “second voltage rail” in claim 1 of the ’665 patent as “a second voltage rail that is distinct from the third voltage rail but may or may not be distinct from the first voltage rail.” EX1012, 1. This construction has no bearing on Patent Owner’s arguments

⁸ To the extent Petitioner belatedly argues express disavowal is required, that is incorrect for the additional reason that “when the scope of the invention is clearly stated in the specification, and is described as the advantage and distinction of the invention, it is not necessary to disavow explicitly a different scope.” *On Demand Mach. Corp. v. Ingram Indus., Inc. Inc.*, 442 F.3d 1331, 1340 (Fed. Cir., 2006).

in this Preliminary Response. EX2003, ¶83.

D. “To Charge The [Respective] Pad Capacitance” (all claims)

Per the parties’ stipulation, the district court construed the phrase “to charge the [respective] pad capacitance” in claims 1, 6, and 14 as “to charge the pad capacitance of said physical pad having [respective] capacitance.” EX1012, 2.

Patent Owner submits that this construction makes no difference to Patent Owner’s arguments in this Preliminary Response. EX2003, ¶83.

V. THE PETITION FAILS TO ESTABLISH A REASONABLE LIKELIHOOD OF SUCCESS

Petitioner challenges all 18 claims of the ’665 patent on three Grounds, as shown below:

Ground	35 U.S.C. §	Claims	Prior Art References
1	103(a)	1-18	Verhaege
2	103(a)	1-18	Verhaege, Miller
3	103(a)	1-18	Ker

Pet., 11.

As explained below, Petitioner fails to show that Grounds 1 and 3 satisfy the requirement of ESD charge-sharing between pads (as required by all claims). *See* §§V.A.1, V.C.1. Ground 2 fails because Petitioner does not establish a reasonable likelihood of success for its proposed modification of adding Miller’s shared

trigger signal to Verhaege. *See* §V.B.1.

An independent reason all three Grounds fail is because none satisfies the claim requirement for control circuitry that activates the output transistor for ESD charge-sharing between pads *in response to the ESD event at another I/O pad*.

See §§IV.B, V.A.2 (Ground 1), V.B.2 (Ground 2), and V.C.2 (Ground 3); *see also* EX2003, ¶¶37, 99-105 (providing a summary of opinions).

A. Ground 1 (Obviousness over Verhaege)

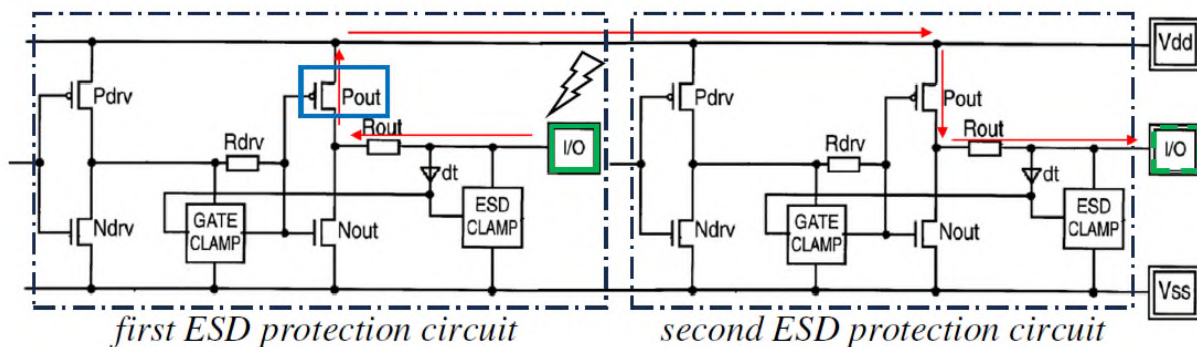
Ground 1 fails for two reasons: (1) Verhaege does not disclose or render obvious ESD charge-sharing between pads; and (2) Verhaege does not disclose or render obvious the “*enable circuitry*” (claim 1) or “*control circuit[ry]*” (claim 6 and 14) which must be located in a different I/O cell than where the ESD event occurs. EX2003, ¶106; *see generally id.*, ¶¶107-118.

For Ground 1, Petitioner asserts all Challenged Claims are obvious over Verhaege (*i.e.*, single-reference obviousness). Pet., 10-11, §V.A. Notably, Petitioner does not contend Verhaege anticipates any Challenged Claim. Pet., 10-11. For example, Petitioner’s failure to assert that Verhaege actually discloses claim element 1[d] is a tacit admission it does not. *See id.*, 18 (“Verhaege renders obvious ‘charg[ing] the pad capacitance to reduce a maximum voltage developed in the system as a result of the ESD event.’ Although Verhaege discloses a single pad circuit, ... [i]t would have been obvious to a POSITA that ... the Verhaege

invention should be repeated at every I/O pad.”); *see generally id.*, 16-18.

Petitioner’s assertions for the corresponding limitation in independent claims 6 and 14 are substantially similar. *See id.*, 30-32 (claim 6), 43-44 (claim 14, cross-referencing claim element 6[d] to explain that “a POSITA would include the Verhaege circuit at every I/O pad ...”).

Petitioner’s Obviousness Theory. Because, as discussed *supra* §IV.A, the Challenged Claims all require ESD charge-sharing among different I/O pads, Petitioner modifies Verhaege (for certain claim elements) as shown below to add a second I/O cell sharing Vdd and Vss rails with a first I/O cell. Pet., 18. Notably, the structure, function, and operation of the two I/O cells are identical to one another (*i.e.*, Petitioner identified no modification other than duplicating the cells and connecting their power rails). *Id.*

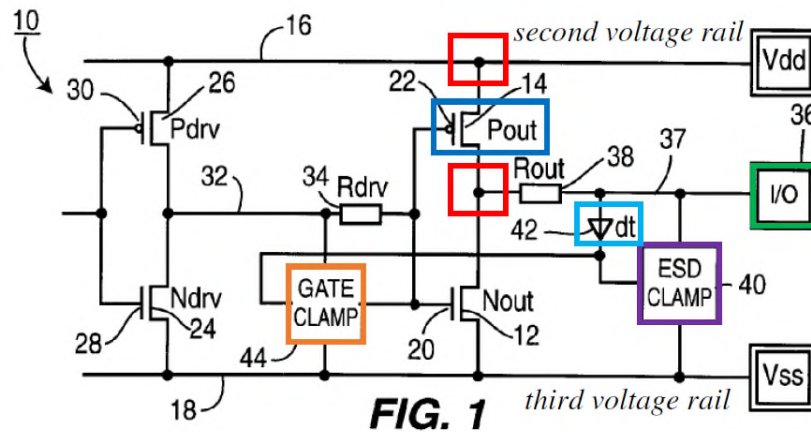


Id., 18 (all modifications and annotations by Petitioner); *see also id.* (“The annotated figure [] shows the ESD protection circuit of Verhaege’s Figure 1 repeated for two I/O pads.”).

But even Petitioner’s modified circuit does not meet the requirements—present in every independent claim—of (1) ESD charge-sharing between pads; or (2) that the claimed control/enable circuitry act “*in response to [an/the] ESD event*” *on a different I/O cell*. See *supra* §IV.A; EX2003, ¶¶107-115. To understand why, it is helpful to first review the color mapping scheme Petitioner employs. While Petitioner first presents the table below in connection with explaining the ’665 patent, Petitioner uses the same colors when mapping Verhaege’s circuit.

Component	Color	
First and second nodes	Red	
Control block	Orange	
Enable circuitry	Light Blue	
Clamp device	Purple	
Output transistor	Dark Blue	
I/O pad	Green	

Pet., 6. Relevant here, Petitioner shows the “[c]ontrol block” in orange, the “[e]nable circuitry” in light blue, the “[o]utput transistor” in dark blue, and the “I/O pad” in green. Petitioner applies this mapping to Verhaege as shown below.

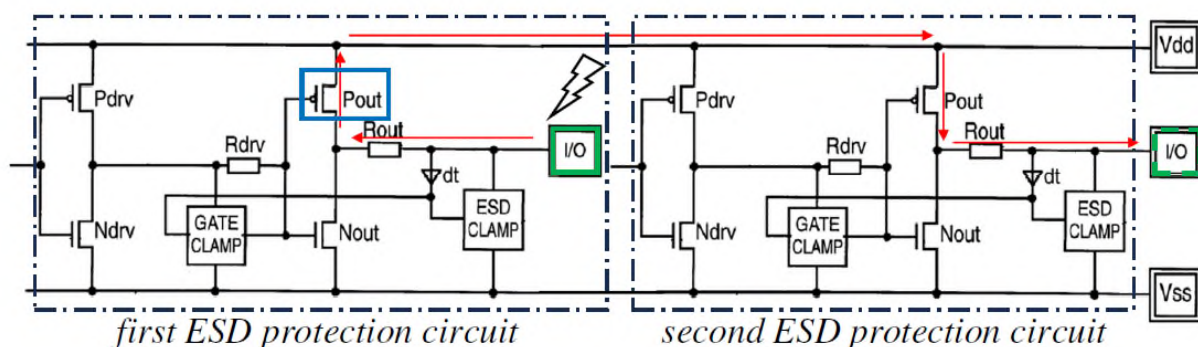


Id., 22 (all annotations added by Petitioner). For purposes of this Preliminary Response, Patent Owner uses Petitioner’s own mapping to demonstrate Petitioner has failed to establish a reasonable likelihood of unpatentability for any Challenged Claim.

In relevant part, Petitioner explains Verhaege’s circuit operation as follows. “Verhaege’s Figure 1 shows enable circuitry comprising dynamic trigger device 42 (light blue). The input of dynamic trigger device 42 is connected to I/O pad 36 (green) where the ESD event originates.” Pet., 22. “Dynamic trigger device 42 is also connected to the control block, i.e., gate clamp 44 (orange)” and “gate clamp 44 then ‘turn[s] on the at least one of the one or more output transistor devices,’ i.e., PMOS transistor 14 (dark blue), by grounding the gates of the output transistors.” *Id.* This explanation is fatal to Petitioner’s obviousness argument.

Returning now to Petitioner’s modified figure, Petitioner added a “lightning bolt” to the I/O pad in the left cell. Thus, that is the I/O pad where the ESD event

occurs.



Pet., 18 (all modifications and annotations by Petitioner).

Petitioner's theory is as follows: "The ESD energy flows from the first I/O pad [on the left in a green box] to the Vdd rail,⁹ increasing its voltage and charging the capacitance of the second I/O pad [on the right in a dashed green box]." Pet., 18. Petitioner added the red arrows to show this purported flow of current. *Id.*

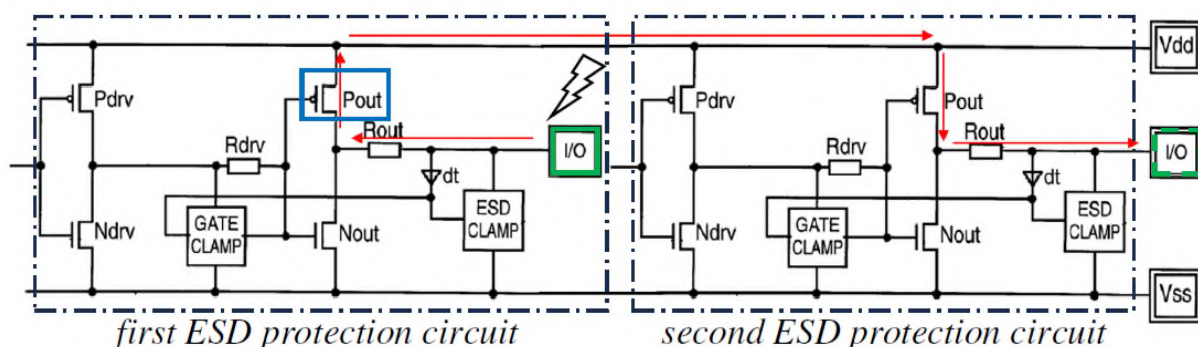
Petitioner explains "the PMOS transistor (dark blue) of the first circuit connects the first I/O pad (solid green) to the Vdd rail." Pet., 18. For purposes of this Preliminary Response only, Patent Owner does not dispute this statement. But Petitioner's further assertion that "the first I/O pad is [thus] electrically connected to all other pads" and "[c]harg[es] the capacitance of the second pad" (*id.*) is not

⁹ Patent Owner does not agree that Verhaege discloses shunting ESD current through Pout, but the Board need not decide that issue to deny institution.

only entirely unsupported, but incorrect. This is fatal to Petitioner’s obviousness assertion for two independent reasons.

1. Petitioner Fails to Show Verhaege Discloses or Renders Obvious ESD Charge-Sharing Between Pads

To begin, in Petitioner’s modified circuit below, it cannot legitimately be disputed that for charge-sharing between pads, the Pout transistors in both the left and right I/O cells must be turned on. If either one is off, no charge will flow along the path outlined by Petitioner. But Petitioner offers no explanation for how both Pout transistors are turned on at the same time, let alone in response to an ESD event. EX2003, ¶¶107-115.



Pet., 18 (all modifications and annotations by Petitioner). Petitioner added the red arrows, and baldly asserts “[t]he ESD energy flows from the first I/O pad to the Vdd rail, increasing its voltage and charging the capacitance of the second I/O pad.” *Id.*, 18.

At most, Petitioner explains how a positive *ESD event on the left pad* (which it illustrates with a lightning bolt) would turn on the Pout transistor *in the*

left I/O cell and (purportedly) cause the voltage on the shared Vdd rail to rise.

Pet., 18; EX2003, ¶107. Putting aside whether this is correct or not, nowhere in the Petition (or the accompanying expert declaration)¹⁰ does Petitioner explain why or how increased voltage on the shared Vdd rail would cause anything to happen in the I/O cell on the right, let alone cause Pout to turn on in the righthand I/O cell and share ESD charge. *Id.*, ¶¶108-112.

Apart from failing to proffer any explanation—which in itself warrants denying institution—Petitioner’s two-cell modification does not operate in the manner required by the claims. In particular, unless the righthand Pout transistor was already turned on (and Petitioner offers no reason to believe it would be), it would act as an open circuit and **prevent** ESD charge-sharing between pads.

EX2003, ¶112. For the same reason, a voltage surge on the Vdd rail would not activate the dynamic trigger (dt) in the righthand I/O cell to turn on Pout. *Id.*, ¶¶112-113. Indeed, Petitioner’s own explanation of how Verhaege operates confirms this: “A POSITA would understand ... dynamic trigger device 42 must ‘instruct’ gate clamp 44 ... [to] ‘turn[s] on the at least one of the one or more output transistor devices,’ i.e., PMOS transistor 14 (dark blue), by grounding the

¹⁰ Petitioner cites ¶67 of its expert declaration, but that essentially regurgitates the Petition with no additional explanation. *Compare* Pet., 18 and EX1002, ¶67.

gates of the output transistors.” Pet., 22; *see also* EX1002, ¶73 (same). In other words—even under Petitioner’s own analysis—the gate clamp in the righthand I/O cell turns on Pout *when its dynamic trigger (dt) detects a voltage spike on its input node* (i.e., the node connected to the righthand I/O pad), not when the Vdd rail spikes. EX2003, ¶113.

And unless Pout in the righthand cell is turned on, no current will flow from the shared Vdd rail to the righthand I/O pad, and no ESD charge-sharing occurs. EX2003, ¶¶114-115.

2. Petitioner Fails to Show Verhaege Discloses or Renders Obvious the Claimed “*Enable Circuitry*” (Claim 1) and “*Control Circuit[ry]*” (Claim 6 and 14)

As discussed *supra* §IV.B, the claimed “*enable circuitry*” (Claim 1) and “*control circuit[ry]*” (Claim 6 and 14) must turn on the “*output [buffer/transistor]*” in response to an ESD event *on a different I/O cell*. Under Petitioner’s mapping, Verhaege’s dynamic trigger (dt) in the righthand I/O cell must turn on Pout (also in the righthand I/O cell) in response to the ESD event (lightning bolt) on the left I/O pad. *See* §IV.B; EX2003, ¶¶116-117.

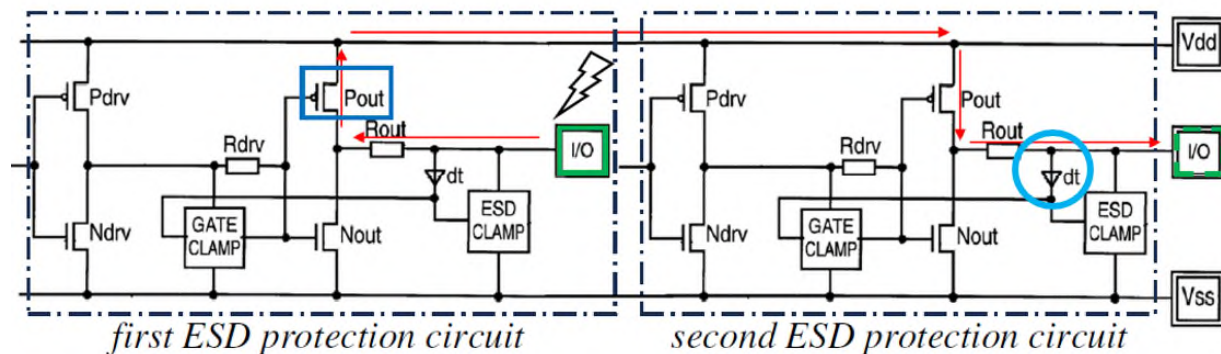
Petitioner fails to explain how Verhaege’s “dynamic trigger” (dt) in the righthand I/O cell does this. EX2003, ¶¶116-118. More specifically, Petitioner’s mapping of Verhaege’s dynamic trigger fails to satisfy the claimed requirements of:

- “*enable circuitry configured to ... instruct the control block to turn on the at least one of the one or more output transistor devices, in response to the ESD event*” (claim element 1[f]);
- “*a control circuit configured to instruct the control block to activate at least a portion of the output buffer when an ESD event occurs*” (claim element 6[d]); or
- “*control circuitry operable to[] activate at least a portion of the respective output buffer in response to an ESD event to charge the respective pad capacitance*” (claim element 14[d]).

Petitioner offers no explanation whatsoever for how the “dynamic trigger” in the righthand I/O cell of Petitioner’s “two-cell” configuration of Verhaege turns on the righthand Pout transistor when an ESD event occurs on the left I/O pad. While that alone is fatal to Petitioner’s obviousness challenge, actual analysis of Petitioner’s modified circuit demonstrates Verhaege’s “dynamic trigger” does not—and cannot—turn on the righthand Pout transistor to allow its I/O pad to be charged by ESD current from the left I/O pad.

As a reminder, Petitioner maps Verhaege’s dynamic trigger 42 (abbreviated as “dt”) to the “*enable circuitry*” (claim 1), “*control circuit*” (claim 6), and “*control circuitry*” (claim 14). See Pet., 22 (claim 1, “Verhaege’s Figure 1 shows enable circuitry comprising dynamic trigger device 42 (light blue).”); 31-32 (claim 6, identifying dt as “the control circuit (light blue)”; 43 (claim 14, “Verhaege teaches control circuitry comprising dynamic trigger device 42 (light blue)”).

Under Patent Owner’s construction, that dynamic trigger must be on the right, as shown by the blue circle below. EX2003, ¶116-117.



Id., 18 (all modifications and annotations by Petitioner, except light blue circle added by Patent Owner).

But Petitioner provides no explanation whatsoever for how the claimed “*enable circuitry*” (which Petitioner maps to the dynamic trigger “dt”) in the I/O cell on the right “*instruct[s] the control block*” (which Petitioner maps to the gate clamp) “*to turn on the at least one of the one or more output transistor devices*” (which Petitioner maps to Pout) “*in response to the ESD event*” occurring in the left I/O cell. EX1001, cl. 1[d] and 1[f]; see Pet., 21-22 (lacking any explanation of how the dynamic trigger dt in the I/O cell on the right “instruct[s] control block to turn on” the Pout transistor); EX2003, ¶117. Indeed, Petitioner’s analysis for claim elements 1[f], 6[d], and 14[d] does not show or discuss a two-cell configuration of Verhaege at all. See Pet., 21-22, 30-31, 43.

Moreover, because the claims require the output transistor (which Petitioner

maps to Pout) to “*turn on*” (claim 1) or “*activate*” (claims 6 and 14), the logical implication is that Pout is off to begin with. Otherwise, it could not “*activate*” / “*turn on*” because it would already be on/activated. EX2003, ¶118. In other words, in the righthand cell, the dynamic trigger could only detect a voltage spike on the Vdd rail (*e.g.*, from an ESD event on the left I/O pad) if Pout was *already turned on*. *Id.* This approach—which requires that Pout already be on so the voltage spike on the Vdd rail can reach the input node of the dynamic trigger—creates a logical fallacy: turning on a transistor (Pout) that is already on. *Id.* This makes no sense and is not what is claimed.

In summary, Petitioner’s modified version of Verhaege does not satisfy the requirement that the claimed I/O cell’s control/enable circuitry act “*in response to [an/the] ESD event*” on a different I/O cell to “*turn on*” or “*activate*” the “*output [transistor/buffer]*” to “*charge the [] pad capacitance to reduce a maximum voltage developed in the system as a result of the ESD event.*” See EX1001, cl. 1, 6, and 14; EX2003, ¶¶116-118.

B. Ground 2 (Verhaege in combination with Miller)

As tacit acknowledgement that Ground 1 (*i.e.*, single reference obvious over Verhaege) fails to meet various claim elements, Petitioner presents a second ground combining Verhaege with Miller. See Pet., §V.B. Petitioner’s proposed combination of Verhaege and Miller does not render the Challenged Claims

unpatentable for at least two independent reasons: (1) Petitioner fails to establish a reasonable expectation of success for the proposed modification; and (2) the combination fails to disclose the claimed “*enable circuitry*” and “*control circuit[ry]*.” EX2003, ¶¶119-120.

Petitioner relies on Miller (without citation) for its purported disclosure that “most integrated circuits had multiple I/O pads,” and that “Miller [uses] the ESD protection circuit of every I/O pad, in parallel, to disperse an ESD event more effectively.” Pet., 48. Patent Owner does not challenge that assertion here, with the caveat that Miller only uses the ESD protection circuitry of other I/O *cells*, not the actual I/O *pads* of the other I/O cells. EX2003, ¶¶76-81 (summarizing Miller reference).

Petitioner specifically cites Miller Fig. 3 (*see, e.g.,* Pet., 50) for its teaching “to use a single trigger line to carry the activation signal” between I/O cells. Pet., 51. This is shown below, where a single “transient detector circuit” 360 provides a “trigger” to clamps 320 and 340 in two I/O cells (which merely trigger shunting ESD charge between the Vdd and Vss rails, not between I/O *pads*).

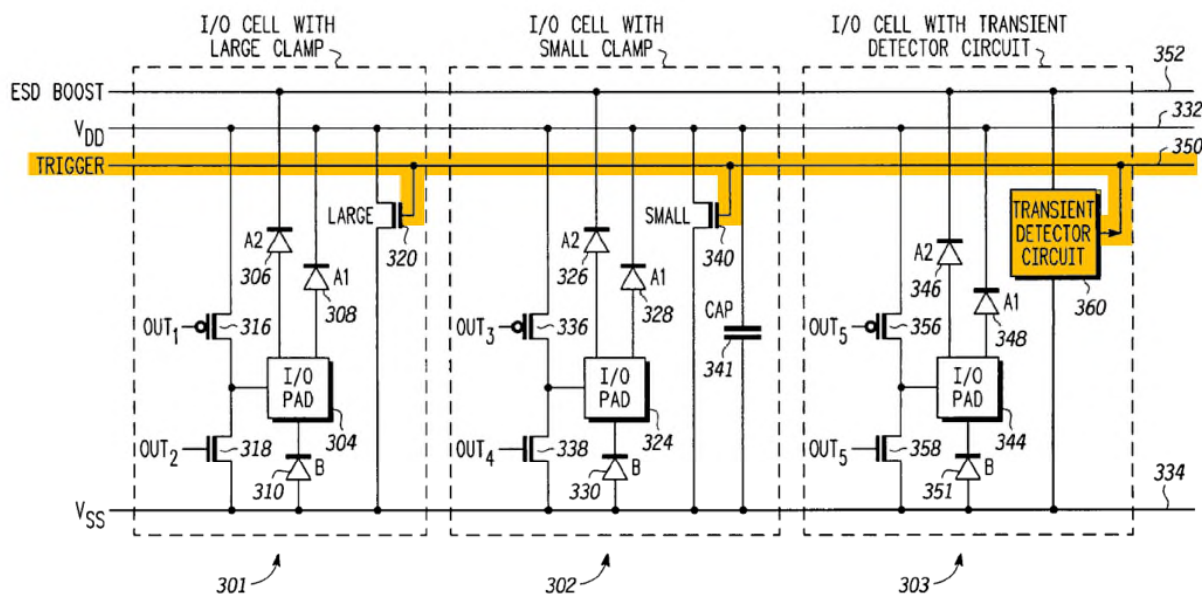
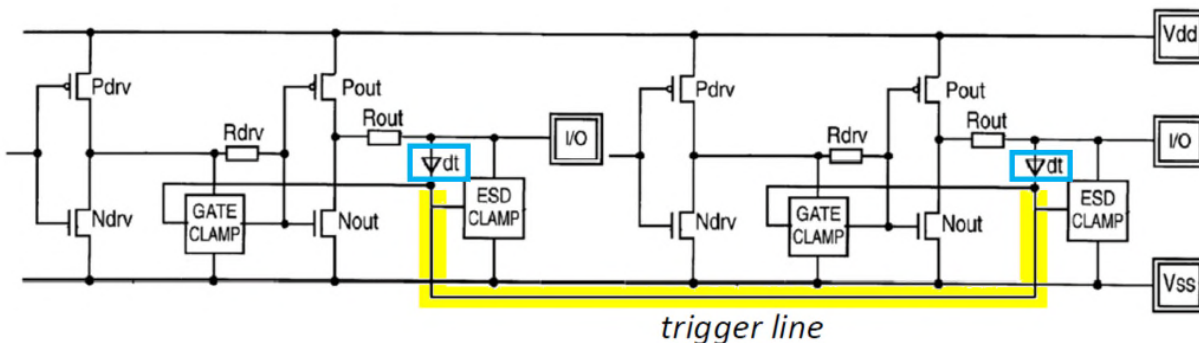


FIG. 3

EX1006, Fig. 3 (highlighted by Patent Owner). Notably, Miller shows *a single “detector circuit”* that provides the trigger signal for multiple I/O cells. *Id.*; EX2003, ¶81.

Petitioner modifies the disclosure and teachings of Miller in multiple ways when applying Miller to Verhaege. EX2003, ¶119. Most relevant here is that, unlike Miller, Petitioner’s modification to Verhaege leaves in place a dynamic trigger device (labelled “dt”) *in every I/O cell*, rather than having a single “detector circuit” shared across multiple I/O cells (as in Miller). Petitioner’s modification is shown below in yellow, which adds a dedicated “trigger line” connecting the triggers (dt) of two I/O cells.



Pet., 51 (modifications by Petitioner, highlighting by Patent Owner). In Petitioner’s words, its proposed combination is nothing more than “a simple modification to the Verhaege circuit—connecting the trigger devices as shown in Miller—to activate multiple pad circuits during an ESD event.” *Id.*, 48.

But, as explained below, Petitioner fails to establish a reasonable expectation of success for the proposed modification and, even if the modification were accepted, it does not satisfy the claim elements.

1. Petitioner Fails to Establish a Reasonable Expectation of Success

It is hornbook law that, for an obviousness combination, Petitioner bears the burden of showing a reasonable expectation of success vis-à-vis the proposed modification. *See, e.g., KEYnetik, Inc. v. Samsung Elecs. Co.*, 841 F. App’x 219, 227 (Fed. Cir. 2021) (“[Patent Owner] argues that the Board committed legal error in stating that ‘Petitioner has no [] burden to show that a POSITA would have had a reasonable expectation of success in combining the references.’ We agree with [Patent Owner] and remand to the Board.”); *see also id.*, 228 (“I agree with the

majority that the Board’s analysis ... was fundamentally flawed because it applied an incorrect legal standard. ... [T]he Board stated that [Petitioner] had no burden to establish a reasonable expectation of success from combining the prior art references at issue. We have held the exact opposite.”).¹¹ Petitioner has failed to meet its burden here. EX2003, ¶¶121-128.

Petitioner’s expectation of success analysis is (at best) totally conclusory, and states in its entirety:

A POSITA would reasonably expect this combination to succeed. First, the building blocks of both references—such as pads, transistors, clamp devices, and voltage rails—were well understood and behave in predictable ways when combined. (EX-1002 ¶137.) Second, a POSITA would expect the modification to succeed because incorporating the ESD strategy of Miller requires only a small change to Verhaege. Finally, the combination would foreseeably yield desirable results because an ESD protection circuit like Verhaege’s would benefit from sharing the ESD energy across multiple pad circuits as taught by Miller. (*Id.*)

Pet., 49. And Petitioner’s sole citation—to a single paragraph of its expert

¹¹ The Petitioner’s burden for reasonable expectation of success stands separate and independent from its burden to establish a motivation to combine. *Eli Lilly & Co. v. Teva Pharms. Int’l GmbH*, 8 F.4th 1331, 1344 (Fed. Cir. 2021).

declaration—is equally conclusory and practically a verbatim recitation of the Petition. The entirety of ¶137 of its expert declaration states:

A POSITA would reasonably expect this combination to succeed for at least three reasons. First, the components of both references—such as pads, transistors, clamp devices, and voltage rails—were well understood and behave in predictable ways when combined. Second, a POSITA would expect the modification to succeed because incorporating the ESD strategy of Miller requires only a small change to Verhaege. Third, the combination would foreseeably yield desirable results because an ESD protection circuit like Verhaege’s would benefit from sharing the ESD energy across multiple pad circuits as taught by Miller.¹²

EX1002, ¶137.

This is plainly insufficient, especially where Petitioner ignores significant architectural differences between Miller’s shared trigger approach and Petitioner’s proposed implementation in Verhaege. *See Qiagen N. Am. Holdings, Inc. v. Handylab, Inc.*, Nos. 2020-2249, 2020-2250, 2020-2273, 2020-2276, 2021 WL 5024387, at *4 (Fed. Cir. Oct. 29 2021) (affirming Board decision of no unpatentability where Petitioner “failed to establish by a preponderance of the

¹² Petitioner’s third argument (if relevant at all) relates to motivation to combine, not reasonable expectation of success.

evidence that a POSA would reasonably have expected to be successful in combining Zou I's microfluidic chip with a cartridge as taught by McNeely or Pease" because the Petitioner's analysis was "conclusory" and Petitioner's expert declaration "does not elaborate on reasonable expectation of success"); *see also*, *e.g.*, *Xerox Corp. v. Bytemark, Inc.*, IPR2022-00624, Paper 9, 15 (PTAB Aug. 24, 2022) (designated precedential Feb. 10, 2023) (denying institution by giving little weight to expert testimony that "merely repeats, *verbatim*, the conclusory assertion for which it is offered to support," and "does not cite to any additional supporting evidence or provide any technical reasoning [in] support").

What's more, the conclusory statements, even if true about the combination (they are not, *see infra*), would not establish a reasonable expectation of success. EX2003, ¶¶123-128. First, that the building blocks are of two ESD systems, by itself, is of no moment. This is tantamount to arguing any combination of two ESD circuits establishes a reasonable expectation of success—at bottom, allowing such an argument to suffice would eviscerate the requirement of establishing reasonable expectation of success altogether. Second, that the modification is allegedly a small change adds nothing. In circuitry, a small change, *e.g.*, adding one circuit element or one additional connection, can render a system inoperable, *e.g.*, by creating a non-drivable load, short-circuit, or bus contention. While it is not Patent Owner's burden, the below establishes that Petitioner's modification is

not a “small change” and raises these very inoperability issues, issues Petitioner improperly ignores.

In particular, the I/O cells in Miller share *a single control circuit* (i.e., “detector circuit” 360) for detecting an ESD condition. EX2003, ¶123. And the “trigger bus 350” (which transmits the “trigger” signal to the various I/O cells) is controlled and activated exclusively by the detector circuit 360, as can be seen in Miller Fig. 3 below. *Id.*, ¶¶121, 123.

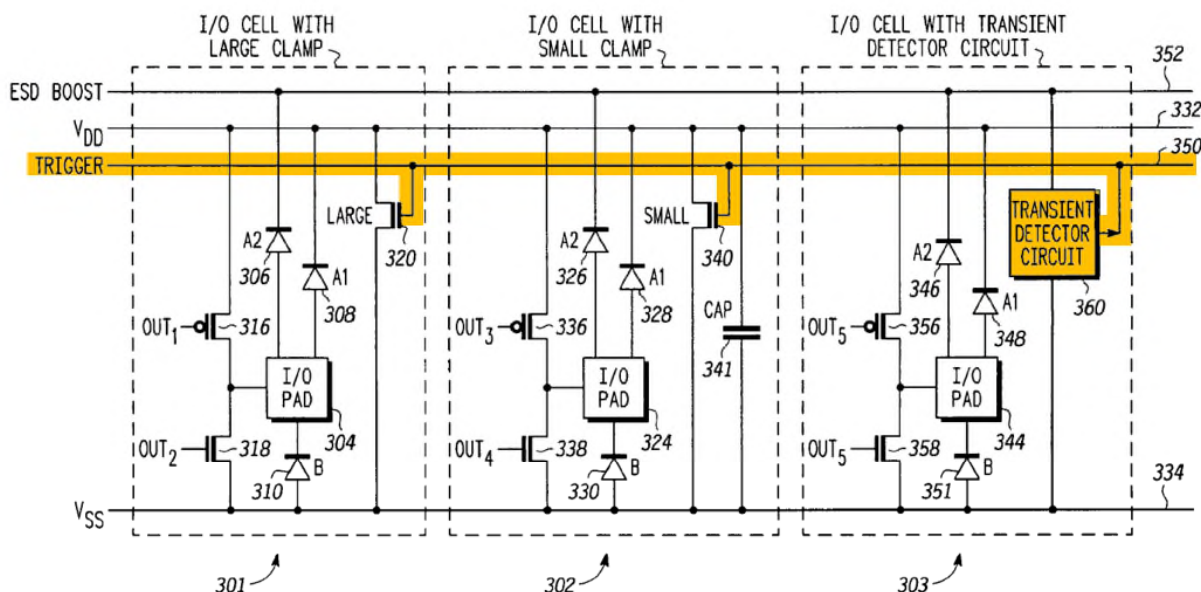
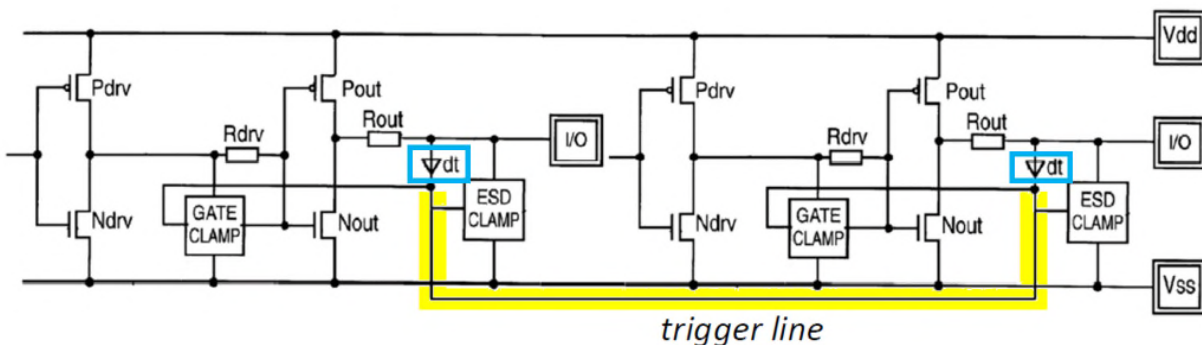


FIG. 3

EX1006, Fig. 3 (highlighted by Patent Owner). Because there is only one control mechanism (i.e., detector circuit 360) in Miller, there is no need to arbitrate between (or otherwise resolve) competing/conflicting circuits wishing to control trigger bus 350. EX2003, ¶¶125-127.

By contrast, Petitioner’s proposed modification to Verhaege in which multiple I/O cells have a common trigger line *has a “dynamic trigger device” circuit in each I/O cell* (shown by blue boxes in the figure below). Thus, there is a need for an arbitration scheme (or other design protocol) to determine how the “trigger line” will operate when one “dynamic trigger device” (labelled “dt”) in a first I/O cell is driving the trigger line low and another “dynamic trigger device” (also labelled “dt”) in a second I/O cell is driving the trigger line high. EX2003, ¶¶123-127. In other words, the two “dynamic trigger devices” in different cells may contend with each other to control the trigger line. This glaring failure becomes even more problematic because the dynamic triggers (dt) in each cell of Petitioner’s made-up embodiment are identical to each other, creating the possibility of a “tie” when driving opposite signals values on the trigger line Petitioner added. *Id.*



Pet., 51 (modifications by Petitioner, highlighting by Patent Owner).

Without a protocol/scheme to control priority of the trigger line, the overall

circuit proposed by Petitioner may not function properly, and could even be non-deterministic (*viz.*, producing different results under the same inputs). Thus, one cannot simply combine/modify Verhaege based on Miller in the way Petitioner proposes without accounting for this significant architectural difference between Miller and Verhaege. EX2003, ¶127. Petitioner and its expert completely ignore this issue and their conclusory assertions that “only a small change to Verhaege” is necessary and that “pads, transistors, clamp devices, and voltage rails” “were well understood” do not—and cannot—suffice to carry its burden of establishing a reasonable expectation of success.¹³ Pet., 49; EX1002, ¶137. Indeed, even if

¹³ Petitioner’s other assertion (repeated verbatim by its expert) that a reasonable expectation of success exists because “the combination would foreseeably yield desirable results because an ESD protection circuit like Verhaege’s would benefit from sharing the ESD energy across multiple pad circuits as taught by Miller” is a non-sequitur. Pet., 49; EX1002, ¶137. Even if a proposed combination might produce “desirable results” or “benefits,” that says nothing about whether the combination has a reasonable expectation of success. Moreover, Petitioner’s logic is pure hindsight and relies on the false premise that Miller discloses “sharing the ESD energy across multiple pad circuits.” Miller plainly discloses no such thing as

Petitioner’s bare bones assertion were somehow credited—which it should not be—the assertion is completely silent about trigger/control circuitry, arbitration schemes, and circuit operation when conflicting signals are trying to control the trigger line. This is a textbook case of a petitioner failing to meet its burden of establishing a reasonable expectation of success. *See* EX2003, ¶¶121-128.

2. Petitioner Fails to Show the Verhaege/Miller Combination Discloses or Renders Obvious the Claimed “*Enable Circuitry*” (Claim 1) and “*Control Circuitry*” (Claims 6 and 14)

For the reasons explained in §V.A.2 *supra*, Verhaege fails to disclose claim elements 1[f], 6[d], and 14[d]. Miller does not disclose these claim elements either. EX2003, ¶¶129-132; *see also id.*, ¶¶76-81. Indeed, Petitioner does not even argue that Miller does. *See generally* Pet., §V.B.

Rather, Petitioner contends that cherry-picking one teaching from Miller (*viz.*, a shared trigger line) and applying it to Verhaege results in a modified system that meets the missing claim elements. *See* Pet., §V.B. Petitioner is plainly incorrect, as explained below. Thus, even if Petitioner’s proposed modification to Verhaege were accepted—which it should not be for the reasons explained above—the resulting combination still does not render the Challenged Claims

the shared trigger line in Miller activates clamps that share excess ESD charge between the Vdd and Vss rails, not between pads. EX2003, ¶¶76-81.

obvious. EX2003, ¶¶129-132.

As discussed in §§II.B and IV.B *supra*, an important aspect of the '665 patent is that each I/O cell has *its own* control circuitry to detect an ESD event on an adjacent I/O pad and to activate (*viz.*, turn on) its own PMOS output transistor in response thereto. This allows ESD charge from the I/O pad where the ESD event occurred to flow to the pad of each I/O cell that detects the ESD event.

For example, independent claim 14 requires each pad (*viz.*, I/O cell) have its own “*respective control circuitry operable to: activate at least a portion of the respective output buffer in response to an ESD event to charge the respective pad capacitance ... as a result of the ESD event.*” Thus, even though Miller discloses a detector circuit in only one I/O cell, Petitioner cannot remove the dynamic trigger (dt) 42 from any of Verhaege’s I/O cells because the claim requires “*respective control circuitry*” in each cell.

Claim 1 has a similar requirement. Claim element 1[d] requires the claimed “*pad circuit*” have “*a control block configured, to turn on, when instructed, at least one of the one or more output transistor devices to charge the pad capacitance ... as a result of the ESD event.*” Petitioner maps the claimed “*control block*” to Verhaege’s “gate clamp 44.” Pet., 49. To the extent Petitioner argues claim 1 allows a control block in *another* I/O cell to provide the “instruct[ion]” for “turn[ing] on” the claimed output transistor (*e.g.*, the PMOS transistor), the

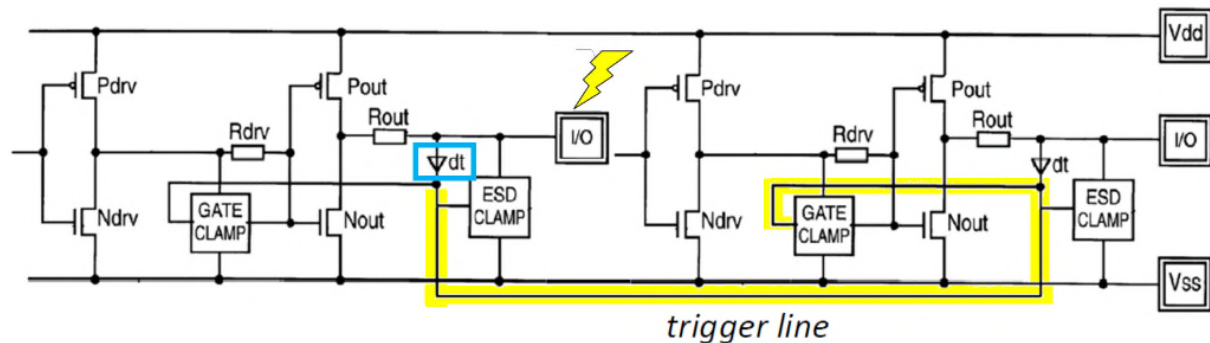
language of claim element 1[f] forecloses this possibility. Claim element 1[f] requires the “*pad circuit*” have “*enable circuitry configured to ... instruct the control block to turn on the at least one of the one or more output transistor devices, in response to the ESD event.*” Thus, it is the “*enable circuitry*” (which Petitioner maps to Verhaege’s trigger device 42, *see id.*, 21-22, 53) in the claimed I/O cell (not some other I/O cell) that must “*instruct the control block to turn on*” the PMOS output transistor.

Independent claim 6 likewise requires a “*control block*” that “*control[s] the output buffer*” (element 6[b]) and “*a control circuit*” (similar to the “*enable circuit[]*” in claim 1) that is “*configured to instruct the control block to activate at least a portion of the output buffer when an ESD event occurs*” (element 6[d]).

As discussed in §IV.B *supra*, the “ESD event” recited in claims 1, 6, and 14 that causes the PMOS transistor in the output buffer to turn on necessarily occurs in a *different* I/O cell than the cell being claimed.

Petitioner’s proposed modification to Verhaege is shown below, with an ESD event (lightning bolt) added by Petitioner to the left I/O pad. According to Petitioner, in this circumstance, the dynamic trigger (dt) in the blue box will generate and send a trigger signal on the trigger line (highlighted in yellow) to the righthand I/O cell’s gate clamp. Pet., 51. While the gate clamp in the I/O cell on the right will, according to Petitioner, then activate that cell’s Pout transistor, it

would do so based on the dynamic trigger (dt) in blue on the left, not the dynamic trigger (dt) in the righthand I/O cell. EX2003, ¶131. Thus, this combined circuitry—under Petitioner’s own theory of operation—fails to meet the requirements of claims 1, 6, and 14 as explained above, which all require the claimed I/O cell have *its own* “*control circuit[ry]*” or “*enable circuitry*” that turns on the output transistor (which Petitioner maps to Pout in Verhaege). *Id.*, ¶¶129-132.



Pet., 51 (modifications by Petitioner, highlighting by Patent Owner). Thus, even if Petitioner’s proposed modification to Verhaege based on Miller were implemented, the resulting circuit does not meet all the limitations of any Challenged Claim. EX2003, ¶¶129-132.

C. Ground 3 (Obviousness Over Ker)

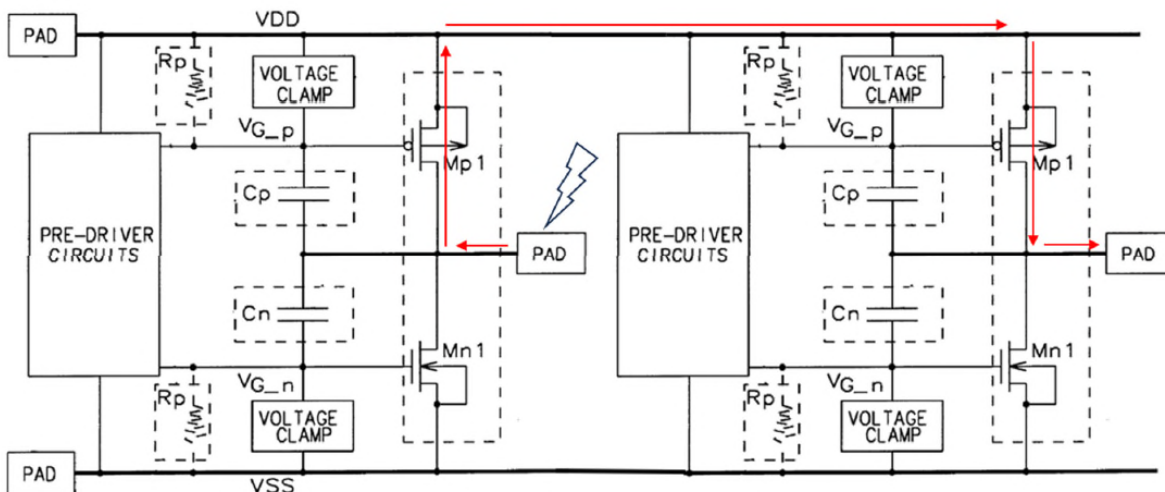
Petitioner’s arguments for Ground 3 fail for fundamentally the same reasons that Ground 1 fails—Ker does not disclose (or render obvious) ESD charge-sharing among pads, nor does Ker disclose the control circuitry to detect an ESD event in

another I/O pad and activate the necessary Pout transistor. EX2003, ¶¶133-151.

Rather, Ker employs the conventional technique of shunting charge resulting from an ESD event on a pad to a voltage rail, not another pad. *See supra* §§II.B and III.B; EX2003, ¶¶63-75. Petitioner fails to show how Ker satisfies claim elements 1[d], 1[f], 6[d], 6[e], or 14[d]. The requirements of those limitations have been discussed previously and will not be repeated here.

For Ground 3, Petitioner asserts all Challenged Claims are obvious over Ker (*i.e.*, single-reference obviousness). Pet., 10-11, §V.C. Notably, Petitioner does not contend Ker anticipates any Challenged Claim. *Id.*, 10-11. For example, Petitioner’s failure to assert that Ker actually discloses claim element 1[d] is a tacit admission it does not. *See id.*, fn.8 (admitting that “[w]ithout more, a signal port is not a control block.”); *id.* 64-65 (“Ker renders the limitation obvious A POSITA would have appreciated that the ESD detection circuits were interchangeable and would have understood how to modify the Figure 28 circuit to use the more advanced detection circuit shown in Figure 37 as the control block.”); *id.*, 66 (“Although Ker describes a single I/O pad circuit, a POSITA ... would have been motivated to repeat the Ker circuit at each I/O pad.”). Petitioner’s assertions for the corresponding limitations in independent claims 6 and 14 are substantially similar. *See id.*, 79 (claim 6, modifying Ker to “repeat the Ker circuit at every I/O pad”), 91-93 (claim 14, showing a modified version of Ker).

Lacking any anticipation arguments, Petitioner modifies Ker in multiple ways. Most relevant here is that (as with Verhaege) Petitioner creates the “two-cell” version of Ker (shown below) and relies on it for each of claims 1 (Pet., 67), claim 6 (*id.*, 79), and claim 14 (*id.*, 92).



Id., 67 (annotations added by Petitioner); *see also id.*, 79 (same), 92 (same).

Petitioner added the lightning bolt to the left pad to indicate where an ESD event occurs, and the red arrows to show the purported ESD current flow. *Id.*, 66-67.

To understand the flaws in Petitioner’s modified circuit, it is helpful to review certain of Petitioner’s claim mappings. Petitioner maps “Mp1” to the claimed “*one or more output transistors devices*” (claim 1, Pet., 62-63) and “*output buffer*” (claim 6, *id.*, 74-75; claim 14, *id.*, 90-91). And Petitioner maps the combination of Rp and Cp to the claimed “*enable circuitry*” (claim 1, *id.*, 69-70) and “*control circuit[ry]*” (claim 6, *id.*, 78-79; claim 14, *id.*, 93-94). Petitioner also

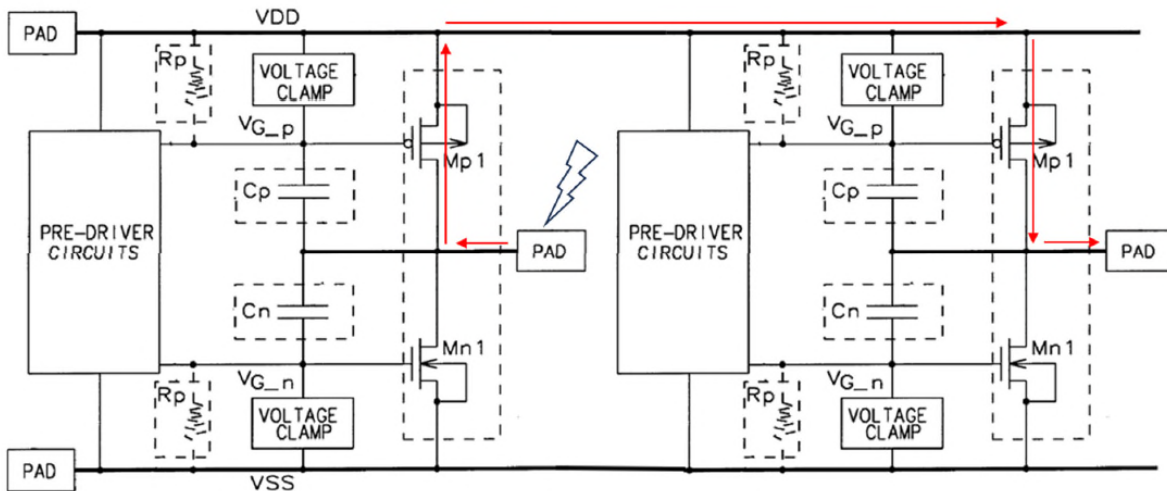
grafts on an additional transistor from Ker Fig. 37 (not shown in the image above but illustrated in orange in Petitioner’s expert declaration (EX1002) at ¶202) as the claimed “*control block*” in claims 1 and 6. Pet., 64-65 (claim 1), 75 (claim 6, “Ker teaches a control block comprising output signal ports VG_p and VG_n (orange) and other circuitry.”).

1. Petitioner Fails to Show Ker Discloses or Renders Obvious Charge-Sharing Between Pads

With Petitioner’s mapping in place, we can analyze Petitioner’s invalidity theory—and plainly show why it fails. EX2003, ¶¶134-137. It is unclear whether Petitioner relies on a positive ESD event or a negative ESD event for its Ker analysis, so Patent Owner address both scenarios. *Id.*, ¶¶135-136.

First, to the extent Petitioner’s theory is that a positive-polarity ESD event (*i.e.*, an accumulation of positive charge) on the left pad would cause current to flow as Petitioner’s red arrow shows, this is demonstrably incorrect. EX2003, ¶¶137-139. The reason is because a positive ESD event would raise the voltage on node VG_p, which controls the gate of output transistor Mp1. *Id.*, ¶137. Because Mp1 is a PMOS transistor, applying a positive/high voltage on the gate ***will turn the transistor off*** so no current will flow between the source and drain of the transistor. *Id.*, ¶41. This is a fundamental electrical engineering concept and Petitioner’s expert admits as much in his declaration (EX1002) at ¶¶21-25. Accordingly, any theory based on a positive ESD event on the pad fails *ab initio*.

Second, any theory premised on a negative-polarity ESD event (*i.e.*, accumulation of negative charge) on the left pad fares no better. EX2003, ¶¶140-147. To begin, it cannot legitimately be disputed that for charge-sharing between pads in Petitioner’s modified version of Ker below, the Mp1 transistors in both the left and right I/O cells must be turned on. *Id.*, ¶140. If either one is turned off, no current will flow along the path outlined by Petitioner in red arrows. *Id.* This is fatal as Petitioner fails to explain how a negative ESD-strike could activate both Mp1 transistors. *Id.*, ¶¶142-146.



Pet., 67 (annotation added by Petitioner).

Petitioner is correct that a negative ESD event on the left pad would cause the voltage on the lefthand V_{G_p} node to drop low enough to activate the connected Mp1 output transistor. However, even assuming Petitioner intended the red arrows

to reflect the flow of negative charge rather than the direction of current flow,¹⁴ Petitioner still utterly fails to show how the detection circuit (comprised of Rp and Cp) in either the left or right I/O cell would “*activate*” (claims 6 and 14) or “*turn on*” (claim 1) the Mp1 output transistor in the righthand I/O cell. EX2003, ¶¶142-147.

On this crucial point, Petitioner merely waves its hands, and simply asserts that, because there is a shared Vdd line “the ESD energy can flow to other pads connected to the rail as shown [in Petitioner’s modified figure].” Pet., 66-67 (claim 1); 79 (claim 6, similar), 92-93 (claim 14, similar). But, unless the righthand cell’s Mp1 transistor is activated—and Petitioner has not even attempted to show how or why it would be—no current can flow through it (*i.e.*, no current can flow the Vdd rail to righthand I/O pad). EX2003, ¶145.

The only I/O pad ESD event Ker discloses that turns on Mp1 in the righthand I/O cell is an ESD event on the righthand cell’s I/O pad itself. EX2003,

¹⁴ According to the fundamental engineering principle that current flows from high voltage to low voltage, current would flow *from Vdd downward through Mp1 onto the left pad*—the opposite of what Petitioner’s modified version of Ker shows. EX2003, ¶140, fn.8. In other words, Petitioner has the current flow direction backward. *Id.*

¶145. Thus, even if there were a purported voltage “increase” on the Vdd rail from the lefthand I/O cell, it would not travel down through the righthand cell’s Mp1 transistor (to the ESD detection capacitor) unless the righthand cell’s Mp1 transistor were already turned on. *Id.* This leaves Petitioner with a circular argument—the event that would cause Mp1 (in the righthand cell) to turn on requires that Mp1 already be turned on. *Id.*, ¶146. This makes no sense and does not establish a reasonable likelihood of success.

In summary, Petitioner has failed to show Ker renders obvious ESD charge-sharing between/among the pads.

2. Petitioner Fails to Show Ker Discloses or Renders Obvious the Claimed “*Enable Circuitry*” (Claim 1) and “*Control Circuit[ry]*” (Claim 6 and 14)

As explained *supra* §V.A.2, because the claims require the output transistor (which Petitioner maps to Mp1) to “*turn on*” (claim 1) or “*activate*” (claims 6 and 14), the logical implication is Mp1 is off to begin with. Otherwise, it could not “*activate*” / “*turn on*” because it would already be on/activated. EX2003, ¶148.

And, as previously explained, the claimed “*pad capacitance*” to which charge is being shared, and its associated “*enable circuitry*” (claim 1) and “*control circuit[ry]*” (claim 6 and 14), must be located in a different I/O cell than where the ESD event occurs. *See* §IV.B. Petitioner’s invalidity theory plainly shows the “lightning strike” on the left-hand cell. *See* Pet., 67. Thus, the claimed “*enable*

circuitry” and “*control circuit[ry]*” that turn on Mp1 (under Petitioner’s mapping) must be located in the righthand I/O cell. EX2003, ¶¶149-150.

But neither Petitioner nor its expert even attempt to explain how Rp and Cp (the purported “*enable circuitry*” (claim 1, *id.*, 69-70) and “*control circuit[ry]*” (claim 6, *id.*, 78-79; claim 14, *id.*, 91-93)) in the righthand I/O cell would detect an ESD event on the left I/O pad and turn on Mp1 in the righthand cell. *See* EX1002, ¶¶206 (claim 1), 239 (claim 6), 276 (claim 14); EX2003, ¶¶150-151.

On this crucial point, Petitioner merely waves its hands. The entirety of Petitioner’s analysis is pure say-so: “when output transistor Mp1 connects pad 500 to Vdd during an ESD event, allowing the ESD energy to flow to the Vdd rail, the ESD energy can flow to other pads connected to the rail as shown [in Petitioner’s modified figure].” Pet., 66-67 (claim 1); 79 (claim 6, similar), 92-93 (claim 14, similar). And Dr. Chen just parrots, practically verbatim, the same conclusory language. EX1002, ¶206. It is difficult to imagine a more conclusory opinion. Petitioner and its expert simply ignore the requirements of the claim language (discussed *supra* §IV.B) and totally fail to explain how or why dumping negative charge to the Vdd rail turns on Mp1 in the righthand I/O cell. EX2003, ¶¶150-151.

Indeed, the righthand I/O cell’s detection circuitry is nothing more than an instance of Ker’s single-cell embodiment, which was designed to be activated by

an ESD event on its own pad (*i.e.*, righthand I/O pad, not the left-hand circuitry).¹⁵ EX2003, ¶150. There is simply nothing about Ker’s disclosed single I/O cell that would, in Petitioner’s two-cell version of Ker, cause an ESD event in the lefthand I/O cell to activate the righthand cell’s Mp1 output transistor. *Id.*

Moreover, as was the case for Ground 1 (Verhaege), Petitioner has boxed itself in with circular reasoning: output transistor Mp1 (in the righthand I/O cell) must already be on for any current to flow from the Vdd rail to the righthand I/O pad. But Petitioner failed to show how Mp1 (in righthand I/O cell) could be turned on by the detection circuit *unless Mp1 was already on*. EX2003, ¶151. This is not the invention of the Challenged Claims.

In summary, Petitioner and its expert’s *ipse-dixit* does not, and cannot, establish a reasonable likelihood Ker renders any Challenged Claim obvious. *See, e.g., Xerox Corp. v. Bytemark, Inc.*, IPR2022-00624, Paper 9, 15 (PTAB Aug. 24, 2022) (designated precedential Feb. 10, 2023) (denying institution where expert

¹⁵ Because Ker discloses *only* a single I/O cell—not a combined embodiment—the righthand I/O cell’s functionality in Petitioner’s combined version of Ker is no different than if the righthand cell were a standalone I/O cell. Any other purported functionalities (such as operation in response to an ESD event on the lefthand I/O cell) are merely creations of Petitioner’s own making.

testimony “merely repeats, verbatim, the conclusory assertion for which it is offered to support,” and “does not cite to any additional supporting evidence or provide any technical reasoning [in] support”).

VI. PETITIONER OFFERS NO STIPLUATION AND THE BOARD SHOULD EXERCISE ITS DISCRETION TO DENY INSTITUTION UNDER 35 U.S.C. §314(A)

Petitioner raises no argument against discretionary denial under §314(a) in its Petition, and offers no stipulation that would dispense with a *Fintiv* analysis. The '665 patent is currently being litigated in Delaware district court by the same parties in *Microchip Technology Inc. v. Aptiv Services US, LLC*, No. 23-cv-778-JDW (DED). U.S. Pat. 9,471,074 (the '074 patent) is asserted in the same litigation and Petitioner has challenged that patent in IPR2024-00646.

The Board should exercise its discretion to deny institution because Petitioner is pursuing the same Verhaege (EX1004), Miller (EX1006), and Ker (EX1005) prior art references in district court. *See* EX2001, 5 (reference 1 is Verhege, reference 2 is Miller, and reference 4 is Ker); *see also id.*, 9 (“Exemplary Claim Chart” A-1 is based on Verhaege and A-2 is based on Ker). Petitioner creates the very situation—simultaneous and costly/duplicative litigation in multiple forums—that *inter partes* review was intended to avoid.

Factor 1. The district court case has not been stayed. Microchip is asserting two unrelated patents in the district court action and the Court has not indicated

whether it would stay the case if institution was granted as to only one patent.¹⁶ As such, this factor is neutral. *See, e.g., Samsung Elecs. Co. Ltd. v. Mojo Mobility Inc.*, IPR2023-01094, Paper 11, 7 (PTAB Feb. 9, 2024) (*Fintiv* “cautions against speculating whether the district court would grant a stay if one were requested ... Therefore, we weigh Factor 1 as neutral.”).

Factor 2. The projected statutory deadline for a final written decision is November 13, 2025. No trial date has been set in the district court. As such, prognosticating about a trial date would be speculative, but Patent Owner recognizes some Board decisions have viewed this circumstance as weighing against exercising discretion to deny institution.

Factor 3. The parties and court have made significant investments in the district court action. The Court held a *Markman* hearing on June 21, 2024 and construed the ’665 patent claims on July 15, 2024. *See* EX1012. And the parties already served infringement and invalidity contentions. *See* EX2001 (Petitioner’s invalidity contentions dated December 8, 2023; *Microchip Technology Inc. v. Aptiv Services US, LLC*, No. 23-cv-778-JDW (DED), Dkt. 34 (infringement contentions served October 27, 2023)). Moreover, the parties have already conducted

¹⁶ Patent Owner challenged the second patent in IPR2024-00646, which has an institution decision deadline of September 27, 2024.

substantial discovery, including taking and defending depositions, producing numerous documents and source code inspections, serving multiple third-party subpoenas, and serving and responding to numerous interrogatories. *See, e.g., id.*, Dkt. 28, 38, 49, 90 (third-party subpoenas); 18, 23, 26, 30, 32, 35-37, 41, 48, 50-51, 55-56, 58, 70, 73, 77, 79, 86, 93, 106-107, and 122 (interrogatories and responses). By the time of an institution decision, fact discovery will be even more advanced. This factor favors denying institution. *Samsung Elecs. Co. Ltd. v. Mojo Mobility Inc.*, IPR2023-01094, Paper 11, 9 (PTAB Feb. 9, 2024) (“this factor favors exercising our discretion to deny institution” where “[district court litigation] has already advanced well beyond the pleadings stage,” “claim construction will have been briefed and argued” before an institution decision, and “[f]act discovery is well underway”).

Factor 4. As noted, Petitioner is asserting the same IPR prior art references in district court. *See* EX2001, 5 (listing Verhaege, Miller, and Ker) and 9 (identifying claim charts for the Verhaege and Ker primary references). And Petitioner proffered no stipulation that would eliminate (or even reduce) duplicative litigation. This is significant because IPR statutory estoppel would not take effect until a final written decision in November of 2025. Thus, there is substantial (if not complete) overlap with the IPR and this factor favors discretionary denial. *See, e.g., Apcon, Inc. v. Gigamon Inc.*, IPR2020-01579,

Paper 9, 26 (PTAB Mar. 16, 2021) (denying institution where “the art appears substantially the same, and no stipulation has been filed by Petitioner agreeing not to assert the same art.”); *Intel Corp. v. Koninklijke Philips N.V.*, IPR2021-00328, Paper 16, 5 (PTAB Mar. 29, 2022) (“We also emphasized that complete overlap is not required, that substantial overlap of issues may be sufficient, and that Petitioner had provided no stipulation that it would not pursue any ground that could be raised under §§ 102 or 103 on the basis of prior art patents or printed publications.”).

Factor 5. The parties are the same in district court and the IPR. This factor favors discretionary denial. *See, e.g., Samsung Elecs. Co. Ltd. v. Mojo Mobility Inc.*, IPR2023-01094, Paper 11, 13 (PTAB Feb. 9, 2024) (“[T]his factor weighs in favor of a discretionary denial” where “the same parties are involved in both the present proceeding and the parallel [district court litigation]”); *Teradata Corp. v. SAP SE*, IPR2020-00943, Paper 12, 18 (PTAB Nov. 25, 2020).

Factor 6. As described herein, the Petition suffers from major defects (*e.g.*, no cited art discloses or renders obvious a key claim limitation—control circuitry that triggers ESD charge-sharing when an ESD event occurs in another pad) which counsels in favor of discretionary denial under *Fintiv* Factor 6.

In summary, most *Fintiv* factors favor denial (or are neutral) and the Board

should exercise its discretion under §314(a) to deny institution.

VII. CONCLUSION

For the above reasons, Patent Owner respectfully requests that the Board deny institution.

Respectfully submitted,

Dated: August 13, 2024

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CERTIFICATE OF COMPLIANCE

The undersigned certifies that the foregoing PATENT OWNER'S PRELIMINARY RESPONSE complies with the type volume limitation in 37 C.F.R. § 42.24(c)(1). According to the utilized word-processing system's word count, the petition—excluding the caption, table of contents, table of exhibits, mandatory notices, certificate of word count, and certificate of service—contains 13.925 words.

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CERTIFICATE OF SERVICE

The undersigned certifies that on August 13, 2024, a copy of the following was served in its entirety via electronic mail, upon the following attorneys of record for Petitioner:

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