

**IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE**

MICROCHIP TECHNOLOGY INC.,	)	
	)	
Plaintiff,	)	
	)	
v.	)	C.A. No. 23-778-JDW
	)	
APTIV SERVICES US, LLC,	)	
	)	
Defendant.	)	

APTIV SERVICES US, LLC’S INITIAL INVALIDITY CONTENTIONS

I. INTRODUCTION

Pursuant to the Court’s Scheduling Order (D.I. 24), Defendant Aptiv Services US, LLC (“Aptiv”) hereby provides its Initial Invalidity Contentions in response to Microchip Technology, Inc.’s (“Microchip”) Corrected Initial Infringement Contentions, served December 5, 2023. Specifically, Aptiv addresses the following claims asserted by Microchip (the “Asserted Claims” of the “Asserted Patents”):

- U.S. Patent No. 7,564,665 (the “’665 Patent”), claims 1-3, 5-7, and 10-18
- U.S. Patent No. 9,471,074 (the “’074 Patent”), claims 1-9, 11-12, and 15-17

(Corrected Initial Infringement Contentions at 1).

Discovery and Aptiv’s investigation continue. These disclosures are based on Aptiv’s current knowledge and understanding of the Asserted Patents, Microchip’s infringement theories, the prior art, and other facts and information available at this early stage of the case. Aptiv reserves the right to amend, modify, and/or supplement these Contentions based on new or different information learned in discovery or in view of Microchip’s assertions in this case.

The parties have not yet engaged in claim construction disclosures or briefing and the Court has not yet construed the Asserted Claims. Accordingly, Aptiv reserves the right to amend, modify, and/or supplement these Contentions in view of any claim construction order. Aptiv further reserves the right to amend, modify, or supplement these Contentions in response to any proposed claim construction or alleged supporting evidence offered by Microchip, any report from any expert witness for Microchip regarding claim construction, any claim construction briefing filed by Microchip, and any position taken by Microchip concerning claim construction.

To the extent that these Contentions reflect interpretations of claim limitations that may be consistent with or implicit in Microchip's Preliminary Infringement Contentions, no inference is intended nor should be drawn that Aptiv agrees with such interpretations. These Contentions are not intended to reflect Aptiv's claim construction positions, which will be disclosed in due course in accordance with this Court's Scheduling Order. Aptiv's Contentions, including the attached claim charts, may reflect alternative positions as to claim construction and claim scope.

The accompanying claim charts list specific examples of prior art that included and/or disclosed, either expressly or inherently, each limitation of the identified claims and/or made obvious each limitation of the identified claims. Aptiv has endeavored to identify relevant portions and/or features of the identified prior art. The identified prior art, however, may contain additional descriptions of or alternative support for the claim limitations. The citations included in each chart are illustrative, not exhaustive. Aptiv may rely on un-cited portions or features of the identified prior art, other documents, and fact and expert testimony to provide context or to aid in understanding the identified prior art. Where Aptiv cites to a particular figure in a reference, the citation should be understood to encompass the caption and description of the

figure and any text relating to the figure. Similarly, where Aptiv cites to particular text referring to a figure, the citation should be understood to include the figure and caption as well.

Moreover, as certain prior art references and inventions are described in multiple related patents or publications with similar or identical specifications or disclosures, to the extent Aptiv has identified a citation in one reference, Aptiv reserves the right to rely on parallel or similar citations in related patents or publications. A person of ordinary skill in the art (“POSA”) would read a prior art reference and understand a prior art invention as a whole and in the context of other publications and known technologies. Therefore, to understand and interpret any specific statement or disclosure of a prior art reference or invention, such persons would rely on other information within the reference or invention, along with other publications and known technologies. Aptiv reserves the right to establish what was known to a POSA through other publications, products, and/or testimony. Aptiv also reserves the right to rely on uncited portions of the prior art references, other publications, and testimony to establish that a POSA would have been motivated to combine certain of the cited references so as to render the claims obvious.

Aptiv may also rely on other documents and information, including inventor admissions, concerning the scope of the Asserted Claims, and prior art relevant to the Asserted Claims, referenced in: the Asserted Patents; the patent prosecution histories for the Asserted Patents, and related patents and/or patent applications; any deposition testimony of any inventor of the Asserted Patents; and any papers filed or any evidence produced or submitted by Microchip in connection with this litigation related to the Asserted Patents. In particular, Aptiv reserves the right to contend that the Asserted Claims are invalid under 35 U.S.C. § 102(f) in the event that Aptiv obtains evidence that the inventors named on the Asserted Patents did not invent (either alone or in conjunction with others) the subject matter claimed in the Asserted Patents.

Aptiv's investigation of prior art systems and products is ongoing. Aptiv has diligently sought and will continue to diligently seek discovery from Microchip and third parties to demonstrate earlier invention by Microchip and/or third parties and reserves its right to contend that the Asserted Claims are invalid under 35 U.S.C. § 102(g). To date, Microchip has not produced all relevant discovery requested by Aptiv regarding, among other things, prior art systems and products; therefore, Aptiv reserves the right to raise any such or further deficiencies with Microchip and/or the Court as needed and further reserves the right to amend, modify, and/or supplement its Contentions. Aptiv's further investigation and/or subsequent discovery from Microchip or third parties with knowledge regarding prior art systems and products may reveal additional relevant prior art systems and products and/or further information regarding the systems and products in these Contentions. Aptiv reserves the right to amend, modify, and/or supplement these Contentions, based on further and subsequent investigation and discovery.

Based on Aptiv's present understanding of the Asserted Claims and/or Microchip's apparent construction of the claims, as set forth in Microchip's Infringement Contentions, Aptiv has identified grounds for invalidating Asserted Claims based on indefiniteness, lack of enablement, or insufficient written description under 35 U.S.C. § 112. Aptiv is not adopting Microchip's apparent constructions, nor is Aptiv agreeing that any of Microchip's apparent constructions are correct. Aptiv reserves all rights to advance claim construction positions different from Microchip's apparent constructions. Moreover, Microchip's deficient Infringement Contentions fail to provide Aptiv with adequate notice as to Microchip's infringement theories. Aptiv thus reserves the right to amend, modify, and/or supplement these initial Contentions to further identify bases for invalidity under 35 U.S.C. § 112.

II. EXEMPLARY KNOWLEDGE OF A PERSON OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art at the time of the alleged invention would have had at least a Master's degree in electrical engineering, computer engineering, or a related field and three to five years of experience in integrated circuit device design. Additional education may substitute for some work experience and relevant work experience may substitute for additional formal education.

III. PRIOR ART

Aptiv contends that the Asserted Claims are invalid under 35 U.S.C. §§ 102 and/or 103 based on the following prior art references and systems. Aptiv reserves the right to supplement this list as it learns in the course of discovery of other prior art that would anticipate and/or render obvious the Asserted Claims.

A. Prior Art Patent Publications

The following patent publications constitute prior art to the '665 Patent under 35 U.S.C. § 102(a)(2) because they are issued patents or patent applications that name another inventor and were effectively filed before January 10, 2007. All of these publications are also prior art under § 102(a)(1) because they issued or published before January 10, 2007.

Ref. No.	Publication No.	Short Name	Filing Date	Publication Date
1	US 6,529,359	Verhaege	Aug. 4, 2000	Mar. 4, 2003
2	US 7,589,945	Miller	Aug. 31, 2006	Mar. 13, 2008
3	US 5,168,178	Allen	Aug. 30, 1991	Dec. 1, 1992
4	US 6,249,410	Ker	Aug. 23, 1999	Jun. 19, 2001
5	US 6,385,021	Takeda	April 10, 2000	May 7, 2002
6	US 2004/0027742	Miller '742	August 9, 2002	Feb. 12, 2004
7	US 6,522,511	John	Jun. 15, 2000	Feb. 18, 2003

Ref. No.	Publication No.	Short Name	Filing Date	Publication Date
8	US 7,508,639	Wu	Dec. 19, 2005	Jun. 1, 2006
9	US 7,545,614	Traynor	Sep. 30, 2005	Apr. 5, 2007
10	US 7,692,905	Hung	Nov. 28, 2006	Aug. 29, 2008
11	US 7,742,265	Rice	Jun. 6, 2005	Dec. 7, 2006
12	US 2006/0028776	Stockinger	Aug. 9, 2004	Feb. 9, 2006

The following patent publications constitute prior art to the '074 Patent under 35 U.S.C. § 102(a)(2) because they are issued patents or patent applications that name another inventor and were effectively filed before Mar. 14, 2013. All of these publications are also prior art under § 102(a)(1) because they issued or published before Mar. 14, 2013.

Ref. No.	Publication No.	Short Name	Filing Date	Publication Date
13	US 2003/0178976	Xi	Mar. 25, 2003	Sep. 25, 2003
14	US 6,246,221	Xi '221	Sep. 20, 2000	Jun. 12, 2001
15	US 6,046,577	Rincon-Mora '577	Dec. 30, 1997	Apr. 4, 2000
16	US 6,700,360	Biagi	Mar. 25, 2002	Sep. 25, 2003
17	US 6,710,583	Stanescu	Jan. 10, 2003	Jun. 5, 2003
18	US 6,177,785	Lee	Sep. 29, 1999	Jan. 23, 2001

B. Prior Art Non-Patent Publications

The following non-patent publications also constitute prior art to the '074 Patent. Specifically, the publications are prior art under § 102(a)(1) because they are printed publications published before Mar. 14, 2013.

Ref. No.	Publication	Short Name	Publication Date
18	Rincon-Mora, G. A. (1996) Current Efficient, Low Voltage, Low Drop-Out Regulators [Doctoral dissertation, Georgia Institute of Technology]	Rincon-Mora Dissertation	Nov. 1996

Ref. No.	Publication	Short Name	Publication Date
20	G. A. Rincon-Mora and P. E. Allen, "A low-voltage, low quiescent current, low drop-out regulator," in IEEE Journal of Solid-State Circuits, vol. 33, no. 1, pp. 36-44, Jan. 1998	Rincon-Mora Paper	Jan. 1998
21	Yang, Huan-Chien & Huang, Ming-Hsin & Chen, Ke-Horng. (2008). High-PSR-Bandwidth capacitor-free LDO regulator with 50 μ A minimized load current requirement for achieving high efficiency at light loads. WSEAS Transactions on Circuits and Systems. 7. 428-437.	Yang	May 2008
22	J. Hu, B. Hu, Y. Fan and M. Ismail, "A 500 nA quiescent, 100 mA maximum load CMOS low-dropout regulator," 2011 18th IEEE International Conference on Electronics, Circuits, and Systems, Beirut, Lebanon, 2011, pp. 386-389	Hu	Dec. 2011
23	M. Al-Shyoukh, H. Lee and R. Perez, "A Transient-Enhanced Low-Quiescent Current Low-Dropout Regulator With Buffer Impedance Attenuation," in IEEE Journal of Solid-State Circuits, vol. 42, no. 8, pp. 1732-1742, Aug. 2007	Al-Shyoukh	Aug. 2007
24	Vinson, James E., Bernier, Joseph C., Croft, Gregg D., and Liou, Juin J., "ESD Design and Analysis Handbook," Springer New York, NY 2003	Vinson	Dec. 2003
25	K. Wong and D. Evans, "A 150mA Low Noise, High PSRR Low-Dropout Linear Regulator in 0.13 μ m Technology for RF SoC Applications," 2006 Proceedings of the 32nd European Solid-State Circuits Conference, Montreaux, Switzerland, 2006, pp. 532-535	Wong	Feb. 2007
26	J. Choi <i>et al.</i> , "Design of LDO linear regulator with ultra low-output impedance buffer," 2009 International SoC Design Conference (ISOCC), Busan, Korea (South), 2009, pp. 420-423.	Choi	Nov. 2009
27	Kitchin, Charles, "Biasing and Decoupling Op Amps in Single Supply Applications," AN-581 Application Note (2002)	Kitchin	2002
28	Wolbert, Bob, "Micrel's Guide to Designing with Low-Dropout Voltage Regulators," December 1998	Wolbert	Dec. 1998
29	Garimella, A., Furth, P.M., Surkanti, P.R. et al. Current buffer compensation topologies for LDOs with improved transient performance. <i>Analog Integr Circ Sig Process</i> 73, 131–142 (2012).	Garimella	Nov. 2011

C. Prior Art Systems

The following systems also constitute prior art to the '074 Patent. These systems are prior art under § 102(a)(1) because they were in public use, on sale, or otherwise available to the public before Mar. 14, 2013. The OPTIREG device was in public use, on sale, or otherwise available to the public by at least Mar. 20, 2007. Likewise, the MIC59300 device was in public use, on sale, or otherwise available to the public by at least January 2009.

Ref. No.	Name of System	Short Name	Date of Offer/Use/Release	Identity of Provider
30	OPTIREG™ Linear TLE4271-2	OPTIREG	Mar. 20, 2007	Infineon Technologies AG
31	Micrel Ultra High Speed 3A LDO MIC59300	MIC59300	Jan. 2009	Micrel, Inc.

IV. INVALIDITY GROUNDS

A. Anticipation

Aptiv contends that the Asserted Claims are invalid under 35 U.S.C. § 102 as being anticipated or rendered obvious by the prior art identified in Table 1 below. Under 35 U.S.C. § 102(a), a person is not entitled to a patent if the “claimed invention was patented, described in a printed publication, or in public use, on sale, or otherwise available to the public before the effective filing date of the claimed invention.”

Aptiv provides an exemplary claim chart for each Asserted Patent with citations illustrating how the prior art anticipates every element of the Asserted Claims. Aptiv reserves the right to supplement its contentions based on additional discovery, including discovery from the provider of the identified prior art systems, and Microchip’s assertions in this case.

Table 1: Anticipation Prior Art

Reference	Patent	Exemplary Claim Chart
Verhaege	'665 Patent	A-1
Ker	'665 Patent	A-2
Al-Shyouk	'074 Patent	B-1
Xi	'074 Patent	B-2
Rincon-Mora '577	'074 Patent	B-3
Hu	'074 Patent	B-4
Yang	'074 Patent	B-5
Rincon-Mora Paper	'074 Patent	B-6
Rincon-Mora Dissertation	'074 Patent	B-7
Xi '221	'074 Patent	B-8

B. Obviousness

Aptiv also contends that the Asserted Claims are invalid under 35 U.S.C. § 103 as being obvious in view of the prior art identified in Table 2 below. Under 35 U.S.C. § 103(a), an applicant is not entitled to a patent “if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious” to a POSA at the time the invention was made. The relevant factual inquiries include:

- (a) determining the scope and content of the prior art;
- (b) ascertaining the differences between the prior art and the claims at issue;

(c) resolving the level of ordinary skill in the pertinent art; and

(d) evaluating evidence of secondary considerations.

Graham v. John Deere Co. of Kansas City, 383 U.S. 1, 17-18 (1966). The Supreme Court reiterated the applicability of the *Graham* factors in *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398 (2007).

Aptiv provides an exemplary claim chart for each Asserted Patent with citations illustrating how the prior art discloses or renders obvious every element of the Asserted Claims, including in combination with other prior art or the knowledge of a POSA. Aptiv reserves the right to supplement its contentions based on additional discovery, including discovery from the provider of the identified prior art systems, and Microchip's assertions in this case.

Table 2: Obviousness Prior Art

Reference	Patent	Exemplary Claim Chart
Verhaege	'665 Patent	A-1
Ker	'665 Patent	A-2
Miller	'665 Patent	A-1
Takeda	'665 Patent	A-1
Al-Shyoukh	'074 Patent	B-1
Xi	'074 Patent	B-2
Rincon-Mora '577	'074 Patent	B-3
Yang	'074 Patent	B-4
Hu	'074 Patent	B-5

Rincon-Mora Paper	'074 Patent	B-6
Rincon-Mora Dissertation	'074 Patent	B-7
Xi '221	'074 Patent	B-8
Lee	'074 Patent	B-1
Wolbert	'074 Patent	B-1
Kitchin	'074 Patent	B-1
OPTIREG	'074 Patent	B-1
MIC59300	'074 Patent	B-1
Stanescu	'074 Patent	B-1

1. Prior Art Combinations

The Asserted Claims are obvious based on one or more combinations of the prior art identified in Table 2 above. With respect to the anticipating prior art systems (identified in Table 1), Aptiv contends in the alternative that each of those systems renders the Asserted Claims obvious either alone or in combination with the knowledge of a POSA and/or the other references identified in Table 2. Aptiv further identifies the following exemplary combinations of references identified in Table 2:

- Verhaege in view of Miller or Takeda
- Ker in view of Miller or Takeda
- Al-Shyoukh in view of Kitchin or MIC59300

- Al-Shyoukh in view of Lee or Xi or Rincon-Mora '577 or Wolbert or OPTIREG or MIC59300
- Al-Shyoukh in view of Yang or Stanescu
- Al-Shyoukh in view of Rincon-Mora '577
- Al-Shyoukh in view of Hu
- Xi in view of Kitchin or MIC59300
- Xi in view of Lee or Rincon-Mora '577 or Wolbert or OPTIREG or MIC59300 or Al-Shyoukh
- Xi in view of Al-Shyoukh or Hu
- Xi in view of Rincon-Mora '577
- Xi in view of Yang or Al-Shyoukh or Stanescu
- Rincon-Mora '577 in view of Kitchin or MIC59300
- Rincon-Mora '577 in view of Lee or Xi or Wolbert or OPTIREG or MIC59300 or Al-Shyoukh
- Rincon-Mora '577 in view of Rincon-Mora Paper or Al-Shyoukh or Hu
- Rincon-Mora '577 in view of Yang or Al-Shyoukh or Stanescu
- Yang in view of Kitchin or MIC59300
- Yang in view of Lee or Xi or Rincon-Mora '577 or Wolbert or OPTIREG or MIC59300 or Al-Shyoukh
- Yang in view of Al-Shyoukh or Hu

- Yang in view of Al-Shyoukh or Stanescu
- Hu in view of Kitchin or MIC59300
- Hu in view of Lee or Xi or Rincon-Mora '577 or Wolbert or OPTIREG or MIC59300 or Al-Shyoukh
- Hu in view of Al-Shyoukh
- Hu in view of Rincon-Mora '577
- Hu in view of Yang or Al-Shyoukh or Stanescu
- Rincon-Mora Paper in view of Kitchin or MIC59300
- Rincon-Mora Paper in view of Lee or Xi or Rincon-Mora '577 or Wolbert or OPTIREG or MIC59300 or Al-Shyoukh
- Rincon-Mora Paper in view of Al-Shyoukh or Hu
- Rincon-Mora Paper in view of Yang or Al-Shyoukh or Stanescu
- Rincon-Mora Dissertation in view of Kitchin or MIC59300
- Rincon-Mora Dissertation in view of Lee or Xi or Rincon-Mora '577 or Wolbert or OPTIREG or MIC59300 or Al-Shyoukh
- Rincon-Mora Dissertation in view of Al-Shyoukh or Hu
- Rincon-Mora Dissertation in view of Yang or Al-Shyoukh or Stanescu
- Xi '221 in view of Kitchin or MIC59300
- Xi '221 in view of Lee or Xi or Rincon-Mora '577 or Wolbert or OPTIREG or MIC59300 or Al-Shyoukh

- Xi '221 in view of Al-Shyoukh or Hu
- Xi '221 in view of Rincon-Mora '577
- Xi '221 in view of Yang or Al-Shyoukh or Stanescu

The combinations provided are exemplary and are not intended to be exhaustive. In addition to the specific prior art reference and combinations identified above, the further combination of these references and combinations with the background knowledge of a person of ordinary skill in the art at the time of the alleged invention render the Asserted Claims obvious. To the extent that Microchip contends that a particular claim limitation is not taught in a particular reference, a POSA would have been motivated to combine that reference with any of the other references cited herein or in the accompanying charts to arrive at the allegedly missing limitation and would have had an expectation that such a combination would be successful. Furthermore, Aptiv reserves the right to use additional obviousness combinations of the identified references or references yet to be identified. In particular, Microchip has yet to fully disclose its interpretation of the Asserted Claims because its infringement contentions rely extensively on illegible and incomplete documents.

2. Motivation to Combine and Expectation of Success

a. The '665 Patent

A POSA would have been motivated to combine and expected to succeed in combining the teachings of the prior art in Table 2 to arrive at the invention claimed in the '665 patent. The core components of the Asserted Claims of the '665 patent—pads, output transistors, clamp devices, and voltage rails—were well known by January 10, 2007, the earliest identified priority

date for the '665 patent.¹ The specification of the '665 patent acknowledges that the problem of electrostatic discharge (“ESD”) was well-known in the field and that the problem was only becoming more pronounced as integrated circuits have increased in density and operating supply voltage levels decrease, causing increased sensitive to ESD charges. *See* '665 patent at 1:11-21. The specification further acknowledges that, by the time the specification was filed, “various techniques for improving ESD performance” had already “been devised, published, and/or patented.” *See* '665 patent at 2:8-11.

Verhaege teaches an ESD protection circuit that utilizes a clamp device to control the gates of a pair of CMOS output drivers, thereby redirecting the ESD charge to a voltage rail, allowing the charge to dissipate. Verhaege discloses a “circuit for the protection of an output driver NMOS transistor during EOS/ESD stress.” Verhaege at Abstract. The circuits disclosed in Verhaege include “[a]n I/O pad [that] is connected to the junction between the output driver transistors” and “a clamp which is dynamically trigger[ed] during the EOS/ESD stress so as to ground the gate of the output driver NMOS transistor.” Verhaege at col. 1 lines 38-39; col. 4 lines 45-47.

Similarly, Ker teaches an ESD protection circuit that uses an ESD detection circuit to open the gate of either a PMOS or NMOS output transistor in the event of ESD charge and allows the charge build up to dissipate via the voltage rail. In the event of a large ESD charge

¹ According to Microchip’s Supplemental Response to Aptiv’s Interrogatory No. 4, “the claimed inventions of U.S. Patent No. 7,564,665 (“’665 patent”) were conceived in 2006. The application that led to the '074 patent was filed on January 10, 2007,” however, in Microchip’s initial Response to Aptiv’s Interrogatory No. 4, Microchip stated that “[t]he application that led to the '074 patent was filed on March 11, 2014.” It is Aptiv’s understanding that Microchip intended to refer to the '665 patent when citing the application date of January 10, 2007. In any case, Aptiv reserves the right to amend, modify, and/or supplement these Contentions based on new or different information learned in discovery or in view of Microchip’s assertions in this case.

that may damage the CMOS output transistor, Ker teaches a clamp device that directly connects an I/O pad with the voltage rail, bypassing the output transistor.

Miller teaches a distributed ESD protection system that utilizes clamp transistor devices connected to each I/O cell in an I/O bank. When an ESD event occurs, the system “can provide efficient ESD protection since the clamp transistor devices, which are wired in parallel between V_{DD} bus and a V_{SS} bus, can work together to dissipate the ESD currents.” Miller at [0032].

Takeda likewise teaches a distributed ESD protection system that uses clamps at the individual pad circuit level to dissipate ESD charge at the I/O array level. *See e.g.*, Takeda at Abstract (describing “[a]n ESD protection circuit [] coupled to each of a plurality of I/O circuits . . . The individual ESD protection circuits operate in parallel to provide ESD protection to the I/O circuits [] upon occurrence of an ESD event.”).

A POSA would have been motivated to combine the systems taught in Miller and Takeda with the individual clamp circuits taught in Verhaege and Ker because each reference is directed to the concept of protecting an integrated circuit against ESD damage. Verhaege and Ker are both directed to lower-level systems aimed at dissipating charge from a single I/O pad circuit. Miller and Takeda are one step removed from this, and describe systems for dissipating charge across an entire I/O bank. Because most integrated circuits comprise an I/O bank as opposed to a single I/O pad, a POSA would have been motivated to take the individual ESD protection circuits described in Verhaege and Ker and replicate them across the entire bank, as described in Miller and Takeda. A POSA would likewise have been motivated to take the ESD protection arrays taught in Miller and Takeda and improve upon them by using the individual pad protection circuits taught in Verhaege and Ker.

The clamp transistor devices described in Miller and Takeda are relatively simple and a POSA would have understood that utilizing the more robust circuits taught by Verhaege and Ker would result in improved performance. A POSA would expect this combination to work because the circuits described in Verhaege and Ker, like the clamp circuits described in Miller and Takeda, redirect ESD charge onto voltage rails. In essence, the system taught in Miller and Ker is agnostic as to the particular clamping circuit used, so long as those circuits “are wired in parallel between V_{DD} bus and a V_{SS} bus [and] can work together to dissipate the ESD currents.” Miller at 7:63:67. In fact, Miller itself explains that “though the clamp transistor devices are illustrated herein as n-channel MOSFETS, other clamp devices . . . may be used without departing from the scope of the present disclosure.” Miller at 3:52-58.

b. The '074 Patent

A POSA would have been motivated to combine and expected to succeed in combining the teachings of the '074 obviousness references disclosed in Table 2.

The core components of the Asserted Claims of the '074 patent—operational amplifiers, gm-enhanced current buffers, gm-boost circuits, and feedback loops—were well known by March 11, 2014, the earliest possible priority date for the '074 patent. The specification of the '074 patent further acknowledges that low-drop out (LDO) voltage regulators were well known, as was their use with USB systems. See '074 patent at Background.

It would have been obvious to a POSA designing a low-quiescent current LDO voltage regulator to review Xi, Al-Shyoukh, Rincon-Mora Paper, Rincon-Mora Dissertation, Rincon-Mora '577, Hu, Yang, and Xi '221 because each reference discusses that, with the increasing prevalence of battery powered electronic devices, there was a need for low-dropout voltage

regulators capable of providing stable voltage under a wide range of current loads while also maintaining low quiescent power draw during low or no-current loads.

The Rincon-Mora Paper, for instance, is titled “A Low-Voltage, Low-Quiescent Current, Low Drop-Out Regulator” and describes that “[t]he demand for low-voltage, low drop-out (LDO) regulators is increasing because of the growing demand for portable electronics, i.e., cellular phones, pagers, laptops, etc.” Rincon-Mora Paper at Abstract. It further explains that “current efficiency is an important characteristic of battery powered products. It is defined as the ratio of the load-current to the total battery drain current, which is comprised of load current (I_{Load}) and the quiescent current (I_q) of the regulator.” *Id.* at 36-37. “For many applications,” it teaches, “high load-current is usually a temporary condition, whereas the opposite is true for low load-currents.” *Id.* at 37. As a result, the LDO taught in the Rincon-Mora Paper has a “load dependent boost current” that allows the regulator to service transient high-load requirements while maintaining low quiescent current.

Rincon-Mora '577 discusses a similar goal of minimizing power draw during no-load conditions: “An improved low-dropout (“LDO”) voltage regulator . . . provides improved transient response performance to the application of various load current step stimuli while requiring no standby or quiescent current during zero output load conditions.” Rincon-Mora '577 at Abstract. It further describes that “standby and quiescent current flow are major concerns in [LDO] design.” *Id.* at 1:24-26.

Hu also teaches the construction of an “ultra low quiescent, wide output current range low-dropout regulator[.]” Hu at Abstract. As with several of the other references, Hu discusses that “[e]xtremely low quiescent current power management circuits are highly desirable for battery-powered applications,” but that modern battery-powered devices “require their power

supply modules to source a much wider output current range to support the ever increasing functionality and processing power in the gadgets.” Hu at 386.

Xi, for instance, is directed to an “ultra-low quiescent current low dropout (LDO) voltage regulator with dynamic bias and bandwidth.” Xi at Title. It explains that “LDOs are often used in battery powered devices” where “in order to minimize current drain under light loads, it is common to have a ‘SLEEP’ mode for the regulator in which the maximum load current is limited to a few milliamps and the quiescent current is very low, approximately 10-20 microamps.” Xi at [0003]. In contrast, “[i]n the normal or ‘ON’ mode, the normal load current can be a few hundred milliamps which requires a regulator having a higher bias current, as much as 100 microamps.” *See also*, Xi at [0005] (“[i]t is a general object of the present invention to provide an LDO that switches automatically from SLEEP to ON modes.”)

Al-Shyoukh is similarly concerned with a voltage regulator that is able to respond to transient load increases while maintaining “low quiescent current at no-load conditions.” Al-Shyoukh at 1735; *See also* Al-Shyoukh at 1738 discussing “an undesirable increase in the quiescent current in the LDO under no-load condition.” Al-Shyoukh also explains that that “[d]ynamically-biased shunt feedback is proposed in the buffer to lower its output resistance.” Al Shyoukh at Abstract. This allows “[t]he maximum output-voltage variation [to] be minimized during load transients even if a small output capacitor is used.”

Yang likewise discusses that “[w]ith the increasing demand[] of portable devices, how to use [] battery energy efficiently is the most concern[ing] problem.” Yang at 428. “Therefore, [the] power management system is indispensable for modern consumer products.” *Id.* It goes on to explain that, in power managemenat systems, low-dropout linear regulators are “the most common block due to the characteristics such as simplicity, small board space, low noise, and

cost.” *Id.* The proposed solution is an LDO design in which “the minimum load can be reduced to about 50μA and transient response time can be reduced . . . to be smaller than 4μs.” *Id.*

Stanescu also addresses that “LDOs have emerged as front-line integrated circuits (ICs) in the last decade, being used in palmtop and laptop computers, portable phones, and other entertainment and business products” and that “[d]ue to the growing need to save power, all battery-operated electronic systems use or will probably use LDOs with low ground current.” Stanescu at 1:17-28. As part of the solution to this problem, the specification proposes an LDO that “has a quiescent current of about 50 μA (if the current consumption of the bandgap reference block **14** in FIG. 2 is included, the quiescent current is about 70 μA).” *Id.* at 7:64-8:3.

Xi ’221 likewise teaches that “[r]ecent trends associated with high efficiency battery powered equipment are creating increased demand for power management systems using DC/DC converters feeding low drop-out (LDO) voltage regulators.” Xi ’221 at 1:30-33. The solution taught in Xi is to provide a LDO with variable gain capable of addressing the needs of transient loads.

A POSA with the goal of designing an efficient low-dropout voltage regulator capable of meeting transient high current requirements while maintaining low quiescent draw would have considered each of these prior art references. A POSA would further have understood that the components claimed in the ’074 patent were highly modular and that, given their similar goals and approaches, the specific architectures taught in each reference could be combined together in such a way as to utilize the strengths of each design. A POSA would, for instance, have seen the benefit of the using a folded-cascode amplifier as described in Xi and Yang because those references teach that this allows for low gain and high bandwidth. She would also have expected this combination to be successful because folded-cascode amplifiers are a form of OpAmps,

which are routinely used in such situations. Similarly, a POSA would have seen the benefit of implementing a transient boost circuit of the type described in Rincon-Mora '577 and would have expected this combination to be successful because the specification of Rincon-Mora '577 expressly teaches that “a cost-efficient transient boost circuit 40 can be added to a conventional LDO voltage regulator in the form of a localized positive feedback loop to enhance transient capabilities.” Rincon-Mora '577 at 4:63-65.

A POSA would further have been motivated to combine the bias voltage disable functions taught in Lee, Wolbert, OPTIREG, or MIC59300 with the low-dropout voltage regulators taught in Xi, Al-Shyoukh, Rincon-Mora Paper, Rincon-Mora '577, Rincon-Mora Dissertation, or Hu because each of those references, like those discussed above, addresses the need to reduce quiescent power usage under low-load conditions. *See e.g.*, Lee at 1:7-10 (“The present invention relates to an integrated circuit voltage regulator and, more particularly, to a voltage regulator circuit for generating programmable output voltage and having a low power consumption feature.”); Wolford at 46 (discussing “battery stretching techniques”). Adding to the obviousness of combining these references, this approach of disabling bias current under low-load conditions was expressly addressed in the background of Rincon-Mora '577. *See*, Rincon-Mora '577 at 1:25-29 (“some LDO voltage regulators incorporate a separate enable terminal to switch the device into a standby mode of operation to minimize power consumption when the associated device is disabled.”). The implementation of this common feature in OPTIREG and MIC59300 would have demonstrated to a POSA how the feature could be easily implemented in a voltage regulator system, and further bolstered the POSA’s expectation that such a combination would work.

A POSA would also have been motivated to combine the voltage regulators taught in Xi, Al-Shyoukh, Rincon-Mora Paper, Rincon-Mora '577, Rincon-Mora Dissertation, Hu, Yang, and Xi '221 with the bias noise-reduction capacitors taught in MIC59300 and Kitchin. This type of system was exceedingly common at the time of the purported invention a POSA would have known that the solutions discussed in MIC59300 and Kitchin were well-adapted for use in the voltage regulators taught in the references discussed above. Kitchin, for instance, is a general reference guide not tied to any particular design and MIC59300's datasheet describes the use of noise-reducing capacitors as "good design practice." MIC59300 at 10. A POSA would therefore not only be motivated to implement this design choice, but would expect for that combination to be successful.

A POSA would further have been motivated to combine the teachings of Xi, Al-Shyoukh, Rincon-Mora Paper, Rincon-Mora '577, Hu, and Xi '221 because the authors and inventors of each of these references were employed by the same company, Texas Instruments, Inc., at the time of the publication of each reference.

3. Secondary Considerations of Obviousness

Aptiv is not aware of any evidence that would support any secondary consideration of non-obviousness. In particular, Aptiv is not aware of any evidence that (1) Microchip developed a product embodying the claimed subject matter of any Asserted Claim that has enjoyed commercial success because of the alleged invention; (2) any Asserted Claim is directed to any long-felt but unresolved need; (3) any Asserted Claim addresses any failure of others; (4) there is any teaching away from the claimed subject matter by the prior art; (5) the claimed subject matter of any Asserted Claim has been copied or acclaimed by others; or (6) experts would have been skeptical of the claimed approach or idea set forth in the Asserted Claims. Nor is Aptiv

aware of any evidence that there is a nexus between any such secondary consideration and any Asserted Claim. On the contrary, the contemporaneous independent development of the Accused Products suggests that the claimed invention was obvious and that the claimed apparatus of the '074 patent was the product only of ordinary engineering skill.

In response to Aptiv's Interrogatory No. 6, Microchip listed various secondary considerations that are allegedly met, but provides neither a narrative explanation nor factual support for why this is so. Aptiv reserves the right to amend these contentions with respect to secondary considerations in response to any clarification of or additional evidentiary support for Microchip's position on secondary considerations and/or their alleged nexus with the Asserted Claims.

C. 35 U.S.C. § 112

For the reasons set forth below, the Asserted Claims are invalid for failure to comply with the written description and enablement requirements of 35 U.S.C. § 112.

Pursuant to 35 U.S.C. § 112, ¶ 1, a patent specification “shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make, and use the same[.]” *Id.* The Federal Circuit has held that this language creates two closely related, yet separate requirements for a specification: (i) a written description of the invention (“written description”), and (ii) a written description of the manner and process of making and using the invention (“enablement”). *See Ariad Pharm., Inc. v. Eli Lilly Co.*, 598 F.3d 1336, 1344 (Fed. Cir. 2010) (en banc). Section 112 also mandates that terms used in a patent must be sufficiently “definite.” “[A] patent is invalid for indefiniteness if its claims, read in light of the specification delineating the patent, and the prosecution history, fail to inform,

with reasonable certainty, those skilled in the art about the scope of the invention.” *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 901 (2014).

1. Written Description

35 U.S.C. § 112(a) requires a patent specification to “contain a written description of the invention.” “A specification adequately describes an invention when it ‘reasonably conveys to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date.’” *Juno Therapeutics, Inc. v. Kite Pharma, Inc.*, 10 F.4th 1330, 1335 (Fed. Cir. 2021). “But the hallmark of written description is disclosure. Thus, ‘possession as shown in the disclosure’ is a more complete formulation.” *Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010). “[T]he test requires an objective inquiry into the four corners of the specification from the perspective of a person of ordinary skill in the art. Based on that inquiry, the specification must describe an invention understandable to that skilled artisan and show that the inventor actually invented the invention claimed.” *Id.*

- a. **“a control block configured, to turn on, when instructed, at least one of the one or more output transistor devices to charge the pad capacitance to reduce a maximum voltage developed in the system as a result of the ESD event” / “a control circuit configured to instruct the control block to activate at least a portion of the output buffer when an ESD event occurs, to charge the pad capacitance to reduce a maximum voltage developed in the system as a result of the ESD event” / “one or more pads, each pad comprising ... a respective physical pad having respective capacitance [and] a respective pad circuit comprising . . . respective control circuitry operable to: activate at least a portion of the respective output buffer in response to an ESD event to charge the respective pad capacitance to reduce a maximum voltage developed in the system as a result of the ESD event; and turn on the clamp device in response to the ESD event”**

Claims 1, 6, and 14 of the '665 patent (and their dependent claims 2-5, 7-13, and 15-18) are invalid under § 112 for lack of written description. Specifically, the specification does not describe a single pad with circuitry capable of activating a portion of the output buffers to charge the single pad's capacitance. In each instance where the specification discusses the reduction of voltage developed in a system as a result of an ESD event, it describes sharing the ESD voltage with adjacent pads and using the capacitance of the *neighboring* pad to absorb a portion of the ESD charge. *See e.g.:*

In one set of embodiments, a robust electrostatic discharge (ESD) structure for a variety of digital input/output (I/O) pads may be achieved. Output PMOS devices comprised in the output buffer of the pad and coupled between an I/O pad supply rail and the output pad may be enabled in response to an ESD event, to charge a pad capacitance (which, in some cases, may be approximately 3 pF) corresponding to the physical pad or pad cell, to spread out the energy generated by the ESD event, resulting in a lower peak voltage and therefore better ESD performance. ***By configuring all of the pads comprised within the system, (e.g. integrated circuit or part), to operate this way, the ESD energy may be shared by the respective pad capacitances corresponding to all the pads, thereby reducing the maximum voltage that may develop in the system as a result of the ESD event.***

'665 patent at 2:19-35.

By turning on the p-channel devices, while disabling n-channel devices—e.g. NMOS devices—that may also be comprised in the output buffer, and coupled to the PMOS device(s), the functional control block may operate to couple the high supply rail (i.e. the pad power rail) and its associated capacitance (*such as all the other pad cells*) to the pad affected by the ESD event, *thus charge sharing the ESD pulse*, thereby reducing the maximum voltage developed in the part comprising the pads.

'665 patent at 2:56-65.

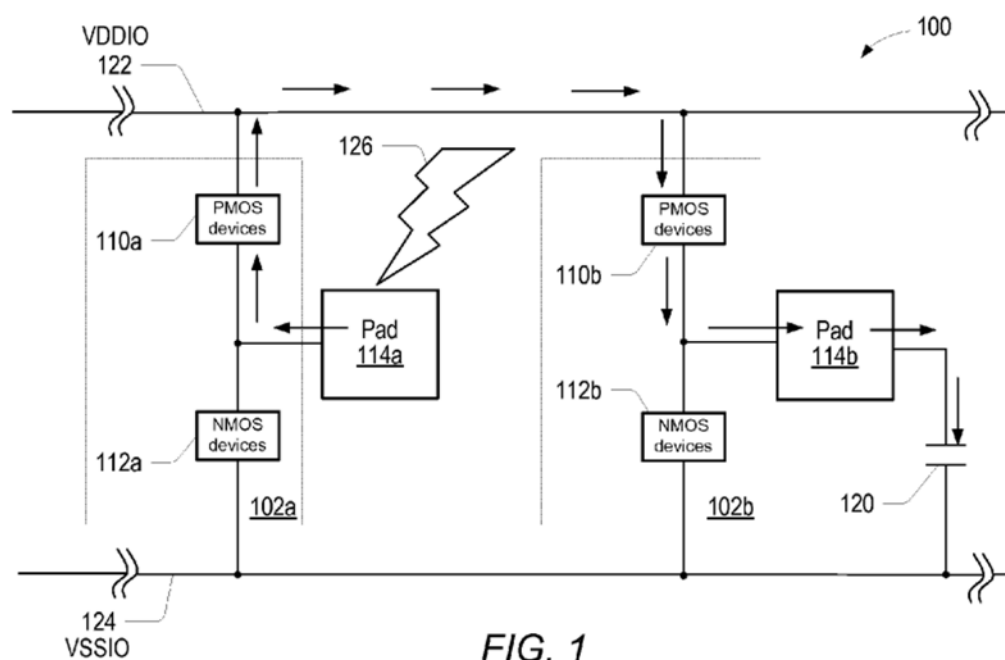


FIG. 1

'665 patent at Fig. 1.

Each pad may comprise a physical pad (114a and 114b) and a corresponding pad circuit (102 a and 102 b, respectively). Each physical pad may have an associated pad capacitance, shown in FIG. 1 only for pad 114 b, where capacitor 120 symbolizes the pad capacitance associated with pad 114 b. The pads may be coupled between an I/O supply/voltage pad rail (VDDIO) 122, which may be a variable I/O pad rail in some embodiments, and low supply/voltage (VSSIO) rail 124, where VSSIO rail 124 has a lower value than VDDIO rail 124. ***Pad circuit 102a may be configured such that in case of an ESD event 126 affecting pad 114a, pad circuit 102 a may turn on PMOS devices 110a in response to the energy of the ESD event, while keeping NMOS devices 112a and 112b turned off, resulting in charge flowing from pad 114 a to pad capacitance 120 through PMOS devices 110a and 110b. Although only two pads are shown in FIG. 1, any and all pads similarly configured between VDDIO rail 122 and***

VSSIO rail 124 may have their respective PMOS devices turned on (including pad circuit 102a), resulting in the charge being shared across all pads (pads 114a and 114b shown in FIG. 1), that is, across the respective pad capacitances associated with all the pads. This may effectively reduce the maximum, or peak, voltage developed in the circuit, or system, as a result of ESD event 126.

'665 patent at 3:65-4:21.

By enabling (i.e. turning on) PMOS device(s) 110, control block 202 ***effectively connects VDDIO rail 122 and its associated capacitance (which may comprise all the other pads or pad cells) to the physical pad affected by the ESD event, thereby sharing the charge generated by the ESD event,*** reducing the maximum voltage developed in the system as the result of the ESD event.

'665 patent at 5:29-35.

The specification does not describe any means by which a single pad may use its output buffer to charge its own pad capacitance to reduce the maximum voltage developed in the system as a result of an ESD event. Nor would a POSA reading the specification immediately envision such a system. The pad capacitance of the circuit that serves as the entry point for the ESD charge would already be fully saturated by the incoming ESD charge and activation of the control circuitry would not be able to charge the pad capacitance further. A POSA would therefore not understand the specification to describe “a control block configured, to turn on, when instructed, at least one of the one or more output transistor devices to charge the pad capacitance to reduce a maximum voltage developed in the system as a result of the ESD event,” “a control circuit configured to instruct the control block to activate at least a portion of the output buffer when an ESD event occurs, to charge the pad capacitance to reduce a maximum voltage developed in the system as a result of the ESD event,” or “one or more pads, each pad comprising ... a respective physical pad having respective capacitance [and] a respective pad circuit comprising . . . respective control circuitry operable to: activate at least a portion of the respective output buffer in response to an ESD event to charge the respective pad capacitance to reduce a maximum voltage developed in the system as a result of the ESD event; and turn on the

clamp device in response to the ESD event.” For these reasons, Claims 1, 6, and 14 of the ’665 patent (and their dependent claims 2-5, 7-13, and 15-18) are invalid for lack of written description.

b. “a gm enhanced current buffer driver”

Claim 1 of the ’074 patent (and its dependent claims 2-18) require “a gm enhanced current buffer driver.” What is actually disclosed in the specification, however, is not a current buffer at all, but rather a voltage buffer. The specification describes, for instance, that the current buffer driver has “low output impedance” which matches the requirements for providing a high frequency pole capable of sourcing current to a wide range of loads. Furthermore, the circuit diagram of the claimed current buffer provided in Figure 3B shows a voltage buffer, not a current buffer, as demonstrated by the high input impedance (connecting to the gate of transistor 384) and low output impedance. To the extent Microchip contends that the term “gm enhanced current buffer driver” should cover both a current buffer and a voltage buffer, the specification lacks adequate written description support.

c. “an operational amplifier”

Claim 1 of the ’074 patent (and its dependent claims 2-18) require “an operational amplifier.” What is actually disclosed in the specification, however, is not an operational amplifier (“OpAmp”), but rather an operational transconductance amplifier (“OTA”). This is clear from the circuit diagram of the alleged OpAmp shown in Figure 3A of the patent, which shows higher impedance at the output (connected to node C) than would be expected from an OpAmp.

2. Enablement

The requirement of enablement mandates that the disclosure in the specification describe “the manner and process of making and using [the invention], in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the [invention].” 35 U.S.C. § 112, ¶ 1. In determining whether undue experimentation is required to practice the claimed invention, a court may assess some or all of the so-called *Wands* factors, which include: (1) the quantity of experimentation necessary; (2) the amount of direction or guidance disclosed in the patent; (3) the presence or absence of working examples in the patent; (4) the nature of the invention; (5) the state of the prior art; (6) the relative skill of those in the art; (7) the predictability of the art; and (8) the breadth of the claims. *In re Wands*, 858 F.2d 731, 737 (Fed. Cir. 1988). “To be enabling, the specification must teach those skilled in the art how to make and use the *full scope* of the claimed invention without undue experimentation.” *MagSil Corp. v. Hitachi Glob. Storage Techs., Inc.*, 687 F.3d 1377, 1380 (Fed. Cir. 2012) (internal quotation marks omitted; emphasis added).

- a. **“a control block configured, to turn on, when instructed, at least one of the one or more output transistor devices to charge the pad capacitance to reduce a maximum voltage developed in the system as a result of the ESD event” / “a control circuit configured to instruct the control block to activate at least a portion of the output buffer when an ESD event occurs, to charge the pad capacitance to reduce a maximum voltage developed in the system as a result of the ESD event” / “one or more pads, each pad comprising ... a respective physical pad having respective capacitance [and] a respective pad circuit comprising . . . respective control circuitry operable to: activate at least a portion of the respective output buffer in response to an ESD event to charge the respective pad capacitance to reduce a maximum voltage developed in the system as a result of the ESD event; and turn on the clamp device in response to the ESD event”**

As discussed above, the specification of the '665 patent fails to describe any single pad capable of performing the claimed function of “charg[ing] the pad capacitance to reduce a maximum voltage developed in the system as a result of the ESD event” or “activat[ing] at least a portion of the respective output buffer in response to an ESD event to charge the respective pad capacitance to reduce a maximum voltage developed in the system as a result of the ESD event.”

Supra Section IV.C.1. For these same reasons, the disclosures in the '665 patent fail to enable a person of skill in the art to make or use the claimed invention. It would not be clear to a POSA how to manufacture or use a device capable of charging its own pad capacitance to reduce the maximum voltage developed by an ESD event. To the extent it is possible to design such a system, significant and undue experimentation would be required. Accordingly, claims 1, 6, and 14 of the '665 patent are invalid for lack of enablement. Dependent claims 2-5, 7-13, and 15-18 are likewise invalid for lack of enablement by virtue of the invalidity of the claim from which they depend.

3. Indefiniteness

35 U.S.C. § 112(b) requires patent claims to “particularly point[] out and distinctly claim[] the subject matter which the inventor or a joint inventor regards as the invention.” In other words, “claims are required to be cast in clear—as opposed to ambiguous, vague, indefinite—terms” because “[i]t is the claims that notify the public of what is within the protections of the patent, and what is not.” *In re Packard*, 751 F.3d 1307, 1313 (Fed. Cir. 2014). “[A] patent is invalid for indefiniteness if its claims, read in light of the specification delineating the patent, and the prosecution history, fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention.” *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 901 (2014).

a. “an enable/disable function to enable/disable the biasing circuit for reducing standby current”

Claim 1 of the ’074 patent (and its dependent claims 2-18) requires “an enable/disable function to enable/disable the biasing circuit for reducing standby current.” The term “function” is a nonce term, and because the claim term, viewed in light of the full claim language and specification, lacks sufficiently definite meaning to a person of skill in the art as the name for structure the term is subject to means-plus-function interpretation pursuant to 35 U.S.C. § 112 ¶ 6. The specification fails to describe any structure whatsoever for this function, much less any structure that would **enable** a biasing circuit in such a way as to reduce standby current. Because there is no structure described in the specification as corresponding to the function of “enabl[ing]/disable[ing] the biasing circuit for reducing standby current,” this term is indefinite.

b. “wherein the gm-boost circuit enables the current buffer driver to have large gm value”

This term appears in Claim 4 of the '074 patent. This claim is indefinite at least because the term “large gm value” is a term of degree, but the claims, read in light of the specification and the prosecution history, fail to provide objective boundaries for those in the art. As a result, a POSA would not be able to determine, with reasonable certainty, the scope of the claim. For this reason, claim 4 of the '074 patent is invalid.

c. “wherein the operational amplifier is a low gain and high bandwidth amplifier”

This term appears in claims 8, 9, and 10 of the '074 patent. These claims are indefinite at least because the term “low gain” is a term of degree, but the claims, read in light of the specification and the prosecution history, fails to provide objective boundaries for those in the art. This is particularly troublesome in this context as operational amplifiers (and operational transconductance amplifiers) are generally understood by those in the art to be high gain devices. This is particularly true of the cascode amplifiers specifically identified as a “low gain” operational amplifier in Claim 10. As a result, a POSA would not understand what is meant by the claims’ reference to a “low gain” operational amplifier, let alone be able to determine what specific range of gain falls within the scope of the claims. For this reason, claims 8-10 of the '074 patent are invalid.

V. ACCOMPANYING DOCUMENT PRODUCTION

Pursuant to the Scheduling Order, Aptiv is producing and/or providing for inspection, alongside its Initial Invalidity Contentions, the known invalidating references referred to herein and in the accompanying claim charts are production numbers APTIV_10005663 - APTIV_10006547.

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CERTIFICATE OF SERVICE

I, Philip A. Rover, hereby certify that on December 8, 2023, I served Aptiv Services US, LLC's Initial Invalidity Contentions by sending the document by electronic transmission to the email addresses listed below:

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