Analysis and Design of ESD Protection Circuits for High-Frequency/RF Applications

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Abstract

Electrostatic discharge (ESD) protection devices can have an adverse effect on the performance of high frequency and RF circuits. This work presents for the first time, an s-parameter based analysis of the performance of RF circuits with various ESD protection designs. Additionally, a design methodology for distributed ESD protection using coplanar waveguides is developed to achieve a better impedance match over a broad frequency range. By using this technique, an ESD device with a parasitic capacitance of 200 fF will attenuate the signal power by only 0.27 dB at 10 GHz.

1. Introduction

As the demand for wireless (RF) systems continues to increase rapidly, providing sufficient ESD protection for these systems poses a major design and reliability challenge. This is due to the fact that in applying ESD protection to RF systems, the protection system must be transparent--the protection circuit must not affect the signal under normal operating conditions [1, 2]. The on-chip protection circuit is placed between the signal pin and the core circuit, as shown in Figure 1. The protection circuit may be composed of various devices, such as diodes, transistors, or silicon controlled rectifiers (SCRs), but in all cases, these devices shunt ESD current coming from the signal pin to the power supply rails and away from the core circuit [3]. However, under normal operating conditions, these protection devices present capacitances and resistances to the signal path, and at sufficiently high frequencies, the capacitances look like short circuits to ground. Thus a poorly designed protection system can generate impedance mismatches, causing reflections of signals, corruption of signal integrity, and inefficient power transfer between the signal pin and the core circuit. Also, while the operation frequency continues to rise, the size of the protection circuits and their associated capacitances are not decreasing as rapidly, resulting in increasingly inefficient power transfer. The simple approach of minimizing capacitance while maintaining high protection levels is becoming increasingly infeasible as the operation frequency rises beyond a few GHz [4]; alternate protection schemes such as the distributed transmission-line ESD protection system may be necessary [5, 6]. Recent work has focused on comparison of ESD protection strategies for RF applications at 2 GHz [7]. However there is no published information that provides performance analysis of RF circuits with various ESD protection design options, particularly of the distributed protection scheme, which is attractive for operations in the multi-GHz regime. In this paper, we introduce a general methodology to quantify the impact of the parasitic capacitance and resistance associated with various ESD protection designs, including distributed protection circuits. Also, it is demonstrated that ESD protection with coplanar waveguides (CPW) can be employed to provide excellent RF performance for frequencies as high as 10 GHz.

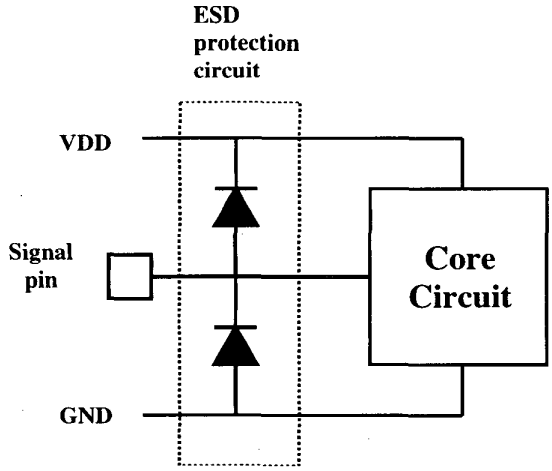

Figure 1. A simple ESD protection system example. The diodes shunt excess current applied to the signal pin towards VDD or GND to protect the core circuit.

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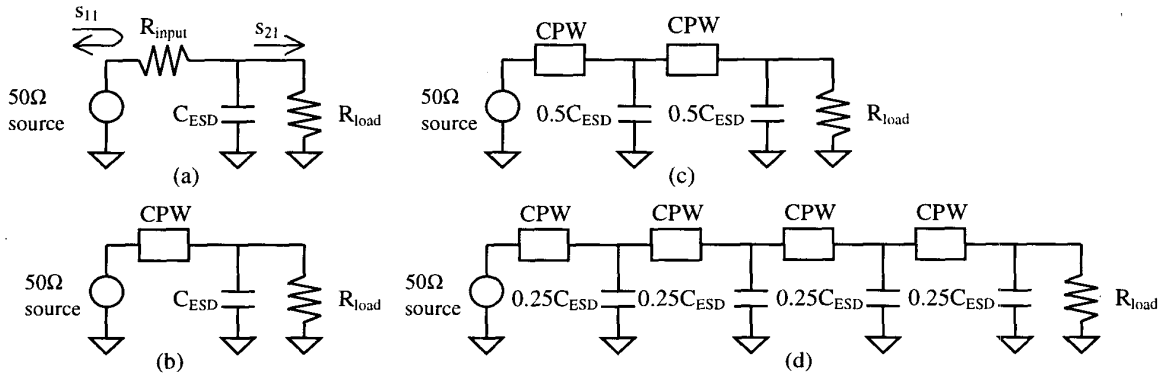

Figure 2. (a) Equivalent circuit with a general ESD protection device between the source and the load. (b) A length of CPW is added to the previous circuit, to improve impedance matching. (c) Two-section transmission line structure formed by CPW and the protection devices. (d) Four-section transmission line structure.

2. S-Parameter Performance Analysis

Starting with a standard 50 Ω system as is commonly found in RF systems, four different implementations of ESD protection is investigated, as shown in Figure 2. A 50 Ω signal source drives the input to the protection circuit, and the output of the protection circuit is connected to the system to be protected, as modeled by a 50 Ω load (R_{load}). In each circuit, the protection device is modeled as a capacitance and input resistance, and interconnects between the pin and ESD circuit or between distributed ESD elements are modeled by a resistance or a coplanar waveguide (CPW). Initially, the capacitance is assumed to be 200 fF, a value sufficient to provide a 2 kV ESD protection level [1]. Figure 2a, which represents the most general ESD protection, consists of the source, load, a resistor representing interconnect and device loss (R_{input}), and the protection device and pad parasitic capacitance (C_{ESD}). Figure 2b introduces a coplanar waveguide (CPW) between the source and the protection device to provide a better impedance match. The required CPW length was calculated using Smith Charts and impedance transformations to minimize reflections. This methodology is discussed in detail in Section 4. Figures 2c and 2d show series circuits with smaller sections for better broadband match as the circuit approaches an ideal transmission line made of infinitesimal sections. For the purpose of this study, transmission lines with a maximum of four sections were examined. Although more sections may yield better performance, any further gain would be marginal. Also, the added complexity of having more sections may be undesirable, and depending on the layout topology, it may be unreasonable to further divide the ESD device and pad capacitances into smaller elements. S-parameter simulations over the frequency range 0-10 GHz are performed on these circuits using the microwave circuit simulator ADS, to generate the reflection

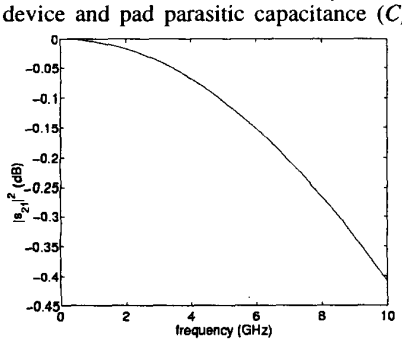

Figure 3. Plot of signal power loss vs. frequency for the circuit in Figure 2a, with a ESD device capacitance of 200 fF.

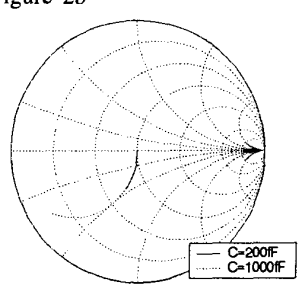

Figure 4. Smith Chart representation of the effect of C_{ESD} on s_{11} for Figure 2a, with zero series resistance (R_{input}=0).

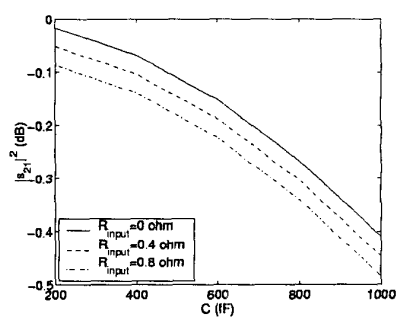

Figure 5. Performance vs. capacitance with varying R_{input}.

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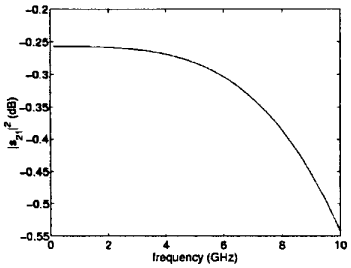

Figure 6. Plot of signal power loss vs. frequency for Figure 2b, with C_{ESD}=200 fF.

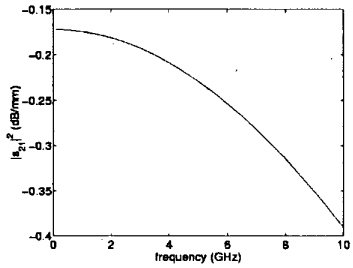

Figure 7. CPW loss per mm vs. frequency, showing the inherent loss found in the CPW due to resistive and dielectric loss.

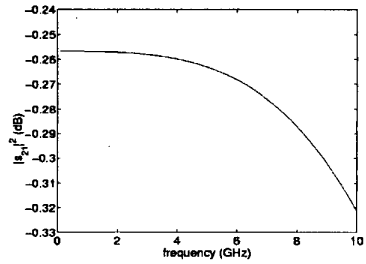

Figure 8. Plot of signal power loss vs. frequency for Figure 2c, with C_{ESD}=200 fF.

parameter s_{11}, and the transmission parameter s_{21}. As shown in Figure 2a, s_{11} corresponds to the amount of signal that is reflected at the input, and s_{21} corresponds to the amount of input signal that reaches the load. The objective of the system designer is to minimize s_{11} and maximize s_{21}. This study uses $|s_{11}|^2$ and $|s_{21}|^2$ as performance metrics since these coefficients are then directly proportional to power.

Next, the simulations are repeated for a set of capacitances, thus modeling different protection devices with different protection levels. The data from these simulations can be used to provide designers with insight into how much complexity is required in the protection system to obtain the desired ESD protection along with sufficient high-speed performance at the operating frequency of interest.

3. Results & Discussion

Figure 3 shows the results from the simulation of the simplest case from Figure 2a, with the input resistance set to zero and C_{ESD}=200 fF. Since the whole system is lossless, all the power loss is due to signal reflection caused by impedance mismatch. While most of the power reaches the load at low frequencies, the capacitance loads the circuit at higher frequencies. Using a larger protection device in the same circuit gives s_{11} like that in Figure 4. It can be observed that the magnitude of the reflection becomes large, thus little power is delivered to the load. Also, with increasing input resistance, the loss increases, as shown in Figure 5.

The effect of employing CPWs in the ESD protection is also examined. Figure 6 corresponds to the circuit in Figure 2b, where the CPW is added to provide some impedance match. In this case, the loss is due to the CPW loss and the mismatch loss. With a CPW length of 1.3 mm, there is a 0.25 dB loss even at low frequencies. As shown in Figure 7, this CPW has a loss of 0.18 dB/mm at low frequencies, with the loss becoming worse with increased frequency, to 0.39 dB/mm at 10 GHz. At higher frequencies, this CPW loss worsens, while the mismatch loss also becomes larger. Comparatively, this result is worse than that of Figure 3, but since Figure 3 shows an ideal case where there is no resistive loss at all, this is to be expected. Note that if the CPW was lossless,

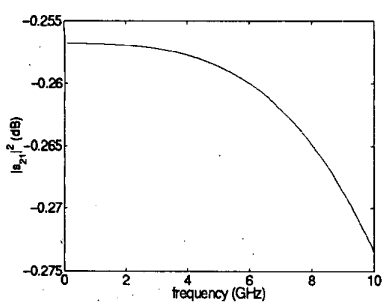

Figure 9. Plot of signal power loss vs. frequency for Figure 2d, with C_{ESD}=200 fF.

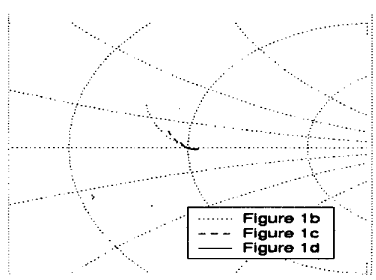

Figure 10. Smith Chart representation of s_{11} for Figures 2b, 2c, and 2d, over the frequency range 0-10 GHz, with C_{ESD}=200 fF.

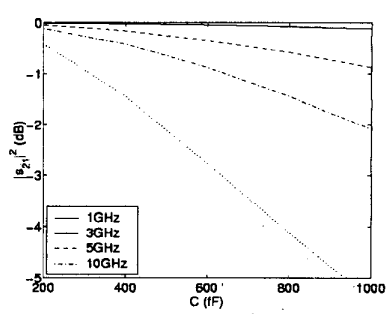

Figure 11. Signal power loss vs. parasitic capacitance, for a set of frequencies for the circuit in Figure 2a.

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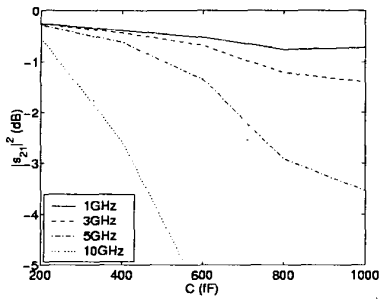

Figure 12. Performance vs. capacitance plot for the circuit in Figure 2b.

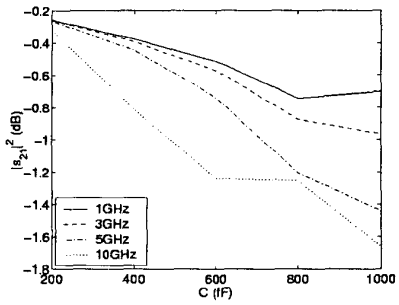

Figure 13. Performance vs. capacitance plot for the circuit in Figure 2c.

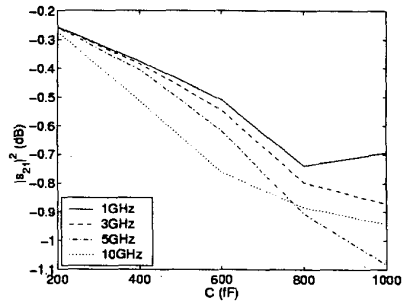

Figure 14. Performance vs. capacitance plot for the circuit in Figure 2d. Note that the variation of the loss over all measured frequencies and capacitances is only 0.85 dB.

the results with the CPW would be better than that of Figure 3.

Figures 8 and 9 show the results from simulating the circuit in Figures 2c and 2d, respectively. The losses observed are less than those seen in both Figures 3 and 6 at higher frequencies. At low frequencies, the CPW losses are again observed. Figure 9 shows loss characteristics that decrease by less than 0.02 dB between 0 and 10 GHz, with the maximum loss of 0.273 dB at 10 GHz, thus demonstrating good broadband characteristics.

Figure 10 shows the reflection parameter s_{11} corresponding to Figures 2b, 2c, and 2d. Note that the reflection observed becomes smaller with increased number of CPW sections.

The impact of the protection level is analyzed next by varying the size of the protection device (C_{ESD}). Figures 11-14 plot the power loss as represented by $|s_{21}|^2$ in the protection systems in Figure 2, against the parasitic capacitance posed by the protection devices. It is clear that higher frequencies and larger capacitances generate larger losses. The ideal case (R_{input}=0) in Figure 11 shows that at low frequencies, the loss is minimal irrespective of the device capacitance. The single CPW case of Figure 12 shows resistive loss in the CPW, resulting in poor performance at all frequencies. However, a more distributed protection system can minimize the loss for a wider frequency range, as shown in Figures 13 and 14. Also, Figure 14, which represents

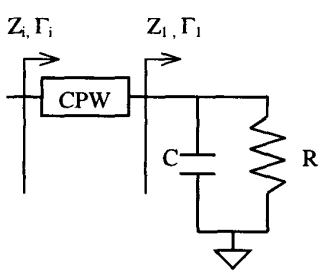

Figure 15. Circuit diagram for the example. *R*=50 Ω and f=10 GHz. The values of C and lengths of CPW vary. The impedances (Z) and reflection coefficients (Γ) are used to calculate the optimal C, CPW length, and number of distributed sections.

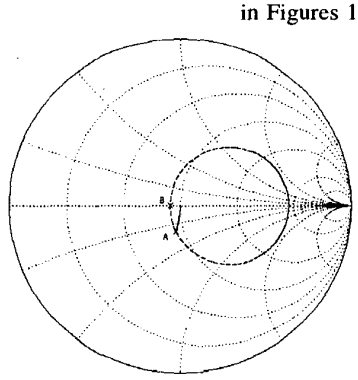

Figure 16. 50 Ω-normalized Smith Chart. Point A shows Γ_l for 200 fF at 10 GHz. Point B shows Γ_i. The dotted circle shows the locus for different lengths of CPW.

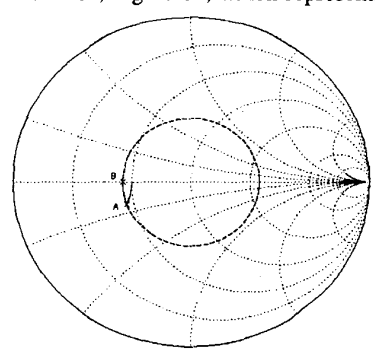

Figure 17. 100 Ω-normalized Smith Chart. Point A shows Γ_l for 200 fF at 10 GHz. Point B shows Γ_i. The dotted circle shows the locus for different lengths of CPW.

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Table 1. Summary of results from the example case. Note that with increased sections, Z_l and SWR approach 50 Ω and 1.00, respectively.

C (fF)	# sections	Z_l	Γ_l	ρ	ϕ	Length (rad)	Z_i	SWR
200	1	35.85-22.52j	-0.43-0.24j	0.494	-2.64	0.502	33.9	1.48
100	2	45.51-14.30j	-0.36-0.13j	0.385	-2.79	0.355	44.4	1.13
67	3	47.88-10.88j	-0.35-0.092j	0.358	-2.88	0.259	47.3	1.06
50	4	48.80-7.66j	-0.34-0.069j	0.348	-2.94	0.200	48.4	1.03
40	5	49.22-6.19j	-0.39-0.056j	0.343	-2.98	0.163	49.0	1.02

the four-segment distributed protection, shows that the loss will only vary by 0.85 dB for all capacitances, thus showing immunity to variations in ESD device depletion capacitance due to changes in DC bias levels.

The above results indeed show that dividing the ESD protection device into a few smaller sections provides better broadband RF performance. With that knowledge, the next section will demonstrate a methodology in designing distributed ESD protection systems.

4. Design Methodology for Distributed ESD Protection

Prior to determining the proper CPW length, three parameters must be fixed. They are the maximum operating frequency f_{max}, the equivalent ESD capacitance C_{ESD}, and the CPW characteristic impedance Z_{CPW}. Selecting f_{max} should consist only of determining the maximum frequency specification for the core circuit. C_{ESD} should be calculated after determining the proper ESD device size required for a particular protection level. The equivalent capacitance may then be calculated from the device junction areas, or obtained through simulations. The CPW characteristic impedance is mainly a function of transmission line width and signal-to-ground spacing. A high characteristic impedance is desirable, but losses should be kept to a minimum. For the following example, f_{max} was set at 10 GHz, C_{ESD} was chosen to be 200 fF for a 2 kV protection level [1], and Z_{CPW} was chosen to be 100 Ω, a high-impedance, low-loss line according to [8]. Along with calculating the CPW length, the number of distributed sections to be created is also determined. The equivalent circuit used to achieve this is shown in Figure 15. First, factors of the ESD capacitance are determined (in this case, 200 fF, 100 fF, 67 fF, 50 fF, 40 fF...) and are represented in the circuit as C. Then Z_l is determined for each capacitance at f_{max}, and R is the 50 Ω load resistance. These impedances correspond to points on arc A on the Smith Charts (Figures 16 & 17). From the impedance Z_l, the reflection coefficient Γ_l is calculated using the formula given by (1).

$$\Gamma_l = \frac{Z_l - Z_{CPW}}{Z_l + Z_{CPW}} \qquad (1)$$

Gamma, like s_{11}, represents the coordinate on the Smith Chart planes in Figures 16 & 17, with the center as the origin, and the outside circle being unity. Converting Γ_l into polar coordinates gives the magnitude ρ and phase ϕ. By adding some length of CPW, we attempt to bring the phase to 180 degrees (point B). For a CPW with characteristic impedance of Z_{CPW}, the locus that results from adding CPW to Z_l is a circle centered about the origin in Figure 17 (the dotted circle). Note that when this is viewed on a Smith Chart normalized to 50 Ω, the circle is not centered at the origin (Figure 16). Since a full circle around requires a CPW which is a half-wavelength ($\lambda/2$), the correct CPW length can be calculated from equation (2).

$$\text{CPW length} = \frac{(\phi - \pi)}{2\pi}\frac{\lambda}{2} \qquad (2)$$

Adding the correct CPW length should yield Γ_i with magnitude $\rho_i=\rho$ and ϕ_i=180 degrees. This can then be transformed into impedance with equation (3).

$$Z_i = \frac{(1+\Gamma_i)}{(1-\Gamma_i)} Z_{CPW} \qquad (3)$$

As a measure of how close Z_i comes to the system impedance (Z_o) of 50 Ω, the standing wave ratio (SWR) can be calculated, as shown in equation (4).

$$\text{SWR} = \frac{1 + \left|\frac{Z_i - Z_o}{Z_i + Z_o}\right|}{1 - \left|\frac{Z_i - Z_o}{Z_i + Z_o}\right|} \qquad (4)$$

A Z_i of 50 Ω results in an SWR of unity, and the closer the SWR is to unity, the better the match that is obtained. All the values calculated for this example are summarized in Table 1.

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Now given the ESD capacitance and the maximum allowable SWR, the number of sections required to achieve those specifications can be readily calculated using the methodolgy above. Note that this is valid because R=50 Ω, and we try to bring Z_i to 50 Ω for each section. Thus the next section to be added can regard Z_i of the present section as just a 50 Ω load.

One last consideration is to determine whether this analysis, performed for a system operating at f_{max}, is valid when the system operates at a frequency lower than f_{max}. It can be shown that at a lower frequency, the capacitance has a larger impedance, thus the arc on the Smith Chart becomes smaller, and ρ decreases, resulting in a smaller SWR. Thus the f_{max} case is the worst case, and if the performance there is satisfactory, then the performance at any lower frequency will be at least as good as that seen at f_{max}.

5. Conclusion

In conclusion, detailed s-parameter analysis of RF circuits with different ESD protection design options has been presented. The effect of the interconnect and device losses, together with the parasitic device capacitances on RF performance has been quantified. It has also been shown that a 4-stage distributed ESD protection can be beneficial at frequencies greater than 3 GHz. A generalized design methodology has been developed to optimize the number and length of coplanar waveguides separating the distributed ESD elements. By using this methodology, an ESD protection scheme with a parasitic capacitance of 200 fF will attenuate the signal power by only 0.27 dB at 10 GHz.

Acknowledgement

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