

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APTIV SERVICES US, LLC,
Petitioner,

v.

MICROCHIP TECHNOLOGY INC.,
Patent Owner.

Case No. IPR2024-00803
U.S. Patent No. 7,564,665

**DECLARATION OF DR. DANIEL FOTY IN SUPPORT
OF PATENT OWNER'S PRELIMINARY RESPONSE**

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I. INTRODUCTION

1. I have been retained by counsel for Microchip Technology Inc. (“Microchip” or “Patent Owner”) in the above-captioned matter as an independent consultant to offer opinions regarding the patentability of the claims in U.S. Patent No. 7,564,665 (“the ’665 patent” or “the challenged patent”).

2. In the preparation of this Declaration, I have confined my analysis to the materials and opinions that were available at the time of the preparation of this Declaration – supplemented with my own knowledge and experience in the field. Should new materials, analyses, or opinions be introduced subsequent to the filing of this Declaration, I reserve the right to provide supplementary Declarations to the extent necessary to address any such newly-introduced items.

II. QUALIFICATIONS

3. My qualifications are set forth in my *curriculum vitae*, included as EX2004, – which includes a listing of cases in which I have provided expert testimony. I have more than thirty years of experience as an engineer, scientist, and consultant in the electronics industry, including in the areas of integrated circuit (IC) design, layout, structure, and operation, in the design and analysis of transistor-based digital and analog circuits, in RF technology for wireless communications, in technology development, and in technical and business development.

4. My *curriculum vitae* contains further details regarding my experience, education, publications, and other qualifications which allow me to render expert opinions in connection with this proceeding.

III. COMPENSATION

5. I am being compensated for my work in this matter at an hourly rate of \$600 for consulting services. My compensation does not depend on the content of my opinions or the outcome of this investigation.

IV. MATERIALS CONSIDERED

6. In preparing this declaration, I reviewed and considered the following materials, along with any other materials referenced in the body of my declaration:

Exhibit	Description
EX1001	U.S. Patent No. 7,564,665 to Holly et al.
EX1002	Declaration of Dr. Mike Shuo-Wei Chen
EX1003	Prosecution History of U.S. Patent No. 7,564,665
EX1004	U.S. Pat. No. 6,529,359 to Verhaege et al.
EX1005	U.S. Pat. No. 6,249,410 to Ker et al.
EX1006	U.S. Pat. No. 7,589,945 to Miller et al.
EX1007	Microchip's Infringement Contentions — Redacted and Excerpted
EX1008	U.S. Patent No. 5,168,178 to Allen et al.
EX1009	U.S. Patent Publication No. 2007/0019345 to Loh et al.
EX1010	U.S. Patent Publication No. 2006/0001448 to Seo et al.

Exhibit	Description
EX1011	U.S. Patent No. 7,102,862 to Lien et al.
EX1012	Claim Construction Order (Dkt. No. 126), dated July 15, 2024 in <i>Microchip Technology Inc. v. Aptiv Services, LLC</i> , Case No. 1:23-cv-00778-JDW (D. Del.)
EX1013	Memorandum (Dkt. No. 125), dated July 12, 2024 in <i>Microchip Technology Inc. v. Aptiv Services, LLC</i> , Case No. 1:23-cv-00307-JDW (D. Del.)
EX2001	Aptiv's District Court Invalidity Contentions (December 8, 2023)
EX2002	C. Ito, K. Banerjee, and R. Dutton, "Analysis and Design of ESD Protection Circuits for High-Frequency/RF Applications," Proceedings of the International Symposium on Quality of Electronic Design, pp. 117-122 (2001)

7. I may use these documents and information, or other information obtained during the course of this proceeding, as well as representative charts, graphs, schematics and diagrams, animations, and models based on those documents and information, to support and to explain my testimony.

8. My opinions are based in part on a review and analysis of the above-mentioned documents and materials. I have also drawn on my education, experience, and knowledge of basic engineering and circuit design principles in forming my opinions.

V. UNDERSTANDING OF THE LAW

A. Legal Standards

9. I am not an attorney, but I have been informed of several legal principles, which I have employed in forming my opinions in this declaration. I have been informed that each patent claim is considered separately for purposes of patentability and that a dependent claim that depends from another claim includes all of the limitations of the claim it depends from.

1. Claim Construction

10. I have been informed that the claims of the challenged patents in this proceeding are to be construed using the same claim construction standard applied in district court. I have been informed the claim construction analysis begins with the ordinary meaning of a claim term, and there is a presumption that the term carries its plain and ordinary meaning to persons of ordinary skill in the art as of the effective filing date of the patent. I have also been informed that the most important sources for determining the meaning of a claim term are the claims, the specification, and the prosecution history of the patent at issue, which collectively is called “intrinsic evidence.” I have been further informed that the meaning of a claim term may also be guided by “extrinsic evidence,” such as contemporaneous dictionaries and treatises, as well as the testimony of technically-skilled witnesses such as myself.

2. Burden of Proof

11. I have been informed that the petitioner in an *inter partes* review bears the burden of establishing unpatentability by “a preponderance of the evidence.” I have been further informed and understand that, to prove an assertion by “a preponderance of the evidence,” the party with the burden of proof must demonstrate that it is more likely than not that the assertion is true.

3. Anticipation

12. I have been informed that a patent claim is unpatentable if it is “anticipated” by prior art. I have been informed that a reference anticipates a claim if the reference discloses each limitation of the claim at issue, either expressly or inherently. I have been informed that a prior art reference may anticipate a claim without disclosing a feature of the claimed invention if that missing characteristic is necessarily present, or inherent, in the single anticipating reference as would have been understood by one of ordinary skill in the art.

13. I have been informed that material not explicitly contained in a single prior art document may still be considered for purposes of anticipation if that material is incorporated by reference into the document.

4. Obviousness

14. I have been informed that a patent claim is unpatentable if it would have been obvious to a person of ordinary skill in the art (“POSITA”) at the time of the claimed invention. I have been further informed that a claimed invention is not

patentable if differences between it and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the pertinent art. I have been informed that factors relevant to the determination of obviousness include the scope and content of the prior art, the level of ordinary skill in the art at the time of the invention, differences between the claimed invention and the prior art, and “secondary considerations” or objective indicia of non-obviousness.

15. I have been informed that a single reference alone can render a patent claim obvious, if any differences between the reference and the claim would have been known or obvious to a POSITA at the time of the invention. That is, if the POSITA could have adapted the reference to meet the claims of the patent by applying known concepts to achieve expected results, then the patent claims are rendered obvious by that reference.

16. I have been informed that the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. I have been further informed and understand that when a patent claim simply arranges old elements with each performing the same function it had been known to perform, and yields no more than one of ordinary skill would expect from such an arrangement, the combination is obvious.

17. I have been informed that a patent claim composed of several limitations is not obvious merely because each limitation was independently known in the prior art. Hindsight reasoning is not an appropriate basis for combining references to form an obviousness combination. I have been further informed that it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine multiple prior art references, or multiple teachings of the same prior art reference.

18. I have been informed that various “secondary considerations” (sometimes referred to as objective indicia of non-obviousness) may support a determination of non-obviousness and that such secondary considerations must be considered as part of an obviousness analysis. I have been informed that even strong evidence of secondary considerations may not be sufficient to rebut a strong showing of obviousness. I have been informed that the patentee bears the burden of showing the existence and effect of secondary considerations of non-obviousness, after which the burden of coming forward with rebuttal evidence shifts to the party arguing obviousness. I have been informed that the following secondary considerations may indicate non-obviousness:

19. Copying: evidence that others, including the accused infringer, copied the patented invention.

20. Long-standing problem or need: evidence of a persistent problem or need in the art that was resolved by the patented invention.

21. Prior failure: evidence that others have tried and failed to solve the problem or failed to provide the need resolved by the claimed invention.

22. Commercial acquiescence of competitors: the willingness of industry to license the patent at issue.

23. Skepticism: evidence that those of ordinary skill in the art were skeptical as to the merits of the invention.

24. Praise: evidence of praise directed to an invention by others in the field.

25. Unexpected results: evidence that those of ordinary skill in the art were surprised by the capabilities of the claimed invention.

26. I have also been informed that the near-simultaneous invention by others can be evidence that a claimed invention is obvious. I have further been informed that the patentee bears the burden of showing a “nexus” between the claimed invention and the evidence proffered on secondary considerations (*e.g.*, proof of commercial success of a product that practices the claimed invention is not enough; there must be evidence that the commercial success resulted, at least in part, from the claimed invention).

B. Priority Date

27. I have been informed that a U.S. patent may claim “priority” to the filing date of one or more earlier filed applications. I have been informed that the priority date, also called the “effective filing date,” is the earliest filing date to which a claim is entitled – and that such date is relevant for determining what qualifies as prior art. I understand that a claim must have written description support in the application(s) to which it claims priority to be entitled to an earlier effective filing date. I have been informed that the priority date determination is done on a claim-by-claim basis, and that claims in the same patent may have different priority dates. I have been instructed to use January 10, 2007 as the priority date for all of the challenged claims in the challenged patent.

C. Level of Skill in the Art

28. I have been informed that the level of ordinary skill in the relevant art at the time of the invention is relevant to inquiries such as the meaning of claim terms, the meaning of disclosures found in the prior art, and the reasons one of ordinary skill in the art may have for combining references.

29. I have been informed that factors that may be considered in determining the level of ordinary skill include: (1) the type of problems encountered in the art; (2) prior art solutions to those problems; (3) rapidity with which innovations are made; (4) sophistication of the technology; and (5) education level of active workers

in the relevant field. I have been further informed that a POSITA is also a person of ordinary creativity.

30. The challenged patent pertains generally to the field of electrostatic discharge (ESD), and more particularly to the circuitry used to protect the (naturally-sensitive) circuitry of integrated circuits from being damaged or otherwise harmed by ESD events.

31. Thus, a person of ordinary skill in the art (“POSITA”) in the technology field of the ’665 patent at the time of the invention would have had a bachelor’s degree in electrical engineering or an equivalent technical degree and two years of experience in mixed-signal (*i.e.*, analog/digital) circuit design; further, a Master’s or Ph.D. degree in a relevant field may substitute for some work experience and vice versa.

32. I was at the time of the alleged invention at least a POSITA in the art relevant to the challenged patent. Further, based on my experience, I understand and know of the capabilities of a POSITA in 2007 – and I am familiar with how a POSITA would have understood and used the terminology found in the challenged patent at the time of its filing, and with the state of the art at that time.

33. From reviewing the Petition, it is my understanding that Petitioner is proposing a different standard for a POSITA – a standard requiring at least a Master’s degree in electrical engineering, computer engineering, or a related field

and three to five years of experience in integrated circuit design. Pet., 10. I disagree with this proposal, as it appears to be excessive; however, even were the Board to adopt this definition, I still qualify as a POSITA at the time of the invention.

34. Notably, Petitioner's expert has proposed a rather different POSITA standard – of “at least a Master's Degree in Electrical Engineering, or a Bachelor's Degree in Electrical Engineering plus two years of experience working on analog circuit design”; this proposed standard is actually relatively close to the standard that I have proposed above. I also qualify as a POSITA under this definition.

35. Regardless of which POSITA definition is used, my analysis and opinions that follow would not in any way be changed or affected.

VI. SUMMARY OF OPINIONS

36. The Petition asserts three Grounds of invalidity challenging Claims 1-18 of the '665 patent (the “Challenged Claims”); all three Grounds are obviousness challenges. I have been asked to evaluate if any of Petitioner's Grounds (and the references cited therein) establish obviousness. Based on my evaluation and analysis, it is my conclusion and opinion that, Petitioner has failed to meet its burden to show that any Challenged Claim is rendered obvious by any of Petitioner's three Grounds.

37. My substantive analysis in §XI provides examples of why Petitioner has failed to meet this burden in the Petition. I provide two reasons why each Ground fails, as summarized in the table below.

	Reason No. 1	Reason No. 2
Ground 1 (Verhaege)	No ESD charge sharing between I/O pads	Lacks “enable circuitry” (claim 1) and “control circuit[ry]” (claims 6 and 14) <i>in the correct I/O cell</i> to turn on the output PMOS transistor for charge sharing
Ground 2 (Verhaege + Miller)	Failure to show reasonable expectation of success	
Ground 3 (Ker)	No ESD charge sharing between I/O pads	

38. This Declaration is intended to support the Patent Owner’s Preliminary Response – and it not intended to be a comprehensive analysis of the Petition or the many shortcomings therein. Should the Board institute an *inter partes* review of the ’665 patent, I reserve the right to provide additional explanations, analysis, and reasons why the Petitioner’s three Grounds fail to establish obviousness.

VII. TECHNOLOGY BACKGROUND

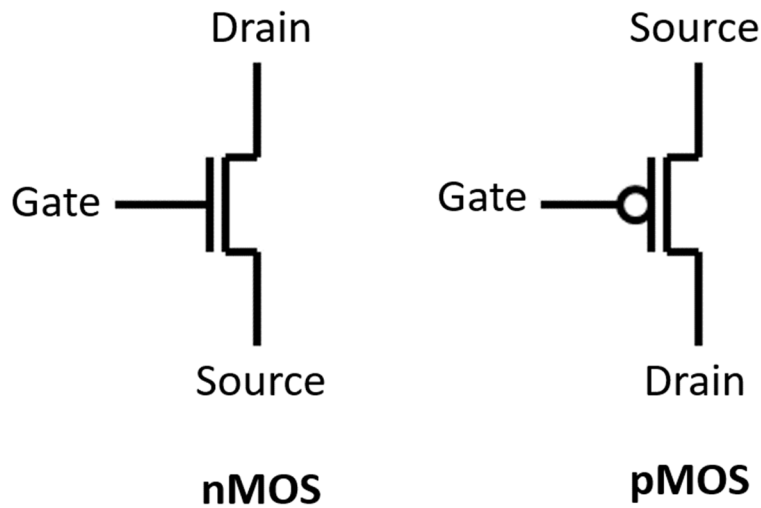
39. Before considering the ’665 patent in detail, some background on the technology of the ’665 patent should be considered. This involves both the basic notions of transistor-based circuits, and of ESD events and their mitigation.

A. Field-Effect Transistors

40. Ever since the invention of the first transistor in 1947, transistors have been used as fundamental building-blocks for the design of electronic circuits.

Although a variety of transistor types have appeared over the years, by 2007 the transistor space was overwhelmingly dominated by a type of transistor that is known as the “field-effect transistor” (for reasons that will be described below). The circuitry disclosed in the ’665 patent is based on the use of field-effect transistors as the fundamental building-blocks – with that particular type being known as the (extremely-ubiquitous) silicon-based metal-oxide-semiconductor field-effect transistor (MOSFET).

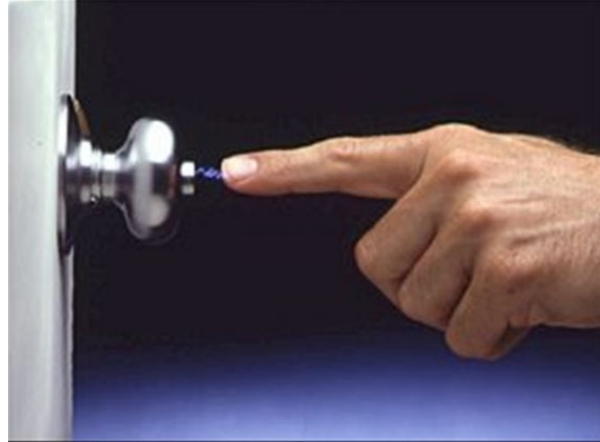
41. MOS transistors have four terminals: (1) gate; (2) source; (3) drain, and (4) substrate. Among other things, a MOS transistor is able act as a switch – that is, based on the voltage applied to the gate terminal, the transistor can be turned “on” (allowing current to flow between the source and drain) or “off” (preventing the flow of current). MOSFET transistors come in two flavors - typically referred to as “nMOS” (shown by the symbol below on the left) and “pMOS” (shown by the symbol below on the right). The substrate terminal is omitted in the symbols below.



The pMOS symbol in particular is notable for its inclusion of a small circle on the gate contact; this symbol is used in electronic circuitry (and logic circuitry) to indicate “NOT” – which is a way of denoting a pMOS transistor as behaving in the opposite (*i.e.*, “NOT”) way as behaves an nMOS transistor. It is a fundamental feature of MOS transistors that an nMOS transistor will turn on when a high voltage (that exceeds a certain threshold) is applied to the gate – and that a pMOS transistor will turn on when a low voltage (that is below a certain threshold) is applied to the gate. In this way, the nMOS and pMOS transistors can be complementary to each other.

B. Electrostatic Discharge (ESD)

42. Electrostatic Discharge (ESD) is a well-known and commonly-observed phenomenon in nature – covering a huge range of scale, such as lightning and the spark which occurs when one reaches for a metal doorknob.



In both cases, separate charge regions build up until the dielectric material (air) between them can no longer sustain the induced voltage – at which point the dielectric material breaks down, charge flows through the breakdown path, and the charge-separation-induced voltage difference between the two sides disappears. In the case of the “doorknob shock,” breakdown is induced by the decreasing distance between the hand and the doorknob – as the incoming hand decreases the distance between itself and the doorknob; as the distance decreases for the same amount of separated charge, the voltage difference between the hand and the doorknob will correspondingly increase. At some point, this voltage difference becomes large enough to induce dielectric breakdown – and a lightning-like spark will occur between the hand and the doorknob as the separated charge flows and the voltage difference is neutralized.

43. There are several notable phenomena associated with electrostatic discharge events of any size or scale, including the rapidity and intensity with which

they occur. Anyone who has observed a lightning strike knows that it is intense but very short-lived – while the more-prosaic doorknob shock lasts for a few tens of nanoseconds. In addition, the doorknob-shock event is further characterized by a very high transient voltage (*i.e.*, thousands or even tens of thousands of volts), as well as a very high transient current (*i.e.*, several amperes). Though short-lived, these events clearly pack a lot of energy punch into a small amount of time – making them potentially destructive to any sensitive electronics that might be on the receiving end of one of these events. Various solutions exist relating to shunting the energy of lightning strikes to ground – so that this energy is directed away from electrical equipment (such as a water pump) that might be damaged by a lightning strike.

44. Not surprisingly, ESD events can be very damaging to integrated circuits – which operate in the real world and are exposed to human touch and similar phenomena. In the particular case of silicon-based CMOS technology, the vulnerabilities can be particularly severe. For example (and as shown in the discussion of the prior subsection), input signals in integrated circuits are provided directly to the gates of the constituent MOS transistors. The gate of a MOS transistor functions as a capacitor with a very thin dielectric layer (such as silicon dioxide

(SiO₂)).¹ Like the doorknob example (where the dielectric (air) between the finger and doorknob breaks down due to an ESD event), the gate dielectric in a MOS transistor can also break down if subject to an ESD event. However, unlike the case of an air dielectric, dielectric breakdown of the MOS transistor gate dielectric will be catastrophic and irreparable; thus, an ESD event in a MOS transistor can destroy the transistor itself and render it permanently non-functional (or at least severely damaged).

45. Not surprisingly, various approaches have been devised in the semiconductor industry over the years to try and ameliorate ESD events – so that when an event occurs, the sensitive circuitry will be protected and remain undamaged. However, any ESD protection circuitry should also have little-or-no effect on the circuitry that it is protecting – so that the performance of the CMOS circuitry will not be reduced (*e.g.*, slowed down) by the presence and active operation of ESD protection circuitry.

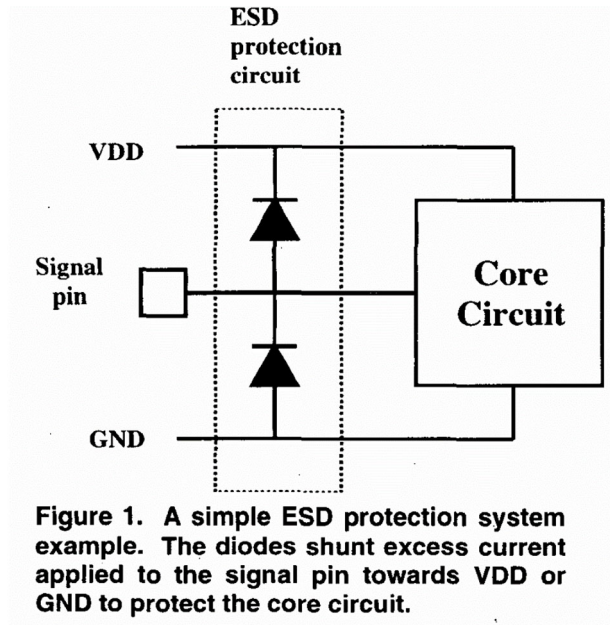
¹ The thickness of this dielectric has been continually decreased with the continued scaling-down of MOS transistor dimensions, a trend popularly known as “Moore’s Law.” With each successive technology generation, the MOSFET gate dielectric becomes thinner – and thus more susceptible to ESD damage.

46. The most-commonly-used generalized method of protection is for the ESD circuitry to shunt the transient ESD energy (*e.g.*, current) away from the protected circuitry – and, more specifically, to shunt that ESD event to one of the power supply rails:

The protection circuit may be composed of various devices, such as diodes, transistors, or silicon controlled rectifiers (SCRs), but in all cases, these devices shunt ESD current coming from the signal pin to the power supply rails and away from the core circuit.

EX2002, 1. The power supply rails provide a readily-available destination for the energy of an ESD event – as to first-order a power supply rail can be treated as being an infinite source or (more importantly here) infinite sink of charge.

47. A simple and commonly-known ESD protection addition to a circuit involves the use of two diodes, configured to cause the shunting described above to occur.



EX2002, 1. In the case of a positive-voltage ESD event striking the signal pin (*i.e.*, an I/O pad), the upper diode will turn on – and provide a shunt path diverting the energy of that event to the VDD power supply rail. Conversely, in the case of a negative-voltage ESD event striking the I/O pad, the lower diode will turn on – and provide a shunt path between the pad and the GND (or VSS) power supply rail. In this manner, the core circuit is protected from being damaged by an ESD event – and the ESD protection circuitry meets the requirement of having little-or-no effect on the operation of that core circuitry.

48. Thus, the general nature of the ESD art is clear. ESD protection is added to the circuitry connected to a particular I/O pad, the added ESD protection circuitry protects the circuitry directly associated with that particular I/O pad, and

the method-of-protection is to shunt the energy (*e.g.*, current) to one of the power supply rails (*viz.*, VDD or VSS/GND).

VIII. THE '665 PATENT

49. U.S. Patent No. 7,564,665 (“the ’665 patent” or “the challenged patent”) is entitled “Pad ESD Spreading Technique.” The listed inventors are P. Holly, D. Rodriguez, and D. Rice. There are various aspects that merit a short but well-organized review of the ’665 patent.

50. As its title indicates, the ’665 patent discloses circuitry which improves the state of the art of ESD protection in integrated circuits; further, that title (“Pad ESD Spreading Technique”) is actually quite descriptive of its teachings – with the “spreading” referring to, should an ESD event occur at a particular I/O pad, the sharing of the charge induced by this event with other I/O pads of the integrated circuit. This is explained clearly in the Abstract:

In case of an ESD event affecting one or more of the digital I/O pads, PMOS devices configured in an output buffer section between an I/O pad supply rail and the physical output pad—within their respective pad circuits in the affected digital I/O pads—may all be turned on in response to the ESD event. This may allow the capacitance of each pad, in some cases approximately 3 pF capacitance per pad, to charge up, absorbing the energy of the ESD event and reducing the peak voltage the integrated circuit or part experiences as a result of the ESD event.

EX1001, Abstract. As will be explained in slightly-more detailed below, the “spreading” (*i.e.*, sharing) of the charge with other I/O pads spreads the ESD-event-

induced charge out over what amounts to a larger capacitor – which, as described, serves to reduce the peak voltage of an ESD event when such an event occurs.

51. As described in the Technology Background section (at Section VII.B), in the particular case of silicon-based CMOS technology, the vulnerabilities associated with pad ESD events are particularly severe – as, for example, input signals in CMOS circuits are provided directly to the gates of the constituent MOS transistors of the CMOS circuits.

52. Thus, reducing the peak voltage of an ESD event will provide improved ESD protection to the sensitive transistors in the circuitry of an integrated circuit that has been fabricated in a scaled-down CMOS manufacturing process. In particular – and as will be described in more detail below – this teaching does not directly involve the shunting of the energy of an ESD event to, *e.g.*, a power supply rail; as detailed in Section VII.B, this shunting to a power rail is the conventional method of deflecting the possibly-damaging high energy of an ESD event away from the sensitive circuitry connected to the I/O pad – something that was known in the art at the time of the '665 patent.

53. This is actually explained in the specification of the '665 patent:

This method may be employed as an additional technique to be used in conjunction with other established solutions, such as various clamp devices and clamp circuits, for example, allowing improved ESD performance over the established solutions used alone.

EX1001, 2:35-39. Thus, the teachings of the '665 patent are not a *replacement* for the known techniques of mitigating the effects of an ESD event; rather, they are an *enhancement* to the use of those known methods – reducing the peak voltage of an ESD event (as described above) during the time between the occurrence of the ESD event and the completion of the shunting of the ESD event energy to, *e.g.*, a power rail.

54. The main embodiment of the teachings of the '665 patent is contained in Figure 1:

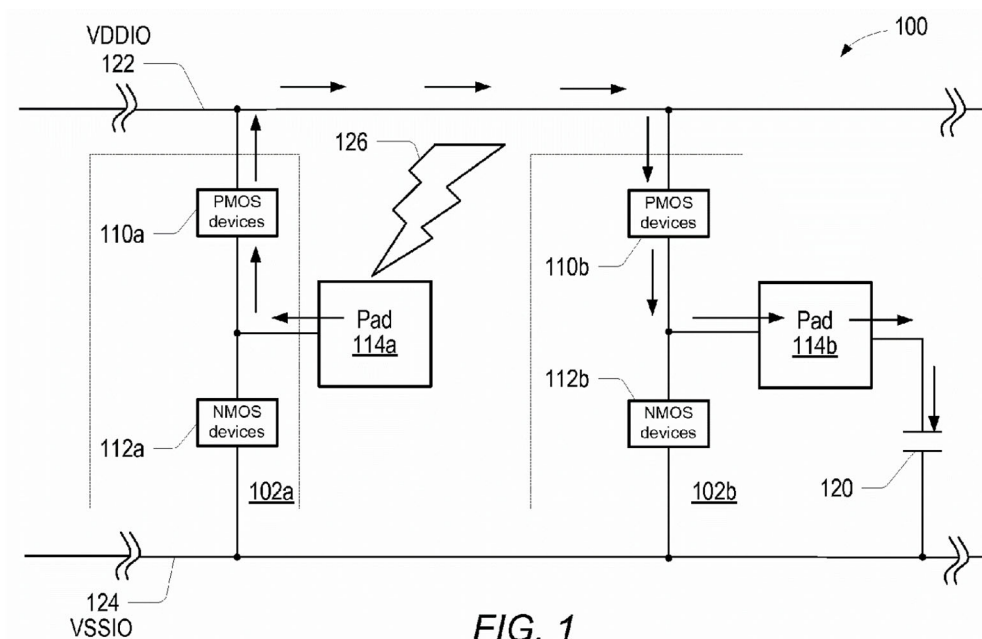


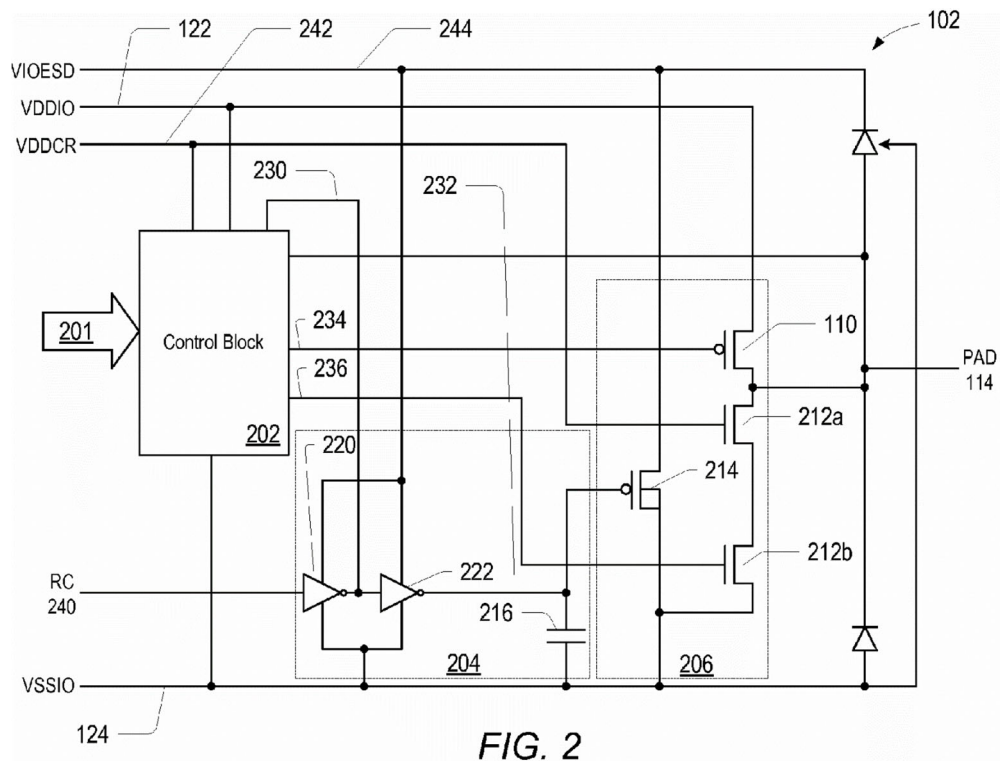
FIG. 1

What is happening here is well-described in the specification:

FIG. 1 shows the partial block diagram of pads comprised in a system 100, for example an integrated circuit, and configured to share a charge developed as a result of an electrostatic discharge (ESD) event, to reduce the maximum voltage developed in the system as a result of the ESD event. Each pad may comprise a physical pad (114a and 114b) and a corresponding pad circuit (102a and 102b, respectively). Each physical pad may have an associated pad capacitance, shown in FIG. 1 only for pad 114b, where capacitor 120 symbolizes the pad capacitance associated with pad 114b. The pads may be coupled between an I/O supply/voltage pad rail (VDDIO) 122, which may be a variable I/O pad rail in some embodiments, and low supply/voltage (VSSIO) rail 124, where VSSIO rail 124 has a lower value than VDDIO rail 124. Pad circuit 102a may be configured such that in case of an ESD event 126 affecting pad 114a, pad circuit 102a may turn on PMOS devices 110a in response to the energy of the ESD event, while keeping NMOS devices 112a and 112b turned off, resulting in charge flowing from pad 114a to pad capacitance 120 through PMOS devices 110a and 110b. Although only two pads are shown in FIG. 1, any and all pads similarly configured between VDDIO rail 122 and VSSIO rail 124 may have their respective PMOS devices turned on (including pad circuit 102a), resulting in the charge being shared across all pads (pads 114a and 114b shown in FIG. 1), that is, across the respective pad capacitances associated with all the pads. This may effectively reduce the maximum, or peak, voltage developed in the circuit, or system, as a result of ESD event 126.

EX1001, 3:61-4:21. This is a detailed description of the ESD charge spreading (*i.e.*, sharing) that was explained above.

55. The '665 patent also discloses an embodiment of pad circuitry that carries out the functions that were described above:



The operation of this circuitry is detailed in the specification at col. 4:22-6:12. Note that this circuitry includes the two-diode structure (shown on the righthand side of the figure) that is used (per the discussion in Section VII.B) for the shunting of the energy of an ESD event to a rail, with the rail that absorbs the event being effectively selected by the polarity of the ESD event.

56. In summary, the '665 patent (as mentioned above) is not a replacement for the conventional prior art techniques of shunting – but rather provides an enhancement to those techniques; these enhancements involve sharing of the charge induced by an ESD event (at a particular pad) with other pads – so that the spreading

out of the charge serves to reduce the peak voltage of the ESD event. Of particular note, given the continual thinning of transistor gate dielectric layers as the manufacturing technology is scaled to smaller dimensions (as discussed in Section VII.B), the vulnerability of transistors to ESD damage has concomitantly risen from process generation to process generation – meaning that the peak voltage level that will cause damage has similarly decreased with time; by reducing the peak voltage of an ESD event (while the time necessary to shunt the energy away elapses), the transistors are better-protected from ESD events – particularly for newer process technology generations.

IX. OVERVIEW OF THE CITED PRIOR ART REFERENCES

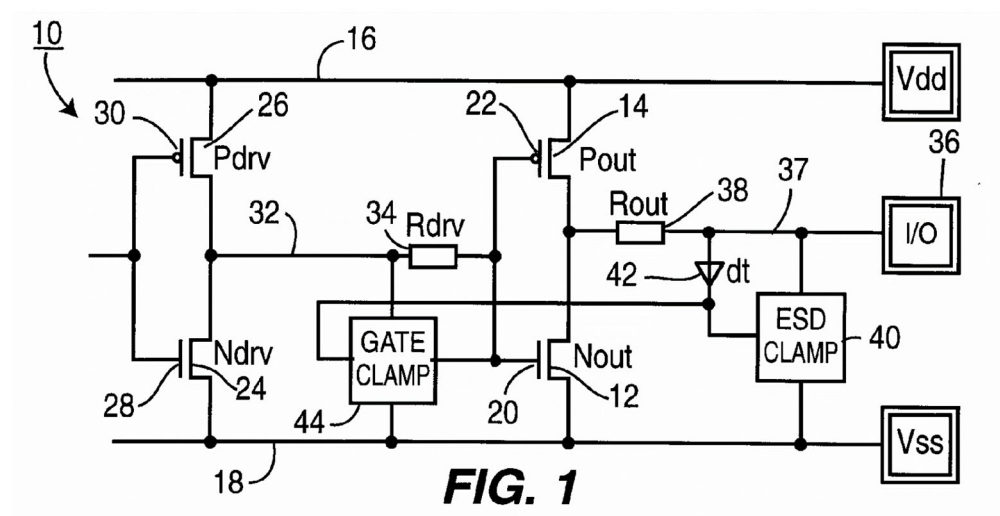
57. Petitioner has asserted three Grounds against all the claims of the '665 patent – which involve two primary references (and one secondary reference). These references will now be briefly considered here – along with some observations of what these references do *not* teach (with respect to the teachings of the '665 patent).

A. Verhaege

58. The Verhaege reference (“Verhaege”) is U.S. Patent No. 6,529,359, entitled “Circuits for Dynamic Turn Off of NMOS Output Drivers During EOS/ESD Stress.” The inventors are K. Verhaege and L. Avery.

59. Before going into the details of Verhaege, it should be noted here at the outset that Verhaege contains no teachings, disclosures, or even discussions involving charge sharing of ESD events to other I/O pads.

60. As the Abstract of Verhaege explains, Verhaege discloses “[a] circuit for the protection of an output driver NMOS transistor during EOS/ESD stress” – and “includes an output driver NMOS transistor and an output driver PMOS transistor connected in series between a Vss line and a Vdd line.” EX1004, Abstract. While Verhaege discloses several embodiments, all of them are variations on the same basic circuitry – so that the disclosures of Verhaege can be readily-understood by examining the main embodiment of Figure 1:



The functionality of this circuitry is explained in the specification of Verhaege:

In the circuit 10, the CMOS output driver circuit (the output driver NMOS transistor 12 and the output driver PMOS transistor 14) is driven by the pre-driver transistors 24 and 26. The dynamic trigger device 42 is used to trigger the ESD clamp 40. The output resistor 38 is a

decoupling resistor between the output drivers and the protection circuit (ESD clamp 40) and is optional in the circuit. The gate clamp 44 grounds the gate 20 of the output driver NMOS transistor 12 under transient over voltage stress conditions. In the circuit 10, the output driver NMOS transistor 12 is turned OFF during EOS/ESD stress, independent of the pre-driver state (high or low). As such, the ESD stress can be diverted to the parallel ESD clamp and the EOS/ESD capability is achieved. Although the clamp 40 is referred to as an ESD clamp, it will also serve as an EOS clamp.

Id., 2:26-40. When a positive-voltage ESD event strikes the I/O pad (36), this causes the “dynamic trigger” 42 to turn on – which activates the ESD clamp (40) and the gate clamp (44). The activated gate clamp pulls down the voltage on the gate (20) of the Nout transistor (12); this turns off the Nout transistor,² and prevents any of the ESD event energy from flowing through the Nout transistor (protecting it from being damaged during an ESD event, as was described in the Abstract of Verhaege). At the same time, the activated ESD clamp 40 serves to shunt the energy of the ESD event through itself and to the power supply rail VSS (18) – serving to evacuate the

² Because the Nout and Pout transistors are both controlled by a common gate signal, the act of turning off Nout should also turn on Pout. The fact that Pout may be turned on in this circumstance is purely incidental to the goal of protecting Nout from damage during an ESD event - and Verhaege provides no discussion of Pout being used to shunt ESD energy at all.

ESD event energy to a power supply rail, as described in the Technology Background section.

61. Thus, Verhaege discloses circuitry that, during a positive-voltage ESD event, will shunt the energy of that ESD event from the I/O pad to the Vss rail through the ESD clamp rather than through the Nout transistor – as a means of protecting the Nout transistor during an ESD event. Further, Verhaege discloses circuitry associated with – and operating entirely within – a single I/O pad and the circuitry to which that I/O pad is connected.

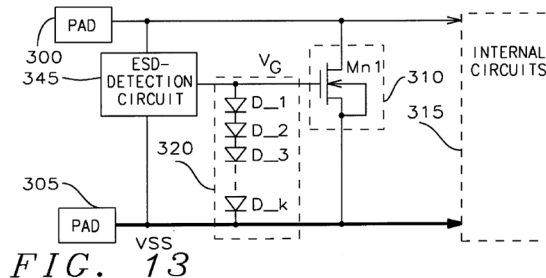
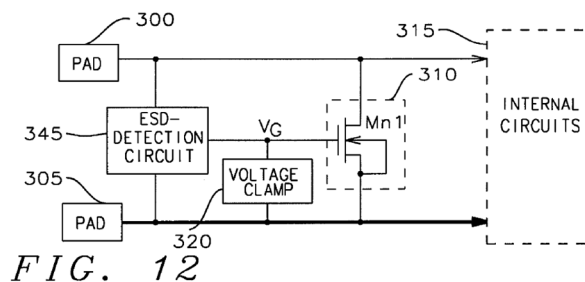
62. Notably, Verhaege includes no discussion of any shunting of ESD event energy to the Vdd rail (via the Pout transistor). Verhaege is also silent on what would happen should a negative-voltage ESD event strike the I/O pad – which is particularly notable, as the “dynamic trigger” would not be turned on by such an ESD event.

B. Ker

63. The Ker reference (“Ker”) is U.S. Patent No. 6,249,410, entitled “ESD Protection Circuit Without Overstress Gate-Driven Effect.” The inventors are M. Ker and H. Chang.

64. Before going into the details of Ker, it should be noted here at the outset that Ker contains no teachings, disclosures, or even discussions involving charge sharing of ESD events to other I/O pads.

65. Ker discloses a number of embodiments for an ESD protection circuit; however, Ker discloses these embodiments largely as building-blocks, which are assembled together to create more-complex embodiments. In addition, many of Ker’s embodiments first identify constituent components as “black boxes” – with possible implementation in actual circuitry disclosed in succeeding embodiments. An example of this can be seen by comparing Figs. 12 and 13, where the generic “voltage clamp” black box is replaced with a series of diodes.

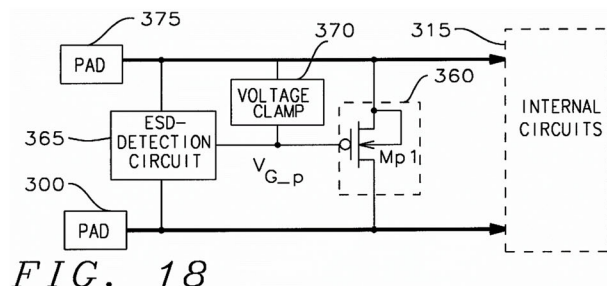
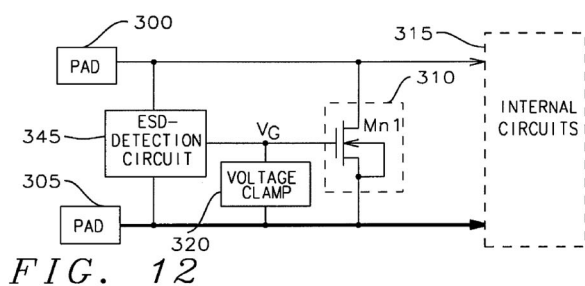


EX1005, Figs. 12-13.

66. Ker states that Fig. 11 is “a first embodiment of an ESD protection circuit,” and that Figs. 12-21 are “implementations” of that embodiment. EX1005, 10:66-11:3. With respect to Fig. 12 (and applicable to similar figures), Ker explains that pad 300 is an “input signal terminal to receive signals from external circuits” (*i.e.*, an I/O pad) and pad 305 is the associated “power supply terminal” (*viz.*, the Vss rail). *Id.*, 11:63-67.

67. In the event that a positive ESD strike takes place on signal pad 300, it is detected by ESD detection circuit 345; this activates nMOS transistor 310 to shunt

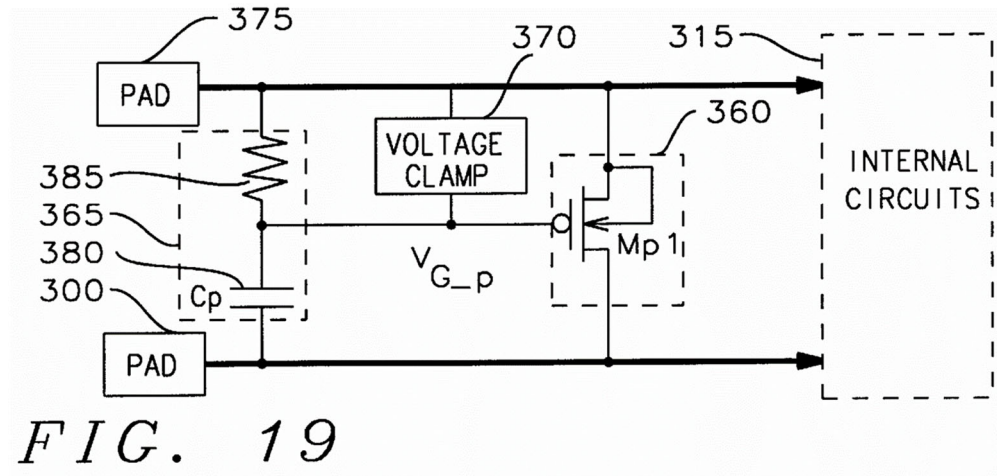
the ESD current to the Vss rail (as described in the Technology Background Section VII.B). EX1005, 12:1-6. Continuing with its building-block approach, Ker discloses an electrical mirror-image of Fig. 12 in Fig. 18 - where the shunting transistor is a pMOS device (Mp1) instead of an nMOS device, and pad 375 represents the Vdd rail (instead of the Vss rail 305). *Id.*, 13:7-15. In this sense, Figs. 12 and 18 are complementary to each other.



Id., Figs. 12 and 18.

68. Because (as discussed in Technology Background Section VII.A) the nMOS and pMOS transistors are activated by opposite polarity voltages on their respective gates, the overall operation of Fig. 18 is the inverse of that of Fig. 12. If a negative polarity ESD event occurs on signal pad 300, the ESD detection circuit 365 activates the “ESD protection PMOS transistor Mp1 360,” and the energy of the ESD event is shunted through Mp1 to the Vdd rail. EX1005, 13:15. A negative polarity ESD event is required in this implementation because transistor 360 is a pMOS device.

69. Ker Fig. 19 “illustrates an implementation of the ESD detection circuit 365,” shown in Fig. 18. EX1005, 13:29-30. The detection circuit comprises resistor (385) and capacitor (380). *Id.*, 13:30-36.



Id., Fig. 19.

70. Ker then combines the Fig. 12 and Fig. 18 electrical-mirror-image embodiments together into the combined dual-form embodiment that is shown in Figure 23. Further, Figure 29 shows this combined circuit with the ESD detector of Fig. 19 explicitly included.

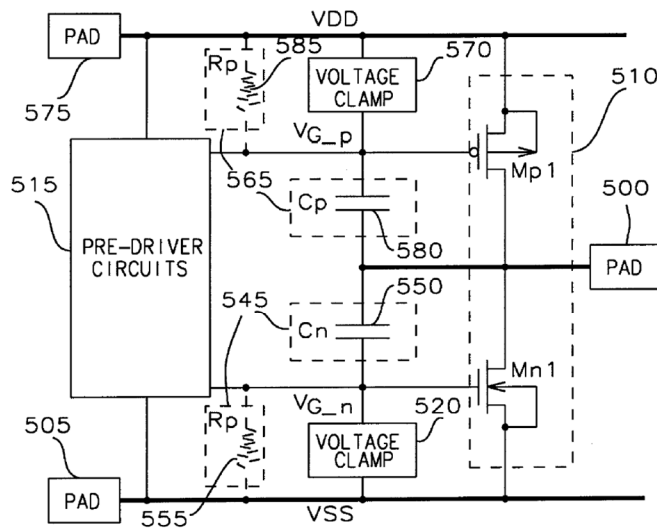


FIG. 29

EX1005, Fig. 29; *see also id.*, 19:37-42 (“An implementation of the first ESD detection circuit 545 and the second ESD detection circuit 565 are shown in FIG. 29. The first capacitor Cn 550 and the optional first resistor Rn 555 form the first ESD detection circuit 545. The second capacitor Cp 580 and the optional second resistor Rp 585 form the second ESD detection circuit 565.”); *see generally id.*, 17:64-19:57.

71. Ker explains how this circuit operates in response to both positive- and negative-polarity ESD events on I/O pad 500. EX1005, 19:37-58. If a positive-voltage ESD event strikes the signal pad 500, the transient voltage of the ESD event signal induces a transient voltage across the detection-circuit capacitor 550 – which serves to pull the voltage on the gate of transistor Mn1 high. When this occurs, the energy of the ESD event is shunted through transistor Mn1 (which, as Ker makes

clear, is specifically-designed to be able to handle this task (*see, e.g., id.*, 15:35-37)) to the power supply rail VSS (and away from the circuits to be protected). Further, as this is a positive-voltage ESD event at the signal pad 500, the same transient voltage will be induced across detection-circuit capacitor 580 – which also serves to pull the voltage on the gate of transistor Mp1 high; this turns (or keeps) transistor Mp1 off.

72. In contrast, if a negative-voltage ESD event strikes the signal pad 500, the transient voltage of the ESD event signal induces a transient voltage across the detection-circuit capacitor 580 – which serves to pull the voltage on the gate of transistor Mp1 low and turn it on. When this occurs, the energy of the ESD event is shunted through transistor Mp1 (which, as Ker makes clear, is specifically-designed to be able to handle this task (*see, e.g., EX1005*, 15:55-57)) to the power supply rail VDD (and away from the circuits to be protected). Further, as this is a negative-voltage ESD event at the signal pad 500, the same transient voltage will be induced across detection-circuit capacitor 550 – which also serves to pull the voltage on the gate of transistor Mn1 low; this turns (or keeps) transistor Mn1 off.

73. Like Verhaege, Ker teaches circuitry that serves to evacuate the energy of an ESD event to a power supply rail, as described in the Technology Background section (in Section VII.B); thus, like Verhaege, Ker discloses circuitry that will shunt the energy of an ESD event from the I/O pad to a power supply rail – as a means of

protecting the sensitive circuitry that the ESD-protection circuitry is designed to protect. Further like Verhaege, Ker discloses circuitry associated with – and operating entirely within – a single I/O cell.

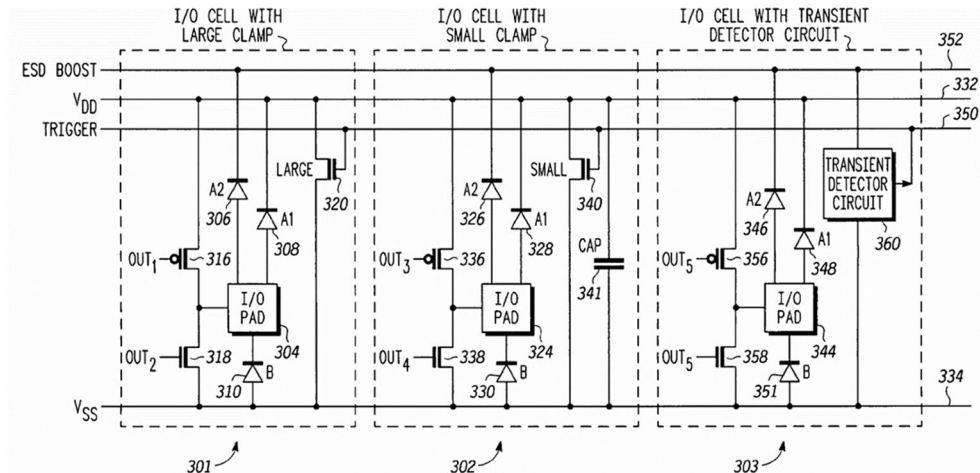
74. However, unlike Verhaege, Ker teaches circuitry that is designed to cope with both positive-voltage ESD events and negative-voltage ESD events – as described, *e.g.*, in the discussion above of the Figure 29 embodiment of Ker.

75. Ker also differs from the general prior art cited in Section VII.B – as that general prior art (using two simple diodes) shunts the energy of a positive-polarity ESD event to the V_{dd} rail, and the energy of a negative-polarity ESD event to the V_{ss} rail. In contrast, in Ker’s Figure 29 embodiment, the energy of a positive-polarity ESD event is shunted to the V_{ss} rail, while the energy of a negative-polarity ESD event to the V_{dd} rail.

C. Miller

76. The Miller reference (“Miller”) is U.S. Patent No. 7,589,945, entitled “Distributed Electrostatic Discharge Protection Circuit with Varying Clamp Size.” The inventors are J. Miller, M. Etherton, M. Khazhinsky, and M. Stockinger.

77. Petitioner does not use Miller as a primary reference, but relies on Miller Fig. 3 to modify the Verhaege circuit of Ground 1 in Ground 2. Miller Figure 3 is shown below; the basic operation of this circuitry will be explained in sequence.

**FIG. 3**

EX1006, Fig. 3.

78. In Figure 3, Miller depicts three I/O cells that are connected together. If there is an ESD event at one of the I/O pads, the circuit operation which follows will be the same, regardless of which I/O pad has received the ESD event.

79. So, in what follows, consider what happens when there is an ESD event at the I/O pad of the leftmost cell. If a negative-polarity ESD event strikes I/O pad 304, the conventional shunting of the energy from this event (as described in Section VII.B) is carried out – that is, the energy is simply shunted between the I/O pad and the Vss rail.

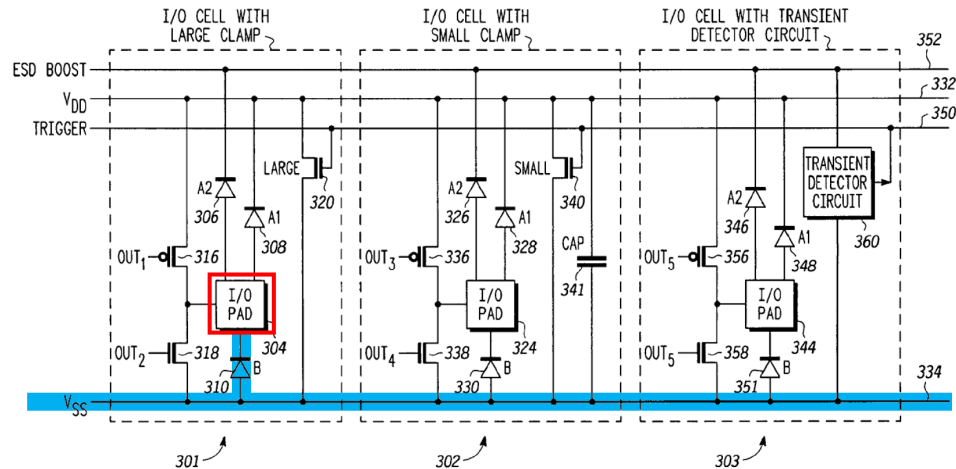


FIG. 3

EX1006, (annotations added).

80. However, if a positive-polarity ESD event strikes I/O pad 304, something rather more complicated happens. In the first step, the energy from this event is shunted out through two diodes – diode 308 shunts the part of the energy of the event to the Vdd rail (which is the conventional practice, as described in Section VII.B), while diode 306 shunts part of the energy of the ESD event to the line labeled “ESD Boost.”

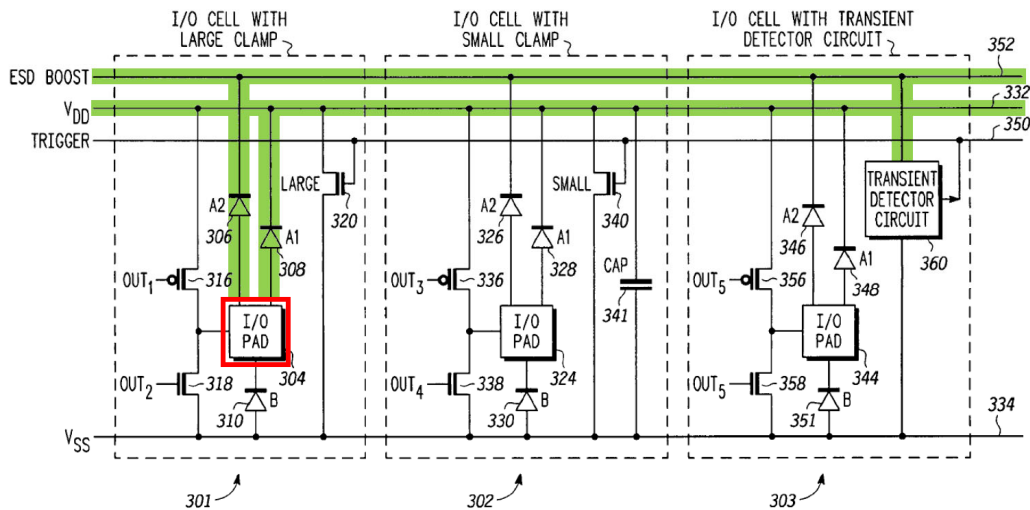


FIG. 3

The energy on the “ESD Boost” is detected by the “Transient Detector Circuit” (360) – which then sends a signal out over the line labeled “Trigger.” The signal on “Trigger” then turns on the transistors 320 and 340 – which serves to reroute the energy of the ESD event from the Vdd rail to the Vss rail.

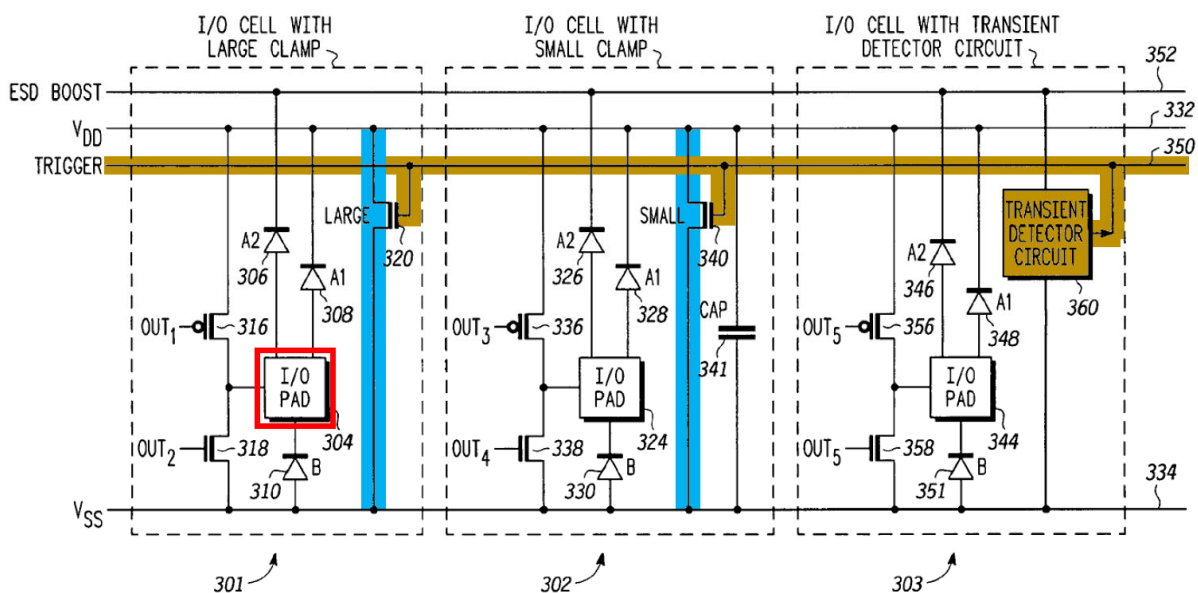


FIG. 3

81. Thus, Miller teaches *a single transient detector circuit* to route ESD energy to the Vss rail. Notably, charge from an ESD event is never directed to any other I/O pad; only the I/O pad which receives the ESD event is involved – with the energy of all ESD events eventually being routed to the Vss rail.

X. CLAIM TERMS

82. In general (and as is usual practice), I have given the terms in the challenged claims their plain and ordinary meanings, as would have been understood by a person of ordinary skill in the art at the time of the alleged invention, taking into consideration the language of the claims, the specification, and the prosecution history of the '665 patent. I have applied these understandings of the claim terms in my analysis and in forming my opinions where appropriate in this Declaration.

83. I have been informed that the district court construed two terms of the '665 patent as follows. I was instructed to use these constructions in my analysis and did so; however, these two terms are largely irrelevant to my analysis, conclusions, and opinions in this Declaration.

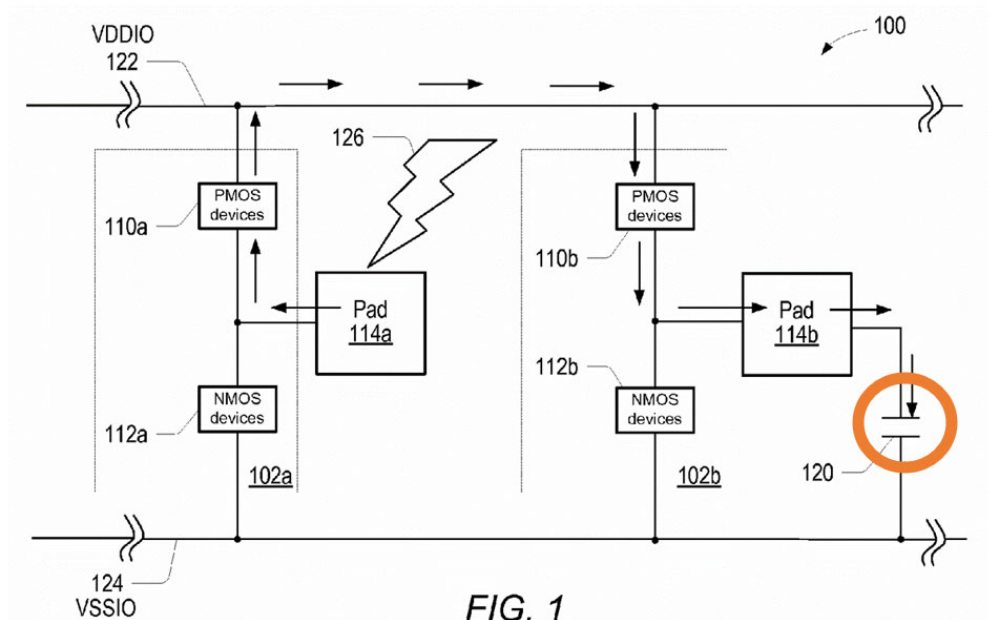
Term	District Court Construction
“second voltage rail” (claim 1)	“a second voltage rail that is distinct from the third voltage rail but may or may not be distinct from the first voltage rail”
“to charge the [respective] pad capacitance” (all claims)	“to charge the pad capacitance of said physical pad having [respective] capacitance”

EX1012, 1-2.

84. I was asked to render my opinion on two aspects of the Challenged Claims – as discussed below; I have been informed that one of these is not in dispute (ESD charge sharing between pads), while the other is disputed (“enable circuitry” and “control circuit[ry]”). However, my analysis and conclusions are the same regardless of whether or not there is any dispute between the parties.

A. ESD Charge Sharing Between Pads

85. It is my understanding that the parties are in agreement that the claims of the '665 patent (particularly, independent claims 1, 6, and 14) require that the charge of an ESD event on one particular I/O pad be spread to (*i.e.*, shared with/among) one (or more) other I/O pads. I agree. This is actually made quite clear in Figure 1 of the '665 patent:



EX1001, Fig.2 (annotation added.) As can be clearly seen, when an ESD event occurs at pad 114a, circuitry is activated (as per the three claim excerpts cited in paragraph 90) that allows the charge induced by that ESD event (at pad 114a) to be spread (*i.e.*, shared) with other pads (such as the depicted pad 114b); the “pad capacitance” which is being charged is *not* the pad where the ESD event has occurred. In particular, the capacitance associated with pad 114b (which is labeled as 120 in Figure 1) provides the “extra” capacitance that is (temporarily) invoked to spread out the charge induced by the ESD event – which serves to thusly reduce the peak voltage associated with the ESD event (during the time between which the ESD event occurs and the energy associated with the event has been shunted to *e.g.* a rail).

86. This circuit functionality is straightforward and easy to understand. There is no circumstance under which the pad capacitance being charged is

associated with the same pad at which the ESD event has occurred; this simply makes no logical sense – as not only is the affected pad already charged up by the ESD event (and thus of no use in spreading out the event-induced charge), but only other pads can provide the functionality described in the claims.

87. This concept is reflected in the claim language itself – as Claims 1, 6, and 14 all contain language that makes this very clear. Claim 1 and 6 contain the phrase “to charge the pad capacitance to reduce a maximum voltage developed in the system as a result of the ESD event,” while Claim 14 contains the nearly-identical phrase “to charge the respective pad capacitance to reduce a maximum voltage developed in the system as a result of the ESD event.” These phrases differ only by the addition of the word “respective” to the Claim 14 language. In all cases, the only way for the “pad capacitance” to reduce the maximum voltage of an ESD event would be for that same amount of charge to be spread out over “more” capacitance (*i.e.*, over a capacitor with a larger capacitance than that of a single pad); this is clear from the simple, well-known relationship between charge and voltage in a simple capacitor:

$$Q = CV,$$

where Q is the amount of charge on the capacitor, C is the capacitance of the capacitor, and V is the voltage across the capacitor. If the amount of charge Q is constant (as it would be for an ESD event), then the only way for the voltage V to be

reduced would be for the capacitance C to be increased. And the only way to increase the capacitance would be for additional in-parallel capacitors to be added to the capacitor of the ESD-affected pad.

88. This simple analysis confirms that an ESD event on one pad must be shared with one-or-more other pads, if the claim language is to be met.

B. The Location of the “Enable Circuitry” (Claim 1) and “Control Circuit[ry]” (Claims 6 and 14)”

89. I was asked to opine on how a POSITA would understand the Challenged Claims vis-à-vis the relative location of where the claimed “enable circuitry” (in claim 1) and the claimed “control circuit[ry]” (in claims 6 and 14). The answer is clear: the claimed circuitry is located in the same I/O cell (or circuit) where all of the other components/elements of the claim reside. In particular, as explained in the section above, the claimed “pad” being charged (*i.e.*, the pad with which ESD charge is being shared) is necessarily a *different* I/O pad than the one where the ESD event occurred. It follows that the other claimed elements (including the “output [buffer/transistor],” “clamp,” “control block,” “enable circuitry,” “control circuit[ry],” etc.) connected thereto are part of the same I/O cell, just as recited in the claims and described throughout the specification.

90. Claim 1 is directed to a “pad circuit” that includes:

enable circuitry configured to turn on the clamp device and instruct the control block to turn on the at least one of the one or more output transistor devices, in response to the ESD event;

EX1001, 6:46-49.

Claim 6 is directed to a “circuit” that includes:

a control circuit configured to instruct the control block to activate at least a portion of the output buffer when an ESD event occurs, to charge the pad capacitance to reduce a maximum voltage developed in the system as a result of the ESD event, wherein the control circuit is further configured to turn on the clamp device in response to the ESD event;

Id., 7:15-19.

And claim 14 requires a “pad” that includes:

“respective control circuitry operable to: activate at least a portion of the respective output buffer in response to an ESD event to charge the respective pad capacitance to reduce a maximum voltage developed in the system as a result of the ESD event”

Id., 8:26-31.

91. All of this claimed circuitry is part of the same “pad circuit” (claim 1), “circuit” (claim 6), or “pad circuit” (claim 14). And, in the context of the ’665 patent, this is plainly the I/O cell that serves to reduce the peak voltage from an ESD event occurring on another I/O pad (via charge spreading).

92. An interpretation that the enable/control circuitry is located in the same I/O cell where the ESD event occurs simply does not make sense. Basically, reading the claims in such a manner—*i.e.*, merely turning on the pMOS devices of the ESD-affected I/O cell to shunt current to the Vdd supply rail—amounts to nothing more than the conventional ESD shunting approach which was discussed in Technology Background, Section VII.B.

93. In other words, if the control/enable circuitry were in the ESD-affected I/O cell, it would turn on only the pMOS devices associated with that cell (*e.g.*, 114a). In that case, the energy of the ESD event would simply be shunted to the Vdd rail (with ***no*** spreading/sharing of charge with other I/O pads that is disclosed in the '665 patent) – and that alone would be that.

94. But merely shunting to a power supply rail is the very technique the '665 patent specification says it is improving upon – by adding “clamp control circuit 204,” which corresponds to the claimed “enable circuit” and “control circuit[ry].” *See, e.g.*, EX1001, 2:35-39 (“This method may be employed as an additional technique to be used in conjunction with other established solutions, such as various clamp devices and clamp circuits, for example, allowing improved ESD performance over the established solutions used alone.”); *id.*, 5:9-35 (discussing control circuit 204).

95. But the '665 invention enables *other I/O cells* to detect ESD activity on a different cell - and to respond in a manner that shares the ESD charge. *See* EX1001, 2:21-39. While the concept of ESD pad charge sharing is depicted at a high-level in Fig. 1, it is Fig. 2 of the '665 patent that shows the details—and specific circuitry such as the “enable circuit” and “control circuit[ry]”—that make it possible for an I/O cell to detect an ESD strike on another cell and respond (*viz.*, by turning on its respective pMOS output transistor) and share the ESD charge. *See* Section VIII (discussing the '665 circuitry in Fig. 2).

96. Indeed, the '665 patent discloses an I/O cell that can be replicated over and over - and in each instance, the added cell can turn on its pMOS output transistor and accept shared ESD charge without having to modify the cell or receive any type of instruction from another I/O cell:

Although only two pads are shown in FIG. 1, any and all pads similarly configured between VDDIO rail 122 and VSSIO rail 124 may have their respective PMOS devices turned on (including pad circuit 102a), resulting in the charge being shared across all pads (pads 114a and 114b shown in FIG. 1), that is, across the respective pad capacitances associated with all the pads.

EX1001, 4:13-21. To accomplish this, the control/enable circuitry must appear in a single instance in each I/O cell – so that individual I/O cells can activate on their own. This is only possible if each I/O cell contains its own control/enable circuitry uniquely within itself.

97. Thus, it is my conclusion and opinion that the terms “enable circuitry” (Claim 1), “control circuit” (Claim 6), and “control circuitry” (Claim 14) reflect this reality – that this circuitry (phrased in three different-but-effectively-the-same ways) must be located in each I/O cell that is receiving ESD charge from the I/O pad where the ESD event occurred.

XI. ANALYSIS

98. For this analysis of the three Grounds offered by Petitioner, two general breakouts will be used. First, I will provide a general overview of problematic issues that appear in common across all three of these grounds; second, I will provide some commentary on each specific Ground itself.

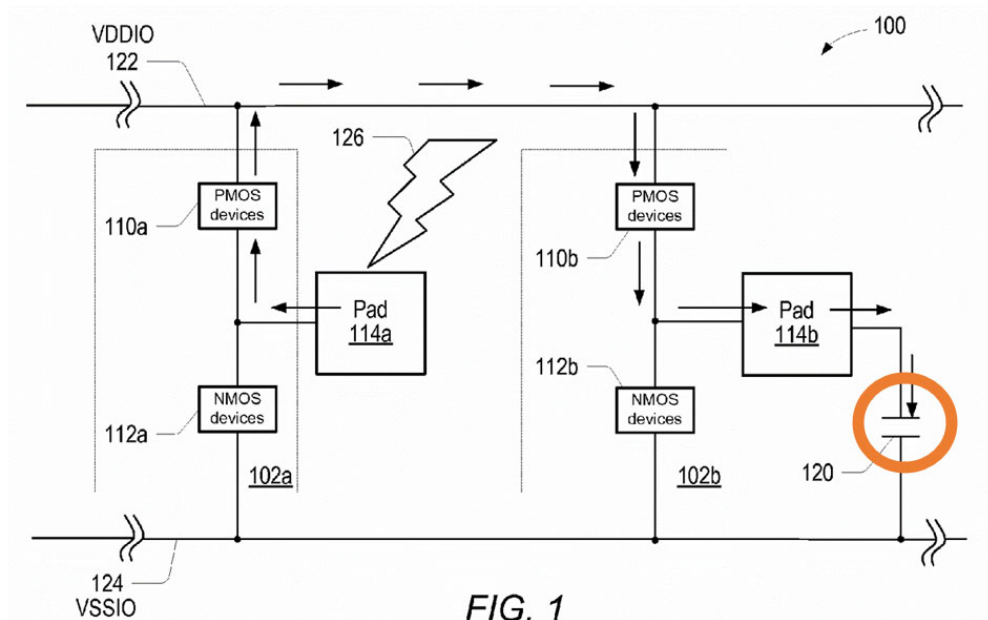
A. General Overview of Relevant Issues Common to All Three Grounds

99. Before considering some detailed analysis of the three Grounds contained in the Petition, some general analytic comments are helpful.

100. Regarding the two primary references (that is, the Verhaege reference and the Ker reference) that Petitioner has cited, both are notable for the simple fact that each makes use of conventional ESD protection circuit functionality; that is, in both cases, the energy of an ESD event is shunted to a power supply rail (either VDD or VSS/GND). Further (and also of notable importance), in both cases, the references only involve the protection of the sensitive circuits associated with its own I/O pad. Neither of these references discloses, discusses, or comprehends the

“spreading” (the word used in the title of the ’665 patent – which could also have been termed “sharing”) of charge from the pad that received an ESD event to other pads in an integrated circuit; this should not be a surprise – since, as noted in the overviews of Verhaege (Section IX.A) and Ker (Section IX.B), each of these references involves the circuitry associated with a single I/O pad. Circuitry involving interactions between/among multiple signal pads are simply not considered by either Verhaege or Ker.

101. In that vein, it should be noted again that the ’665 patent does not teach a *replacement* for the general approach of shunting of ESD event energy to a power supply rail; rather, the ’665 patent teaches an *enhancement* to such known methods (*see, e.g.*, EX1001, 2:35-39); as described in the overview of the ’665 patent (Section VIII), the ’665 patent teaches the use of adjacent pads to (as per the patent title) spread (*i.e.*, share) the charge induced by an ESD event to other signal pads of the IC – so that (effectively) this charge is spread out over what amounts to a larger capacitor (*i.e.*, has larger capacitance). This is explained visually in Figure 1 of the ’665 patent:



EX1001, Fig. 1 (annotation added). As was explained in the overview, this spreading/sharing of charge is a unique teaching of the '665 patent – and the '665 patent specifically teaches that the pMOS devices (*i.e.*, 110b above) of other pad circuitry sets are self-activated in order to facilitate this spreading/sharing. As also explained in the overview of the '665 patent (and as just re-explained above), this serves to reduce the peak voltage of any ESD event – which in turn serves to reduce the risk of damage during an ESD event.

102. Petitioner clearly recognizes that the central teachings of the '665 patent cannot be found in the prior art – either explicitly or implicitly – and thus seeks to modify each of the Verhaege and Ker references. Petitioner relies on a two-step logic process; however, while the first step is fairly simple, the second is simply a leap that is not in any of the art – and Petitioner has provided no reasons (or

reasoning) as to why the resulting modified circuits would function in the manner required by the claims.

103. First, Petitioner argues that as an IC has multiple signal pads, there would be multiple instances of a pad, each with its protective circuitry. This is a fairly straightforward assertion – but the logic ends there.

104. Having postulated a two-cell version of Verhaege (Ground 1) or Ker (Ground 3), Petitioner then tries to argue that the resulting implementations—formed from I/O cells which were each designed to simply shunt its own ESD current at its own pad to a supply rail—somehow results in ESD charge sharing/spreading between I/O pads. But that is simply not how the circuits operate – nor was it how the circuits were designed to operate. And even when Petitioner further modifies its already modified two-cell version of Verhaege to try and establish pad-charge sharing in Ground 2, Petitioner completely fails to address important architectural changes it made – let alone demonstrate that the resulting circuit has a reasonable expectation of success.

105. However, even if one accepts the conclusory leap from the circuitry actually disclosed in either Verhaege or Ker to the synthesized combined embodiments (which I do *not* accept), Petitioner still fails on all three Grounds – since none of the resulting I/O cells have their own “enable circuit” or “control circuit[ry]” to detect an ESD event in a different cell and turn on the respective

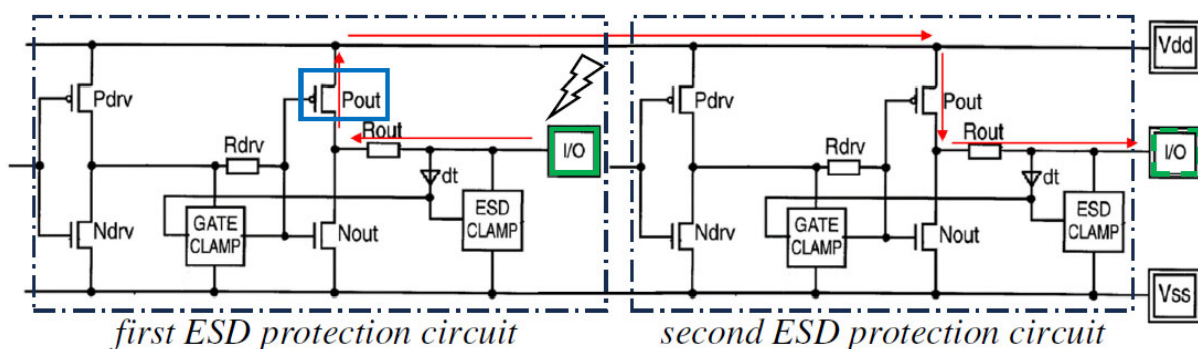
pMOS output transistor that would cause the spreading/sharing of ESD event charge from the affected pad to occur. Petitioner fails to even try and explain how this requirement is met - nor could it, because that is simply not how the I/O cells function at the circuit level; this will be explained in more detail below.

B. Ground 1 (obviousness based on Verhaege)

106. Ground 1 fails for at least the two reasons I explain below, either of which alone is fatal.

1. Petitioner Has Failed to Show That Verhaege Renders Obvious ESD Charge Sharing Between/Among the Pads

107. As noted above, Ground 1 (like all three of Petitioner's grounds) is *not* based on an embodiment disclosed directly by Verhaege – but rather is based on a combined embodiment that mashes together two instances of the cited embodiment disclosed by Verhaege.



Pet., 18. In the left-hand I/O cell, Petitioner adds a lightning bolt to indicate that this is where the ESD strike has occurred. Even if one accepts that the ESD event causes

Pout in the left I/O cell to turn on (which Verhaege is silent about),³ all that will definitely happen is that the energy of the ESD event is shunted to the Vdd rail – which is the conventional, known method of dealing with a positive-polarity ESD event (as explained in Section VII.B).

108. However, Petitioner speculates that somehow the pMOS transistor in the right-hand pad circuitry will turn on – so as to allow the energy of the ESD event to be shared onto the pad of that right-hand circuitry. However, Petitioner offers nothing to show how this would be caused to happen.

109. First, it should be noted (as described in Section IX.A) that Verhaege does not disclose any use of the Pout transistor (in Verhaege’s single-pad-only embodiment) for the shunting of the energy of an ESD event to the VDD rail; rather, Verhaege discloses only the shunting of the energy of an ESD event to the VSS rail,

³ As discussed in Section IX.A, Verhaege is concerned with protecting Nout from damage due to an ESD event, and does so by turning Nout off (and shunting ESD current through the ESD clamp). By the same token, it would be equally important to protect Pout from damage that could occur by conducting current during an ESD event. This is also accomplished by the dedicated “ESD clamp” which, as noted, shunts charge from an ESD event to the Vss supply rail. Accordingly, little (if any) current would flow through Pout, and have little (if any) effect on the Vdd voltage.

via the ESD clamp (40). Thus, the use of a possible second path in Verhaege – through Pout to the VDD rail – has been conjured entirely by Petitioner. This is an observation regarding how Petitioner has not only created an embodiment not disclosed by Verhaege, but has also postulated functionalities that are not disclosed by Verhaege. However, the Board need not consider or resolve this issue – because even if one accepts that Verhaege shunts ESD energy shunting to Vdd via Pout, Petitioner has failed to show that this routing discloses any of the teachings of the '665 patent.

110. In particular, Petitioner has not shown how the right-hand Pout device in its synthesized two-pad Ground 1 embodiment is turned on as a consequence of an ESD event striking the left-hand I/O cell of the combined embodiment. In other words, Petitioner has failed to show the required ESD pad charge sharing.

111. All that Petitioner provides is a conclusory statement that somehow a transient increase in the voltage on the VDD rail (due to purported shunting of the energy of a positive ESD event to that rail) will somehow “charg[e] the capacitance of the second I/O pad” (Pet., 18); however, Petitioner shows no analysis to demonstrate that this is the case – and Petitioner shows no functionality under which the Pout device of the right-hand circuitry would turn on in response to an ESD event in the left-hand circuitry. In particular, Petitioner has not shown *how or why* a positive voltage “spike” on the Vdd rail would cause this to happen.

112. As Petitioner does not offer any explanation for how or why the Pout device of the right-hand I/O cell would be turned on, Petitioner has failed on that alone to show how the combined embodiment of Ground 1 performs the ESD charge sharing with other pads. Unless the Pout transistor of the right-hand I/O cell is turned on, then no current can flow through it - from the Vdd rail to the I/O pad of the right-hand I/O cell. Further, even if a voltage “increase” occurred on the Vdd rail (due to the shunting of the energy of an ESD event in the left-hand I/O cell from that pad and up through the Pout transistor of the left-hand I/O cell to the Vdd rail), that “increase” would not travel down through the Pout of the right-hand I/O cell at all – let alone travel down through the Pout of the right-hand I/O cell to activate the “dynamic trigger circuit” (42) of the right-hand cell; the activation of the “dynamic trigger circuit” (42) of the right-hand cell cannot occur *unless the Pout transistor of the right-hand I/O cell was already turned on*. The only ESD event disclosed in Verhaege that can turn on the Pout transistor of the right-hand I/O cell is an ESD event at the I/O pad of *the right-hand I/O cell itself*.

113. In fact, Petitioner’s own description of the operation of the single-cell embodiment disclosed in Verhaege actually agrees with the explanation of the prior paragraph: “A POSITA would understand ... dynamic trigger device 42 must ‘instruct’ gate clamp 44 ... [to] ‘turn[s] on the at least one of the one or more output transistor devices,’ i.e., PMOS transistor 14 (dark blue), by grounding the gates of

the output transistors.” Pet., 22; *see also* EX1002, ¶73 (same). Thus, as Petitioner’s own explanation recognizes, the Pout transistor of the right-hand circuitry turns on when the dynamic trigger 42 (in the right-hand I/O cell) instructs the gate clamp (also in the right-hand circuitry) to turn on Pout;⁴ this only happens when the “dynamic trigger device” in the right-hand I/O cell detects an ESD event at the pad of the right-hand I/O cell – not when there is a voltage spike on the Vdd rail. In other words, Petitioner’s logic suffers from a cause-and-effect problem – requiring that Pout (in the right-hand I/O cell) *already be turned on* for the dynamic trigger (in the right-hand I/O cell) to be able to detect a voltage rise and turn on Pout (in the

⁴ As noted in the overview of Verhaege (Section IX.A) and elsewhere, Verhaege teaches circuitry that is intended to protect the Nout transistor – by shunting the energy of an ESD event at the I/O pad to the Vss rail *not* through Nout, but rather by turning Nout off to protect it, and instead shunting the energy of the ESD event to Vss via the ESD clamp. While Verhaege is silent about protecting Pout, it would also be important to protect that transistor from ESD damage – by preventing current from an ESD event from flowing through it. Thus, it is unsurprising that Verhaege does *not* teach shunting ESD current through Pout to the Vdd rail – and instead teaches only shunting ESD current to the Vss rail solely via the gate clamp (and through *neither* transistor) during an ESD event.

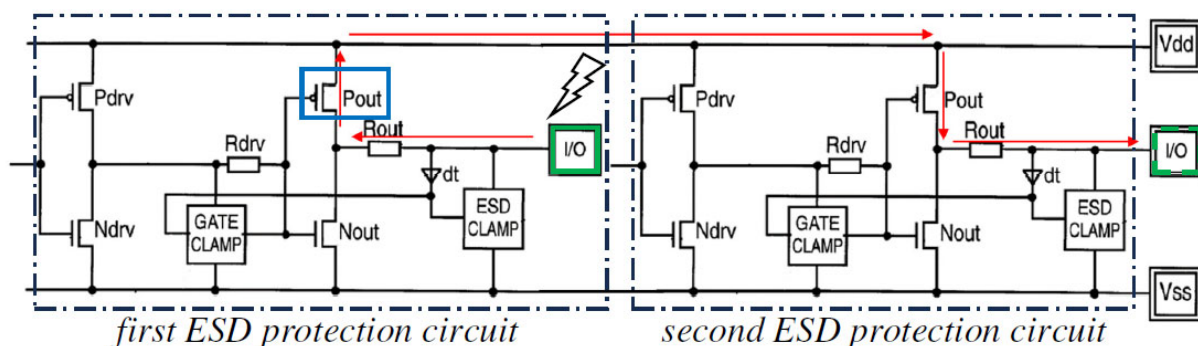
right-hand I/O cell); but without Pout already being turned, this simply cannot happen.

114. Without Pout turned on in the right-hand cell, no current will flow between the Vdd rail on the righthand I/O pad – and therefore, no ESD charge-sharing occurs.

115. Thus, Petitioner has failed to show that Verhaege renders obvious ESD charge sharing between/among the pads.

2. Petitioner Has Failed to Show that Verhaege Renders Obvious the “Enable Circuitry” (Claim 1) or the “Control Circuit[ry]” (Claim 6 and 14)

116. As discussed in Section X.B, the claimed “enable circuitry” of claim 1 and the “control circuit[ry]” of claims 6 and 14 must be located in the I/O cell whose pad shares ESD charge from another I/O cell. Petitioner plainly illustrates the ESD event as occurring in the lefthand I/O cell, as shown below.



Pet., 18.

117. Accordingly, the claimed “enable circuitry” (claim 1) and “control circuit[ry]” (claims 6 and 14) must be in the righthand I/O cell. Petitioner postulates that somehow (as per the above) an ESD event in the left-hand I/O pad will propagate through the Pout device of the right-hand circuitry and activate the “dynamic trigger device” (42) of the right-hand circuitry – which the Petitioner identifies as providing the “enable circuitry” of Claim 1 and the “control circuit[ry]” of Claims 6 and 14. However, Petitioner has failed to show how-or-why the Pout device of the right-hand circuitry would be turned on in response to an ESD event on the left-hand-circuitry’s I/O pad. Indeed, Petitioner has failed to show how an ESD event on the left I/O pad would even reach the “dynamic trigger device” of the right-hand circuitry. Notably, the “dynamic trigger device” of the right-hand circuitry is designed (in Verhaege’s disclosed circuitry) to be activated by an ESD event on the *right-hand circuitry* – not the left-hand circuitry. And again, it must be noted that, according to Verhaege’s teachings, the “dynamic trigger device” serves to activate a shunting of an ESD event (on the immediately-associated I/O pad) to the Vss rail via the “ESD clamp” (40).

118. It is worth noting that Petitioner has painted itself into a corner with its circular reasoning – as Pout (in a non-ESD affected I/O cell) must *already be turned on* for the “dynamic trigger circuit” to be activated. But as Petitioner has not shown how such a Pout would be turned on, the only way for Pout (in a non-ESD-affected

cell) to be turned on would for it to be turned on by activation of the “dynamic trigger device.” But the claims all expressly require “turn[ing] on” or “activat[ing]” Pout, which plainly indicates that Pout was off to begin with. Petitioner’s argument makes no logical sense.

C. Ground 2 (obviousness bases on Verhaege in view of Miller)

119. From the discussion above of Ground 1, it is clear that Petitioner has failed to show that the claims of the ’665 patent are rendered obvious by Verhaege. Thus, Petitioner offers Ground 2 – in which the same synthesized two-cell embodiment of Verhaege is used, but with an addition based on the Miller reference (*i.e.*, Ground 2 is a further modified version of the Verhaege embodiment that Petitioner already modified to create Ground 1).

120. Ground 2 fails for two reasons. First, it suffers from a specific fatal flaw that is unique to Ground 2—failure to establish that the resulting modified circuit has a reasonable expectation of success. Second, Ground 2 fails for the same reason discussed in Section XI.B.2—the claimed “enable circuit” and “control circuit[ry]” (which Petitioner maps to Verhaege’s dynamic trigger (dt)) must reside in the same I/O cell whose pad receives the shared ESD charge. But this is not the case under Petitioner’s mapping.

1. Petitioner Has Failed to Show a Reasonable Expectation of Success for Its Modified Verhaege Circuit

121. As was explained in the overview of Miller (Section IX.C), Miller discloses circuitry in which the energy of an ESD event on a single pad is first shunted from that pad onto the Vdd rail as an intermediate destination for that energy. Then, multiple pathways are activated to shunt that energy from the Vdd rail to its final-resolution destination of the Vss rail.

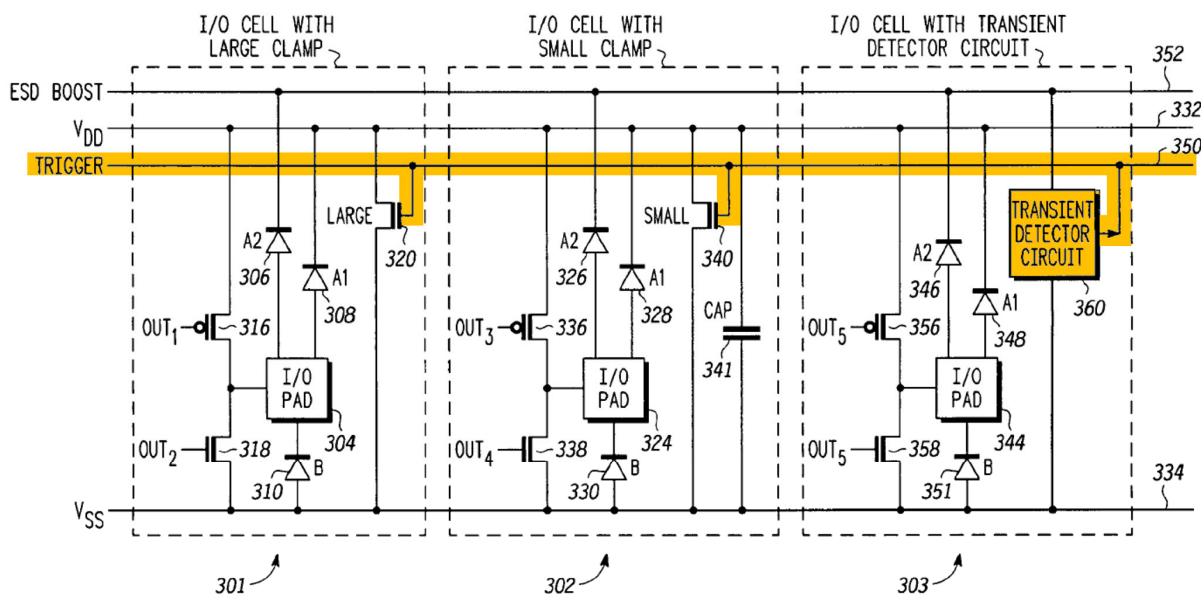
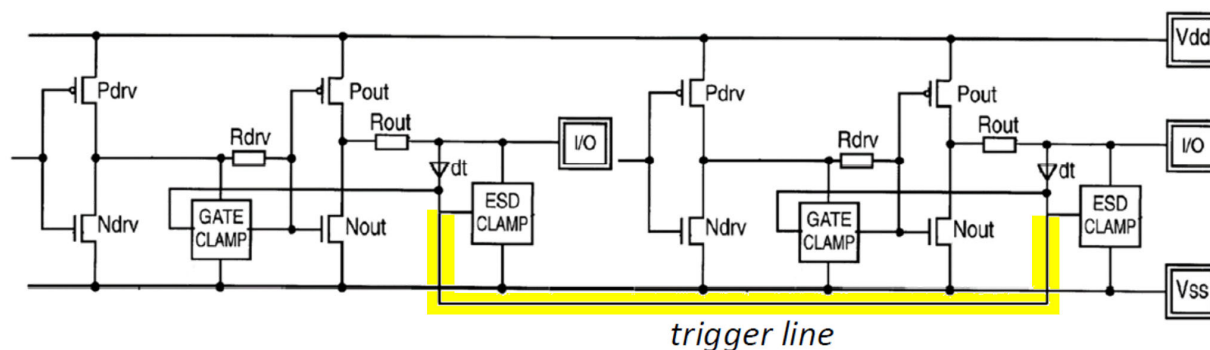


FIG. 3

EX1006 (annotations added). Miller teaches nothing involving the directing of any of that energy (*i.e.*, charge) to any other pad along the way – with the energy of an ESD event at a particular pad being shunted to Vss by first going through Vdd.

122. Petitioner does not actually use the actual circuitry disclosed in Miller to modify Verhaege. Rather, in what can only be characterized as hindsight,

Petitioner uses Miller as a basis for further modification of the synthesized two-cell embodiment that was created for Ground 1 (based on mashing together two instances of Verhaege's single-cell embodiment). The further modification involves the addition of a connection from the "dynamic trigger device" of the left-hand circuitry to the right-hand circuitry, as shown in yellow below.



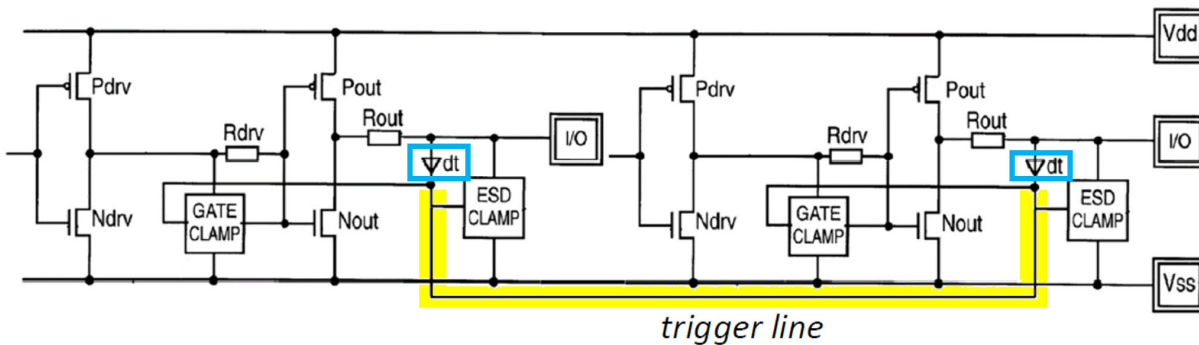
Pet., 51 (modifications by Petitioner, highlighting by Patent Owner).

123. However, this further-modification is, to say the least, problematic. Most notably, as can be seen by inspection of the Figure 3 embodiment of Miller, Miller discloses a *single* detector circuit (360). However, the single-pad-cell embodiment of Verhaege contains its own "dynamic trigger device" – which is triggered by an ESD event on the I/O pad of that cell. Generically, in Petitioner's synthesized mash-up of a two-cell rendition of Verhaege's single-cell embodiment, there will thus be a "dynamic trigger device" in each cell – which will serve to activate the ESD shunting (though ESD clamp 40) to the Vss rail that Verhaege

discloses.⁵ This is significant for two reasons: (1) each cell *must* include a “dynamic trigger device” – because it would otherwise be incapable of executing Verhaege’s disclosed protection scheme for transistor Nout; and (2) Petitioner cannot jettison the dynamic trigger from any I/O cell – because, *e.g.*, claim 14 expressly requires “respective control circuitry” in “each pad” circuit.

124. Petitioner has now added a line to Verhaege that attempts to communicate the presence of an ESD event in the left-hand circuitry to the right-hand circuitry. However, this involves sending a signal from the “dynamic trigger circuit” dt (shown in blue) of the left-hand I/O cell over to the right-hand I/O cell. As just mentioned (and in sharp contrast to Miller and its one “transient detector circuit”), the righthand I/O cell already *has* its own (and *must* have its own) “dynamic trigger circuit” dt (also shown in blue).

⁵ This in fact occurs when there is an ESD event on the specific pad of that specific cell – which will activate the shunting to a rail (the Vss rail in the teachings of Verhaege, and the Vdd rail in the postulations added to Verhaege by Petitioner). Thus, the synthesized two-cell version of Verhaege will operate exactly as does the single-cell version of Verhaege.



Pet., 51 (modifications by Petitioner, highlighting by Patent Owner).

125. Petitioner has provided no explanation or discussion of how the presence of *two* “dynamic trigger circuits” can be made to function properly – since these two dynamic trigger circuits can clearly come into conflict with each other. This is a problem that did not exist in Miller—which has only a single detector circuit shared among multiple I/O cells. Accordingly, there was no need for Miller to address the problem of potential conflicting signals trying to drive a single node – and Miller does not provide a solution (as this would be unnecessary to Miller’s circuitry). Rather, the problem is one of Petitioner’s own making (and one that it ignores).

126. In the synthesized embodiment of Ground 1 – which did not have the yellow-highlighted line shown just above – the output of the “dynamic trigger circuit” is connected only to the ESD clamp and gate clamp *of its own I/O cell*. In contrast, in the Ground 2 embodiment, these formerly-independent nodes are blithely connected together – into a single topological node. Thus, in this

embodiment, this single node is controlled by two *independent* “dynamic trigger circuits” – rather than one, each of which could be trying to drive a different value onto the common signal line.

127. Petitioner has simply ignored this important issue – and Petitioner has offered no explanation of how conflicts at this (now-single) node can be prevented or avoided. Further, Petitioner (as discussed in Section XI.A) has noted that the ’665 patent teaches that multiple (rather than one) I/O cells can be used to spread out (*i.e.*, share) the charge induced by an ESD event on a particular pad. This would only serve to further compound the problem of which dynamic trigger would control the shared node. This is not a mere triviality, but represents an architectural difference between Miller and Verhaege that must be account for. But Petitioner totally ignored the problem it created.

128. Thus, Petitioner has failed to show that the synthesized embodiment of Ground 2 has a reasonable expectation of success.

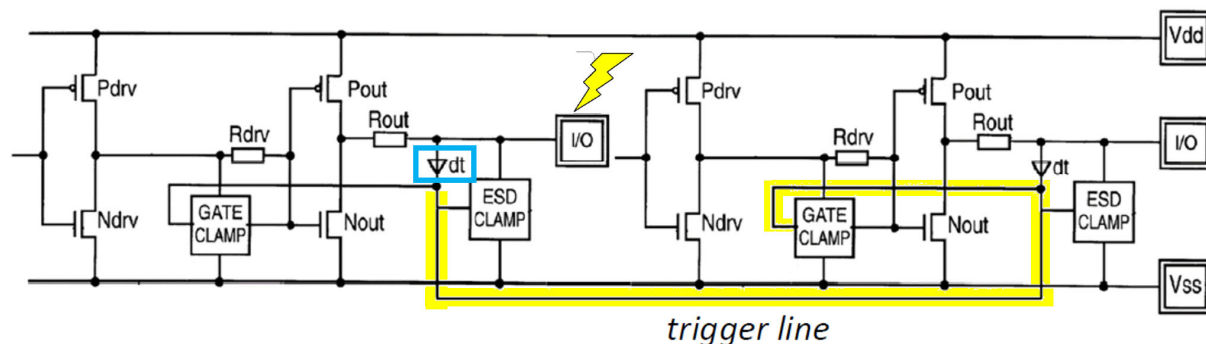
2. Petitioner Has Failed to Show How the Verhaege/Miller Combination Discloses the Claimed “Enable Circuitry” (Claim 1) and “Control Circuitry” (Claims 6 and 14)

129. In Section XI.B.2, discussing Ground 1, it was shown that the synthesized two-cell embodiment of Ground 1 (based on mashing together two copies of the single-cell embodiment actually disclosed by Verhaege) has not been shown by Petitioner to disclose either the “enable circuitry” of Claim 1 or the

“control circuit[ry]” of Claims 6 and 14 – for reasons that were detailed there. Not surprisingly, as Petitioner’s Ground 2 embodiment is only a slightly-modified version of Petitioner’s Ground 1 embodiment, once again it has not been shown by Petitioner that the Ground 2 embodiment discloses these claim terms.

130. As described in Section XI.B.2, the claims of the ’665 patent require that each I/O cell have its own enable/control circuitry – so that the pMOS devices (114b) can be activated for a cell other than the one where the ESD event has occurred; this is how charge is spread to (*i.e.*, shared with) other I/O pads, as a method of reducing the peak voltage of an ESD event.

131. However, this is simply not the case in the synthesized Ground 2 embodiment that Petitioner has created; this can readily be seen by simple inspection:



Pet., 51 (modifications by Petitioner, highlighting by Patent Owner). In this embodiment, the right-hand cell circuitry is being controlled by the control circuitry (*i.e.*, the “dynamic trigger circuit”) of the *left-hand cell circuitry* – not the control

circuitry (*i.e.*, the “dynamic trigger circuit”) of the right-hand cell circuitry. Thus, this combined embodiment fails to disclose the claim elements of Claims 1, 6, and 14 that require that each I/O cell circuit be controlled by control/enable circuitry within itself, in response to an ESD event on a different I/O pad.

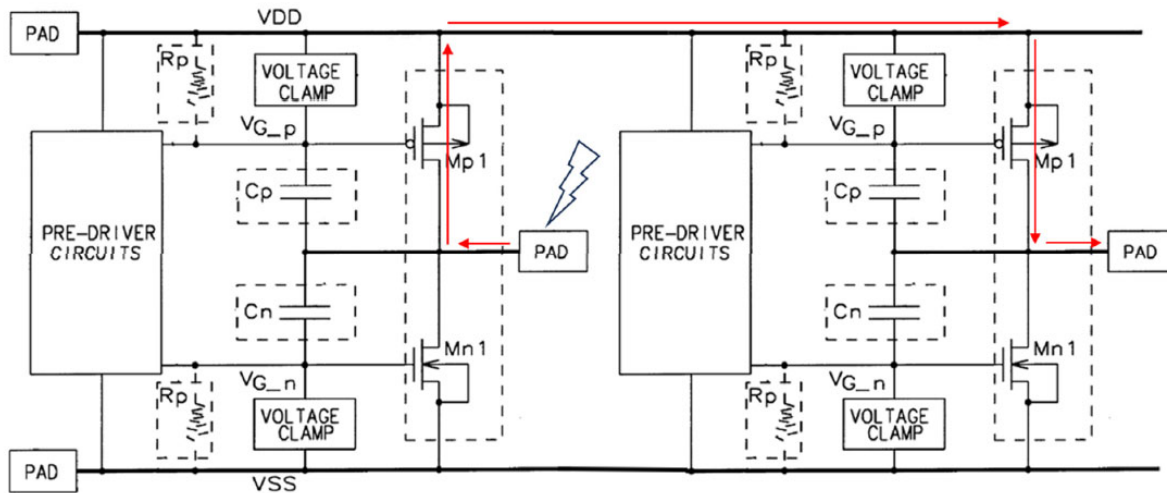
132. Thus, Petitioner has failed to show that the control/enable claim elements are disclosed or rendered-obvious via the embodiment created for Ground 2.

D. Ground 3 (obviousness based on Ker)

133. Ground 3 is based on an embodiment that was created by Petitioner, in a manner that is basically identical to the type of synthetic embodiment created by Petitioner for Ground 1; thus, it suffers from the same deficiencies as were discussed for Verhaege in Ground 1.

1. Petitioner Has Failed to Show That Ker Renders Obvious ESD Charge Sharing Between/Among the Pads

134. As noted above, Ground 3 (like all three of Petitioner’s grounds) is *not* based on an embodiment disclosed directly by Ker – but rather is based on a combined embodiment that mashes together two instances of the cited embodiment disclosed by Ker.



Pet., 67. In the left-hand I/O cell, Petitioner adds a lightning bolt to indicate that this is where the ESD strike has occurred.

135. As foreshadowed above, Petitioner has failed to understand the operating details of Ker – which can be shown by examining how an ESD event affects the left-hand cell of the two-cell mashed-up embodiment that Petitioner has created for Ground 3. As noted in the overview of Ker provided earlier (in Section IX.B), unlike Verhaege (which contemplates and discusses only positive-polarity ESD events), Ker contemplates both positive-polarity and negative-polarity ESD events.⁶

⁶ As was also noted there, the cited single-cell embodiment of Ker (which is shown at Figure 29 of Ker), differs somewhat from the conventional prior-art approaches to ESD protection against both positive-polarity and negative-polarity events –

136. In the Ground 3 presentation, it is not clear whether Petitioner's invalidity theory relies on a positive ESD event or a negative ESD event - therefore, here I will address both scenarios.

137. ***Positive ESD Event.*** If Petitioner's theory relies on a positive polarity ESD event on the lefthand pad, it fails immediately – because a positive ESD pulls the voltage on node V_{G_p} high; since V_{G_p} controls the gate voltage on pMOS transistor Mp1, Mp1 is turned off. *See* Section VII.A (describing operation of a pMOS transistor); Section IX.B (describing Ker). With Mp1 turned off, no ESD current can (or will) flow between the I/O pad on the left (where the ESD event occurred) and the Vdd rail. Thus, Petitioner's diagram showing the purported flow of current is incorrect – because it simply cannot happen. Unless Mp1 in the left I/O cell is on, there can be no ESD charge sharing with the righthand I/O cell, as per Petitioner's annotated version of its synthesized Ground 3 embodiment.

138. Rather, as described in Section IX.B (and in Ker itself), a positive ESD event at the lefthand pad turns on Mn1 (an nMOS transistor) by pulling its gate high

wherein Ker shunts the energy of positive-polarity ESD events to the V_{ss} rail (rather than the Vdd rail), and shunts the energy of negative-polarity ESD events to the V_{dd} rail (rather than the V_{ss} rail).

- which serves to shunt the ESD current through Mn1 to Vss; however, this is of no consequence here, as Petitioner has not discussed such an event.

139. In summary, the functionality depicted by Petitioner for this synthesized Ground 3 embodiment will not function as shown in the case of a positive-polarity ESD event.

140. **Negative ESD Event.** Now, consider what happens if the depicted ESD event is a negative polarity event. To begin, it is apparent that – as was the case for Verhaege (Ground 1) – for charge-sharing to occur between pads in Petitioner’s multi-cell implementation of Ker, the Mp1 transistors in both the left-hand I/O cell and the right-hand I/O cell must be turned on. If either transistor is off, there simply cannot be any ESD-charge pad sharing; therefore, both cells must be analyzed. In the case of a negative ESD strike on the left I/O pad, the negative-polarity energy will activate the upper detection circuitry (based on capacitor Cp); this will pull the

gate of transistor Mp1 in the left I/O cell low, which will turn on transistor Mp1.⁷

This will shunt the energy of the negative polarity ESD event to the Vdd rail.⁸

141. However, nothing unconventional has happened – as the energy of the ESD event has been shunted to a rail (with Ker being different only in the relatively-unimportant difference that, as mentioned above, a negative-polarity event is shunted to the Vdd rail rather than to the Vss rail). At this point, as was also the case with Ground 1, Petitioner is stranded in trying to find some way to create additional functionality for this synthesized Ground 3 embodiment.

142. In particular, Petitioner assumes that the Mp1 transistor of the right-hand cell will somehow turn on – to create the functionality disclosed in the '665

⁷ In the same vein as what was explained above, the negative-polarity event will be detected by the lower detection circuitry – which will also pull the gate of transistor Mn1 low, turning transistor Mn1 off.

⁸ If Petitioner's annotated red arrows are intended to depict current flow, the direction of current is definitionally incorrect -- current flows from a higher potential to a lower potential (*i.e.*, from a higher voltage to a lower voltage) – not the other way around. In short, Petitioner's annotated red arrows point in the wrong direction. For my analysis here, I will assume that Petitioner intended the arrows to reflect that flow of *negative* charge from a negative polarity ESD event.

patent. However, Petitioner has provided nothing which shows that this happens - let alone offer an explanation as to *how or why* this would happen. The Mp1 transistor of the right-hand cell is intended to turn on during a negative-polarity ESD event *at the I/O pad of the **right-hand cell*** – and Petitioner has not shown how it would be turned on by a negative-polarity event at the pad of the left-hand cell.

143. Petitioner provides only a conclusory and unsupported assertion that somehow the energy of the ESD event reaching the Vdd rail will turn on the Mp1 transistor of the right-hand cell. However, as this assertion (as just mentioned) is conclusory and unsupported, it cannot be given credence.

144. As Petitioner does not offer any explanation for how or why the Mp1 transistor of the right-hand circuitry would be turned on, Petitioner has failed on that alone to show how the combined embodiment of Ground 3 performs ESD charge sharing with other pads.

145. Unless the Mp1 transistor of the right-hand I/O cell is turned on, no current can flow through it, from the Vdd rail to the I/O pad of the right-hand I/O cell. Further, even if a voltage “increase” occurred on the Vdd rail (due to the shunting of the energy of an ESD event in the left-hand circuitry from that pad and up through the Pout of the left-hand circuitry to the Vdd rail), that “increase” would not travel down through the Mp1 transistor of the right-hand I/O cell (to activate the ESD detection circuitry of the right-hand cell) *unless Mp1 in the right-hand circuitry*

was already turned on. The only ESD event on an I/O pad disclosed in Ker that can turn on the Mp1 transistor of the right-hand I/O cell is an ESD event at the I/O pad *of the right-hand I/O cell itself.*

146. Additionally, as was the case with Ground 1 (and as summarized for Ground 3 in the preceding paragraph), Petitioner’s failure to show how an ESD-event-induced voltage change on the Vdd rail would somehow turn on the right-hand Mp1 transistor leaves Petitioner stranded with a cause-and-effect problem (*viz.*, the events that must occur for the Mp1 transistor of the right-hand cell to be turned on require (in Petitioner’s reasoning) that *the Mp1 transistor of the right-hand cell already be turned on first*). This makes no logical sense.

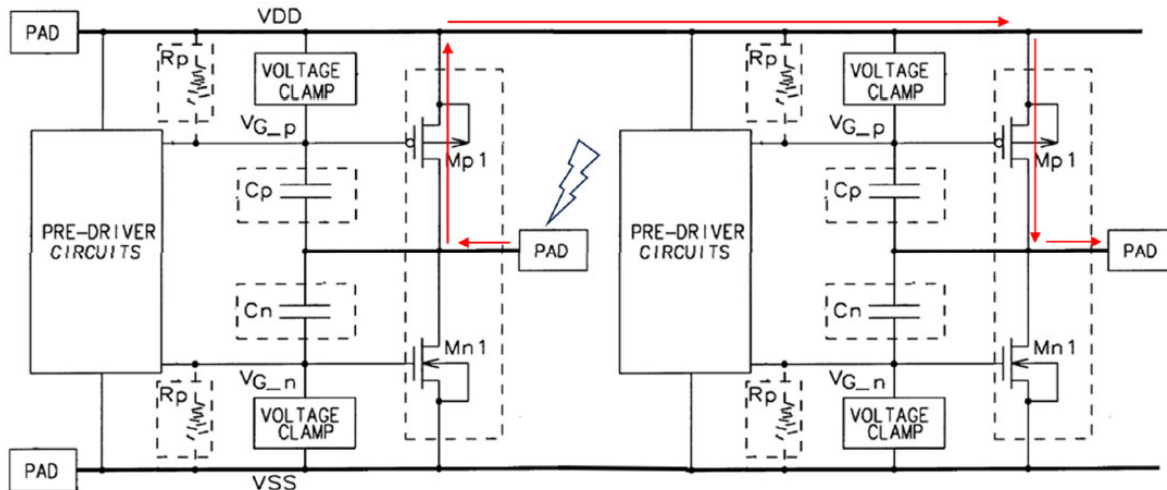
147. Thus, Petitioner has failed to show that Ker renders obvious ESD charge sharing between/among the pads.

2. Petitioner Has Failed to Show That Ker Renders Obvious the “Enable Circuitry” (Claim 1) or the “Control Circuit[ry]” (Claim 6 and 14)

148. As explained previously, because the claims require the output transistor (which Petitioner maps to Mp1) to “turn on” (claim 1) or “activate” (claims 6 and 14), the logical implication is that Mp1 is off to begin with. Otherwise, it could not “activate” / “turn on” because it would already *be* on/activated.

149. Further, as discussed in Section X.B, the claimed “enable circuitry” of claim 1 and the “control circuit[ry]” of claims 6 and 14 must be located in the I/O

cell whose pad receives ESD charge from another I/O cell. Petitioner plainly illustrates the ESD even occurring in the lefthand I/O cell, as shown below.



Pet., 67.

150. Accordingly, the claimed “enable circuitry” (claim 1) and “control circuit[ry]” (claims 6 and 14) must be in the righthand I/O cell - and must also be the circuitry that turns on Mp1 in the righthand cell. Petitioner postulates⁹ that (as per the above) a negative ESD event in the left-hand I/O pad (which, as shown, must specifically be a negative-polarity event to even connect the left I/O pad to the Vdd

⁹ In contrast to Ground 1 where Petitioner plainly relies on a positive voltage ESD event for Verhaege, Petitioner plays fast and loose in Ground 3 for Ker as to whether it relies on a positive voltage ESD event or a negative voltage ESD event; this is a major shortcoming (as discussed in Section XI.D.1) with Petitioner's usage of Ker.

rail) will propagate through the Mp1 device of the right-hand circuitry and somehow activate the detection circuitry of the right-hand I/O cell – which the Petitioner identifies as providing the “enable circuitry” of Claim 1 and the “control circuit[ry]” of Claims 6 and 14. However, Petitioner has failed to show how-or-why the Mp1 device of the right-hand circuitry would be turned on in response to an ESD event on the left-hand-circuitry’s I/O pad. Notably, the detection circuitry in the right-hand I/O cell of Petitioner’s combined embodiment was designed to be activated by an ESD event on the *right-hand circuitry* – not the left-hand circuitry.¹⁰ And again, it must be noted that, according to Ker’s teachings, the detection circuitry serves to activate a shunting of a negative-polarity (but not a positive-polarity) ESD event (on the immediately-associated I/O pad) to the Vdd rail via the Mp1 transistor of that cell. There is nothing in Ker’s disclosed circuitry that would, in the synthesized two-cell embodiment created by Petitioner for Ground 3, cause an ESD event in the left-

¹⁰ Again, Ker discloses only a *single* I/O cell, not a combined embodiment at all. Thus, the functionality of the righthand I/O cell in Petitioner’s combined embodiment is no different than if it were not part of a combined embodiment. This cuts against the notion that the righthand I/O cell does anything in response to an ESD event on the lefthand I/O pad. Any purported additional functionalities, including intercell interactions, are of Petitioner’s own making.

hand cell to activate the Mp1 transistor of the right-hand cell; each cell is self-contained, and provides ESD protection for that cell in-and-of itself.

151. It is worth noting that, as mentioned above, Petitioner has painted itself into a corner with its circular reasoning – as Mp1 (in a non-ESD affected I/O cell) must *already be turned on* for the detection circuitry to be activated. But as Petitioner has not shown how such an Mp1 would be turned on, the only way for Mp1 (in a non-ESD-affected cell) to be turned on would for it to be turned on by activation of the detection circuitry. None of this makes any logical sense.

XII. CONCLUSION

152. I am aware that this declaration will be filed as evidence in an IPR proceeding before the PTAB. I am aware that making willfully false statements in my declaration are punishable by fine or imprisonment, or both (under 18 U.S.C. § 1001), and thus such actions may compromise the validity of the IPR Petition. All statements herein made by me of my own knowledge are true, and all statements made on information and belief are believed to be true.

Decl. of Dr. Daniel Foty

153. I declare under penalty of perjury that the foregoing is true and correct.

Executed this 13th day of August, 2024 in Fletcher, Vermont.



Daniel Foty, Ph.D.