DANIEL FOTY, Ph.D.

SUMMARY

Dr. Foty has more than 30 years of engineering and management experience in the mainstream of the technology industry. During this time, he has worked in semiconductor physics, device design, process integration, modeling/simulation (process, device, and circuit), circuit design/analysis, and wireless communications. After seven years at the microelectronics unit of IBM, he founded his own consulting firm, Gilgamesh Associates, LLC, which works in very demanding areas of technology design and development such as analog, mixed-signal, RF, signal processing, wireless communications, and ultra-low-power design.

Dr. Foty is also an advisor to the Tallinn University of Technology (Estonia) and the University of Pretoria (South Africa). He is also the author of *MOSFET Modeling with SPICE: Principles and Practice*, the more-recent *Moore's Law: The Untold* Story, and several other books. He has also authored well over 100 journal articles and conference presentations, and is a frequent plenary (keynote) speaker at major international conferences throughout the world. He is also a licensed pilot and aircraft owner, possesses both an instrument rating and a seaplane rating, and is a registered "angel pilot" with Patient Airlift Services.

Expertise

- Analog/Mixed-Signal/RF CMOS
- CMOS Integrated Circuit Design
- IC Modeling/Simulation
- CMOS Technology and Process Integration
- Semiconductor Manufacturing/Fabrication
- Nanotechnology
- Design Automation (EDA) Software
- Semiconductor Memory (DRAM, SRAM, Flash)
- Semiconductor Physics
- RF/Radio Technology, Wireless Networks, and Wireless Communications
- Power Management
- Digital Communications, Signal Integrity, and Electromagnetic Interference
- Cryogenic Electronics

PROFESSIONAL EXPERIENCE

1994 to Present **Gilgamesh Associates, LLC**
President

- Analysis of analog/mixed-signal/RF CMOS circuits
- New technologies in high-speed wireless data communications
- Specialized process-design-kits (PDKs) for circuit design/simulation
- Foundry interfacing for fabless IC design companies
- Professional education via short courses and lectures
- Litigation support in various aspects of the integrated circuit industry

1988 to 1994 **IBM Microelectronics Division**
Scientist/Engineer

- Process integration, device design, semiconductor/IC physics
- Process and device simulation; circuit simulation
- Process and device integration for memory and logic technologies
- Process-design-kits (PDKs) for circuit simulation
- Spearheaded initial IBM foray into OEM foundry market; responsible for all "external customer" PDKs and support/interfacing; business grew from nothing to $66M in revenue in first year.

EDUCATION

Ph.D., Materials Science, University of Vermont, 2001
MS, Electrical Engineering, University of Illinois, 1985
BS, Physics and Chemistry, Bates College, 1983

LITIGATION RELATED EXPERIENCE

Dr. Foty has served as a testifying expert, and provided declarations, expert reports, trial testimony, and arbitration-hearing testimony for cases that have touched on the complete spectrum of semiconductor/electronics engineering issues, electronic design automation software, wireless technology, contract interpretations and business processes, and prior art searches in both patents and the public-domain literature. He has also served as a consulting expert. Dr. Foty has been deposed some thirty times, and has testified at trial six times. Below are matters in which he has written expert reports and given testimony either at deposition, trial, or before an arbitration panel.

Type of Matter:	Patent infringement involving silicon-based visible/IR light sensor technology
Law Firm:	Troutman Pepper, LLP, Boston, Massachusetts
Case Name:	SiOnyx v. Samsung
Represented:	Respondent
Case Number:	337-TA-1403
Filing Date:	4/30/2024
Court:	ITC matter
Disposition:	Ongoing.
Date:	February 2024 – present.

Type of Matter:	*Inter Partes* review involving ESD protection
Law Firm:	Orrick, Herrington & Sutcliffe LLP, Menlo Park, California
Case Name:	Aptiv v. Microchip
Represented:	Patent Holder
Case Number:	IPR2024-00803
Filing Date:	4/15/2024
Court:	Patent Trial and Appeal Board
Disposition:	Prepared a declaration supporting Patent Owner's POPR; ongoing.
Date:	June 2024 – present.

Type of Matter:	*Inter Partes* review involving current buffer optimization
Law Firm:	Orrick, Herrington & Sutcliffe LLP, Menlo Park, California
Case Name:	Aptiv v. Microchip
Represented:	Patent Holder
Case Number:	IPR2024-00646
Filing Date:	3/8/2024
Court:	Patent Trial and Appeal Board
Disposition:	Prepared a declaration supporting Patent Owner's POPR; ongoing.
Date:	May 2024 – present.

Type of Matter:	Patent infringement involving current buffer optimization and ESD protection
Law Firm:	Gish PLLC, New York, New York
Case Name:	Microchip v. Aptiv

Represented:	Patent holder
Case Number:	C.A. No. 1:23-CV-00778-JDW
Filing Date:	3/20/2023
Court:	US District Court of the District of Delaware
Disposition:	Ongoing.
Date:	May 2023 – present.

Type of Matter:	*Inter Partes* review involving silicon-based display technology
Law Firm:	Orrick, Herrington & Sutcliffe LLP, Menlo Park, California
Case Name:	BoE v. Samsung Display Corporation
Represented:	Petitioner
Case Number:	IPR2023-01221
Filing Date:	7/26/2023
Court:	Patent Trial and Appeal Board
Disposition:	Prepared a declaration supporting the petitioner; ongoing.
Date:	June 2023 – present.

Type of Matter:	*Inter Partes* review involving silicon-based display technology
Law Firm:	Orrick, Herrington & Sutcliffe LLP, Menlo Park, California
Case Name:	BoE v. Samsung Display Corporation
Represented:	Petitioner
Case Number:	IPR2023-00941
Filing Date:	6/9/2023
Court:	Patent Trial and Appeal Board
Disposition:	Prepared two declarations supporting the petitioner; deposed twice; ongoing.
Date:	May 2023 – present.

Type of Matter:	Patent infringement involving dynamic memory technology
Law Firm:	Irell & Manella LLP, Los Angeles, California
Case Name:	Demaray v. Samsung
Represented:	Patent holder
Case Number:	6:20-CV-634-ADA
Filing Date:	3/4/2022
Court:	US District Court of the Western District of Texas
Disposition:	Ongoing.
Date:	May 2023 – present.

Type of Matter:	Patent infringement involving silicon-based display technology
Law Firm:	Orrick, Herrington & Sutcliffe LLP, Menlo Park, California
Case Name:	Samsung Display Corporation v. BoE
Represented:	Respondent
Case Number:	337-TA-1351
Filing Date:	12/28/2022
Court:	ITC matter
Disposition:	Prepared a declaration; prepared an expert report and a rebuttal expert report; testified at hearing; ongoing.

Date:	March 2023 – present.
Type of Matter:	Patent infringement involving wireless communications technology
Law Firm:	Folio Law Group, LLP, Seattle, Washington
Case Name:	Dali Wireless v. AT&T Corp
Represented:	Patent holder
Case Number:	Case No. 2:22-cv-00012
Filing Date:	1/7/2022
Court:	US District Court of the Eastern District of Texas
Disposition:	Prepared an expert report; deposed; ongoing.
Date:	March 2023 – present.
Type of Matter:	Patent infringement power management technology
Law Firm:	Bunsow DeMory LLP, Redwood City, California
Case Name:	BitMICRO v. Kioxia
Represented:	Patent holder
Case Number:	6:22-cv-00331-ADA
Filing Date:	3/30/2022
Court:	US District Court of the Western District of Texas
Disposition:	Settled.
Date:	November 2022 – August 2023.
Type of Matter:	Patent infringement power management technology
Law Firm:	Bunsow DeMory LLP, Redwood City, California
Case Name:	BitMICRO v. Intel
Represented:	Patent holder
Case Number:	W-22-CV-00335-ADA
Filing Date:	3/30/2022
Court:	US District Court, Western District of Texas
Disposition:	Venue has been shifted to the Northern District of California; ongoing; settled.
Date:	November 2022 – December 2023.
Type of Matter:	Patent infringement involving semiconductor technology
Law Firm:	Mintz, Levin, Cohn, Ferris, Glovsky and Popeo, P.C., Boston MA
Case Name:	Daedalus Prime v. Samsung and TSMC
Represented:	Patent holder
Case Number:	337-TA-1336
Filing Date:	9/13/2022
Court:	ITC matter
Disposition:	Consulting expert; settled.
Date:	September 2022 – August 2023.
Type of Matter:	Patent infringement involving wireless communications technology
Law Firm:	Folio Law Group, LLP, Seattle, Washington

Case Name:	Dali Wireless v. Corning
Represented:	Patent holder
Case Number:	3:20-cv-06469-EMC
Filing Date:	9/16/2020
Court:	US District Court of the Northern District of California
Disposition:	Prepared an expert report, deposed; matter settled.
Date:	May 2022 – November 2022.

Type of Matter:	*Inter Partes* review involving power conversion technology in solar power systems
Law Firm:	Sheridan Ross LLP, Denver, Colorado
Case Name:	SolarEdge Technologies, Ltd. v. Koolbridge Solar, Inc.
Represented:	Patent holder
Case Number:	IPR2022-00007, -00010, -00013
Filing Date:	10/11/2021, 10/11/2021, 10/8/2021
Court:	Patent Trial and Appeal Board
Disposition:	Prepared three declarations supporting the patent holder; deposed; ongoing.
Date:	June 2022 – present.

Type of Matter:	Patent infringement involving wireless communications technology
Law Firm:	Folio Law Group, LLP, Seattle, Washington
Case Name:	Dali Wireless v. Corning
Represented:	Patent holder
Case Number:	6:20-cv-00827-ADA
Filing Date:	10/22/2020
Court:	US District Court of the Western District of Texas
Disposition:	Prepared an expert report; matter settled.
Date:	November 2021 – February 2022.

Type of Matter:	Patent infringement involving integrated circuit layout for lithographic control
Law Firm:	Jones Day LLP, Chicago, Illinois
Case Name:	NXP Semiconductors v. Impinj
Represented:	Plaintiff
Case Number:	2:20-cv-01503-RSM-SKV337-TA-1272
Filing Date:	10/7/2020
Court:	US District Court of the Western District of Washington,
Disposition:	Ongoing.
Date:	November 2021 – present.

Type of Matter:	Patent infringement involving integrated circuit technology
Law Firm:	Jones Day LLP, Washington DC (ITC matter)
Case Name:	MediaTek v. NXP Semiconductors
Represented:	Respondent
Case Number:	337-TA-1272

Filing Date:	6/21/2021
Court:	International Trade Commission
Disposition:	Ongoing.
Date:	April 2021 – present.

Type of Matter:	Patent infringement involving portable vehicle battery jump starters
Law Firm:	Fox Rothschild LLP, Philadelphia, Pennsylvania (ITC matter)
Case Name:	The Noco Company v. Deltran Global
Represented:	Respondent
Case Number:	337-TA-1256
Filing Date:	1/19/2021
Court:	International Trade Commission
Disposition:	Prepared an expert report; deposed; plaintiff withdrew complaint against Deltran.
Date:	June 2021 – November 2021.

Type of Matter:	Patent infringement involving integrated circuit technology and signal integrity
Law Firm:	Jones Day LLP, Chicago, Illinois
Case Name:	WSOU v. Xilinx
Represented:	Respondent
Case Number:	1:20-cv-01228-CFC; 1:20-cv-01229-CFC
Filing Date:	09/16/2020
Court:	US District Court District of Delaware
Disposition:	Prepared an expert report; matter settled.
Date:	April 2021 – December 2022.

Type of Matter:	Patent infringement involving wireless communications technology
Law Firm:	Folio Law Group, LLP, Seattle, Washington
Case Name:	Dali Wireless v. JMA
Represented:	Patent holder
Case Number:	1:19-cv-02367-RGA
Filing Date:	12/30/2019
Court:	US District Court District of Delaware
Disposition:	Settled.
Date:	March 2021 – November 2021.

Type of Matter:	Patent infringement involving wireless communications technology
Law Firm:	Folio Law Group, LLP, Seattle, Washington
Case Name:	Dali Wireless v. Commscope
Represented:	Patent holder
Case Number:	1:19-cv-00952
Filing Date:	5/22/2019
Court:	US District Court District of Delaware

Disposition:	Prepared an expert report; deposed; ongoing.
Date:	March 2021 – present.

Type of Matter:	Patent infringement involving integrated circuit technology (ITC matter)
Law Firm:	Troutman Pepper LLP, Boston, Massachusetts
Case Name:	Tela v. Intel
Represented:	Patent holder
Case Number:	337-TA-1246
Filing Date:	12/18/2020
Court:	International Trade Commission
Disposition:	Settled; this includes all prior disputes between the parties
Date:	March 2021 – April 2021.

Type of Matter:	Patent infringement involving wireless battery charging and discharging
Law Firm:	Feinberg Day Kramer Alberti Limtonkovich & Belloli LLP
Case Name:	Garrity Power Services v. Samsung
Represented:	Patent holder
Case Number:	2:20-cv-00269-JRG
Filing Date:	08/17/2020
Court:	US District Court Eastern District of Texas
Disposition:	Case dismissed by the Court
Date:	October 2020 – March 2022.

Type of Matter:	*Inter Partes* review involving wireless battery charging and discharging
Law Firm:	Spencer Fane LLP, Plano, Texas
Case Name:	Samsung v. Garrity Power Services
Represented:	Patent holder
Case Number:	IPR2021-00389
Filing Date:	12/31/2020
Court:	Patent Trial and Appeal Board
Disposition:	Prepared a declaration; PTAB denied institution.
Date:	October 2020 – July 2021.

Type of Matter:	Patent infringement involving MOS transistor design and MOS transistor manufacturing processes
Law Firm:	Fish & Richardson LLP, Boston, Massachusetts
Case Name:	Innovative Foundry Technologies v. SMIC, Broadcom, Cypress Semiconductor, and Dish Network
Represented:	Respondents
Case Number:	6:19-cv-00719-ADA
Filing Date:	12/20/2019
Court:	US District Court Western District of Texas
Disposition:	Settled
Date:	June 2020 – April 2021.

Type of Matter:	Patent infringement involving digital communications integrated circuit technology
Law Firm:	Morrison & Foerster LLP, Los Angeles, California
Case Name:	Analog Devices v. Xilinx
Represented:	Respondent
Case Number:	1:19-cv-02225-RGA
Filing Date:	12/05/2019
Court:	US District Court District of Delaware
Disposition:	Settled
Date:	April 2020 – April 2022.

Type of Matter:	Patent infringement involving integrated circuit technology
Law Firm:	Pepper Hamilton LLP, Boston, Massachusetts
Case Name:	Intel v. Tela
Represented:	Respondent
Case Number:	3:18-cv-02848-WHO
Filing Date:	05/15/2018
Court:	US District Court Northern District of California
Disposition:	Prepared two expert reports; deposed; matter settled.
Date:	March 2019 – April 2021.

Type of Matter:	Patent infringement involving integrated circuit technology (ITC matter)
Law Firm:	Mintz, Levin, Cohn, Ferris, Glovsky and Popeo, P.C., Boston, Massachusetts
Case Name:	Globalfoundries v. TSMC
Represented:	Patent holder
Case Number:	337-TA-1177
Filing Date:	08/26/2019
Court:	International Trade Commission
Disposition:	Settled.
Date:	August 2019 – October 2019.

Type of Matter:	*Inter Partes* review involving wireless/RF technology
Law Firm:	Jones, Day LLP, Cleveland, Ohio
Case Name:	Intel v. Qualcomm
Represented:	Patent holder
Case Number:	IPR2019-00128, IPR2019-00129, IPR2019-00047, IPR2019-00048, IPR2019-00049
Filing Date:	11/8/2018
Court:	Patent Trial and Appeal Board
Disposition:	Prepared five declarations supporting patent owner responses; deposed; PTAB upheld all challenged claims of the patent as valid.
Date:	June 2019 – July 2020.

Type of Matter:	Patent infringement involving integrated circuit technology

Law Firm:	Pepper Hamilton LLP, Boston, Massachusetts
Case Name:	Tela v. Intel
Represented:	Patent holder
Case Number:	337-TA-1148
Filing Date:	12/19/2018
Court:	International Trade Commission
Disposition:	Prepared two declarations supporting claim construction; prepared an expert report; deposed; testified at the hearing/trial in December 2019.
Date:	March 2019 – December 2019.

Type of Matter:	Patent infringement involving RF/wireless technology
Law Firm:	Quinn Emanuel Urquhart & Sullivan LLP, New York, New York
Case Name:	Qualcomm v. Apple
Represented:	Patent holder
Case Number:	3:17-cv-02402-CAB-MDD
Filing Date:	12/29/2017
Court:	US District Court Southern District of California
Disposition:	Settled.
Date:	January 2018 – December 2018.

Type of Matter:	Patent infringement involving RF/wireless technology
Law Firm:	Quinn Emanuel Urquhart & Sullivan LLP, New York, New York
Case Name:	Qualcomm v. Apple
Represented:	Patent holder
Case Number:	337-TA-1093
Filing Date:	7/7/2017
Court:	International Trade Commission
Disposition:	Prepared two expert reports regarding RF-IC/wireless technology; deposed; testified at the hearing/trial in September 2018.
Date:	January 2018 – September 2018.

Type of Matter:	Patent infringement involving integrated circuit technology and printed-circuit board technology
Law Firm:	Dovel and Luner, LLP, Santa Monica, California
Case Name:	X2Y v. Intel
Represented:	Patent holder
Case Number:	3:18-cv-01394-HZ
Filing Date:	07/25/2018
Court:	US District Court District of Oregon
Disposition:	Prepared a declaration supporting claim construction; deposed; case settled.
Date:	June 2017 – December 2019.

Type of Matter:	Patent infringement involving integrated circuit technology
Law Firm:	Jones, Day LLP, San Francisco, California, and Slater Matsil LLP, Dallas, Texas

Case Name:	IPBridge v. Xilinx
Represented:	Respondent
Case Number:	3:17-cv-06376-JD
Filing Date:	11/01/2017
Court:	US District Court Northern District of California
Disposition:	Settled.
Date:	February 2017 – February 2019.

Type of Matter:	Patent infringement involving analog circuits
Law Firm:	Covington & Burling LLP, San Diego, California
Case Name:	Tessera v. Broadcom
Represented:	Patent holder
Case Number:	1:16-cv-00380-LPS-CJB
Filing Date:	05/23/2016
Court:	US District Court District of Delaware
Disposition:	Settled.
Date:	December 2016 – December 2017.

Type of Matter:	Patent infringement involving integrated circuit design methods and integrated circuit design-automation software
Law Firm:	Jones, Day LLP, Cleveland, Ohio
Case Name:	Synopsys v. ATopTech
Represented:	Patent holder
Disposition:	Prepared an expert report; deposed; matter was suspended when ATopTech filed for Chapter 11 bankruptcy.
Date:	June 2016 – March 2017.

Type of Matter:	Patent infringement involving integrated circuit process/manufacturing technology for wireless communications
Law Firm:	McKool Smith, LLP, Dallas, Texas
Case Name:	Ericsson v. TCL
Represented:	Plaintiff
Disposition:	Prepared an expert report regarding the costs and timelines associated with the development of integrated circuits for wireless communications, and the related difficulties encountered; trial was stayed when an IPR proceeding began, matter has since ended.
Date:	November 2015 – March 2016.

Type of Matter:	*Inter Partes* review involving integrated circuit design methods and integrated circuit design-automation software
Law Firm:	Jones, Day LLP, Cleveland, Ohio
Case Name:	ATopTech v. Synopsys
Represented:	Patent holder
Disposition:	Prepared two declarations; deposed.
Date:	November 2014 – January 2016.

Type of Matter:	*Inter Partes* review involving a semiconductor flash memory technology patent
Law Firm:	Aka Chan LLP, Santa Clara, California
Case Name:	Silicon Motion Technology Corp. v. Phison Electronics Corp.
Represented:	Petitioner
Disposition:	Prepared a declaration; deposed; hearing before the PTAB in September 2014, PTAB ruled completely in Petitioners' favor
Date:	May 2014 – September 2014.

Type of Matter:	Patent infringement involving integrated circuit design
Law Firm:	Bragalone, Conroy, PC, Dallas, Texas
Case Name:	HSM v. Elpida Memory et al. (was HSM v. Fujitsu et al.)
Represented:	Plaintiff
Disposition:	Prepared numerous declarations and two expert reports; deposed; all respondents eventually settled.
Date:	February 2012 – February 2016.

Type of Matter:	Patent infringement involving integrated circuit process/manufacturing technology (ITC matter)
Law Firm:	McKool Smith, LLP, Dallas, Texas
Case Name:	Samsung v. Ericsson
Represented:	Defendant
Disposition:	Was assigned one patent in a larger matter, having done much original engineering work on the technology in question; produced extensive background prior art (having created much of it), demonstrated that the accused technology clearly did not practice the teachings of the patent, and clearly showed that the aforementioned prior art would call the patent's validity seriously into question; plaintiff dropped that patent from the action.
Date:	January 2013 – May 2013.

Type of Matter:	Patent infringement involving integrated circuit design, with a focus on RF-ICs for wireless communications
Law Firm:	Antonelli, Harrington, & Thompson, LLP, Houston, Texas
Case Name:	Semiconductor Ideas to the Market, BV v. Texas Instruments et al.
Represented:	Plaintiff
Disposition:	Prepared a declaration for pre-hearing; major defendant (Qualcomm) settled following this expert's examination of their Confidential Business Information (CBI) in June, 2012; other defendants settled shortly thereafter.
Date:	May 2012 – August 2012.

Type of Matter:	Bond forfeiture proceeding (ITC matter)
Law Firm:	Adduci, Mastriani, & Schaumberg, LLP, Washington, D.C.
Case Name:	Tessera v. Freescale
Represented:	Plaintiff

Disposition:	Following unfavorable ITC ruling, respondent argued that posted bond (pending final disposition) should be returned to them; prepared a declaration for hearing; ITC ruled against respondent, who then agreed to cease litigation and forfeit the bond.
Date:	April 2012 – October 2012.

Type of Matter:	Theft of trade secrets involving integrated circuit design, manufacturing, and characterization technology
Law Firm:	Shore, Chan, Bragalone, and DePumpo, LLP, Dallas, Texas
Case Name:	Xicor v. SST
Represented:	Plaintiff
Disposition:	Prepared a declaration for hearing regarding plaintiff's identification of its trade secrets; following favorable ruling on this, defendant agreed to settle on terms favorable to the plaintiff
Date:	February 2012 – September 2012.

Type of Matter:	Patent infringement in integrated circuit substrates (ITC matter)
Law Firm:	Alston + Bird, LLP, Atlanta, Georgia
Case Name:	X2Y v. Intel
Represented:	Plaintiff
Disposition:	Consulted on technology involved
Date:	August 2011 – August 2012.

Type of Matter:	Theft of trade secrets involving design of power management integrated circuits (ITC enforcement proceeding)
Law Firm:	Alston + Bird, LLP, Menlo Park, California
Case Name:	Richtek v. uPI, and Sapphire Technology
Represented:	Plaintiff
Disposition:	Prepared an expert report and a supplemental expert report; deposed; testified at hearing/trial; subsidiary respondent Sapphire settled and exited the case shortly before trial.
Date:	June 2011 – March 2012; follow-on district/superior court cases temporarily stayed, but pending.

Type of Matter:	Patent infringement in switching power supplies
Law Firm:	McDermott, Will & Emery, LLP, Miami, Florida
Case Name:	Power Integrations, Inc. v. Fairchild Semiconductor International, Inc.
Representing:	Defendant
Disposition:	Presented the tutorial at the Markman hearing in San Jose, California (Northern District of California) in March; matter ongoing, but no longer involved.
Date:	December 2010 – March 2011.

Type of Matter:	Patent infringement in the power management methodologies of portable/mobile device (ITC matter)

Law Firm:	Finnegan, Henderson, Farabow, Garrett & Dunner, LLP, Washington, D.C.
Case Name:	HTC v. Apple
Represented:	Plaintiff
Disposition:	Deposed in March; testified at trial/hearing (ITC) in May; outcome pending.
Date:	November 2010 – May 2011.

Type of Matter:	Theft of trade secrets involving design of power management integrated circuits (ITC matter)
Law Firm:	Alston + Bird, LLP, Menlo Park, California
Case Name:	Richtek v. uPI, AMD, Sapphire Technology, Diamond Multimedia, and XFX Technology
Represented:	Plaintiff
Disposition:	Prepared an expert report and a supplemental expert report; deposed twice (three days total); subsidiary respondents settled and exited the case during May 2010 – July 2010; main respondent uPI agreed on 21 July 2010 to a Consent Order that included a ten-year ban on importation of the accused products to avoid an ITC hearing.
Date:	January 2010 – July 2010; ITC enforcement proceeding opened against uPI and Sapphire, June 2011 – March 2012 (see above); follow-on district/superior court cases temporarily stayed, but pending.

Type of Matter:	Patent infringement and theft of trade secrets involving integrated circuit manufacturing
Law Firm:	Keker and Van Nest, LLP, San Francisco, California
Case Name:	TSMC v. SMIC
Represented:	Plaintiff
Disposition:	Deposed; testified at trial September 2009; jury returned guilty verdict on all 18 counts; parties settled during damages phase of trial.
Date:	July 2007 – September 2009.

Type of Matter:	Theft of Trade Secrets
Law Firm:	Baker & McKenzie, LLP, San Diego, California
Case Name:	Neology Inc. v. B. Roesner et al.
Represented:	Plaintiff
Disposition:	Reviewed materials produced during discovery and found considerable facially-labeled trade secret material in the possession of the defendant. Case Settled
Date:	April 2007 – May 2007

Type of Matter:	Theft of Trade Secrets
Law Firm:	Weil, Gotshal, and Manges, LLP, New York, New York
Case Name:	Synopsys v. Nassda

Represented:	Defendant
Disposition:	Wrote an expert report on behalf of defendant but was not deposed. Case Settled
Date:	September 2003 - August 2004

Type of Matter:	Theft of Trade Secrets
Law Firm:	Howrey, Simon, Arnold & White, LLP, Menlo Park, California
Case Name:	Silvaco, Inc. v. Circuit Semantics, Inc.
Represented:	Defendant
Disposition:	Wrote an expert report on behalf of defendant and was deposed. Case Settled
Date:	February 2003 - September 2003

Type of Matter:	Contract dispute, Copyright Infringement, and Theft of Trade Secret matter involving integrated circuit design tools
Law Firm:	Russo & Hale, LLP, Palo Alto, California
Case Name:	Virtual Silicon Technology, Inc. v. Library Technologies, Inc.,
Represented:	Plaintiff
Disposition:	On behalf of plaintiff, wrote an expert report, was deposed and testified at arbitration hearing. Decision of binding arbitration released in November 2003; all findings-of-fact in favor of the plaintiff.
Date:	December 2002 - November 2003

PUBLICATIONS

Books

1. D. Foty, "Moore's Law: The Untold Story," August 2017.

2. D. Foty, "The Rise and Fall of Classical Athens: A Short History," January 2018.

3. D. Foty, "Thomas Seebeck: His Life and Science," September 2018.

4. D. Foty, "Essential Digital, Analog, and Semiconductor Electronics Technology," Chapter 19 in *Concise Higher Electrical Engineering* (ed. by E. Chikuni, M. Khan, and O. Okoro), Juta Academic, 2008.

5. D. Foty, *MOSFET Modeling with SPICE: Principles and Practice*, Prentice-Hall (now Pearson Education), 1997 (now in its third printing; Vietnamese-language edition published in 2006).

6. Proceedings of the Symposium on Low Temperature Electronics and High Temperature Superconductors (ed. by S. Raider, C. Claeys, D. Foty, T. Kawai, and R. Kirschman) (published in October 1993).

7. Proceedings of the Symposium on Low Temperature Electronic Device Operation (ed. by D. Foty) (published in December 1991).

Guest Journal Editor

1. Guest editor, special issue on Low Voltage/Low Power Design, Analog Integrated Circuits and Signal Processing, December 1999.

Refereed Journal Publications

1. D. Foty, "Nanoscale Electron Devices: Difficulties, Granularities, and Applications" (Invited Paper), Romanian Journal of Information Sciences and Technology, (published by the Romanian Academy of Sciences), January 2009, vol. 12(3), pp. 317 – 338.

2. D. Foty, "An Evaluation of Deep-Submicron CMOS Design Optimized for Operation at 77K" (Invited Paper), Analog Integrated Circuits and Signal Processing vol. 49, pp. 97 – 105 (2006).

3. D. Foty and K. Runge, "What's Ahead in High-Speed Wireless Data Communications? The Future Will Be Better Tomorrow – And Different Than What We've Been Expecting" (Invited Paper), the African Journal of Information and Communications Technology (online publication).

4. S. Terry, J. Rochelle, D. Binkley, B. Blaylock, D. Foty, and M. Bucher, "Comparison of a BSIM3V3 and EKV MOST Model for a 0.5μm Process and Implications for Analog Circuit Design," IEEE Transactions on Nuclear Science vol. NS-50, pp. 915 - 920 (2003).

5. D. Binkley, C. Hopper, S. Tucker, B. Moss, J. Rochelle, and D. Foty, "A CAD Methodology for Optimizing Transistor Current and Sizing in Analog CMOS Design," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems vol. CAD-22, pp. 225 – 237 (2003).

6. D. Foty, "Perspectives on Analytical Modeling of Small Geometry MOSFETs in SPICE for Low Voltage/Low Power CMOS Circuit Design" (Invited Paper), Analog Integrated Circuits and Signal Processing vol. 21, pp. 229 – 252 (1999).

7. D. Foty, "Taking a Deep Look at Analog CMOS," IEEE Circuits and Devices, March 1999, pp. 23 – 28.

8. D. Foty, "MOSFET Modeling for Circuit Simulation: Where Do We Go From Here?," IEEE Circuits and Devices, July 1998, pp. 26 – 31.

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67. D. Foty, "MOS Modeling and SPICE: Are You an Educated Model Consumer?" (Conference Tutorial), presented at the Custom Integrated Circuits Conference, Santa Clara, California, 5 May 1997.

68. D. Foty, "The SPICE FET Models: Pitfalls and Prospects" (Conference Tutorial), presented at the Design Automation Conference, Las Vegas, Nevada, 5 June 1996.

69. D. Foty and E. Nowak, "Performance, Reliability, and Supply Voltage Reduction, with the Addition of Temperature as a Design Variable" (Invited Paper), presented at the Symposium on Low Voltage-Low Power Integrated Circuits, 1993 European Solid State Device Research Conference, Grenoble, France, 16 September 1993.

70. D. Foty and E. Nowak, "Performance/Reliability Trade-Off and Optimized nMOSFET Design for 77K CMOS Logic," presented at the Symposium on Low Temperature Electronics and High Temperature Superconductors, Honolulu, Hawaii, 20 May 1993.

71. D. Foty, "The Design of Deep Submicron FETs for Low Temperature Operation" (Invited Paper), presented at the Symposium on Low Temperature Electronics and High Temperature Superconductors, Honolulu, Hawaii, 20 May 1993.

72. D. Foty, H. Hanafi, P. Agnello, and H. Ho, "Mixed Schottky/p-n Junction Behavior in Diodes Produced by Outdiffusion from Polycrystalline Cobalt Disilicide," presented at the 1992 International Electron Devices Meeting, San Francisco, California, 16 December 1992.

73. D. Foty, "Low Temperature Electronics and Future Electron Devices (Invited Paper), presented at the Symposium on Low Temperature Electronic Device Operation, Washington, DC, 7 May 1991.

74. D. Foty, "Impurity Ionization in MOSFETs at Very Low Temperatures," presented at the First International Conference on Low Temperature Electronics, Berkeley, California, 24 April 1990.

75. D. Foty and T. Furukawa, "Behavior of an NMOS Trench Isolated Corner Parasitic Device at Low Temperature," presented at the Symposium on Low Temperature Electronics, Materials, and Processing, Hollywood, Florida, 17 October 1989.

76. D. Foty and S. Titcomb, "Freeze-Out and Field Dependent Ionization in MOSFETs at Very Low Temperatures," presented at the Symposium on Low Temperature Electronics and High Temperature Superconductors, Honolulu, Hawaii, 20 October 1987.

Co-Authored Conference Presentations

1. S. Sinha and D. Foty, "SiGe Technology for mm-Wave Applications," (Invited Conference Plenary Lecture), presented at the 13th Baltic Electronics Conference, Tallinn, Estonia, 3 October 2012.

2. B.C. Mabuza, S. Sinha and D. Foty, "On-chip Impedance Tuning for mm-Wave Applications," presented at the South African Conference on Semiconductor and Superconductor Technology, Stellenbosch, South Africa 8 April 2009.

3. S. Terry, J. Rochelle, D. Binkley, B. Blaylock, D. Foty, and M. Bucher, "Comparison of a BSIM3V3 and EKV MOST Model for a 0.5µm Process and Implications for Analog Circuit Design," presented at the IEEE Nuclear Science Symposium, Norfolk, Virginia, 15 November 2002.

4. M. Bucher, D. Kazazis, F. Krummenacher, D. Binkley, D. Foty, and Y. Papananos, "Analysis of Transconductances at All Levels of Inversion in Deep Submicron CMOS," presented at the 9th International Conference on Electronics, Circuits, and Systems, Dubrovnik, Croatia, 18 September 2002.

5. D. Binkley, M. Bucher, and D. Foty, "Design-Oriented Characterization of CMOS Over the Continuum of Inversion Level and Channel Length," presented at the 7th International Conference on Electronics, Circuits, and Systems, Kaslik, Lebanon, 18 December 2000.

6. G. Gildenblat, M. Bradford, and D. Foty, "A New MOS C-V Simulator for Low Temperature Applications," presented at the Symposium on Low Temperature Electronics and High Temperature Superconductors, Honolulu, Hawaii, 20 May 1993.

Conference Panel Participation

1. Member of Panel Discussion, 2nd Regional African Conference of the International Telecommunications Society, Lusaka, Zambia, 15 March 2018.

2. Member of Panel Discussion, 12th International Conference on Synthesis, Modeling, Analysis, and Simulation Methods and Applications to Circuit Design, Istanbul, Turkey, 7 September 2015.

3. Member of Panel Discussion, Future Wireless Telecommunications, "Telecosm," Lake George, New York, 16 October 2007.

4. Moderator of Panel Discussion, International Workshop on System-on-Chip, Banff, Alberta, Canada, 22 July 2005.

5. Member of Panel Discussion, Custom Integrated Circuits Conference, San Jose, California, 23 September 2003.

6. Co-moderator of Panel Discussion, Fabless Semiconductor Association Modeling Workshop, Santa Clara, California, 9 September 2002.

7. Member of Panel Discussion, Workshop on Compact Modeling, International Conference on the Modeling and Simulation of Microsystems, San Juan, Puerto Rico, 23 April 2002.

8. Member of Panel Discussion, "Vermont's High-Tech Future – Does it Have One?," Room 11, the Statehouse, Montpelier, Vermont, 26 April 2001.

9. Member of Panel Discussion, Fabless Semiconductor Association Quarterly Meeting, San Jose, California, 5 September 1999.

10. Member of Panel Discussion, Fabless Semiconductor Association Modeling Workshop, San Jose California, 24 May 1999.

11. Member of Panel Discussion, Symposium on Low Voltage-Low Power Integrated Circuits at the 1993 European Solid State Device Research Conference, Grenoble, France, 16 September 1993.

12. Member of Panel Discussion, Symposium on Low Temperature Electronics and High Temperature Superconductors, Honolulu, Hawaii, 19 May 1993.

Invited Seminars/Lectures

1. "Digital Semiconductor Electronics: Why It Happened, And Where It's Going," short course hosted by the University of Pretoria, Pretoria, South Africa, 15 August 2011.

2. "The Untold Story of 'Moore's Law': *Why* It Happened," short course hosted at the summer school of the Universitatea Politehnica Bucureşti, held in Iaşi, Romania, 4 – 5 July 2011.

3. "Some Background Thoughts On mm-Wave Radio Technology," seminar presented at the University of Pretoria, Pretoria, South Africa, 17 August 2010.

4. "Digital Semiconductor-Based Electronics: Why It Became A Juggernaut," short course hosted by the University of Pretoria, Pretoria, South Africa, 16 August 2010.

5. “Some Thoughts On mm-Wave Radio Technology,” short course hosted at the summer school of the Universitatea Politehnica Bucureşti, held in Oradea, Romania, 13 July 2010.

6. “Silicon-Based Semiconductor Electronics – How It Came To Dominate,” short course hosted at the summer school of the Universitatea Politehnica Bucureşti, held in Oradea, Romania, 12 July 2010.

7. “The Powerful Entropy Challenge: Dealing With Power Consumption,” presented at the IEEE South Africa Section Meeting, Pretoria, South Africa, 18 August 2009.

8. "Digital CMOS Electronics: The Background Story," short course hosted by the University of Pretoria, Pretoria, South Africa, 17 August 2009.

9. “An Overview of mm-Wave Radio Technology,” short course hosted at the summer school of the Universitatea Politehnica Bucureşti, held in Iaşi, Romania, 13 July 2009.

10. “Modern Electronics: How We Got Here,” short course hosted at the summer school of the Universitatea Politehnica Bucureşti, held in Iaşi, Romania, 13 July 2009.

11. “Prospects for mm-Wave Radio Technology: An Overview,” short course hosted at the summer school of the Universitatea Politehnica Bucureşti, held in Oradea, Romania, 22 July 2008.

12. “Into the NanoSmall: The Unexpected Challenges,” short course hosted at the summer school of the Universitatea Politehnica Bucureşti, held in Oradea, Romania, 22 July 2008.

13. “A Concise History of Modern Electron Devices,” short course hosted at the summer school of the Universitatea Politehnica Bucureşti, held in Oradea, Romania, 22 July 2008.

14. "Issues In mm-Wave Radio Systems: Prospects and Challenges," short course hosted by the University of Pretoria, Pretoria, South Africa, 8 May 2008.

15. "Prospects for mm-Wave Radio Technology: An Executive Summary for Decision-Makers," presented at the IEEE Region 8 meeting, University of Pretoria, Pretoria, South Africa, 8 May 2008.

16. “The MOS Transistor, On a Tourist Visa,” short course hosted at the summer school of the Universitatea Politehnica Bucureşti, held in Iaşi, Romania, 16 July 2007.

17. “Semiconductor Electronics: Some Fundamental Background,” short course hosted at the summer school of the Universitatea Politehnica Bucureşti, held in Iaşi, Romania, 16 July 2007.

18. "The MOS Transistor and CMOS Technology: Past, Present, and Future," short course hosted by Tallinn University of Technology, Tallinn, Estonia, 13 – 14 November 2006.

19. "New Directions in Technology for High-Speed Wireless Data Communications," seminar presented at the Universitatea Politehnica Bucureşti, Bucharest, Romania, 28 July 2006.

20. "The MOS Transistor and CMOS Technology: History as a Guide to the Future," short course hosted at the summer school of the Universitatea Politehnica Bucureşti, held in Braşov, Romania, 25 July 2006.

21. "The Underpinnings of the MOS Transistor and CMOS Technology in the 21st Century - Scaling Theory and New Methods in Analog/RF Design," short course hosted by l'École Polytechnique de Montréal, Montréal, Québec, Canada; sponsored by ReSMiQ and the local IEEE Solid State Circuits Society chapter, 27 October 2005.

22. "The Underpinnings of the MOS Transistor and CMOS Technology in the 21st Century – Scaling Theory and New Methods in Analog/RF Design," short course hosted by the Department of Electrical, Electronic, and Computer Engineering, University of Pretoria, Pretoria, South Africa, and sponsored by the IEEE South Africa Section, 9 – 10 May 2005.

23. "What's Ahead in High-Speed Wireless Data Communications? The Future Will Be Better Tomorrow – And Different Than What We've Been Expecting," seminar presented at the Department of Electrical Engineering, University of Cape Town, Cape Town, South Africa, 7 May 2005.

24. "Low Temperature CMOS: A Bad Idea Whose Time Has (Finally) Come?", seminar presented at the Department of Computer-Aided Design, L'viv Polytechnic National University, L'viv, Ukraine, 28 February 2005.

25. "The Underpinnings of the MOS Transistor and CMOS Technology in the 21st Century – Scaling Theory and New Methods in Analog/RF Design," Full-day "Eurotraining" course, held at the Danish Technical University, Lyngby, Denmark, 27 October 2004.

26. "The Underpinnings of the MOS Transistor and CMOS Technology in the 21st Century – Scaling Theory and New Methods in Analog/RF Design," Full-day "Eurotraining" course, held at the Politechnico di Torino, Turin, Italy, 25 October 2004.

27. "CMOS Scaling and Low Temperature CMOS: A Bad Idea Whose Time Has Come?", seminar presented at the Department of Electrical and Computer Engineering, Oakland University, Auburn Hills, Michigan, 25 March 2004.

28. "Modernizing the Interpretation of the MOS Transistor for the 21st Century: Generalized Methods and Their Extension to Nanotechnology," presented at the IEEE Southeast Michigan Spring Section Meeting, Auburn Hills, Michigan, 24 March 2004.

29. "Re-Interpreting the MOS Transistor for the 21st Century: Generalized Methods and Their Extension to Nanotechnology," seminar presented at Tallinn Technical University, Tallinn, Estonia, 13 November 2003.

30. "Re-Interpreting the MOS Transistor for the 21st Century: Generalized Methods and Their Extension to Nanotechnology," seminar presented at Helsinki University of Technology, Espoo, Finland, 7 November 2003.

31. "A Practical Examination of MOS Transistor Model 'Accuracy' in Modern CMOS Technology," presented at the MOS Arbeitskreis Meeting, Crolles, France, 5 May 2003.

32. "Building a New Framework for Deep Submicron Analog/RF CMOS Design – and Beyond," invited seminar presented at the Department of Electrical Engineering, Columbia University, New York, New York, 25 April 2003.

33. "A New Framework for Deep Submicron Analog/RF CMOS Design – and Beyond," seminar presented at the Department of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, Georgia, 20 March 2003.

34. "Starting Over: Modernizing the Framework for Deep Submicron Analog CMOS Design," seminar presented at the Nokia Research Center, Helsinki, Finland, 29 November 2002.

35. "Modernizing the Framework for Deep Submicron Analog CMOS Design," Distinguished Guest Lecturer, IEEE Baltic Region Meeting (sponsored by Tallinn Technical University), Sagadi, Estonia, 19 – 20 August 2002.

36. "Modernizing the Framework for Deep Submicron Analog CMOS Design," seminar presented at Helsinki University of Technology, Espoo, Finland, 16 August 2002.

37. "gm/Id-Based MOSFET Modeling and Modern Analog Design," presented at the MOS Arbeitskreis Meeting, Ünterpremstatten, Austria, 19 November 2001.

38. "MOS Modeling and Analog Circuit Design," lecture as part of "Practical Aspects of Analog Design," professional short course sponsored by Mead Microelectronics, San Francisco, California, 13 November 2001.

39. "MOS Modeling and Analog Circuit Design," lecture as part of "Transistor-Level Analog IC Design," professional short course sponsored by Mead Microelectronics, Lausanne, Switzerland, 10 October 2001.

40. "Please Stop Imitating Us!' – An Engineer Looks at the (Unstable) State of the Humanities," presented at a meeting of the National Association of Scholars, Burlington,Vermont, 14 July 2001.

41. "Introduction to the Fabless Semiconductor Association (FSA) and the Modeling Committee Activities," presented at the MOS Arbeitskreis Meeting, Munich, Germany, 5 March 2001.

42. "The EKV MOSFET Model: A MOS Model of, by, and for Analog Designers," presented at Broadcom Corp., Irvine, California, 30 November 2000.

43. "Modeling and Simulation for Mixed-Signal IC Design," lecture as part of "Transistor-Level Analog IC Design," professional short course sponsored by Mead Microelectronics, Lausanne, Switzerland, 27 September 2000.

44. "MOS Models as a Factor in the Quality of Electronic Design," presented at the Rockwell Scientific Center, Thousand Oaks, California, 17 March 2000.

45. "MOS Models as a Factor in the Quality of Electronic Design," presented at Micron Technology, Inc., Boise Idaho, 4 March 2000.

46. "Modeling and Simulation for Mixed-Signal IC Design," lecture as part of "Practical Aspects of Analog and Mixed-Signal ICs," professional short course sponsored by Mead Microelectronics, Monterey, California, 3 February 2000.

47. "Modeling and Simulation for Mixed-Signal IC Design," lecture as part of "Transistor-Level Analog IC Design," professional short course sponsored by Mead Microelectronics, Lausanne, Switzerland, 30 September 1999.

48. "AC Simulation Aspects of MOS Modeling," presented at the Fabless Semiconductor Association Modeling Workshop, San Jose, California, 25 May 1999.

49. D. Foty, M. Bucher, and C. Enz, "The EKV MOSFET Model – A MOS Model for the Analog Designer," presented at the Fabless Semiconductor Association Modeling Workshop, San Jose, California, 25 May 1999.

50. Several lectures on MOS device physics, modeling, and analog design, presented at Mentor Graphics, Heliopolis, Cairo, Egypt, 5 – 8 May 1999.

51. "A Brief History of MOS Modeling (or, How We Got In This Mess In the First Place)," presented at Philips Research Laboratories, Eindhoven, The Netherlands, 24 March 1999.

52. "An Overview of MOS Modeling for SPICE Circuit Simulation," presented at Mitel Corporation, Bromont, Québec, Canada, 2 February 1999.

53. "Modeling and Simulation for Mixed-Signal IC Design," lecture as part of "Practical Aspects of Analog and Mixed-Signal ICs," professional short course sponsored by Mead Microelectronics, Monterey, California, 12 December 1998.

54. "MOS Modeling Challenges for Deep Submicron CMOS," lecture presented as part of "Deep Submicron CMOS Design," professional short course sponsored by Mead Microelectronics, Lausanne, Switzerland, 12 October 1998.

55. "Modeling the Temperature-Dependent Characteristics of MOSFETs for Circuit Simulation," presented at the Electronic Parts Selection and Management Workshop, Center for the Analysis of Life-Cycle Engineering, University of Maryland, College Park, Maryland, 17 June 1998.

56. "A Primer on Trench Isolation Technology (or, Why Do Process Engineers Hate Circuit Designers?)," presented at the Fabless Semiconductor Association Modeling Subcommittee Meeting, Opti, Inc., Milpitas, California, 12 May 1998.

57. C. Enz, M. Bucher, and D. Foty, "The EKV MOSFET Model for Analog and Mixed-Mode Circuit Design," satellite broadcast class, National Technological University (hosted by North Carolina State University, Raleigh, North Carolina), 30 April 1998.

58. "MOS Modeling Challenges for Deep Submicron CMOS Circuit Simulation," presented at Digital Equipment Corporation, Hudson, Massachusetts, 13 April 1998.

59. "Challenges for 0.25µm CMOS Circuit Design: Scaling, MOS Modeling, and Complexity," presented at CERN, Geneva, Switzerland, 6 February 1998.

60. "MOS Modeling Challenges for Deep Submicron CMOS," lecture presented as part of "Deep Submicron CMOS Design," professional short course sponsored by Mead Microelectronics, Monterey, California, 11 December 1997.

61. C. Enz, M. Bucher, and D. Foty, "The EKV MOSFET Model for Analog and Mixed-Mode Circuit Design," one-day short course sponsored by the Fabless Semiconductor Association, San Jose, California, 8 November 1997.

62. "MOS Modeling Issues in the Emerging Analog and Low Power Era," presented Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan, 27 August 1997.

63. "Current Problems in MOSFET Modeling for Analog Circuit Simulation," presented at Level One Communications, Inc., Sacramento, California, 9 August 1997.

64. Guest lecturer, Centre National pour les Récherches Scientifique (CNRS) Summer Lecture Series, La Londe des Maures, France, 23 – 28 June 1997.

65. "MOSFET Modeling and Analog Circuit Design," presented at the Centre National pour les Récherches Scientifique (CNRS) Summer Lecture Series, La Londe des Maures, France, 27 June 1997.

66. "Benchmarking and Pre-Screening SPICE FET Models for Circuit Simulation Usage," presented at the Fabless Semiconductor Association Modeling Subcommittee Meeting, Adaptec, Inc., Milpitas, California, 6 May 1997.

67. "Benchmarking and Pre-Screening SPICE FET Models for Circuit Simulation Usage," presented at Cirrus Logic, Inc., Fremont, California, 6 May 1997.

68. "MOSFET Modeling and SPICE: Are You an Educated Model Consumer?," presented at Cirrus Logic, Inc., Fremont, California, 6 May 1997.

69. "MOS Modeling and SPICE: Are You an Educated Model Consumer?," satellite broadcast class, National Technological University (hosted by North Carolina State University, Raleigh, North Carolina), 21 April 1997.

70. "An Overview of the SPICE FET Modeling Infrastructure" lecture presented as part of "Modeling and Simulation of MOS Analog ICs," professional short course sponsored by Mead Microelectronics, Lausanne, Switzerland, 18 February 1997.

71. "An Overview of the SPICE FET Modeling Infrastructure" lecture presented as part of "Modeling and Simulation of MOS Analog ICs," professional short course sponsored by Mead Microelectronics, Monterey, California, 12 December 1996.

72. "Analytical MOSFET Modeling and SPICE - Past, Present, and Future", seminar presented at the Department of Electrical Engineering, Ohio State University, Columbus, Ohio, 9 May 1995.

73. "Constraints on CMOS Technology for Low Voltage/Low Power Applications", seminar presented at the Department of Electrical Engineering, Ohio State University, Columbus, Ohio, 8 May 1995.

74. "Submicron FET Design: Physical Considerations and Technological Choices", seminar presented at the Electrical Engineering Department, University of Hawaii, Honolulu, Hawaii, 24 May 1993.

75. "Aspects of the Design of Deep Submicron FETs for CMOS Operation at 300K and 77K", seminar presented at the Department of Electrical Engineering, Pennsylvania State University, University Park, Pennsylvania, 10 November 1992.

PROFESSIONAL AFFILIATIONS & AWARDS

Honorary Member of the Applied Radio Electronics Science Academy of Ukraine

Senior Member, The Institute of Electrical and Electronic Engineers (IEEE); and of the Electron Devices, Lasers and Electro-Optics, Circuits and Systems, and Communications Societies of the IEEE.

Reviewer/evaluator of funding proposals, Natural Science and Engineering Research Council of Canada, 1991 - present.

Reviewer/evaluator of funding proposals, California MICRO program, 2001 - present.

Reviewer/evaluator of funding proposals, National Research Foundation of South Africa, 2007- present.

Industrial and Academic Mentoring

Member of the Advisory Board, Department of Electrical, Electronic & Computer Engineering, University of Pretoria, South Africa, 2012 – present.

Advisor to the Tshwane University of Technology, Pretoria, South Africa, 2007 - present.

Advisor to the University of Pretoria, Pretoria, South Africa, 2005 – present.

Advisor to the Tallinn University of Technology, Tallinn, Estonia, 2004 – present.

Industrial Mentor for "Development and Applications of a New MOS C-V Simulator for the 2 - 300K Temperature Range" (Professor Gennady Gildenblat, Principal Investigator, Department of Electrical Engineering, Pennsylvania State University, University Park, Pennsylvania), funded by the IBM Shared University Research Contract program, calendar year 1992.

Committees/Conferences

1. Member of the Organizing Committee, and Chair of the Track on Electromagnetics and Antennas, Africon 2011, Victoria Falls, Zambia, September 2011.

2. Member of the Organizing Committee, and Chair of the Track on Electron Devices and Circuits, Africon 2009, Nairobi, Kenya, September 2009.

3. Session Chair, 31st International Conference on Semiconductor Physics, Sinaia, Romania, 14 October 2008.

4. Session Chair, Africon 2007, Windhoek, Namibia, 27 September 2007.

5. Session Chair, 13th International Conference on the Mixed Design of Integrated Circuits and Systems, Gdynia, Poland, 24 June 2006.

6. Session Chair, International Workshop on System-on-Chip, Banff, Alberta, Canada, 22 July 2005.

7. Session Chair, 7th International Symposium on Signals, Circuits, and Systems, 4Iaşi, Romania, 15 July 2005.

8. Member of the Scientific Committee, European Conference on Circuit Theory and Design (ECCTD), 2005.

9. Special Session Organizer, 12th International Conference on the Mixed Design of Integrated Circuits and Systems, Krakow, Poland, 22 - 25 June 2005.

10. Special Session Organizer, International Symposium on Industrial Electronics, Dubrovnik, Croatia, 20 – 23 June 2005.

11. Session Chair, 12th International Conference on Telecommunications, Cape Town, South Africa, 4 – 6 May 2005.

12. Session Chair, 11th International Conference on Electronics, Circuits, and Systems, Tel Aviv, Israel, 13 - 15 December 2004.

13. Session Chair, the 12th International Symposium on Electron Devices for Microwave and Optoelectronic Applications, Berg-en-Dal, Kruger National Park, South Africa, 8 - 9 November 2004.

14. Member of the International Program Committee, International Conference on Mixed Design of Integrated Circuits and Systems, 2004 – present.

15. Member of the Technical Program Committee, International Symposium on Signals, Circuits, and Systems, 2004 – present.

16. Special Session Organizer, 11th International Conference on Electronics, Circuits, and Systems, Tel Aviv, Israel, 13 – 15 December 2004.

17. Session Chair, 4th Electronic Circuits and Systems Conference, Bratislava, Slovakia, 11 – 12 September 2003.

18. Member of the Scientific Committee, European Conference on Circuit Theory and Design (ECCTD), 2003.

19. Session Chair, 9th International Conference on Electronics, Circuits, and Systems, Dubrovnik, Croatia, 16 - 18 September 2002.

20. Member, Analog Signal Processing Technical Committee, IEEE Circuits and Systems Society, 2002 – present.

21. Member, Program Committee, Analog Circuits and Signal Processing, International Symposium on Circuits and Systems (ISCAS), 2002 – present.

22. Session Chair, International Symposium on Quality Electronic Design, San Jose, California (ISQED), 18 – 20 March 2002.

23. Chairman, Modeling Subcommittee, Fabless Semiconductor Association, 2001 – 2003.

24. Chairman, Fabless Semiconductor Association Modeling Workshop, 2001 – present.

25. Member of Technical Program Committee, European Conference on Circuit Theory and Design (ECCTD), 2001.

26. Member, IEEE Advisory Committee, 2001 – present.

27. Member of the Organizing Committee, International Symposium on Quality Electronic Design (ISQED), 2000 – 2002.

28. Member of the Modeling Committee, International Symposium on Quality Electronic Design (ISQED), 2000 – 2002.

29. Chairman of the Modeling Committee, International Symposium on Quality Electronic Design (ISQED), 2001.

30. Session Chair, International Symposium on Quality Electronic Design, San Jose, California (ISQED), 26 – 28 March 2001.

31. Lead Organizer, Fabless Semiconductor Association Workshop, 2000 – present.

32. Member of the MOS Arbeitskreis, 2000 – present.

33. Co-Chairman, Modeling Subcommittee, Fabless Semiconductor Association, 1999 – 2000.

34. Member of the Executive Committee, Modeling Subcommittee, Fabless Semiconductor Association, 1998 – present.

35. Member, Modeling Subcommittee, Fabless Semiconductor Association, 1996 – present.

36. Organizer, Symposium on Low Temperature Electronics and High Temperature Superconductors, Honolulu, Hawaii, 16 - 21 May 1993.

37. Organizer, Symposium on the Physics and Fabrication of Semiconductor Nanostructures, Washington DC, 5 - 10 May 1991.

38. Lead Organizer, Symposium on Low Temperature Electronic Device Operation, Washington DC, 5 - 10 May 1991.

39. Co-Chaired the Symposium on Low Temperature Electronics, Materials, and Processing, Hollywood, Florida, 17 October 1989.