Trials@uspto.gov
571-272-7822

Paper 10
Entered: November 7, 2024

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APTIV SERVICES US, LCC,
Petitioner,

v.

MICROCHIP TECHNOLOGY INC.,
Patent Owner.

IPR2024-00803
Patent 7,564,665 B2

Before BRIAN J. McNAMARA and CHRISTOPHER L. OGDEN, and JASON M. REPKO, *Administrative Patent Judges*.

REPKO, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Aptiv Services US, LLC ("Petitioner") filed a petition requesting *inter partes* review of claims 1–18 of U.S. Patent No. 7,564,665 B2 (Ex. 1001, "the '665 patent"). Paper 2 ("Pet."). Microchip Technology Inc. ("Patent Owner") filed a Preliminary Response. Paper 9 ("Prelim. Resp.").

To institute an *inter partes* review, we must determine "that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a). For the reasons discussed below, Petitioner has not shown a reasonable likelihood that it would prevail with respect to any claim challenged in the Petition. Thus, we do not institute an *inter partes* review.

A. Related Matters

According to the parties, the '665 patent has been asserted in *Microchip Technology Inc. v. Aptiv Services US, LLC*, No. 23-cv-778-JDW (DED). Pet. 97; Paper 3, 1 (Mandatory Notices).

B. The '665 Patent

The challenged patent relates to protecting integrated circuits (ICs) against damage from an electrostatic discharge (ESD). Ex. 1001, 1:6–9. For example, a build-up of static charge near the IC can lead to a short discharge of very high current. *Id.* at 1:22–26. This can damage an IC or cause it to malfunction. *Id.* at 1:22–28.

The challenged patent purports to reduce the maximum voltage that may develop in the system from an ESD event. *Id.* at 2:29–35. In particular, an IC has several digital Input/Output (I/O) pads. *Id.*, Abst. All I/O pads in the system have an output buffer with an output PMOS device that responds to an ESD event by charging a pad capacitance. *Id.* at 3:44–50. By configuring all pads in this way, the ESD energy is shared by the respective

pad capacitances, which reduces the maximum voltage developed in the system from the event. *Id.* at 3:50–56.

C. Claims

Of the challenged claims, three are independent: claims 1, 6, and 14. Those claims are reproduced below.

> 1. A pad circuit configured to provide protection against electrostatic discharge (ESD) in a system comprising the pad circuit, the pad circuit comprising:
>
> a first node coupled to a first voltage rail;
>
> a second node coupled to a physical pad having capacitance;
>
> one or more output transistor devices coupled between the first node and the second node, and operable to at least partially drive an output signal at the second node;
>
> a control block configured, to turn on, when instructed, at least one of the one or more output transistor devices to charge the pad capacitance to reduce a maximum voltage developed in the system as a result of the ESD event;
>
> a clamp device configured between a second voltage rail and a third voltage rail to reduce, when turned on, the maximum voltage developed in the system as the result of the ESD event;
>
> enable circuitry configured to turn on the clamp device and instruct the control block to turn on the at least one of the one or more output transistor devices, in response to the ESD event;
>
> wherein the second voltage rail is configured to provide power to the enable circuitry, and wherein the third voltage rail has a value below the first voltage rail.

Ex. 1001, 6:29–52.

6. A circuit configured to provide protection against electrostatic discharge (ESD) in a system comprising the circuit, the circuit comprising:

an output buffer configured to couple to a physical pad having capacitance, to drive at least one output signal at the physical pad;

a control block configured to control the output buffer;

a clamp device coupled between a first supply rail and a low supply rail, wherein the clamp device is configured to absorb, when turned on, a portion of an energy generated by the ESD event, to reduce the maximum voltage developed in the system as the result of the ESD event; and

a control circuit configured to instruct the control block to activate at least a portion of the output buffer when an ESD event occurs, to charge the pad capacitance to reduce a maximum voltage developed in the system as a result of the ESD event, wherein the control circuit is further configured to turn on the clamp device in response to the ESD event;

wherein the first supply rail is configured to provide power to the control circuit.

Id. at 7:3–24.

14. A system comprising:

one or more pads, each pad comprising:

a respective physical pad having respective capacitance;

a respective clamp device configured to absorb, when turned on, a portion of an energy generated by an ESD event, to thereby further reduce the maximum voltage developed in the system as the result of the ESD event; and

a respective pad circuit comprising:

a respective output buffer coupled to the respective physical pad, and operable to drive at least one respective output signal at the respective physical pad; and

respective control circuitry operable to: activate at least a portion of the respective output buffer in response to an ESD event to charge the respective pad capacitance to reduce a maximum voltage developed in the system as a result of the ESD event; and

turn on the clamp device in response to the ESD event.

Id. at 8:13–33.

D. Evidence

Name	Reference	Exhibit No.
Verhaege	US 6,529,359 B1, issued Mar. 4, 2003	1004
Ker	US 6,249,410 B1, issued June 19, 2001	1005
Miller	US 7,589,945 B2, issued Sept. 15, 2009	1006

E. Asserted Grounds

Petitioner asserts that claims 1–18 are unpatentable on the following grounds. Pet. 11.

Claims Challenged	Pre-AIA[1] 35 U.S.C. §	Reference(s)/Basis
1–18	103(a)	Verhaege
1–18	103(a)	Verhaege, Miller
1–18	103(a)	Ker

[1] Congress amended §§ 102 and 103 when it passed the Leahy-Smith America Invents Act (AIA). Pub. L. No. 112–29, § 3(c), 125 Stat. 284, 287 (2011). Petitioner argues the prior art qualifies under the pre-AIA version. Pet. 10–11. We agree. Here, the '665 patent was granted based on Application No. 11/621,724, filed on January 10, 2007. Ex. 1001, code (22).

II. ANALYSIS

A. Level of Ordinary Skill in the Art

According to Petitioner, "A person of ordinary skill in the art ('POSITA') in the field of the '665 patent in 2007 would have at least a Master's degree in electrical engineering, computer engineering, or a related field and three to five years of experience in integrated circuit design." Pet. 10 (citing Ex. 1002 ¶ 51).

Patent Owner argues that Petitioner's definition is "excessively high." Prelim. Resp. 3 n.1. In Patent Owner's view, "a POSITA would have had a bachelor's degree in electrical engineering or an equivalent technical degree and two years of experience in mixed-signal (i.e., analog/digital) circuit design." *Id.* (citing Ex. 2003 ¶¶ 30–34).

We need not resolve this dispute because our decision would be the same under either definition.

B. Claim Construction

The Board is required to construe only the terms in controversy and only to the extent necessary to resolve the controversy. *Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (citing *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

In Patent Owner's view, "the claims require sharing ESD charge from one pad ***with a different I/O pad***." Prelim. Resp. 27. Patent Owner argues that charge sharing is the only way that charging the pad capacitance can reduce a maximum voltage, as recited. *Id.* at 24–25.

Apart from the charge sharing, Patent Owner argues that the recited enable or control circuitry is not located in the circuit where the ESD event occurs. *Id.* at 27–33. Patent Owner argues that Petitioner disagrees with this interpretation. *Id.*

Petitioner does not propose a construction for any terms. Pet. 10. Petitioner, though, argues that it would have been obvious to duplicate Verhaege's and Ker's protection circuits. *See, e.g.*, *id.* at 18 (discussing claim 1 and Verhaege), 48 (discussing the Verhaege-Miller combination), 66 (discussing claim 1 and Kerr). For example, Petitioner argues that "a POSITA would have been motivated to use the improved protection circuit of Verhaege, apply it at every I/O pad, and *share the ESD energy* across multiple pad circuits as taught by Miller." *See id.* at 48 (emphasis added). From statements like these, Patent Owner draws the conclusion that Petitioner must also be interpreting the claims to require charge sharing. Prelim. Resp. 25–27.

For the reasons discussed in Section II.C below, Petitioner has not shown a reasonable likelihood of showing that any claims are unpatentable even under the implied claim construction used in its obviousness rationale. The Board need not expressly construe any claims in reaching that conclusion.

C. Petitioner's Challenges

1. Obviousness: Verhaege

Petitioner asserts that claims 1–18 are unpatentable as obvious over Verhaege alone. Pet. 11.

a. Claims 1, 6, and 14

i. Verhaege

Verhaege describes a circuit for protecting an output-driver transistor from an ESD event. Ex. 1004, 1:33–38. In particular, the circuit turns off an output driver during electrical overstress and electrostatic stress (EOS/ESD). *Id.* at 1:9–13. To do this, Verhaege uses a dynamically triggered clamp that

grounds an output-driver transistor's gate during the EOS/ESD. *Id.* at 4:44–46.

ii. Control Circuitry in Claims 1, 6, and 14

The independent claims recite an ESD event and circuitry responding to it. In particular, claim 1 recites, in part,

> a control block configured, to turn on, when instructed, at least one of the one or more output transistor devices to charge the pad capacitance to reduce a maximum voltage developed in the system *as a result of the ESD event*.

Ex. 1001, 6:29–49 (emphasis added). Claim 6 recites, in part,

> a control circuit configured to instruct the control block to activate at least a portion of the output buffer *when an ESD event occurs*, to charge the pad capacitance to reduce a maximum voltage developed in the system as a result of the ESD event.

Id. at 7:3–22 (emphasis added). Claim 14 recites, in part,

> respective control circuitry operable to: activate at least a portion of the respective output buffer *in response to an ESD event* to charge the respective pad capacitance to reduce a maximum voltage developed in the system as a result of the ESD event.

Id. at 8:13–31 (emphasis added).

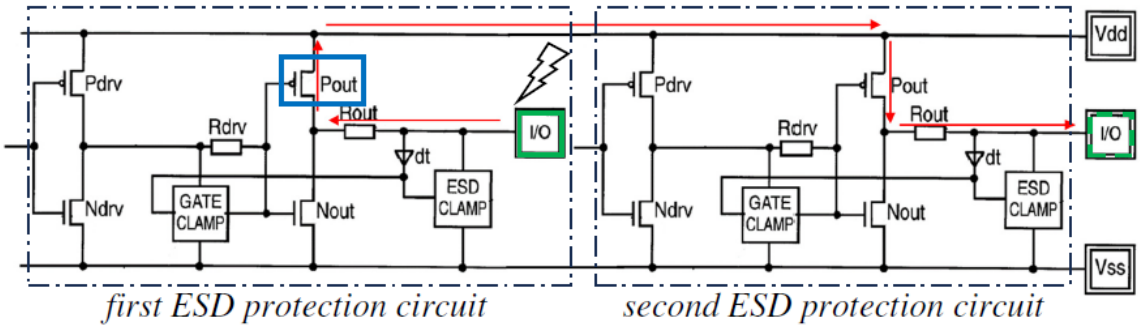
iii. Petitioner's Two-Circuit Diagram

In the obviousness rationale based on Verhaege alone, Petitioner assumes that the claims require multiple pads, each having its own control block (claim 1):

> Verhaege renders obvious "charg[ing] the pad capacitance to reduce a maximum voltage developed in the system as a result of the ESD event." Although Verhaege discloses *a single pad circuit*, most integrated circuits had multiple I/O pads by at least 2007. (EX-1002 ¶ 67.) It would have been obvious to a POSITA that, because an ESD event could occur at any I/O pad, the Verhaege invention should be *repeated at every I/O pad*.

Pet. 18 (citing Ex. 1002 ¶ 67) (emphasis added). Petitioner relies on the same reasoning for claims 6 and 14. *See. id.* at 31 (arguing in the challenge to claim 6 that "a POSITA would repeat the Verhaege circuit at every I/O pad to protect the entire circuit from ESD"); *id.* at 43 (arguing in the challenge to claim 14 that "a POSITA would include the Verhaege circuit at every I/O pad").

Petitioner created the figure below to illustrate its obviousness rationale. *Id.* at 18.



This figure shows a first ESD-protection circuit receiving the ESD event (lightning bolt). *Id.* The energy from the ESD event (red) flows from the first pad (green) to a second circuit with a second pad (green). *Id.* Petitioner highlights the output transistor on the first ESD-protection circuit in dark blue. *Id.* at 18. Petitioner argues that, like the enable circuitry recited in claim 1, the gate clamp is configured to turn on an output transistor. *Id.* at 17. Petitioner adds a red line from the first circuit to the second to show how the ESD energy is shared in the system. *Id.* at 18.

iv. Patent Owner's Preliminary Response

Consistent with Petitioner's obviousness rationale, Patent Owner argues that the claims require charge sharing between two pads. *See* Prelim. Resp. 25–27. Patent Owner argues that charge sharing is the only way that charging the pad capacitance can reduce a maximum voltage, as recited. *Id.*

at 24–25. According to Patent Owner, it is impossible to reduce the recited maximum voltage by charging the I/O pad that received the ESD event. *Id.* (citing Ex. 2003 ¶¶ 85–88). Patent Owner argues that Petitioner agrees with its view, citing Petitioner's initial invalidity contentions in the parallel district-court case (*see supra* Section I.A). *Id.* at 26–27 (citing Ex. 2001, 25). According to Petitioner's initial invalidity contentions, "The pad capacitance of the circuit that serves as the entry point for the ESD charge would already be fully saturated by the incoming ESD charge and activation of the control circuitry would not be able to charge the pad capacitance further." Ex. 2001, 27.

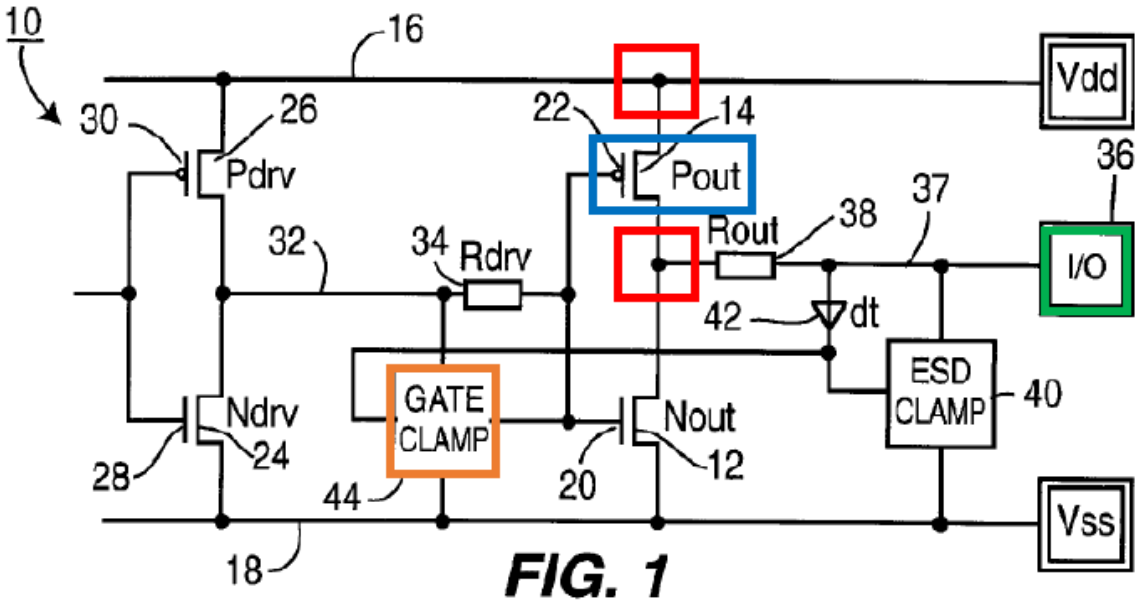
Patent Owner disagrees that Petitioner's proposed two-circuit combination (Pet. 18) teaches or suggests the claimed subject matter because Patent Owner argues that output transistor (dark blue) is in the same circuit as the ESD (as indicated by the lightning bolt)—the first ESD-protection circuit on the left. *See* Prelim. Resp. 25–27. According to Patent Owner, the ESD event and the output transistor must correspond to different pads. *Id.*

v. The Two-Circuit Obviousness Rationale

We agree with Patent Owner that Petitioner has not shown that its two-circuit system teaches or suggests the subject matter recited in claims 1, 6, and 14.

To address the pad and control circuitry, Petitioner relies on control circuitry on the first circuit and the I/O pad in the second circuit: "The ESD energy flows from the first I/O pad to the Vdd rail, increasing its voltage and *charging the capacitance of the second I/O pad.*" Pet. 18 (emphasis added). This explanation suggests that Petitioner's proposed two-circuit system relies on components in different circuits—that is, a transistor from the first and a I/O pad from the second. *See id.*

The rest of Petitioner's challenge, though, refers to Verhaege's single circuit having both the control circuitry and I/O pad. *See id.* at 13–17, 19–24. For example, Petitioner annotates Verhaege's Figure 1 to explain how gate clamp 44 in a single circuit turns on transistor 14. *Id.* at 17.



This annotated figure shows gate clamp 44 (orange) connected to output transistor 12 and output transistor 14 (blue). *Id.* (citing Ex. 1004, 2:23–25). Here, Petitioner argues, "In response to an ESD event, gate clamp 44 connects the gates of both output transistors to ground, which turns off NMOS transistor 12 and turns on PMOS transistor 14." *Id.* (citing Ex. 1004, 2:23–25, 2:32–37; Ex. 1002 ¶ 65). Petitioner maps I/O pad 36 (green) to the recited "physical pad having capacitance." *Id.* at 15 (citing Ex. 1002 ¶ 61). That is, unlike the two-circuit rationale, all the components are on the same pad, and the ESD event occurs on that pad. *Id.* at 17.[2]

[2] Although not made explicit in the challenge to claim 1 based on Verhaege, Petitioner asserts that gate clamp 44 performs part of the control block's function (Pet. 18), and in its challenge based on Verhaege and Miller, Petitioner states that Verhaege's control block corresponds to gate clamp 44, referring to pages 16 through 18 of the Petition. *Id.* at 49. Gate clamp 44 is

Petitioner does not argue that this single-circuit design discloses "charg[ing] the pad capacitance to reduce a maximum voltage developed in the system as a result of the ESD event." *See id.* at 17–18. So the single-circuit mapping does not appear to be an alternative to the two-circuit rationale. Rather, Petitioner explains that charge sharing would have been obvious, relying on the two-circuit system for this feature. *Id.* at 18. By relying on a single-circuit design for some limitations and a two-circuit design for others, Petitioner presents multiple contradictory theories for how Verhaege teaches or suggests the claimed circuit. *See id.* at 17–18. Thus, Petitioner has not sufficiently explained how the control block in the two-circuit configuration is "configured, to turn on, when instructed, at least one of the one or more output transistor devices to charge the pad capacitance to reduce a maximum voltage developed in the system as a result of the ESD event," as recited in claim 1.

Petitioner's rationale for claims 6 and 14 are deficient in the same way. *See Id.* at 31–32. As for claim 6, Petitioner states that "a POSITA would repeat the Verhaege circuit at every I/O pad to protect the entire circuit from ESD," but annotates Verhaege's single I/O pad. *Id.* at 31–32. Petitioner refers to its previous discussion, presumably for claim 1, and does not reproduce the two-circuit diagram. *Id.* In the challenge to claim 14, Petitioner refers to the reasoning for claim 6. *Id.* at 43. Because the challenges to claim 6 and 14 rely on the challenge to claim 1, Petitioner has not sufficiently explained how Verhaege teaches or suggests "a control circuit configured to instruct the control block to activate at least a portion of

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highlighted in orange in Petitioner's annotations to Verhaege's Figure 1, but neither gate clamp is highlighted in Petitioner's two-circuit combination. *Id.* at 18.

the output buffer when an ESD event occurs, to charge the pad capacitance to reduce a maximum voltage developed in the system as a result of the ESD event," as in claim 6 (*id.* at 7:3–22) or "control circuitry operable to: activate at least a portion of the respective output buffer in response to an ESD event to charge the respective pad capacitance to reduce a maximum voltage developed in the system as a result of the ESD event," as recited in claim 14 (*id.* at 8:13–31).

For at least this reason, Petitioner has not shown a reasonable likelihood of prevailing in its challenges to claims 1, 6, and 14.

vi. Charge Sharing

Apart from the internal contradictions in Petitioner's mapping of the claim elements, Petitioner does not sufficiently explain how two of Verhaege's circuits would have worked together to share the ESD charge under its own theory.

Verhaege discloses a single circuit that shunts ESD energy from the I/O pin on the same pad. Ex. 1004, 2:26–40. Verhaege's circuit is shown below. *Id.*, Fig. 1.

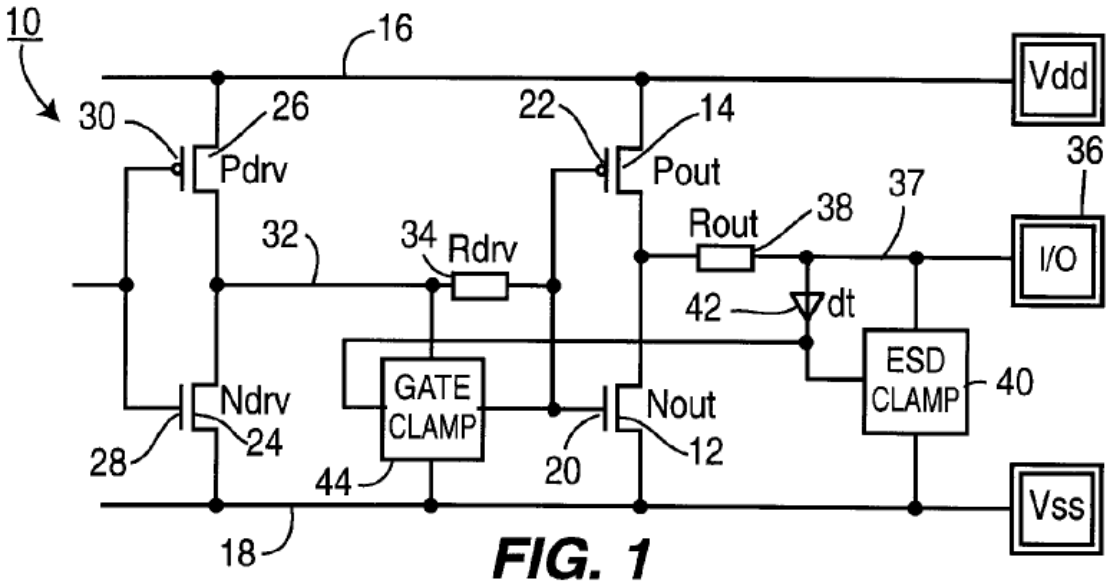


FIG. 1

Verhaege's circuit 10 has transistors 24 and 26 to drive the CMOS output-driver circuit: NMOS transistor 12 and PMOS transistor 14. *Id.* at 2:25–29. Dynamic trigger 42 triggers ESD clamp 40. *Id.* at 2:29–30. Gate clamp 44 grounds transistor 12's gate 20 under transient voltage stress. *Id.* at 2:32–34. Transistor 12 is turned off during stress, independent of the pre-driver state. *Id.* at 2:35–37. The ESD stress is diverted to the parallel ESD clamp. *Id.* 2:35–40. In its obviousness rationale, Petitioner relies on Verhaege's gate clamp, arguing that "gate clamp 44 then 'turn[s] on the at least one of the one or more output transistor devices,' i.e., PMOS transistor 14 (dark blue), by grounding the gates of the output transistors." Pet. 22 (citing Ex. 1004, 2:32–34).

Patent Owner argues that Petitioner does not explain how the two-circuit operation would teach or suggest charge sharing. Prelim. Resp. 40. According to Patent Owner, Petitioner only explains how a positive ESD event on the first circuit (left in its two-circuit illustration, *supra* Section II.C.1.a.ii) would turn on the Pout transistor in the same circuit. *Id.* at 40–41. Patent Owner argues that Petitioner does not "explain why or how increased voltage on the shared Vdd rail would cause anything to happen in the I/O cell on the right, let alone cause Pout to turn on in the righthand I/O cell and share ESD charge." *Id.* at 41. Patent Owner's expert testifies that, unless Pout is turned on in the right-hand circuit in Petitioner's diagram, no current will flow from the shared Vdd rail to the I/O pad on the second circuit, which means that no ESD charge-sharing would occur. Ex. 2003 ¶¶ 114–115.

We agree with Patent Owner that Petitioner's explanation is insufficient to demonstrate Verhaege or Petitioner's proposed two-circuit combination teaches the control block. Even if Pout were already turned on

at the time of an ESD event, claim 1 requires "a control block configured, *to turn on*, when instructed, *at least one of the one or more output transistor devices* to charge the pad capacitance to reduce a maximum voltage developed in the system as a result of the ESD event. Ex. 1001, 6:29–49 (emphasis added). Claims 6 and 14 recite "activate" instead of "turn on" in similar limitations. *Id.* at 7:3–22 (claim 6); *id.* at 8:13–31 (claim 14). Patent Owner argues that, unlike claims 1, 6, and 14, the dynamic trigger in the second circuit in Petitioner's two-circuit design could only detect the voltage spike on the Vdd rail if Pout were already turned on. Prelim. Resp. 45.

At bottom, the deficiencies identified by Patent Owner here are stem from Petitioner reliance on Verhaege's single-circuit operation for most of the limitations, instead of Petitioner's proposed two-circuit design. *See* Pet. 13–24 (claim 1), 27–33 (claim 6), 40–44 (claim 14).

For this additional reason, Petitioner has not shown a reasonable likelihood of prevailing in its challenges to claims 1, 6, and 14.

vii. Impermissible Hindsight

Petitioner's obviousness rationale is deficient for the additional reason that it appears to be based entirely on impermissible hindsight.

Petitioner argues, "It would have been obvious to a POSITA that, because an ESD event could occur at any I/O pad, the Verhaege invention should be repeated at every I/O pad." Pet. 18 (citing Ex. 1002 ¶ 67); *id* at 30–32 (claim 6); *id.* at 43 (claim 14). Yet Petitioner acknowledges that "there were many obvious ways to activate multiple circuits during an ESD event." *Id.* at 51. The Petition does not sufficiently explain why it would have been obvious to have chosen the way that is claimed. *See id.* at 18, 30–32, 43. Rather, Petitioner's obviousness rationale appears to be based on impermissible hindsight gleaned entirely from the challenged patent's

specification. *See InTouch Tech., Inc. v. VGO Commc'ns, Inc.*, 751 F.3d 1327, 1351 (Fed. Cir. 2014) ("It appears that [the expert] relied on the . . . patent itself as her roadmap for putting what she referred to as pieces of a 'jigsaw puzzle' together."). For this additional reason, Petitioner has not shown a reasonable likelihood of prevailing in its challenges to claims 1, 6, and 14.

viii. Conclusion

Petitioner does not sufficiently explain how its proposed two-circuit combination teaches or suggests the subject matter of claims 1, 6, and 14. *See supra* Sections II.C.1.a.v and vi. Also, Petitioner's obviousness rationale is based solely on impermissible hindsight. *See supra* Section II.C.1.a.vii. Thus, Petitioner has not shown a reasonable likelihood of prevailing in its challenges to claims 1, 6, and 14 based on Verhaege alone.

b. Dependent Claims

Claims 2–5, 7–13, and 15–18 depend from one of claims 1, 6, or 14. Petitioner's analysis of claims 2–5, 7–13, and 15–18 does not remedy the deficiencies of the challenges to claims 1, 6, and 14. *See* Pet. 24–45. For example, the analysis of claim 2 refers to the analysis of claim 1 for charge sharing. *Id.* at 24–25. The challenges to claims 3–5, 7, 10, 13, and 17 refer to Verhaege's single-circuit diagram, not Petitioner's two-circuit diagram. *Id.* at 25–27, 33–36, 39–40, 46. Petitioner's analysis of claim 18 mirrors the analysis for claim 13. *Id.* at 46. Claim 9 further limits the PMOS device, and Petitioner's arguments about it do not remedy the issues with the obviousness rationale. *Id.* at 36. The analysis of claims 11, 12, and 16 are based on the challenge to claim 6. *Id.* at 38–39, 45. Thus, Petitioner has not shown a reasonable likelihood of prevailing on its challenges to claims 2–5, 7–13, and 15–18 based on Verhaege alone.

2. *Obviousness: Verhaege and Miller*

Petitioner asserts that claims 1–18 are unpatentable as obvious over Verhaege and Miller. Pet. 47–58.

a. *Claim 1, 6, and 14*

i. *Miller*

Miller's ESD-protection system uses multiple pad circuits. Ex. 1006, 7:14–32. Miller's system is shown below with Petitioner's annotations. Pet. 47.

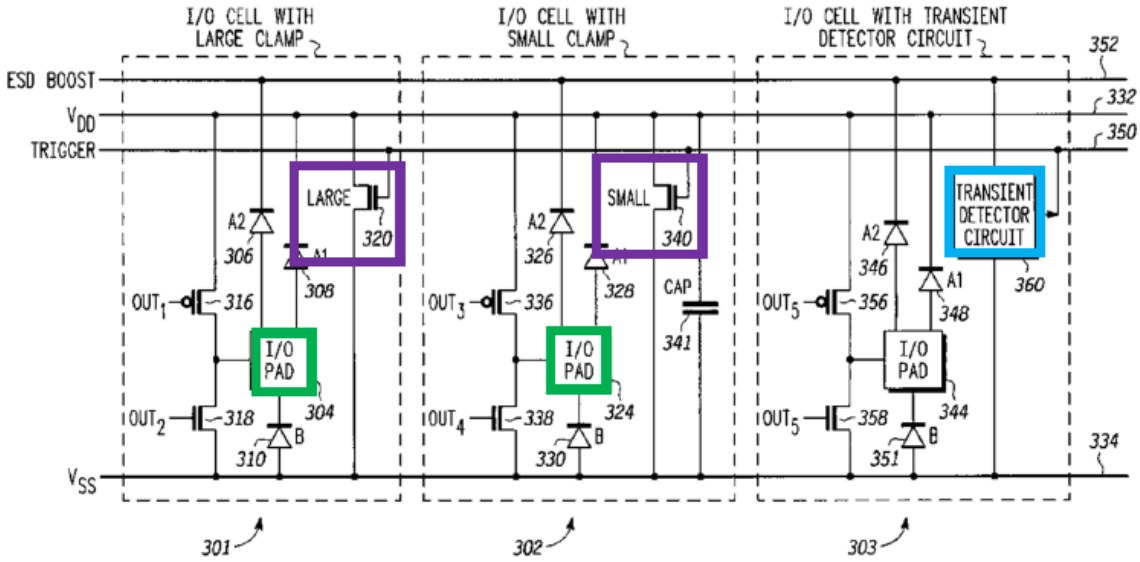


FIG. 3

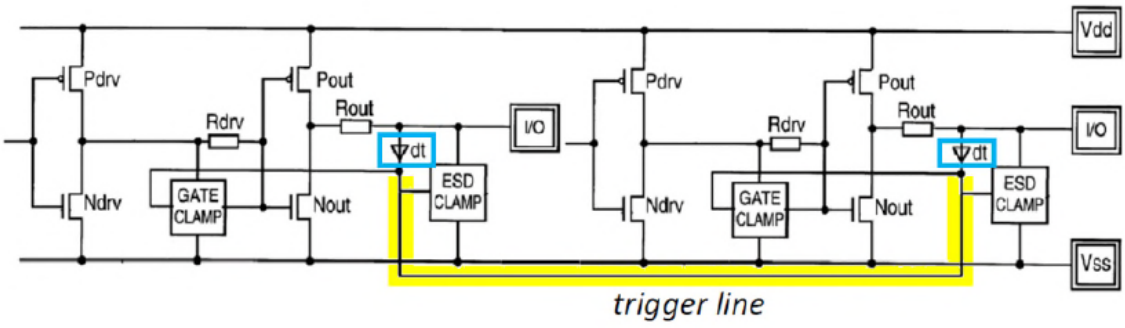
Annotated Figure 3 shows three I/O pads (304, 324, and 344) highlighted in green, two ESD protection clamp transistor devices (320 and 340) in purple, and a single transient-detector circuit (360) in light blue. *Id.* The primary high-current ESD path from an ESD event at I/O pad 304 flows through forward-biased diode 308 to V_{DD} bus 332, then through each of large clamp transistor device 320 and small clamp transistor device 340 to V_{SS} bus 334. *Id.* at 7:14–19. A secondary low-current ESD path flows through forward-biased diode 306 to ESD boost bus 352, powering transient-detector circuit

360. *Id.* at 7:25–28. Transient-detector circuits detect the sudden large voltage change from the ESD event on ESD boost bus 352. *Id.* at 7:28–33. In response, transient-detector circuit 360 drives the gates of the large and small clamp transistor devices (320 and 340) to approximately the boost-bus voltage through trigger bus 350. *Id.* The clamp transistor devices are wired in parallel between the V_{DD} and V_{SS} busses, and together, they dissipate the ESD currents. *Id.* at 7:63–67.

ii. The Petition

Like the Verhaege ground, the Verhaege-Miller combination is based on charge sharing. *See* Pet. 48. In particular, Petitioner asserts that a person of ordinary skill in the art "would have been motivated to use the improved protection circuit of Verhaege, apply it at every I/O pad, and *share the ESD energy* across multiple pad circuits as taught by Miller." *Id.* (emphasis added).

From Miller's teachings, Petitioner argues that it would have been obvious to create a trigger line to connect Verhaege's trigger devices. *Id.* at 51. Petitioner creates its own circuit diagram to illustrate this reasoning. *Id.* The trigger line is shown below, with yellow highlighting by Patent Owner. Prelim. Resp. 48 (citing Pet. 51).



Petitioner argues that its circuit would reduce the maximum voltage, as claimed:

> During an ESD event, both protection circuits are activated by the trigger line. The gate clamps ground the gates of the PMOS output transistors, turning them on and connecting the I/O pads to the Vdd rail. This allows excess ESD energy at one I/O pad to flow to the other I/O pad, thereby "charg[ing] the pad capacitance and reducing the maximum voltage developed in the system."

Pet. 51.

iii. Verhaege

Petitioner, though, relies on the same teachings from Verhaege's single-circuit in its mapping to the remaining limitations. *See id.* at 49 (addressing limitations [1a] through [1c] by stating "See Section V.A."); *id.* at 53 (addressing limitation [1f] by stating "See Section V.A."). Also, Petitioner's diagram does not provide any labels showing which components correspond to the recited transistors and circuitry. *See id.* at 52. Like the challenge to claim 1, the Verhaege-Miller combination is based on an ESD event on one I/O pad affecting another I/O pad's circuit. *See id.* at 52 (claim 1); *id.* at 56 (claim 6); *id.* at 58 (claim 14). Thus, the Petition is deficient for all the reasons discussed with respect to the challenge based on Verhaege alone. *See supra* Sections II.C.1.a.v and vi; *see also* Prelim. Resp. 55 (arguing that its arguments for the challenge based on Verhaege alone apply to its combination with Miller).

iv. Impermissible Hindsight

Petitioner invites the Board to compare the diagram that it created to the one in disclosed in the challenged patent. *See id.* at 52 (citing Ex. 1001, Fig. 1). Here, the Petition suffers from "the distortion caused by hindsight bias" by relying on the challenged patent's own figure as support of its

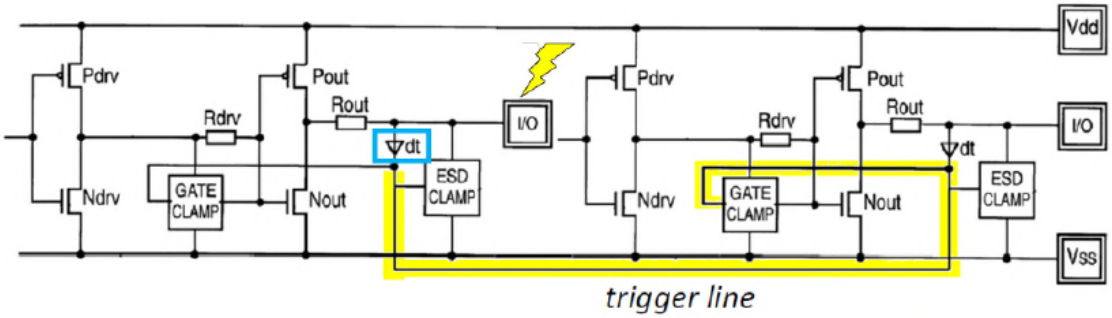
obviousness conclusions. *See Zoltek Corp. v. United States*, 815 F.3d 1302, 1313 (Fed. Cir. 2016) (citing *KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398, 421 (2007)).

Also, Petitioner explains that "the building blocks of both references—such as pads, transistors, clamp devices, and voltage rails—were well understood and behave in predictable ways when combined." Pet. 49 (citing Ex. 1002 ¶ 137). The Petition appears to rely on nothing more than the challenged patent itself to put these "building blocks" together. *Id.* This too reflects impermissible hindsight reasoning. *See InTouch Tech.,* 751 F.3d at 1348–49 (concluding that the expert's "testimony was nothing more than impermissible hindsight; she opined that all of the elements of the claims disparately existed in the prior art, but failed to provide the glue to combine these references.").

For this additional reason, Petitioner has not shown a reasonable likelihood of prevailing in its challenges to claims 1, 6, and 14 based on the Verhaege-Miller combination.

v. Miller's Dynamic Trigger

Independent of the deficiencies discussed above, Petitioner does not explain how adding Miller's trigger line to Verhaege's dynamic trigger would meet the control or enable circuitry recited in claims 1, 6, and 14. Under Petitioner's theory, the dynamic trigger (dt) in the left I/O cell will send a trigger signal along the trigger line to the right I/O cell's gate clamp during an ESD event. Pet. 51. To illustrate this scenario, Patent Owner annotates Petitioner's diagram, as shown below. Prelim. Resp. 58.



Petitioner maps Verhaege's gate clamp to claim 1's control block. Pet. 49. For the enable circuitry, Petitioner refers to Section V.A of the Petition—that is, the section describing the challenge based on Verhaege alone. *Id.* at 51. The part of Section V.A that analyzes the enable circuitry (Section V.A.2.g) explains that "dynamic trigger device 42 must 'instruct' gate clamp 44." *Id.* at 42.

Petitioner's analysis of the second voltage rail providing power to the enable circuitry does not mention Verhaege's dynamic trigger, instead identifying Miller's transient-detector circuit 360 as "enable circuitry." *Id.* at 53. Petitioner states that a person of ordinary skill in the art "would have appreciated that this configuration was compatible with Verhaege." *Id.* at 54 (citing 102 ¶ 151).[3] No further reasoning is given. *Id.*; *see also id.* at 48–49 (discussing Miller's trigger device). Notably, Miller's transient-detector circuit 360 is not labeled in the circuit diagram that Petitioner created. *See id.* at 49. Because Petitioner has identified different features from Miller and Verhaege as teaching or suggesting the same claim limitation without further explanation, Petitioner has not clearly described what corresponds to the enable circuitry in its Verhaege-Miller combination. *Id.* Petitioner's

[3] The cited part of the Chen Declaration here merely repeats Petitioner's argument: "Like the addition of a designated voltage rail, this limitation is compatible with Verhaege." Ex. 1002 ¶ 151.

challenges to claims 6 and 14 have the same deficiency. *See id.* at 55–56 (referring to Section V.A. and the analysis of claim 1 in the challenge to claim 6), 57–58 (referring to Section V.A. and the analysis of claims 1 and 6 in the challenge to claim 14). For the reasons discussed above, we determine that Petitioner has not sufficiently explained how the Verhaege-Miller combination teaches or suggests the subject matter of claims 1, 6, and 14.

vi. Conclusion

Thus, Petitioner has not shown a reasonable likelihood of prevailing in its challenges to claims 1, 6, and 14 based on the Verhaege-Miller combination.

b. Dependent Claims

Claims 2–5, 7–13, and 15–18 depend from one of claims 1, 6, or 14. Petitioner's analysis of claims 2–5, 7–13, and 15–18 does not remedy the deficiencies of the challenges to claims 1, 6, and 14. *See* Pet. 54–59. For example, the analysis of claim 2 refers to the analysis of charge sharing recited in claim 1. *Id.* at 54–55. Petitioner's only analysis for claims 3–5, 8, 9, 11–13, and 15–18 is a reference to the challenge based on Verhaege alone. *Id.* at 55, 57–59 (stating only "See Section V.A."). Petitioner's analysis of claim 7 is based on the "first supply rail of" claim 6. *Id.* at 56. Claim 10 further limits the clamp device, and Petitioner merely asserts that clamp devices are MOSFET transistors. *Id.* at 57. Thus, Petitioner has not shown a reasonable likelihood of prevailing on its challenges to claims 2–5, 7–13, and 15–18 based on the Verhaege-Miller combination.

3. Obviousness: Ker

Petitioner asserts that claims 1–18 are unpatentable as obvious over Ker. Pet. 59–96.

a. Claims 1, 6, and 14

i. Ker

Ker's Figure 28 is reproduced below. Ex. 1005, Fig. 28.

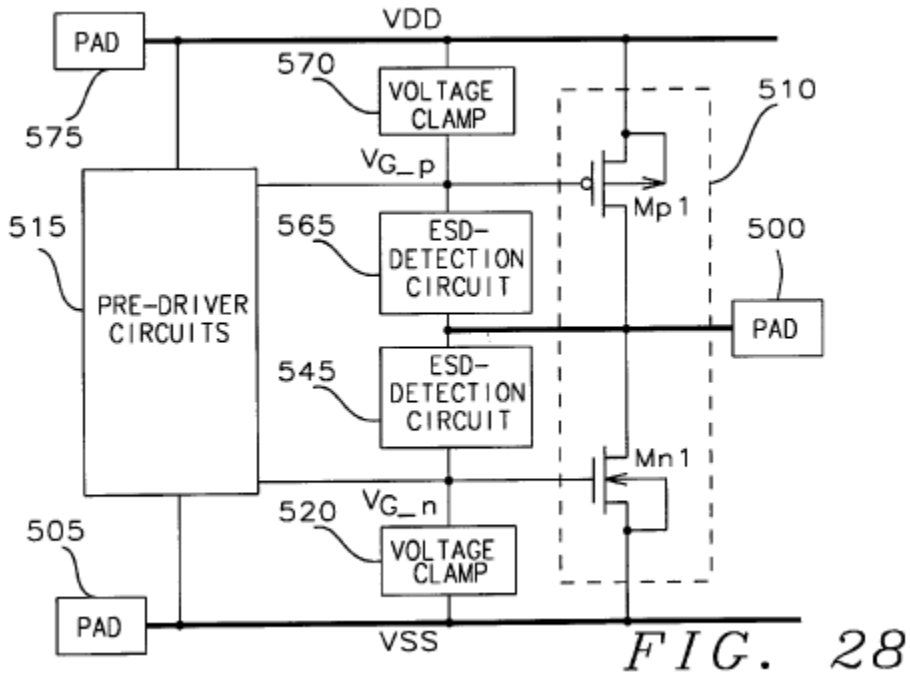


FIG. 28

A ESD event at pad 500 with a first polarity causes ESD-detection circuit 545 to send a signal to V_{G_n}. *Id.* at 18:24–30. For the opposite polarity, the second ESD circuit 565 senses the ESD source's voltage level and places another activation signal at the second output-signal port of the internal pre-driver circuit 515. *Id.* at 18:30–35. In both cases, an activated driver circuit (510) dissipates the charge from the ESD source. *Id.* at 18:28–36. Before the voltage levels become potentially damaging, voltage-clamping circuits 520 and 570 are activated to prevent the damage. *Id.* at 18:52–60.

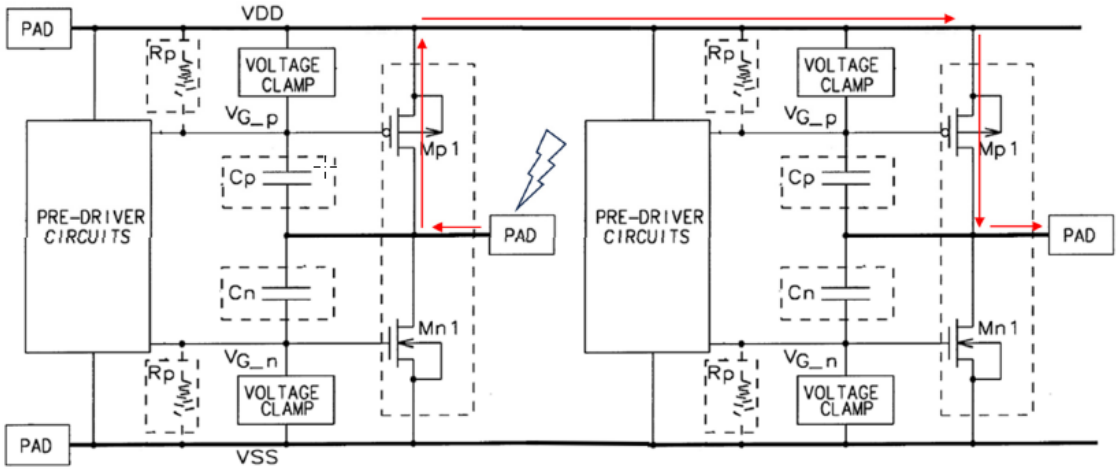
ii. The Petition

Similar to the grounds based on Verhaege, the Ker ground is also based on repeating the circuitry at multiple pads. *See* Pet. 66, 79, 92. In the challenge to claim 1, Petitioner argues that "a POSITA would have been motivated to repeat the Ker circuit at each I/O pad." *Id.* at 66. Petitioner

makes a similar argument for claims 6 and 14. *See id.* at 79 (claim 6); *id.* at 92 (arguing in the challenge to claim 14 that "[b]ecause a POSITA would repeat the Ker circuit at every I/O pad for ESD protection, the energy can then flow to other pad circuits.").

According to Petitioner, "Ker renders the [claim 1's control block] limitation obvious because, as indicated by the generic disclosure of Figure 28, the ESD detection circuit can take multiple forms." *Id.* at 64. Petitioner argues that "Ker discloses numerous ESD detection circuits, including the one shown in Figure 37." *Id.* Petitioner argues that an ordinarily skilled artisan would have appreciated that the ESD-detection circuits would have been interchangeable and would have modified Figure 28 to use Figure 37's control block. *Id.* (citing Ex. 1002 ¶¶ 199–202). Petitioner then refers to Figure 29 "for simplicity" to illustrate its obviousness rationale. *Id.* at 65 n.8.

Relying on Ker's Figures 28, 29, and 37 and its own reasoning about duplicating circuits, Petitioner creates the following diagram. *Id.* at 66.



Petitioner asserts that, "when output transistor Mp1 connects pad 500 to Vdd during an ESD event, allowing the ESD energy to flow to the Vdd

rail, the ESD energy can flow to other pads connected to the rail [as shown above in red]." *Id.* According to the Petition, "This 'charge[s] the pad capacitance' of the other I/O pads connected to the rail, thereby 'reduc[ing] the maximum voltage developed in the system as a result of the ESD event.'" *Id.* Petitioner does not provide any citations to Ker or the Declaration of Dr. Chen in support of these assertions. *See id.*

Petitioner makes similar arguments in its unpatentability arguments for claims 6 and 14. *See id.* at 79 (claim 6); *id.* at 91–92 (claim 14).

iii. The Enable and Control Circuitry

Patent Owner argues that the two-cell version of Ker is Petitioner's own creation:

> Because Ker discloses *only* a single I/O cell—not a combined embodiment—the righthand I/O cell's functionality in Petitioner's combined version of Ker is no different than if the righthand cell were a standalone I/O cell. Any other purported functionalities (such as operation in response to an ESD event on the lefthand I/O cell) are merely creations of Petitioner's own making.

Prelim. Resp. 66 n. 15. Patent Owner argues that Petitioner has not explained how Rp and Cp (mapped to the enable and control circuitry) in the right I/O cell would detect an event on the left I/O cell and turn on Mp1 in the right cell. *Id.* at 65. According to Patent Owner, the right I/O cell is an instance of Ker's single-cell embodiment designed to be activated by an ESD event on itself. *Id.* at 65–66.

In Patent Owner's view, Petitioner's reasoning is circular: The right cell's output transistor (Mp1) must be on for the current to flow from the Vdd rail to its I/O pad, but Petitioner does not explain how the right cell's output transistor (Mp1) could be turned on by the detection circuit unless

Mp1 were already on. *Id.* at 66 (citing Ex. 2003 ¶ 151). Patent Owner argues, "The entirety of Petitioner's analysis is pure say-so." *Id.* at 65.

We agree that the Petition lacks a sufficient explanation of how its two-cell version of Ker teaches or suggests all the limitations of the claim. *See id.* at 64–66. We also agree with Patent Owner that the corresponding obviousness rationale is conclusory. *See id.* As with Petitioner's analysis of Verhaege, the challenge based on Ker presents an incomplete and contradictory correspondence between various embodiments in the prior art and the claim limitations.

In its analysis, Petitioner relies on three of Ker's figures, each illustrating different embodiments (Figures 28, 29, and 37), but Petitioner does not sufficiently explain how its combination of these embodiments collectively teach or suggest the subject matter recited in claims 1, 6, and 14. *See* Pet. 59–71 (claim 1); *id.* at 74–81 (claim 6); *id.* at 88–94 (claim 14). Ker describes Figure 28 and 29 as "schematic diagrams of implementations of the output drive circuit of FIG. 27." Ex. 1005, 11:12–13. Figure 27 "is a schematic diagram of an output drive circuit incorporating an embodiment of the ESD protection circuit of [Ker's] invention." *Id.* at 11:9–11. Figure 32 is a schematic diagram of a different embodiment. *Id.* at 11:17–19.

Petitioner's basis for combining these embodiments is that a "POSITA would have appreciated that the ESD detection circuits were interchangeable and would have understood how to modify the Figure 28 circuit to use the more advanced detection circuit shown in Figure 37 as the control block" Pet. 65 (citing Ex. 1002 ¶¶ 199–202). Dr. Chen testifies that "the components of the circuit, including resistors, capacitors, and transistors, behave in predictable ways." Ex. 1002 ¶ 203. Yet neither Petitioner nor Dr. Chen explains what reason or motivation one of ordinary

skill in the art would have had to combine those embodiments. *See id.* ¶¶ 199–202; Pet. 65. Dr. Chen's conclusory analysis here suffers from hindsight bias. *See ActiveVideo Networks, Inc. v. Verizon Commc'ns, Inc.*, 694 F.3d 1312, 1327 (Fed. Cir. 2012) ("[T]he expert's testimony on obviousness was essentially a conclusory statement that a person of ordinary skill in the art would have known, based on the 'modular' nature of the claimed components, how to combine any of a number of references to achieve the claimed inventions. This is not sufficient and is fraught with hindsight bias."); *InTouch*, 751 F.3d at 1348 (explaining that the expert's "testimony was nothing more than impermissible hindsight; she opined that all of the elements of the claims disparately existed in the prior art, but failed to provide the glue to combine these references").

Petitioner does not identify any teachings related to charge sharing in any of those embodiments. Rather, Petitioner argues that the charge sharing would have been obvious and creates its own circuit diagram to show this. *See* Pet. 67 (claim 1); *id.* at 79 (claim 6); *id.* at 91–92 (claim 14). To address the rest of the limitations, however, Petitioner does not rely on the two-cell diagram that it created. *See id.* at 60–71 (claim 1); *id.* at 74–81 (claim 6); *id.* at 88–94 (claim 14). Thus, it is unclear how the two-cell circuit that Petitioner created teaches or suggests the other features in claims 1, 6, and 14.

Under Petitioner's theory that the claim requires charge sharing (*see, e.g.*, *id.* at 66), the ESD event occurs on a different pad than the recited "pad capacitance" and associated enable (claim 1) and control circuitry (claim 6 and 14). For example, Petitioner's two-cell version of Ker shows the ESD event on the left being shared with the pad on the right. *See id.* at 66 (claim 1), 79 (claim 6), 93 (claim 14). The rest of Petitioner's analysis refers to

Ker's single circuit, which has all the components on the same device. *See id.* at 60–71 (claim 1); *id.* at 74–81 (claim 6); *id.* at 88–94 (claim 14). Petitioner argues that Rp and Cp are the enable and control circuitry. *See id.* at 69–70 (claim 1); *id.* at 78–79 (claim 6); *id.* at 91–93 (claim 14). Petitioner does not fully explain whether Rp and Cp in the right or left cell would detect an ESD event, or how its two-cell version would turn on Mp1 in either cell because Petitioner annotates Ker's Figure 29, not its two-cell version. *See id.* at 69 (claim 1); *id.* at 78 (claim 6); *id.* at 92 (claim 14).

"Ker describes a single I/O pad circuit." *Id.* at 66. Petitioner's argument about the two-cell version of Ker for claims 1 and 6 lacks any citations to Ker or Dr. Chen's Declaration. *See id.* at 66–67 (claim 1); *id.* at 79 (claim 6). For claim 14, Petitioner cites the Declaration of Dr. Chen for its argument that, "[b]ecause a POSITA would repeat the Ker circuit at every I/O pad for ESD protection, the energy can then flow to other pad circuits." *Id.* at 92 (citing Ex. 1002 ¶ 276). In the cited paragraph, Dr. Chen refers to the analysis of claim 6 without providing additional technical reasoning or support from the record. *See* Ex. 1002 ¶ 276. Dr. Chen's declaration merely repeats the Petition's argument. *Compare* Pet. 66–67, *with* Ex. 1002 ¶ 206. Thus, Dr. Chen's assertions (Ex. 1002 ¶ 206) are entitled to little weight. *See Xerox Corp. v. Bytemark, Inc.*, IPR2022-00624, Paper 9 at 15 (PTAB Aug. 24, 2022) (precedential); 37 C.F.R. § 42.65(a) ("Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.").

On this record, Petitioner has not shown a reasonable likelihood of prevailing in its challenges to claims 1, 6, and 14 based on Ker.

b. Dependent Claims

Claims 2–5, 7–13, and 15–18 depend from one of claims 1, 6, or 14. Petitioner's analysis of claims 2–5, 7–13, and 15–18 does not remedy the deficiencies of the challenges to claims 1, 6, and 14. *See* Pet. 71–73, 81–88, 94–96. The challenge to claim 2 relies on claim 1's challenge. *Id.* at 71–72. The challenges to claims 3–5, 7, 10, 13, and 17 refer only to Ker, not the two-circuit diagram. *Id.* at 72–73, 81–83, 85–86, 87–88, 96. Claim 9 further limits the PMOS device, and Petitioner's arguments about it do not remedy the issues with the obviousness rationale. *Id.* at 84. The analysis of claims 11, 12, and 16 are based on the challenge to claim 6. *Id.* at 86–87, 95. Petitioner's analysis of claim 18 mirrors the analysis of claim 15. *Id.* at 96. Thus, Petitioner has not shown a reasonable likelihood of prevailing on its challenges to claims 2–5, 7–13, and 15–18 based on Ker.

III. CONCLUSION

Petitioner has not shown a reasonable likelihood of showing that any of the challenged claims are unpatentable. Thus, we do not institute an *inter partes* review. *See* 35 U.S.C. § 314(a).

IV. ORDER

It is ORDERED that the Petition is *denied*.

FOR PETITIONER:

Mehran Arjomand
Alex Yap
MORRISON & FOERSTER LLP
marjomand@mofo.com
ayap@mofo.com

FOR PATENT OWNER:

Travis Jensen
Jeremy Lang
ORRICK, HERRINGTON & SUTCLIFFE LLP
t61ptabdocket@orrick.com
ptabdocketjjl2@orrick.com