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APPLICATION NUMBER	PATENT NUMBER	GROUP ART UNIT	FILE WRAPPER LOCATION
10/973,076	7502958	2114	9200

OC000000081543883

Correspondence Address/Fee Address Change

The following fields have been set to Customer Number 56436 on 03/18/2016

- **Correspondence Address**
- **Maintenance Fee Address**

The address of record for Customer Number 56436 is:

56436
Hewlett Packard Enterprise
3404 E. Harmony Road
Mail Stop 79
Fort Collins, CO 80528

HL Klemove v. Foras Techs.
IPR2024-00813
Exhibit 1004

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APPLICATION NUMBER	PATENT NUMBER	GROUP ART UNIT	FILE WRAPPER LOCATION
10/973,076	7502958	2114	9200

OC000000038097154

Correspondence Address/Fee Address Change

The following fields have been set to Customer Number 22879 on 10/01/2009

- **Correspondence Address**
- **Maintenance Fee Address**
- **Power of Attorney Address**

The address of record for Customer Number 22879 is:

22879
HEWLETT-PACKARD COMPANY
Intellectual Property Administration
3404 E. Harmony Road
Mail Stop 35
FORT COLLINS, CO 80528

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,502,958 B2
APPLICATION NO. : 10/973076
DATED : March 10, 2009
INVENTOR(S) : Scott L. Michaelis et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In column 7, line 2, delete "531" and insert -- 5-31 --, therefor.

Signed and Sealed this

Eighteenth Day of August, 2009

David J. Kappos

David J. Kappos
Director of the United States Patent and Trademark Office

Electronic Acknowledgement Receipt

EFS ID:	5660313
Application Number:	10973076
International Application Number:	
Confirmation Number:	6989
Title of Invention:	SYSTEM AND METHOD FOR PROVIDING FIRMWARE RECOVERABLE LOCKSTEP PROTECTION
First Named Inventor/Applicant Name:	Scott L. Michaelis
Customer Number:	22879
Filer:	Steven L. Webb/Marci Santillanes
Filer Authorized By:	Steven L. Webb
Attorney Docket Number:	200404941-1
Receipt Date:	08-JUL-2009
Filing Date:	25-OCT-2004
Time Stamp:	08:15:42
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Certificate of Correction	200404941-1.pdf	451017 edc191aa571be45f0dc3490eb3af1187d40507f8	no	3

Warnings:

Information:

Total Files Size (in bytes):	451017

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

ATTORNEY DOCKET NUMBER: 200404941-1

IN RE APPLICATION OF: U.S. Patent No. 7,502,958

USPTO CONFIRMATION CODE: 6989

APPLICATION NO.: 10/973,076

FILED: Oct. 25, 2004

EXAMINER: Dieu-Minh Le

GROUP ART UNIT: 2114

FOR: SYSTEM AND METHOD FOR PROVIDING FIRMWARE RECOVERABLE LOCKSTEP PROTECTION

37 CFR 1.322 & 37 CFR 1.323 REQUEST FOR CERTIFICATE OF CORRECTION

HONORABLE COMMISSIONER OF PATENTS & TRADEMARKS

Sir:

The following is a request for a certificate of correction in Serial Number 10/973,076, now Patent Number 7,502,958.

A certificate of correction under 35 USC 254 is respectfully requested in the above-identified patent.

☒ All errors were the fault of the USPTO, no fee required. In the event that a further fee is required, please charge the amount to Deposit Account No. 082025.

☐ All errors were the fault of the applicant and, accordingly, please charge **$100.00** to our Deposit Account No. 082025. In the event that a further fee is required, please charge the amount to the same Deposit Account.

☐ The errors were the fault of both the applicant and USPTO and, accordingly, please charge **$100.00** to our Deposit Account No. 082025. In the event that a further fee is required, please charge the amount to the same Deposit Account.

The exact locations where the errors appear in the patent and patent application are as follows:

In column 7, line 2, delete "531" and insert - - 5-31 - -, therefor.
(Amendment to specification filed on Nov. 27, 2007, page 10, line 17)

The requested corrections are attached on Form PTO 1050.

Respectfully Submitted

6/14/09
DATE

Name: Steven L. Webb
Registration No.: 44,395

Attorney/Agent of Record

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, Colorado 80527-2400

PTO/SB/44 (04-05)
Approved for use through 04/30/2007. OMB 0651-0033
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(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,502,958

APPLICATION NO. : 10/973,076

ISSUE DATE : Mar. 10, 2009

INVENTOR(S) : Scott L. Michaelis, et al.

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In column 7, line 2, delete "531" and insert -- 5-31 - -, therefor.

MAILING ADDRESS OF SENDER (Please do not use customer number below):

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Intellectual Property Administration
P. O. Box 272400
Fort Collins, Colorado 80527-2400

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If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/973,076	03/10/2009	7502958	200404941-1	6989

22879 7590 02/18/2009
HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 626 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Scott L. Michaelis, Plano, TX;
Anurupa Rajkumari, Round Rock, TX;
William B. McHardy, Fort Collins, CO;

OIPE IAP10 JAN 26 2009 PATENT & TRADEMARK OFFICE
OIPE IAP10 JAN 27 2009 PATENT & TRADEMARK OFFICE

PART B - FEE(S) TRANSMITTAL

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Marci Santillanes (Depositor's name)
Marci Santillanes (Signature)
01-27-09 (Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/973,076	10/25/2004	Scott L. Michaelis	200404941-1	6989

TITLE OF INVENTION: SYSTEM AND METHOD FOR PROVIDING FIRMWARE RECOVERABLE LOCKSTEP PROTECTION

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	03/02/2009

01 FC:1501 1510.00 DA
02 FC:1504 300.00 DA

EXAMINER	ART UNIT	CLASS-SUBCLASS
LE, DIEU MINH T	2114	714-012000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Hewlett-Packard Development Company, L.P.
(B) RESIDENCE: (CITY and STATE OR COUNTRY): Houston, Texas

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
☒ Issue Fee
☒ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

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☐ Payment by credit card. Form PTO-2038 is attached.
☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 08-2025 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)
☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature [signature] Date 1/27/09

Typed or printed name Steven L. Webb Registration No. 44,395

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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PAGE 1/2 * RCVD AT 1/27/2009 3:01:58 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-6/35 * DNIS:2732885 * CSID:970 898 2590 * DURATION (mm-ss):01-18

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PART B - FEE(S) TRANSMITTAL

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22879 7590 11/28/2008

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Marci Santillanes	(Depositor's name)
Marci Santillanes	(Signature)
01-27-09	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/973,076	10/25/2004	Scott L. Michaelis	200404941-1	6989

TITLE OF INVENTION: SYSTEM AND METHOD FOR PROVIDING FIRMWARE RECOVERABLE LOCKSTEP PROTECTION

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	03/02/2009

EXAMINER	ART UNIT	CLASS-SUBCLASS
LE, DIEU MINH T	2114	714-012000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
   - ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
   - ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

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   (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
   1 _____
   2 _____
   3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Hewlett-Packard Development Company, L.P.
(B) RESIDENCE: (CITY and STATE OR COUNTRY): Houston, Texas

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
- ☒ Issue Fee
- ☒ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)
- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 08-2025 (enclose an extra copy of this form).

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- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
- ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date 1/27/09

Typed or printed name Steven L. Webb Registration No. 44,395

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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Alexandria, Virginia 22313-1450
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NOTICE OF ALLOWANCE AND FEE(S) DUE

22879 7590 11/28/2008

HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER	
LE, DIEU MINH T	
ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 11/28/2008

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/973,076	10/25/2004	Scott L. Michaelis	200404941-1	6989

TITLE OF INVENTION: SYSTEM AND METHOD FOR PROVIDING FIRMWARE RECOVERABLE LOCKSTEP PROTECTION

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	03/02/2009

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

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(Depositor's name)

(Signature)

(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/973,076	10/25/2004	Scott L. Michaelis	200404941-1	6989

TITLE OF INVENTION: SYSTEM AND METHOD FOR PROVIDING FIRMWARE RECOVERABLE LOCKSTEP PROTECTION

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	03/02/2009

EXAMINER	ART UNIT	CLASS-SUBCLASS
LE, DIEU MINH T	2114	714-012000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1_____

2_____

3_____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/973,076	10/25/2004	Scott L. Michaelis	200404941-1	6989

22879 7590 11/28/2008

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FORT COLLINS, CO 80527-2400

EXAMINER
LE, DIEU MINH T

ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 11/28/2008

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 626 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 626 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

Notice of Allowability	Application No.	Applicant(s)	
	10/973,076	MICHAELIS ET AL.	
	Examiner	Art Unit	
	Dieu-Minh Le	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the communication filed 10/16/2008*.

2. ☒ The allowed claim(s) is/are *1-6, 9-22, 24-28[now as 1-25]*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 10/16/2008
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/Dieu-Minh Le/
Primary Examiner, Art Unit 2114

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	102	("20020144177" | "20020152420" | "20030051190" | "20030070050" | "20030126498" | "20030135711" | "20030140281" | "20040006722" | "20040019771" | "20040078650" | "20040078651" | "20040153857" | "20050172164" | "20050240806" | "20050240811" | "20050240829" | "20060085677" | "20060136672" | "20060248384" | "20060248684" | "4358823" | "5226152" | "5249188" | "5537655" | "5675794" | "5751932" | "5758058" | "5764660" | "5896523" | "5915082" | "5991900" | "6065135" | "6141770" | "6148348" | "6220581" | "6263452" | "6438687" | "6473869" | "6560682" | "6604177" | "6615366" | "6625749" | "6675324" | "6687851" | "6754787" | "6920581" | "6948092" | "7003691" | "7020800" | "7085959" | "7134047" | "7155721" | "7191292" | "7225355" | "7237144" | "7251746").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/20 12:49

L2	36602	(pair spare slave redundan$4 backup back-up "back up" second$4) adj2 processor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/20 13:14
L3	2501	lockstep lock-step	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/20 13:14
L4	494	L2 and L3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/20 13:14
L5	95	(recover$4 reestablish$3 restart$3) with L3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/20 13:14
L6	139793	firmware	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/20 13:14
L7	26	L4 and L5 and L6	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/20 13:14
L8	6	L7 and 1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/20 13:14
L9	31	(michaelis-scott$ rajkumari-anurupa$ mchardy-william$).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/20 13:29

L10	821	(714/11).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/20 13:29
L11	387	(714/12).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/20 13:29
L12	703	(714/13).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/20 13:29
L13	698	(714/10).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/20 13:29
L14	107	(712/31).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/20 13:29
L15	2280	L10 L11 L12 L13 L14	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/20 13:29
L16	413	(712/34).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/20 13:33
L17	60263	(switch$4 chang$4 failover fail-over "fail over") same (spare slave redundan$4 backup back-up "back up" second$4) same processor	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/20 13:34

L18	222	(loss lose los$3 lost$3) same (lockstep lock-step "lock step")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/20 13:34
L19	92	(detect$3 track$3 monitor$3) same L18	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/20 13:34
L20	15400	trigger$3 same ("operating system" OS operating-system) same (idle stop$4 interrupt$3 halt$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/20 13:34
L21	10	L20 and L19 and L17	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/20 13:34
L22	7	(7 21) and (15 16)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/20 13:37
L23	12	("Advanced Configuration and Power Interface" ACPI) and (7 21)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/20 13:39
L24	18	("714"/$).ccls. and 7	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/20 13:40
L25	0	("710"/$).ccls. and 7	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/20 13:40

S1	14	(("7085959") or ("20050172164") or ("5675794") or ("6438687") or ("6920581") or ("5915082") or ("6625749")).PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/08/26 17:54
S2	2	("7085959").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/08/27 15:05
S3	730	(714/11).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/27 15:06
S4	337	(714/12).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 15:32
S5	606	(714/13).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/27 15:07
S6	36	("20020144177" | "20030070050" | "20040006722" | "20040019771" | "20040153857" | "5226152" | "5249188" | "5751932" | "5758058" | "5764660" | "6065135" | "6148348" | "6473869" | "6560682" | "6604177" | "6615366" | "6625749" | "6687851" | "6754787").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/27 15:08
S7	44	("20020144177" | "20030070050" | "20040006722" | "20040019771" | "20040153857" | "6625749" | "6687851" | "6754787")".PN"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/27 15:09

S9	2222	lockstep lock-step	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 15:21
S11	25008	(loss adj S9) LOL	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 15:22
S12	51	(detect$3 or track$4) adj S11	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 15:23
S13	1547	(boot$4 or initializ$4) adj processor	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 16:41
S14	246	spare adj processor	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 15:27
S15	12	S12 and S13 and S14	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 15:30
S16	25	(michaelis-scott$ or myer-sylvia$ or mchardy-william$).in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 16:14
S18	632	(714/10).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 15:33

S19	95	(712/31).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 16:08
S20	52536	(switch$4 chang$4 failover fail-over "fail over") same (spare slave redundan$4 backup back-up "back up" second$4) same processor	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 16:54
S21	81	S20 same S13	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 16:28
S22	168219	without same ("shut$4 down" stop$4 idle interrupt$4) same (OS "operating system")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 16:33
S23	6	S21 and S22	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 16:33
S24	20342	multi-processor "multi processor" and S11 and S13	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 16:45
S25	176	S24 and S20 and S22	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 16:46
S26	7	S25 and S14	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 16:53

S27	87	(recover$4 reestablish$3 restart$3) with S9	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 16:54
S28	31827	(pair spare slave redundan$4 backup back-up "back up" second$4) adj2 processor	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 16:55
S29	101834	firmware	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 16:56
S30	21	S27 and S28 and S29	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 16:57
S31	15153	trigger$3 same ("operating system" OS operating-system) same (idle stop$4 interrupt$3 halt$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/02/14 14:49
S32	207	(loss lose los$3 lost$3) same (lockstep lock-step "lock step")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/02/14 14:52
S33	86	(detect$3 track$3 monitor$3) same S32	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/02/14 14:56
S34	3	S33 same S31	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/02/14 14:56

S35	3	S32 same S31	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/02/14 15:02
S36	10	S32 and S31	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/02/14 15:02
S37	33339	(pair spare slave redundan$4 backup back-up "back up" second$4) adj2 processor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/02/14 15:05
S38	2323	lockstep lock-step	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/02/14 15:06
S39	92	(recover$4 reestablish$3 restart$3) with S38	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/02/14 15:06
S40	114677	firmware	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/02/14 15:06
S41	11	S37 same S39 same S40	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/02/14 15:06
S42	764	(714/11).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/02/14 15:07

S43	352	(714/12).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/02/14 15:07
S44	659	(714/13).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/02/14 15:07
S45	658	(714/10).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/02/14 15:07
S46	96	(712/31).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/02/14 15:07
S47	2	(S42 S43 S44 S45 S46) and S31 and S33	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/02/14 15:07
S48	2	(S42 S43 S44 S45 S46) and S31 and S32 and S37 and S40	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/02/14 15:08
S49	28	(michaelis-scott$ or myer-sylvia$ or mchardy-william$).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/11 17:01
S50	15230	trigger$3 same ("operating system" OS operating-system) same (idle stop$4 interrupt$3 halt$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/11 17:02

S51	214	(loss lose los$3 lost$3) same (lockstep lock-step "lock step")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/11 17:02
S52	91	(detect$3 track$3 monitor$3) same S51	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/11 17:02
S53	781	(714/11).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/11 17:02
S54	360	(714/12).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/11 17:02
S55	670	(714/13).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/11 17:02
S56	665	(714/10).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/11 17:02
S57	98	(712/31).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/11 17:02
S58	4	(S53 S54 S55 S56 S57) and S50 and S52	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/11 17:02

S59	34280	(pair spare slave redundan$4 backup back-up "back up" second$4) adj2 processor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/11 17:03
S60	2381	lockstep lock-step	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/11 17:03
S61	481	S59 and S60	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/11 17:03
S62	94	(recover$4 reestablish$3 restart$3) with S60	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/11 17:03
S63	121775	firmware	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/11 17:03
S64	26	S61 and S62 and S63	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/11 17:03
S65	36	("20020144177" | "20030070050" | "20040006722" | "20040019771" | "20040153857" | "5226152" | "5249188" | "5751932" | "5758058" | "5764660" | "6065135" | "6148348" | "6473869" | "6560682" | "6604177" | "6615366" | "6625749" | "6687851" | "6754787"). PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/11 17:04

S66	57	("20020144177" | "20030070050" | "20040006722" | "20040019771" | "20040153857" | "6625749" | "6687851" | "6754787")".PN"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/11 17:04
S67	79	S65 S66	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/11 17:04
S68	32	S63 and S67	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/11 17:05
S69	4	S68 and S52	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/11 17:06
S70	2	S69 and S50	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/11 17:06

11/20/08 1:45:51 PM
C:\ Documents and Settings\ MLe\ My Documents\ EAST\ Workspaces\ 10973076b.wsp

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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	10/973,076
Filing Date	October 25, 2004
First Named Inventor	Scott L. Michaelis
Art Unit	2114
Examiner Name	Le, Dieu Minh T.
Attorney Docket Number	200404941-1

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/M.L./		US- 2002/0152420	10-17-2002	Chaudhry et al.	
		US- 2003/0126498	07-03-2003	Bigbee et al.	
		US- 2003/0135711	07-17-2003	Shoemaker et al.	
		US- 2004/0078651	04-22-2004	Stafford et al.	
		US- 2005/0240811	10-27-2005	Stafford et al.	
		US- 2006/0248384	11-02-2006	Stafford	
		US- 2006/0085677	04-20-2006	Stafford et al.	
		US- 2006/0248684	11-9-2006	Vosbikian et al.	
		US- 4,358,823	11-9-1982	McDonald et al.	
		US- 5,537,655	07-16-1996	Truong	
		US- 5,675,794	10-07-1997	Meredith	
		US- 5,991,900	11-23-1999	Garnett	
		US- 6,220,581	04-24-2001	Mueller	
		US- 6.263,452	07-17-2001	Jewett et al.	
		US- 6,438,687	08-20-2002	Klein	
		US- 7,134,047	11-07-2006	Quach	
		US- 7,225,355	05-29-2007	Yamazaki et al.	
		US-			
		US-			

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]

Examiner Signature	/Dieu Minh Le/	Date Considered	11/20/2008

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND** TO: **Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10973076	MICHAELIS ET AL.
	Examiner	**Art Unit**
	Dieu-Minh Le	2114

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	02/14/2008	05/13/2008	07/02/2008	11/20/2008					
1	1	✓	=	=	=					
2	2	✓	=	=	=					
3	3	✓	=	=	=					
4	4	✓	=	=	=					
5	5	✓	=	=	=					
6	6	✓	=	=	=					
	7	✓	-	-	-					
	8	O	-	-	-					
7	9	O	=	=	=					
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	30	✓	-	-	-					
	31	✓	-	-	-					
	32	✓	-	-	-					
	33	O	-	-	-					
	34	✓	-	-	-					
	35	✓	-	-	-					

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10973076	MICHAELIS ET AL.
	Examiner	**Art Unit**
	Dieu-Minh Le	2114

SEARCHED

Class	Subclass	Date	Examiner
714	10-13; 712/31,34	11/20/08	dml
714	(upadated the above search)	11/20/08	dml

SEARCH NOTES

Search Notes	Date	Examiner
EAST search all files updated.	11/20/08	dml
Inventor names search	11/20/08	dml
NPL search [files IEEE, Google scholar]	11/20/08	dml

INTERFERENCE SEARCH

Class	Subclass	Date	Examiner
714	10-13; 712/31,34	11/20/08	dml
	Interference text search - see data file		

	/Dieu-Minh Le/ Primary Examiner.Art Unit 2114

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10973076	MICHAELIS ET AL.
	Examiner	**Art Unit**
	Dieu-Minh Le	2114

ORIGINAL		INTERNATIONAL CLASSIFICATION										
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED					
714	12	G	0	6	F	11 / 00 (2006.01.01)						

CROSS REFERENCE(S)

CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
712	31				

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	15	17		33										
2	2	16	18		34										
3	3	17	19		35										
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9	11	24	27												
10	12	25	28												
11	13		29												
12	14		30												
13	15		31												
14	16		32												

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 25	
/Dieu-Minh Le/ Primary Examiner.Art Unit 2114 (Primary Examiner)	11/20/2008 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 1

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P. O. Box 272400
Fort Collins, Colorado 80527-2400

PATENT APPLICATION

ATTORNEY DOCKET NO. 200404941-1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Scott L. Michaelis et al. **Confirmation No.:**

Application No.: **Examiner:**

Filing Date: **Group Art Unit:**

Title: SYSTEM AND METHOD FOR PROVIDING FIRMWARE RECOVERABLE LOCKSTEP PROTECTION

Mail Stop Amendment
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

This Information Disclosure Statement is submitted:

(X) under 37 CFR 1.97(b), or
(Within three months of filing national application; or date of entry of national application; or before mailing date of first office action on the merits; whichever occurs last)

( ) under 37 CFR 1.97(c) together with either a:
( ) Statement under 37 CFR 1.97(e), or
( ) a $180.00 fee under 37 CFR 1.17(p), or
(After the CFR 1.97 (b) time period, but before final action or notice of allowance, whichever occurs first)

( ) under 37 CFR 1.97 (d) together with a:
( ) Statement under 37 CFR 1.97(e)(1) or (2), and
( ) a $180.00 fee set forth in 37 CFR 1.17(p).
(Filed after final action, a notice of allowance, on or before payment of the issue fee)

Please charge to Deposit Account **08-2025** the sum of $0.00 . At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account **08-2025** pursuant to 37 CFR 1.25.

(X) Applicant(s) submit herewith Form PTO 1449 - Information Disclosure Statement together with any required copies of patents, publications or other information of which applicant(s) are aware, which applicant(s) believe(s) may be material to the examination of this application and for which there may be a duty to disclose in accordance with 37 CFR 1.56.

( ) A concise explanation of the relevance of foreign language patents, foreign language publications and other foreign language information listed on PTO Form 1449, as presently understood by the individuals(s) designated in 37 CFR 1.56 (c) most knowledgeable about the content is given on the attached sheet, or where a foreign language patent is cited in a search report or other action by a foreign patent office in a counterpart foreign application, an English language version of the search report or action which indicates the degree of relevance found by the foreign office is listed on form PTO 1449 and is enclosed herewith.

It is requested that the information disclosed herein be made of record in this application.

"Express Mail" label no. **EV 375345153US**

Date of Deposit **Oct. 25, 2004**

I hereby certify that this is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to: Commissioner for Patents, Alexandria, VA 22313-1450.

By

Typed Name: **Phyllis Ewing**

Respectfully submitted,

Scott L. Michaelis et al.

By

Jody C. Bishop

Attorney/Agent for Applicant(s)
Reg. No. **44,034**

Date: **Oct. 25, 2004**

Telephone No.: **(214) 855-8007**

FORM PTO-1449 LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	ATTY. DOCKET NO. **200404941-1**	APPLICATION NO.	CONFIRMATION NO.
	APPLICANT **Scott L. Michaelis et al.**		
	FILING DATE	GROUP	

REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	1A	5,226,152	07/06/1993	Klug et al.	
	1B	5,249,188	09/28/1993	McDonald	
	1C	5,751,932	05/12/1998	Horst et al.	
	1D	5,758,058	05/26/1998	Milburn	
	1E	5,764,660	06/09/1998	Mohat	
	1F	6,065,135	05/16/2000	Marshall et al.	
	1G	6,148,348	11/14/2000	Garnett et al.	
	1H	6,473,869	10/29/2002	Bissett et al.	
	1I	6,560,682	05/06/2003	Miller et al.	
	1J	6,604,177	08/05/2003	Kondo et al.	
	1K	6,615,366	09/02/2003	Grochowski et al.	

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	1L					
	1M					
	1N					
	1O					
	1P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

	1Q	Attorney Docket No. 200404946-1, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR USING INFORMATION RELATING TO A DETECTED LOSS OF LOCKSTEP FOR DETERMINING A RESPONSIVE ACTION "
	1R	Attorney Docket No. 200404944-1, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR ESTABLISHING A SPARE PROCESSOR FOR RECOVERING FROM LOSS OF LOCKSTEP IN A BOOT PROCESSOR"
	1S	Attorney Docket No. 200404943-1, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR CONFIGURING LOCKSTEP MODE OF A PROCESSOR MODULE"

EXAMINER	DATE CONSIDERED

FORM PTO-1449 LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	ATTY. DOCKET NO. **200404941-1**	APPLICATION NO.	CONFIRMATION NO.
	APPLICANT **Scott L. Michaelis et al.**		
	FILING DATE	GROUP	

REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	2A	6,625,749	09/23/2003	Quach	
	2B	6,687,851	02/03/2004	Somers et al.	
	2C	6,754,787	06/22/2004	Miller et al.	
	2D	2002/0144177	10/03/2002	Kondo et al.	
	2E	2003/0070050	04/10/2003	Miller et al.	
	2F	2004/0006722	01/08/2004	Safford	
	2G	2004/0019771	01/29/2004	Quach	
	2H	2004/0153857	08/05/2004	Yamazaki et al.	
	2I				
	2J				
	2K				

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	2L					
	2M					
	2N					
	2O					
	2P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

	2Q	Attorney Docket No. 200404974-1, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR MAINTAINING IN A MULTI-PROCESSOR SYSTEM A SPARE PROCESSOR THAT IS IN LOCKSTEP FOR USE IN RECOVERING FROM LOSS OF LOCKSTEP FOR ANOTHER PROCESSOR
	2R	Attorney Docket No. 200404973-1, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR SWITCHING THE ROLE OF BOOT PROCESSOR TO A SPARE PROCESSOR RESPONSIVE TO DETECTION OF LOSS OF LOCKSTEP IN A BOOT PROCESSOR "
	2S	Attorney Docket No. 200404971-1, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR REESTABLISHING LOCKSTEP FOR A PROCESSOR MODULE FOR WHICH LOSS OF LOCKSTEP IS DETECTED"

EXAMINER	DATE CONSIDERED

FORM PTO-1449 LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	ATTY. DOCKET NO. **200404941-1**	APPLICATION NO.	CONFIRMATION NO.
	APPLICANT **Scott L. Michaelis et al.**		
	FILING DATE	GROUP	

REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	3A				
	3B				
	3C				
	3D				
	3E				
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	3I				
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FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	3L					
	3M					
	3N					
	3O					
	3P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

	3Q	Attorney Docket No. 200404970-1, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR SYSTEM FIRMWARE CAUSING AN OPERATING SYSTEM TO IDLE A PROCESSOR"
	3R	Attorney Docket No. 200404972-1, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR REINTRODUCING A PROCESSOR MODULE TO AN OPERATING SYSTEM AFTER LOCKSTEP RECOVERY"
	3S	

EXAMINER	DATE CONSIDERED

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	102	("20020144177" | "20020152420" | "20030051190" | "20030070050" | "20030126498" | "20030135711" | "20030140281" | "20040006722" | "20040019771" | "20040078650" | "20040078651" | "20040153857" | "20050172164" | "20050240806" | "20050240811" | "20050240829" | "20060085677" | "20060136672" | "20060248384" | "20060248684" | "4358823" | "5226152" | "5249188" | "5537655" | "5675794" | "5751932" | "5758058" | "5764660" | "5896523" | "5915082" | "5991900" | "6065135" | "6141770" | "6148348" | "6220581" | "6263452" | "6438687" | "6473869" | "6560682" | "6604177" | "6615366" | "6625749" | "6675324" | "6687851" | "6754787" | "6920581" | "6948092" | "7003691" | "7020800" | "7085959" | "7134047" | "7155721" | "7191292" | "7225355" | "7237144" | "7251746").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/20 12:49

L2	36602	(pair spare slave redundan$4 backup back-up "back up" second$4) adj2 processor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/20 13:14
L3	2501	lockstep lock-step	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/20 13:14
L4	494	L2 and L3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/20 13:14
L5	95	(recover$4 reestablish $3 restart$3) with L3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/20 13:14
L6	139793	firmware	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/20 13:14
L7	26	L4 and L5 and L6	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/20 13:14
L8	6	L7 and 1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/20 13:14
L9	31	(michaelis-scott$ rajkumari-anurupa$ mchardy-william$).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/20 13:29
L10	821	(714/11).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/20 13:29

L11	387	(714/12).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/20 13:29
L12	703	(714/13).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/20 13:29
L13	698	(714/10).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/20 13:29
L14	107	(712/31).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/20 13:29
L15	2280	L10 L11 L12 L13 L14	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/20 13:29
L16	413	(712/34).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/20 13:33
L17	60263	(switch$4 chang$4 failover fail-over "fail over") same (spare slave redundan$4 backup back-up "back up" second$4) same processor	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/20 13:34
L18	222	(loss lose los$3 lost$3) same (lockstep lock-step "lock step")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/20 13:34
L19	92	(detect$3 track$3 monitor$3) same L18	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/20 13:34

L20	15400	trigger$3 same ("operating system" OS operating-system) same (idle stop$4 interrupt$3 halt$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/20 13:34
L21	10	L20 and L19 and L17	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/20 13:34
L22	7	(7 21) and (15 16)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/20 13:37
L23	12	("Advanced Configuration and Power Interface" ACPI) and (7 21)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/20 13:39
L24	18	("714"/$).ccls. and 7	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/20 13:40
L25	0	("710"/$).ccls. and 7	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/20 13:40

11/20/08 1:49:19 PM
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PTO/SB/08a (09-08)
Approved for use through 10/31/2008. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	10/973,076
Filing Date	October 25, 2004
First Named Inventor	Scott L. Michaelis
Art Unit	2114
Examiner Name	Le, Dieu Minh T.
Attorney Docket Number	200404941-1

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US- 2002/0152420	10-17-2002	Chaudhry et al.	
		US- 2003/0126498	07-03-2003	Bigbee et al.	
		US- 2003/0135711	07-17-2003	Shoemaker et al.	
		US- 2004/0078651	04-22-2004	Stafford et al.	
		US- 2005/0240811	10-27-2005	Stafford et al.	
		US- 2006/0248384	11-02-2006	Stafford	
		US- 2006/0085677	04-20-2006	Stafford et al.	
		US- 2006/0248684	11-9-2006	Vosbikian et al.	
		US- 4,358,823	11-9-1982	McDonald et al.	
		US- 5,537,655	07-16-1996	Truong	
		US- 5,675,794	10-07-1997	Meredith	
		US- 5,991,900	11-23-1999	Garnett	
		US- 6,220,581	04-24-2001	Mueller	
		US- 6.263,452	07-17-2001	Jewett et al.	
		US- 6,438,687	08-20-2002	Klein	
		US- 7,134,047	11-07-2006	Quach	
		US- 7,225,355	05-29-2007	Yamazaki et al.	
		US-			
		US-			

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND** TO: **Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

Electronic Patent Application Fee Transmittal

Application Number:	10973076
Filing Date:	25-Oct-2004
Title of Invention:	SYSTEM AND METHOD FOR PROVIDING FIRMWARE RECOVERABLE LOCKSTEP PROTECTION
First Named Inventor/Applicant Name:	Scott L. Michaelis
Filer:	Nellie Clare Kaufman/Kalyn Black
Attorney Docket Number:	200404941-1

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Request for continued examination	1801	1	810	810
		Total in USD ($)		**810**

Electronic Acknowledgement Receipt

EFS ID:	4129514
Application Number:	10973076
International Application Number:	
Confirmation Number:	6989
Title of Invention:	SYSTEM AND METHOD FOR PROVIDING FIRMWARE RECOVERABLE LOCKSTEP PROTECTION
First Named Inventor/Applicant Name:	Scott L. Michaelis
Customer Number:	22879
Filer:	Nellie Clare Kaufman/Kalyn Black
Filer Authorized By:	Nellie Clare Kaufman
Attorney Docket Number:	200404941-1
Receipt Date:	16-OCT-2008
Filing Date:	25-OCT-2004
Time Stamp:	18:35:04
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	200404941-1-RCE.pdf	48267 d22daa769079dd538bb5819fbcf8f8898ec29267	no	2

Warnings:

Information:

2	Information Disclosure Statement (IDS) Filed (SB/08)	200404941-1-IDS.pdf	56808 0129016389d565cc0506af37f33be1b9cf2d2048	no	1
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
3	Fee Worksheet (PTO-06)	fee-info.pdf	30765 899a66f1970af17cebda20cb14ab40cf3d5e55b8	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	135840	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, Colorado 80527-2400

PATENT APPLICATION

ATTORNEY DOCKET NO. 200404941-1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Scott L. Michaelis

Confirmation No.: 6989

Application No.: 10/973,076

Examiner: Le, Dieu Minh T.

Filing Date: October 25, 2004

Group Art Unit: 2114

Title: SYSTEM AND METHOD FOR PROVIDING FIRMWARE RECOVERABLE LOCKSTEP PROTECTION

Mail Stop RCE
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

REQUEST FOR CONTINUED EXAMINATION (RCE) 37 CFR 1.114

Subsection (b) of 35 U.S.C. 132, effective on May 29, 2000, provides for continued examination of a utiltity or plant application filed on or after June 8, 1995.
See The American Inventors Protection Act of 1999 (AIPA).

This is a Request for Continued Examination (RCE) under CFR 1.114 of the above-identified application.

NOTE: 37 CFR 1.114 is effective on May 20, 2000. If the above- application was filed prior to May 29, 2000, applicant may wish to consider filing a continued prosecution application (CPA) under CFR 1.53(d) (PTO/SB/29) instead of a RCE to be eligible for the patent term adjustment provisions of the AIPA. See Changes to Application Examination and Provisional Application Practice, Interim Rule, 65 Fed. Reg. 14865 (Mar. 20, 2000), 1233 off. Gaz. Pat. Office

Submission under 37 CFR 1.114

☐ Previously submitted

- ☐ Consider the amendment(s)/reply under 37 CFR 1.116 previously filed on _____.
  (Any unentered amendment(s) referred to above will be entered).
- ☐ Consider the arguments in the Appeal Brief or Reply Brief prevously filed on _____.
- ☐ Other _____

☒ Enclosed

- ☐ Amendment/Reply
- ☐ Affidavit(s)/Declaration(s)
- ☒ Information Disclosure Statement (IDS)
- ☐ Other _____

Miscellaneous

- ☐ Suspension of action is requested under 37 CFR 1.103(c) for a period of _____ months.
  The fee for this Suspension is (37 CFR 1.17(i)) $130.00
- ☐ Other _____

☒ RCE filing fee $810.00

☐ A Petition for Extension of Time

☐ 1st Month $130 ☐ 2nd Month $490 ☐ 3rd Month $1110 ☐ 4th Month $1730

☒ Please charge to Deposit Account 08-2025 the sum of $ 810 . At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that my regulate fees.

Respectfully submitted,

Scott L. Michaelis

By: /Robert W. Nelson/

Robert W. Nelson, Esq.

Attorney/Agent for Applicant(s)

Reg No. : 37,898

Date : October 16, 2008

Telephone : (303) 298-9888

Document code: WFEE

United States Patent and Trademark Office
Sales Receipt for Accounting Date: 10/21/2008

PYOUNG1 SALE #00000001 Mailroom Dt: 10/16/2008 082025 10973076
01 FC : 1801 810.00 DA

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

22879 7590 07/16/2008

HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER	
LE, DIEU MINH T	
ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 07/16/2008

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/973,076	10/25/2004	Scott L. Michaelis	200404941-1	6989

TITLE OF INVENTION: SYSTEM AND METHOD FOR PROVIDING FIRMWARE RECOVERABLE LOCKSTEP PROTECTION

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1440	$300	$0	$1740	10/16/2008

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

22879 7590 07/16/2008

HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)

(Signature)

(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/973,076	10/25/2004	Scott L. Michaelis	200404941-1	6989

TITLE OF INVENTION: SYSTEM AND METHOD FOR PROVIDING FIRMWARE RECOVERABLE LOCKSTEP PROTECTION

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1440	$300	$0	$1740	10/16/2008

EXAMINER	ART UNIT	CLASS-SUBCLASS
LE, DIEU MINH T	2114	714-012000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1_____

2_____

3_____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/973,076	10/25/2004	Scott L. Michaelis	200404941-1	6989

22879 7590 07/16/2008

HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER
LE, DIEU MINH T

ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 07/16/2008

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 626 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 626 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

Notice of Allowability	Application No.	Applicant(s)	
	10/973,076	MICHAELIS ET AL.	
	Examiner	Art Unit	
	Dieu-Minh Le	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the communication filed on 06/06/2008*.

2. ☒ The allowed claim(s) is/are *1-6, 9-22, 24-28 [now as 1-25]*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 6/06/08
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/DIEU-MINH THAI LE/
PRIMARY EXAMINER
ART UNIT 2114

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10973076	MICHAELIS ET AL.
	Examiner	**Art Unit**
	Dieu-Minh Le	2114

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	02/14/2008	05/13/2008	07/02/2008						
1	1	✓	=	=						
2	2	✓	=	=						
3	3	✓	=	=						
4	4	✓	=	=						
5	5	✓	=	=						
6	6	✓	=	=						
	7	✓	-	-						
	8	O	-	-						
7	9	O	=	=						
8	10	O	=	=						
9	11	✓	=	=						
10	12	✓	=	=						
11	13	✓	=	=						
12	14	O	=	=						
13	15	=	=	=						
14	16	=	=	=						
15	17	=	=	=						
16	18	=	=	=						
17	19	=	=	=						
18	20	=	=	=						
19	21	✓	=	=						
20	22	✓	=	=						
	23	✓	-	-						
21	24	✓	=	=						
22	25	✓	=	=						
23	26	=	=	=						
24	27	=	=	=						
25	28	=	=	=						
	29	✓	-	-						
	30	✓	-	-						
	31	✓	-	-						
	32	✓	-	-						
	33	O	-	-						
	34	✓	-	-						
	35	✓	-	-						

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10973076	MICHAELIS ET AL.
	Examiner	**Art Unit**
	Dieu-Minh Le	2114

ORIGINAL		INTERNATIONAL CLASSIFICATION	
CLASS	SUBCLASS	CLAIMED	NON-CLAIMED
714	12	G 0 6 F 11 / 00 (2006.01.01)	

CROSS REFERENCE(S)

CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
712	31				

NONE (Assistant Examiner) (Date)		Total Claims Allowed: 25	
/Dieu-Minh Le/ (Primary Examiner)	7/02/2008 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 1

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10973076	MICHAELIS ET AL.
	Examiner	**Art Unit**
	Dieu-Minh Le	2114

SEARCHED

Class	Subclass	Date	Examiner
714	10-13; 712/31	7/2/08	dml
714	(upadated the above search)	7/2/08	dml

SEARCH NOTES

Search Notes	Date	Examiner
EAST search all files updated.	7/2/08	dml
East search updated	7/1/08	dml
Inventor names search	7/2/08	dml
NPL search [files IEEE, Google scholar]	7/2/08	dml

INTERFERENCE SEARCH

Class	Subclass	Date	Examiner
714	10-112	7/2/08	dml
	Interference text search - see data file		

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	72	("20020144177" | "20030051190" | "20030070050" | "20030140281" | "20040006722" | "20040019771" | "20040078650" | "20040153857" | "20050172164" | "20050240806" | "20050240829" | "20060136672" | "5226152" | "5249188" | "5751932" | "5758058" | "5764660" | "5896523" | "5915082" | "6065135" | "6141770" | "6148348" | "6473869" | "6560682" | "6604177" | "6615366" | "6625749" | "6675324" | "6687851" | "6754787" | "6920581" | "6948092" | "7003691" | "7020800" | "7085959" | "7155721" | "7191292" | "7237144" | "7251746").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/01 18:20
L2	214	(loss lose los$3 lost$3) same (lockstep lock-step "lock step")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/01 18:26
L3	91	(detect$3 track$3 monitor$3) same L2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/01 18:26
L4	126820	firmware	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/01 18:29

L5	2632	(recover$4 reestablish$3 restart$3) same L4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/01 18:29
L6	13	5 same 3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/01 18:37
L7	0	6 and 1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/01 18:37
L8	0	5 and 3 and 1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/01 18:37
L9	788	(714/11).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/01 18:38
L10	364	(714/12).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/01 18:38
L11	683	(714/13).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/01 18:38
L12	672	(714/10).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/01 18:38

L13	103	(712/31).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/01 18:38
L14	29	(L9 L10 L11 L12 L13) and 3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/01 18:38
L15	5	14 and 4 and 5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/01 18:38
L16	3	("advanced configuration and power interface" ACPI) and 1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/01 18:43
L17	34872	(pair spare slave redundan$4 backup back-up "back up" second$4) adj2 processor	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/01 18:44
L18	126820	firmware	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/01 18:44
L19	19	L17 and L18 and 3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/01 18:44
L20	0	19 and 1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/01 18:45

S1	14	(("7085959") or ("20050172164") or ("5675794") or ("6438687") or ("6920581") or ("5915082") or ("6625749")).PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/08/26 17:54
S2	2	("7085959").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/08/27 15:05
S3	730	(714/11).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/27 15:06
S4	337	(714/12).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 15:32
S5	606	(714/13).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/27 15:07
S6	36	("20020144177" | "20030070050" | "20040006722" | "20040019771" | "20040153857" | "5226152" | "5249188" | "5751932" | "5758058" | "5764660" | "6065135" | "6148348" | "6473869" | "6560682" | "6604177" | "6615366" | "6625749" | "6687851" | "6754787").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/27 15:08
S7	44	("20020144177" | "20030070050" | "20040006722" | "20040019771" | "20040153857" | "6625749" | "6687851" | "6754787")".PN"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/27 15:09

S9	2222	lockstep lock-step	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 15:21
S11	25008	(loss adj S9) LOL	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 15:22
S12	51	(detect$3 or track$4) adj S11	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 15:23
S13	1547	(boot$4 or initializ$4) adj processor	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 16:41
S14	246	spare adj processor	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 15:27
S15	12	S12 and S13 and S14	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 15:30
S16	25	(michaelis-scott$ or myer-sylvia$ or mchardy-william$).in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 16:14
S18	632	(714/10).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 15:33

S19	95	(712/31).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 16:08
S20	52536	(switch$4 chang$4 failover fail-over "fail over") same (spare slave redundan$4 backup back-up "back up" second$4) same processor	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 16:54
S21	81	S20 same S13	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 16:28
S22	168219	without same ("shut$4 down" stop$4 idle interrupt$4) same (OS "operating system")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 16:33
S23	6	S21 and S22	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 16:33
S24	20342	multi-processor "multi processor" and S11 and S13	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 16:45
S25	176	S24 and S20 and S22	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 16:46
S26	7	S25 and S14	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 16:53

S27	87	(recover$4 reestablish$3 restart$3) with S9	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 16:54
S28	31827	(pair spare slave redundan$4 backup back-up "back up" second$4) adj2 processor	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 16:55
S29	101834	firmware	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 16:56
S30	21	S27 and S28 and S29	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 16:57
S31	15153	trigger$3 same ("operating system" OS operating-system) same (idle stop$4 interrupt$3 halt$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/02/14 14:49
S32	207	(loss lose los$3 lost$3) same (lockstep lock-step "lock step")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/02/14 14:52
S33	86	(detect$3 track$3 monitor$3) same S32	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/02/14 14:56
S34	3	S33 same S31	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/02/14 14:56

S35	3	S32 same S31	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/02/14 15:02
S36	10	S32 and S31	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/02/14 15:02
S37	33339	(pair spare slave redundan$4 backup back-up "back up" second$4) adj2 processor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/02/14 15:05
S38	2323	lockstep lock-step	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/02/14 15:06
S39	92	(recover$4 reestablish$3 restart$3) with S38	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/02/14 15:06
S40	114677	firmware	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/02/14 15:06
S41	11	S37 same S39 same S40	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/02/14 15:06
S42	764	(714/11).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/02/14 15:07

S43	352	(714/12).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/02/14 15:07
S44	659	(714/13).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/02/14 15:07
S45	658	(714/10).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/02/14 15:07
S46	96	(712/31).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/02/14 15:07
S47	2	(S42 S43 S44 S45 S46) and S31 and S33	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/02/14 15:07
S48	2	(S42 S43 S44 S45 S46) and S31 and S32 and S37 and S40	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/02/14 15:08

7/1/08 6:45:28 PM
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EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	23	(("6161770") or ("6675324") or ("6948092") or ("7003691") or ("7155721") or ("7237144") or ("7251746") or ("20030051190") or ("20040019771") or ("20040006722") or ("20040078650")).PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/07/02 08:49
L2	214	(loss lose los$3 lost$3) same (lockstep lock-step "lock step")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/02 09:12
L3	91	(detect$3 track$3 monitor $3) same L2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/02 09:12
L4	126820	firmware	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/02 09:12
L5	2632	(recover$4 reestablish$3 restart$3) same L4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/02 09:12
L6	13	L5 same L3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/02 09:12
L7	34872	(pair spare slave redundan $4 backup back-up "back up" second$4) adj2 processor	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/02 09:13

L8	13	L7 and 6	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/02 09:13
L9	0	1 and 8	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/02 09:14
L10	16	3 and 5 and 7	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/02 09:15
L11	0	10 and 1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/02 09:15
L12	788	(714/11).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/02 09:17
L13	364	(714/12).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/02 09:17
L14	683	(714/13).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/02 09:17
L15	672	(714/10).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/02 09:17

L16	103	(712/31).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/02 09:17
L17	352	(L12 L13 L14 L15 L16) and firmware	US-PGPUB; USPAT; USOCR	OR	ON	2008/07/02 09:17
L18	11	17 and ((loss lose los$3 lost$3) same (lockstep lock-step "lock step"))	US-PGPUB; USPAT; USOCR	OR	ON	2008/07/02 09:17
L20	10	18 and 7	US-PGPUB; USPAT; USOCR	OR	ON	2008/07/02 09:25

7/2/08 9:27:17 AM
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PTO/SB/08a (01-08)
Approved for use through 05/31/2008. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet | | of | |

Complete if Known	
Application Number	10/973,076
Filing Date	October 25, 2004
First Named Inventor	Scott L. Michaelis et al.
Art Unit	2114
Examiner Name	Dieu Minh T. Le
Attorney Docket Number	200404941-1

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/M.L./		US- 6,141,770	10-31-2000	Fuchs et al.	
		US- 6,675,324	01-06-2004	Marisetty et al.	
		US- 6,948,092	09-20-2005	Kondo et al.	
		US- 7,003,691	02-21-2006	Safford et al.	
		US- 7,155,721	12-26-2006	Safford et al.	
		US- 7,237,144	06-26-2007	Safford et al.	
		US- 7,251,746	07-31-2007	Fox et al.	
		US- 2003/0051190	03-13-2003	Marisetty et al.	
		US- 2004/0019771	01-29-2004	Quach	
		US- 2004/0006722	01-08-2004	Safford	
/M.L./		US- 2004/0078650	04-22-2008	Safford et al.	
		US-			
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		US-			

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]

Examiner Signature	/Dieu Minh Le/	Date Considered	07/01/2008

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, Colorado 80527-2400

PATENT APPLICATION

ATTORNEY DOCKET NO. 200404941-1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Scott L. Michaelis et al.

Confirmation No.: 6989

Application No.: 10/973,076

Examiner: Dieu Minh T. Le

Filing Date: October 25, 2004

Group Art Unit: 2144

Title: SYSTEM AND METHOD FOR PROVIDING FIRMWARE RECOVERABLE LOCKSTEP PROTECTION

Mail Stop RCE
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

REQUEST FOR CONTINUED EXAMINATION (RCE) 37 CFR 1.114

Subsection (b) of 35 U.S.C. 132, effective on May 29, 2000, provides for continued examination of a utiltity or plant application filed on or after June 8, 1995.
See The American Inventors Protection Act of 1999 (AIPA).

This is a Request for Continued Examination (RCE) under CFR 1.114 of the above-identified application.

NOTE: 37 CFR 1.114 is effective on May 20, 2000. If the above- application was filed prior to May 29, 2000, applicant may wish to consider filing a continued prosecution application (CPA) under CFR 1.53(d) (PTO/SB/29) instead of a RCE to be eligible for the patent term adjustment provisions of the AIPA. See Changes to Application Examination and Provisional Application Practice, Interim Rule, 65 Fed. Reg. 14865 (Mar. 20, 2000), 1233 off. Gaz. Pat. Office

Submission under 37 CFR 1.114

☐ Previously submitted

- ☐ Consider the amendment(s)/reply under 37 CFR 1.116 previously filed on _____.
  (Any unentered amendment(s) referred to above will be entered).
- ☐ Consider the arguments in the Appeal Brief or Reply Brief prevously filed on _____.
- ☐ Other _____

☒ Enclosed

- ☐ Amendment/Reply
- ☐ Affidavit(s)/Declaration(s)
- ☒ Information Disclosure Statement (IDS)
- ☐ Other _____

Miscellaneous

- ☐ Suspension of action is requested under 37 CFR 1.103(c) for a period of _____ months.
  The fee for this Suspension is (37 CFR 1.17(i)) $130.00
- ☐ Other _____

☒ RCE filing fee $810.00

☐ A Petition for Extension of Time

☐ 1st Month $120 ☐ 2nd Month $460 ☐ 3rd Month $1050 ☐ 4th Month $1640

☐ Please charge to Deposit Account 08-2025 the sum of $ 810 . At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that my regulate fees.

Respectfully submitted,

Scott L. Michaelis et al.

By: /Robert W. Nelson/

Robert W. Nelson

Attorney/Agent for Applicant(s)

Reg No. : 37,898

Date : June 6, 2008

Telephone : (303) 298-9888

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, Colorado 80527-2400

PATENT APPLICATION

ATTORNEY DOCKET NO. 200404941-1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Scott L. Michaelis et al.

Confirmation No.: 6989

Application No.: 10/973,076

Examiner: Dieu-Minh Le

Filing Date: October 25, 2004

Group Art Unit: 2114

Title: SYSTEM AND METHOD FOR PROVIDING FIRMWARE RECOVERABLE LOCKSTEP PROTECTION

Mail Stop Amendment
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

This Information Disclosure Statement is submitted:

☒ under 37 CFR 1.97 (b), or
(Within three months of filing national application; or date of entry of national application; or before mailing date of first action on the merits; whichever occurs last)

☐ under 37 CFR 1.97 (c), together with either a:
- ☐ Statement under 37 CFR 1.97 (e), or
- ☐ a $180 fee under 37 CFR 1.17 (p), or

(After the CFR 1.97 (b) time period, but before final action or notice of allowance, whichever occurs first)

☐ under 37 CFR 1.97 (d), together with a:
- ☐ Statement under 37 CFR 1.97 (e)(1) or (2), and
- ☐ a $180 fee set forh in 37 CFR 1.17 (p)

(Filed after final action, a notice of allowance, on or before payment of the issue fee)

Please charge to Deposit Account **08-2025** the sum of $ 0.00 . At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account **08-2025** pursuant to 37 CFR 1.25.

Applicant(s) submit herewith form PTO/SB/08B - Information Disclosure Statement together with any required copies of patents, publications or other information of which applicant(s) are aware, which applicant(s) believe(s) may be material to the examination of this application and for which there may be a duty to disclose in accordance with 37 CFR 1.56.

☐ A concise explanation of the relevance of foreign language patents, foreign language publications and other foreign language information listed on PTO/SB/08B, as presently understood by the individual(s) designated in 37 CFR 1.56 (c) most knowledgeable about the content is given on the attached sheet, or where a foreign language patent is cited in a search report or other action by a foreign patent office in a counterpart foreign application, an english language version of the search report or action which indicates the degree of relevance found by the foreign office is listed on form PTO/SB/08B and is enclosed.

It is requested that the information disclosed herein be made of record in this application.

Respectfully submitted,

Scott L. Michaelis et al.

By: /Robert W. Nelson/

Robert W. Nelson

Attorney/Agent for Applicant(s)

Reg No. : 37,898

Date : June 6, 2005

Telephone : (303) 298-9888

Rev 10/07 (E-IDS)

PTO/SB/08a (01-08)
Approved for use through 05/31/2008. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet | | of | |

Complete if Known	
Application Number	10/973,076
Filing Date	October 25, 2004
First Named Inventor	Scott L. Michaelis et al.
Art Unit	2114
Examiner Name	Dieu Minh T. Le
Attorney Docket Number	200404941-1

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US- 6,141,770	10-31-2000	Fuchs et al.	
		US- 6,675,324	01-06-2004	Marisetty et al.	
		US- 6,948,092	09-20-2005	Kondo et al.	
		US- 7,003,691	02-21-2006	Safford et al.	
		US- 7,155,721	12-26-2006	Safford et al.	
		US- 7,237,144	06-26-2007	Safford et al.	
		US- 7,251,746	07-31-2007	Fox et al.	
		US- 2003/0051190	03-13-2003	Marisetty et al.	
		US- 2004/0019771	01-29-2004	Quach	
		US- 2004/0006722	01-08-2004	Safford	
		US- 2004/0078650	04-22-2008	Safford et al.	
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

Electronic Patent Application Fee Transmittal

Application Number:	10973076
Filing Date:	25-Oct-2004
Title of Invention:	SYSTEM AND METHOD FOR PROVIDING FIRMWARE RECOVERABLE LOCKSTEP PROTECTION
First Named Inventor/Applicant Name:	Scott L. Michaelis
Filer:	Robert Wayne Nelson/Joy Reinhart
Attorney Docket Number:	200404941-1

Filed as Large Entity

Utility Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Request for continued examination	1801	1	810	810
Total in USD ($)				**810**

Electronic Acknowledgement Receipt

EFS ID:	3415192
Application Number:	10973076
International Application Number:	
Confirmation Number:	6989
Title of Invention:	SYSTEM AND METHOD FOR PROVIDING FIRMWARE RECOVERABLE LOCKSTEP PROTECTION
First Named Inventor/Applicant Name:	Scott L. Michaelis
Customer Number:	22879
Filer:	Robert Wayne Nelson/Joy Reinhart
Filer Authorized By:	Robert Wayne Nelson
Attorney Docket Number:	200404941-1
Receipt Date:	06-JUN-2008
Filing Date:	25-OCT-2004
Time Stamp:	12:59:52
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Continued Examination (RCE)	RCE.pdf	146123 76ee82fe9d2b225f1f4654b2a881698a3b0050d5	no	2

Warnings:

This is not a USPTO supplied RCE SB30 form.					
Information:					
2	Information Disclosure Statement (IDS) Filed	IDS.pdf	303396 89c51b318c3e79858b2e02d517fd9af641e54a9b	no	2
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
3	Fee Worksheet (PTO-06)	fee-info.pdf	8220 7605b5d7089851605e897d2b82611917965117 45	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	457739	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

22879 7590 06/03/2008

HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER	
LE, DIEU MINH T	
ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 06/03/2008

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/973,076	10/25/2004	Scott L. Michaelis	200404941-1	6989

TITLE OF INVENTION: SYSTEM AND METHOD FOR PROVIDING FIRMWARE RECOVERABLE LOCKSTEP PROTECTION

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1440	$300	$0	$1740	09/03/2008

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

22879 7590 06/03/2008

HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)

(Signature)

(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/973,076	10/25/2004	Scott L. Michaelis	200404941-1	6989

TITLE OF INVENTION: SYSTEM AND METHOD FOR PROVIDING FIRMWARE RECOVERABLE LOCKSTEP PROTECTION

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1440	$300	$0	$1740	09/03/2008

EXAMINER	ART UNIT	CLASS-SUBCLASS
LE, DIEU MINH T	2114	714-012000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1_____

2_____

3_____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/973,076	10/25/2004	Scott L. Michaelis	200404941-1	6989

22879 7590 06/03/2008

HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER
LE, DIEU MINH T

ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 06/03/2008

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 626 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 626 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

Notice of Allowability	Application No.	Applicant(s)	
	10/973,076	MICHAELIS ET AL.	
	Examiner	Art Unit	
	Dieu-Minh Le	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *to the communication filed on 4/10/08 and interview on 5/12/2008* .

2. ☒ The allowed claim(s) is/are *1-6, 9-22, 24-28 [now as 1-25]*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/DIEU-MINH THAI LE/
PRIMARY EXAMINER
ART UNIT 2114

Interview Summary	Application No.	Applicant(s)	
	10/973,076	MICHAELIS ET AL.	
	Examiner	Art Unit	
	Dieu-Minh Le	2114	

All participants (applicant, applicant's representative, PTO personnel):

(1) *Dieu-Minh Le*. (3)_____.

(2) *Steven Webb*. (4)_____.

Date of Interview: *12 May 2008*.

Type: a)☒ Telephonic b)☐ Video Conference
c)☐ Personal [copy given to: 1)☐ applicant 2)☐ applicant's representative]

Exhibit shown or demonstration conducted: d)☐ Yes e)☒ No.
If Yes, brief description: _____.

Claim(s) discussed: *1-6,9-22 and 24-28*.

Identification of prior art discussed: *none*.

Agreement with respect to the claims f)☒ was reached. g)☐ was not reached. h)☐ N/A.

Substance of Interview including description of the general nature of what was agreed to if an agreement was reached, or any other comments: *Main issue discussed was 35 USC 101 in claim 21. Applicant's representative agreed to amend the claims according to examiner's amendment*.

(A fuller description, if necessary, and a copy of the amendments which the examiner agreed would render the claims allowable, if available, must be attached. Also, where no copy of the amendments that would render the claims allowable is available, a summary thereof must be attached.)

THE FORMAL WRITTEN REPLY TO THE LAST OFFICE ACTION MUST INCLUDE THE SUBSTANCE OF THE INTERVIEW. (See MPEP Section 713.04). If a reply to the last Office action has already been filed, APPLICANT IS GIVEN A NON-EXTENDABLE PERIOD OF THE LONGER OF ONE MONTH OR THIRTY DAYS FROM THIS INTERVIEW DATE, OR THE MAILING DATE OF THIS INTERVIEW SUMMARY FORM, WHICHEVER IS LATER, TO FILE A STATEMENT OF THE SUBSTANCE OF THE INTERVIEW. See Summary of Record of Interview requirements on reverse side or on attached sheet.

/DIEU-MINH LE/

Examiner Note: You must sign this form unless it is an Attachment to a signed Office action.

Examiner's signature, if required

1. This office action is in response to the communication filed on 04/10/2008 and the Interview on 05/12/2008.

2. Claims 1-6, 9-22, and 24-28 [now as 1-25] are allowable over the prior art of record.

3. An Examiner's Amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 C.F.R. § 1.312. To ensure consideration of such an amendment, it **MUST** be submitted no later than the payment of the Issue Fee.

EXAMINER'S AMENDMENT:

IN THE CLAIMS:

Please replace all prior versions of claims in the application with the current listing claims in the **ATTACHMENT:**

4. Authorization for this Examiner's Amendment was given in a telephone interview with Mr. Steven Webb Registration No. 44,395 on 05/12/2008.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dieu-Minh Le whose telephone number is (571) 272-

3660. The examiner can normally be reached on Monday - Thursday from 8:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571)272-3644. The Tech Center 2100 phone number is (571) 272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Dieu-Minh Thai Le/
DIEU-MINH THAI LE
PRIMARY EXAMINER
ART UNIT 2114

DML.
05/12/2008

ATTACHMENT:

LISTING OF CLAIMS:

1. (Currently amended) A method comprising:

detecting loss of lockstep for a lockstep pair of processors; ~~and~~

using firmware to trigger an operating system to idle the lockstep pair of processors, recover lockstep for the lockstep pair of processors, and trigger the operating system to recognize the lockstep pair of processors having recovered lockstep; and

responsive to said detecting loss of lockstep, using said firmware to determine if lockstep is recoverable for the lockstep pair of processors, wherein said using said firmware to determine if lockstep is recoverable further comprises determining if a lockstep mismatch has occurred between the lockstep pair of processors.

2. (Original) The method of claim 1 wherein said using firmware to trigger an operating system to idle the lockstep pair of processors further comprises:

using the firmware to trigger the operating system to idle a master processor of the lockstep pair of processors.

3. (Original) The method of claim 2 wherein said using firmware to trigger the operating system to recognize the lockstep pair of processors having recovered lockstep further comprises:

using the firmware to trigger the operating system to recognize the master of the lockstep pair of processors.

4. (Original) The method of claim 1 wherein said detecting loss of lockstep comprises:

detecting corrupt data in one of said lockstep pair of processors that would lead to a lockstep mismatch if acted upon.

5. (Original) The method of claim 1 wherein said detecting loss of lockstep comprises:

detecting a precursor to lockstep mismatch.

6. (Original) The method of claim 1 wherein said detecting loss of lockstep comprises:

detecting lockstep mismatch between the lockstep pair of processors.

7-8. (Cancelled)

9. (Currently amended) The method of claim [[8]] 1 further comprising:

if determined that a lockstep mismatch has not occurred between the lockstep pair of processors, then determining that the loss of lockstep is recoverable.

10. (Currently amended) The method of claim [[8]] 1 further comprising:

if determined that a lockstep mismatch has occurred between the lockstep pair of processors, then determining that the loss of lockstep is not recoverable.

11. (Original) The method of claim 1 further comprising:

determining if said lockstep pair of processors for which said loss of lockstep is detected comprises a system boot processor.

12. (Original) The method of claim 11 wherein if determined that said lockstep pair of processors for which said loss of lockstep is detected comprises a system boot processor, further comprising:

swapping the role of system boot processor to another processor in the system.

13. (Original) The method of claim 12 further comprising:

after said swapping, recovering the lockstep for the lockstep pair of processors.

14. (Original) The method of claim 13 further comprising:

after recovering lockstep for the lockstep pair of processors, holding the recovered pair of processors in idle as a spare for the processor to which the role of system boot processor was swapped.

15. (Original) A system comprising:

an Advanced Configuration and Power Interface (ACPI)-compatible operating system;

master processor operable to process instructions scheduled by said ACPI-compatible operating system;

slave processor lockstepped with the master processor operable to perform redundant processing of said instructions scheduled for the master processor; and

firmware operable, responsive to detection of loss of lockstep between the master and slave processors, to use an ACPI method to trigger the operating system to idle the master processor, attempt to recover lockstep between the master and slave processors, and if recovery of lockstep is successful then use an ACPI method to reintroduce the master processor to the operating system.

16. (Original) The system of claim 15 further comprising:

error detection logic for detecting loss of lockstep between the master and slave processors.

17. (Original) The system of claim 15 further comprising:

error detection logic for detecting a precursor to loss of lockstep.

18. (Original) The system of claim 17 wherein said precursor to loss of lockstep is treated as said detection of loss of lockstep.

19. (Original) The system of claim 17 wherein said error detection logic comprises a parity-based mechanism.

20. (Original) The system of claim 15 further comprising error detection logic for detecting lockstep mismatch between the master and slave processors.

21. (Currently amended) A system comprising a pair of lockstep processors and ~~firmware that includes~~ computer-executable ~~software~~ firmware code stored to a computer-readable medium, the computer-executable ~~software~~ firmware code comprising:

firmware code, responsive to detection of loss of lockstep between ~~a~~ the pair of lockstep processors, for determining if the lockstep is recoverable for the pair of lockstep processors, wherein said firmware code for determining if the lockstep is recoverable further comprises firmware code for determining if a lockstep mismatch has occurred between the pair of lockstep processors; and

firmware code, responsive to determining that the lockstep is recoverable, for triggering an operating system to idle the processors, attempting to recover lockstep between the pair of processors, and if lockstep is successfully recovered between the pair of processors, triggering said operating system to recognize the processors as being available for receiving instructions.

22. (Original) The system of claim 21 wherein the code for attempting to recover lockstep further comprises:

code for resetting the pair of processors.

23. (Cancelled)

24. (Original) The system of claim 21 wherein said operating system is an Advanced Configuration and Power Interface (ACPI)-compatible operating system, said code for triggering the operating system to idle the processors comprises:

code for using an ACPI method to idle the processors.

25. (Original) The system of claim 21 wherein said operating system is an Advanced Configuration and Power Interface (ACPI)-compatible operating system, said code for triggering said operating system to recognize the processors as being available for receiving instructions comprises:

code for using an ACPI method to cause the operating system to check for the processors.

26. (Original) A method comprising:

establishing, in a multi-processor system, a hot spare processor for a system boot processor;

detecting loss of lockstep for a lockstep pair of processors in said multi-processor system;

determining if said lockstep pair of processors for which the loss of lockstep is detected is the system boot processor;

if determined that said lockstep pair of processors for which the loss of lockstep is the system boot processor, copying a state of the system boot processor to the hot spare processor; and

if determined that said lockstep pair of processors for which the loss of lockstep is not the system boot processor, then triggering an operating system to a) idle the lockstep pair of processors, b) attempt to recover lockstep between the lockstep pair of processors, and c) if lockstep is successfully recovered between the lockstep pair of processors, trigger said operating system to recognize the processors as being available for receiving instructions.

27. (Original) The method of claim 26 wherein if determined that said lockstep pair of processors for which the loss of lockstep is the system boot processor further comprising:

attempting to recover lockstep between the lockstep pair of processors after copying the state of the system boot processor to the hot spare processor.

28. (Original) The method of claim 27 wherein if determined that said lockstep pair of processors for which the loss of lockstep is the system boot processor further comprising:

if lockstep is successfully recovered between the lockstep pair of processors, establishing the lockstep pair of processors for which lockstep was recovered as a hot spare processor.

29-35. (Cancelled)

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10973076	MICHAELIS ET AL.
	Examiner	**Art Unit**
	Dieu-Minh Le	2114

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	02/14/2008	05/13/2008							
1	1	✓	=							
2	2	✓	=							
3	3	✓	=							
4	4	✓	=							
5	5	✓	=							
6	6	✓	=							
	7	✓	-							
	8	O	-							
7	9	O	=							
8	10	O	=							
9	11	✓	=							
10	12	✓	=							
11	13	✓	=							
12	14	O	=							
13	15	=	=							
14	16	=	=							
15	17	=	=							
16	18	=	=							
17	19	=	=							
18	20	=	=							
19	21	✓	=							
20	22	✓	=							
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21	24	✓	=							
22	25	✓	=							
23	26	=	=							
24	27	=	=							
25	28	=	=							
	29	✓	-							
	30	✓	-							
	31	✓	-							
	32	✓	-							
	33	O	-							
	34	✓	-							
	35	✓	-							

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10973076	MICHAELIS ET AL.
	Examiner	**Art Unit**
	Dieu-Minh Le	2114

ORIGINAL		INTERNATIONAL CLASSIFICATION	
CLASS	SUBCLASS	CLAIMED	NON-CLAIMED
714	12	G 0 6 F 11 / 00 (2006.01.01)	

CROSS REFERENCE(S)

CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
712	31				

NONE (Assistant Examiner) (Date)		Total Claims Allowed: 25	
/Dieu-Minh Le/ (Primary Examiner)	5/12/08 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 1

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10973076	MICHAELIS ET AL.
	Examiner	**Art Unit**
	Dieu-Minh Le	2114

SEARCHED

Class	Subclass	Date	Examiner
714	10-13; 712/31	2/14/2008	dml
714	(upadated the above search)	5/12/08	dml

SEARCH NOTES

Search Notes	Date	Examiner
EAST search all files updated.	2/14/2008	dml
East search updated	5/12/08	dml
Inventor names search	5/12/08	dml
NPL search [files IEEE, Google scholar]	5/12/08	dml

INTERFERENCE SEARCH

Class	Subclass	Date	Examiner
714	10-112	5/12/08	dml
	Interference text search - see data file		

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CONFIRMATION NO. 6989

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
10/973,076	10/25/2004 **RULE**	714	2114	200404941-1

APPLICANTS

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Anurupa Rajkumari, Round Rock, TX;
William B. McHardy, Fort Collins, CO;

**** CONTINUING DATA **************************

**** FOREIGN APPLICATIONS **************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****
12/08/2004

Foreign Priority claimed	35 USC 119(a-d) conditions met	Verified and Acknowledged	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
☐ Yes ☑ No	☐ Yes ☑ No	/DIEU-MINH T LE/ (Examiner's Signature)	TX	5	~~35~~ 25	~~5~~ 4
		☐ Met after Allowance dml (Initials)				

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INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400
UNITED STATES

TITLE

System and method for providing firmware recoverable lockstep protection

FILING FEE RECEIVED		
1236	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	28	(michaelis-scott$ or myer-sylvia$ or mchardy-william$).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/11 17:01
L2	15230	trigger$3 same ("operating system" OS operating-system) same (idle stop$4 interrupt$3 halt$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/11 17:02
L3	214	(loss lose los$3 lost$3) same (lockstep lock-step "lock step")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/11 17:02
L4	91	(detect$3 track$3 monitor$3) same L3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/11 17:02
L5	781	(714/11).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/11 17:02
L6	360	(714/12).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/11 17:02
L7	670	(714/13).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/11 17:02
L8	665	(714/10).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/11 17:02
L9	98	(712/31).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/11 17:02

L10	4	(L5 L6 L7 L8 L9) and L2 and L4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/11 17:02
L11	34280	(pair spare slave redundan$4 backup back-up "back up" second$4) adj2 processor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/11 17:03
L12	2381	lockstep lock-step	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/11 17:03
L13	481	L11 and L12	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/11 17:03
L14	94	(recover$4 reestablish $3 restart$3) with L12	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/11 17:03
L15	121775	firmware	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/11 17:03
L16	26	13 and L14 and L15	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/11 17:03
L17	36	("20020144177" | "20030070050" | "20040006722" | "20040019771" | "20040153857" | "5226152" | "5249188" | "5751932" | "5758058" | "5764660" | "6065135" | "6148348" | "6473869" | "6560682" | "6604177" | "6615366" | "6625749" | "6687851" | "6754787").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/11 17:04

L18	57	("20020144177" | "20030070050" | "20040006722" | "20040019771" | "20040153857" | "6625749" | "6687851" | "6754787")".PN"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/11 17:04
L19	79	L17 L18	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/11 17:04
L20	32	15 and 19	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/11 17:05
L21	4	20 and 4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/11 17:06
L22	2	21 and 2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/11 17:06

5/11/08 5:07:25 PM
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EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	34280	(pair spare slave redundan$4 backup back-up "back up" second $4) adj2 processor	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/11 22:19
L2	214	(loss lose los$3 lost $3) same (lockstep lock-step "lock step")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/11 22:19
L3	12	mismatch$3 same L1 same L2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/11 22:19
L5	2	3 same recover$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/11 22:21
L6	2318	(advanced adj configuration adj2 power adj interface) ACPI	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/11 22:23
L7	23105	(master pair spare slave redundan$4 backup back-up "back up" second $4) adj processor	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/11 22:24
L8	9	7 same 6 same (lockstep lock-step "lock step")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/11 22:25
L9	9	8 same firmware	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/11 22:26
L10	781	(714/11).ccls.	US-PGPUB; USPAT; USOCR	OR	ON	2008/05/11 22:27

L11	360	(714/12).ccls.	US-PGPUB; USPAT; USOCR	OR	ON	2008/05/11 22:27
L12	670	(714/13).ccls.	US-PGPUB; USPAT; USOCR	OR	ON	2008/05/11 22:27
L13	546	(714/10).ccls.	US-PGPUB; USPAT; USOCR	OR	ON	2008/05/11 22:27
L14	22	(detect$3 track$3 monitor$3) same 2 same 1	US-PGPUB; USPAT; USOCR	OR	ON	2008/05/11 22:37
L15	10	14 and 10	US-PGPUB; USPAT; USOCR	OR	ON	2008/05/11 22:38
L16	6	14 and (11 12 13)	US-PGPUB; USPAT; USOCR	OR	ON	2008/05/11 22:38
L17	12	15 16	US-PGPUB; USPAT; USOCR	OR	ON	2008/05/11 22:38
L18	4	17 and 6	US-PGPUB; USPAT; USOCR	OR	ON	2008/05/11 22:39

5/11/08 10:40:01 PM
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HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P. O. Box 272400
Fort Collins, Colorado 80527-2400

PATENT APPLICATION

ATTORNEY DOCKET NO. 200404941-1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Scott L. Michaelis et al. **Confirmation No.:**

Application No.: **Examiner:**

Filing Date: **Group Art Unit:**

Title: SYSTEM AND METHOD FOR PROVIDING FIRMWARE RECOVERABLE LOCKSTEP PROTECTION

Mail Stop Amendment
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

This Information Disclosure Statement is submitted:

(X) under 37 CFR 1.97(b), or
(Within three months of filing national application; or date of entry of national application; or before mailing date of first office action on the merits; whichever occurs last)

( ) under 37 CFR 1.97(c) together with either a:
( ) Statement under 37 CFR 1.97(e), or
( ) a $180.00 fee under 37 CFR 1.17(p), or
(After the CFR 1.97 (b) time period, but before final action or notice of allowance, whichever occurs first)

( ) under 37 CFR 1.97 (d) together with a:
( ) Statement under 37 CFR 1.97(e)(1) or (2), and
( ) a $180.00 fee set forth in 37 CFR 1.17(p).
(Filed after final action, a notice of allowance, on or before payment of the issue fee)

Please charge to Deposit Account **08-2025** the sum of $0.00 . At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account **08-2025** pursuant to 37 CFR 1.25.

(X) Applicant(s) submit herewith Form PTO 1449 - Information Disclosure Statement together with any required copies of patents, publications or other information of which applicant(s) are aware, which applicant(s) believe(s) may be material to the examination of this application and for which there may be a duty to disclose in accordance with 37 CFR 1.56.

( ) A concise explanation of the relevance of foreign language patents, foreign language publications and other foreign language information listed on PTO Form 1449, as presently understood by the individuals(s) designated in 37 CFR 1.56 (c) most knowledgeable about the content is given on the attached sheet, or where a foreign language patent is cited in a search report or other action by a foreign patent office in a counterpart foreign application, an English language version of the search report or action which indicates the degree of relevance found by the foreign office is listed on form PTO 1449 and is enclosed herewith.

It is requested that the information disclosed herein be made of record in this application.

"Express Mail" label no. **EV 375345153US**

Date of Deposit **Oct. 25, 2004**

I hereby certify that this is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to: Commissioner for Patents, Alexandria, VA 22313-1450.

By

Typed Name: **Phyllis Ewing**

Respectfully submitted,

Scott L. Michaelis et al.

By

Jody C. Bishop

Attorney/Agent for Applicant(s)
Reg. No. **44,034**

Date: **Oct. 25, 2004**

Telephone No.: **(214) 855-8007**

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.L./

FORM PTO-1449 LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	ATTY. DOCKET NO. 200404941-1	APPLICATION NO.	CONFIRMATION NO.
	APPLICANT Scott L. Michaelis et al.		
	FILING DATE	GROUP	

REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	1A	5,226,152	07/06/1993	Klug et al.	
	1B	5,249,188	09/28/1993	McDonald	
	1C	5,751,932	05/12/1998	Horst et al.	
	1D	5,758,058	05/26/1998	Milburn	
	1E	5,764,660	06/09/1998	Mohat	
	1F	6,065,135	05/16/2000	Marshall et al.	
	1G	6,148,348	11/14/2000	Garnett et al.	
	1H	6,473,869	10/29/2002	Bissett et al.	
	1I	6,560,682	05/06/2003	Miller et al.	
	1J	6,604,177	08/05/2003	Kondo et al.	
	1K	6,615,366	09/02/2003	Grochowski et al.	

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	1L					
	1M					
	1N					
	1O					
	1P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

	1Q	Attorney Docket No. 200404946-1, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR USING INFORMATION RELATING TO A DETECTED LOSS OF LOCKSTEP FOR DETERMINING A RESPONSIVE ACTION "
	1R	Attorney Docket No. 200404944-1, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR ESTABLISHING A SPARE PROCESSOR FOR RECOVERING FROM LOSS OF LOCKSTEP IN A BOOT PROCESSOR"
	1S	Attorney Docket No. 200404943-1, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR CONFIGURING LOCKSTEP MODE OF A PROCESSOR MODULE"

EXAMINER	DATE CONSIDERED
/Dieu Minh Le/	05/11/2008

~~ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH.~~ /M.L./

FORM PTO-1449 LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	ATTY. DOCKET NO. **200404941-1**	APPLICATION NO.	CONFIRMATION NO.
	APPLICANT **Scott L. Michaelis et al.**		
	FILING DATE	GROUP	

REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	2A	6,625,749	09/23/2003	Quach	
	2B	6,687,851	02/03/2004	Somers et al.	
	2C	6,754,787	06/22/2004	Miller et al.	
	2D	2002/0144177	10/03/2002	Kondo et al.	
	2E	2003/0070050	04/10/2003	Miller et al.	
	2F	2004/0006722	01/08/2004	Safford	
	2G	2004/0019771	01/29/2004	Quach	
	2H	2004/0153857	08/05/2004	Yamazaki et al.	
	2I				
	2J				
	2K				

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	2L					
	2M					
	2N					
	2O					
	2P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

	2Q	Attorney Docket No. 200404974-1, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR MAINTAINING IN A MULTI-PROCESSOR SYSTEM A SPARE PROCESSOR THAT IS IN LOCKSTEP FOR USE IN RECOVERING FROM LOSS OF LOCKSTEP FOR ANOTHER PROCESSOR
	2R	Attorney Docket No. 200404973-1, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR SWITCHING THE ROLE OF BOOT PROCESSOR TO A SPARE PROCESSOR RESPONSIVE TO DETECTION OF LOSS OF LOCKSTEP IN A BOOT PROCESSOR "
	2S	Attorney Docket No. 200404971-1, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR REESTABLISHING LOCKSTEP FOR A PROCESSOR MODULE FOR WHICH LOSS OF LOCKSTEP IS DETECTED"

EXAMINER	DATE CONSIDERED
/Dieu Minh Le/	05/11/2008

~~ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH.~~ /M.L./

FORM PTO-1449 LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	ATTY. DOCKET NO. **200404941-1**	APPLICATION NO.	CONFIRMATION NO.
	APPLICANT **Scott L. Michaelis et al.**		
	FILING DATE	GROUP	

REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	3A				
	3B				
	3C				
	3D				
	3E				
	3F				
	3G				
	3H				
	3I				
	3J				
	3K				

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	3L					
	3M					
	3N					
	3O					
	3P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

	3Q	Attorney Docket No. 200404970-1, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR SYSTEM FIRMWARE CAUSING AN OPERATING SYSTEM TO IDLE A PROCESSOR"
	3R	Attorney Docket No. 200404972-1, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR REINTRODUCING A PROCESSOR MODULE TO AN OPERATING SYSTEM AFTER LOCKSTEP RECOVERY"
	3S	

EXAMINER	DATE CONSIDERED
/Dieu Minh Le/	05/11/2008

~~ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH.~~ /M.L./

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:	)	
Scott L. Michaelis et al.	)	
Attorney Docket 200404941-1	)	Examiner: Dieu Minh T Le
Serial No. 10/973,076	)	Group Art Unit: 2114
Filing Date: October 25, 2004	)	Confirmation No. 6989
For: SYSTEM AND METHOD FOR PROVIDING FIRMWARE RECOVERABLE LOCKSTEP PROTECTION	)	

RESPONSE

To: Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office Action of February 27, 2008, please amend the above-identified application as set forth below.

Amendments to the claims begin on page 2 of this paper.

Remarks begin on page 9 of this paper.

In the Claims

1. (Currently amended) A method comprising:

detecting loss of lockstep for a lockstep pair of processors; ~~and~~

using firmware to trigger an operating system to idle the lockstep pair of processors, recover lockstep for the lockstep pair of processors, and trigger the operating system to recognize the lockstep pair of processors having recovered lockstep; and

responsive to said detecting loss of lockstep, using said firmware to determine if lockstep is recoverable for the lockstep pair of processors, wherein said using said firmware to determine if lockstep is recoverable further comprises determining if a lockstep mismatch has occurred between the lockstep pair of processors.

2. (Original) The method of claim 1 wherein said using firmware to trigger an operating system to idle the lockstep pair of processors further comprises:

using the firmware to trigger the operating system to idle a master processor of the lockstep pair of processors.

3. (Original) The method of claim 2 wherein said using firmware to trigger the operating system to recognize the lockstep pair of processors having recovered lockstep further comprises:

using the firmware to trigger the operating system to recognize the master of the lockstep pair of processors.

4. (Original) The method of claim 1 wherein said detecting loss of lockstep comprises:

detecting corrupt data in one of said lockstep pair of

processors that would lead to a lockstep mismatch if acted upon.

5. (Original) The method of claim 1 wherein said detecting loss of lockstep comprises:

detecting a precursor to lockstep mismatch.

6. (Original) The method of claim 1 wherein said detecting loss of lockstep comprises:

detecting lockstep mismatch between the lockstep pair of processors.

7-8. (Cancelled)

9. (Currently amended) The method of claim [[8]] 1 further comprising:

if determined that a lockstep mismatch has not occurred between the lockstep pair of processors, then determining that the loss of lockstep is recoverable.

10. (Currently amended) The method of claim [[8]] 1 further comprising:

if determined that a lockstep mismatch has occurred between the lockstep pair of processors, then determining that the loss of lockstep is not recoverable.

11. (Original) The method of claim 1 further comprising:

determining if said lockstep pair of processors for which said loss of lockstep is detected comprises a system boot processor.

12. (Original) The method of claim 11 wherein if determined that said lockstep pair of processors for which said loss of

lockstep is detected comprises a system boot processor, further comprising:

swapping the role of system boot processor to another processor in the system.

13. (Original) The method of claim 12 further comprising:

after said swapping, recovering the lockstep for the lockstep pair of processors.

14. (Original) The method of claim 13 further comprising:

after recovering lockstep for the lockstep pair of processors, holding the recovered pair of processors in idle as a spare for the processor to which the role of system boot processor was swapped.

15. (Original) A system comprising:

an Advanced Configuration and Power Interface (ACPI)-compatible operating system;

master processor operable to process instructions scheduled by said ACPI-compatible operating system;

slave processor lockstepped with the master processor operable to perform redundant processing of said instructions scheduled for the master processor; and

firmware operable, responsive to detection of loss of lockstep between the master and slave processors, to use an ACPI method to trigger the operating system to idle the master processor, attempt to recover lockstep between the master and slave processors, and if recovery of lockstep is successful then use an ACPI method to reintroduce the master processor to the operating system.

16. (Original) The system of claim 15 further comprising:

error detection logic for detecting loss of lockstep

between the master and slave processors.

17. (Original) The system of claim 15 further comprising:

error detection logic for detecting a precursor to loss of lockstep.

18. (Original) The system of claim 17 wherein said precursor to loss of lockstep is treated as said detection of loss of lockstep.

19. (Original) The system of claim 17 wherein said error detection logic comprises a parity-based mechanism.

20. (Original) The system of claim 15 further comprising error detection logic for detecting lockstep mismatch between the master and slave processors.

21. (Currently amended) A system comprising ~~firmware that includes~~ computer-executable ~~software~~ firmware code stored to a computer-readable medium, the computer-executable ~~software~~ firmware code comprising:

firmware code, responsive to detection of loss of lockstep between a pair of lockstep processors, for determining if the lockstep is recoverable for the pair of lockstep processors, wherein said firmware code for determining if the lockstep is recoverable further comprises firmware code for determining if a lockstep mismatch has occurred between the pair of lockstep processors; and

firmware code, responsive to determining that the lockstep is recoverable, for triggering an operating system to idle the processors, attempting to recover lockstep between the pair of processors, and if lockstep is successfully recovered between the pair of processors, triggering said

operating system to recognize the processors as being available for receiving instructions.

22. (Original) The system of claim 21 wherein the code for attempting to recover lockstep further comprises:

code for resetting the pair of processors.

23. (Cancelled)

24. (Original) The system of claim 21 wherein said operating system is an Advanced Configuration and Power Interface (ACPI)-compatible operating system, said code for triggering the operating system to idle the processors comprises:

code for using an ACPI method to idle the processors.

25. (Original) The system of claim 21 wherein said operating system is an Advanced Configuration and Power Interface (ACPI)-compatible operating system, said code for triggering said operating system to recognize the processors as being available for receiving instructions comprises:

code for using an ACPI method to cause the operating system to check for the processors.

26. (Original) A method comprising:

establishing, in a multi-processor system, a hot spare processor for a system boot processor;

detecting loss of lockstep for a lockstep pair of processors in said multi-processor system;

determining if said lockstep pair of processors for which the loss of lockstep is detected is the system boot processor;

if determined that said lockstep pair of processors for which the loss of lockstep is the system boot processor, copying a state of the system boot processor to the hot spare

processor; and

if determined that said lockstep pair of processors for which the loss of lockstep is not the system boot processor, then triggering an operating system to a) idle the lockstep pair of processors, b) attempt to recover lockstep between the lockstep pair of processors, and c) if lockstep is successfully recovered between the lockstep pair of processors, trigger said operating system to recognize the processors as being available for receiving instructions.

27. (Original) The method of claim 26 wherein if determined that said lockstep pair of processors for which the loss of lockstep is the system boot processor further comprising:

attempting to recover lockstep between the lockstep pair of processors after copying the state of the system boot processor to the hot spare processor.

28. (Original) The method of claim 27 wherein if determined that said lockstep pair of processors for which the loss of lockstep is the system boot processor further comprising:

if lockstep is successfully recovered between the lockstep pair of processors, establishing the lockstep pair of processors for which lockstep was recovered as a hot spare processor.

29-35. (Cancelled)

R E M A R K S

Claim 1, 9, 10 and 21 have been amended. Claims 7-8, 23 and 29-35 have been cancelled. Claims 2-6, 11-20, 22 and 24-28 stand as originally filed.

Claims 1-35 were considered in the Office Action.

Claims 1-7, 11-13, 21-25, 29-32, and 34-35 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Marshall et al., U.S. Patent 5,915,082 in view of Safford et al., U.S. Patent 7,085,959.

Claims 8-10, 14, and 33 stand objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 15-20 and 26-28 stand allowed.

Claim 1 has been amended to include all of the limitations of objected-to dependent claim 8 and intervening dependent claim 7. Claim 1 has thus been rewritten to contain all limitations that were indicated by the Examiner to be allowable in objected-to claim 8. Claim 1 and its dependent claims 2-6 and 9-14 are believed allowable for at least the reasons relied on by the Examiner with respect to claim 8.

Claim 21 has been also amended to substantially include all of the limitations of objected-to dependent claim 8. An element-by-element comparison of claims 1 and 21, as amended, illustrates that claim 21 is now allowable for at least the reasons that claim 8 is allowable:

(1) detecting loss of lockstep for a lockstep pair of processors

(21) detection of loss of lockstep between a pair of lockstep processors

(1) using firmware to trigger an operating system to idle the lockstep pair of processors
(21) firmware code ... for triggering an operating system to idle the processors

(1) using firmware to ... recover lockstep for the lockstep pair of processors
(21) firmware code ... to recover lockstep between the pair of processors

(1) using firmware to ... trigger the operating system to recognize the lockstep pair of processors having recovered lockstep
(21) firmware code ... for ... triggering said operating system to recognize the processors as being available for receiving instructions

(1) responsive to said detecting loss of lockstep, using said firmware to determine if lockstep is recoverable for the lockstep pair of processors
(21) firmware code, responsive to detection of loss of lockstep between a pair of lockstep processors, for determining if the lockstep is recoverable for the pair of lockstep processors

(1) wherein said using said firmware to determine if lockstep is recoverable further comprises determining if a lockstep mismatch has occurred between the lockstep pair of processors
(21) wherein said firmware code for determining if the lockstep is recoverable further comprises firmware code for determining if a lockstep mismatch has occurred between the pair of lockstep processors

Claim 21 has thus been rewritten to substantially contain all limitations that were indicated by the Examiner to be allowable in objected-to claim 8. Claim 21 and its dependent claims 22, 24 and 25 are believed allowable for at least the reasons relied on by the Examiner with respect to claim 8.

The remaining claims, as amended, are thus believed allowable as indicated by the Examiner. Claim sets 15-20 and 26-28 were previously allowed, and the independent claims of claim set 1-6, and 9-14 and claim set 21, 22, 24 and 25 have been amended to include all of the limitations of objected to claim 8.

In view of the above, all of the claims are believed to be in condition for allowance, and the Applicants respectfully request that a timely Notice of Allowance be issued.

Respectfully submitted,
KLAAS, LAW, O'MEARA & MALKIN, P.C.

By: /Guy K. Clinger/
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Electronic Acknowledgement Receipt

EFS ID:	3136474
Application Number:	10973076
International Application Number:	
Confirmation Number:	6989
Title of Invention:	System and method for providing firmware recoverable lockstep protection
First Named Inventor/Applicant Name:	Scott L. Michaelis
Customer Number:	22879
Filer:	Guy Kenneth Clinger/Angela Troussel
Filer Authorized By:	Guy Kenneth Clinger
Attorney Docket Number:	200404941-1
Receipt Date:	10-APR-2008
Filing Date:	25-OCT-2004
Time Stamp:	18:24:17
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	Transmittal.pdf	590529 05c5925172108b2b46322d0145b0c53a6986ee93	no	1

Warnings:

Information:

2	Amendment After Final	Amendment.pdf	75874 83044ae5548daec5707c6dd9c6adb72b62cb3592	no	1
Warnings:					
Information:					
3	Claims	Claims.pdf	75778 20f8d0380ba3bfde435ba2f740f298790e0bbdee	no	6
Warnings:					
Information:					
4	Applicant Arguments/Remarks Made in an Amendment	Remarks.pdf	75830 d3752d060c741fbdfe29695a397a443840b12716	no	3
Warnings:					
Information:					
			Total Files Size (in bytes):	818011	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, Colorado 80527-2400

PATENT APPLICATION

ATTORNEY DOCKET NO. 200404941-1

Inventor(s): Scott L. Michaelis et al.

Confirmation No.: 6989

Application No.: 10/973,076

Examiner: Dieu Minh T. Le

Filing Date: October 25, 2004

Group Art Unit: 2114

Title: SYSTEM AND METHOD FOR PROVIDING FIRMWARE RECOVERABLE LOCKSTEP PROTECTION

Mail Stop After Final
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL LETTER FOR RESPONSE/AMENDMENT

Transmitted herewith is/are the following in the above-identified application:

- [x] Response/Amendment
- [ ] New fee as calculated below
- [x] No additional fee
- [ ] Other _____ Fee$_____
- [ ] Petition to extend time to respond
- [ ] Supplemental Declaration

CLAIMS AS AMENDED BY OTHER THAN A SMALL ENTITY

(1) FOR	(2) CLAIMS REMAINING AFTER AMENDMENT	(3) NUMBER EXTRA	(4) HIGHEST NUMBER PREVIOUSLY PAID FOR	(5) PRESENT EXTRA	(6) RATE	(7) ADDITIONAL FEES
TOTAL CLAIMS	25	MINUS	35	= 0	X $50	$ 0
INDEP. CLAIMS	4	MINUS	5	= 0	X $210	$ 0
[ ] FIRST PRESENTATION OF A MULTIPLE DEPENDENT CLAIM					+ $370	$ 0
EXTENSION FEE	[ ] 1st Month $120	[ ] 2nd Month $460	[ ] 3rd Month $1050	[ ] 4th Month $1640		$ 0
OTHER FEES						$
TOTAL ADDITIONAL FEE FOR THIS AMENDMENT						$ 0

Charge $ 0 to Deposit Account 08-2025. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

Scott L. Michaelis et al.

By: /Guy K. Clinger/

Guy K. Clinger, Esq.

Attorney/Agent for Applicant(s)

Reg No. : 42,422

Date : April 10, 2008

Telephone : (303) 298-9888

Rev 10/07 (E-TransAmd)

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
10/973,076	10/25/2004	

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT 04/10/2008	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 25	Minus	** 35	= 0	X $ =		OR	X $50=	0
Independent (37 CFR 1.16(h))	* 4	Minus	***5	= 0	X $ =		OR	X $210=	0
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)	OR	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/SHEILA D. CHAPMAN/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/973,076	10/25/2004	Scott L. Michaelis	200404941-1	6989

22879 7590 02/27/2008
HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER
LE, DIEU MINH T

ART UNIT	PAPER NUMBER
2114	

NOTIFICATION DATE	DELIVERY MODE
02/27/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

JERRY.SHORMA@HP.COM
mkraft@hp.com
ipa.mail@hp.com

Office Action Summary	Application No.	Applicant(s)	
	10/973,076	MICHAELIS ET AL.	
	Examiner	Art Unit	
	Dieu-Minh Le	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 27 November 2007.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-35 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) 15-20 and 26-28 is/are allowed.

6)☒ Claim(s) 1-7,11-13,21-25,29-32,34 and 35 is/are rejected.

7)☒ Claim(s) 8-10,14 and 33 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 25 October 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the communications filed 11/27/07 in application 10/973,076.

2. Claims 1-35 are again presented for examination.

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 1-7, 11-13, 21-25, 29-32, and 34-35 are again rejected under 35 U.S.C. 103(a) as being unpatentable over Marshall et al. (U.S. 5,915,082 hereafter referred to as Marshall) in view of Safford et al. (U.S. 7,085,959 hereafter referred to as Safford).

This rejection is being applied for the same reasons set forth in the previous Office Action mailed 09/12/2007.
As per claims 1-7, 11-13, 21-25, 29-32, and 34-35, see the previous office action for the detailed teaching of Marshall and Safford as well as the motivation and reason for combined.

Applicant asserts that Marshall in combining with Safford do not disclose or suggest following limitation:

+ triggering an operating system to idle a lockstep pair of processors for which a loss of lockstep has been detected.

Examiner respectfully transverses Applicant's argument as follows:

First, in response to Applicant's argument that the references fail to show certain features of Applicant's invention, it is noted that the feature upon which Applicant relies (i.e., *triggering an operating system* ***to idle*** *a lockstep pair of processors* ***for which a loss of lockstep has been detected***) is not recited in the rejected claim 1; (i.e., *triggering an operating system to idle* ***a lockstep pair of processors for which a loss of lockstep has been detected***) is not recited in the rejected claim 21; and (i.e., *triggering an operating system to idle a* ***lockstep pair of processors for which a loss of lockstep has been detected***) is not recited in the rejected claim 29. Although the claim is interpreted in light of the specification, limitations from the specification is not read into the claims. *In re Van Guens, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).*

Second, it is ***not*** true that both Marshall and Stafford failed to teach "*triggering an operating system to idle a*

lockstep pair of processors for which a loss of lockstep has been detected" limitation. Examiner would like to bring Applicant attention to Marshall's error detection and fault isolation for lockstep processor systems [abstract, col. 1, lines 10-20] comprising a data connectivity among multi-processors, firmware, OS embed, error detection and recovery, user interface, etc…. as depicted in figure 2, col. 4, lines 13-35. Marshall further disclosed the memory read/write operations, data comparison, and isolation operations [col. 3, lines 35-49 and col. 4, lines 41-57]. ***These operations are executed from the operations system in order to configuring and error signaling used to enhance recovery from loss of lockstep in a multi-processors system*** [abstract, col. 2, lines 11-24 and col. 12, claim 1].

Third, Safford explicitly demonstrated a method and apparatus for recovery from loss of lock step [abstract, col. 2, lines 13-32] comprising ***capability to signal the computer system (i.e., operating system) to idle the lockstep of processors [col. 4, lines 30-63].*** Stafford clearly illustrated a computer system having a means for detecting and recovering of a loss of lock step including idling the lockstep of processor. It is

obvious to an ordinary skill in the art to realize that this idle process performed by the computer operating system therein.

Fourth, it would have been obvious to a person having ordinary skill in the art at the time of Applicant's invention to first realizing Marshall's ***configuring and error signaling used to enhance recovery from loss of lockstep in a multi-processors system*** as being the use of firmware to trigger an operating system to idle the lockstep pair of processors as claimed by Applicant. This is because Marshall's mutli-data processors /fault tolerant system explicitly performed data failure detection and recovery (i.e., ***loss of lockstep*** and/or ***fail-over***) within plurality of processors via ***state information, parity information***, and ***boot information*** processes. By utilizing these capabilities, the multi-data processing system can be directed or redirected promptly and functioned properly during failover recovery process in supporting the system operation; second, by applying the ***configuring and error signaling used to enhance recovery from loss of lockstep in a multi-processors system*** as taught by Safford in conjunction with the error detection and fault isolation for lockstep processor systems as taught by Marshall, the multi-processors within fault tolerant/failure recovery networking system including

master/slave capability (i.e., failover) can enhance its operation performance, more specifically to ensuring the error detected, corrected, and replaced (i.e., backup) in proper and efficient manner via its state information functionality. Therefore, it is obvious to an ordinary skill in the art that the combination of both Marshall and Stafford do teach applicant’s above limitation.

Applicant's arguments filed 11/27/2007 have been fully considered but they are not persuasive.

Allowable Subject Matter

5. Claims 8-10, 14, and 33 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. Claims 15-20 and 26-28 are allowable over the prior art of record.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. § 1.136(a).

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 C.F.R. § 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dieu-Minh Le whose telephone number is (571) 272-3660. The examiner can normally be reached on Monday - Thursday from 8:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Scott Baderman can be reached on (571)272-3644.
The Tech Center 2100 phone number is (571) 272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through

Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/DIEU-MINH T. LE/
DIEU-MINH THAI LE
PRIMARY EXAMINER
ART UNIT 2114

DML
02/14/08

Notice of References Cited	Application/Control No. 10/973,076	Applicant(s)/Patent Under Reexamination MICHAELIS ET AL.	
	Examiner Dieu-Minh Le	Art Unit 2114	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-5,896,523	04-1999	Bissett et al.	713/400
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10973076	MICHAELIS ET AL.
	Examiner	**Art Unit**
	Dieu-Minh Le	2114

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	02/14/2008								
	1	✓								
	2	✓								
	3	✓								
	4	✓								
	5	✓								
	6	✓								
	7	✓								
	8	O								
	9	O								
	10	O								
	11	✓								
	12	✓								
	13	✓								
	14	O								
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	28	=								
	29	✓								
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	31	✓								
	32	✓								
	33	O								
	34	✓								
	35	✓								

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10973076	MICHAELIS ET AL.
	Examiner	**Art Unit**
	Dieu-Minh Le	2114

SEARCHED			
Class	**Subclass**	**Date**	**Examiner**
714	10-13; 712/31	2/14/2008	dml

SEARCH NOTES		
Search Notes	**Date**	**Examiner**
EAST search all files updated.	2/14/2008	dml

INTERFERENCE SEARCH			
Class	**Subclass**	**Date**	**Examiner**

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	15153	trigger$3 same ("operating system" OS operating-system) same (idle stop$4 interrupt$3 halt$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/02/14 14:49
L2	207	(loss lose los$3 lost$3) same (lockstep lock-step "lock step")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/02/14 14:52
L3	86	(detect$3 track$3 monitor$3) same 2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/02/14 14:56
L4	3	3 same 1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/02/14 14:56
L5	3	2 same 1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/02/14 15:02
L6	10	2 and 1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/02/14 15:02
L7	33339	(pair spare slave redundan$4 backup back-up "back up" second$4) adj2 processor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/02/14 15:05

L8	2323	lockstep lock-step	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/02/14 15:06
L9	92	(recover$4 reestablish$3 restart$3) with L8	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/02/14 15:06
L10	114677	firmware	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/02/14 15:06
L11	11	7 same L9 same L10	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/02/14 15:06
L12	764	(714/11).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/02/14 15:07
L13	352	(714/12).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/02/14 15:07
L14	659	(714/13).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/02/14 15:07
L15	658	(714/10).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/02/14 15:07

L16	96	(712/31).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/02/14 15:07
L17	2	(L12 L13 L14 L15 L16) and 1 and 3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/02/14 15:07
L18	2	(L12 L13 L14 L15 L16) and 1 and 2 and 7 and 10	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/02/14 15:08
S1	14	(("7085959") or ("20050172164") or ("5675794") or ("6438687") or ("6920581") or ("5915082") or ("6625749")).PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/08/26 17:54
S2	2	("7085959").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/08/27 15:05
S3	730	(714/11).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/27 15:06
S4	337	(714/12).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 15:32
S5	606	(714/13).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/27 15:07

S6	36	("20020144177" | "20030070050" | "20040006722" | "20040019771" | "20040153857" | "5226152" | "5249188" | "5751932" | "5758058" | "5764660" | "6065135" | "6148348" | "6473869" | "6560682" | "6604177" | "6615366" | "6625749" | "6687851" | "6754787"). PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/27 15:08
S7	44	("20020144177" | "20030070050" | "20040006722" | "20040019771" | "20040153857" | "6625749" | "6687851" | "6754787")".PN"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/27 15:09
S9	2222	lockstep lock-step	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 15:21
S11	25008	(loss adj S9) LOL	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 15:22
S12	51	(detect$3 or track$4) adj S11	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 15:23
S13	1547	(boot$4 or initializ$4) adj processor	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 16:41
S14	246	spare adj processor	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 15:27

S15	12	S12 and S13 and S14	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 15:30
S16	25	(michaelis-scott$ or myer-sylvia$ or mchardy-william$).in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 16:14
S18	632	(714/10).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 15:33
S19	95	(712/31).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 16:08
S20	52536	(switch$4 chang$4 failover fail-over "fail over") same (spare slave redundan$4 backup back-up "back up" second$4) same processor	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 16:54
S21	81	S20 same S13	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 16:28
S22	168219	without same ("shut$4 down" stop$4 idle interrupt$4) same (OS "operating system")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 16:33
S23	6	S21 and S22	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 16:33

S24	20342	multi-processor "multi processor" and S11 and S13	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 16:45
S25	176	S24 and S20 and S22	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 16:46
S26	7	S25 and S14	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 16:53
S27	87	(recover$4 reestablish$3 restart$3) with S9	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 16:54
S28	31827	(pair spare slave redundan$4 backup back-up "back up" second$4) adj2 processor	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 16:55
S29	101834	firmware	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 16:56
S30	21	S27 and S28 and S29	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 16:57

2/14/08 3:10:57 PM
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Application Number	Application/Control No.	Applicant(s)/Patent under Reexamination
	10/973,076	MICHAELIS ET AL.

Document Code - DISQ	Internal Document – DO NOT MAIL

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Date Filed : 11/27/07	This patent is subject to a Terminal Disclaimer	

Approved/Disapproved by:
BRIAN

U.S. Patent and Trademark Office

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:	
Scott L. Michaelis et al.	
Attorney Docket 200404941-1	Examiner: Dieu Minh T Le
Serial No. 10/973,076	Group Art Unit: 2114
Filing Date: October 25, 2004	Confirmation No. 6989
For: SYSTEM AND METHOD FOR PROVIDING FIRMWARE RECOVERABLE LOCKSTEP PROTECTION	

RESPONSE

To: Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office Action of September 12, 2007, please amend the above-identified application as set forth below.

Amendments to the claims begin on page 2 of this paper.

Amendments to the specification begin on page 9 of this paper.

Remarks begin on page 17 of this paper.

In the Claims

1. (Original) A method comprising:

detecting loss of lockstep for a lockstep pair of processors; and

using firmware to trigger an operating system to idle the lockstep pair of processors, recover lockstep for the lockstep pair of processors, and trigger the operating system to recognize the lockstep pair of processors having recovered lockstep.

2. (Original) The method of claim 1 wherein said using firmware to trigger an operating system to idle the lockstep pair of processors further comprises:

using the firmware to trigger the operating system to idle a master processor of the lockstep pair of processors.

3. (Original) The method of claim 2 wherein said using firmware to trigger the operating system to recognize the lockstep pair of processors having recovered lockstep further comprises:

using the firmware to trigger the operating system to recognize the master of the lockstep pair of processors.

4. (Original) The method of claim 1 wherein said detecting loss of lockstep comprises:

detecting corrupt data in one of said lockstep pair of processors that would lead to a lockstep mismatch if acted upon.

5. (Original) The method of claim 1 wherein said detecting loss of lockstep comprises:

detecting a precursor to lockstep mismatch.

6. (Original) The method of claim 1 wherein said detecting loss of lockstep comprises:

detecting lockstep mismatch between the lockstep pair of processors.

7. (Original) The method of claim 1 further comprising:

responsive to said detecting loss of lockstep, using said firmware to determine if lockstep is recoverable for the lockstep pair of processors.

8. (Original) The method of claim 7 wherein said using said firmware to determine if lockstep is recoverable further comprises:

determining if a lockstep mismatch has occurred between the lockstep pair of processors.

9. (Original) The method of claim 8 further comprising:

if determined that a lockstep mismatch has not occurred between the lockstep pair of processors, then determining that the loss of lockstep is recoverable.

10. (Original) The method of claim 8 further comprising:

if determined that a lockstep mismatch has occurred between the lockstep pair of processors, then determining that the loss of lockstep is not recoverable.

11. (Original) The method of claim 1 further comprising:

determining if said lockstep pair of processors for which said loss of lockstep is detected comprises a system boot processor.

12. (Original) The method of claim 11 wherein if determined that said lockstep pair of processors for which said loss of

lockstep is detected comprises a system boot processor, further comprising:

swapping the role of system boot processor to another processor in the system.

13. (Original) The method of claim 12 further comprising:

after said swapping, recovering the lockstep for the lockstep pair of processors.

14. (Original) The method of claim 13 further comprising:

after recovering lockstep for the lockstep pair of processors, holding the recovered pair of processors in idle as a spare for the processor to which the role of system boot processor was swapped.

15. (Original) A system comprising:

an Advanced Configuration and Power Interface (ACPI)-compatible operating system;

master processor operable to process instructions scheduled by said ACPI-compatible operating system;

slave processor lockstepped with the master processor operable to perform redundant processing of said instructions scheduled for the master processor; and

firmware operable, responsive to detection of loss of lockstep between the master and slave processors, to use an ACPI method to trigger the operating system to idle the master processor, attempt to recover lockstep between the master and slave processors, and if recovery of lockstep is successful then use an ACPI method to reintroduce the master processor to the operating system.

16. (Original) The system of claim 15 further comprising:

error detection logic for detecting loss of lockstep

between the master and slave processors.

17. (Original) The system of claim 15 further comprising:

error detection logic for detecting a precursor to loss of lockstep.

18. (Original) The system of claim 17 wherein said precursor to loss of lockstep is treated as said detection of loss of lockstep.

19. (Original) The system of claim 17 wherein said error detection logic comprises a parity-based mechanism.

20. (Original) The system of claim 15 further comprising error detection logic for detecting lockstep mismatch between the master and slave processors.

21. (Original) A system comprising firmware that includes computer-executable software code stored to a computer-readable medium, the computer-executable software code comprising:

code, responsive to detection of loss of lockstep between a pair of lockstep processors, for determining if the lockstep is recoverable for the pair of lockstep processors; and

code, responsive to determining that the lockstep is recoverable, for triggering an operating system to idle the processors, attempting to recover lockstep between the pair of processors, and if lockstep is successfully recovered between the pair of processors, triggering said operating system to recognize the processors as being available for receiving instructions.

22. (Original) The system of claim 21 wherein the code for

attempting to recover lockstep further comprises:

code for resetting the pair of processors.

23. (Original) The system of claim 21 wherein the code for determining if the lockstep is recoverable further comprises:

code for determining if lockstep mismatch occurred between the pair of lockstep processors.

24. (Original) The system of claim 21 wherein said operating system is an Advanced Configuration and Power Interface (ACPI)-compatible operating system, said code for triggering the operating system to idle the processors comprises:

code for using an ACPI method to idle the processors.

25. (Original) The system of claim 21 wherein said operating system is an Advanced Configuration and Power Interface (ACPI)-compatible operating system, said code for triggering said operating system to recognize the processors as being available for receiving instructions comprises:

code for using an ACPI method to cause the operating system to check for the processors.

26. (Original) A method comprising:

establishing, in a multi-processor system, a hot spare processor for a system boot processor;

detecting loss of lockstep for a lockstep pair of processors in said multi-processor system;

determining if said lockstep pair of processors for which the loss of lockstep is detected is the system boot processor;

if determined that said lockstep pair of processors for which the loss of lockstep is the system boot processor, copying a state of the system boot processor to the hot spare processor; and

if determined that said lockstep pair of processors for which the loss of lockstep is not the system boot processor, then triggering an operating system to a) idle the lockstep pair of processors, b) attempt to recover lockstep between the lockstep pair of processors, and c) if lockstep is successfully recovered between the lockstep pair of processors, trigger said operating system to recognize the processors as being available for receiving instructions.

27. (Original) The method of claim 26 wherein if determined that said lockstep pair of processors for which the loss of lockstep is the system boot processor further comprising:

attempting to recover lockstep between the lockstep pair of processors after copying the state of the system boot processor to the hot spare processor.

28. (Original) The method of claim 27 wherein if determined that said lockstep pair of processors for which the loss of lockstep is the system boot processor further comprising:

if lockstep is successfully recovered between the lockstep pair of processors, establishing the lockstep pair of processors for which lockstep was recovered as a hot spare processor.

29. (Original) A system comprising:

means for detecting loss of lockstep between a pair of processors;

means for determining if lockstep is recoverable for the pair of processors; and

means, responsive to the determining means determining that the lockstep is recoverable for the pair of processors, for triggering an operating system to idle the processors, recovering the lockstep for the pair of processors, and

reintroducing to the operating system the processors having recovered lockstep.

30. (Original) The system of claim 29 wherein the means for triggering the operating system to idle the processors uses an Advanced Configuration and Power Interface (ACPI) method for said triggering.

31. (Currently amended) The system of claim [[19]] 29 wherein the means for reintroducing uses an Advanced Configuration and Power Interface (ACPI) method for reintroducing to the operating system the processors having recovered lockstep.

32. (Original) The system of claim 29 wherein said means for detecting loss of lockstep comprises:

means for detecting a precursor to loss of lockstep.

33. (Original) The system of claim 32 wherein said means for detecting a precursor to loss of lockstep comprises a parity-based means.

34. (Original) The system of claim 29 wherein said means for detecting loss of lockstep comprises:

means for detecting a lockstep mismatch.

35. (Original) The system of claim 29 wherein said means for determining comprises:

means for determining if the detected loss of lockstep is a lockstep mismatch.

In the Specification

Please amend original paragraphs 1, 25, 37, 38, 44-46 and 48-51 of the specification as follows:

[0001] The present application is related to the following concurrently filed and commonly assigned U.S. Patent Applications: Serial No. [[_____]] 10/973,077 [Attorney Docket No. 200404944-1] titled "SYSTEM AND METHOD FOR ESTABLISHING A SPARE PROCESSOR FOR RECOVERING FROM LOSS OF LOCKSTEP IN A BOOT PROCESSOR"; Serial No. [[_____]] 10/973,004 [Attorney Docket No. 200404943-1] titled "SYSTEM AND METHOD FOR CONFIGURING LOCKSTEP MODE OF A PROCESSOR MODULE"; Serial No. [[_____]] 10/972,835 [Attorney Docket No. 200404946-1] titled "SYSTEM AND METHOD FOR USING INFORMATION RELATING TO A DETECTED LOSS OF LOCKSTEP FOR DETERMINING A RESPONSIVE ACTION"; Serial No. [[_____]] 10/972,588 [Attorney Docket No. 200404973-1 titled "SYSTEM AND METHOD FOR SWITCHING THE ROLE OF BOOT PROCESSOR TO A SPARE PROCESSOR RESPONSIVE TO DETECTION OF LOSS OF LOCKSTEP IN A BOOT PROCESSOR"; Serial No. [[_____]] 10/973,003 [Attorney Docket No. 200404971-1] titled "SYSTEM AND METHOD FOR REESTABLISHING LOCKSTEP FOR A PROCESSOR MODULE FOR WHICH LOSS OF LOCKSTEP IS DETECTED"; Serial No. [[_____]] 10/972,888 [Attorney Docket No. 200404970-1] titled "SYSTEM AND METHOD FOR SYSTEM FIRMWARE CAUSING AN OPERATING SYSTEM TO IDLE A PROCESSOR"; Serial No. [[_____]] 10/973,075 [Attorney Docket No. 200404972-1] titled "SYSTEM AND METHOD FOR REINTRODUCING A PROCESSOR MODULE TO AN OPERATING SYSTEM AFTER LOCKSTEP RECOVERY"; and Serial No. [[_____]] 10/972,796 [Attorney Docket No. 200404974-1] titled "SYSTEM AND METHOD FOR MAINTAINING IN A MULTI-PROCESSOR SYSTEM A SPARE PROCESSOR THAT IS IN LOCKSTEP FOR USE IN RECOVERING FROM LOSS OF

LOCKSTEP FOR ANOTHER PROCESSOR", the disclosures of which are hereby incorporated herein by reference.

[0025] Once the processor pair 12 is reset and lockstep is recovered, firmware 15 reintroduces master processor 12A to OS 11 in operational block 106. In this embodiment, firmware 15 updates the ACPI device table information for master processor 12A to indicate that such master processor 12A is "present, functioning and enabled." As discussed in the ACPI 2.0 specification for the _STA status method of a device, the _STA (status) object returns the status of a device, which can be one of the following: enabled, disabled, or removed. In this respect, in the result code (bitmap) bit 0 is set if the device is present; bit 1 is set if the device is enabled and decoding its resources; bit 2 is set if the device should be shown in the UI; bit 3 is set if the device is functioning properly (cleared if the device failed its diagnostics); bit 4 is set if the battery is present; and bits 5-31 are reserved. A device can only decode its hardware resources if both bits 0 and 1 are set. If the device is not present (bit 0 cleared) or not enabled (bit 1 cleared), then the device must not decode its resources. Bits 0, 1 and 3 are the "present, enabled and functioning" bits mentioned above. Firmware 15 utilizes an ACPI method 107 to trigger OS 11 to "check for" master processor 12A, thereby reintroducing the master processor 12A to OS 11. As a result of checking for master processor 12A, OS 11 will recognize that such master processor 12A is again available and will thus begin scheduling tasks for master processor 12A once again. An example technique that may be utilized by firmware 15 for reintroducing a processor to the OS after recovery of lockstep in accordance with certain embodiments is described further in concurrently filed and commonly assigned U.S. Patent Application Serial No.

[[_____]] 10/973,075 [Attorney Docket No. 200404972-1] titled "SYSTEM AND METHOD FOR REINTRODUCING A PROCESSOR MODULE TO AN OPERATING SYSTEM AFTER LOCKSTEP RECOVERY", the disclosure of which is hereby incorporated herein by reference.

[0037] However, if determined in block 301 that the master processor 12A is the system's boot processor, operation advances to block 302 whereat the state of the "good" processor in the lockstep processor pair 12 is copied over to each of processors 31A and 31B in the spare lockstep processor pair 31. Example techniques that may be utilized by firmware 35 for switching the state of a "good" processor in the lockstep processor pair 12 in accordance with certain embodiments is described further in co-pending U.S. Patent Application Serial No. 10/187,833 (published as publication no. US 2004/0006722 A1) filed July 3, 2002 and titled "METHOD AND APPARATUS FOR RECOVERY FROM LOSS OF LOCK STEP" and in concurrently filed and commonly assigned U.S. Patent Application Serial No. [[_____]] 10/972,588 [Attorney Docket No. 200404973-1] titled "SYSTEM AND METHOD FOR SWITCHING THE ROLE OF BOOT PROCESSOR TO A SPARE PROCESSOR RESPONSIVE TO DETECTION OF LOSS OF LOCKSTEP IN A BOOT PROCESSOR", the disclosures of which are each hereby incorporated herein by reference.

[0038] Thus, operational block 302 essentially makes the spare processor pair 31 the system's boot processor, and then in block 303 firmware 35 resets the lockstep processor pair 12 and reestablishes its lockstep. Once lockstep is reestablished for lockstep processor pair 12, that pair is held in operational block 304 as a hot spare for the new boot processor pair 31. That is, firmware 35 updates the device

tree 203 of FIGURE 2 to reflect that lockstep processor pair 12 is a hot spare for the boot processor pair 31. Thus, should a recoverable LOL be detected for the new boot processor 31, the above process may be used by firmware 35 to make the spare lockstep processor pair 12 the boot processor and then recover lockstep for pair 31. An example technique for resetting the lockstep processor pair 12 and reestablishing its lockstep in which the lockstep processor pair 12 is then held as a hot spare is described further in concurrently filed and commonly assigned U.S. Patent Application Serial No. [[_____]] 10/972,796 [Attorney Docket No. 200404974-1] titled "SYSTEM AND METHOD FOR MAINTAINING IN A MULTI-PROCESSOR SYSTEM A SPARE PROCESSOR THAT IS IN LOCKSTEP FOR USE IN RECOVERING FROM LOSS OF LOCKSTEP FOR ANOTHER PROCESSOR", the disclosure of which is hereby incorporated herein by reference.

[0044] Turning now to FIGURE 5, an operational flow diagram for one embodiment is shown. In operational block 501, the system is powered on. In operational block 502, the system's firmware establishes a hot spare for the system's boot processor. For instance, in the example system 40 of FIGURE 4, if CPU 2 (402) is designated as the boot processor, the firmware 35 identifies a processor on the same bus as the boot processor, such as CPU 3 (403), as a hot spare, and firmware 35 updates the device tree to designate that such CPU 3 (403) is a hot spare for the boot processor CPU 2 (402). An example technique that may be utilized by firmware 35 for establishing a hot spare for the boot processor in accordance with certain embodiments is described further in concurrently filed and commonly assigned U.S. Patent Application Serial No. [[_____]] 10/973,077 [Attorney Docket No. 200404944-1] titled "SYSTEM AND METHOD FOR ESTABLISHING A SPARE PROCESSOR

FOR RECOVERING FROM LOSS OF LOCKSTEP IN A BOOT PROCESSOR", the disclosure of which is hereby incorporated herein by reference.

[0045] In operational block 503, the firmware establishes lockstep mode on the appropriate processor modules (or lockstep processor pairs). As described further in concurrently filed and commonly assigned U.S. Patent Application Serial No. [[_____]] 10/973,004 [Attorney Docket No. 200404943-1] titled "SYSTEM AND METHOD FOR CONFIGURING LOCKSTEP MODE OF A PROCESSOR MODULE", the disclosure of which is hereby incorporated herein by reference, in certain embodiments whether lockstep is activated for the system (or for any given partition of a system) is configurable by a system administrator. Thus, rather than the processors of a system being fixed in either lockstep mode or not in lockstep mode, certain embodiments permit lockstep mode to be activated and deactivated for a system as may be desired by a system administrator. In the event that lockstep mode is not activated for the system, then the processors that would have been used as slave processors in lockstep mode are available to be used as "master" processors for processing instructions, thus increasing the total amount of computing resources available to the OS. If for example, having a greater number of processors available for computing separate instructions is more desirable than guarding fully against SDC on a given partition of a customer's system, then lockstep processing may be disabled for such partition, and lockstep processing may be enabled for those partitions in which fully guarding against SDC is of more importance.

[0046] In operational block 504, the boot process boots the system OS and completes with the firmware passing control of

the system over to the OS. During system runtime, if the system is operating in lockstep mode, then error detect logic present in the system (such as error detect logic 13A-13C of FIGURE 1) monitors for LOL. Thus, block 505 represents the continuous monitoring by the error detect logic of their respective processors for LOL. If an LOL is detected by the error logic, then the firmware is notified of the detected LOL in block 506. An example technique that may be utilized for notifying the firmware of the detected LOL in accordance with certain embodiments is described further in concurrently filed and commonly assigned U.S. Patent Application Serial No. [[_____]] 10/972,835 [Attorney Docket No. 200404946-1] titled "SYSTEM AND METHOD FOR USING INFORMATION RELATING TO A DETECTED LOSS OF LOCKSTEP FOR DETERMINING A RESPONSIVE ACTION", the disclosure of which is hereby incorporated herein by reference. As mentioned above, the firmware determines whether the detected LOL is recoverable. If determined that the LOL is recoverable, then operation continues in the firmware for recovering the LOL in the manner described hereafter.

[0048] If the processor for which LOL is detected is not the system boot processor, then operation advances to block 508 whereat the processor for which the LOL is detected is idled, and actions are taken to reestablish its lockstep. As described above, an ACPI "eject" method may be used to instruct the system's OS to idle the processor, such as described more fully in concurrently filed and commonly assigned U.S. Patent Application Serial No. [[_____]] 10/973,003 [Attorney Docket No. 200404971-1] titled "SYSTEM AND METHOD FOR REESTABLISHING LOCKSTEP FOR A PROCESSOR MODULE FOR WHICH LOSS OF LOCKSTEP IS DETECTED", the disclosure of which is hereby incorporated herein by reference. In order to

reestablish lockstep, the processor may be reset. At the end of this step, the processor is executing in firmware space and lockstep has been reestablished for the processor.

[0049] The processor is then ready to be introduced back to the OS. Thus, in block 509, the firmware reintroduces to the OS the processor having its lockstep recovered. An example technique that may be utilized for reintroducing the processor back to the OS in block 509 in accordance with certain embodiments is described further in concurrently filed and commonly assigned U.S. Patent Application Serial No. [[_____]] 10/973,075 [Attorney Docket No. 200404972-1] titled "SYSTEM AND METHOD FOR REINTRODUCING A PROCESSOR MODULE TO AN OPERATING SYSTEM AFTER LOCKSTEP RECOVERY", the disclosure of which is hereby incorporated herein by reference. Operation then continues in block 510, wherein the processor whose lockstep was recovered is available to run tasks as scheduled by the OS and the system's processors are monitored for another LOL in block 505. That is, in block 510 the system is back to a stable state with full lockstep protection again being provided.

[0050] Unfortunately, as mentioned above, in certain systems the system boot processor that initialized the OS during the systems boot-up process cannot easily be idled and returned to firmware control. Thus, a different technique than that described above for non-boot processors is employed in this embodiment. Accordingly, if determined in block 507 that the LOL is detected for the system's boot processor, operation advances to block 511 whereat the state of the "good" boot processor is copied to the hot spare that was established for the boot processor in block 502. As mentioned above, example techniques that may be utilized by the firmware

for switching the state of a "good" processor in the lockstep processor pair that is the system boot processor in accordance with certain embodiments is described further in co-pending U.S. Patent Application Serial No. 10/187,833 (published with publication no. US 2004/0006722 A1) filed July 3, 2002 and titled "METHOD AND APPARATUS FOR RECOVERY FROM LOSS OF LOCK STEP" and in concurrently filed and commonly assigned U.S. Patent Application Serial No. [[_____]] 10/972,588 [Attorney Docket No. 200404973-1] titled "SYSTEM AND METHOD FOR SWITCHING THE ROLE OF BOOT PROCESSOR TO A SPARE PROCESSOR RESPONSIVE TO DETECTION OF LOSS OF LOCKSTEP IN A BOOT PROCESSOR", the disclosures of which are each hereby incorporated herein by reference.

[0051] In operational block 512, the firmware reestablishes lockstep on the processor for which the LOL was detected (e.g., by resetting the processor), and the firmware establishes the processor having recovered lockstep as the hot spare for the new boot processor. Such processor whose lockstep has been recovered may be established as a spare for the new boot processor in the manner described above in block 502, and as discussed further in concurrently filed and commonly assigned U.S. Patent Application Serial No. [[_____]] 10/973,077 [Attorney Docket No. 200404944-1] titled "SYSTEM AND METHOD FOR ESTABLISHING A SPARE PROCESSOR FOR RECOVERING FROM LOSS OF LOCKSTEP IN A BOOT PROCESSOR", the disclosure of which is hereby incorporated herein by reference. Operation of the system continues in block 513 wherein the processors are monitored for another LOL in block 505. In block 513 the system is back to a stable state with full lockstep protection again being provided.

R E M A R K S

Claim 31 has been amended. Claims 1-30 and 32-35 stand as originally filed.

Claims 1-35 were considered in the Office Action. Claims 29-35 stand rejected under 35 U.S.C. 112, second paragraph as being indefinite. The only failure specified for these claims is the improper dependency of claim 31. Claim 31 has been amended to correct this error, and claims 29-35 are believed to be in order for allowance.

Claims 1-35 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Marshall et al., U.S. Patent 5,915,082 in view of Safford et al., U.S. Patent 7,085,959.

The Examiner has requested that the disclosure be amended to specify the serial number or patent number of related applications. The disclosure has been so amended.

Claims 1-35 stand rejected under the judicially created doctrine of obviousness-type double patenting over claims in applications 10/973,003, 10/973,075, 10/972,888 and 10/972,796. A terminal disclaimer over these commonly owned applications has been filed with this response.

Applicants believe that the currently pending claims are not anticipated by or obvious over the cited references for at least the reasons set forth below and respectfully request reconsideration.

Independent claims 1, 15, 21, 26 and 29 all include the limitation of triggering an operating system to idle a lockstep pair of processors for which a loss of lockstep has been detected. The cited references do not disclose or suggest this limitation. The Examiner has indicated that Safford explicitly teaches “capability to signal the computer system (i.e., operating system) to idle the lockstep of processors [col. 4, lines 30-63].” Applicants respectfully

disagree that Safford teaches the signaling of an operating system to idle a lockstep pair of processors.

> "FIG. 4 is a flow chart illustrating a process 200 for recovery from a loss of lock step using the computer system 100 shown in FIG. 3. The process 200 will be shown with an error condition in the first processor pair 111/113. The operation 200 begins in block 205 with the system 100 operating in a normal lock step fashion. In block 210, the processor 111 detects an error event that indicates an impending loss of lock step. **In block 215, the processor 111 signals the node controller 130 that the first processor pair 111/113 has broken lock step and that the first processor pair 111/113 should be taken "off-line."** In block 220, the node controller 130 copies the architected state of the first processor pair 111/113 to the hot standby processor pair 125/127. In an embodiment, the architected state of the first processor pair 111/113 may be stored in the node controller 130, and to facilitate recovery, the node controller 130 copies the stored state to the third processor pair 125/127. Alternatively, the node controller 130 may copy the state of the first processor pair 111/113 directly from the processors 111 and 113 to the processors 125 and 127 without any intermediate storage of the architected state in the node controller 130, or other component of the computer system 100. The processor pair 125/127 then becomes the logical CPU 0 in the computer system 100, and the computer system 100 operates without a hot standby processor pair. In block 225, recovery actions are executed on the first processor pair 111/113 (e.g., all caches are flushed on the processors 111 and 113). In block 230, the node controller 130 "reboots" the processors 111 and 113, and the processors 111 and 113 become the new "hot standby" processor pair on the system 100. In block 235, the operation 200 ends, with the computer system 100 operating the processors 121, 123, 125, and 127 in lock step, and with the processors 111/113 idle and in hot standby."
> (Safford, col. 4, lines 30-63, emphasis added)

Applicants note that Safford, and particularly the cited section above, teaches that the processor signals a **node controller**, not an operating system. Note in FIG. 3 that the node controller 130 is illustrated as an independent block

alongside the CPU hardware blocks, and does not appear to comprise an operating system running on a CPU. Furthermore, Safford signals to the node controller that a processor pair should be taken offline, not that an operating system should idle the processor. If Safford's node controller merely disables the processor pair by taking it offline, this may lead to the operating system timing out and crashing as described in paragraph 8 of Applicants' specification. The claimed invention avoids this problem by triggering an operating system to idle a lockstep pair of processors for which a loss of lockstep has been detected before taking them offline, in contrast to the cited references.

The dependent claims depend upon independent claims which are allowable over the cited art as discussed above. The dependent claims are likewise in condition for allowance at least because they depend on allowable independent claims, along with a variety of other non-obvious differences over the cited references.

In view of the above, all of the claims are believed to be in condition for allowance, and the Applicants respectfully request that a timely Notice of Allowance be issued.

Respectfully submitted,
KLAAS, LAW, O'MEARA & MALKIN, P.C.

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PATENT APPLICATION

ATTORNEY DOCKET NO. 200404941-1

Inventor(s): Scott L. Michaelis et al.

Confirmation No.: 6989

Application No.: 10/973,076

Examiner: Dieu Minh T Le

Filing Date: October 25, 2004

Group Art Unit: 2114

Title: SYSTEM AND METHOD FOR PROVIDING FIRMWARE RECOVERABLE LOCKSTEP PROTECTION

Mail Stop Amendment
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL LETTER FOR RESPONSE/AMENDMENT

Transmitted herewith is/are the following in the above-identified application:

- [x] Response/Amendment
- [ ] New fee as calculated below
- [ ] No additional fee
- [x] Other Terminal Disclaimer — Fee$ 130
- [ ] Petition to extend time to respond
- [ ] Supplemental Declaration

CLAIMS AS AMENDED BY OTHER THAN A SMALL ENTITY

(1) FOR	(2) CLAIMS REMAINING AFTER AMENDMENT	(3) NUMBER EXTRA	(4) HIGHEST NUMBER PREVIOUSLY PAID FOR	(5) PRESENT EXTRA	(6) RATE	(7) ADDITIONAL FEES
TOTAL CLAIMS	35	MINUS	35	= 0	X $50	$ 0
INDEP. CLAIMS	5	MINUS	5	= 0	X $210	$ 0
[ ] FIRST PRESENTATION OF A MULTIPLE DEPENDENT CLAIM					+ $370	$ 0
EXTENSION FEE	[ ] 1st Month $120	[ ] 2nd Month $460	[ ] 3rd Month $1050	[ ] 4th Month $1640		$ 0
OTHER FEES						$ 130
TOTAL ADDITIONAL FEE FOR THIS AMENDMENT						$ 130

Charge $ 130 to Deposit Account 08-2025. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

Scott L. Michaelis et al.

By: /Guy K. Clinger/

Guy K. Clinger, Esq.

Attorney/Agent for Applicant(s)

Reg No. : 42,422

Date : November 27, 2007

Telephone : (303) 298-9888

Rev 10/07 (E-TransAmd)

Electronic Patent Application Fee Transmittal

Application Number:	10973076
Filing Date:	25-Oct-2004
Title of Invention:	System and method for providing firmware recoverable lockstep protection
First Named Inventor/Applicant Name:	Scott L. Michaelis
Filer:	Guy Kenneth Clinger/Mariko Mizuno
Attorney Docket Number:	200404941-1

Filed as Large Entity

Utility Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Statutory disclaimer	1814	1	130	130
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
			Total in USD ($)	**130**

Electronic Acknowledgement Receipt

EFS ID:	2513738
Application Number:	10973076
International Application Number:	
Confirmation Number:	6989
Title of Invention:	System and method for providing firmware recoverable lockstep protection
First Named Inventor/Applicant Name:	Scott L. Michaelis
Customer Number:	22879
Filer:	Guy Kenneth Clinger/Mariko Mizuno
Filer Authorized By:	Guy Kenneth Clinger
Attorney Docket Number:	200404941-1
Receipt Date:	27-NOV-2007
Filing Date:	25-OCT-2004
Time Stamp:	15:53:16
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1		200404941-1_Response.pdf	45142 a48eb2c205ce145aa1eab915c21eaaaaed51d399	yes	19

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment - After Non-Final Rejection	1	1
	Claims	2	8
	Specification	9	16
	Applicant Arguments/Remarks Made in an Amendment	17	19

Warnings:					
Information:					
2	Terminal Disclaimer Filed	200404941-1_Terminal_Disclaimer.pdf	317890 1d6261e7184fbd47116de62f94d105d9eea0049b	no	1
Warnings:					
Information:					
3	Fee Worksheet (PTO-06)	E_TransAmd.pdf	27720 3474d358b91dea9991ef56493229ee86c60f1978	no	1
Warnings:					
Information:					
4	Fee Worksheet (PTO-06)	fee-info.pdf	8179 44fc54afa07e5f4032e54448a2c8213fdf9ab8ce	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	398931		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PATENT APPLICATION

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
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Fort Collins, Colorado 80527-2400

ATTORNEY DOCKET NO. 200404941-1

Inventor(s): Scott L. Michaelis et al.

Confirmation No.: 6989

Application No.: 10/973,076

Examiner: Dieu Minh T. Le

Filing Date: October 25, 2004

Group Art Unit: 2114

Title: SYSTEM AND METHOD FOR PROVIDING FIRMWARE RECOVERABLE LOCKSTEP PROTECTION

Commissioner For Patents
P0 Box 1450
Alexandria, VA 22313-1 450

TERMINAL DISCLAIMER RESPONSIVE TO A PROVISIONAL DOUBLE PATENTING REJECTION

Petitioner, Hewlett-Packard Development Company, L.P. is the owner of 100 percent interest in the instant application. Petitioner hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application, which would extend beyond the expiration date of the full statutory term defined in 35 U.S. C. 154 to 156 and 173 as shortened by any terminal disclaimer filed prior to the grant of any patent granted on pending co-owned Application Numbers 10/973,003, 10/973,075, 10/972,888 and 10/972,796, all filed on October 25, 2004. Petitioner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and all patents that may be granted on the pending co-owned applications listed above are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, petitioner does not disclaim the terminal part of any patent granted on the instant application that would extend to the expiration date of the full statutory term as defined in 35 U.S.C. 154 to 156 and 173 of any patent granted on the pending co-owned applications listed above, as shortened by any terminal disclaimer filed prior to the patent grant, in the event that any such granted patent: expires for failure to pay a maintenance fee, is held unenforceable, is found invalid by a court of competent jurisdiction, is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321, has all claims canceled by a reexamination certificate, is reissued, or is in any manner terminated prior to the expiration of its full statutory term as shortened by any terminal disclaimer filed prior to its grant.

For submissions on behalf of an organization (e.g., corporation), the undersigned is empowered to act on behalf of the organization.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Please charge the required fee set forth in 37 CFR 1.20(d) of $130.00 to Deposit Account 08-2025. At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees.

Note: An attorney or agent of record must sign this document

Respectfully submitted,

Scott L. Michaelis et al.

By: SLWebb

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Attorney/Agent for Applicant(s)

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Document code: WFEE

United States Patent and Trademark Office
Sales Receipt for Accounting Date: 12/14/2007

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01 FC : 1814 130.00 DA

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Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	
10/973,076	10/25/2004	☐ To be Mailed

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY ☐ RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT 11/27/2007	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 35	Minus	** 35	= 0	X $ =		OR	X $50=	0
Independent (37 CFR 1.16(h))	* 5	Minus	***5	= 0	X $ =		OR	X $210=	0
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)	OR	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
alexander jenkins

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/973,076	10/25/2004	Scott L. Michaelis	200404941-1	6989

22879 7590 09/12/2007
HEWLETT PACKARD COMPANY
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INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER
LE, DIEU MINH T

ART UNIT	PAPER NUMBER
2114	

MAIL DATE	DELIVERY MODE
09/12/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/973,076	MICHAELIS ET AL.	
	Examiner	Art Unit	
	Dieu-Minh Le	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 25 October 2004.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-35 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-35 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 10/25/04 is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 10/25/04.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

Part III DETAILED ACTION

Specification

1. This Office Action is in response to the application 10/973,076 filed on 10/25/04.

2. Claims 1-35 are presented for examination.

3. The disclosure is objected to because of the following informalities: Applicant is required to update all the related applications with the Serial No. or U.S. Patents No. on pages 1, 9, 14, 17-20.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 29-35 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 31, the phrase "of claim 19" should be changed to --claim 29-- because claim 29 is a system claim.

Double Patenting Rejections

5. Claims 1-35 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-27 of U.S. application 10/973,003; claims 1-20 of U.S. application 10/973,075; claims 1-38 of U.S application 10/972,888 and claims 1-26 of U.S. application 10/972,796. Although the conflicting claims are not identical, they are not patentably distinct from each other because the claimed subject matter contains obvious modifications to previous claims 1-27 of U.S. application 10/973,003; claims 1-20 of U.S. application 10/973,075; claims 1-38 of U.S application 10/972,888 and claims 1-26 of U.S. application 10/972,796.

As to claims 1, 15, 21 and 29, these claims include limitations of: detecting loss of lockstep, recover or

reestablishing lockstep for the lockstep pair of processors, which already included in claims 1-27 of U.S. application 10/973,003; claims 1-20 of U.S. application 10/973,075; claims 1-38 of U.S application 10/972,888 and claims 1-26 of U.S. application 10/972,796. It is well settled that the omission of an element and its function [i.e.,firmware] is an obvious expedient if the remaining elements perform the same function as before. In re Karlson, 136, USPQ 184 (CCPA 1963). Also note Ex parte Rainu, 168 USPQ 375 (Bd. App. 1969). Therefore, omitting various elements from the previous claimed subject matter would have been obvious to one of ordinary skill in the art in this case since the remaining elements do in fact perform the same functions as before. Elimination/Changing of an element or its function will not serve as a basis for patentability.

4. The obviousness-type double patenting rejection is a judicially established doctrine based upon public policy and is primarily intended to prevent prolongation of the patent term by prohibiting claims in a second patent not patentably distinct from claims in a first patent. *In re Vogel*, 164 USPQ 619 (CCPA 1970). A timely filed terminal disclaimer in compliance with 37 C.F.R. § 1.321(b) would overcome an actual or provisional rejection on this ground provided the conflicting application or

patent is shown to be commonly owned with this application. See 37 C.F.R. § 1.78(d).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Marshall et al. (U.S. Patent 5,915,082 hereafter referred to as Marshall) in view of Safford et al. (U.S. Patent 7,085,959 hereafter referred to as Safford).

As per claim 1:

Marshall substantially teaches the invention. Marshall teaches:

- A method comprising:
- detecting loss of lockstep for a lockstep pair of processors [col. 1, lines 10-19; col. 2, lines 53-59; col. 12, claim 1];
- recover lockstep (i.e., fail-over process) for the lockstep pair of processors, to recognize the lockstep pair of processors having recovered lockstep [abstract, col. 2, lines 53-65; col. 3, lines 1-15].

Marshall does not explicitly address:
- using firmware to trigger an operating system to idle the lockstep pair of processors.

However, Marshall does disclose capability of:
- An error detection and fault isolation for lockstep processor systems [abstract, col. 1, lines 10-20] comprising:
- a data connectivity among multi-processors, firmware, OS, error detection and recovery, user interface, etc…. [fig. 2, col. 4, lines 13-35];

- ***configuring and error signaling used to enhance recovery from loss of lockstep in a multi-processors system***

[abstract, col. 2, lines 11-24 and col. 12, claim 1].

In addition, Safford explicitly teaches:

- A method and apparatus for recovery from loss of lock step [abstract, col. 2, lines 13-32] comprising:
- capability to signal the computer system (i.e., operating system) to idle the lockstep of processors [col. 4, lines 30-63].

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of Applicant's invention to first realizing Marshall's ***configuring and error signaling used to enhance recovery from loss of lockstep in a multi-processors system*** as being the use of firmware to trigger an operating system to idle the lockstep pair of processors as claimed by Applicant. This is because Marshall's mutli-data processors /fault tolerant system explicitly performed data failure detection and recovery (i.e., ***loss of lockstep*** and/or ***fail-over***) within plurality of processors via ***state information, parity information***, and ***boot information*** processes. By utilizing these capabilities, the multi-data processing system can be

directed or redirected promptly and functioned properly during failover recovery process in supporting the system operation; second, by applying the ***configuring and error signaling used to enhance recovery from loss of lockstep in a multi-processors system*** as taught by Safford in conjunction with the error detection and fault isolation for lockstep processor systems as taught by Marshall, the multi-processors within fault tolerant/failure recovery networking system including master/slave capability (i.e., failover) can enhance its operation performance, more specifically to ensuring the error detected, corrected, and replaced (i.e., backup) in proper and efficient manner via its state information functionality.

This modification would have been obvious because a person having ordinary skill in the art would have been motivated to do so to improve the multi-data processors, failover, and/or fault-tolerant system operation availability and network/system performance therein with a mechanism to enhance the data connectivity, data debugging, data reliability, and data throughput which eventually will increase its performance, such as data throughput between internal and external devices.

As per claims 2-3:

Marshall further teaches:

- detecting loss of lockstep for a lockstep pair of processors [col. 1, lines 10-19; col. 2, lines 53-59; col. 12, claim 1];
- recognizing a master processor (i.e., ***master/slave processors***) of the lockstep pair of processors [abstract, col. 3, lines 1-15].

Marshall does not explicitly address:
- using firmware to trigger an operating system .

However, Marshall does disclose capability of:
- An error detection and fault isolation for lockstep processor systems [abstract, col. 1, lines 10-20] comprising:
- a data connectivity among multi-processors, firmware, OS, error detection and recovery, user interface, etc…. [fig. 2, col. 4, lines 13-35];
- ***configuring and error signaling used to enhance recovery from loss of lockstep in a multi-processors system*** [abstract, col. 2, lines 11-24 and col. 12, claim 1].

In addition, Safford explicitly teaches:

- A method and apparatus for recovery from loss of lock step [abstract, col. 2, lines 13-32] comprising:
- capability to signal the computer system (i.e., operating system) to idle the lockstep of processors [col. 4, lines 30-63].

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of Applicant's invention to first realizing Marshall's ***configuring and error signaling used to enhance recovery from loss of lockstep in a multi-processors system*** as being the use of firmware to trigger an operating system to idle the lockstep pair of processors as claimed by Applicant. This is because Marshall's mutli-data processors /fault tolerant system explicitly performed data failure detection and recovery (i.e., ***loss of lockstep*** and/or ***fail-over***) within plurality of processors via ***state information, parity information***, and ***boot information*** processes. By utilizing these capabilities, the multi-data processing system can be directed or redirected promptly and functioned properly during failover recovery process in supporting the system operation; second, by applying the ***configuring and error signaling used to enhance recovery from loss of lockstep in a multi-processors system*** as taught by Safford in conjunction with the error

detection and fault isolation for lockstep processor systems as taught by Marshall, the multi-processors within fault tolerant/failure recovery networking system including master/slave capability (i.e., failover) can enhance its operation performance, more specifically to ensuring the error detected, corrected, and replaced (i.e., backup) in proper and efficient manner via its state information functionality for the same reasons set forth as described in claim 1, **supra.**

As per claims 4-10:

Marshall further teaches:

- detecting corrupt data in one of said lockstep pair of processors [col. 6, lines 3-27 and col. 7, lines 15-27].
- detecting loss of lockstep for a lockstep pair of processors [col. 1, lines 10-19; col. 2, lines 53-59; col. 12, claim 1];
- responsive to said detecting loss of lockstep, using said firmware to determine if lockstep is recoverable for the lockstep pair of processors [col. 3, lines 22-50];
- determining that the loss of lockstep is or is not recoverable [col. 3, lines 22-50].

Marshall does not explicitly address:

- lockstep mismatch…

However, Marshall does disclose capability of:

- An error detection and fault isolation for lockstep processor systems [abstract, col. 1, lines 10-20] comprising:

- a data connectivity among multi-processors, firmware, OS, error detection and recovery, user interface, etc…. [fig. 2, col. 4, lines 13-35];

- ***configuring and error signaling used to enhance recovery from loss of lockstep in a multi-processors system*** [abstract, col. 2, lines 11-24 and col. 12, claim 1] via ***comparison (as well as miscomparing) process (i.e., lockstep mismatch) in supporting the error detection and correction*** [col. 3, lines 1-14; col. 7, lines 28-50; and col. 12, claim 1].

In addition, Safford explicitly teaches:

- A method and apparatus for recovery from loss of lock step [abstract, col. 2, lines 13-32] comprising:

- ***capability to signal the computer system (i.e., operating system) to idle the lockstep of processors*** [col. 4, lines

30-63] via ***comparison results of lockstep within processors*** [col. 2, lines 55 through col. 3, lines 9].

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of Applicant's invention to first realizing Marshall's ***configuring and error signaling used to enhance recovery from loss of lockstep in a multi-processors system*** via ***comparison (as well as miscomparing) process (i.e., lockstep mismatch) in supporting the error detection and correction*** as being the lockstep mismatch...as claimed by Applicant. This is because Marshall's mutli-data processors /fault tolerant system explicitly performed data failure detection and recovery (i.e., ***loss of lockstep*** and/or ***fail-over***) within plurality of processors via ***state information, parity information***, and ***boot information*** processes; second, by applying the ***configuring and error signaling used to enhance recovery from loss of lockstep in a multi-processors system*** *via* ***comparison results of lockstep within processors*** as taught by Safford in conjunction with the error detection and fault isolation for lockstep processor systems as taught by Marshall, the multi-processors within fault tolerant/failure recovery networking system including master/slave capability (i.e., failover) can enhance its operation performance, more

specifically to ensuring the error detected, corrected, and replaced (i.e., backup) in proper and efficient manner via its state information functionality.

This modification would have been obvious because a person having ordinary skill in the art would have been motivated to do so to improve the data processing system operation availability and memory/system performance.

As per claims 11-14:

Marshall further teaches:

- swapping (i.e., master/slave role) the role of system boot processor to another processor in the system [col. 3, lines 1-14].
- recovering the lockstep for the lockstep pair of processors [abstract, col. 2, lines 53-65; col. 3, lines 1-15];
- responsive to said detecting loss of lockstep, using said firmware to determine if lockstep is recoverable for the lockstep pair of processors [col. 3, lines 22-50];
- determining that the loss of lockstep is or is not recoverable [col. 3, lines 22-50].

Marshall does not explicitly address:

- boot processor.

However, Marshall does disclose capability of:

- An error detection and fault isolation for lockstep processor systems [abstract, col. 1, lines 10-20] comprising:

- a data connectivity among multi-processors, firmware, OS, error detection and recovery, user interface, etc…. [fig. 2, col. 4, lines 13-35];

- ***configuring and error signaling used to enhance recovery from loss of lockstep in a multi-processors system*** [abstract, col. 2, lines 11-24 and col. 12, claim 1] via ***retry operation (i.e., reboot or boot processor)*** [col. 8, lines 27-38 and col. 9, lines 1-30].

In addition, Safford explicitly teaches:

- A method and apparatus for recovery from loss of lock step [abstract, col. 2, lines 13-32] comprising:

- ***capability to signal the computer system (i.e., operating system) to idle the lockstep of processors*** [col. 4, lines 30-63] via ***reboot processor*** [col. 5, claim 3].

- switching or changing spare processor to an active processor via an architecture state (i.e., ***system information state***) [col. 5, claim 1].

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of Applicant's invention to first realizing Marshall's ***configuring and error signaling used to enhance recovery from loss of lockstep in a multi-processors system*** via ***retry operation (i.e., reboot or boot processor)*** as being boot processor as claimed by Applicant. This is because Marshall's mutli-data processors /fault tolerant system explicitly performed data failure detection and recovery (i.e., ***loss of lockstep*** and/or ***fail-over***) within plurality of processors via ***state information, parity information***, and ***boot information*** processes; second, by applying the ***configuring and error signaling used to enhance recovery from loss of lockstep in a multi-processors system*** *via* ***reboot processor*** as taught by Safford in conjunction with the error detection and fault isolation for lockstep processor systems as taught by Marshall, the multi-processors within fault tolerant/failure recovery networking system including master/slave capability (i.e., failover) can enhance its operation performance, more specifically to ensuring the error detected, corrected, and

replaced (i.e., backup) in proper and efficient manner via its state information functionality.

This modification would have been obvious because a person having ordinary skill in the art would have been motivated to do so to improve the multi-data processors, failover, and/or fault-tolerant system operation availability and network/system performance therein with a mechanism to enhance the data connectivity, data debugging, data reliability, and data throughput which eventually will increase its performance, such as data throughput between internal and external devices.

As per claims 15-20:

Due to the similarity of claims 15-20 to claims 1-14 except for ***a system*** comprising master/slave processors, firmware operable to detection of loss of lockstep, a parity based mechanism, etc… instead of ***a method*** comprising master/slave processors, firmware operable to detection of loss of lockstep, a parity based mechanism, etc…; therefore, these claims are also rejected under the same rationale applied against claims 1-14. **In addition, all of the limitations have been noted in the rejection as per claims 1-14. Such as,** Marshall discloses capability of error detection and fault isolation for lockstep processor systems [abstract, col. 1, lines 10-20] comprising ***a***

data connectivity among multi-processors, firmware, OS, MASTER/SLAVE PROCESSORS, error detection and recovery, user interface, etc…. [fig. 2, col. 4, lines 13-35].

As per claims 21-25:

These claims are the same as per claims 1-14. The only minor different is that these claims are directed to ***a system comprising firmware that includes computer-executable software code stored to a computer readable medium*** comprising code, responsive to detection of loss of lockstep, code, responsive to determining that the lockstep is recoverable, etc…instead ***a method*** comprising master/slave processors, firmware operable to detection of loss of lockstep, a parity based mechanism, etc…as described in claims 1-14. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to realize that a ***computer readable medium*** is a necessary item for such computer networking system, more specifically to system for detecting and recovery corrupted boot failure. Since the recovery data failure within the computing system obviously needs a means for instruction or code means resided within the computer readable storage medium for performing the data storing, receiving, transmitting operation via the data capturing, detecting, and restoring

functionalities. Therefore, these claims are also rejected under the same rationale applied against claims 1-14.

As per claims 26-28:

These claims are the same as per claims 1-14. The only minor different is that these claims are directed to ***a multi-processor system having a hot spare processor*** comprising detecting loss of lockstep, copying a state of the system boot processor to the hot spare processor, etc…instead ***a method*** comprising master/slave processors, firmware operable to detection of loss of lockstep, a parity based mechanism, etc…as described in claims 1-14. **In addition, all of the limitations have been noted in the rejection as per claims 1-14. Such as,** Marshall discloses capability of error detection and fault isolation for lockstep processor systems [abstract, col. 1, lines 10-20] comprising ***a data connectivity among multi-processors, firmware, OS, MASTER/SLAVE PROCESSORS, error detection and recovery, user interface, etc….*** [fig. 2, col. 4, lines 13-35. In addition, Safford explicitly teaches the method and apparatus for recovery from loss of lock step [abstract, col. 2, lines 13-32] comprising capability to signal the computer system (i.e., operating system) to idle the lockstep of processors [col. 4, lines 30-63] via reboot processor [col. 5,

claim 3]. Safford further illustrates ***switching or changing spare processor to an active processor via an architecture state*** (i.e., ***system information state***) [col. 5, claim 1].

As per claims 29-35:

Due to the similarity of claims 29-35 to claims 1-14 except for ***a system*** comprising MEANS for detecting loss of lockstep, MEANS for responsive to the determining means, a parity based MEANS, etc… instead of ***a method*** comprising detecting loss of lockstep, firmware operable to detection of loss of lockstep, a parity based mechanism, etc…; therefore, these claims are also rejected under the same rationale applied against claims 1-14. **In addition, all of the limitations have been noted in the rejection as per claims 1-14. Such as,** Marshall discloses capability of error detection and fault isolation for lockstep processor systems [abstract, col. 1, lines 10-20] comprising ***a data connectivity among multi-processors, firmware, OS, MASTER/SLAVE PROCESSORS, error detection and recovery, user interface, etc….*** [fig. 2, col. 4, lines 13-35.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

9. A shortened statutory period for response to this action is set to expired THREE (3) months, ZERO days from the date of this letter. Failure to respond within the period for response will cause the application to be abandoned. 35 U.S.C. 133.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dieu-Minh Le whose telephone number is (703)305-9408. The examiner can normally be reached on Monday - Thursday from 8:30 AM to 6:30 PM.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dieu-Minh Le whose telephone number is (571) 272-3660. The examiner can normally be reached on Monday - Thursday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571)272-3644. The Tech Center 2100 phone number is (571) 272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DIEU-MINH THAI LE
PRIMARY EXAMINER
ART UNIT 2114

DML
09/02/07

FORM PTO-1449 LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	ATTY. DOCKET NO. 200404941-1	APPLICATION NO. 10/973,076	CONFIRMATION NO.
	APPLICANT Scott L. Michaelis et al.		
	FILING DATE 10/25/04	GROUP 2114	

REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
AML	1A	5,226,152	07/06/1993	Klug et al.	
	1B	5,249,188	09/28/1993	McDonald	
	1C	5,751,932	05/12/1998	Horst et al.	
	1D	5,758,058	05/26/1998	Milburn	
	1E	5,764,660	06/09/1998	Mohat	
	1F	6,065,135	05/16/2000	Marshall et al.	
	1G	6,148,348	11/14/2000	Garnett et al.	
	1H	6,473,869	10/29/2002	Bissett et al.	
	1I	6,560,682	05/06/2003	Miller et al.	
✓	1J	6,604,177	08/05/2003	Kondo et al.	
AML	1K	6,615,366	09/02/2003	Grochowski et al.	

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	1L					
	1M					
	1N					
	1O					
	1P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

AML	1Q	Attorney Docket No. 200404946-1, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR USING INFORMATION RELATING TO A DETECTED LOSS OF LOCKSTEP FOR DETERMINING A RESPONSIVE ACTION "
AML	1R	Attorney Docket No. 200404944-1, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR ESTABLISHING A SPARE PROCESSOR FOR RECOVERING FROM LOSS OF LOCKSTEP IN A BOOT PROCESSOR"
AML	1S	Attorney Docket No. 200404943-1, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR CONFIGURING LOCKSTEP MODE OF A PROCESSOR MODULE"

EXAMINER	DATE CONSIDERED
[illegible]	8/22/07

Rev 05/04 (PTO1449)

FORM PTO-1449 LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	ATTY. DOCKET NO. 200404941-1	APPLICATION NO. 10/973,076	CONFIRMATION NO.
	APPLICANT Scott L. Michaelis et al.		
	FILING DATE 10/25/04	GROUP 2114	

REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
BAL	2A	6,625,749	09/23/2003	Quach	
	2B	6,687,851	02/03/2004	Somers et al.	
	2C	6,754,787	06/22/2004	Miller et al.	
	2D	2002/0144177	10/03/2002	Kondo et al.	
	2E	2003/0070050	04/10/2003	Miller et al.	
	2F	2004/0006722	01/08/2004	Safford	
✓	2G	2004/0019771	01/29/2004	Quach	
BAL	2H	2004/0153857	08/05/2004	Yamazaki et al.	
	2I				
	2J				
	2K				

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	2L					
	2M					
	2N					
	2O					
	2P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

BAL	2Q	Attorney Docket No. 200404974-1, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR MAINTAINING IN A MULTI-PROCESSOR SYSTEM A SPARE PROCESSOR THAT IS IN LOCKSTEP FOR USE IN RECOVERING FROM LOSS OF LOCKSTEP FOR ANOTHER PROCESSOR
BAL	2R	Attorney Docket No. 200404973-1, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR SWITCHING THE ROLE OF BOOT PROCESSOR TO A SPARE PROCESSOR RESPONSIVE TO DETECTION OF LOSS OF LOCKSTEP IN A BOOT PROCESSOR"
BAL	2S	Attorney Docket No. 200404971-1, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR REESTABLISHING LOCKSTEP FOR A PROCESSOR MODULE FOR WHICH LOSS OF LOCKSTEP IS DETECTED"

EXAMINER	DATE CONSIDERED
Brad Hoch	08/12/07

FORM PTO-1449	ATTY. DOCKET NO.	APPLICATION NO.	CONFIRMATION NO.
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT	200404941-1	10/973,076	
	APPLICANT: Scott L. Michaelis et al.		
(Use several sheets if necessary)	FILING DATE: 10/25/04	GROUP: 2114	

REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	3A				
	3B				
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FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	3L					
	3M					
	3N					
	3O					
	3P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

BRL	3Q	Attorney Docket No. 200404970-1, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR SYSTEM FIRMWARE CAUSING AN OPERATING SYSTEM TO IDLE A PROCESSOR"
BRL	3R	Attorney Docket No. 200404972-1, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR REINTRODUCING A PROCESSOR MODULE TO AN OPERATING SYSTEM AFTER LOCKSTEP RECOVERY"
	3S	

EXAMINER	DATE CONSIDERED
[signature]	08/22/07

Notice of References Cited	Application/Control No. 10/973,076	Applicant(s)/Patent Under Reexamination MICHAELIS ET AL.	
	Examiner Dieu-Minh Le	Art Unit 2114	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-5,915,082	06-1999	Marshall et al.	714/11
*	B	US-7,085,959	08-2006	Safford, Kevin David	714/11
*	C	US-6,625,749	09-2003	Quach, Nhon	714/10
*	D	US-6,920,581	07-2005	Bigbee et al.	714/10
*	E	US-2005/0172164	08-2005	Fox et al.	714/013
*	F	US-2003/0140281	07-2003	Fu et al.	714/38
*	G	US-2005/0240829	10-2005	Safford et al.	714/043
*	H	US-2005/0240806	10-2005	Bruckert et al.	714/006
*	I	US-7,191,292	03-2007	Chaudhry et al.	711/133
*	J	US-2006/0136672	06-2006	Chaudhry et al.	711/122
*	K	US-7,020,800	03-2006	Fu et al.	714/38
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
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	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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Bib Data Sheet

CONFIRMATION NO. 6989

SERIAL NUMBER	FILING OR 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
10/973,076	10/25/2004 RULE	714	2114	200404941-1

APPLICANTS

Scott L. Michaelis, Plano, TX;
Anurupa Rajkumari, Round Rock, TX;
William B. McHardy, Fort Collins, CO;

**** CONTINUING DATA ******************************** N/A [illegible]

**** FOREIGN APPLICATIONS ******************************** N/A [illegible]

IF REQUIRED, FOREIGN FILING LICENSE GRANTED **
12/08/2004

	STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
Foreign Priority claimed ☐ yes ☒ no 35 USC 119 (a-d) conditions met ☐ yes ☒ no ☐ Met after Allowance Verified and Acknowledged [signature] Examiner's Signature Initials	TX	5	35	5

ADDRESS
22879

TITLE
System and method for providing firmware recoverable lockstep protection

FILING FEE RECEIVED		
1236	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

Index of Claims

Application/Control No.	Applicant(s)/Patent under Reexamination
10/973,076	MICHAELIS ET AL.
Examiner	**Art Unit**
Dieu-Minh Le	2114

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
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Claim Final	Claim Original	Date 9/2/07							
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Search Notes	Application/Control No.	Applicant(s)/Patent under Reexamination
	10/973,076	MICHAELIS ET AL.
	Examiner	**Art Unit**
	Dieu-Minh Le	2114

SEARCHED			
Class	Subclass	Date	Examiner
714	11	8/22/2007	DML
	12		
	13		
	10		
712	31	8/22/2007	DML

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
EAST search files US-PGPUB, USPAT, USOCR, EPO, JPO, DERWENT, IBM-TDB.	8/22/2007	DML
Inventor names search.	8/22/2007	DML

PALM Intranet

Application Number Submit

IDS Flag Clearance for Application 10973076

IDS Information

Content	Mailroom Date	Entry Number	IDS Review	Last Modified	Reviewer
WIDS	2004-10-25	8	Y ☑	2007-09-04 05:41:10.0	MLe
Update					

10/973,076

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2222	lockstep lock-step	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 15:21
L3	25008	(loss adj 1) LOL	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 15:22
L4	51	(detect$3 or track$4) adj 3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 15:23
L5	1547	(boot$4 or initializ$4) adj processor	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 16:41
L6	246	spare adj processor	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 15:27
L7	12	4 and 5 and 6	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 15:30
L8	25	(michaelis-scott$ or myer-sylvia$ or mchardy-william$).in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 16:14
L10	632	(714/10).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 15:33

EAST Search History

L11	95	(712/31).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 16:08
L12	52536	(switch$4 chang$4 failover fail-over "fail over") same (spare slave redundan$4 backup back-up "back up" second$4) same processor	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 16:54
L13	81	12 same 5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 16:28
L14	168219	without same ("shut$4 down" stop$4 idle interrupt$4) same (OS "operating system")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 16:33
L15	6	13 and 14	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 16:33
L16	20342	multi-processor "multi processor" and 3 and 5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 16:45
L17	176	16 and 12 and 14	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 16:46
L18	7	17 and 6	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 16:53

EAST Search History

L19	87	(recover$4 reestablish$3 restart$3) with 1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 16:54
L20	31827	(pair spare slave redundan$4 backup back-up "back up" second$4) adj2 processor	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 16:55
L21	101834	firmware	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 16:56
L22	21	19 and 20 and 21	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 16:57
S1	14	(("7085959") or ("20050172164") or ("5675794") or ("6438687") or ("6920581") or ("5915082") or ("6625749")).PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/08/26 17:54
S2	2	("7085959").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/08/27 15:05
S3	730	(714/11).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/27 15:06
S4	337	(714/12).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/29 15:32

EAST Search History

S5	606	(714/13).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/27 15:07
S6	36	("20020144177"|"20030070050"|"20040006722"|"20040019771"|"20040153857"|"5226152"|"5249188"|"5751932"|"5758058"|"5764660"|"6065135"|"6148348"|"6473869"|"6560682"|"6604177"|"6615366"|"6625749"|"6687851"|"6754787").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/27 15:08
S7	44	("20020144177"|"20030070050"|"20040006722"|"20040019771"|"20040153857"|"6625749"|"6687851"|"6754787")".PN"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/27 15:09

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P. O. Box 272400
Fort Collins, Colorado 80527-2400

102504

14230 U.S. PTO

PATENT APPLICATION

ATTORNEY DOCKET NO. 200404941-1

IN THE U.S. PATENT AND TRADEMARK OFFICE
Patent Application Transmittal Letter

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

13441 U.S. PTO
10/973076
102504

Sir:

Transmitted herewith for filing under 37 CFR 1.53(b) is a(n): (X) Utility ( ) Design
(X) original patent application,
( ) continuation-in-part application

INVENTOR(S): **Scott L. Michaelis et al.**

TITLE: **SYSTEM AND METHOD FOR PROVIDING FIRMWARE RECOVERABLE LOCKSTEP PROTECTION**

Enclosed are:

(X) The Declaration and Power of Attorney. (X) signed ( ) unsigned or partially signed

(X) 5 sheets of drawings (one set) ( ) Associate Power of Attorney

( ) Form PTO-1449 (X) Information Disclosure Statement and Form PTO-1449

( ) Priority document(s) ( ) (Other) _____ (fee $_____)

CLAIMS AS FILED BY OTHER THAN A SMALL ENTITY				
(1) FOR	(2) NUMBER FILED	(3) NUMBER EXTRA	(4) RATE	(5) TOTALS
TOTAL CLAIMS	35 — 20	15	X $18	$ 270
INDEPENDENT CLAIMS	5 — 3	2	X $88	$ 176
ANY MULTIPLE DEPENDENT CLAIMS	0		$300	$ 0
BASIC FEE: Design ($350.00); Utility ($790.00)				$ 790
TOTAL FILING FEE				$ 1,236
OTHER FEES				$
TOTAL CHARGES TO DEPOSIT ACCOUNT				$ 1,236

Charge $ 1,236 to Deposit Account 08-2025. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

"Express Mail" label no. EV 375345153US

Date of Deposit Oct. 25, 2004

I hereby certify that this is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to: Commissioner for Patents, Alexandria, VA 22313-1450

By _____

Typed Name: Phyllis Ewing

Respectfully submitted,

Scott L. Michaelis et al.

By _____

Jody C. Bishop

Attorney/Agent for Applicant(s)
Reg. No. 44,034
Date: Oct. 25, 2004
Telephone No.: (214) 855-8007

- Attach as First Page to Transmitted Papers -

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR U.S. LETTERS PATENT

Title:

SYSTEM AND METHOD FOR PROVIDING FIRMWARE RECOVERABLE LOCKSTEP PROTECTION

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SYSTEM AND METHOD FOR PROVIDING FIRMWARE RECOVERABLE LOCKSTEP PROTECTION

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present application is related to the following concurrently filed and commonly assigned U.S. Patent Applications: Serial No. _____ [Attorney Docket No. 200404944-1] titled "SYSTEM AND METHOD FOR ESTABLISHING A SPARE PROCESSOR FOR RECOVERING FROM LOSS OF LOCKSTEP IN A BOOT PROCESSOR"; Serial No. _____ [Attorney Docket No. 200404943-1] titled "SYSTEM AND METHOD FOR CONFIGURING LOCKSTEP MODE OF A PROCESSOR MODULE"; Serial No. _____ [Attorney Docket No. 200404946-1] titled "SYSTEM AND METHOD FOR USING INFORMATION RELATING TO A DETECTED LOSS OF LOCKSTEP FOR DETERMINING A RESPONSIVE ACTION"; Serial No. _____ [Attorney Docket No. 200404973-1 titled "SYSTEM AND METHOD FOR SWITCHING THE ROLE OF BOOT PROCESSOR TO A SPARE PROCESSOR RESPONSIVE TO DETECTION OF LOSS OF LOCKSTEP IN A BOOT PROCESSOR"; Serial No. _____ [Attorney Docket No. 200404971-1] titled "SYSTEM AND METHOD FOR REESTABLISHING LOCKSTEP FOR A PROCESSOR MODULE FOR WHICH LOSS OF LOCKSTEP IS DETECTED"; Serial No. _____ [Attorney Docket No. 200404970-1] titled "SYSTEM AND METHOD FOR SYSTEM FIRMWARE CAUSING AN OPERATING SYSTEM TO IDLE A PROCESSOR"; Serial No. _____ [Attorney Docket No. 200404972-1] titled "SYSTEM AND METHOD FOR REINTRODUCING A PROCESSOR MODULE TO AN OPERATING SYSTEM AFTER LOCKSTEP RECOVERY"; and Serial No. _____ [Attorney Docket No. 200404974-1] titled "SYSTEM AND METHOD FOR MAINTAINING IN A MULTI-PROCESSOR SYSTEM A SPARE PROCESSOR THAT IS IN LOCKSTEP FOR USE IN RECOVERING FROM LOSS OF LOCKSTEP FOR ANOTHER PROCESSOR", the disclosures of which are hereby incorporated herein by reference.

DESCRIPTION OF RELATED ART

[0002] Silent Data Corruption ("SDC") is a difficult problem in the computing industry. In general, SDC refers to data that is corrupt, but which the system does not detect as being corrupt. SDCs primarily occur due to one of two factors: a) a broken hardware unit or b) a "cosmic" event that causes values to change somewhere in the system. Broken hardware means

that a "trusted" piece of hardware is silently giving wrong answers. For example, the arithmetic unit in a processor is instructed to add 1+1 and it returns the incorrect answer 3 instead of the correct answer 2. An example of a cosmic event is when a charged particle (e.g., alpha particle or cosmic ray) strikes a region of a computing system and causes some bits to change value (e.g., from a 0 to a 1 or from a 1 to a 0).

[0003] Numerous techniques have been developed for detecting SDC to prevent the SDC from remaining "silent" or "undetected" within a system, as well as preventing such SDC from propagating through the system. Examples of these techniques include parity-based mechanisms and error correcting codes (ECCs) on buses and memory locations, as well as checksums and/or cyclic redundancy checks (CRC) over regions of memory. Parity-based mechanisms are often employed in processors, wherein a parity bit is associated with each block of data when it is stored. The parity bit is set to one or zero according to whether there is an odd or even number of ones in the data block. When the data block is read out of its storage location, the number of ones in the block is compared with the parity bit. A discrepancy between the values indicates that the data block has been corrupted. ECCs are parity-based mechanisms that track additional information for each data block. The additional information allows the corrupted bit(s) to be identified and corrected.

[0004] Parity/ECC mechanisms have been employed extensively for caches, memories, and similar data storage arrays. In the remaining circuitry on a processor, such as data paths, control logic, execution logic, and registers (the "execution core"), it is more difficult to apply parity/ECC mechanisms for SDC detection. Thus, there is typically some unprotected area on a processor in which data corruption may occur and the parity/ECC mechanisms do not prevent the corrupted data from actually making it out onto the system bus. One approach to SDC detection in an execution core (or other unprotected area of the processor chip) is to employ "lockstep processing." Generally, in lockstep processing two processors are paired together, and the two processors perform exactly the same operations and the results are compared (e.g., with an XOR gate). If there is ever a discrepancy between the results of the lockstep processors, an error is signaled. The odds of two processors experiencing the exact same error at the exact same moment (e.g., due to a cosmic event occurring in both processors at exactly the same time or due to a mechanical failure occurring in each processor at exactly the same time) is nearly zero.

[0005] A pair of lockstep processors may, from time to time, lose their lockstep. "Loss of lockstep" (or "LOL") is used broadly herein to refer to any error in the pair of lockstep processors. One example of LOL is detection of data corruption (e.g., data cache error) in one of the processors by a parity-based mechanism and/or ECC mechanism. Another example of LOL is detection of the output of the paired processors not matching, which is referred to herein as a "lockstep mismatch." It should be recognized that in some cases the data in the cache of a processor may become corrupt (e.g., due to a cosmic event), which once detected (e.g., by a parity-based mechanism or ECC mechanism of the processor) results in LOL. Of course, unless such corrupt data is acted upon by the processor, the output of that processor will not fail to match the output of its paired processor and thus a "lockstep mismatch" will not occur. For example, suppose that a value of "1" is stored to first location of cache in each of a pair of lockstep processors and a value of "1" is also stored to a second location of cache in each of the pair of lockstep processors. Further suppose that a cosmic event occurs for a first one of the processors, resulting in the first location of its cache being changed from "1" to "0", and thus corrupted. This data corruption in the first processor is a LOL for the pair. An error detection mechanism of this first processor may detect the data corruption, thus detecting the LOL. If the processors are instructed to act on the data of their first cache locations, then a lockstep mismatch will occur as the output of each of the processors will not match. For instance, if the processors each add the data stored to the first location of their respective cache with the data stored to the second location of their respective cache, the first processor (having the corrupt data) will output a result of "1" (0+1=1) while the second processor outputs a result of "2" (1+1=2), and thus their respective outputs will not match.

[0006] By employing such techniques as parity-based error detection mechanisms and output comparisons for lockstep paired processors, SDC detection can be enhanced such that practically no SDC occurring in a processor goes undetected (and thus such SDC does not remain "silent") but instead results in detection of LOL. However, the issue then becomes how best for the system to respond to detected LOL. The traditional response to detected LOL has been to crash the system to ensure that the detected error is not propagated through the system. That is, LOL in one pair of lockstep processors in a system halts processing of the system even if other processors that have not encountered an error are present in the system. However, with the increased desire for many systems to maintain high availability, crashing the system each time LOL is detected is not an attractive proposition. This is particularly unattractive for large systems having many processors because cosmic events typically occur more frequently as the

processor count goes up, which would result in much more frequent system crashes in those large systems. High availability is a major desire for many customers having large, multi-processor systems, and thus having their system crash every few weeks is not an attractive option. Of course, permitting corrupt data to propagate through the system is also not a viable option.

[0007] Prior solutions attempting to resolve at least some detected SDCs without requiring the system to be crashed have been Operating System ("OS") centric. That is, in certain solutions the OS has been implemented in a manner to recover from a detected LOL without necessarily crashing the system. This OS-centric type of solution requires a lot of processor and platform specific knowledge to be embedded in the OS, and thus requires that the OS provider maintain the OS up-to-date as changes occur in later versions of the processors and platforms in which the OS is to be used. This is such a large burden that most commonly used OSs do not support lockstep recovery.

[0008] Certain solutions have attempted to recover from a LOL without involving the OS in such recovery procedure. For instance, in one technique upon LOL being detected, firmware is used to save the state of one of the processors in a lockstep pair (the processor that is considered "good") to memory, and then both processors of the pair are reset and reinitialized. Thereafter, the state is copied from the memory to each of the processors in the lockstep pair. This technique makes the processors unavailable for an amount of time without the OS having any knowledge regarding this unavailability, and if the amount of time required for recovery is too long, the system may crash. That is, typically, if a processor is unresponsive for X amount of time, the OS will assume that the processor is hung and will crashdump the system so that the problem can be diagnosed. Further, in the event that a processor in the pair cannot be reset and reinitialized (e.g., the processor has a physical problem and fails to pass its self-test), this technique results in crashing the system.

BRIEF SUMMARY OF THE INVENTION

[0009] According to at least one embodiment, a method comprises detecting loss of lockstep for a pair of processors. The method further comprises triggering, by firmware, an operating system to idle the processors, and recovering, by the firmware, lockstep between the pair of processors. After lockstep is recovered between the pair of processors, the method

further comprises triggering, by the firmware, the operating system to recognize the processors as being available for receiving instructions.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] FIGURE 1 shows an example embodiment of a system that uses firmware for controlling recovery from detected loss of lockstep (LOL);

[0011] FIGURE 2 shows a block diagram of one embodiment implemented for the IA-64 processor architecture;

[0012] FIGURE 3 shows an example system in which firmware utilizes a hot spare processor for recovering from LOL for the system's boot processor;

[0013] FIGURE 4 shows an example system having multi-processor cells in which an embodiment for using firmware for recovering from LOL may be employed;

[0014] FIGURE 5 shows a detailed operational flow diagram for one embodiment; and

[0015] FIGURE 6 shows a more general operational flow diagram for certain embodiments.

DETAILED DESCRIPTION

[0016] Turning to FIGURE 1, an example embodiment of a system 10 that uses firmware for controlling recovery from detected loss of lockstep (LOL) is shown. System 10 includes OS 11, as well as master processor 12A and slave processor 12B (collectively referred to as a lockstep processor pair 12). In certain implementations the lockstep processor pair 12 may be implemented on a single silicon chip, which is referred to as a "dual core processor" in which master processor 12A is a first core and slave processor 12B is a second core. Master processor 12A includes cache 14A, and slave processor 12B includes cache 14B. OS 11 and lockstep processor pair 12 are communicatively coupled to bus 16. Typically, master processor 12A and slave processor 12B are coupled to bus 16 via an interface that allows each of such processors to receive the same instructions to process, but such interface only communicates the output of master processor 12A back onto bus 16. The output of slave processor 12B is used solely for checking the output of mater processor 12A. While only one lockstep processor pair

12 is shown for simplicity in the example of FIGURE 1, system 10 may include any number of such lockstep processor pairs. As one specific example, system 10 may have 64 lockstep processor pairs, wherein the master processors of the pairs may perform parallel processing for the system.

[0017] In this example, master processor 12A includes error detect logic 13A, and slave processor 12B includes error detect logic 13B. While shown as included in each of the processors 12A and 12B in this example, in certain embodiments the error detect logic 13A and 13B may be implemented external to processors 12A and 12B. Error detect logic 13A and 13B include logic for detecting errors, such as data cache errors, present in their respective processors 12A and 12B. Examples of error detect logic 13A and 13B include known parity-based mechanisms and ECC mechanisms. Error detect logic 13C is also included, which may include an XOR (exclusive OR) gate, for detecting a lockstep mismatch between master processor 12A and slave processor 12B. As mentioned above, a lockstep mismatch refers to the output of master processor 12A and slave processor 12B failing to match. While shown as external to the lockstep processor pair 12 in this example, in certain embodiments error detect logic 13C may be implemented on a common silicon chip with processors 12A and 12B.

[0018] Lockstep mismatch is one way of detecting a LOL between the master processor 12A and slave processor 12B. A detection of an error by either of error detect logic 13A and 13B also provides detection of LOL in the processors 12A and 12B. Because the detection of LOL by error detect logic 13A and 13B may occur before an actual lockstep mismatch occurs, the detection of LOL by error detect logic 13A and 13B may be referred to as a detection of a "precursor to lockstep mismatch". In other words, once an error (e.g., corrupt data) is detected by error detect logic 13A or 13B, such error may eventually propagate to a lockstep mismatch error that is detectable by error detect logic 13C.

[0019] Firmware 15 is also included in system 10, which in this embodiment is invoked upon an error being detected by any of the error detect logics 13A, 13B, and 13C. In certain embodiments, processors 12A and 12B are processors from the Itanium Processor Family (IPF). IPF is a 64-bit processor architecture co-developed by Hewlett-Packard Company and Intel Corporation, which is based on Explicitly Parallel Instruction Computing (EPIC). IPF is a well-known family of processors. IPF includes processors such as those having the code names of MERCED, MCKINLEY, and MADISON. In addition to supporting a 64-bit processor bus and a set of 128 registers, the 64-bit design of IPF allows access to a very large memory (VLM)

and exploits features in EPIC. While a specific example implementation of one embodiment is described below for the IPF architecture, embodiments of firmware for recovering from LOL described herein are not limited in application to an IPF architecture, but may be applied as well to other architectures (e.g., 32-bit processor architectures, etc.).

[0020] Processor architecture generally comprises corresponding supporting firmware, such as firmware 15 of system 10. For example, as described further below in conjunction with the specific example of FIGURE 2, the IPF processor architecture comprises such supporting firmware as Processor Abstraction Layer (PAL), System Abstraction Layer (SAL), and Extended Firmware Interface (EFI). Such supporting firmware may enable, for example, the OS to access a particular function implemented for the processor. For instance, the OS may query the PAL as to the size of the cache implemented for the processor, etc. Other well-known functions provided by the supporting firmware (SAL, EFI) include, for example: (a) performing I/O configuration accesses to discover and program the I/O Hardware (SAL_PCI_CONFIG_READ and SAL_PCI_CONFIG_WRITE); (b) retrieving error log data from the platform following a Machine Check Abort (MCA) event (SAL_GET_STATE_INFO); (c) accessing persistent store configuration data stored in non-volatile memory (EFI variable services: GetNextVariableName, GetVariable and SetVariable); and accessing the battery-backed real-time clock/calendar (EFI GetTime and SetTime). Accordingly, the supporting firmware, such as the PAL, is implemented to provide an interface to the processor(s) for accessing the functionality provided by such processor(s). Each of those interfaces provide standard, published procedure calls that are supported. While shown as external to the lockstep processor pair 12 in this example, in certain embodiments all or a portion of firmware 15 may be implemented on a common silicon chip with processors 12A and 12B.

[0021] In the example embodiment of FIGURE 1, upon firmware 15 being invoked responsive to detection of LOL (by any of error detect logics 13A, 13B, and 13C), firmware 15 determines, in operational block 101, whether the detected LOL is a recoverable LOL. That is, firmware 15 determines in block 101 whether the detected LOL is of a type from which the firmware can recover lockstep for the lockstep processor pair 12 without crashing the system. As described further herein, lockstep is recoverable for certain detected LOLs (which may be referred to as "recoverable LOLs"), while lockstep is not recoverable for other detected LOLs (which may be referred to as "non-recoverable LOLs"). If the lockstep is not recoverable from

the detected LOL, then in the example of FIGURE 1 firmware 15 crashes the system in block 102.

[0022] As described further herein, firmware 15 is implemented in a manner that allows for recovery from certain detected errors without requiring that OS 11 be implemented with specific knowledge for handling such recovery. However, if the lockstep is determined to be recoverable, firmware 15 cooperates with OS 11 via standard OS methods to recover the lockstep. For instance, in the example embodiment of FIGURE 1, Advanced Configuration and Power Interface (ACPI) methods are used by firmware 15 to cooperate with OS 11. Accordingly, no processor or platform specific knowledge is required to be embedded in OS 11, but instead any ACPI-compatible OS may be used, including without limitation HP-UX and Open VMS operating systems.

[0023] In the example embodiment of FIGURE 1, if lockstep is determined to be recoverable in block 101, then firmware 15 triggers OS 11 to idle the master processor 12A in block 103. In this embodiment, firmware 15 utilizes an ACPI method 104 to "eject" master processor 12A, thereby triggering OS 11 to idle the master processor 12A (i.e., stop scheduling tasks for the processor). Of course, by idling master processor 12A, slave processor 12B will in turn be idled. Thus, idling master processor 12A results in idling the lockstep processor pair 12. In this example embodiment, OS 11 is not aware of the presence of slave processor 12B, but is instead aware of master processor 12A. The interface of lockstep processor pair 12 to bus 16 manages copying to slave processor 12B the instructions that are directed by OS 11 to master processor 12A. Thus, firmware 15 need not direct OS 11 to eject slave processor 12B, as OS 11 is not aware of such slave processor 12B in this example implementation. Again, by idling master processor 12A, slave processor 12B is also idled as it merely receives copies of the instructions directed to master processor 12A. Of course, if in a given implementation OS 11 is aware of slave 12B, firmware 15 may be implemented to also direct OS 11 to idle such slave processor 12B in a manner similar to that described for idling master processor 12A. An example technique that may be utilized by firmware 15 for triggering OS 11 to idle master processor 12A in accordance with certain embodiments is described further in concurrently filed and commonly assigned U.S. Patent Application Serial No. _____ [Attorney Docket No. 200404970-1] titled "SYSTEM AND METHOD FOR SYSTEM FIRMWARE CAUSING AN OPERATING SYSTEM TO IDLE A PROCESSOR", the disclosure of which is hereby incorporated herein by reference.

[0024] Firmware 15 then attempts to recover lockstep for the lockstep processor pair 12 in block 105. For instance, firmware 15 resets the processor pair 12. During such reset of processor pair 12, system 10 can continue to operate on its remaining available processors (not shown in FIGURE 1). An example technique that may be utilized by firmware 15 for recovering lockstep in accordance with certain embodiments is described further in concurrently filed and commonly assigned U.S. Patent Application Serial No. _____ [Attorney Docket No. 200404974-1] titled "SYSTEM AND METHOD FOR MAINTAINING IN A MULTI-PROCESSOR SYSTEM A SPARE PROCESSOR THAT IS IN LOCKSTEP FOR USE IN RECOVERING FROM LOSS OF LOCKSTEP FOR ANOTHER PROCESSOR", the disclosure of which is hereby incorporated herein by reference.

[0025] Once the processor pair 12 is reset and lockstep is recovered, firmware 15 reintroduces master processor 12A to OS 11 in operational block 106. In this embodiment, firmware 15 updates the ACPI device table information for master processor 12A to indicate that such master processor 12A is "present, functioning and enabled." As discussed in the ACPI 2.0 specification for the _STA status method of a device, the _STA (status) object returns the status of a device, which can be one of the following: enabled, disabled, or removed. In this respect, in the result code (bitmap) bit 0 is set if the device is present; bit 1 is set if the device is enabled and decoding its resources; bit 2 is set if the device should be shown in the UI; bit 3 is set if the device is functioning properly (cleared if the device failed its diagnostics); bit 4 is set if the battery is present; and bits 5-31 are reserved. A device can only decode its hardware resources if both bits 0 and 1 are set. If the device is not present (bit 0 cleared) or not enabled (bit 1 cleared), then the device must not decode its resources. Bits 0, 1 and 3 are the "present, enabled and functioning" bits mentioned above. Firmware 15 utilizes an ACPI method 107 to trigger OS 11 to "check for" master processor 12A, thereby reintroducing the master processor 12A to OS 11. As a result of checking for master processor 12A, OS 11 will recognize that such master processor 12A is again available and will thus begin scheduling tasks for master processor 12A once again. An example technique that may be utilized by firmware 15 for reintroducing a processor to the OS after recovery of lockstep in accordance with certain embodiments is described further in concurrently filed and commonly assigned U.S. Patent Application Serial No. _____ [Attorney Docket No. 200404972-1] titled "SYSTEM AND METHOD FOR REINTRODUCING A PROCESSOR MODULE TO AN OPERATING SYSTEM AFTER LOCKSTEP RECOVERY", the disclosure of which is hereby incorporated herein by reference.

[0026] FIGURE 2 shows a block diagram of one embodiment of the above system 10, which is implemented for the IPF processor architecture and is labeled as system 10_A. The quintessential model of the traditional IPF architecture is given in the Intel IA-64 Architecture Software Developer's Manual, Volume 2: IA-64 System Architecture, in section 11.1 *Firmware Model*, the disclosure of which is hereby incorporated herein by reference. Accordingly, in this example embodiment of system 10_A, firmware 15, labeled as firmware 15_A, includes processor abstraction layer (PAL) 201 and platform/system abstraction layer (SAL) 202. In general, PAL 201 is firmware provided by Intel for its processors, and SAL 202 is developed by an original equipment manufacturer (OEM) for the specific system/platform in which the processors are to be employed. PAL 201, SAL 202, as well as an extended firmware interface (EFI) layer (not shown), together provide, among other things, the processor and system initialization for an OS boot in an IPF system.

[0027] The boot-up process of a traditional IPF system, for example, proceeds as follows: When the system is first powered on, there are some sanity checks (e.g., power on self-test) that are performed by microprocessors included in the system platform, which are not the main system processors that run applications. After those checks have passed, power and clocks are given to a boot processor (which may, for example, be master processor 12A). The boot processor begins executing code out of the system's Read-Only Memory (ROM) (not specifically shown in FIGURE 2). The code that executes is the PAL 201, which gets control of system 10. PAL 201 executes to acquire all of the processors in system 10_A (recall that there may be many lockstep processor pairs 12) such that the processors begin executing concurrently through the same firmware.

[0028] After it has performed its duty of initializing the processor(s), PAL 201 passes control of system 10_A to SAL 202. It is the responsibility of SAL 202 to discover what hardware is present on the system platform, and initialize it to make it available for the OS 11. When main memory is initialized and functional, the firmware 15_A is copied into the main memory. Then, control is passed to EFI (not shown), which is responsible for activating boot devices, which typically includes the disk. The EFI reads the disk to load a program into memory, typically referred to as an operating system loader. The EFI loads the OS loader into memory, and then passes it control of system 10_A by branching the boot processor into the entry point of such OS loader program.

[0029] The OS loader program then uses the standard firmware interfaces to discover and initialize system 10_A further for control. One of the things that the OS loader typically has to do in a multi-processor system is to retrieve control of the other processors (those processors other than the boot processor). For instance, at this point in a multi-processor system, the other processors may be executing in do-nothing loops. In an ACPI-compatible system, OS 11 makes ACPI calls to parse the ACPI tables to discover the other processors of a multi-processor system in a manner as is well-known in the art. Then OS 11 uses the firmware interfaces to cause those discovered processors to branch into the operating system code. At that point, OS 11 controls all of the processors and the firmware 15_A is no longer in control of system 10_A.

[0030] As OS 11 is initializing, it has to discover from the firmware 15_A what hardware is present at boot time. And in the ACPI standards, it also discovers what hardware is present or added or removed at run-time. Further, the supporting firmware (PAL, SAL, and EFI) are also used during system runtime to support the processor. For example, OS 11 may access a particular function of master processor 12A via the supporting firmware 15_A, such as querying PAL 201 for the number, size, etc., of the processor's cache 14A. Some other well-known firmware functions that OS 11 may employ during runtime include: (a) PAL 201 may be invoked to configure or change processor features such as disabling transaction queuing (PAL_BUS_SET_FEATURES); (b) PAL 201 may be invoked to flush processor caches (PAL_CACHE_FLUSH); (c) SAL 202 may be invoked to retrieve error logs following a system error (SAL_GET_STATE_INFO, SAL_CLEAR_STATE_INFO); (d) SAL 202 may be invoked as part of hot-plug sequences in which new I/O cards are installed into the hardware (SAL_PCI_CONFIG_READ, SAL_PCI_CONFIG_WRIT); (e) EFI may be invoked to change the boot device path for the next time the system reboots (SetVariable); (f) EFI may be invoked to change the clock/calendar hardware settings; and (g) EFI may be invoked to shutdown the system (ResetSystem).

[0031] A "device tree" is provided, which is shown as device tree 203 in this example. Device tree 203 is stored in SRAM (Scratch RAM) on the cell, which is RAM that is reinitialized. Firmware 15A builds the device tree 203 as it discovers what hardware is installed in the system. Firmware then converts this information to the ACPI tables format and presents it to OS 11 so that OS 11 can know what is installed in the system. The ACPI device tables (not shown) are only consumed by OS 11 at boot time, so they are never updated as things change.

For OS 11 to find the current status, it calls an ACPI "method" to discover the "current status". The _STA method described above is an example of such an ACPI method. When _STA is called, the AML can look for properties on the device specified in the firmware device tree and convert that into the Result Code bitmap described above. So, if lockstep has been lost on a processor, firmware 15A will set the device tree property that indicates loss of lockstep, then when OS 11 calls _STA for that device, the "lockstep lost" property directs the AML code to return to "0" in the "functioning properly" bit so that OS 11 can know there is a problem with that processor.

[0032] If a lost lockstep is recovered in accordance with the recovery technique described herein, firmware 15A can indicate that lockstep has been recovered in the device tree 203. Then when _STA is called on that device responsive to the OS receiving the "check for device" ACPI method, the present, enabled and functioning bits will all be set and OS 11 will know the CPU is safe to use. A simple example of device tree 203 is shown below in Table 1:

Device	Status	Lockstep Enabled
Processor A	Present, Enabled, and Functioning	Yes

Table 1

[0033] Example interactions between the PAL 201, SAL 202, and device tree 203 for responding to a detected LOL (e.g., determining it is recoverable and if so then recovering from such LOL) for an IPF system in accordance with certain embodiments are described further herein (e.g., in conjunction with FIGURE 5 below), as well as in the co-pending U.S. Patent Applications incorporated by reference herein.

[0034] In certain embodiments, a different recovery technique is employed when LOL is detected for the system's boot processor than is employed for other processors of the system. For various reasons, in certain system architectures problems arise in attempting to idle (or eject) the boot processor from the system. Thus, in certain embodiments, a hot spare processor is used for recovering from LOL for the system's boot processor. More specifically, upon LOL being detected for a boot processor, a hot spare processor (i.e., an idling processor that is available in the system) is transferred the role of boot processor, and then the old boot processor having LOL is reset to reestablish its lockstep. Turning to FIGURE 3, an example system 30 is shown in which firmware utilizes this hot spare technique for recovering from LOL

for a boot processor. As with system 10 of FIGURE 1, system 30 includes OS 11, bus 16, and lockstep processor pair 12 with its error detect logic 13A-13C. System 30 further includes a second lockstep processor pair 31 that is communicatively coupled to bus 16. Lockstep processor pair 31 includes master processor 31A and slave processor 31B. Master processor 31A includes cache 32A, and slave processor 31B includes cache 32B. As with error detect logic 13A-13C implemented for lockstep processor pair 12, lockstep processor pair 31 has error detect logic 33A-33C.

[0035] Suppose that during the system boot-up procedure, master processor 12A assumes the role of boot processor. In this example embodiment, lockstep processor pair 31 may be held as a hot spare for recovering from a LOL that may be detected for the boot processor 12A. Of course, additional lockstep processor pairs may be included in system 30 (not specifically shown in the example of FIGURE 3), and those additional lockstep processor pairs, which are not the system boot processor, may recover from LOL in the manner described above with FIGURE 1. Thus, hot spare processor pair 31 is not needed for recovering from LOL detected for any non-boot processor, but may instead be used only for recovery of LOL for the boot processor (processor 12A in this example).

[0036] Firmware 35 is included in this example, and upon detection of LOL by any of error detect logics 13A-13C, it determines whether the lockstep is recoverable in block 101 (as described with FIGURE 1 above). If not, firmware 35 crashes the system in block 102 in this example embodiment. If the lockstep is recoverable, then operation advances to block 301 whereat the firmware determines whether the processor for which the LOL was detected is the system's boot processor. Because the LOL is detected for the lockstep processor pair 12 in this example, firmware 35 determines whether master processor 12A is the system's boot processor. This can be determined, for example, by accessing the device tree 203 of FIGURE 2, as such device tree includes a field for each processor indicating whether such processor is the system's boot processor. This field in the device tree may be set by the firmware during the boot-up process to identify the corresponding processor that is used as the system's boot processor. If determined in block 301 that the master processor 12A is not the system's boot processor, then operation advances to block 103, and the lockstep recovery process proceeds in the manner described above with FIGURE 1.

[0037] However, if determined in block 301 that the master processor 12A is the system's boot processor, operation advances to block 302 whereat the state of the "good"

processor in the lockstep processor pair 12 is copied over to each of processors 31A and 31B in the spare lockstep processor pair 31. Example techniques that may be utilized by firmware 35 for switching the state of a "good" processor in the lockstep processor pair 12 in accordance with certain embodiments is described further in co-pending U.S. Patent Application Serial No. 10/187,833 (published as publication no. US 2004/0006722 A1) filed July 3, 2002 and titled "METHOD AND APPARATUS FOR RECOVERY FROM LOSS OF LOCK STEP" and in concurrently filed and commonly assigned U.S. Patent Application Serial No. _____ [Attorney Docket No. 200404973-1] titled "SYSTEM AND METHOD FOR SWITCHING THE ROLE OF BOOT PROCESSOR TO A SPARE PROCESSOR RESPONSIVE TO DETECTION OF LOSS OF LOCKSTEP IN A BOOT PROCESSOR", the disclosures of which are each hereby incorporated herein by reference.

[0038] Thus, operational block 302 essentially makes the spare processor pair 31 the system's boot processor, and then in block 303 firmware 35 resets the lockstep processor pair 12 and reestablishes its lockstep. Once lockstep is reestablished for lockstep processor pair 12, that pair is held in operational block 304 as a hot spare for the new boot processor pair 31. That is, firmware 35 updates the device tree 203 of FIGURE 2 to reflect that lockstep processor pair 12 is a hot spare for the boot processor pair 31. Thus, should a recoverable LOL be detected for the new boot processor 31, the above process may be used by firmware 35 to make the spare lockstep processor pair 12 the boot processor and then recover lockstep for pair 31. An example technique for resetting the lockstep processor pair 12 and reestablishing its lockstep in which the lockstep processor pair 12 is then held as a hot spare is described further in concurrently filed and commonly assigned U.S. Patent Application Serial No. _____ [Attorney Docket No. 200404974-1] titled "SYSTEM AND METHOD FOR MAINTAINING IN A MULTI-PROCESSOR SYSTEM A SPARE PROCESSOR THAT IS IN LOCKSTEP FOR USE IN RECOVERING FROM LOSS OF LOCKSTEP FOR ANOTHER PROCESSOR", the disclosure of which is hereby incorporated herein by reference.

[0039] One example system in which firmware 35 of FIGURE 3 may be employed is shown in FIGURE 4. FIGURE 4 shows system 40 that includes multi-processor cells A-D, labeled 41_A-41_D, respectively. Cell A 41_A is shown in more detail, and should be understood that cells B-D 41_B-41_D have substantially the same architecture as that of cell A 41_A in this example. The architecture of cell A 41_A described hereafter corresponds to that of Hewlett-Packard's Superdome™ systems. As shown, multi-processor cell A 41_A includes coherency controller 404

that is communicatively coupled to two buses, labeled 405 and 406, respectively. A plurality of processors are included within cell A 41_A, shown as CPU 0, CPU 1, CPU 2 and CPU 3 (and labeled 400-403, respectively). More particularly, a plurality of processors are communicatively coupled to each of the buses 405 and 406. In this example, CPU 0 (400) and CPU 1 (401) are each communicatively coupled to the first bus 405, and CPU 2 (402) and CPU 3 (403) are each communicatively coupled to the second bus 406. It should be understood that each of CPU 0 (400), CPU 1 (401), CPU 2 (402), and CPU 3 (403) may in actuality be a lockstep processor pair, such as the lockstep processor pair 12 of FIGURES 1-3. Thus, for instance, CPU 0 (400) includes both a master processor and a slave processor, as with processors 12A and 12B included in the lockstep processor pair 12 of FIGURES 1-3.

[0040] Coherency controller 404 decodes the address an interrupt is targeted towards and determines which bus (405 or 406) the interrupt packet should be delivered to. Each CPU on the destination bus sees the interrupt and compares the interrupt target address with its internal "LID" register to determine if it is the targeted CPU. If the match is correct, the CPU responds to the interrupt. If the match is not correct, the CPU ignores the interrupt packet.

[0041] As shown, the example firmware 35 described above with FIGURE 3 may be employed to manage the recovery from detected LOLs for the processors of cells A-D (41_A-41_D). In this example architecture, when designating a hot spare for the boot processor, such hot spare is selected to be another processor communicatively coupled to the same bus as the boot processor. For instance, suppose that during the boot-up of system 40, CPU 2 (402) is designated as the boot processor. Accordingly, firmware 35 will identify another processor that is communicatively coupled to bus 406 to designate as a hot spare for such boot processor, such as CPU 3 (403). During runtime if a LOL is detected for CPU 2 (402), then firmware 35 operates according to the process described above in FIGURE 3 to switch the designation of boot processor to the hot spare, CPU 3 (403). In performing this switch the LID register of the CPU that lost lockstep is copied into the LID register of the Hot-Spare CPU and the Hot-Spare CPU pair will then assume the ID of the failed CPU and start responding to interrupts directed to that ID. The LID of the failed CPU is quickly re-written to a different value so that it will no longer respond to interrupts directed to that ID. CPU 2 (402) can then be reset to recover its lockstep, and such CPU 2 (402) may then be held as a hot spare for the new boot processor CPU 3 (403).

[0042] It should be recognized that in the example system of FIGURE 4, if a hot spare were used for recovering from LOL for all processors, rather than just for the boot

processor, much of the potential processing resources would be required to be held as spare resources. For instance, a hot spare would be required on each of the buses of each cell. Because there are two processors coupled to each bus in this example (i.e., CPU 0 and CPU 1 coupled to bus 405, and CPU 2 and CPU 3 coupled to bus 406), reserving a hot spare processor for each bus would result in holding half of the total processing resources in spare. This is an undesirably expensive and wasteful solution. Thus, according to the illustrated embodiment, only a hot spare processor is reserved for the boot processor. Thus, continuing with the above example in which CPU 2 is the boot processor and CPU 3 is held in idle as a hot spare, both of CPU 0 and CPU 1 are active (i.e., neither are held in spare). Further, none of the processors of cells B-D need to be held as hot spares. In the event of a recoverable LOL occurring for any of non-boot processors of the cells, the lockstep recovery process of FIGURE 1 (i.e., operational blocks 103-106) can be utilized without requiring a hot spare for lockstep recovery for those non-boot processors.

[0043] While in the above example embodiment, a hot spare CPU is maintained for recovery from LOL for the system's boot processor, in an alternative embodiment a hot spare need not be held as such, but rather a processor can be dynamically made a "spare" when needed for recovery from LOL encountered for the system boot processor. That is, assuming as in the above example of FIGURE 4 that CPU 2 is the system's boot processor, CPU 3 does not have to be held as a hot spare for CPU 2, but instead CPU 3 can be idled and made a "spare" upon detection of LOL in CPU 2. Thus, the resource of this spare CPU need not be wasted during normal runtime, but can be dynamically turned into a spare processor that is available for recovering from LOL encountered on CPU 2 in the manner described above. As an example of this embodiment, the firmware may send an "eject request" on a healthy processor pair (e.g., CPU 3), and lie to the OS by indicating (e.g., in response to an ACPI _STA method for the healthy processor pair) that such processor pair is not functioning. This would cause the OS to eject that processor pair as though it had encountered a LOL. This processor would become the "hot spare" and be used to replace the boot processor. The system boot processor role would be assumed by the idled healthy processor pair, just as described above in the example of FIGURE 4 in which the healthy CPU 3 is held idle for the system boot processor, CPU 2. The only difference being that now the firmware had to take some initial action to turn the healthy processor pair into a "hot spare" by idling it and making it appear to the OS as though it was not functioning. Thus, the LIDs would be swapped. That is, the LID register of the boot processor that lost lockstep is copied into the LID register of the now spare processor pair (CPU 3 in this

example), and the LID register of this spare processor pair would be copied into the LID register of the original boot processor. Lockstep is then reestablished on the original boot processor, and it can be reintroduced to the OS with the ID of the original non-boot processor that replaced it as the system boot processor.

[0044] Turning now to FIGURE 5, an operational flow diagram for one embodiment is shown. In operational block 501, the system is powered on. In operational block 502, the system's firmware establishes a hot spare for the system's boot processor. For instance, in the example system 40 of FIGURE 4, if CPU 2 (402) is designated as the boot processor, the firmware 35 identifies a processor on the same bus as the boot processor, such as CPU 3 (403), as a hot spare, and firmware 35 updates the device tree to designate that such CPU 3 (403) is a hot spare for the boot processor CPU 2 (402). An example technique that may be utilized by firmware 35 for establishing a hot spare for the boot processor in accordance with certain embodiments is described further in concurrently filed and commonly assigned U.S. Patent Application Serial No. _____ [Attorney Docket No. 200404944-1] titled "SYSTEM AND METHOD FOR ESTABLISHING A SPARE PROCESSOR FOR RECOVERING FROM LOSS OF LOCKSTEP IN A BOOT PROCESSOR", the disclosure of which is hereby incorporated herein by reference.

[0045] In operational block 503, the firmware establishes lockstep mode on the appropriate processor modules (or lockstep processor pairs). As described further in concurrently filed and commonly assigned U.S. Patent Application Serial No. _____ [Attorney Docket No. 200404943-1] titled "SYSTEM AND METHOD FOR CONFIGURING LOCKSTEP MODE OF A PROCESSOR MODULE", the disclosure of which is hereby incorporated herein by reference, in certain embodiments whether lockstep is activated for the system (or for any given partition of a system) is configurable by a system administrator. Thus, rather than the processors of a system being fixed in either lockstep mode or not in lockstep mode, certain embodiments permit lockstep mode to be activated and deactivated for a system as may be desired by a system administrator. In the event that lockstep mode is not activated for the system, then the processors that would have been used as slave processors in lockstep mode are available to be used as "master" processors for processing instructions, thus increasing the total amount of computing resources available to the OS. If for example, having a greater number of processors available for computing separate instructions is more desirable than guarding fully against SDC on a given partition of a customer's system, then lockstep processing

may be disabled for such partition, and lockstep processing may be enabled for those partitions in which fully guarding against SDC is of more importance.

[0046] In operational block 504, the boot process boots the system OS and completes with the firmware passing control of the system over to the OS. During system runtime, if the system is operating in lockstep mode, then error detect logic present in the system (such as error detect logic 13A-13C of FIGURE 1) monitors for LOL. Thus, block 505 represents the continuous monitoring by the error detect logic of their respective processors for LOL. If an LOL is detected by the error logic, then the firmware is notified of the detected LOL in block 506. An example technique that may be utilized for notifying the firmware of the detected LOL in accordance with certain embodiments is described further in concurrently filed and commonly assigned U.S. Patent Application Serial No. _____ [Attorney Docket No. 200404946-1] titled "SYSTEM AND METHOD FOR USING INFORMATION RELATING TO A DETECTED LOSS OF LOCKSTEP FOR DETERMINING A RESPONSIVE ACTION", the disclosure of which is hereby incorporated herein by reference. As mentioned above, the firmware determines whether the detected LOL is recoverable. If determined that the LOL is recoverable, then operation continues in the firmware for recovering the LOL in the manner described hereafter.

[0047] In block 507, the firmware determines whether the processor for which the LOL is detected is the system's boot processor. This determination may be made by searching for the processor for which the LOL is detected in the device tree (e.g., tree 203 of FIGURE 2) and evaluating the fields associated with such processor in the device tree to determine whether the device tree identifies such processor as the boot processor.

[0048] If the processor for which LOL is detected is not the system boot processor, then operation advances to block 508 whereat the processor for which the LOL is detected is idled, and actions are taken to reestablish its lockstep. As described above, an ACPI "eject" method may be used to instruct the system's OS to idle the processor, such as described more fully in concurrently filed and commonly assigned U.S. Patent Application Serial No. _____ [Attorney Docket No. 200404971-1] titled "SYSTEM AND METHOD FOR REESTABLISHING LOCKSTEP FOR A PROCESSOR MODULE FOR WHICH LOSS OF LOCKSTEP IS DETECTED", the disclosure of which is hereby incorporated herein by reference. In order to reestablish lockstep, the processor may be reset. At the end of this step,

the processor is executing in firmware space and lockstep has been reestablished for the processor.

[0049] The processor is then ready to be introduced back to the OS. Thus, in block 509, the firmware reintroduces to the OS the processor having its lockstep recovered. An example technique that may be utilized for reintroducing the processor back to the OS in block 509 in accordance with certain embodiments is described further in concurrently filed and commonly assigned U.S. Patent Application Serial No. _____ [Attorney Docket No. 200404972-1] titled "SYSTEM AND METHOD FOR REINTRODUCING A PROCESSOR MODULE TO AN OPERATING SYSTEM AFTER LOCKSTEP RECOVERY", the disclosure of which is hereby incorporated herein by reference. Operation then continues in block 510, wherein the processor whose lockstep was recovered is available to run tasks as scheduled by the OS and the system's processors are monitored for another LOL in block 505. That is, in block 510 the system is back to a stable state with full lockstep protection again being provided.

[0050] Unfortunately, as mentioned above, in certain systems the system boot processor that initialized the OS during the systems boot-up process cannot easily be idled and returned to firmware control. Thus, a different technique than that described above for non-boot processors is employed in this embodiment. Accordingly, if determined in block 507 that the LOL is detected for the system's boot processor, operation advances to block 511 whereat the state of the "good" boot processor is copied to the hot spare that was established for the boot processor in block 502. As mentioned above, example techniques that may be utilized by the firmware for switching the state of a "good" processor in the lockstep processor pair that is the system boot processor in accordance with certain embodiments is described further in co-pending U.S. Patent Application Serial No. 10/187,833 (published with publication no. US 2004/0006722 A1) filed July 3, 2002 and titled "METHOD AND APPARATUS FOR RECOVERY FROM LOSS OF LOCK STEP" and in concurrently filed and commonly assigned U.S. Patent Application Serial No. _____ [Attorney Docket No. 200404973-1] titled "SYSTEM AND METHOD FOR SWITCHING THE ROLE OF BOOT PROCESSOR TO A SPARE PROCESSOR RESPONSIVE TO DETECTION OF LOSS OF LOCKSTEP IN A BOOT PROCESSOR", the disclosures of which are each hereby incorporated herein by reference.

[0051] In operational block 512, the firmware reestablishes lockstep on the processor for which the LOL was detected (e.g., by resetting the processor), and the firmware

establishes the processor having recovered lockstep as the hot spare for the new boot processor. Such processor whose lockstep has been recovered may be established as a spare for the new boot processor in the manner described above in block 502, and as discussed further in concurrently filed and commonly assigned U.S. Patent Application Serial No. _____ [Attorney Docket No. 200404944-1] titled "SYSTEM AND METHOD FOR ESTABLISHING A SPARE PROCESSOR FOR RECOVERING FROM LOSS OF LOCKSTEP IN A BOOT PROCESSOR", the disclosure of which is hereby incorporated herein by reference. Operation of the system continues in block 513 wherein the processors are monitored for another LOL in block 505. In block 513 the system is back to a stable state with full lockstep protection again being provided.

[0052] In certain embodiments, if the lockstep cannot be recovered in operational block 508 (e.g., the processor fails its self-test when being reset), then that processor is simply not reintroduced back to the OS in block 509. A message can be generated for the system administrator to provide notice of the loss of this processor, and if desired the system administrator can schedule an orderly shutdown and service of the system (e.g., for replacing the processor). Similarly, if the lockstep cannot be recovered in operational block 512 (e.g., the processor fails its self-test when being reset), then a message can be generated for the system administrator to provide notice of the loss of this processor (as thus loss of lockstep recovery protection for the boot processor). In other words, if the lockstep cannot be reestablished in block 512, then if a LOL occurs in the new boot processor there will not be a spare processor for taking over its role (and thus the system may crash). If desired, the system administrator can schedule an orderly shutdown and re-boot in order to establish a new boot processor that has a hot spare available and/or schedule service of the system (e.g., for replacing the failed processor).

[0053] While a detailed flow diagram of one embodiment is shown in FIGURE 5, embodiments hereof are not limited to that example operational flow. For instance, a more general operational flow according to one embodiment is shown in FIGURE 6. In FIGURE 6, LOL for a pair of processors is detected in operational block 61. In block 62, firmware triggers an OS to idle the processors for which the LOL was detected. In block 63, the firmware recovers lockstep between the pair of processors. In block 64, after lockstep is recovered between the pair of processors, the firmware triggers the OS to recognize the processors as again being available

for receiving instructions. As described above, the above technique may be modified for recovering from LOL for the boot processor in certain systems.

CLAIMS

What is claimed is:

1. A method comprising:

detecting loss of lockstep for a lockstep pair of processors; and

using firmware to trigger an operating system to idle the lockstep pair of processors, recover lockstep for the lockstep pair of processors, and trigger the operating system to recognize the lockstep pair of processors having recovered lockstep.

2. The method of claim 1 wherein said using firmware to trigger an operating system to idle the lockstep pair of processors further comprises:

using the firmware to trigger the operating system to idle a master processor of the lockstep pair of processors.

3. The method of claim 2 wherein said using firmware to trigger the operating system to recognize the lockstep pair of processors having recovered lockstep further comprises:

using the firmware to trigger the operating system to recognize the master of the lockstep pair of processors.

4. The method of claim 1 wherein said detecting loss of lockstep comprises:

detecting corrupt data in one of said lockstep pair of processors that would lead to a lockstep mismatch if acted upon.

5. The method of claim 1 wherein said detecting loss of lockstep comprises:

detecting a precursor to lockstep mismatch.

6. The method of claim 1 wherein said detecting loss of lockstep comprises:

detecting lockstep mismatch between the lockstep pair of processors.

7. The method of claim 1 further comprising:

responsive to said detecting loss of lockstep, using said firmware to determine if lockstep is recoverable for the lockstep pair of processors.

8. The method of claim 7 wherein said using said firmware to determine if lockstep is recoverable further comprises:

determining if a lockstep mismatch has occurred between the lockstep pair of processors.

9. The method of claim 8 further comprising:

if determined that a lockstep mismatch has not occurred between the lockstep pair of processors, then determining that the loss of lockstep is recoverable.

10. The method of claim 8 further comprising:

if determined that a lockstep mismatch has occurred between the lockstep pair of processors, then determining that the loss of lockstep is not recoverable.

11. The method of claim 1 further comprising:

determining if said lockstep pair of processors for which said loss of lockstep is detected comprises a system boot processor.

12. The method of claim 11 wherein if determined that said lockstep pair of processors for which said loss of lockstep is detected comprises a system boot processor, further comprising:

swapping the role of system boot processor to another processor in the system.

13. The method of claim 12 further comprising:

after said swapping, recovering the lockstep for the lockstep pair of processors.

14. The method of claim 13 further comprising:

after recovering lockstep for the lockstep pair of processors, holding the recovered pair of processors in idle as a spare for the processor to which the role of system boot processor was swapped.

15. A system comprising:

an Advanced Configuration and Power Interface (ACPI)-compatible operating system;

master processor operable to process instructions scheduled by said ACPI-compatible operating system;

slave processor lockstepped with the master processor operable to perform redundant processing of said instructions scheduled for the master processor; and

firmware operable, responsive to detection of loss of lockstep between the master and slave processors, to use an ACPI method to trigger the operating system to idle the master processor, attempt to recover lockstep between the master and slave processors, and if recovery of lockstep is successful then use an ACPI method to reintroduce the master processor to the operating system.

16. The system of claim 15 further comprising:

error detection logic for detecting loss of lockstep between the master and slave processors.

17. The system of claim 15 further comprising:

error detection logic for detecting a precursor to loss of lockstep.

18. The system of claim 17 wherein said precursor to loss of lockstep is treated as said detection of loss of lockstep.

19. The system of claim 17 wherein said error detection logic comprises a parity-based mechanism.

20. The system of claim 15 further comprising error detection logic for detecting lockstep mismatch between the master and slave processors.

21. A system comprising firmware that includes computer-executable software code stored to a computer-readable medium, the computer-executable software code comprising:

code, responsive to detection of loss of lockstep between a pair of lockstep processors, for determining if the lockstep is recoverable for the pair of lockstep processors; and

code, responsive to determining that the lockstep is recoverable, for triggering an operating system to idle the processors, attempting to recover lockstep between the pair of processors, and if lockstep is successfully recovered between the pair of processors, triggering said operating system to recognize the processors as being available for receiving instructions.

22. The system of claim 21 wherein the code for attempting to recover lockstep further comprises:

code for resetting the pair of processors.

23. The system of claim 21 wherein the code for determining if the lockstep is recoverable further comprises:

code for determining if lockstep mismatch occurred between the pair of lockstep processors.

24. The system of claim 21 wherein said operating system is an Advanced Configuration and Power Interface (ACPI)-compatible operating system, said code for triggering the operating system to idle the processors comprises:

code for using an ACPI method to idle the processors.

25. The system of claim 21 wherein said operating system is an Advanced Configuration and Power Interface (ACPI)-compatible operating system, said code for triggering said operating system to recognize the processors as being available for receiving instructions comprises:

code for using an ACPI method to cause the operating system to check for the processors.

26. A method comprising:

establishing, in a multi-processor system, a hot spare processor for a system boot processor;

detecting loss of lockstep for a lockstep pair of processors in said multi-processor system;

determining if said lockstep pair of processors for which the loss of lockstep is detected is the system boot processor;

if determined that said lockstep pair of processors for which the loss of lockstep is the system boot processor, copying a state of the system boot processor to the hot spare processor; and

if determined that said lockstep pair of processors for which the loss of lockstep is not the system boot processor, then triggering an operating system to a) idle the lockstep pair of processors, b) attempt to recover lockstep between the lockstep pair of processors, and c) if lockstep is successfully recovered between the lockstep pair of processors, trigger said operating system to recognize the processors as being available for receiving instructions.

27. The method of claim 26 wherein if determined that said lockstep pair of processors for which the loss of lockstep is the system boot processor further comprising:

attempting to recover lockstep between the lockstep pair of processors after copying the state of the system boot processor to the hot spare processor.

28. The method of claim 27 wherein if determined that said lockstep pair of processors for which the loss of lockstep is the system boot processor further comprising:

if lockstep is successfully recovered between the lockstep pair of processors, establishing the lockstep pair of processors for which lockstep was recovered as a hot spare processor.

29. A system comprising:

means for detecting loss of lockstep between a pair of processors;

means for determining if lockstep is recoverable for the pair of processors; and

means, responsive to the determining means determining that the lockstep is recoverable for the pair of processors, for triggering an operating system to idle the processors, recovering the lockstep for the pair of processors, and reintroducing to the operating system the processors having recovered lockstep.

30. The system of claim 29 wherein the means for triggering the operating system to idle the processors uses an Advanced Configuration and Power Interface (ACPI) method for said triggering.

31. The system of claim 19 wherein the means for reintroducing uses an Advanced Configuration and Power Interface (ACPI) method for reintroducing to the operating system the processors having recovered lockstep.

32. The system of claim 29 wherein said means for detecting loss of lockstep comprises:

means for detecting a precursor to loss of lockstep.

33. The system of claim 32 wherein said means for detecting a precursor to loss of lockstep comprises a parity-based means.

34. The system of claim 29 wherein said means for detecting loss of lockstep comprises:

means for detecting a lockstep mismatch.

35. The system of claim 29 wherein said means for determining comprises:

means for determining if the detected loss of lockstep is a lockstep mismatch.

ABSTRACT

According to at least one embodiment, a method comprises detecting loss of lockstep for a pair of processors. The method further comprises triggering, by firmware, an operating system to idle the processors, and recovering, by the firmware, lockstep between the pair of processors. After lockstep is recovered between the pair of processors, the method further comprises triggering, by the firmware, the operating system to recognize the processors as being available for receiving instructions.

FIG. 1

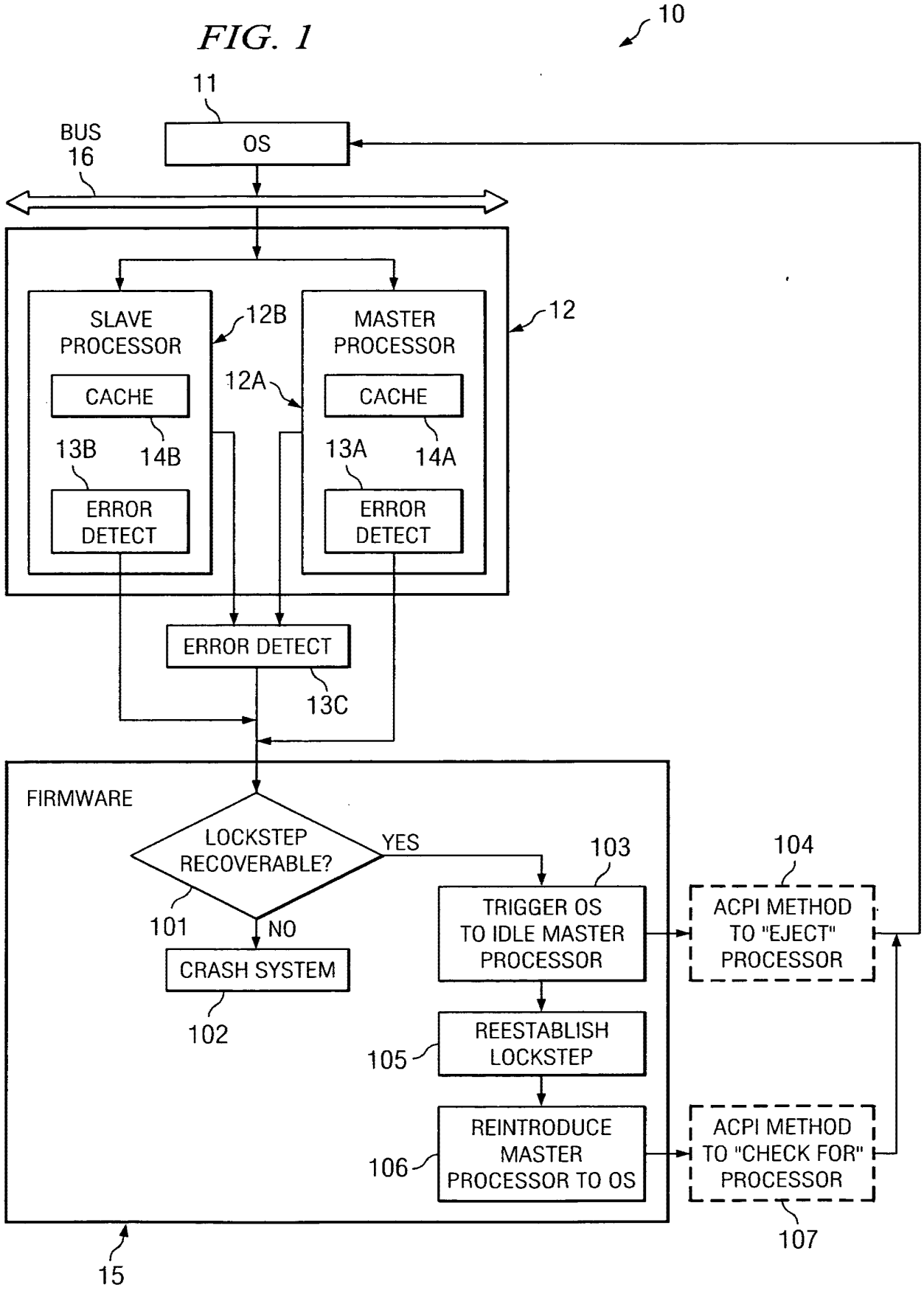

10
11
OS
BUS
16
SLAVE
PROCESSOR
12B
MASTER
PROCESSOR
12
12A
CACHE
CACHE
13B
14B
13A
14A
ERROR
DETECT
ERROR
DETECT
ERROR DETECT
13C
FIRMWARE
LOCKSTEP
RECOVERABLE?
YES
103
104
101
NO
TRIGGER OS
TO IDLE MASTER
PROCESSOR
ACPI METHOD
TO "EJECT"
PROCESSOR
CRASH SYSTEM
102
REESTABLISH
LOCKSTEP
105
REINTRODUCE
MASTER
PROCESSOR TO OS
106
ACPI METHOD
TO "CHECK FOR"
PROCESSOR
107
15

FIG. 2

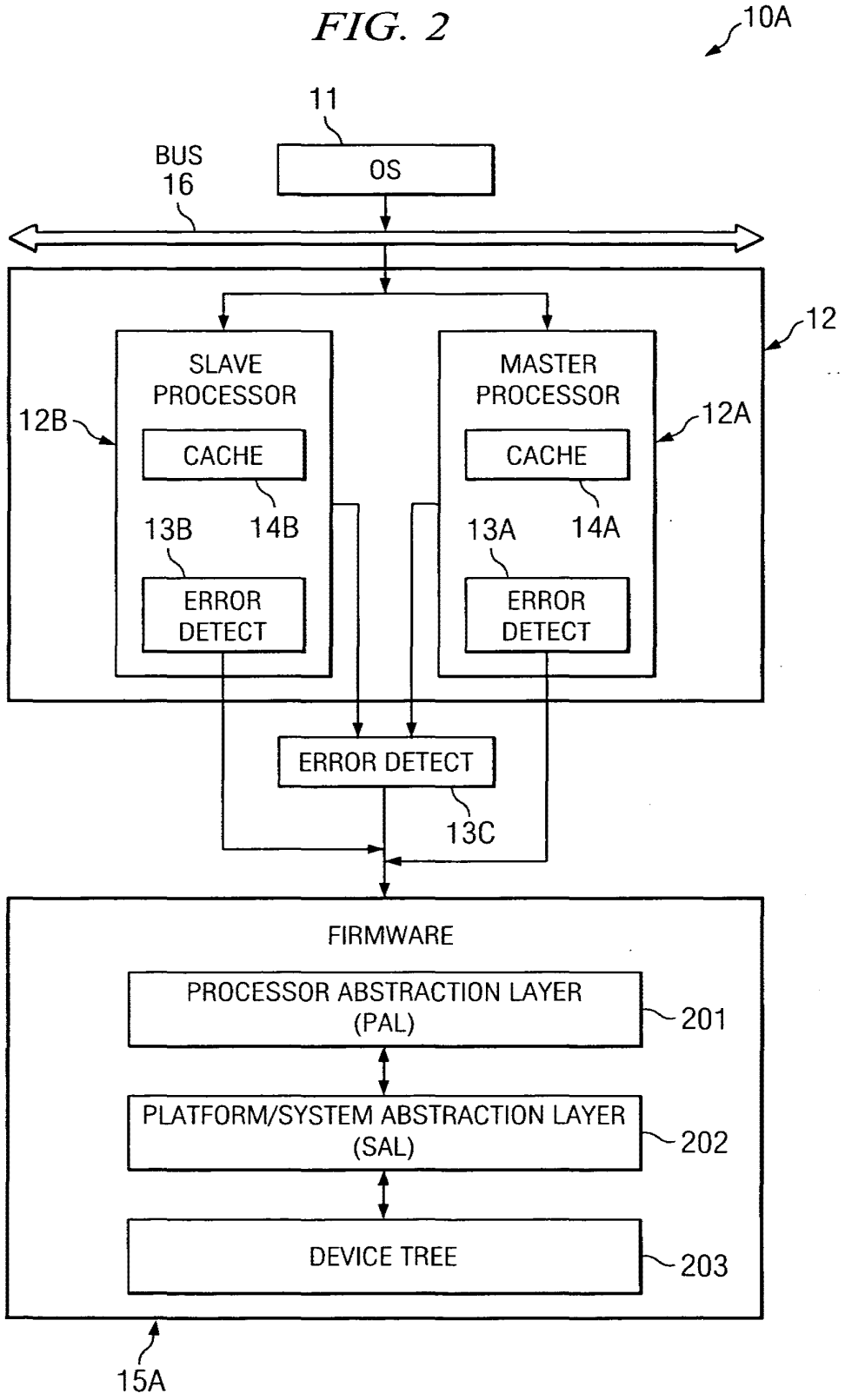

10A
11
OS
BUS
16
12
SLAVE
PROCESSOR
MASTER
PROCESSOR
12B
12A
CACHE
CACHE
13B
14B
13A
14A
ERROR
DETECT
ERROR
DETECT
ERROR DETECT
13C
FIRMWARE
PROCESSOR ABSTRACTION LAYER
(PAL)
201
PLATFORM/SYSTEM ABSTRACTION LAYER
(SAL)
202
DEVICE TREE
203
15A

FIG. 3

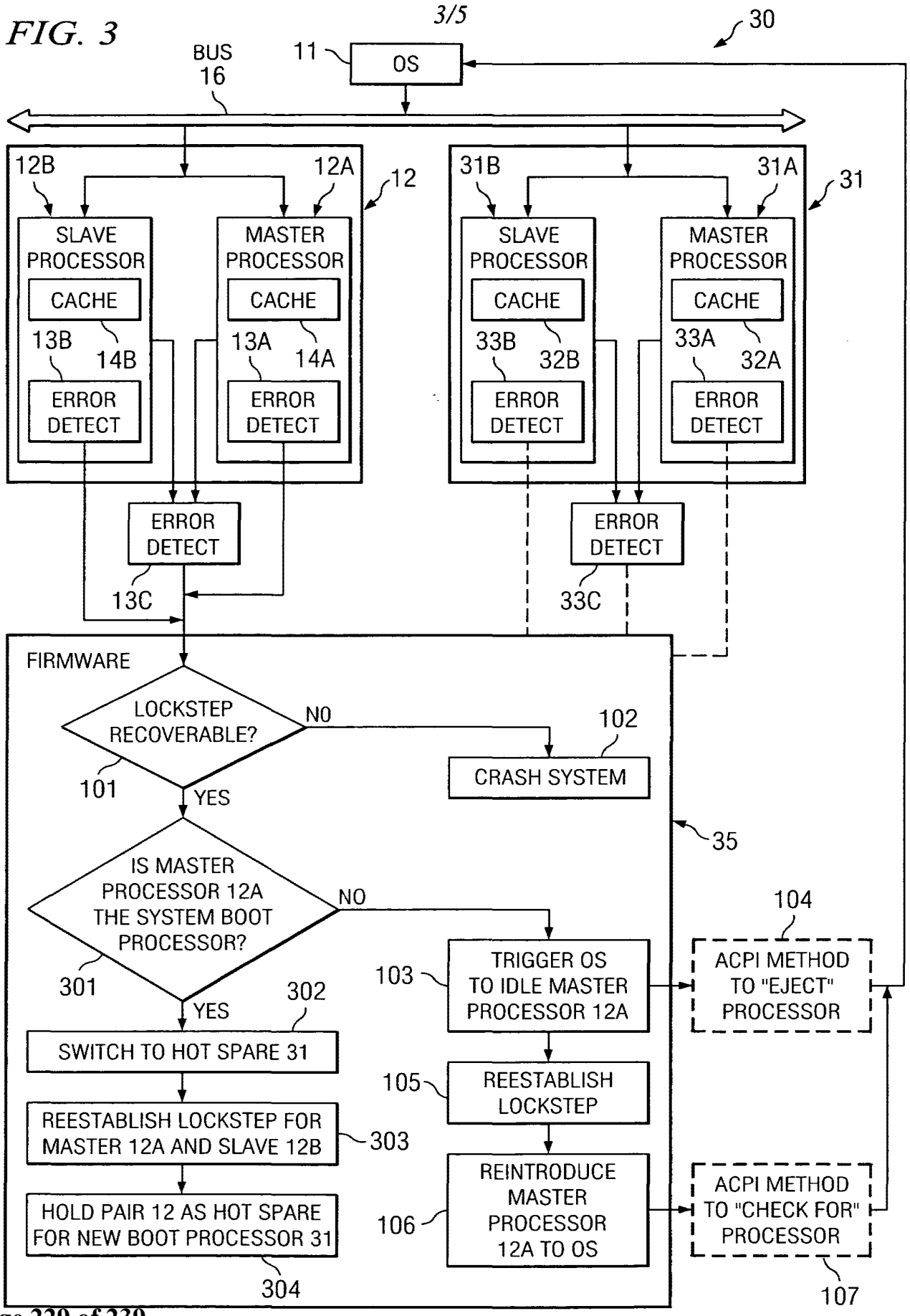

30
BUS
16
11
OS
12B
12A
12
SLAVE PROCESSOR
CACHE
13B
14B
ERROR DETECT
MASTER PROCESSOR
CACHE
13A
14A
ERROR DETECT
31B
31A
31
SLAVE PROCESSOR
CACHE
33B
32B
ERROR DETECT
MASTER PROCESSOR
CACHE
33A
32A
ERROR DETECT
ERROR DETECT
13C
ERROR DETECT
33C
FIRMWARE
LOCKSTEP RECOVERABLE?
NO
102
CRASH SYSTEM
101
YES
35
IS MASTER PROCESSOR 12A THE SYSTEM BOOT PROCESSOR?
NO
104
TRIGGER OS TO IDLE MASTER PROCESSOR 12A
103
ACPI METHOD TO "EJECT" PROCESSOR
301
YES
302
SWITCH TO HOT SPARE 31
105
REESTABLISH LOCKSTEP
REESTABLISH LOCKSTEP FOR MASTER 12A AND SLAVE 12B
303
REINTRODUCE MASTER PROCESSOR 12A TO OS
ACPI METHOD TO "CHECK FOR" PROCESSOR
HOLD PAIR 12 AS HOT SPARE FOR NEW BOOT PROCESSOR 31
106
304
107

FIG. 4

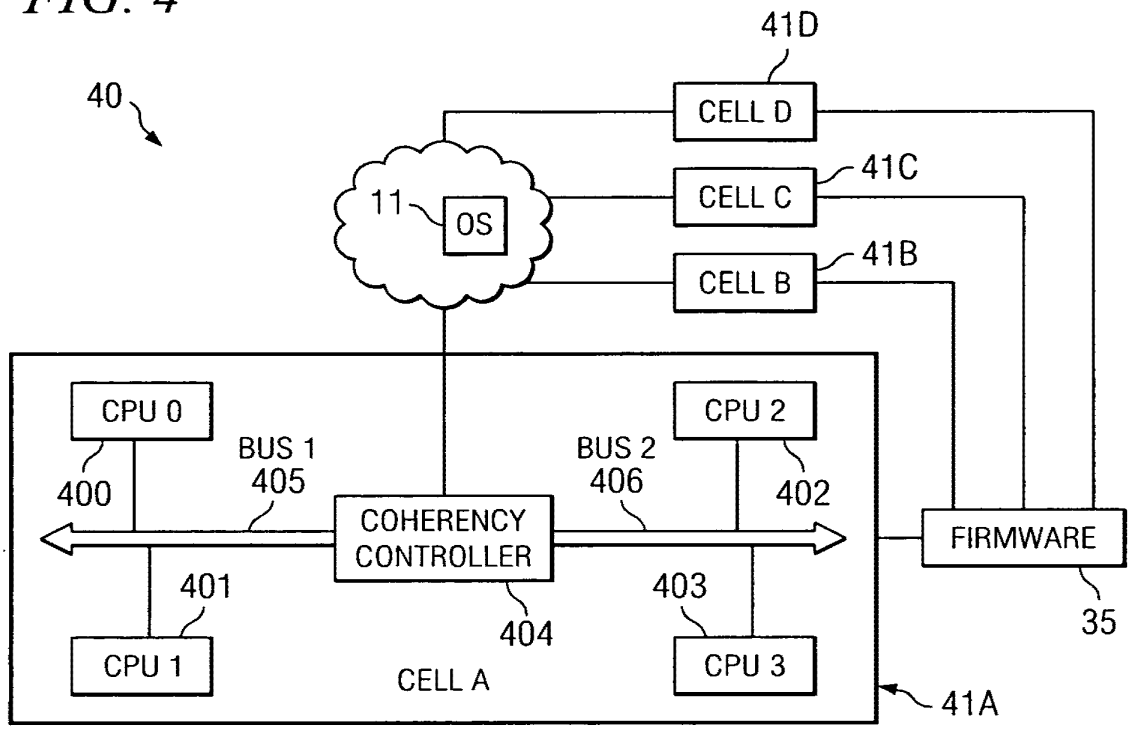

40
41D
CELL D
41C
CELL C
41B
CELL B
11
OS
CPU 0
CPU 2
BUS 1
405
BUS 2
406
400
402
COHERENCY
CONTROLLER
FIRMWARE
401
403
404
35
CPU 1
CELL A
CPU 3
41A

FIG. 6

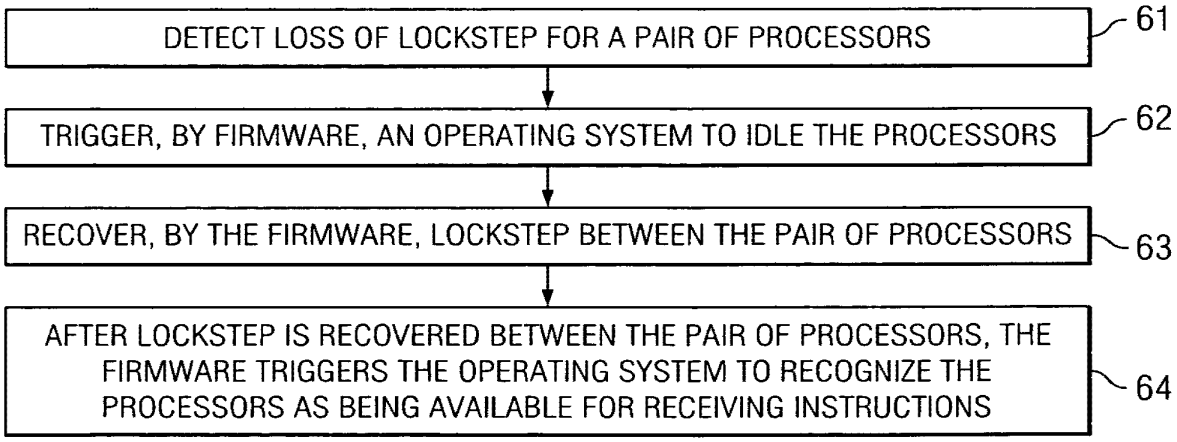
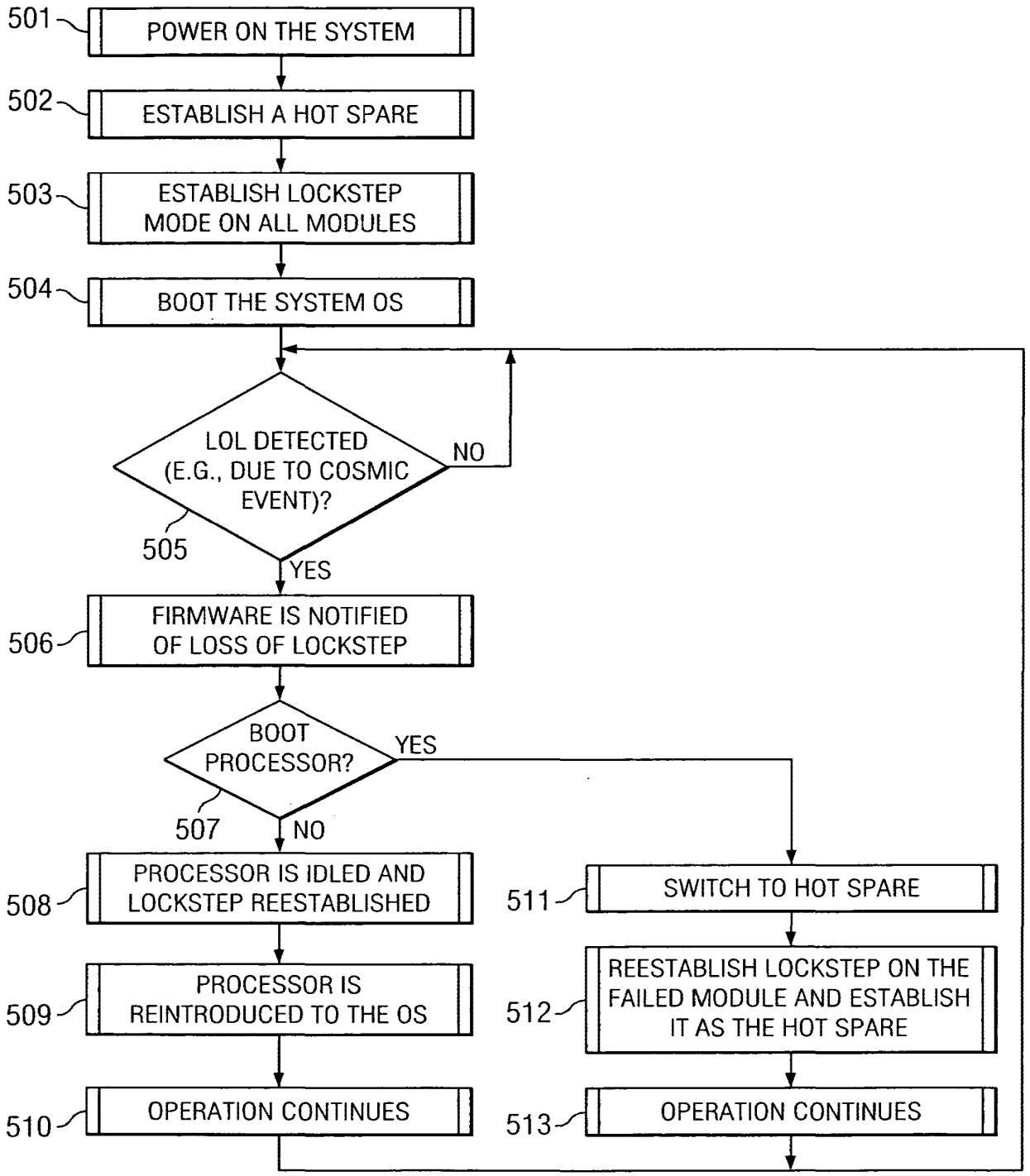

DETECT LOSS OF LOCKSTEP FOR A PAIR OF PROCESSORS
61
TRIGGER, BY FIRMWARE, AN OPERATING SYSTEM TO IDLE THE PROCESSORS
62
RECOVER, BY THE FIRMWARE, LOCKSTEP BETWEEN THE PAIR OF PROCESSORS
63
AFTER LOCKSTEP IS RECOVERED BETWEEN THE PAIR OF PROCESSORS, THE FIRMWARE TRIGGERS THE OPERATING SYSTEM TO RECOGNIZE THE PROCESSORS AS BEING AVAILABLE FOR RECEIVING INSTRUCTIONS
64

FIG. 5


501
POWER ON THE SYSTEM
502
ESTABLISH A HOT SPARE
503
ESTABLISH LOCKSTEP MODE ON ALL MODULES
504
BOOT THE SYSTEM OS
LOL DETECTED (E.G., DUE TO COSMIC EVENT)?
NO
505
YES
506
FIRMWARE IS NOTIFIED OF LOSS OF LOCKSTEP
BOOT PROCESSOR?
YES
507
NO
508
PROCESSOR IS IDLED AND LOCKSTEP REESTABLISHED
509
PROCESSOR IS REINTRODUCED TO THE OS
510
OPERATION CONTINUES
511
SWITCH TO HOT SPARE
512
REESTABLISH LOCKSTEP ON THE FAILED MODULE AND ESTABLISH IT AS THE HOT SPARE
513
OPERATION CONTINUES

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

ATTORNEY DOCKET NO. 200404941-1

As a below named inventor, I hereby declare that:

My residence/post office address and citizenship are as stated below next to my name;

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

SYSTEM AND METHOD FOR PROVIDING FIRMWARE RECOVERABLE LOCKSTEP PROTECTION

the specification of which is attached hereto unless the following box is checked:

( ) was filed on _____ as US Application No. or PCT International Application Number _____ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment(s) referred to above. I acknowledge the duty to disclose all information which is material to patentability as defined in 37 CFR 1.56.

Foreign Application(s) and/or Claim of Foreign Priority

I hereby claim foreign priority benefits under Title 35, United States Code Section 119 of any foreign application(s) for patent or inventor(s) certificate listed below and have also identified below any foreign application for patent or inventor(s) certificate having a filing date before that of the application on which priority is claimed:

COUNTRY	APPLICATION NUMBER	DATE FILED	PRIORITY CLAIMED UNDER 35 U.S.C. 119
			YES: ___ NO: ___
			YES: ___ NO: ___

Provisional Application

I hereby claim the benefit under Title 35, United States Code Section 119(e) of any United States provisional application(s) listed below:

APPLICATION NUMBER	FILING DATE

U. S. Priority Claim

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

APPLICATION NUMBER	FILING DATE	STATUS (patented/pending/abandoned)

POWER OF ATTORNEY:

As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith:

Send Correspondence to:

Customer Number 022879

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, Colorado 80527-2400

Direct Telephone Calls to:

Richard Stokey

(281) 518-3184

Even though the attorney is listed, please associate HP's Customer Number 022879 with this case.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Post Office Address: 1524 Bamburgh Drive, Plano, TX 75075

Scott L Michaelis
Inventor's Signature

10/20/2004
Date

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION (continued)

ATTORNEY DOCKET NO. 200404941-1

Full Name of # 2 joint inventor: Anurupa Rajkumari Citizenship: India

Residence: 2511 Echo Wood Place, Round Rock, TX 78681

Post Office Address: 2511 Echo Wood Place, Round Rock, TX 78681

Anurupa Rajkumari 10/20/04

Inventor's Signature Date

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Residence: 4023 Sunstone Drive, Fort Collins, CO 80525

Post Office Address: 4023 Sunstone Drive, Fort Collins, CO 80525

William McHardy 10/19/04

Inventor's Signature Date

Full Name of # 4 joint inventor: Citizenship:

Residence:

Post Office Address:

Inventor's Signature Date

Full Name of # 5 joint inventor: Citizenship:

Residence:

Post Office Address:

Inventor's Signature Date

Full Name of # 6 joint inventor: Citizenship:

Residence:

Post Office Address:

Inventor's Signature Date

Full Name of # 7 joint inventor: Citizenship:

Residence:

Post Office Address:

Inventor's Signature Date

Full Name of # 8 joint inventor: Citizenship:

Residence:

Post Office Address:

Inventor's Signature Date

(Use Page Two For Additional Inventor(s) Signature(s))

PATENT APPLICATION SERIAL NO. _____

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

10/28/2004 EHAILE1 00000061 082025 10973076

01 FC:1001 790.00 DA
02 FC:1201 176.00 DA
03 FC:1202 270.00 DA

PTO-1556
(5/87)

*U.S. Government Printing Office: 2002 — 489-267/69033

PATENT APPLICATION FEE DETERMINATION RECORD
Effective October 1, 2004

Application or Docket Number: 10923076

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	35	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	35 minus 20=	* 15
INDEPENDENT CLAIMS	5 minus 3 =	* 2
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
BASIC FEE	395.00	OR	BASIC FEE	790.00
X$ 9=		OR	X$18=	270
X44=		OR	X88=	176
+150=		OR	+300=	
TOTAL		OR	TOTAL	1236

CLAIMS AS AMENDED - PART II

AMENDMENT A

	(Column 1)		(Column 2)	(Column 3)
	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDI-TIONAL FEE		RATE	ADDI-TIONAL FEE
X$ 9=		OR	X$18=	
X44=		OR	X88=	
+150=		OR	+300=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B

	(Column 1)		(Column 2)	(Column 3)
	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDI-TIONAL FEE		RATE	ADDI-TIONAL FEE
X$ 9=		OR	X$18=	
X44=		OR	X88=	
+150=		OR	+300=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

	(Column 1)		(Column 2)	(Column 3)
	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDI-TIONAL FEE		RATE	ADDI-TIONAL FEE
X$ 9=		OR	X$18=	
X44=		OR	X88=	
+150=		OR	+300=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
***If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P. O. Box 272400
Fort Collins, Colorado 80527-2400

PATENT APPLICATION

ATTORNEY DOCKET NO. 200404941-1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Scott L. Michaelis et al. **Confirmation No.:**

Application No.: **Examiner:**

Filing Date: **Group Art Unit:**

Title: SYSTEM AND METHOD FOR PROVIDING FIRMWARE RECOVERABLE LOCKSTEP PROTECTION

Mail Stop Amendment
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

This Information Disclosure Statement is submitted:

(X) under 37 CFR 1.97(b), or
(Within three months of filing national application; or date of entry of national application; or before mailing date of first office action on the merits; whichever occurs last)

( ) under 37 CFR 1.97(c) together with either a:
( ) Statement under 37 CFR 1.97(e), or
( ) a $180.00 fee under 37 CFR 1.17(p), or
(After the CFR 1.97 (b) time period, but before final action or notice of allowance, whichever occurs first)

( ) under 37 CFR 1.97 (d) together with a:
( ) Statement under 37 CFR 1.97(e)(1) or (2), and
( ) a $180.00 fee set forth in 37 CFR 1.17(p).
(Filed after final action, a notice of allowance, on or before payment of the issue fee)

Please charge to Deposit Account **08-2025** the sum of $0.00 . At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account **08-2025** pursuant to 37 CFR 1.25.

(X) Applicant(s) submit herewith Form PTO 1449 - Information Disclosure Statement together with any required copies of patents, publications or other information of which applicant(s) are aware, which applicant(s) believe(s) may be material to the examination of this application and for which there may be a duty to disclose in accordance with 37 CFR 1.56.

( ) A concise explanation of the relevance of foreign language patents, foreign language publications and other foreign language information listed on PTO Form 1449, as presently understood by the individuals(s) designated in 37 CFR 1.56 (c) most knowledgeable about the content is given on the attached sheet, or where a foreign language patent is cited in a search report or other action by a foreign patent office in a counterpart foreign application, an English language version of the search report or action which indicates the degree of relevance found by the foreign office is listed on form PTO 1449 and is enclosed herewith.

It is requested that the information disclosed herein be made of record in this application.

"Express Mail" label no. **EV 375345153US**

Date of Deposit **Oct. 25, 2004**

I hereby certify that this is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to: Commissioner for Patents, Alexandria, VA 22313-1450.

By

Typed Name: **Phyllis Ewing**

Respectfully submitted,

Scott L. Michaelis et al.

By

Jody C. Bishop

Attorney/Agent for Applicant(s)
Reg. No. **44,034**

Date: **Oct. 25, 2004**

Telephone No.: **(214) 855-8007**

FORM PTO-1449 LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	ATTY. DOCKET NO. **200404941-1**	APPLICATION NO.	CONFIRMATION NO.
	APPLICANT **Scott L. Michaelis et al.**		
	FILING DATE	GROUP	

REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	1A	5,226,152	07/06/1993	Klug et al.	
	1B	5,249,188	09/28/1993	McDonald	
	1C	5,751,932	05/12/1998	Horst et al.	
	1D	5,758,058	05/26/1998	Milburn	
	1E	5,764,660	06/09/1998	Mohat	
	1F	6,065,135	05/16/2000	Marshall et al.	
	1G	6,148,348	11/14/2000	Garnett et al.	
	1H	6,473,869	10/29/2002	Bissett et al.	
	1I	6,560,682	05/06/2003	Miller et al.	
	1J	6,604,177	08/05/2003	Kondo et al.	
	1K	6,615,366	09/02/2003	Grochowski et al.	

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	1L					
	1M					
	1N					
	1O					
	1P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

	1Q	Attorney Docket No. 200404946-1, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR USING INFORMATION RELATING TO A DETECTED LOSS OF LOCKSTEP FOR DETERMINING A RESPONSIVE ACTION "
	1R	Attorney Docket No. 200404944-1, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR ESTABLISHING A SPARE PROCESSOR FOR RECOVERING FROM LOSS OF LOCKSTEP IN A BOOT PROCESSOR"
	1S	Attorney Docket No. 200404943-1, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR CONFIGURING LOCKSTEP MODE OF A PROCESSOR MODULE"

EXAMINER	DATE CONSIDERED

FORM PTO-1449 LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	ATTY. DOCKET NO. **200404941-1**	APPLICATION NO.	CONFIRMATION NO.
	APPLICANT **Scott L. Michaelis et al.**		
	FILING DATE	GROUP	

REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	2A	6,625,749	09/23/2003	Quach	
	2B	6,687,851	02/03/2004	Somers et al.	
	2C	6,754,787	06/22/2004	Miller et al.	
	2D	2002/0144177	10/03/2002	Kondo et al.	
	2E	2003/0070050	04/10/2003	Miller et al.	
	2F	2004/0006722	01/08/2004	Safford	
	2G	2004/0019771	01/29/2004	Quach	
	2H	2004/0153857	08/05/2004	Yamazaki et al.	
	2I				
	2J				
	2K				

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	2L					
	2M					
	2N					
	2O					
	2P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

	2Q	Attorney Docket No. 200404974-1, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR MAINTAINING IN A MULTI-PROCESSOR SYSTEM A SPARE PROCESSOR THAT IS IN LOCKSTEP FOR USE IN RECOVERING FROM LOSS OF LOCKSTEP FOR ANOTHER PROCESSOR
	2R	Attorney Docket No. 200404973-1, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR SWITCHING THE ROLE OF BOOT PROCESSOR TO A SPARE PROCESSOR RESPONSIVE TO DETECTION OF LOSS OF LOCKSTEP IN A BOOT PROCESSOR "
	2S	Attorney Docket No. 200404971-1, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR REESTABLISHING LOCKSTEP FOR A PROCESSOR MODULE FOR WHICH LOSS OF LOCKSTEP IS DETECTED"

EXAMINER	DATE CONSIDERED

FORM PTO-1449 LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	ATTY. DOCKET NO. **200404941-1**	APPLICATION NO.	CONFIRMATION NO.
	APPLICANT **Scott L. Michaelis et al.**		
	FILING DATE	GROUP	

REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	3A				
	3B				
	3C				
	3D				
	3E				
	3F				
	3G				
	3H				
	3I				
	3J				
	3K				

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	3L					
	3M					
	3N					
	3O					
	3P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

	3Q	Attorney Docket No. 200404970-1, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR SYSTEM FIRMWARE CAUSING AN OPERATING SYSTEM TO IDLE A PROCESSOR"
	3R	Attorney Docket No. 200404972-1, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR REINTRODUCING A PROCESSOR MODULE TO AN OPERATING SYSTEM AFTER LOCKSTEP RECOVERY"
	3S	

EXAMINER	DATE CONSIDERED