A 2.4-GHz Low-IF Receiver for Wideband WLAN in 0.6-μm CMOS—Architecture and Front-End

Farbod Behbahani, John C. Leete, *Member, IEEE*, Yoji Kishigami, Andreas Roithmeier, Koichi Hoshino, *Student Member, IEEE*, and Asad A. Abidi, *Fellow, IEEE*

***Abstract*—This paper presents the 2.4-GHz front-end and the first downconversion section of a fully integrated low-IF receiver. The dual-conversion receiver and rejects the image repeatably by 60 dB using integrated polyphase filters without calibration or tuning. The gain of the RF mixer and IF amplifier is switchable to slide the available dynamic range of the following stages based on the conditions of the input signal. The front-end and downconversion sections drain 35 mA on average from a 3.3-V supply. Minimum cascade noise figure is 7.2 dB, and maximum cascade IIP3 is −3.4 dBm.**

I. Introduction

THERE IS a push to migrate more radio signal processing into baseband digital signal processors (DSPs). In narrowband systems, for example, a wide dynamic range but low rate analog-to-digital converter (A/D) can digitize several adjacent channels and then select the desired channel. However, in wideband systems, the analog radio must absorb the input signal dynamic range. Adaptation in the digital part may improve the trade-off between performance and power dissipation. New system standards such as Bluetooth relax radio specifications to make it easier to integrate the analog and digital parts in the radio. On-chip image rejection and direct-conversion architectures are of interest to eliminate IF filters.

A comprehensive mixed-mode design of the entire radio requires that analog and digital sections be designed together. New uses of wireless to transmit high-speed data, mainly to access the Internet, are creating a demand for wideband radio systems. Traditional radio design must expand to enable this, for instance by using adaptive beam steering to suppress the principal interferers and strong multipath components to improve reception [1]. In multiple access systems where the capacity is mainly limited by co-channel interferers, these methods also raise capacity.

To date, only limited adaptation has been demonstrated in the analog portion of widespread radio receivers. In a cellular telephone, it may consist of switchable RF gain and variable gain at IF which prevents saturation in the front-end or under- or overloading the baseband A/D.

This paper describes the design and implementation of the front-end and downconversion sections of a *fully integrated dual-conversion superheterodyne* receiver (RX), with on-chip circuits for large image rejection. Section II describes the system at a high level. The architecture is described in Sections III and IV explains the circuit design in detail. Measurements of the image-reject front-end are reported in Section V. The total RX measurement results will appear in [2]

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F. Behbahani, J. C. Leete, A. Roithmeier, K. Hoshino, and A. A. Abidi are with the Integrated Circuits and Systems Laboratory, Department of Electrical Engineering, University of California, Los Angeles, CA 90095 USA.

Y. Kishigami is with Asahi Chemical Industries, Ltd., Fuji, Japan.

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II. System Description

This adaptive receiver was designed for a wireless local area network (WLAN) operating in the 2.4 GHz ISM band. It supports selectable channel bandwidths (BW) of 625 kHz, 2.5 MHz, and 10 MHz for 0.5, 2, and 8 Mbaud symbol rates, respectively. When there are a few users in a cell, the largest BW is selected to maximize data throughput. With many users, selecting the low BW setting frees up additional channels, thereby granting access to many more users. The modulation used is 4, 16, or 64-QAM, which need SNR of 13.5, 20.4, and 26.5 dB at the detector, respectively, for a BER of 1e-6. In very good channel conditions, 64-QAM is used for high throughput rates. However, if the received S/N drops below 26.5 or 20.4 dB, the modulation is switched to 16 and 4-QAM respectively, to maintain integrity of data transfer, albeit at a lower rate. Adaptation of the symbol rate and constellation provides variable bit rate from 1 to 48 Mbit/s.

The system uses adaptive beam forming with an antenna array. One transceiver must now be attached to every antenna. Aside from the antenna and preselect filter, all other off-chip components must be eliminated. In any case, off-chip channel-select filters cannot be used because their BW is usually fixed. These considerations dictate a highly integrated architecture, and active filters with programmable bandwidth. Due to space limitations, details of the design of the IF strip and the measurements for the whole RX will appear in a companion paper [2].

III. Architecture Rationale

The main objectives in choosing receiver architecture are wide dynamic range, high sensitivity, fewest off-chip components, and lowest power consumption. Fig. 1 shows the block diagram of this dual-conversion low-IF receiver [3], which implements the Weaver architecture. The RF front-end comprises a low noise amplifier (LNA) and an RF quadrature mixer, which downconverts the RF signal to the first IF (IF1). A two-stage polyphase filter following the RF mixer partly rejects the image. Strictly the *first image* in a Weaver architecture need not be suppressed here, because the IF mixers *upconvert* it into the stopband of the subsequent channel select bandpass filter; nevertheless, it was decided to suppress the first image

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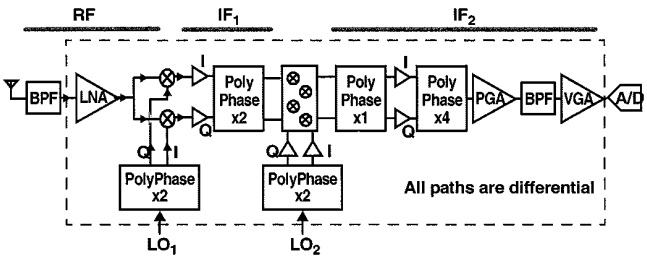

Fig. 1. Receiver block diagram.

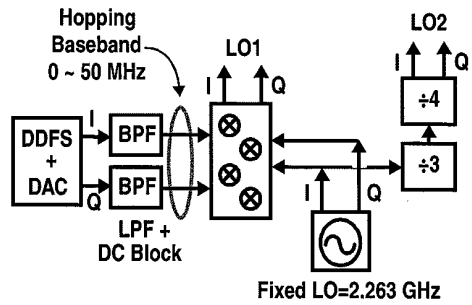

Fig. 2. Proposed frequency synthesizer.

in this receiver to somewhat relax the dynamic range of the IF mixers and the IF2 amplifiers. The IF mixer *downconverts* the *desired* signal at IF1 to a low IF2. Following downconversion, a five-stage wideband polyphase filter rejects the second image entirely on-chip. Amplifiers before the IF1 polyphase filter and within the IF2 polyphase filter compensate loss in the filter passband. In the IF2 strip, the pre-filter programmable gain amplifier (PGA) amplifies the signal to overcome filter noise, while the continuously variable gain post-filter amplifier (VGA) further amplifies the filtered signal to the optimal signal loading (90% full scale) of the A/D converter. The RX is designed for integration with the synthesizer. All signal paths are differential to minimize interaction among the various blocks, or through the substrate.

In a direct conversion receiver, the required $\mathrm{SNR}_{\mathrm{min}}$ of 26.5 dB dictates that image rejection is on the order of 40 dB. This requires better than 1% matching between the various blocks in the I and Q paths, such as amplifiers, channel-select filters, and A/D converters. This is not easy to achieve in practice [4]. Furthermore, a signal at zero-IF competes with dc offset and $1/f$ noise which can significantly degrade SNR of 64-QAM signals at narrow channel bandwidths. For these reasons, the second IF is chosen to be nonzero.

With the same BW, selectivity, and dynamic range, the lower the IF, the less the power consumed by the on-chip bandpass filter [5]. However, a wideband channel at low IF occupies a larger fractional bandwidth over which the image must be rejected. This means more stages in the polyphase filter, therefore higher loss in its passband [6]. For these reasons, a second IF with passband of 5 to 15 MHz is finally used to accommodate the widest 10-MHz channel.

Due to the practical issues discussed in the Section IV-B, the RF mixer can only reject the image by about 35 dB. Thus, IF1 is chosen high enough so that the first image is rejected by an additional 30 dB in the antenna preselect filter. This leads to the final dual-downconversion receiver. A high IF1 also means that spurious signals which might be downconverted by odd-harmonics of LO2 lie in the preselect filter's stopband.

It is very desirable to avoid use of multiple VCOs on the same chip, which tend to injection lock through parasitic coupling. Fig. 2 shows the block diagram of the frequency synthesizer intended for integration with the receiver (not implemented on this prototype). LO2 is a fixed fraction of the frequency of LO1. A direct digital frequency synthesizer (DDFS) and digital-to-analog converter (DAC) generate a fast hopping baseband tone. The VCO upconverts the DAC output in a single-sideband mixer. Quadrature LO2 is generated by dividing the differential VCO frequency by 12, which results in an IF1 of $(2442+10)/(12+1) = 188$ MHz.

The 2.4-GHz ISM band is 80 MHz wide. By dehopping the input signal at the 1st mixer, the BW of IF1 is limited to one channel (a maximum of 10 MHz). This simplifies the design of IF1 amplifiers and the first polyphase filter.

The IF mixer must reject the image by 60 dB on-chip; double-quadrature downconversion desensitizes the ultimate on-chip image rejection to phase errors in IF1 and LO2, and to gain errors in the IF1 paths [7], [8]. Although it is possible to reject the image in a DSP by digitizing separate I and Q paths after the mixer [8], the A/D must digitize the image as well and therefore must have higher dynamic range (DR). Furthermore, the amplifiers and filters after the mixers must be matched in gain as well as the mixers are, which is 0.1% for 60-dB image rejection. This is very difficult in practice. This receiver rejects the image in the analog domain before amplifying and filtering the desired signal in a single scalar path at IF2.

IV. Circuit Design

A. Low Noise Amplifier

Noise figure (NF) is the most important characteristic of an LNA, and depends on the active device noise, passive device loss, the LNA circuit topology, and how close the operating frequency is to device f_T. The differential inductively degenerated common-source (CS) LNA used here gives sub-3-dB NF at 2.4 GHz. Since the frequency of operation is much lower than $f_T/2$ and the Q of the input matching circuit is relatively low, gate-induced noise is not important [9], [10]. To include short channel noise enhancement [11], we have developed a subcircuit model in HSPICE to represent the measured excess noise factor. The measured and simulated NF of the final LNA agree well over a wide frequency band.

1) FET Noise Model in SPICE: The drain current noise power due to the channel noise is expressed as

$$\hat{i}_n^2 = 4\,\mathrm{kT}\Gamma_e \gamma g_{ds0} \tag{1}$$

where Γ_e is the excess noise factor with respect to the basic Spice model. The BSIM2 models used in our design forces $\gamma = 2/3\,(\Gamma_e = 1)$, as in the classical model. Fig. 3 shows the SPICE subcircuit used to model noise enhancement. A scaled current noise from the replica FET is applied between drain and source of M, the principal FET, raising its excess noise factor to Γ_e. The large inductors and capacitors suppress signals applied to

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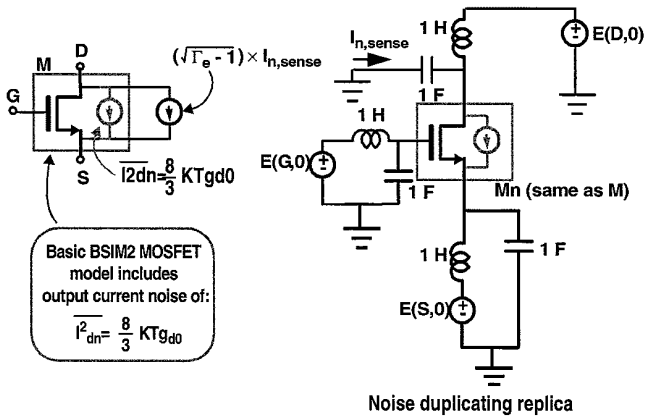

Fig. 3. HSPICE subcircuit to capture enhanced thermal noise.

M from appearing in the replica Mn. This subcircuit works well when the drain and source diffusion resistors have negligible effect.

Noise measured at 50 MHz on a single FET biased at the same point as the LNA shows that $\Gamma_e = 3$. This was used to simulate the actual LNA at 2.4 GHz, including a package model where the pin inductance and capacitance is calculated based on physical dimensions.

In [12] it is shown that feedback through $C_{\rm GD}$ drives the $Y_{\rm in}$ of the LNA away from $Y^*_{s,\rm OPT}$ and raises the NF. The higher the $C_{\rm GD}$ or the gain from gate to the drain of the input FET, the larger will be the NF. This effect is important here because of the relatively large $C_{\rm GD}$ in 0.6-μm CMOS, and it is used to optimize the size of the cascode MOSFET.

2) LNA Optimization: Choosing the right size of FET and laying it out well are both important to obtain a good LNA. Fig. 4 shows a simple CS LNA in cascode configuration to lower undesired capacitive feedback. However, now the combined junction capacitance at the common node raises the noise the cascode FET contributes to the output at 2.4 GHz. This junction capacitance may be lowered with a dual-gate layout [13].

Fig. 5 shows how LNA NF varies with the width of the cascode FET, for a fixed input FET of 150/0.6 μm with interdigitated layout biased at $V_{gs} - V_t = 0.3$ V. The NF is close to minimum when the two FETs are the same size, which gives the opportunity to merge them into one dual-gate FET. This last step further lowers the NF by 0.2 dB because of the lower junction capacitance.

The dual-gate design is explored across various widths at a constant bias of 4 mA, and the resulting NF and IIP3 is shown in Fig. 6. For each width, the input ideal matching circuit is adjusted to obtain narrowband input impedance match to 50 Ω. If $C_{\rm GD}$ and induced gate noise were both zero, the NF would fall indefinitely with width. However, the noise voltage across $C_{\rm GD}$ rises at small FET widths and degrades NF. The size of 150 μm/0.6 μm is finally used because it gives largest dynamic range, and close to the lowest NF.

The LNA (Fig. 7) is fully differential to minimize the effect of noise and interference from other blocks. Three downbonds (each about 1.8 nH) in parallel implement $L_s = 0.9$ nH to present 50 Ω real resistance at the gate of the input MOSFET with each FET biased at 4 mA. The on-chip load $L_d = 5$ nH is a single-layer rectangular spiral inductor in metal-3 layer designed using in-house software to give the highest impedance [14].

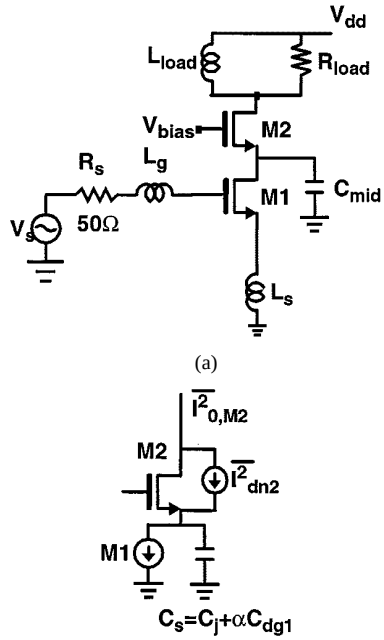

Fig. 4. (a) Common-source LNA circuit. (b) How cascode FET contributes RF noise.

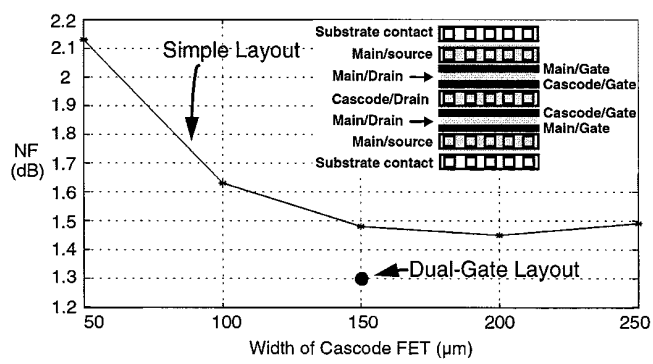

Fig. 5. Overall noise figure at 2.4 GHz for CS LNA ($V_{gs} - V_t = 300$ mV). Inset shows dual-gate layout.

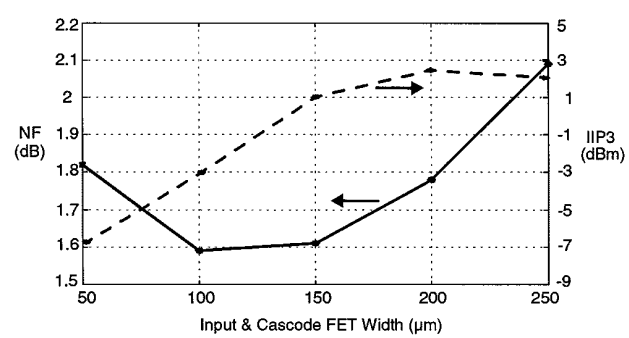

Fig. 6. NF and IIP3 of a simple CS LNA versus MOSFET width.

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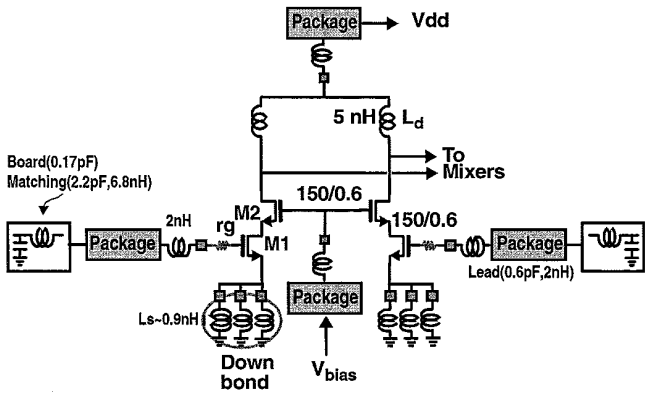

Fig. 7. Complete circuit of differential common-source LNA.

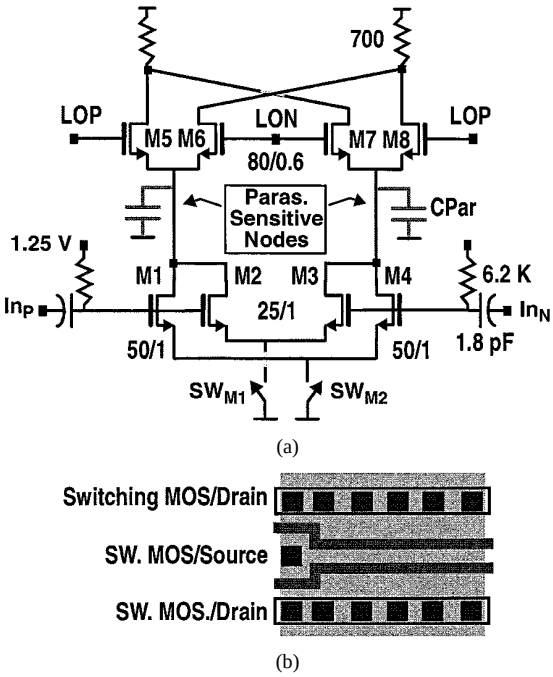

Fig. 8. a) RF mixer. b) Pseudo-dual-gate layout of switching transistors.

B. RF Mixer

The RF mixer downconverts the RF band (2.402 to 2.482 GHz) to IF1 (188 MHz) with tunable low side LO injection (2.212 to 2.292 GHz). Passive FET downconversion mixers used in quadrature arrangement with capacitive loads suffer from large conversion loss because they are nonunilateral [12]. Therefore, the Gilbert-cell-type mixer (Fig. 8) is used. Sharp transitions in the LO waveform lower both the noise [15] and distortion due to mixer switches. Raising the amplitude of a sinewave LO sharpens the transition, but if the LO voltage drives the switch FETs deep into triode, mixer nonlinearity worsens because of the nonlinear output resistance of the transconductance FETs. In the circuit of Fig. 8(a), $C_{\rm Par}$ should be minimized to reduced the noise contribution of the switch transistors [15]. The pseudo-dual-gate layout shown in Fig. 8(b) lowers the switch noise contribution by 2 dB. The switch FETs are biased at $V_{GS} - V_t = 0.2$ V for best noise and linearity. With resistive load, R_L, the resulting noise current is $4\,{\rm kT}/R_L$. Considering that for an ideal doubly balanced mixer, the voltage conversion gain is ${\rm Gain}_v = (2/\pi) g_{m,{\rm Main}}.R_L$, and using results from [15]:

$$\text{Relative Load Noise} = \frac{\hat{i}_n^2(\text{load})}{\hat{i}_n^2(\text{transconductance})} \simeq \frac{1}{\gamma} \cdot \frac{2}{\pi {\rm Gain}_v}. \quad (2)$$

Two major sources of nonlinearity in the mixer are the input transconductor and the switches. As is now customary for MOS mixers, the transconductor consists of a grounded-source differential pair. The FETs are biased at $V_{\rm eff} = V_{GS} - V_t = 0.5$ V. Simulations show that this circuit is 10 dB more linear than a differential pair with a constant tail current, leading to a mixer IIP3 of +18 dBm referred to 100 Ω differential source resistance. With the output biased at 2 V, the transconductor and the switches contribute equal nonlinearity at a mixer gain of 5 dB.

The DR of the front-end may be slid up or down. When the desired signal is low, the front-end NF must be lowest for sensitivity. If the desired signal is larger, a higher NF can be tolerated, and the DR is slid up for higher IIP3 by switch selecting the gain of the RF mixer and IF1 amplifier. Mixer transconductance FET size may be selected as 25/1, 50/1, or 75/1 μm. DC and ac voltage drop across the switches is negligible. Table I summarizes simulated mixer performance. With 50/1 μm input FETs the switches and resistive load each contribute about 27% of the total output noise.

TABLE I
SIMULATION RESULTS OF ONE DIFFERENTIAL RF MIXER

Input Dev. size(μm)	I_{Bias} (mA)	Gain (dB)	V_n diff. (nV/$\sqrt{\rm Hz}$)	IIP3 (dBm) Ref. 100Ω diff.
25/1	0.95	-5	9.4	17
50/1	1.9	0.5	6.2	
75/1	2.7	3	5	15.5

The mixer is ac-coupled to the LNA output. The LNA output is biased at a high level for linearity, while the mixer input is biased close to ground. The coupling capacitor is poly over diffusion. Its voltage coefficient and bottom plate parasitic degrade linearity. The bottom plate is connected to the LNA output to absorb the parasitic into the tuned load, and also to raise the reverse bias across the bottom depletion layer. The output of the mixer is ac-coupled to the following amplifier, for the same reasons. The total voltage loss due to the input and output coupling capacitors is about 2.5 dB.

At moderate $V_{\rm eff}$, g_m is proportional to the overdrive voltage, and so is the IM3 for a given input. Therefore, doubling the $V_{\rm eff}$ at constant bias current halves the g_m (3 dB higher input noise) but raises IIP3 by 3 dB [10]. Thus at a fixed power consumption, the input dynamic range is always constant. On the other hand, switch selecting a smaller MOSFET at constant $V_{\rm eff}$ will lower mixer gain and when the mixer is the bottleneck, improve overall linearity, at the price of higher mixer NF and lower spurious-free dynamic range (SFDR).

A two-stage LO polyphase filter generates quadrature signals from a differential LO input to the receiver. The quadrature ac-

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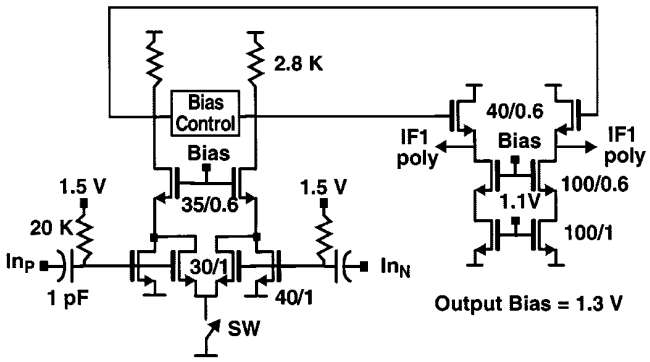

Fig. 9. IF1 amplifier.

TABLE II
SIMULATION RESULTS OF THE IF1 AMPLIFIER AND BUFFER

W_{eff} (μm)	I_{bias} (mA)	Gain (dB)	V_n diff (nV/√Hz)	IIP3 (dBm)
40	6.2	6	4.6	15
70	8.5	10	3.5	10.5

curacy must be enough for 38-dB image rejection over a BW of 1.6 to 2.6 GHz, which covers the input 80-MHz tuning range of the first LO and allows ±25% safety margin for process spreads in the $R \times C$ defining the filter zeros. The capacitance at the LO input of the RF mixer loads the polyphase filter output, increasing loss in its passband. To overcome this, four on-chip inductors are placed at the LO inputs to resonate with this capacitance. LO1 inductors are made by three layers of metal in series for $L = 5.5$ nH, self resonance at 3.2 GHz, and $R_S = 14\ \Omega$ [14]. Simulations show that these inductors lower loss in the polyphase filter by 3.5 dB.

C. IF1 Amplifier and Polyphase Filter

The IF1 amplifier gain of 5 dB compensates loss in the IF1 polyphase filter and in the passive IF mixer. Furthermore, to avoid overload by adjacent channels, it drives the strongly frequency-dependent input impedance IF1 polyphase filter with low source impedance [7]. The first stage of the amplifier is common-source with 11-dB gain (Fig. 9); like the RF mixer, it uses a grounded source FET input stage to improve the linearity. Without cascode devices, the simulated IIP3 of the CS amplifier is about +24 dBm (referred to 100 Ω), so that at minimum gain of 11 dB, the resulting IIP3 is +12 dBm. A cascode suppresses r_{DS} nonlinearity. At an input bias of 1.5 V, the IIP3 of the CS amplifier with cascode (Fig. 9) improves to +28 dBm, now limited by the input FET nonlinearity.

The nMOS source-follower (SF) second-stage level shifts the signal to the 1.3-V bias required by the IF mixer. However, the output signal suffers loss and nonlinearity due to body effect. The bias current and the size of the input device are optimized for the required output impedance with best linearity. When loaded with the polyphase filter, its IIP3 is +27 dBm and gain is −4 dB.

To slide dynamic range, the effective size of the input MOSFETs is switchable from 40/1 to 70/1 μm. Table II shows the

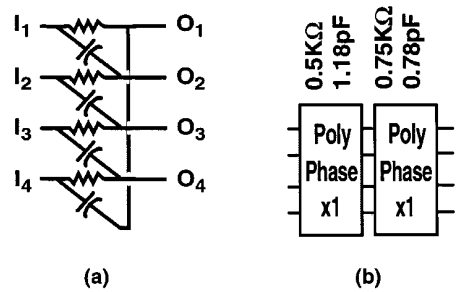

Fig. 10. IF1 and LO2 polyphase filters.

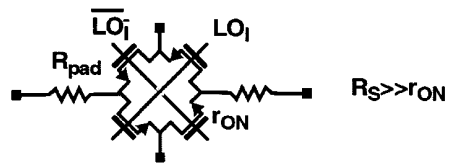

Fig. 11. Passive mixer with padding resistors.

characteristics of the IF1 amplifier with two gain settings. At the lower gain setting, the cascade loss is about 1.5 dB from the input of the IF1 amplifier, through the polyphase filters and mixers, to the input of the IF2 amplifier.

Following this amplifier, a two-stage *RC* polyphase filter rejects the image of the first mixer by about 35 dB. For this image rejection, the RF mixers should match in gain by about 2%, and the phase accuracy of the quadrature LO should be commensurate. The IF1 polyphase filter (Fig. 10) is designed for this image rejection over the required BW.

D. IF Mixer

The much greater challenge is in the IF mixers, which must reject the image by 60 dB after downconversion from 188 MHz to IF2. Now the mixer gain must match to 0.1% [7]. In a Gilbert-cell mixer, matching the transconductors to this level requires very large-area devices (>300 μm^2), or very strong degeneration with well-matched resistors. Since the high input frequency to the mixers requires a high f_T for the input devices, their channel length should be close to minimum. Large area then is obtained by scaling up width, resulting in a proportional rise in power consumption. Strong degeneration requires a large ratio of $V_{R,\mathrm{degen}}/(V_{GS} - V_t)$, which is not practical at low supply voltage. For these reasons, Gilbert-cell-type mixers are suitable for moderate image rejection of up to 40 dB or so, but well-matched passive mixers are the better choice for higher image rejection.

One solution to improve gain matching of passive mixers, shown in Fig. 11, is to pad them with well-matched resistors. If the switch ON-resistance is much smaller than the padding resistor, the latter sets the mixer gain. The sensitivity to the switch ON resistance is now lower by the factor $R_{\mathrm{Pad}}/r_{\mathrm{ON}}$. The polyphase filters surrounding the IF mixer naturally pad the mixer switches with well-matched impedance.

As the mixer transitions from ON to OFF, its r_{ON} rises and will exceed R_{Pad}. To avail the benefits of padding, this transition interval must be made as short as possible relative to the LO

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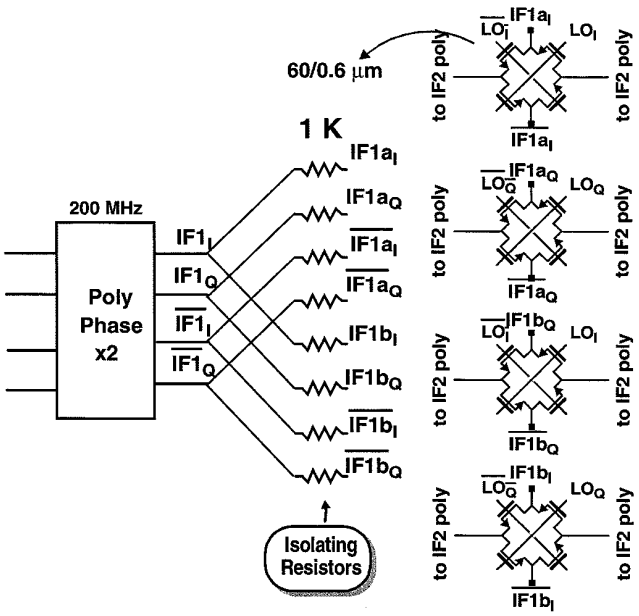

Fig. 12. Isolating resistors before the passive 4-mixer structure lower loading between the differential inputs, and undesired charge sharing between the capacitive loads.

period. If the shortest transition time is limited by, say, the rise-time of CMOS inverters (0.3 ns here) which drive the mixers, the longer the LO period, the better the suppression of FET mismatch. Thus in 0.6-μm CMOS, mixers that must reject the image by 60 dB should not be switched at LO frequencies higher than a few hundred megaHertz. This justifies the choice of the dual-conversion in this receiver.

When passive mixers are configured into the single sideband select arrangement implementing the relationship $I \times I + Q \times Q$ and $I \times Q - Q \times I$, where the terms in each product refer to the IF input and the LO, the four nonunilateral switch MOSFETs short together the differential inputs. In other words, the circuit driving the mixers is loaded by a small resistor $2.r_{\rm ON}$, leading to large attenuation, which is overcome by dissipating more power in the driving circuit. To circumvent this problem, isolation resistors between the mixers can raise the impedance between differential inputs, as shown in Fig. 12 [7]. The resistors raise the total conversion loss of the passive mixers from 4 to 5.5 dB, but this is acceptable. Simulation shows that the loss is 1.5 dB higher if the isolating resistors follow the mixers.

The sources/drains of the switch FETs are biased at 1.3 V. With $W/L = 60/0.6$ μm and 3.3-V gate voltage, $r_{\rm ON}$ is 70 Ω for each switch. CMOS inverters driving the LO port switch from 0 to V_{dd} (3.3 V). Isolation resistors are 1 kΩ, and the polyphase resistor after the mixer 5.6 kΩ. Thus, the padding impedance is two orders of magnitude larger than $r_{\rm ON}$. Now the mixer FETs may mismatch by up to 8% without degrading image rejection.

E. IF2 Amplifier and Polyphase Filter

At IF2, this receiver amplifies and filters in scalar, not quadrature, paths. Therefore, to avoid spectrum folding around 0 Hz, IF2 must be chosen higher than BW/2, where BW is the bandwidth of the widest channel. This has important repercussions on the design of the IF2 polyphase filter [7]. For uniform image rejection across the band, the higher the signal $f_{\max}/f_{\min}$, the more polyphase filter stages needed in cascade. Theoretically with perfect components, a five-stage polyphase filter is needed to reject the image by 60 dB over a BW of 3.5 to 20 MHz. This covers the maximum channel BW of 10 MHz, and allows $\pm$25% margin for process spreads if IF2 $=$ 10 MHz.

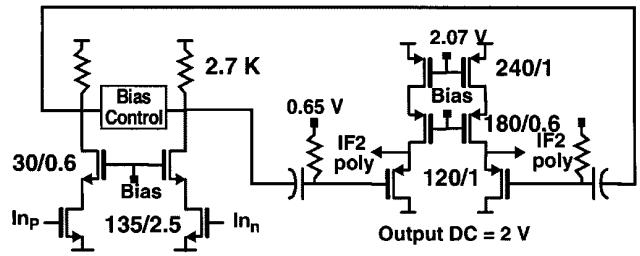

Fig. 13. IF2 amplifier.

Various options were considered to customize the polyphase filter to the widely varying channel bandwidths, such as scaling IF2 with bandwidth, or switching the elements of the polyphase filter. None were found beneficial in terms of reducing chip area.

The passive polyphase filters and passive mixers are lossy. Without amplification, their total loss exceeds 20 dB and will degrade the overall receiver NF. If the IF1 amplifier were solely to compensate this loss, the 20-dB gain would degrade both SFDR and blocking dynamic range. Instead, gain is distributed between the IF1 amplifier and a second amplifier, which is optimally placed where the losses preceding and following it are roughly equal. This point is after the first stage of the IF2 polyphase filter. The amplifier gain is 10 dB, and it drives the polyphase filter with low output impedance (Fig. 13). In addition to the requirements of modest power consumption, adequate DR, gain, and low output impedance, any amplifier inserted in the two I and Q branches of the polyphase filter must also match in gain and phase to 0.1% for 60-dB image rejection. This requires very careful design. From [16] $\sigma_{Vt} = 10$ mV/$\sqrt{\rm WL}$ for the 9-nm gate oxide of this process. From [17] σ_β/β is 0.7%/$\sqrt{\rm WL}$ for 0.8-μm CMOS, which is used as a pessimistic estimate for 0.6-μm CMOS. As the desired amplification bandwidth at IF2 is about 20 MHz, long-channel FETs with low f_T may be used. The gate area of these FETs is large at modest W/L ratios, which means that good matching is achieved without prohibitive bias current. The final amplifier, shown in Fig. 13, was designed using Monte Carlo simulations in HSPICE, with an added safety margin of 2$\times$.

The input of the common-source stage is biased by the output of the IF1 amplifier through the preceding polyphase filter and passive mixers. The source follower output is ac coupled. The coupling capacitor between the two stages creates zero at dc and pole at about 5 MHz. This partly compensates high-frequency droop in the polyphase filter passband. All four IF2 differential amplifiers drain a total of 9.5 mA. Its input-referred noise, including the filter load, is 6.4 nV/$\sqrt{\rm Hz}$, and IIP3 is $+$15 dBm referred to 100 Ω. Now the loss from the input of the IF2 amplifier to the output of the IF2 polyphase filter is only 1 dB.

On the chip, all amplifier FETs are placed in the same orientation, and dummy stages on both sides of the amplifier array

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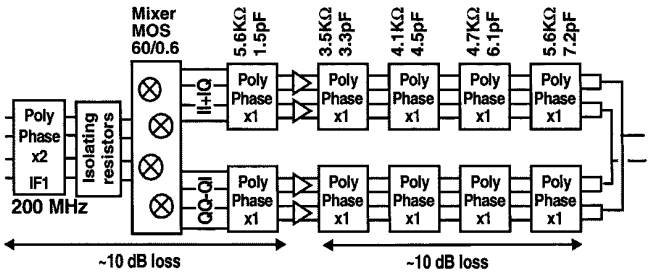


Fig. 14. Complete image reject chain.

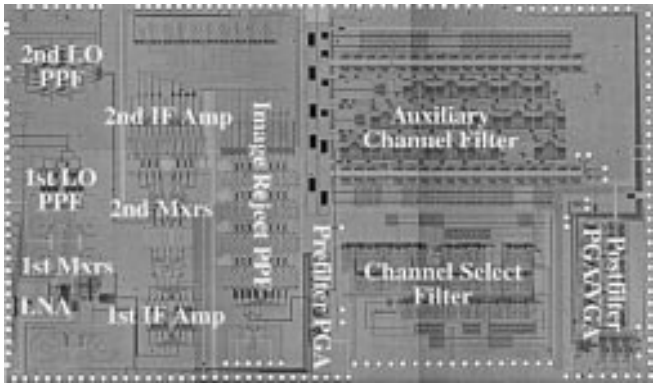


Fig. 15. Chip photo of integrated receiver.

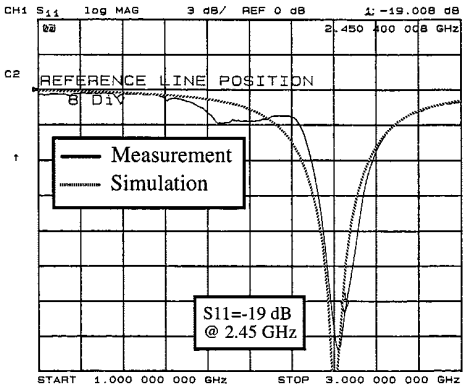
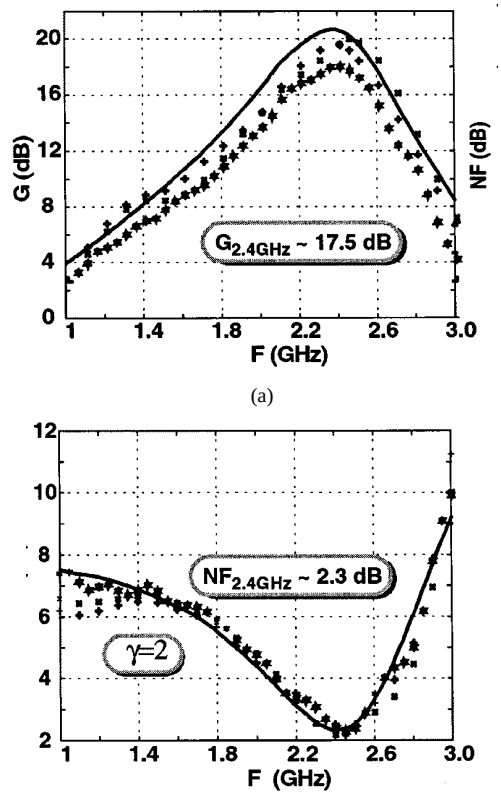


Fig. 16. Measured and simulated s_{11} for packaged LNA test chip.



(a)

(b)

Fig. 17. Simulated (solid) and measured (points) results of three samples for the stand-alone LNA. (a) Gain. (b) NF.

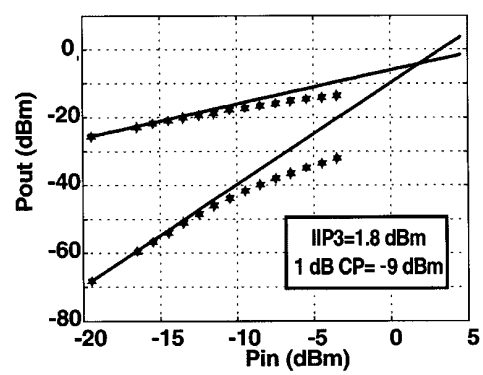


Fig. 18. Input-referred third-order intercept point (IIP3).

protect against nonuniform lithography at the boundary. A wide common-ground line lowers stray IR voltage drop, which would introduce mismatch. The layout is on a common centroid to cancel linear processing gradients.

The resistance tapers up in the polyphase filter stages, as shown in Fig. 14, to lower passband loss [7]. The resistance of the fifth stage, where the signal is attenuated most after IF2 amplification, as well as resistance in the first stage, prior to amplification, together determines total noise. The optimal ordering of the polyphase filter stages to best balance loss, noise, and loading is found through simulation.

V. Measurement Results

Fig. 15 shows the die photograph of the complete receiver. It is implemented in a 0.6-μm single-poly triple-metal epi-CMOS process, operating at 3.3 V. The chip area is 20 mm^2. A stand-alone version of the LNA was fabricated to compare measured performance with simulation results. Fig. 16 shows the measured and simulated s_{11} of the LNA. The measured and simulated NF and gain for three samples of the LNA are compared in Fig. 17. Owing to careful noise modeling, an accurate model of the package parasitics, and the correct de-embedding procedure [18] the NF is predicted very accurately. The measured gain is somewhat lower, probably due to a slight mistuning of the output circuit, and because loss in the drain junction diodes, which is known to lower the gain [19], was not simulated. The measured IIP3 of the LNA is shown in Fig. 18.

Table III summarizes the measured performance of front-end and downconversion part of the RX in three gain modes operating from a 3.3-V supply. This comprises all the blocks from

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TABLE III
MEASURED PERFORMANCE SUMMARY OF THE FRONT-END AND IMAGE-REJECT DOWNCONVERSION BLOCKS

Mode	2.2 GHz mixer gain	270 MHz amp gain	Idd (mA)	Gain (dB)	NF (dB)	IIP3 (dBm)
1	H	H	36	20.3	7.2	-9.5
2	M	L	32.4	14.3	11	-6.8
3	L	L	30.7	9.2	16	-3.4

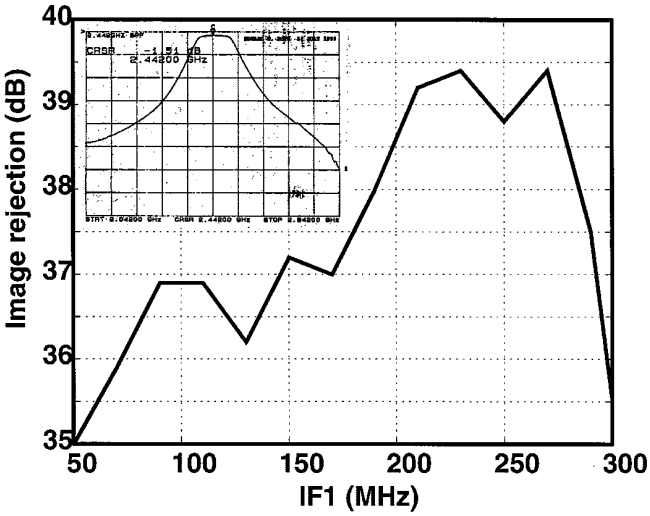

Fig. 19. Measured on-chip image rejection for RF mixer. Inset shows frequency response of antenna prefilter.

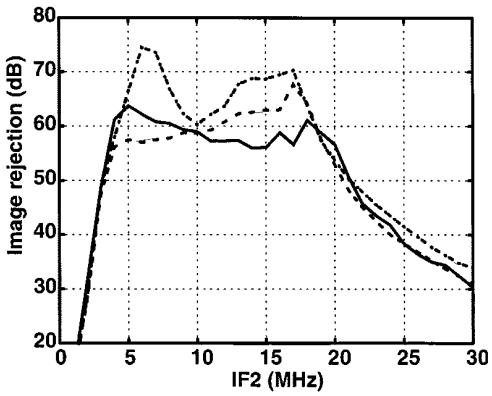

Fig. 20. Measured on-chip image rejection for the IF mixer.

the input of the LNA to the output of the IF2 polyphase filter. The measurement results of the IF strip (from input of the PGA1 to the output of the RX) and the whole RX are presented elsewhere [2]. Fig. 19 plots the on-chip image rejection of the RX at the first IF of 190 MHz. The wideband image rejection of 35 dB is close to the intended value, the remaining rejection being obtained from the stopband of the preselect filter. Image rejection at the second IF of about 60 dB is shown in Fig. 20 for three samples. The main difference from the results reported in a prototype earlier in [7] is that the IF2 amplifiers are embedded in the polyphase filters. It may be concluded that these amplifiers match to better than 0.1% in gain, as designed, to deliver this image rejection.

The chip was mounted in a 64-pin ceramic quad flatpack (CQFP) for all tests. Unlike the discrete chip components matching the input impedance of the stand-alone LNA, transmission line stubs and two capacitors are used in a differential arrangement to match the input impedance of the LNA in the complete receiver.

VI. CONCLUSION

A fully integrated double-downconversion low-IF superheterodyne RX is implemented in a 0.6-μm CMOS process. Together with the preselect filter, the circuit obtains a minimum 67-dB image rejection at the RF mixer. By means of polyphase filters and a double-quadrature downconversion, the image after IF downconversion is repeatably rejected by 60 dB on-chip. The gain of the RF mixer and IF1 amplifiers is switched to optimally slide the RX dynamic range. The front-end and downconversion blocks drain 35 mA from a 3.3-V supply and provide maximum gain and IIP3 of 20.3 and -3.4 dB, respectively. The minimum cascade NF is 7.2 dB.

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Farbod Behbahani was born in Tehran, Iran, in 1967. He received the B.S. and M.S. degrees (with honors) in electrical engineering from Sharif University of Technology, Tehran, Iran, in 1990 and 1993, respectively, and the Ph.D. degree from the University of California, Los Angeles (UCLA), in 1999.

From 1992 to 1995, he worked for Philips Semiconductors as an RF and Analog Integrated Circuit Designer. From 1995 to 1999, he was a Research Assistant at UCLA. Since 1999, he has been with Valence Semiconductor Inc., Irvine, CA, where he is the Director of Engineering, RF and wireless. His research interests include RF CMOS and adaptive architecture for wireless radio. He has received two U.S. patents and is an author or co-author of more than 25 technical papers in the area of integrated circuit design and communication systems.

Dr. Behbahani was a corecipient of the second prize in the annual Iranian national research contest in 1996 and the IEEE Solid-State Circuits Society Predoctoral Fellowship in 1997. He received the Young Scientist Award from the Association of Professors and Scholars of Iranian Heritage in California in 1999.

John C. Leete (S'94–M'99) received the B.S. degree in electrical engineering from North Carolina State University, Raleigh, in 1995 and the M.S. degree in electrical engineering from the University of California, Los Angeles, in 1999.

He is currently with Broadcom Corporation, El Segundo, CA. His current interests include RF IC design for wireless communications and ESD protection strategies for RF circuits and systems.

Mr. Leete is a member of Phi Kappa Phi and Eta Kappa Nu.

Yoji Kishigami was born in Tokushima, Japan, in 1967. He received the B.S. and M.S. degrees in physics from Kyoto University, Kyoto, Japan, in 1991 and 1993, respectively.

He joined Asahi Kasei Corporation, Fuji, Japan, in 1993, where he has been engaged in the research and development of RF ICs. From 1998 to 1999, he was a Research Scholar in the Department of Electrical Engineering, University of California, Los Angeles, where he worked on the design of CMOS RF circuits.

Andreas Roithmeier, biography and photograph not available at time of publication.

Koichi Hoshino (M'97–S'99) received the B.S. degree in electrical engineering from the Science University of Tokyo, Tokyo, Japan, in 1993. He is currently working toward the M.S. degree in electrical engineering at the University of California, Los Angeles (UCLA).

From 1993 to 1998, he was with NEC Corporation, Kawasaki, Japan, where he was a Si-MMIC Design Engineer in the Compound Semiconductor Device Division. Since 1999, he has been a Research Assistant at UCLA. His areas of interest include RF CMOS IC design for wireless communications. He has received two U.S. patents.

Asad A. Abidi (S'75–M'80–SM'95–F'96) received the B.Sc. (Hons.) degree from Imperial College, London, U.K., in 1976 and the M.S. and Ph.D. degrees in electrical engineering from the University of California, Berkeley, in 1978 and 1981.

He was at Bell Laboratories, Murray Hill, NJ, from 1981 to 1984 as a Member of Technical Staff in the Advanced LSI Development Laboratory. Since 1985, he has been with the Electrical Engineering Department, University of California, Los Angeles, where he is a Professor. He was a Visiting Faculty Researcher at Hewlett Packard Laboratories during 1989. His research interests are in CMOS RF design, high-speed analog integrated circuit design, data conversion, and other techniques of analog signal processing. He was the Program Secretary for the International Solid-State Circuits Conference from 1984 to 1990 and General Chairman of the Symposium on VLSI Circuits in 1992. He was Secretary of the IEEE Solid-State Circuits Council from 1990 to 1991. From 1992 to 1995, he was Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS.

Dr. Abidi has received the 1988 TRW Award for Innovative Teaching and the 1997 IEEE Donald G. Fink Award. He was a corecipient of the Best Paper Award at the 1995 European Solid-State Circuits Conference, the Jack Kilby Best Student Paper Award at the 1996 International Solid-State Circuits Conference (ISSCC), the Jack Raper Award for Outstanding Technology Directions Paper at the 1997 ISSCC, and the Design Contest Award at the 1998 Design Automation Conference.

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