DECLARATION OF JUNE ANN MUNFORD

1. My name is June Ann Munford. I am over the age of 18, have personal knowledge of the facts set forth herein, and am competent to testify to the same.

2. I earned a Master of Library and Information Science (MLIS) from the University of Wisconsin-Milwaukee in 2009. I have over ten years of experience in the library/information science field. Beginning in 2004, I have served in various positions in the public library sector including Assistant Librarian, Youth Services Librarian and Library Director. I have attached my Curriculum Vitae as Appendix CV.

3. During my career in the library profession, I have been responsible for materials acquisition for multiple libraries. In that position, I have cataloged, purchased and processed incoming library works. That includes purchasing materials directly from vendors, recording publishing data from the material in question, creating detailed material records for library catalogs and physically preparing that material for circulation. In addition to my experience in acquisitions, I was also responsible for analyzing large collections of library materials, tailoring library records for optimal catalog

search performance and creating lending agreements between libraries during my time as a Library Director.

4. I am fully familiar with the catalog record creation process in the library sector. In preparing a material for public availability, a library catalog record describing that material would be created. These records are typically written in Machine Readable Catalog (herein referred to as "MARC") code and contain information such as a physical description of the material, metadata from the material's publisher, and date of library acquisition. In particular, the 008 field of the MARC record is reserved for denoting the date of creation of the library record itself. As this typically occurs during the process of preparing materials for public access, it is my experience that an item's MARC record indicates the date of an item's public availability.

5. Typically, in creating a MARC record, a librarian would gather various bits of metadata such as book title, publisher and subject headings among others and assign each value to a relevant numerical field. For example, a book's physical description is tracked in field 300 while title/attribution is tracked in field 245. The 008 field of the MARC record is reserved for denoting the creation of the library record itself. As this is the only date reflecting the inclusion of said materials within the library's collection, it is my experience

that an item's 008 field accurately indicates the date of an item's public availability.

6. I have reviewed Exhibit 1004, "Adaptive Analog IF Signal Processor for a Wide-Band CMOS Wireless Receiver" by Farbod Behbahani, et al. as published in *IEEE Journal of Solid-State Circuits*, August 2001.

7. Attached hereto as Appendix BEHBAHANI01 is a true and correct copy of the MARC record for *IEEE Journal of Solid-State Circuits* as held by the Carnegie Library of Pittsburgh. I secured this record myself from the library's public catalog. The MARC record contained within Appendix BEHBAHANI01 accurately describes the title, author, publisher, and ISSN number of *IEEE Journal of Solid-State Circuits.* The 'Lib Has' field of this record visible on page 3 indicates this collection includes the August 2001 edition of *IEEE Journal of Solid-State Circuits* containing "Adaptive Analog IF Signal Processor for a Wide-Band CMOS Wireless Receiver".

8. Attached hereto as Appendix BEHBAHANI02 is a true and correct copy of "Adaptive Analog IF Signal Processor for a Wide-Band CMOS Wireless Receiver" as published in *IEEE Journal of Solid-State Circuits* as held by the Carnegie Library of Pittsburgh. I secured these scans myself from the

library's collection. In comparing Exhibit 1004 to Appendix BEHBAHANI02, it is my determination that Exhibit 1004 is a true and correct copy of "Adaptive Analog IF Signal Processor for a Wide-Band CMOS Wireless Receiver" by Farbod Behbahani, et al. as published in *IEEE Journal of Solid-State Circuits* August 2001.

9. The 008 field of the MARC record in Appendix BEHBAHANI01 indicates the date of record creation. The 008 field of Appendix BEHBAHANI01 indicates the Carnegie Library of Pittsburgh first acquired this journal as of September 1, 1975 and held the journal in perpetuity until 2008. Considering this information, it is my determination that *IEEE Journal of Solid-State Circuits* August 2001 and therefore "Adaptive Analog IF Signal Processor for a Wide-Band CMOS Wireless Receiver" was made available to the public shortly after its initial release in August 2001.

10. I have reviewed Exhibit 1006, "A Broad-Band Tunable CMOS Channel-Select Filter for a Low-IF Wireless Receiver" by Farbod Behbahani, et al. as published in *IEEE Journal of Solid-State Circuits*, April 2000.

11. The 'Lib Has' field of Appendix BEHBAHANI01 visible on page 3 indicates the Carnegie Library of Pittsburgh's collection includes the April

2000 edition of *IEEE Journal of Solid-State Circuits* containing "A Broad-Band Tunable CMOS Channel-Select Filter for a Low-IF Wireless Receiver".

12. Attached hereto as Appendix BEHBAHANI03 is a true and correct copy of "A Broad-Band Tunable CMOS Channel-Select Filter for a Low-IF Wireless Receiver" as published in *IEEE Journal of Solid-State Circuits* as held by the Carnegie Library of Pittsburgh. I secured these scans myself from the library's collection. In comparing Exhibit 1006 to Appendix BEHBAHANI03, it is my determination that Exhibit 1006 is a true and correct copy of "A Broad-Band Tunable CMOS Channel-Select Filter for a Low-IF Wireless Receiver" by Farbod Behbahani, et al. as published in *IEEE Journal of Solid-State Circuits* April 2000.

13. The 008 field of the MARC record in Appendix BEHBAHANI01 indicates the date of record creation. The 008 field of Appendix BEHBAHANI01 indicates the Carnegie Library of Pittsburgh first acquired this journal as of September 1, 1975 and held the journal in perpetuity until 2008. Considering this information, it is my determination that *IEEE Journal of Solid-State Circuits* April 2000 and therefore "A Broad-Band Tunable CMOS Channel-

Select Filter for a Low-IF Wireless Receiver" was made available to the public shortly after its initial release in April 2000.

14. I have reviewed Exhibit 1005, "A 2.4-GHz Low-IF Receiver for Wideband WLAN in 0.6-µm CMOS - Architecture and Front-End" by Farbod Behbahani, et al. as published in *IEEE Journal of Solid-State Circuits*, December 2000.

15. The 'Lib Has' field of Appendix BEHBAHANI01 visible on page 3 indicates the Carnegie Library of Pittsburgh's collection includes the December 2000 edition of *IEEE Journal of Solid-State Circuits* containing "A 2.4-GHz Low-IF Receiver for Wideband WLAN in 0.6-µm CMOS - Architecture and Front-End".

16. Attached hereto as Appendix BEHBAHANI04 is a true and correct copy of "A 2.4-GHz Low-IF Receiver for Wideband WLAN in 0.6-µm CMOS - Architecture and Front-End" as published in *IEEE Journal of Solid-State Circuits* as held by the Carnegie Library of Pittsburgh. I secured these scans myself from the library's collection. In comparing Exhibit 1005 to Appendix BEHBAHANI04, it is my determination that Exhibit 1005 is a true and correct copy of "A 2.4-GHz Low-IF Receiver for Wideband WLAN in 0.6-

μm CMOS - Architecture and Front-End" by Farbod Behbahani, et al. as published in *IEEE Journal of Solid-State Circuits* December 2000.

17. The 008 field of the MARC record in Appendix BEHBAHANI01 indicates the date of record creation. The 008 field of Appendix BEHBAHANI01 indicates the Carnegie Library of Pittsburgh first acquired this journal as of September 1, 1975 and held the journal in perpetuity until 2008. Considering this information, it is my determination that *IEEE Journal of Solid-State Circuits* December 2000 and therefore "A 2.4-GHz Low-IF Receiver for Wideband WLAN in 0.6-μm CMOS - Architecture and Front-End" was made available to the public shortly after its initial release in December 2000.

18. I have reviewed Exhibit 1011, "Internally Varying Analog Circuits Minimize Power Dissipation" by Y. Tsividis, et. al as published in *IEEE Circuits & Devices Magazine*, January 2003.

19. Attached hereto as Appendix TSIVIDIS01 is a true and correct copy of the MARC record for *IEEE Circuits & Devices Magazine* as held by the Carnegie Library of Pittsburgh. I secured this record myself from the library's public catalog. The MARC record contained within Appendix

TSIVIDIS01 accurately describes the title, author, publisher, and ISSN number of *IEEE Circuits & Devices Magazine.* The 'Lib Has' field of this record visible on page 2 indicates this collection includes the January 2003 edition of *IEEE Circuits & Devices Magazine* containing "Internally Varying Analog Circuits Minimize Power Dissipation".

20. Attached hereto as Appendix TSIVIDIS01 is a true and correct copy of "Internally Varying Analog Circuits Minimize Power Dissipation" as published in *IEEE Circuits & Devices Magazine* as held by the Carnegie Library of Pittsburgh library. I secured these scans myself from the library's collection. In comparing Exhibit 1011 to Appendix TSIVIDIS01, it is my determination that Exhibit 1011 is a true and correct copy of "Internally Varying Analog Circuits Minimize Power Dissipation" by Y. Tsividis, et al. as published in *IEEE Circuits & Devices Magazine* January 2003.

21. The 008 field of the MARC record in Appendix TSIVIDIS01 indicates the date of record creation. The 008 field of Appendix TSIVIDIS01 indicates the Carnegie Library of Pittsburgh first acquired this journal as of April 17, 1992 and held the journal in perpetuity until 2006. Considering this information, it is my determination that *IEEE Circuits & Devices Magazine* January 2003 and therefore "Internally Varying Analog Circuits Minimize

Power Dissipation" was made available to the public shortly after its initial release in January 2003.

22. I have been retained on behalf of the Petitioner to provide assistance in the above-illustrated matter in establishing the authenticity and public availability of the documents discussed in this declaration. I am being compensated for my services in this matter at the rate of $200.00 per hour plus reasonable expenses. My statements are objective, and my compensation does not depend on the outcome of this matter.

23. I declare under penalty of perjury that the foregoing is true and correct. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: 4/4/2023

June Ann Munford

June A. Munford
Curriculum Vitae

Education

University of Wisconsin-Milwaukee - MS, Library & Information Science, 2009
Milwaukee, WI

- Coursework included cataloging, metadata, data analysis, library systems, management strategies and collection development.
- Specialized in library advocacy, cataloging and public administration.

Grand Valley State University - BA, English Language & Literature, 2008
Allendale, MI

- Coursework included linguistics, documentation and literary analysis.
- Minor in political science with a focus in local-level economics and government.

Professional Experience

Researcher / Expert Witness, October 2017 – present
Freelance ● Pittsburgh, Pennsylvania & Grand Rapids, Michigan

- Material authentication and public accessibility determination. Declarations of authenticity and/or public accessibility provided upon research completion. Experienced with appeals and deposition process.

- Research provided on topics of public library operations, material publication history, digital database services and legacy web resources.

- Past clients include Alston & Bird, Arnold & Porter, Baker Botts, Fish & Richardson, Erise IP, Irell & Manella, O'Melveny & Myers, Perkins-Coie, Pillsbury Winthrop Shaw Pittman and Slayden Grubert Beard.

Library Director, February 2013 - March 2015
Dowagiac District Library ● Dowagiac, Michigan

- Executive administrator of the Dowagiac District Library. Located in

Southwest Michigan, this library has a service area of 13,000, an annual operating budget of over $400,000 and total assets of approximately $1,300,000.

● Developed careful budgeting guidelines to produce a 15% surplus during the 2013-2014 & 2014-2015 fiscal years while being audited.

● Using this budget surplus, oversaw significant library investments including the purchase of property for a future building site, demolition of existing buildings and building renovation projects on the current facility.

● Led the organization and digitization of the library's archival records.

● Served as the public representative for the library, developing business relationships with local school, museum and tribal government entities.

● Developed an objective-based analysis system for measuring library services - including a full collection analysis of the library's 50,000+ circulating items and their records.

November 2010 - January 2013
Librarian & Branch Manager, Anchorage Public Library ● Anchorage, Alaska

● Headed the 2013 Anchorage Reads community reading campaign including event planning, staging public performances and creating marketing materials for mass distribution.

● Co-led the social media department of the library's marketing team, drafting social media guidelines, creating original content and instituting long-term planning via content calendars.

● Developed business relationships with The Boys & Girls Club, Anchorage School District and the US Army to establish summer reading programs for children.

June 2004 - September 2005, September 2006 - October 2013
Library Assistant, Hart Area Public Library
Hart, MI

● Responsible for verifying imported MARC records and original MARC

cataloging for the local-level collection as well as the Michigan Electronic Library.

● Handled OCLC Worldcat interlibrary loan requests & fulfillment via ongoing communication with lending libraries.

Professional Involvement

Alaska Library Association - Anchorage Chapter
● Treasurer, 2012

Library Of Michigan
● Level VII Certification, 2008
● Level II Certification, 2013

Michigan Library Association Annual Conference 2014
● New Directors Conference Panel Member

Southwest Michigan Library Cooperative
● Represented the Dowagiac District Library, 2013-2015

Professional Development

Library Of Michigan Beginning Workshop, May 2008
Petoskey, MI
● Received training in cataloging, local history, collection management, children's literacy and reference service.

Public Library Association Intensive Library Management Training, October 2011
Nashville, TN
● Attended a five-day workshop focused on strategic planning, staff management, statistical analysis, collections and cataloging theory.

Alaska Library Association Annual Conference 2012 - Fairbanks, February 2012
Fairbanks, AK
● Attended seminars on EBSCO advanced search methods, budgeting, cataloging, database usage and marketing.

Depositions

2019 ● Fish & Richardson

Apple v. Qualcomm (IPR2018-001281, 39521-00421IP, IPR2018-01282 and 39521-00421IP2)

2019 ● Erise IP

Implicit, LLC v. Netscout Systems, Inc (Civil Action No. 2:18-cv-53-JRG)

2019 ● Perkins-Coie

Adobe Inc. v. RAH Color Technologies LLC (Cases IPR2019-00627, IPR2019-00628, IPR2019-00629 and IPR2019-00646)

2020 ● O'Melveny & Myers

Maxell, Ltd. v. Apple Inc. (Case No. 5:19-cv-00036-RWS)

2021 ● Pillsbury Winthrop Shaw Pittman LLP

Intel v. SRC (IPR2020-1449)

2022 ● Perkins-Coie

Realtek v. Future Link (IPR2021-01182)

2023 ● Fish & Richardson

Neuroderm Ltd. v. Abbvie, Inc (Case No. PGR2022-00040)

2023 ● Fish & Richardson

Nearmap US Inc. v. Pictometry International Corp. (IPR2022-00735)

2023 ● Fish & Richardson

Samsung Electronics v. MemoryWeb LLC (Case No. 39843-0136PS1)

2023 ● Pillsbury Winthrop Shaw Whitman LLP

Gravel Rating Systems v. Costco Wholesale Corp. (Civil Action No. 4:21-cv-149-ALM)

Limited Case and Clientele History

Alston & Bird

- Ericsson

  v. Collision Communications (IPR2022-01233)

- Nokia

  v. Neptune Subsea, Xtera (Case No. 1:17-cv-01876)

- Universal Electronics Inc

  v. Roku Inc (IPR2022-00818)

Arnold & Porter

- Ivantis

  v. Glaukos (Case No. 8:18-cv-00620)

- Samsung

  v. Jawbone (Case No. 2:21-cv-00186)

Benesch Friedlander Coplan & Aronoff

- Voyis

  v. Cathx (Case No. 5:21-cv-00077-RWS)

Erise I.P.

- Apple
  - v. Ericsson Inc. (IPR2022-00715)
  - v. Future Link Systems (IPRs 6317804, 6622108, 6807505, and 7917680)
  - v. INVT (Case No. 20-1881)
  - v. Navblazer LLC (IPR2020-01253)
  - v. Qualcomm (IPR2018-001281, 39521-00421IP, IPR2018-01282, 39521-00421IP2)
  - v. Quest Nettech Corp (Case No. 2:19-cv-00118-JRG)
  - v. Telefonaktiebolaget LM Ericsson (IPR2022-00275)

- Fanduel
  - v. CGT (Case No. 19-1393)

- Garmin
  - v. Phillips North America LLC (Case No. 2:19-cv-6301-AB-KS)

- Netscout
  - v. Longhorn HD LLC (Case No. 2:20-cv-00349)
  - v. Implicit, LLC (Civil Action No. 2:18-cv-53-JRG)

- Sony Interactive Entertainment LLC
  - v. Bot M8 LLC (IPR2020-01288)
  - v. Infernal Technology LLC (Case No. 2:19-CV-00248-JRG)

- Unified Patents

v. GE Video Compression (Civil Action No. 2:19-cv-248)

Fish & Richardson

- Apple

  v. AliveCor (3:21-cv-03958)

  v. LBS Innovations (Case No. 2:19-cv-00119-JRG-RSP)

  v. Koss Corporation (IPR2021-00305)

  v. Masimo (IPR 50095-0012IP1, 50095-0012IP2, 50095-0013IP1, 50095-0013IP2, 50095-0006IP1, 50095-0135IP1)

  v. Neonode (Case No. 21-cv-08872-EMC)

  v. Qualcomm (IPR2018-001281, 39521-00421IP, IPR2018-01282, 39521-00421IP2)

- Dell

  v. Neo Wireless (IPR2022-00616)

- Dish Network

  v. Entropic Communications, LLC (Case No. 2:2023-CV-01043)

  v. Realtime Adaptive Streaming (Case No. 1:17-CV-02097-RBJ)

  v. TQ Delta LLC (Case No. 18-1798)

- Evapco Dry Cooling

  v. SPG Dry Cooling (IPR2021-00688)

- Genetec

  v. Sensormatic Electronics (Case No. 1:20-CV-00760)

- Huawei

v. Bell Northern Research LLC (IPR2019-01174)

- Kianxis

  v. Blue Yonder (Case No. 3:20-cv-03636)

- LG Electronics

  v. Bell Northern Research LLC (Case No. 3:18-cv-2864-CAB-BLM)

- Metaswitch

  v. Sonus Networks (IPR2018-01719)

- Microsoft

  v. Throughputer Inc (IPR2022-00757)

- Mom Enterprises

  v. Ddrops Company (Case No. 1:22-cv-00332)

- MLC Intellectual Property

  v. MicronTech (Case No. 3:14-cv-03657-SI)

- Nearmap Inc

  v. EagleView Technologies (IPR2022-01009)

- Neuroderm Ltd.

  v. Abbvie, Inc (Case No. PGR2022-00040)

- Realtek Semiconductor

v. Future Link (IPR2021-01182)

- Quectel
  - v. Koninklijke Philips (Case No. 1:20-cv-01710)

- Samsung
  - v. Aire Technology (IPR2022-00877)
  - v. Bell Northern Research (Case No. 2:19-cv-00286-JRG)
  - v. Communication Technologies Inc (IPR2022-01221)
  - v. Jawbone Innovations (IPR2022-00865)
  - v. MemoryWeb LLC (IPR2022-00885)
  - v. Dodots Licensing Solutions (IPR2023-00701)
  - v. Telefonaktiebolaget LM Ericsson (IPR2021-00615)

- Texas Instruments
  - v. Vantage Micro LLC (IPR2020-01261)

- Xilinx
  - v. Sentient Sensors LCC (Case No. 1:22-cv-00173)

Irell & Manella

- Curium

O'Melveny & Myers

- Apple
  - v. Maxell (Case No. 5:19-cv-00036-RWS)

- Micron Technology Inc.

  v. Besang Inc (IPR2023-00900)

- Samsung

  v. Daedalus Prime LLC (1335 Investigation)

Perkins-Coie

- Heru Industries

  v. The UAB Research Foundation (IPR2022-01148)

- Intel Corporation

  v. BitMICRO (Case No. 5:23-cv-00625)

- Realtek Semiconductor

  v. Future Link (IPR2021-01182)

- Twitter Inc

  v. VOIP-Pal.com (Case No. 3:20-cv-02397-JD)

- TCL Industries

  v. Koninklijke Philips NV (IPR2021-00495, IPR2021-00496 and IPR2021-00497)

Pillsbury Winthrop Shaw Pittman

- Intel

  v. FG SRC LLC (Case No. 6:20-cv-00315)

- Gravel Rating Systems

v. Costco (Case No. 4:21-cv-149)
v. Lowe's Home Centers (Case No. 4:21-cv-150)
v. T-Mobile USA (Case No. 4:21-cv-152)
v. Kohl's Inc. (Case No. 4:21-cv-258)
v. Under Armor (Case No. 4:21-cv-356)

Quinn Emanuel

- Wolfspeed

    v. The Trustees of Purdue University (Case No. 1:2021-cv-00840)

Stern, Kessler, Goldstein & Fox

- Preliminary Research

Sheppard, Mullin, Richter & Hampton LLP

- Cadence Design Systems Inc.

    v. Semiconductor Design Technologies (Case No. 3:23-cv-01001)

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005    20150414133918.0
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022    0018-9200
030    IJSCBC
032    925080|bUSPS
035    325360|bMULS|a200004|a300007
040    MUL|cMUL|dNSD|dYUS|dHUL|dSER|dNSD|dOCL|dAIP|dNST|dNSD|dDLC
       |dNST|dDLC|dNST|dIUL|dWaOLN|dUtOrBLW
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210 0  IEEE j. solid-state circuits
222  0 IEEE journal of solid-state circuits
245 00 IEEE journal of solid-state circuits.
246 10 Journal of solid-state circuits
246 23 IEEE journal of solid state circuits
246 23 Journal of solid state circuits
260    New York, N.Y. :|bInstitute of Electrical and Electronics
       Engineers,|c©1966-
300    volumes :|billustrations ;|c28 cm
310    Monthly,|b1991-
321    Quarterly,|b1966-
321    Bimonthly,|b<1986- >
336    text|btxt|2rdacontent
337    unmediated|bn|2rdamedia
338    volume|bnc|2rdacarrier
362 0  Vol. SC-1, no. 1 (Sept. 1966)-
510 1  Computer & control abstracts|x0036-8113|b1968-
510 1  Electrical & electronics abstracts|x0036-8105|b1968-
510 1  Index to IEEE publications|x0099-1368
510 1  Physics abstracts. Science abstracts. Series A|x0036-8091
       |b1968-
510 2  Chemical abstracts|x0009-2258|b1966-1982
510 2  Energy research abstracts|x0160-3604
510 2  Engineering index annual (1968)|x0360-8557
510 2  Engineering index bioengineering abstracts|x0736-6213
510 2  Engineering index energy abstracts|x0093-8408
510 2  International aerospace abstracts|x0020-5842
510 2  ISMEC bulletin|x0306-0039
510 2  Pollution abstracts with indexes|x0032-3624
510 2  Safety science abstracts journal|x0160-1342
510 0  Engineering abstracts monthly|x0013-7960
510 0  Nuclear science abstracts|x0029-5612
510 1  Applied science & technology index|x0003-6986
550    Issued by the IEEE Solid-State Circuits Council.
650  0 Semiconductors|vPeriodicals.
650  0 Integrated circuits|vPeriodicals.
650  0 Solid state electronics|vPeriodicals.
710 2  IEEE Solid-State Circuits Council.
850    CaSRU|aDLC|aIC|aInU|aMChB|aNN|aNcU|aOkU|aPPT|aViBlbV
890    IEEE journal of solid-state circuits.
901    |cSer
935    ADM-6317
936    Vol. 26, no. 1 (Jan. 1991) (surrogate) LIC
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Location	Carnegie Library of Pittsburgh - Off Site Storage (Please ask for assistance)
Lib Has	Volume 1 (1966) to Volume 4 (1969).
Location	CLP Main (Oakland) Second Floor - Magazines
Lib Has	Volume 4 (1969) to Volume 43 (2008).

The eLNetwork is a collaboration of the Allegheny County Library Association and Carnegie Library of Pittsburgh

Title	**IEEE journal of solid-state circuits.**
Publisher	New York, N.Y. : Institute of Electrical and Electronics Engineers, ©1966-
Description	volumes : illustrations ; 28 cm
Frequency	Monthly, 1991- Quarterly, 1966- Bimonthly, <1986- >
Pub Date	Vol. SC-1, no. 1 (Sept. 1966)-

Location	Carnegie Library of Pittsburgh - Off Site Storage (Please ask for assistance)
Lib Has	Volume 1 (1966) to Volume 4 (1969).
Location	CLP Main (Oakland) Second Floor - Magazines
Lib Has	Volume 4 (1969) to Volume 43 (2008).

Details

Indexed In:	Computer & control abstracts 0036-8113 1968- Electrical & electronics abstracts 0036-8105 1968- Index to IEEE publications 0099-1368 Physics abstracts. Science abstracts. Series A 0036-8091 1968- Chemical abstracts 0009-2258 1966-1982 Energy research abstracts 0160-3604 Engineering index annual (1968) 0360-8557 Engineering index bioengineering abstracts 0736-6213 Engineering index energy abstracts 0093-8408 International aerospace abstracts 0020-5842 ISMEC bulletin 0306-0039 Pollution abstracts with indexes 0032-3624 Safety science abstracts journal 0160-1342 Engineering abstracts monthly 0013-7960 Nuclear science abstracts 0029-5612 Applied science & technology index 0003-6986
Issued By	Issued by the IEEE Solid-State Circuits Council.
Subject	Semiconductors -- Periodicals. Integrated circuits -- Periodicals. Solid state electronics -- Periodicals.
Addt'l Author	IEEE Solid-State Circuits Council.
Key Title	IEEE j. solid-state circuits IEEE journal of solid-state circuits
Addt'l Title	IEEE journal of solid state circuits Journal of solid state circuits
ISSN	0018-9200

IEEE
JOURNAL
OF
SOLID
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36
JULY-DEC
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IPR2024-00816
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IEEE JOURNAL OF

SOLID-STATE CIRCUITS

A PUBLICATION OF THE IEEE SOLID-STATE CIRCUITS SOCIETY

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A PUBLICATION OF THE IEEE SOLID-STATE CIRCUITS SOCIETY

AUGUST 2001 VOLUME 36 NUMBER 8 IJSCBC (ISSN 0018–9200)

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Adaptive Analog IF Signal Processor for a Wide-Band CMOS Wireless Receiver

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***Abstract*—An IF strip for a wireless receiver supports a variable baud rate by changing analog filter bandwidth. Sliding and step adaptive dynamic range are both used at IF to dissipate only the necessary power at prevailing channel conditions. A combination of VGA and PGA is developed for 64-QAM. The total signal processor draws an average of 16 mA from 3.3 V and a peak of 73 mA. The differential input noise is as low as $3.9\text{nV}/\sqrt{\text{Hz}}$, while maximum IIP3 is +22 dBm with respect to 100 ohms.**

***Index Terms*—Author, please supply index terms. E-mail keywords@ieee.org for info.**

I. Introduction

THE complexity of wireless systems increases with the growing power of digital signal processors (DSPs). As complexity grows, smaller form-factor and higher integration become more important, which leads inevitably to a fully integrated receiver (RX). Two main challenges are on-chip image-rejection and wide dynamic range. Image rejection is addressed in detail elsewhere [1], [2]. This paper focuses on the second challenge.

In a wireless RX, the communication channel conditions can vary largely. In most mobile systems, this large dynamic range (DR) must be absorbed by the analog radio; otherwise the A/D and the digital front-end must resolve a very large number of bits. Sigma–delta modulators have been used in narrow-band systems to obtain a very high DR [3]. However, they are not practical in wide-band systems. Therefore, wide DR *analog* circuits are key to the realization of low-power wide-band systems.

This receiver implements adaptive dynamic range in the IF section. Most wireless systems are designed for the worst case; that is, the dynamic range is specified for the desired signal at a minimum detectable level, accompanied by the largest anticipated interferers. In practice, the receiver only infrequently needs this high instant DR. DR is obtained at the expense of a disproportionate rise in power consumption: doubling the power consumed by a circuit lowers its noise floor by 3 dB with constant IP3, thus raising its spurious-free dynamic range (SFDR) by only 2 dB. An important idea here, which has also been noted elsewhere [4], is that providing no more than the required DR at any given time lowers the *average* power consumption.

Section II describes the system that the IF strip was designed for and Section III introduces the idea of adaptive DR. Circuit design of the programmable gain amplifier (PGA), variable gain amplifier (VGA), and filters is discussed in Sections IV and V. Measurements are given in Section VI.

Manuscript received March 15, 2001.

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Publisher Item Identifier S 0018-9200(01)05828-0.

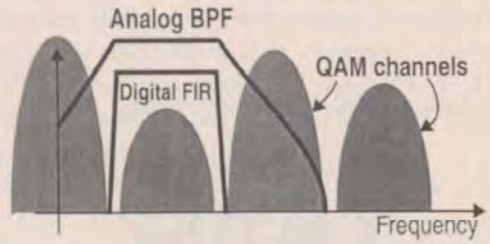

Fig. 1. Complete channel select filter is a combination of the analog BPF and a digital FIR filter.

II. System Description

The basic RX architecture has been described in detail elsewhere [5]. The IF section supports selectable bandwidths (BWs) of 625 kHz, 2.5 MHz, and 10 MHz. The modulation may be 4-QAM, 16-QAM, or 64-QAM. A receiver with adaptive BW requires a fully integrated bandpass filter (BPF). This system uses every channel in each cell [6] to increase the total number of users per cell. With the resulting very small guard-bands, a sharp channel select filter is necessary. It is impractical to implement this entirely as an analog circuit. Instead, following coarse analog filtering, a high-order FIR filter implemented in DSP isolates one channel (Fig. 1).

The 2.4-GHz ISM band does not regulate interferers. Microwave ovens emitting in the middle of the band are often the largest interferer for other users. These considerations call for an RX design with the largest possible DR. This is addressed at two levels: first, with circuits designed for the highest possible DR at a given power consumption, and second, by adaptive use of circuit blocks.

The front-end and image-reject downconversion sections of the RX are described in [5]. Fig. 2 is taken from [7] and shows a block diagram of the RX; the IF section is the main focus of this paper. This section of the receiver follows image rejection, and comprises a prefilter programmable gain amplifier (PGA), bandpass filter (BPF), a post-filter PGA, and finally a continuously variable gain amplifier (VGA). The BPF is usually the bottleneck to DR. The prefilter PGA (PGA1) trades off between the NF and the IIP3 of the IF strip. The BPF attenuates near-by channels and rejects far-away channels. The post-filter PGA + VGA amplifies the signal to 90% of the A/D full scale.

The following sections cover details of the circuit design.

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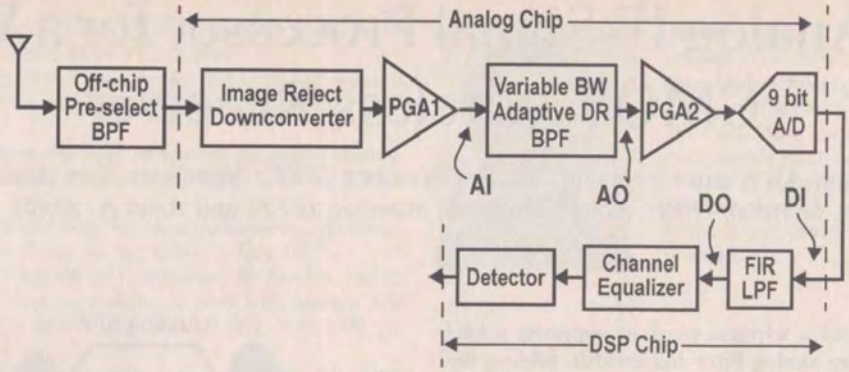

Fig. 2. Block diagram of complete WLAN receiver.

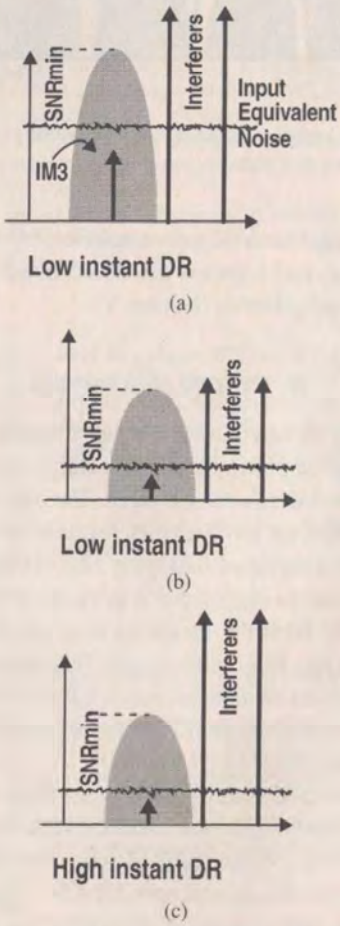

Fig. 3. Three different scenarios for received signals. (a) Strong desired signal. High noise can be tolerated. (b) Weak desired signal and weak interferers. Low linearity can be tolerated. (c) Weak desired signal and large interferers. Low noise and high linearity is required.

III. Adaptive Dynamic Range

In wireless systems, the minimum detectable signal (MDS) and spurious-free dynamic range (SFDR) together quantify the ability of the receiver to detect a very weak desired signal in the presence of strong interferers. A radio signal of interest is received in roughly different conditions. The desired signal may be strong enough to overcome large noise and intermodulation due to nearby interferers [Fig. 3(a)]. In this case, a high receiver NF is acceptable. Alternatively, the desired signal and the interferers are weak, so the signal-to-interference ratio (S/I) is still good (Fig. 3(b)), yet low IIP3 is acceptable. In both cases, the

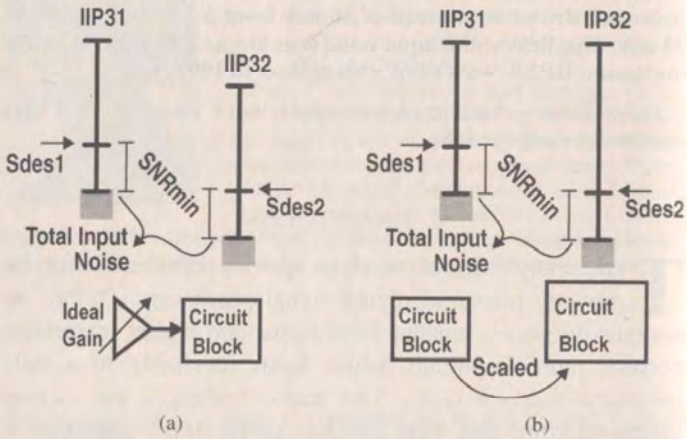

Fig. 4. An illustration of how to achieve: (a) slide DR with preamplification and (b) step DR by substitution of a scaled circuit block.

receiver dynamic range may be modest. The worst-case is when the desired signal is weak but the interferers strong (Fig. 3(c)). Now the instant receiver input signal DR is high, which requires high IIP3 and low NF.

For least power consumption, the RX DR should adapt to the prevailing conditions. Two types of adaptive DR are possible, *sliding* and *step* [Fig. 4(a)]. In sliding DR, the *instant* DR of the RX is constant but slides to best accommodate the input signal conditions. Fig. 4(a) shows how, by adding a gain stage in front of a noisy and nonlinear circuit block, input referred noise and IIP3 drop by the gain of the amplifier. This *slides* down the entire DR and enables detection of a weaker signal accompanied by weak interferers.

Suppose that at some point the receiver needs higher DR. Scaling up all the transistors in a circuit keeping $V_{GS} - V_t$ constant and scaling down all resistors by the same factor lowers input mean square noise and raises bias current proportional to the scale factor, while IIP3 remains unchanged [Fig. 4(b)]. The scaled circuit can pass a weak desired signal accompanied by strong interferers. Thus, DR may be *stepped up* by substituting a scaled version of a nominal circuit.

The circuits comprising this receiver (Fig. 2) use both types of adaptive DR. Assume that the DR and linearity of PGA1 is higher than that of the BPF, while the filter contributes the largest noise at the input. Then the IF strip input IP3 (for interferers in the BPF stopband) can be expressed as

$$\mathrm{IIP3_{IF}}\ (\mathrm{dBm}) = \mathrm{IIP3_{BPF}}\ (\mathrm{dBm}) - \mathrm{Gain_{PGA1}}\ (\mathrm{dBM}). \quad (1)$$

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When the gain of PGA1 is lowered, $\mathrm{IIP3_{IF}}$ is higher. On the other hand, $\mathrm{NF_{IF}}$ also rises due to the dominant noise of the BPF. Thus, lowering gain in PGA1 slides up the DR.

The on-chip filter is usually the bottleneck to achievable DR in a fully integrated RX. In this design, the BPF adapts power dissipation to the instantaneous needs, as shown in Fig. 4(b). Two filters are implemented with the same topology, but one, scaled up to consume 10× more power, offers 10× lower mean square noise but the same linearity. An algorithm described below senses which of the previously described conditions is present. In the first two instances [Fig. 3(a) and (b)], a BPF dissipating low power is employed for nominal RX DR. However, in the worst-case scenario, the high-power scaled filter is switched in raising total DR. Since the worst-case scenario is infrequent, the low-power filter determines the average RX power consumption.

The algorithm to sense the input signal and determine instant DR is key. Signal power is sensed at four points along the IF strip (Fig. 2): input and output of the analog BPF and input and output of the digital channel select filter. These measured signal levels indicate how much of the received signal is being rejected, respectively, by the analog filter and the digital filter.

The signal at the output of the digital filter (point D_o in Fig. 2) is only the desired channel, with possibly some possible IM3 from adjacent interferers. By comparing the signal level at the output of the analog BPF (A_o) and at the input of the A/D (D_{I}), the post-filter gain is measured. Then, by comparing the signal level at the input and the output of the digital filter (D_{I} and D_o), the relative strength of the out-of-channel signal that passes through the analog filter is calculated. The signal level at A_{I} and A_o is a measure of the out-of-band interferers being rejected by the analog BPF. If the *desired* signal at the output of the analog BPF is strong, as measured by $\mathrm{Power_{Do}}$–$\mathrm{Gain_{Post\text{-}analog\text{-}filter}}$, the scenario is as shown in Fig. 3(a). If the total signal power is comparable at A_{I} and A_o, and at D_{I} and D_o, the condition is like Fig. 3(a) or (b). In both cases, the required instant DR is low. If the signal levels are significantly different at either of the above pairs of nodes (A_{I} and A_o and D_{I} and D_o) and there is a weak signal at D_o, the condition must be the one shown in Fig. 3(c).

An abrupt switch from the low-power to the high-power filter causes the BER to increase momentarily. However, as data transmitted in frames is preceded by a preamble and training sequence, the desired filter is switched during the preamble and settles during that time, eliminating increase in bit error rate (BER) during the data sector. If the interference increases abruptly during the data sector to the point that the BER exceeds the limit, that data frame is dropped. This frequency-hopping transceiver uses many adaptive algorithms at each hop, which necessitate a lengthy preamble of typically 300 symbols out of a frame that is 5000 symbols long. Therefore, the turn-around time of a few symbol periods can be tolerated. The actual number of symbols required for the system to settle depends on the channel conditions.

IV. Programmable and Variable Gain Amplifiers

As the received QAM waveform modulates carrier amplitude, it requires linear amplification in the receiver. Two sets of pre-filter and post-filter amplifiers are implemented, with different goals. The pre-BPF amplifier, PGA1, slides the input DR of the BPF to best fit the instant level of the input signal, as shown in Fig. 4(a). As mentioned before, for a weak desired signal where a low NF is needed, PGA1 is set to high gain to overcome the high NF of the filter. When the input signal is strong, PGA1 is set to low gain and high OIP3 to preserve the IIP3 of the BPF. The post-BPF amplifiers boost the signal to optimally load the ADC input (90% of the 1 V full scale). If the BPF could perfectly isolate the desired channel, intermodulation would no longer be a concern in the post-BPF circuits. However, when the analog BPF's selectivity is poor at low BW settings as well as the desired channel, it passes a few adjacent channels, thus, the need for a linear post-filter amplifier.

Amplifier gain may be controlled by varying: 1) transconductance (g_{m}); 2) load impedance; or 3) feedback factor. Bias current sets transconductance. When the input signals are large, the transconductance gain must be low, and simultaneously the intercept point must rise. However, lowering the bias current also lowers the intercept point, which is contrary to what is wanted. Furthermore, as the MOSFET transconductance is at best a square-root function of bias current, the current must change by 100× for 20 dB of change in gain.

Next consider varying gain with the load resistance. If the load is linear, the transconductance amplifier determines both noise and linearity. Therefore, as in the case above, the amplifier DR does not improve when gain is lowered. However, if supply-limited clipping at the output node determines circuit nonlinearity, IP3 improves with lower gain.

Finally, gain may be changed with variable feedback factor. A noiseless feedback block does not affect the equivalent input noise of the amplifier but improves linearity by the loop gain. Therefore, feedback trades off the gain for DR. In this respect, feedback is superior to the methods described above and is used here. In practice, the feedback components add noise of their own that shrinks the improvement in the DR.

A programmable gain amplifier implementing a set of discrete gains may be realized by an array of switch-selectable amplifiers, each optimized for the best DR at fixed gain. By contrast, in a VGA, the gain changes continuously and cannot be optimum over the whole range. For this reason, at a given power consumption and gain range, the DR of a PGA is higher than that for a VGA. Therefore, the PGA should be used in a receiver whenever possible.

The constellation points are very close together in complex modulation schemes like 64-QAM. A sudden variation in gain can easily be mistaken for a change in signal level, and this increases the BER. To avoid this, gain must be stepped in small increments. Fig. 5 shows 64-QAM SNR with PGA gain step [6]. To ensure an SNR of above 40 dB, the gain must be accurate to 0.027 dB. With an 80-dB gain range, this requires 11-bit resolution of PGA gain, which is clearly impractical. On the other extreme, a simple VGA designed to cover 85 dB of gain range dissipates excessive power. The solution is to combine the two.

The best combination is found by exploiting certain features of the system. At the beginning of each hop, the frame starts with a training sequence during which algorithms, such as for carrier recovery, beam forming, clock recovery, and automatic

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gain control (AGC) [6], converge. A jump in gain in this training period does not degrade the BER. Furthermore, the channel does not vary much over the data sector of each frame. Thus, a PGA with a high DR can coarsely set the gain in this time, and during the data sector, VGAs can track the channel variations.

The required VGA range is determined using a channel model. The largest data frame is 5000 symbols, which lasts at most 8 ms at 625 kS/s. Assuming a maximum speed of 2 m/s for the indoor mobile transceiver, an indoor channel model [11] defines the VGA variation to be limited within -14 dB and $+6$ dB for 98% of the time. This needs 20 dB of gain variation in the VGA. The gain range is asymmetric because the system is more prone to ADC overload; thus, the attenuation range exceeds amplification.

A. PGA Circuit Design

The PGAs used in this work all consist of a degenerated differential pair with resistive load. Degeneration improves the linearity of the amplifier and the resistor load alleviates the nonlinearity due to the MOSFET output impedance. The ratio between the nonlinear MOSFET output impedance and the linear load resistor affects overall amplifier linearity, and here limits the maximum gain of each stage to about 15 dB.

As shown in Fig. 6, the local feedback loop gain is changed by switching the degeneration resistor. Although long channel devices do not suffer from excessive noise and their output impedance is large, their large C_{gd} strongly loads the preceding stage and limits the BW. For this reason, all MOSFETs are minimum channel length.

Control switches change the effective degeneration and thus the effective G_m of the stage

$$G_m = \frac{g_m}{1 + g_m R_s} = \frac{g_m}{1 + \frac{2IR_s}{V_{GS} - V_t}} = \frac{g_m}{1 + \frac{2V_{Rs}}{V_{GS} - V_t}} \quad (2)$$

where the term $2V_{Rs}/(V_{GS} - V_t)$ is the loop gain. With a given MOSFET size and bias current (i.e., the same g_m and $V_{GS} - V_t$), the headroom available for V_{Rs} limits the loop gain and therefore the gain range.

Gain is also changed with load impedance, but without tradeoff in linearity. Now headroom limits the maximum gain. In order to increase the gain, part of the dc current is supplied by the current sources to reduce the voltage drop on R_L [Fig. 7(a)]. This method has some advantages over supplying all the dc by current sources and inserting floating resistors reported before [12] [Fig. 7(b)]. With the current source MOSFETs biased at a certain V_{DS}, their output noise current (i_n^2) is proportional to their dc current. Using R_L to supply the main part of the dc current reduces the total noise from the load current source. Furthermore, a lower bias current results in larger output impedance for the current sources and improves the output linearity. Common-mode feedback (CMFB) is applied to the gates of the current source FETs.

Fig. 8 shows the low-power fine-step PGA (LPWstep in Fig. 9) designed to drive the 0.4-pF input capacitance of the BPF. The gain of this stage varies from 3 to 15 dB in 3-dB steps. For 3-dB gain, all the degeneration switches are open (maximum degeneration) and all the load switches are closed (minimum load resistance), whereas for 15-dB gain

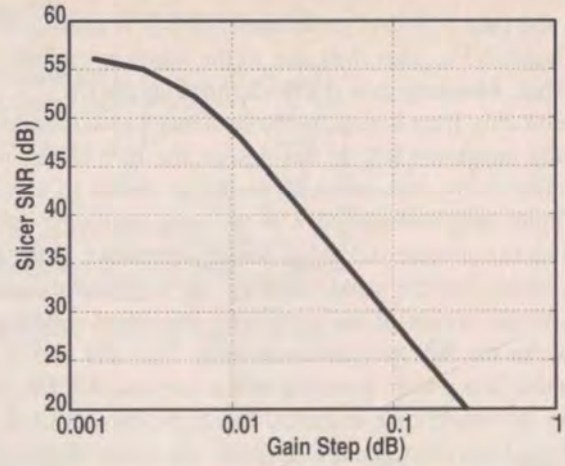

Fig. 5. Detected SNR of 64-QAM bitstream as a function of a gain jump during reception.

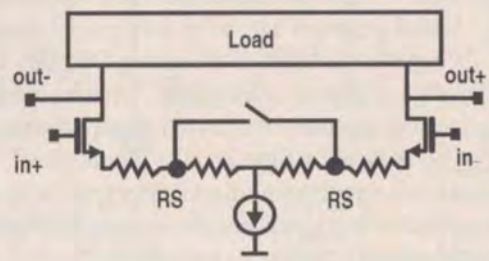

Fig. 6. Switched degeneration with a single tail current source. Voltage headroom limits loop gain.

the switches are in the opposite positions. The high-power low-noise fine-step PGA (HPW step) resembles the circuit of Fig. 8, except it is scaled by factor of 9. The gain of the coarse-step PGA (HPWfix) is 15 dB, and this defines the high gain portion of the fine-step PGA. For 0-dB gain, the amplifier bias current is shut off and its inputs are shorted to its outputs.

The total gain and the bias current of the PGA are set as follows. To overcome the input noise of the low-power BPF, the coarse PGA and two fine-step PGAs amplify the input by up to 30 dB (Fig. 9). The bias current of the PGA blocks is set by two parameters: the required input noise and the filter input capacitance, which is, respectively, 0.4 and 4 pF for the low-power and the high-power versions. The pole frequency associated with the load resistor of the PGA driving the LPF input lies beyond 40 MHz.

The post-filter PGA (PGA2) implements 60-dB gain variation in 3-dB steps, divided among three stages of low-power coarse PGAs and one low-power fine PGA. The HPF function is combined with the PGA function, as will be explained in Section V. Switches sized large enough to drop negligible voltage when in the ON state also contribute negligible noise and nonlinearity.

The gain and noise are related as follows:

$$\text{Gain} \propto G_m, \quad \hat{v}_n \propto \sqrt{\frac{1}{G_m}} \quad (3)$$

where G_m is the degenerated transconductance. Equation (3) assumes that the noise of the input MOSFETs is dominant, which is usually the case in a highly linear low-voltage design. Thus, gain (in dB) decreases twice [illegible] (in dB).

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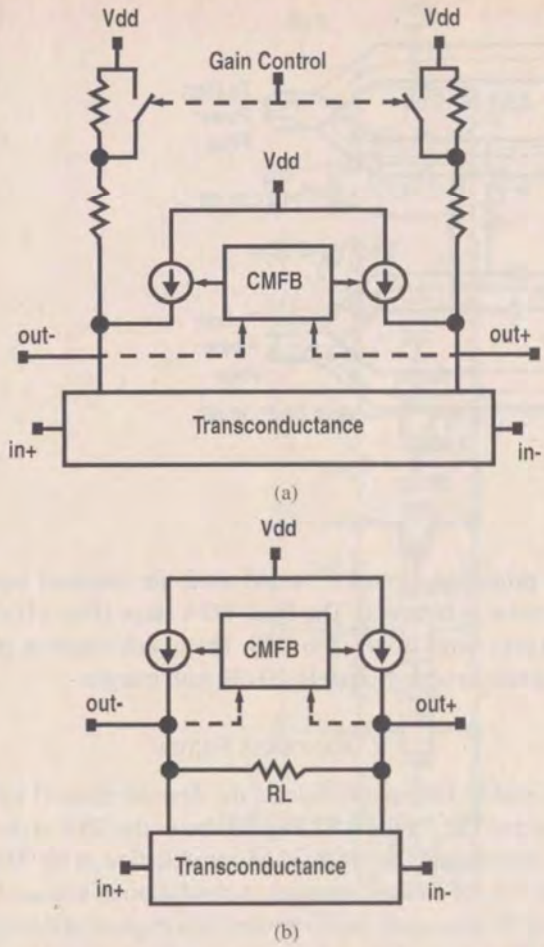

Fig. 7. Biaising alternatives with resistor loads. (a) RL connected to supply. A small part of current is supplied by the current sources. (b) Floating load resistor. All bias current is supplied by the current sources.

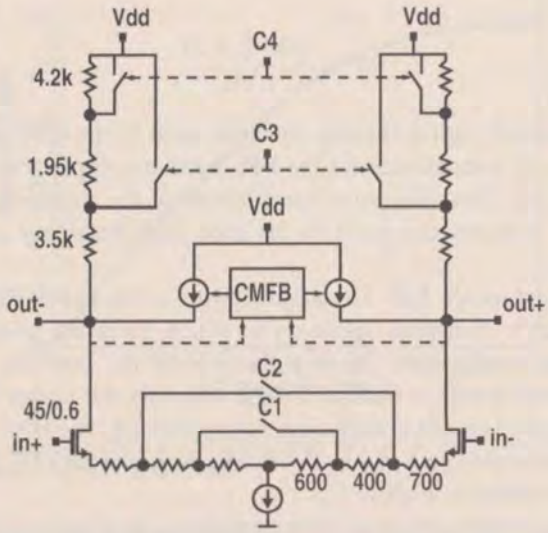

Fig. 8. Fine-step PGA, low-power version.

Short-channel MOSFETs are noisier than long —channel ones [13]. The higher the G_m (weaker degeneration), the higher the noise contributed by the MOSFETs, which leads to a weaker decrease in v_n. On the other hand, as the load resistance is increased, the current sources in parallel with the load must be larger to maintain constant headroom. As a result, their noise contribution and thus v_n increase.

At a constant output swing, feedback lowers amplifier nonlinearity by the loop gain T [14] as

$$\begin{aligned} G_m &= \frac{g_m(\mathrm{OL})}{1+T} \\ \mathrm{IM3(constant\ output\ level)} &= \frac{\mathrm{IM3(OL)}}{1+T} \\ \mathrm{OIP3(input\ limited)} &= \mathrm{OIP3(OL)} \cdot \sqrt{1+T} \\ \mathrm{IIP3(input\ limited)} &= \frac{\mathrm{OIP3}}{\mathrm{Gain}} \\ &= \mathrm{IIP3} \cdot (1+T)^{1.5} \end{aligned} \tag{4}$$

where OL is the open-loop case without feedback. Equation (4) is valid if the input dominates nonlinearity. However, nonlinearity in FET output impedance is not enclosed by the loop. If this is dominant, the resulting OIP3 will be constant. Now we have

$$\begin{aligned} \mathrm{OIP3} &= \mathrm{OIP3(OL)} \\ \mathrm{IIP3(output\ limited)} &= \frac{\mathrm{OIP3}}{\mathrm{Gain}} = \frac{\mathrm{OIP3(OL)}}{\mathrm{Gain}}(1+T). \end{aligned} \tag{5}$$

In practice, at large gains, nonlinearity in the output impedance dominates and produces a constant OIP3. This can be improved with the cascade topology [5].

B. VGA Circuit Design

To continuously vary the gain of the amplifier, a MOSFET in the triode region can be used as voltage-controlled resistor both for degeneration and as the load. However, a MOSFET resistor is nonlinear, especially at low $V_{GS} - V_t$, when a small-signal swing can force it into saturation. Linearity may be improved at the expense of range by padding it with linear resistors either in series or in parallel (Fig. 10).

With parallel padding [Fig. 10(b)], the linear resistor dominates when the MOS r_{ON} is at its maximum, which corresponds to low gain, large input signal, and therefore maximum nonlinearity. Thus, parallel padding is better than series. The correct choice of W/L balances linearity with the net variation in resistance. To achieve a wide range, padded stages are used as shown in the differential configuration of Fig. 11. The resulting structure has been termed soft switching [15]. In each stage, the worst-case linearity appears when the MOSFET is turned OFF. The resistors should be turned OFF one by one. In a previous circuit [15], a supply voltage of 5 V was dropped across the various nodes and one control ramp voltage applied to all the gates turned off the FETs successively. In a low-voltage design, however, the voltage drop is low and the MOSFETs will tend to turn off together. Here a resistor ladder generates six staggered voltages from a single control signal (Ext_cont). By properly selecting the resistor values, the decibel gain can be made linear with Ext_cont (V).

In addition to its use for degeneration, the soft-switched variable resistor (SSVR) may also be used for the load. Now $\mathrm{IIP3_{VGA}} = \mathrm{IP3_{SSVR}} - \mathrm{Gain_{VGA}}$ (dB). Since $\mathrm{Gain_{VGA}}$ is higher than 0 dB, this limits the $\mathrm{IIP3_{VGA}}$. If used as degeneration, the input signal is divided between the input transistors and the SSVR. Furthermore, at high gain settings, the input

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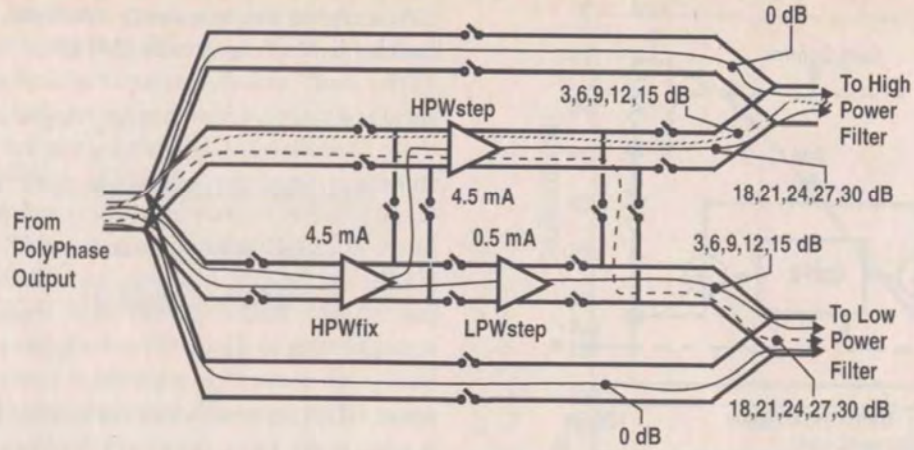

Fig. 9. Combination of PGA stages realizing PGA1.

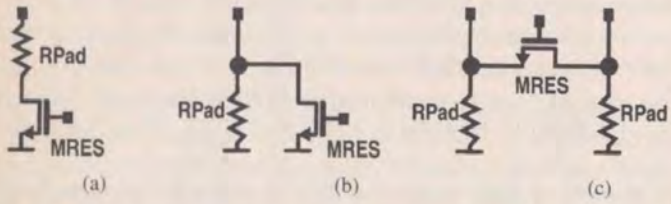

Fig. 10. Illustrating degeneration by: (a) serial resistor padding, (b) parallel padding and (c) parallel differential padding.

swing is lower than the output swing. Thus, on considerations of linearity, SSVR is better suited to degeneration.

This differential circuit does not use constant current bias. Simulations show that removing the tail current source improves linearity by up to 10 dB. The MOSFET resistor can be used floating or grounded. Although the floating SSVR has 0 dc voltage drop and higher linearity, with grounded SSVR, the dc path changes, and so does the dc current. For low-voltage applications, the change of bias due to the grounded MOSFET resistors is desirable. In this design, a combination of both has been used. In Fig. 11, as cont1 rises to increase the gain, the voltage of node 1 decreases, providing higher voltage drop on the other resistors.

The variable transconductance section of the VGA with SSVR degeneration is designed as follows. First, a bias voltage is chosen at the input (V_{IP} and V_{IN}) as dictated by the preceding stage, or for highest linearity. Then the length of the input FETs is selected either from considerations of excess noise in short channel FETs, or from the maximum tolerable capacitance at the input. Next, the $V_{GS} - V_t$ is selected for the desired linearity by setting the fixed degeneration resistor. For a degeneration stage with constant input bias voltage, higher $V_{GS} - V_t$ results in weaker degeneration and lower linearity, but higher G_m/I_{bias}. The degeneration element consists of fixed linear resistors, in series with a floating differential MOSFET resistor. The FET W/L is chosen to be the largest that gives the required linearity. The worst-case scenario is when the MOSFET is close to the OFF. The top half resistor (the linear resistor between the MOSFET resistor and input FETs) is divided into two parts and another MOSFET resistor is inserted at the new middle node. This procedure is repeated until the required variation range is obtained.

The prototype circuit is scaled until the required input referred noise is obtained. The final VGA stage [Fig. 11(a)] provides a gain range from -1 to 8 dB. Three such stages in cascade give a gain variable from 0 to 20 dB with margin.

V. Bandpass Filter

The analog BPF partly selects the desired channel to lower the required DR for the A/D. Fig. 12 shows the SNR at the input of the demodulator for a 64-QAM constellation, with 90% A/D loading [6], for a single channel. A resolution of at least 8 bit is required. If the out-of-band channel power passing through the A/D (I) is comparable to or larger than the desired signal (S), then the A/D must resolve the following number of additional bits to accommodate the interferers, which is roughly:

$$N = \frac{\text{Int}\left(\frac{I}{S} + 3\right)}{6 \text{ dB}}.$$

A powerful digital channel equalizer used in the DSP, shown in Fig. 2, compensates for the BPF passband ripple and group delay [6]. This relaxes the specification of the analog filter. A g_m–C realization is used for its good high-frequency performance.

A high-order LPF is cascaded with a low-order HPF for symmetric transition regions [7], which gives the minimum power consumption. To vary the BW of the resulting BPF, the lower cutoff is fixed at 5 MHz and only the higher cutoff frequency is tuned to define the filter passband. The HPF offers programmable gain of 0 to 45 dB. The details of the BPF design are presented elsewhere [7].

Fig. 13 shows the post-filter amplifiers. The first three blocks are a PGA-HPF, which give a coarse-gain variation of 0 to 45 dB in steps of 15 dB. Next, a fine-step PGA increments gain in 3-dB steps up to 15 dB. Finally, three VGA stages in cascade provide 27 dB of continuous gain variation prior to the A/D.

VI. Standalone IF Strip Implementation and Measurement Results

The IF strip was implemented in a 0.6-μm CMOS process and operates at a 3.3-V supply. First, the PGA blocks (Fig. 9) are

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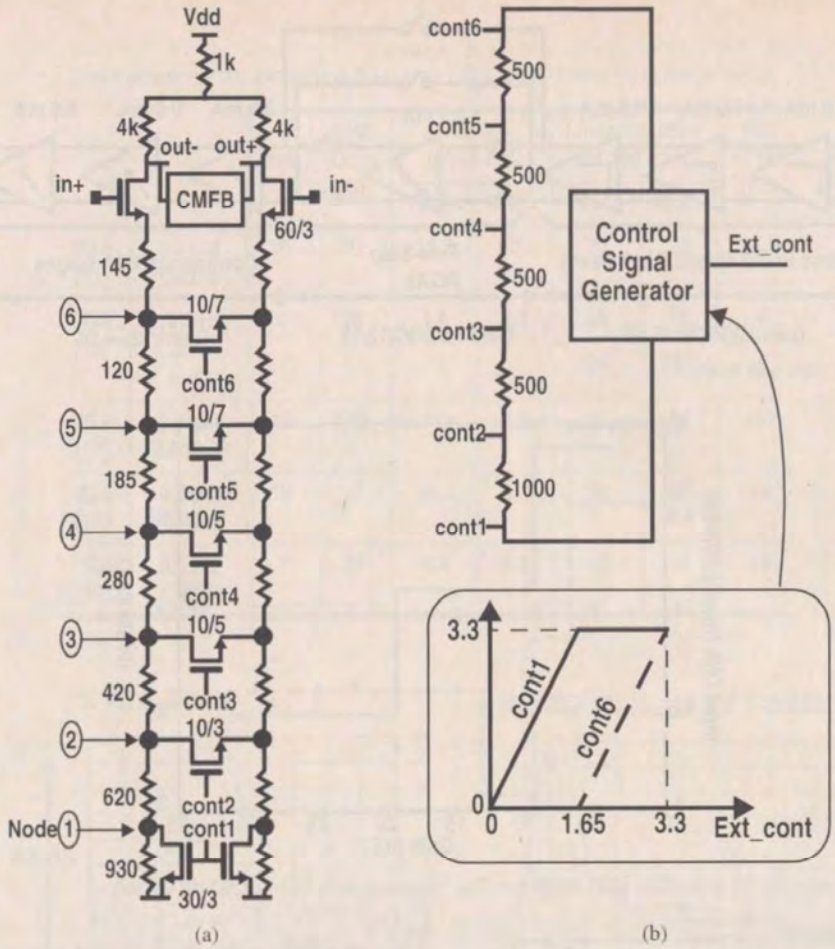

Fig. 11. (a) VGA circuit using soft-switched degeneration. (b) Resistor ladder and control voltages.

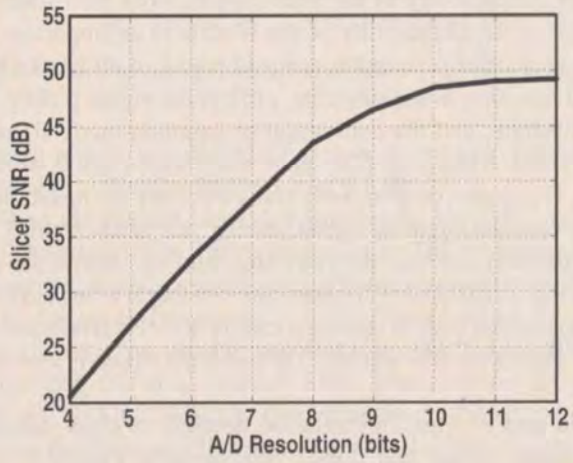

Fig. 12. Detected SNR of a 64-QAM signal versus A/D resolution, assuming signal loads A/D 90% at the peak.

experimentally characterized. Fig. 14 shows the OIP3 and the differential input referred noise of the PGA1. The low-power fine-step PGA (LPWstep) is the same one as in Fig. 8. Since the measured OIP3 versus gain is almost constant, it may be concluded that output impedance nonlinearity dominates. The input noise decreases due to the growing transconductance as the gain rises from 3 to 9 dB. For 12- and 15-dB gain settings, load resistance is stepped up, as is the current through the output current sources (Fig. 8). Now current source noise raises the total input-referred noise of the stage.

Fig. 15 plots the gain of one VGA stage biased at 0.6 mA versus the input control voltage. The gain (in dB) is fairly linear with $V_{\mathrm{Cont}}(\mathrm{V})$, with a peak deviation of 0.4 dB. The input noise and OIP3 of the VGA is shown in Fig. 16. The noise is very close to simulations, however, the OIP3 is about 4 dB lower than expected mainly due to the shortcomings of the BSIM2 models used. Table I compares the result of this design with recent published works. The characteristics of this work are scaled to match the gain and the power consumption of each reference circuit by cascading the required number of stages and scaling the resulting circuit for power. Except for the model in [16], the designed VGA and PGA surpass the others in DR. The circuit in [16] has lower noise due to high g_{m} bipolar transistors, but it requires a high supply voltage.

The low-power and high-power LPFs drain 6 mA and 60 mA from the supply, with 50 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ and 17 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ differential input noise, respectively. Since switched capacitors control filter bandwidth, the g_{m} variation is not very large. The input noise density is therefore almost independent of the BW. The in-band and stopband IIP3 of both LPFs are 18 and 22.5 dBm (referred to 100 Ω differential) respectively. They are measured for a BW of 10 MHz, with two tones of 10 and 11 MHz for in-band IIP3. For stopband IIP3, two sets of tones were used, 30/50 MHz and 40/70 MHz. Each stage of the PGA-HPF consumes 1.8 mA, with 40 and 7.9 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ noise for 0- and 15-dB gain respectively. The OIP3 of the PGA-HPF for in-band and out-of-band interferers is 28 and 24 dBm (referred to 100 Ω) respectively.

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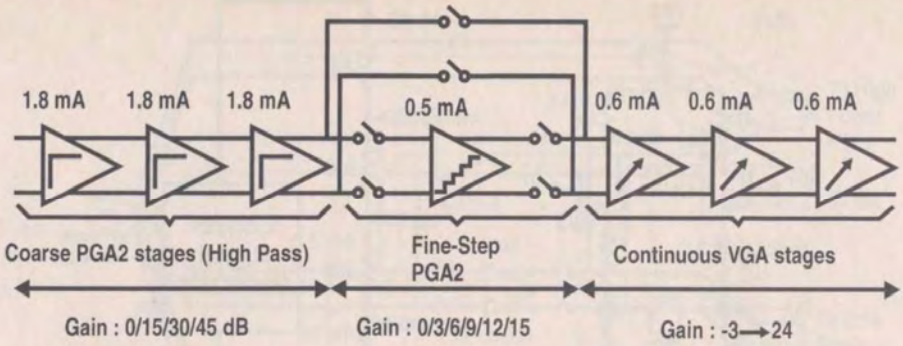

Fig. 13. Post-filter PGA2 with HPF, and VGA.

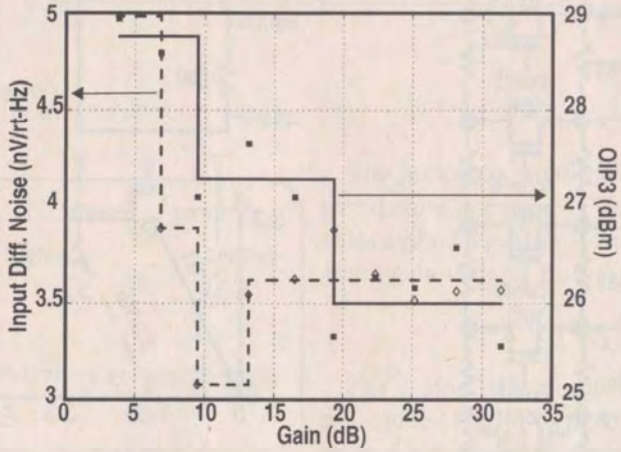

Fig. 14. Measured noise and output of IP3 of prefilter PGA (shown in Fig. 9) versus gain, when LPWstep is used.

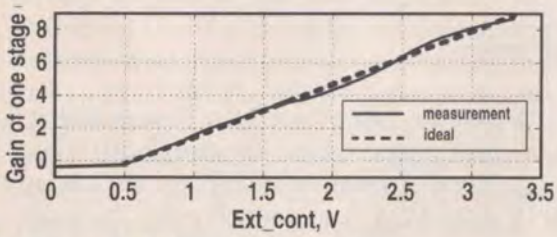

Fig. 15. Gain of one VGA stage versus control voltage.

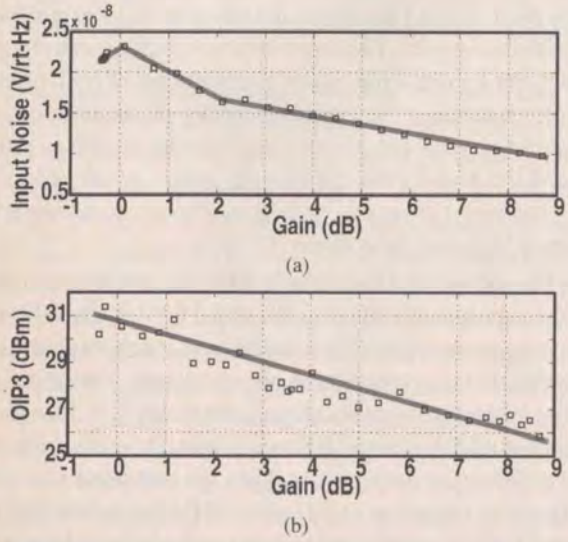

Fig. 16. (a) Noise and (b) output IP3 of one VGA stage versus gain.

Since the transconductance stages used in the filters do not have any common-mode rejection, mismatch between two sides of the transconductance stages causes common-mode to differential conversion. Now noise on the substrate and supply can appear differentially at the filter output. With post-filter gain as high as 83 dB, stability of the IF strip is an important concern. Very careful common-centroid layout of all blocks limits signal injection to the substrate, differential signal pickup from the substrate, and the conversion of common-mode signals to differential. Total post-filter gain was varied from 0 to 83 dB [Fig. 17(a)] on the packaged test chip with no instability. A small constant input is applied during this measurement on a network analyzer, and the filter stopband lies below the noise floor. Fig. 17(b) (from [7]) shows the variable BW in the IF strip. The passband ripple in the worst case of 10 MHz BW is less than 3 dB. For lower BW settings, the passband ripple is less than 1 dB.

Two sets of measurements are devised to show adaptivity in dynamic range and power consumption. First the output SNR_{min} at 1.6 Vptp differential output is set to 14 dB for a 625-kHz-wide channel. As the BPF significantly attenuates interferers lying in its stopband, linearity of the post-filter blocks is not important. At minimum detectable input signal [Fig. 18(a)], the input NF should be as low as possible. With weak interferers, prefilter gain is set to maximum (30 dB) to overcome filter noise. Strong interferers will generate in-band IM3 products. The interferers are made stronger, the IM3 components rise, and, when the interferer tones are at −42 dBm, the distortion products are equal to the input equivalent noise. Since the filter limits overall IIP3, the gain of the prefilter amplifier is lowered to improve linearity. However, this increases the NF at the input and will degrade SNR of the desired signal, but

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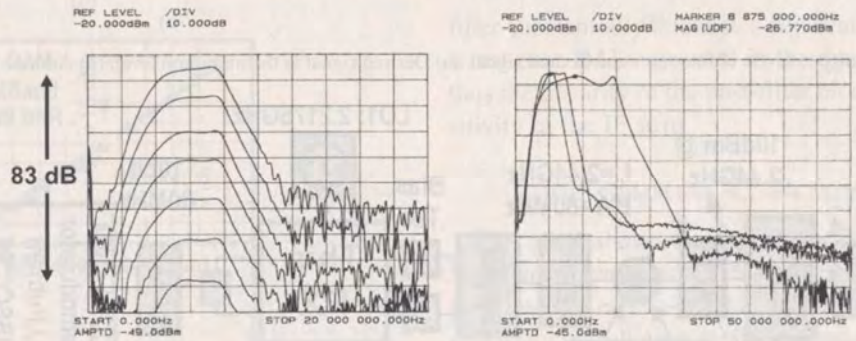
TABLE I
COMPARISON OF THE DESIGNED PGA AND VGA WITH OTHER PUBLISHED WORKS

		mA	MHz (Ours 50)	Noise (nV/rt-Hz)		Linearity (dBm wrt 100 ohm)		Rel SFDR (dB)
				Theirs	Ours	Theirs	Ours	
VGA [11]	0.6 μm CMOS	10	20	12.7	7	20	22	+4.8
VGA [16]	12 GHz BJT (5 V)	8	35	1.6	4.7	30	26	-8
						24	25.5	-5
VGA [17]	0.6 μm BiCMOS	12	200	1.9	5.1	-3	24	+12
VGA [18]	0.6 μm CMOS	10	10	25.8	4.2	28	26	+9
PGA [19]	0.6 μm CMOS	2	71	5.4	9.7	-3	14	+8



(a) (b)

Fig. 17. IF strip frequency response: (a) when changing post-filter gain by 85 dB and (b) at the three BW settings.

the high-power, low-noise LPF is now activated to improve the instant DR of the IF strip by about 6.5 dB.

When the desired input signal is larger, the DR must slide to the best level. Fig. 18(b) shows sliding DR for progressively larger input signals, when higher NF due to lower prefilter gain can be tolerated. For example, if the desired signal rises from -92 to -88 dBm, the NF can rise from 9.5 to 13.5 dB while maintaining the same detector SNR. Thus, for the low-power LPF, the prefilter gain can drop from 30 to 21 dB, which increases the IF strip IIP3 from –8.6 to 0.4 dBm. For the high-power LPF, gain can drop from 21 to 9 dB which raises the IF strip IIP3 from 0.4 to 12.4 dBm.

When the desired signal is higher than -70 dBm, a satisfactory SNR is obtained even with 0-dB prefilter gain. Now IIP3 is the highest possible (22.5 dBm). Using the low-power LPF, the receiver SFDR is higher than 70.5 dB. Two-tone interferers as large as -70 dBm + 70.5 dB = +0.5 dBm may be tolerated at the input to the IF strip. There is no need to switch in the high-power LPF.

Next, consider a desired channel of 625 kHz BW at the input to the IF strip, accompanied by strong nearby adjacent channel interferers which are only mildly attenuated in the analog filter. If the interferers are stronger than the desired signal, after amplification they will occupy the A/D input full scale. Since the quantization noise relative to the total peak signal at the input of the A/D is constant, this degrades the SNR for the smaller desired signal. In general, the signal-to-quantization-noise ratio is

$$\mathrm{SNR}\left(\frac{A}{D}\mathrm{Output}\right) = 6.02N + 1.8 - \text{Rel Crest Factor} - \text{Margin} + \text{OSF} \tag{6}$$

where relative crest factor is with respect to a single tone. The two first terms represent Full scale/$N_{\text{Quantization}}$ [20]. The maximum possible signal corresponds to a dc input at full scale. However, SNR is calculated with the rms signal, which is always less then the peak for non-dc waveforms. The Crest Factor, defined as the ratio between the peak value and the rms of a waveform, takes this into account. To avoid A/D overload, the peak signal is usually set less than the A/D full scale, which is the Margin. The quantization noise has a flat spectral density from DC to $f_s/2$. Increasing the sampling rate beyond the Nyquist rate by the oversampling factor (OSF) lowers the in-band quantization noise.

In the scenario being examined, two-tone interferers pass through the filter with little attenuation and are amplified by the AGC to 90% of the full scale of the 8-bit A/D. To avoid aliasing of the bandpass signal, the sampling frequency must

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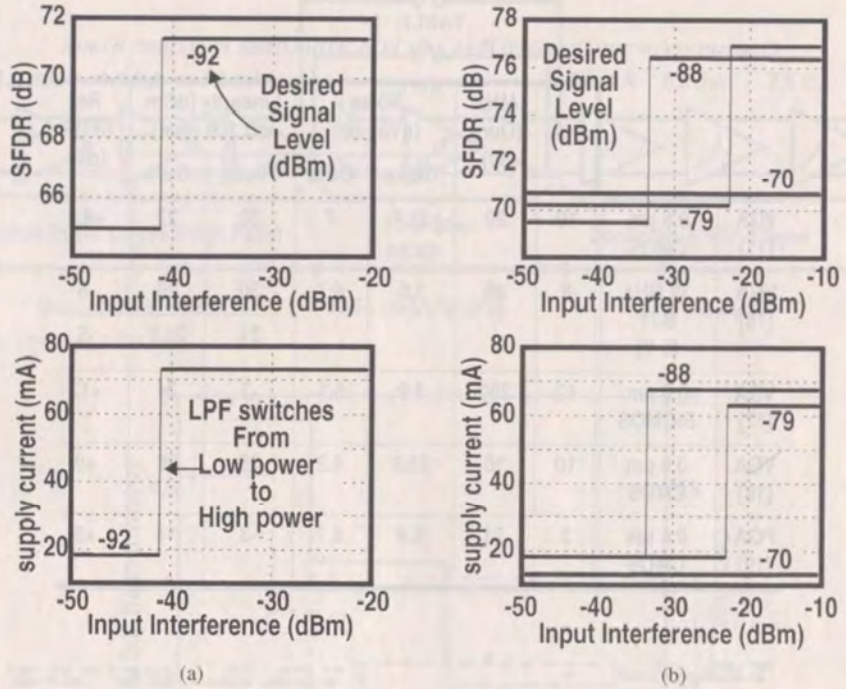

Fig. 18. Adapting dynamic range to levels of interferer and desired signal. (a) Desired signal at the minimum level. (b) At three levels of the desired signal.

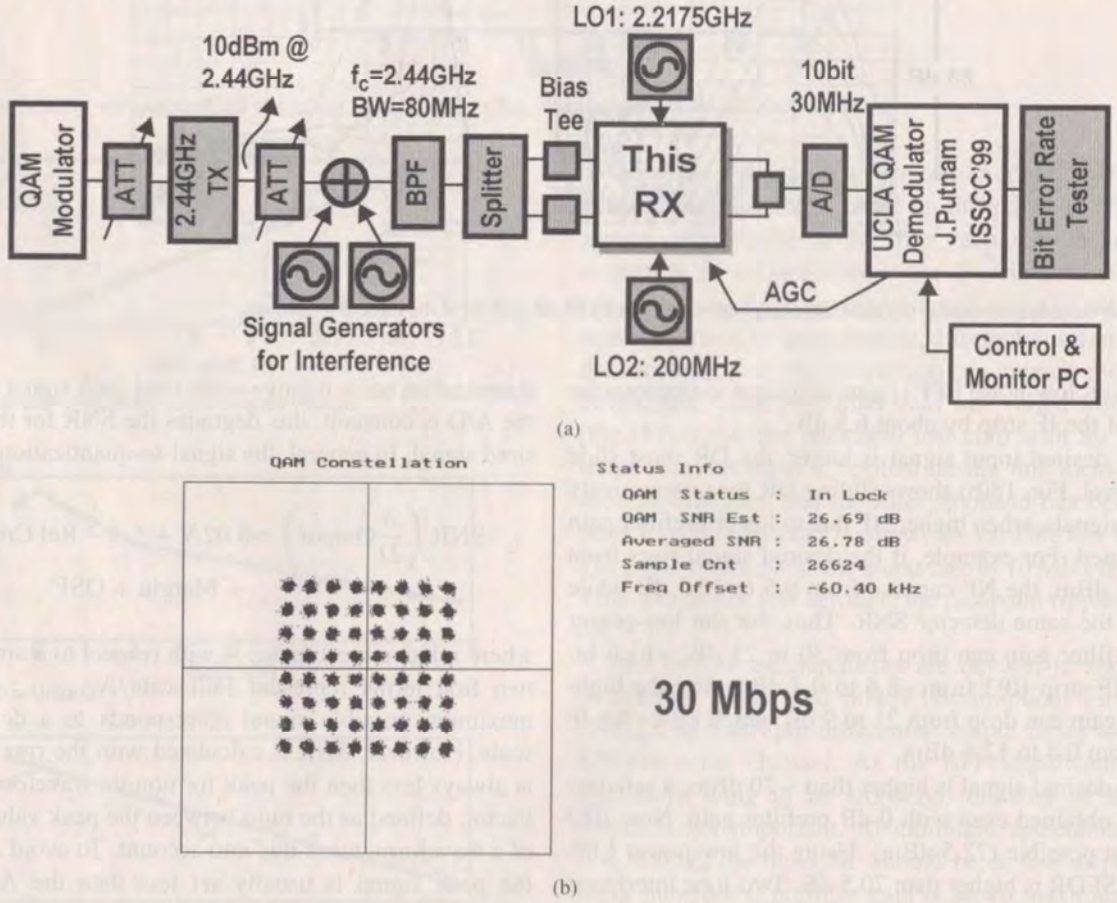

Fig. 19. (a) RX measurement setup. (b) Measured 64-QAM constellation at the baseband.

be $4 \times (5\text{ MHz} + 625\text{ kHz}/2) = 21.25$ MHz. For two equal sinusoids at different frequencies, we have

$$\text{Rel Crest Factor} = 20\log\left(\frac{\text{Peak of Two Tones}}{\text{RMS of Two Tones}}\right) - 3\text{ dB} = 3\text{ dB}.$$

Thus,

$$\text{SNR}\left(\frac{A}{D}\text{Output}\right) = 6 \times 8 + 1.8 - 3 - 20\log(0.9) + 10\log\left(\frac{\frac{21.25}{2}}{0.625}\right) = 58.2\text{ dB}$$

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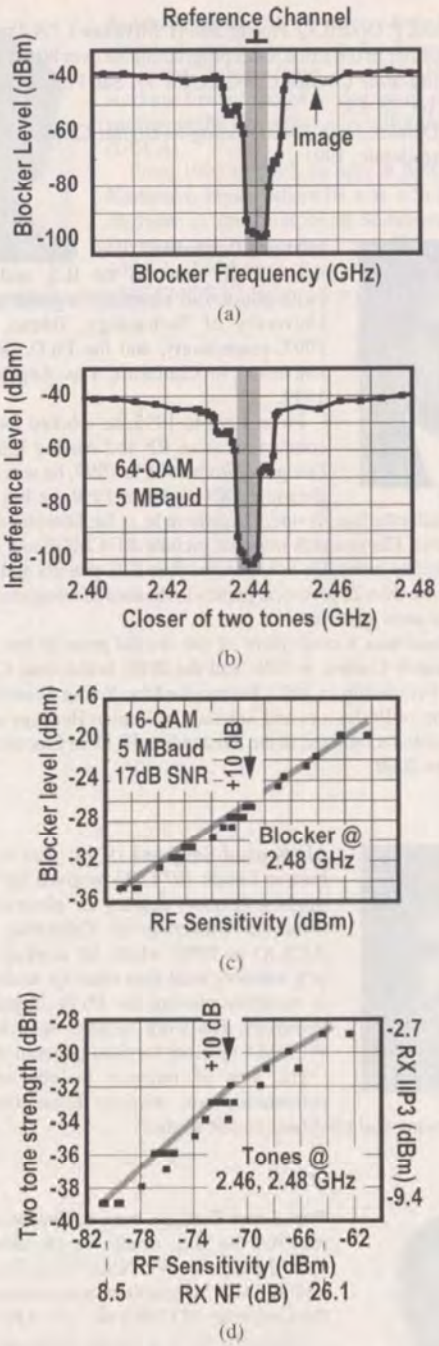

Fig. 20. Complete receiver measurements. (a) Single-tone blocker strength at various frequencies which desensitizes receiver by 3 dB. (b) Two-tone strength which desensitizes receiver by 3 dB because the intermodulation product lies on the reference channel. (c) Sensitivity versus blocker strength as the IF section adapts. (d) Sensitivity versus IIP3 as the IF section adapts to two in-band tones.

If the last VGA, whose OIP3 is 27 dBm, amplifies each tone to the maximum level of -1.5 dBM, the output node will dominate the nonlinearity. Thus, IM3 with respect to the peak power is $-2 \times (27 - (-1.5)) = 57$ dB. In this extreme case, the poor close-in rejection of the analog BW degrades the sensitivity of the IF strip by only $58.2 - 57 = 1.2$ dB. Assuming 4-QAM modulation with $\mathrm{SNR}_{\min} = 13.5$ dB, the DSP is able to demodulate a desired signal lying $57 - 13.5 = 43.5$ dB below the interferer level.

When the channel bandwidth is 2.5 MHz and 10 MHz, the SNR at the output of the A/D drops to 55.9 and 51.9 dB, respectively, due to the lower oversampling ratio. In these cases, the filter substantially attenuates adjacent and farther channels, the worst-case IM3 stays well in the quantization noise floor, and thus the linearity of the post-filter blocks does not limit the sensitivity of the IF strip.

TABLE II
COMPLETE RX PERFORMANCE

NF	8.5 dB, min
IIP3	-9.4 dBm to -2.7 dBm
Channel BW	625 kHz, 2.5 MHz, and 10 MHz
Max throughput	50 Mbps (with 64-QAM)
Inband ripple Stopband rejection	0.5 dB , 2.5 dB 53 dB , 65 dB
Image Rejection	>75 dB for RF mixer 60 dB for IF mixer
Max RX voltage gain	115 dB
Bias Current	50 mA, Average 100 mA, Peak
Supply Voltage	3.3 V
Process / Area	1P3M, 0.6 μm CMOS / 20 mm^2

VII. COMPLETE RX MEASUREMENT RESULTS

Fig. 19(a) shows the measurement setup for the whole RX. Separately developed QAM modulator and demodulator chips were used for end-to-end data transmission. Fig. 19(b) shows the received constellation at the baseband for 64-QAM, 5-Mbaud signal at a BER of 10^{-6}. In this case, with -71.5 dBM input power the total NF of the RX is deduced to be 8.5 dB.

Interferer measurement results are shown in Fig. 20. The interferer levels shown desensitize the receiver by 3 dB in the desired channel. Fig. 20(a) plots the blocker tolerance level. It shows that the on-chip filter largely suppresses the blocker. The blocker tolerance at image frequency is only 2 dB worse than the other side of the BPF, proving the effectiveness of the on-chip image rejection. Fig. 20(b) shows the two-tone test results and the frequency axis corresponds to the closer tone. Fig. 20(c) and (d) show the effect of the sliding DR in the RX. Dots are the measurements for various gain combinations of RF mixer, first IF amplifier [5], and prefilter PGA. By decreasing the gain in the path, the blocking immunity and linearity of the RX increases, and so does the NF. When the input signal is strong, the high NF can be tolerated. For instance, if the input desired signal is 10 dB higher than the sensitivity level, the blocking tolerance improves by 10 dB and the IIP3 improves by about 5 dB. The IIP3 of the RX ranges from -9.4 dBM to -2.7 dBM and the blocker may be as large as -20 dBM. Table II summarizes all the RX performance.

VIII. CONCLUSION

An IF strip is implemented in a 0.6-μm CMOS for a wireless RX. The active filter in the IF strip supports various baud rates. The dynamic range adapts to the prevailing channel condition by selecting one of the two vers[illegible] lower or

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low-noise. A BPF realized by an LPF in series with HPF lowers power consumption. A combined VGA and PGA provided the optimum solution for a packet 64-QAM modulation. Adaptation using a sensing algorithm that switches either gains or circuit blocks is shown to significantly improve the RX dynamic range without increasing average power consumption. A complete receiver consisting of the IF strip integrated with the RF front-end has been evaluated using end-to-end BER measurements with 64-QAM. Cascade NF of the receiver is 8.5 dB at maximum sensitivity, and cascade IP3 is -2.7 dBm with respect to 50 Ω at maximum linearity.

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A Broad-Band Tunable CMOS Channel-Select Filter for a Low-IF Wireless Receiver

Farbod Behbahani, Weeguan Tan, Ali Karimi-Sanjaani, *Student Member, IEEE*, Andreas Roithmeier, and Asad A. Abidi, *Fellow, IEEE*

***Abstract*—This paper presents a broad-band bandpass filter (BPF) designed as a channel-select filter for wireless applications. It is implemented as a low-pass filter (LPF) in series with a high-pass filter (HPF) for lower power consumption compared to true BPF. Semiscaling of the filter nodes is superior in the wireless receiver over traditional full scaling. The HPF is built with low-pass feedback of an amplifier. The bandwidth is selectable from 625 kHz, 2.5 MHz, or 10 MHz. The filter stopband loss is more than 50 dB extending beyond 100 MHz, and passband ripple less than 2.5 dB. Fabricated in a 0.6-μm CMOS process, it provides a minimum input noise of 16 nV/$\sqrt{\text{Hz}}$ noise with 22.5-dBm out-of-band IIP3, while draining an average 14 mA from 3.3 V.**

***Index Terms*—Bandpass filters, CMOS analog integrated circuits, radio receivers, transconductance-capacitor filters, wireless LAN.**

I. Introduction

FREQUENCY-DIVISION multiple access wireless systems allocate different frequency bands to various applications [1]. Each band contains many channels, from which a given user is assigned one channel. The preselect radio-frequency (RF) filter before the receiver passes all these channels. Then, a sharper channel-select filter in the intermediate-frequency (IF) section isolates the desired channel for demodulation or detection. An off-chip passive filter may be used for this purpose for its high selectivity and wide dynamic range, but at the expense of power consumption in the driving circuits. Also, the receiver (RX) is no longer fully integrated, and one or more filters take precious board space. Furthermore, the fixed bandwidth in a passive filter precludes bandwidth (BW) adaptation.

On-chip active filters, on the other hand, consume power and chip area and limit overall RX dynamic range. Nevertheless, they enable high integration and BW adaptation. The main specifications of an on-chip active filter in a wireless receiver are: 1) its frequency response, including the passband ripple, stopband attenuation, selectivity, and group delay; 2) its dynamic range, including the noise and the linearity; 3) its current drain or power consumption; and 4) the chip area. The linearity of wireless building blocks is usually defined by the third-order intercept point of the (IP3) rather than total harmonic distortion.

Manuscript received December 7, 1999.

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Publisher Item Identifier S 0018-9200(00)02659-7.

The channel-select filter must suppress adjacent and all other channels sufficiently to pass only the desired signal to the detector. In most modern wireless systems, it is realized with some combination of analog and digital filters. If there were no analog filtering, the desired signal at the input of the analog-to-digital converter (A/D) will be accompanied by all the other channels in the band, in particular large adjacent channels, which will later be removed in the digital filter. The large interferers, which are eventually of no interest, raise the required resolution of the A/D. In the special case of narrow channels, it is possible to digitize a wide band with a large dynamic range using a bandpass $\Sigma\Delta$ A/D and a large oversampling factor [2], [3]. For example, in [2], an 8-kHz desired channel and adjacent channels are sampled at 16.8 MHz with a peak signal-to-(noise + distortion) ratio of 98 dB. However, for wide-band applications, a large oversampling factor requires impractically high clock rates and is not feasible. Therefore, most interferers must be removed prior to A/D conversion. On the other hand, the sharper the analog filter, the higher the required pole-Q's, and the lower its dynamic range at a given power consumption [4]. An important design tradeoff is how to divide the total required filtering between the analog and the digital sections for best performance. In applications requiring very high selectivity, the optimum lies with partial channel selection in the analog section, followed by a highly selective digital filter.

This paper describes the design and implementation of a variable-BW bandpass filter (BPF). Section II describes the filter structure and Section III covers the optimum transconductance design for our application. Low-pass filter (LPF) and high-pass filter (HPF) design are discussed in Sections IV and V, and Section VI describes solutions to some common-mode feedback problems. The frequency and Q control loops are explained in Section VII. Last, the experimental results are given in Section VIII.

II. Filter Structure

This paper presents a variable BW BPF designed for a fully adaptive wireless local-area network (WLAN) system. The main concern was to integrate as many functions as possible. Fig. 1 shows the block diagram of the RX. The passband is selectable as one of 625 kHz, 2.5 MHz, and 10 MHz, with a stopband that exceeds 100 MHz. The RF preselect filter attenuates incoming signals farther than 100 MHz away from the desired channel. An attenuation of at least 50 dB is desired across the filter stopband. Unlike many wireless systems which use every other channel in a cell, our system uses every channel

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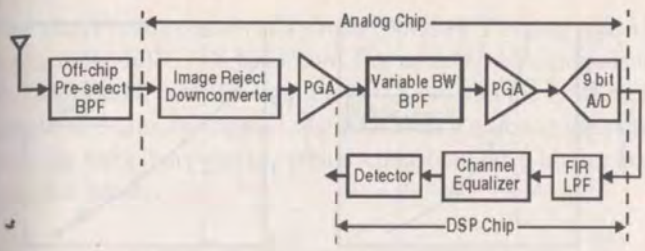

Fig. 1. Block diagram of receiver, showing location of analog filter.

[5] for maximum capacity. To adequately reject the adjacent channel, the filter must be of high order, very likely with high-Q poles. These poles boost filter noise and limit the dynamic range (DR) of the entire RX [4]. Therefore, the analog filter is implemented for partial channel selection, mainly to relax the required A/D DR. A high-order finite impulse response (FIR) digital filter, itself consuming a reasonable power and chip area in the baseband digital signal processor, subsequently isolates the desired channel [5].

With the same BW and selectivity, the higher the filter center frequency, the larger the pole Q's. This translates to higher power consumption for a given dynamic range [4]. Therefore, the filter center frequency should be the lowest possible. A center frequency of 10 MHz was chosen for a bandwidth of up to 10 MHz, which results in a passband spanning 5–15 MHz. A polyphase filter preceding the BPF rejects the image after downconversion over this band [7]. The lower its bandwidth, the more selective an LPF in absolute frequency. Therefore, the lower edge of the filter passband is fixed at 5 MHz for all bandwidths. This also positions the channel of interest beyond the $1/f$ noise corner in the filter. The filter center frequency, which defines the receiver IF, now changes with channel bandwidth.

G_m-C filters are well suited to high frequencies. Accurately modeled parasitic capacitances may be absorbed in the natural grounded capacitors in the filter. This filter is realized as a G_m-C circuit. Like every integrated continuous-time filter, it too requires a tuning loop.

The textbook approach prescribes synthesis of a bandpass (BP) filter from a low-pass (LP) prototype using the bilinear transform. This works well for narrow-band filters [6]. However, when the BW is comparable to the center frequency, such as here, the LP to BP transformation results in a much sharper lower transition (Fig. 2(a)). This is disadvantageous in an active filter, because the associated high-Q poles boost the filter noise at the lower end of the passband. As interferers entering a wireless receiver are equally likely to lie above or below the channel of interest, the upper and lower transition bands should be symmetric. This is realized with an LPF in cascade with an HPF [8], implemented here as a fifth-order elliptic and a third-order Chebychev filter, respectively, to obtain the desired characteristics. Whereas the textbook LP to BP transformation results in an eighth-order bandpass elliptic filter with two conjugate pole pairs of $Q = 7.8$, the largest pole Q in the LPF is 6.9, and 1.3 in the HPF. For a given noise floor, this saves 40% in power consumption compared to a true bandpass filter.

The lower and upper cutoff frequencies may be independently adjusted in the cascade. The HPF fixes the lower edge of the

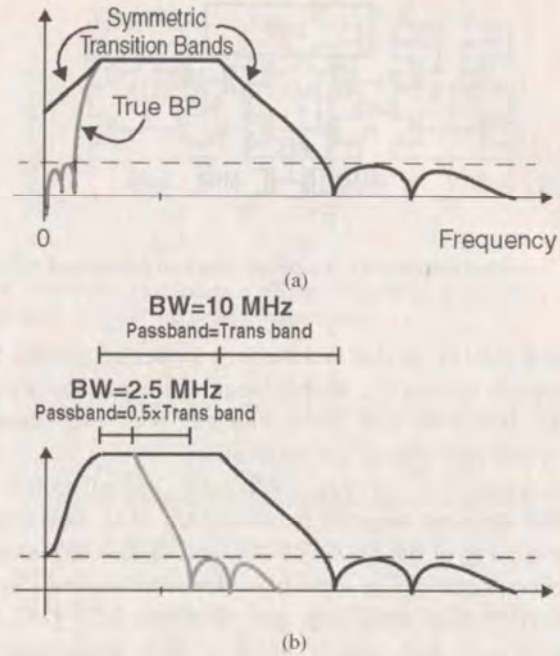

Fig. 2. (a) Broad-band bandpass filter synthesized from cascade of low-pass and high-pass, compared with true bandpass (gray). (b) Selectivity of cascade BPF is worse at lower bandwidths.

passband to 5 MHz, while the LPF adjusts the overall BW with it upper cutoff [Fig. 2(b)]. If the LPF is designed for the desired selectivity at maximum bandwidth, then selectivity will worsen at lower BW's. For instance, in Fig. 2(b), at a BW of 10 MHz, the transition band of the LPF is equal to the passband. When the LPF poles are scaled to a BW of 2.5 MHz, the transition band expands to twice the passband, worsening selectivity by a factor of two. In the extreme case of 625-kHz BW, the transition band expands to 5.625 MHz, which is 9× the BW. As explained later, the transition band in the actual filter is sharper than this.

III. Transconductors with Wide Dynamic Range

The electrical characteristics of the G_m-C filter strongly depend on the G_m circuit. These characteristics are: noise factor, current efficiency G_m/I_{bias}, linearity as measured by intercept point, tuning range, frequency response, maximum signal swing at the input and the output, and dc gain. Limited dc gain generates a pole at the output of a simple G_m-C integrator, which introduces parasitic loss and restricts the maximum pole-Q the filter can implement. Poles and zeros in the G_m stage may generate excess loss or peaking in the filter response [4].

Various transconductor circuits are reported in the literature. The transconductance of a MOS differential pair may be changed with bias current [9]. This method usually does not provide a high linearity, and the tuning range is limited. A MOS resistor may be used as voltage-controlled degeneration [10]. Degeneration improves the linearity of a simple differential pair, but the available triode region of the MOS resistor limits tuning range. At low $V_{\text{GS}} - V_t$, small signals can push the degeneration MOSFET into saturation. For higher linearity, the MOS resistor may be padded with a fixed linear resistor, which now limits the range of G_m variation. An improved version of padded MOS degeneration is called soft switching, first

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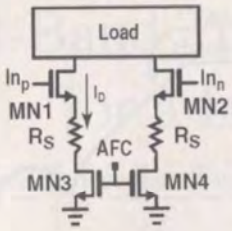

Fig. 3. Variable transconductor (simplified) based on degenerated differential pair.

presented in [11]. In this technique, a ladder of padded MOS degeneration widens G_m tuning range while maintaining good linearity. However, now noise changes with G_m variation, which is not desirable in our application.

Transconductors also use nonlinearity cancellation to improve the dynamic range of the filter [12]–[14]. This requires good modeling of the MOS devices, and cancellation depends on process, temperature, and bias. Transconductors can also be linearized with high loop gain feedback [15], [16], [20]. However, loop gain usually drops at high frequencies and linearity degrades. As the filter may have to remove strong interferers far away from the passband, the resulting poorer IP3 at high frequencies is undesirable.

A. Transconductance Core

The transconductor used in this filter employs variable wide-band resistor degeneration (Fig. 3). MOS resistors MN3 and MN4 operate in the triode region as voltage-controlled degeneration, and are padded with linear resistors in series to improve linearity. To understand this circuit, first consider a MOSFET degenerated by a linear resistor R_s. With constant output signal, the linearity improves by the loop gain $(1+T)$

$$1+T = 1 + g_{mN}\cdot R_S = 1 + \frac{2\cdot I_D}{(V_{\rm GS}-V_t)_N}\times R_S$$
$$= 1 + \frac{2\cdot V_{R_S}}{(V_{\rm GS}-V_t)_N} = \frac{2\cdot(V_G - V_t)}{V_G - V_t - V_{\rm Rs}} - 1 \quad (1)$$

where $V_{\rm Rs}$ is the bias voltage across the resistor. This shows that the linearity of the G_m stage is a function of V_G, the input bias voltage. The total available headroom, set by the supply voltage, is divided across the input stage (transconductance core, MN1-4 and Rs) and the load. The higher the voltage drop across the input stage, the higher the linearity. At constant V_G, a larger $V_{\rm Rs}$ results in stronger feedback (higher T), and therefore better linearity. On the other hand, the current efficiency of the G_m stage is

$$\frac{G_m}{I_d} = \frac{1}{I_d}\cdot\frac{g_{mN}}{1+R_S\cdot g_{mN}}$$
$$= \frac{1}{I_d}\cdot\frac{(2I_d)/(V_{\rm GS}-V_t)_N}{1+(2I_dR_S)/(V_{\rm GS}-V_t)_N}$$
$$= \frac{1}{\frac{(V_{\rm GS}-V_t)}{2}+V_{\rm Rs}}. \quad (2)$$

Strong feedback (large $V_{\rm Rs}$) raises the bias current necessary for the same transconductance. Fig. 4 plots the simulated tradeoff between the current efficiency $(G_m/I_{\rm bias})$ and linearity of the G_m stage. In the first case, $V_{\rm GS}-V_t$ is kept constant at 0.6 V and

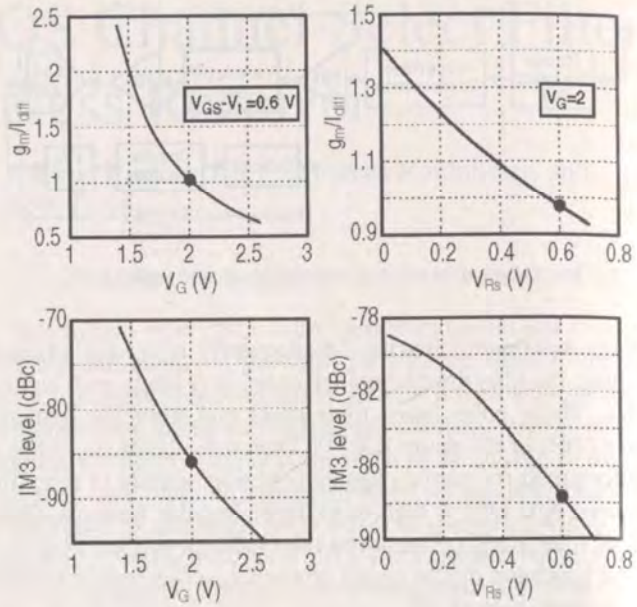

Fig. 4. Current efficiency and linearity of transconductor versus bias voltage and degeneration. Dots show the bias values used.

V_G is swept. In the second case, V_G is constant at 2 V and $V_{\rm Rs}$ is swept. Linearity is simulated with two tones, each 0.2 $V_{\rm pp,diff}$. This design is centered at V_G of 2 V and $V_{\rm Rs}$ of 0.6 V. It should be noted that as the dc degeneration voltage gets larger, the body bias of the field-effect transistor (FET) increases and its $V_{\rm GS}-V_t$ is lowered. Both latter effects create more nonlinearity in the circuit. Therefore, output linearity improves less than the increase in loop gain.

For greater voltage headroom, the bias current source is removed from under the transconductance differential pair. Simulations show that this improves linearity by up to 10 dB. However, the G_m stage now amplifies a common-mode input with the same gain as a differential-mode input. Eventually, true differential sensing of the filter output will strip off the common mode. However, imbalance in the differential circuits due to dc offsets or mismatch causes common-mode to differential conversion. This is precarious, because now parasitic common-mode feedback through the substrate and supply lines may induce differential oscillation in the high gain IF strip. The IF circuits were laid out with great care to symmetrically position individual transistors, and even entire circuit blocks on a center line. This minimizes systematic offsets, and symmetrically couples both halves of differential circuits to the substrate.

B. Active Load

The filter simulates inductors with gyrators, which consist of pairs of transconductors in differential negative feedback. The transconductor inputs and outputs bias at the same voltage. Assuming this is 2 V, and allowing for signal swing of 0.8 $V_{\rm PP}$, the headroom for the active load with 3.3 V supply is

$$\text{Load headroom} = V_{\rm DD} - \left(V_{\rm Out,bias} + \frac{V_{O,\rm pp}}{2} + V_{\rm margin}\right)$$
$$= 3.3 - \left(2 + \frac{0.8}{2} + 0.3\right) = 0.6\ \text{V}.$$

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The active load consists of a single PMOSFET biased with V_{DS} equal to the full 0.6-V headroom. For an acceptable impedance, the PMOSFET length is chosen as 4.5 μm and the NMOSFET length as 3 μm. In contrast, the PMOS in a cascode load fitted into the same bias voltage would contribute 50% higher noise spectral density.

C. Noise, Linearity, and Power Consumption

With the above bias voltages, the G_m/I_{bias} of the transconductance is about 1 (Fig. 4). The noise performance of the transconductor circuit is specified by an excess noise factor Γ defined as follows:

$$\hat{i}_{\text{nO}}^2 = 4kT\Gamma \times G_m. \tag{3}$$

An expression for the output noise in the transconductor circuit is

$$\hat{i}_{\text{nO}}^2 = 4kT \times \left\{ \left(\frac{1 + g_{mN} \cdot R_S - \frac{\gamma}{2}}{g_{mN}} \right) \cdot \left(\frac{g_{mN}}{1 + g_{mN} \cdot R_S} \right)^2 + \gamma \times g_{mP} \right\} \tag{4}$$

where $\gamma = 2/3$ is the noise factor of a long-channel FET.

Since $1 + g_{mN} \cdot R_S > \gamma/2 = 1/3$, then

$$\hat{i}_{\text{nO}}^2 \cong 4kTG_m \times \left(1 + \gamma \times \frac{g_{mP}}{G_m}\right). \tag{5}$$

Therefore

$$\Gamma = 1 + \gamma \times \frac{g_{mP}}{G_m} = 1 + \gamma \times \frac{g_{mP}/I_d}{G_m/I_d} = 1 + \gamma \times \frac{1}{G_m/I_d} \times \frac{2}{(V_{\text{GS}} - V_t)_P}. \tag{6}$$

For more linearity, the loop gain must be higher, which means lower G_m/I_d. Now the noise overhead of the active load is significant. Furthermore, the lower the headroom on the active load transistor, the higher its noise. An interesting alternative is the CMOS inverter-type transconductor [17], which lowers excess noise because both sources of noise (NMOS and PMOS) also contribute signal transconductance. However, at low supply voltages, this transconductor is not linear enough for this filter.

D. Parasitic Capacitances

The large FET's in the transconductor impose a large gate capacitance, with two adverse effects. First, the C_{gate}, which appears in parallel with the filter tuning capacitors, can cause large deviations in the filter frequency response. Second, C_{gd} generates a zero in the right-half s-plane at frequencies close to the passband edge of the LPF, and the resulting phase shift may peak the frequency response in the passband

$$\omega_Z = G_m/C_{\text{gd},N} = \frac{g_{mN}}{C_{\text{gs},N}} \times \frac{1}{1 + g_{mN} \cdot R_S} \times \frac{C_{\text{gs},N}}{C_{\text{gd},N}} = \frac{\omega_{T,N}}{\text{Loop Gain}} \times \frac{C_{\text{gs},N}}{C_{\text{gd},N}}. \tag{7}$$

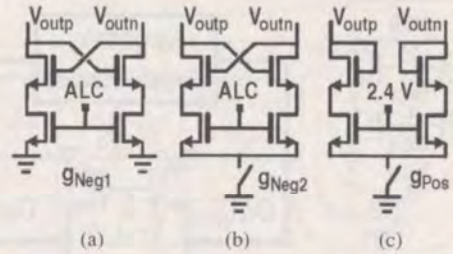

Fig. 5. (a) Negative conductance stage. (b) Auxiliary switched negative conductance. (c) Switched positive conductance.

TABLE I
RANGE OF TOTAL NEGATIVE CONDUCTANCE AT THE OUTPUT

N_{Pos}	N_{neg2}	Range
on	off	$0 \rightarrow -1.5\times G_m/40$
off	off	$-G_m/40 \rightarrow -G_m/16$
off	on	$-G_m/20 \rightarrow -G_m/8$

Long channel devices suffers from low ω_T. In addition, higher loop gain lowers the zero frequency. Nevertheless, $\omega_Z = 2\pi \times 2.2$ GHz in this transconductor lies more than two decades higher than the passband edge, causing negligible parasitic phase shift.

E. Increasing dc Gain

Simulations show that the dc voltage gain of the basic G_m stage is about 20 when driving a capacitor load. As the output impedance in the HSPICE BSIM2 MOS models at the time of the design was not trustworthy, the design allows for a spread of 50% in output impedance. A gain as low as ten would produce unacceptable passband loss in the filter frequency response. To compensate this, a negative conductance stage, implemented by a cross-coupled transconductor, is put in parallel with the output of the main transconductor [Fig. 5(a)]. Using $|g_{\text{Neg}}| = |-G_m/8|$ can compensate a dc gain as low as eight. An auxiliary switchable negative conductance g_{Neg2} is in parallel with this [Fig. 5(b)]. At the other extreme, if the net output impedance becomes negative due to overcompensation, it should be possible to set g_{Neg} to zero. However, sweeping the control voltage (V_{ALC}) over its full range from 2.4 to 3.2 V changes g_{Neg} by a maximum of 2.5×. To obtain a net output g_{Neg} of zero, a switchable positive conductance stage is inserted in parallel [Fig. 5(c)]. g_{Pos} is constant and equal to $G_m/40$. Each g_{Neg} stage varies between $-G_m/40$ and $-G_m/16$. Table I shows the range of total negative conductance at the output for various switch positions. Simulations show that g_{Neg1} alone covers the nominal case. At the price of a slightly more complicated control loop, this approach consumes about 3× less power and is less nonlinear and noisy than if of one g_{Neg} and one g_{Pos} were required to cover the full range of process variations.

F. Final G_m Circuit

The final G_m stage shown in Fig. 6(a) is designed for a low-noise version ($G_{m,H}$) of the LPF. The total filter consumes 50 mA from 3.3 V. The receiver also uses another LPF with the

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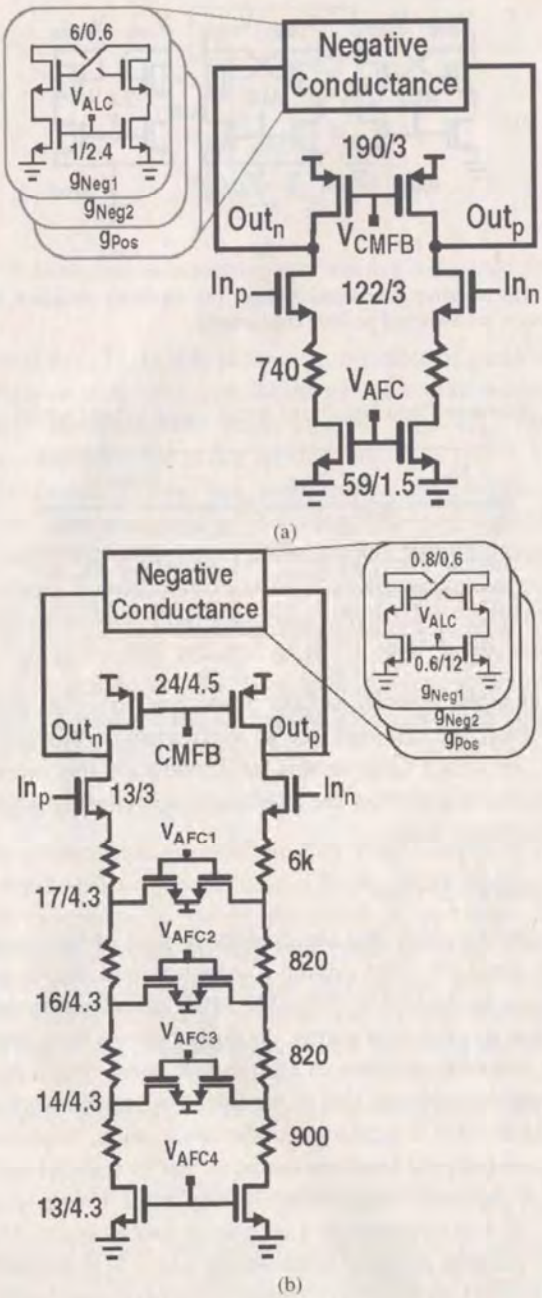

Fig. 6. Variable transconductor (actual), as used in (a) low-noise LPF and (b) low-power LPF and HPF.

same frequency response and linearity, which consumes 10× lower power ($G_{m,L}$) but with a 10-dB higher noise floor. All the transconductances and capacitors in this filter are scaled down by a factor of ten. The low power transconductance is shown in Fig. 6(b). For a reason that will be explained later, $G_{m,L}$ should be tunable by more than 50%, while the $G_{m,H}$ need only vary by 13%. Compared to the high power transconductor, $G_{m,L}$ includes several stages of variable degeneration to expand range without giving up linearity. At any time, only one of the degeneration MOSFET's is on, and its gain control voltage varies from 1.6 to 3.3 V. The range of degenerated transconductance overlaps across the MOSFET's in the ladder. This guarantees continuous sweep of 50% in transconductance. Table II summarizes the important characteristics of the final transconductors.

TABLE II
CHARACTERISTICS OF THE FILTER TRANSCONDUCTANCE

	Hi/Low Power
G_m nominal	660/66 (μS)
g_m/I_{diff}	1
Noise factor, γ	2.3
g_m variation	13%/50%
Input/Output swing	1.6 Vpp,diff
IIP3 (ref. 100 Ω)	29 (dBm)

IV. Low-Pass Filter Design

The low-pass filter's cutoff frequency, which defines the upper edge of the bandpass filter, is selectable as 5.65, 7.5, and 15 MHz. A passband ripple as large as 3 dB is tolerable, but the stopband attenuation should be higher than 50 dB. Depending on the channel conditions, either the low-power or the low-noise LPF is selected. Each LPF is based on a doubly terminated LC ladder, which is more forgiving of deviations in component values from the ideal. This property is particularly valuable because in this filter, the transconductor FET's themselves contribute substantial but poorly modeled capacitance, with a different dependence on process variations than the linear capacitors.

A. Filter Structure

The prototype filter is designed for 1-dB passband ripple, 60-dB stopband attenuation, 15-MHz passband edge frequency, and a transition band narrower than the passband. A fifth-order elliptic filter meets these specifications. The floating inductors are replaced with gyrator-C circuits. The capacitances and transconductors of the filter are built from unit capacitors (C_u) and unit G_m stages (G_{mu}) [6]. The ratio between the filter node capacitors and the transconductors should be ideally constant over temperature and process. Parasitic capacitors at the nodes arise mainly from the drain junctions and the NMOS gates. They vary differently with fabrication process than the main linear capacitors. In the ith node, the parasitic capacitance from the transconductors C_{Pi} is absorbed in the total node capacitance C_i

$$C_i = C_{Pi} + n_i \cdot C_u. \tag{8}$$

Since the ratio $C_{Pi}/n_i \cdot C_u$ varies from node to node, if C_{Pi} is a significant part of C_i it disturbs the designed ratio of node capacitors, and thus the filter frequency response. At high bandwidth settings, $C_{Pi}/n_i \cdot C_u$ is largest. C_P comprises the input and output capacitance of G_m, which are 1.2 and 0.5 pF for $G_{m,H}$, respectively. Table III shows the standard deviation of the different types of the capacitance. These spreads cause two problems. First, the passband ripple increases. This happens to be not very important in the intended use. Second, the master control loop and slave filter do not match well. The consequences of this are discussed later.

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TABLE III
STANDARD DEVIATION OF THE DIFFERENT TYPES OF THE CAPACITANCE OVER VARIOUS RUNS IN OUR PROCESS

	Lin. Cap.	$C_{G,PMOS}$	$C_{G,NMOS}$	$C_{D,PMOS}$	$C_{D,NMOS}$	Gate Cap./ Lin. Cap.
Average (fF)	2264	3392	3577	932	536	
Rel. σ (%)	2.3	3.2	3.5	4.9	3.8	1.8

TABLE IV
PEAK GAIN TO THE INTERNAL NODES, AND THE POWER MERIT FOR THREE TYPES OF SCALING

	Node Max. gain (dB)				Power merit
	1	2	3	4	Relative $I_{bias}.V^2_N$ (dB)
No Scaling	4	8.7	8.2	4.5	0
Full Scaling	0	0	0	0	6.5
Semi Scaling	4	5.1	4.5	4.7	1.4

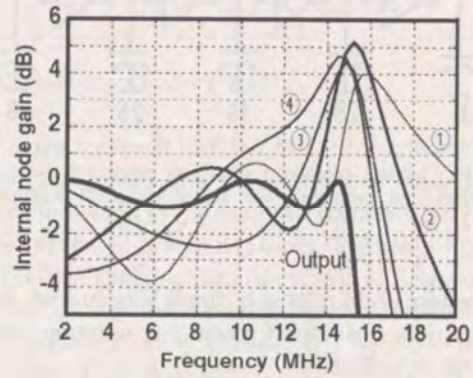

Fig. 7. Gain versus frequency to the filter internal nodes (shown numbered) after semiscaling.

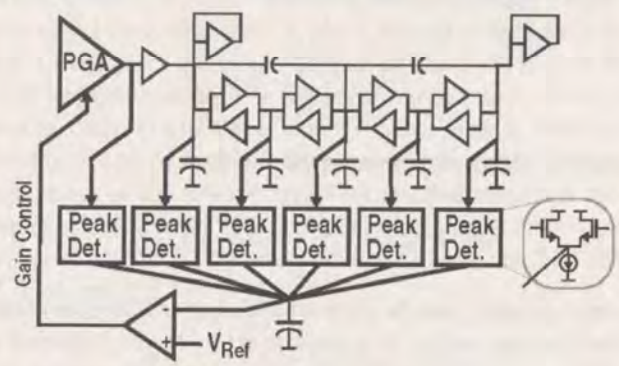

Fig. 8. Prefilter AGC prevents saturation at internal nodes.

B. Filter Amplitude Scaling

There are two steps in scaling an active filter to maximize dynamic range: amplitude scaling, and noise scaling. In an unscaled filter, the input signal may be amplified more to internal nodes than to the filter output, the peak gain at a frequency close to the passband edge. An input signal with strong power spectral density at this frequency can drive the internal transconductors into saturation. The textbook solution is to scale the filter by the L_∞ norm. That is, all node impedances are scaled so as to make the peak gain from the input to all the filter nodes to 0 dB across the entire passband [6]. As a consequence, gain from the major noise sources in the filter to the output also rises, increasing the input-referred noise of the filter. In a wireless receiver, the higher in-band noise of an L_∞-scaled filter always weakens the signal-to-noise ratio of the desired channel, whereas in an unscaled filter, only an interferer that happens to lie close to the passband edge, or a very strong desired signal drives internal nodes into saturation. In practice, strong interferers appear with equal likelihood across the band, and only sometimes lie close to the passband edge. Furthermore, a prefilter automatic gain control (AGC) can lower a strong in-band signal. Therefore, a partly scaled filter may be preferred in a wireless receiver because its lower noise is always desirable.

This filter is scaled as follows. While scaling gain to the internal filter nodes, Σg_m, which represents the power consumption, and the output noise are monitored. Initially, scaling lowers the peak gain to the internal nodes faster than it causes noise to rise. With further scaling, however, noise increases substantially. Table IV shows the peak gain to the internal nodes, and the power figure-of-merit for three stages in scaling. Discussion in the next section justifies choice of this figure of merit. To begin with, in the unscaled filter the largest gain to an internal node is 8.7 dB, while the end-to-end filter peak gain is 0 dB in the passband. Scaling the peak down to 5.1 dB lowers the figure of merit by 1.4 dB, which means that dynamic range improves. Further scaling to level all the peak gains to 0 dB lowers the figure of merit ($I_{\text{bias}} \cdot V^2_{O,n}$) by 5.1 dB, which is almost the same as the decrease in peak gain. However, the resulting higher noise always degrades sensitivity. With full scaling, therefore, average dynamic range is worse.

As a result of these trends, this filter is only partly scaled. Fig. 7 shows the frequency response of the filter nodes after semiscaling. To prevent premature saturation of G_m stages, the scheme in Fig. 8 detects signal peaks at all the nodes. If the peak value exceeds some limit, the prefilter variable-gain amplifier lowers the input signal.

C. Filter Noise Scaling

Following scaling for gain, the filter is scaled for the noise. Scaling up all the G_m stages and the filter capacitors together increases the bias current but proportionally lowers output noise spectral density ($V^2_{O,n}$). The power merit and frequency response of all nodes remain unchanged. This is why $I_{\text{bias}} \times V^2_{O,n}$ is a fundamental figure of merit. The procedure for noise scaling starts by identifying those filter nodes that contribute significantly to total noise but whose associated

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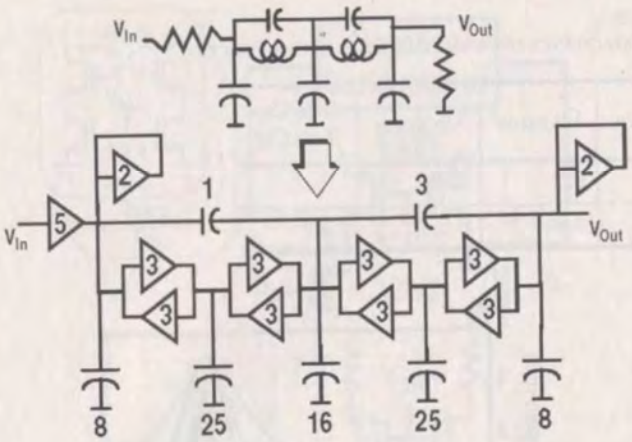

Fig. 9. LPF ladder prototype and its active G_m-C realization. Transconductors and capacitors are scaled to small multiples of unit values.

transconductors drain relatively small bias current. Scaling up these nodes does not impact power consumption much, but it lowers noise significantly.

Noise scaling is optimized as follows. $N_{\rm Tot}$, the total output noise power spectral density, is calculated, where $N_{\rm Oi}$ is the noise that the ith G_m stage contributes to the filter output

$$N_{\rm Tot} = \sum_{i=1}^{K} N_{\rm Oi}. \tag{9}$$

As all G_m stages use the same circuit, then

$$N_{\rm Oi} \propto \frac{1}{G_{\rm mi}} \propto \frac{1}{I_i} \rightarrow N_{\rm Oi} \cdot I_i = \alpha_i \tag{10}$$

where $G_{\rm mi}$ and I_i are the transconductance and the bias current of the ith stage and α_i is a constant set by the circuit topology and $V_{\rm GS} - V_t$. Noise scaling aims to minimize the noise with a constant total bias $I_{\rm Tot}$

$$N_{\rm Tot} = \sum_{i=1}^{K} \frac{\alpha_i}{I_i} = \sum_{i=1}^{K-1} \frac{\alpha_i}{I_i} + \frac{\alpha_K}{I_{\rm Tot} - \sum_{i=1}^{K-1} I_i} \tag{11}$$

$$\frac{\partial N_{\rm Tot}}{\partial I_i} = 0 \rightarrow \frac{N_{\rm Oi}}{I_i} = \frac{N_{\rm Tot}}{I_{\rm Tot}} = \text{Constant}. \tag{12}$$

Thus, for the lowest $N_{\rm Tot}$ at a fixed $I_{\rm Tot}$, all the G_m stages should be scaled to the contribute the same noise to the filter output per unit bias current. However, G_m stages whose outputs connect together are not independent and must be scaled together. Ideally, the optimum scale factor β_i for the ith G_m stage is

$$\beta_i = \sqrt{\frac{N_{\rm Oi}/I_i}{N_{\rm Tot}/I_{\rm Tot}}}. \tag{13}$$

In this way, the filter is scaled for both gain and noise. Fig. 9 shows the final component sizes after scaling and roundoff to small integers.

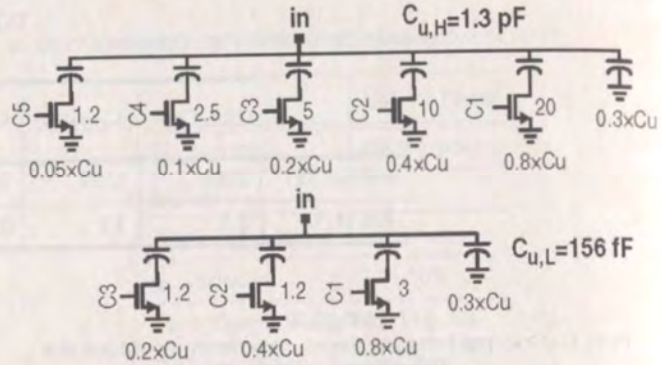

Fig. 10. Grounded unit capacitor in low-noise and low-power LPF. Switch widths are shown; all lengths are minimum. Floating capacitors (not shown) consist of same array, activated by complimentary switches.

D. Switched Capacitor Array

The cutoff frequency of the adaptive LPF must vary from 5.7 to 15 MHz. Allowing an additional ±25% to compensate for process and temperature variations, the tuning range encompasses 3.8–18.8 MHz, requiring $G_{\rm mu}/C_u$ to vary by 5×. If $G_{\rm mu}$ alone is tuned over this range, the passband noise spectral density rises by 7 dB at the lowest frequency. On the other hand, if C_u is varied, the noise spectral density stays constant.

Each capacitor consists of a subarray of switched capacitors. The switch on-resistance introduces some loss in the circuit, lowering the effective Q of the capacitor (Q_c). Filters with higher Q poles require higher Q_c. Since $Q_c = 1/(r_{\rm on}\omega C)$, high-frequency poles need larger switches. Switch sizes were chosen by modeling resistors in series with C_u, and exploring the impact of limited Q_c on filter response. Fig. 10 shows the C_u for grounded and floating capacitors used in high-power and low-power LPF's. The low-power LPF uses fewer switched capacitors, because the nominal capacitance is 10× smaller and even the smallest switch now introduces a parasitic, which compresses the capacitance swing between switch ON and OFF. The switched capacitor ratio is about 8% for the high-power capacitors, and 30% for the low power. To guarantee continuous coverage of G_m/C, G_m must span a wider range than the switched capacitor ratio. Therefore, the G_m variation for the high power and the low power was chosen to be 13% and 50%, respectively.

V. High-Pass Filter Design

The HPF transition band should be similar to the LPF transition band. A third-order Chebychev high-pass satisfies this condition. However, there is a practical problem in a direct implementation of the HPF. Although no filter capacitor connects to ground, inevitable parasitics to ground produce rolloff at high frequencies. When using this G_m stage, the parasitic upper cutoff in the HPF lies close to the highest designed cutoff in the LPF (15 MHz). This is unacceptable.

This HPF is implemented by applying low-pass feedback to 45-dB switchable gain stage [Fig. 11(a)]. This follows the LPF. A transconductance stage (G_L) with input connected to its output through a low-pass biquad is inserted in parallel with a fixed load resistor. At high frequencies, there is no feedback, and G_L produces no signal current. As G_L's output resistance is much higher than R_L, the gain at high frequency is $G_{\rm mA} \times R_L$.

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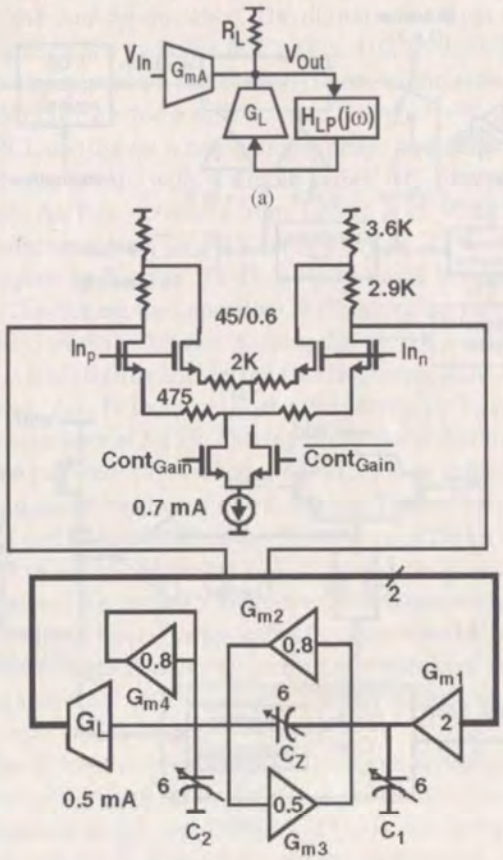

Fig. 11. (a) HPF consists of amplifier with low-pass feedback at output load. (b) Details of HPF, showing switched gain transconductor and LPF biquad in feedback with feedforward compensation capacitor.

At low frequencies, however, the biquad applies unity gain feedback causing the transconductor to appear as a resistance $1/G_L$. When $R_L \gg 1/G_L$, overall dc gain G_{mA}/G_L is smaller. In the actual design, the gain varies from 0 dB at dc to 15 dB beyond 5 MHz, implementing a high-pass amplifier. The passband gain is switchable between 0 and 15 dB with the degeneration resistors in G_{mA}.

The feedback loop's noise contribution is only important for in-band signals, that is, for signals lying in the stopband of the low-pass feedback. The feedback elements generate an output noise with a spectral density proportional to G_L. In the high gain mode, with dc gain of 0 dB, $G_{mA,H} = G_L$. As the output current noise of these two blocks is proportional to their transconductance, G_L adds 3 dB to the input noise of the amplifier. In the low gain mode, $G_{mA,L}$ is 15 dB lower, and now G_L contributes most of the output noise. However, low postfilter gain is only selected when the signal is large, in which case the higher noise is not much of concern.

Now consider nonlinearity due to loop components. The LPF and G_L give rise to in-band third-order intermodulation (IM3).

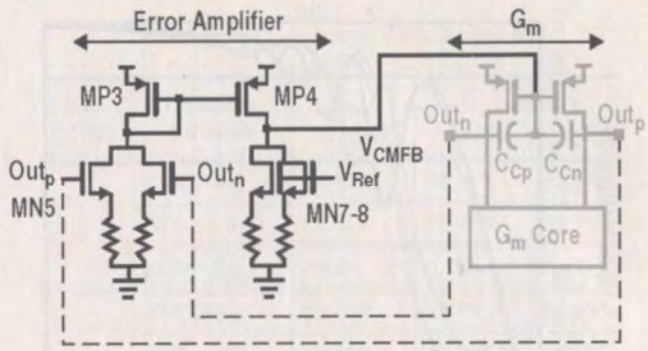

Fig. 12. Common-mode feedback amplifier.

The BW of the feedback LPF is 1 MHz. To generate IM3 at frequencies higher than 5 MHz, at least one of the tones must lie in the transition band of the low-pass feedback, and this is significantly attenuated before it reaches the input of G_L. Hence, G_L itself cannot generate significant IM3 at frequencies above 5 MHz. Any in-band IM3 that the low-pass feedback generates lies in its stopband and is attenuated. Thus, loop nonlinearity does not affect the overall HPF.

Next consider stability. The low-pass biquad induces large phase shift in the loop. Although a high-order feedback filter would sharpen the HPF transition band, it makes loop compensation impossible. This is why a second-order LPF is used. Fig. 11(b) shows the block diagram of this HPF biquad stage. Feedforward capacitor C_Z creates a transmission zero to compensate the loop with better than 60° phase margin. The transfer function is shown in (14) at the bottom of the page. Three identical stages in cascade produce a comparable transition band to the main LPF. The HPF uses the same G_{mu} stage and C_u as the low-power LPF. Taking into account the zero, the final HPF is of third order.

VI. Common-Mode Feedback

A common-mode feedback (CMFB) sets the input and output bias in a fully differential transconductor. Associated with each transconductor is the CMFB circuit (Fig. 12). MN5-8 form the common mode detector and error amplifier, and MN5-6 generate a sum current at their drains, which depends on the G_m stage output CM voltage. MN7-8 compare this with the current generated by V_{REF}. The output voltage (V_{CMFB}) feeds back to the gates of the PMOS load transistors in the main transconductor, driving the output bias of the G_m stage to V_{REF}. Resistor degeneration linearizes the error amplifier to suppress bias shifts caused by a large differential sinewave at the G_m output due to second-order distortion in the FET's.

There are some special problems of CMFB in multiple differential transconductors connected in a filter. At many places in the LPF, the outputs of G_m stages connect together. Independent CMFB in each stage will create multiple feedback loops

$$\frac{V_O}{V_I}(s) = \frac{G_{m1} \cdot G_{m2} \cdot \left(1 + \frac{C_Z}{G_{m2}} s\right)}{[(C_1 + C_2)(C_2 + C_Z) - C_Z^2] \cdot s^2 + [G_{m4}(C_1 + C_Z) + (G_{m3} - G_{m2})C_Z] \cdot s + G_{m2} \cdot G_{m3}} \tag{14}$$

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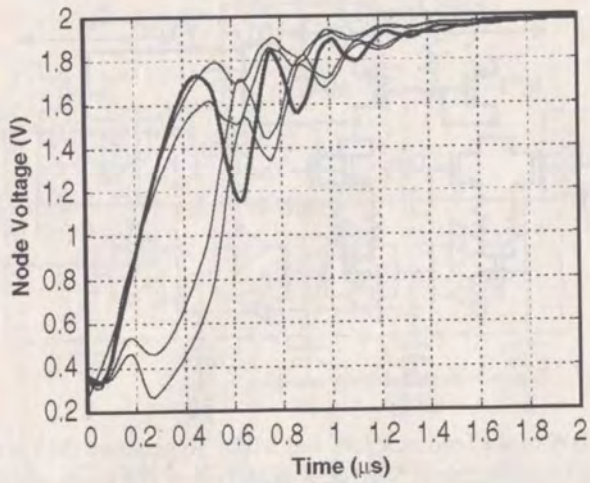

Fig. 13. Common-mode step response at filter's internal nodes.

competing to force the same CM voltage at the shared node. In the presence of mismatch or offsets, this may drive some of the active load PMOSFET's into triode or cutoff. To prevent this, all active loads connecting to an output node are merged and driven by a single CMFB.

Two comparable poles in the two-stage loop amplifier erode phase margin. Miller multiplied capacitors C_{Cp} and C_{Cn} between V_{OUT} and V_{CMFB} in Fig. 12 compensate the loop. To differential transconductor inputs, the node CMFB is at a virtual ground, so that these C_C's are connected between the output and ground and absorbed into the actual grounded capacitor which sets the filter poles.

The large common-mode gain in this transconductor poses a problem in gyrator loops. Although the loop is connected in negative feedback for differential signals, it is always in positive feedback for common mode. This can only be guaranteed stable if the negative CMFB gain overcomes the positive feedback gain in the gyrator loop. Due to the local CMFB, the CM closed loop output impedance presented to the G_m stage is

$$R_{O,C} = \frac{R_{O,O}}{(1 + g_{m,P} \cdot R_{O,O} \times \mathrm{Gain}_{\mathrm{ErrAmp}})} \tag{15}$$

where $R_{O,O}$ is the open-loop output impedance of G_m, $R_{O,O} = r_{\mathrm{op}} \| (1 + g_{mN} \cdot R_s) r_{\mathrm{on}}$. The net common-mode loop gain is

$$T_{\mathrm{Global}} = G_m \cdot R_{O,C} \approx \frac{1}{g_{m,P} \cdot R_s \times \mathrm{Gain}_{\mathrm{ErrAmp}}}. \tag{16}$$

This quantity is always less than one, which means that at dc the global loop is always stable. At high frequencies, the Miller-multiplied C_C shorts the input and the output of the PMOS active load devices, lowering the output impedance to $1/g_{\mathrm{mP}}$. Since $G_m < g_{\mathrm{mP}}$ (as explained in Section III), the positive feedback loop gain remains less than one. In the actual circuit, stability of the gyrator loops requires C_C to be 3× value required for stability of the local CMFB loops.

It is difficult to simulate the phase margin for this multiple loop circuit using only ac analysis in SPICE. Transient analysis of, for instance, the response to a large step in CM V_{REF} from 0 to 2 V gives more insight. Fig. 13 shows the simulated step response test for all the filter nodes in the worst case, when G_m is maximum and C_u minimum.

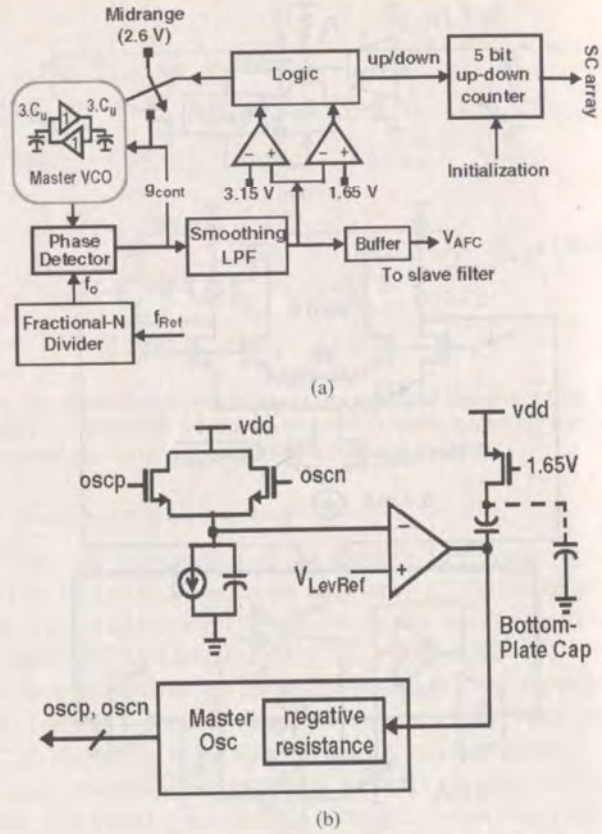

Fig. 14. (a) Automatic frequency control loop. (b) Automatic level control loop.

VII. Frequency and Q-Tuning Loops

Tuning loops set the ratio G_{mu}/C_u (for frequency response) and the output negative resistance (for pole Q). The literature covers many different methods for the design of these loops [18]. This filter uses a master–slave vector-locked loop (VLL). With the desired value of G_{mu}/C_u, a voltage-controlled oscillator (VCO) consisting of an undamped gyrator-based resonator oscillates at a known frequency f_0 enforced by an automatic frequency control (AFC) loop. The VCO also controls Q. In the event of a net negative resistance at the output of the G_m, the amplitude of oscillation grows until it pushes the transistors into triode region. On the other hand, the amplitude decays if the net resistance is positive. Only a zero net output conductance produces stable linear oscillation at a known amplitude. An automatic level control (ALC) adjusts the negative resistance. As all control loops operate similarly, only the phase-locked loop (PLL) for the high-power filter is described below.

A. AFC Loop

The AFC [Fig. 14(a)] is a mixed analog–digital loop, consisting of an analog phase detector and smoothing filter, digital comparator block, logic, reset circuits, and the 5-bit up–down counter.

V_{AFC}, the continuous output of the AFC loop, biases the gates of the active degeneration FET's in the G_m block (Fig. 6)

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and sets the transconductance. The digital word from the 5-bit counter selects the switches in C_u (Fig. 10). In the low-power filter, the digital section routes V_{AFC} to one of the active degeneration MOSFET's for coarse discrete tuning.

The PLL consists of a conventional phase frequency detector and a charge pump, with a simple series RC filter for compensation. As V_{AFC} changes from 1.65 to 3.15 V, it raises the transconductance and the VCO frequency by 13%. However, as mentioned in Section IV-D, a 500% range is required for G_m/C_u. Switching the capacitors in C_u gives the rest.

The AFC works as follows. Assume that the frequency of VCO (f_{VCO}) is initially much lower than the frequency at the output of the divider (f_0). To increase f_0, the PLL drives up V_{AFC} until it hits the upper limit of 3.15 V. This trips a comparator, which decrements the counter. This switches C_u to a lower value, causing a jump up in the frequency of oscillation. The reverse happens when f_{VCO} is initially higher than f_0, and V_{AFC} crosses the lower threshold of 1.65 V. Since the PLL is second-order and slightly underdamped, the control voltage rings as it approaches the final value. Although V_{AFC} finally settles to some value between 1.65 and 3.15 V, it might overshoot this range at the peaks of the ringing waveform. An LPF smooths the PLL control voltage before comparison with the trip levels.

Feedback from the counter to the comparator/logic prevents overflow (underflow) when the C_u is minimum (maximum), corresponding to the word 00 000 (11111). To lower settling time, the counter is initialized with the steady-state value expected from simulations. Then, the control voltage is initialized midway between the upper and lower limits. This guarantees a short settling time for the PLL.

B. Tuning AFC Loop to Three Different BW's

The AFC must be able to tune the filter to three widely separated frequencies. One possibility is to scale the $G_{m,\mathrm{VCO}}$ relative to G_{mu}, so that the oscillator remains locked to a fixed reference frequency while G_m/C in the filter steps to the desired values. This approach is not practical if the G_m stage, as here, suffers from significant parasitics, which will upset the ratio accuracy between master and slave over the wide range of filter settings. Instead, the VCO replicates the G_{mu} and C_u in the main filter, and is locked to synthesized reference frequency proportional to the filter BW (Fig. 20).

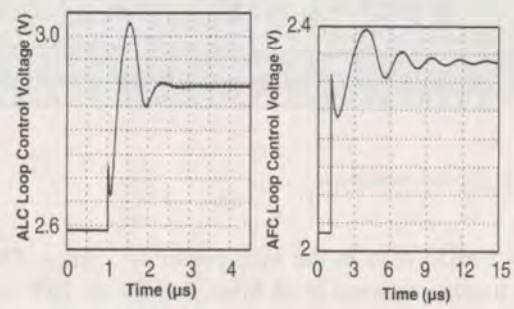
As in any master–slave scheme, the main concern is how accurately the VCO oscillation frequency tracks the filter BW. To simulate this, the capacitors in an ideal G_m-C filter and VCO are expressed as combinations of C_i (at the G_m input), C_o (at the G_m output), and C_u (unit linear capacitors). Then, based on the data in Table III, each capacitor is skewed from nominal to simulate mismatch among different capacitor types (this does not simulate random mismatch between capacitors of the same type). Table V shows that filter BW follows the VCO oscillation frequency with an accuracy better than $\pm 1\%$, for 3σ deviations in the various capacitors.

C. ALC Loop

The ALC is very similar to the AFC, except that it controls amplitude of oscillation instead of frequency [Fig. 14(b)]. A 2-bit counter selects the three discrete states of the negative conductance circuit. Comparators with trip points at 2.4 and 3.2 V define the valid range of control voltage. Initially, both g_{Pos} and g_{Neg2} are off and the control voltage is set midscale to 2.8 V. If the transconductor output conductance is net positive, the peak detector senses zero. The ALC now raises the negative conductance by increasing V_{ALC}. In steady state, the net output conductance is zero, and the amplitude of oscillation is 200 mV.

TABLE V
VARIATION IN VCO FREQUENCY AND FILTER BW

BW (MHz)	Parameter Variation	C_o (±15%)	C_i (±10%)	C_u (±7%)
15	ΔVCO (f_0)	±1.45%	±3.51%	±3.9%
	ΔFilter (BW)	±1.87%	±2.75%	±4.7%
	$\lvert\Delta BW-\Delta f_0\rvert$	0.42%	0.76%	0.8%
5.7	ΔVCO (f_0)	±0.75%	±1.4%	±6.65%
	ΔFilter (BW)	±0.35%	±0.86%	±6.1%
	$\lvert\Delta BW-\Delta f_0\rvert$	0.35%	0.54%	0.65%



(a) (b)

Fig. 15. Simulated response to a 300-mV step in (a) ALC loop, with AFC inactive and (b) AFC loop, with ALC inactive.

D. Simultaneous Compensation of AFC and ALC

At power up, the ALC induces oscillation. As a result the AFC loop becomes active and changes G_m, but as there is no tail current source, this also changes the FET bias current. Since the output conductance depends on bias, the ALC reacts by adjusting the negative conductance to compensate for the new output conductance. In this way, the two loops interact and can possibly oscillate in a limit cycle. The solution is to substantially slow down the AFC loop compared to the ALC. Fig. 15(a) shows that with AFC inactive, the ALC loop settles in about 1.5 μs in response to a 300-mV step. Fig. 15(b) shows that with ALC inactive, the AFC loop settling time is about 15 μs, which is considerably slower than the ALC. Sufficient phase margin may be deduced from the small overshoot in the settling transient.

VIII. EXPERIMENTAL RESULTS

The variable-gain BPF IC (Fig. 16) was implemented in a 3M1P 0.6-μm CMOS technology. The linear degeneration resistors consume the largest area in the low-power G_m stage and

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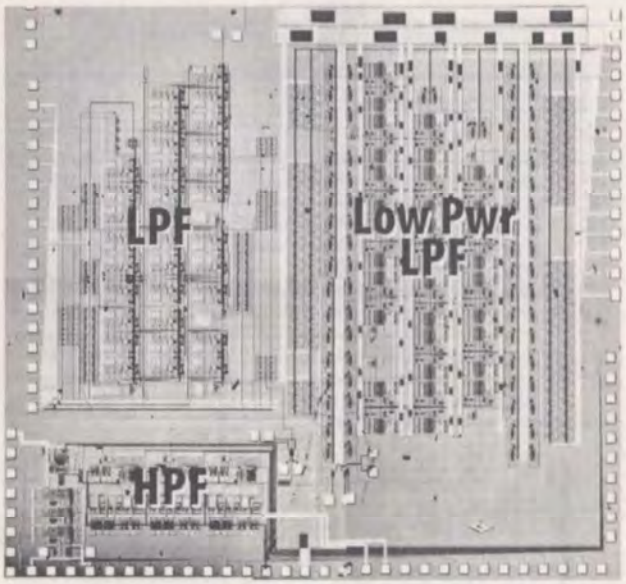
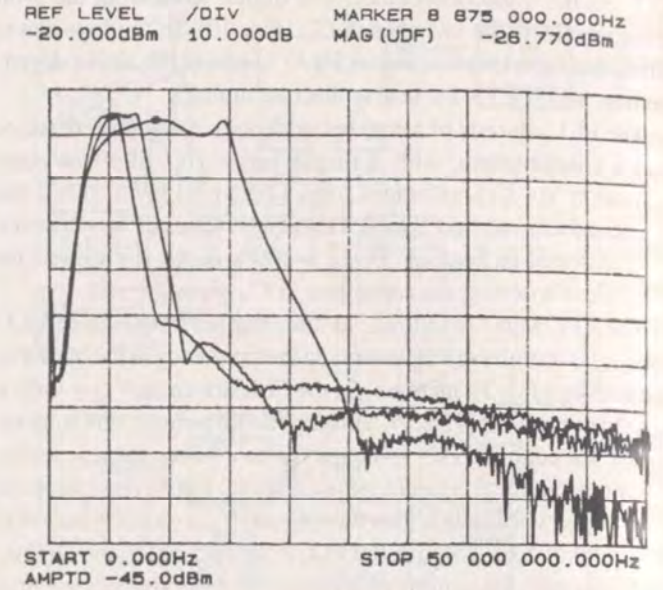


Fig. 16. Chip microphotograph.

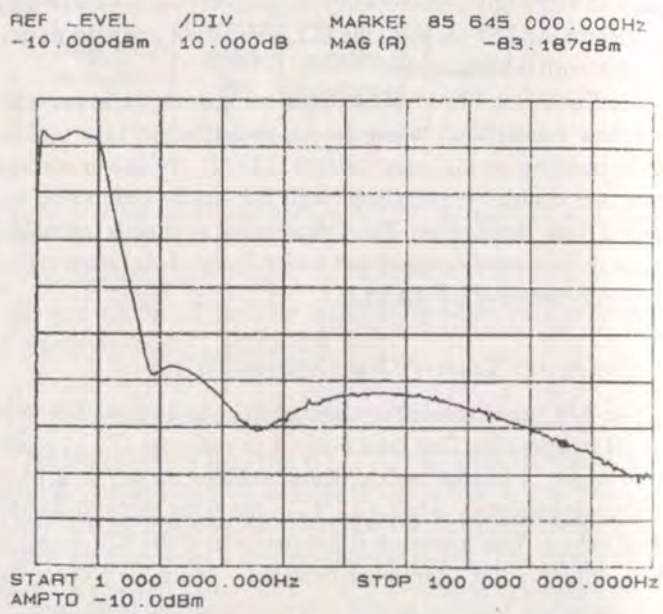
the large PMOS load in the high power G_m stage. The LPF cutoff is tunable between 4–18 MHz, and for the HPF between 3–8 MHz. Fig. 17(a) shows the composite frequency response. At the highest BW, the passband suffers from 2.5-dB ripple, but the stopband loss is more than 60 dB. At lower BW, the ripple decreases to 1 dB (as initially designed), but the stopband attenuation worsens to 50 dB. At high BW, most of the linear capacitors are turned off, and parasitic capacitors significantly alter the pole-zero constellation, worsening the passband ripple. At lower BW, the filter response is closer to designed because the linear capacitors dominate the parasitics. As the LPF is tuned down in frequency, the floating capacitors, which generate nulls in the elliptic filter's magnitude response, appear larger relative to the grounded capacitors, causing the first null to decrease faster than the corner pole frequency. Thus, the transition region becomes sharper, which is desirable, but at the expense of 10-dB-worse stopband loss. Fig. 17(b) shows that the stopband of the filter extends to 100 MHz, beyond which the RF preselect filter at the receiver input strongly attenuates out-of-band signals. The measured passband gain ranges over 47 dB in three steps of 15.7 dB each.

The low-power LPF and low-noise LPF drain 5.4 and 56 mA from 3.3 V, respectively. Input-referred average passband differential noise density is 50 nV/$\sqrt{\text{Hz}}$ and 15.2 nV/$\sqrt{\text{Hz}}$, respectively. In-band IIP3, measured with two tones at 10 and 11 MHz for 15-MHz BW, is +18.5 dBm (referred to 100-Ω differential). This is unchanged for close-in out-of-band tones at 20 and 30 MHz. However, the out-of-band IIP3 with two sets of tones at 30 and 50 MHz and 40 and 70 MHz is +22.5 dBm. As the LPF input stage, where out-of-band tones experience little filtering, dominates the distortion, the IIP3 is not much changed.

The three-stage HPF consumes a total of 5.4 mA at all gains from 0 to 45 dB. The lower cutoff frequency is adjustable from 3 to 10 MHz. Output IP3 specifies linearity for a circuit with variable gain, and for one HPF stage this is found to remain almost constant at +28 dBm (referred to 100-Ω diff), limited by



(a)



(b)

Fig. 17. Measured filter frequency response. (a) Various BW settings, passband, and transition band. (b) Stopband.

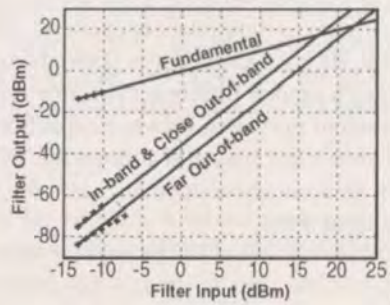


Fig. 18. Measured filter input IP3 at 0-dB passband gain, for two tones in-band and out-of-band.

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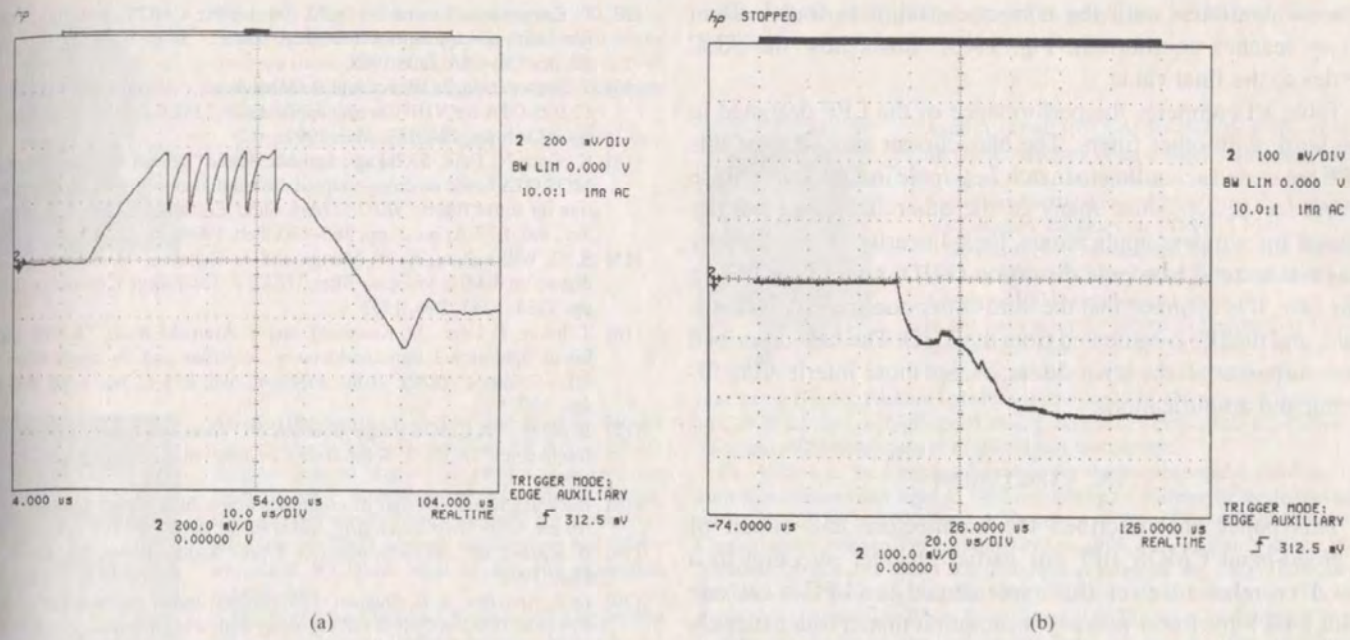

(a) (b)

Fig. 19. Measured settling transient following reset for: (a) AFC and (b) ALC loop.

TABLE VI
COMPARISON OF THE PERFORMANCE OF THIS WORK WITH RECENT PUBLISHED WORKS

Source	Filter order	Technology	cutoff	I/Pole (mA)	Noise (nV/rt-Hz)		Linearity (IIP3, dBm)		Our relative DR (dB)	Their test conditions
					Theirs	Ours	Theirs	Ours		
[21]	6th elliptic+2nd Butterwoth	1μm CMOS	230 kHz	0.74	70	61	30	22.5	−6.3	24 dB gain in filter; Stopband IIP3
[22]	3rd elliptic	0.5μm CMOS	5.5 MHz	1.2	114	48	17.4	20	+10	
[23]	5th elliptic	0.5μm CMOS	2 Mhz	0.77	32.3	60	7	22.5	+10.1	IIP3 ref. to diff. 50 ohms
[24]	6th elliptic	0.5μm CMOS	700 kHz	1.6	30	41.5	30	22.5	−10	AGC within filter. Noise at max. gain. IIP3 at min. gain.
[25]	7th elliptic	1μm BiCMOS	150 kHz--1.5MHz	1.48	140	43	26.7	20	+3.5	IP3 converted from THD
[26]	3rd Buttherworth	BJT	192 kHz	0.33	273	91.2	22.6	20	+6.9	IP3 converted from THD
[27]	5th elliptic	0.8μm CMOS	4 kHz	0.66	130	64	10.8	20	+15.3	

the main amplifier transconductance (G_{mA} in Fig. 6). Average input in-band noise at 0-dB gain is 40 nV/$\sqrt{\text{Hz}}$, dropping to 7.9 nV/$\sqrt{\text{Hz}}$ at gains of 15 dB and higher.

Fig. 18 shows that total IIP3 for the BPF is +18 dBm for in-band tones and out-of-band tones at 20 and 30 MHz. For far out-of-band interferers, namely 30/50 MHz and 30/70 MHz, the IIP3 is +22.5 dBm. As the LPF strongly attenuates interferers in its stopband prior to the following HPF, it (the LPF) governs total filter IP3.

The measured settling behavior of the ALC and AFC loop after applying reset signal is shown in Fig. 26. In Fig. 19(a), the filter capacitance was initially too high. V_{AFC} increases, driving G_{mu} higher until it trips the comparator. At that point the AFC logic switches off a capacitor and resets V_{AFC}. This

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process continues until the correct capacitor is found. Then V_{AFC} reaches equilibrium. Fig. 19(b) shows how the ALC settles to the final value.

Table VI compares the performance of the LPF designed in the work with other filters. The bias current and noise of this LPF are scaled according to match I_{bias}/pole in each case (Noise power $\propto$ I_{bias}). Since many of the other filters are not designed for wireless applications, their linearity is specified by single-tone total harmonic distortion (THD) rather than IP3. In this case, it is assumed that the third-order nonlinearity is dominant, and the IP3 is estimated from the THD. The LPF described here surpasses all the other filters, except those interleaving filtering and amplification.

IX. Conclusion

This paper has described the architecture and circuit of a broad-band CMOS BPF for partial channel selection in a low-IF wireless receiver. It is implemented as a LPF in cascade with a HPF for lower power consumption than a true bandpass filter. The bandwidth is selectable from 625 kHz, 2.5 MHz, and 10 MHz, with the lower passband edge fixed at 5 MHz. By careful design of the transconductor, the optimum linearity and dynamic range is obtained for a given power consumption. The HPF is implemented by using a low-pass feedback. This overcomes the HPF sensitivity to the parasitic capacitances to ground.

We show two low-power and high-power versions of the LPF drain 5.4 and 56 mA from a 3.3-V supply, with input noise of 50 and 15.2 nV/$\sqrt{\text{Hz}}$, respectively. The HPF drains 5.8 mA with 7.9 nV/$\sqrt{\text{Hz}}$ input noise, when it has gain higher than 15 dB. The gain of HPF is variable from 0 to 45 dB in 15-dB steps. The BPF provides better than 50-dB stopband rejection and less than 2.5-dB passband ripple.

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A 2.4-GHz Low-IF Receiver for Wideband WLAN in 0.6-μm CMOS—Architecture and Front-End

Farbod Behbahani, John C. Leete, *Member, IEEE*, Yoji Kishigami, Andreas Roithmeier, Koichi Hoshino, *Student Member, IEEE*, and Asad A. Abidi, *Fellow, IEEE*

***Abstract*—This paper presents the 2.4-GHz front-end and the first downconversion section of a fully integrated low-IF receiver. The dual-conversion receiver and rejects the image repeatably by 60 dB using integrated polyphase filters without calibration or tuning. The gain of the RF mixer and IF amplifier is switchable to slide the available dynamic range of the following stages based on the conditions of the input signal. The front-end and downconversion sections drain 35 mA on average from a 3.3-V supply. Minimum cascade noise figure is 7.2 dB, and maximum cascade IIP3 is −3.4 dBm.**

I. Introduction

THERE IS a push to migrate more radio signal processing into baseband digital signal processors (DSPs). In narrowband systems, for example, a wide dynamic range but low rate analog-to-digital converter (A/D) can digitize several adjacent channels and then select the desired channel. However, in wideband systems, the analog radio must absorb the input signal dynamic range. Adaptation in the digital part may improve the trade-off between performance and power dissipation. New system standards such as Bluetooth relax radio specifications to make it easier to integrate the analog and digital parts in the radio. On-chip image rejection and direct-conversion architectures are of interest to eliminate IF filters.

A comprehensive mixed-mode design of the entire radio requires that analog and digital sections be designed together. New uses of wireless to transmit high-speed data, mainly to access the Internet, are creating a demand for wideband radio systems. Traditional radio design must expand to enable this, for instance by using adaptive beam steering to suppress the principal interferers and strong multipath components to improve reception [1]. In multiple access systems where the capacity is mainly limited by co-channel interferers, these methods also raise capacity.

To date, only limited adaptation has been demonstrated in the analog portion of widespread radio receivers. In a cellular telephone, it may consist of switchable RF gain and variable gain at IF which prevents saturation in the front-end or under- or overloading the baseband A/D.

This paper describes the design and implementation of the front-end and downconversion sections of a *fully integrated dual-conversion superheterodyne* receiver (RX), with on-chip circuits for large image rejection. Section II describes the system at a high level. The architecture is described in Sections III and IV explains the circuit design in detail. Measurements of the image-reject front-end are reported in Section V. The total RX measurement results will appear in [2]

Manuscript received April 19, 2000, revised July 25, 2000.

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Publisher Item Identifier S 0018-9200(00)09469-5.

II. System Description

This adaptive receiver was designed for a wireless local area network (WLAN) operating in the 2.4 GHz ISM band. It supports selectable channel bandwidths (BW) of 625 kHz, 2.5 MHz, and 10 MHz for 0.5, 2, and 8 Mbaud symbol rates, respectively. When there are a few users in a cell, the largest BW is selected to maximize data throughput. With many users, selecting the low BW setting frees up additional channels, thereby granting access to many more users. The modulation used is 4, 16, or 64-QAM, which need SNR of 13.5, 20.4, and 26.5 dB at the detector, respectively, for a BER of 1e-6. In very good channel conditions, 64-QAM is used for high throughput rates. However, if the received S/N drops below 26.5 or 20.4 dB, the modulation is switched to 16 and 4-QAM respectively, to maintain integrity of data transfer, albeit at a lower rate. Adaptation of the symbol rate and constellation provides variable bit rate from 1 to 48 Mbit/s.

The system uses adaptive beam forming with an antenna array. One transceiver must now be attached to every antenna. Aside from the antenna and preselect filter, all other off-chip components must be eliminated. In any case, off-chip channel-select filters cannot be used because their BW is usually fixed. These considerations dictate a highly integrated architecture, and active filters with programmable bandwidth. Due to space limitations, details of the design of the IF strip and the measurements for the whole RX will appear in a companion paper [2].

III. Architecture Rationale

The main objectives in choosing receiver architecture are wide dynamic range, high sensitivity, fewest off-chip components, and lowest power consumption. Fig. 1 shows the block diagram of this dual-conversion low-IF receiver [3], which implements the Weaver architecture. The RF front-end comprises a low noise amplifier (LNA) and an RF quadrature mixer, which downconverts the RF signal to the first IF (IF1). A two-stage polyphase filter following the RF mixer partly rejects the image. Strictly the *first image* in a Weaver architecture need not be suppressed here, because the IF mixers *upconvert* it into the stopband of the subsequent channel select bandpass filter; nevertheless, it was decided to suppress the first image

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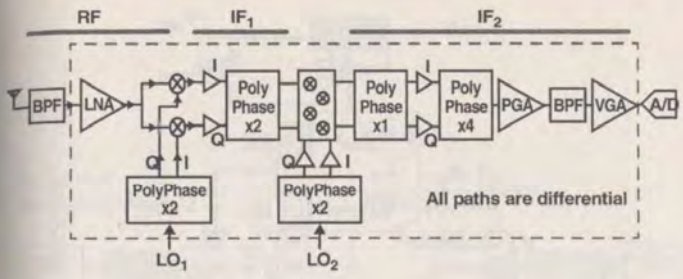

Fig. 1. Receiver block diagram.

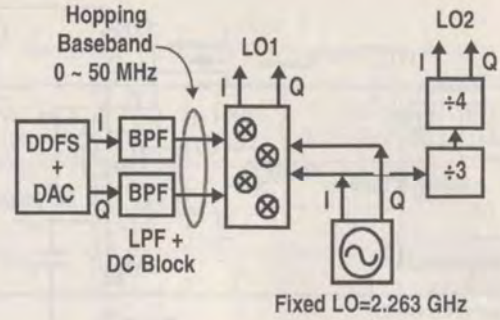

Fig. 2. Proposed frequency synthesizer.

in this receiver to somewhat relax the dynamic range of the IF mixers and the IF2 amplifiers. The IF mixer *downconverts* the *desired* signal at IF1 to a low IF2. Following downconversion, a five-stage wideband polyphase filter rejects the second image entirely on-chip. Amplifiers before the IF1 polyphase filter and within the IF2 polyphase filter compensate loss in the filter passband. In the IF2 strip, the pre-filter programmable gain amplifier (PGA) amplifies the signal to overcome filter noise, while the continuously variable gain post-filter amplifier (VGA) further amplifies the filtered signal to the optimal signal loading (90% full scale) of the A/D converter. The RX is designed for integration with the synthesizer. All signal paths are differential to minimize interaction among the various blocks, or through the substrate.

In a direct conversion receiver, the required $\mathrm{SNR}_{\min}$ of 26.5 dB dictates that image rejection is on the order of 40 dB. This requires better than 1% matching between the various blocks in the I and Q paths, such as amplifiers, channel-select filters, and A/D converters. This is not easy to achieve in practice [4]. Furthermore, a signal at zero-IF competes with dc offset and $1/f$ noise which can significantly degrade SNR of 64-QAM signals at narrow channel bandwidths. For these reasons, the second IF is chosen to be nonzero.

With the same BW, selectivity, and dynamic range, the lower the IF, the less the power consumed by the on-chip bandpass filter [5]. However, a wideband channel at low IF occupies a larger fractional bandwidth over which the image must be rejected. This means more stages in the polyphase filter, therefore higher loss in its passband [6]. For these reasons, a second IF with passband of 5 to 15 MHz is finally used to accommodate the widest 10-MHz channel.

Due to the practical issues discussed in the Section IV-B, the RF mixer can only reject the image by about 35 dB. Thus, IF1 is chosen high enough so that the first image is rejected by an additional 30 dB in the antenna preselect filter. This leads to the final dual-downconversion receiver. A high IF1 also means that spurious signals which might be downconverted by odd-harmonics of LO2 lie in the preselect filter's stopband.

It is very desirable to avoid use of multiple VCOs on the same chip, which tend to injection lock through parasitic coupling. Fig. 2 shows the block diagram of the frequency synthesizer intended for integration with the receiver (not implemented on this prototype). LO2 is a fixed fraction of the frequency of LO1. A direct digital frequency synthesizer (DDFS) and digital-to-analog converter (DAC) generate a fast hopping baseband tone. The VCO upconverts the DAC output in a single-sideband mixer. Quadrature LO2 is generated by dividing the differential VCO frequency by 12, which results in an IF1 of $(2442 + 10)/(12 + 1) = 188$ MHz.

The 2.4-GHz ISM band is 80 MHz wide. By dehopping the input signal at the 1st mixer, the BW of IF1 is limited to one channel (a maximum of 10 MHz). This simplifies the design of IF1 amplifiers and the first polyphase filter.

The IF mixer must reject the image by 60 dB on-chip; double-quadrature downconversion desensitizes the ultimate on-chip image rejection to phase errors in IF1 and LO2, and to gain errors in the IF1 paths [7], [8]. Although it is possible to reject the image in a DSP by digitizing separate I and Q paths after the mixer [8], the A/D must digitize the image as well and therefore must have higher dynamic range (DR). Furthermore, the amplifiers and filters after the mixers must be matched in gain as well as the mixers are, which is 0.1% for 60-dB image rejection. This is very difficult in practice. This receiver rejects the image in the analog domain before amplifying and filtering the desired signal in a single scalar path at IF2.

IV. Circuit Design

A. Low Noise Amplifier

Noise figure (NF) is the most important characteristic of an LNA, and depends on the active device noise, passive device loss, the LNA circuit topology, and how close the operating frequency is to device f_T. The differential inductively degenerated common-source (CS) LNA used here gives sub-3-dB NF at 2.4 GHz. Since the frequency of operation is much lower than $f_T/2$ and the Q of the input matching circuit is relatively low, gate-induced noise is not important [9], [10]. To include short channel noise enhancement [11], we have developed a subcircuit model in HSPICE to represent the measured excess noise factor. The measured and simulated NF of the final LNA agree well over a wide frequency band.

1) FET Noise Model in SPICE: The drain current noise power due to the channel noise is expressed as

$$\bar{i}_n^2 = 4\,\mathrm{kT}\Gamma_e \gamma g_{ds0} \tag{1}$$

where Γ_e is the excess noise factor with respect to the basic Spice model. The BSIM2 models used in our design forces $\gamma = 2/3\,(\Gamma_e = 1)$, as in the classical model. Fig. 3 shows the SPICE subcircuit used to model noise enhancement. A scaled current noise from the replica FET is applied between drain and source of M, the principal FET, raising its excess noise factor to Γ_e. The large inductors and capacitors suppress signals applied to

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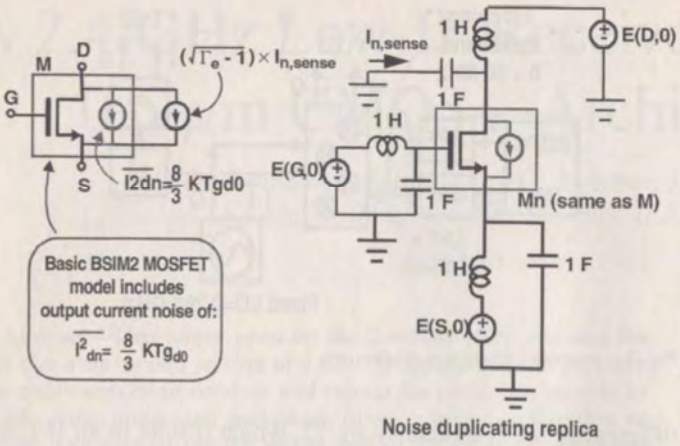

Fig. 3. HSPICE subcircuit to capture enhanced thermal noise.

M from appearing in the replica Mn. This subcircuit works well when the drain and source diffusion resistors have negligible effect.

Noise measured at 50 MHz on a single FET biased at the same point as the LNA shows that $\Gamma_e = 3$. This was used to simulate the actual LNA at 2.4 GHz, including a package model where the pin inductance and capacitance is calculated based on physical dimensions.

In [12] it is shown that feedback through C_{GD} drives the Y_{in} of the LNA away from $Y^*_{s,OPT}$ and raises the NF. The higher the C_{GD} or the gain from gate to the drain of the input FET, the larger will be the NF. This effect is important here because of the relatively large C_{GD} in 0.6-μm CMOS, and it is used to optimize the size of the cascode MOSFET.

2) LNA Optimization: Choosing the right size of FET and laying it out well are both important to obtain a good LNA. Fig. 4 shows a simple CS LNA in cascode configuration to lower undesired capacitive feedback. However, now the combined junction capacitance at the common node raises the noise the cascode FET contributes to the output at 2.4 GHz. This junction capacitance may be lowered with a dual-gate layout [13].

Fig. 5 shows how LNA NF varies with the width of the cascode FET, for a fixed input FET of 150/0.6 μm with interdigitated layout biased at $V_{gs} - V_t = 0.3$ V. The NF is close to minimum when the two FETs are the same size, which gives the opportunity to merge them into one dual-gate FET. This last step further lowers the NF by 0.2 dB because of the lower junction capacitance.

The dual-gate design is explored across various widths at a constant bias of 4 mA, and the resulting NF and IIP3 is shown in Fig. 6. For each width, the input ideal matching circuit is adjusted to obtain narrowband input impedance match to 50 Ω. If C_{GD} and induced gate noise were both zero, the NF would fall indefinitely with width. However, the noise voltage across C_{GD} rises at small FET widths and degrades NF. The size of 150 μm/0.6 μm is finally used because it gives largest dynamic range, and close to the lowest NF.

The LNA (Fig. 7) is fully differential to minimize the effect of noise and interference from other blocks. Three downbonds (each about 1.8 nH) in parallel implement $L_s = 0.9$ nH to present 50 Ω real resistance at the gate of the input MOSFET

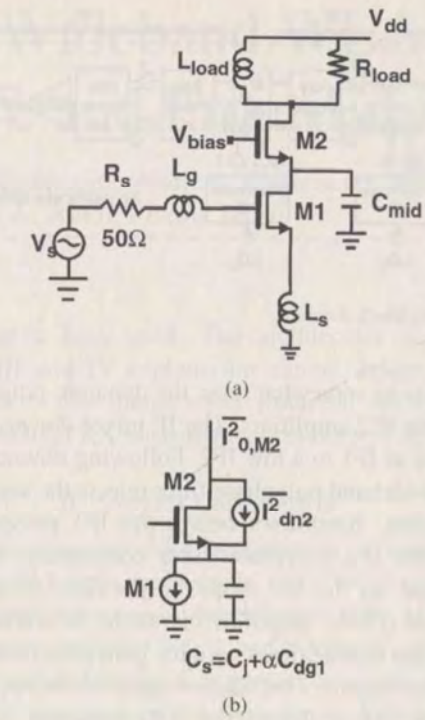

Fig. 4. (a) Common-source LNA circuit. (b) How cascode FET contributes RF noise.

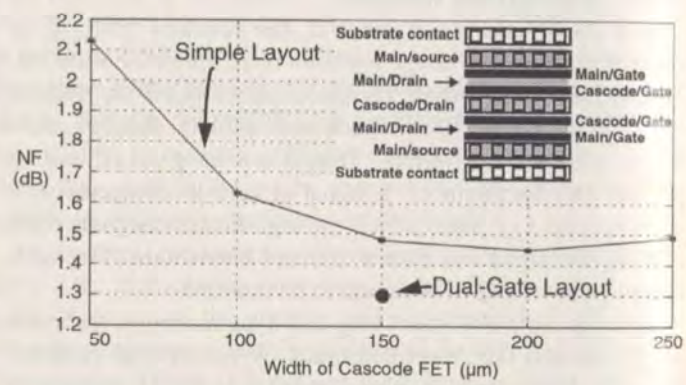

Fig. 5. Overall noise figure at 2.4 GHz for CS LNA ($V_{gs} - V_t = 300$ mV). Inset shows dual-gate layout.

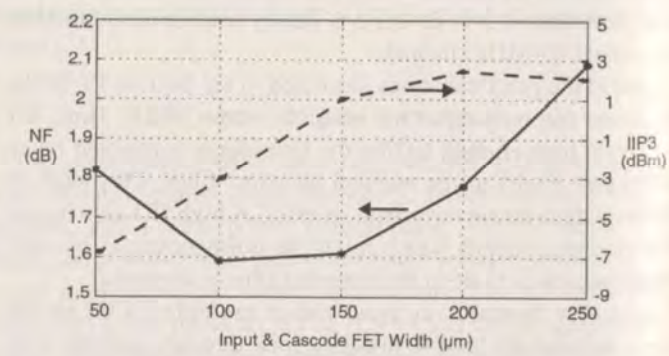

Fig. 6. NF and IIP3 of a simple CS LNA versus MOSFET width.

with each FET biased at 4 mA. The on-chip load $L_d = 5$ nH is a single-layer rectangular spiral inductor in metal-3 layer designed using in-house software to give the highest impedance [14].

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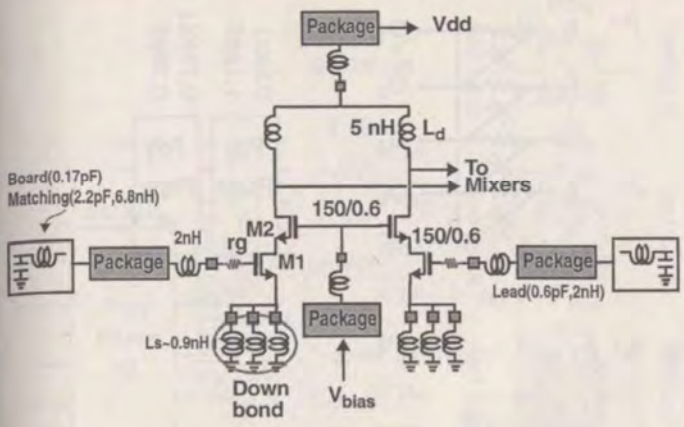

Fig. 7. Complete circuit of differential common-source LNA.

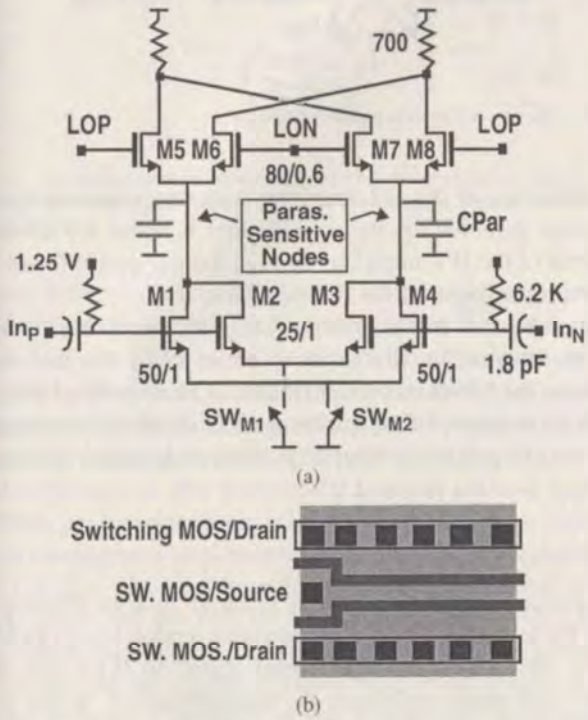

Fig. 8. a) RF mixer. b) Pseudo-dual-gate layout of switching transistors.

B. RF Mixer

The RF mixer downconverts the RF band (2.402 to 2.482 GHz) to IF1 (188 MHz) with tunable low side LO injection (2.212 to 2.292 GHz). Passive FET downconversion mixers used in quadrature arrangement with capacitive loads suffer from large conversion loss because they are nonunilateral [12]. Therefore, the Gilbert-cell-type mixer (Fig. 8) is used. Sharp transitions in the LO waveform lower both the noise [15] and distortion due to mixer switches. Raising the amplitude of a sinewave LO sharpens the transition, but if the LO voltage drives the switch FETs deep into triode, mixer nonlinearity worsens because of the nonlinear output resistance of the transconductance FETs. In the circuit of Fig. 8(a), C_{Par} should be minimized to reduced the noise contribution of the switch transistors [15]. The pseudo-dual-gate layout shown in Fig. 8(b) lowers the switch noise contribution by 2 dB. The switch FETs are biased at $V_{GS} - V_t = 0.2$ V for best noise and linearity. With resistive load, R_L, the resulting noise current is

TABLE I
SIMULATION RESULTS OF ONE DIFFERENTIAL RF MIXER

Input Dev. size(μm)	I_{Bias} (mA)	Gain (dB)	V_n diff. (nV/$\sqrt{\mathrm{Hz}}$)	IIP3 (dBm) Ref. 100Ω diff.
25/1	0.95	-5	9.4	17
50/1	1.9	0.5	6.2	
75/1	2.7	3	5	15.5

$4\,\mathrm{kT}/R_L$. Considering that for an ideal doubly balanced mixer, the voltage conversion gain is $\mathrm{Gain}_v = (2/\pi) g_{m,\mathrm{Main}} . R_L$, and using results from [15]:

$$\text{Relative Load Noise} = \frac{\hat{i}_n^2(\text{load})}{\hat{i}_n^2(\text{transconductance})} \simeq \frac{1}{\gamma} \cdot \frac{2}{\pi \mathrm{Gain}_v}. \quad (2)$$

Two major sources of nonlinearity in the mixer are the input transconductor and the switches. As is now customary for MOS mixers, the transconductor consists of a grounded-source differential pair. The FETs are biased at $V_{\mathrm{eff}} = V_{GS} - V_t = 0.5$ V. Simulations show that this circuit is 10 dB more linear than a differential pair with a constant tail current, leading to a mixer IIP3 of +18 dBm referred to 100 Ω differential source resistance. With the output biased at 2 V, the transconductor and the switches contribute equal nonlinearity at a mixer gain of 5 dB.

The DR of the front-end may be slid up or down. When the desired signal is low, the front-end NF must be lowest for sensitivity. If the desired signal is larger, a higher NF can be tolerated, and the DR is slid up for higher IIP3 by switch selecting the gain of the RF mixer and IF1 amplifier. Mixer transconductance FET size may be selected as 25/1, 50/1, or 75/1 μm. DC and ac voltage drop across the switches is negligible. Table I summarizes simulated mixer performance. With 50/1 μm input FETs the switches and resistive load each contribute about 27% of the total output noise.

The mixer is ac-coupled to the LNA output. The LNA output is biased at a high level for linearity, while the mixer input is biased close to ground. The coupling capacitor is poly over diffusion. Its voltage coefficient and bottom plate parasitic degrade linearity. The bottom plate is connected to the LNA output to absorb the parasitic into the tuned load, and also to raise the reverse bias across the bottom depletion layer. The output of the mixer is ac-coupled to the following amplifier, for the same reasons. The total voltage loss due to the input and output coupling capacitors is about 2.5 dB.

At moderate V_{eff}, g_m is proportional to the overdrive voltage, and so is the IM3 for a given input. Therefore, doubling the V_{eff} at constant bias current halves the g_m (3 dB higher input noise) but raises IIP3 by 3 dB [10]. Thus at a fixed power consumption, the input dynamic range is always constant. On the other hand, switch selecting a smaller MOSFET at constant V_{eff} will lower mixer gain and when the mixer is the bottleneck, improve overall linearity, at the price of higher mixer NF and lower spurious-free dynamic range (SFDR).

A two-stage LO polyphase filter generates quadrature signals from a differential LO input to the resistive [illegible] ac-

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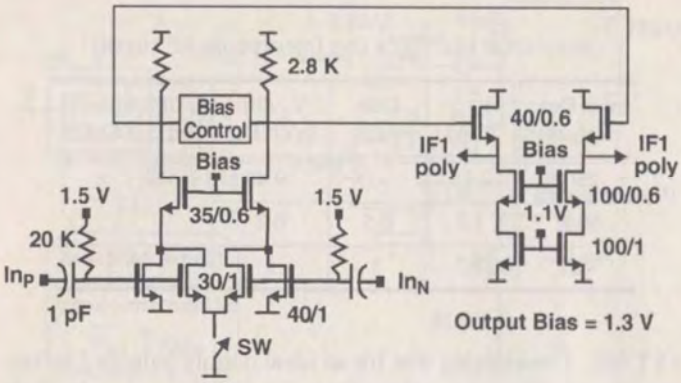

Fig. 9. IF1 amplifier.

TABLE II
SIMULATION RESULTS OF THE IF1 AMPLIFIER AND BUFFER

W_{eff} (μm)	I_{bias} (mA)	Gain (dB)	V_n diff (nV/√Hz)	IIP3 (dBm)
40	6.2	6	4.6	15
70	8.5	10	3.5	10.5

curacy must be enough for 38-dB image rejection over a BW of 1.6 to 2.6 GHz, which covers the input 80-MHz tuning range of the first LO and allows ±25% safety margin for process spreads in the $R \times C$ defining the filter zeros. The capacitance at the LO input of the RF mixer loads the polyphase filter output, increasing loss in its passband. To overcome this, four on-chip inductors are placed at the LO inputs to resonate with this capacitance. LO1 inductors are made by three layers of metal in series for $L = 5.5$ nH, self resonance at 3.2 GHz, and $R_S = 14\ \Omega$ [14]. Simulations show that these inductors lower loss in the polyphase filter by 3.5 dB.

C. IF1 Amplifier and Polyphase Filter

The IF1 amplifier gain of 5 dB compensates loss in the IF1 polyphase filter and in the passive IF mixer. Furthermore, to avoid overload by adjacent channels, it drives the strongly frequency-dependent input impedance IF1 polyphase filter with low source impedance [7]. The first stage of the amplifier is common-source with 11-dB gain (Fig. 9); like the RF mixer, it uses a grounded source FET input stage to improve the linearity. Without cascode devices, the simulated IIP3 of the CS amplifier is about +24 dBm (referred to 100 Ω), so that at minimum gain of 11 dB, the resulting IIP3 is +12 dBm. A cascode suppresses r_{DS} nonlinearity. At an input bias of 1.5 V, the IIP3 of the CS amplifier with cascode (Fig. 9) improves to +28 dBm, now limited by the input FET nonlinearity.

The nMOS source-follower (SF) second-stage level shifts the signal to the 1.3-V bias required by the IF mixer. However, the output signal suffers loss and nonlinearity due to body effect. The bias current and the size of the input device are optimized for the required output impedance with best linearity. When loaded with the polyphase filter, its IIP3 is +27 dBm and gain is −4 dB.

To slide dynamic range, the effective size of the input MOSFETs is switchable from 40/1 to 70/1 μm. Table II shows the

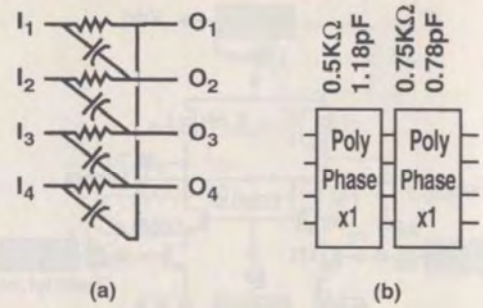

Fig. 10. IF1 and LO2 polyphase filters.

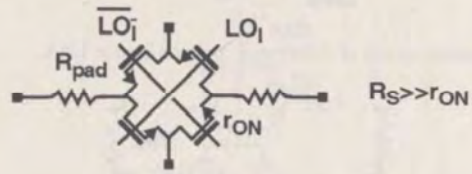

Fig. 11. Passive mixer with padding resistors.

characteristics of the IF1 amplifier with two gain settings. At the lower gain setting, the cascade loss is about 1.5 dB from the input of the IF1 amplifier, through the polyphase filters and mixers, to the input of the IF2 amplifier.

Following this amplifier, a two-stage RC polyphase filter rejects the image of the first mixer by about 35 dB. For this image rejection, the RF mixers should match in gain by about 2%, and the phase accuracy of the quadrature LO should be commensurate. The IF1 polyphase filter (Fig. 10) is designed for this image rejection over the required BW.

D. IF Mixer

The much greater challenge is in the IF mixers, which must reject the image by 60 dB after downconversion from 188 MHz to IF2. Now the mixer gain must match to 0.1% [7]. In a Gilbert-cell mixer, matching the transconductors to this level requires very large-area devices (>300 μm^2), or very strong degeneration with well-matched resistors. Since the high input frequency to the mixers requires a high f_T for the input devices, their channel length should be close to minimum. Large area then is obtained by scaling up width, resulting in a proportional rise in power consumption. Strong degeneration requires a large ratio of $V_{R,\text{degen}}/(V_{GS} - V_t)$, which is not practical at low supply voltage. For these reasons, Gilbert-cell-type mixers are suitable for moderate image rejection of up to 40 dB or so, but well-matched passive mixers are the better choice for higher image rejection.

One solution to improve gain matching of passive mixers, shown in Fig. 11, is to pad them with well-matched resistors. If the switch ON-resistance is much smaller than the padding resistor, the latter sets the mixer gain. The sensitivity to the switch ON resistance is now lower by the factor $R_{\text{Pad}}/r_{\text{ON}}$. The polyphase filters surrounding the IF mixer naturally pad the mixer switches with well-matched impedance.

As the mixer transitions from ON to OFF, its r_{ON} rises and will exceed R_{Pad}. To avail the benefits of padding, this transition interval must be made as sh[illegible] the LO

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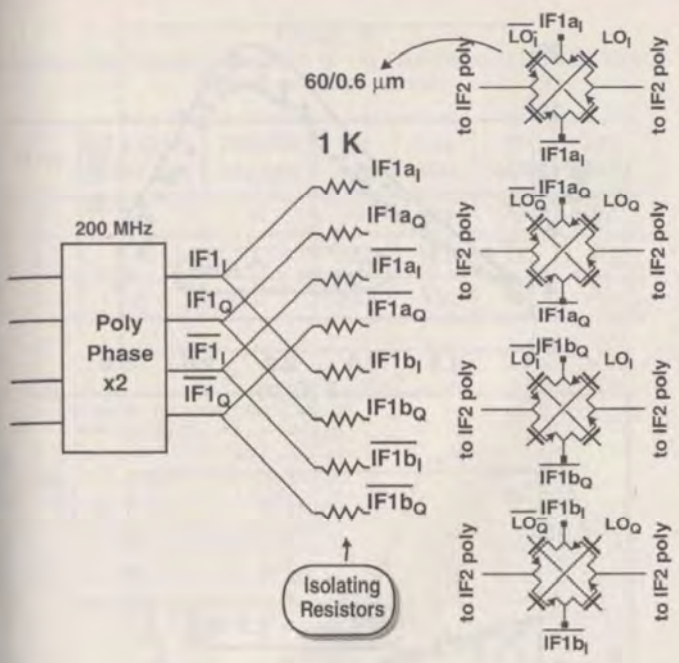

Fig. 12. Isolating resistors before the passive 4-mixer structure lower loading between the differential inputs, and undesired charge sharing between the capacitive loads.

period. If the shortest transition time is limited by, say, the rise-time of CMOS inverters (0.3 ns here) which drive the mixers, the longer the LO period, the better the suppression of FET mismatch. Thus in 0.6-μm CMOS, mixers that must reject the image by 60 dB should not be switched at LO frequencies higher than a few hundred megaHertz. This justifies the choice of the dual-conversion in this receiver.

When passive mixers are configured into the single sideband select arrangement implementing the relationship $I \times I + Q \times Q$ and $I \times Q - Q \times I$, where the terms in each product refer to the IF input and the LO, the four nonunilateral switch MOSFETs short together the differential inputs. In other words, the circuit driving the mixers is loaded by a small resistor $2.r_{ON}$, leading to large attenuation, which is overcome by dissipating more power in the driving circuit. To circumvent this problem, isolation resistors between the mixers can raise the impedance between differential inputs, as shown in Fig. 12 [7]. The resistors raise the total conversion loss of the passive mixers from 4 to 5.5 dB, but this is acceptable. Simulation shows that the loss is 1.5 dB higher if the isolating resistors follow the mixers.

The sources/drains of the switch FETs are biased at 1.3 V. With $W/L = 60/0.6$ μm and 3.3-V gate voltage, r_{ON} is 70 Ω for each switch. CMOS inverters driving the LO port switch from 0 to V_{dd} (3.3 V). Isolation resistors are 1 kΩ, and the polyphase resistor after the mixer 5.6 kΩ. Thus, the padding impedance is two orders of magnitude larger than r_{ON}. Now the mixer FETs may mismatch by up to 8% without degrading image rejection.

E. IF2 Amplifier and Polyphase Filter

At IF2, this receiver amplifies and filters in scalar, not quadrature, paths. Therefore, to avoid spectrum folding around 0 Hz, IF2 must be chosen higher than BW/2, where BW is the bandwidth of the widest channel. This has important repercussions

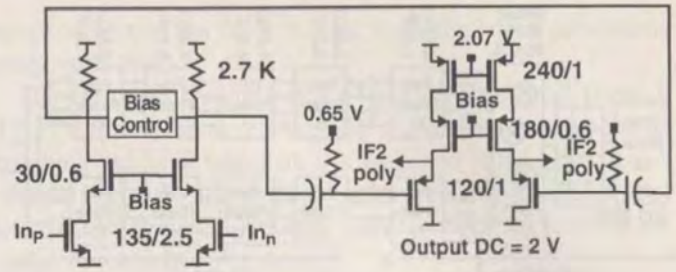

Fig. 13. IF2 amplifier.

on the design of the IF2 polyphase filter [7]. For uniform image rejection across the band, the higher the signal f_{max}/f_{min}, the more polyphase filter stages needed in cascade. Theoretically with perfect components, a five-stage polyphase filter is needed to reject the image by 60 dB over a BW of 3.5 to 20 MHz. This covers the maximum channel BW of 10 MHz, and allows $\pm 25\%$ margin for process spreads if IF2 = 10 MHz.

Various options were considered to customize the polyphase filter to the widely varying channel bandwidths, such as scaling IF2 with bandwidth, or switching the elements of the polyphase filter. None were found beneficial in terms of reducing chip area.

The passive polyphase filters and passive mixers are lossy. Without amplification, their total loss exceeds 20 dB and will degrade the overall receiver NF. If the IF1 amplifier were solely to compensate this loss, the 20-dB gain would degrade both SFDR and blocking dynamic range. Instead, gain is distributed between the IF1 amplifier and a second amplifier, which is optimally placed where the losses preceding and following it are roughly equal. This point is after the first stage of the IF2 polyphase filter. The amplifier gain is 10 dB, and it drives the polyphase filter with low output impedance (Fig. 13). In addition to the requirements of modest power consumption, adequate DR, gain, and low output impedance, any amplifier inserted in the two I and Q branches of the polyphase filter must also match in gain and phase to 0.1% for 60-dB image rejection. This requires very careful design. From [16] $\sigma_{Vt} = 10$ mV/$\sqrt{\text{WL}}$ for the 9-nm gate oxide of this process. From [17] σ_β/β is 0.7%/$\sqrt{\text{WL}}$ for 0.8-μm CMOS, which is used as a pessimistic estimate for 0.6-μm CMOS. As the desired amplification bandwidth at IF2 is about 20 MHz, long-channel FETs with low f_T may be used. The gate area of these FETs is large at modest W/L ratios, which means that good matching is achieved without prohibitive bias current. The final amplifier, shown in Fig. 13, was designed using Monte Carlo simulations in HSPICE, with an added safety margin of 2×.

The input of the common-source stage is biased by the output of the IF1 amplifier through the preceding polyphase filter and passive mixers. The source follower output is ac coupled. The coupling capacitor between the two stages creates zero at dc and pole at about 5 MHz. This partly compensates high-frequency droop in the polyphase filter passband. All four IF2 differential amplifiers drain a total of 9.5 mA. Its input-referred noise, including the filter load, is 6.4 nV/$\sqrt{\text{Hz}}$, and IIP3 is +15 dBm referred to 100 Ω. Now the loss from the input of the IF2 amplifier to the output of the IF2 polyphase filter is only 1 dB.

On the chip, all amplifier FETs are placed in the same orientation, and dummy stages on both sides of the amplifier array

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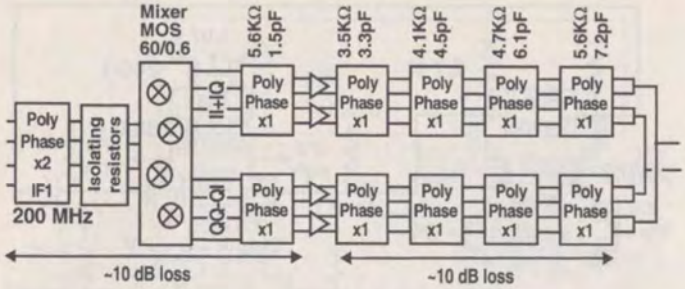

Fig. 14. Complete image reject chain.

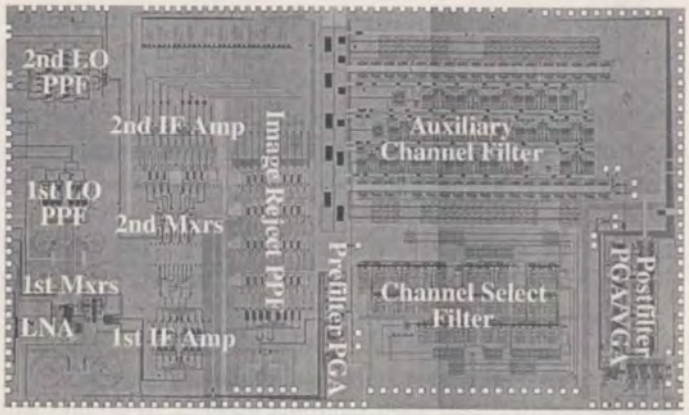

Fig. 15. Chip photo of integrated receiver.

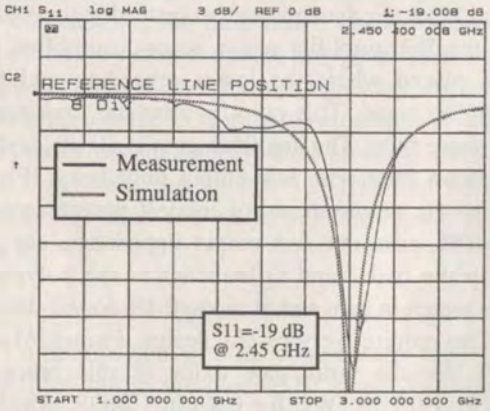

Fig. 16. Measured and simulated s_{11} for packaged LNA test chip.

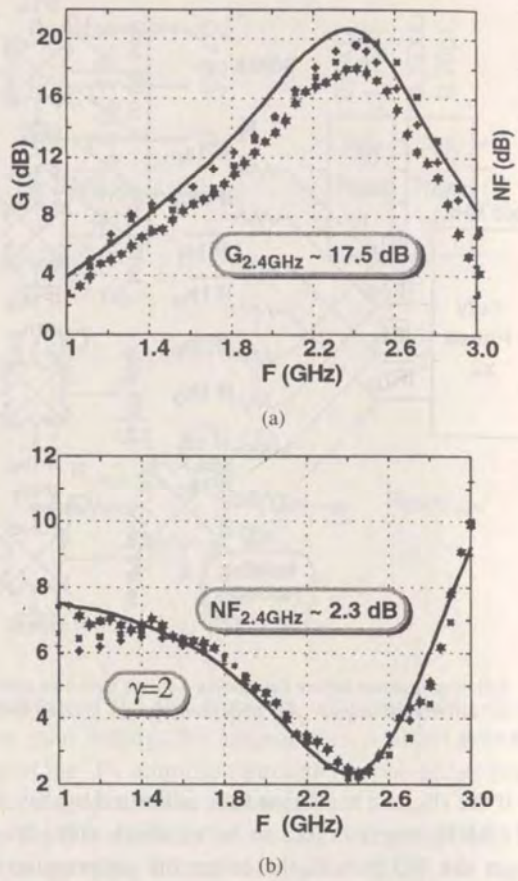

Fig. 17. Simulated (solid) and measured (points) results of three samples for the stand-alone LNA. (a) Gain. (b) NF.

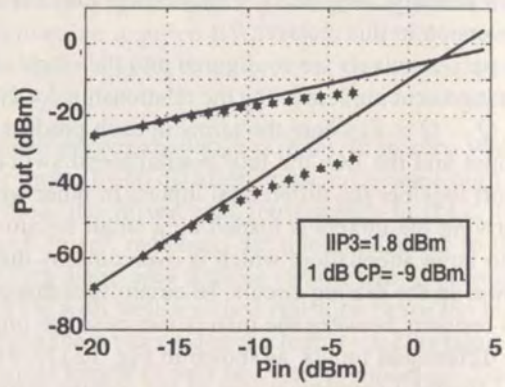

Fig. 18. Input-referred third-order intercept point (IIP3).

protect against nonuniform lithography at the boundary. A wide common-ground line lowers stray IR voltage drop, which would introduce mismatch. The layout is on a common centroid to cancel linear processing gradients.

The resistance tapers up in the polyphase filter stages, as shown in Fig. 14, to lower passband loss [7]. The resistance of the fifth stage, where the signal is attenuated most after IF2 amplification, as well as resistance in the first stage, prior to amplification, together determines total noise. The optimal ordering of the polyphase filter stages to best balance loss, noise, and loading is found through simulation.

V. Measurement Results

Fig. 15 shows the die photograph of the complete receiver. It is implemented in a 0.6-μm single-poly triple-metal epi-CMOS process, operating at 3.3 V. The chip area is 20 mm^2. A stand-alone version of the LNA was fabricated to compare measured performance with simulation results. Fig. 16 shows the measured and simulated s_{11} of the LNA. The measured and simulated NF and gain for three samples of the LNA are compared in Fig. 17. Owing to careful noise modeling, an accurate model of the package parasitics, and the correct de-embedding procedure [18] the NF is predicted very accurately. The measured gain is somewhat lower, probably due to a slight mistuning of the output circuit, and because loss in the drain junction diodes, which is known to lower the gain [19], was not simulated. The measured IIP3 of the LNA is shown in Fig. 18.

Table III summarizes the measured performance of front-end and downconversion part of the RX in three gain modes operating from a 3.3-V supply. This comprises all the blocks from

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TABLE III
MEASURED PERFORMANCE SUMMARY OF THE FRONT-END AND IMAGE-REJECT DOWNCONVERSION BLOCKS

Mode	2.2 GHz mixer gain	270 MHz amp gain	Idd (mA)	Gain (dB)	NF (dB)	IIP3 (dBm)
1	H	H	36	20.3	7.2	-9.5
2	M	L	32.4	14.3	11	-6.8
3	L	L	30.7	9.2	16	-3.4

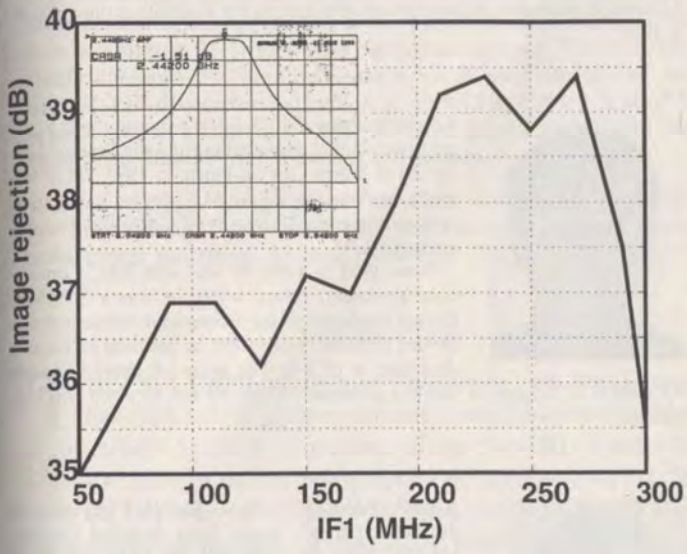

Fig. 19. Measured on-chip image rejection for RF mixer. Inset shows frequency response of antenna prefilter.

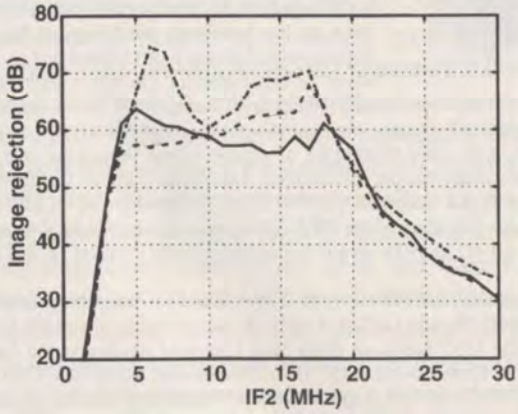

Fig. 20. Measured on-chip image rejection for the IF mixer.

the input of the LNA to the output of the IF2 polyphase filter. The measurement results of the IF strip (from input of the PGA1 to the output of the RX) and the whole RX are presented elsewhere [2]. Fig. 19 plots the on-chip image rejection of the RX at the first IF of 190 MHz. The wideband image rejection of 35 dB is close to the intended value, the remaining rejection being obtained from the stopband of the preselect filter. Image rejection at the second IF of about 60 dB is shown in Fig. 20 for three samples. The main difference from the results reported in a prototype earlier in [7] is that the IF2 amplifiers are embedded in the polyphase filters. It may be concluded that these amplifiers match to better than 0.1% in gain, as designed, to deliver this image rejection.

The chip was mounted in a 64-pin ceramic quad flatpack (CQFP) for all tests. Unlike the discrete chip components matching the input impedance of the stand-alone LNA, transmission line stubs and two capacitors are used in a differential arrangement to match the input impedance of the LNA in the complete receiver.

VI. CONCLUSION

A fully integrated double-downconversion low-IF superheterodyne RX is implemented in a 0.6-μm CMOS process. Together with the preselect filter, the circuit obtains a minimum 67-dB image rejection at the RF mixer. By means of polyphase filters and a double-quadrature downconversion, the image after IF downconversion is repeatably rejected by 60 dB on-chip. The gain of the RF mixer and IF1 amplifiers is switched to optimally slide the RX dynamic range. The front-end and downconversion blocks drain 35 mA from a 3.3-V supply and provide maximum gain and IIP3 of 20.3 and -3.4 dB, respectively. The minimum cascade NF is 7.2 dB.

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Andreas Roithmeier, biography and photograph not available at time of publication.

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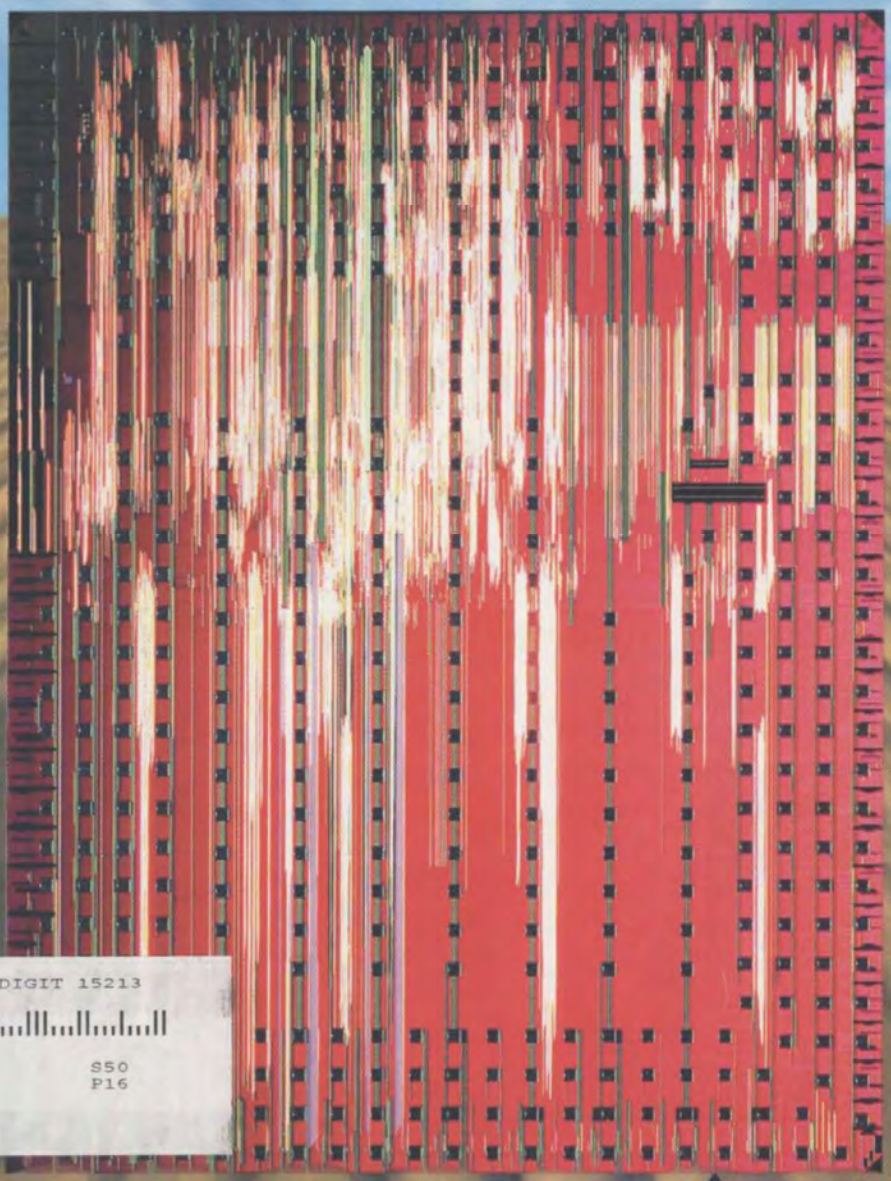

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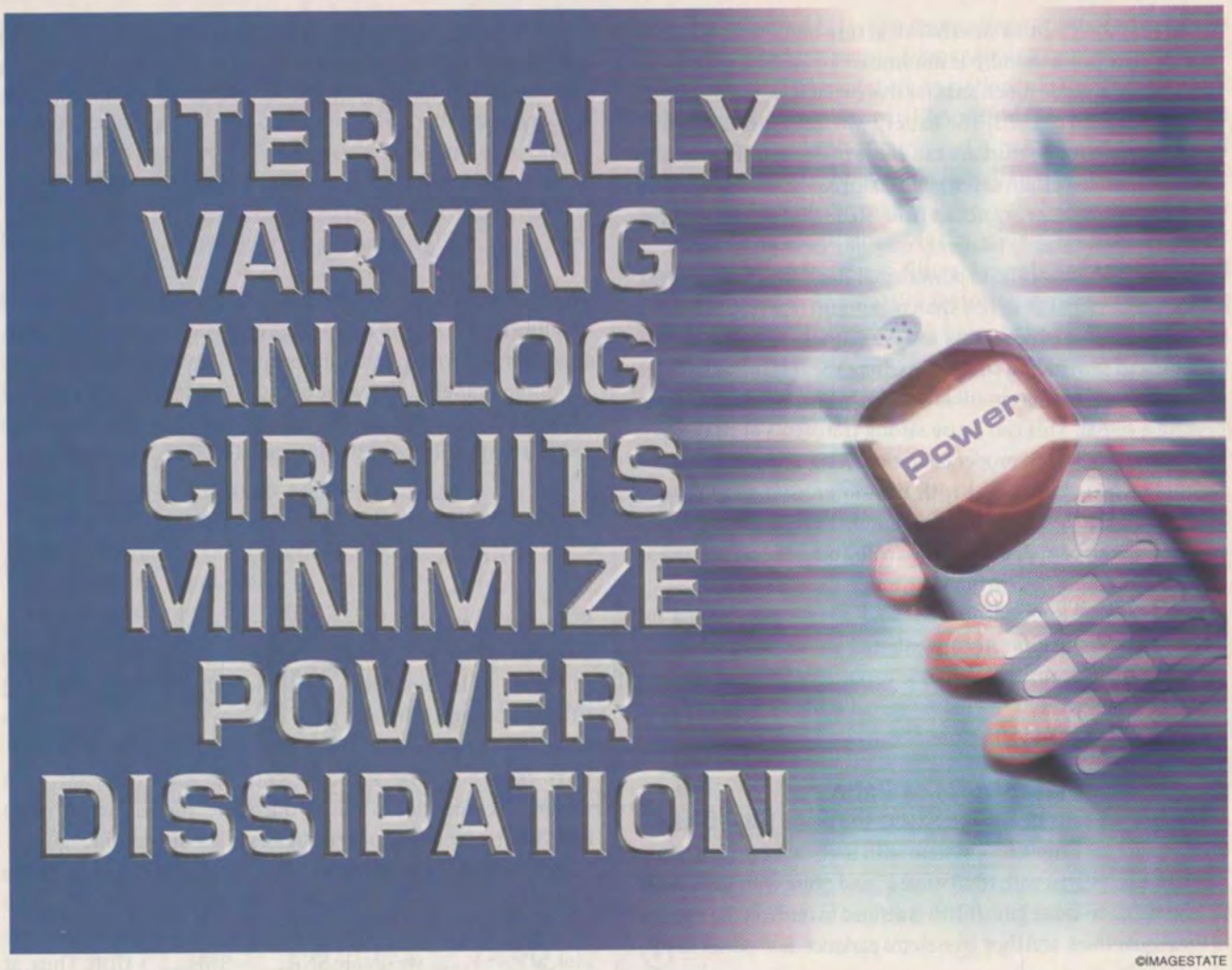
INTERNALLY VARYING ANALOG CIRCUITS MINIMIZE POWER DISSIPATION



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Significant Power Dissipation Savings Can Be Obtained by Allowing the Internal Circuit Attributes to Vary Dynamically As Needed for the Task At Hand

Y. Tsividis, N. Krishnapura, Y. Palaskas, and L. Toth

Low energy drain is key to the success of portable, battery-operated equipment. If the energy drain per task can be slashed down, battery life can proportionately be increased. Most conventional analog circuits are designed worst-case, for adequate performance while handling the most demanding tasks. This requires large power dissipation; when these circuits are called to perform less demanding tasks, they continue to dissipate the same large power unnecessarily. In other words, in such cases we are *stuck* with a fixed circuit.

The solution is to allow the *internal* attributes of the circuit to vary, depending on the task at hand. In this article we review several recently proposed techniques that make this possible. We call these circuits *internally varying*. (We cannot call these circuits "time varying," as in some systems context this term implies time-varying input-output behavior, which is not necessarily our goal.) The variables that control the internal variations can be independent variables controlled by the larger system, in which case we have an *adjustable* or *programmable* internally varying circuit; or, they can be derived from the signals being handled by the circuit, in which case we have an *adaptive* internally varying circuit.

As discussed below, internally varying circuits have in general a time-dependent power dissipation $p(t)$; the total energy drain W between times t_1 and t_2, is given by:

$$W = \int_{t_1}^{t_2} p(t)dt. \tag{1}$$

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By varying the circuit's internal structure and making it optimum for the task at hand, p is minimized for each task, and over time W can be made much smaller than what it would have been for conventional circuits. The battery will last much longer.

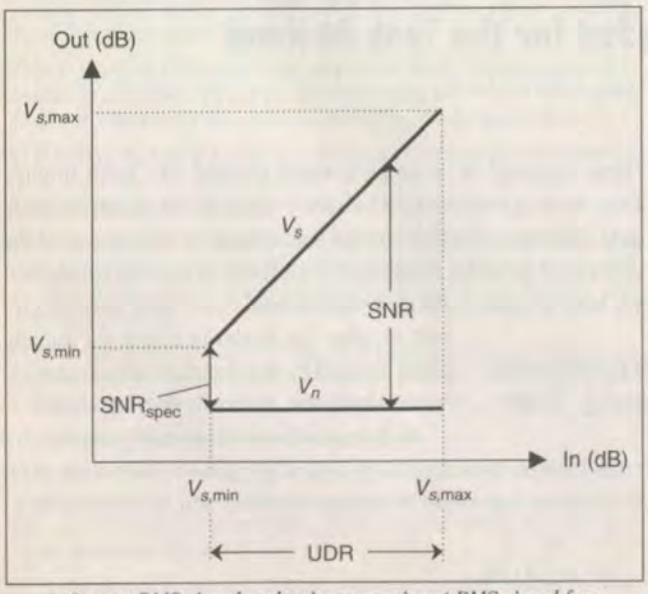
Varying a circuit structure can cause undesired disturbances at the output. In certain cases, such disturbances do not occur to a significant extent or are not an issue. Reducing the power dissipation in such cases is relatively easy; for example, it has been done for a very long time in power amplifiers, which sometimes are called to transmit at less than maximum power. Such cases will not be considered in this article. Rather, we will consider general and demanding situations where the internal attributes of a *dynamical* analog circuit are varied, while the circuit is processing a signal. This can cause strong transients at the output and can interfere with proper operation. A significant part of the techniques we discuss deal with how to *prevent or eliminate such transients*. Although much of our discussion is of a general nature that can be applied to many analog circuits, we will use as a specific example the particularly tough case of filters.

We first give some definitions and review the reasons for large power dissipation in conventional signal processing circuits. We then discuss the dynamic variation of several internal aspects of such circuits, including gain distribution, impedance levels, bias levels, and structure.

Signal-to-Noise Ratio and Usable Dynamic Range: Two Distinct Quantities

We consider for simplicity a system with unity voltage gain. For a given in-band signal with RMS value V_s and noise with RMS value V_n, the signal-to-noise ratio (SNR) is defined in terms of the squares of these quantities, and thus, in systems parlance, is a "power ratio":

$$\mathrm{SNR} = \frac{V_s^2}{V_n^2}. \tag{2}$$



1. Output RMS signal and noise versus input RMS signal for a unity-gain signal processor.

A simple specification often encountered is that this quantity be no less than a certain value, SNR_{spec}. The range of signal values over which this happens will be defined as the *usable dynamic range* (UDR):

$$\mathrm{UDR} = \frac{V_{s,max}^2}{V_{s,min}^2}. \tag{3}$$

We assume that $V_{s,max}$ is made as large as possible; the value of this quantity is such that an appropriate distortion measure (e.g., harmonic or intermodulation distortion) does not exceed a maximum allowed value. The value of $V_{s,max}$, together with the desired UDR, sets $V_{s,min}$ from (3). We assume that V_n is kept below this level so that SNR from (2) is just equal to SNR_{spec} at that point:

$$V_n^2 = \frac{V_{s,min}^2}{\mathrm{SNR}_{spec}} = \frac{V_{s,max}^2}{\mathrm{SNR}_{spec} \times \mathrm{UDR}}. \tag{4}$$

Since for conventional circuits the noise floor is constant, this guarantees that $\mathrm{SNR} > \mathrm{SNR}_{spec}$ at larger signal levels, as shown in Figure 1. In this figure we show $\mathrm{SNR}_{dB} = 10\log(\mathrm{SNR})$ and $\mathrm{UDR}_{dB} = 10\log(\mathrm{UDR})$, and their relation to $V_{s,dB}$ and $V_{n,dB}$, the latter two obtained as 20 times the log of their ratio to an arbitrary reference. The subscript "dB" in each case has been dropped in order not to clutter the figure. Ratios such as in (2) and (3) correspond to linear distances in the dB plots in Figure 1.

Notice that the maximum SNR is in general not equal to the usable dynamic range; it becomes equal to it only if SNR_{spec} is 0 dB, which is a very unlikely specification in practice. From the plot, at $V_s = V_{s,max}$ we obtain $\mathrm{SNR}_{max} = \mathrm{SNR}_{spec} + \mathrm{UDR}$. Thus, at large signal levels, UDR represents a "waste" above the required SNR_{spec}, which leads to major problems in the design of conventional circuits, as is now discussed.

Power Dissipation and Chip Area Waste in Fixed Circuits

The tradeoffs involved among SNR, chip area, and power dissipation in conventional continuous-time active circuits have been studied in the literature; see, for example, [1]-[5]. In their simplest form [2], these tradeoffs can be illustrated using a first-order RC low-pass circuit with bandwidth $1/(2\pi RC)$, in which the resistor noise power spectral density, equal to $4kTR$, is processed by the equivalent noise bandwidth of the circuit, $1/4RC$; thus, a mean-square noise of $4kTR \times [1/(4RC)] = kT/C$ appears at the output [6]. Therefore, low noise requires large capacitance (large chip area) and, for a given bandwidth, low resistance; the resulting large admittance levels require large currents in order to be driven at large signal swings, which results in large power dissipation. Finally, since these admittance levels are also proportional to band-edge frequency, so is power dissipation.

Similar results can be derived for larger circuits. For illustration purposes, we use here the case of a second-order bandpass filter with a high quality factor Q (ratio of center frequency to bandwidth), implemented with a resonator fed by an input de-

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vice; two implementations of this circuit are shown in Figure 2 [7]-[10]. The voltage gain is 1 at the center frequency. We will concentrate on the circuit on the left, which is implemented with transconductors and capacitors. The center frequency of this circuit is $G_m / (2\pi C)$. The tradeoffs between noise, capacitance, and power dissipation for this circuit have been studied quite early by Bloom and Voorman [1]. A detailed calculation of noise shows that kT / C again appears as above, along with some new factors [1]:

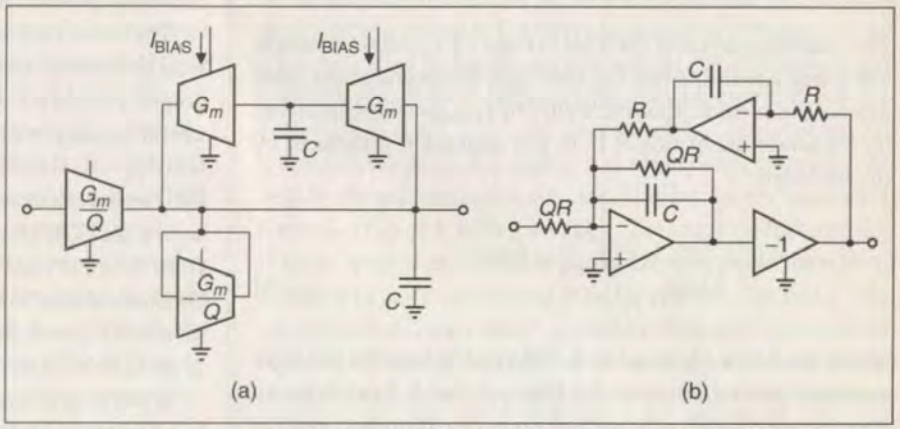
$$V_n^2 \approx 2Q\gamma \frac{kT}{C}. \tag{5}$$

Here the factor of 2 accounts for the contributions of the two large transconductors (which can be shown to be dominant), and Q appears due to the fact that there is a gain of Q between the equivalent input noise of these transconductors and the output. The quantity γ is the "excess noise factor" of the transconductors (typically 2 to 3). The value of C must be chosen to give a sufficiently low noise from (5), to satisfy the specs illustrated in Figure 1. Solving (5) for C, and using (4) in the result, we obtain:

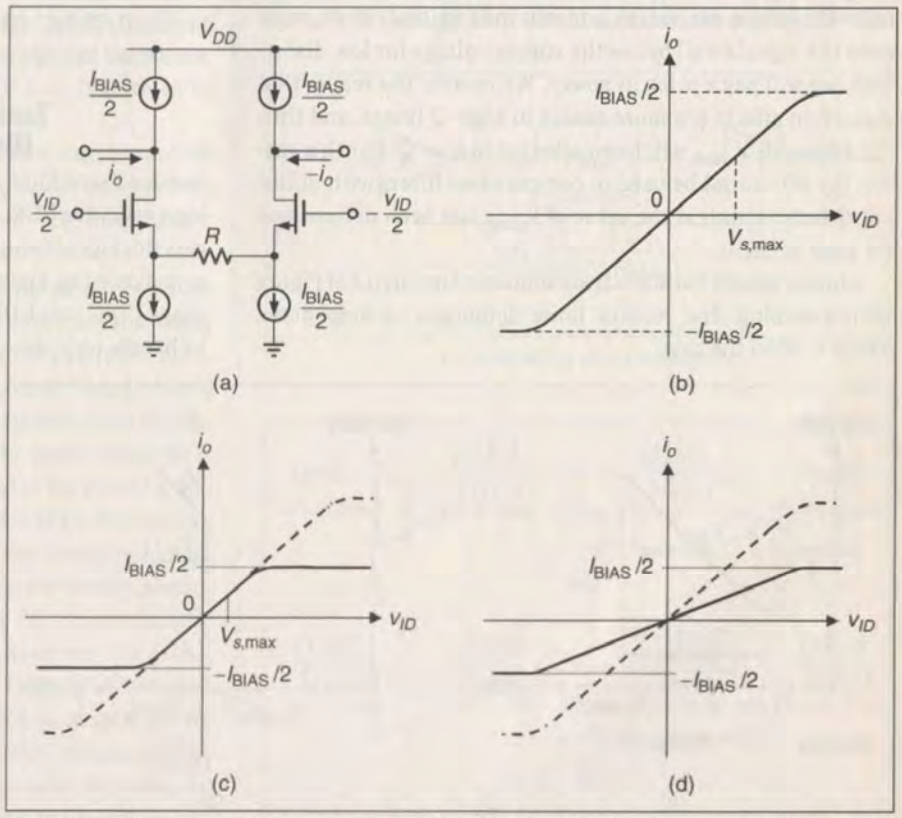
$$C \approx \frac{2Q\gamma kT}{V_{s,\max}^2} \times \mathrm{SNR}_{\mathrm{spec}} \times \mathrm{UDR}. \tag{6}$$

Thus, large UDR and small signal swings (necessary to achieve low distortion) require large capacitance. This is the reason that, in many integrated filters, especially ones with high-Q poles, the chip area is dominated by the capacitors. In fact, *for each 3 dB improvement in UDR* (a factor of 2 increase in this power ratio), *the capacitance area must be doubled.*

Figure 3(a) shows a simplified schematic of a transconductor that will be used as an example in this article. Such a transconductor would be appropriate for use in the balanced version of the circuit in Figure 2(a). Assuming that the transistor transconductance is much larger than the resistor conductance, the transconductance of the circuit is approximately equal to $1/R$. [The resistor can be replaced by a MOS transistor in the triode region, which behaves linearly as long as the input signal is balanced [11]. The gate voltage of this device can be used for limited transconductance tuning (e.g., to counteract tolerances and temperature variations).] The input-output characteristic is as shown in Figure 3(b). The value $V_{s,\max}$ used above is marked in the figure, and it has to be at a point well below clipping if low distortion is desired. This means that the maximum output current will be well below $I_{\mathrm{BIAS}}/2$. We should note here that, for a given transconductor nonlinearity, distortion in filters depends not only on signal level but also on the quality factor Q, generally increasing with the latter [12]. Thus, $V_{s,\max}$ needs to be kept especially low in high-Q filters.



2. Unity-gain second-order bandpass filters: (a) Transconductor-C (gyrator-C); (b) active RC (Tow-Thomas).



3. Balanced input-output tranconductor; (a) simplified circuit; (b) output current versus input differential voltage (the slope is equal to the transconductance, G_m); (c) effect of varying the bias current while keeping G_m constant; (d) effect of varying G_m by scaling all elements in (a).

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For future reference, we show in Figure 3 what happens if the bias current is changed [Figure 3(c)] and if the transconductance is changed (e.g., by changing the number of several transconductor units placed in parallel) [Figure 3(d)].

The transconductor bias currents in Figure 2(a), assuming class A operation and low distortion, must be larger than the maximum current these elements are expected to drive (which, for the two larger transconductors, is approximately the capacitor admittance at the center frequency times the maximum peak voltage) by a factor that we will denote by b (e.g., 3 to 6):

$$I_{\mathrm{BIAS}} = b \times 2\pi f C \times \sqrt{2} V_{s,\max}. \tag{7}$$

The total bias current of the filter in Figure 2(a) is approximately twice this amount, since the two large transconductors draw most of the current. This, multiplied by V_{DD}, gives an expression for the power dissipation P. If, in this relation, C is replaced by (6), we obtain:

$$P \approx akTQf \times \frac{V_{DD}}{V_{s,\max}} \times \mathrm{SNR}_{\mathrm{spec}} \times \mathrm{UDR} \tag{8}$$

where the factor a is equal to $8\sqrt{2}\pi b\gamma$ and in practice can have a value of several hundred. We thus see that P, in addition to being proportional to the center frequency, is proportional to the UDR; *improving the required UDR by 3 dB requires doubling the power dissipation!* The factor $V_{DD} / V_{s,\max}$ results from the above derivation and reminds us that, if we must keep the signals well below the supply voltage for low distortion, we will pay a price in power. We remind the reader that distortion effects are more severe in high-Q filters, and thus the allowable $V_{s,\max}$ will be smaller for higher Q. For this reason (6)-(8) cannot be used to compare two filters with different Q factors, unless the value of $V_{s,\max}$ has been determined for each of them.

Similar results (with $\gamma = 1$) are found for the circuit of Figure 2(b), assuming that resistor noise dominates op-amp noise, which is often the case.

For high-order circuits, results similar to the above are found [3], [4]. Here the problems are compounded by the fact that each circuit block contributes noise, and this noise is especially large for filters containing high-Q poles, such as required, for example, for very narrow passband and/or very sharp transition characteristics. One can use the same formulas as above, with Q corresponding to the highest-Q pole pair, and appropriately changing the value of the constant a in (8), depending on filter order, architecture, and node voltage scaling strategy [13], [14]. Again, *the total capacitance and the power dissipation are proportional to the required UDR*, but the constant of proportionality is larger. In the rest of this article we will continue to use the above relations for illustrative purposes.

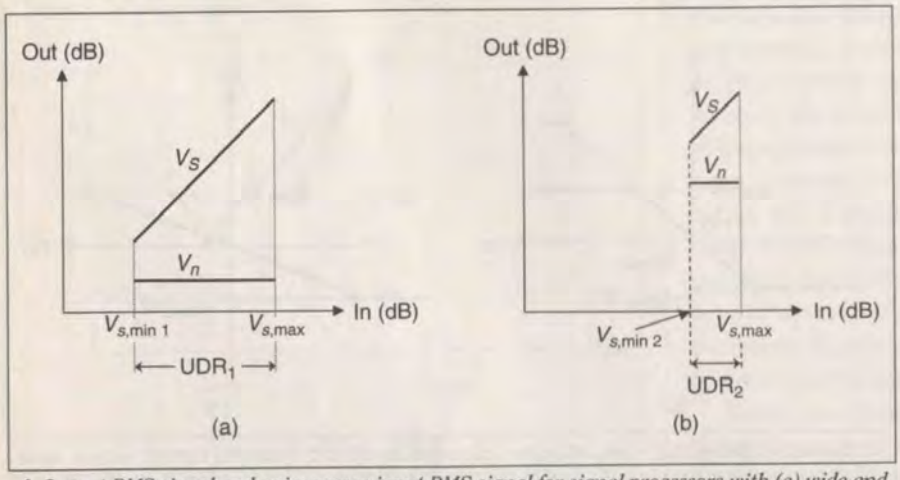
The above simple estimates suffice to demonstrate the practical limitations of conventional on-chip active filters. For example, consider a second-order section with Q of 20 and a center frequency of 10 MHz, $\mathrm{SNR}_{\mathrm{spec}} = 40$ dB, and operating with $V_{DD} = 3$ V and $V_{s,\max} = 0.5$ V. Assume $\gamma = 3$ and $a = 200$. We will contrast two cases, one with low UDR [Figure 4(b)] and one with high UDR [Figure 4(a)]. If UDR = 20 dB, the required C from (6) is 2 pF, and the resulting P from (8) is 1 mW. If, instead, the spec calls for UDR = 60 dB, the capacitance becomes 20,000 pF and the power 10 W, either of which would rule out an integrated implementation.

It can thus be appreciated that, in integrated filter design, we can run out of pF and of mW pretty quickly. The reason can be traced to the fixed nature of conventional circuits. In the rest of this article, we review several techniques through which the internal attributes of the circuits can be varied, thus making possible drastic savings in chip area and/or power dissipation.

Technique 1: Companding (Dynamic Gain Scaling)

Assume that a filter must satisfy specs as in Figure 4(a), requiring a very wide UDR, denoted by UDR_1 in that figure. We can process this signal using a filter with a much narrower range UDR_2 as indicated in Figure 4(b), if we can first compress the signal range UDR_1 into UDR_2, process the signal with a filter designed to handle only this narrow range, and expand the range at the output back to UDR_1 (the extent to which this is possible may be limited if large "blockers" are present—see below). This process of compressing and expanding is called "companding." It has been used in telecommunications and audio recording for a very long time [15], [16], but its use in signal processing [17] is more difficult, as will be explained shortly.

Companding can be done as shown in Figure 5. Assume for simplicity that the filter has unit gain, that the signal is in the passband, and that the noise of the input and output gain elements is negligible in comparison to the filter noise. The input



4. Output RMS signal and noise versus input RMS signal for signal processors with (a) wide and (b) narrow usable dynamic range.

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and output gain blocks are controlled together, and their gains are inverses of one another (see below).

We consider two representative cases in Figure 6. In (a), the input signal is significantly smaller than what the filter can handle; g is thus made larger than unity (5 in this example), to increase the signal so that it remains well above the filter's noise floor. The output gain element attenuates the signal back to its original level and at the same time attenuates the noise by the same amount. In (b), the input is assumed to be as large as the filter can handle, so g is made equal to 1. The signal is sufficiently above noise, so that the output SNR is satisfactory. The output gain is also equal to 1 in this case, and both the signal and the noise pass to the output of the system essentially unchanged. In some cases, even larger signals can be handled at the system input, in which case g will have to be made smaller than 1. In all cases the same, narrow-UDR filter is used, since the signal presented to the filter is always kept large and therefore it does not require a low noise floor. Thus, the filter can be designed economically with small capacitors and low power dissipation. As expected from the above calculations, power savings by a factor of UDR_1 / UDR_2 can be achieved in the filter; for example, if the dynamic range is narrowed by 40 dB, the required filter dissipation can in principle be decreased 10,000 times! This savings is, of course, not attainable in practice for the overall system because the supporting circuitry will also require some power; the savings can be drastic nevertheless.

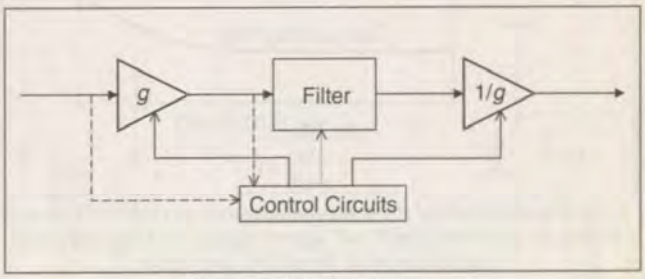
It can be seen from Figure 6 that, in all cases, the output SNR is approximately the same. This tendency toward flatness of the SNR characterizes all companding systems (see, for example, the measurements in [18]).

The key to the above technique is keeping the signal amplitude at the input to the filter constant at a near-optimum value (large enough to be well above the filter noise, but not so large as to excite the filter nonlinearities to a significant extent). Thus, g should in principle be inversely proportional to the amplitude of the signal at the input of the system. If the system input amplitude is known, an appropriate control can be applied to the g and $1/g$ elements to achieve this; if it is not known, an envelope detector can be used, connected to the input or output of the first gain element [17] (Figure 5), using well-known feedforward or feedback automatic gain control (AGC) techniques [19]. (In the special case where the filter is the IF or baseband filter in a receiver, the output gain block may or may not be necessary; the function of this block should be considered in the context of the AGC strategy of the receiver.) Depending on the signal characteristics, measures other than the envelope (e.g., the rms value) may be used, but using the envelope is safer, especially if the signal's crest factor is large and not precisely known. In general, the required circuits have release time constants corresponding to many signal cycles; this type of companding is referred to as "syllabic" companding, since in speech processing such time constants would be comparable to the duration of word syllables. Issues with the design and use of envelope detectors are similar to those encountered in AGC design [19].

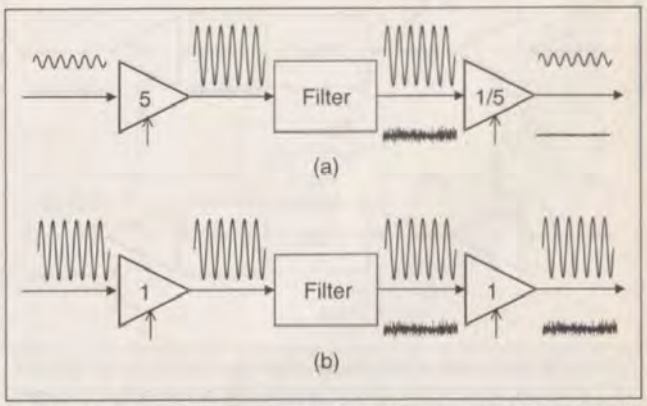
Varying a circuit structure can cause undesired disturbances at the output. These techniques deal with how to prevent or eliminate such transients.

The above technique can be applied also when the system's input and output variables are of a different type than those at the input and output of the filter. As an example, Figure 7 shows a system called to handle current signals [20]. These are converted to voltage by the input transconductor connected as a resistor ($v_1 = i_{IN} / G_{mc}$), are processed by the voltage-in, voltage-out filter in the center, and are converted back to current by the output transconductor. This system corresponds to the one in Figure 5, with $g = 1 / G_{mc}$. The transconductance G_{mc} is made variable and proportional to the system's input current envelope by using an envelope detector as above. The input resistor-connected transconductor could be replaced by a variable resistor, but using an input transconductor ensures good matching with the characteristics of the output transconductor.

Both transconductors are required to handle a large, fixed signal voltage. G_{mc} can be varied over wide ranges if transconductor cells are switched in parallel as necessary. The combined bias current will vary along with the combined transconductance, as illus-



5. Companding signal processor.



6. The main path of the companding signal processor of Figure 5 with (a) small input signal amplitude and (b) input signal amplitude increased by a factor of 5.

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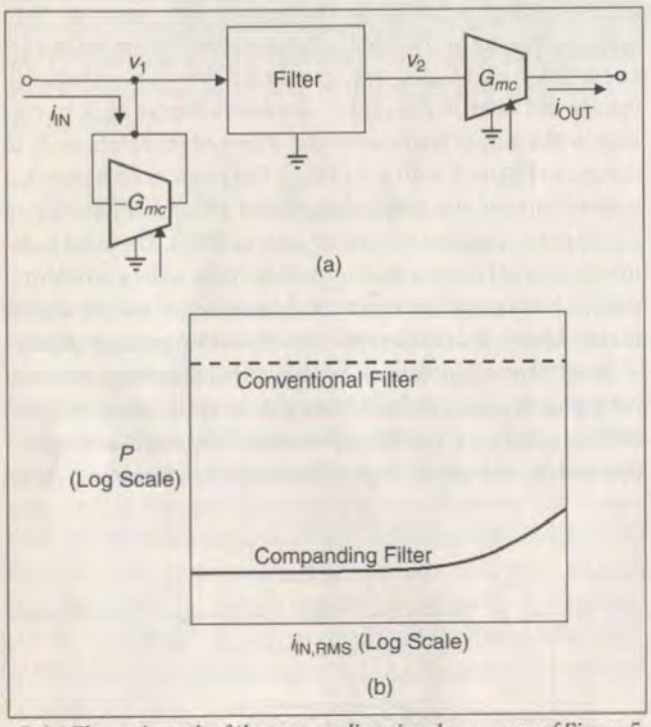
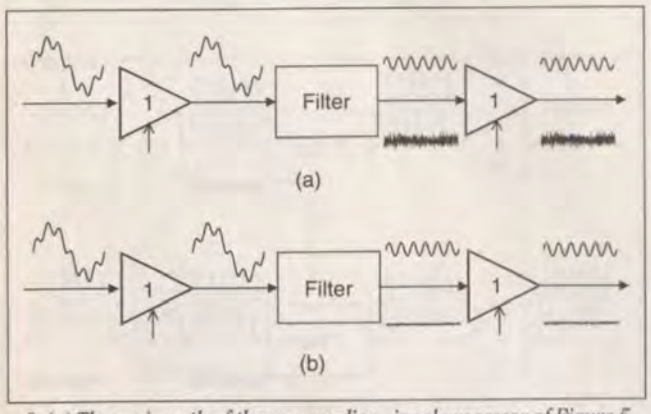
trated in Figure 3(d). Thus, if the signal is small, the total G_{mc} and I_{BIAS} will be small. Large power dissipation will be needed only when the signal is large. Figure 7(b) shows this behavior. Depending on the statistics of the input signal, drastic savings can be possible in the overall energy drain [20].

Leaving Headroom for Blockers

In certain applications (notably wireless), out-of-band signals can be much larger than in-band ones. This situation is depicted in Figure 8(a), where a large low-frequency blocker is superimposed on a small desired signal. Let the peak values of these signals be $V_{peak,blocker}$ and $V_{peak,signal}$, respectively. If the blocker were not present [Figure 6(a)], the system would have given g a value inversely proportional to $V_{peak,signal}$; however,



7. (a) The main path of the companding signal processor of Figure 5 in the case of current input and current output. (b) Resulting power dissipation versus input RMS amplitude.



8. (a) The main path of the companding signal processor of Figure 5 with a desired input of the same magnitude as in Figure 6(a), superimposed on a much larger out-of-band "blocker"; output signal-to-noise ratio is deteriorated. (b) The system in (a) redesigned to provide adequate output signal-to-noise ratio in the presence of the blocker.

in the presence of the blocker [Figure 8(a)], g will instead be inversely proportional to $V_{peak,signal} + V_{peak,blocker}$, so it will assume a value which will be smaller by the factor $(V_{peak,signal} + V_{peak,blocker}) / V_{peak,signal}$. Although the blocker is removed at the output of the filter, the signal power at this point has been weakened by the square of the above factor, compared to the case in Figure 6(a), and the SNR has been thus weakened by the same factor, as seen in Figure 8(a). To correct this problem, the design of the system has to be revised so that the noise floor is made smaller by the same factor, too, as shown in Figure 8(b); this means that the filter should be designed with an SNR of

$$\mathrm{SNR}_{filter} = \mathrm{SNR}_{spec} \times \mathrm{HR} \tag{9}$$

where HR is the headroom for blockers, defined by:

$$\mathrm{HR} = \left(\frac{V_{peak,signal} + V_{peak,blocker}}{V_{peak,signal}} \right)^2 . \tag{10}$$

Thus, if blockers with total peak value as large as that of the signal are expected, a headroom of 6 dB should be allowed; if blockers with total peak value 10 times that of the signal are expected, the headroom becomes 21 dB. This headroom comes at the expense of capacitance and power dissipation. Thus, all estimates as to how much savings companding affords those quantities must be lowered by the headroom. Appropriate optimization, in which the gain within the filter is made progressively higher towards the output (i.e., as the blocker is progressively rejected), can help [13], [14].

Avoiding Output Transients

The use of companding in filters encounters a difficulty not present in companding transmission systems. Filters are dynamical circuits; changes at the input appear as changes at the output with certain delay. Assume that, in Figure 5, the input signal strength suddenly changes, thus momentarily changing the signal at the input of the filter. The envelope detector senses the system input change and adjusts g to restore the filter input to its original level. The output element's gain, $1/g$, changes accordingly at the same time, which is *before* the change at the filter input has had a chance to propagate to the output. Thus, the output element's gain changes too soon, and an undesirable transient occurs at the system output [17]. In some applications this is not a problem, as these changes may occur before the time comes to process the useful signal (for example, during the preamble slot in certain wireless protocols). If, however, continuous service is desired, this transient must be eliminated or prevented in the first place. Several schemes that have been proposed to accomplish this are now described; some may prove to be more practicable than others.

State variable correction: The above problem can be avoided if the dynamics of the filter are properly taken into account. It has been pointed out [21] that if the input gain in Figure 6 is switched from a value g_{OLD} to a value g_{NEW}, no transient will appear at the output if all state variables are "up-

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dated" by the same factor involved in the change of g. Thus, the voltage on a capacitor must be changed at that instant, from a value v_{OLD} to a value $v_{NEW} = v_{OLD} \times (g_{NEW} / g_{OLD})$. This can be accomplished, for example, by charging the capacitors in a filter appropriately at the transition [21]. If, instead, g is not switched but rather is changed continuously, a likewise continuous modification of the state variables can be used; this problem has a general analytical solution [22], but the resulting circuits have proven not to be easy to design [23]. State variable correction is indicated in Figure 5 by the dotted arrow going from the control circuits to the filter.

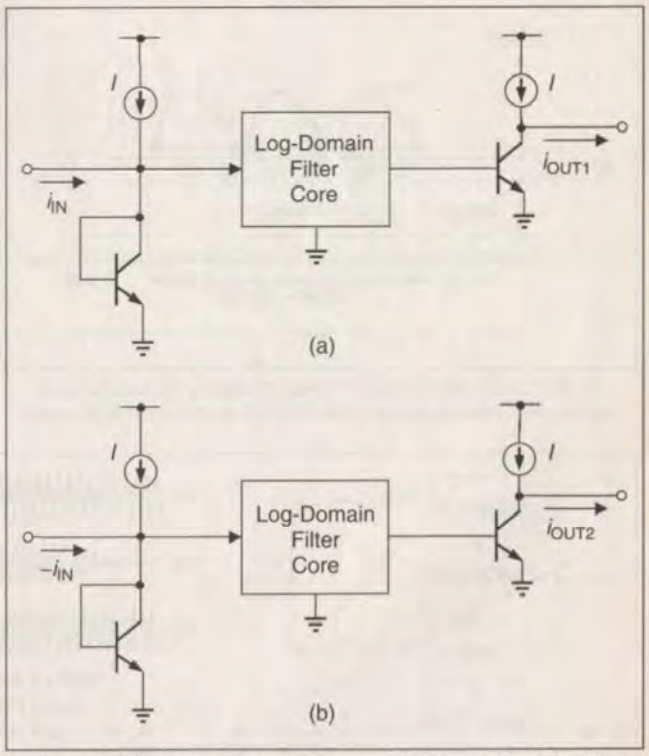
Zero-crossing switching: Consider a state variable v in the filter. According to the scheme just described [21], this value needs to be updated to $v_{NEW} = v_{OLD} \times (g_{NEW} / g_{OLD})$. If, however, we wait to perform this change at a moment that v crosses the time axis, $v_{OLD} = 0$ and thus $v_{NEW} = 0$, too. Thus, no updating is needed [24]. The implementation of this idea relies on accurate detection of zero crossings, which is complicated in practice, especially for high-frequency signals.

Feed-forward cancellation: Another way to solve the output transient problem is to allow the transient to occur but add to the output a second transient that is precisely the negative of the first [24]. To produce this second transient, a duplicate filter is needed; this filter is fed by the same signal as the main filter, until the time for the gain switching comes; then, the input of the second filter is switched to 0. Because, at the time of switching, this second filter has all its state variables identical to those in the main filter, it can be shown that the transient that occurs at its output, if multiplied by an appropriate gain, is opposite from that in the main filter; adding the two filter outputs results in elimination of that transient, and the signal appears undisturbed by the gain switching.

Combining companding with log domain: Consider again the system of Figure 7(a), using transconductors at the input and output. The simplest transconductor is a single transistor. If the two transconductors are replaced by bipolar transistors, we obtain the system of Figure 9(a). The transconductors are now of course nonlinear, and the total voltage at the filter input is proportional to the logarithm of the instantaneous transistor current. It can be shown that if this voltage is processed by a "log domain" filter core, and the filter's output is processed by an exponential nonlinearity as in Figure 9(a), the input-output behavior is linear [25], [26] (this is a perfectly sound concept, which has been widely misunderstood). Now, to vary the gain of the input "transconductor" in Figure 9(a), one can vary its bias current in proportion to the signal envelope [27], since $g_m = qI / kT$ for a bipolar transistor. If a second filter is used as shown in Figure 9(b), with the same bias but the opposite input signal, the transients due to the bias change are the same at the output of both filters; thus, if the *difference* of the two outputs is taken, this transient cancels out, although the signal components add [28]. Key to this idea is the fact that, since the two systems are *linear* from input to output, both signal and bias are treated by them by one and the same transfer function. A chip using this approach [28] has been demonstrated to give a very large UDR, which approaches the fundamental limits of power dissipation of *passive* RC circuits with the same UDR! (Passive circuits do dissipate some power—from the input signal source.)

Divide-and-conquer: Rather than switching the gain elements in the system of Figure 5, one can use more than one path with different, but fixed, gain elements, as shown in the example of Figure 10(a) [29]. Here the gain elements are fixed. The three paths should be closely matched. Depending on the input signal, the path switched to the output is changed; large signals are processed by the top path, smaller ones by the middle path, and very small ones by the bottom path. Transients at the output are avoided, since the paths have the same outputs, as long as no large distortion occurs. Thus, for example, assume that as the signal is being processed by the middle path, its amplitude begins to decrease, which would result in a decreased *SNR* at the output; the decreased signal level is appropriate for the bottom path, which has a better output SNR thanks to the larger gain at its input (see Figure 6). Other than that, both paths produce the same output signal, so when the output is switched to the lower path, no transients occur. More sophisticated schemes can be used, where some filters are switched off part of the time to save power, while output transients can still be avoided by employing a special switching sequence [30].

The overall signal-to-noise-plus-distortion ratio (SNDR) of this system is as shown in Figure 10(b). As seen, the total UDR has been divided into three regions, and each filter is only required to handled a limited UDR. The sloping off of each curve



9. The circuit in Figure 7(a), with transconductors replaced by bipolar transistors and the main filter replaced by a log-domain core; two paths, driven differentially, are shown, with the output assumed to also be taken differentially.

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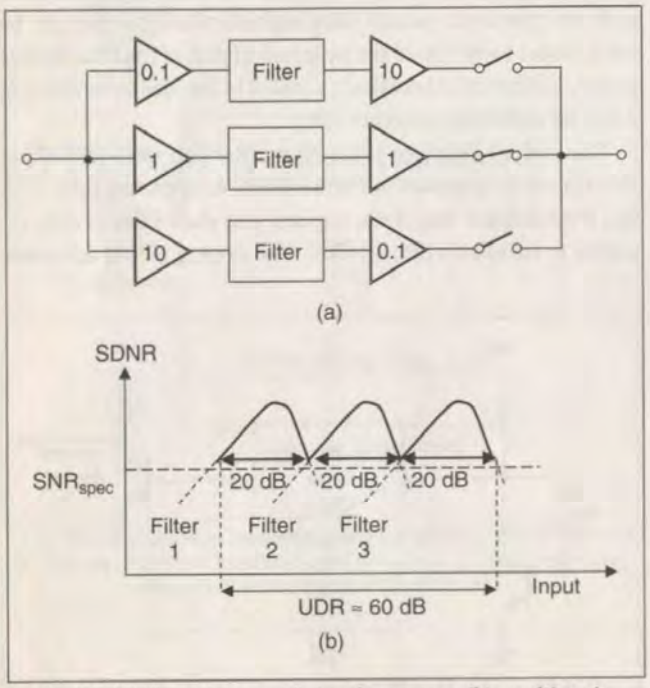
toward the right is due to increase in distortion. Consider the example presented earlier, where a total desired UDR of 60 dB resulted in a capacitance of 20,000 pF and a power dissipation of 10 W. Using instead the divide-and conquer technique, each of the filters need only handle a UDR of 20 dB, and it thus requires only 2 pF and 1 mW! Such savings more than make up for the fact that three filters plus supporting circuitry are used. Of course, if blockers are present, the required headroom (see above) will reduce the savings that can be obtained.

Companding techniques can also be applied to switched-capacitor circuits [31].

Technique 2: Dynamic Impedance Scaling

Consider a system designed to handle very small signals in the worst case, as in Figure 4(a). Due to the large UDR, the capacitance values will be large, as seen from (6). However, this worst-case signal situation may not be present continuously; part of the time, this same system may be called to handle large signals with limited UDR or SNR_{max}. This, for example, can be the case in wireless systems, when the desired signal happens to be strong and no strong blocker is present [32]. At those instances, the very low noise floor of this system is unnecessary and can be allowed to increase by scaling C down [33], resulting, for example, in the situation shown in Figure 4(b). Of course, the transconductances or conductances of the filter will have to be scaled together with C, in order to leave the frequency response unchanged. The reason one may want to do such impedance scaling becomes clear from (7): lowering capacitances and transconductances allows one to also lower I_{BIAS}, and thus the total power dissipation can be made small. This can also be seen from the transconductor characteristics in Figure 3(d). In principle, for every 3 dB reduction in UDR, the power dissipation can be cut to half.

One way to achieve the above scenario would be to use two filters, designed with different capacitance values, and place one or the other in service as required [34], turning the other filter off. This, however, causes transients at the output, which may take a long time to die out, especially in the case of filters with high-Q poles; the result may be loss of data.

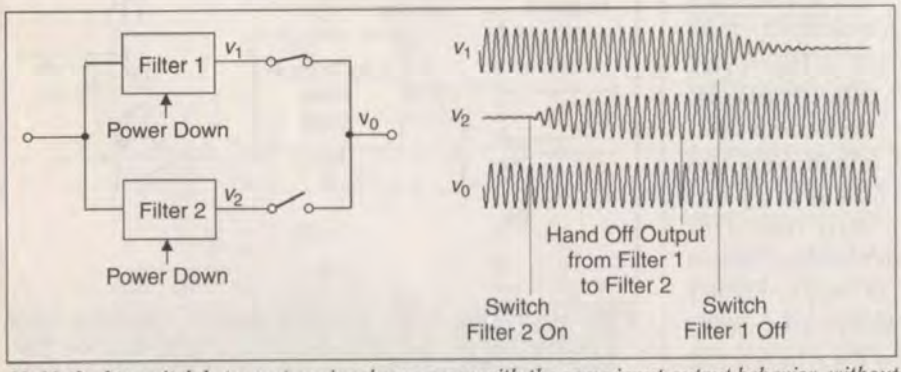


10. (a) "Divide-and-conquer" signal processor; (b) resulting signal-to-noise-plus-distortion ratio (SNDR) versus input RMS value.

Avoiding Output Transients

Delayed output switching: To prevent the system from seeing the output transients, one can use the approach in Figure 11. Before the output is to be switched, both filters are switched on; after the outputs of both filters become the same, the output can be handed off to the second filter, and then the first filter can be turned off [30].

Individual element switching: One can diminish the delay involved above by switching individual filter elements rather than entire filters. An example is shown in Figure 12. Here, when it is acceptable to increase the noise floor, the upper resistor and upper capacitor are switched out of the circuit, and the op amp's bias can be reduced (see also "dynamic biasing" below); the system now performs as in Figure 4(b). When the system is needed to process again signals with a low noise floor, the above two elements should be switched in; in order to avoid output transients, the op-amp bias is first increased; then the upper capacitor is switched between output and ground, so that its voltage becomes equal to that of the lower capacitor; and, finally, the two capacitors are connected in parallel. The system now performs as in Figure 4(a).



11. Method to switch between two signal processors with the same input-output behavior, without causing output transients.

Technique 3: Dynamic Biasing

The fact that a circuit has been designed to handle large signals does not necessarily mean that such signals will always be present. When they are not (i.e., when $V_{s,max}$ happens to be small) the bias currents can be reduced, as seen from (7). In many cases it is desirable to do this dynamically, without interrupting the filter operation. For example, in the transconductor of Figure 3 all four bias currents can be scaled down to-

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gether, without causing major output disturbances, provided that the transconductance of the MOSFETs remains sufficiently larger than the conductance of the resistor (if a triode-operated MOSFET is used in lieu of the resistor [11], its gate voltage is assumed to be referenced to its source and drain potentials); a second-order variation of its transconductance will be corrected by the automatic tuning system of the filter. This type of dynamic biasing leads to changes in the transconductor characteristic as shown in Figure 3(c). The biasing in certain op-amp architectures can similarly be varied without causing major disturbances at the output. In general, dynamic biasing decreases bias current values when they are not needed to handle large signal swings. The total current in a conventional and in a dynamically biased class A circuit, under changing signal amplitudes conditions, is illustrated in Figure 13. This technique is sometimes used in power amplifiers, but it is extendable to other circuits. The bias current is adapted to the average value of the signal, in a "syllabic" manner. (Another possibility is to use class AB, class B, or other related circuits in which the supply current is a function of the instantaneous value of the signal. These are not internally varying circuits in the sense considered in this article.)

We note that dynamic biasing is also encountered in the course of applying companding [27], [20], [28] (Figures 7 and 9) and/or dynamic impedance scaling (Figure 12).

Voltage-Mode Versus Current-Mode: A Key Difference

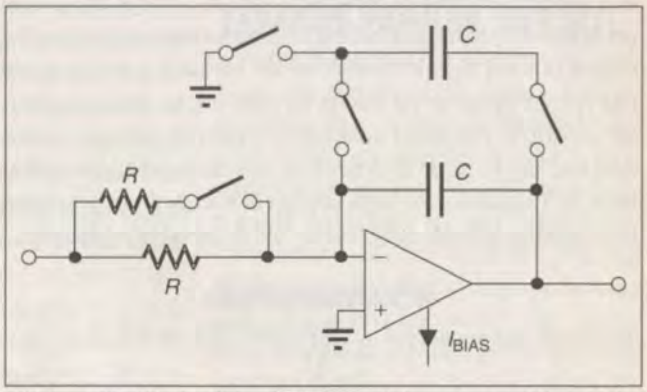
We have seen above that a relaxed SNR can result in power savings, if things are done properly. The mechanisms through which such savings can be accomplished can be very different from case to case. This will be illustrated by an example.

Consider first a voltage-mode circuit, such as a voltage amplifier or the filters in Figure 2. As was seen above, if the impedance levels are raised (thus making possible smaller power dissipation), the noise increases. The maximum signal that can be handled is not affected by impedance scaling. Thus, signal and noise versus power dissipation behave qualitatively as in Figure 14(a).

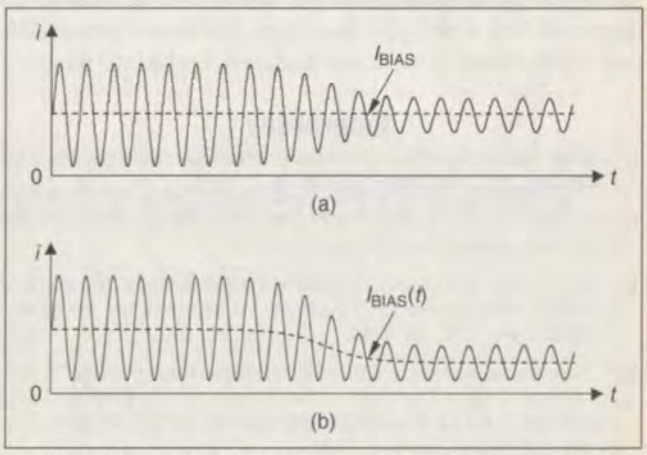
Consider now a current-mode circuit, such as a current mirror. If the bias current is decreased, the shot noise current (the rms value of which is proportional to the square root of the bias current) decreases as well; thus the behavior of noise with power dissipation is opposite from that in voltage-mode circuit. However, with decreasing bias current the maximum signal swing decreases proportionately; i.e., faster than the rms noise current decreases. The situation is thus as in Figure 14(b). It is seen that the decreased noise made possible by lowering the bias current can only be taken advantage of if the signal current happens to be small.

Technique 4: Dynamic Structure Variation

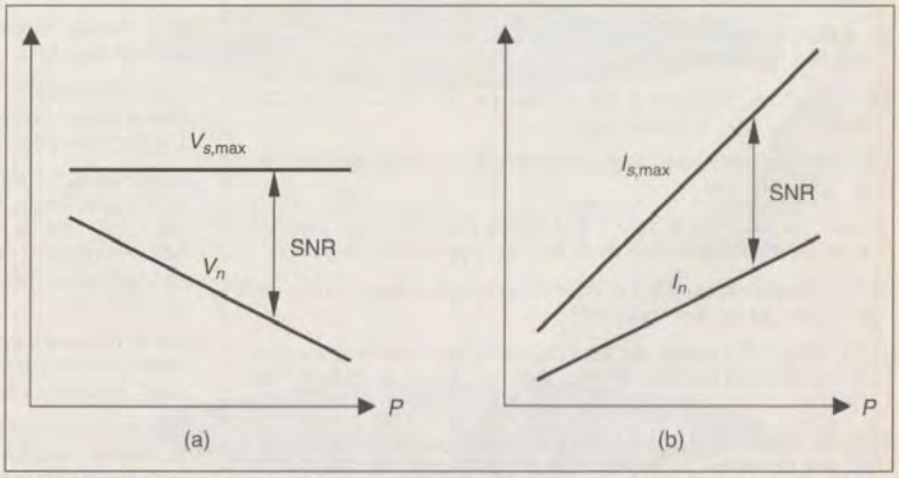
A fourth possibility is to dynamically vary the very structure of the circuit (e.g., change the architecture of a filter dynamically). A straightforward way to accomplish this is to use two or more filters with different structures and make sure that output transients are avoided using the technique in Figure 11. It may also be possible to use a single filter and vary its structure dynami-



12. An active RC circuit in which dynamic impedance scaling can be performed without causing output transients.



13. Typical bias and total signal currents in (a) a conventional circuit and (b) a dynamically biased circuit.



14. Mechanism through which the signal-to-noise ratio is improved with increasing power dissipation in (a) a voltage-mode circuit and (b) a current-mode circuit.

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cally, using techniques related to the ones discussed. This approach has not been investigated to any extent yet.

Conclusions

We have reviewed several techniques that make possible the dynamic variation of analog circuits internally, without affecting their input-output characteristics. A mixture of more than one of these techniques is appropriate in some cases. We used filters as a specific example of dynamical analog circuits and placed particular emphasis on avoiding or eliminating transients at the output of such circuits, which would normally have occurred due to such dynamic variations. By allowing for dynamic internal variations, the power dissipation of such circuits can be lowered and can be made to depend on how demanding the task at hand is. This allows for large savings of energy drain over time, thus making possible long battery life in portable equipment.

Acknowledgments

This work was supported by NSF Grant CCR-99-02781.

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