Fully Integrated Active *RC* Filters in MOS Technology

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Abstract—**A fully integrated continuous-time low-pass filter has been fabricated in CMOS technology. The device implements an active *RC* network using integrated capacitors and MOS transistors operated in the nonsaturation region as voltage-controlled resistors. The filter topology is fully balanced for good linearity and for good power supply rejection. The cutoff frequency is voltage adjustable around 3 kHz allowing compensation for process and temperature variations. With ±5 V power supplies a dynamic range of over 94 dB has been achieved.**

I. Introduction

THE basic problem that has hindered the straightforward monolithic realization of active *RC* filters has been the unpredictability of element values due to fabrication process and temperature variations. These variations can cause time constant errors of over 100 percent. Therefore, approaches based on fixed time constant implementation relying on absolute element values are naturally doomed to failure in the context of IC processes available today. However, these processes do allow for accurate realization of element value ratios and hence, of time constant ratios. If these time constants are voltage- or current-controlled, they can be automatically tuned to predetermined values by an on-chip control system; the latter uses an off-chip reference, such as a crystal clock [1], [2] or an external resistor [3]. Control circuits for achieving this automatic tuning have been discussed elsewhere [1], [2], [4], [5] and are not considered here; instead, we will focus on the implementation of the filters themselves.

Several filters have been proposed based on the above principle, and utilizing no switching. As adjustable elements they have used gyrators with variable junction capacitance [2], variable transconductance elements [1], [3], [6], and special operational amplifiers with a variable junction capacitor [7]. A common characteristic of all these approaches is that, like switched-capacitor filters, they are based on nonstandard techniques requiring specialized design. In contrast to this, the filters most extensively studied and best understood, namely those consisting of resistors, capacitors, and operational amplifiers (henceforth referred to as active *RC*), had not yielded to integration so far. In this paper, a method will be presented to integrate such filters on a chip, attaining excellent performance [8].

In active *RC* networks, the time constants can be made adjustable by using voltage-controlled resistors. MOS technology is naturally suited for this approach. Indeed, in this technology high quality capacitors and operational amplifiers are routinely implemented and the MOS transistor, operated in the nonsaturation region, is basically a voltage-controlled resistor. However, there is a potential major drawback in the arbitrary replacement of resistors with transistors. The strong nonlinearity of the MOSFET prohibits the use of large signals, limiting drastically the dynamic range [9]. In the following sections it will be shown how, by proper use of fully balanced networks, the bothersome transistor nonlinearities can be cancelled out, allowing the implementation of filters with wide dynamic range. The resulting filters operate in continuous time utilizing no switching, and thus they have none of the disadvantages associated with analog sampled-data filters. Specifically, there is no need for input antialiasing and output smoothing filters, no Nyquist rate limitations, no potential for operational amplifier high-frequency noise being aliased into the baseband, and no extraneous components at the output due to clock feedthrough. Further, in cases where switched-capacitor or digital filters are desirable, the filters proposed here represent an attractive candidate for implementing input antialiasing and output smoothing filters.

II. Technique for the Linearization of MOSFET Characteristics

A. Transistor Nonlinearities

The drain current of an n-channel MOS transistor in nonsaturation is given by [10]

$$I_D = 2K\Big\{(V_C - V_B - V_{FB} - \phi_B)(V_1 - V_2) - \frac{1}{2}\left[(V_1 - V_B)^2 - (V_2 - V_B)^2\right] - \frac{2}{3}\gamma\left[(V_1 - V_B + \phi_B)^{3/2} - (V_2 - V_B + \phi_B)^{3/2}\right]\Big\} \tag{1a}$$

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with

$$\gamma = \frac{1}{C'_{ox}}(2qN_A\epsilon_S)^{1/2} \tag{1b}$$

$$K = \frac{1}{2}\mu C'_{ox}\frac{W}{L} \tag{1c}$$

where I_D is the drain current in the triode region, V_C, V_B, V_1, V_2 are the gate, substrate, drain, and source potentials with respect to ground, W and L are the channel width and length, μ is the carrier effective mobility in the channel, V_{FB} is the flat-band voltage, N_A is the substrate doping concentration, C'_{ox} is the gate oxide capacitance per unit area, ϵ_s is the silicon dielectric constant, q is the electron charge and ϕ_B is the approximate surface potential in strong inversion for zero backgate bias (classically, this potential has been taken to be $2\phi_F$ with ϕ_F the Fermi potential, but ϕ_B is actually higher by several kT/q [11]). It is assumed that the source and the drain voltages V_1 and V_2 never become too low to forward bias the drain and the source junctions and never become too high to drive the device into saturation. The ground potential is defined such that V_1 and V_2 vary around zero. In that case the substrate voltage should be negative in order to keep the drain and the source junctions reversed biased (such a definition for ground potential is convenient when two power supplies of opposite values are present).

The 3/2 power terms in (1a) can be expanded in Taylor series with respect to V_1 and V_2. Then I_D can be written in the general form

$$I_D = K\left[a_1(V_1 - V_2) + a_2(V_1^2 - V_2^2) + a_3(V_1^3 - V_2^3) + \cdots\right] \tag{2}$$

where the coefficients a_1 are independent of V_1 and V_2 and are functions of the gate and substrate potentials (V_C and V_B) and all the process and physical parameters involved in the making of the device. The inverse of (Ka_1) is the small-signal resistance R of the transistor; it can be shown that

$$R = \frac{1}{Ka_1} = \left[\mu C'_{ox}\frac{W}{L}(V_C - V_T)\right]^{-1} \tag{3}$$

where V_T is the threshold voltage corresponding to $-V_B$ backgate bias. The value of R may be varied with V_C (henceforth called the control voltage); therefore, for small signals, the MOSFET can be used as a voltage-controlled resistor.

An indication on how the nonlinear higher order terms in (2) affect the transistor characteristics is given by the relative magnitude of the coefficients a_i compared to a_1. Fig. 1 shows the ratios $a_2/a_1, a_3/a_1$, etc., for common process parameters, as computed from (1a). A typical practical situation is illustrated by taking $V_2 = 0$ V, $V_1 = 1$ V, $V_C - V_T = 2$ V, $\mu C'_{ox}(W/L) = 10\ \mu A/V^2$ and $V_B = -5$ V (for usual power supplies of ± 5 V the n-channel transistor substrate is considered connected to the minimum available potential). Then, the first term in the right-hand side of

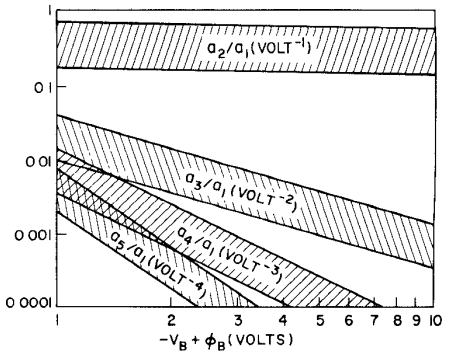

Fig. 1. Coefficients of the nonlinear components in the MOS transistor characteristics normalized to a_1 for different substrate biases and different control (gate) voltages. Each band corresponds to 4 V < $V_C - V_T$ < 1 V (bottom of band for 4 V); $\phi_B = 0.7$ V, $\gamma = 1$ V$^{1/2}$.

(2) is 20 μA, the second term is $-6\ \mu$A, the third term is $3\times10^{-2}\ \mu$A, the forth one is $-2\times10^{-3}\ \mu$A, etc. It is seen that the dominant deviation from linearity comes from the second-order term. In the next subsection a simple circuit technique for the cancellation of this term will be presented.

B. Nonlinearity Cancellation

The proposed technique will be illustrated by developing an active *RC* integrator in which MOSFET's are used instead of resistors. The classical implementation is shown in Fig. 2(a). The gain factor of this integrator is given by $(1/RC)$. Consider replacing the resistor with a MOSFET whose small-signal channel resistance is R, as shown in Fig. 2(b). Using the relation (2) with $Ka_1 = 1/R$ we have

$$V_{out} = -\frac{1}{RC}\int_{-\infty}^{t} V_{in}\,dt' - \frac{K}{C}\int_{-\infty}^{t}\left(a_2V_{in}^2 + a_3V_{in}^3 + \cdots\right)dt'. \tag{4}$$

The first term in (4) represents the ideal response of the integrator [identical with the response of the circuit of Fig. 2(a)] and the second one represents the error due to transistor nonlinearities. For large signals, the error term in the output becomes significant and produces excessive second-order harmonic distortion which limits the dynamic range. Considering the same transistor as in the example of the previous paragraph ($V_C - V_T = 2$ V, $V_B = -5$ V, coefficients a_i given as in Fig. 1) the total harmonic distortion (THD) is approximately 7.5 percent for an input signal of 2 $V_{p\text{-}p}$. If THD of less than 1 percent is desired, it is easy to calculate that input signals no larger than 250 $mV_{p\text{-}p}$ should be applied. However, if the $a_2V_{in}^2$ term in (4) were cancelled, the remaining integrator output error due to the higher order terms would be considerably less, resulting in only 0.03 percent THD for the same device and 2 $V_{p\text{-}p}$ signal level. A partial cancellation of this type was effectively accomplished in a circuit proposed quite early [12] which implemented a grounded linearized resistor with parasitic dc paths. A fully floating linearized resistor without dc

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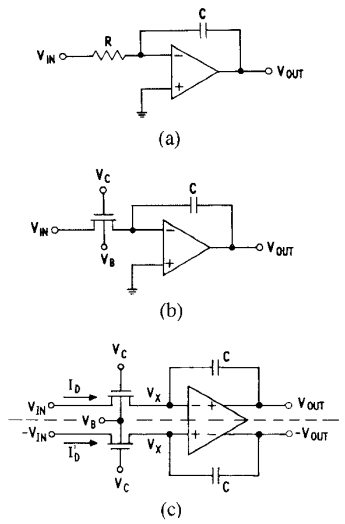

Fig. 2. (a) Classical active RC integrator. (b) Small-signal active RC integrator with variable gain factor. (c) Large-signal active RC integrator with variable gain factor realized as a fully balanced circuit.

parasitic paths was proposed recently [13]. Both schemes in [12] and [13] use extra circuitry in addition to the MOS transistor to implement the device linearization. It will be shown below that overall linearity can be accomplished without necessarily having to linearize every transistor separately and without the need for any extra circuitry; linearization schemes are considered further elsewhere [14]–[16].

The cancellation of the second-order term in the output of the circuit of Fig. 2(b) can be accomplished simply by using the fully balanced version of the latter as shown in Fig. 2(c). It consists of two identical capacitors, two identical transistors with identical gate and substrate bias, and one operational amplifier whose output voltages are required to be always symmetric with respect to ground (V_{out} and $-V_{out}$). The two input voltages are also assumed balanced (V_{in} and $-V_{in}$). One can regard this scheme as the combination of the circuit in Fig. 2(b) with its own mirror image taken with respect to the symmetry axis shown in Fig. 2(c).

The fully balanced integrator will now be analyzed. Assuming infinite op amp gain and zero offset voltage, the two inputs of the operational amplifier are at the same potential V_x (not virtual ground in general). Writing the KVL equations for the two outputs we have

$$V_{out}(t) = -\frac{1}{C}\int_{-\infty}^{t} I_D\,dt' + V_x \tag{5a}$$

$$-V_{out}(t) = -\frac{1}{C}\int_{-\infty}^{t} I_D'\,dt' + V_x. \tag{5b}$$

The solution for V_{out} is obtained by subtracting (5b) from (5a):

$$V_{out}(t) = -\frac{1}{2C}\int_{-\infty}^{t} \left(I_D - I_D'\right) dt'. \tag{6}$$

The values of the currents I_D and I_D' are given according to (2):

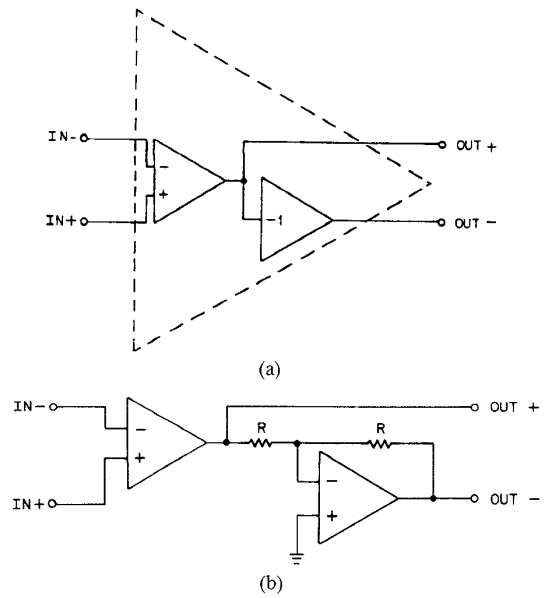

Fig. 3 (a) Definition of balanced output operational amplifier. (b) A possible implementation of the balanced output operational amplifier.

$$I_D = K\left\{a_1\left[V_{in} - V_x\right] + a_2\left[V_{in}^2 - V_x^2\right] + a_3\left[V_{in}^3 - V_x^3\right] + \cdots\right\} \tag{7a}$$

$$I_D' = K\left\{a_1\left[(-V_{in}) - V_x\right] + a_2\left[(-V_{in})^2 - V_x^2\right] + a_3\left[(-V_{in})^3 - V_x^3\right] + \cdots\right\}. \tag{7b}$$

When (7b) is subtracted from (7a), all the even order terms in V_{in} and all the terms in V_x cancel out:

$$I_D - I_D' = 2K\left[a_1 V_{in} + a_3 V_{in}^3 + a_5 V_{in}^5 + \cdots\right]. \tag{8}$$

Since the terms containing $a_3, a_5, \cdots$ are much smaller than the linear one (see previous subsection), the right-hand side of (8) is practically linear in V_{in}. Using (8) in (6), we obtain

$$V_{out}(t) \cong -\frac{1}{RC}\int_{-\infty}^{t} V_{in}\,dt'. \tag{9}$$

This result proves that the fully balanced integrator of Fig. 2(c) has practically the same transfer characteristic as the circuit of Fig. 2(a), even for large signals. It is emphasized that the circuit developed is not a differential scheme since it does not act on the difference of two arbitrary signals, say V_a and V_b; instead, $V_a = V_{in}$ and $V_b = -V_{in}$. The circuit thus accepts *one* balanced input (V_{in} and $-V_{in}$) and produces *one* balanced output (V_{out} and $-V_{out}$). The requirement of the operational amplifier to balance the output can be met as shown in Fig. 3(a). The circuit contains a high gain stage followed by an inverter. Clearly, no matter how it is connected in an external network, the two outputs will always be balanced. Fig. 3(b) shows a simple practical implementation.

In many filter applications multiple input integrators are

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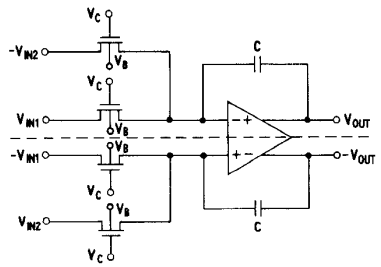

Fig. 4. Fully balanced differential integrator.

needed. Fig. 4 shows a fully balanced differential integrator. This time the circuit operates on two independent large signals: V_{in1} and V_{in2}, performing the integral of their difference. In a completely analogous fashion to our previous analysis, it can be shown that the transistors of each pair cancel their nonlinearities among themselves independently of the others, just as before. The same principle can be used to implement various other linearized filter building blocks of the active *RC* type, such as [16] summers (replacing the capacitors with MOS transistors), differentiators (interchanging the capacitors with the transistors), variable gain amplifiers (replacing the capacitors with resistors), etc. These filter building blocks are input–output compatible and can be connected to each other without any additional interfacing circuitry. Due to the automatic balancing at the output of the operational amplifiers, signal inversion is available at any node pair. The filters thus obtained are naturally balanced from input to output which is a desirable feature for good power supply rejection and increased signal level.

III. Nonidealities

When the ideas introduced in the previous section are applied in practice, the actual circuits will exist in the presence of many nonideal conditions such as device mismatches, errors in the signal balancing, operational amplifier offsets, etc. Analyzing the effects of the latter, it can be shown that the proposed circuits still exhibit good performance [17]; a similar conclusion is suggested by the experimental results to be presented in this paper.

In the previous section only the resistive part of the channel was considered and therefore, strictly speaking, the results derived there are valid only at dc. In fact there are parasitic distributed capacitances from the channel to the gate and to the substrate. These capacitances together with the channel resistance form an intrinsic time constant of the device which will influence the frequency response of the filter in which the MOSFET is used. In order to minimize this effect, the filter should be designed such that the intrinsic transistor time constants are much smaller than the actual time constants needed to be implemented. This strategy usually requires the use of transistors with channel length not larger than several hundred μm [17], or the use of large capacitance values. That is why this filtering technique is more naturally suited for high frequencies where shorter transistors are required.

It was mentioned before that the signal at the balanced operational amplifier inputs [V_x in Fig. 2(c)] is not at virtual ground due to the nonlinearities of the MOS transistors. The question arises whether this introduces any complications in the design of the op amps with respect to the input common mode rejection. It can be calculated [16] that for usual cases, the signal at the amplifier summing nodes is no more than a fifth of the integrator input signal. This indicates that the op amp common mode input signal is relatively small and does not pose any special design problems.

IV. Filter Design and CMOS Implementation

Based on the principles presented before, we have designed and fabricated a fifth-order low-pass filter in CMOS technology. The circuit, whose diagram is shown in Fig. 5, is the fully balanced version of a standard active *RC* ladder filter. It is synthesized from multiple-input balanced integrators identical with the one developed before (see Fig. 4). The gates of all transistors used as resistors are connected to the same potential V_C (control voltage). Varying V_C, one can change the frequency response in a manner equivalent to frequency axis scaling.

The process used is a Bell Laboratories standard twin-tub CMOS [18], having the capability to implement capacitors between the gate polysilicon and a second polysilicon layer. The design rules were based on 3.5 μm minimum linewidth.

Since MOSFET's and poly1-to-poly2 capacitors are readily available the only remaining circuit element needed is the balanced-output operational amplifier. The key specification in the design of this element is the proper matching of its outputs; they should be balanced within 1 percent [17] for low filter distortion. For speedy and reliable first-time design, the straightforward implementation shown in Fig. 3(b) was chosen. It uses two regular operational amplifiers and two p-tub resistors matched to each other. One problem with the use of p-tub resistors is their nonlinearity. to reduce this effect, they had to be designed with relatively large dimensions: 40×600 μm for approximately 35 kΩ; in this twin-tub CMOS technology the p-tub resistor nonlinearity comes from its width and length modulation with the signal (due to depletion regions in the junction between the p-tub and the n-tub). The operational amplifiers used are based on a previously designed circuit [19]. With respect to these op amps, two design factors had to be considered; capability to drive resistors and stability when connected as in Fig. 3(b) and in the actual filter. Since the filter MOST resistors are of the order of several MΩ (see below), the effective loads of the operational amplifiers are given by the p-tub resistors used in the inverters [see Fig. 3(b)]. Therefore, the output stage of the op amps was designed to drive low impedances which was reflected in a power dissipation of 2 mW per amplifier. Good output driving capability also increases the amplifier phase margin. This is desirable in order to avoid possible

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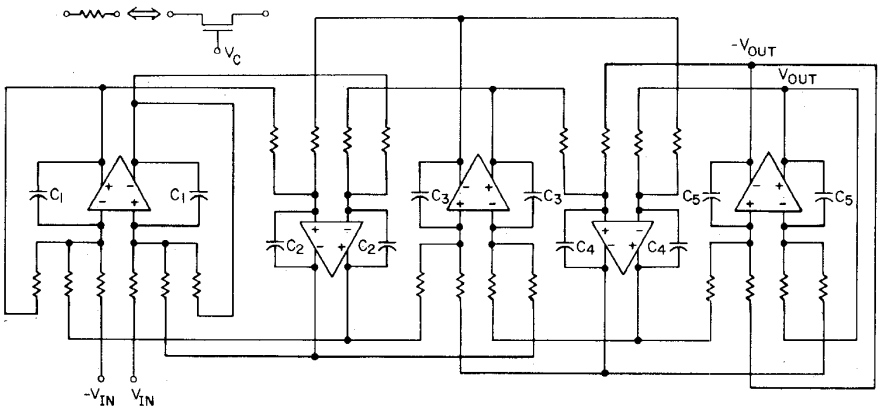

Fig. 5. Fully balanced active *RC* ladder filter (fifth-order all-pole).

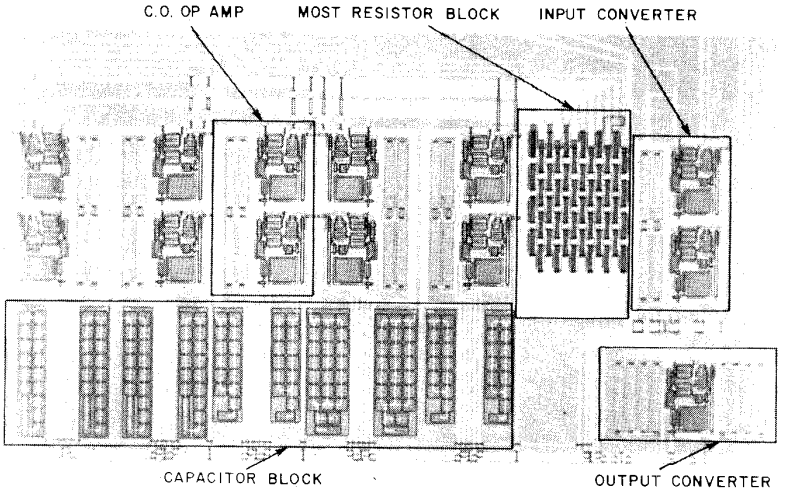

Fig. 6. Chip microphotograph.

stability problems caused by cascading two operational amplifiers inside a feedback loop. For the same reason, each op amp had to be overcompensated.

The pole locations of the filter were chosen to implement a Chebyshev transfer function with 0.1 dB passband ripple and a cutoff frequency tunable around 3 kHz. These specification require the implementation of large time constants. For practical values of total integrated capacitance, large resistance values must be used (on the order of a couple of MΩ). They were implemented with p-channel MOSFET's having very small shape factors: $W/L = 0.01$ realized with $W = 4$ μm and $L = 400$ μm (p-channel devices were used because they have smaller mobility than the n-channel ones, and thus larger resistances). For such device sizes, the parasitic capacitances to the gate and to the substrate cannot be neglected despite the fact that the actual filter time constants were designed to have much larger values than the transistor intrinsic time constants [16]. This distributed capacitance effect can be simulated simply by modeling each transistor as a series combination of many shorter transistors. Using such simulation it was found that the previous effect produces a peaking of almost 1 dB near the band edge. An empirical optimization was performed by perturbing the value of each capacitor separately and observing the effect on the computer simulated frequency response. The peaking could be eliminated very easily by increasing C_2 and C_4 by the same properly chosen amount. However, by doing this, the passband ripple was increased to about 0.2 dB near the band edge. It should be mentioned that this simulation predicted very well the behavior of the actual device and the above compensation worked as expected (see Section V).

Fig. 6 shows a microphotograph of the experimental chip. For precise control over the shape of the frequency response, proper accuracy in the ratios between the filter time constants had to be insured (1 percent accuracy is usually enough to give passband deviations of less than 0.1 dB for filters of this type because they are naturally insensitive to parameter variations). This was accomplished by matching both the resistors and the capacitors. Because there is better control over the latter, the MOST resistors were designed to be identical and the time constant ratios were implemented as capacitor ratios. In order to improve the MOST resistor matching, a layout strategy was used

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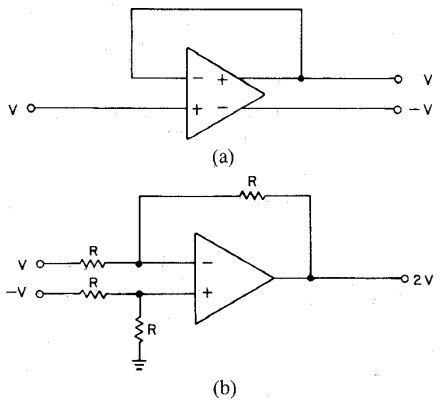


Fig. 7. (a) Unbalanced-to-balanced input converter. (b) Balanced-to-unbalanced output converter.

where each resistor was used split into four identical parts and the parts were interleaved with all the others (see Fig. 6). In this way local process variations influence evenly all resistors. The capacitors were fabricated over a grounded p-tub to reduce the power supply coupling through the substrate.

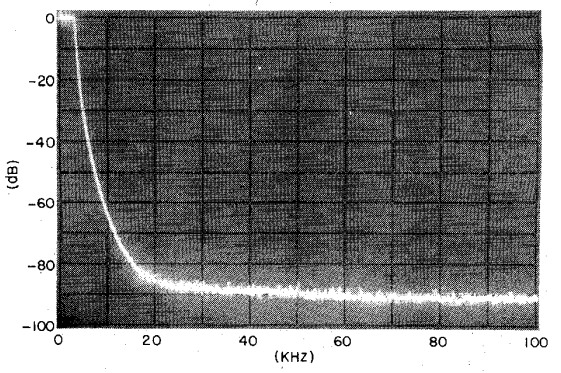
Included in the chip was also a "single-ended to balanced" input converter and a "balanced to single-ended" output converter. These were implemented with p-tub resistors, according to the diagrams shown in Fig. 7. The active chip area including the converters is 4 mm^2.

V. Experimental Results

All the data to be presented were measured for the complete system including the balanced filter and the input and output converters. The filter dc gain is 0 dB and the power supplies used were ± 5 V.

Figs. 8 and 9 show the frequency response of the filter with stopband and passband details. Input signals of up to 10 MHz were also applied and the filter stopband rejection was found always better than 60 dB; this reflects the continuous time nature of the system. Varying the control voltage V_C, the frequency response could be changed as shown in Fig. 10. Clearly, this effect is similar to a frequency axis scaling. A more exact characterization of the frequency response dependence on V_C is contained in Fig. 11; the experimentally observed cutoff frequency (-3 dB point) is plotted versus the control voltage. It should not be surprising that the curve is a straight line because the dependence of $1/R$ in V_C in (3) is practically of the first degree (neglecting the small variation of mobility with the gate voltage).

The linearity performance of the filter is illustrated in Fig. 12. Here, the measured total harmonic distortion is shown as a function of the signal level for different values of $V_C - V_T$. In generating these plots, the input signal frequency was taken at one-third of the respective filter bandwidth such that the second and the third harmonic distortion components fall into the passband. The points



(a)

Fig. 8. Filter frequency response.

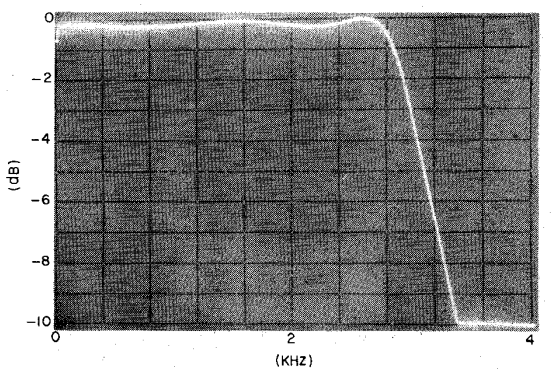


Fig. 9. Passband details of filter frequency response.

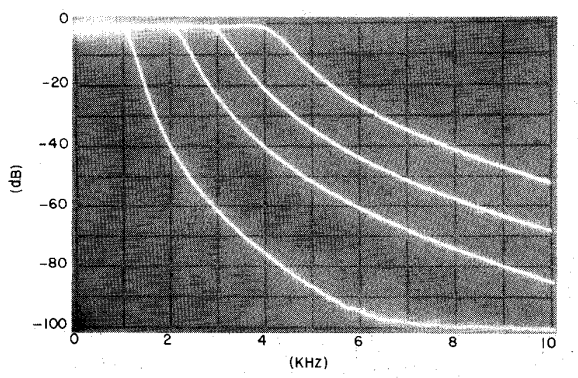


Fig. 10. Frequency response for various control voltages.

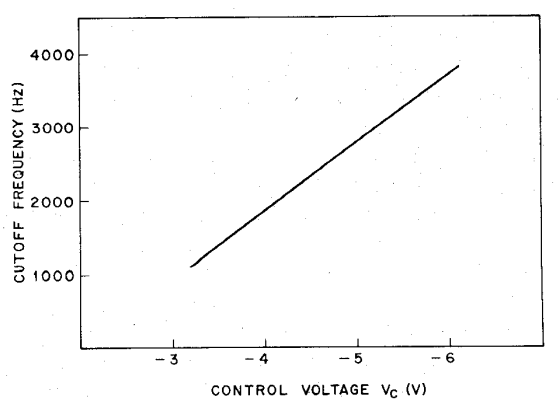


Fig. 11. Cutoff frequency (-3 dB point) versus control voltage.

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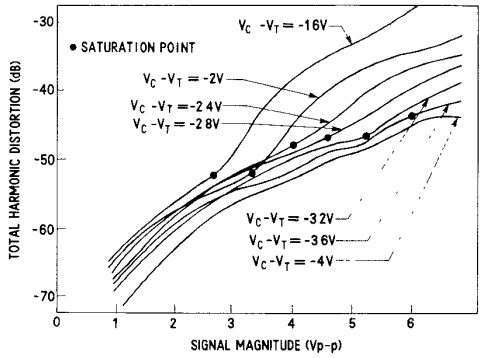

Fig. 12. Total harmonic distortion for various control voltages.

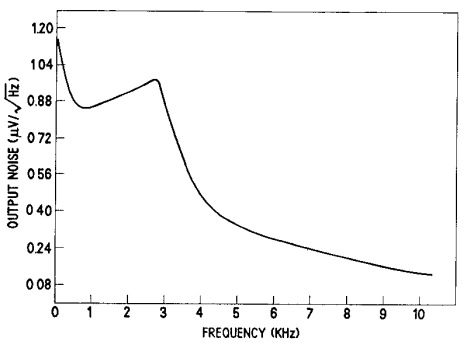

Fig. 13. Filter output noise.

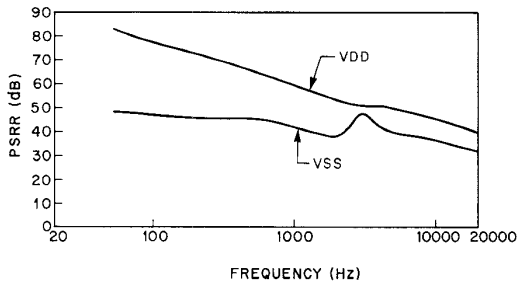

Fig. 14. Power supply rejection ratio (PSRR) versus frequency.

TABLE I
PERFORMANCE PARAMETERS OF THE FILTER INCLUDING INPUT AND OUTPUT CONVERTERS

Power supply voltages	±5 V
C-message weighted noise	34 μV rms
Wide band noise (2 Hz–12 MHz)	50 μV rms
Dynamic range[a] (based on −40 dB THD and *C*-message weighted noise)	94–96 dB
PSRR (1 kHz)	
$+V_{DD}$	−60 dB
$-V_{SS}$	−40 dB
Power dissipation	20 mW

[a]Depending on the value of control voltage.

where the transistors get into the saturation region of operation (shown on the distortion curves) mark a change in the shape of these curves. If a certain application requires the use of large signals with THD smaller than that indicated by Fig. 12 (e.g., −50 dB THD at signals of 6 $V_{p\text{-}p}$), the input signal could be first attenuated by an appropriate factor, then passed through the filter and finally amplified by the same factor. From the curves of Fig. 12 notice that a prefiltering attenuation and post-filtering amplification by only a factor of 2 would accomplish at least 10 dB improvement in THD. Such a strategy would inherently increase the output noise level and a penalty in overall dynamic range would be paid; however, this should not be critical for many applications because the starting dynamic range of the filter itself is very large (see below).

The output noise of the filter was measured to be 34 μV rms for *C*-message weighting, 42 μV rms for 3 kHz-flat weighting and 50 μV rms for 15 kHz-flat weighting. The wide band noise (2 Hz–12 MHz) remains at 50 μV rms which shows that practically all of it comes at low frequencies. This can be verified from the noise spectrum plotted in Fig. 13. Comparing these experimental results with simulations indicates that, in this implementation, the noise is mostly due to the resistor thermal noise at all but very low frequencies, where the $1/f$ noise of the operational amplifiers becomes predominant.

The power supply rejection performance is shown in Fig. 14 for both positive and negative supplies. It is emphasized that the PSRR is dominated by the performance of the balanced operational amplifiers and not by the other components of the filter. This is indicated by the fact that the curves of Fig. 14 are similar to those of a single balanced output operational amplifier. In addition, the coupling from the negative supply (V_{SS}) can only come from the operational amplifiers because the MOST resistors are p-channel (substrate connected to V_{DD}) and all the capacitors were fabricated over a grounded p-tub.

The power dissipation was 20 mW. This reflects the fact that two regular operational amplifiers were used for each integrator.

A summary of the filter performance is shown in Table I.

VI. CONCLUSIONS

A method has been described for the integration of active *RC* filters with wide dynamic range in MOS technology. MOSFET's operated in nonsaturation are used as voltage-controlled resistors and are linearized with a simple circuit technique based on fully balanced operation. As an application, a CMOS fifth-order low-pass filter for voice-band was fabricated. The filter works in continuous-time (no switching) and therefore offers natural advantages over sampled-data systems, such as no need for antialiasing or smoothing filtering, no Nyquist rate limitations, no switching noise, and no operational amplifier noise aliasing into the baseband. In addition, the filter design is straightforward, based on well established active *RC* filter theory. The simplicity and predictability of the design were reflected in successful results from the first trial. The behavior of the actual implementation was in good agree-

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ment with computer simulations and analytical results. The filter exhibited low noise and good linearity, resulting in wide dynamic range.

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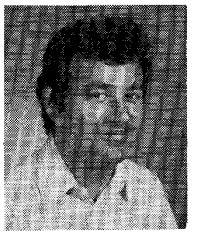

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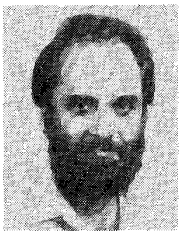

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