

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APPLE INC.,
Petitioner

v.

THETA IP, LLC,
Patent Owner

Case No. IPR2024-00816
Patent No. 7,010,330

**PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 7,010,330**

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I. INTRODUCTION

Apple Inc., (“Petitioner”) respectfully requests *inter partes* review (“IPR”) of claims 1-7, 9-13, 16, 23, 25, 26, 28-29 (“Challenged Claims”) of U.S. Patent No. 7,010,330 (“’330 Patent”).

II. THE ’330 PATENT

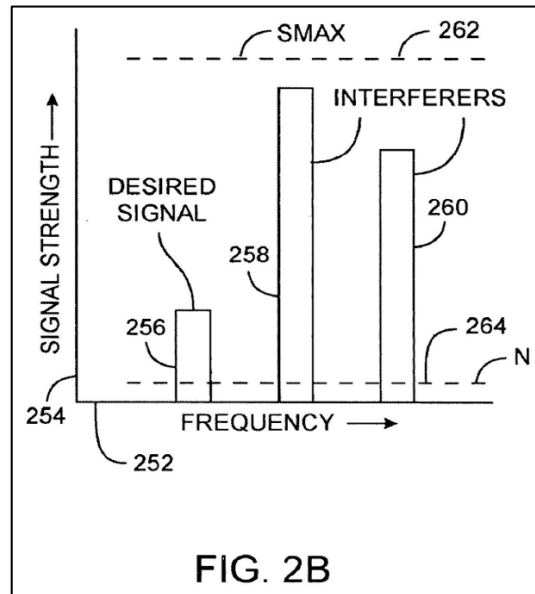
A. The ’330 Patent’s Alleged Invention

The ’330 Patent describes methods for reducing power dissipation in wireless transceivers, targeting the problem of battery drain in portable devices such as laptops and handheld devices. ’330 Patent (Ex. 1001), 1:16-30. The patent explains that prior art transceivers were designed to function properly under “worst-case operating conditions”—when the strength of a desired signal is low and the strength of interfering signals is high. *Id.*, 1:26-37. When better than worst-case conditions exist (e.g., high desired signal and/or low interferers), the alleged invention ***reduces “receiver circuit currents”***¹ . . . below what is necessary for the worst case condition[,]” ***reducing power dissipation*** and increasing battery life. *Id.*, 1:38-48.

The ’330 Patent connects the concept of power dissipation to the “dynamic range” of the receiver. *Id.*, 5:28-62. The dynamic range is defined on the upper end by the maximum signal strength that can be recovered—referred to as *S*_{max}—and on the lower end by the noise floor (*N*)—the level approaching which desired signals

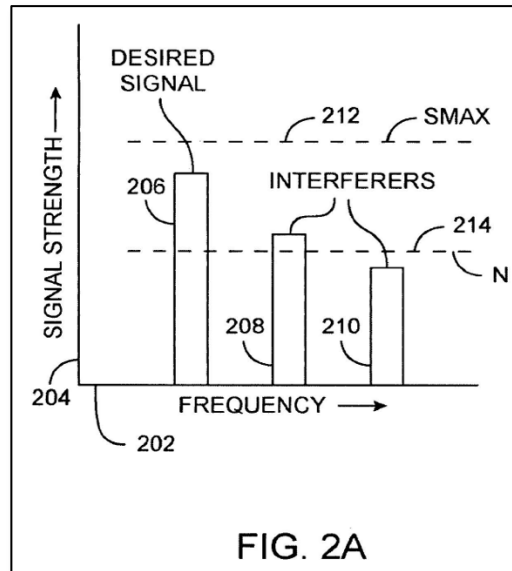
¹ All emphases added unless otherwise noted.

may be misinterpreted, causing bit-errors. *Id.*, 6:1-20. Fig. 2B below illustrates the dynamic range required under worst-case conditions. Here, (1) the desired signal strength is low, requiring a low noise floor (N), and (2) the interferers are strong, requiring a large S_{max}^2 :



Id., Fig. 2B, 5:51-62 (describing the same). Fig. 2A below illustrates the dynamic range required under better than worst-case conditions. Here, (1) the desired signal strength is high, allowing for an increased noise floor (N), and (2) the interferers are relatively weak, allowing S_{max} to be lowered without risking corruption from intermodulation distortion:

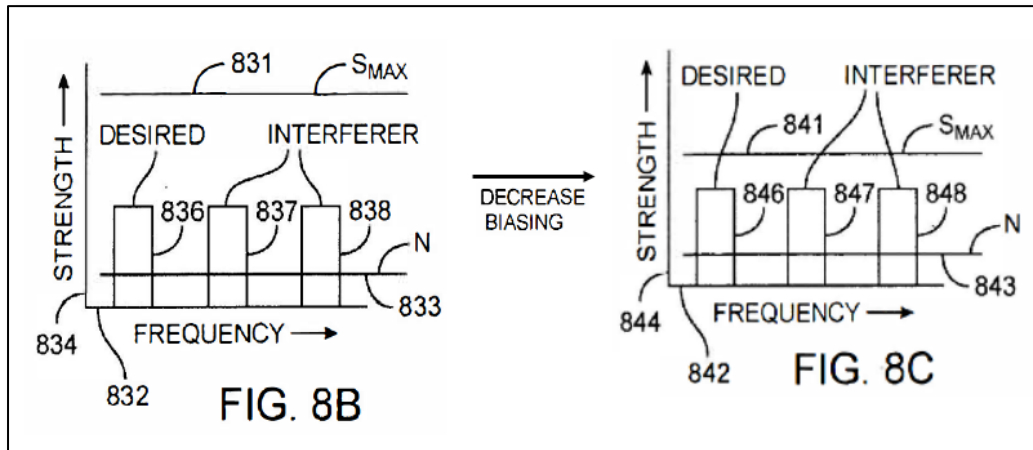
² If S_{max} falls below the strength of interferer signals, intermodulation distortion may corrupt reception of the desired signal. '330 Patent, 6:28-46, Fig. 3.



Id., Fig. 2A, 5:33-50 (describing the same).

The '330 Patent identifies three variables used to adjust the dynamic range, saving power when better than worst-case conditions are experienced: DC bias current, signal path impedance, and gain.

First, a DC bias current may be used to lower S_{max} , saving power when conditions permit accommodating a lower maximum signal strength. *Id.*, 6:18-20, 9:5-12. Figs. 8B and 8C illustrate saving power by decreasing bias current, which lowers S_{max} , when the desired signal strength and interferer signal strengths permit a lower S_{max} :



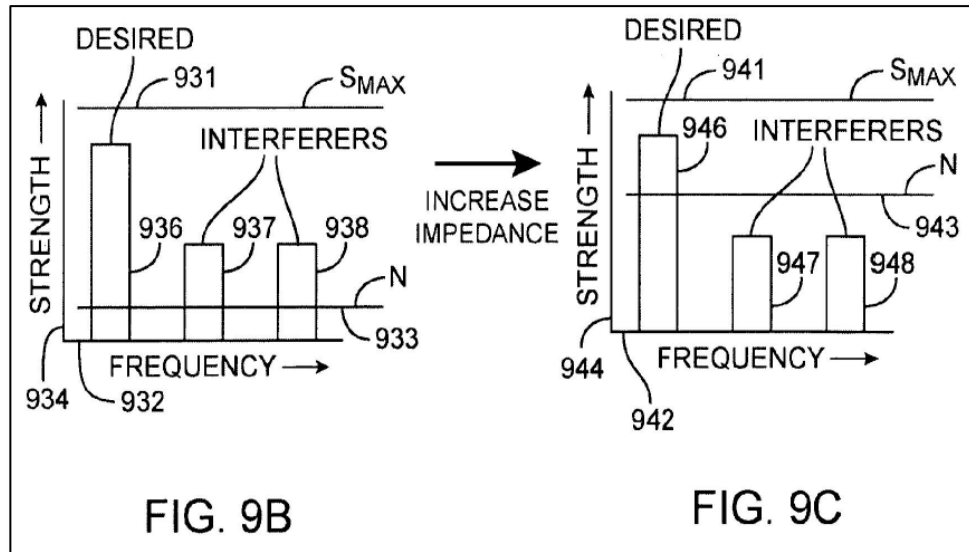
Id., Figs. 8B-8C.

Second, increasing the signal path impedance permits a lower AC drive/switching³ current to be used in the RF signal path, saving power. *Id.*, 6:17-18, 7:44-59. In one example, illustrated in Fig. 6, an RC filter circuit is “scaled[,]” doubling the signal path impedance, which allows the “circuit’s required drive current” to be cut in half. *Id.*, 7:44-59. Although the patent does not explain *why*

³ The '330 Patent specification repeatedly refers to a “drive current” as the AC current that flows through the signal path. *See* '330 Patent, 7:44-67, 9:21-23, 9:55-59, 10:10-18. But the Challenged Claims uses “switching current”—a phrase that does not appear in the specification. Patent Owner has conceded that “switching current” and “drive current” are used interchangeably in the '330 Patent and its continuations. *Theta Markman Br.* (Ex. 1007), 12-14. Accordingly, Petitioner will treat these terms as interchangeable in this Petition.

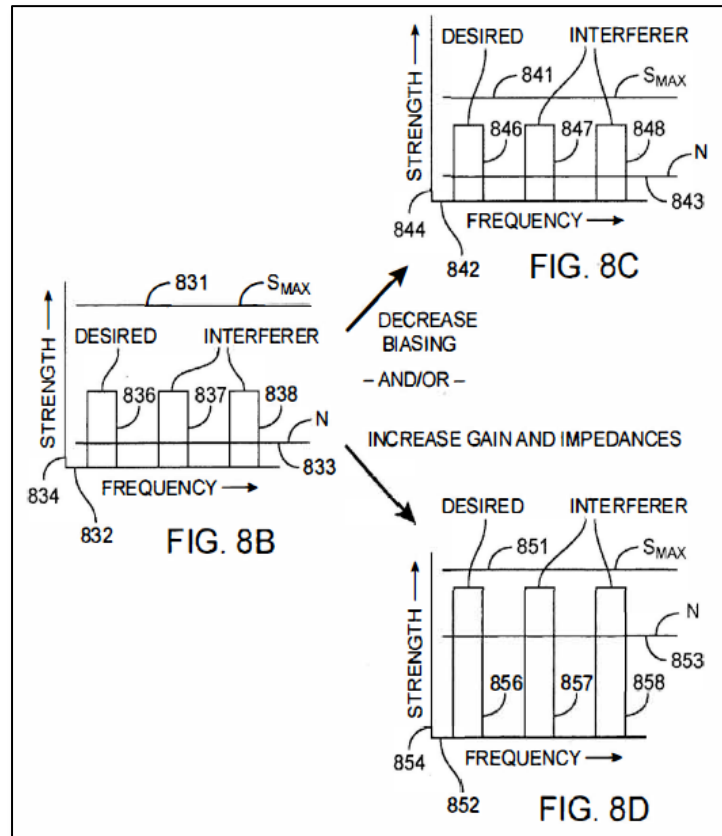
increasing the signal path impedance also increases the noise floor (N),⁴ the patent repeatedly notes that the signal path impedance can be increased to save power by lowering drive/switching current only if conditions permit increasing the noise floor (N). *Id.*, 6:7-9 (“Circuit impedances and currents are set such that the noise floor 264 is sufficiently low for an acceptable bit-error rate[.]”), 8:8-9 (“[I]mpedances are increased, which raise the noise floor.”), 9:19-23 (teaching that the noise floor is increased “by increasing one or more impedance in function block 810, such that drive currents inside that block are reduced.”). Figs. 9B and 9C illustrate saving power by increasing impedance, which increases noise floor (N), when the desired signal strength and interferer signal strengths permit such a noise floor increase:

⁴ A POSITA would recognize that resistor thermal noise is often a dominant source of noise in an RC filter, so increasing impedance by increasing the signal path resistance as taught by the ’330 Patent (’330 Patent, 7:44-52) would indeed increase the noise introduced by the filter. *Dec.* (Ex. 1003), ¶33.



Id., Figs. 9B-9C.

The third variable used to adjust a circuit's dynamic range is gain. While gain does not directly correspond to power savings, it does provide a mechanism by which all signals—desired and interferers—can be increased, creating room for power savings to be realized by increasing impedance. As illustrated in Figs. 8B-8D below, when the desired signal and interferer signals are all low, power savings can be realized by (1) lowering the bias current, which lowers S_{MAX} , as shown in Fig. 8C, (2) increasing gain and increasing impedance, which increases noise floor (N), as shown in Fig. 8D, or (3) all three—lowering the bias current, increasing gain, and increasing impedance:



Id., Figs. 8B-8D, Fig. 12, 10:60-67 (explaining that a combination of all three adjustments may be used when the desired signal and interferer signals are all low).

In sum, the '330 Patent teaches saving power when signal conditions are better than worst-case by decreasing the dynamic range via (1) decreasing the DC bias current, (2) increasing signal path impedance, and/or (3) increasing gain.

B. The '330 Patent's Prosecution

The '330 Patent was filed on February 23, 2004, claiming priority to Provisional Application Nos. 60/451,229 and 60/451,230, both filed March 1, 2003. For this proceeding, Petitioner applies March 1, 2003, as the priority date for the Challenged Claims.

A single office action was issued on January 5, 2005, rejecting all originally presented claims. '330 *Patent File History* (Ex. 1002), 284-93. In response, applicant amended claim 1 to recite, “reducing a switching current in the signal path by dynamically changing an impedance of a component in the signal path based on the first signal strength.” *Id.*, 302 (emphasis in original). Claim 23 was amended similarly. *Id.*, 305. The applicant also expressly distinguished the claimed switching current adjustment from DC bias current adjustment in the prior art. *Id.*, 308.

Claims 10 and 26 were amended to require maintaining the bias current in the signal path while receiving the data portion of the signal. *Id.*, 303, 306. The applicant argued that nothing in the cited art taught or suggested “limit[ing] changes to a bias current while receiving a preamble[.]” *Id.*, 309.

Finally, regarding claims 17 and 29, applicant argued that the prior art did not teach both dynamic gain and dynamic impedance adjustments, as required by those claims. *Id.*, 309-10.

C. Claim Construction

In this proceeding, claims are interpreted under the same standard applied by Article III courts (i.e., the *Phillips* standard). 37 C.F.R. § 42.100(b); 83 Fed. Reg. 197 (Oct. 11, 2018); *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (*en banc*). Petitioner applies the plain and ordinary meaning of all claim terms as understood by a POSITA for all terms not expressly construed below. Petitioner does

not waive any argument in any litigation that claim terms in the '330 Patent are indefinite or that additional terms might need construction in a different proceeding.

The parties are disputing the correct construction of a number of terms in parallel litigation. As explained in the detailed mapping below, the Proposed Grounds satisfy either party's proposal for the disputes in the below chart:⁵

Claim Term	Theta's Constructions	Apple's Constructions
"impedance"	Plain and ordinary meaning, but if construed, should be construed as "opposition to the flow of alternating current"	Plain and ordinary meaning
"switching current"	Plain and ordinary meaning	"the current that carries a signal through a load"

The parties also dispute the meaning of "signal path" and "dynamically changing/adjust[ing]" (the "dynamic limitation").

⁵ *Joint Markman Statement* (Ex. 1008). Although alternative positions have been exchanged in the parallel litigation for various terms, this chart captures the current state of parties' primary positions. Further, although the Court has yet to issue a *Markman* order, in advance of the *Markman* hearing, the Court preliminarily concluded all disputed claim language should be accorded its plain and ordinary meaning.

Regarding “signal path,” Apple argued that signal path excludes the “digital signal processing” block, and Theta argued that no such exclusion is proper. *See Theta Sur-Reply* (Ex. 1009), 1-3 (arguing that the signal path “can be both analog or digital at different points in the signal path[,]” and as such, “is not limited to only analog components”).

For the dynamic limitation, Apple argued it should exclude “reliance on a signal strength threshold,” and Theta argued that no such exclusion is proper. *Theta Markman Br.*, 14-16 (arguing the terms only “require varying ‘during operation based—at least in part—on information gained during operation.’”).

For purposes of this proceeding, Petitioner proposes this Board adopt Patent Owner’s interpretation of the dynamic limitation. *See Western Digital Corporation v. SPEX Technologies, Inc.*, IPR2018-00084, Paper 14, *11 (PTAB Apr. 25, 2018); *see also General Electric v. Vestas*, IPR2018-00928, Paper 9, *16-17 (PTAB Nov. 5, 2018); *10x Genomics, Inc. v. Bio-Rad Laboratories, Inc.*, IPR2020-00086, Paper 8, *19 (PTAB Apr. 27, 2020) (finding “judicial efficiency will be enhanced by allowing Petitioner to rely upon a claim construction that Patent Owner is relying upon in the related district court litigation to assert infringement of the challenged patent”).

D. A Person of Ordinary Skill in the Art

As of March 1, 2003, a person of ordinary skill in the art (POSITA) would have had a master's degree in electrical engineering or the equivalent, and two or more years of experience with wireless communications devices. *Dec.*, ¶¶ 39-41. Additional education or experience might substitute for the above requirements. *Id.*

III. REQUIREMENTS UNDER 37 C.F.R. § 42.104

A. Standing Under 37 C.F.R. § 42.104(a)

Petitioner certifies the '330 Patent is eligible for IPR and Petitioner is not barred or estopped from requesting IPR challenging the claims of the '330 Patent. Petitioner is not the owner of the '330 Patent, has not filed civil action challenging the validity of any claim of the '330 Patent, and this Petition is filed less than one year after Petitioner was served with a complaint alleging infringement of the '330 Patent.

B. Identification of Challenge Under 37 C.F.R. § 42.104(b)

Petitioner requests the Challenged Claims be found unpatentable on the following grounds:

Proposed Ground of Unpatentability	Exhibits
Ground 1: Claims 1-7, 9-13, 16, 23, 25, 26, 28-29 are obvious⁶ under §103(a) over “Adaptive Analog IF Signal Processor for a Wide-Band CMOS Wireless Receiver” by Behbahani et al. (“<i>Behbahani</i>”) in view of “A 2.4-GHz Low-IF Receiver for Wideband WLAN in 0.6μm CMOS – Architecture and Front-End” by Leete et al. (“<i>Leete</i>”) and in further view of “A Broad-Band Tunable CMOS Channel-Select Filter for a Low-IF Wireless Receiver” by Tan et al. (“<i>Tan</i>”)	Ex. 1004 Ex. 1005 Ex. 1006

IV. OVERVIEW OF THE PRIOR ART

A. Behbahani

Behbahani published in August 2001. *Behbahani* (Ex. 1004), 1205. Petitioner’s declarant, Dr. Asad A. Abidi, is listed as a co-author on *Behbahani* and was the supervising faculty member overseeing the research underlying *Behbahani*. *Dec.*, ¶45. Dr. Abidi explains that, as indicated on the face of the article, it was made publicly available in the August 2001 IEEE Journal of Solid-State Circuits, and

⁶ In the parallel litigation, Theta contends it has evidence of secondary indicia of nonobviousness and stated that it intends to supplement the record beyond the minimal responses provided to date. Petitioner does not address those partial contentions herein, but reserves its right to fully respond to any evidence or arguments advanced in this proceeding.

therefore qualifies as prior art under 35 U.S.C. §102(b) (pre-AIA). *Id.*; *see also* *Munford Dec.*, (Ex. 1010), ¶¶6-9.

Behbahani was cited on the face of the '330 Patent, but was not discussed by the Examiner during prosecution. As set forth below in Section VI, a discretionary denial under § 325(d) is not warranted on this record.

Behbahani teaches a wireless receiver that implements an “adaptive dynamic range” method to save power by decreasing the dynamic range when conditions are better than worst case:

This receiver implements *adaptive dynamic range* in the IF [Intermediate Frequency] section. ***Most wireless systems are designed for the worst case***; that is, the dynamic range is specified for the desired signal at a minimum detectable level, accompanied by the largest anticipated interferers. ***In practice, the receiver only infrequently needs this high instant DR [dynamic range]. DR is obtained at the expense of a disproportionate rise in power consumption*** An important idea here, which has also been noted elsewhere [4], is that ***providing no more than the required DR at any given time lowers the average power consumption.***

Behbahani, 1205.

Two separate adaptive techniques are combined to accomplish *Behbahani*'s goals—(1) step-based DR and (2) sliding DR. *Id.*, 1206-07. For *Behbahani*'s step-based adaptive DR, the receiver switches/steps between two scaled filters. *Id.* A

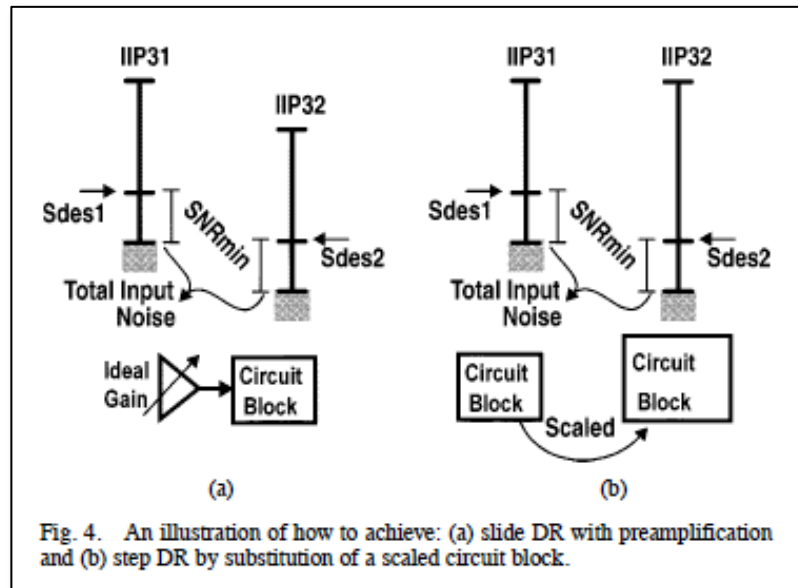
“high-power filter” is used during the range⁷ of worst-case signal conditions (i.e., low desired signal and high interferers), and a separate “low-power filter” is used for the range of conditions that are better than worst-case. *Id.* (“Since the worst-case scenario is infrequent, the low-power filter determines the average RX power consumption.”). As set forth in the proposed grounds below, switching from the high-power filter to the low-power filter satisfies both power saving mechanisms described and claimed in the Challenged Patent, (1) lowering the bias current and (2) increasing the signal path impedance, lowering the drive/switching current.

When the low-power filter is utilized during better than worst-case conditions, *Behbahani’s* sliding DR technique uses a gain stage in advance of the low-power filter to slide a smaller DR up or down based on strengths of the received signals. *Id.*, 1206-07.

Below, Fig. 4(a) illustrates a gain stage used to slide a small DR (that results from using the low-power filter) to accommodate specific signal strength conditions,

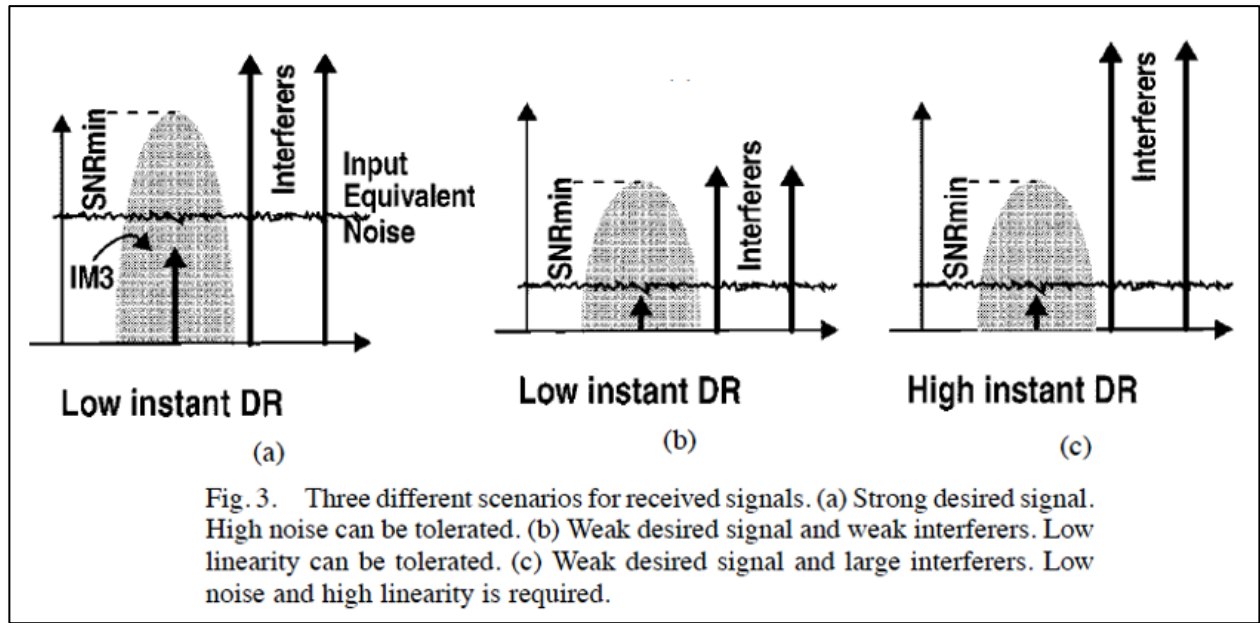
⁷ Petitioner’s declarant, Dr. Abidi, explains that worst-case conditions exist when the desired signal is very low and the interferers are very high, but notes that these “worst-case” conditions do capture a range of scenarios in which low-desired and high-interferer signals are received, rather than a single discrete “worst-case” condition. *Dec.*, ¶47.

and Fig. 4(b) illustrates switching from the low-power filter to high-power filter to expand the DR when worst-case conditions are encountered:



Id., 1206.

Behbahani describes three different desired and interferer signal scenarios below in Figure 3. Figs. 3(a) and Fig. (b) depict better than worst-case conditions in which “receiver dynamic range may be modest” and the gain-based sliding DR approach is sufficient. *Id.* 120Fig. 3(c) depicts worst-case conditions (i.e., low desired signal and high interferers), requiring the system to expand the dynamic range by switching in the high-power filter. *Id.*



Id., Fig. 3 (rearranged).

Behbahani, like the '330 Patent, discloses a wireless receiver architecture and design intended to achieve reduced power dissipation. *Compare '330 patent*, Abstract, 1:16-18, 2:38-59, 6:1-27, *with Behbahani*, Abstract, 1205. Thus, *Behbahani* is in the same field of endeavor as the '330 Patent. *Dec.*, ¶¶45-52.

Behbahani is also reasonably pertinent to certain problems addressed by the '330 Patent such as accommodating different signal conditions by dynamically adjusting dynamic range. *Compare '330 Patent*, 5:28-64, 6:1-27, *with Behbahani*, Abstract, 1205, Fig. 3; *Dec.*, ¶¶45-52. Therefore, *Behbahani* is analogous art to the '330 Patent.

B. Leete

Leete was published in December 2000. *Leete* (Ex. 1005), 1908. Petitioner's declarant, Dr. Asad A. Abidi, is listed as a co-author on *Leete* and was the supervising faculty member overseeing the research underlying *Leete*. *Dec.*, ¶53. Dr. Abidi explains that, as indicated on the face of the article, it was made publicly available in the December 2000 IEEE Journal of Solid-State Circuits, and therefore qualifies as prior art under 35 U.S.C. §102(b) (pre-AIA). *Id.*; *see also Munford Dec.*, ¶¶14-17. *Leete* was not cited or considered during prosecution of the '330 patent.

Leete is intended to be used in conjunction with *Behbahani*. Specifically, *Leete* provides details about the RF circuitry not described in *Behbahani* itself. *Behbahani*, 1205. In one example, *Leete* describes the RF front-end, including a low noise amplifier (LNA) and an RF downconverter (including mixers) that converts the RF signal to an intermediate frequency (IF). *Leete*, 1908. As discussed in the Proposed Grounds below, *Behbahani* focuses on the IF and digital portions of the receiver, effectively picking up where *Leete* leaves off. *Dec.*, ¶54.

Like the '330 Patent, *Leete* teaches a wireless receiver architecture and design intended to achieve reduced power dissipation. *Compare* '330 patent, Abstract, 1:16-18, 2:38-59, 6:1-27, *with Leete*, Introduction, 1908, Fig. 1. Thus, *Leete* is in the same field of endeavor as the '330 Patent. *Dec.*, ¶¶53-55.

Leete is also reasonably pertinent to certain problems addressed by the '330 Patent, such as accommodating a wide dynamic range, low power consumption, and minimizing noise in the components of the wireless receiver architecture. *Compare '330 Patent*, 5:28-64, 6:1-27, *with Leete*, 1908, 1910; *Dec.*, ¶¶53-55. Therefore, *Leete* is analogous art to the '330 Patent.

C. Tan

Tan published in April 2000. *Tan* (Ex. 1006), 476. Petitioner's declarant, Dr. Asad A. Abidi, is listed as a co-author on *Tan* and was the supervising faculty member overseeing the research underlying *Tan*. *Dec.*, ¶56. Dr. Abidi explains that, as indicated on the face of the article, it was made publicly available in the April 2000 IEEE Journal of Solid-State Circuits, and therefore qualifies as prior art under 35 U.S.C. §102(b) (pre-AIA). *Id.*; *see also Munford Dec.*, ¶¶10-13.

Tan was cited on the face of the '330 Patent, but was not discussed by the Examiner during prosecution. As set forth below in Section VI, a discretionary denial under § 325(d) is not warranted on this record.

Behbahani cites *Tan* to describe the details of the bandpass filter used in *Behbahani*: "The details of the BPF design are presented elsewhere [7]." *Behbahani*, 1210. The citation [7] in *Behbahani* is to *Tan*. The Proposed Grounds rely upon certain details in *Tan* to explain the operation of the low-power and high-power filters in *Behbahani*.

Like the '330 Patent, *Tan* teaches a wireless receiver architecture and design intended to achieve reduced power dissipation. *Compare* '330 patent, Abstract, 1:16-18, 2:38-59, 6:1-27, *with Tan*, Introduction, 476. Thus, *Tan* is in the same field of endeavor as the '330 Patent. *Dec.*, ¶¶56-58.

Tan is also reasonably pertinent to certain problems addressed by the '330 Patent, such as accommodating a wide dynamic range, low power consumption, and minimizing noise in the components of the wireless receiver architecture. *Compare* '330 Patent, 5:28-64, 6:1-27, *with Tan*, 476; *Dec.*, ¶¶56-58. Therefore, *Tan* is analogous art to the '330 Patent.

V. THE CHALLENGED CLAIMS ARE UNPATENTABLE

A. Ground 1: *Behbahani* in view of *Leete* in further view of *Tan*

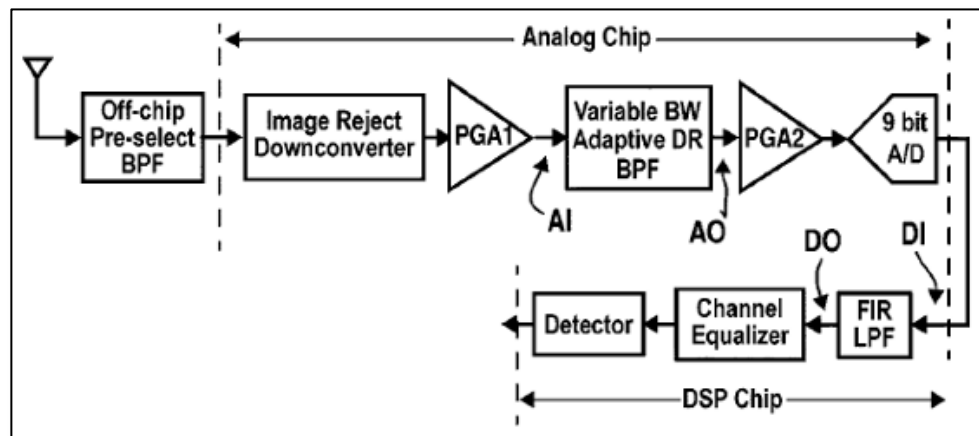
1. Claim 1

Claim 1(Pre): “1. A method of receiving a signal using an integrated circuit, the integrated circuit comprising a signal path including a low-noise amplifier configured to receive the signal, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer, the method comprising:”

To the extent the preamble is limiting, *Behbahani* in view of *Leete* discloses a method of receiving an RF signal using an integrated circuit, the integrated circuit comprising a signal path including a low-noise amplifier coupled to a mixer, which is coupled to a low-pass filter (i.e., an LNA->mixer->filter topology).

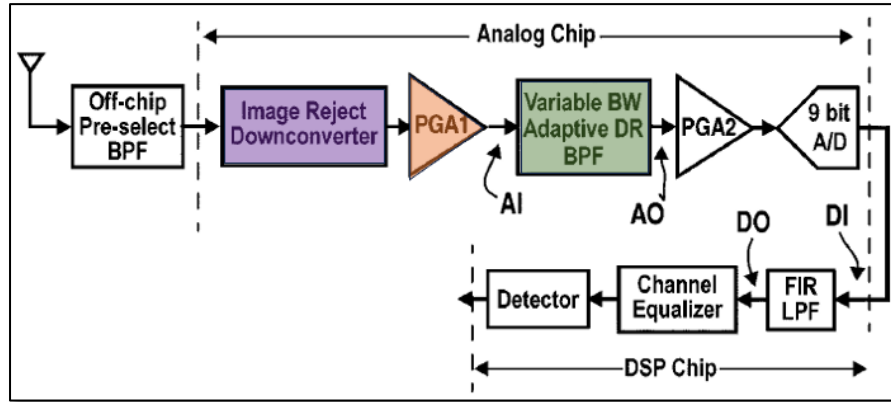
Behbahani and Leete describe different aspects of the same circuit—a POSITA would have been motivated to combine their teachings

As an initial matter, the two references describe the same research, focusing on different aspects of the same receiver circuit, and were intended to be used in conjunction. *Dec.*, ¶60. Fig. 2 from *Behbahani* describes the “complete WLAN receiver” circuitry:



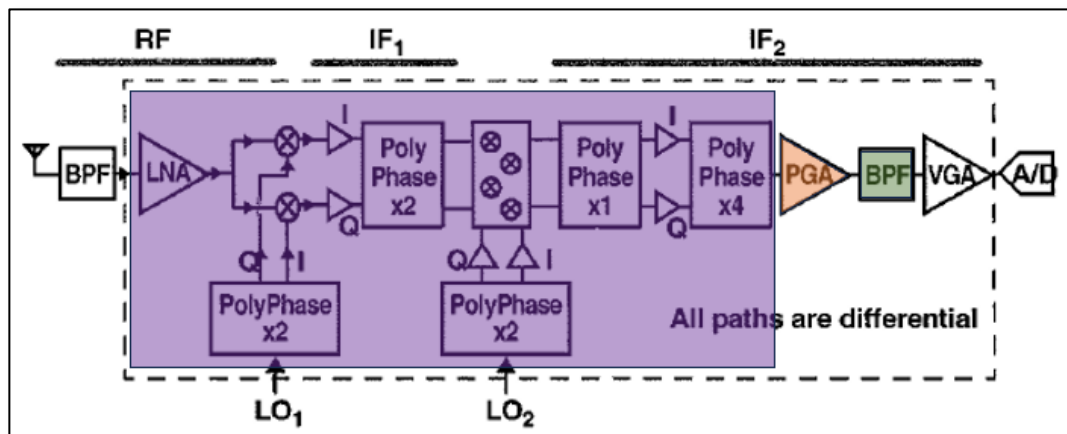
Behbahani, 1206. *Behbahani* explains that “the IF section is the main focus of this paper” and notes that “[t]he front-end and image-reject downconversion sections of the [receiver] are described in [5].” *Id.*, 1205. The citation “[5]” in *Behbahani* is the *Leete* article. *Leete* does in fact describe a “2.4-GHz front-end and the first downconversion section of a fully integrated low-IF receiver.” *Leete*, Abstract.

On the “analog chip” and in advance of **PGA1** and the **variable filter**, *Behbahani* represents the receiver circuitry with a single box labeled “**Image Reject Downconverter**”:



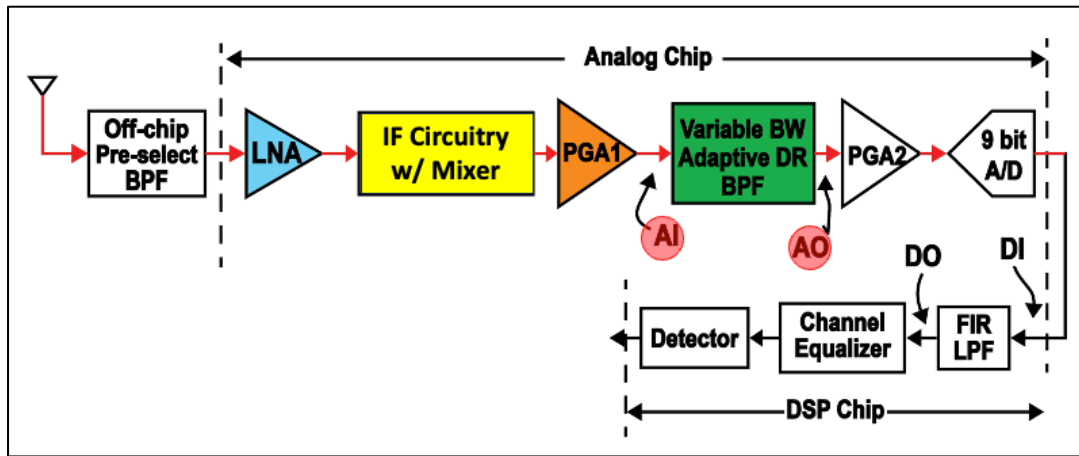
Behbahani, Fig. 2 (annotated).

As *Behbahani* notes, *Leete* provides the details of this downconverter circuitry. *Leete* teaches that the “RF front-end comprises a *low noise amplifier (LNA)* and an *RF quadrature mixer*, which downconverts the RF signal to the first IF (IF1).” *Leete*, 1908 (further noting an additional “IF mixer *downconverts* the *desired* signal at IF1 to a low IF2”). This detailed circuitry is depicted in *Leete*’s Fig. 1 below:



Id. at Fig. 1 (annotated).

Consistent with *Behbahani's* express intent to use the two references conjunctively, the “Image Reject Downconverter” box from *Behbahani's* Fig. 2 has been replaced with an LNA and the other IF circuitry, including the mixer stage:



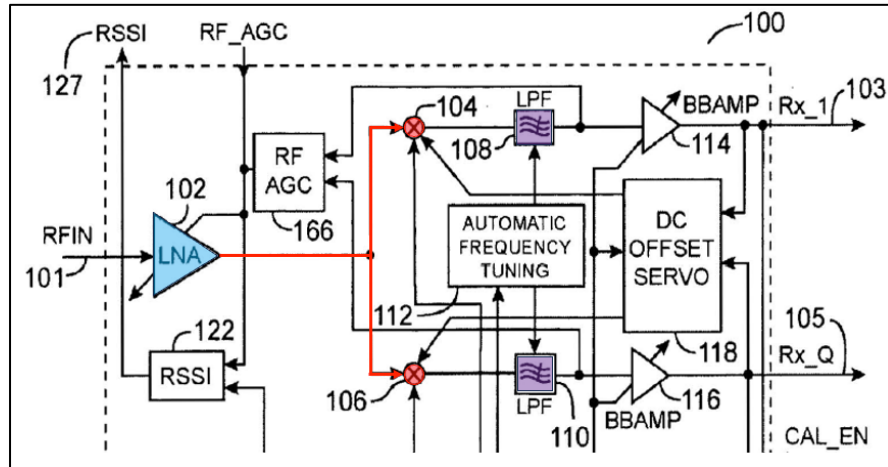
Behbahani modified by *Leete*, Figure 2 (annotated).

A POSITA would have been motivated to combine *Behbahani* and *Leete* as depicted above at least because *Behbahani* expressly motivates the combination, teaching that *Leete* provides the receiver details preceding PGA1. *Dec.*, ¶¶60-68; *Norian Corp. v. Stryker Corp.*, 363 F.3d 1321, 1328 (Fed. Cir. 2004) (finding a sufficient motivation to combine references where one explicitly cites the other). Further, a POSITA would have understood that the LNA->mixer->filter topology is commonplace, further motivating the proposed combination of *Behbahani* and *Leete*. *Dec.*, ¶¶69-72 (discussing extensive use of this topology in the field of wireless transceivers). Finally, a POSITA would have understood that placing *Leete's* LNA in *Behbahani's* circuit as proposed uses a known technique to improve

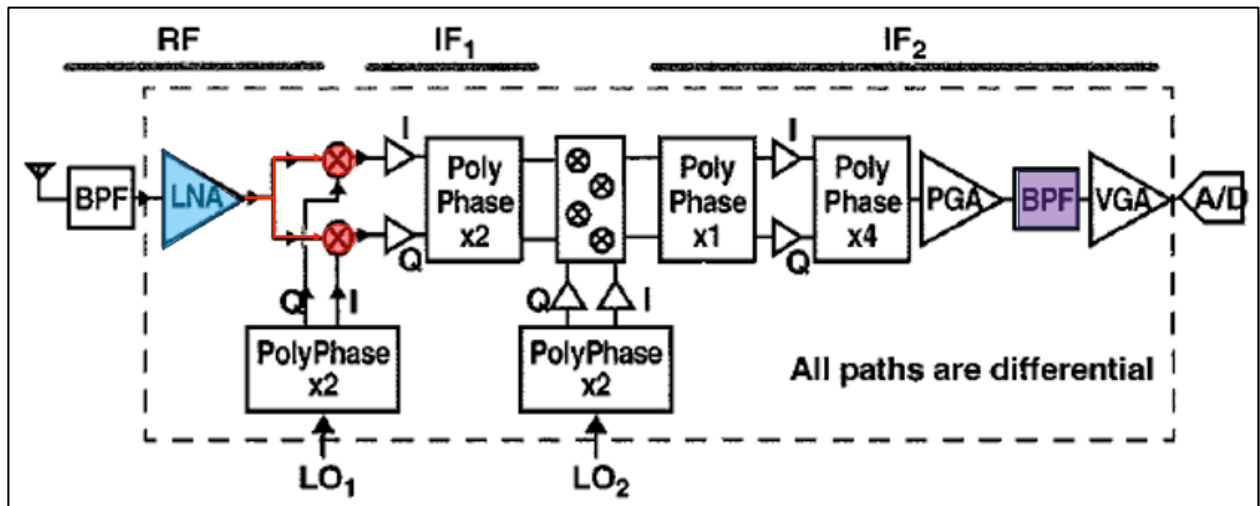
a similar device in the same way. *Id.* (explaining that, not only does *Leete*’s circuitry improve *Behbahani*’s receiver, it completes *Behbahani*’s receiver, providing implementation detail not covered by *Behbahani*). As set forth above, both circuits are similar. In fact, they are describing different portions of the same receiver circuit. *Id.* (discussing a 2000 IEEE paper by the same research team that published before *Behbahani* and *Leete*, that included the same LNA-equipped figure as *Leete*, and that described both the IF stages (*Leete*’s focus) and *Behbahani*’s step-based and sliding DR concepts). A POSITA would have understood that benefits of an LNA in a wireless receiver include the ability to introduce gain without significant noise, improving the receiver’s ability to recover a desired signal. *Id.* A POSITA would further have understood that such a benefit applies equally to *Behbahani*’s Fig. 2 as it does to the more detailed version of the same receiver circuit as depicted in *Leete*’s Fig. 1 and would have expected success in treating their teachings conjunctively, as the authors intended. *Id.*

Leete’s quadrature RF mixer—with its separate I and Q paths—satisfies the claimed “mixer.” Although the Challenged Claims generically refer to a “mixer,” the ’330 Patent’s detailed description describes the same two-signal path quadrature mixer arrangement as *Leete*. ’330 Patent, 4:15-17 (“The receiver includes a signal path formed by low-noise amplifier 102, *I and Q mixers 104 and 106*, low pass filters 108 and 110[.]”), 4:35-39 (teaching that “quadrature mixers 104 and 106 . . .

down-convert the received signal”). As shown below, both *Leete* and the ’330 Patent place the **quadrature mixer** (with separate I and Q paths) between an **LNA** and **filter**:



Id., Fig. 1 (annotated).

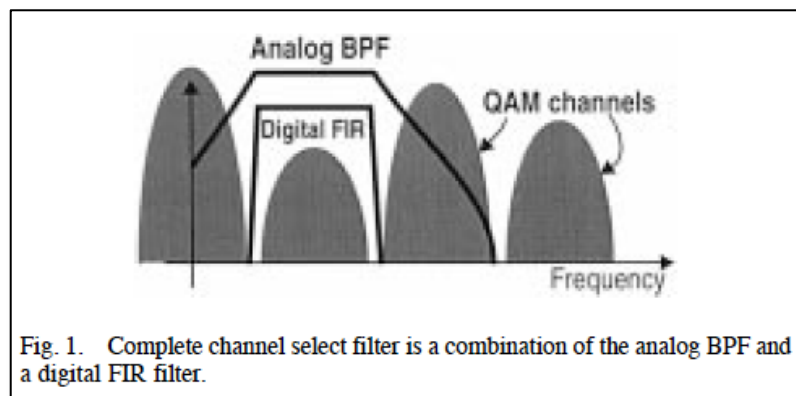


Leete, Fig. 1 (annotated). Based on the similar disclosures in the ’330 Patent and in *Leete* and based on the prevalence of quadrature mixers in receivers at the time, a POSITA would have understood that *Leete*’s quadrature mixer stage satisfies the claimed “mixer.” *Dec.*, ¶¶73-76.

In sum, a POSITA would have been motivated to combine *Behbahani* and *Leete* as described above, producing a receiver circuit with an LNA->mixer->filter topology, as claimed. *Id.*

Behbahani's "Variable BW Adaptive DR BPF" Includes a Low Pass Filter

Depicted in Fig. 1 below, *Behbahani* teaches an analog bandpass filter (BPF) that “attenuates near-by channels and rejects far-away channels.”



Behbahani, Fig. 1, 1205. *Behbahani* explains that its “BPF realized by an LPF [low-pass filter] in series with HPF [high-pass filter] lowers power consumption.” *Behbahani*, 1216; *see also id.*, 1210 (describing the BPF as “[a] high-order LPF [] cascaded with a low-order HPF”).

Accordingly, a POSITA would have understood that *Behbahani's* BPF includes a low-pass filter, satisfying the filter component recited in the preamble. *Dec.*, ¶77.

Behbahani's Mixer is "Coupled" to its Filter—"Coupled" Should be Interpreted to Capture both Direct and Indirect Connections

That *Behbahani* teaches other circuit components (e.g., PGA1) between its mixer and low-pass filter does not preclude a finding that the mixer and low-pass filter are “coupled” as claimed. The ’330 patent does not ascribe any specific meaning to “coupled to[.]” Indeed, with only one (unhelpful) exception, the term “coupled to” is used exclusively in the claims themselves and in the “Summary” section that merely repeats the claim language. As shown below, however, the ’330 Patent illustrates circuit arrangements in which the mixer and filter—components that are “coupled” in the claims—are separated by a gain stage:

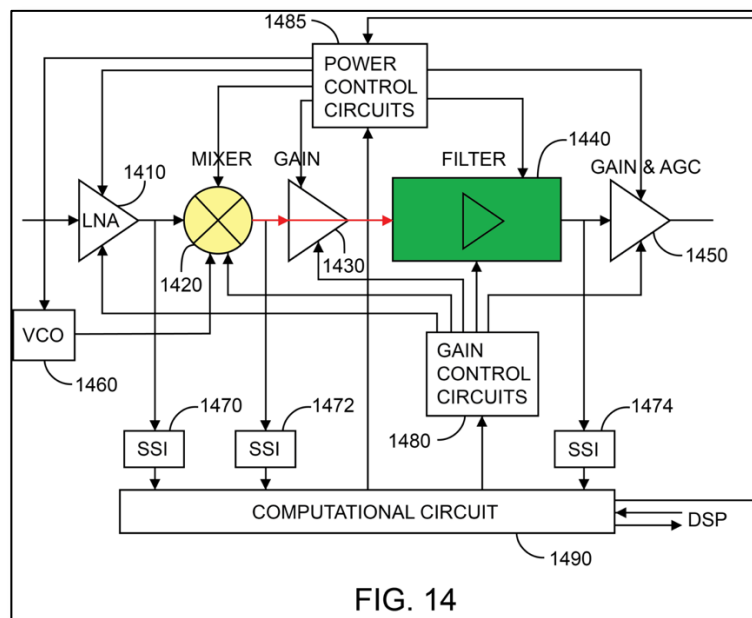


FIG. 14

'330 Patent, Fig. 14 (annotated). Particularly in light of the patent's limited discussion of the term, it is improper to construe "coupled" so narrowly as to exclude the topology illustrated in Fig. 14.

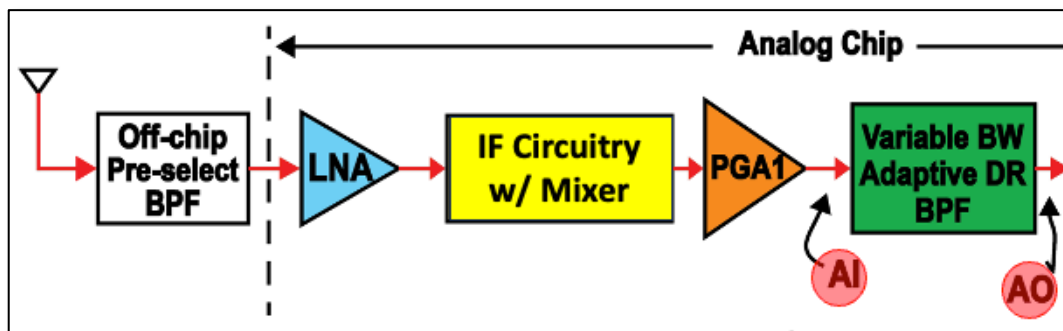
Permitting indirect connections (i.e., allowing for intervening circuitry) aligns with the extensive case law on the meaning of couple. *See, e.g., Bradford Co. v. Conteyor N. Am., Inc.*, 603 F.3d 1262, 1270–71 (Fed. Cir. 2010) (holding “coupled to ... should be construed broadly so as to allow an indirect attachment”); *Ymax Corp. v. Focal IP, LLC*, IPR2016-01258, Paper No. 60, 23 (Dec. 28, 2017) (citing *Bradford* for the proposition that “it is settled that ‘coupled to’ generally means that direct connection is not required”); *Silicon Graphics, Inc. v. n Vidia Corp.*, 58 F. Supp. 2d 331, 346 (D. Del. 1999) (adopting the ordinary meaning of couple as “coupled or connected, directly or indirectly” where a claim recited “cache [] coupled to the input” and a figure depicted cache and the input separated by intervening circuitry).

Because “coupled to” captures both direct and indirect connections, *Behbahani*’s LNA is coupled to its mixer and its mixer is coupled to the low-pass filter (i.e., in an LNA->mixer->filter topology), as claimed, regardless of any intervening circuitry. *Dec.*, ¶¶78-83.

Behbahani’s LNA, Mixer, and Filter are Components of an Integrated Circuit That Receives a Signal

Behbahani teaches a receiver that receives a signal. *Behbahani*, 1207. (describing “measured signal levels [that] indicate how much of the **received signal** is being rejected, respectively, by the analog filter and the digital filter”). Indeed, the whole point of an RF *receiver* is to receive RF signals. *Dec.*, ¶84.

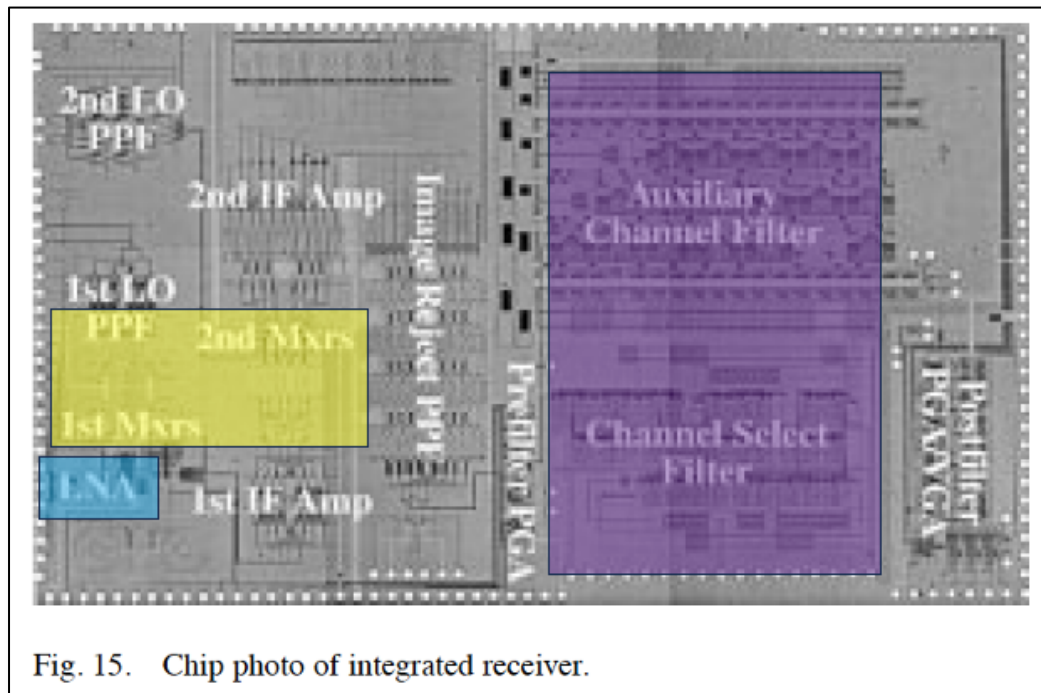
Behbahani's Fig. 2 depicts certain components of the receiver as being contained within an analog integrated circuit. Specifically, as shown below in an annotated excerpt of Figure 2, an "analog chip" includes a signal path (annotated in red), an LNA (annotated in blue) configured to receive the signal, a mixer (annotated in yellow) having an input coupled to an output of the LNA, and a low-pass filter (annotated in green) having an input coupled to an output of the mixer (annotated in yellow):



Behbahani modified by *Leete*, Figure 2 (excerpt, annotated); *Dec.*, ¶¶85-89 (explaining the signal path).

A POSITA would have understood that the "analog chip" reference in *Behbahani* means the components are in fact integrated on a single analog chip. *Dec.*, 874 (explaining that the term chip was commonly used to describe an integrated circuit). This is consistent with the disclosures in the '330 Patent using the terms "chip" and "integrated circuit" interchangeably. '330 Patent, 4:2-5. ("This transceiver may be completely or partially integrated on a *semiconductor chip*, or it may be integrated onto *multiple integrated circuits*."). Further, *Behbahani* expressly

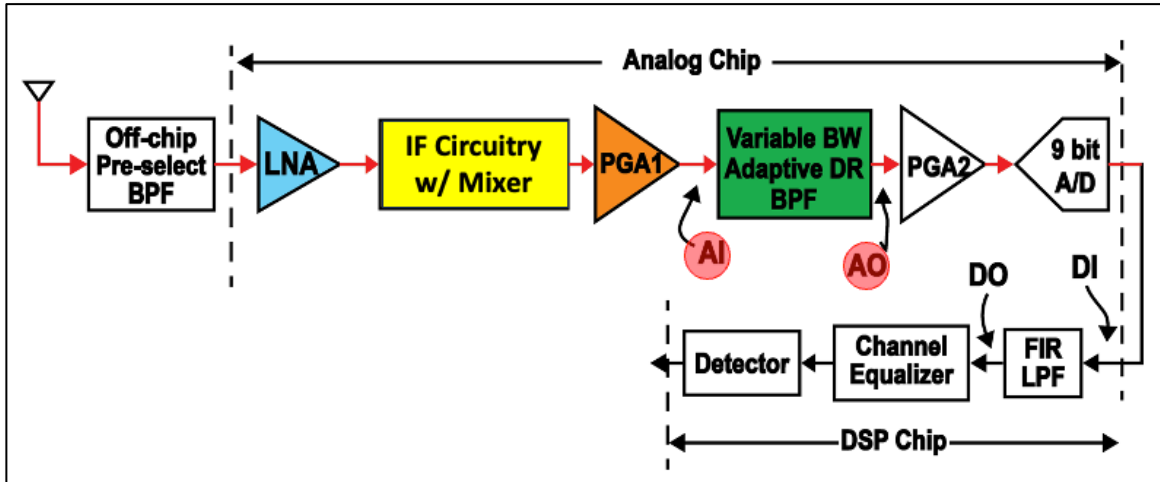
notes that a goal of the described research is to support “a fully integrated receiver (RX)” with “on-chip image-rejection[.]” *Behbahani*, 1205. Indeed, *Leete*’s Fig. 15 is a “[c]hip photo” of an “integrated receiver” that shows an LNA, mixers, and filters all on the same integrated circuit:



Leete, Fig. 15 (annotated); *Dec.*, ¶¶85-89 (describing the same).

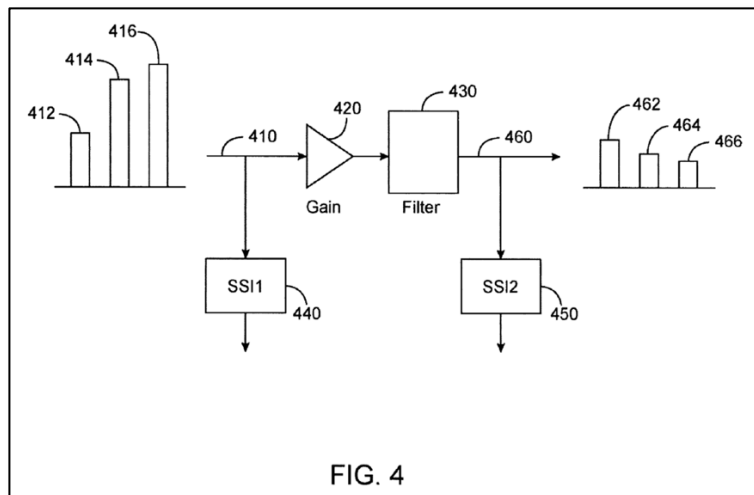
Claim 1(a): “determining a first signal strength at a first node in the signal path in the integrated circuit; and”

As discussed above, *Behbahani* teaches a path for an analog signal in an integrated circuit. See Claim 1 (Pre) (explaining that the components depicted in *Behbahani*’s Fig. 2 and referred to as “analog chip” are part of an integrated circuit). And as set forth in detail below, *Behbahani* teaches a process for determining signal strength at nodes A_1 and A_0 , which are in the analog signal path on the “analog chip”:



Behbahani modified by *Leete*, Figure 2 (annotated).

The '330 patent teaches determining the *relative* strengths of a desired signal and interferer signals, rather than absolute strengths of these signals. It does so by comparing a cumulative signal strength at a first node to a cumulative signal strength at a second node. Fig. 4 below illustrates this concept.



'330 Patent, Fig. 4. SSI1 is the “sum of desired signal 412 and interfering signals 414 and 416,” and SSI2 is the “sum of desired signal 462 and interfering signals 464

and 466.” ’330 Patent, 6:52-64. The patent explains that the combination of optional gain element 420 and filter 430 produce a gain of one for the desired signal, meaning the strength of the desired signal is identical in the SSI1 and SSI2 measurements. *Id.*, 6:64-67. It also explains that the interfering signal levels are reduced by filter 430. *Id.*, 7:1-5. Accordingly, if SSI2 is significantly smaller than SSI1, large interferer signals have been reduced by filter 430. *Id.* (explaining that comparing these values indicates how much of the combined signal has been filtered). From this information, the system determines what combination of “bias, impedance, and gain . . . may be optimized to reduce power dissipation.” *Id.*, 7:5-8.

With respect to dynamic impedance adjustments, which are the focus of Claim 1, the ’330 Patent explains that power can be saved by (1) increasing impedance when signal strength measurements indicate a high desired signal strength or (2) increasing gain *and* impedance where signal strength measurements indicate low desired signal strength without large interferer signals. *See id.*, Figs. 8B, 8D, 9B, 9C, 10B, 10C, 11B, 11D, 12 (and their corresponding disclosures).

Behbahani teaches a nearly identical process for determining relative signal strengths and using that information to employ its adaptive sliding DR and adaptive step DR techniques. *Behbahani* emphasizes the importance of measuring signal strength to its adaptive DR techniques, and notes that, like the ’330 Patent, signal

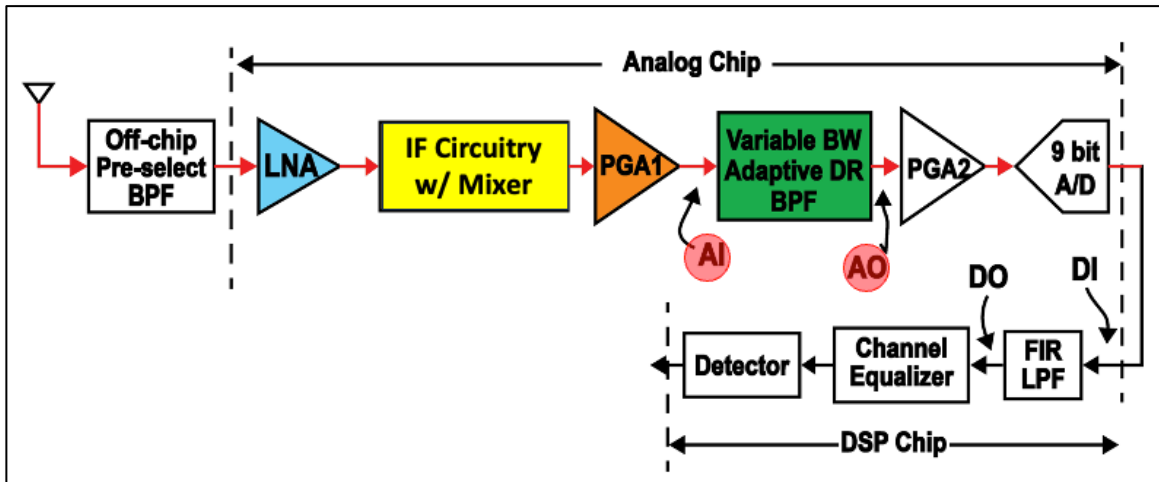
power is sensed at the input and output of the analog low-pass filter to indicate how much of the received signal is being rejected:

The algorithm to sense the input signal and determine instant DR is key. Signal power is sensed at four points along the IF strip (Fig. 2): input and output of the analog BPF and input and output of the digital channel select filter. These measured signal levels indicate how much of the received signal is being rejected, respectively, by the analog filter and the digital filter.

Behbahani, 1207.⁸

Behbahani's Fig. 2 shows a first signal strength measured at node A_I located in the signal path before the analog low-pass filter and a second signal strength measured at node A_O located in the signal path after the analog low-pass filter:

⁸ Although *Behbahani* describes a more precise process of ascertaining the absolute and relative strengths of a desired signal and interfering signals than is described in the '330 Patent, the claims do not preclude this additional precision. To simplify the mapping, Petitioner focuses on the signal strength measurements in *Behbahani* that align with the simpler process described in the '330 Patent.



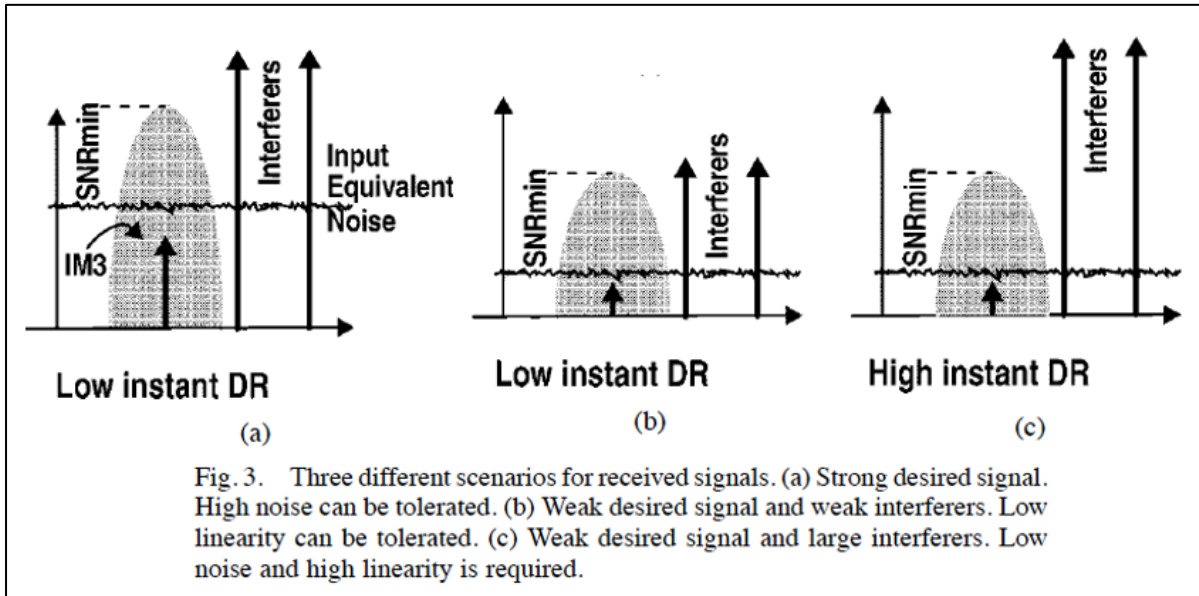
Behbahani modified by *Leete*, Figure 2 (annotated). Like the '330 Patent, *Behbahani* teaches that the difference between signal levels at nodes “A_I and A_O is a measure of the out-of-band interferers⁹ being rejected by the analog [low-pass filter].” *Behbahani*, 1207. *Behbahani* also measures the output of the digital filter (D_O),¹⁰ which indicates the absolute signal strength of a received desired signal. *Id.*

Behbahani explains that a weak desired signal (i.e., a low D_O) and significantly different levels at nodes A_I and A_O indicates worst case conditions as depicted in Fig. 3(c) below. *Id.* (“If the signal levels are significantly different at . . .

⁹ *Behbahani* teaches that major interferer signals originate from external devices. *Behbahani*, 1205 (“Microwave ovens emitting in the middle of the [2.4-GHz] band are often the largest interferer[.]”).

¹⁰ Petitioner’s Proposed Grounds do not rely on D_O or any other measurements on the signal path that are not part of the “analog chip.”

the above pairs of nodes (A_I and $A_O \dots$) and there is a weak signal at D_O , the condition must be the one shown in Fig. 3(c).”).



Id., Fig. 3 (rearranged). When such worst-case conditions are experienced, *Behbahani's* switched DR process uses the high-power filter to expand the DR and accommodate a low desired signal and high interferers. *Id.*, 1206. And, when signal strength measurements indicate appropriately better than worst-case conditions, *Behbahani's* system switches in the low-power filter, saving power, and implements the sliding DR process to track the desired signal strength. *Id.* The specific adjustments and their impact are discussed in more detail below with reference to limitation [1(b)].

In sum, *Behbahani*, like the '330 Patent, measures the signal strength of received signals at multiple nodes in the signal path on an integrated circuit,

including at nodes A_I and A_O, and uses those measurements to adjust DR. *Dec.*, ¶¶92-98.

Claim 1(b): “reducing a switching current in the signal path by dynamically changing an impedance of a component in the signal path based on the first signal strength.”

As discussed in Section II.C, the parties have advanced competing constructions in the parallel litigation for a number of terms—each of which is implicated by this limitation. The Proposed Grounds satisfy both parties’ proposals for most of these disputes, so the Board need not resolve them. For example, Petitioner proposed “signal path” is a path for an analog signal and that “switching current” is “the current that carries a signal through a load.” Patent Owner advocated a “plain and ordinary meaning” for both terms. Additionally, Patent Owner proposed that “impedance” is “opposition to the flow of alternating current,” and Petitioner advocated a plain and ordinary meaning for that term. As set forth below, satisfying both parties’ proposals, when *Behbahani*’s system switches from its high-power filter to its low-power filter, it increases the “opposition to the flow of alternating current” (i.e., impedance) in the analog signal path and results in a reduced current that carries the AC signal through a load (i.e., through the filter load).

As discussed in Section II.C, Petitioner proposes the Board adopt Patent Owner’s construction of the dynamic limitation, requiring only that an adjustment is made during operation based on information gained during operation. As set forth

below, *Behbahani* teaches switching from a high-power filter to a low-power filter based on signal strength measurements taken during operation.

A. The '330 Patent's Sole Inventor Admitted That *Behbahani's* Scaled Filter Approach Adjusts Signal Path Impedance Consistent With The Alleged Invention

Patent Owner cannot dispute that *Behbahani* teaches the dynamic impedance concept. Indeed, the Challenged Patent's sole inventor has previously pointed to *Behbahani's* scaled filter approach as an example of how one might dynamically adjust impedance in the signal path to respond to changing signal strengths. Inventor Tsividis, in a January 2003 article titled, "Internally Varying Analog Circuits Minimize Power Dissipation," described a "Dynamic Impedance Scaling" approach to save power when experiencing better than worst-case conditions. *See* Ex. 1011, 70; *Munford Dec.*, ¶¶18-21 (attesting to the public availability of this article). Dr. Tsividis' January 2003 article concludes its discussion by pointing to *Behbahani's* switched filter process as an exemplary means by which dynamic impedance scaling can be implemented. Ex. 1011, 70. Accordingly, for the dynamic impedance limitations that have plagued prior invalidity challenges, the Proposed Grounds here rely on *Behbahani's* scaled filter approach—an approach that Challenged Patent's inventor expressly identified as an example of how one could dynamically adjust impedance to save power.

A brief discussion of the January 2003 article connects its subject matter to the Challenged Claims and highlights that Dr. Tsividis did in fact point to *Behbahani* when discussing the concept in the dynamic impedance limitations. The article explains that systems are often designed “to handle very small signals in the worst case,” providing large Usable Dynamic Ranges (UDR), which require filters with large capacitance values. *Id.* It noted that, “when the desired signal happens to be strong and no strong blocker is present[,]” “the very low noise floor of this system is unnecessary and can be allowed to increase by scaling [the capacitance] down[.]” In addition to decreasing capacitance, the article explained that “the transconductances or conductances of the filter will have to be scaled together with [the capacitance] in order to leave the frequency response unchanged.” *Id.* Finally, the article explained that “impedance scaling” by “lowering capacitances and transconductances allows one to also lower I_{BIAS} , and thus the total power dissipation can be made small.” *Id.*; *see also id.*, 71 (“not[ing] that dynamic biasing is also encountered in the course of applying [] dynamic impedance scaling[.]”).

Increasing the resistance and decreasing capacitance in a filter circuit is the only specific example of dynamically adjusting signal path impedance discussed in the '330 Patent. '330 Patent, 7:44-52 (discussing Fig. 6 and its corresponding disclosure). Accordingly, a POSITA would understand that inventor Tsividis' description of dynamic impedance scaling in his January 2003 article aligns

precisely with his disclosure of dynamic impedance scaling described and claimed in the '330 Patent. *Dec.*, ¶¶100-105. Both proposed ***increasing signal path impedance*** by (1) decreasing transconductance (and increasing resistance)¹¹ and (2) decreasing capacitance of a filter, ***allowing lower DC bias current*** and ***lower AC switching current*** to save power.

Dr. Tsividis' January 2003 article concludes its discussion by pointing to *Behbahani's* switched filter process as an exemplary means by which dynamic impedance scaling can be implemented. Ex. 1011, 70 ("One way to achieve the above scenario would be to use two filters, designed with different capacitance values, and place one or the other in service as required [34], turning the other filter off."). Reference [34] is the same *Behbahani* reference that forms the basis of all Proposed Grounds herein. *Id.*, 72.

Accordingly, for the dynamic impedance limitations, the Proposed Grounds here rely on *Behbahani's* scaled filter approach—an approach that Challenged Patent's

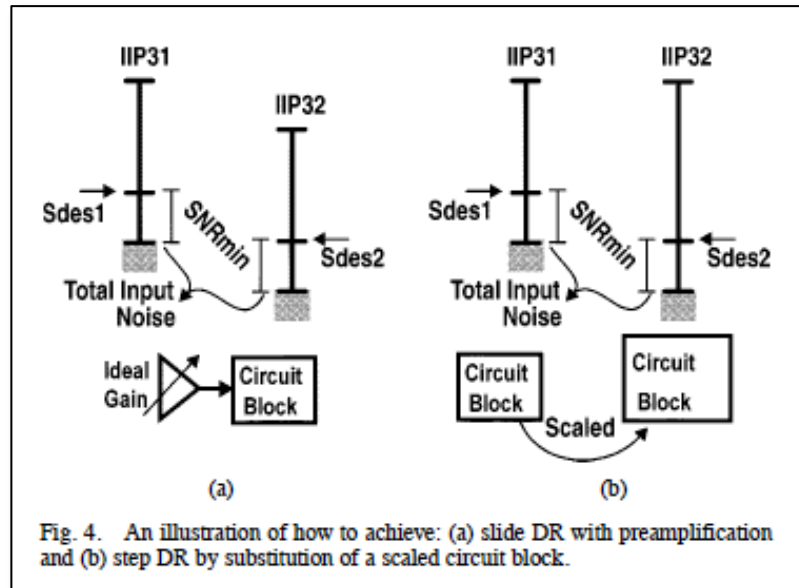
¹¹ As discussed in more detail with reference to the *Tan* paper, a POSITA would have understood that decreasing transconductance in filters was generally accompanied by an increased resistance. *Dec.*, ¶¶100-105. Accordingly, a POSITA would have understood that the January 2003 article's dynamic filter that maintains the same frequency response by ***decreasing transconductance*** and decreasing capacitance is analogous to the '330 Patent's dynamic filter that maintains the same frequency response by ***increasing resistance*** and decreasing capacitance. *Id.*

inventor expressly identified as an example of how one could dynamically adjust impedance to save power. “[A] patentee’s admissions about the scope and content of the prior art provide a factual foundation as to what a skilled artisan would have known at the time of invention[.]” *Qualcomm Inc. v. Apple Inc.*, 24 F.4th 1367, 1376 (Fed. Cir. 2022).

B. Switching From *Behbahani*’s High-Power Filter to Low-Power Filter Increases Signal Path Impedance

As explained above, *Behbahani* teaches a wireless receiver that implements an “adaptive dynamic range” method to save power by decreasing the dynamic range when conditions are better than worst-case. *Behbahani*, 1205. A step-based DR technique switches between two scaled filters, using “high-power filter” only during worst-case conditions and a separate “low-power filter” for conditions that are better than worst-case. *Id.*, 1206-07.

Fig. 4(b) below illustrates switching from the low-power filter to high-power filter to expand the DR when worst-case conditions are encountered:



Id. at 1206. A POSITA would understand that switching back—from the high-power filter to the low-power filter—when conditions improve is one means through which *Behbahani*'s system saves power during periods of better than worst-case conditions. *Dec.*, ¶¶107-110. Indeed, *Behbahani* expressly teaches that the high-power filter is used *only* during the infrequent periods of worst-case conditions. *Behbahani*, 1205 (“An important idea here . . . is that providing no more than the required DR at any given time lowers the average power consumption.”), 1207 (“[A] BPF dissipating low power is employed for nominal RX DR. However, in the worst-case scenario, the high-power scaled filter is switched in raising total DR. Since the worst-case scenario is infrequent, the low-power filter determines the average RX power consumption.”); *Dec.*, ¶¶107-110 (discussing the same).

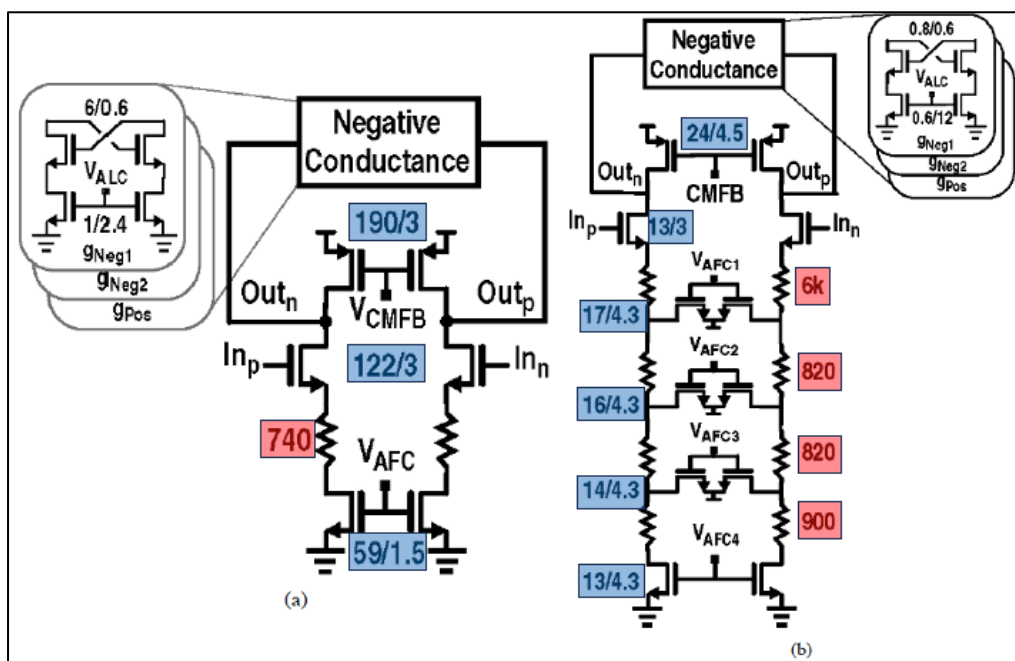
Scaling circuits was a well-known technique at the time. *Dec.*, ¶¶111-14 (discussing state of the art). As *Behbahani* explains, “[t]wo filters are implemented

with the same topology, but one, scaled up to consume 10x more power, offers 10x lower mean square noise but the same linearity.” *Behbahani*, 1207. *Behbahani* provides some detail about the scaled filters, including that its high-power filter “[s]cale[s] up all the transistors[,]” while “scaling down all resistors by the same factor[,]” which “**raises bias current** proportional to the scale factor[.]” *Id.*, 1206. *Behbahani* also explains that the filter input capacitance scales proportionately, noting the “filter input capacitance [] is, respectively, 0.4 and 4 pF for the low-power and the high-power versions.” *Id.*, 1208.

Tan provides additional details about the scaled filters discussed in *Behbahani*, and these additional details confirm that transitioning from the high-power to low-power filter increases signal path impedance. As with the *Leete* reference, *Behbahani* and *Tan* describe different aspects of the same circuit, and a POSITA would have been motivated to combine their teachings. *Dec.*, ¶116 (explaining that the authors intended *Behbahani*’s and *Tan*’s teachings to be used conjunctively and concluding that a POSITA would have expected success in doing so, as the authors intended). *Behbahani* notes that additional “details of the [filter] design are presented elsewhere [7].” *Behbahani*, 1210. [7] is a reference to *Tan*. *Id.*, 1216.

As suggested, *Tan* does in fact provide more detail on the scaled filter design used by the *Behbahani* receiver. For example, *Tan* proposes scaled G_m -C filters. *Tan*,

477. Tan notes that the “electrical characteristics of the G_m - C filter strongly depend on the G_m circuit.” *Id.* Examining the G_m circuit—a circuit that dictates the overall filter characteristics—reveals that the proposed low-power filter does in fact have lower transconductance, higher resistance, lower capacitance, and a lower bias current. *Dec.*, ¶¶117-124. Figs. 6(a) and 6(b) below illustrate how the transconductances and resistances vary together in the proposed scaled filters:



Tan, Figs. 6(a)-(b) (annotated). Annotated blue above, the transistor Width/Length ratio is directly related to transconductance, with a higher W/L ratio resulting in a higher transconductance. *Dec.*, ¶¶117-124. In the above example, we see W/L ratios ranging between 40-60 for the low-noise (high-power) filter stage depicted in Fig. 6(a) and much smaller W/L ratios ranging between 3-5.3 for the low-power filter stage depicted in Fig. 6(b). *Id.* (identifying a more than ten times increase in

transconductance with the high-power stage). Annotated red above, resistance has an inverse relationship to transconductance. For example, Fig. 6(a)'s higher transconductance is accompanied by a relatively small 740 Ohms in one leg of the circuit, while Fig. 6(b)'s lower transconductance is accompanied by a much higher 8,540 Ohms in one leg of its circuit. *Id.* A POSITA would have understood that the inverse relationship between transconductance and resistance was well known at the time. *Id.* (explaining that higher current capability of high transconductance transistors is typically paired with the low resistance to that higher current in the form of smaller resistors).

Consistent with *Behbahani's* own teachings, *Tan* describes a low-power filter that exhibits “the same frequency response and linearity” as the high-power filter, but that scales all “transconductances and capacitors in th[e] filter . . . by a factor of 10” and “consumes 10x lower power.” *Tan*, 480. *Tan* also confirms that the high-power filter utilizes a higher transconductance G_m (accompanied by lower resistance), higher capacitance, and higher bias current. *Id.*, 481; *Dec.*, ¶¶117-124 (explaining how *Tan's* teachings confirm that the signal path impedance changes when switching between scaled filters).

In sum, *Behbahani's* low-power filter has higher resistance (accompanying a lower transconductance), lower capacitance, and lower bias current than its high-power filter. *Dec.*, ¶124. This is precisely the arrangement disclosed in the '330

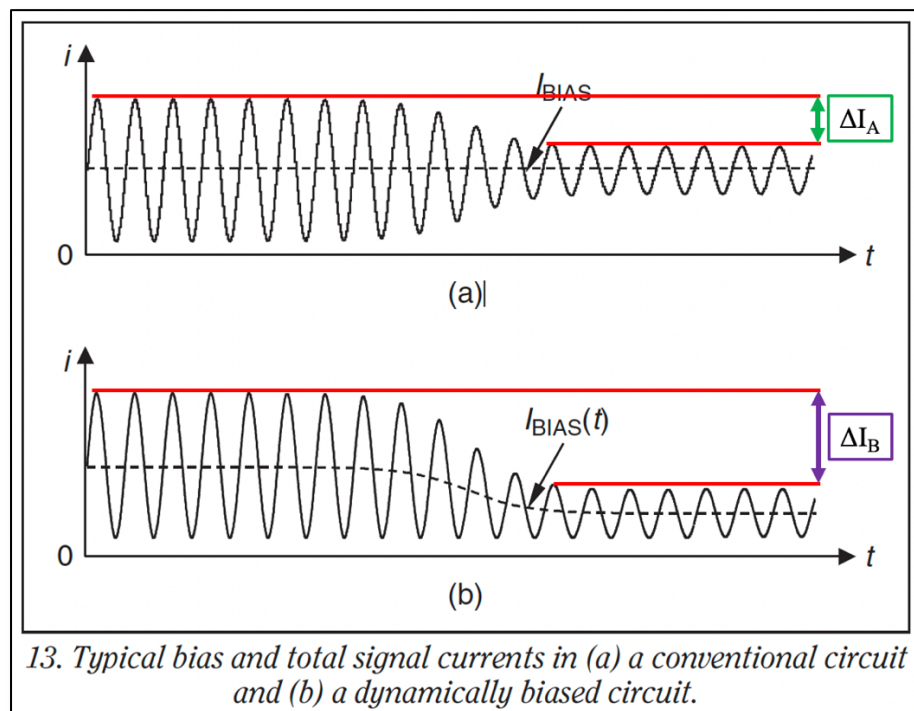
Patent and Dr. Tsividis' January 2003 paper. *Compare* '330 Patent, Fig. 6, 7:44-67 (describing a filter with increased resistance and decreased capacitance, which allows lower bias and drive currents); *with* Ex. 1011, 70 (describing a filter with lower capacitance and transconductances (accompanying higher resistance) that “allows one to also lower I_{BIAS} ”). A POSITA would have understood that, consistent with the '330 Patent and its inventors own publications, switching from *Behbahani's* high-power filter to its low-power filter dynamically changes (increases) an impedance of a component (the filter) in the signal path, as claimed. *Dec.*, ¶124.

C. Switching From a High-Power Filter to Low-Power Filter Lowers the Switching Current

As noted above, the '330 Patent does not identify a mechanism through which switching/drive current is reduced when signal path impedance is increased. Instead, the patent vaguely suggests that driving a larger signal path load impedance may *require* less current. '330 Patent, 7:49-52 (when the impedance load is doubled, “the output current required . . . is reduced by one-half”). This appears to be a reference to the well-understood Ohm's law, which defines the relationship between current (I), resistance (R), and voltage (V)— $V=I*R$. *Dec.*, ¶125. Per this relationship, if the voltage across a load is to be kept constant and the resistive load is doubled, only half the current is required to generate that constant voltage across the load. *Id.* Despite the vague references to Ohm's law, the '330 Patent never explains the mechanisms by which a drive current is reduced when a signal path impedance is

increased. At best, it alludes to a relationship between bias current and drive current, without elaboration. *See, e.g.*, '330 Patent, 7:60-67 (noting that increasing the signal path impedance is an example “where drive currents and possibly bias currents may be reduced”), 9:55-59 (“since the drive current is reduced, one or more bias current may also be reduced”).

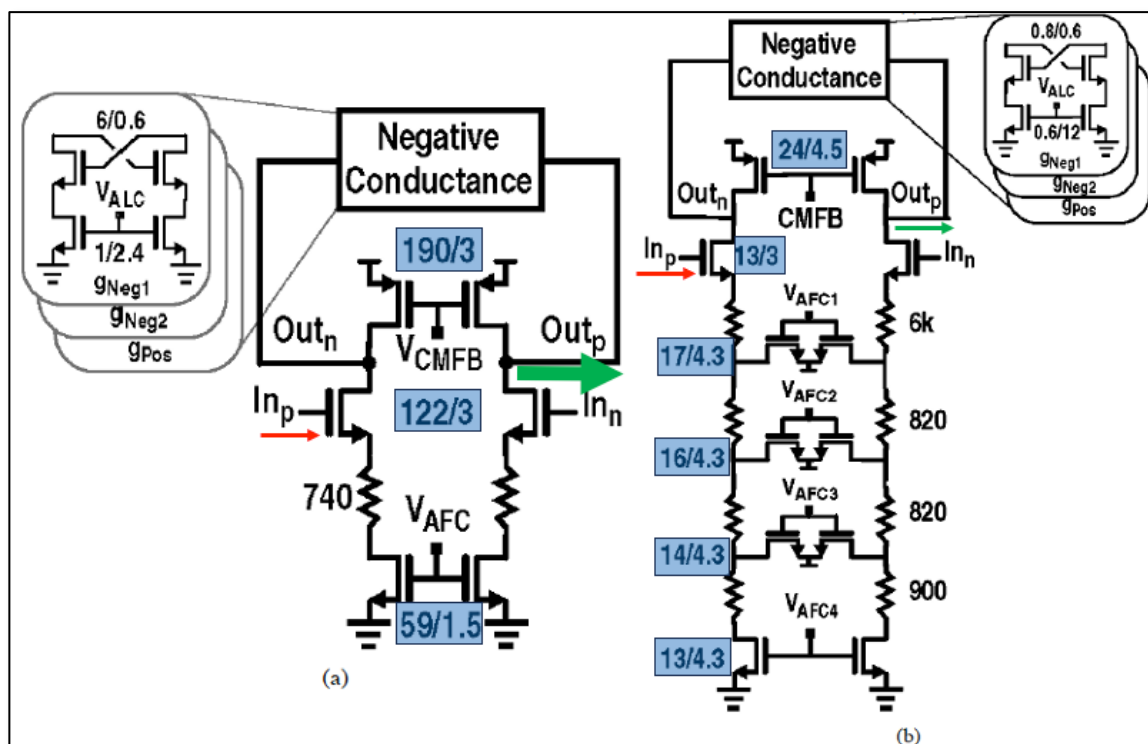
Dr. Tsividis' January 2003 article does provide a helpful example that illustrates the relationship between bias current and drive current.



Ex. 1011, 71 (annotated). As shown above, the AC drive current is a function of a DC bias current. *Dec.*, ¶126. In a conventional circuit that does not dynamically adjust the DC bias current (I_{BIAS}), small desired signals result in a total current drop ΔI_A , and the power remains unchanged, even when the signal level drops. *Id.* Power

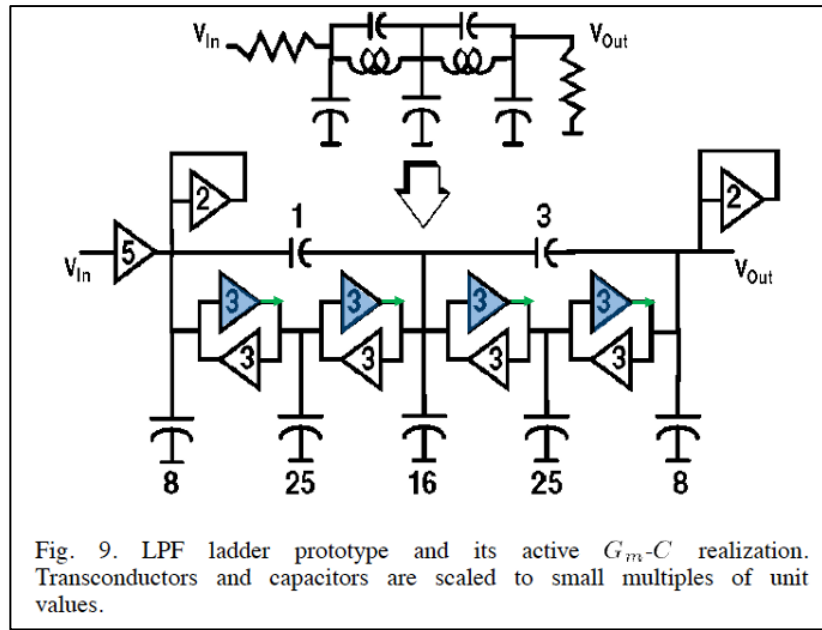
savings can be realized when the bias current $I_{BIAS}(t)$ is dynamically lowered as depicted in 13(b) above. There, lowering a DC bias ($I_{BIAS}(t)$) saves power by lowering the average switching current that flows through the circuit. *Id.* (noting that the dotted line represents average power).

Tan's additional filter detail confirms that the low-power filter will reduce an AC switching current in addition to increasing the signal path impedance. Specifically, the lower transconductance values in the low-power filter stages will, by their electrical characteristics, produce lower AC current in the signal path. In simple terms, transconductance is a measure of the output current over input voltage: $g_m = \Delta I_{out} / \Delta V_{in}$. *Dec.*, ¶¶102-105 (discussing the well understood concept of transconductance), ¶¶117-123. As discussed above, the transconductance of the low-power stage is more than ten times lower than the low noise (high-power) stage. Focusing on In_p and Out_p for simplicity, the below annotated Figs. 6(a)-(b) from *Tan*, shows that, for the same input voltage, the output current in the high-power filter will be much larger than the output current in the low-power filter as a result of the significantly different transconductance values:



Tan, Figs. 6(a)-(b) (annotated); *Dec.*, ¶128. (discussing the same).

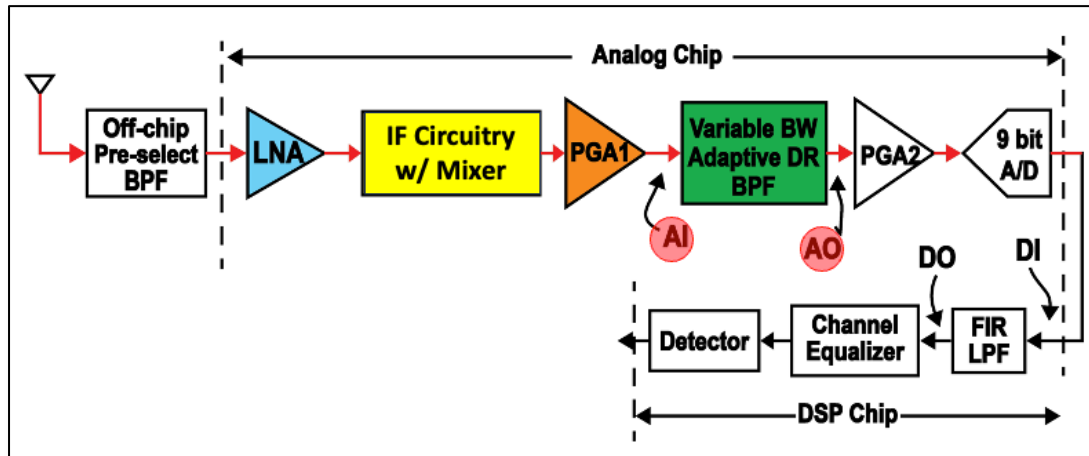
Tan's Fig. 9 depicts the full low pass G_m -C filter structure. As *Tan* explains, the filter uses pairs of transconductors in a differential negative feedback configuration (known as a gyrator) to simulate inductors in an LC ladder filter. *Tan*, 478, 480, Fig. 9. Each of the transconductors in this filter (represented by triangles in Fig. 9) includes either the circuit depicted in Fig. 6(a) (for the high-power filter) or Fig. 6(b) (for the low-power filter). *Dec.*, ¶128. Focusing on the forward current path through the transconductors of the filter circuit to simplify the discussion, the switching current carrying the IF signal is relatively higher when the transconductors are the high-power configuration of Fig. 6(a) and relatively lower when the transconductors are the low-power configuration of Fig. 6(b):



Tan, Fig. 9 (annotated); *Dec.*, ¶128 (explaining that the higher switching current that results from the high-power transconductor's larger transconductance produces an overall larger switching current through the filter).

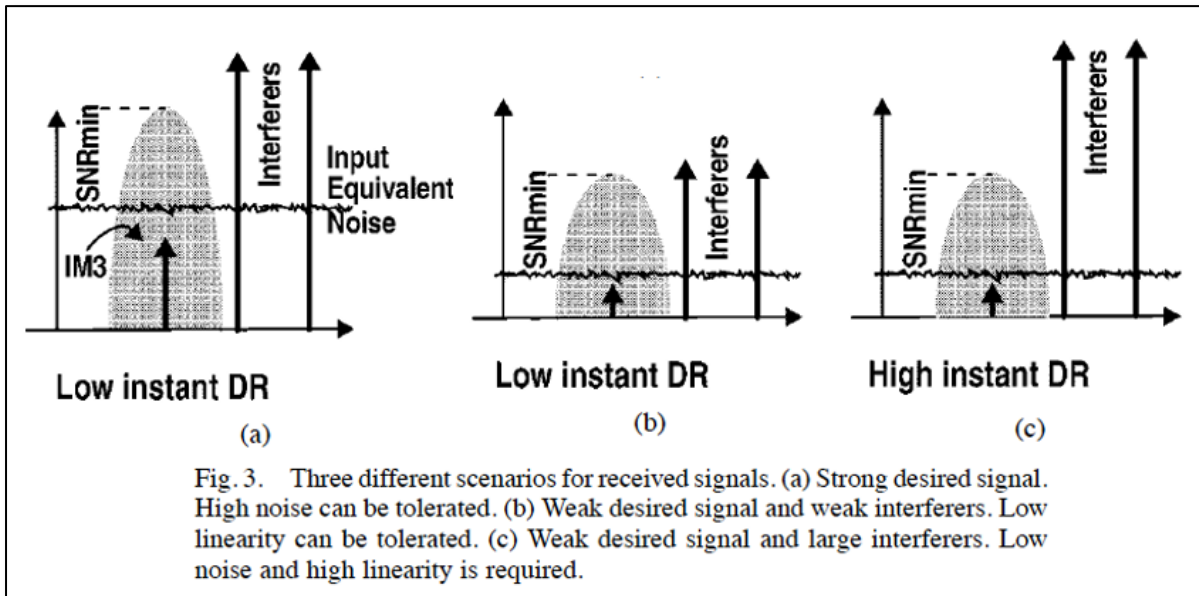
D. Behbahani Switches From a High-Power Filter to a Low-Power Filter Based on Signal Strength Measurements

As described above with reference to limitation [1(a)], *Behbahani* takes multiple signal strength measurements to ascertain signal conditions, including at a first signal strength measured at node A_I located in the signal path (annotated in red) before the analog low-pass filter and a second signal strength measured at node A_O located in the signal path after the analog low-pass filter:



Behbahani modified by *Leete*, Figure 2 (annotated). Like the '330 Patent, *Behbahani* teaches that the difference between signal levels at nodes “A_I and A_O is a measure of the out-of-band interferers being rejected by the analog [low-pass filter].” *Behbahani*, 1207. *Behbahani* also measures the output of the digital filter (D_O), which indicates the absolute signal strength of a received desired signal. *Id.*

Behbahani explains that a weak desired signal (i.e., a low D_O) and significantly different levels at nodes A_I and A_O indicates worst case conditions as depicted in Fig. 3(c) below. *Id.* (“If the signal levels are significantly different at . . . the above pairs of nodes (A_I and A_O . . .) and there is a weak signal at D_O, the condition must be the one shown in Fig. 3(c).”).



Id., Fig. 3 (rearranged).

When such worst-case conditions are experienced, *Behbahani's* switched DR process uses the high-power filter to expand the DR and accommodate a low desired signal and high interferers. *Id.*, 1206. And, when signal strength measurements indicate better than worst-case conditions, *Behbahani's* system switches in the low-power filter, saving power, and implements the sliding DR process to track the desired signal strength. *Id.*; see also *Dec.*, ¶¶129-132 (confirming *Behbahani's* use of signal strength measurements to implement sliding DR and switched DR.).

Accordingly, a POSITA would understand that switching from the high-power filter to low-power filter is based on signal strength measurements taken at multiple nodes in the signal path on an integrated circuit, including at nodes A_I and A_O . *Dec.*, ¶¶129-132.

In sum, switching from *Behbahani*'s high-power filter to its low-power filter based on signal strength measurements (1) increases the signal path impedance and (2) lowers the DC bias applied to the filter stage. It also lowers the switching current—the current carrying an AC signal. *Id.*, ¶133.

2. Claim 2

Claim 2(a): “The method of claim 1 wherein the signal comprises a preamble portion and a data portion,”

Behbahani teaches a method of receiving a signal using an integrated circuit. See Claim 1 (Pre) (explaining that the components depicted in *Behbahani*'s Fig. 2 and referred to as “analog chip” are part of an integrated circuit).

Behbahani further teaches that such signal comprises a preamble portion and a data portion. Specifically, *Behbahani* explains that switching between the low-power and high-power filters should occur during the preamble to ensure bit errors that result from the switch have settled out before the data portion is received:

An abrupt switch from the low-power to the high-power filter causes the BER [bit error rate] to increase momentarily. However, as *data* transmitted in frames is ***preceded by a preamble*** and training sequence, the desired filter is switched ***during the preamble*** and settles during that time, eliminating increase in bit error rate (BER) ***during the data sector***.

Behbahani, 1207.

Claim 2(b): “the impedance of a component is changed while receiving the preamble portion, and”

Behbahani teaches changing an impedance of a component in the signal path. See Claim [1(b)]. When *Behbahani*’s system switches from its high-power filter to its low-power filter, it changes (increases) the “opposition to the flow of alternating current” (i.e., impedance) in the analog signal path and results in a reduced current that carries the AC signal through a load (i.e., through the low-pass filter load)). *Id.*

Further, *Behbahani* expressly teaches that “the ***desired filter is switched during the preamble*** and settles during that time[.]” *Behbahani*, 1207. Accordingly, *Behbahani* teaches that changing of impedance (e.g., switching from high-power filter to its low-power filter) of a component occurs while receiving the preamble portion of the signal. *Dec.*, ¶¶135-36.

Claim 2(c): “the method further comprises receiving the data portion of the signal.”

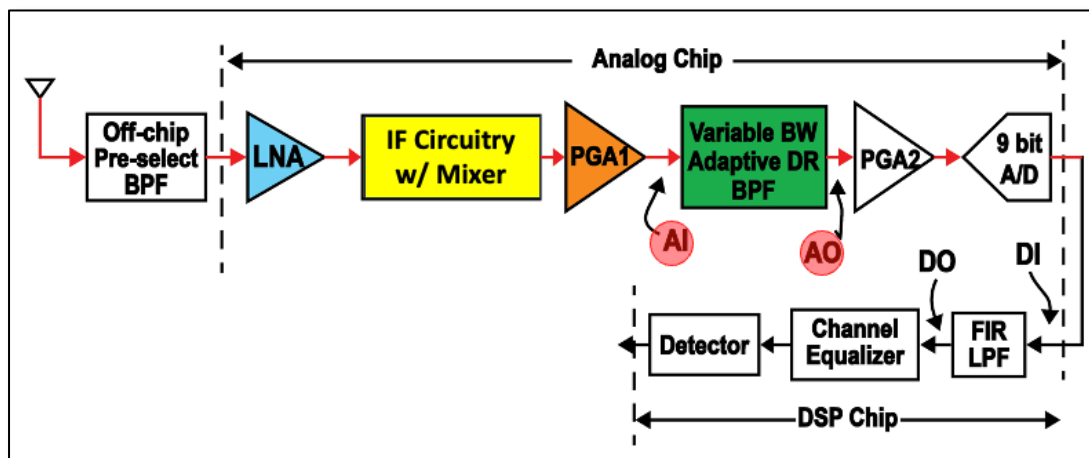
Behbahani explains that that the received signal includes “data transmitted in frames” that is received after the desired filter switched during receipt of the preamble has settled, “eliminating increase in bit error rate (BER) during the ***data sector***.” *Behbahani*, 1207. A POSITA would have understood that *Behbahani*’s “data sector” is the received data portion of the signal. *Dec.*, ¶137.

3. Claim 3

Claim 3: “The method of claim 2 further comprising: determining a second signal strength at a second node in the signal path, wherein the second node in the signal path is after the first node in the signal path.”

As discussed above with respect to claims [1(Pre)] through [1(a)], *Behbahani* teaches a method for receiving a signal using an integrated circuit, and determining a first signal strength at a first node (A_I) in the signal path and a second signal strength at a second node (A_O) in the signal path in the integrated circuit.

Behbahani’s Fig. 2 below depicts node A_O after node A_I in the signal path:



Behbahani modified by *Leete*, Figure 2 (annotated); see Claim [1(Pre)-1(a)].

4. Claim 4

Claim 4: “The method of claim 3 wherein the impedance of the component in the signal path is also changed based on the second signal strength.”

Behbahani teaches changing an impedance of a component in the analog signal path based on signal strength measurements (including first and second signal strength measurements at nodes A_I and A_O) taken during operation. See Claim

[1(Pre)-1(b)]. Namely, as explained in more detail with reference to element [1(b)] and Claim 3, *Behbahani* teaches switching from the high-power filter to low-power filter (which changes the signal path impedance) based on signal strength measurements taken at multiple nodes in the signal path on an integrated circuit, including at nodes A_I and A_O. *See* Claims [1(b)], 3.

5. Claim 5

Claim 5: “The method of claim 2 wherein the component in the signal path comprises a MOS transistor.”

Behbahani switches between a high-power filter and low-power filter based on signal strength measurements and the specific filter structures are described in detail by *Tan* and illustrated at least in Figs. 6(a)-(b) and Fig. 9. *See* Claim [1(b)].

As discussed above in the [1(b)] mapping, *Tan* describes a transconductance core that is key to the variable filter design in which different transconductor circuits are used for the low-power filter and for the high-power filter. *See, e.g., Tan*, 478-80, Fig. 6. *Tan* explains that each of these transconductance cores utilizes MOSFET transistors. *Id.*, 478. A POSITA would have understood that MOS is a reference to the physical structure of the transistor—Metal Oxide Semiconductor. *Dec.*, ¶143. A POSITA would also have understood that FET is a reference to operation of the device as a Field-Effect Transistor. *Id.* (noting that *Tan* at 478 expressly defines FET as “field-effect transistor”). Accordingly, a POSITA would have understood that the

variable filter described by Tan and relied upon by Petitioner in the mapping above does in fact comprise MOS transistors, as claimed. *Id.*, ¶¶141-44.

6. Claim 6

Claim 6: “The method of claim 2 wherein the component in the signal path comprises a resistor.”

Behbahani switches between a high-power filter and low-power filter based on signal strength measurements, and the specific filter structures are described in detail by *Tan* and illustrated at least in Figs. 6(a)-(b) and Fig. 9. *See* Claim [1(b)].

As discussed above in the [1(b)] mapping, *Tan* describes a transconductance core that is key to the variable filter design in which different transconductor circuits are used for the low-power filter and for the high-power filter. *See, e.g., Tan*, 478-80, Fig. 6. As illustrated in Fig. 6, *Tan* explains that each of these transconductance cores includes resistors. *Id.*; *see also Behbahani*, 1206 (explaining that its high-power filter “[s]cale[s] up all the transistors” while “**scaling down all resistors** by the same factor”). Accordingly, a POSITA would have understood that the variable filter described by *Tan* and relied upon by Petitioner in the mapping above does in fact comprise resistors, as claimed. *Dec.*, ¶¶145-151.

7. Claim 7

Claim 7: “The method of claim 2 wherein the component in the signal path comprises a capacitor.”

Behbahani switches between a high-power filter and low-power filter based on signal strength measurements, and the specific filter structures are described in detail by Tan and illustrated at least in Figs. 6(a)-(b) and Fig. 9. *See* Claim [1(b)].

As discussed above in the [1(b)] mapping, *Tan* describes a transconductance core that is key to the variable filter design in which different transconductor circuits are used for the low-power filter and for the high-power filter. *See, e.g., Tan*, 478-80, Fig. 6. As illustrated in Fig. 9, *Tan* explains that each of these transconductance cores includes capacitors *Id.*; *see also Behbahani*, 1208 (“filter input capacitance [] is, respectively, 0.4 and 4 pF for the low-power and the high-power versions.”). Accordingly, a POSITA would have understood that the variable filter described by *Tan* and relied upon by Petitioner in the mapping above does in fact comprise capacitors, as claimed. *Dec.*, ¶¶152-59.

8. Claim 9

Claim 9: The method of claim 4 wherein the component in the signal path is included in the low-pass filter.

Behbahani switches between a high-power filter and low-power filter based on signal strength measurements, and the specific filter structures are described in detail by *Tan* and illustrated at least in Figs. 6(a)-(b) and Fig. 9. *See* Claim [1(b)]. Further, as described above with respect to claim [1(Pre)], *Behbahani* discloses that the component (i.e., variable BW adaptive DR BPF) in the signal path includes a low-pass filter (LPF). *See* Claim 1(Pre) (explaining *Behbahani*’s BPF as a high-order

LPF cascaded with a low-order HPF). As discussed in detail with reference to Claim [1(b)], the impedance of the low-pass filter, specifically, is increased when switching from the high-power filter to the low-pass filter, resulting from changes to the transconductance stages and capacitors that comprise the variable low-pass filters. See Claim [1(b)].

9. Claim 10

Claim 10(Pre): “A method of receiving a signal comprising a preamble portion and a data portion using an integrated circuit, the integrated circuit comprising a signal path including a low-noise amplifier configured to receive the signal, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer, the method comprising:”

See Claim [1(Pre)], Claim 2.

Claim 10(a): “determining a first signal strength at a first node in the signal path in the integrated circuit; and”

See Claim [1(a)].

Claim 10(b): “while receiving the preamble portion of the signal, dynamically changing a bias current in the signal path based on the first signal strength, and while receiving the data portion of the signal, maintaining the bias current in the signal path.”

Behbahani teaches switching between a low-power and high-power filter during receipt of a preamble portion of a signal to ensure that circuit has settled by the time the data portion of the signal is received. See Claim 2. And, as also discussed above, *Behbahani* teaches (1) that switching between these filters based on first and second signal strength measurements and (2) that switching between the filters

dynamically changes the bias current of the filter circuit. *See* Claim [1(a)-(b)]. A POSITA would have understood that, absent further DR adjustments based on changing signal conditions, the new bias current applied after switching filters is maintained while receiving the data portion of the signal. *Dec.*, ¶¶165-69 (discussing *Behbahani*'s teaching at p. 1207 that adjustments should settle during the preamble time, "eliminating increase in bit error rate (BER) during the data sector"). Accordingly, a POSITA would have understood that *Behbahani* dynamically changes a bias current in the signal path based on a signal strength measurement and maintains the new bias current while receiving the data portion of the signal, as claimed. *Id.*

10. Claim 11

Claim 11: "The method of claim 10 wherein the method further comprises receiving the data portion of the signal."

See Claim [2(c)].

11. Claim 12

Claim 12: "The method of claim 11 further comprising: determining a second signal strength at a second node in the signal path, wherein the second node in the signal path is after the first node in the signal path."

See Claim 3.

12. Claim 13

Claim 13: "The method of claim 12 wherein the bias current in the signal path is also changed based on the second signal strength."

As discussed above with respect to claims [1(Pre)] through [1(b)], and [10(b)], *Behbahani* teaches changing a bias current of a component (e.g. low-pass filter) in the analog signal path based on signal strength measurements (including measurements at nodes A_I and A_O) taken during operation. *See* Claim [1(Pre)-1(b)], [10(b)].

13. Claim 16

Claim 16: “The method of claim 11 wherein the bias current is a bias current for the low-pass filter.”

Behbahani teaches switching between low-power and high-power filters based on signal strength measurements and teaches that switching between these filters dynamically changes the bias current of the low-pass filter circuits. *See* Claim [1(a)-(b)]. And, as discussed above with reference to Claim 9, these filters include low pass filter stages that have distinct bias currents. *Dec.*, ¶174 (explaining that the low pass filter stages in each of the low-power and high-power filter stages is dynamically changed).

14. Claim 23

Claim 23(Pre): “A wireless transceiver integrated circuit comprising: a receiver comprising a signal path, the signal path comprising: a low-noise amplifier; a mixer having an input coupled to an output of the low-noise amplifier; and a low-pass filter having an input coupled to an output of the mixer; and”

Behbahani in view of *Leete* discloses a method of receiving an RF signal using an integrated circuit, the integrated circuit comprising a signal path including a low-

noise amplifier followed by a mixer, which is followed by a low-pass filter. *See* Claim [1(Pre)].

Claim 23 additionally requires that the receiver is part of a “wireless transceiver[.]” A POSITA would have understood that *Behbahani*’s receiver circuitry is in fact part of a wireless transceiver, i.e., is in a device that includes both transmission and reception functionality. *Dec.*, ¶¶176-78. Indeed, although *Behbahani* focuses on the details of receiver circuitry, *Behbahani* expressly notes that the receiver is part of a transceiver. *Behbahani*, 1207 (“This frequency-hopping *transceiver* uses many adaptive algorithms at each hop[.]”), 1208 (noting “a maximum speed of 2 m/s for the indoor mobile *transceiver*”). Accordingly, a POSITA would have understood that, although the paper focuses on the receiver circuitry, *Behbahani* does in fact teach that its receiver circuitry is intended to be used in a mobile device with a complete transceiver. *Dec.*, ¶178.

Claim 23(a): “a first signal strength indicator circuit coupled to the signal path, and configured to determine a first signal strength;”

Behbahani teaches determining a first signal strength at a first node (A_1) in the signal path in the integrated circuit. *See* Claim [1(a)].

Although *Behbahani* does not provide details about the specific circuit used to measure signal strength, *Tan* does. *Tan*—a reference expressly referenced by *Behbahani* and intended to be used in conjunction with *Behbahani* (*see* Claim [1(b)])—provides an example of circuitry used to detect signals at various points in

the low-pass filter signal path as a means of implementing a prefilter automatic gain control (AGC). *Tan*, 481. In this example, signal peaks are detected by current summing circuitry that is designed to “lower the input signal” via gain control when peak values exceed a predefined limit. *Id.* A POSITA would have been motivated to utilize *Tan*’s signal strength measurement circuitry to measure nodes A_I and A_O in *Behbahani* for a number of reasons. First, as already explains with reference to limitation [1(b)] above, *Behbahani* and *Tan* describe different aspects of the same circuit, and a POSITA would have been motivated to combine their teachings at least based on *Behbahani*’s express teaching that the references are intended to be used conjunctively. *Dec.*, ¶¶179-181 (explaining that the authors intended *Behbahani*’s and *Tan*’s teachings to be used conjunctively and concluding that a POSITA would have expected success in doing so). Second, a POSITA would have understood that using *Tan*’s signal strength measurement circuits in *Behbahani*’s receiver, as proposed, uses a known technique to improve a similar device in the same way. *Id.* *Tan*’s peak detectors provide the benefit that the circuit can be dynamically adjusted to avoid clipping the peaks in the amplifier and filter circuits, which could cause a damaging amount of distortion. *Id.* (explaining the importance of detecting the peak levels and using those peak levels to adjust gain). Finally, a POSITA would further have understood that signal strength measurement circuitry was well understood that

the time, which further motivates the combination and supports a conclusion that a POSITA would have expected success in combining these teachings. *Id.*

Claim 23(b): “wherein an impedance in the signal path is configured to be dynamically adjusted to reduce a switching current in response to the first signal strength.”

See Claim [1(b)].

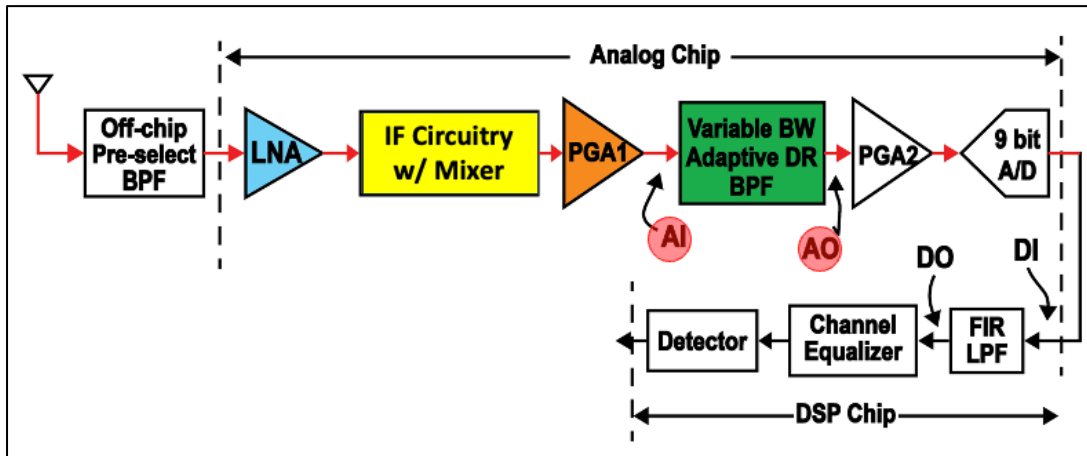
15. Claim 25

Claim 25 (a): “The wireless transceiver of claim 23 further comprising: a second signal strength indicator circuit coupled to the output of the low-pass filter, and configured to determine a second signal strength,”

As described above, *Behbahani* renders obvious signal strength indicator circuits (including a first signal strength indicator circuit and a second signal strength indicator circuit) to detect the signal power at nodes A_I and A_O . *See* Claim [23(a)].

As discussed above, a second signal strength is measured at a second node A_O . *See* Claim [1(a)].

Behbahani’s Fig. 2 (modified by *Leete* as described in reference to Claim 1) below a second signal strength measured at node A_O located in the signal path and coupled to the output of the low-pass filter:



Behbahani modified by *Leete*, Figure 2 (annotated); *see also* Claim [1(Pre)] (explaining that *Behbahani*'s Variable BW Adaptive DR BPF includes a low-pass filter).

A POSITA would have understood that the second signal strength indicator circuit is coupled to the output of the low-pass filter. *Dec.*, ¶185 (explaining that the node A_O is coupled to the output of a low-pass filter, and that the second signal strength indicator circuit would be coupled to the output of the low-pass filter in order to process the second signal strength measured at node A_O).

Claim 25 (b): “wherein the first signal strength indicator is coupled to the output of the mixer, and”

As discussed above, “coupled to” should be interpreted broadly enough to capture both direct and indirect connections. *See* Claim [1(Pre)]. As discussed above, a first signal strength is measured at a first node A_I . *See* Claim [1(a)]. Applying this meaning of “coupled to,” as illustrated in the annotated Fig. 2 above, the first node

A_I where the first signal strength is measured is coupled to the output of a mixer.
Dec., ¶186.

It appears patent owner intended to include “circuit” to “the first signal strength indicator circuit”, but to the extent patent owner did not intent to include “circuit”, our prior art teaches the claim either way.

A POSITA would have understood that the first signal strength indicator circuit is coupled to the output of the mixer. *Dec.*, ¶188 (explaining that the first signal strength measured at node A_I is coupled to the output of a mixer, and that the first signal strength indicator circuit would be coupled to the output of the mixer in order to process the first signal strength measured at node A_I).

Claim 25 (c): “wherein the impedance in the signal path is configured to be adjusted in response to the first and second signal strengths.”

Behbahani teaches changing an impedance of a component in the signal path based on two analog signal strength measurements (at nodes A_I and A_O) taken during operation. *See* Claim [1(a)-(b)].

16. Claim 26

Claim 26(Pre): “A wireless transceiver integrated circuit comprising: a receiver comprising a signal path, the signal path comprising: a low-noise amplifier; a mixer having an input coupled to an output of the low-noise amplifier; and a low-pass filter having an input coupled to an output of the mixer; and”

See Claim [23(Pre)].

Claim 26(a): “a first signal strength indicator circuit coupled to the signal path, and configured to determine a first signal strength, the first signal strength [is] the strength of a signal comprising a preamble portion and a data portion;”

Behbahani renders obvious signal strength indicator circuits to detect the signal power at nodes A_I and A_O . *See* Claim [23(a)]. As also discussed above, *Behbahani* teaches (1) dynamically adjusting the bias current and signal path impedance based on signal strength measurements at nodes A_I and A_O and (2) making the dynamic adjustment when receiving the preamble portion to ensure all changes as a result of the dynamic adjustment have settled out when the data portion is received. *See* Claims [1(a)-(b)], 2, 13.

This limitation requires the signal strength comprises a preamble portion and a data portion. To the extent this limitation merely requires the overall signal to sequentially comprise both preamble portions and data portions and to measure the overall signal as a means of determining when to dynamically adjust the bias current, it is satisfied as discussed in the prior mappings.

To the extent the limitation alternatively requires a signal strength measurement that includes a measure of signal strength capturing periods during which the preamble is received and period during which the data portion is received, the claim appears to be inoperable and finds no support in the Challenged Patent specification. Read in conjunction with the remainder of Claim 26, this limitation requires (1) measuring the signal strength at a node, (2) dynamically adjusting a bias

current in response to the signal strength measurement, (3) making that dynamic adjustment during reception of the preamble portion, and (4) maintaining the new bias current during reception of the data portion. Accordingly, the signal strength measurement that determines when to dynamically adjust the bias current necessarily takes place *before* the data portion is received. Where the signal strength measurement required to capture signal strength energy during both the preamble portion and data portion, the required dynamic adjustment could not take place, as claimed. Indeed, there would be no way to make the adjustment before the data portion is received if the data portion must be part of the claimed signal strength measurement. Accordingly, Petitioner has not mapped prior art to this alternative read.

Claim 26(b): “wherein a bias current in the signal path is configured to be dynamically adjusted during the preamble portion of the signal in response to the first signal strength and further configured to be maintained during the data portion of the signal.”

See Claim [10(b)].

17. Claim 28

Claim 28(a): “The wireless transceiver of claim 26 further comprising: a second signal strength indicator circuit coupled to the output of the low-pass filter, and configured to determine a second signal strength,”

See Claim [25(a)].

Claim 28(b): “wherein the first signal strength indicator is coupled to the output of the mixer, and”

See Claim [25(b)].

Claim 28(c): “wherein the bias current in the signal path is configured to be adjusted in response to the first and second signal strengths.”

See Claims [10(a)-(b)], 13.

18. Claim 29

Claim 29(Pre): “A wireless transceiver integrated circuit comprising: a receiver comprising a signal path, the signal path comprising: a first circuit; and a second circuit having an input coupled to an output of the first circuit; and”

Behbahani teaches a wireless transceiver integrated circuit comprising: a receiver comprising a signal path, the signal path comprising: a first circuit (*Behbahani*’s PGA1); and a second circuit having an input coupled to an output of the first circuit (*Behbahani*’s Variable BW Adaptive DR BPF). See Claim [1(Pre)], [23(Pre)].

Claim 29(a): “a first signal strength indicator circuit coupled to the signal path, and configured to determine a first signal strength;”

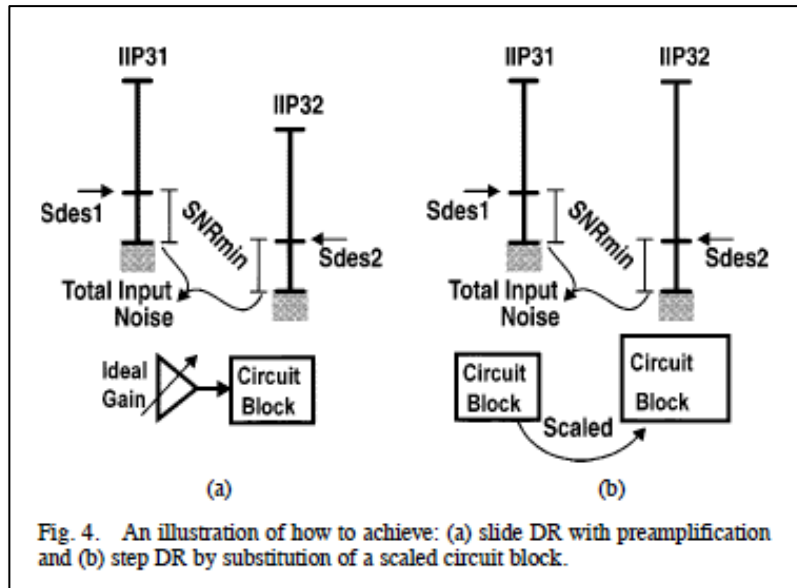
See Claim 23(a).

Claim 29(b): “wherein a gain of the first circuit is configured to be dynamically adjusted in response to the first signal strength, and”

As discussed above, *Behbahani* teaches two separate adaptive techniques are for adjusting dynamic range (DR) responsive to signal conditions—(1) step-based DR and (2) sliding DR. *Behbahani*, 1206-07. For *Behbahani*’s step-based adaptive DR, as discussed at length in the above mappings, the receiver switches/steps between two scaled filters. *Id.* A “high-power filter” is used only during worst-case

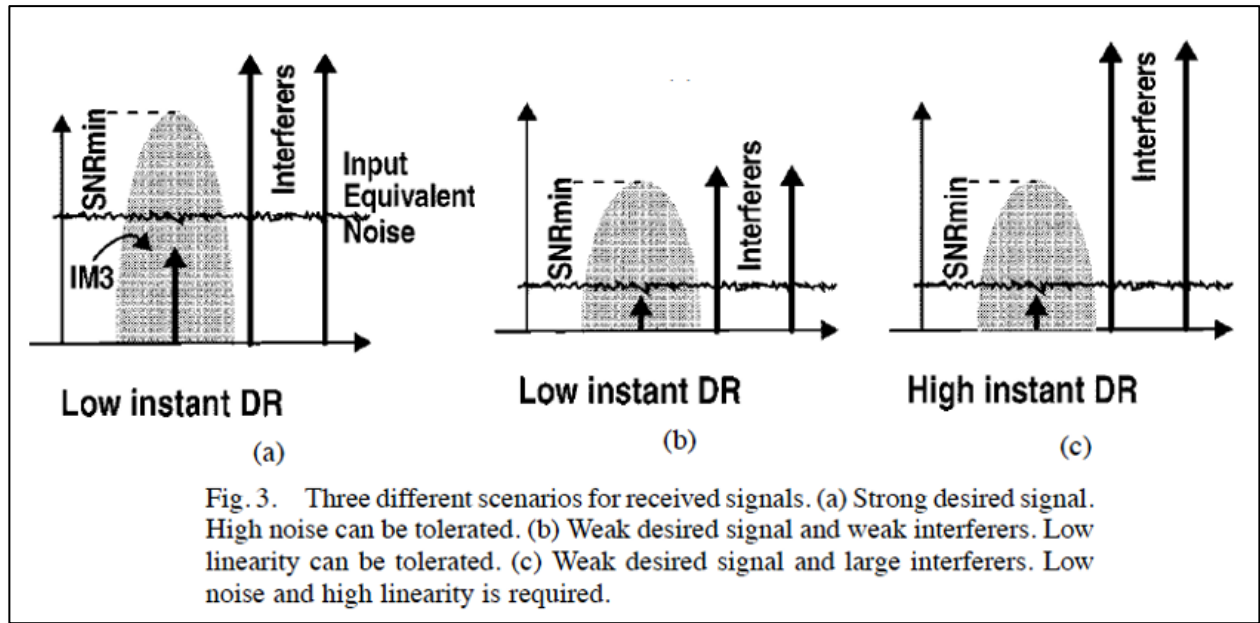
conditions, and a separate “low-power filter” is used for conditions that are better than worst-case. *Id.* When the low-power filter is utilized during better than worst-case conditions, *Behbahani’s* sliding DR technique uses a gain stage in advance of the low-power filter to slide a smaller DR up or down based on strengths of the received signals. *Id.*

Behbahani’s step-based adaptive DR is responsive to signal strength measurements, including at A_I and A_O . *See* Claims [1(a)-(b)], 3, 4. *Behbahani’s* sliding DR is similar responsive to signal strength measurements. Indeed, the same signal strength measurement algorithm used to determine when to deploy step-based DR is also used to implement sliding DR. *Behbahani*, 1207 (describing the “algorithm to sense the input signal and determine instant DR” and noting when the algorithm triggers sliding DR and when it triggers step-based DR). Specifically, Fig. 4(a) illustrates a gain stage (PGA1 in Fig. 2) used to slide a smaller DR (that results from using the low-power filter) to accommodate specific signal strength conditions, and Fig. 4(b) illustrates switching from the low-power filter to high-power filter to expand the DR when worst-case conditions are encountered:



Id., 1206.

Behbahani describes three different desired and interferer signal scenarios below in Figure 3. Figs. 3(a) and Fig. (b) depict better than worst-case conditions in which “receiver dynamic range may be modest” and the gain-based sliding DR approach is sufficient. *Id.* Fig. 3(c) depicts worst-case conditions (i.e., low desired signal and high interferers), requiring the system to expand the dynamic range by switching in the high-power filter. *Id.*



Id., Fig. 3 (rearranged).

Behbahani explains that measurements indicating comparable signal power at A_I and A_O means the “required instant DR is low” as is the examples illustrated in Figs. 3(a) and 3(b). *Id.* at 1207. When such a low instant DR can be tolerated, *PGA1* is used to slide the smaller DR up or down to accommodate the instant level of the desired signal:

The pre-BPF amplifier, *PGA1*, *slides the input DR of the BPF to best fit the instant level of the input signal*, as shown in Fig. 4(a). As mentioned before, *for a weak desired signal* where a low NF is needed, *PGA1 is set to high gain* to overcome the high NF of the filter. *When the input signal is strong, PGA1 is set to low gain* and high OIP3 to preserve the IIP3 of the BPF.

Id. Accordingly, like the step-based DR addressed in detail for Claim 1 above, *Behbahani's* sliding DR that adjusts PGA1 is also responsive to signal strength measurements A₁ and A₀. *Dec.*, ¶¶198-202.

Claim 29(c): “wherein an impedance in the second circuit is configured to be dynamically adjusted in response to the first signal strength.”

See Claim 23(b).

VI. DISCRETION UNDER 35 U.S.C. §325(d)

Section 325(d) provides that, in determining whether to institute a post-grant review, “the Director may take into account whether, and reject the petition or request because, the same or substantially the same prior art or arguments previously were presented to the Office.” The Board uses a two-part framework for evaluating arguments under § 325(d):

- (1) whether the same or substantially the same art previously was presented to the Office or whether the same or substantially the same arguments previously were presented to the Office; and
- (2) if either condition of first part of the framework is satisfied, whether the petitioner has demonstrated that the Office erred in a manner material to the patentability of challenged claims.

Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH, IPR2019-01469, Paper 6 at 8 (PTAB Feb. 13, 2020) (precedential) (“*Advanced Bionics*”). In applying the two-part framework, the Board considers several nonexclusive factors

set forth in *Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 at 17–18 (PTAB Dec. 15, 2017).

The Proposed Grounds rely on *Behbahani* and *Tan*, which were cited on the face of the '330 Patent, but were not discussed by the Examiner during prosecution. The fact neither reference was applied in a rejection weighs strongly against denying institution under § 325(d). See *CrowdStrike, Inc. v. Webroot Inc.*, IPR2023-00126, Paper 9 at 14 (PTAB May 5, 2023) (“[the Board] cannot determine the extent to which [cited reference] was evaluated during the examination because it was never used in a rejection” and because “[cited reference] was not the basis of a rejection, there is no overlap of arguments.”); *Scientific Design Co. Inc. v. Shell Oil Co.*, IPR2022-00158, Paper 7, 24-26 (PTAB Apr. 4, 2022) (declining to exercise discretion under § 325(d) based on “credit[ing] Petitioner’s argument that although the references ‘were cited in an IDS, together with 111 references, none of them was used in any rejections, or otherwise addressed by the examiner’”); *Bowtech, Inc. v. MCP IP, LLC*, IPR2019-00379, Paper 14 at 18 (PTAB Jul. 3, 2019) (“[the Board has] consistently held that a reference that was neither applied against the claims nor discussed by the Examiner does not weigh in favor of exercising our discretion under § 325(d).”).

As highlighted by the strength of the Proposed Grounds, it is evident that the Examiner did not appreciate *Behbahani*’s disclosures and how this reference in

combination with *Tan* and *Leete* (not previously before the Office) render the Challenged Claims obvious. When a reference was never “substantively discussed by the Examiner[,]” “a petitioner’s showing that the challenged claims are unpatentable over the asserted prior art may itself be evidence of material error by the Office during prosecution.” *Quasar Science LLC v. Colt International Clothing, Inc. d/b/a Colt LED*, IPR2023-00611, Paper 10 at 14 (PTAB Oct. 10, 2023) (“Quasar”).

Therefore, denial under 35 U.S.C. § 325(d) is not warranted.

VII. DISCRETIONARY DENIAL IS NOT WARRANTED

A. The *General Plastic* Factors Favor Institution

The Board set forth seven factors it considers in determining whether to exercise discretion to deny a petition under § 314(a). *General Plastic Industrial Co., Ltd. v. Canon Kabushiki Kaisha*, IPR2016-01357, Paper 19 at 15-19 (PTAB Sept. 6, 2017) (precedential). Here, these factors weigh heavily in favor of institution.

There is one prior PTAB challenge to the ’330 Patent—*Lenovo et al., v. Theta IP, LLC*, IPR2023-00694. With respect to the first five *General Plastic* factors, it weighs against a discretionary denial that Apple is not a party to any prior IPR, that this is Apple’s first IPR challenge to the ’330 Patent, and that Apple did not coordinate with *Lenovo et al.*, in any way. See *Unified Patents, Inc. v. Certified Measurement, LLC*, IPR2018-00548, Paper 7, 7-8 (PTAB Sept. 5, 2018) (finding

that it “weighs especially heavily against a discretionary denial” when the Petitioner is not a party to any prior proceeding, and it is Petitioner’s first challenge to the challenged Patent); *see also Foursquare Labs, Inc. v. Mimzi LLC*, IPR2019-01287, Paper 11 (PTAB Jan. 14, 2020) (petitioners individually sued with no evidence of coordination weighed against denying institution); *see Alcatel-Lucent USA Inc. v. Oyster Optics, LLC*, Case IPR2017-02146, slip op. at 12 (PTAB Feb. 28, 2018) (Paper 12) (“Once resolution of factor 1 indicates that Petitioner had not previously filed a petition against the same patent, factors 2– 5 bear little relevance[.]”).

Relevant to factor (3), the Board in *General Plastic* discussed the “potential for abuse” due to “[m]ultiple, staggered petitions challenging the same patent and same claims[.]” *Gen. Plastic*, IPR2016-01357, Paper 19 at 17. The Board explained, “[t]he absence of any restrictions on follow-on petitions would allow petitioners the opportunity to strategically stage their prior art and arguments in multiple petitions, using our decisions as a roadmap, until a ground is found that results in the grant of review.” *Id.* Apple is not using the earlier proceedings as a “roadmap” here. Apple employs entirely different art, different arguments and a different expert. Apple makes no use of the art, argument, responses, or holdings in the *Lenovo* IPR to “refine” failed arguments there. *See Toshiba Am. Info. Sys., Inc. v. Wallelex Microelectronics Ltd.*, IPR2018-01538, Paper 11, at 20-21 (PTAB Mar. 5, 2019) (“apply[ing] different prior art ... based on different arguments, made by different a

petitioner,” does not amount to “a roadmap in a manner unfair to Patent Owner.”); *see Google LLC v. Realtime Adaptive Streaming, LLC*, IPR2019-01036, Paper 9 at 10-12 (PTAB Nov. 13, 2019) (finding Factor Three is “neutral or slightly favors institution” when prior IPR was instituted, there was no “readily apparent ‘unfair benefit’ obtained through use of [the] Institution Decision” from the prior IPR).

As to the sixth factor, the instant petition respects the finite resources of the Board. The Petition presents non-cumulative Grounds with new art. In IPR2023-00694, *Lenovo et al.*, presented four grounds of unpatentability under 35 U.S.C. § 103(a). *Lenovo* relied on several combinations of prior art including *Cummins*, *Rauhala*, *Meador*, *Furuno*, and *Saito*. None of the references used by *Lenovo* are relied upon in this instant challenge. Petitioner presents a single ground of unpatentability of the Challenged Claims in view of new art. Petitioner’s combination is fundamentally different than the grounds raised in IPR2023-00694, presenting non-cumulative art with fundamentally different disclosures.

Regarding the seventh factor, there is no readily identifiable roadblock for the Board to issue a final determination within the statutory one-year limit.

Accordingly, the Board should reach the merits of this petition, and institute review of all Challenged Claims.

B. The *Fintiv* Factors Favor Institution

Under the “*Fintiv* factors,” the Board may consider parallel litigation, including an early trial date, in determining whether to institute under 35 U.S.C. § 314(a). *NHK Spring Co., Ltd., v. Intri-Plex Technologies, Inc.*, IPR2018-00752, Paper 8 at 19–20 (PTAB Sept. 12, 2018) (precedential); *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 at 2–3, 6 (PTAB Mar. 20, 2020) (precedential). Per the Interim *Fintiv* Guidance (“*Fintiv Memo*”),¹² “the PTAB will not discretionarily deny institution of an IPR” where a petitioner proffers a *Sotera* stipulation. *Fintiv Memo*, 7. Petitioner stipulates that, if the instant IPR is instituted, it will not pursue invalidity grounds against the Challenged Claims in the parallel district court proceeding that were brought in the petition or that could have reasonably been raised in the petition. Accordingly, the Board should not discretionarily deny institution under *Fintiv*.

VIII. CONCLUSION

For the forgoing reasons, Petitioner respectfully requests *inter partes* review of the Challenged Claims.

Respectfully submitted,

By: /s/ Paul R. Hart

Paul R. Hart, Reg. No. 59,646

COUNSEL FOR PETITIONER

¹²https://www.uspto.gov/sites/default/files/documents/interim_proc_discretionary_denials_aia_parallel_district_court_litigation_memo_20220621_.pdf.

IX. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8

A. Real Parties-in-Interest Under 37 C.F.R. § 42.8(b)(1)

Petitioner is the real party-in-interest.

B. Related Matters Under 37 C.F.R. § 42.8(b)(2)

The '330 Patent is presently the subject of a patent infringement lawsuit filed against Petitioner in the United States District Court for the Western District of Texas, Waco Division: *Theta IP, LLC v. Apple Inc.*, Case No. 6:23-cv-00314. The '330 Patent has also been at issue in the following matters:

- *Lenovo Inc. et al v. Theta IP, LLC*, IPR2023-00694, denied institution.
- *Theta IP, LLC v. Motorola Mobility LLC et al.*, 1-22-cv-03441 (NDIL).
- *Theta IP, LLC v. Samsung Electronics Co., Ltd. et al.*, 2-16-cv-00527 (EDTX), dismissed.

Family members of the '330 Patent have also been challenged in the following PTAB proceedings:

- U.S. Patent No. 10,129,825 challenged in *Lenovo et al., v. Theta IP, LLC*, IPR2023-00697, instituted.
- U.S. Patent No. 10,524,202 challenged in *Lenovo et al., v. Theta IP, LLC*, IPR2023-00698, instituted.

C. Lead and Back-Up Counsel Under 37 C.F.R. § 42.8(b)(3)

Petitioner provides the following designation and service information for lead and back-up counsel. 37 C.F.R. § 42.8(b)(3) and (b)(4).

Lead Counsel	Back-Up Counsel
Paul R. Hart, (Reg. No. 59,646) Paul.Hart@eriseip.com <u>Postal and Hand-Delivery Address:</u> ERISE IP, P.A. 717 17 th St., Suite 1400 Denver, Colorado 80202 Telephone: (913) 777-5600 Fax: (913) 777-5601	Adam P. Seitz (Reg. No. 52,206) Adam.Seitz@eriseip.com <u>Postal and Hand-Delivery Address:</u> ERISE IP, P.A. 7015 College Blvd., Suite 700 Overland Park, Kansas 66211 Telephone: (913) 777-5600 Fax: (913) 777-5601

APPENDIX OF EXHIBITS

Exhibit 1001	U.S. Patent No. 7,010,330 (the “’330 Patent”)
Exhibit 1002	File History for U.S. Patent 7,010,330 (the “’330 File History”)
Exhibit 1003	Asad Abidi Declaration (“Dec.”)
Exhibit 1004	Farbod Behbahani et al., <i>Adaptive Analog IF Signal Processor for a Wide-Band CMOS Wireless Receiver</i> , 36 IEEE Journal of Solid-State Circuits 1205, (Aug. 2001) (“ <i>Behbahani</i> ”)
Exhibit 1005	Farbod Behbahani et al., <i>A 2.4-GHz Low-IF Receiver for Wideband WLAN in 0.6μm CMOS – Architecture and Front-End</i> , 35 IEEE Journal of Solid-State Circuits 1908, (Dec. 2000) (“ <i>Leete</i> ”)
Exhibit 1006	Farbod Behbahani et al., <i>A Broad-Band Tunable CMOS Channel-Select Filter for a Low-IF Wireless Receiver</i> , 35 IEEE Journal of Solid-State Circuits 476, (April 2000) (“ <i>Tan</i> ”)
Exhibit 1007	Theta IP, LLC’s Response Claim Construction Br., Dec. 08, 2023 (<i>Theta Markman Br.</i>)
Exhibit 1008	Joint Claim Construction Statement, Jan. 18, 2024 (<i>Joint Markman Statement</i>)
Exhibit 1009	Theta IP, LLC’s Sur-Reply Claim Construction Br., Jan. 16, 2024 (<i>Theta Markman Br. Sur-Reply</i>)
Exhibit 1010	June A. Munford Declaration (“ <i>Munford Dec.</i> ”)
Exhibit 1011	Y. Tsividis et al., <i>Internally Varying Analog Circuits Minimize Power Dissipation</i> , IEEE Circuits & Devices Magazine, Jan. 2003.
Exhibit 1012	Mihai Banu & Yannis Tsividis, <i>Fully Integrated Active RC Filters in Technology</i> , 18 IEEE Journal of Solid-State Circuits 644, (Dec. 1983) (“ <i>Fully Integrated</i> ”)
Exhibit 1013	Farbod Behbahani et. al, <i>An Adaptive 2.4GHz Low-IF Receiver in 0.6μm CMOS for Wideband Wireless LAN</i> , IEEE International Solid-State Circuits Conference, 2000 (“ <i>Kishigami</i> ”).
Exhibit 1014	U.S. Patent No. 6,335,952 to Lee et al. (“ <i>Lee</i> ”)
Exhibit 1015	Reinhold Ludwig & Pavel Bretchko, <i>RF Circuit Design, Theory and Applications</i> , (2000) (“ <i>Ludwig</i> ”)
Exhibit 1016	A. Dao, <i>Integrated LNA and Mixer Basics</i> , Texas Instruments, National Semiconductor, App. Note 884 (April 1993) (“ <i>Texas</i> ”)
Exhibit 1017	U.S. Patent No. 6,498,927 to Kang et al. (“ <i>Kang</i> ”)
Exhibit 1018	U.S. Patent No. 6,366,622 to Brown et al. (“ <i>Brown</i> ”)
Exhibit 1019	Rex Miller & Mark R. Miller, <i>Barron’s Electronics The Easy Way</i> (4 th ed.) (2002) (“ <i>Barron</i> ”)
Exhibit 1020	<i>Intentionally left blank</i>

Exhibit 1021	Thomas Byunghak Cho & Paul R. Gray, <i>A 10 b, 20 Msample/s, 35 mW Pipeline A/D Converter</i> , IEEE Journal Of Solid-State Circuits Conference 166 (Mar. 1995) (“ <i>Cho</i> ”)
Exhibit 1022	<i>Intentionally left blank</i>
Exhibit 1023	Roubik Gregorian & Gabor C. Temes, <i>Analog MOS Integrated Circuits for Signal Processing</i> (Robert A. Johnson & George Szentirmai eds., 1986) (“ <i>Gregorian</i> ”)
Exhibit 1024	John Pritiskutch & Brett Hanson, <i>UNDERSTANDING LDMOS DEVICE FUNDAMENTALS</i> , AN1226 App. Note (July 2000) (“ <i>STMicroelectronics</i> ”)
Exhibit 1025	U.S. Patent No. 6,353,640 to Hessel et al. (“ <i>Hessel</i> ”)
Exhibit 1026	John G. Proakis & Masoud Salehi, <i>Communications Systems Engineering</i> , (1994) (“ <i>Proakis</i> ”)
Exhibit 1027	S. Khorram et. al, <i>A CMOS Limiting Amplifier and Signal-Strength Indicator</i> , 1995 Symposium on VSLI Circuits Digest of Technical Papers, (1995) (“ <i>Khorram</i> ”)

CERTIFICATION OF WORD COUNT

The undersigned certifies pursuant to 37 C.F.R. §42.24 that the foregoing Petition for *Inter Partes* Review, excluding any table of contents, mandatory notices under 37 C.F.R. §42.8, certificates of service or word count, or appendix of exhibits, contains 13,957 words according to the word-processing program used to prepare this document (Microsoft Word).

Dated: May 1, 2024

Respectfully submitted,

By: /s/ Paul R. Hart
Paul R. Hart, Reg. No. 59,646

COUNSEL FOR PETITIONER

CERTIFICATE OF SERVICE ON PATENT OWNER
UNDER 37 C.F.R. § 42.105(a)

Pursuant to 37 C.F.R. §§ 42.6(e) and 42.105(b), the undersigned certifies that on May 1, 2024, a complete and entire copy of this Petition for *Inter Partes* Review and Exhibits were provided via Priority Mail Express to the Patent Owner by serving the correspondence address of record for the '330 patent:

WOMBLE BOND DICKINSON (US) LLP
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ATLANTA, GA 30357-0037
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A complete and entire copy of this Petition for *Inter Partes* Review and Exhibits were also emailed to counsel of record in the parallel litigation:

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Respectfully submitted,

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