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Application Number	
Filing Date	
First Named Inventor	Yannis Tsividis
Title	Power Dissipation Reduction in Wireless Transceivers
Art Unit	
Examiner Name	
Attorney Docket Number	10037P007CC2

SIGNATURE of Applicant or Patent Practitioner

Signature	/RWB/	Date (Optional)	3/24/2016
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DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION (37 CFR 1.63)		
☒ Declaration Submitted with Initial Filing **OR** ☐ Declaration Submitted after Initial Filing (surcharge (37 CFR 1.16(f)) required)	**Attorney Docket Number**	10037P007CC2
	First Named Inventor	Yannis Tsividis
	COMPLETE IF KNOWN	
	Application Number	
	Filing Date	
	Art Unit	
	Examiner Name	

Power Dissipation Reduction in Wireless Transceivers

(Title of the Invention)

As a below named inventor, I hereby declare that:

This declaration is directed to:

☒ The attached application,

OR

☐ United States Application Number or PCT International Application Number _____

filed on _____

The above-identified application was made or authorized to be made by me.

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POWER DISSIPATION REDUCTION IN WIRELESS TRANSCEIVERS

CROSS-REFERENCES TO RELATED APPLICATIONS

[0001] This application is a continuation of U.S. Patent Application No. 11/318,646, filed December 27, 2005, which is a continuation of U.S. Patent Application Number 10/784,613, filed February 23, 2004, which claims the benefit of United States provisional application number 60/451,229, filed March 1, 2003, which is incorporated by reference.

[0002] This application claims the benefit of United States provisional application number 60/451,230, filed March 1, 2003, which is incorporated by reference.

BACKGROUND

[0003] The present invention relates to power dissipation reduction techniques for electronic circuits, for example wireless transceiver integrated circuits.

[0004] Wireless networking is quickly becoming ubiquitous, as desktop, notebook, and handheld computers are connected to share Internet access and files. Wireless networking cards compatible with PCMCIA and compact flash form factors are popular for laptops and handhelds respectively, particularly as mobile users connect to the Internet on the road at coffee shops, hotels, and airports.

[0005] A downside of this connectivity is a corresponding drain on battery life, especially for these portable devices. The power consumed by a wireless transmitter and receiver reduces the usefulness of a device and sends a user on a hunt for an electrical outlet for recharging.

[0006] One reason why this power drain is high is that electronic circuits are typically designed to function properly under worst-case operating conditions. For a wireless transceiver, the worst case condition is when a desired signal reception strength is low, while other transceivers or nearby electronic equipment generate interfering signals and other spurious noise.

[0007] But a wireless transceiver does not always operate in these worst-case conditions. For example, a base station, router or access point may be nearby such that the received signal is strong. Also, there may be no interfering signals, or they may be relatively weak. In these situations, receiver circuit currents can be reduced below what is necessary for the worst case condition. If this is done, power dissipation is reduced, and battery life is increased.

[0008] Thus, what is needed are circuits and methods that can adapt to a better-than-worst-case condition and reduce circuit currents and therefore power dissipation accordingly.

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SUMMARY

[0009] Accordingly, embodiments of the present invention provide methods and circuits for reducing power dissipation in wireless transceivers and other electronic circuits and systems. Embodiments of the present invention use bias current reduction, impedance scaling, gain, and other dynamic changes either separately or in combination to reduce power dissipation in response to better-than-worst case conditions. For example, bias currents are reduced in response to a need for reduced signal handling capability, impedances are scaled thus reducing required drive and other bias currents in response to a strong received signal, or gain is varied and impedances are scaled in response to a low received signal in the presence of no or weak interfering signals. Alternately, currents may start low and be increased in response to worse-than-best-case conditions, or they may start at a point in between and vary up or down. These variations may be made to electronic systems generally, and are particularly suited and discussed below in the context of a wireless transceiver that may be used in networking devices, cellular telephones, and other wireless systems.

[0010] An exemplary embodiment of the present invention provides a method of receiving a signal using an integrated circuit. The integrated circuit includes a signal path having a low-noise amplifier configured to receive the signal, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer. The method itself includes determining a first signal strength at a first node in the signal path in the integrated circuit and dynamically changing an impedance of a component in the signal path based on the first signal strength.

[0011] A further exemplary embodiment of the present invention provides a method of receiving a signal using an integrated circuit. The integrated circuit includes a signal path having a low-noise amplifier configured to receive the signal, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer. The method itself includes determining a first signal strength at a first node in the signal path in the integrated circuit and dynamically changing a bias current in the signal path based on the first signal strength.

[0012] Another exemplary embodiment of the present invention provides a method of receiving a signal using an integrated circuit. The integrated circuit includes a signal path having

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a first circuit and a second circuit having an input coupled to an output of the first circuit. The method itself includes determining a first signal strength at a first node in the signal path in the integrated circuit. The first node is before the first circuit in the signal path. The method further includes dynamically changing a gain of the first circuit based on the first signal strength and dynamically changing an impedance of a component in the second circuit based on the first signal strength.

[0013] Still a further exemplary embodiment of the present invention provides a wireless transceiver integrated circuit including a receiver having a signal path, the signal path including a low-noise amplifier, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer, as well as a first signal strength indicator circuit coupled to the signal path and configured to determine a first signal strength. An impedance in the signal path is configured to be dynamically adjusted in response to the first signal strength.

[0014] Yet a further exemplary embodiment of the present invention provides a wireless transceiver integrated circuit. This integrated circuit includes a receiver comprising a signal path, the signal path having a low-noise amplifier, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer, as well as a first signal strength indicator circuit coupled to the signal path, and configured to determine a first signal strength. A bias current in the signal path is configured to be dynamically adjusted in response to the first signal strength.

[0015] Another exemplary embodiment of the present invention provides a wireless transceiver integrated circuit. This circuit includes a receiver comprising a signal path, the signal path having a first circuit; and a second circuit having an input coupled to an output of the first circuit; as well as a first signal strength indicator circuit coupled to the signal path, and configured to determine a first signal strength. A gain of the first circuit is configured to be dynamically adjusted in response to the first signal strength, and an impedance in the second circuit is configured to be dynamically adjusted in response to the first signal strength.

[0016] A better understanding of the nature and advantages of the present invention may be gained with reference to the following detailed description and the accompanying drawings.

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BRIEF DESCRIPTION OF THE DRAWINGS

[0017] Figure 1 is a block diagram of a wireless transceiver that may benefit by incorporation of embodiments of the present invention;

[0018] Figures 2A and 2B illustrate examples of desired and interfering signals and noise that may be received by a circuit in a wireless receiver;

[0019] Figure 3 illustrates what can occur as a maximum signal handling capability is reduced in the worst-case signal condition;

[0020] Figure 4 illustrates a portion of a receiver consistent with an embodiment of the present invention;

[0021] Figure 5 illustrates the relationship between a required bias current and a given output signal for a representative circuit;

[0022] Figure 6 is an example of how a circuit's impedances may be scaled to reduce drive currents, and depending on the circuit configuration used, to reduce associated bias currents as well;

[0023] Figure 7 illustrates how gain may be inserted in a signal path to improve a circuit's signal to noise ratio;

[0024] Figures 8A-8D illustrate some of the possible power saving techniques that may be used when received desired and interferer signals are all at a low power level;

[0025] Figures 9A-9C illustrate one of the possible power saving techniques that may be used when a received desired signal is strong while all interfering signals are at a low power level;

[0026] Figures 10A-10C illustrate one of the possible power saving techniques that may be used when received desired and interferer signals are all at a high power level;

[0027] Figures 11A-11D illustrate one of the possible power saving techniques that may be used when a received desired signal is weak while one or more interfering signals are strong;

[0028] Figure 12 is a summary illustrating four different input conditions and some of the appropriate power-saving changes that may be made in response to those conditions;

[0029] Figure 13 shows how power may be saved as a function of time by employing one or more of the power saving methods consistent with embodiments of the present invention;

[0030] Figure 14 is a block diagram of a portion of a receiver consistent with an embodiment of the present invention; and

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[0031] Figure 15 is a block diagram of a portion of a transmitter consistent with an embodiment of the present invention.

DESCRIPTION OF EXEMPLARY EMBODIMENTS

[0032] Figure 1 is a block diagram of a wireless transceiver that may benefit by incorporation of embodiments of the present invention. This wireless transceiver may be designed to send and receive signals consistent with the IEEE 802.11a, 802.11b, 802.11g, or other signaling standard or combination of standards. This figure, as with all the included figures, is shown for illustrative purposes only and does not to limit either the possible embodiments of the present invention or the claims.

[0033] There are three main portions of this transceiver circuit, a receiver, transmitter, and synthesizer. This transceiver may be completely or partially integrated on a semiconductor chip, or it may be integrated onto multiple integrated circuits. In a specific embodiment, the circuitry bounded by dashed line 100 is integrated on a single chip coupled to one or more external components or circuits. The integrated circuit or circuits forming this wireless transceiver may incorporate various integrated circuit devices such as a bipolar, CMOS, or BiCMOS devices made using a silicon, silicon-germanium (SiGe), gallium arsenide or other III-V process, or other manufacturing process. Embodiments of the present invention may also be applicable to circuits manufactured using nanotechnology processing.

[0034] The receiver includes a signal path formed by low-noise amplifier 102, I and Q mixers 104 and 106, low pass filters 108 and 110, and baseband amplifiers 114 and 116. Other circuitry in the receiver includes received strength indicator 122, automatic gain control circuit 166, baseband gain control circuit 120, tuning circuit 112, and offset cancellation circuit 118.

[0035] The transmitter includes input up-converter mixers 124 and 126, summing node 176, which may be conceptual rather than an actual circuit, transmit variable gain amplifier 128, and power amplifier 130.

[0036] The synthesizer includes a voltage-controlled oscillator 148, which drives I and Q buffers 154 and 152, prescaler 156, reference clock buffer 142 and divider 158, phase-frequency detector 160, charge pump 162, and loop filter 146, which in a specific embodiment is formed by external components.

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[0037] Signals are received on an antenna, not shown, and typically pass through an RF switch and bandpass filter before being received by the low-noise amplifier 102 on line 101. The low noise amplifier gains the received signal and provides it to quadrature mixers 104 and 106. I and Q mixers 104 and 106 down-convert the received signal to baseband by multiplying them with quadrature versions of the oscillator signal provided by buffers 152 and 154. This down conversion also produces a high frequency component at a frequency that is equal to the sum of the frequencies of the received signal and the VCO. This unwanted signal is filtered by low pass filters 108 and 110, which in turn drive baseband amplifiers 114 and 116. The outputs of baseband amplifiers 114 and 116 are typically converted to digital signals by analog-to-digital converters at the front end of a digital signal processing block.

[0038] In the transmit mode, I and Q versions of the signal to be transmitted are provided on lines 121 and 123 to up-convert mixers 124 and 126. These up-convert mixers multiply the I and Q portions of the transmit signal by quadrature versions of the VCO signal provided by buffers 152 and 154. The outputs of the up-convert mixers 124 and 126 are summed, and amplified by transmit VGA 128, which in turn drives power amplifier 130. The output of power amplifier 130 is typically filtered, and passes through the RF switch to the antenna for transmission.

[0039] A reference clock is received and buffered by the reference buffer 142. The VCO generates quadrature oscillatory signals that are divided by prescaler 156. The reference clock is typically generated by a crystal or other stable periodic clock source. The phase-frequency detector 116 compares the phase or frequency (depending on whether the synthesizer is tracking or acquiring the correct frequency) of the divided VCO signal and the reference clock, or a divided version of the reference clock, and generates an error signal, which drives the charge pump 162. The output signal of the charge pump 162 is filtered by the loop filter 146, which is commonly a lead-lag filter, and which provides a tuning or correction signal to the VCO 148.

[0040] Embodiments of the present invention may be used to reduce the power dissipation of one or more of these included circuits. For example, the power dissipation in the low-noise amplifier 102, down-convert mixers 104 and 106, low pass filters 108 and 110, or baseband amplifiers 114 and 116 may be optimized. Also, power dissipation in up-convert mixers 124 126, variable gain amplifier 128, and power amplifier 130 may also be optimized. Similarly, VCO 148 and prescaler 156 currents may be adjusted. Embodiments of the present invention

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may also be applied in other circuits which may be included in other integrated circuit receivers, transmitters, transceivers, or other electronic circuits or systems.

[0041] When a receiver is actively receiving a desired signal, each block in the signal path has at its input the desired signal as well as noise and possibly interfering signals. The desired signal is the useful, information-carrying portion of a received signal. The noise may be thermal, shot, or other noise generated on the integrated circuit, in addition to received noise generated by sources external to the chip. The noise at the input of a block may be referred to as the equivalent input noise. The interfering signal or signals, or interferers, may be generated by similar transceivers, or other electrical equipment, circuits, or systems.

[0042] Figures 2A and 2B illustrate examples of desired signals, interferers, and noise that may be received by one of the various circuits in a wireless receiver. In each of these figures, the signal strength is plotted along a Y-axis 204 or 254 as a function of frequency along an X-axis 202 or 252. In the example of Figure 2A, a received desired signal 206 is large in comparison to interfering signals 208 and 210. In these examples, two interfering signals are shown for illustrative purposes, though there may be no such signals, one such signal, or more than two such signals in the frequency range of interest. Also, while for these examples the interferers are shown as being at a higher frequency than the desired signal, there may be one or more interferers at higher or lower frequencies as the desired signal. In this specific example, the acceptable noise floor 214 is relatively high, while maximum signal handling capability Smax 212 (that is the maximum signal power that can be handled with an acceptably low distortion) needs only to be high enough to accommodate the desired signal. For this specific example, the circuit receiving this input spectrum only requires a relatively small dynamic range for proper operation, that is the range between Smax 212 and the noise floor 214 is relatively small.

[0043] Conversely, in the example shown in Figure 2B, the desired signal 256 is relatively weak compared to the large interferers 258 and 260. In this example, the noise floor 264 should be relatively low so as to prevent an unacceptable level of error in the recovery the desired signal 256. The maximum signal handling capability Smax 262 should be relatively high to accommodate the large interferers in order to avoid the creation of intermodulation products as described below. Accordingly, in this specific example, the circuit receiving this input spectrum should have a large dynamic range, particularly in comparison to the example of Figure 2A.

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[0044] It should be noted that the noise level or noise floors shown in these and the other included figures is the noise density integrated over the bandwidth of interest. For simplicity and comparison, this level is shown as a horizontal line, and is not meant to imply noise density.

[0045] Often in wireless receivers, a circuit at different times will receive an input spectrum similar to those shown in Figures 2A and 2B. The input spectrum of Figure 2B is generally considered the worst-case input signal, and typical design methodology involves designing a receiver for this condition, specifically the weakest desired signal accompanied by largest interference level. Circuit impedances and currents are set such that the noise floor 264 is sufficiently low for an acceptable bit-error rate, while bias currents are set sufficiently high for the required Smax 262.

[0046] Conversely, the input spectrum in Figure 2A is that of the best-case input signal, specifically, a robust desired signal accompanied by no or low-level interferers. In this case, the noise floor 214 may be allowed to rise, while the maximum signal handling capability Smax 212 may be reduced. When this is done, the receiver circuit may save significant power. For example, the circuit's impedances may be increased, thus reducing required drive currents. Similarly, bias currents may be lowered, thus reducing the maximum signal in handling capability.

[0047] The minimum power dissipation for a circuit is proportional to the required maximum signal-to-noise ratio, which is the ratio between Smax 212 or 262 and N 214 and 264. Thus, a circuit receiving an input similar to the one shown in Figure 2A can dissipate less power than one receiving the input as shown in Figure 2B, while still achieving an acceptable bit-error rate.

[0048] Figure 3 illustrates what can occur when the maximum signal handling capability Smax 314 is reduced in the worst-case condition, that is when a weak desired signal 306 is accompanied by large interferers 310 and 312. Again, signal strength is plotted along a Y-axis 304 as a function of frequency along X-axis 302. In this specific example, Smax 314 is reduced below the peak levels of the interferers 310 and 312. Since Smax is low, the circuit cannot handle the interferers linearly. The resulting nonlinearities lead to a mixing of the interferers and the creation of intermodulation products 308 (for example, a third-order intermodulation distortion, IM3), one of which in this example occurs at the same frequency as the desired signal 306. As can be seen, if the intermodulation products 308 become excessive, the received signal bit error rate may become excessive, and the desired signal 306 may be lost. Accordingly, while

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Smax may be lowered even under some unfavorable conditions in order to reduce power, care should be taken to avoid corruption of the received desired signal.

[0049] Figure 4 illustrates a portion of a receiver consistent with an embodiment of the present invention. Included is a filter 430. An optional gain element 420 is placed in front of the filter 430 in order to increase signal levels. Signal strength indicator circuits 440 and 450 are connected to input line 410 and output line 460. In this specific example, the input signal spectrum on line 410 is shown as desired signal 412 and interferers 414 and 416. The signal spectrum at the output line 460 is shown as desired signal 462 and interferers 464 and 466. The signal strength indicators 440 and 450 do not provide information as to the relative sizes of the desired and interfering signals. Rather, a cumulative signal level is provided at their outputs. For example, the first signal strength indicator 440 outputs a level corresponding to the sum of desired signal 412 and interfering signals 414 and 416, while the second signal strength indicator 450 provides a signal level corresponding to the sum of desired signal 462 and interfering signals 464 and 466. In this specific example, the gain of the gain and filter circuit combinations is shown as approximately one, while the interfering signals 414 and 416 signal levels are reduced.

[0050] A comparison of the signal levels provided by the signal strength indicators 440 and 450 indicates that much of the combined received signal on line 410 has been filtered. Accordingly, it may be deduced that large interfering signals present at the input are being filtered by the filter 430. From this information, as will be shown in greater detail below, the bias, impedance, and gain of the gain stage 420 and filter 430 combination may be optimized to reduce power dissipation.

[0051] There are several real world situations where the received signal is better than the worst-case condition such that power can be saved. For example, large interferers may be present only part of the time, that is, on a temporary or transient basis. The interfering equipment may be some distance from the transceiver, or it may be operating in the low power mode. Also, the desired signal may be very strong as compared to the noise and interferers, for example a hub, router, or access point may be nearby.

[0052] Some transceivers consistent with embodiments of the present invention are designed to work with more than one data transfer specification or standard. In this case, when a transceiver is operating in a mode having a lower data rate, the power saving techniques described here may be employed.

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[0053] Figure 5 illustrates the relationship between a required biased current 516 for a given output signal 514 for a representative circuit 510. If the output signal current level is relatively low, such as the output current shown as 526, the corresponding bias current 528 may be low. Conversely, if the output signal current level is larger as with the example 536, the corresponding bias current level 538 should also be high. Accordingly, if a bias current is initially set high to handle large a large input signal, for example a large interferer, this current may be reduced if the input signal is smaller.

[0054] There are many ways by which these bias currents can be reduced. For example, the current may be generated by placing a voltage across a resistor by applying a bias voltage to the base of a device whose emitter is connected to ground through a resistance. In this case, the resistor may be increased by opening switches across portions of the resistance, or lowering the bias voltage applied at the base. Several ways in which this may be done will be readily understood by one skilled in the art.

[0055] Figure 6 is an example of how a circuit's impedances may be scaled to reduce drive currents, and, depending on the circuit configuration used, associated bias currents as well. A driver 612 has a load R 614 and C 616. The frequency response of this circuit is the same as that seen by driver 622, which drives an impedance of 2R 624 and C/2 626. But the impedance of the load seen by driver 622 is double that seen by 612, thus the output current required by the driver 622 is reduced by one-half.

[0056] As an example, the output stage of each of these drivers may be a Class A emitter follower formed by an emitter follower connected to a current source. When the outputs are driven high, the emitter of driver 622 need supply only one-half the drive current as driver 612. In this way, an impedance can be scaled in order to decrease a circuit's required drive current.

[0057] Also, the discharge current for driver 622 is only one half that of driver 612 for a given negative-going slew rate. Thus, the current source of 622 may be reduced by the same factor of one-half as compared to driver 612. In this example, the bias current, that is the current in the pull-down current source can be reduced. Many other examples where drive currents and possibly bias currents may be reduced will be appreciated by one skilled in the art.

[0058] Figure 7 illustrates another degree of freedom that made be employed to reduce current levels in a transceiver. Specifically, a gain element 720 may be inserted in front of a circuit block 730 in order to improve the combined circuit's signal-to-noise ratio by a factor equal to the

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gain of the inserted gain block. This is particularly useful when large interferers are absent and the desired received signal is moderate or low. Specifically, gain is added to the signal while impedances are increased, which raise the noise floor. In this way, a given signal-to-noise ratio may be maintained while the power is decreased.

[0059] The gain of such an element may be varied by increasing a current in a differential pair or increasing a load resistance using switches. Many other examples where the gain of this element may be varied will be appreciated by one skilled in the art.

[0060] These variables, or degrees of freedom, specifically reducing bias currents, increasing impedances, and increasing gain may be used as in the following examples.

[0061] Figure 8A is a block diagram of a functional block 820 and optional gain element 810 in accordance with an embodiment of the present invention. Functional block 820, like the functional blocks in the following diagrams, may be a filter, mixer, amplifier, or other circuit or circuits in a wireless transceiver or other electronic circuits or system. An input signal is received on line 812 by the optional gain element 814. When the optional gain block 810 is not used, the input signal may be received directly by the function block 820. The gain of the optional gain element 812 is controlled by a gain control signal on line 814. The functional block receives an output signal from the optional gain element 810 and provides an output VOUT on line 822. The lines in this and the other included figures may be one or more lines, depending on whether single-ended, differential, or other type of signaling is employed.

[0062] One or more impedances are under control of signals on impedance control lines 824. Similarly, one or more bias currents in the function block are under control of one or more signals on bias control lines 826. These various control lines may be logic signals, analog signals, voltage or currents lines, or other signal or bias lines. In other embodiments of the present invention, the gain control element 810 may be included in the function block 820. Also, various embodiments may not incorporate either or both the impedance control and bias control.

[0063] Figure 8B is an example input that may be present on line VIN 812. In this example, a desired signal 836 is relatively weak, as are interfering signals 837 and 838. The initial bias and circuit configuration is such that the noise floor 833 and maximum signal handling capability Smax 831 are adjusted for worst case conditions. The circuit of Figure 8A, as with all the circuits described here, receives noise at its input which may be referred to as input equivalent noise or input referred noise. Additionally, the circuit of Figure 8A generates noise which is

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added to the input referred noise. Depending on the gain characteristics of the circuitry, the output noise at various frequencies may be greater than, equal to, or less than the input referred noise. For simplicity, the noise floor and maximum signal handling capability Smax, in this and the other figures, are shown as straight lines, though the noise and Smax are typically curved as a function of frequency.

[0064] That the input spectrum is as shown in Figure 8B can be determined, for example, by low signal strength indications on line VIN 812 and VOUT 822. That is, a low level signal strength indication on line VIN 812 indicates that no portion of the input signal is particularly large.

[0065] For this exemplary input, there are at least two methods by which the power dissipation for this circuitry may be reduced. Depending on the exact circuits and structures used, one of these methods may be preferred.

[0066] In Figure 8C, the bias current is decreased, thereby lowering the maximum signal handling capability 841 as compared to 831, closer to the desired and interfering signal levels. Again, the bias currents in the function block 820 may be reduced by switching impedances that appear across a voltage thereby changing a resulting bias current, by reducing a voltage at the gate of a MOS or base of a bipolar transistor, or by other methods.

[0067] In Figure 8D, a second method of reducing power dissipation in the function block 820 is employed. Specifically, Smax 851 is held constant as compared Smax 831. The desired and interfering signals are amplified such that they are closer to the available signaling handling capability 851. Also, the noise floor 853 is raised as compared to noise floor 833 in Figure 8B. Specifically, the noise contributed by the function block 820 is increased, such that the noise at its output is increased to noise floor 853. This is done by increasing one or more impedance in function block 810, such that drive currents inside that block are reduced. Depending on the exact configuration, this may also allow some biasing currents to be reduced, while maintaining the maximum signal handling capability 851 at a sufficient level. Alternately, these two methods of reducing power dissipation in function block 820 may be done in combination.

[0068] The included examples are explained for the exemplary situation where biasing and other parameters are set for worst-case conditions, and then changed to save power when it is discovered that the conditions are better-than-worst case. Alternately, the bias currents and other

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parameters may be set for maximum power savings, or an intermediate point, and the power can be adjusted from there.

[0069] Figure 9A illustrates a block diagram including an optional gain element 910 and function block 920. Again, an input signal is received on line 912 by optional gain element 910 which in turn drives function block 920. The function block provides an output VOUT on line 922, and receives impedance and bias control signals on lines 924 and 926.

[0070] Figure 9B shows the spectrum for what may be considered a best-case received signal. Specifically, the desired signal 936 is strong, while the interfering signals 937 and 938 are relatively weak. This may be determined, for example, by detecting a large signal level at the input line VIN 812 and a large signal level after a filter, since these readings would indicate that a large signal is received, but that it is at the desired signal frequency.

[0071] The maximum signaling capability 931 and noise floor 933 are shown as being set for the worst case conditions. In this case, the noise floor 933 is lower than the maximum allowed for proper signal reception. Accordingly, one or more impedance in the function block 920 may be increased, such that the noise floor 943 rises as shown in Figure 9C. In this way one or more the driving currents in the function block 920 may be reduced. Similarly, since the drive current is reduced, one or more bias current may also be reduced, depending on the exact circuit configuration.

[0072] Figure 10A illustrates a block diagram showing an optional gain element 1010 driving a function block 1020. An input signal is received by the gain element 1010 on line 1012, and an output is provided by function block 1020 on line VOUT 1022. One or more gain control signals present on lines 1014 control the gain of gain control element 1010, while one or more impedance and bias control signals are received by the function block 1020 on line to 1024 and 1026.

[0073] Figure 10B illustrates a received signal that may be received on line VIN 1012. In this example, the desired signal 1036 and interferers 1037 and 1038 are each relatively large. This may be determined, for example, by detecting a large signal level at the input line VIN 812 and a smaller signal level after a filter, since these readings would indicate that a large signal is received, but that interferers are being reduced.

[0074] As before, in this example, the noise floor 1033 and maximum signal handling capability 1031 are initially set for the worst case conditions. Since the desired signal is

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relatively large in this case, the noise floor may be allowed to rise, a shown by noise floor 1043 in Figure 10C. Since the desired signal 1046 and interferers 1047 are large, the maximum signal handling capability Smax 1041 remains constant. Again, the noise floor is increased by increasing impedances in the function block 1020. This reduces the required drive current, and may also allow for a reduction in bias currents.

[0075] Figure 11A illustrates a block diagram including an optional gain element 1110 and function block 1120 in accordance with an embodiment of the present convention. An input signal is received on line 1112 by the optional gain control element 1110, while an output signal is provided by the function block 1120 on line VOUT 1122. Gain, impedance, and bias control signals are received on lines 1114, 1124, and 1126.

[0076] Figure 11B is an exemplary input signal that may be received by the gain control element 1110 on line VIN 1112. In this specific example, the desired signal 1136 is relatively low or weak while the interfering signals 1137 and 1138 are large. This may be determined, for example, by detecting a large signal level at the input line VIN 812 and a much smaller signal level after a filter, since these readings would indicate that a large signal is received and that large interferers are being reduced such that the resulting signal, the desired signal, is relatively weak.

[0077] Again, the maximum signal handling capability 1131 and noise floor 1133 are initially set for worst case conditions. If the desired signal is sufficiently low, while the interferers are sufficiently high, power savings may not be achievable over the worst case settings, since this is in fact the worst case condition. But, if the desired signal is somewhat larger than the worst case condition, then power may be saved in at least two different ways.

[0078] For example, Figure 11C shows the maximum signal handling capability 1141 being lowered. In this case, the interfering signals 1147 in 1148 began to clip and distort, thereby creating intermodulation products 1145, which distort the desired signal 1146. So long as care is taken to not corrupt the desired signal 1146 beyond an acceptable limit, typically measured by a bit-error rate, power may be reduced in this way.

[0079] Similarly, in Figure 11D, the noise floor 1153 is raised somewhat, thereby saving power. Again, this may be done so long as the noise floor is not sufficiently high that the system bit-error rate becomes unacceptable.

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[0080] Figure 12 is a summary of the above four examples. The received signal strengths are shown in column 1210, while appropriate power saving responses are listed in column 1220. Specifically, in row 1230, the desired signal and interferer signal strengths are both weak or small. In this case, proper responses include decreasing Smax, or increasing one or more circuit impedances while increasing the circuit gain. Depending on the exact circuit configuration, one of these options may be preferred over the other. Alternately, they may be done in combination, or done in combination with other power saving techniques. Also, in some specific embodiments, when both desired signal and interferer signal strengths are small, the gain may need to be increased while the impedance is maintained or not increased in order to keep the noise floor low.

[0081] In row 1240, the desired signal strength is strong or large, while the interfering signals are small. In this case, an appropriate response is to increase one or more of the circuit impedances. Again, depending on the exact circuit in question, one or more of the bias currents may also be reduced.

[0082] In row 1250, both the desired signals and interfering signal strengths are large. Again, in this case an appropriate response is to increase one or more of the circuit impedances.

[0083] In row 1260, the received desired signal strength is weak or small, while the interfering signals are large. Since this is the worst case situation for which the circuit is designed, substantial power savings are difficult to achieve. However, again, if the received signal is above a minimum level necessary for proper operation, some distortion of the interferers or raising of the noise floor may be acceptable.

[0084] It should be noted that not all possible signal conditions are listed here. For example, either the signal or interferer may be of a relatively medium strength, or the interferer may be absent. Also, these terms are for exemplary purposes and are not meant to convey specific signal conditions, but rather are only qualitative. The proper response to a specific condition depends on the embodiment of the present invention, the particular circuit topology, the requirements of the signaling standard used, as well as other constraints.

[0085] Figure 13 is an example shown how power may be saved as a function of time by employing one or more of these methods consistent with embodiments of the present invention. Power is plotted along a Y-axis 1304 as a function of time along X-axis 1302. Conventional worst case design would fix power dissipation at line 1310. As can be seen, dynamic power

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dissipation 1320 under the control of variable gains, impedances, biasing, or combination thereof, allows for a lower average power 1330 as compared to the power dissipated 1310 by the conventional design.

[0086] Figure 14 is a block diagram of a portion of a receiver consistent with an embodiment of the present invention. Included are low-noise amplifier 1410, mixer 1420, gain stage 1430, filter 1440, AGC amplifier 1450, and VCO 1460. Signal strength detection is done at the output of the low-noise amplifier by signal strength indicator 1470, at the output of the mixer by signal strength indicator 1472, and at the output of the filter by signal strength indicator 1474. The outputs of the signal strength indicator circuits are received by the computational circuit 1470, which in turn controls gain and power control circuits 1480 and 1485. Power and gain control circuits 1480 and 1485 control the gain, biasing, and impedance levels of the circuits in the receiver signal path. Also, the gain and power control circuits may control the same parameters in the VCO 1460. This figure is greatly simplified for purposes of explanation. For example, the quadrature nature of the mixers and following circuits are not shown. Also, power-down and start-up circuits are not included.

[0087] The current level in the low-noise amplifier determines a multitude of parameters including voltage gain, linearity, input impedance matching, and noise figure. When conditions are better than worst-case, some of these parameters may be relaxed while maintaining an acceptable bit-error rate, thus saving power.

[0088] The bias current in the mixers effect that block's noise figure and linearity. Care is taken in reducing power in this block so as not to increase nonlinearities, particularly the third-order nonlinearity as measured by IP3, the third-order intercept point, beyond an acceptable limit.

[0089] A key parameter of the VCO is phase noise, an increase in which increases the sidebands on either side of the oscillation signal. During transmission, the phase noise should be kept low to avoid interference with adjacent channels and for preserving modulation information.

[0090] During reception however, if the conditions are better than worst case, the phase noise requirement for the VCO is relaxed, and power can be saved consistent with embodiments of the present invention. The achievable phase noise power spectral density is approximately inversely proportional to the bias current used. Thus, when low phase noise is not required during reception, bias current in the VCO can be reduced.

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[0091] Most of the power savings in a transceiver in accordance with embodiments of the present invention is achieved in the receiver portion. Additional power may be saved in the transmitter section.

[0092] Figure 15 is a block diagram of a transmitter portion consistent with an embodiment of the present invention. Included is a signal path formed by gain stage 1510 and power amplifier 1520. The output power level is sensed by output level sensing circuit 1550, which in turn adjusts the biasing of the power amplifier 1520 through the power control circuit 1540. Additionally, a transmitter level control signal is received by power control circuits 1530 and 1540, which in turn control the biasing of gain stage 1510 and power amplifier 1520. Gain control circuit 1560 also adjusts the gain of gain stage 1510 and power amplifier 1520. Additional circuitry that varies impedances in each of these circuits may also be included.

[0093] Since the gain, impedance and biasing of these blocks are being dynamically varied, care must be taken to not negatively affect the signal being processed. For example, specific embodiments of the present invention perform some or all of these variations during preamble. Also, as changes occur, the circuits in some embodiments are limited such that they may only adapt to an improvement in conditions after frames are completed. If conditions worsen, the circuits may be allowed to change in order to save the data. Alternately, a system may be manually calibrated, for example at set up, and when the network configuration is changed.

[0094] The above description of specific embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form described, and many modifications and variations are possible in light of the teaching above. The embodiments were chosen and described in order to best explain the principles of the invention and its practical applications to thereby enable others skilled in the art to best utilize the invention in various embodiments and with various modifications as are suited to the particular use contemplated.

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CLAIMS

What is claimed is:

1. A method of power dissipation control in a receiver circuit within a battery powered mobile device when the receiver circuit is receiving and processing an RF input signal that includes a desired signal and an interferer signal, the method comprising:

determining a strength of the desired signal with respect to the strength of the interferer signal;

causing a variable decrease in power dissipation of a signal path within the receiver circuit and a resultant decreased battery drain, by variably scaling a bias current of a component in the receiver circuit upon determination that the strength of the desired signal has increased relative to the strength of the interferer signal;

causing a variable increase in power dissipation of the signal path within the receiver circuit and a resultant increased battery drain, by variably scaling the bias current of the component in the receiver circuit upon determination that the strength of the desired signal has decreased relative to the strength of the interferer signal;

wherein the variably scaling includes varying the bias current of the component in the receiver circuit through a plurality of values, responsive to the strength of the desired signal relative to the strength of the interferer signal, where the plurality of values is greater than or equal to three in number.

2. The method of claim 1, wherein the bias current of the component in the receiver circuit is reduced by switching an impedance that appears across a voltage thereby changing the bias current.

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3. A method of power dissipation control in a receiver circuit within a battery powered mobile device when the receiver circuit is receiving an RF input signal that includes a desired signal and an interferer signal, the method comprising:

determining a strength of the desired signal with respect to the interferer signal, wherein the receiver circuit comprises a defined signal path between the RF input signal and a processed signal output;

causing a variable decrease in power dissipation of the defined signal path within the receiver circuit and a resultant decreased battery drain, by variably scaling an impedance of a component in the receiver circuit upon determination that the strength of the desired signal has increased relative to the strength of the interferer signal; and

causing a variable increase in power dissipation of the defined signal path within the receiver circuit and a resultant increased battery drain, by variably scaling the impedance of the component in the receiver circuit upon determination that the strength of the desired signal has decreased relative to the strength of the interferer signal;

wherein the variable scaling includes:

setting the impedance of the component in the receiver circuit in between a high level and a low level;

adjusting the impedance of the component in the receiver circuit up or down; and

wherein the variable scaling occurs while the receiver circuit is processing signals received from the RF input signal.

4. The method of claim 3 wherein variably scaling the impedance of a component in the receiver circuit comprises variably scaling an impedance of a low noise amplifier (LNA).

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5. The method of claim 3 wherein variably scaling the impedance of a component in the receiver circuit comprises variably scaling an impedance of a mixer.

6. The method of claim 3 wherein variably scaling the impedance of a component in the receiver circuit comprises variably scaling an impedance of a filter.

7. The method of claim 3, wherein the impedance of a component in the receiver circuit comprises a resistance, and wherein a value of the resistance is increased by opening switches across one or more portions of the resistance.

8. The method of claim 3, wherein the defined signal path includes components that comprise: a low noise amplifier (LNA), a filter, a mixer.

9. The method of claim 8 wherein the component is a low noise amplifier.

10. The method of claim 8 wherein the component is a filter.

11. The method of claim 8 wherein the component is a mixer.

12. A method of power dissipation control in a receiver circuit within a battery powered mobile device when the receiver circuit is receiving an RF input signal that includes a desired signal and an interferer signal, the method comprising:

determining a strength of the interferer signal present in the received RF input signal;

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causing a variable decrease in power dissipation of a signal path within the receiver circuit and a resultant decreased battery drain, by variably scaling an impedance of a component in the receiver circuit upon determination that the strength of the interferer signal has decreased;

causing a variable increase in power dissipation of the signal path within the receiver circuit and the resultant decreased battery drain, by variably scaling the impedance of the component in the receiver circuit upon determination that the strength of the interferer signal has increased;

wherein the variable scaling includes:

switching the impedance of the component in the receiver circuit through a plurality of three or more levels between a high level and a low level responsive to the strength of the interferer signal present in the received RF input signal; and

wherein the variable scaling occurs while the receiver circuit is processing signals received from the RF input signal.

13. The method of claim 12, wherein the impedance of the component in the receiver circuit comprises a resistance, and wherein the value of the resistance may be increased by opening switches across one or more portions of the resistance.

14. A method of controlling power dissipation in a receiver circuit within a battery powered mobile device when the receiver circuit is receiving and processing an RF input signal in a signal path of the receiver circuit that includes a desired signal and an interferer signal, the method comprising:

determining a strength of the interferer signal present in the received RF input signal;

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causing a decrease in power dissipation of the signal path of the receiver circuit resulting in a decrease in drain on battery life, by variably scaling a gain of a component in the signal path of the receiver circuit upon determination that the strength of the interferer signal has decreased;

causing an increase in power dissipation of the signal path of the receiver circuit resulting in an increase in drain on battery life, by variably scaling the gain of the component in the signal path of the receiver circuit upon determination that the strength of the interferer signal has increased;

causing an increase in power dissipation of the signal path of the receiver circuit resulting in an increase in drain on battery life, by variably scaling the gain of the component in the signal path of the receiver circuit upon determination that the strength of the interferer signal has increased;

wherein the variable scaling includes:

setting the gain of the component in the signal path of the receiver circuit in between a high level and a low level; and

adjusting the gain of the component in the signal path of the receiver circuit up or down.

15. The method of claim 14, wherein the gain of the component in the signal path of the receiver circuit is varied by increasing a current in a differential pair and /or increasing a load resistance using switches.

16. A mobile communications device, comprising:

a receiver circuit for receiving an RF input signal that includes a desired signal and an interferer signal;

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a battery that powers the mobile communications device including the receiver circuit;

wherein a strength of the desired signal is determined with respect to the strength of the interferer signal;

wherein a variable decrease in power dissipation of a signal path within the receiver circuit and a resultant decreased battery drain is caused by variably scaling an impedance of a component in the receiver circuit upon determination that the strength of the desired signal has increased relative to the strength of the interferer signal; and

wherein a variable increase in power dissipation of the signal path within the receiver circuit and a resultant increased battery drain, is caused by variably scaling the impedance of the component in the receiver circuit upon determination that the strength of the desired signal has decreased relative to the strength of the interferer signal; and

wherein the variable scaling includes:

setting the impedance of the component in the receiver circuit in between a high level and a low level; and

adjusting the impedance of the component in the receiver circuit up or down; and

wherein the variable scaling occurs while the receiver circuit is processing signals received from the RF input signal.

17. The method of claim 16, wherein the impedance of the component in the receiver circuit comprises a resistance, and wherein a value of the resistance may be varied by opening and closing switches across one or more portions of the resistance responsive to the determined strength of the desired signal with respect to the interferer signal.

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POWER DISSIPATION REDUCTION IN WIRELESS TRANSCEIVERS

ABSTRACT OF THE DISCLOSURE

Methods and circuits for reducing power dissipation in wireless transceivers and other electronic circuits and systems. Embodiments of the present invention use bias current reduction, impedance scaling, and gain changes either separately or in combination to reduce power dissipation. For example, bias currents are reduced in response to a need for reduced signal handling capability, impedances are scaled thus reducing required drive and other bias currents in response to a strong received signal, or gain is increased and impedances are scaled in response to a low received signal in the presence of no or weak interfering signals.

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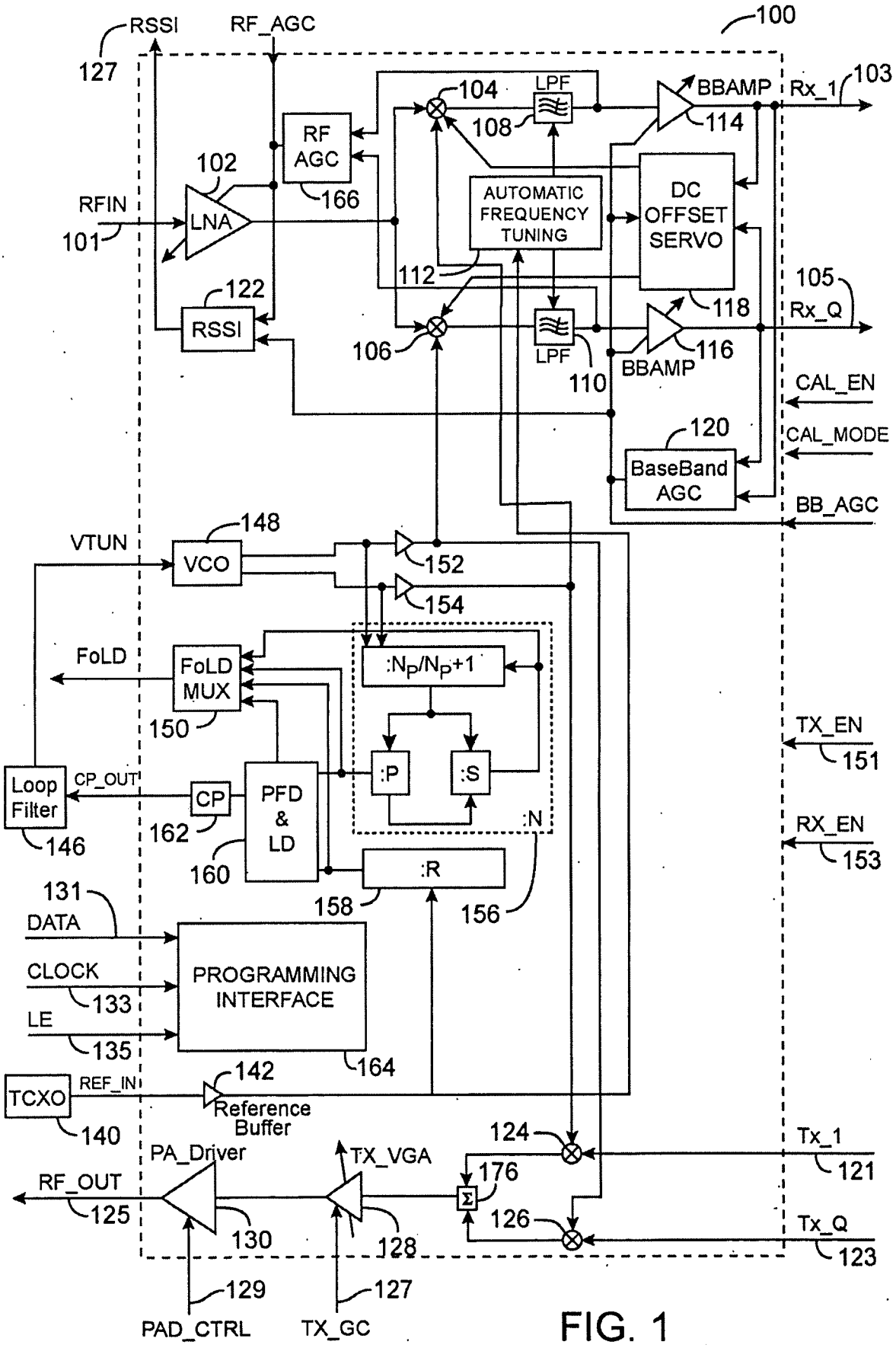

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DC OFFSET SERVO
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Rx_Q
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RSSI
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LPF
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BBAMP
116
CAL_EN
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BaseBand AGC
BB_AGC
VTUN
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VCO
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FoLD
FoLD MUX
150
:N_P/N_P+1
TX_EN
151
Loop Filter
146
CP_OUT
CP
162
PFD & LD
160
:P
:S
:N
RX_EN
153
:R
158
156
131
DATA
CLOCK
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LE
135
PROGRAMMING INTERFACE
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TCXO
140
REF_IN
142
Reference Buffer
124
Tx_1
121
PA_Driver
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TX_GC

FIG. 1

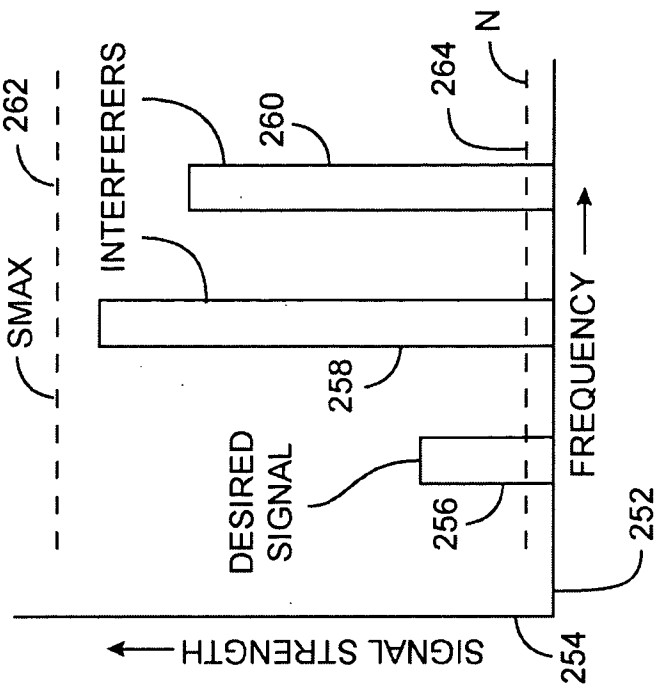

SMAX
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INTERFERERS
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264
N
258
DESIRED
SIGNAL
256
FREQUENCY
252
SIGNAL STRENGTH
254

FIG. 2B

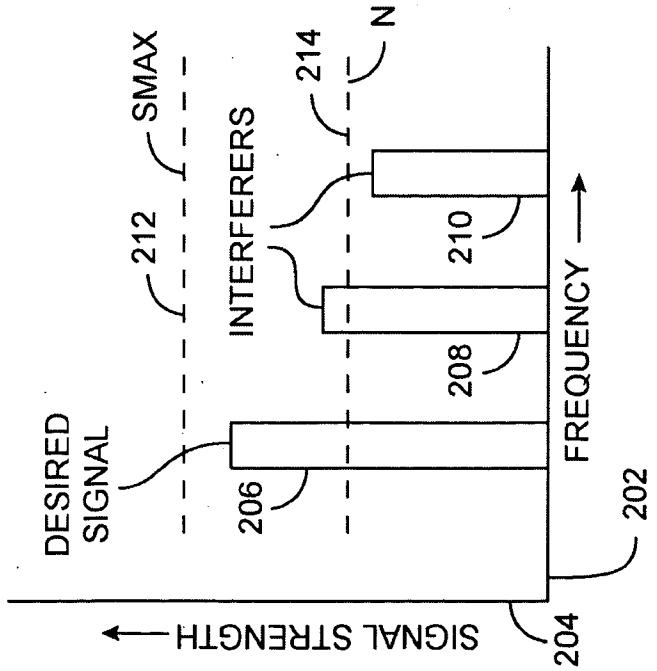

SMAX
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INTERFERERS
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208
DESIRED
SIGNAL
206
FREQUENCY
202
SIGNAL STRENGTH
204

FIG. 2A

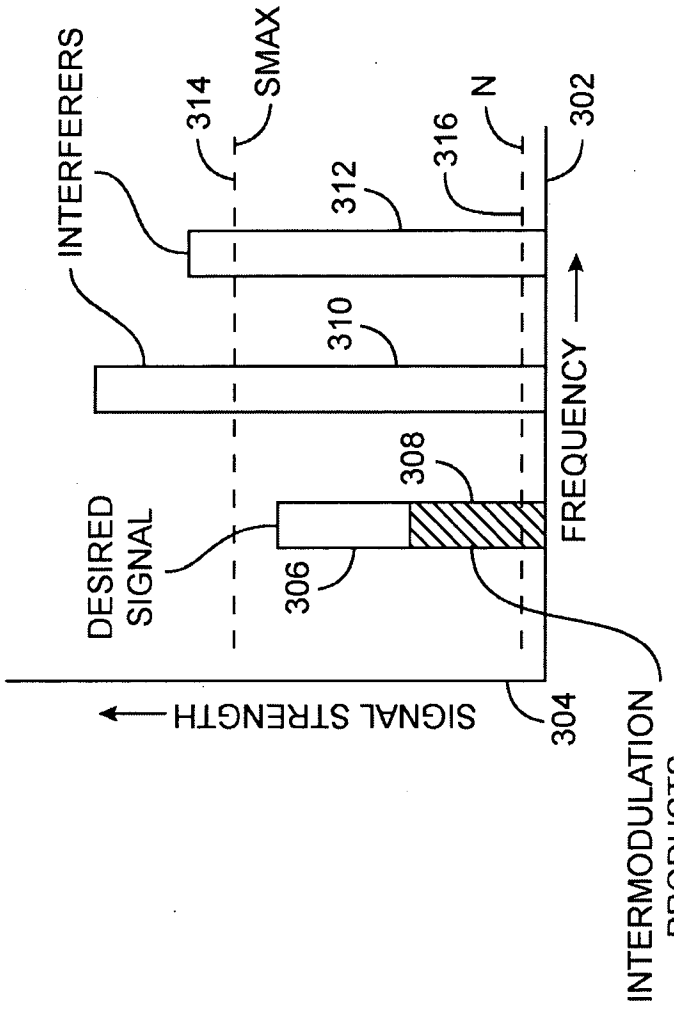

INTERFERERS
DESIRED SIGNAL
INTERMODULATION PRODUCTS
SIGNAL STRENGTH
FREQUENCY
SMAX
N
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306
308
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312
314
316

FIG. 3

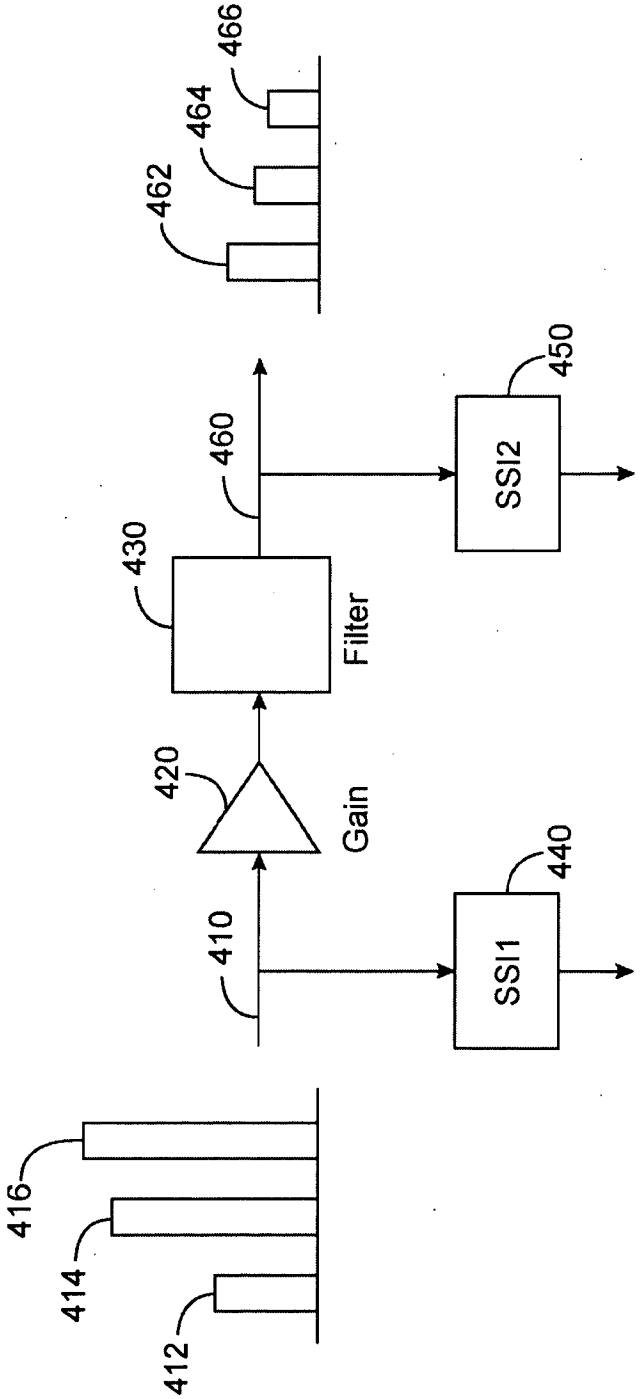

466
464
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450
460
SSI2
430
Filter
420
Gain
440
410
SSI1
416
414
412

FIG. 4

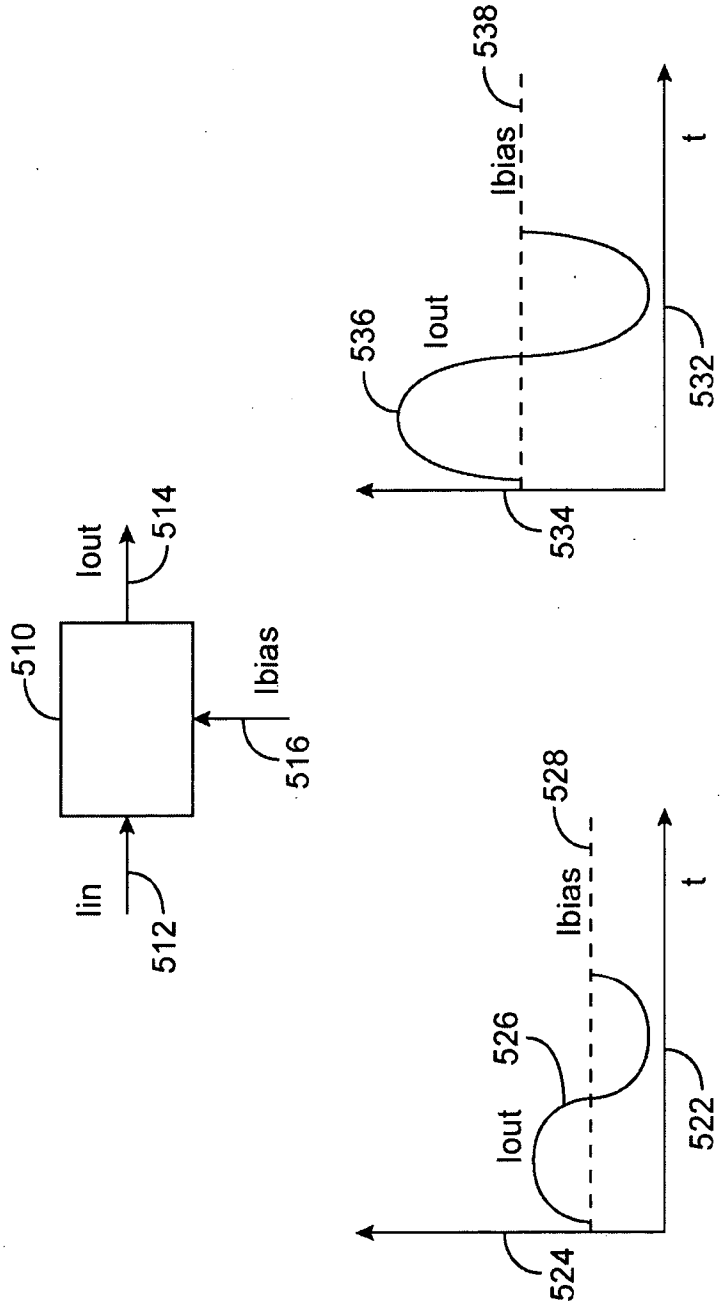

510
Iout
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Ibias
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Iin
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Ibias
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Iout
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Ibias
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526
Iout
522
524

FIG. 5

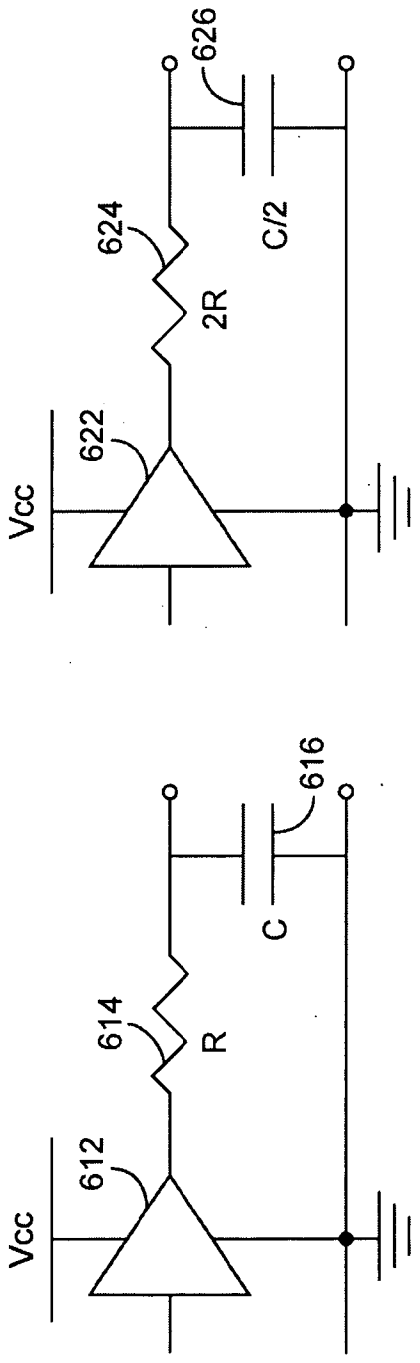


FIG. 6

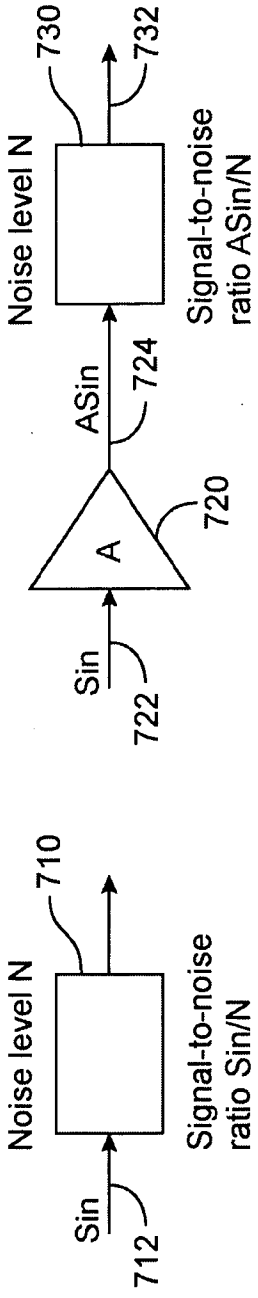

730
732
Noise level N
Signal-to-noise ratio ASin/N
ASin
724
A
720
Sin
722
710
Noise level N
Signal-to-noise ratio Sin/N
Sin
712

FIG. 7

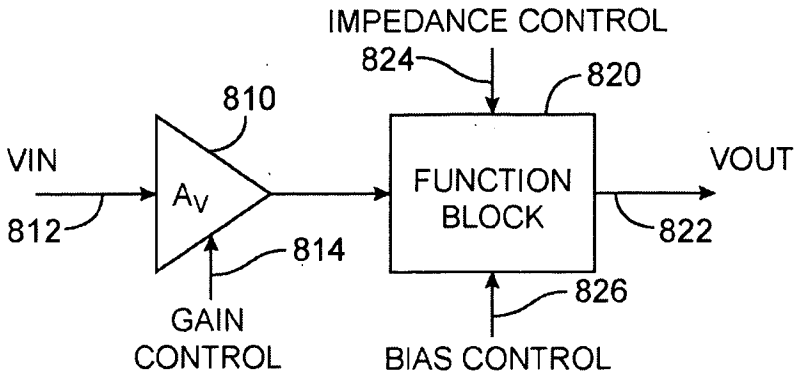


FIG. 8A

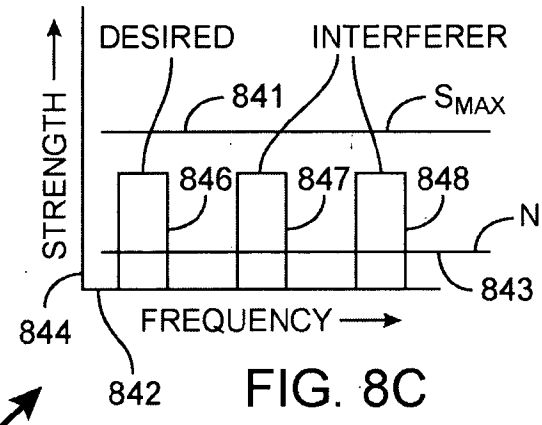


FIG. 8C

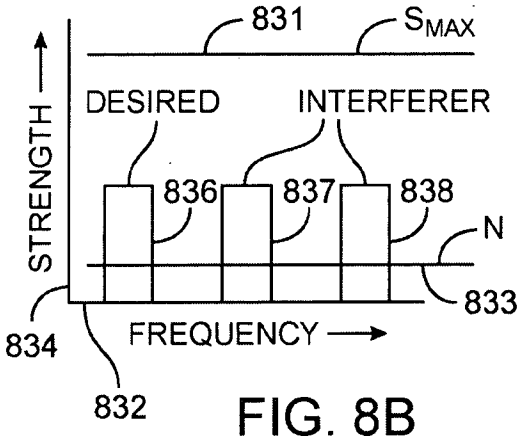


FIG. 8B

DECREASE BIASING

– AND/OR –

INCREASE GAIN AND IMPEDANCES

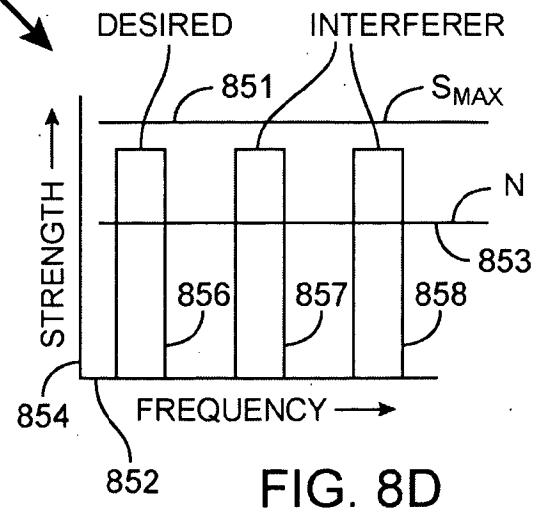


FIG. 8D

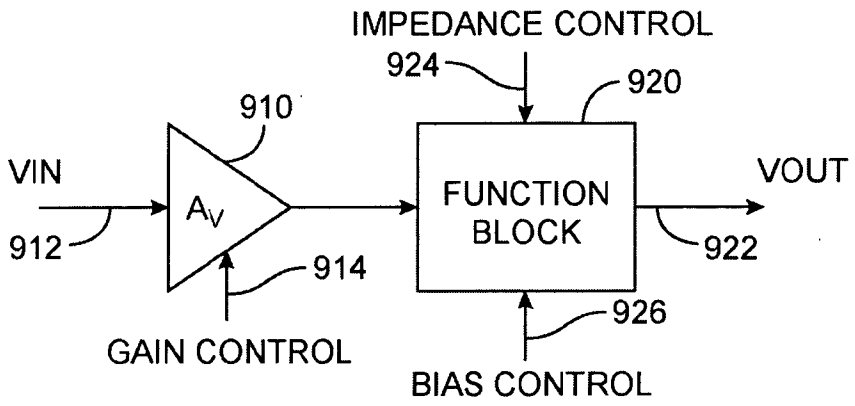


FIG. 9A

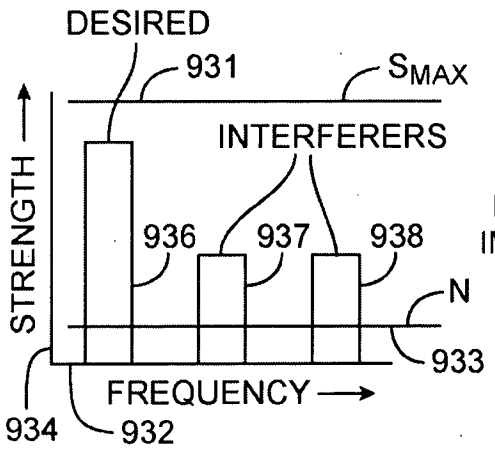


FIG. 9B

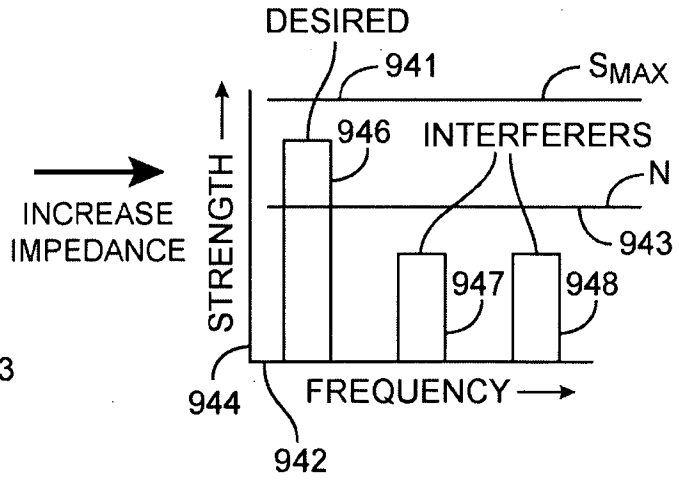


FIG. 9C

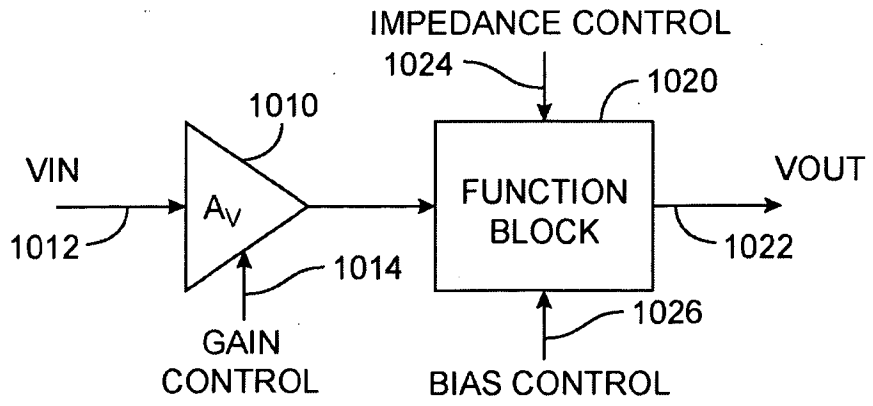


FIG. 10A

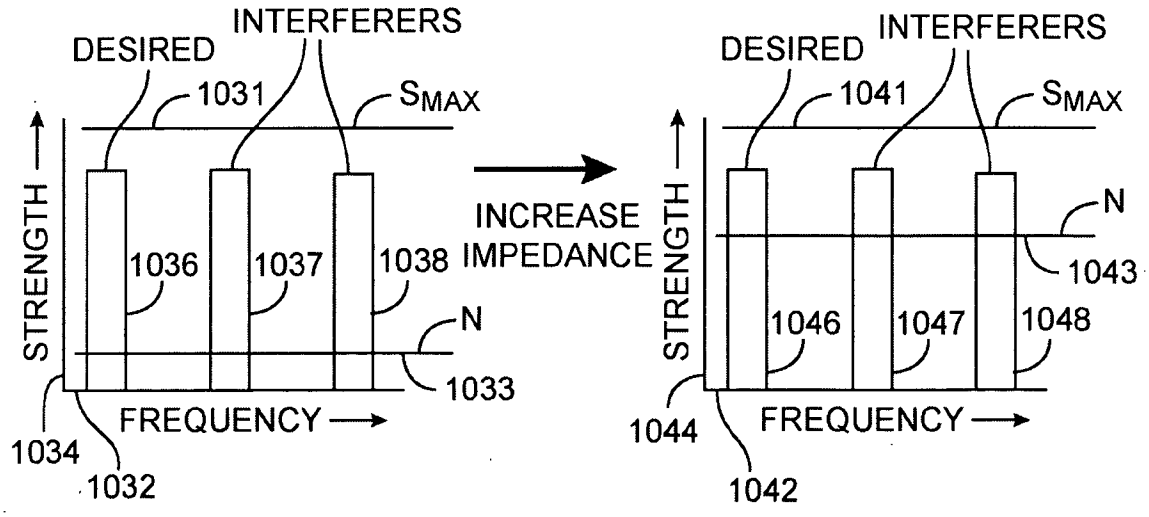


FIG. 10B

FIG. 10C

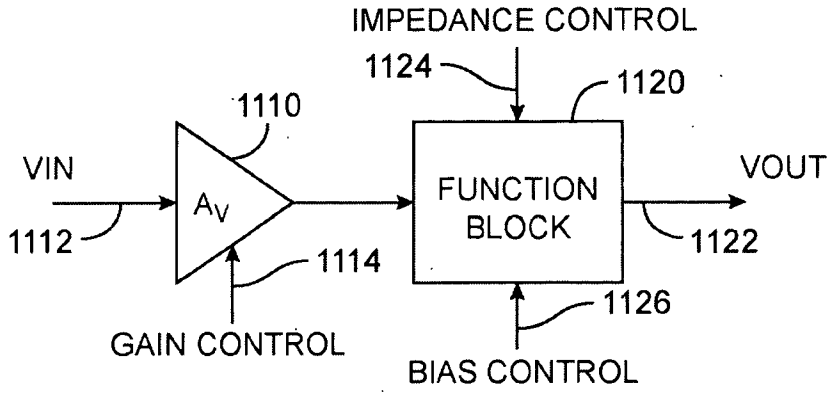


FIG. 11A

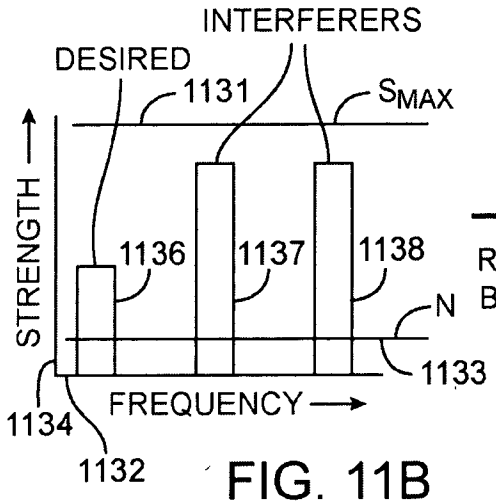


FIG. 11B

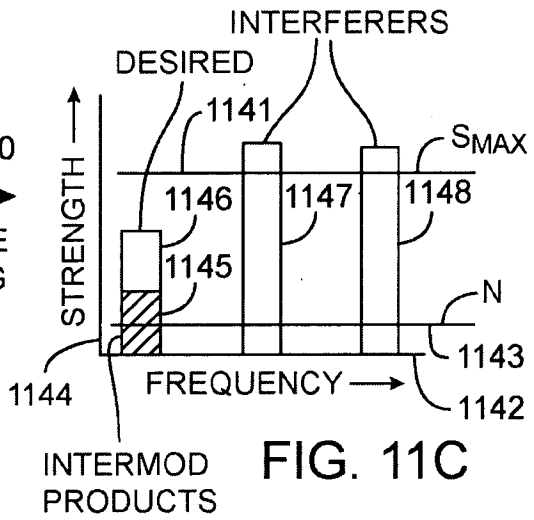


FIG. 11C

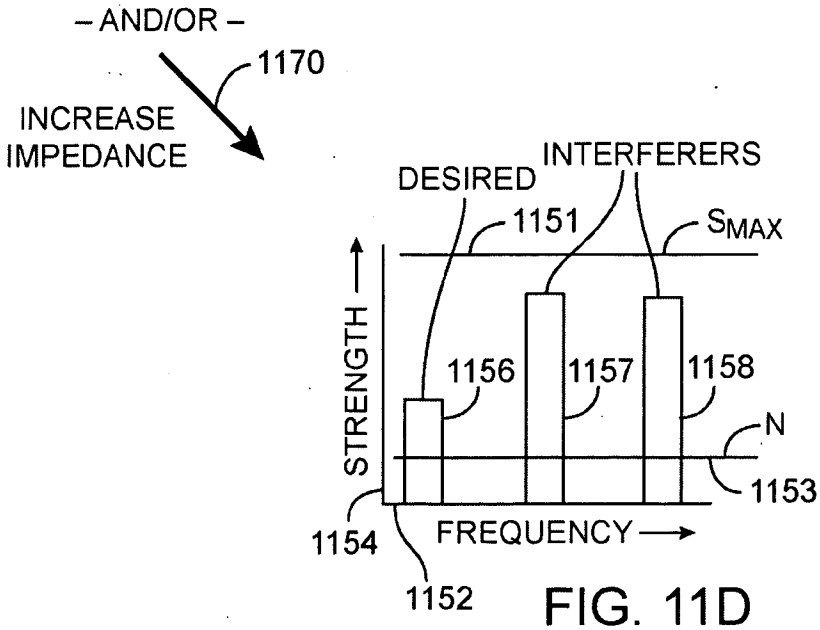


FIG. 11D

	1210 RECEIVED SIGNAL		1220 RESPONSE TO RECEIVED SIGNAL		
	SIGNAL STRENGTH	INTERFERER STRENGTH	DECREASE SMAX	INCREASE IMPEDANCE NOT GAIN	INCREASE IMPEDANCE AND GAIN
1230	SMALL	SMALL	YES	NO	YES
1240	LARGE	SMALL	NO	YES	NO
1250	LARGE	LARGE	NO	YES	NO
1260	SMALL	LARGE	NO	NO	NO

FIG. 12

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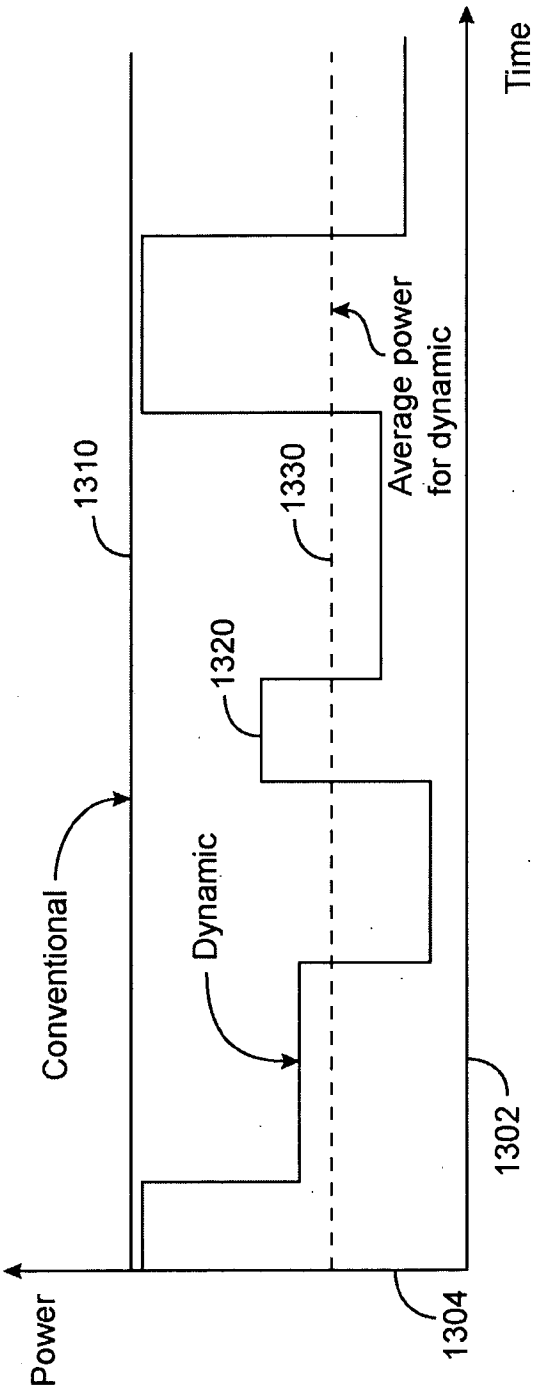

Power
Time
Conventional
Dynamic
1310
1320
1330
1302
1304
Average power
for dynamic

FIG. 13

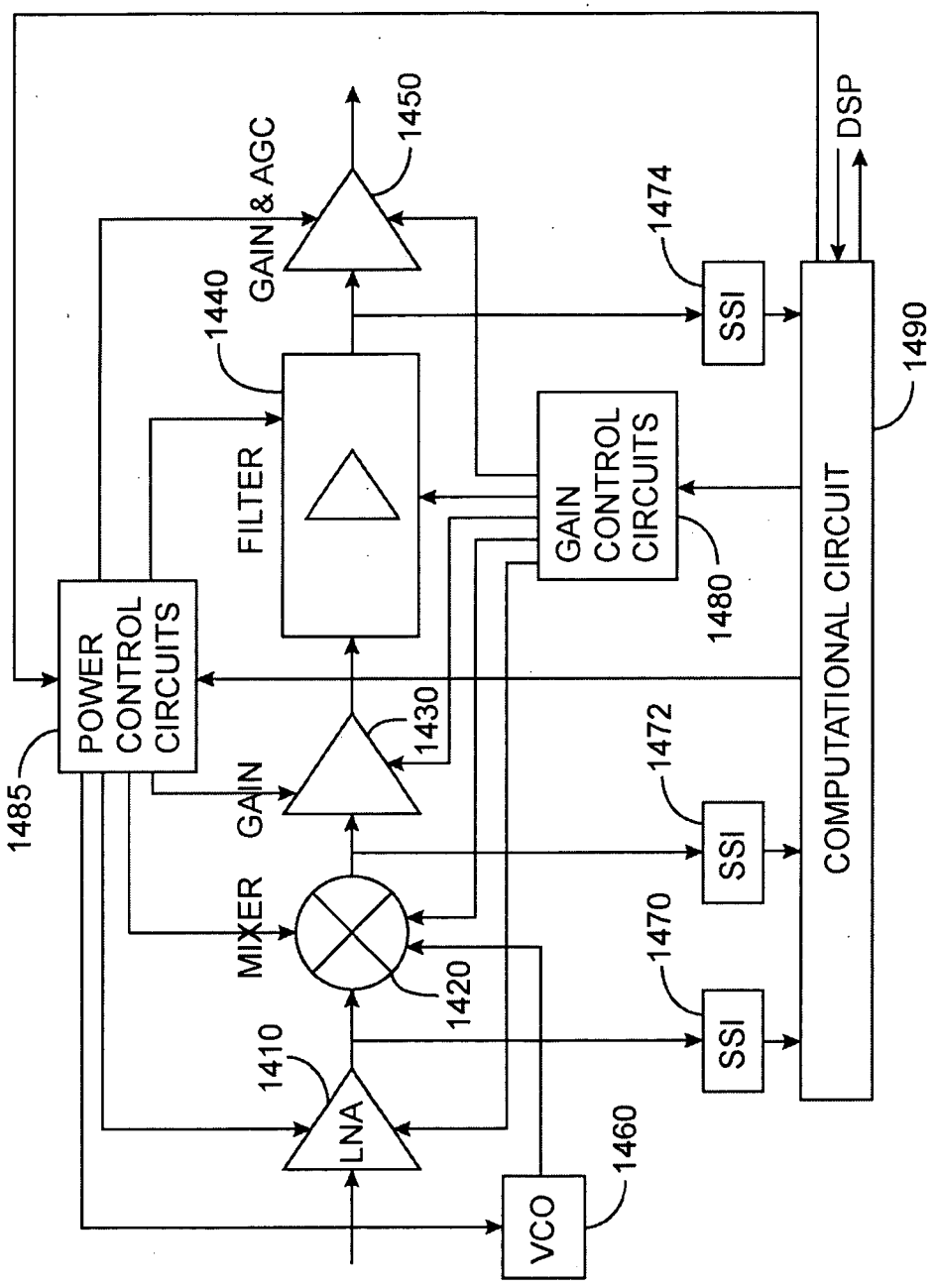

1485
POWER CONTROL CIRCUITS
1410
LNA
1420
MIXER
1430
GAIN
1440
FILTER
1450
GAIN & AGC
1460
VCO
1470
SSI
1472
SSI
1474
SSI
1480
GAIN CONTROL CIRCUITS
1490
COMPUTATIONAL CIRCUIT
DSP

FIG. 14

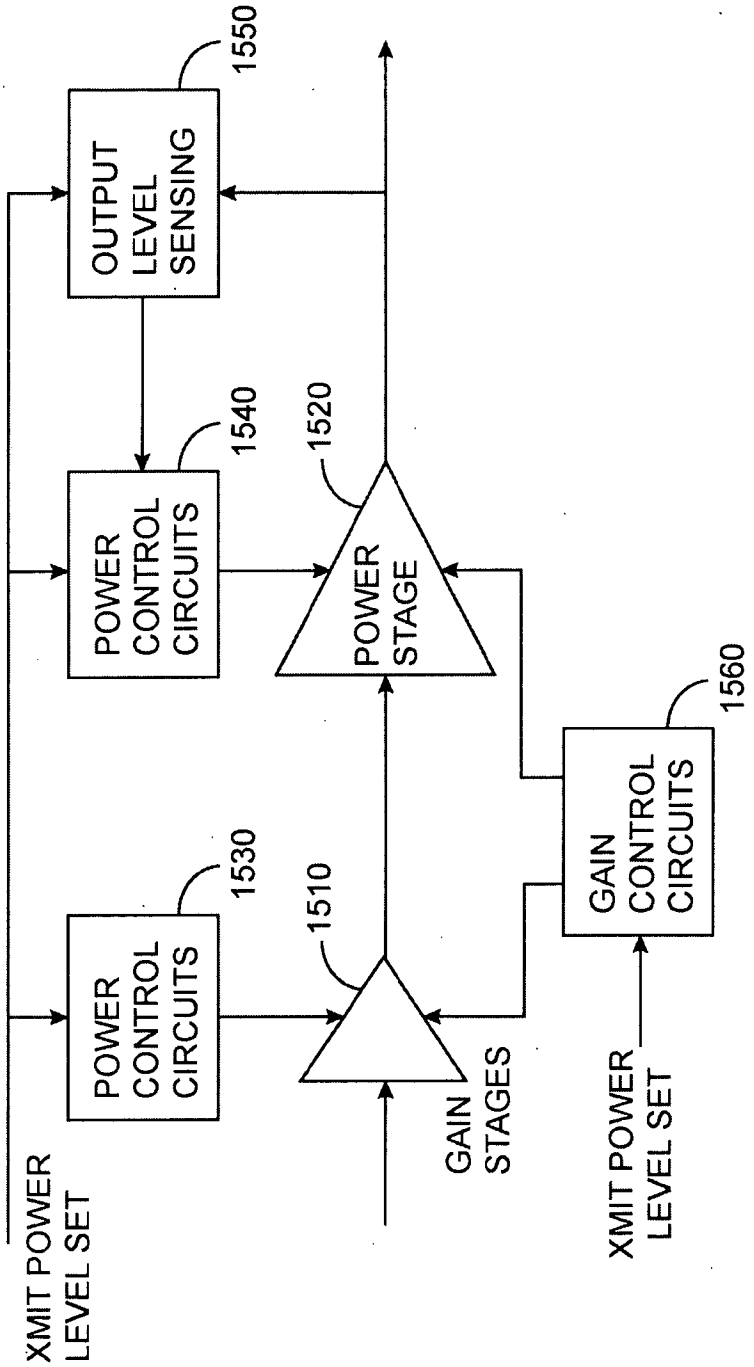

OUTPUT LEVEL SENSING
1550
POWER CONTROL CIRCUITS
1540
POWER STAGE
1520
POWER CONTROL CIRCUITS
1530
1510
GAIN CONTROL CIRCUITS
1560
XMIT POWER LEVEL SET
GAIN STAGES
XMIT POWER LEVEL SET

FIG. 15

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	Power Dissipation Reduction in Wireless Transceivers
First Named Inventor/Applicant Name:	Yannis Tsividis
Filer:	Roger W. Blakely/Jessica Clark
Attorney Docket Number:	10037P007CC2

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Utility filing Fee (Electronic filing)	4011	1	70	70
Utility Search Fee	2111	1	300	300
Utility Examination Fee	2311	1	360	360
Pages:				
Claims:				
Independent Claims in Excess of 3	2201	2	210	420
Miscellaneous-Filing:				
Petition:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1150**

Electronic Acknowledgement Receipt

EFS ID:	25302634
Application Number:	15080432
International Application Number:	
Confirmation Number:	6094
Title of Invention:	Power Dissipation Reduction in Wireless Transceivers
First Named Inventor/Applicant Name:	Yannis Tsividis
Customer Number:	8791
Filer:	Roger W. Blakely/Jessica Clark
Filer Authorized By:	Roger W. Blakely
Attorney Docket Number:	10037P007CC2
Receipt Date:	24-MAR-2016
Filing Date:	
Time Stamp:	19:49:26
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$1150
RAM confirmation Number	6063
Deposit Account	022666
Authorized User	BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 CFR 1.16 (National application filing, search, and examination fees)

Charge any Additional Fees required under 37 CFR 1.17 (Patent application and reexamination processing fees)

Charge any Additional Fees required under 37 CFR 1.19 (Document supply fees)

Charge any Additional Fees required under 37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	10037P007CC2_20160324_ADS.pdf	1793337 5fba1d63c8fabbf38ac27b3d270e363d396a53b0	no	8
Warnings:					
Information:					
2	Power of Attorney	10037P007CC2_20160324_POAwTrans.pdf	1166614 750294cad6b9d66159013a1dd25e140737f2bf66	no	2
Warnings:					
Information:					
3	Oath or Declaration filed	10037P007CC2_20160324_Decl.pdf	118541 a17d0d8e66c4ce4ebfd551c8e0168bf60730562f	no	2
Warnings:					
Information:					
4		10037P007CC2_20160324_App.pdf	947614 68f8a8eb06a547210a5f2229382f9611c07ea640	yes	24

Multipart Description/PDF files in .zip description

Document Description	Start	End
Specification	1	17
Claims	18	23
Abstract	24	24

Warnings:					
Information:					
5	Drawings-only black and white line drawings	10037P007CC2_20160324_Figs.pdf	214193 454ef132fedc618b0152e6fa42d1854117293004	no	15
Warnings:					
Information:					
6	Fee Worksheet (SB06)	fee-info.pdf	36482 8c32cf96fd1975ef19b824340b36331815b5e096	no	2

Warnings:	
Information:	
Total Files Size (in bytes):	4276781

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	10037P007CC2
	Application Number	
Title of Invention	Power Dissipation Reduction in Wireless Transceivers	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 — Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Yannis		Tsividis	

Residence Information (Select One) ● US Residency Non US Residency Active US Military Service

City	State/Province	Country of Residence
New York	NY	US

Mailing Address of Inventor:

Address 1	Dept. of Electrical Engineering
Address 2	Columbia University

City	State/Province	Postal Code	Country
New York	NY	10027	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	08791	
Email Address		Add Email Remove Email

Application Information:

Title of the Invention	Power Dissipation Reduction in Wireless Transceivers		
Attorney Docket Number	10037P007CC2	**Small Entity Status Claimed**	☒
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	15	**Suggested Figure for Publication (if any)**	14

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	10037P007CC2
	Application Number	
Title of Invention	Power Dissipation Reduction in Wireless Transceivers	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	● Customer Number	US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	08791		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Continuation of	11318646	2005-12-27

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	10037P007CC2
	Application Number	
Title of Invention	Power Dissipation Reduction in Wireless Transceivers	

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
11318646	Continuation of	10784613	2004-02-23	7010330	2006-03-07

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
10784613	Claims benefit of provisional	60451229	2003-03-01

Prior Application Status			Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
10784613	Claims benefit of provisional	60451230	2003-03-01

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	10037P007CC2
	Application Number	
Title of Invention	Power Dissipation Reduction in Wireless Transceivers	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	10037P007CC2
	Application Number	
Title of Invention	Power Dissipation Reduction in Wireless Transceivers	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1 — Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

● Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor
Person to whom the inventor is obligated to assign.	Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

Organization Name	Theta IP, LLC		
Mailing Address Information For Applicant:			
Address 1	710 Inglenook Court		
Address 2			
City	Coppell	**State/Province**	TX
Country	US	Postal Code	75019
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	10037P007CC2
	Application Number	
Title of Invention	Power Dissipation Reduction in Wireless Transceivers	

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Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

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See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/RWB/			Date (YYYY-MM-DD)	2016-03-24
First Name	Roger	Last Name	Blakely	Registration Number	25831

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PTO/AIA/14 (11-15)
Approved for use through 04/30/2017. OMB 0651-0032
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	10037P007CC2
	Application Number	
Title of Invention	Power Dissipation Reduction in Wireless Transceivers	

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Electronic Acknowledgement Receipt

EFS ID:	25302634
Application Number:	15080432
International Application Number:	
Confirmation Number:	6094
Title of Invention:	Power Dissipation Reduction in Wireless Transceivers
First Named Inventor/Applicant Name:	Yannis Tsividis
Customer Number:	8791
Filer:	Roger W. Blakely/Jessica Clark
Filer Authorized By:	Roger W. Blakely
Attorney Docket Number:	10037P007CC2
Receipt Date:	24-MAR-2016
Filing Date:	
Time Stamp:	19:49:26
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$1150
RAM confirmation Number	6063
Deposit Account	022666
Authorized User	BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

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Charge any Additional Fees required under 37 CFR 1.16 (National application filing, search, and examination fees)

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Charge any Additional Fees required under 37 CFR 1.19 (Document supply fees)

Charge any Additional Fees required under 37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	10037P007CC2_20160324_ADS.pdf	1793337 5fba1d63c8fabbf38ac27b3d270e363d396a53b0	no	8
Warnings:					
Information:					
2	Power of Attorney	10037P007CC2_20160324_POAwTrans.pdf	1166614 750294cad6b9d66159013a1dd25e140737f2bf66	no	2
Warnings:					
Information:					
3	Oath or Declaration filed	10037P007CC2_20160324_Decl.pdf	118541 a17d0d8e66c4ce4ebfd551c8e0168bf60730562f	no	2
Warnings:					
Information:					
4		10037P007CC2_20160324_App.pdf	947614 68f8a8eb06a547210a5f2229382f9611c07ea640	yes	24

Multipart Description/PDF files in .zip description

Document Description	Start	End
Specification	1	17
Claims	18	23
Abstract	24	24

Warnings:					
Information:					
5	Drawings-only black and white line drawings	10037P007CC2_20160324_Figs.pdf	214193 454ef132fedc618b0152e6fa42d1854117293004	no	15
Warnings:					
Information:					
6	Fee Worksheet (SB06)	fee-info.pdf	36482 8c32cf96fd1975ef19b824340b36331815b5e096	no	2

Warnings:	
Information:	
Total Files Size (in bytes):	4276781

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National Stage of an International Application under 35 U.S.C. 371
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New International Application Filed with the USPTO as a Receiving Office
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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
15/080,432	03/24/2016	2422	1150	10037P007CC2	17	5

CONFIRMATION NO. 6094

8791
BLAKELY SOKOLOFF TAYLOR & ZAFMAN
1279 Oakmead Parkway
Sunnyvale, CA 94085-4040

FILING RECEIPT

OC000000082036287

Date Mailed: 04/08/2016

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Yannis Tsividis, New York, NY;

Applicant(s)

Theta IP, LLC, Coppell, TX;

Power of Attorney: The patent practitioners associated with Customer Number 08791

Domestic Priority data as claimed by applicant

This application is a CON of 11/318,646 12/27/2005
which is a CON of 10/784,613 02/23/2004 PAT 7010330
which claims benefit of 60/451,229 03/01/2003
and claims benefit of 60/451,230 03/01/2003

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 04/07/2016

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The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 15/080,432**

Projected Publication Date: 07/21/2016

Non-Publication Request: No

Early Publication Request: No
**** SMALL ENTITY ****
Title

Power Dissipation Reduction in Wireless Transceivers

Preliminary Class

348

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

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Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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Apple EX1002 Page 62

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 15/080,432

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	70		N/A	
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	300		N/A	
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	360		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	17 minus 20 =	*	x 40 =	0.00	OR		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	5 minus 3 =	* 2	x 210 =	420			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			0.00			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				0.00			
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	1150		TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application. No.	:	15/080,432	Confirmation No. 6094
Inventor(s)	:	Yannis Tsividis	
Filed	:	03/24/2016	
TC/A.U.	:		
Examiner	:		
Docket No.	:	10037P007CC2	
Customer No.	:	8791	

Mail Stop Amendment
Commissioner for Patents
PO Box 1450
Alexandria VA 22313-1450

PRELIMINARY AMENDMENT

Sir:

Prior to examination, please amend the above-identified application as follows:

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Claims are reflected in the listing of claims which begins on page 4 of this paper.

Remarks/Arguments begin on page 10 of this paper.

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Amendments to the Specification:

Please replace paragraph [0047] with the following amended paragraph:

[0047] The minimum power dissipation for a circuit is proportional to the required maximum signal-to-noise ratio, which is the ratio between Smax 212 or 262 and N 214 ~~and~~ or 264. Thus, a circuit receiving an input similar to the one shown in Figure 2A can dissipate less power than one receiving the input as shown in Figure 2B, while still achieving an acceptable bit-error rate.

Please replace paragraph [0071] with the following amended paragraph:

[0071] The maximum signaling capability 931 and noise floor 933 are shown as being set for the worst case conditions. In this case, the noise floor 933 is lower than the maximum allowed for proper signal reception. Accordingly, one or more impedance in the function block 920 may be increased, such that the noise floor 943 rises as shown in Figure 9C. In this way one or more of the driving currents in the function block 920 may be reduced. Similarly, since the drive current is reduced, one or more bias current may also be reduced, depending on the exact circuit configuration.

Amendments to the Abstract:

Please replace the Abstract with the Abstract that appears on the following page:

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ABSTRACT

~~Methods~~ Processes, methods and circuits for improving battery life by reducing ~~power dissipation in~~ the battery power-drain of battery-powered devices using wireless transceivers is disclosed~~and other electronic circuits and systems~~. Embodiments of the present invention ~~use~~ provide for dynamically changing the bias current ~~reduction~~, impedance ~~scaling,~~ and gain, ~~changes~~ either separately or in combination, during circuit operation to optimize or to reduce power dissipation. ~~For example, bias currents are reduced in response to a need for reduced signal handling capability, impedances are scaled thus reducing required drive and other bias currents in response to a strong received signal, or gain is increased and impedances are scaled in response to a low received signal in the presence of no or weak interfering signals.~~The dynamic variations may be implemented by varying the value of a resistance and/or a capacitance by opening switches across one or more portions of the resistance. Also, the dynamic variations may include setting any of the gain, bias current, or impedance parameters of the receiver circuit in between a high and low level, followed by adjusting the parameter up or down in response to a desired signal and an interferer signal.

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Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (original) A method of power dissipation control in a receiver circuit within a battery powered mobile device when the receiver circuit is receiving and processing an RF input signal that includes a desired signal and an interferer signal, the method comprising:

determining a strength of the desired signal with respect to the strength of the interferer signal;

causing a variable decrease in power dissipation of a signal path within the receiver circuit and a resultant decreased battery drain, by variably scaling a bias current of a component in the receiver circuit upon determination that the strength of the desired signal has increased relative to the strength of the interferer signal;

causing a variable increase in power dissipation of the signal path within the receiver circuit and a resultant increased battery drain, by variably scaling the bias current of the component in the receiver circuit upon determination that the strength of the desired signal has decreased relative to the strength of the interferer signal;

wherein the variably scaling includes varying the bias current of the component in the receiver circuit through a plurality of values, responsive to the strength of the desired signal relative to the strength of the interferer signal, where the plurality of values is greater than or equal to three in number.

2. (original) The method of claim 1, wherein the bias current of the component in the receiver circuit is reduced by switching an impedance that appears across a voltage thereby changing the bias current.

3. (original) A method of power dissipation control in a receiver circuit within a battery powered mobile device when the receiver circuit is receiving an RF input signal that includes a desired signal and an interferer signal, the method comprising:

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determining a strength of the desired signal with respect to the interferer signal, wherein the receiver circuit comprises a defined signal path between the RF input signal and a processed signal output;

causing a variable decrease in power dissipation of the defined signal path within the receiver circuit and a resultant decreased battery drain, by variably scaling an impedance of a component in the receiver circuit upon determination that the strength of the desired signal has increased relative to the strength of the interferer signal; and

causing a variable increase in power dissipation of the defined signal path within the receiver circuit and a resultant increased battery drain, by variably scaling the impedance of the component in the receiver circuit upon determination that the strength of the desired signal has decreased relative to the strength of the interferer signal;

wherein the variable scaling includes:

setting the impedance of the component in the receiver circuit in between a high level and a low level;

adjusting the impedance of the component in the receiver circuit up or down; and

wherein the variable scaling occurs while the receiver circuit is processing signals received from the RF input signal.

4. (original) The method of claim 3 wherein variably scaling the impedance of a component in the receiver circuit comprises variably scaling an impedance of a low noise amplifier (LNA).

5. (original) The method of claim 3 wherein variably scaling the impedance of a component in the receiver circuit comprises variably scaling an impedance of a mixer.

6. (original) The method of claim 3 wherein variably scaling the impedance of a component in the receiver circuit comprises variably scaling an impedance of a filter.

7. (original) The method of claim 3, wherein the impedance of a component in the receiver circuit comprises a resistance, and wherein a value of the resistance is increased by opening switches across one or more portions of the resistance.

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8. (original) The method of claim 3, wherein the defined signal path includes components that comprise: a low noise amplifier (LNA), a filter, a mixer.

9. (original) The method of claim 8 wherein the component is a low noise amplifier.

10. (original) The method of claim 8 wherein the component is a filter.

11. (original) The method of claim 8 wherein the component is a mixer.

12. (original) A method of power dissipation control in a receiver circuit within a battery powered mobile device when the receiver circuit is receiving an RF input signal that includes a desired signal and an interferer signal, the method comprising:

determining a strength of the interferer signal present in the received RF input signal;

causing a variable decrease in power dissipation of a signal path within the receiver circuit and a resultant decreased battery drain, by variably scaling an impedance of a component in the receiver circuit upon determination that the strength of the interferer signal has decreased;

causing a variable increase in power dissipation of the signal path within the receiver circuit and the resultant decreased battery drain, by variably scaling the impedance of the component in the receiver circuit upon determination that the strength of the interferer signal has increased;

wherein the variable scaling includes:

switching the impedance of the component in the receiver circuit through a plurality of three or more levels between a high level and a low level responsive to the strength of the interferer signal present in the received RF input signal; and

wherein the variable scaling occurs while the receiver circuit is processing signals received from the RF input signal.

13. (original) The method of claim 12, wherein the impedance of the component in the receiver circuit comprises a resistance, and wherein the value of the resistance may be increased by opening switches across one or more portions of the resistance.

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14. (original) A method of controlling power dissipation in a receiver circuit within a battery powered mobile device when the receiver circuit is receiving and processing an RF input signal in a signal path of the receiver circuit that includes a desired signal and an interferer signal, the method comprising:

determining a strength of the interferer signal present in the received RF input signal;

causing a decrease in power dissipation of the signal path of the receiver circuit resulting in a decrease in drain on battery life, by variably scaling a gain of a component in the signal path of the receiver circuit upon determination that the strength of the interferer signal has decreased;

causing an increase in power dissipation of the signal path of the receiver circuit resulting in an increase in drain on battery life, by variably scaling the gain of the component in the signal path of the receiver circuit upon determination that the strength of the interferer signal has increased;

causing an increase in power dissipation of the signal path of the receiver circuit resulting in an increase in drain on battery life, by variably scaling the gain of the component in the signal path of the receiver circuit upon determination that the strength of the interferer signal has increased;

wherein the variable scaling includes:

setting the gain of the component in the signal path of the receiver circuit in between a high level and a low level; and

adjusting the gain of the component in the signal path of the receiver circuit up or down.

15. (original) The method of claim 14, wherein the gain of the component in the signal path of the receiver circuit is varied by increasing a current in a differential pair and /or increasing a load resistance using switches.

16. (original) A mobile communications device, comprising:

a receiver circuit for receiving an RF input signal that includes a desired signal and an interferer signal;

a battery that powers the mobile communications device including the receiver circuit;

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wherein a strength of the desired signal is determined with respect to the strength of the interferer signal;

wherein a variable decrease in power dissipation of a signal path within the receiver circuit and a resultant decreased battery drain is caused by variably scaling an impedance of a component in the receiver circuit upon determination that the strength of the desired signal has increased relative to the strength of the interferer signal; and

wherein a variable increase in power dissipation of the signal path within the receiver circuit and a resultant increased battery drain, is caused by variably scaling the impedance of the component in the receiver circuit upon determination that the strength of the desired signal has decreased relative to the strength of the interferer signal; and

wherein the variable scaling includes:

setting the impedance of the component in the receiver circuit in between a high level and a low level; and

adjusting the impedance of the component in the receiver circuit up or down; and

wherein the variable scaling occurs while the receiver circuit is processing signals received from the RF input signal.

17. (currently amended) The ~~method~~ mobile communication device of claim 16, wherein the impedance of the component in the receiver circuit comprises a resistance, and wherein a value of the resistance may be varied by opening and closing switches across one or more portions of the resistance responsive to the determined strength of the desired signal with respect to the interferer signal.

18. (new) A method for conserving battery power in a mobile communication device, the method comprising:

receiving a radio signal by a radio receiver, of the transceiver, that include a desired signal and an interferer signal;

powering to the radio transceiver by a battery;

processing of the received radio signals in a signal path within the radio receiver;

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determining the strength of the interferer signal by a circuit coupled to the signal path of the receiver;

adjusting a gain and an impedance of the signal path of the receiver through a plurality of more than two levels responsive to the determined strength of the interferer signal;

where in adjusting the gain and impedance of the signal path result in improving a power drain from the battery.

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REMARKS/ARGUMENTS

Please enter this preliminary amendment prior to examination of this case.

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Apple EX1002 Page 73

CONCLUSION

Applicant respectfully requests examination of this application.

Respectfully submitted,

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Dated: 04/20/2016

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CERTIFICATE OF TRANSMISSION (37 CFR 1.8A)

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.

Date: 04/20/2016

Jessica A. Clark 4/20/2016
Jessica A. Clark *Date*

IPR2024-00817
Apple EX1002 Page 74

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application. No.	:	15/080,432	Confirmation No. 6094
Applicant	:	Yannis Tsividis	
Filed	:	03/24/2016	
TC/A.U.	:		
Examiner	:		
Docket No.	:	10037P007CC2	
Customer No.	:	8791	

Commissioner for Patents
PO Box 1450
Alexandria VA 22313-1450

AUTHORIZATION FOR EXTENSION OF TIME, ALL REPLIES

Sir:

Authorization is given to treat any concurrent or future reply requiring a petition for an extension of time under 37 CFR §1.136(a) for its timely submission, as incorporating a petition for extension of time for the appropriate length of time. If any other petition is necessary for consideration of this paper, it is hereby so petitioned. Please charge any shortage in fees in connection with the filing of this paper, including extension of time fees, to Deposit Account 02-2666 and please credit any excess fees to such deposit account.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 04/20/2016

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IPR2024-00817
Apple EX1002 Page 75

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application. No.	:	15/080,432	Confirmation No. 6094
Inventor(s)	:	Yannis Tsividis	
Filed	:	03/24/2016	
TC/A.U.	:		
Examiner	:		
Docket No.	:	10037P007CC2	
Customer No.	:	08791	

Commissioner for Patents
PO Box 1450
Alexandria VA 22313-1450

NOTICE OF COPENDING U.S. PATENT APPLICATION

Sir:

In accordance with the duty of disclosure, Applicant hereby provides notice of the following copending application, which may have similar subject matter:

U.S. Patent Application No. 15/080,421, filed 03/24/2016

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 04/20/2016

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Jessica A. Clark 4/20/2016
Jessica A. Clark *Date*

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Apple EX1002 Page 76

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application No.	15/080,432
Filing Date	March 24, 2016
First Inventor	Yannis Tsividis
Art Unit	
Examiner Name	
Attorney Docket No.	10037P007CC2 Conf. No. 6094

DUTY OF DISCLOSURE STATEMENT

In accordance with the duty of disclosure, enclosed is a copy of an Information Disclosure Statement (IDS) Citation Form PTO/SB/08 or PTO-1449, together with copies of the documents cited on that form, except for copies not required to be submitted (e.g., copies of U.S. patents and U.S. published patent applications need not be enclosed). This IDS and IDS Citation Form are being submitted within three (3) months of filing of the application. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s). Some or all of the references listed on the enclosed PTO/SB/08 were previously identified in one or more prior applications as follows:
Application No. 10/784,613, filed February 23, 2004
Application No. 11/318,646, filed December 27, 2005
and copies of the references were furnished at that time. Accordingly, per 37 CFR §1.98(d)(1) additional copies of those references are not submitted herewith.

The submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

OR

☒ None

☐ The IDS Filing Fee in the amount of $90.00 as set forth in 37 CFR 1.17(p) has been submitted herewith.

☒ It is requested that any requisite fees be debited from Deposit Account 02-2666.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of signature.

Signature	/Roger W. Blakely, Jr./	Date (MM-DD-YYYY)	04-20-2016
Name/Print	Roger W. Blakely, Jr.	Registration Number	25831

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.

Jessica A. Clark /Jessica A. Clark/ *Date* *04-20-16*

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Substitute for form 1449A/PTO	Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	15/080,432
	Filing Date	03/24/2016
	First Named Inventor	Yannis Tsividis
	Group Art Unit	
	Examiner Name	
Sheet 1 of 5	Attorney Docket No: 10037P007CC2	

US PATENT DOCUMENTS					
Examiner Initial *	**Cite No [1]**	**USP Document Number**	**Publication or Issue Date MM-DD-YYYY**	**Name of Patentee or Applicant of cited Document**	**Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear**
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	15/080,432
	Filing Date	03/24/2016
	First Named Inventor	Yannis Tsividis
	Group Art Unit	
	Examiner Name	
Sheet 2 of 5	Attorney Docket No: 10037P007CC2	

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Examiner Initial *	**Cite No [1]**	**USP Document Number**	**Publication or Issue Date MM-DD-YYYY**	**Name of Patentee or Applicant of cited Document**	**Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear**
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EXAMINER **DATE CONSIDERED**

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Sheet 3 of 5	Attorney Docket No: 10037P007CC2	

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Examiner Initials*	Cite No [1]	Foreign Patent Document Country Code/Number/Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[2]
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Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
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	First Named Inventor	Yannis Tsividis
	Group Art Unit	
	Examiner Name	
Sheet 4 of 5	Attorney Docket No: 10037P007CC2	

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	**Cite No [1]**	**Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.**	**T[2]**
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		YOSHIZAWA, ATSUSHI , et al., "An Anti-Blocker Structure MOSFET-C Filter For a Direct Conversion Receiver", IEEE 2001 Custom Integrated Circuits Conference, (2001), Pgs. 5-8	

EXAMINER **DATE CONSIDERED**

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449) as modified by BSTZ 03/26/07

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional) [2] Applicant is to place a check mark here if English language Translation is attached

Substitute for form 1449A/PTO	*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	15/080,432
	Filing Date	03/24/2016
	First Named Inventor	Yannis Tsividis
	Group Art Unit	
	Examiner Name	
Sheet 5 of 5	Attorney Docket No: 10037P007CC2	

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	**Cite No [1]**	**Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.**	**T[2]**
		ZARGARI, MASOUD , et al., "A Single-Chip Dual-Band Tri-Mode CMOS Transceiver for IEEE 802.11a/b/g WLAN", 2004 IEEE International Solid-State Circuits Conference, (2004), Pgs. 96-97	

EXAMINER **DATE CONSIDERED**

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449) as modified by BSTZ 03/26/07

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional) [2] Applicant is to place a check mark here if English language Translation is attached

Electronic Patent Application Fee Transmittal

Application Number:	15080432
Filing Date:	24-Mar-2016
Title of Invention:	Power Dissipation Reduction in Wireless Transceivers
First Named Inventor/Applicant Name:	Yannis Tsividis
Filer:	Roger W. Blakely/Jessica Clark
Attorney Docket Number:	10037P007CC2

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Independent Claims in Excess of 3	2201	1	210	210
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**210**

Electronic Acknowledgement Receipt

EFS ID:	25545239
Application Number:	15080432
International Application Number:	
Confirmation Number:	6094
Title of Invention:	Power Dissipation Reduction in Wireless Transceivers
First Named Inventor/Applicant Name:	Yannis Tsividis
Customer Number:	8791
Filer:	Roger W. Blakely/Jessica Clark
Filer Authorized By:	Roger W. Blakely
Attorney Docket Number:	10037P007CC2
Receipt Date:	20-APR-2016
Filing Date:	24-MAR-2016
Time Stamp:	14:17:51
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$210
RAM confirmation Number	590
Deposit Account	022666
Authorized User	BLAKELY JR., ROGER W.

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 CFR 1.16 (National application filing, search, and examination fees)

Charge any Additional Fees required under 37 CFR 1.17 (Patent application and reexamination processing fees)

Charge any Additional Fees required under 37 CFR 1.19 (Document supply fees)

Charge any Additional Fees required under 37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		10037P007CC2_20160420_PrelimAmd.pdf	361619 9d57a93a2e0396a0214638e61c682735a82b25cf	yes	12

Multipart Description/PDF files in .zip description

Document Description	Start	End
Preliminary Amendment	1	1
Specification	2	2
Abstract	3	3
Claims	4	9
Applicant Arguments/Remarks Made in an Amendment	10	11
Authorization for Extension of Time all replies	12	12

Warnings:

Information:

2	Transmittal Letter	10037P007CC2_20160420_NotCopendingApp.pdf	26711 28ef2a37e634efbb668522dd998823b12a58788f	no	1

Warnings:

Information:

3	Transmittal Letter	10037P007CC2_20160420_IDSLetter.pdf	69174 3d34260c9d82fd91dd242778d62cdc478a7605b8	no	1

Warnings:

Information:

4	Information Disclosure Statement (IDS) Form (SB08)	10037P007CC2_20160420_IDS.pdf	63424 3c710f7f9e70b3b7e398c1b473f2d3c304a79489	no	5

Warnings:

Information:

This is not an USPTO supplied IDS fillable form

5	Fee Worksheet (SB06)	fee-info.pdf	30460 6dbde6ea64f69e11b163bff26b25eeff1c2b5819	no	2

Warnings:	
Information:	
Total Files Size (in bytes):	551388

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 15/080,432	Filing Date 03/24/2016	☐ To be Mailed

ENTITY: ☐ LARGE ☒ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	04/20/2016	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 18	Minus	** 20	= 0	X $40 =	0
	Independent (37 CFR 1.16(h))	* 5	Minus	***5	= 0	X $210 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
SHERRY DAVIS

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/080,432	03/24/2016	Yannis Tsividis	10037P007CC2

CONFIRMATION NO. 6094

8791
BLAKELY SOKOLOFF TAYLOR & ZAFMAN
1279 Oakmead Parkway
Sunnyvale, CA 94085-4040

PUBLICATION NOTICE

OC000000084531501

Title: Power Dissipation Reduction in Wireless Transceivers

Publication No.US-2016-0212701-A1
Publication Date:07/21/2016

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently http://pair.uspto.gov/. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/080,432	03/24/2016	Yannis Tsividis	10037P007CC2	6094

8791 7590 11/01/2016

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
1279 Oakmead Parkway
Sunnyvale, CA 94085-4040

EXAMINER
VUONG, QUOCHIEN B

ART UNIT	PAPER NUMBER
2647	

MAIL DATE	DELIVERY MODE
11/01/2016	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 15/080,432	Applicant(s) TSIVIDIS, YANNIS	
	Examiner QUOCHIEN B. VUONG	Art Unit 2647	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04/20/2016*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-18* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-18* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *03/24/2016* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

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The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 04/20/2016 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112(a):

> (a) IN GENERAL.—The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor or joint inventor of carrying out the invention.

The following is a quotation of the first paragraph of pre-AIA 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1, 2, 12, 13 and 18 are rejected under 35 U.S.C. 112(a) or 35 U.S.C. 112 (pre-AIA), first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor or

a joint inventor, or for pre-AIA the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claims 1 and 2 recite "*wherein the variably scaling includes varying the bias current of the component in the receiver circuit through a plurality of values, responsive to the strength of the desired signal relative to the strength of the interferer signal, where the plurality of values is greater than or equal to three in number*." in claim 1, lines 14-17, which was not described in the specification.

Claims 12 and 13 recite "*switching the impedance of the component in the receiver circuit through a plurality of three or more levels between a high level and a low level responsive to the strength of the interferer signal present in the received RF input signal*", in claim 12, lines 13-15, which was not described in the specification.

Claim 18, recites "adjusting a gain and an impedance of the signal path of the receiver through a plurality of more than two levels responsive to the determined strength of the interferer signal;" in claim 18, lines 9-10, which was not described in the specification.

The following is a quotation of 35 U.S.C. 112(b):
(b) CONCLUSION.—The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention.

The following is a quotation of 35 U.S.C. 112 (pre-AIA), second paragraph:
The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 18 is rejected under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor, or for pre-AIA the applicant regards as the invention.

Claim 18 recites the limitation "*the transceiver*" in claim 18, line 3. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of pre-AIA 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 14 is rejected under pre-AIA 35 U.S.C. 102(b) as being anticipated by Clark (US 5,001,776).

Regarding claim 1, Clark (figure 1) discloses a method of controlling power dissipation in a receiver circuit within a battery powered mobile device when the receiver circuit is receiving and processing an RF input signal in a signal path of the receiver circuit that includes a desired signal and an interferer signal, the method comprising: determining a strength of the interferer signal present in the received RF input signal; causing a decrease in power dissipation of the signal path of the receiver circuit resulting in a decrease in drain on battery life, by variably scaling a gain of a component in the signal path of the receiver circuit upon determination that the strength

of the interferer signal has decreased; causing an increase in power dissipation of the signal path of the receiver circuit resulting in an increase in drain on battery life, by variably scaling the gain of the component in the signal path of the receiver circuit upon determination that the strength of the interferer signal has increased; causing an increase in power dissipation of the signal path of the receiver circuit resulting in an increase in drain on battery life, by variably scaling the gain of the component in the signal path of the receiver circuit upon determination that the strength of the interferer signal has increased; wherein the variable scaling includes: setting the gain of the component in the signal path of the receiver circuit in between a high level and a low level; and adjusting the gain of the component in the signal path of the receiver circuit up or down (column 2, line 34 – column 4, line 66).

Claim Rejections - 35 USC § 103

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-13 and 15-18 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Clark in view of Leifso et al. (US 6,870,425).

Regarding claim 1, Clark (figure 1) discloses a method of power dissipation control in a receiver circuit within a battery powered mobile device when the receiver circuit is receiving and processing an RF input signal that includes a desired signal and

an interferer signal, the method comprising: determining a strength of the desired signal with respect to the strength of the interferer signal; causing a variable decrease in power dissipation of a signal path within the receiver circuit and a resultant decreased battery drain, by variably scaling a gain of a component in the receiver circuit upon determination that the strength of the desired signal has increased relative to the strength of the interferer signal; causing a variable increase in power dissipation of the signal path within the receiver circuit and a resultant increased battery drain, by variably scaling the gain of the component in the receiver circuit upon determination that the strength of the desired signal has decreased relative to the strength of the interferer signal; wherein the variably scaling includes varying the gain of the component in the receiver circuit through a plurality of values, responsive to the strength of the desired signal relative to the strength of the interferer signal (column 2, line 34 - column 4, line 66). Clark does not specifically disclose variably scaling a bias current of a component in the receiver circuit upon determination that the strength of the desired signal has increased relative to the strength of the interferer signal; causing a variable increase in power dissipation of the signal path within the receiver circuit and a resultant increased battery drain, by variably scaling the bias current of the component in the receiver circuit upon determination that the strength of the desired signal has decreased relative to the strength of the interferer signal; wherein the variably scaling includes varying the bias current of the component in the receiver circuit through a plurality of values, responsive to the strength of the desired signal relative to the strength of the interferer signal, where the plurality of values is greater than or equal to three in number. However,

Leifso disclose varying a gain of an amplifier by variably scaling a bias with a plurality of values greater than or equal to three in number (see claim 17; selected from the group of Rd~(1-i), Rd~1/i and Rd~(1-i)/i)). Therefore, it would have been obvious for one having ordinary skill in the art at the time the invention was made to adapt the teaching of varying the gain of the amplifier by varying the scaling bias of Leifso et al. to the method of Clark as a system design preference for performing the same function as controlling and adjusting the gain of the amplifier; and the plurality of values greater than or equal to three to the method of Clark to have more choice and control of the gain of the amplifier.

Regarding claim 2, Leifso et al. disclose wherein the bias current of the component in the receiver circuit is reduced by switching an impedance that appears across a voltage thereby changing the bias current (see claim 17).

Regarding claim 3, Clark (figure 1) discloses a method of power dissipation control in a receiver circuit within a battery powered mobile device when the receiver circuit is receiving an RF input signal that includes a desired signal and an interferer signal, the method comprising: determining a strength of the desired signal with respect to the interferer signal, wherein the receiver circuit comprises a defined signal path between the RF input signal and a processed signal output; causing a variable decrease in power dissipation of the defined signal path within the receiver circuit and a resultant decreased battery drain, by variably scaling a gain of a component in the receiver circuit upon determination that the strength of the desired signal has increased relative to the strength of the interferer signal; and causing a variable increase in power

dissipation of the defined signal path within the receiver circuit and a resultant increased battery drain, by variably scaling the gain of the component in the receiver circuit upon determination that the strength of the desired signal has decreased relative to the strength of the interferer signal; wherein the variable scaling includes: setting the gain of the component in the receiver circuit in between a high level and a low level; adjusting the gain of the component in the receiver circuit up or down; and wherein the variable scaling occurs while the receiver circuit is processing signals received from the RF input signal (column 2, line 34 - column 4, line 66). Clark does not specifically disclose variably scaling an impedance of a component in the receiver circuit upon determination that the strength of the desired signal has increased relative to the strength of the interferer signal; and causing a variable increase in power dissipation of the defined signal path within the receiver circuit and a resultant increased battery drain, by variably scaling the impedance of the component in the receiver circuit upon determination that the strength of the desired signal has decreased relative to the strength of the interferer signal; wherein the variable scaling includes: setting the impedance of the component in the receiver circuit in between a high level and a low level; adjusting the impedance of the component in the receiver circuit up or down. However, Leifso disclose varying a gain of an amplifier by variably scaling an impedance (see claim 17). Therefore, it would have been obvious for one having ordinary skill in the art at the time the invention was made to adapt the teaching of varying the gain of the amplifier by variably scaling the impedance of Leifso et al. to the method of Clark as a system design preference for performing the same function as controlling and adjusting the gain of the amplifier.

Regarding claim 4, Clark discloses wherein variably scaling the impedance of a component in the receiver circuit comprises variably scaling an impedance of a low noise amplifier (LNA) (figure 1, amplifier 108).

Regarding claim 5, Clark discloses wherein variably scaling the impedance of a component in the receiver circuit comprises variably scaling an impedance of a mixer (figure 1, mixer 110).

Regarding claim 6, Clark discloses wherein the circuit in the signal path whose gain or impedance is varied can be other parameters or component and would obviously including a filter (120) (column 4, lines 30-43).

Regarding claim 7, Leifso et al. disclose wherein the impedance of a component in the receiver circuit comprises a resistance, and wherein a value of the resistance is increased by opening switches across one or more portions of the resistance (see claim 17).

Regarding claim 8, Clark (figure 1) discloses wherein the defined signal path includes components that comprise: a low noise amplifier (LNA) (108), a filter (120), a mixer (110).

Regarding claim 9, Clark disclose wherein the component is a low noise amplifier (108),

Regarding claim 10, Clark disclose wherein the component is a filter (120).

Regarding claim 11, Clark disclose wherein the component is a mixer (110).

Regarding claim 12, Clark (figure 1) discloses a method of power dissipation control in a receiver circuit within a battery powered mobile device when the receiver

circuit is receiving an RF input signal that includes a desired signal and an interferer signal, the method comprising: determining a strength of the interferer signal present in the received RF input signal; causing a variable decrease in power dissipation of a signal path within the receiver circuit and a resultant decreased battery drain, by variably scaling an impedance of a component in the receiver circuit upon determination that the strength of the interferer signal has decreased; causing a variable increase in power dissipation of the signal path within the receiver circuit and the resultant decreased battery drain, by variably scaling a gain of the component in the receiver circuit upon determination that the strength of the interferer signal has increased; wherein the variable scaling includes: switching the gain of the component in the receiver circuit through a plurality of levels between a high level and a low level responsive to the strength of the interferer signal present in the received RF input signal; and wherein the variable scaling occurs while the receiver circuit is processing signals received from the RF input signal (column 2, line 34 - column 4, line 66). Clark does not specifically disclose variably scaling an impedance of a component in the receiver circuit upon determination that the strength of the interferer signal has decreased; causing a variable increase in power dissipation of the signal path within the receiver circuit and the resultant decreased battery drain, by variably scaling the impedance of the component in the receiver circuit upon determination that the strength of the interferer signal has increased; wherein the variable scaling includes: switching the impedance of the component in the receiver circuit through a plurality of three or more levels between a high level and a low level responsive to the strength of the

interferer signal present in the received RF input signal. However, Leifso disclose varying a gain of an amplifier by variably scaling an impedance with a plurality of three or more levels (see claim 17; selected from the group of Rd~(1-i), Rd~1/i and Rd~(1-i)/i)). Therefore, it would have been obvious for one having ordinary skill in the art at the time the invention was made to adapt the teaching of varying the gain of the amplifier by varying the scaling impedance of Leifso et al. to the method of Clark as a system design preference for performing the same function as controlling and adjusting the gain of the amplifier; and the plurality of three or more levels to the method of Clark to have more choice and control of the gain of the amplifier.

Regarding claim 13, Leifso et al. disclose wherein the impedance of the component in the receiver circuit comprises a resistance, and wherein the value of the resistance may be increased by opening switches across one or more portions of the resistance (see claim 17).

Regarding claim 15, Clark does not disclose wherein the gain of the component in the signal path of the receiver circuit is varied by increasing a current in a differential pair and /or increasing a load resistance using switches. However, Leifso et al. disclose changing the gain by changing a current and/or changing a load resistance (claim 17). Therefore, it would have been obvious for one having ordinary skill in the art at the time the invention was made to adapt the teaching of varying the gain of the amplifier by varying the current in a differential pair and /or increasing a load resistance of Leifso et al. to the method of Clark as a system design preference for performing the same function as controlling and adjusting the gain of the amplifier.

Regarding claim 16, Clark (figure 1) discloses a mobile communications device, comprising: a receiver circuit for receiving an RF input signal that includes a desired signal and an interferer signal; a battery that powers the mobile communications device including the receiver circuit; wherein a strength of the desired signal is determined with respect to the strength of the interferer signal; wherein a variable decrease in power dissipation of a signal path within the receiver circuit and a resultant decreased battery drain is caused by variably scaling an impedance of a component in the receiver circuit upon determination that the strength of the desired signal has increased relative to the strength of the interferer signal; and wherein a variable increase in power dissipation of the signal path within the receiver circuit and a resultant increased battery drain, is caused by variably scaling a gain of the component in the receiver circuit upon determination that the strength of the desired signal has decreased relative to the strength of the interferer signal; and wherein the variable scaling includes: setting the gain of the component in the receiver circuit in between a high level and a low level; and adjusting the gain of the component in the receiver circuit up or down; and wherein the variable scaling occurs while the receiver circuit is processing signals received from the RF input signal (column 2, line 34 - column 4, line 66). Clark does not specifically disclose variably scaling the impedance of the component in the receiver circuit upon determination that the strength of the desired signal has decreased relative to the strength of the interferer signal; and wherein the variable scaling includes: setting the impedance of the component in the receiver circuit in between a high level and a low level; and adjusting the impedance of the component in the receiver circuit up or down.

However, Leifso disclose varying a gain of an amplifier by variably scaling an impedance (see claim 17). Therefore, it would have been obvious for one having ordinary skill in the art at the time the invention was made to adapt the teaching of varying the gain of the amplifier by varying the impedance of Leifso et al. to the method of Clark as a system design preference for performing the same function as controlling and adjusting the gain of the amplifier.

Regarding claim 17, Leifso et al. disclose wherein the impedance of the component in the receiver circuit comprises a resistance, and wherein a value of the resistance may be varied by opening and closing switches across one or more portions of the resistance responsive to the determined strength of the desired signal with respect to the interferer signal (see claim 17).

Regarding claim 18, Clark (figure 1) disclose a method for conserving battery power in a mobile communication device, the method comprising: receiving a radio signal by a radio receiver, of the transceiver, that include a desired signal and an interferer signal; powering to the radio transceiver by a battery; processing of the received radio signals in a signal path within the radio receiver; determining the strength of the interferer signal by a circuit coupled to the signal path of the receiver; adjusting a gain of the signal path of the receiver through a plurality of levels responsive to the determined strength of the interferer signal; where in adjusting the gain of the signal path result in improving a power drain from the battery (column 2, line 34 - column 4, line 66). Clark does not specifically disclose adjusting an impedance of the signal path of the receiver through a plurality of more than two levels responsive to the determined

strength of the interferer signal. However, Leifso et al. disclose adjusting an impedance of the signal path of the receiver through a plurality of more than two levels (see claim 17; selected from the group of Rd~(1-i), Rd~1/i and Rd~(1-i)/i)). Therefore, it would have been obvious for one having ordinary skill in the art at the time the invention was made to adapt the teaching of adjusting the impedance of Leifso et al. to the method of Clark as a system design preference for performing the same function as controlling and adjusting the gain of the amplifier; and the plurality of more than two levels to the method of Clark to have more choice and control of the gain of the amplifier.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the “right to exclude” granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on nonstatutory double patenting provided the reference application or patent either is shown to be commonly owned with the examined application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. See MPEP § 717.02 for applications subject to examination under the first inventor to file provisions of the AIA as explained in MPEP § 2159. See MPEP §§ 706.02(l)(1) - 706.02(l)(3) for applications not subject to examination under the first inventor to file provisions of the AIA. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO Internet website contains terminal disclaimer forms which may be used. Please visit www.uspto.gov/patent/patents-forms. The filing date of the application in which the form is filed determines what form (e.g., PTO/SB/25, PTO/SB/26, PTO/AIA/25, or PTO/AIA/26) should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.

Claims 1-18 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-30 of U.S. Patent No. 7,010,330. Although the claims at issue are not identical, they are not patentably distinct from each other because claims 1-18 of the present application merely broaden the scope of claims 1-30 of the U.S.

Patent No. 7,010,330. This type of broadening is known to be obvious in a way that could unduly extend patent rights and cause potential conflicts in ownership as the narrow claims would be covered by the scope of the broad claim. Therefore, double patenting exists between the applications and a terminal disclaimer must be required in each and every case where double patenting exists.

Claims 1-18 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-8 of U.S. Patent No. 9,331,728. Although the claims at issue are not identical, they are not patentably distinct from each other because claims 1-18 of the present application merely broaden the scope of claims 1-8 of the U.S. Patent No. 9,331,728. This type of broadening is known to be obvious in a way that could unduly extend patent rights and cause potential conflicts in ownership as the narrow claims would be covered by the scope of the broad claim. Therefore, double patenting exists between the applications and a terminal disclaimer must be required in each and every case where double patenting exists.

Claim 1-18 are provisionally rejected on the ground of nonstatutory double patenting as being unpatentable over claim 1-18 of copending Application No. 15/080,432 (reference application). Although the claims at issue are not identical, they are not patentably distinct from each other because both are drawn to the same invention of a method of controlling a battery power consumption of a transceiver.

Although the claims at issue are not identical, they are not patentably distinct from each other. Therefore, double patenting exists between the applications and a

terminal disclaimer must be required in each and every case where double patenting exists.

This is a provisional nonstatutory double patenting rejection because the patentably indistinct claims have not in fact been patented.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to QUOCHIEN B. VUONG whose telephone number is (571)272-7902. The examiner can normally be reached on M-F 9:30-18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nay Maung can be reached on (571) 272-7882. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/QUOCHIEN B VUONG/
Primary Examiner, Art Unit 2647

Notice of References Cited	Application/Control No. 15/080,432	Applicant(s)/Patent Under Reexamination TSIVIDIS, YANNIS	
	Examiner QUOCHIEN B. VUONG	Art Unit 2647	Page 1 of 1

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*	B	US-6,870,425 B2	03-2005	Leifso; Curtis R.	H03F3/45085	330/254
	C	US-				
	D	US-				
	E	US-				
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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BIB DATA SHEET

CONFIRMATION NO. 6094

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
15/080,432	03/24/2016	455	2647	10037P007CC2

APPLICANTS
Theta IP, LLC, Coppell, TX;

INVENTORS
Yannis Tsividis, New York, NY;

**** CONTINUING DATA ***************************
This application is a CON of 11/318,646 12/27/2005 PAT 9331728
which is a CON of 10/784,613 02/23/2004 PAT 7010330
which claims benefit of 60/451,229 03/01/2003
and claims benefit of 60/451,230 03/01/2003

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED **** ** SMALL ENTITY **
04/07/2016

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /QUOCHIEN B VUONG/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		NY	15	17	5

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1279 Oakmead Parkway
Sunnyvale, CA 94085-4040
UNITED STATES

TITLE
Power Dissipation Reduction in Wireless Transceivers

FILING FEE RECEIVED		
1360	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15080432	TSIVIDIS, YANNIS
	Examiner	Art Unit
	QUOCHIEN B VUONG	2647

CPC- SEARCHED		
Symbol	Date	Examiner
H04B 1/04, 1/16, 1/40, 1/109, 1/0457, 1/1607, 17/309, 17/318, 17/336,17/345, 2001/045, 2001/0416	10/27/2016	/QV/
H04W 52/52, 52/0261, 88/02	10/27/2016	/QV/
H03G 3/004, 3/20	10/27/2016	/QV/

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
455	63.1,67.13,127.1,127.2,127.5,226.1,226.2,232.1,234.1,250.1,251.1,295,296,343.1,572,574	10/27/2016	/QV/
370	442	10/27/2016	/QV/
330	127,134,144	10/27/2016	/QV/

SEARCH NOTES		
Search Notes	Date	Examiner
EAST search	10/27/2016	/QV/
Inventor name search	10/27/2016	/QV/

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15080432	TSIVIDIS, YANNIS
	Examiner	Art Unit
	QUOCHIEN B VUONG	2647

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	10/28/2016								
	1	✓								
	2	✓								
	3	✓								
	4	✓								
	5	✓								
	6	✓								
	7	✓								
	8	✓								
	9	✓								
	10	✓								
	11	✓								
	12	✓								
	13	✓								
	14	✓								
	15	✓								
	16	✓								
	17	✓								
	18	✓								

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	8	"9331728".pn. "7010330".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/10/27 16:42
L2	8	"5001776".pn. "6933779".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/10/27 17:18
L3	545702	(RSSI (signal adj (strength level quality)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/10/27 17:24
L4	4381	3 same ((chang$3 varr$4 adjust$3 increas$3) with impedance)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/10/27 17:32
L5	32589	455/63,1,67.13,127.1,127.2,127.5,226.1,226.2,232.1,234.1,250.1,251.1,295,296,311,343.1,572,574.ccls. 370/442.ccls. 330/127,134,144.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/10/27 17:35
L6	177	4 and 5	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/10/27 17:40
L7	2056	3 same ((bias near4 current) gain) same ((lower less reduc$3) near4 (power battery))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/10/27 18:09
L8	316	7 and 5	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/10/27 18:12
L9	23	6 AND ((H03G3/004 OR H03G3/20 OR H04B2001/0416 OR H04B17/318 OR H04B1/04 OR H04B1/1607 OR H04B17/309 OR H04B1/16 OR H04W88/02 OR H04W52/0261 OR H04W52/52).CPC.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/10/27 18:40
L10	124	8 AND ((H03G3/20 OR H04B1/109 OR H04B17/318 OR H04B2001/0416 OR H04B17/336 OR H04B17/345 OR H04B1/40 OR H04B17/309 OR H04B1/1607 OR H04B1/04 OR H04B1/0475 OR H04B1/06 OR H04B1/16 OR H04B2001/045 OR H04W52/52 OR H04W52/0261 OR H04W88/02).CPC.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/10/27 19:05
L11	121	tsividis-yannis.in.	US-PGPUB; USPAT; USOCR;	OR	ON	2016/10/27 19:34

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			FPRS; EPO; JPO; DERWENT; IBM_TDB				

EAST Search History (Interference)

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /Q.B.V/

Substitute for form 1449A/PTO	Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	15/080,432
	Filing Date	03/24/2016
	First Named Inventor	Yannis Tsividis
	Group Art Unit	2647
	Examiner Name	Quochien Vuong
Sheet 1 of 5	Attorney Docket No: 10037P007CC2	

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Examiner Initial *	**Cite No [1]**	**USP Document Number**	**Publication or Issue Date MM-DD-YYYY**	**Name of Patentee or Applicant of cited Document**	**Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear**
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EXAMINER /QUOCHIEN B VUONG/ **DATE CONSIDERED** 10/27/2016

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449) as modified by BSTZ 03/26/07
* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional) [2] Applicant is to place a check mark here if English language Translation is attached

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Substitute for form 1449A/PTO	*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	15/080,432
	Filing Date	03/24/2016
	First Named Inventor	Yannis Tsividis
	Group Art Unit	2647
	Examiner Name	Quochien Vuong
Sheet 2 of 5	Attorney Docket No: 10037P007CC2	

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Sheet 3 of 5	Attorney Docket No: 10037P007CC2	

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Sheet 4 of 5	Attorney Docket No: 10037P007CC2	

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	First Named Inventor	Yannis Tsividis
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	Examiner Name	Quochien Vuong
Sheet 5 of 5	Attorney Docket No: 10037P007CC2	

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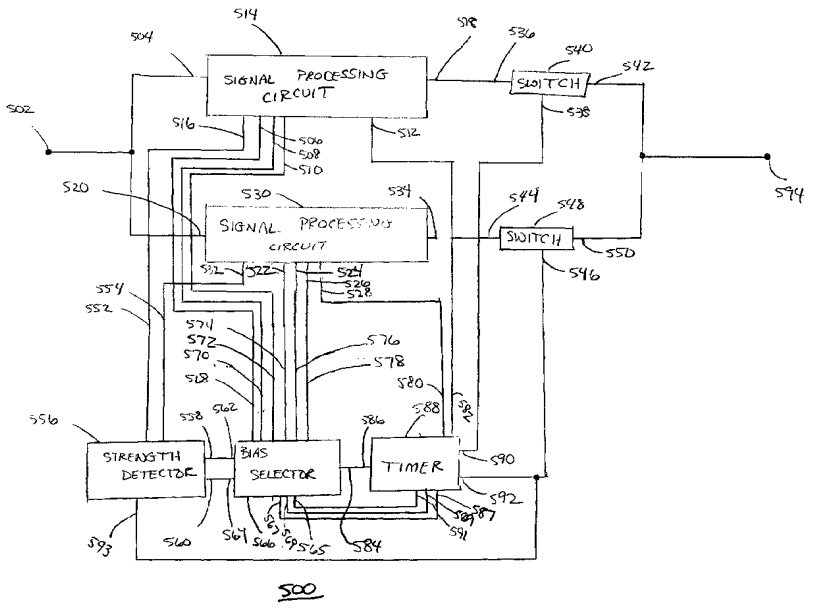
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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: CIRCUIT AND METHOD FOR DYNAMICALLY MODIFIABLE SIGNAL PROCESSOR



(57) Abstract: Techniques are provided for the implementation of a signal processing circuit which expands the dynamic range of the signal processing circuit without interrupting the output of the circuit. The technique can receive an input signal (502) process the signal through one (514) of a plurality of signal processing circuits, and switch to processing the signal through another (530) of the plurality of signal processing circuits without disturbing the output of the system.

WO 2004/017589 A1

CIRCUIT AND METHOD FOR DYNAMICALLY MODIFIABLE SIGNAL PROCESSOR

SPECIFICATION

This application claims priority to U.S. Provisional Application Serial Number 60/222,429 filed August 1, 2000, U.S. Provisional Application Serial Number 60/237,312 filed October 2, 2000, U.S. Provisional Application Serial Number 60/260,722 filed January 10, 2001, and U.S. Provisional Application Serial Number 60/288,976 filed May 4, 2001, each of which is incorporated by reference herein in its entirety.

BACKGROUND OF THE INVENTION

The present invention relates to signal processors and, more particularly, to signal processors that are dynamically modifiable for optimal performance and reduced power dissipation.

In order to expand the dynamic range of a signal processing system, companding signal processors can be used. A companding signal processor uses an input amplifier to amplify or attenuate a signal before it is provided to the signal processor, and an output amplifier is used to amplify or attenuate the signal provided by the signal processor. The gain of the output amplifier is the inverse of the gain of the input amplifier, thus conserving the linearity of the signal processor. Ideally, the gains of the input amplifier and output amplifier can be varied dynamically. A signal strength detector can be used to measure the strength of the input signal and provide a corresponding gain control signal. Y. Tsividis, "Externally linear, time-invariant systems and their application to companding signal processors," IEEE Transactions on Circuits and Systems II, Vol. 44, No. 2, February 1997. The gain signal sets the amplification factors of the input amplifier and the output amplifier. However, this approach has the problem in that because the signal processor has memory, distortion in the output of the signal processor occurs whenever the amplification factors of the input amplifier and the output amplifier are changed.

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The analog floating point technique addresses the problem of distortion in the output whenever the amplification factors change. E. Blumenkrantz, "The analog floating point technique," Proc. IEEE Symposium on Low Power Electronics, p. 72-73, 1995. This technique avoids distortion by altering the state variables of the signal processor when the amplification factors change. However, implementation of the analog floating point technique is complicated to implement, and is sensitive to parasitics and component mismatch. Accordingly, there is a need for circuits which expand the dynamic range of a signal processor without interrupting the output of the system or causing distortion.

SUMMARY OF THE INVENTION

It is therefore an object of this invention to provide a circuit which has a large dynamic range and which operates in an energy-efficient manner without interrupting the output of the circuit or causing distortion.

In accordance with the present invention, there is provided a signal processing system having a system input for receiving an input signal having an in-band component and an out-band component, and a system output for providing a system output signal. The system further includes a plurality of signal processing circuits each having an input coupled to the system input and an output for providing a respective output signal, each one of the signal processing circuits being adapted for optimal processing of input signals over a different range of in-band component to out-band component ratios. Also included are a plurality of switches each having a switch input coupled to the output of a respective one of the signal processing circuits, a switch output connected to the system output and a switch control input responsive to a first switch control signal for connecting the switch input to the switch output and responsive to a second switch control signal for disconnecting the switch input from the switch output. Finally, there is provided a signal strength detector having at least one input each coupled to the output of a preselected one of the signal processing circuits and a plurality of outputs each coupled to the switch control input of a respective one of the plurality of switches. The signal strength detector is responsive to a comparison of the strength of the output signal of each one of the signal processing circuits having an output coupled to the at least one input of the signal

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strength detector with at least one limit for selecting a particular one of the signal processing circuits and for providing a first switch control signal to the switch control input of the switch having its switch input coupled to the output of the particular one of the signal processing circuit. The signal strength detector providing the second switch control signal to the switch control input of each one of the switches having its switch input coupled to the output of a respective one of the signal processing circuits not selected by the signal strength detector.

According to another embodiment of the invention, there is provided a signal processing system having a system input for receiving an input signal and a system output for providing a system output signal, and a plurality of signal processing circuits each having an input coupled to the system input and an output for providing a respective output signal. Each signal processor having a different saturation level and a different signal-to-noise ratio. Also included are a plurality of switches each having a switch input coupled to the output of a respective one of the signal processing circuits, a switch output coupled to the system output, and a switch control input responsive to a first switch control signal for connecting the switch input to the switch output and responsive to a second switch control signal for disconnecting the switch input from the switch output. Finally there is provided a signal strength detector having an input coupled to the system input and a plurality of outputs each corresponding to a respective one of the signal processing circuits. The signal strengh detector is responsive to a comparison of the strength of the input signal received at the system input with at least one limit for selecting a particular one of the signal processing circuits having a respective saturation level and a respective signal-to-noise ratio suitable or processing the input signal and for providing the first switch control signal to the switch control input of a respective one of the plurality of switches having its switch input coupled to the output of the selected one of the signal processing circuits and for providing the second switch control signal to the switch control inputs of respective ones of the switches having the switch input coupled to the output of respective ones of the signal processing circuits not selected by the signal strength detector.

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According to another embodiment of the present invention, there is provided a signal processing system having a system input for receiving an input signal, a system output for providing a system output signal, and a first and second signal processing circuit each having an input, an output, a power control input responsive to a first power control signal for causing the signal processing circuit to be in a powered up state and responsive to a second power control signal for causing the signal processing circuit to be in a powered down state, and at least one bias control input responsive to at least one bias control signal for biasing the signal processing circuit for optimal processing of the signal having a respective signal strength. Also provided are a plurality of output switches each having a switch input connected to the output of a respective one of the first and second signal processing circuits, a switch output coupled to the system output and a switch control input responsive to the first switch control signal for connecting the switch input to the switch output and being responsive to a second switch control signal for disconnecting the switch input from the switch output. At any given time one of the first or second signal processing circuits is active by being in a powered up state, receiving at least one bias control signal at its at least one bias control input and having its output connected to the system output by a respective one of the output switches, and the other one of the first and second signal processing circuits is inactive by being in a powered down state and having its output disconnected from the system output by a respective one of the output switches. Also provided is a signal strength detector having a first and second input connected to respective internal nodes of the first and second signal processing circuits and at least one input for specifying at least one bias control signal, if any, to be applied to the at least one bias control input of the inactive one of the signal processing circuits. The signal strength detector is responsive to a comparison of the strength of a signal on the respective internal node of an inactive one of the signal processing circuits with at least one limit for determining whether at least one bias control signal is to be applied to the at least one bias control input of the inactive one of the signal processing circuits for changing the bias thereto and for providing on the at least one output at least one signal specifying, if any, the at least one bias control signal to be applied to

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the bias control input an inactive one of the signal processing circuits. There is further provided a bias selector responsive to the at least one output signal provided on the at least one output of the signal strength detector for providing on at least one first output the at least one bias control signal specified by the at least one signal on the at least one output of the signal strength detector to the at least one bias control input of the inactive one of the signal processing circuits and providing on a second output a signal indicating that at least one bias control signal has been applied to the inactive one of the signal processing circuits. Finally there is included a timer circuit responsive to the signal on the second output of the bias selector circuit for providing the first power control signal to the power control input of the inactive one of the signal processing circuits, and after a predetermined delay for applying the first switch control signal to the switch control input of the switch having its input coupled to the output of the inactive one of the signal processing circuits and applying the second switch control signal to the switch control input of the switch having its switch input connected to the output of the active one of the signal processing circuits and applying the second power control signal to the power control input of the active one of the signal processing circuits. According to a further embodiment of the present invention, there is provided a signal processing system having a system input for receiving an input signal having an in-band component and an out-band component, and a system output for providing a system output signal. The system further includes a plurality of signal processing circuits each having an input coupled to the system output, an output for providing a respective output signal and a power control input responsive to a first power control signal for causing the signal processing circuit to be in a powered up state and responsive to a second power control signal for causing the signal processing circuit to be in a powered down state, each one of the plurality of signal processing circuits being adapted to have a different saturation level and signal-to-noise ratio for optimal processing of signals having a different range of in-band component to out-band component ratios. Also provided is a plurality of output switches each one having an input coupled to the output of a respective one of the plurality of signal processing circuits, an output connected to the system output and a switch control input responsive to a first switch control signal for connecting the input

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of the switch to the output of the switch and responsive to the a second switch control signal for disconnecting the input of the switch from the output of the switch. Also provided are a plurality of output switches each one having an input coupled to the output of a respective one of the plurality of signal processing circuits, an output connected to the system output and a switch control input responsive to a first switch control signal for connecting the input of the switch to the output of the switch and responsive to a second switch control signal for disconnecting the input of the switch from the output of the switch. In addition, the system includes a signal strength detector having a first input connected to the system output, at least one output for providing a signal indicating a selective one of the plurality of signal processing circuits. The signal strength detector is responsive to the comparison of the strength of an output signal with at least one limit for selecting one of the plurality of signal processing circuits for processing the input signal and providing at least one signal on the at least one output indicating the signal processing circuit selected by the signal strength detector. Finally there is included a timer circuit having at least one input each coupled to a respective one of at least one output of the signal strength detector and a first plurality of outputs each one connected to the power control input of the respecdtive one of the plurality of signal processing circuits and a second plurality of outputs each one connected to the switch control input of a respective one of the plurality of output switches. The timer circuit is responsive to at least one signal provided by the signal strength detector for providing the first power control signal to the power control input of the signal processing circuits selected by the signal strength detector and providing after a predetermined delay the first switch control signal to the switch control input of a respective one of the plurality of output switches having its input connected to the output of the signal processing circuits selected by the signal strength detector to thereby connect the output of the signal processing circuit selected by the signal strength detector to the system output and providing after the predetermined delay the second switch control signal to the switch control input of respective ones of the plurality of output switches each having a switch input connected to the output of a respective one of the plurality of signal processing circuits not selected by the signal processing detector to thereby disconnect the output

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of each one of the signal processing circuits not selected by the signal strength detector from the system output. The timer circuit is responsive to at least one signal provided by the signal strength detector for providing at least the predetermined delay the second power control signal to the power control input of each one of the plurality of signal processing circuits not selected by the signal strength detector. According to another aspect of the present invention, there is provided a method for processing an input signal received by a system input to derive an output signal at a system output. The method includes providiing a plurality of signal processors each having an input coupled to the system output and an output. Each one of the signal processors is adapted to process an input signal having a different range of in-band component to out-band component ratios without saturating and without having a signal-to-noise ratio approaching one. The method further includes providing a plurality of switches, each one for controllably connecting and disconnecting the output of a respective one of the signal processors to the system output terminal. The method also includes detecting the strength of the respective output signal at each one of at least one selected output of the signal processors to compare the strength of the respective output signal with at least one limit to select one of the signal processors for optimal processing of the input signal. Finally, the method includes causing a respective one of the switches to connect the output of the selected signal processors to the signal output and causing other ones of the switches to disconnect the outputs of all other signal processors from the system output.

BRIEF DESCRIPTION OF THE DRAWINGS

Further objects, features, and advantages of the invention will become apparent from the following detailed description taken in conjunction with the accompanying figures showing illustrative embodiments of the invention, in which:

Fig. 1 is a block diagram illustrating a prior art signal processing system;

Fig. 2 is a block diagram illustrating a signal processing system in accordance with the present invention;

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Fig. 3 is a block diagram illustrating still another signal processing system in accordance with the present invention;

Fig. 4 is a block diagram illustrating yet another signal processing system in accordance with the present invention;

Fig. 5(a) is a block diagram illustrating a still further signal processing system in accordance with the present invention;

Fig. 5(b) is a block diagram illustrating an additional signal processing system in accordance with the present invention;

Fig. 6 is a block diagram illustrating a further additional signal processing system in accordance with the present invention;

Fig. 7(a) is a block diagram illustrating a first filter bank in accordance with the present invention;

Fig. 7(b) is a block diagram illustrating a second filter bank in accordance with the present invention;

Fig. 7(c) is a block diagram illustrating a third filter bank in accordance with the present invention;

Fig. 8 is a circuit diagram illustrating a Tow-Thomas biquad in accordance with the present invention;

Fig. 9 is a circuit diagram illustrating a transconductor in accordance with the present invention;

Fig. 10 is a circuit diagram illustrating an additional biquad in accordance with the present invention;

Fig. 11 is a circuit diagram illustrating a peak detector and a threshold detector in accordance with the present invention;

Fig. 12(a) is a block diagram illustrating an additional signal strength detector in accordance with the present invention;

Fig. 12(b) is a block diagram illustrating an additional signal strength detector in accordance with the present invention;

Fig. 13 is a circuit diagram illustrating a timer in accordance with the present invention;

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Fig. 14(a) is a block diagram illustrating a further additional signal processing circuit in accordance with the present invention;

Fig. 14(b) is a block diagram illustrating a further additional signal processing circuit in accordance with the present invention;

Fig. 15 is a block diagram illustrating a further additional signal processing circuit in accordance with the present invention;

Fig. 16 is a circuit diagram illustrating a biquad in accordance with the present invention;

Fig. 17 is a circuit diagram illustrating a dynamic input scaling unit in accordance with the present invention;

Fig. 18 is a circuit diagram illustrating a dynamic output scaling unit in accordance with the present invention;

Fig. 19 is a circuit diagram illustrating a portion of a bias selector in accordance with the present invention;

Fig. 20 is a circuit diagram illustrating a portion of a bias selector in accordance with the present invention;

Fig. 21 is a block diagram illustrating a further additional signal strength detector in accordance with the present invention;

Fig. 22 is a circuit diagram illustrating an on-off transconductor in accordance with the present invention.

Throughout the figures, unless otherwise stated, the same reference numerals and characters are used to denote like features, elements, components, or portions of the illustrated embodiments. Moreover, while the subject invention will now be described in detail with reference to the figures, and in connection with the illustrative embodiments, changes and modifications can be made to the described embodiments without departing from the true scope and spirit of the subject invention as defined by the appended claims.

DETAILED DESCRIPTION OF THE INVENTION

Figure 1 illustrates an example of a prior art signal processing system 100. The signal processing system 100 is a companding filter. A companding filter

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amplifies or attenuates an input signal that is applied to a filter circuit, and attenuates or amplifies the output signal from the circuit. The prior art companding filter 100 includes an input 102, a signal strength detector 104, an input variable gain amplifier 106, a main filter 108, an output variable gain amplifier 110, and an output 112.

The input 102 of the signal processing system 100 corresponds to input 101 of the signal strength detector 104 and an input 120 of the input variable gain amplifier 106. The input variable gain amplifier 106 amplifies or attenuates the signal received by the input 120 depending on a gain control input signal received at a gain control input 103 of the input variable gain amplifier 106 and outputs the resultant signal at its output 105. The output 105 of the input variable gain amplifier 106 corresponds to input 107 of the main filter 108. The main filter 108 processes the signal received at the input 107 and produces an output signal at its output 109. The output 109 of the main filter 108 corresponds to input 111 of the output variable gain amplifier 110. The output variable gain amplifier 110 amplifies or attenuates the signal received at the input 111 depending on a gain control signal received at a gain control input 113 of the output variable gain amplifier 110 and outputs the resultant signal at its output 112. The gain of the output variable gain amplifier 110 is the inverse of the gain of the input variable gain amplifier 106. The output 114 of the output variable gain amplifier 110 is connected to the output 112 of the signal processing system 100.

The signal strength detector 104 measures the strength (e.g., the voltage envelope) of the signal applied to the input 101 of the signal strength detector 104 and outputs a gain control signal at its output 115, which is connected to the gain control inputs 103 and 113 of the input variable gain amplifier 106 and the output variable gain amplifier 110, respectively. Depending on the strength of the signal at the input 101 of the signal strength detector 104, different gain control signals are provided at the output 115 of the signal strength detector 104. If the signal applied to the input 101 of the signal strength detector 104 is small, the gain control signal should be large causing the signal applied to the input 102 of the signal processing system 100 to be amplified before it is applied to the main filter 108, such that the signal is large compared to the filter noise, i.e. the noise generated by the filter. If the

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signal applied to the input 101 of the signal strength detector 104 is large, the gain control signal should be small causing the signal applied to the input 102 of the signal processing system 100 to be slightly amplified or even attenuated before it is applied to the signal processing circuit 108 to avoid saturating the main filter 108.

Fig. 2 illustrates an example of a signal processing system 200. The signal processing system 200 generates a processed signal with a strong in channel component well above the filter noise. The signal processing system 200 includes three banks of filters in parallel with each other. The first bank of filters includes a plurality of filters 202, 220, 232, a plurality of amplifiers 214, 226 and a first bank switch 238. The second bank of filters includes a plurality of filters 204, 222, 234, a plurality of amplifiers 216, 228 and a second bank switch 240. The third bank of filters includes a plurality of filters 206, 224, 236, a plurality of amplifiers 218, 230 and a third bank switch 242.

It is noted that a different number of filter banks may be used, and each one of the filter banks may have more or fewer filters and associated amplifiers.

A signal received by the input 201 of the signal processing system 200 , which typically includes an in-band component and an out-band component, is conveyed to an input 203 of the filter 202 of the first filter bank. Preferably, the filter 202 has enough linear range to accommodate the in-band component and the out-band component of the signal without saturating. The filter 202 processes the signal received at its input 203 and outputs a processed signal at its output 209. The output 209 of the filter 202 corresponds to input 215 of the amplifier 214. The amplifier 214 is a fixed gain amplifier, which amplifies the signal received at its input 215 and produces an output signal at its output 221. The output 221 of the amplifier 214 corresponds to input 227 of the filter 220. The filter 220 processes the signal received at its input 227 and outputs a processed signal at its output 233. The output 233 of the filter 220 corresponds to input 239 of the amplifier 226. The amplifier 226 is a fixed gain amplifier, which amplifies the signal it receives at its input 239 and produces an output signal at its output 245. The output 245 of the amplifier 226 corresponds to input 251 of the filter 232. The filter 232 processes the signal received at its input 251 and outputs a processed signal at its output 257. The output 257 of the filter 232

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corresponds to input 263 of the switch 238. An output 275 of the switch 238 is connected to the output 244 of the signal processing system 200.

The signal received by the input 201 of the signal processing system 200 is also conveyed to an input 205 of the filter 204 of the second filter bank. Preferably, the filter 204 has enough linear range to accommodate the in-band component and the out-band component of the signal without saturating. The filter 204 processes the signal received at its input 205 and provides a processed signal at its output 211. The output 211 of the filter 204 corresponds to input 217 of the amplifier 216. The amplifier 216 is a fixed gain amplifier, which amplifies the signal received at its input 217 and produces an amplified signal at its output 223. The output 223 of the amplifier 216 corresponds to input 229 of the filter 222. The filter 222 processes the signal received at its input 229 and outputs a processed signal at its output 235. The output 235 of the filter 222 corresponds to input 241 of the amplifier 228. The amplifier 228 is a fixed gain amplifier, which amplifies the signal received at its input 241 and produces an amplified signal at its output 247. The output 247 of the amplifier 228 corresponds to input 253 of the filter 234. The filter 234 processes the signal received at its input 253 and outputs a processed signal at its output 259. The output 259 of the filter 234 corresponds to input 265 of the switch 240 and to an input 271 of the signal strength detector 208. An output 277 of the switch 240 is connected to the output 244 of the signal processing system 200.

The signal received by the input 201 of the signal processing system 200 is also conveyed to an input 207 of the filter 206 of the third filter bank. Preferably, the filter 206 has enough linear range to accommodate the in-band component and the out-band component of the signal without saturating. The filter 206 processes the signal received at its input 207 and outputs a processed signal at its output 213. The output 213 of the filter 206 corresponds to input 231 of the amplifier 218. The amplifier 218 is a fixed gain amplifier, which amplifies the signal received at its input 219 and produces an amplified signal at its output 225. The output 225 of the amplifier 218 corresponds to input 231 of the filter 224. The filter 224 processes the signal received at its input 231 and provides a processed signal at its output 237. The output 237 of the filter 224 corresponds to input 243 of the amplifier 230. The

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amplifier 230 is a fixed gain amplifier, which amplifies the signal received at its input 243 and produces an amplified signal at its output 249. The output 249 of the amplifier 230 corresponds to input 255 of the filter 236. The filter 236 processes the signal received at its input 255 and outputs a processed signal at its output 261. The output 261 of the filter 236 corresponds to input 267 of the switch 242. The output 279 of the switch 242 is connected to the output 244 of the signal processing system 200.

Preferably, the filters 202, 204, 206 have the same transfer function; the filters 220, 222, 224 have the same transfer function; and the filters 232, 234, 236 have the same transfer function.

Each filter bank should be optimized to effectively process signals with a different in-band component / out-band component ratio. The first filter bank is optimized for input signals having a large out-band component and a relatively small in-band component. The first filter bank is optimized by having the amplifiers 214, 226 have a gain of more than one. Preferably, the amplifiers 214, 226 have gains of ten so that each amplifier provides a signal with ten times the amplitude of the input signal. The second bank is optimized for input signals having an out-band component which is slightly larger than the in-band component. The second filter bank is optimized by having the amplifier 216 have a gain of one, and having the amplifier 228 have a gain greater than one. Preferably, the amplifier 228 has a gain of ten, causing the amplifier 228 to provide a signal at its output 247 with ten times the amplitude of the signal received at its input 241. The third bank is optimized for input signals having an out-band component that is approximately equal to the in-band component. The third filter bank is optimized by having the amplifiers 218, 230 each have a gain substantially equal to one. Preferably, the amplifiers 214, 216, 218, 226, 228 and 230 are clamped such that they will not provide any of the filters 220, 222, 224, 232, 234 and 236, respectively, with an input signal that will saturate the filter.

The signal strength detector 208 selects the filter bank that is the most suitable for processing the signal received by the input 201 of the signal processing system 200. An input 271 of the signal strength detector 208 is connected to the output 259 of the filter 234, and outputs 281, 283, 285 of the signal strength detector

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208 are connected to the switch control inputs 287, 289, 291 of the switches 238, 240, 242, respectively. The signal strength detector 208 can detect the voltage envelope of the signal on the output 259 of the filter 234. A low-pass-filtered rectifier, well-known for use in many other applications, is one example of a circuit which can be used as an envelope detector. The signal strength detector 208 determines if the voltage envelope of the output 259 of the filter 234 exceeds a first limit whereby the output signal of the filter is approaching the minimum tolerable signal to noise ratio of the filter, or a second limit whereby the filter is entering saturation. In the exemplary embodiment of the signal processing system 200 the first, second and third filter banks are designed such that there exists a first limit representing the point where the first filter bank is near saturation and the output signal of the second filter bank is near the minimum tolerable signal to noise ratio of the second filter bank, and a second limit representing the point where the second filter bank is near saturation and the output signal of the third filter bank is near the minimum tolerable signal to noise ratio of the third filter bank.

If the signal strength detector 208 detects that the voltage envelope of the signal at the output 259 of the filter 234 does not exceed the first limit or the second limit, the signal strength detector 208 selects the first filter bank by providing a logical one on its output 281 to cause the switch 238 to close and a logical zero on its outputs 283, 285 to cause the switches 240, 242, respectively, to open, thereby connecting the first filter bank to the output 244 of the signal processing system 200 and disconnecting the second filter bank and the third filter bank from the output 244. For purposes of the specification and claims, positive logic is assumed. If the signal strength detector 208 detects that the voltage envelope of the signal at the output 259 of the filter 234 exceeds the first limit but not the second limit, the signal strength detector 208 selects the second filter bank by providing a logical one on its output 283 to cause the switch 240 to close and a logical zero on its outputs 281, 285 to cause the switches 238, 242, respectively, to open, thereby connecting the second filter bank to the output 244 of the signal processing system 200 and disconnecting the first filter bank and the third filter bank from the output 244. If the signal strength detector 208 detects that the voltage envelope of the signal at the outputs 259 of the filter 234

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exceeds the first limit and the second limit, the signal strength detector 208 selects the third filter bank by providing a logical one on its output 285 to cause the switch 242 to close and logical zero on its outputs 281, 283 to cause the switches 240, 242, respectively, to open, thereby connecting the third filter bank to the output 244 of the signal processing system 200 and disconnecting the first filter bank and the second filter bank from the output 244.

In an alternate exemplary embodiment, the signal strength detector 208 measures the strengths of the signals at other nodes in the signal processing system 200. The signal strength detector 208 may, for example, measure the voltage envelopes of the signals on outputs 233, 235, 237 of the filters 220, 222, 224, respectively.

In another alternate exemplary embodiment, the first, second and third banks of filters, and associated amplifiers, shown in Fig. 2, can each be replaced by a respective sixth order bandpass Chebychev filters 700, 730, 760, shown in Figs. 7(a), 7(b), 7(c), respectively. The sixth order bandpass Chebychev filter 700 of Fig. 7(a) advantageously has a ripple of 0.25 dB, a bandwidth of 0.5 MHz, and a center frequency of 1.25 Mhz. The sixth order bandpass Chebychev filter 730 of Fig. 7(b) advantageously has a ripple of 0.25 dB, a bandwidth of 0.5 MHz, and a center frequency of 1.25 MHz. The sixth order bandpass Chebychev filter 760 of Fig. 7(c) advantageously has a ripple of 0.25 dB, a bandwidth of 0.5 MHz, a center frequency of 1.25 MHz. Preferably, each of the sixth order bandpass Chebychev filters 700, 730, 760 can be implemented by connecting three standard Tow-Thomas biquads 800 together in series.

Fig. 8 illustrates the standard Tow-Thomas biquad circuit 800. The Tow-Thomas biquad 800 includes a transconductor 808, a transconductor 824, a transconductor 834, a transconductor 844, a capacitor 816, and a capacitor 854. The center frequency ω_0 of the Tow-Thomas biquad 800 can be calculated by the equation:

$$\omega_0 = Q\, G_m / C \qquad (1)$$

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where Q is the quality factor of the Tow-Thomas biquad circuit 800. The absolute value of the transconductors and capacitors can be scaled by the same factor, i.e. impedance scaling, without affecting the transfer function of the Tow-Thomas biquad 800, since the transfer function depends on the ratios between these values. Impedance scaling does not change the transfer function of the Tow-Thomas biquad 800, however it does change the power dissipation and the noise level of the Tow-Thomas biquad 800.

A signal received by the input 802 of the Tow-Thomas biquad 800 is conveyed to a positive input 804 of a transconductor 808. The transconductor 808 processes the difference between the signal received at the positive input 804 and the signal received at a negative input 806, which is connected to ground, and provides a signal at an output 810. The signal at the output 810 is equal to the difference in the signal received by the positive input 804 and the signal received by the negative input 806 of the transconductor 808, scaled by a transconductance G_{in} of the transconductor 808. The transconductance G_{in} of the transconductor 808 sets the gain of the biquad 800, for example, if G_{in} is ten times G_m, the effective input amplification for the biquad 800 is ten. The output 810 of the transconductor 808 is connected to a terminal 814 of the capacitor 816, a negative input 822 of a transconductor 824, an output 830 of the transconductor 824, a positive input 832 of the transconductor 834, an output 850 of the transconductor 844, and the output 812 of the Tow-Thomas biquad 800. These connections form a node 860. The other terminal 818 of the capacitor 816 is connected to ground. The capacitor 816 integrates the currents provided at node 860.

The transconductor 824 processes the difference between the signal received at a positive input 826, which is connected to ground, and the signal received at the negative input 822 and provides a signal at the output 830. The signal at the output 830 of the transconductor 824 is equal to the difference in the signal received by its positive input 826 and the signal received by its negative input 822, scaled by its transconductance G_m. The output 830 of the transconductor 824 is connected to one terminal 814 of a capacitor 816, the negative input 822 of the transconductor 824, the output 830 of the transconductor 824, the positive input 832 of the transconductor

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834, the output 850 of the transconductor 844, and the output 812 of the Tow-Thomas biquad 800. The transconductor 824 forms a feedback loop with the node 860.

The transconductor 834 processes the difference between the signal received at its positive input 832 and the signal received at its negative input 836, which is connected to ground, and provides a signal at an output 840. The signal at the output 840 is equal to the difference in the signal received by the positive input 832 and the signal received by the negative input 836, scaled by a transconductance QG_m. The output 840 of the transconductor 834 is connected to one terminal 852 of a capacitor 854 and a negative input 842 of the transconductor 844. The other terminal 856 of the capacitor 854 is connected to ground.

The transconductor 844 processes the difference between the signal received at its positive input 846, which is connected to ground, and the signal received at its negative input 842 and provides a signal at an output 850. The signal at the output 850 is equal to the difference in the signal received by the positive input 846 and the signal received by the negative input 842 of the transconductor 844, scaled by a transconductance QG_m. The output 850 of the transconductor 844 is connected to on terminal 814 of the capacitor 816, the negative input 822 of the transconductor 824, the output 830 of the transconductor 824, the positive input 832 of the transconductor 834, and the output 812 of the Tow-Thomas biquad 800. The transconductors 834, 844 and the capacitor 854 form a feedback loop to the node 860.

In an exemplary embodiment of the Tow-Thomas biquad 800, a first diode and a second diode are connected to the node 860. The cathode of the first diode is connected to the node 860, and an anode of the first diode is connected to ground. The anode of the second diode is connected to the node 860, and a cathode of the second diode is connected to ground. This arrangement limits the voltage swing at the node 860 to approximately $\pm$ 0.7 volts.

In another exemplary embodiment of the Tow-Thomas biquad 800, a first diode and a second diode are connected to the input 804. The cathode of the first diode is connected to the input 804, and an anode of the first diode is connected to ground. The anode of the second diode is connected to the input 804, and a cathode

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of the second diode is connected to ground. This arrangement limits the voltage swing at the input 804 to approximately ± 0.7 volts.

In still another embodiment of the Tow-Thomas biquad 800, a first diode and a second diode are connected to the output 840. The cathode of the first diode is connected to the output 840, and an anode of the first diode is connected to ground. The anode of the second diode is connected to the output 840, and a cathode of the second diode is connected to ground. This arrangement limits the voltage swing at the output 840 to approximately ± 0.7 volts.

Fig. 9 illustrates the transconductor 808 in greater detail. The transconductors 808, 826, 834 and 844 are similar in construction. The transconductor 808 includes an NMOS transistor Q1, an NMOS transistor Q2, a PMOS transistor Q3, a PMOS transistor Q4, an NMOS transistor Q5, an NMOS transistor Q6, and a current source 924.

A signal received by the positive input 804 of the transconductor 808 is conveyed to the gate 905 of the NMOS transistor Q_1. The NMOS transistor Q_1 allows current to flow from its source 907 to its drain 906, or vice versa, depending on the signal at the gate 905 and the relative voltages at its source 907 and at its drain 906. The drain 906 of the NMOS transistor Q_1 is connected to the drain 913 and the gate 911 of the PMOS transistor Q_3, and the gate 914 of the PMOS transistor Q_4. The source 907 of the NMOS transistor Q_1 is connected to the drain 918 of the NMOS transistor Q_5, and the source 910 of the NMOS transistor Q_2.

A signal received by the negative input 806 of the transconductor 808 is conveyed to a gate 908 of the NMOS transistor Q_2. The drain 909 of the NMOS transistor Q_2 is connected to the drain 916 of the PMOS transistor Q_4 and is the output 810 of the transconductor 808. The source 910 of the NMOS transistor Q_2 is connected to the drain 918 of the NMOS transistor Q_5, and the source 907 of the NMOS transistor Q_1.

The drain 913 of the PMOS transistor Q_3 is connected to the drain 906 of the NMOS transistor Q_1, the gate 911 of the PMOS transistor Q_3, and the gate 914 of the PMOS transistor Q_4. The source 912 of the PMOS transistor Q_3 is connected to supply voltage V_{dd}. The gate 911 of the PMOS transistor Q_3 is connected to the drain

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906 of the NMOS transistor Q_1, the drain 913 of the PMOS transistor Q_3, and the gate 914 of the PMOS transistor Q_4.

The drain 916 of the PMOS transistor Q_4 is connected to the drain 909 of the NMOS transistor Q_2, and the output 810 of the transconductor 808. The source 912 of the PMOS transistor Q_3 is connected to supply voltage V_{dd}. The gate 914 of the PMOS transistor Q_4 is connected to the drain 906 of the NMOS transistor Q_1, the drain 913 and the gate 911 of the PMOS transistor Q_3.

The drain 918 of the NMOS transistor Q_5 is connected to the source 907 of the NMOS transistor Q_1 and the source 910 of the NMOS transistor Q_2. The source 919 of the NMOS transistor Q_5 is connected to supply voltage V_{ss}. The gate 917 of the NMOS transistor Q_5 is connected to the gate 920 and the drain 921 of the NMOS transistor Q_6, and the positive terminal 925 of the current source 924.

The drain 921 of the NMOS transistor Q_6 is connected to the gate 920 of the NMOS transistor Q_6, the gate 917 of the NMOS transistor Q_5, and the positive terminal 925 of the current source 924. The source 922 of the NMOS transistor Q_6 is connected to supply voltage V_{ss}. The gate 920 of the NMOS transistor Q_6 is connected to the gate 917 of the NMOS transistor Q_5, the drain 921 of the NMOS transistor Q_6, and the negative terminal 925 of the current source 924.

The current source 924 produces a bias current I_{bias} for the transconductor 808. The bias current I_{bias} produced by the current source 924 controls the center frequency of the filter. The bias current I_{bias} of the transconductor 808 is adjusted to give a stable center frequency in the presence of fabrication tolerances and temperature variations. The bias current I_{bias} can be any value, for example 100 micro-amperes, and the transistors Q_1, Q_2, Q_3, Q_4, Q_5, Q_6 of the transconductor 808 are scaled to yield the desired transconductances. The transconductance for the transconductors is calculated using the equation:

$$G_m = I_{tail} / (V_{GS} - V_T), \quad (2)$$

where I_{tail} is the current passing through the transistor Q_5 of the transconductor 808, V_T is the threshold voltage of the to transistors Q_5, Q_6, and V_{GS} is the gate-source voltage of the transistors Q_5, Q_6. The linear range of the

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transconductor is related to the quantity $V_{GS} - V_T$. Once the bias current I_{bias} has been set, the transistors Q_5, Q_6 are scaled such that, the following equation is satisfied:

$$(W_{Q5} / L_{Q5}) / (W_{Q6} / L_{Q6}) = I_{tail} / I_{bias}. \quad (3)$$

The negative terminal 925 of the current source 924 is connected to the drain 921 and the gate 920 of the transistor Q_6, and the gate 917 of the transistor Q_5. The positive terminal of the current source 924 is connected to supply voltage V_{dd}. The preferred form of the current source 924 is a resistor connected to the between the supply voltage V_{dd} and the drain 921 and the gate 920 of the NMOS transistor Q_6.

Referring to Fig. 7(a), a signal received by the input 702 of the sixth order bandpass Chebychev filter 700 of the first filter bank is conveyed to an input 704 of a Tow-Thomas biquad 706. The Tow-Thomas biquad 706 processes the signal received at its input 704 and provides a signal at its output 708. Advantageously, the Tow-Thomas biquad 706 has a transconductance G_{in} for transconductor 808 of 771 micro-amperes per volt, transconductance G_m for a transconductor 824 of 185 micro-amperes per volt, a transconductance QG_m for transconductors 834 and 844 of 591 micro-amperes per volt, and a capacitance for capacitors 816, 854 of 77 picofarads. The output 708 of the Tow-Thomas biquad 706 corresponds to input 710 of a Tow-Thomas biquad 712.

In the alternative, the Tow-Thomas biquad 706 can be optimized to use less power. To optimize the Tow-Thomas biquad 706 to use less power, the transconductance G_{in} for the transconductor 808 can be 979 micro-amperes per volt, the transconductance G_m for the transconductor 824 can be 235 micro-amperes per volt, the transconductance QG_m for transconductors 834 and 844 can be 750 micro-amperes per volt, and the capacitance for capacitors 816, 854 can be 97.5 picofarads.

The Tow-Thomas biquad 712 processes the signal received at its input 710 and provides a signal at its output 714. Advantageously, the Tow-Thomas biquad 712 has a transconductance G_{in} for the transconductor 808 of 2312 micro-amperes per volt, a transconductance G_m for the transconductor 824 of 185 micro-amperes per volt, a transconductance QG_m for the transconductors 834 and 844 of 1210 micro-amperes per volt, and a capacitance for the capacitors 816, 854 of 196 picofarads.

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The output 714 of the Tow-Thomas biquad 712 corresponds to input 716 of a Tow-Thomas biquad 718.

In the alternative, the Tow-Thomas biquad 712 can be optimized to use less power. To optimize the Tow-Thomas biquad 712 to use less power, the transconductance G_{in} for the transconductor 808 can be 294 micro-amperes per volt, the transconductance G_m for the transconductor 824 can be 23.5 micro-amperes per volt, the transconductance QG_m for the transconductors 834 and 844 can be 154 micro-amperes per volt, and the capacitance for the capacitors 816, 854 can be 25 picofarads.

The Tow-Thomas biquad 718 processes the signal received at its input 716 and provides a signal at its output 720. The Tow-Thomas biquad 718 has a transconductance G_{in} for the transconductor 808 of 971 micro-amperes per volt, a transconductance G_m for the transconductor 824 of 185 micro-amperes per volt, a transconductance QG_m for the transconductors 834 and 844 of 1210 micro-amperes per volt, and a capacitance for the capacitors 816, 854 of 126 picofarads. The output 720 of the Tow-Thomas biquad 718 corresponds to output 722 of the sixth order bandpass Chebychev filter 700.

In the alternative, the Tow-Thomas biquad 718 can be optimized to use less power. To optimize the Tow-Thomas biquad 718, the transconductance G_{in} for the transconductor 808 can be 123 micro-amperes per volt, the transconductance G_m for the transconductor 824 can be 23.5 micro-amperes per volt, the transconductance QG_m for the transconductors 834 and 844 can be 154 micro-amperes per volt, and the capacitance for the capacitors 816, 854 can be 16 picofarads.

Referring to Fig. 7(b), a signal received by the input 732 of the sixth order bandpass Chebychev filter 730 of the second filter bank is conveyed to an input 734 of a Tow-Thomas biquad 736. The Tow-Thomas biquad 736 processes the signal received at its input 734 and provides a signal at its output 738. Advantageously, the Tow-Thomas biquad 736 has a transconductance G_{in} for the transconductor 808 of 9.29 micro-amperes per volt, a transconductance G_m for the transconductor 824 of 2.23 micro-amperes per volt, a transconductance QG_m for the transconductors 834 and 844 of 7.12 micro-amperes per volt, and a capacitance for the capacitors 816, 854 of

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0.9252 picofarads. The output 738 of the Tow-Thomas biquad 736 corresponds to input 740 of a Tow-Thomas biquad 742.

The Tow-Thomas biquad 742 processes the signal received at its input 740 and provides a signal at its output 744. Advantageously, the Tow-Thomas biquad 742 has a transconductance G_{in} for the transconductor 808 of 9.29 micro-amperes per volt, a transconductance G_m for the transconductor 824 of 2.23 micro-amperes per volt, a transconductance QG_m for the transconductors 834 and 844 of 14.59 micro-amperes per volt, and a capacitance for the capacitors 816, 854 of 2.3664 picofarads. The output 744 of the Tow-Thomas biquad 742 corresponds to input 746 of a Tow-Thomas biquad 748.

The Tow-Thomas biquad 748 processes the signal received at its input 746 and provides a signal at its output 750. Advantageously, the Tow-Thomas biquad 748 has a transconductance G_{in} for the transconductor 808 of 9 micro-amperes per volt, a transconductance G_m for the transconductor 824 of 2.23 micro-amperes per volt, a transconductance QG_m for the transconductors 834 and 844 of 14.59 micro-amperes per volt, and a capacitance for the capacitors 816, 854 of 1.5191 picofarads. The output 750 of the Tow-Thomas biquad 748 corresponds to output 752 of the sixth order bandpass Chebychev filter 730.

Referring to Fig. 7(c), a signal received by the input 762 of the sixth order bandpass Chebychev filter 760 of the third filter bank is conveyed to an input 764 of a Tow-Thomas biquad 766. The Tow-Thomas biquad 766 processes the signal received at its input 764 and provides a signal at its output 768. The Tow-Thomas biquad 766 includes a transconductance G_{in} for the transconductor 808 of 0.7292 micro-amperes per volt, a transconductance G_m for the transconductor 824 of 0.7 micro-amperes per volt, a transconductance QG_m for the transconductors 834 and 844 of 2.2349 micro-amperes per volt, and a capacitance for the capacitors 816, 854 of 0.2904 picofarads. The output 768 of the Tow-Thomas biquad 766 corresponds to input 770 of a Tow-Thomas biquad 772.

The Tow-Thomas biquad 772 processes the signal received at its input 770 and provides a signal at its output 774. The Tow-Thomas biquad 772 includes a transconductance G_{in} for the transconductor 808 of 1.1438 micro-amperes per volt, a

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transconductance G_m for the transconductor 824 of 0.7 micro-amperes per volt, a transconductance QG_m for the transconductors 834 and 844 of 4.58 micro-amperes per volt, and a capacitance for the capacitors 816, 854 of 0.7428 picofarads. The output 74 of the Tow-Thomas biquad 772 corresponds to input 776 of a Tow-Thomas biquad 778.

The Tow-Thomas biquad 778 processes the signal received at its input 776 and provides a signal at its output 780. The Tow-Thomas biquad 778 includes a transconductance G_{in} for the transconductor 808 of 2.8269 micro-amperes per volt, a transconductance G_m for the transconductor 824 of 0.7 micro-amperes per volt, a transconductance QG_m for the transconductors 834 and 844 of 4.58 micro-amperes per volt, and a capacitance for the capacitors 816, 854 of 0.4769 picofarads. The output 780 of the Tow-Thomas biquad 778 corresponds to output 782 of the sixth order bandpass Chebychev filter 760.

Referring to Fig. 12(a), there is shown an exemplary embodiment of a signal strength detector 1200, which may be used as the signal strength detector 208 in the signal processing circuit 200 illustrated in Fig. 2. The signal strength detector 1200 has an input 1202 corresponding to the input 271 of the signal strength detector 208, and the outputs 1240, 1242, 1244, corresponding to the outputs 281, 283, 285 of the signal strength detector 208, respectively.

The signal strength detector 1200 senses the voltage envelope of the input signals received at the input 1202, and selects an appropriate signal processing circuit given two threshold limits. The first threshold limit represents a point at which the first filter bank is near saturation and the output signal of the second filter bank is near its minimum tolerable signal to noise ratio. The second threshold limit represents the point at which the second filter bank is near saturation and the output signal of the third filter bank is near its minimum tolerable signal to noise ratio. The signal strength detector 1200 includes a peak detector 1180, a first threshold detector 1175, a second threshold detector 1176, a two input NOR gate 1228, a two input AND gate 1230, and a two input AND gate 1232. The peak detector 1180 and the first threshold detector 1175 are described in more detail below in relation to Fig. 11.

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A signal received at the input 1202 of the signal strength detector 1200 is conveyed to an input 1204 of the peak detector 1180. The peak detector 1180 processes the signal received at the input 1204 and provides a signal at an output 1206 of the peak detector 1180. The signal output at the output 1206 is conveyed to an input 1208 of the first threshold detector 1175 and an input 1210 of the second threshold detector 1176. The first threshold detector 1175 processes the signal received at its input 1208 and provides a signal at an output 1212. The first threshold detector 1175 transmits a logical one on the output 1212 if the signal at the input 1208 exceeds the first threshold limit, and a logical zero on the output 1212 if the signal at the input 1208 does not exceed the first threshold limit. The signal output at the output 1212 of the first threshold detector 1175 is conveyed to an input 1216 of the two input NOR gate 1228, an input 1220 of the two input AND gate 1230, and an input 1224 of the two input AND gate 1232. The second threshold detector 1176 processes the signal received at its input 1210 and provides a signal at an output 1214. The second threshold detector 1176 transmits a logical one on the output 1212 if the signal at the input 1208 exceeds the second threshold limit, and a logical zero on the output 1212 if the signal at the input 1208 does not exceed the second threshold limit. The signal output at the output 1214 of the second threshold detector 1176 is conveyed to the other input 1218 of the two input NOR gate 1228, an inverted input 1222 of the two input AND gate 1230, and the other input 1226 of the two input AND gate 1232.

The two input NOR gate 1228 processes the signals received at its input 1216 and its input 1218, and provides a signal at the output 1234. The output 1234 is connected to the output 1240 of the signal strength detector 1200. The two input AND gate 1230 processes the signals received at its input 1220 and its inverted input 1222, and provides a signal at the output 1236. The output 1236 is connected to the output 1242 of the signal strength detector 1200. The two input AND gate 1232 processes the signals received at its input 1224 and its input 1226, and provides a signal at the output 1238. The output 1238 is connected to the output 1244 of the signal strength detector 1200.

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Fig. 11 illustrates a portion 1100 of the signal strength detector 1200 of Fig. 12 in greater detail. The signal strength detector portion 1100 includes the peak detector 1180 and the first threshold detector 1175. The peak detector 1180 includes an NMOS transistor Q_1, a PMOS transistor Q_3, an NMOS transistor Q_4, a PMOS transistor Q_5, a PMOS transistor Q_6, a capacitor 1173, and a transconductor 1107.

A signal received by the input 1102 of the peak detector 1180 is conveyed to a positive input 1103 of the transconductor 1107. The transconductor 1107 processes the difference between the signal received at its positive input 1103 and a signal received at its negative input 1105, which is connected to ground, and provides a signal at an output 1109. The signal at the output 1109 is equal to the difference in the signal received by the positive input 1103 and the signal received by the negative input 1105, scaled by a transconductance G_{in} of the transconductor 1107. The transconductor 1107 has a transconductance G_m of 1 miliampere per volt. The signal provided at the output 1109 of the transconductor 1107 is conveyed the gate 1104 of the PMOS transistor Q_3, the gate 1106 of the NMOS transistor Q_4, the gate 1108 of the PMOS transistor Q_5, the drain 1110 of the PMOS transistor Q_5, the source 1112 of the PMOS transistor Q_6, the backgate 1114 of the PMOS transistor Q_6, and a drain 1116 of the NMOS transistor Q_1. The PMOS transistor Q_3 and the NMOS transistor Q_4 form an inverter receiving the signal received by the input 1102. The source 1118 of the PMOS transistor Q_3 is connected to supply voltage V_{dd}. The gate 1104 of the PMOS transistor Q_3 is connected to the input 1102, the gate 1106 of the NMOS transistor Q_4, the gate 1108 of the PMOS transistor Q_5, the drain 1110 of the PMOS transistor Q_5, the source 1112 of the PMOS transistor Q_6, the backgate 1114 of the PMOS transistor Q_6, and the drain 1116 of the NMOS transistor Q_1. The backgate 1120 of the PMOS transistor Q_3 is connected to supply voltage V_{dd}, and the drain 1122 of the PMOS transistor Q_3 is connected to the drain 1124 of the NMOS transistor Q_4, the source 1130 of the PMOS transistor Q_5 and the gate 1134 of the PMOS transistor Q_6. The source 1128 of the NMOS transistor Q_4 is connected to supply voltage V_{ss}. The gate 1106 of PMOS transistor Q_4 is connected to the input 1102, the gate 1104 of the PMOS transistor Q_3, the gate 1108 of the PMOS transistor Q_5, the drain 1110 of the PMOS transistor Q_5, the source 1112 of the PMOS transistor

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Q_6, the backgate 1114 of the PMOS transistor Q_6, and the drain 1116 of the NMOS transistor Q_1. The backgate 1126 of the NMOS transistor Q_4 is connected to supply voltage V_{ss}. The drain 1124 of the NMOS transistor Q_4 is connected to the drain 1122 of the PMOS transistor Q_3, the source 1130 of the PMOS transistor Q_5 and the gate 1134 of the PMOS transistor Q_6.

The PMOS transistor Q_5 is connected to act as a diode for the signal received at the input 1102 of the peak detector 1180. The gate 1108 and the drain 1110 of the PMOS transistor Q_5 are connected to each other, the input 1102, the gate 1104 of the PMOS transistor Q_3, the gate 1106 of the NMOS transistor Q_4, the source 1112 of the PMOS transistor Q_6, the backgate 1114 of the PMOS transistor Q_6, and the drain 1116 of the NMOS transistor Q_1. The backgate 1132 of the PMOS transistor Q_5 is connected to supply voltage V_{dd}. The source 1130 of the PMOS transistor Q_5 is connected to the drain 1122 of the PMOS transistor Q_3, the drain 1124 of the NMOS transistor Q_4 and the gate 1134 of the PMOS transistor Q_6.

The PMOS transistor Q_6 acts as a PMOS switch for the signal at the input 1102 of the peak detector 1180. The gate 1134 of the PMOS transistor Q6 is connected to the source 1130 of the PMOS transistor Q_5, the drain 1122 of the PMOS transistor Q_3, and the drain 1124 of the NMOS transistor Q_4. The source 1112 and the backgate 1114 of the PMOS transistor Q_6 are connected to each other, the input 1102, the gate 1108 of the PMOS transistor Q_5, the drain 1110 of the PMOS transistor Q_5, the gate 1104 of the PMOS transistor Q_3, the gate 1106 of the NMOS transistor Q_4, and the drain 1116 of the NMOS transistor Q_1. The drain 1136 of the PMOS transistor Q_6 is connected to a gate 1138 of the NMOS transistor Q_1,an output 1172 of the peak detector 1180, and a terminal 1171 of the capacitor 1173. A terminal 1181 of the capacitor 1173 is connected to supply voltage V_{ss}.

The NMOS transistor Q_1 of the peak detector 1180 forms half of an NMOS current mirror that acts as a current memory which stores the peak current of the signal received at the input 1102 of the peak detector 1180. The other half of the NMOS current mirror that acts as a current memory is the NMOS transistor Q_2 of a threshold detector 1175 connected to the output 1172 of the peak detector 1180. The source 1144 of the NMOS transistor Q_1 is connected to supply voltage V_{ss}. The gate

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of the NMOS transistor Q_1 is connected to the output 1172 of the peak detector 1180 and the drain 1136 of the PMOS transistor Q_6. The backgate 1142 of the NMOS transistor Q_1 is connected to supply voltage V_{ss}. And the drain 1116 of the NMOS transistor Q_1 is connected to the input 1102, the source 1112 of the PMOS transistor Q6, the backgate 1114 of the PMOS transistor Q_6, the gate 1108 and drain 1110 of the PMOS transistor Q_5, the gate 1104 of the PMOS transistor Q_3, and the gate 1106 of the NMOS transistor Q_4.

The first threshold detector 1175 compares the voltage envelope of a signal received at the input 1102 of the peak detector 1180 to a reference current supplied by a current source 1170. The first threshold detector 1175 includes an NMOS transistor Q_2, a PMOS transistor Q_7, a PMOS transistor Q_8, the current source 1170, a PMOS transistor Q_9, and an NMOS transistor Q_{10}. Any number of threshold detectors can be connected to the peak detector 1180 to derive a corresponding number of signal strength detector outputs. A signal received by the input 1174 of the first threshold detector 1175 is conveyed to the gate 1140 of the NMOS transistor Q_2.

The NMOS transistor Q_2 of the first threshold detector 1175 forms half of an NMOS current mirror that acts as a current memory which stores the peak current corresponding to the voltage signal received at the input 1102 of the peak detector 1180. The other half of the NMOS current mirror that acts as a current memory consists of the NMOS transistor Q_1 of the peak detector 1180 connected to the input 1174 of the first threshold detector 1175. The source 1146 of the NMOS transistor Q_2 is connected to supply voltage V_{ss}. The drain 1150 of the NMOS transistor Q_2 is connected to the gate 1153 of the PMOS transistor Q_9, the gate 1159 of the NMOS transistor Q_{10}, and the drain 1154 of a PMOS transistor Q_7. The gate 1140 of the NMOS transistor Q_2 is connected to the input 1174 of the first threshold detector 1175. The backgate 1148 of the NMOS transistor Q_2 is connected to supply voltage V_{ss}.

The NMOS transistor Q_9 and the NMOS transistor Q_{10} form an inverter. The gate 1153 of the PMOS transistor Q_9 is connected to the gate 1159 of the NMOS transistor Q_{10}, the drain 1154 of the NMOS transistor Q_7, and the drain 1150 of the NMOS transistor Q_2. The source 1155 of the PMOS transistor Q_9 is

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connected to supply voltage V_{dd}. The drain 1157 of the PMOS transistor Q_9 is connected to the drain 1161 of the NMOS transistor Q_{10} and the output 1152 of the first threshold detector 1175. The source 1163 of the NMOS transistor Q_{10} is connected to supply voltage V_{ss}. The drain 1161 of the NMOS transistor Q_{10} is connected to the drain 1157 of the PMOS transistor Q_9 and the output 1152 of the first threshold detector 1175.

The NMOS transistor Q_7, an NMOS transistor Q_8 and the current source 1170 form a current mirror that causes a current to flow through the NMOS transistor Q_7 that mirrors the current of the current source 1170. The gate 1158 of the NMOS transistor Q_7 is connected to the gate 1162 of the NMOS transistor Q_8, the drain 1164 of the NMOS transistor Q_8, and the positive terminal 1166 of the current source 1170. The source 1156 of the NMOS transistor Q_7 is connected to supply voltage V_{dd} and the source 1160 of the NMOS transistor Q_8. The drain 1154 of the NMOS transistor Q_7 is connected to the gate 1153 of the PMOS transistor Q_9, the gate 1159 of the NMOS transistor Q_{10}, and the drain 1150 of the NMOS transistor Q_2. The gate 1162 and the drain 1164 of the NMOS transistor Q_8 are connected to each other, the gate of the NMOS transistor Q_7 and the positive terminal 1166 of the current source 1170. The source 1160 of the NMOS transistor Q_8 is connected to the source 1156 of the NMOS transistor Q_7 and supply voltage V_{dd}. The current source 1170 includes a positive terminal 1166 and a negative terminal 1168. The positive terminal 1166 of the current source 1170 is connected to the gate 1158 of the NMOS transistor Q_7, the gate 1162 of the NMOS transistor Q_8, and the drain 1164 of the NMOS transistor Q_8. The negative terminal 1168 of the current source 1170 is connected to ground.

The current source 1170 produces a reference current that represents the threshold voltage of the first threshold detector 1175. The current can be any value, for example 100 uA, and the transistors Q_7, Q_8 of the first threshold detector 1175 are scaled to yield the desired current through the transistor Q_7. The preferred form of a current source is a resistance connected between the drain of NMOS transistor Q_8 and ground. In the present example the reference current generated by the current source in the first threshold detector 1175 is 7.7 micro-amperes.

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The output 1152 of the first threshold detector 1175 indicates which filter bank should be used given the voltage envelope of the signal received at the input 1102 of the peak detector 1180. If the current flowing through the transistor Q_2, which represents the voltage envelope of the signal received at the input 1102 of the peak detector 1180, exceeds the current flowing through the transistor Q_7, which is related to the reference current of the current source 1170, the output 1152 of the first threshold detector 1175 would be a logical one. If the current flowing through the transistor Q_2 does not exceed the current flowing through the transistor Q_7, the output 1152 of the first threshold detector 1175 would be a logical zero. In this manner, the first threshold limit of the signal strength detector 1200 is current generated by the current source 1170.

The second threshold detector 1176 (not shown in Fig. 11) may be similar to the first threshold detector 1175 as shown in Fig. 11. It would have a counterpart to NMOS transistor Q_2 of the first threshold detector 1175, with the gate of the counterpart transistor connected to the output 1172 of the peak detector 1180. The second threshold detector 1176 would also have its counterpart to the current mirror, which in the first threshold detector 1175 consists of NMOS transistors Q_7 and Q_8, and reference current source 1170. The counterpart to the current source 1170 of the second threshold detector 1176 would produce a reference current that represents the second threshold limit. In the present example, the counterpart to the current source 1170 would generate 77 micro-amperes.

Referring to Fig. 2, the signal processing system 200 can have more than three filter banks. If the filter system 200 includes more than three filter banks, the signal strength detector 208 must be adapted to select an appropriate filter bank from the more than three filter banks. In order to select the appropriate filter bank from a signal processing system with more than three filter banks, the signal strength detector may be modified to have a group of peak detectors, each similar to the peak detector 1180 shown in Fig. 11, to sense the voltage envelope of the output signal provided by each of the filter banks of the system 200, except for the filter bank configured to process the largest input signal range and the filter bank configured to process the smallest input signal range. For example, if the filter system 200 has five

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filter banks, a filter bank configured to process the largest input signals, a filter bank configured to process the smallest input signals, and a group of three filter banks configured to process intermediate input signals, the voltage envelopes of the output signals produced by the group of three intermediate signal filter banks are measured by the signal strength detector. Assuming that the filter banks are designed such that the saturation level of each filter bank, except the largest signal filter bank, overlaps the minimum tolerable signal to noise ratio of another filter bank, the signal strength detector has three threshold detectors, preferably similar to the first threshold detector 1175 shown in Fig. 11, to compare the voltage envelope of the output signal of each one of the three intermediate signal filter banks with a corresponding first threshold limit. Each first threshold limit indicates when the corresponding filter bank is approaching saturation. For example, if the signal strength detector measures the voltage envelopes of the signals of the three intermediate signal filter banks, three threshold detectors are needed to compare the detected envelopes with three different first threshold limits. The strength detector also uses an additional threshold detector, preferably similar to the first threshold detector 1175 shown in Fig. 11, to compare the voltage envelope of the output signal from the filter bank configured to process the smallest input signals with a second threshold limit. The second threshold limit indicates when the output signal of the smallest signal filter bank is approaching its saturation point. Once the voltage envelopes of the output signals the three intermediate signal filter banks and the smallest signal filter bank are compared to respective first and second threshold limits, the strength detector selects the filter bank that is configured to process the smallest input signal without saturating.

In an alternate embodiment of the signal processing system 200 of Fig. 2, the respective gains of amplifiers 216, 218, 230 each have a first selected value and the respective gains of amplifiers 214, 226, 228 each have a second selected value. The filters 202, 204, 206 each have the same transfer function; and the filters 222, 224 each have the same transfer function. This allows the signal processing system 200 to have an alternate structure shown in Fig. 3.

A signal received by the input 301 of the signal processing system 300, which include an in-band component and an out-band component, is conveyed to an

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input 303 of a filter 302. Preferably, the filter 302 has enough linear range to accommodate the signal on the input 301 of the signal processing system 300 without saturating. The filter 302 processes the signal received at its input 303 and produces a processed signal at its output 305. The output 305 of the filter 302 corresponds to input 307 of an amplifier 314 and an input 309 of an amplifier 316. The amplifier 314 amplifies or attenuates the signal received at its input 307 and provides an amplified signal at its output 311. The output 311 of the amplifier 314 corresponds to input 315 of a filter 320. The filter 320 processes the signal received at its input 315 and produces a processed signal at its output 319. The output 319 of the filter 320 corresponds to input 323 of an amplifier 326. The amplifier 326 amplifies or attenuates the signal received at its input 323 and outputs an amplified signal at its output 329. The output 329 of the amplifier 326 corresponds to input 335 of a filter 332. The filter 332 processes the signal received at its input 335 and produces a processed signal at its output 341. The output 341 of the filter 332 corresponds to input 347 of a switch 338. The switch 338 outputs the signal received at its input 347 on its output 353 when the signal received at its switch control input 361 is a logical one, and isolates its input 347 from its output 353 when the signal received at its switch control input 361 is a logical zero. The output 353 of the switch 338 is connected to the output 344 of the signal processing system 300.

The amplifier 316 amplifies or attenuates the signal received at its input 309 and outputs an amplified signal at its output 313. The output 313 of the amplifier 316 corresponds to input 317 of a filter 322. The filter 322 processes the signal received at its input 317 and produces a processed signal at its output 321. The output 321 of the filter 322 corresponds to input 325 of an amplifier 328 and an input 327 of an amplifier 330. The amplifier 328 amplifies or attenuates the signal received at its input 325 and provides an amplified signal at its output 331. The output 331 of the amplifier 328 corresponds to input 337 of a filter 334. The filter 334 processes the signal received at its input 337 and produces a processed signal at its output 343. The output 343 of the filter 334 corresponds to input 349 of a switch 340 and an input 375 of the signal strength detector 308. The switch 340 outputs the signal received at its input 349 on its output 355 when the signal received at its switch control input 363 is

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a logical one, and does not output the signal received at its input 349 on its output 355 when the signal received at its switch control input 363 is a logical zero. The output 355 of the switch 340 is connected to the output 344 of the signal processing system 300.

The amplifier 330 amplifies or attenuates the signal received at its input 327 and outputs an amplified signal at its output 333. The output 333 of the amplifier 330 corresponds to input 339 of a filter 336. The filter 336 processes the signal received at its input 339 and produces a processed signal at its output 345. The output 345 of the filter 336 corresponds to input 351 of a switch 342. The switch 342 outputs the signal received at its input 351 on its output 357 when the signal received at its switch control input 365 is a logical one, and does not output the signal received at its input 351 on its output 357 when the signal received at its switch control input 365 is a logical zero. The output 357 of the switch 342 is connected to the output 344 of the signal processing system 300.

Preferably, the signal processing system 300 is optimized such that the signal processing pathways that terminate at outputs 341, 343, 345 of the filters 332, 334, 336, respectively, are each adapted for a different in-band component / out-band component ratio. The signal processing pathways that terminate at the output 341 of the filter 332 is adapted for processing an input signal that has a large out-band component and a relatively small in-band component. This signal processing path is so adapted by having the respective gains of amplifiers 314, 326 to be greater than one. Preferably, the amplifiers 314, 326 have respective gains of ten so that each amplifier provides a signal with ten times the amplitude of the signal at its input. The signal processing path that terminates at the output 343 of the filter 334 is adapted for processing an input signal that has an out-band component which is slightly larger than the in-band component. This signal processing path is so adapted by having the gains of the amplifier 316 equal to one, and having the gain of amplifier 328 greater than one. Preferably, the amplifier 328 has a gain of ten, causing the amplifier 328 to provide a signal at its output 331 with ten times the amplitude of the signal received at its input 325. The signal processing path that terminates at the output 345 of the filter 336 is adapted to process an input signal that has an out-band component that is

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approximately equal to the in-band component. This signal processing path is so adapted by having the respective gains of amplifiers 316, 330 each equal to one. Preferably, the amplifiers 314, 316, 326, 328 and 330 are clamped such that they will not provide any of the filters 320, 322, 332, 334 and 336 with an input signal that will saturate the filter.

The signal strength detector 308 analyzes the voltage envelope of the signal received on its input 375 to determine if the voltage envelope of the signal received on the input 375 exceeds or is below respective limits whereby the filter 334 is entering saturation or the signal received at the input 375 is approaching the minimum tolerable signal to noise ratio of the filter 334. For the filter system 300, there can be two limits. A first limit represents the point where the filter 332 is near saturation and the filter 334 is near the minimum tolerable signal to noise ratio. A second limit represents the point where the filter 334 is near saturation and the filter 336 is near the minimum tolerable signal to noise ratio.

If the signal strength detector 308 detects that the voltage envelope of the signal received at its input 375 does not exceed the first limit or the second limit, the signal strength detector 308 selects the signal that was processed by the filter 332 by providing a logical one on its output 367 to close the switch 338 and a logical zero on its outputs 369, 371 to open the switches 340, 342, respectively. In this manner, the signal from the output 341 of the filter 332 is provided to the output 344 of the signal processing system 300, and the outputs 343, 345 of the filters 334, 336, respectively, are disconnected from the output 344 of the signal processing system 300. If the signal strength detector 308 detects that the voltage envelope of the signal received at the input 375 of the signal strength detector 308 falls below the second limit, but exceeds the first limit, the signal strength detector 308 selects the signal that was processed by the filter 334 by providing a logical one on its output 369 to close the switch 340 and a logical zero on its outputs 367, 371 to open the switches 338, 342, respectively, thereby connecting the signal from the output 343 of the filter 334 to the output 344 of the signal processing system 300 and disconnecting the outputs 341, 345 of the filters 332, 336 from the output 344 of the signal processing system 300. If the signal strength detector 308 detects that the voltage envelope of the signal

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received at the input 375 of the signal strength detector 308 exceeds the first limit and the second limit, the signal strength detector 308 selects the signal that was processed by the filter 336 by providing a logical one on its output 371 to close the switch 342 and a logical zero on its outputs 367, 369 to open the switches 338, 340, respectively, thereby connecting the signal from the output 345 of the filter 336 to the output 344 of the signal processing system 300 and disconnecting the outputs 341, 343 of the filters 332, 334 from the output 344 of the signal processing system 300.

In an exemplary embodiment, the signal strength detector 1200 of Fig. 12(a) may be used as the signal strength detector 308. Referring the Fig. 12(a), the input 1202 of the signal strength detector 1200 may serve as input 375 of the signal strength detector 308 in Fig. 3, and the outputs 1240, 1242, 1244 of the signal strength detector 1200 may serve as outputs 367, 369 and 371 of the signal strength detector 308 of Fig. 3, respectively. In addition, the threshold detector 1175 may be adjusted to reflect the first limit, while the threshold detector 1176 may be adjusted to reflect the second limit.

Fig. 4 illustrates another exemplary signal processing system 400 according to the present invention. The signal processing system 400 includes multiple companding signal processors 434, 436, 438 with different fixed input and output gains configured in parallel with each other. A signal received by an input 402 of the signal processing system 400 is conveyed to an input 401 of the companding signal processor 434, an input 403 of the companding signal processor 436, an input 405 of the companding signal processor 438, and an input 452 of a signal strength detector 410.

The signal received by the input 401 of the companding signal processor 434 corresponds to input 407 of an amplifier 404. The amplifier 404 amplifies or attenuates the signal received at its input 407 and produces an output signal at its output 415. The gain of the amplifier 404 is fixed at a first amplification level. The output 415 of the amplifier 404 corresponds to input 421 of the filter 414. The filter 414 processes the signal received at its input 421 and outputs a processed signal at its output 427. The output 427 of the filter 414 corresponds to input 435 of the amplifier 420. The amplifier 420 amplifies or attenuates the signal received at its

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input 435 and produces an output signal at its output 443. The gain of the amplifier 420 is fixed at an inverse of the first amplification level. The output 443 of the amplifier 420 is connected to the input 455 of a switch 426. The switch 426 outputs the signal received at its input 455 on its output 461 when a signal received at its switch control input 467 is a logical one, and does not output the signal received at its input 455 on its output 461 when the signal received at its switch control input 467 is a logical zero. The output 461 of the switch 426 is connected to the output 432 of the signal processing system 400.

The signal received by the input 403 of the companding signal processor 436 corresponds to input 409 of an amplifier 406. The amplifier 406 amplifies or attenuates the signal received at its input 409 and produces an output signal at its output 417. The gain of the amplifier 406 is fixed at a second amplification level. The output 417 of the amplifier 406 corresponds to input 423 of a filter 416. The filter 416 processes the signal received at its input 423 and provides a processed signal at its output 429. The output 429 of the filter 416 is connected to the input 437 of an amplifier 422. The amplifier 422 amplifies or attenuates the signal received at its input 437 and produces an output signal at its output 445. The gain of the amplifier 422 is fixed at an inverse of the second amplification level. The output 445 of the amplifier 422 corresponds to input 457 of the switch 428. The switch 428 outputs the signal received at its input 457 on its output 463 when the signal received at its switch control input 469 is a logical one, and does not output the signal received at its input 457 on its output 463 when the signal received at its switch control input 469 is a logical zero. The output 463 of the switch 428 is connected to the output 432 of the signal processing system 400.

The signal received by the input 405 of the companding signal processor 438 corresponds to input 411 of an amplifier 408. The amplifier 408 amplifies or attenuates the signal received at its input 411 and produces an output signal at its output 419. The gain of the amplifier 408 is fixed at a third amplification level. The output 419 of the amplifier 408 corresponds to input 425 of the filter 418. The filter 418 processes the signal received at its input 425 and outputs a processed signal at its output 431. The output 431 of the filter 418 corresponds to input 439 of

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the amplifier 424. The amplifier 424 amplifies or attenuates the signal received at its input 439 and produces an output signal at its output 447. The gain of the amplifier 424 is fixed at an inverse of the third amplification level. The output 447 of the amplifier 424 is connected to the input 459 of a switch 430. The switch 430 outputs the signal received at its input 459 on its output 465 when a signal received at its switch control input 471 is a logical one, and does not output the signal received at its input 459 on its output 465 when the signal received at its switch control input 471 is a logical zero. The output 465 of the switch 430 is connected to the output 432 of the signal processing system 400.

The first companding signal processor 434 is configured to process signals with a larger signal voltage envelope than the second companding signal processor 436 and the third companding signal processor 438. Moreover, the corresponding signal processors are advantageously designed such that the saturation level of each companding signal processor except for the one designed to process the largest signals, overlaps the minimum tolerable signal to noise ratio of another one of the companding signal processors. The second companding signal processor 436 is configured to process signals with a smaller signal voltage envelope than the first companding signal processor 434 and a larger signal voltage envelope than the third companding signal processor 438. The third companding signal processor 438 is configured to process signals with a smaller signal voltage envelope than the first companding signal processor 434 and the second companding signal processor 436. Preferably, the first companding signal processor 434, the second companding signal processor 436, and the third companding signal processor 438 are each adapted to effectively process a signal over a different signal amplitude range. In one exemplary embodiment, the transfer functions of the filter 414, 416, 418 are the same, and the first amplification level, the second amplification level and the third amplification level are different. Preferably, the first amplification level is greater than the second amplification level which is greater than the third amplification level.

The signal strength detector 410 selects the one of the companding signal processors 434, 436, 438 that has the most suitable saturation level and minimum tolerable signal to noise ratio for processing the signal received by the input

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402 of the signal processing system 400, which is connected to the input 452 of the signal strength detector 410. Only one of the companding filters 434, 436, 438 is selected by the signal strength detector 410 at any one time. The signal strength detector 410 analyzes the signal received at the input 402 to determine if the voltage envelope of the signal received at the input 402 exceeds a first limit whereby the signal received at the input 402 is approaching the minimum tolerable signal to noise ratio of the companding signal processor 436 and a second limit whereby the companding signal processor 436 is entering saturation. The first limit representing the point where the signal received at the input 402 is near the minimum tolerable signal to noise ratio of the companding filter 436 and the companding filter 434 is near saturation, and the second limit representing the point where the companding filter 436 is near saturation and the signal received at the input 402 is near its minimum tolerable signal to noise ratio. A low-pass-filtered rectifier, well-known for use in many other applications, is one example of a circuit which can be used as an envelope detector.

The signal strength detector 410 selects the first companding signal processor 434 if the voltage envelope of the signal received by the input 402 does not exceed the first limit or the second limit. The signal strength detector 410 selects the first companding signal processor 434 by providing a logical one on an output 473 of the signal strength detector 410, and a logical zero on outputs 475, 477 of the signal strength detector 410. The signal strength detector 410 selects the second companding signal processor 436 if the voltage envelope of the signal received by the input 402 is above the first limit but below the second limit. The signal strength detector 410 selects the second companding signal processor 436 by providing a logical one on an output 475 of the signal strength detector 410, and a logical zero on the outputs 473, 477 of the signal strength detector 410. The signal strength detector 410 selects the third companding signal processor 438 if the voltage envelope of the signal received by the input 402 is above the first limit and the second limit. The signal strength detector 410 selects the third companding signal processor 438 by providing a logical one on an output 477 of the signal strength detector 410, and a logical zero on the outputs 473, 475 of the signal strength detector 410. The outputs

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473, 475, 477 of the signal strength detector 410 are connected to the switch control inputs 467, 469, 471, respectively, of the switches 426, 428, 430.

In an alternate exemplary embodiment, the amplifiers 404, 406, 408 are clamped such that they will not provide any of the filters 414, 416, 418 with an input signal that will saturate the filter.

In an exemplary embodiment, the companding signal processor 434 of the filter 400 of Fig. 4 may be implemented as a biquad 1000, shown in Fig. 10, with a bandwidth of 100 kHz. The biquad 1000 can have a center frequency of 2 MHz and a quality factor of 20. The biquad 1000 can be optimized for relatively small input signals by having a relatively large effective amplification at the input of the biquad and a commensurately large effective attenuation at the output of the biquad 1000. The biquad 1000 processes the signal received at the input 401 and provides a signal at the output 455. Referring to Fig. 10, the biquad 1000 may advantageously have a transconductance G_{in} for a transconductor 1008 of 500 micro-amperes per volt, a transconductance G_m for a transconductors 1024 and 1062 of 50 micro-amperes per volt, a transconductance QG_m for transconductors 1034 and 1044 of 1000 micro-amperes per volt, a capacitance for capacitors 1016, 1054 of 80 picofarads, and a resistance for a resistor 1068 of 2 KΩ or $1/G_{in}$.

In the exemplary embodiment, the companding signal processor 436 of the filter 400 of Fig. 4 may be implemented as a biquad 1000, shown in Fig. 10, advantageously having a bandwidth of 100 kHz. The biquad 1000 can advantageously have a center frequency of 2 MHz and a quality factor of 20. The biquad 1000 can advantageously be optimized for average input signals by having little or no effective amplification at the input of the biquad and a commensurate effective attenuation at the output of the biquad 1000. The biquad 1000 processes the signal received at the input 403 and provides a signal at the output 457. Referring to Fig. 10, the biquad 1000 may advantageously have a transconductance G_{in} for the first transconductor 1008 of 50 micro-amperes per volt, a transconductance G_m for the transconductors 1024 and 1062 of 50 micro-amperes per volt, a transconductance QG_m for the transconductors 1034 and 1044 of 1000 micro-amperes per volt, a

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capacitance for the capacitors 1016, 1054 of 80 picofarads, and a resistance for the resistor 1068 of 20 KΩ or $1/G_{in}$.

In the exemplary embodiment, the companding signal processor 438 of the filter 400 of Fig. 4 can be implemented as a biquad 1000, shown in Fig. 10, advantageously having a bandwidth of 100 kHz. The biquad 1000 can advantageously have a center frequency of 2 MHz and a quality factor of 20. The biquad 1000 can advantageously be optimized for relatively large input signals by having relatively large attenuation at the input of the biquad and a commensurate effective amplification at the output of the biquad 1000. The biquad 1000 processes the signal received at the input 405 and provides a signal at the output 459. Referring to Fig. 10, the biquad 1000 advantageously has a transconductance G_{in} for the first transconductor 1008 of 5 micro-amperes per volt, a transconductance G_m for the transconductors 1024 and 1062 of 50 micro-amperes per volt, a transconductance QG_m for the transconductors 1034 and 1044 of 1000 micro-amperes per volt, a capacitance for the capacitors 1016, 1054 of 80 picofarads, and a resistance for the resistor 1068 of 200 KΩ or $1/G_{in}$.

Fig. 10 illustrates an exemplary biquad 1000 suitable for implementing the companding filter 434, 436 and 438 of the signal processor 400 of Fig. 4. The biquad 1000 includes a first transconductor 1008, a second transconductor 1024, a third transconductor 1034, a fourth transconductor 1044, a fifth transconductor 1062, a first capacitor 1016, a second capacitor 1054, and a resistor 1068. The center frequency of the biquad 1000 can be calculated by equation (1). The absolute value of the transconductors and capacitors can be scaled by the same factor, i.e. impedance scaling, without affecting the transfer function of the biquad 1000, since the transfer function depends on the ratios between these values. Impedance scaling does not change the transfer function of the biquad 1000, however it does change the power dissipation and the noise level of the biquad 1000.

A signal received by the input 1002 of the biquad 1000 is conveyed to a positive input 1004 of the first transconductor 1008 of the biquad 1000. The first transconductor 1008 processes the difference between the signal received at its positive input 1004 and a signal received at its negative input 1006, which is

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connected to ground, and provides a signal at an output 1010. The signal at the output 1010 is equal to the difference in the signal received by the positive input 1004 and the signal received by the negative input 1006, scaled by a transconductance G_{in} of the first transconductor 1008. The first transconductance G_{in} of the first transconductor 1008 sets the gain of the biquad, for example, if G_{in} is ten times G_m the effective input amplification for the biquad 1000 is ten. The output 1010 of the first transconductor 1008 is connected to one terminal 1014 of the first capacitor 1016, a negative input 1022 of the second transconductor 1024, an output 1030 of the second transconductor 1024, a positive input 1032 of the third transconductor 1034, and an output 1050 of the fourth transconductor 1044. These connections form a first node 1074. The other terminal of the first capacitor 1016 is connected to ground. The first capacitor 1016 integrates the signals provided at the first node 1074.

The second transconductor 1024 processes the difference between the signal received at its positive input 1026, which is connected to ground, and the signal received at its negative input 1022 and provides a signal at its output 1030. The signal at the output 1030 is equal to the difference in the signal received by the positive input 1026 and the signal received at the negative input 1022, scaled by a transconductance G_m of the second transconductor 1024. The output 1030 of the second transconductor 1024 is connected to one terminal 1014 of the first capacitor 1016, the negative input 1022 of the second transconductor 1024, the output 1030 of the second transconductor 1024, the positive input 1032 of the third transconductor 1034, and the output 1050 of the fourth transconductor 1044. The second transconductor 1024 forms a feedback loop with the first node 1074.

The third transconductor 1034 processes the difference between the signal received at the positive input 1032 and the signal received at its negative input 1036, which is connected to ground, and provides a signal at an output 1040. The signal at the output 1040 is equal to the difference in the signal received by its positive input 1032 and the signal received by its negative input 1036, scaled by a transconductance QG_m of the third transconductor 1034. The output 1040 of the third transconductor 1034 is connected to one terminal 1052 of the second capacitor 1054, a negative input 1042 of the fourth transconductor 1044, and a positive input 1058 of

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the fifth transconductor 1062. These connections form a second node 1076. The other terminal 1056 of the second capacitor 1054 is connected to ground.

The fourth transconductor 1044 processes the difference between the signal received at its positive input 1046, which is connected to ground, and the signal received at its negative input 1042 and provides a signal at the output 1050. The signal at its output 1050 is equal to the difference in the signal received by the positive input 1046 and the signal received by the negative input 1042, scaled by a transconductance QG_m of the fourth transconductor 1044. The output 1050 of the fourth transconductor 1044 is connected to one terminal 1014 of the first capacitor 1016, the negative input 1022 of the second transconductor 1024, the output 1030 of the second transconductor 1024, and the positive input 1032 of the third transconductor 1034. The third and fourth transconductors 1034, 1044 and the second capacitor 1054 form a feedback loop with the second node 1076.

The fifth transconductor 1062 processes the difference between the signal received at its positive input 1058, and the signal received at its negative input 1060, which is connected to ground, and provides a signal at an output 1064. The signal at the output 1064 is equal to the difference in the signal received by the positive input 1058 and the signal received by the negative input 1060 of the fifth transconductor 1062, scaled by a transconductance QG_m of the fifth transconductor 1062. The output 1064 of the fifth transconductor 1062 is connected to one terminal 1066 of the resistor 1068 and the output 1072 of the biquad 1000. An other terminal 1070 of the resistor 1068 is connected to ground. The resistor 1068, together with the transconductor 1062, creates an amplifier at the output of the biquad 1000 resulting in an effective output amplification or attenuation.

In another exemplary embodiment, a first diode and a second diode are connected to the first node 1074. The cathode of the first diode is connected to the first node 1074, and an anode of the first diode is connected to ground. The anode of the second diode is connected to the first node 1074, and a cathode of the second diode is connected to ground. This arrangement limits the voltage swing at the first node 1074 to approximately $\pm$ 0.7 volts.

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In further exemplary embodiment, a first diode and a second diode are connected to the second node 1076. The cathode of the first diode is connected to the second node 1076, and an anode of the first diode is connected to ground. The anode of the second diode is connected to the second node 1076, and a cathode of the second diode is connected to ground. This arrangement limits the voltage swing at the second node 1076 to approximately ± 0.7 volts.

In another embodiment, a first diode and a second diode are connected to the input 1004. The cathode of the first diode is connected to the input 1004, and an anode of the first diode is connected to ground. The anode of the second diode is connected to the input 1004, and a cathode of the second diode is connected to ground. This arrangement limits the voltage swing at the input 1004 to approximately ± 0.7 volts.

In an exemplary embodiment of the signal processing system 400 of Fig. 4, the signal strength detector 410 can be implemented by using the signal strength detector 1200 shown in Fig. 12. Referring to Fig. 12(a), the input 1202 of the signal strength detector 1200 may serve as the input 434 of the signal strength detector 410 and the outputs 1240, 1242, 1244 of the signal strength detector 1200 mat serve as the outputs 477, 475, 473 of the signal strength detector 410, respectively. Also, the first threshold detector 1175 may be adjusted to reflect the first limit, and the second threshold detector 1176 may be adjusted to reflect the second limit. The reference current of the current source 1170 of the first threshold detector 1175 can be 11 micro-amperes, and the reference current of the current source 1170 of the second threshold detector 1176 can be 110 micro-amperes.

Fig. 5(a) illustrates a signal processing system 500 according to another exemplary embodiment of the present invention. The characteristics of the signal processing system 500 can be changed dynamically. The signal processing system 500 includes an input 502, a first signal processing circuit 514, a second signal processing circuit 530, a signal strength detector 556, a bias selector 566, a timer 588, a first switch 540, a second switch 548 and an output 594.

A signal received by the input 502 of the signal processing system 500 is conveyed to an input 504 of the first signal processing circuit 514, and an input 520

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of the second signal processing circuit 530. The first signal processing circuit 514 includes the input 504, an input 506, an input 508, an input 510, a power input 512, an output 516 and an output 518. The first signal processing circuit 514 processes the signal received at its input 504 based on respective signals received at the inputs 506, 508, 510, 512, and outputs processed signals at its outputs 516, 518. The signal processing circuit 514 can be turned on and off by a signal applied to its power input 512. If a logical high signal is received at the power input 512, the first signal processing circuit 514 is turned on. Conversely, if a logical zero signal is received at the power input 512, the first signal processing circuit 514 is turned off. The output 516 of the first signal processing circuit 514 corresponds to input 552 of the signal strength detector 556. The output 518 of the first signal processing circuit 514 corresponds to input 536 of the first switch 540. The first switch 540 outputs the signal received at its input 536 on its output 542 when the signal received at its switch control input 538 is a logical one, and isolates its input 536 from its output 542 when the signal received at its switch control input 538 is a logical zero. The output 542 of the first switch 540 is connected to the output 594 of the signal processing system 500.

The second signal processing circuit 530 includes the input 520, an input 522, an input 524, an input 526, a power input 528, an output 532 and an output 534. The second signal processing circuit 530 processes the signal received at its input 520 based on respective signals received at the inputs 522, 524, 526, 528, and outputs processed signals at its outputs 532, 534. The second signal processing circuit 530 can be turned on and off by a signal applied to the input 528. If a logical high signal is received at the power input 528, the second signal processing circuit 530 is turned on. Conversely, if a logical zero signal is received at the power input 528, the second signal processing circuit 530 is turned off. The output 532 of the second signal processing circuit 530 corresponds to input 554 of the signal strength detector 556. The output 534 of the second signal processing circuit 530 corresponds to input 544 of the second switch 548. The second switch 548 outputs the signal received at its input 544 on its output 550 when the signal received at its switch control input 546 is a logical one, and isolates its input 544 from its output 550 when the signal received

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at its switch control input 546 is a logical zero. The output 550 of the second switch 548 is connected to the output 594 of the signal processing system 500.

The signal strength detector 556 selects the most suitable bias for the inactive signal processing circuit 514 or 530 (i.e., the one of the first and second signal processing circuits 514, 530 that does not have its output 518, 534 connected to the system output 594) for processing the signal received from an internal node of the active signal processing circuit (i.e., the one of the first and second signal processing circuits 514, 530 having its output 518, 534 connected to the system output 594) of the signal processing circuits 514, 530 at the inputs 552, 554 of the signal strength detector 556 based on the voltage envelope of the signal received from the active signal processing circuit 514 or 530. The amplitude or envelope signal can be derived using an envelope detector. A low-pass-filtered rectifier, well-known for use in many other applications, is one example of a circuit which can be used as an envelope detector. The first and second signal processing circuits 514 and 530 can be biased so that the signal processing circuits 514, 530 have a high effective range, (i.e., the filter works in a satisfactory way for a range of large signals between saturation and the noise floor of the filter) with a third bias, a medium effective range (i.e., the filter works in a satisfactory way for a range of medium signals between saturation and the noise floor of the filter), with a second bias, and a low effective range (i.e., the filter works in a satisfactory way for a range of small signals between saturation and the noise floor of the filter), with a first bias. The signal strength detector 556 selects the appropriate bias based upon a first limit and a second limit. The second limit indicates the onset of saturation of the active signal processing circuit. The first limit indicates that the signal from the internal node of the active signal processing circuit 514 or 530 is approaching the minimum tolerable signal to noise ratio of the active signal processing circuit 514 or 530. The outputs 558, 560 the signal strength detector 556 indicate the appropriate bias as determined by the strength detector 556. The signal strength detector 556 drives the output 558 to a logical zero and the output 560 to a logical zero if the voltage envelope of the signal received from the active signal processing circuit 514 or 530 does not exceed the first limit or the second limit. The signal strength detector 556 drives the output 558 to a logical zero and the output 560

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to a logical one if the voltage envelope of the signal received from the active signal processing circuit 514 or 530 exceeds the first limit but does not exceed the second limit. And, the strength detector 556 drives the output 558 to a logical one and the output 560 to a logical one if the voltage envelope of the signal received from the active signal processing circuit 514 or 530 exceeds the first limit and the second limit. The outputs 558, 560 of the signal strength detector 556 are connected to inputs 562, 564 of a bias selector 566.

The bias selector 566 provides signals that indicate the bias setting for each of the first and second signal processing circuits 514, 530. The bias selector includes the input 562, the input 564, an input 565, an input 567, an input 569, an output 568, an output 570, an output 572, an output 574, an output 576, an output 578, and an output 584. The outputs 568, 670, 572 of the bias selector 566 are connected to the inputs 506, 508, 510, respectively, of the first signal processing circuit 514. The outputs 574, 576, 578 of the bias selector 566 are connected to the inputs 522, 524, 526, respectively, of the second signal processing circuit 530, and the output 584 of the bias selector 566 corresponds to input 586 of a timer 588. The outputs 568, 570, 572 of the bias selector 566 indicate the bias setting for the first signal processing circuit 514, and the outputs 574, 576, 578 of the bias selector 566 indicate the bias setting for the second signal processing circuit 530. The input 565 indicates when the timer 588 has completed the transition from one of the first and second signal processing circuits 514, 530 to the other of the first and second signal processing circuits 514, 530. The inputs 567, 569 indicate the current state of the timer 588.

The bias selector 566 transmits the bias setting for the active signal processing circuit 514 or 530 to the active signal processing circuit 514 or 530. If the strength detector 556 indicates that the appropriate bias setting is different than the bias setting of the active signal processing circuit 514 or 530, the bias selector 566 transmits the appropriate bias setting to the inactive signal processing circuit (i.e., the one of the first and second signal processing circuits 514, 430 not having its output 518, 534 connected to the system output 594). The timer 588 eventually changes the inactive signal processing circuit into the active signal processing circuit, and the active signal processing circuit into the inactive signal processing circuit. Once the

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timer 588 completes this transition, the bias selector 566 discontinues providing the inactive signal processing circuit with a bias setting.

The timer 588 provides signals that selectively connect and disconnect the first and second signal processing circuits 514, 530 to and from the system output 594 of the signal processing system 500, and selectively turn the first and second signal processing circuits 514, 530 on and off. The timer 588 includes the input 586, an output 580, an output 582, an output 590, an output 592, an output 587, an output 589 and an output 591. The outputs 580, 582 of the timer 588 are connected to the inputs 528, 512, of the first and second signal processing circuits 530, 514, respectively. The outputs 590, 592 of the timer 588 are connected to the switch control inputs 538, 546, of the first and second switches 540, 548, respectively. The timer 588 provides signals that cause only one of the outputs 518, 534 of one of the first and second signal processing circuits 514, 530, to be connected to the system output 594 of the signal processing system 500 at any one time.

The timer 588 provides signals to the first and second switches 540, 548 and the first and second signal processing circuits 514, 530 that allow the system output 594 to switch between output 518, 534 of the first signal processing circuit 514 and the second signal processing circuit 530 without causing transients to appear at the system output 594 of the signal processing system 500. To switch from the output of one signal processing circuit to the output of the other signal processing circuit, the timer 558 provides a signal at the output 580, 582 to turn on the first or second signal processing circuit 530, 514 selected by the bias selector 566. If the bias selector 566 selected the first signal processing circuit 514, and the second signal processing circuit 530 is connected to the system output 594, the timer 588 turns on the first signal processing circuit 514 by providing first a logical one on its output 582. If the bias selector 566 selected the signal processing circuit 530, and the signal processing circuit 514 is connected to the system output 594, the timer 588 turns on the second signal processing circuit 530 by providing a logical one on the output 580.

After the first or second signal processing circuit 514, 530 selected by the signal strength detector 588 is turned on, the timer 588 waits a length of time sufficient for transients at the outputs 518, 534 of the first and second signal

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processing circuits 514, 530, to die out. After the length of time elapses, the timer 588 connects the output 518, 534 of the first or second signal processing circuit 514, 530, indicated by the bias selector 566, to the system output 594 of the signal processing system 500. If the bias selector 566 selected the first signal processing circuit 514, the timer 588 closes the first switch 540 by providing a logical one on the output 590, and opens the second switch 548 by providing a logical zero on the output 592. If the bias selector 566 selected the second signal processing circuit 530, the timer 588 closes the second switch 548 by providing a logical one on its output 592, and opens the first switch 540 by providing a logical zero on its output 590.

In an alternate exemplary embodiment, more than two signal processor circuits are provided for selective connection between the system input 502 and the system output 594 of the signal processing system 500 with appropriate modifications to the signal strength detector 556, the bias selector 566, and the timer 588.

In another alternate exemplary embodiment, the first and second signal processing circuits 514, 530 are not turned off, but are placed in a standby mode whereby they consume less power than when they are fully on. Placing the first and second signal processing circuits 514, 530 in a standby mode reduces the length of time the timer 588 has to wait before the transients at the outputs 518, 534, of the first and second signal processing circuits 514, 530 die out, therefore speeding up switching time.

In an exemplary embodiment, the first signal processing circuit 514 can be the signal processing circuit 1500 illustrated in Fig. 15. The input 504 of the first signal processing circuit 514 becomes an input 1502 of the signal processing circuit 1500, the input 506 becomes an input 1504, the input 508 becomes an input 1506, the input 510 becomes an input 1508, the input 512 becomes an input 1523, and the output 518 becomes an output 1520. The signal processing circuit 1500 includes a dynamic input scaling unit 1518, a biquad 1526, and a dynamic output scaling unit 1538.

A signal received at the input 1502 of the signal processing circuit 1500 is conveyed to an input 1510 of the dynamic input scaling unit 1518; a signal received at the input 1504 is conveyed to an input 1512 of the dynamic scaling unit

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1518 and an input 1532 of the dynamic output scaling unit 1538; a signal received at the input 1506 is conveyed to an input 1514 of the dynamic input scaling unit 1518 and an input 1534 of the dynamic output scaling unit 1538; a signal received at the input 1508 is conveyed to an input 1516 of the dynamic input scaling unit 1518 and an input 1536 of the dynamic output scaling unit 1538; and a signal received at the input 1523 is conveyed to an input 1524 of the biquad 1526. The dynamic input scaling unit 1518 processes the signal received at the input 1510 and provides a signal at an output 1520 of the dynamic input scaling unit 1518 based on the signal received at the input 1510 and the signals received at the inputs 1504, 1506, 1508. The output 1520 corresponds to input 1522 of the biquad 1526.

The biquad 1526 processes the signal received at its input 1522 and produces a signal at its output 1528 if the signal received at the input 1524 is a logical one. If the signal received at the input 1524 is a logical zero, the biquad 1526 does not produce a signal at the output 1528. The output 1528 of the biquad 1526 is connected to the input 1530 of the dynamic output scaling unit 1538.

The dynamic output scaling unit 1538 processes the signal received at the input 1530 and provides a signal at its output 1540 based on the signal received at the input 1530 and the signals received at inputs 1532, 1534, 1536. The output 1540 is connected to the output 1542 of the signal processing circuit 1500.

In an exemplary embodiment, the dynamic input scaling unit 1518 can be the dynamic input scaling unit 1700 illustrated in Fig. 17. The input 1512 of the dynamic input scaling unit 1518 corresponds to input 1702 of the dynamic input scaling unit 1700, the input 1516 corresponds to an input 1708, the input 1510 corresponds to input 1704, and the output 1520 becomes an output 1756. The dynamic input scaling unit 1700 includes a first switch 1714, a second switch 1734, a first resistor 1720, a second resistor 1726, a first transconductor 1742, and a second transconductor 1752.

A signal received at the input 1702 of the dynamic input scaling unit 1700 is conveyed to an inverted switch control input 1710 of the first switch 1714, and an input 1732 of the second switch 1734; a signal received at the input 1704 is conveyed to one terminal 1718 of the first resistor 1720 and an input 1712 of the first

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switch 1714; and an input 1708 is conveyed to a switch input 1750 of the transconductor 1752. The first switch 1714 connects its input 1712 to its output 1716 if the signal received at the inverted switch control input 1710 is a logical zero. If the signal at the inverted switch-control input 1710 is a logical one, the first switch 1714 disconnects its input 1712 from its output 1716 resulting in an open circuit. The first resistor 1720 is connected between the input 1712 signal received at the input 1718 of the and the output 1716 of the first switch 1714. The output 1716 of the first switch 1714 and the other terminated 1722 of the first resistor 1720 are both connected to one terminal 1724 of the second resistor 1726, a positive input 1738 of the first transconductor 1742, and a positive input 1746 of the second transconductor 1752. The first switch 1714 and the first resistor 1720 form one half of a voltage divider, which is used to adapt a filter to be useful over a high effective range.

The other terminal 1728 of the second resistor 1726 corresponds to input 1730 of the second switch 1734. The second switch 1734 connects its input 1730 to its output 1736 if the signal received at the switch control input 1732 is a logical one. If the signal at the switch control input 1732 is a logical zero, the second switch 1734 disconnects its input 1730 from its output 1736 resulting in an open circuit. The second switch 1734 and the second resistor 1726 form the other half of the voltage divider used to adapt signal processing circuit 1500 to have a high effective range.

The first transconductor 1742 processes the difference between the signal received at its positive input 1738 and the signal received at its negative input 1740, which is connected to ground, and provides a signal at its output 1744. The signal at the output 1744 of the first transconductor 1742 is equal to the difference in the signal received by the positive input 1738 of the first transconductor 1742 and the signal received by its negative input 1740, scaled by a transconductance G_m of the first transconductor 1742. The output 1744 of the first transconductor 1742 corresponds to output 1754 of the second transconductor 1752, and the output 1756 of the dynamic input scaling unit 1518. When the first switch 1714 is closed, the switch 1734 is open, and the second transconductor 1752 is off (as a result of a logical zero

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signal received at its control input 1750), the voltage output of the first transconductor 1742 adapts the signal processing circuit 1500 to a medium effective range.

If a logical one signal is received at the control terminal 1750 of the second transconductor 1752, it processes the difference between the signal received at its positive input 1746 and the signal received at its negative input 1748, which is connected to ground, and provides a signal at the output 1754. If the signal at its control input 1750 is a logical zero, the second transconductor 1752 acts as an open circuit between its input 1746 and its output 1754. If the signal at the control input 1750 is a logical one, the signal at the output 1754 of the second transconductor 1752 is equal to the difference in the signal received by its positive input 1746 and the signal received by its negative input 1748, scaled by a transconductance $9G_m$ of the second transconductor 1752. The output 1754 of the second transconductor 1752 is connected to the output 1744 of the first transconductor 1742, and to the output 1756 of the dynamic input scaling unit 1518. When the second transconductor 1752 is on, i.e. when the signal at its control input 1750 is a logical one, the voltage output of the transconductor 1752 combines with the voltage output of the transconductor 1742 to adapt a signal processing circuit to have a low effective range.

Referring again to Fig. 15, the biquad 1526 of the signal processing circuit 1500 can be the biquad 1600 illustrated in Fig. 16. Turning to Fig. 16, the biquad 1600 includes a first transconductor 1614, a second transconductor 1622, a third transconductor 1630, a fourth transconductor 1644, a first capacitor 1606, and a second capacitor 1636. The center frequency Wo of the biquad 1600 can be calculated equation (1). The absolute value of the transconductors and capacitors can be scaled by the same factor, i.e. impedance scaling, without affecting the transfer function of the biquad 1600, since the transfer function depends on the ratios between these values. Impedance scaling does not change the transfer function of the biquad 1600, however it does change the power dissipation and the noise level of the biquad 1600.

A signal received by the input 1602 of the biquad 1600 is conveyed to one terminal 1604 of the capacitor 1606, a negative input 1610 of the first transconductor 1614, an output 1616 of the first transconductor 1614, a positive input

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1618 of the second transconductor 1622, and an output 1632 of the third transconductor 1630. These connections form a node 1617. The other terminal 1608 of the first capacitor 1606 is connected to ground. The first capacitor 1606 buffers the first node 1074 by being connected to ground through the capacitor 1606.

If its control input 1652 receives a logical one signal, the first transconductor 1614 processes the difference between the signal received at its positive input 1612, which is connected to ground, and the signal received at its negative input 1610, and provides a signal at its output 1616. The signal at the output 1616 is equal to the difference between the signal received by the positive input 1610 and the signal received by the negative input 1612, scaled by a transconductance G_m of the first transconductor 1614 if the signal received at the control input 1652 is a logical one. If the signal received at the control input 1652 is a logical zero, the output 1616 of the first transconductor 1614 acts as an open circuit. The output 1616 of the transconductor 1614 is connected to one terminal 1604 of the first capacitor 1606, the negative input 1610 of the first transconductor 1614, the positive input 1618 of the second transconductor 1622, and the output 1632 of the third transconductor 1630. The transconductor 1614 forms a feedback loop at the node 1617.

If its control input 1656 receives a logical one signal, the transconductor 1622 processes the difference between the signal received at its positive input 1618 and the signal received at its negative input 1620, which is connected to ground, and outputs a signal at its output 1624. The signal at the output 1624 is equal to the difference between the signal received by the positive input 1618 and the signal received by the negative input 1620, scaled by a transconductance QG_m of the second transconductor 1622 if the signal received at the control input 1656 is a logical one. If the signal received at the input 1656 is a logical zero, the output 1624 of the second transconductor 1622 acts as an open circuit. The output 1624 of the second transconductor 1622 is connected to one terminal second 1634 of the second capacitor 1636, the negative input 1626 of the third transconductor 1630, and the positive input 1640 of the fourth transconductor 1644. These connections form a node 1625. The other terminal 1638 of the capacitor 1636 is connected to ground so as to buffer node 1625.

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If its second control input 1654 receives a logical one signal the third transconductor 1630 processes the difference between the signal received at its positive input 1628, which is connected to ground, and the signal received at its negative input 1626 and outputs a signal at its output 1632. The signal at the output 1632 is equal to the difference between the signal received by the positive input 1628 and the signal received by the negative input 1626, scaled by a transconductance QG_m of the third transconductor 1630 if the signal received at the control input 1654 is a logical one. If the signal received at the input 1654 is a logical zero, the output 1632 of the third transcondutor 1630 acts as an open circuit. The output 1632 of the third transconductor 1630 is connected to one terminal 1604 of the capacitor 1606, the negative input 1610 of the first transconductor 1614, the output 1616 of the first transconductor 1614, and the positive input 1618 of the second transconductor 1622. The second and third transconductors 1622, 1630 form a feedback loop at the node 1617.

If its control input 1658 receives a logical one signal, the fourth transconductor 1644 processes the difference between the signal received at its positive input 1640 and the signal received at its negative input 1642, which is connected to ground, and provides a signal at its output 1646. The signal at the output 1646 is equal to the difference in the signal received by the positive input 1640 and the signal received by the negative input 1642 of the fourth transconductor 1644, scaled by a transconductance QG_m of the fourth transconductor 1644 if the signal at its control input 1658 is a logical one. If the signal received at the control input 1658 is a logical zero, the output 1646 of the fourth transconductor acts as an open circuit. The output 1646 of the fourth transconductor 1644 corresponds to output 1648 of the biquad 1600.

In an exemplary embodiment, a first diode and a second diode are connected to the node 1617. The cathode of the first diode is connected to the node 1617, and the anode of the first diode is connected to ground. The anode of the second diode is connected to the node 1617, and the cathode of the second diode is connected to ground. The first and second diodes serve to limit the voltage swing at node 1617 to approximately ±0.7 v.

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In an exemplary embodiment, a first diode and a second diode are connected to the node 1625. The cathode of the first diode is connected to the node 1625, and the anode of the first diode is connected to ground. The anode of the second diode is connected to the node 1625, and the cathode of the second diode is connected to ground. The first and second diodes serve to limit the voltage swing at node 1625 to approximately ±0.7 v.

In an alternative exemplary embodiment, the dynamic output scaling unit 1538 can be the dynamic output scaling unit 1800 illustrated in Fig. 18. The input 1530 of the dynamic output scaling unit 1538 corresponds to input 1802 of the dynamic output scaling unit 1800, the input 1532 corresponds to input 1804; the input 1534 corresponds to input 1806, the input 1536 corresponds to input 1808, and the output 1540 corresponds to output 1852. The dynamic output scaling unit 1800 includes a first resistor 1812, a first switch 1820, a second resistor 1826, a second switch 1834, a third resistor 1840, and a third switch 1848.

A signal received at the input 1802 of the dynamic output scaling unit 1800 is applied to one terminal 1810 of the first resistor 1812, one terminal 1824 of the second resistor 1826, and one terminal 1838 of the third resistor 1840. A signal received at the input 1804 is conveyed to a switch control input 1846 of the third switch 1848; a signal received at the input 1806 is conveyed to a switch control input 1832 of the second switch 1834; and a signal received at the input 1808 is conveyed to its terminal input 1818 of the first switch 1820. The first resistor 1812 couples the signal applied to its terminal 1810 to input 1816 of the first switch 1820. The first switch 1820 connects its input 1816 to its output 1822 if the signal received at the switch control input 1818 is a logical one. If the signal at the switch control input 1818 is a logical zero, the first switch 1820 disconnects its input 1816 from its output 1822 resulting in an open circuit between the input and its output. The output 1822 of the first switch 1820 is connected to ground. The resistor 1812 and the switch 1820 form an effective amplifier which provides a relatively small gain for the signal received at the input 1802, which is used to adapt the signal processor circuit 1500 to have a low effective range.

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The second resistor 1826 couples the signal applied to its terminal 1824 to an input 1830 of the second switch 1834. The second switch 1834 connects its input 1830 to its output 1836 if the signal received at the switch control input 1832 is a logical one. If the signal at the switch control input 1832 is a logical zero, the switch 1834 disconnects its input 1830 from its output 1836 resulting in an open circuit between the input and the output. The output 1836 of the second switch 1834 is connected to ground. The resistor 1826 and the switch 1834 form an effective amplifier which provides a medium gain for the signal received at the input 1802, which is used to adapt the signal processing circuit 1500 to have a medium effective range.

The third resistor 1840 couples the signal applied to its terminal 1838 to the input 1844 of the third switch 1848. The switch 1848 connects its input 1844 to its output 1850 if the signal received at the switch control input 1846 is a logical one. If the signal at the switch control input 1846 is a logical zero, the third switch 1848 disconnects its input 1844 output 1850 resulting in an open circuit between the input and the output. The output 1850 of the third switch 1848 is connected to ground. The resistor 1840 and the switch 1848 form an effective amplifier which provides a relatively large gain for the signal received at the input 1802, which is used to adapt the signal processing circuit 1500 to have a high effective range.

In an exemplary embodiment, the signal strength detector 556 of the signal processing circuit 1500 of Fig. 15 is described in Fig. 21 as signal strength detector 2100. The signal strength detector 2100 senses the voltage envelope of the selected input signal of the inputs 552, 554 (shown in Fig. 5), and selects an appropriate signal processing circuit 514, 530 based on a first and a second threshold limit. An input signal is selected when a first switch 2106 or a second switch 2114 is closed. The first threshold limit represents a point at which the signal received from the active signal processing circuit 514 or 530 is near its minimum tolerable signal to noise ratio. The second threshold limit represents a point at which the active signal processing circuit 514 or 530 is near saturation. The signal strength detector 2100 includes the first switch 2106, the second switch 2114, a peak detector 2120, a first threshold detector 2126, and a second threshold detector 2134. The peak detector

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2120, the first threshold detector 2126, and the second threshold detector 2134 are described in more detail above in relation to Fig. 11.

A signal received at the input 554 is conveyed to the input 2102 of the first switch 2106; a signal received at the input 552 is conveyed to an input 2110 of the second switch 2114; and a signal received at the input 593 is conveyed to a switch control input 2104 of the first switch 2106 and an inverted switch control input 2112 of the second switch 2114. If the signal received at the input 593 is a logical one, the first switch 2106 closes connecting the signal received at its input 2102 to its output 2108 and the second switch 2114 opens. The output 2108 of the first switch 2106 is connected to the input 2118 of a peak detector 2120. If the signal received at the input 593 is a logical zero, the second switch 2114 closes connecting the signal received at its input 2110 and to its 2116, and the first switch 2106 closes. The output of the second switch 2114 is connected to the input 2118 of the peak detector 2120.

The peak detector 2120 processes the signal received at its input 2118 and provides a signal at its output 2122. The signal output at the output 2122 is conveyed to the input 2124 of a first threshold detector 2126 and the input 2132 of a second threshold detector 2134. The first threshold detector 2126 provides a logical one signal at its output 2128 if the signal at its input 2124 exceeds the first threshold limit, and provides a logical zero signal on its output 2128 if the signal at its input 2124 does not exceed the first threshold limit. The output 2128 of the first threshold detector 2126 is connected to the output 558 of the signal strength detector 2100. The second threshold detector 2134 provides a logical one signal on its output 2136 if the signal at its input 2132 exceeds the second threshold limit, and provides a logical zero signal on its output 2136 if the signal at its input 2132 does not exceed the second threshold limit. The output 2136 of the second threshold detector 2134 is connected to the output 560 of the strength detector 2100.

The first threshold detector 2126, which is similar to the first threshold detector 1175 shown in Fig. 11, is configured to detect the first limit. Referring to Fig. 11, the current source 1170 of the threshold detector 2126 produces a reference current that represents the first limit. The reference current provided by its current source 1170 of the first threshold detector 2126 can be 11 micro-amperes. The

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second threshold detector 2136, which is also similar to the first threshold detector 1175 shown in Fig. 11, is configured to detect the second limit. The current source 1170 of the threshold detector 2134 produces a reference current that represents the second limit. The reference current provided by the current source 1170 of the second threshold detector 2134 can be 110 micro-amperes.

In an exemplary embodiment, the bias selector 566 (shown in Fig. 5) can be the bias selector 1900 as described in Figs. 19 and 20. The bias selector 1900 indicates the bias setting for the first and second signal processing circuits 514, 530, and when the timer 588 (shown in Fig. 5) should switch the active signal processing circuit from one signal processing circuit to the other signal processing circuit.

Referring to Fig. 19, signals received at the inputs 562, 564 are conveyed to an array of AND gates, and a signal received at the input 1906 is conveyed to the clock inputs 1944, 1952 and 1960 of positive edge triggered D-type flip flops 1946, 1954 and 1962, respectively. The data output 1948 of the positive edge triggered D-type flip flop 1946 is connected to the output 584 of the bias selector 566.

A five input AND gate 1908 processes the inverse of a signal from the data output 1948 of the positive edge triggered D-type flip flop 1946, the inverse of a signal from the data output 1956 of the positive edge triggered D-type flip flop 1954, the inverse of a signal from the data output 1964 of the positive edge triggered D-type flip flop 1962, the inverse of a signal by the input 562, and the inverse of a signal received by the input 564, and produces an output which is provided to a respective input of a four input OR gate 1920. A five input AND gate 1910 processes the inverse of the signal from the data output 1948 of the positive edge triggered D-type flip flop 1946, the inverse of the signal from the data output 1956 of the positive edge triggered D-type flip flop 1954, the signal from the data output 1964 of the positive edge triggered D-type flip flop 1962, the signal received by the input 562, and the signal by the input 564, and produces an output which is provided to a respective input of the four input OR gate 1920. A five input AND gate 1914 processes the inverse of the signal from the data output 1948 of the positive edge triggered D-type flip flop 1946, the signal from the data output 1956 of the positive edge triggered D-

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type flip flop 1954, the inverse of the signal from the data output 1964 of the positive edge triggered D-type flip flop 1962, the signal received by the input 562, and the signal received by the input 564, and produces an output which is provided to a respective input of the four input OR gate 1920. A five input AND gate 1916 processes the inverse of the signal from the data output 1948 of the positive edge triggered D-type flip flop 1946, the inverse of the signal from the data output 1956 of the positive edge triggered D-type flip flop 1954, the signal from the data output 1964 of the positive edge triggered D-type flip flop 1962, the inverse of the signal received by the input 562, and the inverse of the signal by the input 564, and produces an output which is provided to a respective input of the four input OR gate 1920. The four input OR gate 1920 processes the signals received at its inputs and produces an output which is provided to the data input 1942 of the positive edge triggered D-type flip flop 1946.

A five input AND gate 1924 processes the inverse of the signal from the data output 1948 of the positive edge triggered D-type flip flop 1946, the inverse of the signal from the data output 1956 of the positive edge triggered D-type flip flop 1954, the signal from the data output 1964 of the positive edge triggered D-type flip flop 1962, the signal received by the input 562, and the signal received by the input 564, and produces an output which is provided to a respective input of a two input OR gate 1930. A five input AND gate 1926 processes the signal from the data output 1948 of the positive edge triggered D-type flip flop 1946, the inverse of the signal from the data output 1956 of the positive edge triggered D-type flip flop 1954, the inverse of the signal from the data output 1964 of the positive edge triggered D-type flip flop 1962, the inverse of the signal by the input 562 and the inverse of the signal received by the input 564, and produces an output which is provided to a respective input of the two input OR gate 1930. The two input OR gate 1930 processes the signals received at its inputs and produces an output which is provided to the data input 1950 of the positive edge triggered D-type flip flop 1954.

A five input AND gate 1932 processes the inverse of the signal from the data output 1948 of the positive edge triggered D-type flip flop 1946, the inverse of the signal from the data output 1956 of the positive edge triggered D-type flip flop

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1954, the signal from the data output 1964 of the positive edge triggered D-type flip flop 1962, the inverse of the signal by the input 562, and the inverse of the signal by the input 564, and produces an output which is provided to a respective input of a three input OR gate 1940. A five input AND gate 1934 processes the signal from the data output 1948 of the positive edge triggered D-type flip flop 1946, the signal from the data output 1956 of the positive edge triggered D-type flip flop 1954, the inverse of the signal from the data output 1964 of the positive edge triggered D-type flip flop 1962, the inverse of the signal received by the input 562, and the inverse of the signal received by the input 564, and produces an output which is provided to a respective input of the three input OR gate 1940. A five input AND gate 1936 processes the signal from the data output 1948 of the positive edge triggered D-type flip flop 1946, the inverse of the signal received from the data output 1956 of the positive edge triggered D-type flip flop 1954, the signal received from the data output 1964 of the positive edge triggered D-type flip flop 1962, the signal received by the input 562 and the signal received by the input 564, and produces an output which is provided to a respective input of the three input OR gate 1940. The three input OR gate 1940 processes the signals received at its inputs and produces an output which is provided to the data input 1958 of the positive edge triggered D-type flip flop 1960.

A three input AND gate 1966 processes the inverse of the signal from the data output 1948 of the positive edge triggered D-type flip flop 1946, the inverse of the signal from the data output 1956 of the positive edge triggered D-type flip flop 1954, and the inverse of the signal from the data output 1964 of the positive edge triggered D-type flip flop 1962, and produces an output which is provided to one input of a two input OR gate 1970. A three input AND gate 1968 processes the signal from the data output 1948 of the positive edge triggered D-type flip flop 1946, the signal from the data output 1956 of the positive edge triggered D-type flip flop 1954, and the inverse of the signal from the data output 1964 of the positive edge triggered D-type flip flop 1962, and produces an output which is provided to the other input of the two input OR gate 1970. The two input OR gate 1970 processes the signals received at its inputs and produces an output signal at its output 1972 which is

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provided to the data input 2002 of a positive edge triggered D-type flip flop 2006, shown in Fig. 20.

A three input AND gate 1974 processes the inverse of the signal from the data output 1948 of the positive edge triggered D-type flip flop 1946, the inverse of the signal from the data output 1956 of the positive edge triggered D-type flip flop 1954 and the signal from the data output 1964 of the positive edge triggered D-type flip flop 1962, and produces an output which is provided to one input of a two input OR gate 1978. A three input AND gate 1976 processes the signal from the data output 1948 of the positive edge triggered D-type flip flop 1946, the inverse of the signal from the data output 1956 of the positive edge triggered D-type flip flop 1954, and the inverse of the signal from the data output 1964 of the positive edge triggered D-type flip flop 1962, and produces an output which is provided to the other input of the two input OR gate 1978. The two input OR gate 1978 processes the signals received at its inputs and produces an output signal at its output 1980 which is provided to the data input 2010 of a positive edge triggered D-type flip flop 2014, shown in Fig. 20.

A three input AND gate 1982 processes the inverse of the signal from the data output 1948 of the positive edge triggered D-type flip flop 1946, the signal received from the data output 1956 of the positive edge triggered D-type flip flop 1954, and the inverse of the signal from the data output 1964 of the positive edge triggered D-type flip flop 1962, and produces an output which is provided to one input of a two input OR gate 1986. A three input AND gate 1984 processes the signal from the data output 1948 of the positive edge triggered D-type flip flop 1946, the inverse of the signal from the data output 1956 of the positive edge triggered D-type flip flop 1954 and the signal from the data output 1964 of the positive edge triggered D-type flip flop 1962, and produces an output which is provided to the other input of the two input OR gate 1986. The two input OR gate 1986 processes the signals received at its inputs and produces an output signal at its output 1988 which is provided to the data input 2018 of a positive edge triggered D-type flip flop 2022, shown in Fig. 20.

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Referring now to Fig. 20, a signal received at an input 565 is conveyed to the clock input 2004 of the positive edge triggered D-type flip flop 2006, the clock input 2012 of the positive edge triggered D-type flip flop 2014, and a clock input 2020 of the positive edge triggered D-type flip flop 2006.

A two input AND gate 2026 processes the signal from the data output 2008 of the positive edge triggered D-type flip flop 2006, and the inverse of the signal received by the input 569 of the bias selector 566, and produces an output which is provided to one input of a two input OR gate 2030. A three input AND gate 2028 processes the signal from the output 1972 of the two input OR gate 1970 (shown in Fig. 19), the inverse of the signal received by the input 569 of the bias selector 566, and the signal received by the input 567 of the bias selector 566, and produces an output which is provided to the other input of the two input OR gate 2030. The two input OR gate 2030 processes the signals received at its inputs and produces an output signal at the output 572 of the bias selector 566.

A two input AND gate 2034 processes the signal from the data output 2016 of the positive edge triggered D-type flip flop 2014, and the inverse of the signal received by the input 569 of the bias selector 566, and produces an output which is provided to one input of a two input OR gate 2038. A three input AND gate 2036 processes the signal received from the output 1980 of the two input OR gate 1978 (shown in Fig. 19), the inverse of the signal received by the input 569 of the bias selector 566, and the signal received by the input 567 of the bias selector 566, and produces an output which is provided to the other input of the two input OR gate 2038. The two input OR gate 2038 processes the signals received at its inputs and produces an output signal at the output 570 of the bias selector 566.

A two input AND gate 2042 processes the signal from the data output 2024 of the positive edge triggered D-type flip flop 2022, and the inverse of the signal received by the input 569 of the bias selector 566, and produces an output which is provided to one input of a two input OR gate 2046. A three input AND gate 2044 processes the signal from the output 1988 of the two input OR gate 1986, the inverse of the signal received by the input 569 of the bias selector 566, and the signal received by the input 567 of the bias selector 566, and produces an output which is provided to

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the other input of the two input OR gate 2046. The two input OR gate 2046 processes the signals received at its inputs and produces an output signal at the output 568 of the bias selector 566.

A three input AND gate 2050 processes the signal from the output 1972 of the two input OR gate 1970, the signal received by the input 569 of the bias selector 566, and the inverse of the signal received by the input 567 of the bias selector 566, and produces an output which is provided to one input of the two input OR gate 2054. A two input AND gate 2052 processes the signal from the data output 2008 of the positive edge triggered D-type flip flop 2006, and the signal received by the input 569 of the bias selector 566, and produces an output which is provided to the other input of the two input OR gate 2054. The two input OR gate 2054 processes the signals received at its inputs and produces an output signal at the output 578 of the bias selector 566.

A three input AND gate 2058 processes the signal from the output 1980 of the two input OR gate 1982, the signal received by the input 569 of the bias selector 566 and the inverse of the signal received by the input 567 of the bias selector 566, and produces an output which is provided to one input of the two input OR gate 2062. A two input AND gate 2060 processes the signal from the data output 2016 of the positive edge triggered D-type flip flop 2014 and the signal received by the input 569 of the bias selector 566, and produces an output which is provided to the other input of the two input OR gate 2062. The two input OR gate 2062 processes the signals received at its inputs and produces an output signal at the output 576 of the bias selector 566.

A three input AND gate 2066 processes the signal from the output 1988 of the two input OR gate 1986, the signal received by the input 569 of the bias selector 566 and the inverse of the signal received by the input 567 of the bias selector 566, and produces an output which is provided to one input of the two input OR gate 2070. A two input AND gate 2068 processes the signal from the data output 2024 of the positive edge triggered D-type flip flop 2022 and the signal received by the input 569 of the bias selector 566, and produces an output which is provided to the other input of the two input OR gate 2070. The two input OR gate 2070 processes the

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signals received at its inputs and produces an output signal at the output 574 of the bias selector 566.

In an exemplary embodiment, the timer 588 can be the timer 1300 illustrated in Fig. 13. The input 586 of the timer 588 corresponds to the input 1302 of the timer 1300, and the outputs 580, 582, 590, 592 of the timer 588 correspond to the outputs 1319, 1309, 1394, 1399, respectively, of the timer 1300. The timer 1300 provides outputs 1309, 1319, 1394 and 1399 that selectively connect and disconnect the first and second signal processing circuits 514, 530 to and from the input 502 and the output 594 of the signal processing system 500, and selectively turn the first and second signal processing circuits 514, 530 on and off. The timer 1300 includes a first three input AND gate 1312, a second three input AND gate 1322, a third three input AND gate 1332, a fourth three input AND gate 1342, a first three input OR gate 1350, a second three input OR gate 1358, a third three input OR gate 1397, a two input NAND gate 1392, a two input NOR gate 1305, a two input AND gate 1315, a first D-type flip-flop 1366, a second D-type flip-flop 1374, an XOR gate 1382, and an n-bit overflow counter 1388. The timer 1300 is provided with two inputs: a signal strength detector input 1302 and a clock input 1304.

The first three input AND gate 1312, the second three input AND gate 1322, and the first three input OR gate 1350 combine to produce the most significant bit for the next state of the state machine. The first three input AND gate 1312 includes an inverting input 1306, an input 1308, an input 1310, and an output 1314. The inverting input 1306 is connected to an input 1316 of the second three input AND gate 1322, an inverting input 1326 of the third three input AND gate 1332, an inverting input 1336 of the fourth three input AND gate 1342, the data output 1368 of the first D-type flip-flop 1366, the input 1378 of the two input XOR gate 1382, the input 1390 of the two input NAND gate 1392, the input 1301 of the two input NOR gate 1305, the input 1311 of the two input AND gate 1315, and the input 1395 of the third three input OR gate 1397 are each connected to the output 589 of the timer 588. The input 1308 of the first three input AND gate 1312, the input 1318 of the second three input AND gate 1322, the inverting input 1328 of the third three input AND gate 1332, the input 1338 of the fourth three input AND gate 1342, the data output 1376 of

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the second D-type flip-flop 1374, the input 1380 of the two input XOR gate 1382, the input 1391 of the two input NAND gate 1392, the input 1313 of the two input AND gate 1315, the input 1303 of the two input NOR gate 1305, and the input 1396 of the third three input OR gate 1397 are each connected to the output 587 of the timer 588. The input 1310 of the first three input AND gate 1312, the input 1340 of the fourth three input AND gate 1342, and the counter overflow output 1389 of the n-bit overflow counter 1388, are each connected to the output 591 of the timer 588. The input 1320 of the third three input AND gate 1322 and the inverting input 1330 of the fourth three input AND gate 1332 are connected to the input 1302 of the timer circuit 1300. The clock input 1361 of the first negative edge triggered D-type flip-flop 1366, the clock input 132 of the second negative edge triggered D-type flip-flop 1374 and the clock input 1387 of the n-bit overflow counter 1388 are each connected to the clock input 1304 of the timer 1300.

The first three input OR gate 1350 includes the input 1346, the input 1348 and an output 1352. The input 1346 is connected to the output 1314 of the first three input AND gate 1312. The input 1348 is connected to the output 1324 of the second three input AND gate 1322. And the output 1352 of the first three input OR gate 1350 is connected to a data input 1362 of the first D-type flip-flop 1366.

The third three input AND gate 1332, the fourth three input AND gate 1342, and the second three input OR gate 1358 combine to produce the least significant bit for the next state of the state machine.

The second three input OR gate 1358 includes the input 1354, the input 1356 and the output 1360. The input 1354 is connected to the output 1334 of the third three input AND gate 1332. The input 1356 is connected to the output 1344 of the fourth three input AND gate 1342. And the output 1360 of the second three input OR gate 1358 is connected to the data input 1370 of the second D-type flip-flop 1374.

The first D-type flip-flop 1366 holds the most significant bit of the current state of the timer 1300 until the next negative edge of the clock signal received at the clock input 1304 of the timer 1300. The second D-type flip-flop 1374 holds the least significant bit of the current state of the timer 1300 until the next negative edge of the clock signal received at the clock input 1304 of the timer 1300.

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The two input XOR gate 1382 produces the signal that enables and resets the n-bit overflow counter 1388. The output 1384 of the two input XOR gate 1382 is connected to the enable/reset enable/reset input 1386 of the n-bit overflow counter 1388.

The n-bit overflow counter 1388 provides a signal that indicates when a given period of time has elapsed. The period of time is adjustable within the n-bit counter 1388, by configuring the reset conditions of the n-bit counter 1388 such that the period of time can be altered. The n-bit overflow counter 1388 includes the enable/reset input 1386, the clock input 1387, and the counter overflow output 1389. If the enable/reset input 1386 is a logical zero, the n-bit overflow counter 1388 is reset to zero. If the enable/reset input 1386 is a logical one, the n-bit overflow counter 1388 begins to count by increments of one at every falling edge of the clock signal received at the clock input 1387. The counter overflow output 1389 outputs a logical zero after the n-bit overflow counter 1388 is reset, and continues to output a logical zero until the n-bit overflow counter 1388 overflows. After the n-bit overflow counter 1388 overflows, the counter overflow output 1389 outputs a logical one until the n-bit overflow counter 1388 is reset. The n-bit overflow counter 1388 can be configured or the clock rate can be adjusted to allow for enough time from reset to overflow for the transients in the outputs 518, 534 of the signal processing circuits 514, 530 to die out.

The two input NAND gate 1392 produces a signal at its output 1393 that indicates when a signal processing circuit, having a higher effective range, should be turned on and connected to the input of the signal processing system. The two input NAND gate 1392 includes the input 1390, the input 1391, and an output 1393. The input 1390 of the two input NAND gate 1392 is connected to the inverting input 1306 of the first three input AND gate 1312, the input 1316 of the second three input AND gate 1322, the inverting input 1326 of the third three input AND gate 1332, the inverting input 1336 of the fourth three input AND gate 1342, the output 1368 of the first D-type flip-flop 1366, the output 589 of the timer 588, the input 1378 of the two input XOR gate 1382, the input 1305 of the two input NOR gate 1305, the input 1311 of the two input AND gate 1315, and the input 1395 of the third three input OR gate 1397. The input 1391 of the two input NAND gate 1392 is connected to the input

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1308 of the first three input AND gate 1312, the input 1318 of the second three input AND gate 1322, the inverting input 1328 of the third three input AND gate 1332, the input 1338 of the fourth three input AND gate 1342, the output 1376 of the second D-type flip-flop 1374, the output 587 of the timer 588, the input 1380 of the two input XOR gate 1382, the input 1313 of the two input AND gate 1315, the input 1303 of the two input NOR gate 1305, and an input 1396 of the third three input OR gate 1397. The output 1393 of the two input NAND gate 1392 is connected to the output 1394 of the timer 1300.

The third three input OR gate 1397 produces a signal that indicates when a signal processing circuit, having a lower effective range, should be turned on and connected to the input of the signal processing system. The two input OR gate 1397 includes the input 1395, the input 1396, and an output 1398. The input 1395 of the third three input OR gate 1397 is connected to the inverting input 1306 of the first three input AND gate 1312, the input 1316 of the second three input AND gate 1322, the inverting input 1326 of the third three input AND gate 1332, the inverting input 1336 of the fourth three input AND gate 1342, the output 1368 of the first D-type flip-flop 1366, the output 589 of the timer 588, the input 1378 of the two input XOR gate 1382, the input 1301 of the two input NOR gate 1305, the input 1311 of the two input AND gate 1315, and the input 1390 of the two input NAND gate 1392. The input 1395 of the third three input OR gate 1397 is connected to the input 1308 of the first three input AND gate 1312, the input 1318 of the second three input AND gate 1322, the inverting input 1328 of the third three input AND gate 1332, the input 1338 of the fourth three input AND gate 1342, the output 1376 of the second D-type flip-flop 1374, the output 587 of the timer 588, the input 1380 of the two input XOR gate 1382, the input 1303 of the two input NOR gate 1305, the input 1311 of the two input AND gate 1315, and the input 1391 of the two input NAND gate 1392. The output 1398 of the third three input OR gate 1397 is connected to the output 1399 of the timer 1300.

The two input NOR gate 1305 produces a signal that indicates when a signal processing circuit, having a higher effective range, should be connected to the output of a signal processing system. The two input NOR gate 1305 includes the input 1301, the input 1303, and an output 1307. The input 1301 of the two input NOR

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gate 1305 is connected to the inverting input 1306 of the first three input AND gate 1312, the input 1316 of the second three input AND gate 1322, the inverting input 1326 of the third three input AND gate 1332, the inverting input 1336 of the fourth three input AND gate 1342, the output 1368 of the first D-type flip-flop 1366, the output 589 of the timer 588, the input 1378 of the two input XOR gate 1382, the input 1390 of the two input NAND gate 1392, the input 1311 of the two input AND gate 1315, and the input 1395 of the third three input OR gate 1397. The input 1303 of the two input NOR gate 1305 is connected to the input 1308 of the first three input AND gate 1312, the input 1318 of the second three input AND gate 1322, the inverting input 1328 of the third three input AND gate 1332, the input 1338 of the fourth three input AND gate 1342, the output 1376 of the second D-type flip-flop 1374, the output 587 of the timer 588, the input 1380 of the two input XOR gate 1382, the input 1391 of the two input NAND gate 1392, the input 1313 of the two input AND gate 1315, and the input 1396 of the third three input OR gate 1397. The output 1307 of the two input NOR gate 1305 is connected to the output 1309 of the timer 1300.

The two input AND gate 1315 produces a signal that indicates when a signal processing circuit, having a lower effective range, should be connected to the output of a signal processing system. The two input AND gate 1315 includes the input 1311, the input 1313, and an output 1317. The input 1311 of the two input AND gate 1315 is connected to the inverting input 1306 of the first three input AND gate 1312, the input 1316 of the second three input AND gate 1322, the inverting input 1326 of the third three input AND gate 1332, the inverting input 1336 of the fourth three input AND gate 1342, the output 1368 of the first D-type flip-flop 1366, the output 589 of the timer 588, the input 1378 of the two input XOR gate 1382, the input 1390 of the two input NAND gate 1392, the input 1301 of the two input NOR gate 1305, and the input 1395 of the third three input OR gate 1397. The input 1313 of the two input AND gate 1315 is connected to the input 1308 of the first three input AND gate 1312, the input 1318 of the second three input AND gate 1322, the inverting input 1328 of the third three input AND gate 1332, the input 1338 of the fourth three input AND gate 1342, the output 1376 of the second D-type flip-flop 1374, the output 587 of the timer 588, the input 1380 of the two input XOR gate 1382,

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the input 1391 of the two input NAND gate 1392, the input 1303 of the two input NOR gate 1305, and the input 1396 of the third three input OR gate 1397. The output 1317 of the two input AND gate 1315 is connected to the output 1319 of the timer 1300.

Referring to Fig. 5(b), there is shown a signal processing system 599 according to another exemplary embodiment of the present invention. Unlike the signal processing system 500, the signal processing system 599 includes the input switch 505, the input switch 513, and the outputs 580, 582 of the timer 588 are not only connected to the power control inputs 528, 512 of the signal processing circuits 530, 514, respectively, but also to switch control inputs 519, 517 of the input switches 513, 505, respectively. A signal received by the input 502 is connected to a signal input 501 of the input switch 505 and a signal input 509 of the input switch 513. The input switch 505 includes the signal input 501, a grounded input 503, a switch output 507, and a switch control input 517. The input switch 505 connects the signal input 501 to the switch output 507 if the signal received at the switch control input 517 is a logical one, and connects the switch output 507 to the grounded input 503 if the signal received at the switch control input 517 is a logical zero. The switch 513 includes the signal input 509, a grounded input 511, a switch output 515, and a switch control input 519. The switch 513 connects the signal input 509 to the switch output 515 if the signal received at the switch control input 519 is a logical one, and connects the switch output 515 to the grounded input 511 if the signal received at the switch control input 519 is a logical zero.

Fig. 6 illustrates a further exemplary embodiment of a signal processing system 600 in accordance with the present invention. Whenever a large out-band component is present, relative to the in-band signal, in the signal at the input 602 of the signal processing system 600, a filter with a large signal-to-noise ratio (hereinafter "SNR") is needed to ensure that after the out-band component is filtered out of the signal the in-band component of the signal is still above the minimum tolerable signal to noise ratio of the filter. However, a filter with a large SNR consumes a relatively large amount of power during operation. When no large out-band component is present in the signal at the input of the signal processing system

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600, a filter with a lower SNR can be used, which consumes a smaller amount of power.

A signal received at the input 602 of the signal processing system 600 corresponds to input 601 of a signal processing circuit 604, and an input 603 of a signal processing circuit 606. The signal processing circuit 604 processes the signal received at the input 602 and outputs a processed signal at the output 607. The signal processing circuit 604 can be turned on and off by applying an appropriate signal to a power control input 615. If the signal received at the power input 615 is a logical one, the signal processing circuit 604 is turned on. Conversely, if the signal received at the power input 615 is a logical zero, the signal processing circuit 604 is turned off. The signal processing circuit 604 can process signals with large out-band components because the signal processing circuit 604 has a high SNR. The signal processing circuit 604 therefore introduces low amounts of noise to the processed signal. The output 607 of the signal processing circuit 604 corresponds to input 619 of a switch 612 and an input 641 of the signal strength detector 608. The switch includes the input 619, a switch control input 627, and a switch output 623. The switch output 623 of the switch 612 is connected to the output 616 of the signal processing system 600, and an output 625 of a switch 614.

The signal processing circuit 606 processes the signal received at the input 603 and outputs a processed signal at the output 609. The signal processing circuit 606 can be turned on and off by applying an appropriate signal to a power control input 617. If the signal received at the power control input 617 is a logical one, the signal processing circuit 606 is turned on. Conversely, if the signal received at the power control input 617 is a logical zero signal, the signal processing circuit 606 is turned off. The signal processing circuit 606 has a lower SNR than the signal processing circuit 604, and therefore introduces higher amounts of noise to the processed signal. The output 609 of the signal processing circuit 606 corresponds to input 621 of a switch 614 and an input 643 of the signal strength detector 608. The switch 614 includes the input 621, a switch control input 629, and the switch output 625. The switch output 625 of the switch 614 is connected to the output 616 of the signal processing system 600, and the output 623 of the switch 612.

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The signal strength detector 608 selects the filter bank that is the most suitable from the standpoint of SNR for processing the signal received by the input 602 of the signal processing system 600. The inputs 641, 643 of the signal strength detector 608 are connected to the outputs 607, 609 of the signal processing circuits 604, 606, respectively. The signal strength detector 608 can detect the voltage envelope of the signal at the input 641 of the strength detector 608 and the voltage envelope of the signal at the input 643 of the strength detector 608. A low-pass-filtered rectifier, well-known for use in many other applications, is one example of a circuit which can be used as an envelope detector. The signal strength detector 608 determines if the voltage envelope of the signal received at the input 641 exceeds a first limit, which represents a point near the minimum tolerable signal to noise ratio of the signal processing circuit 606, or if the voltage envelope of the signal received at the input 643 exceeds a second limit, which represents a point near the saturation point of the signal processing circuit 604. If the voltage envelope of the signal at the input 641 exceeds the first limit, or the voltage envdlope of the signal at the input 643 exceeds the second limit, the strength detector 608 provides a logical one on its output 611. If the voltage envelope of the signal at the input 641 does not exceed the first limit, and the voltage envelope of the signal at the input 643 does not exceed the second limit, the strength detector 608 transmits a logical one on its output 611.

The timer 610 provides signals that selectively connect and disconnect the signal processing circuits 604, 606 to and from the output 616 of the signal processing system 600, and selectively turn the signal processing circuits 604, 606 on and off. The timer 610 includes the input 639, a first power control first power control output 631, an second power control output 633, an first switch control output 635, and an second switch control output 637. The outputs 631, 633 of the timer 610 are connected to the power control inputs 615, 617 of the first and second signal processing circuits 604, 606, respectively. The first and second switch control outputs 635, 637 of the timer 610 are connected to the switch control inputs 627, 629 of the switches 627, 629, respectively. The timer 610 provides signals that cause only one of the outputs 607, 609 of one of the signal processing circuits 604, 606 to be connected to the output 616 of the signal processing system 600 at any one time.

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The timer 610 provides signals to the switches 612, 614 and the signal processing circuits 604, 606 that allow the signal processing system 600 to switch between the signal processing circuit 604 and the signal processing circuit 606 without causing transients to appear at the output 616 of the signal processing system 600. To switch from one signal processing circuit to the other signal processing circuit, the timer 610 provides respective signals at the power control outputs 631, 633 to turn on the signal processing circuit 604, 606 selected by the signal strength detector 608 and to turn off the signal processing circuit 604, 606 not selected by the signal strength detector 608. If the strength detector 608 selected the signal processing circuit 604, and the signal processing circuit 606 is connected to the output 616, the timer 610 turns on the signal processing circuit 604 by providing a logical one on the first power control output 631. If the strength detector 608 selected the signal processing circuit 606, and the signal processing circuit 604 is connected to the output 616, the timer 610 turns on the signal processing circuit 606 by providing a logical one on the second power control output 633.

After the signal processing circuit 604, 606 selected by the signal strength detector 608 is turned on, the timer 610 waits a length of time sufficient for transients at the output 607, 609 of the selected signal processing circuits 604, 606, to die out. After the length of time elapses, the timer 610 connects the output 607, 609 of the selected signal processing circuit 604, 606, indicated by the strength detector 608 to the output 616 of the signal processing system 600. If the strength detector 608 selected the signal processing circuit 606, the timer 610 closes the switch 614 by providing a logical one on the switch control second switch control output 637, and opens the switch 612 by providing a logical zero on the switch control first switch control output 635. After the signal processing circuit 614 is disconnected, the timer 610 provides a logical zero on its power control first power control output 631 to turn the disconnected circuit off. If the strength detector 608 selected the signal processing circuit 604, the timer 610 closes the switch 612 by providing a logical one on the switch control first switch control output 635, and opens the switch 614 by providing a logical zero on the switch control second switch control output 637.

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In a further exemplary embodiment, the signal processing circuit 606, shown in Fig. 6, can be a sixth order bandpass Chebychev filter 1400, shown in Fig. 14(a), with a ripple of 0.25 dB, a bandwidth of 0.5 MHz. The sixth order bandpass Chebychev filter 1400 can have a center frequency of 1.25 MHz. The sixth order bandpass Chebychev filter 1400 is constructed by connecting three on-off Tow-Thomas biquads together in series. An on-off Tow-Thomas biquad is constructed in the same manner as the standard Tow-Thomas biquad 800, shown in Fig. 8, with the exception that the transconductors of the on-off Tow-Thomas biquad are capable of being turned on and off, as described below with reference to Fig. 22.

Referring to Fig. 14(a), a signal received by the input 1402 of the sixth order bandpass Chebychev filter 1400 is conveyed to an input 1404 of a first on-off Tow-Thomas biquad 1406. Assuming that it is turned on, the on-off Tow-Thomas biquad 1406 processes the signal received at the input 1404 and provides a signal at its output 1408. The first on-off Tow-Thomas biquad 1406 that is turned on advantageously has a transconductance G_{in} for a transconductor 808 of 771 micro-amperes per volt, a transconductance G_m for a transconductor 824 of 185 micro-amperes per volt, a transconductance QG_m for transconductors 834 and 844 of 591 micro-amperes per volt, and a capacitance for capacitors 816, 854 of 77 picofarads. The output 1408 of the first on-off Tow-Thomas biquad 1406 is connected to the input 1410 of a second on-off Tow-Thomas biquad 1412.

Assuming that it is turned on, the second on-off Tow-Thomas biquad 1412 processes the signal received at the input 1410 and provides a signal at an output 1414. The second on-off Tow-Thomas biquad 1412 that is turned on advantageously has a transconductance G_{in} for the transconductor 808 of 2312 micro-amperes per volt, a transconductance G_m for the transconductor 824 of 185 micro-amperes per volt, a transconductance QG_m for the transconductors 834 and 844 of 1210 micro-amperes per volt, and a capacitance for the capacitors 816, 854 of 196 picofarads. The output 1414 of the second on-off Tow-Thomas biquad 1412 corresponds to input 1416 of a third on-off Tow-Thomas biquad 1418.

Assuming that it is turned on, the third on-off Tow-Thomas biquad 1418 processes the signal received at the input 1416 and provides a signal at an output

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1420. The third on-off Tow-Thomas biquad 1418 that is turned on advantageously has a transconductance G_{in} for the transconductor 808 of 971 micro-amperes per volt, a transconductance G_m for the transconductor 824 of 185 micro-amperes per volt, a transconductance QG_m for the transconductors 834 and 844 of 1210 micro-amperes per volt, and a capacitance for the capacitors 816, 854 of 126 picofarads. The output 1420 of the third on-off Tow-Thomas biquad 1418 corresponds to output 1422 of the sixth order bandpass Chebychev filter 1400.

In a further exemplary embodiment, the signal processing circuit 604, shown in Fig. 6, can be a sixth order bandpass Chebychev filter 1450, shown in Fig. 14(b), with a ripple of 0.25 dB, a bandwidth of 0.5 MHz. The sixth order bandpass Chebychev filter 1450 can have a center frequency of 1.25 MHz. The sixth order bandpass Chebychev filter 1450 is constructed by connecting three on-off Tow-Thomas biquads together in series.

Referring to Fig. 14(b), a signal received by the input 1452 of the sixth order bandpass Chebychev filter 1450 is conveyed to an input 1454 of a first on-off Tow-Thomas biquad 1456. Assuming that it is turned on, The first on-off Tow-Thomas biquad 1456 processes the signal received at the input 1454 and provides a signal at an output 1458. The first on-off Tow-Thomas biquad 1456 that is turned on advantageously has a transconductance G_{in} for a transconductor 808 of 72.9 micro-amperes per volt, a transconductance G_m for a transconductor 824 of 70 micro-amperes per volt, a transconductance QG_m for transconductors 834 and 844 of 223.5 micro-amperes per volt, and a capacitance for capacitors 816, 854 of 29 picofarads. The output 1458 of the first on-off Tow-Thomas biquad 1456 corresponds to input 1460 of a second on-off Tow-Thomas biquad 1462.

Assuming that it is turned on, the second on-off Tow-Thomas biquad 1462 processes the signal received at the input 1460 and provides a signal at an output 1464. The second on-off Tow-Thomas biquad 1462 that is turned on advantageously has a transconductance G_{in} for the transconductor 808 of 114.4 micro-amperes per volt, a transconductance G_m for the transconductor 824 of 70 micro-amperes per volt, a transconductance QG_m for the transconductors 834 and 844 of 458 micro-amperes per volt, and a capacitance for the capacitors 816, 854 of 74 picofarads. The output

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1464 of the second on-off Tow-Thomas biquad 1462 corresponds to the input 1466 of a third on-off Tow-Thomas biquad 1468.

Assuming that it is turned on, the on-off Tow-Thomas biquad 1468 processes the signal received at the input 1466 and provides a signal at an output 1470. The third on-off Tow-Thomas biquad 1468 that is turned on advantageously has a transconductance G_{in} for the transconductor 808 of 283 micro-amperes per volt, a transconductance G_m for the transconductor 824 of 70 micro-amperes per volt, a transconductance QG_m for the transconductors 834 and 844 of 458 micro-amperes per volt, and a capacitance for the capacitors 816, 854 of 48 picofarads. The output 1470 of the third on-off Tow-Thomas biquad 1468 corresponds to output 1472 of the sixth order bandpass Chebychev filter 1450.

Referring to Fig. 22, there is shown an exemplary transconductor 2200 that may be used to implement the on-off Tow-Thomas biquads of Figs. 14(a) and 14(b). The transconductor 2200 is identical to the transconductor 900 shown in Fig. 9, except for the addition of a PMOS transistor Q_7 and an NMOS transistor Q_8. The PMOS transistor Q_7 is connected in series between the gate 917 of the PMOS transistor Q_5 and ground. The NMOS transistor Q8 connected in series between the gate 920 of the NMOS transistor Q_6 and the gate 917 of the PMOS transistor Q_5. If the PMOS transistor Q_7 is turned off and the NMOS transistor Q_8 is turned on by the application of a logical one voltage to the gate terminal 2204, the transconductor 2200 operates in essentially the same manner as the transconductor 900 shown in Fig. 9. However, the PMOS transistor Q_7 is turned on and the NMOS transistor Q_8 is turned off by the application of a logical zero voltage to the gate terminal 2204, the transconductor 2200 is disabled and the output 810 of the transconductor 2200 acts as an open circuit. Each transconductor of the on-off Tow-Thomas biquad may have the configuration of the transconductor 2200, and the gate terminal 2204 of each transconductor may be connected together to provide a terminal for turning each of the Tow-Thomas biquads on or off.

In a further exemplary embodiment, the signal strength detector 608 is described in Fig. 12(b) as signal strength detector 1250. The input 641 of the signal strength detector 608 corresponds to the input 1252 of the signal strength detector

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1250, the input 641 of the signal strength detector 608 corresponds to the input 1253 of the signal strength detector 1250, and the output 611 of the signal strength detector 608 corresponds to the output 1270 of the signal strength detector 1250.

A signal received by the input 1252 of the signal strength detector 1250 is conveyed to an input 1254 of a peak detector 1256, which is similar to the peak detector 1180 as shown in Fig. 11. The peak detector 1256 processes the signal received at the input 1254 and provides a signal at an output 1258. The output 1258 of the peak detector 1256 corresponds to input 1260 of a threshold detector 1262.

The threshold detector 1262 processes the signal received at the input 1260 and provides a signal at an output 1264. The threshold detector 1262, which is similar to the first threshold detector 1175 shown in Fig. 11, is configured by setting a reference current of a current source 1170 (shown in Fig. 11) to detect the first limit, which represents the minimum tolerable signal to noise ratio of the filter 604. The reference current representing the first limit for the threshold detector 1262 can be 30 micro-amperes. The threshold detector 1262 processes the signal at its input 1260 and transmits a signal at its output 1264. The output 1264 of the threshold detector 1262 is connected to an input 1266 of a two input OR gate 1268.

A signal received by the input 1253 of the signal strength detector 1250 is conveyed to an input 1255 of a peak detector 1257, which is similar to the peak detector 1180 as shown in Fig. 11. The peak detector 1257 processes the signal received at the input 1255 and provides a signal at an output 1259. The output 1259 of the peak detector 1257 corresponds to input 1261 of a threshold detector 1263.

The threshold detector 1263 processes the signal received at the input 1261 and provides a signal at an output 1265. The threshold detector 1263, which is similar to the first threshold detector 1175 shown in Fig. 11, is configured by setting a reference current of a current source 1170 (shown in Fig. 11) to detect the second limit, which represents the saturation point of the filter 605. The reference current representing the second limit for the threshold detector 1263 can be 7.7 micro-amperes. The threshold detector 1263 processes the signal at its input 1261 and transmits a signal at its output 1265. The output 1265 of the threshold detector 1263 is connected to an input 1267 of a two input OR gate 1268. The two input OR gate

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1268 processes the signals received at its inputs and provides a signal to the output 1270 of the signal strength detector 1250.

In a further exemplary embodiment, the timer 610 can be the timer 1300 as shown in Fig. 13. The input 639 of the timer 610 corresponds to input 1302 of the timer 1300, and the outputs 635, 637, 631, 633, of the timer 610 correspond to outputs 1309, 1319, 1394, 1399, respectively, of the timer 1300. The n-bit overflow counter 1388 should be configured to allow a period of time to elapse that is at least as long as the longest amount of time it takes for transients at the output of a signal processor circuit after it is turned on to die out before the counter overflow output 1389 changes from a logical zero to a logical one. The outputs 587, 589, 591 are not connected when the timer 1300 is used with the system 600.

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CLAIMS

1. A signal processing system comprises:

a system input for receiving an input signal having an in-band component and an out-band component;

a system output for providing a system output signal;

a plurality of signal processing circuits each having an input coupled to the system input and an output for providing a respective output signal, each one of the signal processing circuits being adapted for optimal processing of input signals over a different range of in-band component to out-band component ratios;

a plurality of switches each having a switch input coupled to the output of a respective one of the signal processing circuits, a switch output connected to the system output, and a switch control input responsive to a first switch control signal for connecting the switch input to the switch output and responsive to a second switch control signal for disconnecting the switch input from the switch output ; and

a signal strength detector having at least one input each coupled to the output of a preselected one of the signal processing circuits and a plurality of outputs each coupled to the switch control input of a respective one of the plurality of switches, the signal strength detector being responsive to a comparison of the strength of the output signal of each preselected one of the signal processing circuits with at least one limit for selecting a particular one of the signal processing circuits and for providing a first switch control signal to the switch control input of the switch having its switch input coupled to the output of the particular one of the signal processing circuit, the signal strength detector providing the second switch control signal to the switch control input of each one of the switches having its switch input coupled to the output of a respective one of the signal processing circuits not selected by the signal strength detector.

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2. The signal processing system of claim 1, wherein each one of the signal processing circuits comprises a plurality of filters each having a filter input and a filter output, and a plurality of amplifiers each having an amplifier input and an amplifier output, the plurality of filters and amplifiers being connected alternatingly in series wherein the amplifier input of each amplifier is coupled to the filter output of a preceding filter and the amplifier output of each amplifier is coupled to the filter input of a succeeding filter, each signal processing circuit having a first filter, the filter input of the first filter being connected to the input of the signal processing circuit, and a last filter, the filter output of the last filter being the output of the signal processing circuit.

3. The signal processing system of claim 1, wherein the plurality of signal processing circuits comprises a first signal processing circuit and a last signal processing circuit, and each filter in the same position in the series of alternatingly connected amplifiers and filters in each one of the plurality of signal processing circuits have a respective common transfer function, and wherein the amplifiers of the first signal processing circuit each have a gain of approximately 10, and each amplifier of the last signal processing circuit have a gain of approximately 1.

4. The signal processing of claim 1, wherein each one of the signal processing circuits comprise a respective sixth order bandpass Chebychev filter.

5. The signal processing system of claim 4, wherein the sixth order bandpass Chebychev filter of each one of the signal processing circuits has a ripple of approximately 0.25 dB, a band width of approximately 0.5 MHz, and a different center frequency and quality factor.

6. The signal processing circuit of claim 5, wherein the sixth order bandpass Chebychev filter of each one of the signal processing circuits comprise three standard Tow-Thomas biquads connected in series.

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7. The signal processing system of claim 6, wherein each one of the Tow-Thomas biquads comprise an input terminal, an output terminal, first, second, third and fourth transconductors each having a normal input and an inverting input and an output, a first capacitor and a second capacitor, the first transconductor having a transconductance G_{in} and having its normal input connected to the input terminal, its inverting input connected to ground and its output connected to the output terminal, the second transconductor having a transconductance G_m and having its inverting input and output connected to the output terminal and its normal input connected to ground, the third transconductor having a transconductance QG_m and having its inverting input connected to a first node, its normal input connected to ground and its output connected to the output terminal, the fourth transconductor having a transconductance QG_m and having its normal input connected to the output terminal, its inverting input connected to ground and its output connected to the first node, the first capacitor being connected between the output terminal and ground, and the second capacitor being connected between the first node and ground.

8. The signal processing system of claim 1, wherein the signal strength detector comprises at least one peak detector each coupled to the output of a preselected one of the signal processing circuits and an output coupled to at least one threshold detector for comparing the output of the peak detector with a respective limit, and a combinatorial logic circuit responsive to the comparison made by each one of the at least one threshold detector for deriving switch control signals for the switch control inputs of respective ones of the plurality of switches.

9. A signal processing comprising:

a system input for receiving a signal having an in-band component and an out-band component;

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an output for providing a system output signal;

a plurality of signal processing pathways each extending from the system input to a respective output of the signal processing pathway, the plurality of signal processing pathways including:

a main signal processing pathway comprising a plurality of filters each having a respective filter input and a respective filter output, and a plurality of amplifiers each having a respective amplifier input and a respective amplifier output, the amplifier input of each amplifier being connected to the filter output of a respective preceding filter, the amplifier output of each amplifier being connected to the filter input of a respective succeeding filter, the main signal processing pathway having a first filter and a last filter, the filter input of the first filter being connected to the system input the filter output of the last filter being the output of the main pathway; and

a plurality of auxiliary signal processing pathways each including at least one amplifier each having a respective amplifier input and a respective amplifier output, and at least one filter each having a respective filter input and a respective filter output, each one of the auxiliary pathways having a branch amplifier and a last filter, the amplifier input of the branch amplifier of each one of the auxiliary pathways being connected to the filter output of a respective preceding one of the filters, except the last filter of the main pathway, the amplifier output of the branch amplifier of each one of the auxiliary signal processing pathways being connected to the filter input of a respective succeeding filter, any additional amplifier or filter following the branch amplifier in each auxiliary pathway being connected in alternating sequence wherein the amplifier input of each additional amplifier being connected to the filter output of a respective succeeding filter

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and the amplifier output of each additional amplifier being connected to the filter input of a respective succeeding filter, each one of the pathways having the same number of filters and amplifiers, the filter output of the last filter of each one of the auxiliary pathways being the output of the auxiliary pathway, each one of the signal processing pathways being adapted for optimal processing of input signals over a different range of in-band component to out-band component ratios;

a plurality of switches each having a switch input connected to the output of a respective one of the signal processing pathways, a switch output coupled to the system output, and a switch control input responsive to a first switch control signal for connecting the switch input to the switch output and responsive to a second switch control signal for disconnecting the switch input from the switch output; and

a signal strength detector having at least one input each connected to the output of a preselected one of the signal processing pathways and a plurality of outputs each connected to the switch control input of a respective one of the switches, the signal strength detector being responsive to the output signal at the output of a previously selected one of the signal processing pathways having its output connected to the system output exceeding a first predetermined level for selecting another one of the signal processing pathways for processing the input signal and for providing the first switch control signal to the switch input of a respective one of the switches having its switch input connected to the output of the selected one of the signal processing pathways to thereby connect the output of the selected one of the signal processing pathways to the system output, the signal strength detector providing the second switch control signal to the switch control input of a respective one of

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the switches having a switch input connected to the output of the previously selected one of the signal processing pathways to thereby disconnect the output of the previously selected one of the signal processing pathways from the system output, the signal strength detector being responsive to the output signal at the output of the previously selected one of the signal processing pathways being below a second predetermined level for selecting a different one of the signal processing pathways for processing the input signal and for providing the first switch control signal to the switch control input of a respective one of the switches having its switch input connected to the output of the selected different one of the signal processing pathways to thereby connect the output of the selected different one of the signal processing pathways to the system output, the signal strength detector providing the second switch control signal to the switch control input of the respective one of the input switches having a switch input connected to the output of the previously selected one of the signal processing pathways to thereby disconnect the output of the previously selected one of the signal processing pathways from the system output.

10. A signal processing system comprising:

a system input for receiving an input signal and a system output for providing a system output signal;

a plurality of signal processing circuits each having an input coupled to the system input and an output for providing a respective output signal, each signal processor having a different saturation level and a different signal to noise ratio with respect to an input signal processed thereby;

a plurality of switches each having a switch input coupled to the output of a respective one of the signal processing circuits, a switch output coupled to the system output, and a switch control input responsive to a first switch

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control signal for connecting the switch input to the switch output and responsive to a second switch control signal for disconnecting the switch input from the switch output;

a signal strength detector having an input coupled to the system input and a plurality of outputs each corresponding to a respective one of the signal processing circuits, the signal strength detector being responsive to a comparison of the strength of the input signal received at the system input with at least one limit for selecting a particular one of the signal processing circuits having a respective saturation level and a respective signal to noise ratio with respect to an input signal processed thereby suitable for processing the input signal and for providing the first switch control signal to the switch control input of a respective one of the plurality of switches having its switch input coupled to the output of the selected one of the signal processing circuits and for providing the second switch control signal to the switch control inputs of respective ones of the switches having the switch input coupled to the output of respective ones of the signal processing circuits not selected by the signal strength detector.

11. The signal processing system of claim 10, wherein each of the signal processing circuits is a companding signal processor comprising:

a filter having a filter input and a filter output;

an input amplifier having an input coupled to the system input and an output coupled to the filter input of the filter, the input amplifier having a respective gain; and

an output amplifier having an input coupled to the filter output of the filter and an output coupled to the output of the signal processing circuit, the output amplifier having a gain which is the inverse of the gain of the input amplifier.

12. The signal processing system of claim 10, wherein the input amplifier of each companding signal processor is adapted to provide an output signal that is

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clamped so as to prevent saturation of the filter having its filter input connected to the output of the input amplifier.

13. The signal processing system of claim 11, wherein the signal processing system comprises a first, second and third companding signal processors, and the signal strength detector compares the strength of the input signal with a first limit and a second limit, the first limit being a signal strength level where the signal received at the system input is near a minimum required signal to noise ratio the noise floor of the second companding signal processor and the first companding signal processor is near saturation, the second limit being the signal strength level where the second companding signal processor is near saturation and the signal received at the system input is near the minimum required signal to noise ratio of the third companding signal processor, wherein the signal strength detector selects the first companding signal processor if the strength of the input signal does not exceed the first limit or the second limit, wherein the signal strength detector selects the second companding signal processor if the strength of the input signal exceeds the first limit but does not exceed the second limit, and wherein the signal strength detector selects the third companding signal processor if the strength of the input signal exceeds the first limit and the second limit.

14. The signal processing system of claim 11, wherein the filter of each one of the companding signal processors comprises a biquad having an input terminal, an output terminal, first, second, third, and fourth transconductors each having a normal input, an inverting input and an input, first and second capacitors and a resistor, the first transconductor having a transconductance G_m and having its inverting input and output connected to the input terminal and its normal input connected to ground, the second transconductor having a transconductance QG_m and having its inverting input connected to a first node, its normal input connected to ground and its output connected to the input terminal, the third transconductor having a conductance QG_m and having its normal input connected to the output terminal, its inverting input connected to ground and

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its output connected to the first node, the fourth transconductor having a transconductance G_m and having its normal input connected to the first node, its inverting input connected to ground and its output connected to the output terminal, the first capacitor being connected between the input terminal and ground, the second capacitor being connected between the first node and ground, and the resistor being connected between the output terminal and ground.

15. A signal processing system comprising:

a system input for receiving an input signal;

a system output for providing a system output signal;

a first and a second signal processing circuit each having an input, an output, a power control input responsive to a first power control signal for causing the signal processing circuit to be in a powered up state and responsive to a second power control signal for causing the signal processing circuit to be in a powered down state, and at least one bias control input responsive to at least one bias control signal for biasing the signal processing circuit for optimal processing of a signal having a respective signal strength;

a plurality of output switches each having a switch input connected to the output of a respective one of the first and second signal processing circuits, a switch output coupled to the system output and a switch control input responsive to a first switch control signal for connecting the switch input to the switch output and being responsive to a second switch control signal for disconnecting the switch input from the switch output, wherein at any given time one of the first or second signal processing circuits is active by being in a powered up state, receiving at least one bias control signal at its at least one bias control input and having its output connected to the system output by a respective one of the output switches, and the other one of the first and second signal processing circuits is inactive by being in a powered down state and having its output disconnected from the system output by a respective one of the output switches;

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a signal strength detector having a first and second input connected to respective internal nodes of the first and second signal processing circuits and at least one output for specifying at least one bias level change corresponding to at least one bias control signal, if any, to be applied to the at least one bias control input of an inactive one of the signal processing circuits, the signal strength detector being responsive to a comparison of the strength of a signal on the respective internal node of an active one of the signal processing circuits with at least one limit for determining whether at least one bias control signal is to be applied to the at least one bias control input of the inactive one of the signal processing circuits for changing the bias thereto, and for providing on the at least one output at least one signal specifying, if any, the at least one bias control signal to be applied to the bias control input of an inactive one of the signal processing circuits;

a bias selector circuit responsive to the at least one output signal provided on the at least one output of the signal strength detector for providing on at least one first output the at least one bias control signal specified by the at least one output of the signal strength detector to the at least one bias control input of the inactive one of the signal processing circuits and providing on a second output a signal indicating that at least one bias control signal has been applied to the inactive one of the signal processing circuits; and

a timer circuit responsive to the signal on the second output of the bias selector circuit for providing the first power control signal to the power control input of the inactive one of the signal processing circuits, and after a predetermined delay for applying the first switch control signal to the switch control input of the switch having its input coupled to the output of the inactive one of the signal processing circuits and applying the second switch control signal to the switch control input of the switch having its switch input connected to the output of the active one of the signal processing circuits and applying the second power control signal to the power control input of the active one of the signal processing circuits.

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16. The signal processing system of claim 15, wherein the signal strength detector determines the at least one bias control signal to be applied to the at least one bias control input of the inactive one of the signal processing circuit based upon a first limit and a second limit, the first limit indicating that the signal-to-noise ratio of the signal on the respective internal node of the active one of the signal processing circuits is approaching a minimum required level and that the signal strength detector determines that a bias control signal corresponding to a next higher bias level is to be applied to the at least one bias control input of the inactive one of the bias control circuits, and the second limit indicates the onset of saturation of the active one of the signal processing circuits and that the signal strength detector determines a bias control signal corresponding to a next lower bias level be applied to the at least one bias control input of the inactive one of the signal processing circuits.

17. The signal processing system of claim 16, wherein each one of the first and second signal processing circuits comprises a dynamic input scaling circuit, a biquad and a dynamic output scaling circuit connected in series.

18. The signal processing system of claim 17, wherein the dynamic input scaling circuit comprises a first input terminal, a third input terminal, an output terminal, a first switch having a switch input, a switch output and an inverting switch control input, a second switch having a switch input, a switch output and a switch control input, a first resistor, a second resistor, a first transconductor having a transconductance G_m and having a normal input, an inverting input and an output, and a second transconductor having a transconductance 9 G_m and having a normal input, an inverting input, a switch input responsive to a logical one signal for enabling the second transconductor and responsive to a logical zero signal for disabling the second transconductor, wherein the switch input of the first switch and one terminal of the first resistor are connected to the first input terminal, and the inverting switch control input of the first switch and the switch control input of the second

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switch are connected to the second input terminal, wherein the other terminal of the first resistor, one terminal of the second resistor, the normal input of the first transconductor and the normal input of the second transconductor are each connected to a first node, and the other terminal of the second resistor is connected to the switch input of the second switch, and wherein the switch output of the second switch, the inverting input of the first transconductor and the inverting input of the second transconductor are each connected to ground, the output of the first transconductor being connected to the output terminal and the third input terminal being connected to the on/off input of the second transconductor.

19. The signal processing system of claim 15, wherein the biquad comprises a first input terminal, a second input terminal, an output terminal, a first transconductor having a transconductance G_m and having a normal input, an inverting input, an on/off input and an output, a second and third transconductor each having a transconductance QG_m and each having a normal input, an inverting input, an on/off input and an output, a fourth transconductor having a transconductance G_m and having a normal input, an inverting input, an on/off input and an output, a first capacitor and a second capacitor, wherein the on/off inputs of the first, second, third and fourth transconductors are responsive to a logical one signal for enabling the respective transconductor and responsive to a logical zero signal for disabling the respective transconductor, and one terminal of the first capacitor, the inverting input of the first transconductor, the output of the second transconductor, the normal input of the third transconductor are each connected to a first node, wherein the inverting input of the second transconductor, the output of the third transconductor, the normal input of the fourth transconductor and one terminal of the second capacitor are each connected to a second node, and the on/off inputs of the first, second, third and fourth transconductors are each connected to the second input terminal, and wherein the other terminal of the first capacitor, the normal input of the first

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transconductor, the normal input of the second transconductor, the inverting input of the third transconductor, the inverting input of the fourth transconductor and the other terminal of the second capacitor are each connected to ground, and the output of the fourth transconductor is connected to the output terminal.

20. The signal processing system of claim 15, wherein the dynamic output scaling circuit comprises first, second and third input terminals, an output terminal, first, second and third resistors, first, second and third switches each having a switch input, a switch output and a switch control input, wherein the switch inputs of the first, second and third switch are connected to the first, second and third input terminals, respectively, and one terminal of the first, second and third resistors are each connected to the output terminal, and wherein the other terminal of the first, second and third resistors are connected to the switch inputs of the first, second and third switches, respectively, and the output terminal of the first, second and third switches are each connected to ground.

21. A signal processing system comprising:

a system input for receiving an input signal;

a system output for providing a system output signal;

a first and a second signal processing circuit each having an input, an output, a power control input responsive to a first power control signal for causing the signal processing circuit to be in a powered up state and responsive to a second power control signal for causing the signal processing circuit to be in a powered down state, an internal node output for providing a signal on an internal node of the signal processing circuit, and at least one bias control input for receiving at least one bias control signal for optimizing the bias of the signal processing circuit to process a signal having a respective signal strength;

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first and second input switches each having a first input connected to the system input, a second input connected to ground, an output coupled to the input of a respective one of the signal processing circuits, and a switch control input responsive to a first switch control signal for connecting the first input of the switch to the output of the switch and responsive to a second input switch control signal for connecting the second input of the switch to the output of the switch;

first and second output switches each having an input coupled to the output of a respective one of the signal processing circuits, an output connected to the system output, and a switch control input responsive to a first output switch control signal for connecting the input of the switch to the output of the switch and responsive to a second output switch control signal for disconnecting the input of the switch from the output of the switch, wherein at any given time one of the signal processing circuits is active in having its input connected to the system input, its output connected to the system output, its power control input receiving the first power control signal and its at least one bias control input receiving at least one bias control signal, and the other one of the signal processing circuits being inactive in having its input disconnected from the system input, its output disconnected from the system output and its power control input receiving the second power control signal;

a signal strength detector having a first and second input each connected to a respective internal node signal output of the signal processing circuits, at least one output for providing at least one output signal specifying, if any, at least one bias control signal to be applied to the at least one bias control input of the inactive one of the signal processing circuits, the signal strength detector being responsive to a comparison of the signal provided by the internal node signal output of the active one of the signal processing circuits with at least one limit for selecting the at least one bias control signal to be applied to the at

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least one bias control input of the inactive one of the signal processing circuits and providing the at least one bias control signal, if any, on the at least one output;

a bias selector circuit responsive to the at least one bias control signal, if any, provided by the at least one output of the signal strength detector for providing on at least one first output the at least one bias control signal, if any, to the at least one bias control input of the inactive one of the signal processing circuits and providing on a second output a signal indicating that at least one bias control signal has been applied to the inactive one of the signal processing circuits; and

a timer circuit responsive to the signal provided on the second output of the bias selector circuit for providing the first power control signal to the power control input of the inactive one of the signal processing circuits, providing a first switch control signal to the switch control input of the input switch having its output coupled to the input of the inactive one of the signal processing circuits and providing after a predetermined delay a first switch control signal to the switch control input of the output switch having its input coupled to the output of the inactive one of the signal processing circuits, providing a second switch control signal to the switch control input of the output switch having its input coupled to the output of the active one of the signal processing circuits, providing the second power control signal to the power control input of the active one of the signal processing circuits and providing the second switch control signal to the switch control input of the input switch having its output coupled to the input of the active one of the signal processing circuits.

22. The signal processing system of claim 20, wherein the signal strength detector is responsive to a comparison between the signal provided by the internal node signal output of the active one of the signal processing circuits with a first limit and a second limit, the first limit indicating that the signal-to-noise ratio

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of the signal from the internal node signal output of the active one of the signal processing circuits is approaching a minimum required level and that the signal strength detector determines that a bias control signal causing the next higher bias level be applied to the at least one bias control input of the inactive one of the signal processing circuit, and the second limit indicating that the inactive one of the signal processing circuits is near saturation and that the signal strength detector selects a bias control signal causing a next lower bias level be applied to the at least one bias control input of the inactive one of the signal processing circuits.

23. The signal processing system of claim 20, wherein each one of the first and second signal processing circuits comprises a dynamic input scaling circuit, a biquad and a dynamic output scaling circuit connected in series between the input and the output of the signal processing circuit.

24. A signal processing system comprising:

a system input for receiving an input signal having an in-band component and an out-band component,

a system output for providing a system output signal;

a plurality of signal processing circuits each having an input coupled to the system input, an output for providing a respective output signal and a power control input responsive to a first power control signal for causing the signal processing circuit to be in a powered up state and responsive to a second power control signal for causing the signal processing circuit to be in a powered down state, each one of the plurality of signal processing circuits being adapted to have a different saturation level and signal to noise ratio for optimal processing of signals having a different range of in-band component to out-band component ratios;

a plurality of output switches each one having an input coupled to the output of a respective one of the plurality of signal processing circuits, an output connected to the system output and a switch control input responsive to a first switch control signal for connecting the input of the switch to the output of the switch and responsive

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to a second switch control signal for disconnecting the input of the switch from the output of the switch;

a signal strength detector having a first input connected to the system output, at least one output for proidiing a signal indicating a selected one of the plurality of signal processing circuits, the signal strength detector being responsive to a comparison of the strength of an output signal with at least one one limit for selecting one of the plurality of signal processing circuits for processing the input signal and providing at least one signal on the at least one output indicating the signal processing circuit selected by the signal strength detector; and

a timer circuit having at least one one input each coupled to a respective one of the at least one output of the signal strength detector and a first plurality of outputs each one connected to the power control input of a respective one of the plurality of signal processing circuits and a second plurality of outputs each one connected to the switch control input of a respective one of the plurality of output switches, the timer circuit being responsive to at least one signal provided by the signal strength detector for providing the first power control signal to the power control input of the signal processing circuit selected by the signal strength detector and providing after a predetermined delay the first switch control signal to the switch control input of a respective one of the plurality of output switches having its input connected to the output of the signal processing circuit selected by the signal strength detector to thereby connect the output of the signal processing circuit selected by the signal strength detector to the system output and providing after the predetermined delay the second switch control signal to the switch control input of respective ones of the plurality of output switches each having a switch input connected to the output of a respective one of the plurality of signal processing circuits not selected by the signal strength detector to thereby disconnect the output of each one of the plurality of signal processing circuits not selected by the signal strength detector from the system output, the timer circuit being responsive to at least one signal provided by the signal strength detector for providing after the predetermined delay the second power control signal to the power control input of each one of the plurality of signal processing circuits not selected by the signal strength detector.

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25. A method for processing an input signal received at a system input to derive an output signal at a system output comprising:

providing a plurality of signal processors each having an input coupled to the system input and an output, each one of the signal processors being adapted to process an input signal having a different range of in-band component to out-band component ratios without saturating and without having a signal-to-noise ratio approaching a minimum required level;

providing a plurality of switches, each one for controllably connecting and disconnecting the output of a respective one of the signal processors to the system output terminal;

detecting the strength of a respective output signal at each one of at least one selected output of the signal processors to compare the strength of the respective output signal with at least one limit to select one of the signal processors for optimal processing of the input signal; and

causing a respective one of the switches to connect the output of the selected signal processors to the system output and causing other ones of the switches to disconnect the outputs of all other signal processors from the system output.

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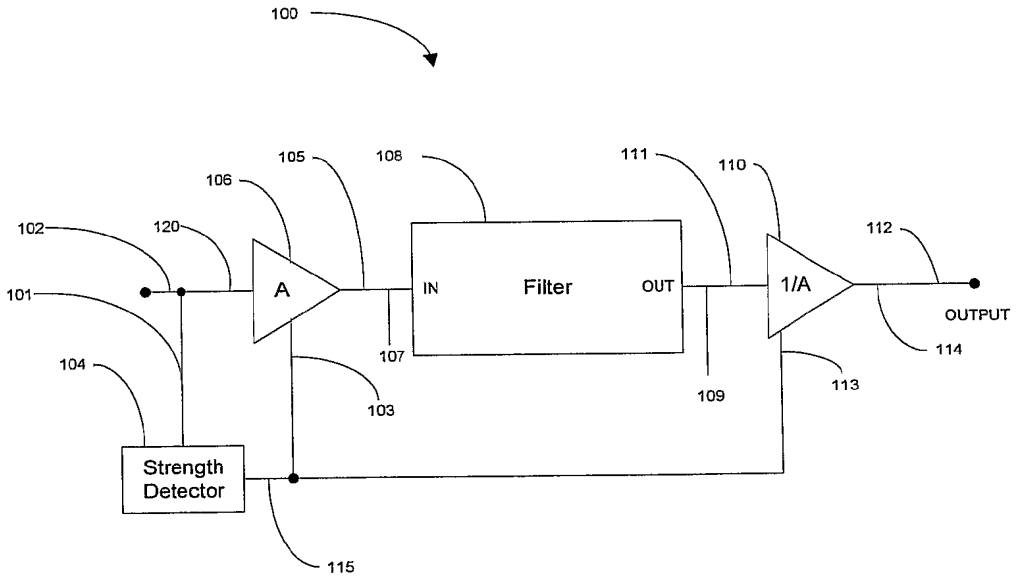


Fig. 1

(Prior Art)

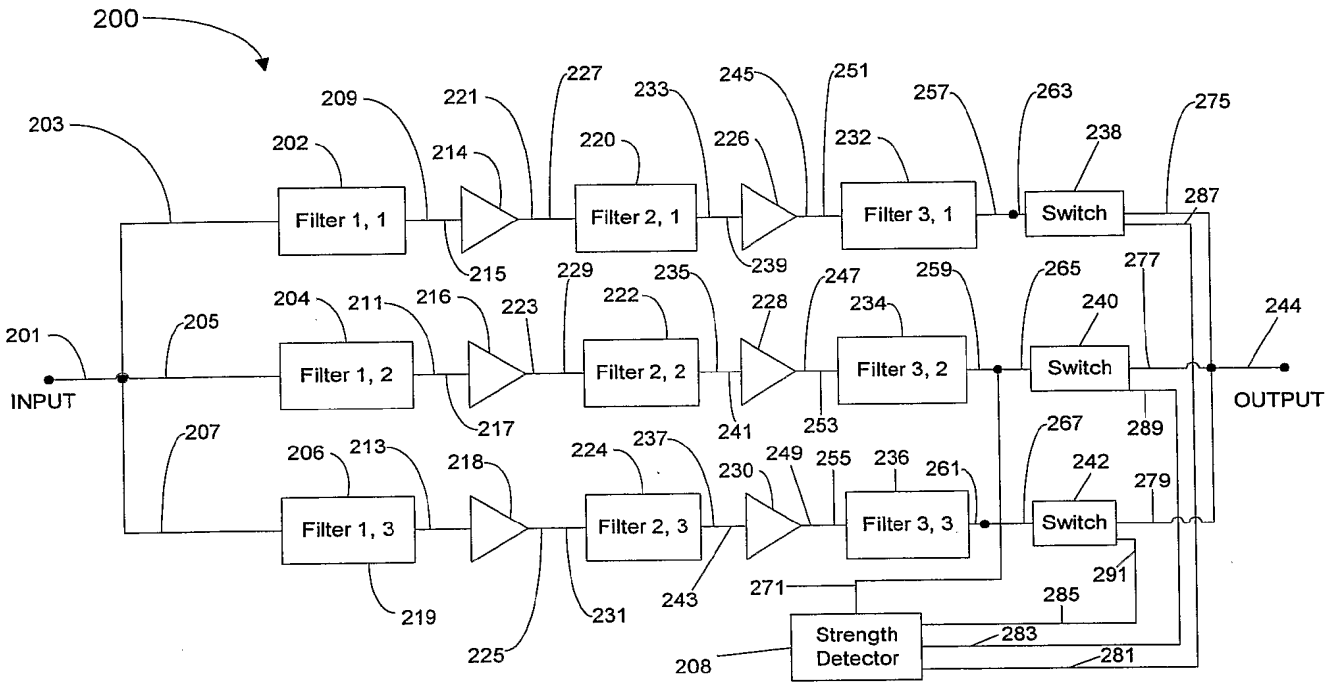

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Filter 1, 1
Filter 2, 1
Filter 3, 1
Switch
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INPUT
Filter 1, 2
Filter 2, 2
Filter 3, 2
Switch
OUTPUT
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289
242
279
Filter 1, 3
Filter 2, 3
Filter 3, 3
Switch
219
231
243
271
291
285
225
Strength Detector
283
208
281

Fig. 2

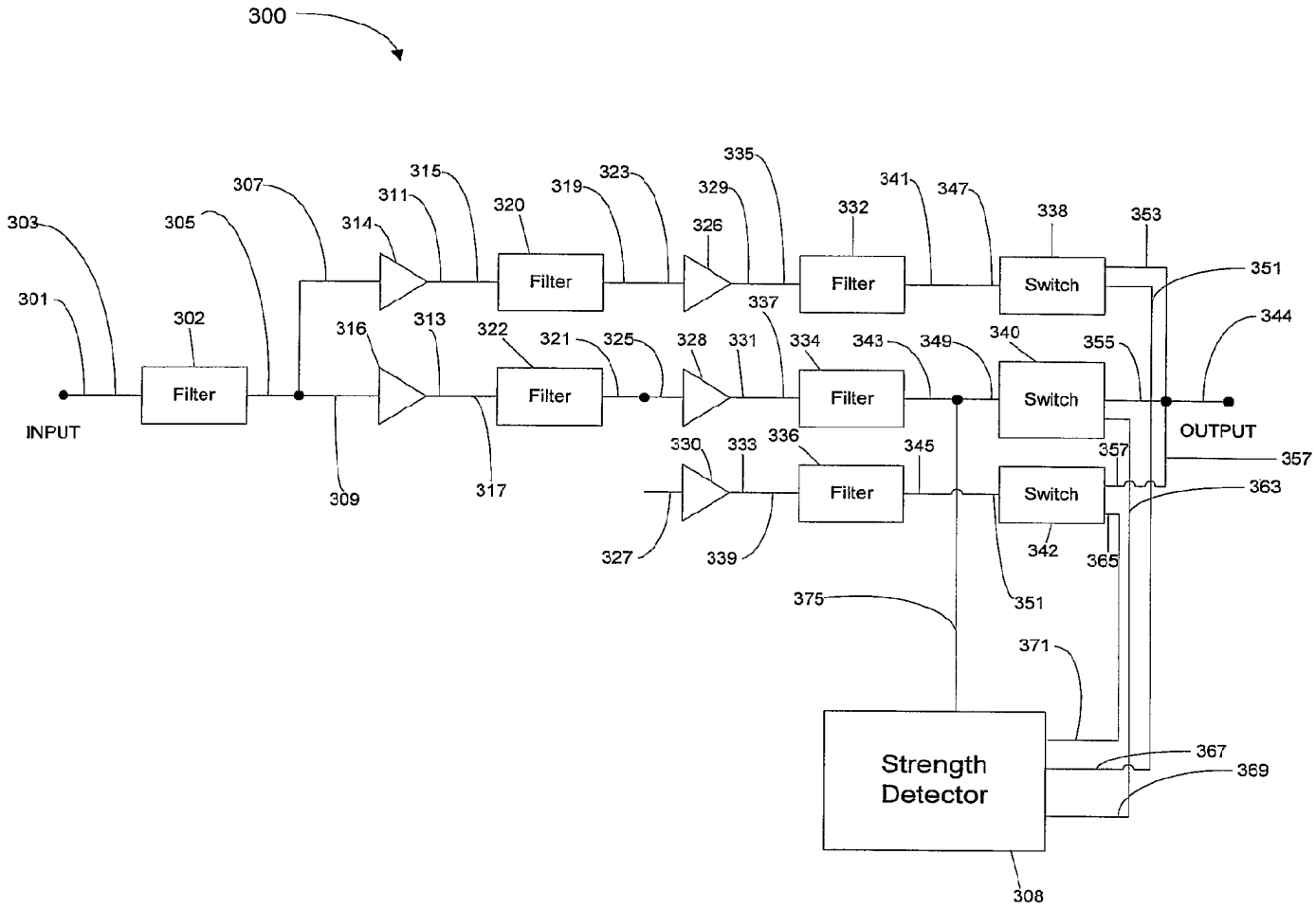

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322
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325
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331
334
343
349
340
355
344
337
INPUT
Filter
Filter
Filter
Filter
Switch
Switch
OUTPUT
309
317
330
333
336
345
357
357
363
327
339
342
365
375
351
371
Strength Detector
367
369
308

Fig. 3

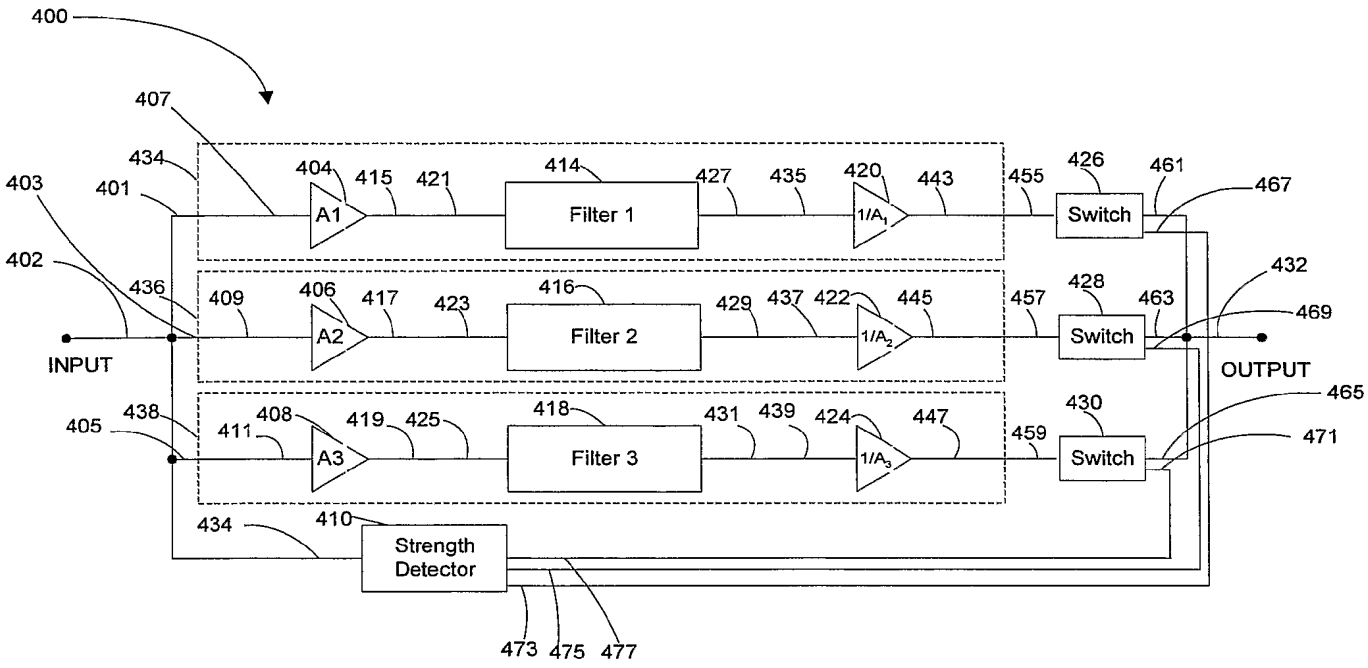
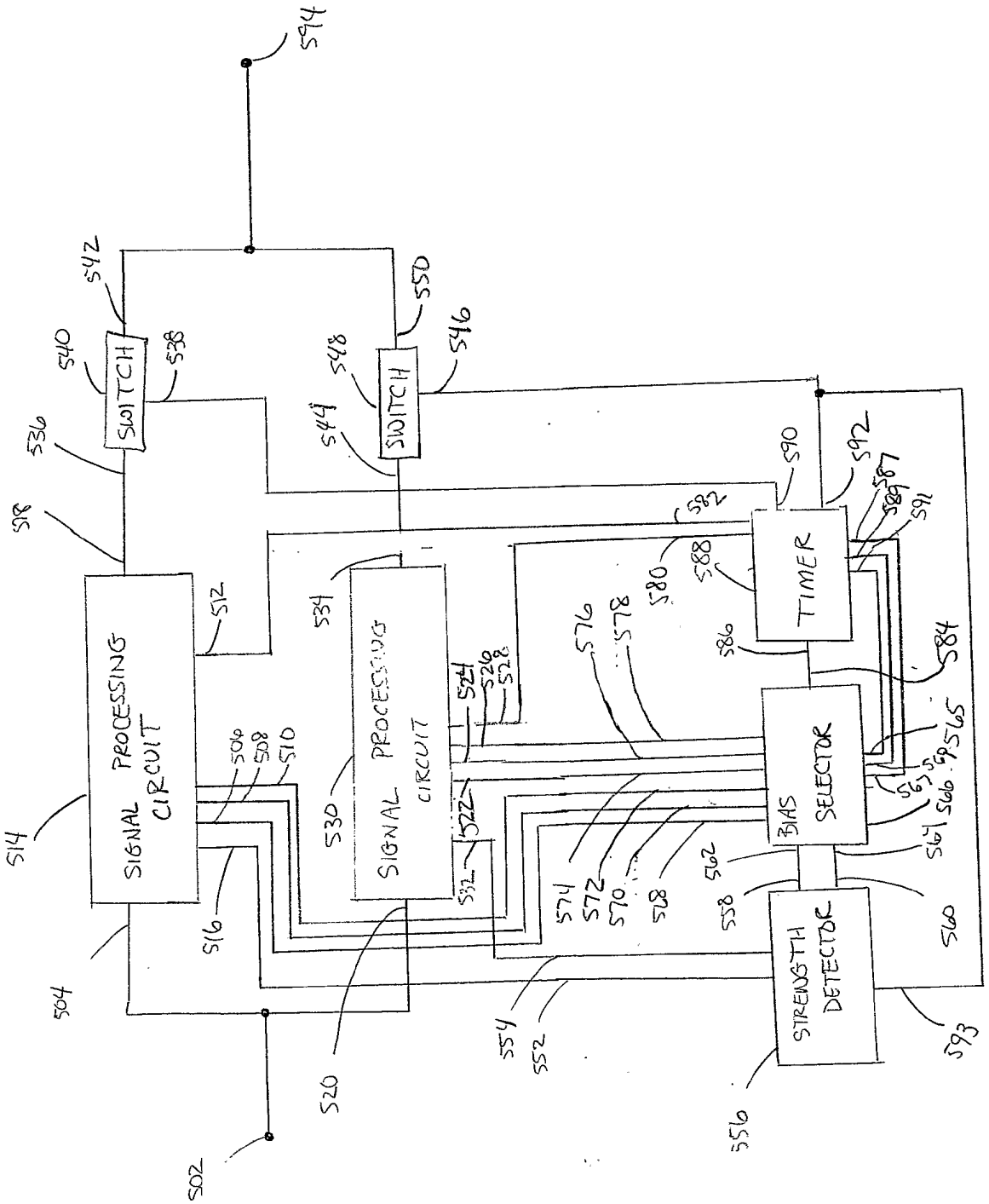
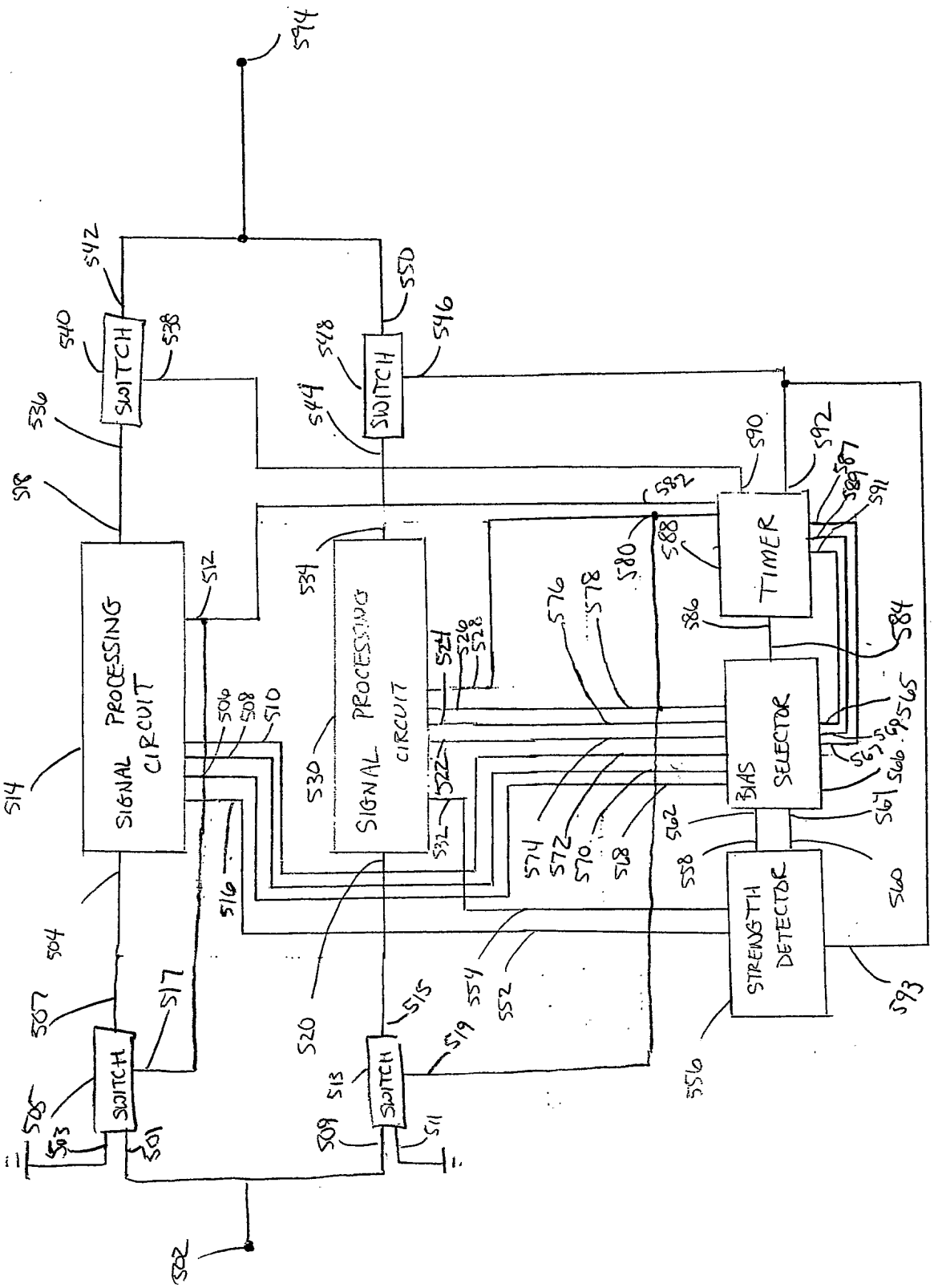

400
407
434
403
401
404
415
421
414
427
435
420
443
455
426
461
467
A1
Filter 1
1/A1
Switch
402
436
409
406
417
423
416
429
437
422
445
457
428
463
432
469
A2
Filter 2
1/A2
Switch
INPUT
OUTPUT
438
405
411
408
419
425
418
431
439
424
447
459
430
465
471
A3
Filter 3
1/A3
Switch
434
410
Strength Detector
473
475
477

Fig. 4


SIGNAL PROCESSING CIRCUIT
SIGNAL PROCESSING CIRCUIT
SWITCH
SWITCH
TIMER
BIAS SELECTOR
STRENGTH DETECTOR
502
504
506
508
510
512
514
516
518
520
522
524
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594

500

FIG. 5(a)


SIGNAL PROCESSING CIRCUIT
SIGNAL PROCESSING CIRCUIT
SWITCH
SWITCH
SWITCH
TIMER
BIAS SELECTOR
STRENGTH DETECTOR

599
FIG. 5(b)

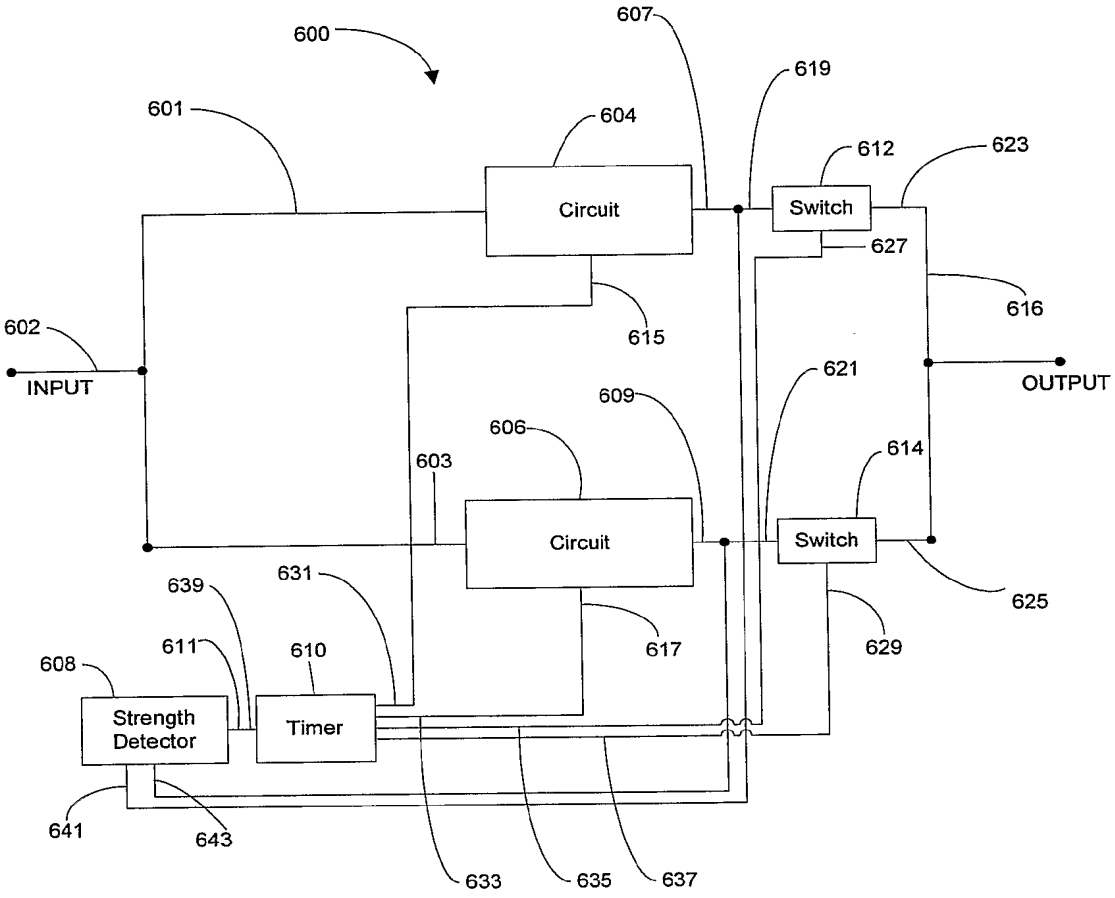
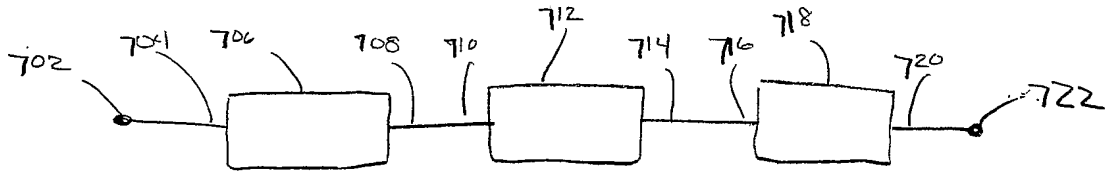
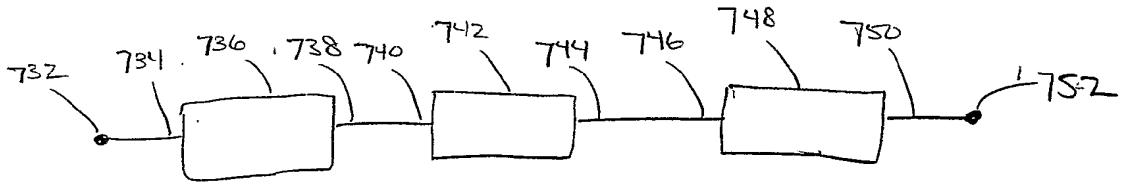

600
607
619
601
604
612
623
Circuit
Switch
627
616
602
615
INPUT
621
OUTPUT
609
606
614
603
Circuit
Switch
639
631
625
611
610
617
629
608
Strength Detector
Timer
641
643
633
635
637

Fig. 6



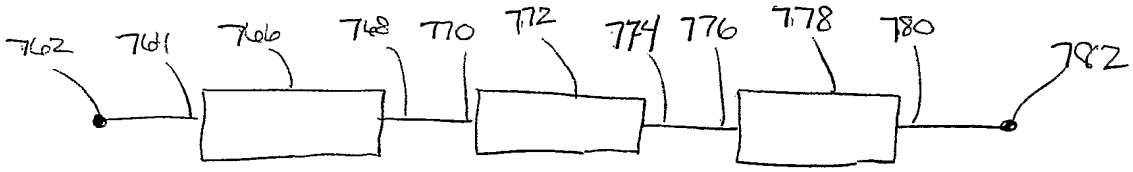
700

Fig. 7(a)



730

Fig. 7(b)



760

Fig. 7(c)

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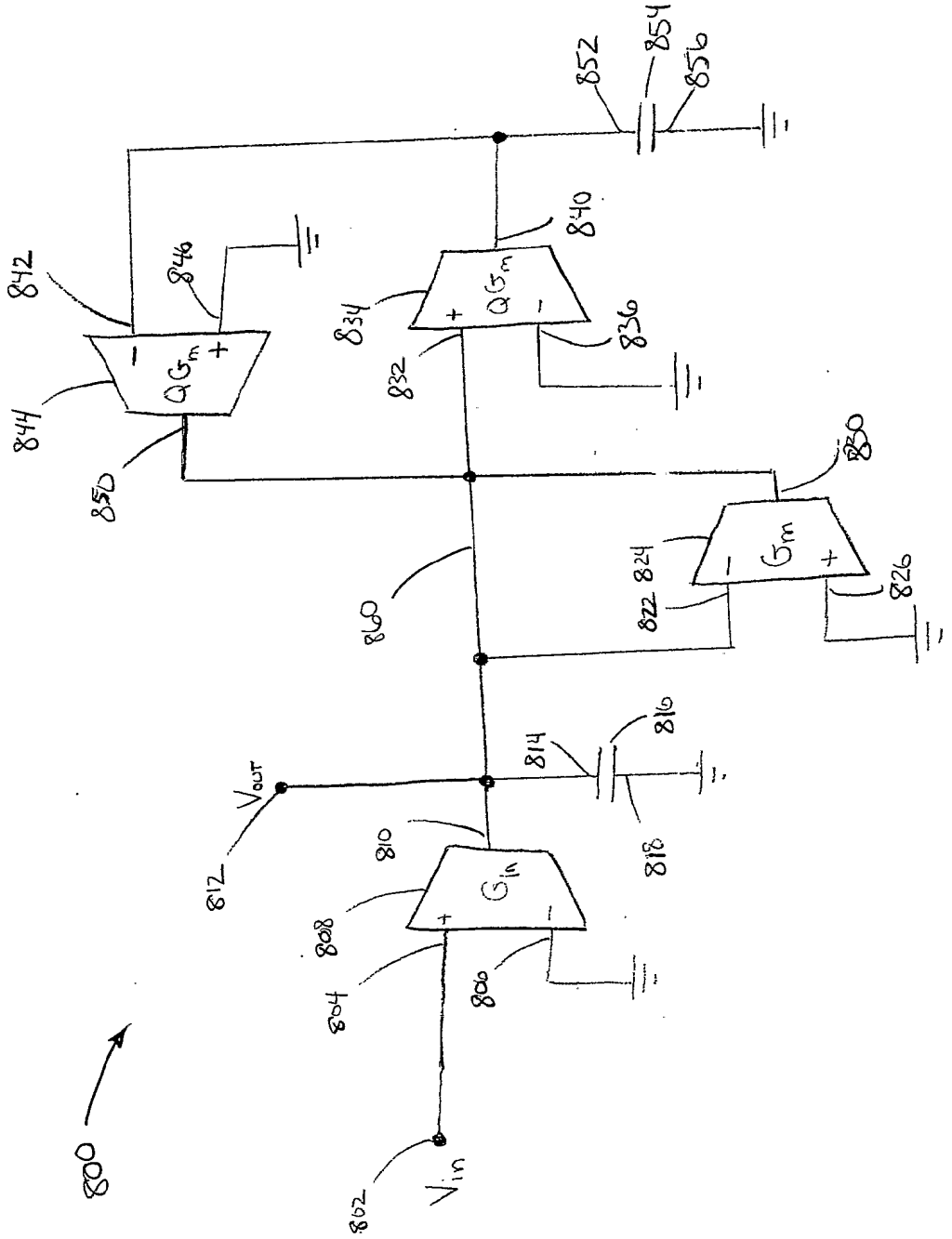

800
802
V_{in}
804
806
808
G_{in}
810
812
V_{out}
814
816
818
820
822
824
826
Gm
830
832
834
836
QGm
840
842
844
846
850
852
854
856
860

FIG 8

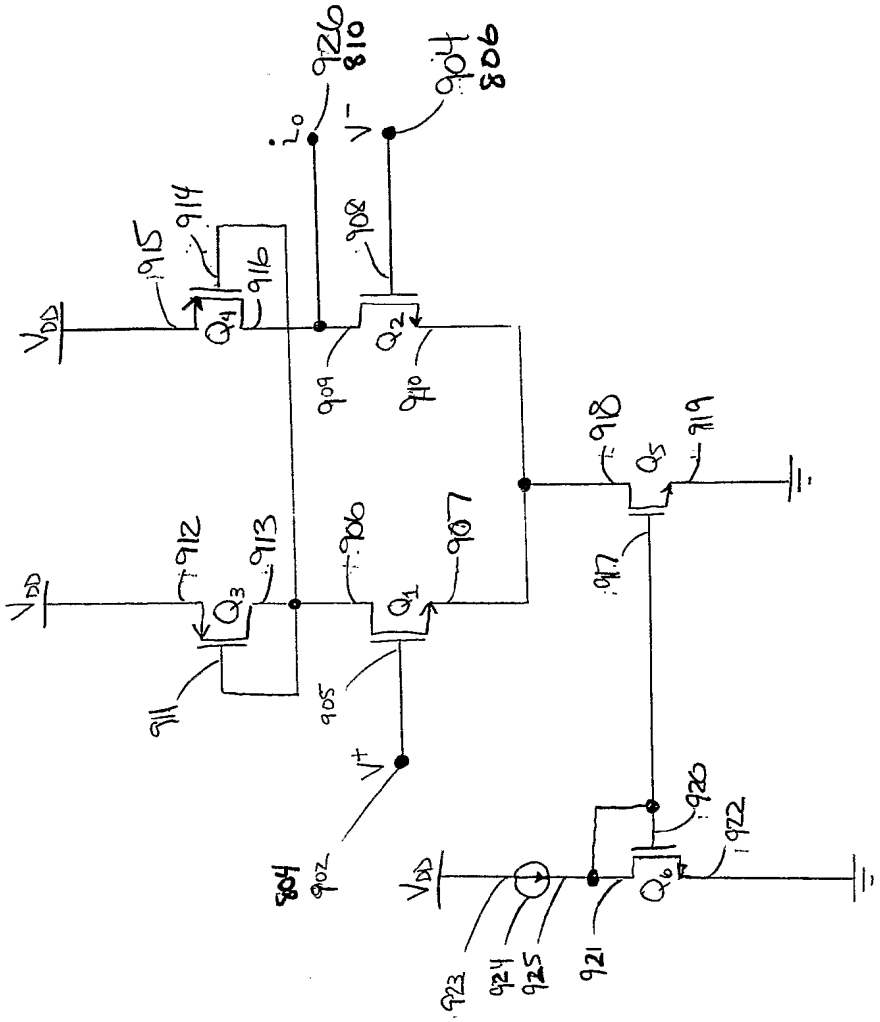

LO
V-
V+
VDD
Q1
Q2
Q3
Q4
Q5
Q6
902
904
905
906
907
908
909
910
911
912
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806
810

FIG. 9

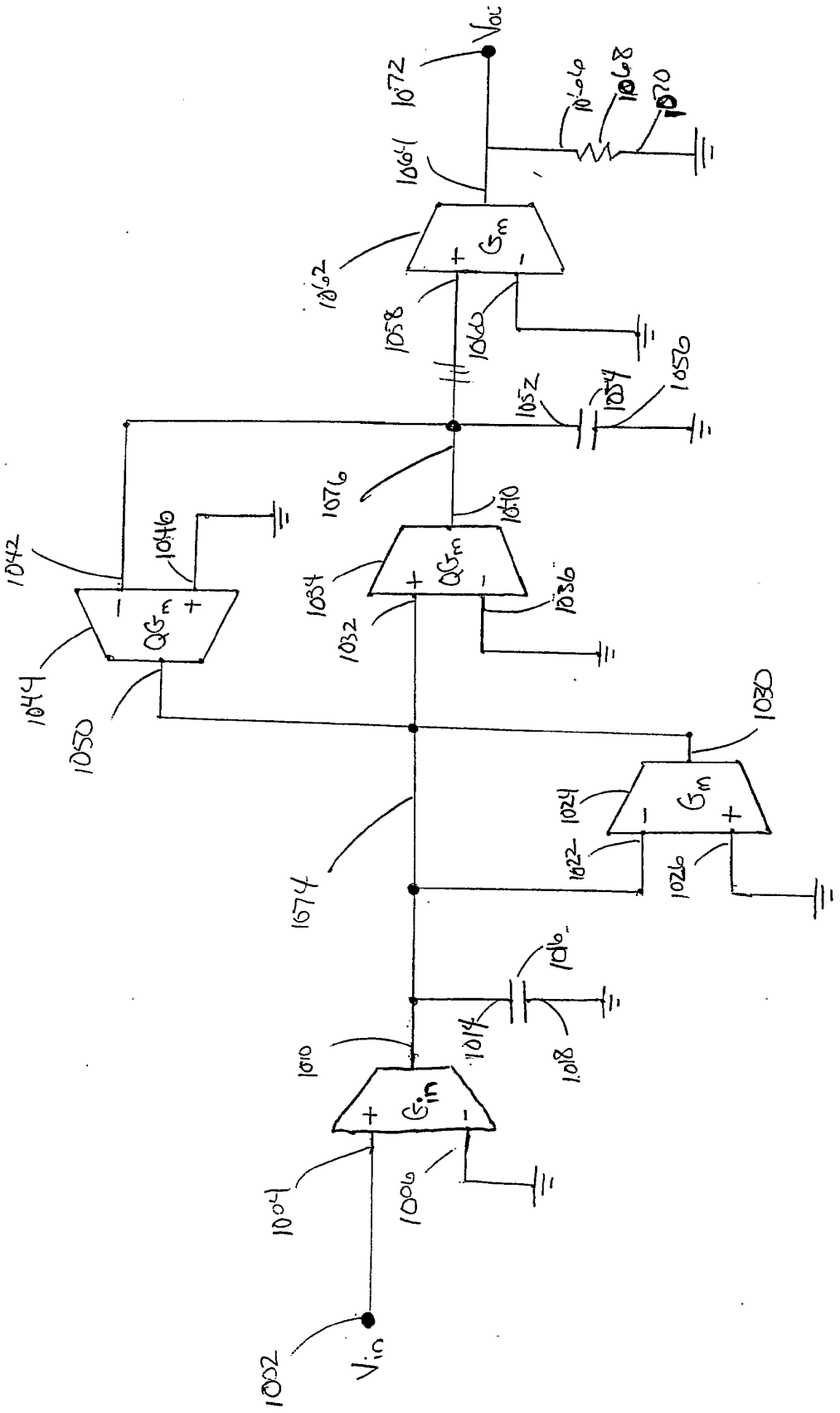
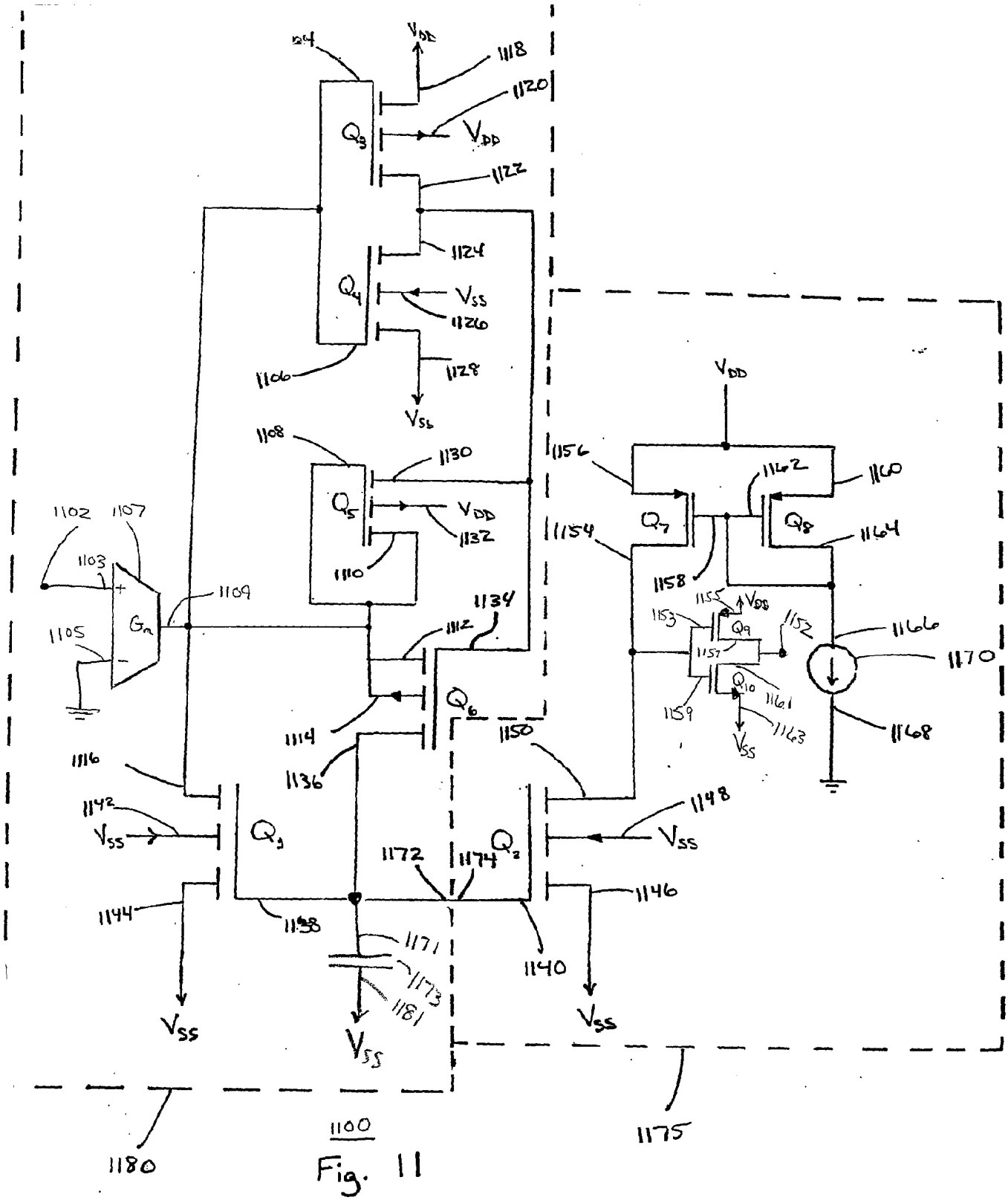

Vdc
1072
1064
1062
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1044
1050
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1036
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1030
1024
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1026
1074
1010
1014
1018
1012
1004
1006
1002
Vin

FIG. 10


1100
1180
1175
Fig. 11

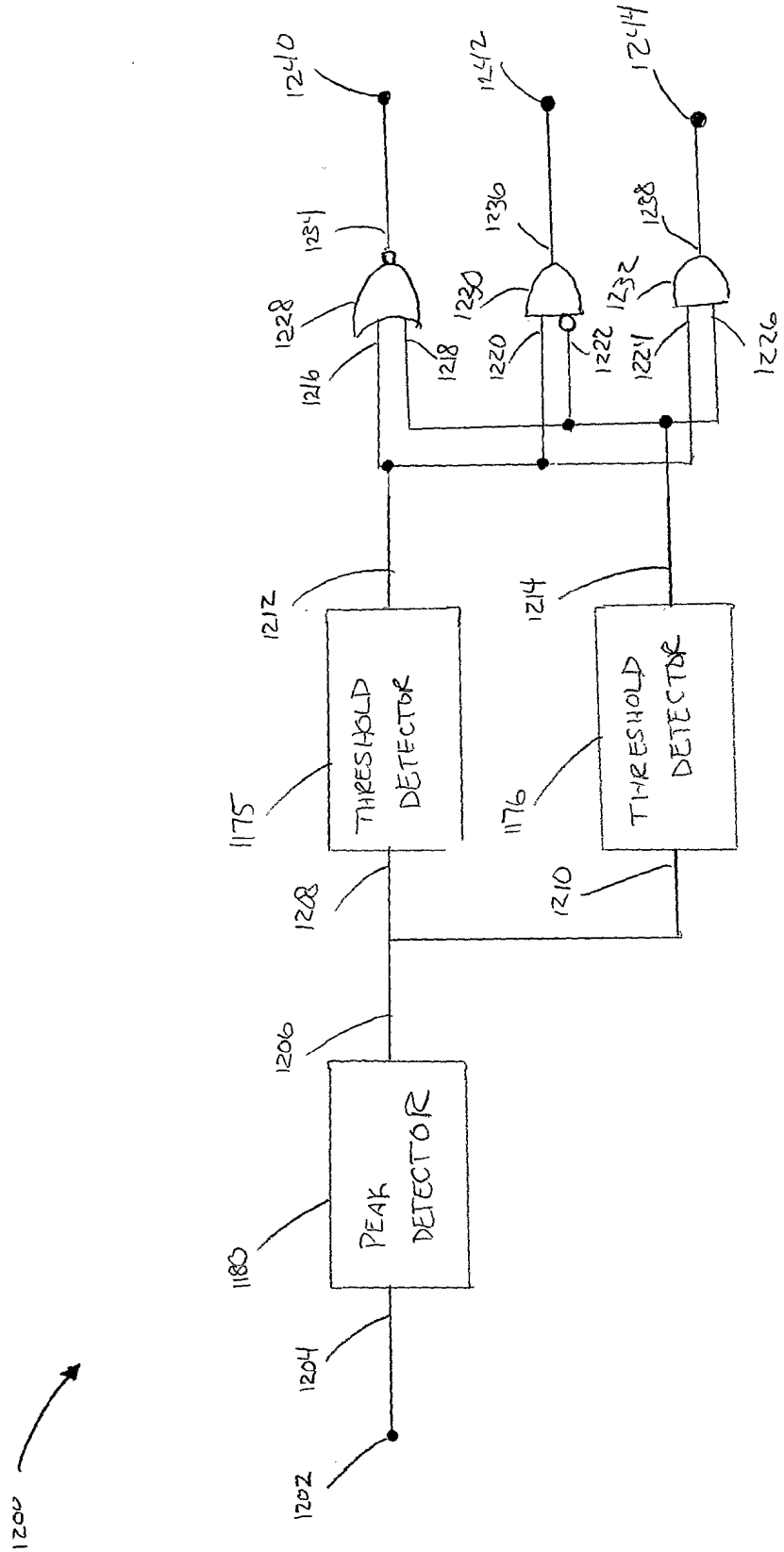

1200
1202
1204
1180
PEAK DETECTOR
1206
1208
1175
THRESHOLD DETECTOR
1212
1176
THRESHOLD DETECTOR
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1210
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1234
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Fig. 12(a)

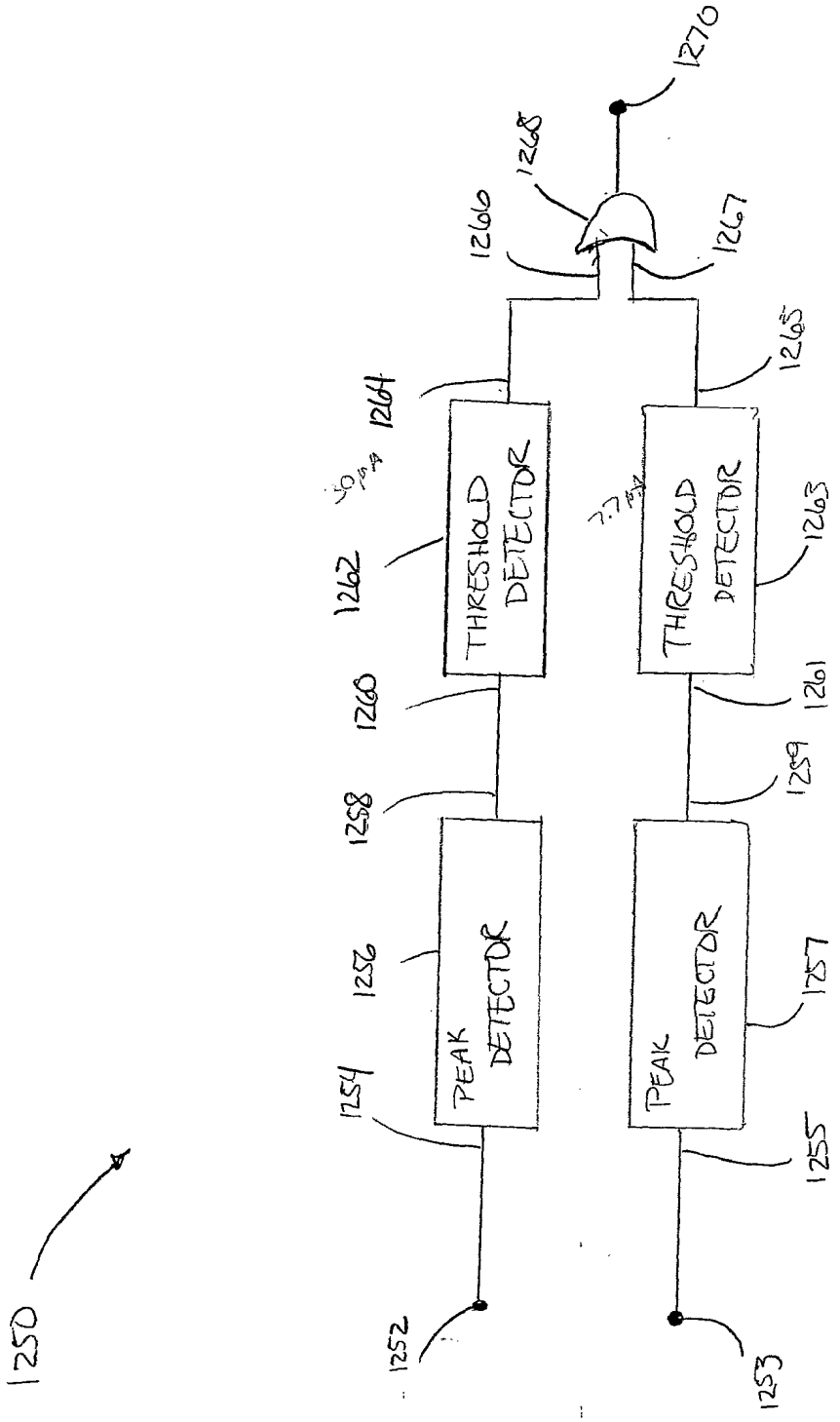

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1268
1270
PEAK DETECTOR
PEAK DETECTOR
THRESHOLD DETECTOR
THRESHOLD DETECTOR

FIG. 12(b)

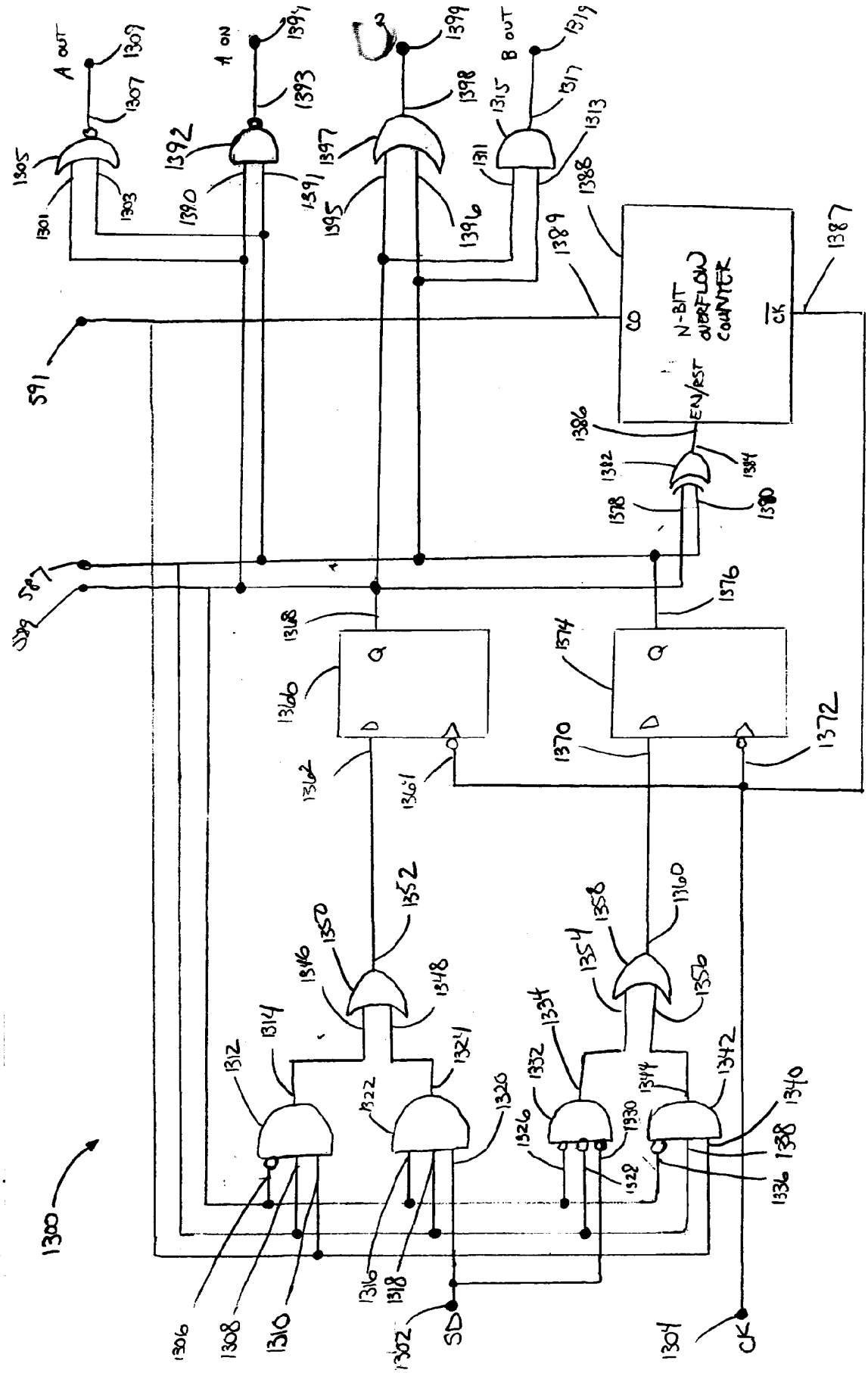


Fig. 13

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Apple EX1002 Page 230

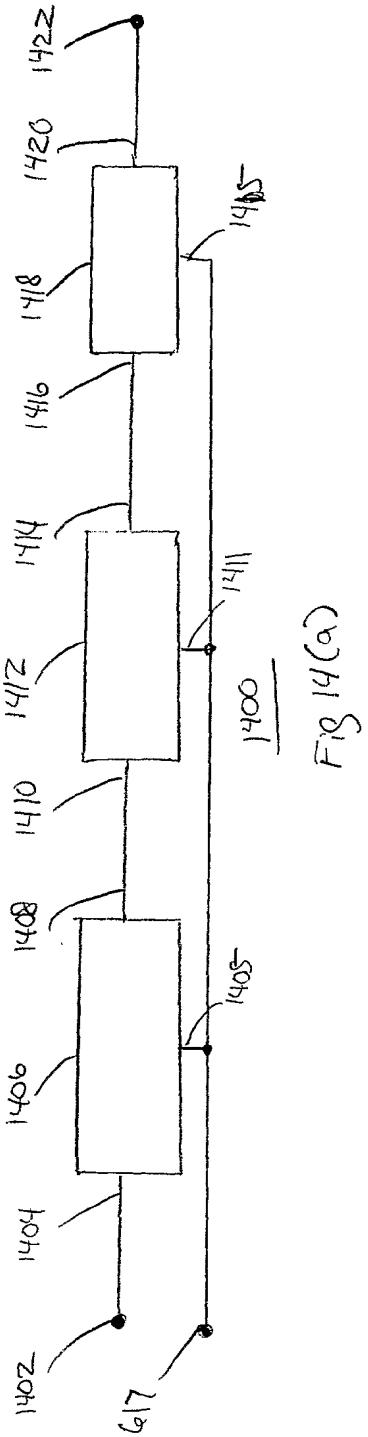


Fig 14(a)

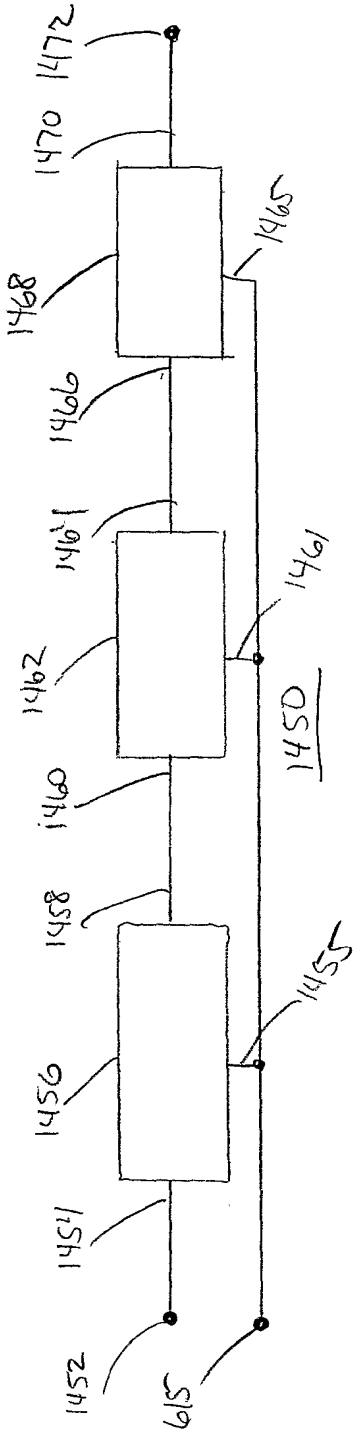
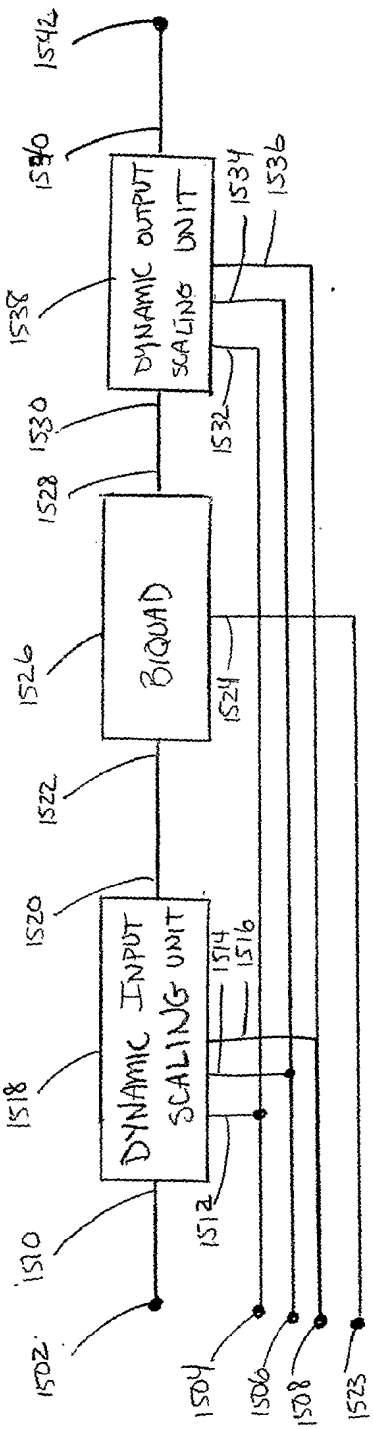


Fig. 14(b)


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1540
DYNAMIC OUTPUT SCALING UNIT
1534
1536
1538
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1532
1528
BIQUAD
1526
1524
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DYNAMIC INPUT SCALING UNIT
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1500

Fig. 15

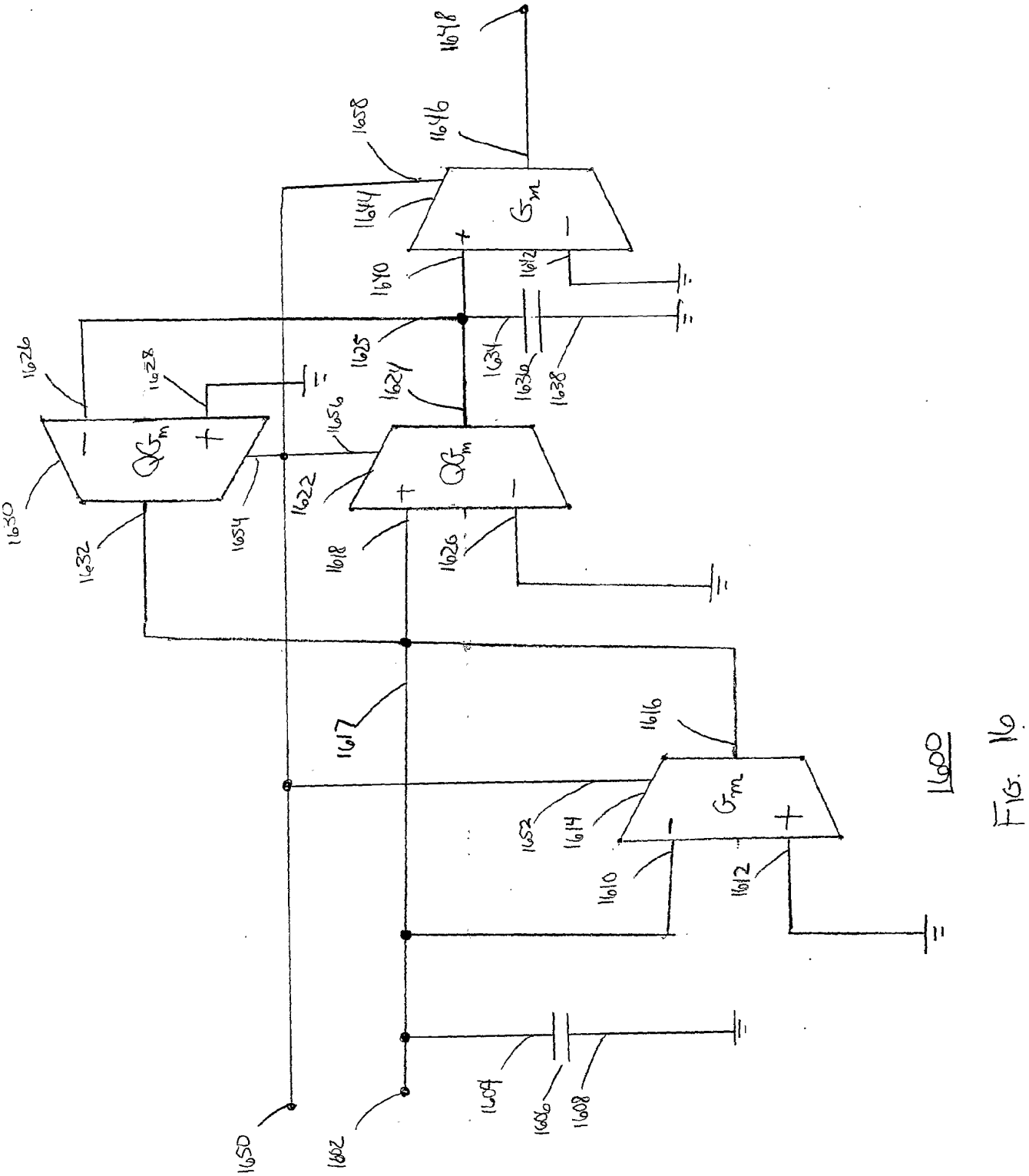
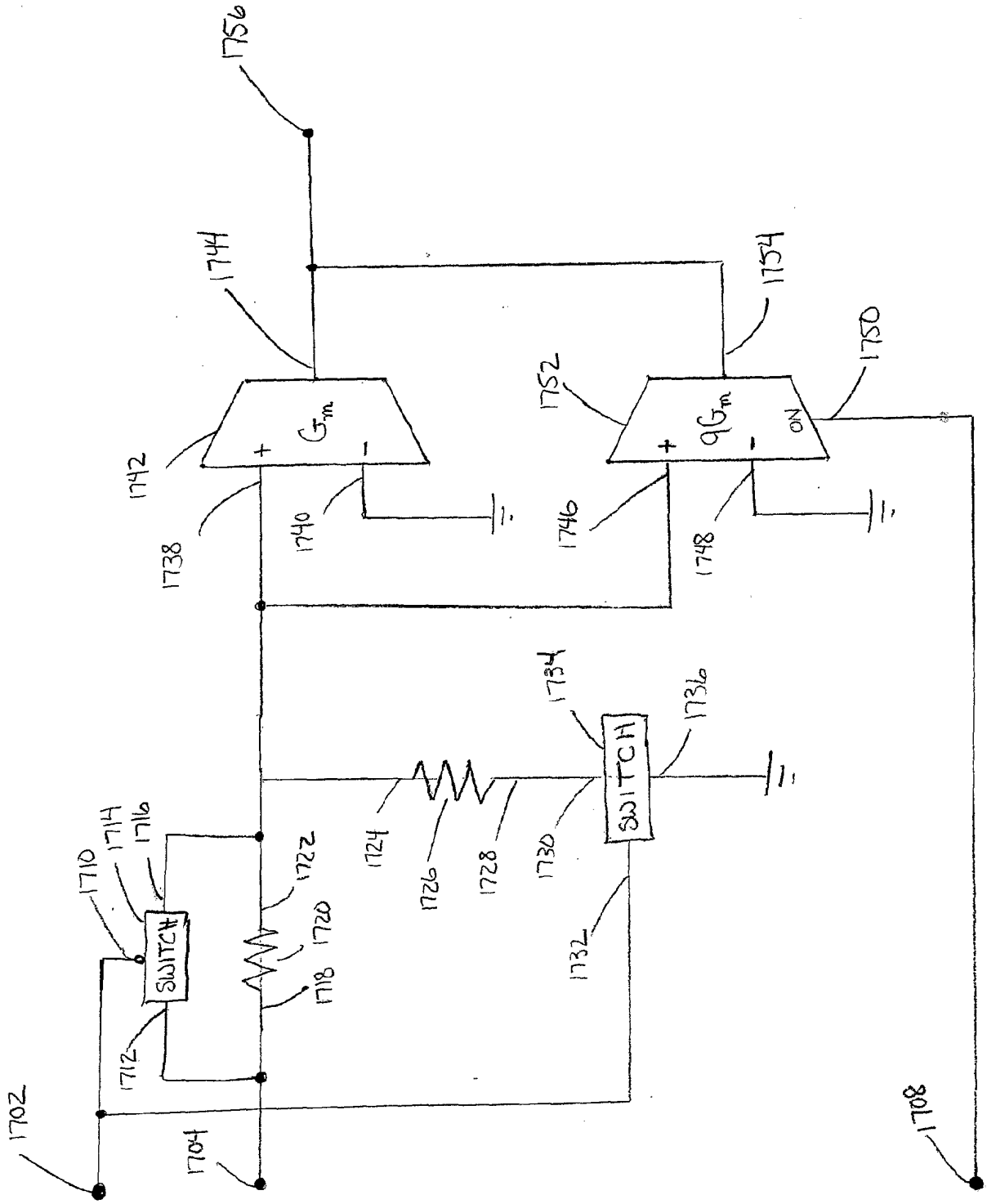
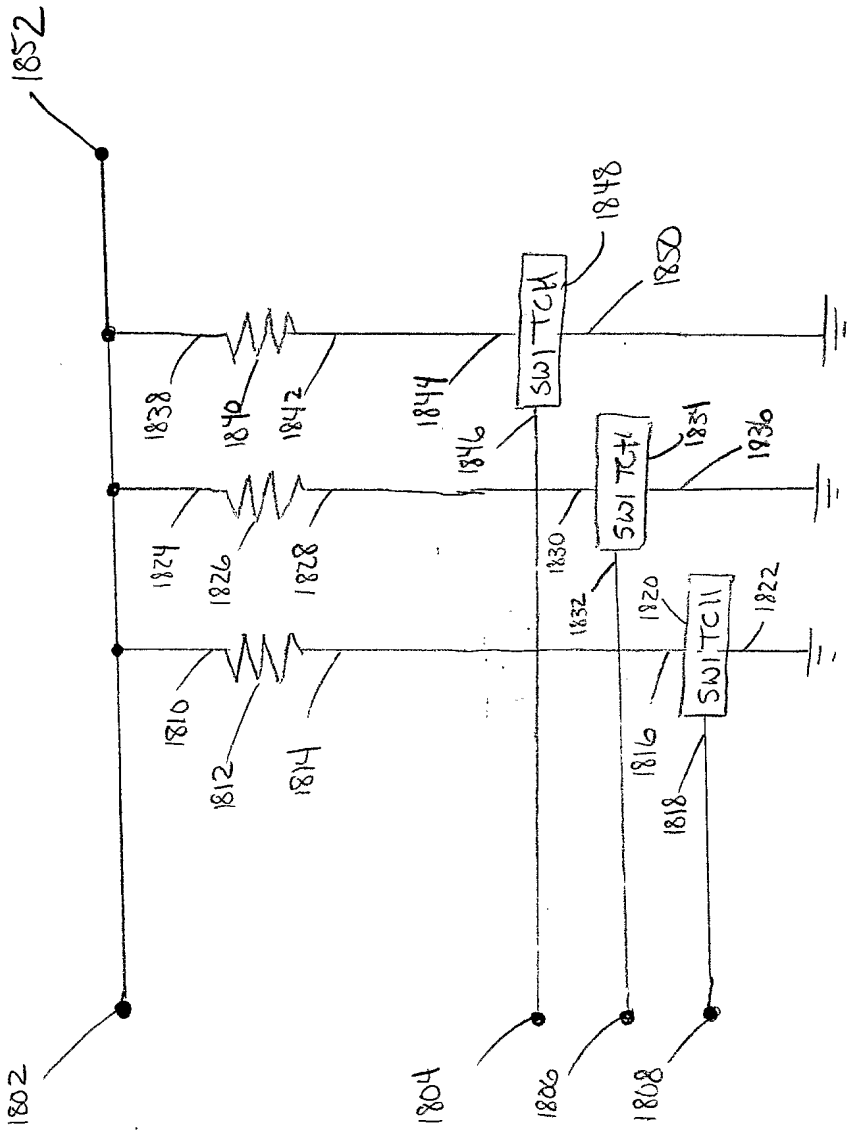

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Gm
QGm

Fig. 16


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G_m
$9G_m$
ON
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SWITCH
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SWITCH
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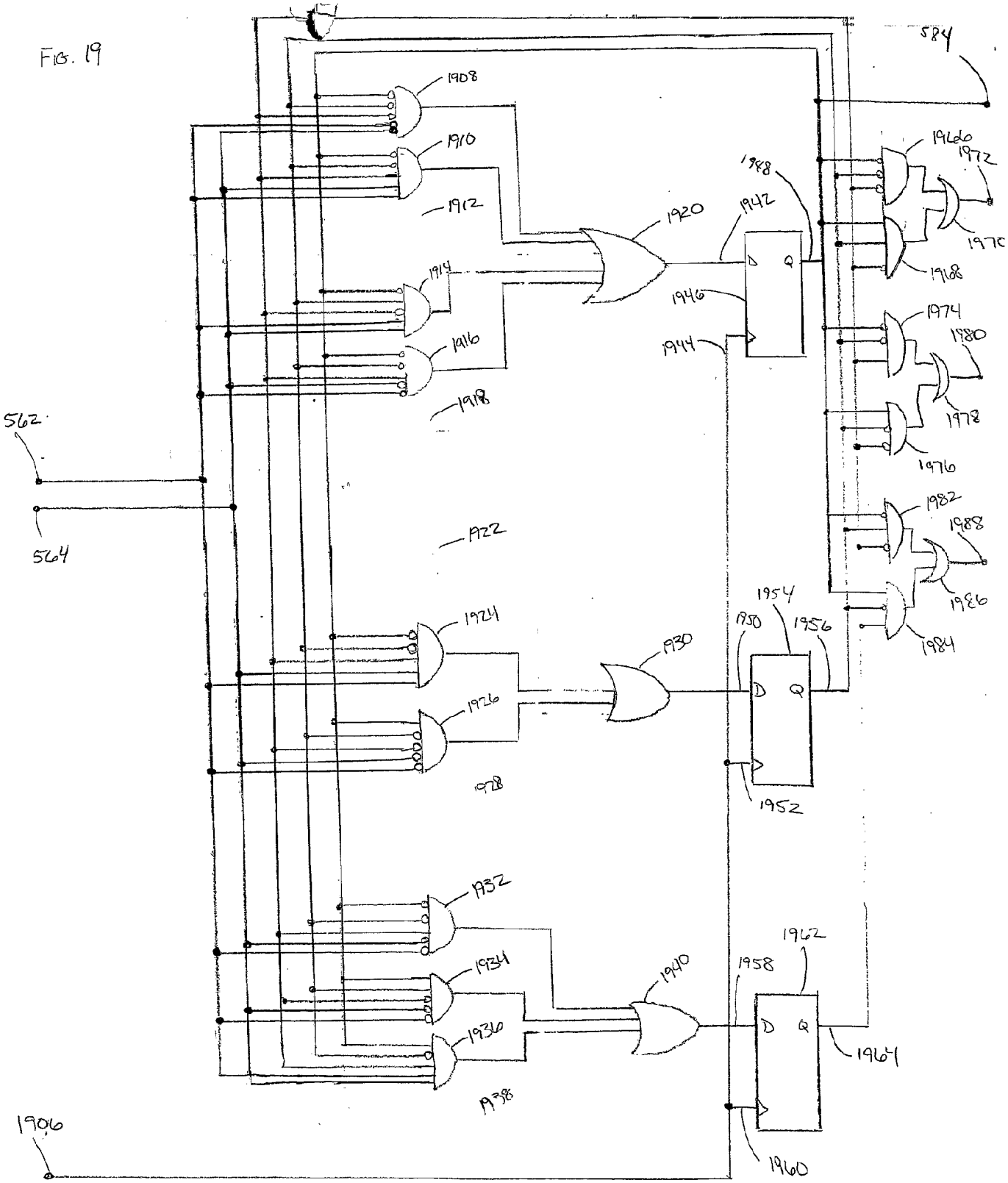
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FIG. 17


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SWITCH
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SWITCH
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SWITCH
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1808

1800

FIG. 18

FIG. 19


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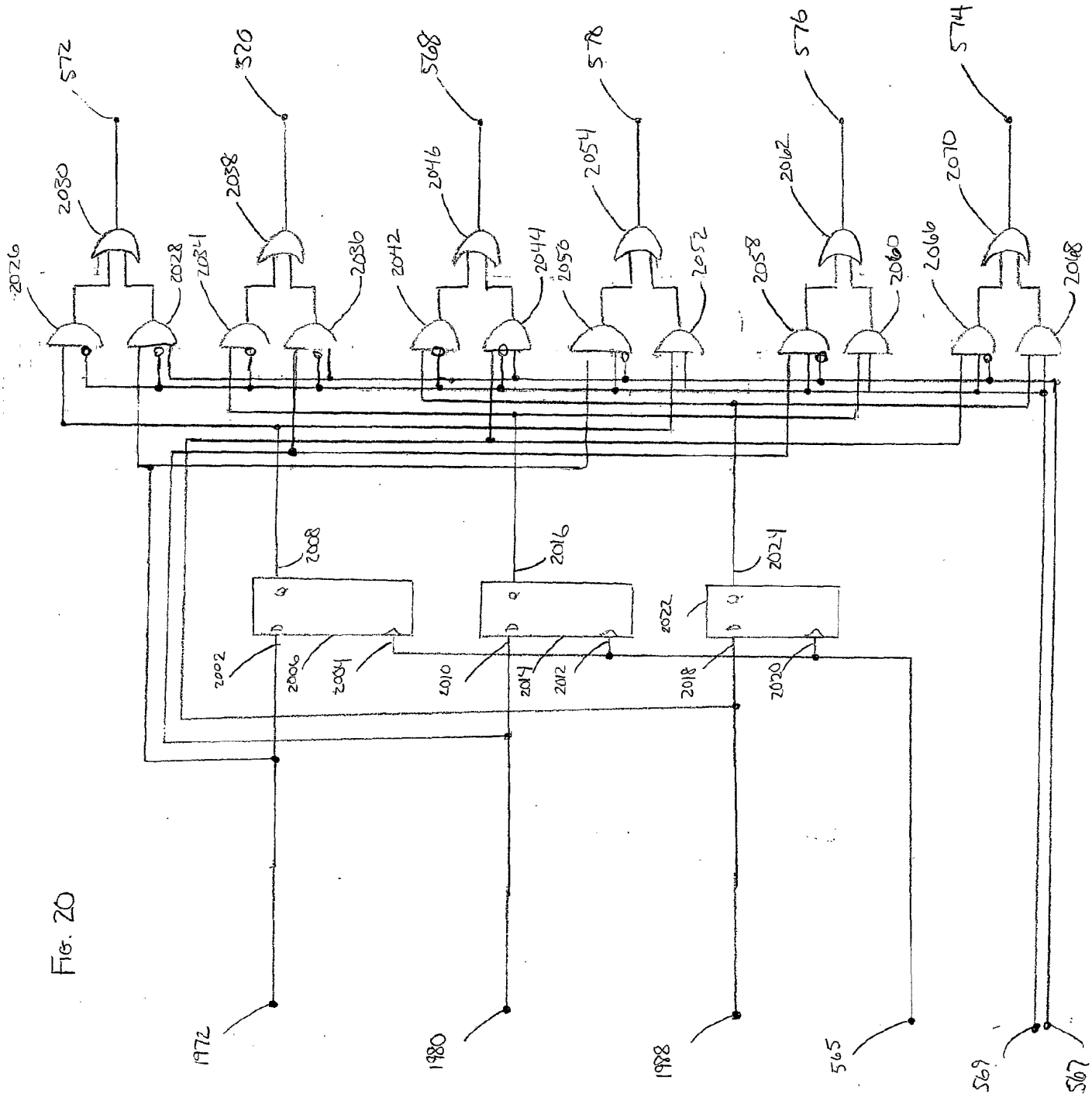

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Fig. 20

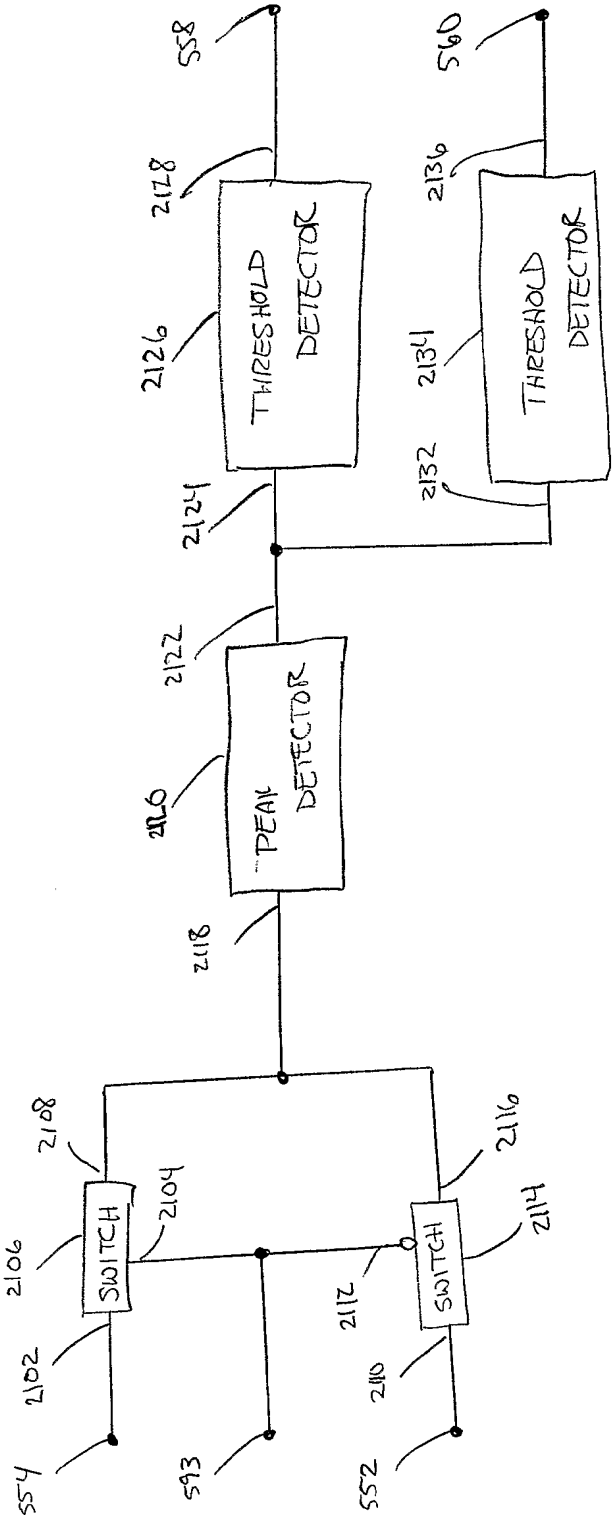
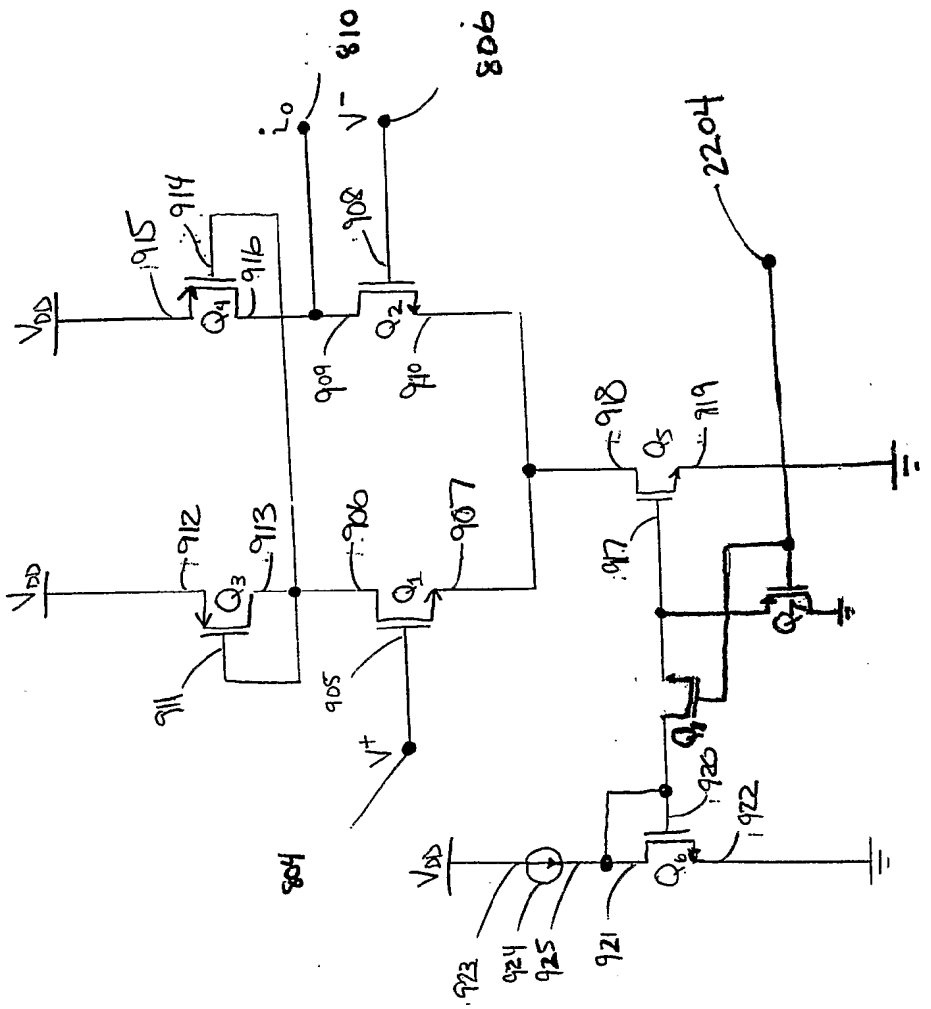

558
560
2128
2136
THRESHOLD DETECTOR
THRESHOLD DETECTOR
2126
2134
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2132
2122
PEAK DETECTOR
2120
2118
2108
2116
SWITCH
SWITCH
2106
2104
2114
2102
2112
2110
554
593
552

FIG. 21


i_o
810
806
V^-
2204
914
915
916
908
V_{DD}
Q_4
Q_2
909
910
918
Q_5
919
912
913
900
907
Q_3
Q_1
917
Q_7
911
905
V^+
804
920
922
Q_6
923
924
925
921

2200

FIG. 22

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US01/24593

A. CLASSIFICATION OF SUBJECT MATTER
IPC(7) : H04L 27/22
US CL : 375/316
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 375/316; 341/139 144, 155; 713/502

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
Please See Continuation Sheet

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5,541,600 A (BLUMENKRANTZ et al.) 30 July 1996, all	1-25
A	US 5,440,721 A (MORGAN et al.) 08 August 1995, all	1-25

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
12 October 2001 (12.10.2001)	16 NOV 2001
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703)305-3230	Authorized officer Shuwang Liu Telephone No. 703 308-9556

Form PCT/ISA/210 (second sheet) (July 1998)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US01/24593

Continuation of B. FIELDS SEARCHED Item 3:
EAST
search terms: signal processing, switch, detector

Form PCT/ISA/210 (second sheet) (July 1998)

Electronic Patent Application Fee Transmittal

Application Number:	15080432
Filing Date:	24-Mar-2016
Title of Invention:	Power Dissipation Reduction in Wireless Transceivers
First Named Inventor/Applicant Name:	Yannis Tsividis
Filer:	Roger W. Blakely/Jessica Clark
Attorney Docket Number:	10037P007CC2

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
SUBMISSION- INFORMATION DISCLOSURE STMT	2806	1	90	90
		Total in USD ($)		**90**

Electronic Acknowledgement Receipt

EFS ID:	27929585
Application Number:	15080432
International Application Number:	
Confirmation Number:	6094
Title of Invention:	Power Dissipation Reduction in Wireless Transceivers
First Named Inventor/Applicant Name:	Yannis Tsividis
Customer Number:	8791
Filer:	Roger W. Blakely/Jessica Clark
Filer Authorized By:	Roger W. Blakely
Attorney Docket Number:	10037P007CC2
Receipt Date:	29-DEC-2016
Filing Date:	24-MAR-2016
Time Stamp:	14:51:30
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$90
RAM confirmation Number	123016INTEFSW00001030022666
Deposit Account	022666
Authorized User	Jessica Clark

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

37 CFR 1.16 (National application filing, search, and examination fees)

37 CFR 1.17 (Patent application and reexamination processing fees)

37 CFR 1.19 (Document supply fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	10037P007CC2_20161229_IDS Letter.pdf	64003 3cdb8ccdc4885b3bf9916d946f05124d4460819e	no	1
Warnings:					
Information:					
2	Information Disclosure Statement (IDS) Form (SB08)	10037P007CC2_20161229_IDS.pdf	35182 87619c9f7b9dbc228f77c6a1fb0f7792aa5559e3	no	2
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
3	Foreign Reference	WO2004017589.pdf	5915349 7c5b80b546f912528f2097bb47c8f2c0cd8d7041	no	120
Warnings:					
Information:					
4	Non Patent Literature	Christensen_2003.pdf	483426 9bdc7fe12c72f6d406726bd4637568feacd9e18c	no	4
Warnings:					
Information:					
5	Non Patent Literature	Rudell_etal_1998.pdf	1814001 c4a8b27f7106b527e6b0d30c16d178341ae08dc3	no	6
Warnings:					
Information:					
6	Non Patent Literature	Schuchter_etal_2001.pdf	867616 948aa8cb2a7ce1f489d250c0a1f253b1082b6aaa	no	4
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			Total Files Size (in bytes):	9210374	

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application No.	15/080,432
Filing Date	March 24, 2016
First Inventor	Yannis Tsividis
Art Unit	2647
Examiner Name	Vuong, Quochien B
Attorney Docket No.	10037P007CC2 Conf. No. 6094

DUTY OF DISCLOSURE STATEMENT

In accordance with the duty of disclosure, enclosed is a copy of an Information Disclosure Statement (IDS) Citation Form PTO/SB/08 or PTO-1449, together with copies of the documents cited on that form, except for copies not required to be submitted (e.g., copies of U.S. patents and U.S. published patent applications need not be enclosed). This IDS and IDS Citation Form are being submitted before the mailing of a final Office Action or Notice of Allowance. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

The submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

OR

☒ None

☒ The IDS Filing Fee in the amount of $90.00 as set forth in 37 CFR 1.17(p) has been submitted herewith.

☒ It is requested that any requisite fees be debited from Deposit Account 02-2666.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of signature.

Signature	/Roger W. Blakely/	Date (MM-DD-YYYY)	12-28-2016
Name/Print	Roger W. Blakely, Jr.	Registration Number	25831

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.

Jessica A. Clark /Jessica A Clark/ Date 12/29/2016

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Substitute for form 1449A/PTO	*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	15/080,432
	Filing Date	03/24/2016
	First Named Inventor	Yannis Tsividis
	Group Art Unit	2647
	Examiner Name	Vuong, Quochien B
Sheet 1 of 1	Attorney Docket No: 10037P007CC2	

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	**Cite No [1]**	**Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.**	**T[2]**
		"Office Action Dated November 1, 2016; U.S. Patent Application No. 15/080,421", (11/1/2016)	

EXAMINER **DATE CONSIDERED**

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449) as modified by BSTZ 03/26/07

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

Electronic Acknowledgement Receipt

EFS ID:	28216532
Application Number:	15080432
International Application Number:	
Confirmation Number:	6094
Title of Invention:	Power Dissipation Reduction in Wireless Transceivers
First Named Inventor/Applicant Name:	Yannis Tsividis
Customer Number:	8791
Filer:	Roger W. Blakely/Jessica Clark
Filer Authorized By:	Roger W. Blakely
Attorney Docket Number:	10037P007CC2
Receipt Date:	31-JAN-2017
Filing Date:	24-MAR-2016
Time Stamp:	12:38:38
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	10037P007CC2_20170131_IDS Letter.pdf	65284 cc55cfd0cbeb22e8a19bff3dd8a214088a272d29	no	1

Warnings:

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Information:					
2	Information Disclosure Statement (IDS) Form (SB08)	10037P007CC2_20170131_IDS.pdf	22739 61a2db95fbab34e2daa827e12832da01b31535e1	no	1
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
3	Other Reference-Patent/App/Search documents	10037P007CC_20161101_OA.pdf	943885 23bee482c87e05b8c1c498bb3ba2b8eed95f7300	no	23
Warnings:					
Information:					
		Total Files Size (in bytes):	1031908		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

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New International Application Filed with the USPTO as a Receiving Office

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OR

☒ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

OR

☐ None

☐ The IDS Filing Fee in the amount of $90.00 as set forth in 37 CFR 1.17(p) has been submitted herewith.

☒ It is requested that any requisite fees be debited from Deposit Account 02-2666.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of signature.

Signature	/Roger W Blakely/	Date (MM-DD-YYYY)	01-31-2017
Name/Print	Roger W. Blakely, Jr.	Registration Number	25831

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.

Jessica A. Clark /Jessica A Clark/ *Date* *01-31-17*

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application. No.	:	15/080,432	Confirmation No. 6094
Inventor(s)	:	Yannis Tsividis	
Filed	:	03/24/2016	
TC/A.U.	:	2647	
Examiner	:	Vuong, Quochien B	
Docket No.	:	10037P007CC2	
Customer No.	:	8791	

Mail Stop Amendment
Commissioner for Patents
PO Box 1450
Alexandria VA 22313-1450

AMENDMENT

Sir:

In response to the Office Action of November 1, 2016, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 9 of this paper.

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Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A method of power dissipation control in a receiver circuit within a battery powered mobile device when the receiver circuit is receiving and processing an RF input signal that includes a desired signal and an interferer signal, the method comprising:

determining a strength of the desired signal with respect to the strength of the interferer signal;

causing a ~~variable~~ decrease in power dissipation of a signal path within the receiver circuit and a resultant decreased battery drain, by ~~variably scaling~~ dynamically adjusting both of, a bias current of a component in a signal path of the receiver circuit and an impedance of a component in the signal path of the receiver circuit, based on the strength of the desired signal relative to the strength of the interferer signal, upon determination that the strength of the desired signal has increased relative to the strength of the interferer signal;

causing ~~a variable~~ an increase in power dissipation of the signal path within the receiver circuit and a resultant increased battery drain, by ~~variably scaling~~ dynamically adjusting both of, the bias current of the component in the signal path of the receiver circuit and the impedance of the component in the signal path of the receiver circuit, based on the strength of the desired signal relative to the strength of the interferer signal, upon determination that the strength of the desired signal has decreased relative to the strength of the interferer ~~signal;~~signal.

~~wherein the variably scaling includes varying the bias current of the component in the receiver circuit through a plurality of values, responsive to the strength of the desired signal relative to the strength of the interferer signal, where the plurality of values is greater than or equal to three in number.~~

2. (currently amended) The method of claim 1, wherein the bias current of the component in the receiver circuit is ~~reduced~~ dynamically adjusted by ~~switching~~ one or both of, a

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changing of the value of an impedance ~~that appears~~ across a voltage, a changing the base voltage of a device whose emitter is connected to ground through a resistor, thereby optimizing the power drain from the battery.~~changing the bias current.~~

3. (currently amended) A method of power dissipation control in a receiver circuit within a battery powered mobile device when the receiver circuit is receiving an RF input signal that includes a desired signal and an interferer signal, the method comprising:

determining a strength of the desired signal with respect to the interferer signal, wherein the receiver circuit comprises a defined signal path between the RF input signal and a processed signal output;

causing a ~~variable~~ decrease in power dissipation of the defined signal path within the receiver circuit and a resultant decreased battery drain, by ~~variably scaling~~ dynamically changing an impedance of a component in the signal path of the receiver circuit upon determination that the strength of the desired signal has increased relative to the strength of the interferer signal; and

causing ~~a variable~~ an increase in power dissipation of the defined signal path within the receiver circuit and a resultant increased battery drain, by ~~variably scaling~~ dynamically changing the impedance of the component in the signal path of the receiver circuit upon determination that the strength of the desired signal has decreased relative to the strength of the interferer signal;

wherein the ~~variable scaling~~ dynamically changing of impedance includes:

setting the impedance of the component in the receiver circuit in between a high level and a low level;

dynamically adjusting the impedance of the component in the receiver circuit up or down; and

wherein the ~~variable scaling~~ dynamically changing of impedance occurs while the receiver circuit is processing signals received from the RF input ~~signal~~.

4. (currently amended) The method of claim 3 wherein ~~variably scaling~~ dynamically changing the impedance of a component in the receiver circuit comprises ~~variably scaling~~ continuously adjusting an impedance of a low noise amplifier (LNA) in the signal path.

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5. (currently amended) The method of claim 3 wherein ~~variably scaling~~ dynamically changing the impedance of a component in the receiver circuit comprises ~~variably scaling~~ continuously adjusting an impedance of a mixer in the signal path.

6. (currently amended) The method of claim 3 wherein ~~variably scaling~~ dynamically changing the impedance of a component in the receiver circuit comprises ~~variably scaling~~ continuously adjusting an impedance of a filter in the signal path.

7. (currently amended) The method of claim 3, wherein the impedance of a component in the receiver circuit comprises a resistance, and wherein a value of the resistance is ~~increased~~ adjusted by opening switches across one or more portions of the resistance.

8. (original) The method of claim 3, wherein the defined signal path includes components that comprise: a low noise amplifier (LNA), a filter, a mixer.

9. (original) The method of claim 8 wherein the component is a low noise amplifier.

10. (original) The method of claim 8 wherein the component is a filter.

11. (original) The method of claim 8 wherein the component is a mixer.

12. (currently amended) A method of power dissipation control in a receiver circuit within a battery powered mobile device when the receiver circuit is receiving an RF input signal that includes a desired signal and an interferer signal, the method comprising:

determining a strength of the interferer signal present in the received RF input signal;

causing a ~~variable~~ decrease in power dissipation of a signal path within the receiver circuit and a resultant decreased battery drain, by ~~variably scaling~~ dynamically changing an impedance of a component in the signal path of the receiver circuit upon determination that the strength of the interferer signal has decreased;

causing a ~~variable~~ increase in power dissipation of the signal path within the receiver circuit and the resultant decreased battery drain, by ~~variably scaling~~ dynamically changing the

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impedance of the component in the signal path of the receiver circuit upon determination that the strength of the interferer signal has increased;

wherein dynamically changing the ~~variable scaling~~ impedance includes:

~~switching~~ dynamically scaling the impedance of the component in the signal path of the receiver circuit through a plurality of ~~three or more~~ levels, between a high level and a low level from at least an intermediate initial point, responsive to the strength of the interferer signal present in the received RF input signal, wherein the high and low levels represent a maximum power saving and a maximum power dissipation; and

wherein the dynamically changing the impedance variable ~~scaling~~ occurs while the receiver circuit is processing signals received from the RF input signal.

13. (original) The method of claim 12, wherein the impedance of the component in the receiver circuit comprises a resistance, and wherein the value of the resistance may be increased by opening switches across one or more portions of the resistance.

14. (currently amended) A method of controlling power dissipation in a receiver circuit within a battery powered mobile device when the receiver circuit is receiving and processing an RF input signal in a signal path of the receiver circuit that includes a desired signal and an interferer signal, the method comprising:

determining a strength of the interferer signal present in the received RF input signal;

causing a decrease in power dissipation of the signal path of the receiver circuit resulting in a decrease in drain on battery life, by ~~variably scaling~~ dynamically varying a gain of a ~~component~~ gain stage in the signal path of the receiver circuit and dynamically changing an impedance of a component in the signal path of the receiver circuit, upon determination that the strength of the interferer signal has decreased; or

alternately causing an increase in power dissipation of the signal path of the receiver circuit resulting in an increase in drain on battery life, by ~~variably scaling~~ dynamically adjusting the gain of the ~~component~~ gain stage in the signal path of the receiver circuit and dynamically changing an impedance of a component in the signal path of the receiver circuit, upon determination that the strength of the interferer signal has increased;

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causing an increase in power dissipation of the signal path of the receiver circuit resulting in an increase in drain on battery life, by ~~variably scaling~~ dynamically adjusting the gain of the ~~component~~ gain stage in the signal path of the receiver circuit and dynamically changing an impedance of a component in the signal path of the receiver circuit, upon determination that the strength of the interferer signal has increased;

wherein the ~~variable scaling~~ dynamically adjusting the gain includes:

setting the gain of the component in the signal path of the receiver circuit in between a high level and a low level; and

~~adjusting~~ varying the gain of the ~~component~~ gain stage in the signal path of the receiver circuit up or down; and

wherein the dynamically changing the impedance includes:

setting the impedance of the component in the receiver circuit in between a high level and a low level;

continuously adjusting the impedance of the component in the signal path of the receiver circuit up or down;

thereby optimizing the power dissipation of the battery powered mobile device.

15. (original) The method of claim 14, wherein the gain of the component in the signal path of the receiver circuit is varied by increasing a current in a differential pair and /or increasing a load resistance using switches.

16. (currently amended) A mobile communications device, comprising:

a receiver circuit for receiving an RF input signal that includes a desired signal and an interferer signal;

a battery that powers the mobile communications device including the receiver circuit;

wherein a strength of the desired signal is determined with respect to the strength of the interferer signal;

wherein a ~~variable~~ decrease in power dissipation of a signal path within the receiver circuit and a resultant decreased battery drain is caused by ~~variably scaling~~ dynamically changing an impedance of a component in a signal path of the receiver circuit upon

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determination that the strength of the desired signal has increased relative to the strength of the interferer signal; and

wherein ~~a variable~~ an increase in power dissipation of the signal path within the receiver circuit and a resultant increased battery drain, is caused by ~~variably scaling~~ dynamically changing the impedance of the component in the signal path of the receiver circuit upon determination that the strength of the desired signal has decreased relative to the strength of the interferer signal; and

wherein the ~~variable scaling~~ dynamically changing an impedance includes:

setting the impedance of the component in the receiver circuit in between a high level and a low level; and

adjusting the impedance of the component in the receiver circuit up or down; and

wherein the ~~variable scaling~~ dynamically changing the impedance occurs while the receiver circuit is processing signals received from the RF input signal.

17. (previously presented) The mobile communication device of claim 16, wherein the impedance of the component in the receiver circuit comprises a resistance, and wherein a value of the resistance may be varied by opening and closing switches across one or more portions of the resistance responsive to the determined strength of the desired signal with respect to the interferer signal.

18. (currently amended) A method for conserving battery power in a mobile communication device, the method comprising:

receiving a radio signal by a radio receiver, of ~~the~~ a wireless transceiver, that include a desired signal and an interferer signal;

powering to the ~~radio~~ wireless transceiver by a battery;

processing of the received radio signals in a signal path within the radio receiver;

determining the strength of the interferer signal by a circuit coupled to the signal path of the receiver;

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~~adjusting~~ dynamically changing a gain of a gain stage and dynamically changing an impedance of the signal path of the receiver ~~through a plurality of more than two levels~~ responsive to the determined strength of the interferer signal;

~~where in~~ wherein adjusting the gain of the gain stage and impedance of the signal path result in improving a power drain from the battery.

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REMARKS/ARGUMENTS

This Amendment is in response to the Office Action mailed November 1, 2016. In the Office Action, all claims have been rejected. Claims 1-7, 12, 14, 16 and 18 have been amended. Support for the amendments may be found, for example, in paragraphs [0008]-[0009], [0012]-[0015], [0050], [0053]-[0055], [0058], [0068] and [0072] of the specification as-filed.

112 Rejection

Claims 1, 2, 12, 13 and 18 were rejected under 35 USC 112(a) or 35 USC 112 (Pre-AIA), first paragraph for failing to comply with the written description requirement. In doing so, the Office Action states that the claims contain subject matter not described in the specification.

Claims 1, 2, 12 and 18 have been amended to fully comply with the written requirement and overcome the objections. Support is presented herein below for the various amendments made.

The Office Action states "Claims 1 and 2 recite 'wherein the variably scaling includes varying the bias current of the component in the receiver circuit through a plurality of values, responsive to the strength of the desired signal relative to the strength of the interferer signal, where the plurality of values is greater than or equal to three in number.' in claim 1, lines 14-17, which was not described in the specification."

The applicant would like to point out the support for the claim language can be found in paragraph [0068] of the specification as-filed, which states "The included examples are explained for the exemplary situation where biasing and other parameters are set for the worst case conditions, and then changed to save power when it is discovered that the conditions are better than worst case. Alternately, the bias current and other parameters can be set for maximum power savings, or an intermediate point, and power can be adjusted from there." In this case, the specification provides for an intermediate set point for the gain, bias and impedance between the worst case input conditions (e.g., the highest dissipation) and the best case input conditions (e.g., the lowest power dissipation) as sufficient to indicate "where a plurality of values is greater than three in number". But the applicant has changed the terminology to match that in the

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specification using "dynamically adjusting" and removed the last feature of claim 1, to overcome the objection of the examiner in this regard. As noted in the American Heritage Dictionary of Student Science, the meaning of the term **dynamic** (adverb: **dynamically**): "Characterized by continuous change or activity. "Cite": dynamic. (n.d.) *The American Heritage® Dictionary of Student Science, Second Edition*. (2014). Copyright © 2014 by Houghton Mifflin Harcourt Publishing Company. Published by Houghton Mifflin Harcourt Publishing Company. All rights reserved.

The Office Action further states "Claims 12 and 13 recite 'switching the impedance of the component in the receiver circuit through a plurality of three or more levels between a high level and a low level responsive to the strength of the interferer signal present in the received RF input signal' in claim 12, lines 13-15, which was not described in the specification."

Here again the applicant directs the attention of the examiner to the support for claim language in paragraph [0068] of the application as-filed, where an initial set point in between the high and low values is clearly indicated. The applicant has amended the claim 12 to read clearly on the specification and overcome the objection. Claim 13 which is rejected as a dependent claim hence should also now be allowable.

The Office Action also states "Claim 18, recites 'adjusting a gain and an impedance of the signal path of the receiver through a plurality of more than two levels responsive to the determined strength of the interferer signal;' in claim 18, lines 9-10, which was not described in the specification."

The applicant has amended the claim to read directly on the specification as required by the examiner and overcome the above 112 rejection.

Claim 18 was also rejected under 35 USC 112(b) or 35 USC 112 (pre-AIA), second paragraph, as being indefinite.

The examiner has rejected the use of "the transceiver" as having no antecedent basis. The applicant has amended the claim to overcome that objection of the examiner.

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Accordingly, withdrawal of the rejections of claims 1, 2, 12, 13 and 18 under 35 USC 112 is respectfully requested.

35 USC 102 Rejection

Claim 14 was rejected under USC 102(b) as being anticipated by Clark (US 5,001,776, hereinafter "Clark").

Clark states in the aim of the invention:

> "Accordingly, it is an object of the present invention to provide an RF communication system transceiving devices capable of adapting their operation to minimize intermodulation distortion." Clark, col. 1, lines 59-62.

Clark describes varying the amplification of the signals by varying the gain of the circuit and by using a square wave of varying amplitude from the local oscillator at the mixer to reduce the intermodulation distortion. The use of high gain in the amplifiers and high value square wave generation by the local oscillator, result in high current drain from the battery and reduce battery life. Hence Clark uses **a two step gain control and a feed back to the transmitting unit** to increase the power of the desired signal so that the gain and amplitude of the local oscillator signals can be reduced to save power.

This is completely different from what is specified in claim 14 where the aim is the optimization of the power drain from the battery based on the relationship between the interferer and the desired frequency input in the radio frequency section of the transducer. The adjustment that is done in claim 14 is a dynamic change, that is based on continuous monitoring of the interferer signal levels to optimize the changes in gain and impedance of the devices and circuits in the path of the RF signal.

Clark on the other hand uses threshold settings as described in his specification and claims to switch between high gain levels and a low gain states to conserve power. The examiner equates col. 2 line 34 to col. 4 line 66 to claim 14. The applicant respectfully disagrees. Clark indicates an intermediate frequency (IF) section where the frequency is an intermediate frequency formed by mixing the local oscillator frequency with the input frequency. See, e.g.,

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Clark, FIG. 1. This is not part of claim 14. Claim 14 is mainly directed at optimizing the power drain of the input radio frequency section of the radio based on the interferer signal has increased or decreased.

As can be clearly seen, Clark does not cover the changing and use of bias and impedance for power optimization. Clark also uses the term gain in one location (see, e.g., Clark, col. 4, lines 34-37). Also, the **amplification factors** of Clark (and thus the current drain) of the RF amplifier 108 and the IF amplifier 122 may be varied (via control lines 138 and 140 respectively) by the controller 130.

Hence in order to further eliminate the objection of the examiner, the applicant has currently amended claim 14 to dynamically varying a gain of a gain stage in the signal path and also an impedance of a component in the signal path based on the determination of the strength of the interferer signal present in the received RF input signal, if it has decreased or increased. Support for this feature can be found in paragraphs [0009], [0012] and [0058] of the specification as-filed.

Claims 1-13 and 15-18 were rejected under 35 U.S.C 103 as unpatentable over Clark (US 5,001,776 hereinafter "Clark") in views of Leifso et al. (US 6,870,425 hereinafter "Leifso").

With respect to independent claim 1, Clark according to the examiner discloses variably scaling the gain of a gain component in the receiver circuit through a plurality of values to address the power dissipation. The examiner indicates that Clark does not specifically disclose variably scaling a bias current of a component in the receiver circuit upon determination of the changes in desired signal relative to the interferer signal. Instead, the examiner points to Leifso as disclosing varying a gain of an amplifier by variably scaling a bias with a plurality of values greater than or equal to three in number. This change in bias to change the gain of an amplifier appears to be equated to the change in bias current to reduce power dissipation by the examiner.

The applicant disagrees with the examiner. Both Clark and Leifso discuss only changes in the gain of the amplifier. Leifso discusses changing the bias to change the gain of an

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amplifier. The aim of Leifso is to provide a variable gain amplifier capable of providing a linear amplification with high dynamic range for even the small signals received. See, e.g., Leifso, column 2, line 28, FIGS. 2-3. This is different from claim 1 in that bias current and impedance are both dynamically adjusted to optimize power dissipation as shown in support for claim language in paragraph [0009] of the specification, which states: "...present invention use **bias current reduction, impedance scaling, gain, and other dynamic changes** either **separately or in combination to reduce power dissipation** in response to better than worst case conditions..." Further, paragraph [0072] of the specification indicates adjustment of the bias current and impedance, and Fig. 10 and its explanation showing separate bias and impedance adjust signals.

In addition, Leifso uses a pair of degeneration transistors to provide the variable bias control for controlling the gain of the RF or IF amplifier. Leifso does not indicate any relationship to the input interferer levels in deciding the gain control. Leifso also does not discuss any sensing of the relative interferer level.

Hence combining Clark who teaches gain switching in an amplifier between a high and low value and Leifso who teaches using a pair of regeneration transistors as part of the gain control, without any reference to the interferer signals does not provide a path to disclosing claim 1, which is directed to dynamically changing the gain, bias and impedance of the devices and circuits in the signal path, independently or in an optimum combination that provides the best case battery power saving for the level of interferer signal present with respect to the desired signal in the RF radio receiver section of the mobile transceiver.

With respect to dependent claim 2, which is allowable by virtue of its dependency from claim 1, Leifso merely discusses changing the gain of an amplifier in the receiver path by changing an impedance that appears across a voltage that changes the bias current of the amplifier and change its gain. As discussed with bias change to change gain, the impedance change to indirectly change gain of an amplifier is not what is being specified in claim 2. Claim 2 is directed to optimizing power drain from a battery by dynamically adjusting "the bias current of the component in the receiver circuit" by changing "an impedance across a voltage" and/or

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"the base voltage of a device whose emitter is connected to ground through a resistor", to achieve an optimized operation of the receiver while reducing the current drain of the radio receiver. See, e.g., support for claim language in paragraphs [0009], [0050], [0055], [0058] and [0072] of the specification as-filed.

The same reasoning as discussed above applies for claim 3, and dependent claims 4-11, where a dynamic change of impedance of a component in the signal path is used to optimize power dissipation. Clark in view of Leifso only uses change of impedance indirectly to change bias current of an amplifier to change the gain of the amplifier. This is completely different from claims 3-11.

Claims 12 and claim 18 were also rejected referencing Clark in view of Leifso. As previously discussed with respect to claim 1, neither Clark alone nor Clark in view of Leifso teach the optimization of an impedance of a device in the signal path of the receiver based on the strength of an interferer signal to improve power dissipation.

For the foregoing reasons, it is believed that all claims currently under consideration are in condition for allowance.

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CONCLUSION

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 04/27/2017

By _____
Roger W. Blakely, Jr.
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1279 Oakmead Parkway
Sunnyvale, California 94085

CERTIFICATE OF TRANSMISSION (37 CFR 1.8A)

I hereby certify that this correspondence is being EFS Web transmitted to the USPTO on the date shown below.

Date: 04/27/2017

Jessica A. Clark 4/27/2017
Jessica A. Clark *Date*

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Apple EX1002 Page 266

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application. No.	:	15/080,432	Confirmation No. 6094
Applicant	:	Yannis Tsividis	
Filed	:	03/24/2016	
TC/A.U.	:	2647	
Examiner	:	Vuong, Quochien B	
Docket No.	:	10037P007CC2	
Customer No.	:	8791	

Commissioner for Patents
PO Box 1450
Alexandria VA 22313-1450

AUTHORIZATION FOR EXTENSION OF TIME, ALL REPLIES

Sir:

Authorization is given to treat any concurrent or future reply requiring a petition for an extension of time under 37 CFR §1.136(a) for its timely submission, as incorporating a petition for extension of time for the appropriate length of time. If any other petition is necessary for consideration of this paper, it is hereby so petitioned. Please charge any shortage in fees in connection with the filing of this paper, including extension of time fees, to Deposit Account 02-2666 and please credit any excess fees to such deposit account.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 04/27/2017

By _____
Roger W. Blakely, Jr.
Reg. No. 25,831
Tel.: (714) 557-3800 (Pacific Coast)

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CERTIFICATE OF TRANSMISSION (37 CFR 1.8A)

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Date: 04/27/2017

Jessica A. Clark 4/27/2017
Jessica A. Clark *Date*

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Apple EX1002 Page 267

Electronic Patent Application Fee Transmittal

Application Number:	15080432
Filing Date:	24-Mar-2016
Title of Invention:	Power Dissipation Reduction in Wireless Transceivers
First Named Inventor/Applicant Name:	Yannis Tsividis
Filer:	Roger W. Blakely/Jessica Clark
Attorney Docket Number:	10037P007CC2

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension - 3 months with $0 paid	2253	1	700	700
Miscellaneous:				
			Total in USD ($)	**700**

Electronic Acknowledgement Receipt

EFS ID:	29055121
Application Number:	15080432
International Application Number:	
Confirmation Number:	6094
Title of Invention:	Power Dissipation Reduction in Wireless Transceivers
First Named Inventor/Applicant Name:	Yannis Tsividis
Customer Number:	8791
Filer:	Roger W. Blakely/Jessica Clark
Filer Authorized By:	Roger W. Blakely
Attorney Docket Number:	10037P007CC2
Receipt Date:	27-APR-2017
Filing Date:	24-MAR-2016
Time Stamp:	18:54:02
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$700
RAM confirmation Number	042817INTEFSW00005917022666
Deposit Account	022666
Authorized User	Jessica Clark

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

37 CFR 1.16 (National application filing, search, and examination fees)

37 CFR 1.17 (Patent application and reexamination processing fees)

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Extension of Time	10037P007CC2_20170427_Ext.pdf	29014 6675d7f84a66490205792dd609a0ac3004b4f377	no	1
Warnings:					
Information:					
2		10037P007CC2_20170427_Amd.pdf	621949 9518f3574e9fc049c0c8c6ded4304d2793e4b69b	yes	16

Multipart Description/PDF files in .zip description

Document Description	Start	End
Amendment/Req. Reconsideration-After Non-Final Reject	1	1
Claims	2	8
Applicant Arguments/Remarks Made in an Amendment	9	15
Authorization for Extension of Time all replies	16	16

Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	30579 25d19f4d7096f1b22554c08f1c858311784bd58b	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	681542	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Docket No.: 10037P007CC2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of:

YANNIS TSIVIDIS

Application No.: 15/080,432

Filed: March 24, 2016

For: **Power Dissipation Reduction in Wireless Transceivers**

Art Group: 2647

Examiner: Vuong, Quochien B

PETITION FOR EXTENSION OF TIME PURSUANT TO 37 C.F.R. § 1.136(a)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with 37 C.F. R. §1.136(a), Applicant for the above-identified application respectfully Petitions the Commissioner for a three (3) month extension of time, extending the period for response to May 01, 2017, from the Office Action dated November 01, 2016. An Amendment is/are attached. You are hereby authorized to charge our Deposit Account No. 02-2666 the amount of $700.00 (petition filing fee).

If it should be determined that a longer extension of time is required to prevent this application from being abandoned, please charge any additional fees to Deposit Account No. 02-2666.

Respectfully submitted,

Blakely, Sokoloff, Taylor & Zafman LLP

Date: April 27, 2017

Roger W. Blakely, Jr., Reg. No. 25831

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CERTIFICATE OF MAILING/TRANSMISSION

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.

Jessica A. Clark *04-27-17*

Jessica A. Clark *Date*

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 15/080,432	Filing Date 03/24/2016	☐ To be Mailed

ENTITY: ☐ LARGE ☒ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT **04/20/2016**

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 18	Minus	** 20	= 0	X $40 =	0
Independent (37 CFR 1.16(h))	* 6	Minus	***5	= 1	X $210 =	210
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	**210**

AMENDMENT **04/27/2017**

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 18	Minus	** 20	= 0	X $40 =	0
Independent (37 CFR 1.16(h))	* 6	Minus	*** 6	= 0	X $210 =	0
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	**0**

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
PAUL STANBACK

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application. No.	:	15/080,432	Confirmation No. 6094
Inventor(s)	:	Yannis Tsividis	
Filed	:	03/24/2016	
TC/A.U.	:	2647	
Examiner	:	Vuong, Quochien B	
Docket No.	:	10037P007CC2	
Customer No.	:	8791	

Mail Stop Amendment
Commissioner for Patents
PO Box 1450
Alexandria VA 22313-1450

SUPPLEMENTAL AMENDMENT AND RESPONSE

Sir:

In further response to the Office Action of November 1, 2016, and after entry of the Amendment filed April 27, 2017, please further amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 9 of this paper.

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Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A method of power dissipation control in a receiver circuit within a battery powered mobile device when the receiver circuit is receiving and processing an RF input signal in a receiver signal path that includes a desired signal and an interferer signal, the method comprising:

determining a strength of the desired signal with respect to the strength of the interferer signal;

causing a decrease in power dissipation of a receiver signal path within the receiver circuit and a resultant decreased battery drain, by dynamically adjusting ~~both~~ one or more of, a bias current of a component in ~~a~~ the receiver signal path of the receiver circuit, ~~and~~ an impedance of a component in the receiver signal path of the receiver circuit, or a gain of a component in the receiver signal path, based on the strength of the desired signal relative to the strength of the interferer signal, upon determination that the strength of the desired signal has increased relative to the strength of the interferer signal;

causing an increase in power dissipation of the receiver signal path within the receiver circuit and a resultant increased battery drain, by dynamically adjusting ~~both~~ one or more of, the bias current of the component in the receiver signal path of the receiver circuit, the gain of the component in the receiver signal path ~~and~~ or the impedance of the component in the receiver signal path of the receiver circuit, based on the strength of the desired signal relative to the strength of the interferer signal, upon determination that the strength of the desired signal has decreased relative to the strength of the interferer signal.

2. (currently amended) The method of claim 1, wherein the bias current of the component in the receiver circuit is dynamically adjusted by one or both of, a changing of the

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value of an impedance across a voltage, a changing of the base voltage of a device whose emitter is connected to ground through a resistor, thereby optimizing the power drain from the battery.

3. (currently amended) A method of power dissipation control in a receiver circuit within a battery powered mobile device when the receiver circuit is receiving an RF input signal in a receiver signal path that includes a desired signal and an interferer signal, the method comprising:

determining a strength of the desired signal with respect to the interferer signal, wherein the receiver circuit comprises a defined receiver signal path between the RF input signal and a processed signal output;

causing a decrease in power dissipation of the defined receiver signal path within the receiver circuit and a resultant decreased battery drain, by dynamically ~~changing~~ adjusting an impedance of a component in the receiver signal path of the receiver circuit upon determination that the strength of the desired signal has increased relative to the strength of the interferer signal; and

causing an increase in power dissipation of the defined receiver signal path within the receiver circuit and a resultant increased battery drain, by dynamically ~~changing~~ adjusting the impedance of the component in the receiver signal path of the receiver circuit upon determination that the strength of the desired signal has decreased relative to the strength of the interferer signal;

~~wherein the dynamically changing of impedance includes:~~

~~setting the impedance of the component in the receiver circuit in between a high level and a low level;~~

~~dynamically adjusting the impedance of the component in the receiver circuit up or down; and~~

wherein the dynamically ~~changing~~ adjusting of the impedance occurs while the receiver circuit is processing signals received from the RF input.

4. (currently amended) The method of claim 3 wherein dynamically ~~changing~~ adjusting the impedance of a component in the receiver circuit comprises ~~continuously~~ dynamically adjusting an impedance of a low noise amplifier (LNA) in the receiver signal path.

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5. (currently amended) The method of claim 3 wherein dynamically ~~changing~~ adjusting the impedance of a component in the receiver circuit comprises ~~continuously~~ dynamically adjusting an impedance of a mixer in the receiver signal path.

6. (currently amended) The method of claim 3 wherein dynamically ~~changing~~ adjusting the impedance of a component in the receiver circuit comprises ~~continuously~~ dynamically adjusting an impedance of a filter in the receiver signal path.

7. (previously presented) The method of claim 3, wherein the impedance of a component in the receiver circuit comprises a resistance, and wherein a value of the resistance is adjusted by opening switches across one or more portions of the resistance.

8. (currently amended) The method of claim 3, wherein the defined receiver signal path includes components that comprise: a low noise amplifier (LNA), a filter, a mixer.

9. (original) The method of claim 8 wherein the component is a low noise amplifier.

10. (original) The method of claim 8 wherein the component is a filter.

11. (original) The method of claim 8 wherein the component is a mixer.

12. (currently amended) A method of power dissipation control in a receiver circuit within a battery powered mobile device when the receiver circuit is receiving an RF input signal in a receiver signal path that includes a desired signal and an interferer signal, the method comprising:

determining a strength of the interferer signal present in the received RF input signal;

causing a decrease in power dissipation of ~~a~~ the receiver signal path within the receiver circuit and a resultant decreased battery drain, by dynamically changing an impedance of a component in the receiver signal path of the receiver circuit upon determination that the strength of the interferer signal has decreased;

causing ~~a~~ an increase in power dissipation of the receiver signal path within the receiver circuit and the resultant decreased battery drain, by dynamically changing the impedance of the

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component in the receiver signal path of the receiver circuit upon determination that the strength of the interferer signal has increased;

wherein dynamically changing the impedance includes:

dynamically adjusting ~~scaling~~ the impedance of the component in the receiver signal path of the receiver circuit through a plurality of levels~~,~~ between a high level and a low level from ~~at least~~ an ~~intermediate~~ initial point, responsive to the strength of the interferer signal present in the received RF input signal, wherein the high and low levels represent a maximum power saving and a maximum power dissipation; and

wherein the dynamically ~~changing~~ adjusting the impedance ~~variable~~ occurs while the receiver circuit is processing signals received from the RF input signal.

13. (original) The method of claim 12, wherein the impedance of the component in the receiver circuit comprises a resistance, and wherein the value of the resistance may be increased by opening switches across one or more portions of the resistance.

14. (currently amended) A method of controlling power dissipation in a receiver circuit within a battery powered mobile device when the receiver circuit is receiving and processing an RF input signal in a receiver signal path of the receiver circuit that includes a desired signal and an interferer signal, the method comprising:

determining a strength of the interferer signal present in the received RF input signal;

causing a decrease in power dissipation of the receiver signal path of the receiver circuit resulting in a decrease in drain on battery life, by dynamically ~~varying~~ adjusting one or more of a bias, a gain ~~of a gain stage~~or an impedance in the receiver signal path of the receiver circuit ~~and dynamically changing an impedance of a component in the signal path of the receiver circuit,~~ upon determination that the strength of the interferer signal has decreased; or

alternately causing an increase in power dissipation of the receiver signal path of the receiver circuit resulting in an increase in drain on battery life, by dynamically adjusting ~~the gain of the gain stage in the signal path of the receiver circuit and dynamically changing~~ one or more of the bias, the gain or the~~an~~ impedance of a component in the receiver signal path of the receiver circuit, upon determination that the strength of the interferer signal has increased;

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~~causing an increase in power dissipation of the signal path of the receiver circuit resulting in an increase in drain on battery life, by dynamically adjusting the gain of the gain stage in the signal path of the receiver circuit and dynamically changing an impedance of a component in the signal path of the receiver circuit, upon determination that the strength of the interferer signal has increased;~~

~~wherein the dynamically adjusting the gain includes:~~

~~setting the gain of the component in the signal path of the receiver circuit in between a high level and a low level; and~~

~~varying the gain of the gain stage in the signal path of the receiver circuit up or down; and~~

~~wherein the dynamically changing the impedance includes:~~

~~setting the impedance of the component in the receiver circuit in between a high level and a low level;~~

~~continuously adjusting the impedance of the component in the signal path of the receiver circuit up or down;~~

thereby optimizing the power dissipation of the battery powered mobile device.

15. (currently amended) The method of claim 14, wherein the gain of the component in the receiver signal path of the receiver circuit is varied by increasing a current in a differential pair and /or increasing a load resistance using switches.

16. (currently amended) A mobile communications device, comprising:

a receiver circuit for receiving an RF input signal that includes a desired signal and an interferer signal;

a battery that powers the mobile communications device including the receiver circuit;

wherein a strength of the desired signal is determined with respect to the strength of the interferer signal;

wherein a decrease in power dissipation of a receiver signal path within the receiver circuit and a resultant decreased battery drain is caused by dynamically ~~changing~~ adjusting an impedance of a component in a receiver signal path of the receiver circuit upon determination

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that the strength of the desired signal has increased relative to the strength of the interferer signal; and

wherein an increase in power dissipation of the receiver signal path within the receiver circuit and a resultant increased battery drain, is caused by dynamically ~~changing~~ adjusting the impedance of the component in the receiver signal path of the receiver circuit upon determination that the strength of the desired signal has decreased relative to the strength of the interferer signal; and

~~wherein the dynamically changing an impedance includes:~~

~~setting the impedance of the component in the receiver circuit in between a high level and a low level; and~~

~~adjusting the impedance of the component in the receiver circuit up or down; and~~

wherein the dynamically changing the impedance occurs while the receiver circuit is processing signals received from the RF input signal.

17. (previously presented) The mobile communication device of claim 16, wherein the impedance of the component in the receiver circuit comprises a resistance, and wherein a value of the resistance may be varied by opening and closing switches across one or more portions of the resistance responsive to the determined strength of the desired signal with respect to the interferer signal.

18. (currently amended) A method for conserving battery power in a mobile communication device, the method comprising:

receiving a radio signal by a radio receiver, of a wireless transceiver, that ~~include~~ includes a desired signal and an interferer signal;

powering to the wireless transceiver by a battery;

processing of the received radio signals in a receiver signal path within the radio receiver;

determining the strength of the interferer signal by a circuit coupled to the receiver signal path ~~of the receiver~~;

dynamically changing one or more of an impedance of the receiver signal path of the receiver, or a gain of ~~a~~ an amplifier gain stage in ~~and dynamically changing an impedance of~~ the

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receiver signal path ~~of the receiver~~ both responsive to the determined strength of the interferer signal;

wherein adjusting the gain of the gain stage and impedance of the receiver signal path result in improving a power drain from the battery.

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REMARKS/ARGUMENTS

Submitted herewith is a copy of the Report on the Filing or Determination of an Action Regarding a Patent or Trademark, which the undersigned mailed to the Director of the U.S. Patent and Trademark Office on June 12, 2017. As the undersigned mentioned to the examiner in a phone call on June 9, 2107, a Markman Hearing has occurred and a Memorandum and Order on Claim Construction setting forth the court ordered construction of various terms in the claims of the patents in suit has been issued.

The purpose of this amendment is to eliminate from the present claims, terms which were not construed by the court, and to replace those terms with terms which were construed by the court. For that purpose, the disputed terms used in the present claims as a result of this amendment, the plaintiff's proposed construction of those terms (plaintiff is also the assignee of the present application) and the court ordered construction of the relevant terms is set forth in the table below. If requested by the examiner, the undersigned will provide a complete copy of the 41 page Memorandum and Order on Claim Construction.

Disputed Term	**Plaintiff's Proposed Construction**	**Court Ordered Construction**
dynamically adjust[ed]	Plain and ordinary meaning. Alternatively, "changing during operation"	"adjust[ed] during operation without reliance upon a signal strength threshold"
impedance	Plain and ordinary meaning. Alternatively, "a value of electrical resistance, electrical reactance, or both"	"opposition to the flow of alternating current"
a component in the receiver signal path	Plain and ordinary meaning. Alternatively, "an active or passive electronic device or circuit element in the receiver signal path"	plain meaning

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interferer signal	Plain and ordinary meaning. Alternatively, "a signal that interferes with the receipt of the received desired signal"	"a signal generated outside the transceiver that interferes with the receipt of the received desired signal"
at least a component in the receiver path	Plain and ordinary meaning. Alternatively, "an active or passive electronic device or circuit element in the receiver signal path"	"at least a component in the receiver"

By way of this amendment, the phrase "continuously adjusting" previously appearing in claims 4-6 and 14 has been changed to "dynamically adjusting", for the reason that neither the word "continuously" nor the phrase "continuously adjusting" was subject to a court order construction, whereas the disputed term "dynamically adjust" or "dynamically adjusted" was construed, as "adjusting during operation without reliance upon a signal strength threshold". Similarly, in claim 12, while "scaling . . . impedance" was subject to the court order construction, the entire phrase "dynamically scaling" was not. Accordingly, by way of this amendment, the phrase "dynamically scaling" has been changed to "dynamically adjusting", as "dynamically adjust" or "dynamically adjusted" was subject to the Court Ordered Construction, as the above table in the case. Also the phrase "dynamically changing" has similarly been changed to "dynamically adjusted", as "dynamically changing" was not construed while "dynamically adjusted" was construed, and further in the interest of consistency of terminology. Further, references to the setting of initial values, etc. have been deleted, as initial values are incidental to the invention itself, and other minor changes have also been made

Finally, the word "variable" has been removed from claim 12, not for the purpose of changing the content of the claim itself, but rather for the reason that the word "variable" was not grammatically correct, and appeared out of place in the claim.Accordingly, with the amendments made herein, it is believed that the clarity of the claims has been enhanced and that all claims in the application are now in condition for allowance.

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CONCLUSION

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 06/27/2017

By _____
Roger W. Blakely, Jr.
Reg. No. 25,831
Tel.: (714) 557-3800 (Pacific Coast)

1279 Oakmead Parkway
Sunnyvale, California 94085

CERTIFICATE OF TRANSMISSION (37 CFR 1.8A)

I hereby certify that this correspondence is being EFS Web transmitted to the USPTO on the date shown below.

Date: 06/27/2017

Jessica A Clark 6/27/2017
Jessica A. Clark *Date*

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application. No.	:	15/080,432	Confirmation No. 6094
Applicant	:	Yannis Tsividis	
Filed	:	03/24/2016	
TC/A.U.	:	2647	
Examiner	:	Vuong, Quochien B	
Docket No.	:	10037P007CC2	
Customer No.	:	8791	

Commissioner for Patents
PO Box 1450
Alexandria VA 22313-1450

AUTHORIZATION FOR EXTENSION OF TIME, ALL REPLIES

Sir:

Authorization is given to treat any concurrent or future reply requiring a petition for an extension of time under 37 CFR §1.136(a) for its timely submission, as incorporating a petition for extension of time for the appropriate length of time. If any other petition is necessary for consideration of this paper, it is hereby so petitioned. Please charge any shortage in fees in connection with the filing of this paper, including extension of time fees, to Deposit Account 02-2666 and please credit any excess fees to such deposit account.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 06/27/2017

By _____
Roger W. Blakely, Jr.
Reg. No. 25,831
Tel.: (714) 557-3800 (Pacific Coast)

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Date: 06/27/2017

Jessica A Clark 6/27/2017
Jessica A. Clark *Date*

IPR2024-00817
Apple EX1002 Page 286

AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court for the Eastern District of Texas, Marshall Division on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
2:16-CV-527	5/18/2016	for the Eastern District of Texas, Marshall Division

PLAINTIFF	DEFENDANT
THETA IP, LLC	SAMSUNG ELECTRONICS CO., LTD., and SAMSUNG ELECTRONICS AMERICA, INC.

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	7,010,330	3/7/2006	THETA IP, LLC
2	9,331,728	5/3/2016	THETA IP, LLC
3			
4			
5			

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director **Copy 3—Upon termination of action, mail this copy to Director**
Copy 2—Upon filing document adding patent(s), mail this copy to Director **Copy 4—Case file copy**

Electronic Acknowledgement Receipt

EFS ID:	29626951
Application Number:	15080432
International Application Number:	
Confirmation Number:	6094
Title of Invention:	Power Dissipation Reduction in Wireless Transceivers
First Named Inventor/Applicant Name:	Yannis Tsividis
Customer Number:	8791
Filer:	Roger W. Blakely/Jessica Clark
Filer Authorized By:	Roger W. Blakely
Attorney Docket Number:	10037P007CC2
Receipt Date:	27-JUN-2017
Filing Date:	24-MAR-2016
Time Stamp:	19:02:41
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		10037P007CC2_20170627_SuppAmd.pdf	469579 abc1c064af733eb958fdce6593ff2db913b11cce	yes	13

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Supplemental Response or Supplemental Amendment	1	1
	Claims	2	8
	Applicant Arguments/Remarks Made in an Amendment	9	11
	Authorization for Extension of Time all replies	12	12
	Miscellaneous Incoming Letter	13	13
Warnings:			
Information:			
	Total Files Size (in bytes):	469579	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 15/080,432	Filing Date 03/24/2016	☐ To be Mailed

ENTITY: ☐ LARGE ☒ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT **06/27/2017**

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 18	Minus	** 20	= 0	X $40 =	0
Independent (37 CFR 1.16(h))	* 6	Minus	***6	= 0	X $210 =	0
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	0

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
BRENDA HARRISON

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/080,432	03/24/2016	Yannis Tsividis	10037P007CC2	6094

8791 7590 09/06/2017

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
1279 Oakmead Parkway
Sunnyvale, CA 94085-4040

EXAMINER
VUONG, QUOCHIEN B

ART UNIT	PAPER NUMBER
2647	

MAIL DATE	DELIVERY MODE
09/06/2017	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 15/080,432	Applicant(s) TSIVIDIS, YANNIS	
	Examiner QUOCHIEN B. VUONG	Art Unit 2647	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06/27/2017*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-18* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-18* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

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Apple EX1002 Page 292

DETAILED ACTION

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 12/29/2016 and 01/31/2017 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

The present application is being examined under the pre-AIA first to invent provisions.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of pre-AIA 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 14 and 18 are rejected under pre-AIA 35 U.S.C. 102(b) as being anticipated by Clark (US 5,001,776).

Regarding claim 1, Clark (figure 1) discloses a method of power dissipation control in a receiver circuit within a battery powered mobile device when the receiver circuit is receiving and processing an RF input signal in a receiver signal path that includes a desired signal and an interferer signal, the method comprising: determining a strength of the desired signal with respect to the strength of the interferer signal; causing a decrease in power dissipation of a receiver signal path within the receiver circuit and a resultant decreased battery drain, by dynamically adjusting one or more of,

a bias current of a component in the receiver signal path of the receiver circuit, an impedance of a component in the receiver signal path of the receiver circuit, or a gain of a component in the receiver signal path, based on the strength of the desired signal relative to the strength of the interferer signal, upon determination that the strength of the desired signal has increased relative to the strength of the interferer signal; causing an increase in power dissipation of the receiver signal path within the receiver circuit and a resultant increased battery drain, by dynamically adjusting one or more of, the bias current of the component in the receiver signal path of the receiver circuit, the gain of the component in the receiver signal path or the impedance of the component in the receiver signal path of the receiver circuit, based on the strength of the desired signal relative to the strength of the interferer signal, upon determination that the strength of the desired signal has decreased relative to the strength of the interferer signal (column 2, line 34 – column 4, line 66).

Regarding claim 14, Clark (figure 1) discloses a method of controlling power dissipation in a receiver circuit within a battery powered mobile device when the receiver circuit is receiving and processing an RF input signal in a receiver signal path of the receiver circuit that includes a desired signal and an interferer signal, the method comprising: determining a strength of the interferer signal present in the received RF input signal; causing a decrease in power dissipation of the receiver signal path of the receiver circuit resulting in a decrease in drain on battery life, by dynamically adjusting one or more of a bias, a gain or an impedance in the receiver signal path of the receiver circuit, upon determination that the strength of the interferer signal has decreased; or

alternately causing an increase in power dissipation of the receiver signal path of the receiver circuit resulting in an increase in drain on battery life, by dynamically adjusting one or more of the bias, the gain or the impedance of a component in the receiver signal path of the receiver circuit, upon determination that the strength of the interferer signal has increased; thereby optimizing the power dissipation of the battery powered mobile device (column 2, line 34 – column 4, line 66).

Regarding claim 18, Clark (figure 1) discloses a method for conserving battery power in a mobile communication device, the method comprising: receiving a radio signal by a radio receiver, of a wireless transceiver, that include includes a desired signal and an interferer signal; powering to the wireless transceiver by a battery; processing of the received radio signals in a receiver signal path within the radio receiver; determining the strength of the interferer signal by a circuit coupled to the receiver signal path dynamically changing one or more of an impedance of the receiver signal path of the receiver, or a gain of an amplifier gain stage in the receiver signal path both responsive to the determined strength of the interferer signal; wherein adjusting the gain of the gain stage and impedance of the receiver signal path result in improving a power drain from the battery (column 2, line 34 – column 4, line 66).

Claim Rejections - 35 USC § 103

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the

> time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-13 and 15-17 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Clark in view of Leifso et al. (US 6,870,425).

Regarding claim 2, Clark discloses the method of claim 1 above. Clark does not specifically disclose wherein the bias current of the component in the receiver circuit is dynamically adjusted by one or both of, a changing of the value of an impedance across a voltage, a changing of the base voltage of a device whose emitter is connected to ground through a resistor, thereby optimizing the power drain from the battery. However, Leifso et al. (figure 4) disclose varying a gain of an amplifier by variably a bias current of the component in the receiver circuit is dynamically adjusted by one or both of, a changing of the value of an impedance across a voltage, a changing of the base voltage of a device whose emitter is connected to ground through a resistor (column 6, line 26 – column 8, line 15). Therefore, it would have been obvious for one having ordinary skill in the art at the time the invention was made to adapt the teaching of dynamic adjusting the gain of the amplifier by dynamically adjusting the current bias of Leifso et al. to the method of Clark as a system design preference for performing the same function as controlling and adjusting the gain of the amplifier in the receiver.

Regarding claim 3, Clark (figure 1) discloses a method of power dissipation control in a receiver circuit within a battery powered mobile device when the receiver circuit is receiving an RF input signal in a receiver signal path that includes a desired signal and an interferer signal, the method comprising: determining a strength of the desired signal with respect to the interferer signal, wherein the receiver circuit

comprises a defined receiver signal path between the RF input signal and a processed signal output; causing a decrease in power dissipation of the defined receiver signal path within the receiver circuit and a resultant decreased battery drain, by dynamically adjusting a gain of a component in the receiver signal path of the receiver circuit upon determination that the strength of the desired signal has increased relative to the strength of the interferer signal; and causing an increase in power dissipation of the defined receiver signal path within the receiver circuit and a resultant increased battery drain, by dynamically adjusting the gain of the component in the receiver signal path of the receiver circuit upon determination that the strength of the desired signal has decreased relative to the strength of the interferer signal; wherein the dynamically adjusting of the gain occurs while the receiver circuit is processing signals received from the RF input (column 2, line 34 - column 4, line 66). Clark does not specifically disclose dynamically adjusting an impedance of a component in the receiver signal path of the receiver circuit upon determination that the strength of the desired signal has increased relative to the strength of the interferer signal; and causing an increase in power dissipation of the defined receiver signal path within the receiver circuit and a resultant increased battery drain, by dynamically adjusting the impedance of the component in the receiver signal path of the receiver circuit upon determination that the strength of the desired signal has decreased relative to the strength of the interferer signal; wherein the dynamically adjusting of the impedance occurs while the receiver circuit is processing signals received from the RF input. However, Leifso et al. (figure 4) disclose adjusting a gain of an amplifier by adjusting an impedance (column 6, line 26 – column 8, line 15;

and claim 17). Therefore, it would have been obvious for one having ordinary skill in the art at the time the invention was made to adapt the teaching of adjusting the gain of the amplifier by adjusting the impedance of Leifso et al. to the method of Clark as a system design preference for performing the same function as controlling and adjusting the gain of the amplifier in the receiver.

Regarding claim 4, Leifso et al. disclose wherein dynamically adjusting the impedance of a component in the receiver circuit comprises dynamically adjusting an impedance of an amplifier (column 6, line 26 – column 8, line 15 and claim 17). And Clark discloses dynamically adjusting a low noise amplifier (LNA) in the receiver signal path (figure 1, amplifier 108).

Regarding claim 5, Clark and Leifso et al. disclose wherein dynamically adjusting the impedance of a component in the receiver circuit. Clark also discloses dynamically adjusting a mixer in the receiver signal path (figure 1, mixer 110).

Regarding claim 6, Clark and Leifso et al. disclose wherein dynamically adjusting the impedance of a component in the receiver circuit. Clark also discloses dynamically adjusting a filter in the receiver signal path (figure 1, mixer 120).

Regarding claim 7, Leifso et al. disclose wherein the impedance of a component in the receiver circuit comprises a resistance, and wherein a value of the resistance is adjusted by opening switches across one or more portions of the resistance (column 6, line 26 – column 8, line 15 and claim 17).

Regarding claim 8, Clark (figure 1) discloses wherein the defined receiver signal path includes components that comprise: a low noise amplifier (LNA) (108), a filter (120), a mixer (110).

Regarding claim 9, Clark disclose wherein the component is a low noise amplifier (108),

Regarding claim 10, Clark disclose wherein the component is a filter (120).

Regarding claim 11, Clark disclose wherein the component is a mixer (110).

Regarding claim 12, Clark (figure 1) a method of power dissipation control in a receiver circuit within a battery powered mobile device when the receiver circuit is receiving an RF input signal in a receiver signal path that includes a desired signal and an interferer signal, the method comprising: determining a strength of the interferer signal present in the received RF input signal; causing a decrease in power dissipation of the receiver signal path within the receiver circuit and a resultant decreased battery drain, by dynamically changing a gain of a component in the receiver signal path of the receiver circuit upon determination that the strength of the interferer signal has decreased; causing an increase in power dissipation of the receiver signal path within the receiver circuit and the resultant decreased battery drain, by dynamically changing the gain of the component in the receiver signal path of the receiver circuit upon determination that the strength of the interferer signal has increased; wherein dynamically changing the gain includes: dynamically adjusting the gain of the component in the receiver signal path of the receiver circuit through a plurality of levels; between a high level and a low level from an initial point, responsive to the strength of

the interferer signal present in the received RF input signal, wherein the high and low levels represent a maximum power saving and a maximum power dissipation; and wherein the dynamically adjusting the gain occurs while the receiver circuit is processing signals received from the RF input signal (column 2, line 34 - column 4, line 66). Clark does not specifically disclose dynamically changing an impedance of a component in the receiver signal path of the receiver circuit upon determination that the strength of the interferer signal has decreased; causing an increase in power dissipation of the receiver signal path within the receiver circuit and the resultant decreased battery drain, by dynamically changing the impedance of the component in the receiver signal path of the receiver circuit upon determination that the strength of the interferer signal has increased; wherein dynamically changing the impedance includes: dynamically adjusting the impedance of the component in the receiver signal path of the receiver circuit through a plurality of levels; between a high level and a low level from an initial point, responsive to the strength of the interferer signal present in the received RF input signal, wherein the high and low levels represent a maximum power saving and a maximum power dissipation; and wherein the dynamically adjusting the impedance occurs while the receiver circuit is processing signals received from the RF input signal. However, Leifso et al. (figure 4) disclose dynamically adjusting a gain of an amplifier by dynamically adjusting an impedance of a component in the receiver (column 6, line 26 – column 8, line 15; and claim 17). Therefore, it would have been obvious for one having ordinary skill in the art at the time the invention was made to adapt the teaching of adjusting the gain of the amplifier by adjusting the impedance of Leifso et al. to the

method of Clark as a system design preference for performing the same function as controlling and adjusting the gain of the amplifier in the receiver.

Regarding claim 13, Leifso et al. disclose wherein the impedance of the component in the receiver circuit comprises a resistance, and wherein the value of the resistance may be increased by opening switches across one or more portions of the resistance (column 6, line 26 – column 8, line 15; and claim 17).

Regarding claim 15, Clark discloses the method of claim 14 above. Clark does not disclose wherein the gain of the component in the receiver signal path of the receiver circuit is varied by increasing a current in a differential pair and /or increasing a load resistance using switches. However, Leifso et al. disclose changing the gain by changing a current and/or changing a load resistance (column 6, line 26 – column 8, line 15; and claim 17). Therefore, it would have been obvious for one having ordinary skill in the art at the time the invention was made to adapt the teaching of varying the gain of the amplifier by varying the current in a differential pair and /or increasing a load resistance of Leifso et al. to the method of Clark as a system design preference for performing the same function as controlling and adjusting the gain of the amplifier in the receiver.

Regarding claim 16, Clark (figure 1) discloses a mobile communications device, comprising: a receiver circuit for receiving an RF input signal that includes a desired signal and an interferer signal; a battery that powers the mobile communications device including the receiver circuit; wherein a strength of the desired signal is determined with respect to the strength of the interferer signal; wherein a decrease in power dissipation

of a receiver signal path within the receiver circuit and a resultant decreased battery drain is caused by dynamically adjusting a gain of a component in a receiver signal path of the receiver circuit upon determination that the strength of the desired signal has increased relative to the strength of the interferer signal; and wherein an increase in power dissipation of the receiver signal path within the receiver circuit and a resultant increased battery drain, is caused by dynamically adjusting the gain of the component in the receiver signal path of the receiver circuit upon determination that the strength of the desired signal has decreased relative to the strength of the interferer signal; and wherein the dynamically changing the gain occurs while the receiver circuit is processing signals received from the RF input signal (column 2, line 34 - column 4, line 66). Clark does not specifically disclose dynamically adjusting an impedance of a component in a receiver signal path of the receiver circuit upon determination that the strength of the desired signal has increased relative to the strength of the interferer signal; and wherein an increase in power dissipation of the receiver signal path within the receiver circuit and a resultant increased battery drain, is caused by dynamically adjusting the impedance of the component in the receiver signal path of the receiver circuit upon determination that the strength of the desired signal has decreased relative to the strength of the interferer signal; and wherein the dynamically changing the impedance occurs while the receiver circuit is processing signals received from the RF input signal. However, Leifso et al. (figure 4) disclose adjusting a gain of an amplifier by adjusting an impedance resistance (column 6, line 26 – column 8, line 15; and claim 17). Therefore, it would have been obvious for one having ordinary skill in the art at the

time the invention was made to adapt the teaching of adjusting the gain of the amplifier by adjusting the impedance of Leifso et al. to the method of Clark as a system design preference for performing the same function as controlling and adjusting the gain of the amplifier in the receiver.

Regarding claim 17, Leifso et al. disclose wherein the impedance of the component in the receiver circuit comprises a resistance, and wherein a value of the resistance may be varied by opening and closing switches across one or more portions of the resistance responsive to the determined strength of the desired signal with respect to the interferer signal (column 6, line 26 – column 8, line 15; and claim 17).

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*,

686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on nonstatutory double patenting provided the reference application or patent either is shown to be commonly owned with the examined application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. See MPEP § 717.02 for applications subject to examination under the first inventor to file provisions of the AIA as explained in MPEP § 2159. See MPEP §§ 706.02(l)(1) - 706.02(l)(3) for applications not subject to examination under the first inventor to file provisions of the AIA. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO Internet website contains terminal disclaimer forms which may be used. Please visit www.uspto.gov/patent/patents-forms. The filing date of the application in which the form is filed determines what form (e.g., PTO/SB/25, PTO/SB/26, PTO/AIA/25, or PTO/AIA/26) should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.

Claims 1-18 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-16 of U.S. Patent No. 7,010,330. Although the claims at

issue are not identical, they are not patentably distinct from each other because both are drawn to the same invention of a method of controlling a battery power consumption of a transceiver.

Regarding claims 1 and 2 of the pending application, claims 1 and 6 of U.S. Patent No. 7,010,330 encompass all the claimed limitation including a method of power dissipation control in a receiver circuit within a battery powered mobile device when the receiver circuit is receiving and processing an RF input signal in a receiver signal path that includes a desired signal and an interferer signal, the method comprising: determining a strength of the desired signal with respect to the strength of the interferer signal; causing a decrease in power dissipation of a receiver signal path within the receiver circuit and a resultant decreased battery drain, by dynamically adjusting one or more of, a bias current of a component in the receiver signal path of the receiver circuit, an impedance of a component in the receiver signal path of the receiver circuit, or a gain of a component in the receiver signal path, based on the strength of the desired signal relative to the strength of the interferer signal, upon determination that the strength of the desired signal has increased relative to the strength of the interferer signal; causing an increase in power dissipation of the receiver signal path within the receiver circuit and a resultant increased battery drain, by dynamically adjusting one or more of, the bias current of the component in the receiver signal path of the receiver circuit, the gain of the component in the receiver signal path or the impedance of the component in the receiver signal path of the receiver circuit, based on the strength of the desired signal relative to the strength of the interferer signal, upon determination

that the strength of the desired signal has decreased relative to the strength of the interferer signal; wherein the bias current of the component in the receiver circuit is dynamically adjusted by one or both of, a changing of the value of an impedance across a voltage, a changing of the base voltage of a device whose emitter is connected to ground through a resistor, thereby optimizing the power drain from the battery.

Regarding claims 3-11 of the pending application, claims 1-16 of U.S. Patent No. 7,010,330 encompass all the claimed limitation including a method of power dissipation control in a receiver circuit within a battery powered mobile device when the receiver circuit is receiving an RF input signal in a receiver signal path that includes a desired signal and an interferer signal, the method comprising: determining a strength of the desired signal with respect to the interferer signal, wherein the receiver circuit comprises a defined receiver signal path between the RF input signal and a processed signal output; causing a decrease in power dissipation of the defined receiver signal path within the receiver circuit and a resultant decreased battery drain, by dynamically adjusting an impedance of a component in the receiver signal path of the receiver circuit upon determination that the strength of the desired signal has increased relative to the strength of the interferer signal; and causing an increase in power dissipation of the defined receiver signal path within the receiver circuit and a resultant increased battery drain, by dynamically adjusting the impedance of the component in the receiver signal path of the receiver circuit upon determination that the strength of the desired signal has decreased relative to the strength of the interferer signal; wherein the dynamically adjusting of the impedance occurs while the receiver circuit is processing signals

received from the RF input; wherein dynamically adjusting the impedance of a component in the receiver circuit comprises dynamically adjusting an impedance of a low noise amplifier (LNA) in the receiver signal path; wherein dynamically adjusting the impedance of a component in the receiver circuit comprises dynamically adjusting an impedance of a mixer in the receiver signal path; wherein dynamically adjusting the impedance of a component in the receiver circuit comprises dynamically adjusting an impedance of a filter in the receiver signal path; wherein the impedance of a component in the receiver circuit comprises a resistance, and wherein a value of the resistance is adjusted by opening switches across one or more portions of the resistance; wherein the defined receiver signal path includes components that comprise: a low noise amplifier (LNA), a filter, a mixer.

Regarding claims 12 and 13 of the pending application, claims 1 and 6 of U.S. Patent No. 7,010,330 encompass all the claimed limitation including a method of power dissipation control in a receiver circuit within a battery powered mobile device when the receiver circuit is receiving an RF input signal in a receiver signal path that includes a desired signal and an interferer signal, the method comprising: determining a strength of the interferer signal present in the received RF input signal; causing a decrease in power dissipation of the receiver signal path within the receiver circuit and a resultant decreased battery drain, by dynamically changing an impedance of a component in the receiver signal path of the receiver circuit upon determination that the strength of the interferer signal has decreased; causing an increase in power dissipation of the receiver signal path within the receiver circuit and the resultant decreased battery drain, by

dynamically changing the impedance of the component in the receiver signal path of the receiver circuit upon determination that the strength of the interferer signal has increased; wherein dynamically changing the impedance includes: dynamically adjusting the impedance of the component in the receiver signal path of the receiver circuit through a plurality of levels; between a high level and a low level from an initial point, responsive to the strength of the interferer signal present in the received RF input signal, wherein the high and low levels represent a maximum power saving and a maximum power dissipation; and wherein the dynamically adjusting the impedance occurs while the receiver circuit is processing signals received from the RF input signal; wherein the impedance of the component in the receiver circuit comprises a resistance, and wherein the value of the resistance may be increased by opening switches across one or more portions of the resistance.

Regarding claims 14 and 15 of the pending application, claims 1 and 6 of U.S. Patent No. 7,010,330 encompass all the claimed limitation including a method of controlling power dissipation in a receiver circuit within a battery powered mobile device when the receiver circuit is receiving and processing an RF input signal in a receiver signal path of the receiver circuit that includes a desired signal and an interferer signal, the method comprising: determining a strength of the interferer signal present in the received RF input signal; causing a decrease in power dissipation of the receiver signal path of the receiver circuit resulting in a decrease in drain on battery life, by dynamically adjusting one or more of a bias, a gain or an impedance in the receiver signal path of the receiver circuit, upon determination that the strength of the interferer signal has

decreased; or alternately causing an increase in power dissipation of the receiver signal path of the receiver circuit resulting in an increase in drain on battery life, by dynamically adjusting one or more of the bias, the gain or the impedance of a component in the receiver signal path of the receiver circuit, upon determination that the strength of the interferer signal has increased; thereby optimizing the power dissipation of the battery powered mobile device; wherein the gain of the component in the receiver signal path of the receiver circuit is varied by increasing a current in a differential pair and /or increasing a load resistance using switches.

Regarding claims 16 and 17 of the pending application, claims 1 and 6 of U.S. Patent No. 7,010,330 encompass all the claimed limitation including a mobile communications device, comprising: a receiver circuit for receiving an RF input signal that includes a desired signal and an interferer signal; a battery that powers the mobile communications device including the receiver circuit; wherein a strength of the desired signal is determined with respect to the strength of the interferer signal; wherein a decrease in power dissipation of a receiver signal path within the receiver circuit and a resultant decreased battery drain is caused by dynamically adjusting an impedance of a component in a receiver signal path of the receiver circuit upon determination that the strength of the desired signal has increased relative to the strength of the interferer signal; and wherein an increase in power dissipation of the receiver signal path within the receiver circuit and a resultant increased battery drain, is caused by dynamically adjusting the impedance of the component in the receiver signal path of the receiver circuit upon determination that the strength of the desired signal has decreased relative

to the strength of the interferer signal; and wherein the dynamically changing the impedance occurs while the receiver circuit is processing signals received from the RF input signal; wherein the impedance of the component in the receiver circuit comprises a resistance, and wherein a value of the resistance may be varied by opening and closing switches across one or more portions of the resistance responsive to the determined strength of the desired signal with respect to the interferer signal.

Regarding claim 18 of the pending application, claim 1 of U.S. Patent No. 7,010,330 encompass all the claimed limitation including a method for conserving battery power in a mobile communication device, the method comprising: receiving a radio signal by a radio receiver, of a wireless transceiver, that include includes a desired signal and an interferer signal; powering to the wireless transceiver by a battery; processing of the received radio signals in a receiver signal path within the radio receiver; determining the strength of the interferer signal by a circuit coupled to the receiver signal path dynamically changing one or more of an impedance of the receiver signal path of the receiver, or a gain of an amplifier gain stage in the receiver signal path both responsive to the determined strength of the interferer signal; wherein adjusting the gain of the gain stage and impedance of the receiver signal path result in improving a power drain from the battery.

Claims 1-18 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-7 of U.S. Patent No. 9,331,728. Although the claims at issue are not identical, they are not patentably distinct from each other because both are

drawn to the same invention of a method of controlling a battery power consumption of a transceiver.

Regarding claims 1 and 2 of the pending application, claims 1-7 of U.S. Patent No. 9,331,728 encompass all the claimed limitation including a method of power dissipation control in a receiver circuit within a battery powered mobile device when the receiver circuit is receiving and processing an RF input signal in a receiver signal path that includes a desired signal and an interferer signal, the method comprising: determining a strength of the desired signal with respect to the strength of the interferer signal; causing a decrease in power dissipation of a receiver signal path within the receiver circuit and a resultant decreased battery drain, by dynamically adjusting one or more of, a bias current of a component in the receiver signal path of the receiver circuit, an impedance of a component in the receiver signal path of the receiver circuit, or a gain of a component in the receiver signal path, based on the strength of the desired signal relative to the strength of the interferer signal, upon determination that the strength of the desired signal has increased relative to the strength of the interferer signal; causing an increase in power dissipation of the receiver signal path within the receiver circuit and a resultant increased battery drain, by dynamically adjusting one or more of, the bias current of the component in the receiver signal path of the receiver circuit, the gain of the component in the receiver signal path or the impedance of the component in the receiver signal path of the receiver circuit, based on the strength of the desired signal relative to the strength of the interferer signal, upon determination that the strength of the desired signal has decreased relative to the strength of the

interferer signal; wherein the bias current of the component in the receiver circuit is dynamically adjusted by one or both of, a changing of the value of an impedance across a voltage, a changing of the base voltage of a device whose emitter is connected to ground through a resistor, thereby optimizing the power drain from the battery.

Regarding claims 3-11 of the pending application, claims 1-7 of U.S. Patent No. 9,331,728 encompass all the claimed limitation including a method of power dissipation control in a receiver circuit within a battery powered mobile device when the receiver circuit is receiving an RF input signal in a receiver signal path that includes a desired signal and an interferer signal, the method comprising: determining a strength of the desired signal with respect to the interferer signal, wherein the receiver circuit comprises a defined receiver signal path between the RF input signal and a processed signal output; causing a decrease in power dissipation of the defined receiver signal path within the receiver circuit and a resultant decreased battery drain, by dynamically adjusting an impedance of a component in the receiver signal path of the receiver circuit upon determination that the strength of the desired signal has increased relative to the strength of the interferer signal; and causing an increase in power dissipation of the defined receiver signal path within the receiver circuit and a resultant increased battery drain, by dynamically adjusting the impedance of the component in the receiver signal path of the receiver circuit upon determination that the strength of the desired signal has decreased relative to the strength of the interferer signal; wherein the dynamically adjusting of the impedance occurs while the receiver circuit is processing signals received from the RF input; wherein dynamically adjusting the impedance of a

component in the receiver circuit comprises dynamically adjusting an impedance of a low noise amplifier (LNA) in the receiver signal path; wherein dynamically adjusting the impedance of a component in the receiver circuit comprises dynamically adjusting an impedance of a mixer in the receiver signal path; wherein dynamically adjusting the impedance of a component in the receiver circuit comprises dynamically adjusting an impedance of a filter in the receiver signal path; wherein the impedance of a component in the receiver circuit comprises a resistance, and wherein a value of the resistance is adjusted by opening switches across one or more portions of the resistance; wherein the defined receiver signal path includes components that comprise: a low noise amplifier (LNA), a filter, a mixer.

Regarding claims 12 and 13 of the pending application, claims 1-7 of U.S. Patent No. 9,331,728 encompass all the claimed limitation including a method of power dissipation control in a receiver circuit within a battery powered mobile device when the receiver circuit is receiving an RF input signal in a receiver signal path that includes a desired signal and an interferer signal, the method comprising: determining a strength of the interferer signal present in the received RF input signal; causing a decrease in power dissipation of the receiver signal path within the receiver circuit and a resultant decreased battery drain, by dynamically changing an impedance of a component in the receiver signal path of the receiver circuit upon determination that the strength of the interferer signal has decreased; causing an increase in power dissipation of the receiver signal path within the receiver circuit and the resultant decreased battery drain, by dynamically changing the impedance of the component in the receiver signal path of the

receiver circuit upon determination that the strength of the interferer signal has increased; wherein dynamically changing the impedance includes: dynamically adjusting the impedance of the component in the receiver signal path of the receiver circuit through a plurality of levels; between a high level and a low level from an initial point, responsive to the strength of the interferer signal present in the received RF input signal, wherein the high and low levels represent a maximum power saving and a maximum power dissipation; and wherein the dynamically adjusting the impedance occurs while the receiver circuit is processing signals received from the RF input signal; wherein the impedance of the component in the receiver circuit comprises a resistance, and wherein the value of the resistance may be increased by opening switches across one or more portions of the resistance.

Regarding claims 14 and 15 of the pending application, claims 1-7 of U.S. Patent No. 9,331,728 encompass all the claimed limitation including a method of controlling power dissipation in a receiver circuit within a battery powered mobile device when the receiver circuit is receiving and processing an RF input signal in a receiver signal path of the receiver circuit that includes a desired signal and an interferer signal, the method comprising: determining a strength of the interferer signal present in the received RF input signal; causing a decrease in power dissipation of the receiver signal path of the receiver circuit resulting in a decrease in drain on battery life, by dynamically adjusting one or more of a bias, a gain or an impedance in the receiver signal path of the receiver circuit, upon determination that the strength of the interferer signal has decreased; or alternately causing an increase in power dissipation of the receiver signal path of the

receiver circuit resulting in an increase in drain on battery life, by dynamically adjusting one or more of the bias, the gain or the impedance of a component in the receiver signal path of the receiver circuit, upon determination that the strength of the interferer signal has increased; thereby optimizing the power dissipation of the battery powered mobile device; wherein the gain of the component in the receiver signal path of the receiver circuit is varied by increasing a current in a differential pair and /or increasing a load resistance using switches.

Regarding claims 16 and 17 of the pending application, 1-7 of U.S. Patent No. 9,331,728 encompass all the claimed limitation including a mobile communications device, comprising: a receiver circuit for receiving an RF input signal that includes a desired signal and an interferer signal; a battery that powers the mobile communications device including the receiver circuit; wherein a strength of the desired signal is determined with respect to the strength of the interferer signal; wherein a decrease in power dissipation of a receiver signal path within the receiver circuit and a resultant decreased battery drain is caused by dynamically adjusting an impedance of a component in a receiver signal path of the receiver circuit upon determination that the strength of the desired signal has increased relative to the strength of the interferer signal; and wherein an increase in power dissipation of the receiver signal path within the receiver circuit and a resultant increased battery drain, is caused by dynamically adjusting the impedance of the component in the receiver signal path of the receiver circuit upon determination that the strength of the desired signal has decreased relative to the strength of the interferer signal; and wherein the dynamically changing the

impedance occurs while the receiver circuit is processing signals received from the RF input signal; wherein the impedance of the component in the receiver circuit comprises a resistance, and wherein a value of the resistance may be varied by opening and closing switches across one or more portions of the resistance responsive to the determined strength of the desired signal with respect to the interferer signal.

Regarding claim 18 of the pending application, claim 1 of U.S. Patent No. 9,331,728 encompass all the claimed limitation including a method for conserving battery power in a mobile communication device, the method comprising: receiving a radio signal by a radio receiver, of a wireless transceiver, that include includes a desired signal and an interferer signal; powering to the wireless transceiver by a battery; processing of the received radio signals in a receiver signal path within the radio receiver; determining the strength of the interferer signal by a circuit coupled to the receiver signal path dynamically changing one or more of an impedance of the receiver signal path of the receiver, or a gain of an amplifier gain stage in the receiver signal path both responsive to the determined strength of the interferer signal; wherein adjusting the gain of the gain stage and impedance of the receiver signal path result in improving a power drain from the battery.

Claims 1-18 are provisionally rejected on the ground of nonstatutory double patenting as being unpatentable over claims 3-9 and 20-28 of copending Application No. 15/080,421 (reference application). Although the claims at issue are not identical,

they are not patentably distinct from each other because both are drawn to the same invention of a method of controlling a battery power consumption of a transceiver.

This is a provisional nonstatutory double patenting rejection because the patentably indistinct claims have not in fact been patented.

Regarding claims 1 and 2 of the pending application, claims 3 and 4 of copending Application No. 15/080,421 encompass all the claimed limitation including a method of power dissipation control in a receiver circuit within a battery powered mobile device when the receiver circuit is receiving and processing an RF input signal in a receiver signal path that includes a desired signal and an interferer signal, the method comprising: determining a strength of the desired signal with respect to the strength of the interferer signal; causing a decrease in power dissipation of a receiver signal path within the receiver circuit and a resultant decreased battery drain, by dynamically adjusting one or more of, a bias current of a component in the receiver signal path of the receiver circuit, an impedance of a component in the receiver signal path of the receiver circuit, or a gain of a component in the receiver signal path, based on the strength of the desired signal relative to the strength of the interferer signal, upon determination that the strength of the desired signal has increased relative to the strength of the interferer signal; causing an increase in power dissipation of the receiver signal path within the receiver circuit and a resultant increased battery drain, by dynamically adjusting one or more of, the bias current of the component in the receiver signal path of the receiver circuit, the gain of the component in the receiver signal path or the impedance of the component in the receiver signal path of the receiver circuit,

based on the strength of the desired signal relative to the strength of the interferer signal, upon determination that the strength of the desired signal has decreased relative to the strength of the interferer signal; wherein the bias current of the component in the receiver circuit is dynamically adjusted by one or both of, a changing of the value of an impedance across a voltage, a changing of the base voltage of a device whose emitter is connected to ground through a resistor, thereby optimizing the power drain from the battery.

Regarding claims 3-11 of the pending application, claims 3-9 and 20-28 of copending Application No. 15/080,421 encompass all the claimed limitation including a method of power dissipation control in a receiver circuit within a battery powered mobile device when the receiver circuit is receiving an RF input signal in a receiver signal path that includes a desired signal and an interferer signal, the method comprising: determining a strength of the desired signal with respect to the interferer signal, wherein the receiver circuit comprises a defined receiver signal path between the RF input signal and a processed signal output; causing a decrease in power dissipation of the defined receiver signal path within the receiver circuit and a resultant decreased battery drain, by dynamically adjusting an impedance of a component in the receiver signal path of the receiver circuit upon determination that the strength of the desired signal has increased relative to the strength of the interferer signal; and causing an increase in power dissipation of the defined receiver signal path within the receiver circuit and a resultant increased battery drain, by dynamically adjusting the impedance of the component in the receiver signal path of the receiver circuit upon determination that the

strength of the desired signal has decreased relative to the strength of the interferer signal; wherein the dynamically adjusting of the impedance occurs while the receiver circuit is processing signals received from the RF input; wherein dynamically adjusting the impedance of a component in the receiver circuit comprises dynamically adjusting an impedance of a low noise amplifier (LNA) in the receiver signal path; wherein dynamically adjusting the impedance of a component in the receiver circuit comprises dynamically adjusting an impedance of a mixer in the receiver signal path; wherein dynamically adjusting the impedance of a component in the receiver circuit comprises dynamically adjusting an impedance of a filter in the receiver signal path; wherein the impedance of a component in the receiver circuit comprises a resistance, and wherein a value of the resistance is adjusted by opening switches across one or more portions of the resistance; wherein the defined receiver signal path includes components that comprise: a low noise amplifier (LNA), a filter, a mixer.

Regarding claims 12 and 13 of the pending application, claims 20 and 28 of copending Application No. 15/080,421 encompass all the claimed limitation including a method of power dissipation control in a receiver circuit within a battery powered mobile device when the receiver circuit is receiving an RF input signal in a receiver signal path that includes a desired signal and an interferer signal, the method comprising: determining a strength of the interferer signal present in the received RF input signal; causing a decrease in power dissipation of the receiver signal path within the receiver circuit and a resultant decreased battery drain, by dynamically changing an impedance of a component in the receiver signal path of the receiver circuit upon determination that

the strength of the interferer signal has decreased; causing an increase in power dissipation of the receiver signal path within the receiver circuit and the resultant decreased battery drain, by dynamically changing the impedance of the component in the receiver signal path of the receiver circuit upon determination that the strength of the interferer signal has increased; wherein dynamically changing the impedance includes: dynamically adjusting the impedance of the component in the receiver signal path of the receiver circuit through a plurality of levels; between a high level and a low level from an initial point, responsive to the strength of the interferer signal present in the received RF input signal, wherein the high and low levels represent a maximum power saving and a maximum power dissipation; and wherein the dynamically adjusting the impedance occurs while the receiver circuit is processing signals received from the RF input signal; wherein the impedance of the component in the receiver circuit comprises a resistance, and wherein the value of the resistance may be increased by opening switches across one or more portions of the resistance.

Regarding claims 14 and 15 of the pending application, claims 3 and 4 of copending Application No. 15/080,421 encompass all the claimed limitation including a method of controlling power dissipation in a receiver circuit within a battery powered mobile device when the receiver circuit is receiving and processing an RF input signal in a receiver signal path of the receiver circuit that includes a desired signal and an interferer signal, the method comprising: determining a strength of the interferer signal present in the received RF input signal; causing a decrease in power dissipation of the receiver signal path of the receiver circuit resulting in a decrease in drain on battery life,

by dynamically adjusting one or more of a bias, a gain or an impedance in the receiver signal path of the receiver circuit, upon determination that the strength of the interferer signal has decreased; or alternately causing an increase in power dissipation of the receiver signal path of the receiver circuit resulting in an increase in drain on battery life, by dynamically adjusting one or more of the bias, the gain or the impedance of a component in the receiver signal path of the receiver circuit, upon determination that the strength of the interferer signal has increased; thereby optimizing the power dissipation of the battery powered mobile device; wherein the gain of the component in the receiver signal path of the receiver circuit is varied by increasing a current in a differential pair and /or increasing a load resistance using switches.

Regarding claims 16 and 17 of the pending application, claims 3 and 4 of copending Application No. 15/080,421 encompass all the claimed limitation including a mobile communications device, comprising: a receiver circuit for receiving an RF input signal that includes a desired signal and an interferer signal; a battery that powers the mobile communications device including the receiver circuit; wherein a strength of the desired signal is determined with respect to the strength of the interferer signal; wherein a decrease in power dissipation of a receiver signal path within the receiver circuit and a resultant decreased battery drain is caused by dynamically adjusting an impedance of a component in a receiver signal path of the receiver circuit upon determination that the strength of the desired signal has increased relative to the strength of the interferer signal; and wherein an increase in power dissipation of the receiver signal path within the receiver circuit and a resultant increased battery drain, is caused by dynamically

adjusting the impedance of the component in the receiver signal path of the receiver circuit upon determination that the strength of the desired signal has decreased relative to the strength of the interferer signal; and wherein the dynamically changing the impedance occurs while the receiver circuit is processing signals received from the RF input signal; wherein the impedance of the component in the receiver circuit comprises a resistance, and wherein a value of the resistance may be varied by opening and closing switches across one or more portions of the resistance responsive to the determined strength of the desired signal with respect to the interferer signal.

Regarding claim 18 of the pending application, claim 3 of copending Application No. 15/080,421 encompass all the claimed limitation including a method for conserving battery power in a mobile communication device, the method comprising: receiving a radio signal by a radio receiver, of a wireless transceiver, that include includes a desired signal and an interferer signal; powering to the wireless transceiver by a battery; processing of the received radio signals in a receiver signal path within the radio receiver; determining the strength of the interferer signal by a circuit coupled to the receiver signal path dynamically changing one or more of an impedance of the receiver signal path of the receiver, or a gain of an amplifier gain stage in the receiver signal path both responsive to the determined strength of the interferer signal; wherein adjusting the gain of the gain stage and impedance of the receiver signal path result in improving a power drain from the battery.

Response to Arguments

Applicant's arguments filed 04/27/2017 and 06/27/2017 have been fully considered but they are not persuasive. Since the claims have been amended again on 06/27/2017, and the detailed rejection above address the amended limitation with Clark and Leifso et al.'s references.

Claims 1, 2, 12, 13 and 18 have been amended, and the previous rejected under 35 U.S.C. 112(a) or 35 U.S.C. 112 has been withdrawn.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to QUOCHIEN B. VUONG whose telephone number is (571)272-7902. The examiner can normally be reached on M-F 9:30-18:00.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nay Maung can be reached on (571) 272-7882. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/QUOCHIEN B VUONG/
Primary Examiner, Art Unit 2647

Substitute for form 1449A/PTO	*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	15/080,432
	Filing Date	03/24/2016
	First Named Inventor	Yannis Tsividis
	Group Art Unit	2647
	Examiner Name	Vuong, Quochien B
Sheet 1 of 1	Attorney Docket No: 10037P007CC2	

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	**Cite No [1]**	**Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.**	**T[2]**
/Q.B.V/		"Office Action Dated November 1, 2016; U.S. Patent Application No. 15/080,421", (11/1/2016)	

EXAMINER /QUOCHIEN B VUONG/ **DATE CONSIDERED** 09/01/2017

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449) as modified by BSTZ 03/26/07

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional) [2] Applicant is to place a check mark here if English language Translation is attached

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /Q.B.V/

Substitute for form 1449A/PTO	Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	15/080,432
	Filing Date	03/24/2016
	First Named Inventor	Yannis Tsividis
	Group Art Unit	2647
	Examiner Name	Vuong, Quochien B
Sheet 1 of 2	Attorney Docket No: 10037P007CC2	

US PATENT DOCUMENTS					
Examiner Initial *	**Cite No [1]**	**USP Document Number**	**Publication or Issue Date MM-DD-YYYY**	**Name of Patentee or Applicant of cited Document**	**Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear**
		US-2002/0050861	05/02/2002	Nguyen, Thinh C., et al.	
		US-2002/0137478	09/26/2002	Masamura, Hitoshi	
		US-2002/0190796	12/19/2002	Park, Joonbae , et al.	
		US-2003/0002452	01/02/2003	Sahota, Gurkanwal S.	
		US-2003/0025623	02/06/2003	Brueske, Daniel E., et al.	
		US-2003/0076168	04/24/2003	Forrester, Tim	
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		US-2003/0169089	09/11/2003	Manku, Tajinder , et al.	
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		US-4,894,566	01/16/1990	Rush, Michael J.	
		US-5,661,437	08/26/1997	Nishikawa, Kenjiro , et al.	
		US-5,949,286	09/07/1999	Jones, Mark A.	
		US-6,100,761	08/08/2000	Ezell, Richard W.	
		US-6,339,711	01/15/2002	Otaka, Shoji , et al.	
		US-6,388,525	05/14/2002	Bien, David E.	
		US-6,509,796	01/21/2003	Nguyen, Thinh C., et al.	
		US-6,633,550	10/14/2003	Gardenfors, Karl H., et al.	
		US-6,639,447	10/28/2003	Manku, Tajinder , et al.	
		US-6,657,498	12/02/2003	Park, Joonbae , et al.	
		US-6,670,901	12/30/2003	Brueske, Daniel E., et al.	
		US-6,710,651	03/23/2004	Forrester, Tim	
		US-6,784,738	08/31/2004	Jin, Xiaodong , et al.	
		US-6,807,406	10/19/2004	Razavi, Behzad , et al.	
		US-6,819,938	11/16/2004	Sahota, Gurkanwal S.	
		US-6,819,939	11/16/2004	Masamura, Hitoshi	
		US-6,944,427	09/13/2005	Haub, David , et al.	
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		US-7,016,654	03/21/2006	Bugeja, Alex	
		US-7,054,605	05/30/2006	Groe, John B.	
		US-7,274,760	09/25/2007	Palaskas, George , et al.	
		US-7,299,021	11/20/2007	Parssinen, Aarno , et al.	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	**Cite No [1]**	**Foreign Patent Document** Country Code/Number/Kind Code (if known)	**Publication Date MM-DD-YYYY**	**Name of Patentee or Applicant of cited Document**	**Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear**	**T[2]**
		WO-2004/017589	02/24/2004	Palaskas, George , et al.		

EXAMINER **DATE CONSIDERED**

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449) as modified by BSTZ 03/26/07
* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional) [2] Applicant is to place a check mark here if English language Translation is attached

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /Q.B.V/

Substitute for form 1449A/PTO	Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	15/080,432
	Filing Date	03/24/2016
	First Named Inventor	Yannis Tsividis
	Group Art Unit	2647
	Examiner Name	Vuong, Quochien B
Sheet 2 of 2	Attorney Docket No: 10037P007CC2	

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	**Cite No [1]**	**Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.**	**T[2]**
		CHRISTENSEN, CRAIG L., "A Low Power, Low Datarate Integrated 433MHz Wireless Transceiver in CMOS", Proceedings of the 15th Biennial University/Government/Industry Microelectronics Symposium, (2003), pp. 70-73	
		RUDELL, JACQUES C., et al., "Recent Developments in High Integration Multi-Standard CMOS Transceivers for Personal Communication Systems", Proceedings of the 1998 International Symposium on Low Power Electronics and Design, (Aug. 10-12, 1998), pp. 149-154	
		SCHUCHTER, WALTER , et al., "A Single Chip FSK/ASK 900MHz Transceiver in a Standard 0.25um CMOS Technology", 2001 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, (2001), pp. 183-186	

EXAMINER /QUOCHIEN B VUONG/ **DATE CONSIDERED** 09/01/2017

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449) as modified by BSTZ 03/26/07

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional) [2] Applicant is to place a check mark here if English language Translation is attached

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15080432	TSIVIDIS, YANNIS
	Examiner	Art Unit
	QUOCHIEN B VUONG	2647

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	10/28/2016	09/01/2017							
	1	✓	✓							
	2	✓	✓							
	3	✓	✓							
	4	✓	✓							
	5	✓	✓							
	6	✓	✓							
	7	✓	✓							
	8	✓	✓							
	9	✓	✓							
	10	✓	✓							
	11	✓	✓							
	12	✓	✓							
	13	✓	✓							
	14	✓	✓							
	15	✓	✓							
	16	✓	✓							
	17	✓	✓							
	18	✓	✓							

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15080432	TSIVIDIS, YANNIS
	Examiner	Art Unit
	QUOCHIEN B VUONG	2647

CPC- SEARCHED		
Symbol	Date	Examiner
H04B 1/04, 1/16, 1/40, 1/109, 1/0457, 1/1607, 17/309, 17/318, 17/336,17/345, 2001/045, 2001/0416	10/27/2016	/QV/
H04W 52/52, 52/0261, 88/02	10/27/2016	/QV/
H03G 3/004, 3/20	10/27/2016	/QV/

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
455	63.1,67.13,127.1,127.2,127.5,226.1,226.2,232.1,234.1,250.1,251.1,295,296,343.1,572,574	10/27/2016	/QV/
370	442	10/27/2016	/QV/
330	127,134,144	10/27/2016	/QV/

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

SEARCH NOTES		
Search Notes	Date	Examiner
EAST search	10/27/2016	/QV/
Inventor name search	10/27/2016	/QV/
Search updated	08/30/2017	/QV/

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

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REQUEST FOR CONTINUED EXAMINATION (RCE) TRANSMITTAL

Address to:
Mail Stop RCE
Commissioner for Patents
P.O. 1450
Alexandria, VA 22313-1450

Application No.	15/080,432
Filing Date	March 24, 2016
First Named Inventor	Yannis Tsividis
Art Unit	2647
Examiner Name	Vuong, Quochien B
Attorney Docket Number	10037P007CC2
Confirmation Number	6094

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, to any international application that does not comply with the requirements of 35 U.S.C 371, or to any design application. See Instruction Sheet for RCEs (not to be submitted to the USPTO on page 2.)

1. **Submission required under 37 CFR 1.114** Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).
   a. ☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office Action may be considered as a submission even if this box is not checked.
      i. ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on ____
      ii. ☐ Other _____
   b. ☒ Enclosed
      i. ☒ Amendment/Reply
      ii. ☐ Affidavit(s)/Declaration(s)
      iii. ☐ Information Disclosure Statement (IDS)
      iv. ☐ Other _____

2. **Miscellaneous**
   a. ☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months. (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)
   b. ☐ Other _____

3. **Fees** The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.
   a. ☒ The Director is hereby authorized to charge the following fees, any underpayment of fees, or credit any overpayments, to Deposit Account No. 090528.
      i. ☒ RCE fee required under 37 CFR 1.17(e)
      ii. ☒ Extension of time fee (37 CFR 1.136 and 1.17) Amt
      iii. ☐ Other: _____
   b. ☐ Check in the amount of $_____ enclosed

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

Name *(Print/Type)*	Roger W. Blakely, Jr.	*Registration No. (Attorney/Agent)*	25831
Signature	/Roger W. Blakely/	Date	March 6, 2018

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.

Name *(Print/Type)*	**Jessica A. Clark**		
Signature	/Jessica A. Clark/	Date	**March 6, 2018**

Based on PTO/SB/30 (10-07) as modified 10/04/2007.
SEND TO: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application. No.	:	15/080,432	Confirmation No. 6094
Inventor(s)	:	Yannis Tsividis	
Filed	:	03/24/2016	
TC/A.U.	:	2647	
Examiner	:	Vuong, Quochien B	
Docket No.	:	10037P007CC2	
Customer No.	:	8791	

Mail Stop RCE
Commissioner for Patents
PO Box 1450
Alexandria VA 22313-1450

AMENDMENT AND REQUEST FOR RECONSIDERATION AFTER REQUEST FOR CONTINUED EXAMINATION

Sir:

In response to the Final Office Action of September 6, 2017, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 8 of this paper.

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Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-18 (cancelled)

19. (new) A method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, and a corresponding increase in battery life of the battery powered portable wireless device, the method comprising:

receiving a wireless signal having a desired signal and an interferer signal, by the wireless transceiver of the battery powered portable wireless device, the wireless transceiver having a receiver signal path comprising a plurality of circuits, wherein the plurality of circuits includes an amplifier, a filter, and a mixer, and wherein the wireless transceiver comprises a circuit for determining a signal strength of the interferer signal and a circuit for determining a signal strength of the desired signal;

wherein a worst-case power dissipation condition results when the signal strength of the desired signal is low and the signal strength of the interferer signal is high; and

wherein the power dissipation reduction in the receiver is achieved by causing a bias current to vary in one or more of the plurality of circuits in the receiver signal path of the wireless transceiver as the signal strength of the interferer signal and the signal strength of the desired signal vary according to the following:

(i) when the signal strength of the interferer signal is high and the signal strength of the desired signal is low, and the desired signal is larger than in the worst-case power dissipation condition, causing the bias current of the one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be reduced compared to the worst-case power dissipation condition, thereby saving power; and

(ii) when the signal strength of the interferer signal is weak and the signal strength of the desired signal is weak, causing the bias current of the one or more of the plurality of circuits in

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the receiver signal path of the wireless transceiver to be decreased compared to the worst-case power dissipation condition, thereby saving power.

20. (new) The method of claim 19, wherein the change in the bias current of the one or more of the plurality of circuits in the receiver signal path is related to a change in an impedance in the one or more of the plurality of circuits in the receiver signal path and wherein the impedance comprises at least a resistor and a capacitor.

21. (new) A method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, and a corresponding increase in battery life of the battery powered portable wireless device, the method comprising:

receiving a wireless signal having a desired signal and an interferer signal, by the wireless transceiver of the battery powered portable wireless device, the wireless transceiver having a receiver signal path comprising a plurality of circuits, wherein the plurality of circuits includes an amplifier, a filter, and a mixer, and wherein the wireless transceiver comprises a circuit for determining a signal strength of the interferer signal and a circuit for determining a signal strength of the desired signal;

wherein a worst-case power dissipation condition from the battery results when the signal strength of the desired signal is low and the signal strength of the interferer signal is high; and

wherein the power dissipation reduction in the receiver is achieved by causing a bias current to vary in one or more of the plurality of circuits in the receiver signal path of the wireless transceiver as the signal strength of the interferer signal and the signal strength of the desired signal vary, according to the following:

when the signal strength of the interferer signal is high and the signal strength of the desired signal is low, and the desired signal has a signal strength that is larger than in the worst-case power dissipation conditions, causing the bias current of the one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be decreased compared to the worst-case power dissipation condition, causing a reduction in power dissipation.

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22. (new) The method of claim 21, wherein the change in the bias current of the one or more of the plurality of circuits in the receiver signal path is related to a change in an impedance in the one or more of the plurality of circuits in the receiver signal path;

and wherein the impedance comprises at least a resistor and a capacitor.

23. (new) A method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, and a corresponding reduction in a drain on battery life of the battery powered portable wireless device, the method comprising:

receiving a wireless signal having a desired signal and an interferer signal, by the wireless transceiver of the battery powered portable wireless device, the wireless transceiver having a receiver signal path comprising a plurality of circuits, wherein the plurality of circuits includes an amplifier, a filter, and a mixer, and wherein the wireless transceiver comprises a circuit for determining a signal strength of the interferer signal and a circuit for determining a signal strength of the desired signal;

wherein a worst-case power dissipation condition results when the signal strength of the desired signal is low and the signal strength of the interferer signal is high; and

wherein the power dissipation reduction in the receiver is achieved by causing a bias current to vary in one or more of the plurality of circuits in the receiver signal path of the wireless transceiver as the signal strength of the interferer signal and the signal strength of the desired signal vary, according to the following:

(i) when the signal strength of the interferer signal is high and the signal strength of the desired signal is weak, and the desired signal is larger than in the worst-case power dissipation condition, causing the bias current of the one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be reduced compared to the worst-case power dissipation condition, thereby saving power;

(ii) when the signal strength of the interferer signal is high and the signal strength of the desired signal is high, causing the bias current of the one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be decreased compared to the worst-case power dissipation condition, thereby saving power;

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(iii) when the signal strength of the interferer signal is weak and the signal strength of the desired signal is weak, causing the bias current of the one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be decreased compared to the worst-case power dissipation condition, thereby saving power; and

(iv) when the signal strength of the interferer signal is weak and the signal strength of the desired signal is high, causing the bias current of the one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be decreased compared to the worst-case power dissipation condition, thereby saving power.

24. (new) The method of claim 23, wherein the change in the bias current of the one or more of the plurality of circuits in the receiver signal path is related to a change in an impedance in the one or more of the plurality of circuits in the receiver signal path;

and wherein the impedance comprises at least a resistor and a capacitor.

25. (new) A method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, and a corresponding reduction in a drain on battery life of the battery powered portable wireless device, the method comprising:

receiving a wireless signal having a desired signal and an interferer signal, by the wireless transceiver of the battery powered portable wireless device, the wireless transceiver having a receiver signal path comprising a plurality of circuits, wherein the plurality of circuits includes an amplifier, a filter, and a mixer, and wherein the wireless transceiver comprises a circuit for determining a signal strength of the interferer signal and a signal strength of the desired signal in the receiver signal path;

wherein a worst-case power dissipation condition in the receiver results when the signal strength of the desired signal is low and the signal strength of the interferer signal is high; and

wherein the power dissipation reduction is achieved by causing an impedance and a bias current of one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to vary as the signal strength of the interferer signal and the signal strength of the desired signal to vary according to the following:

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(i) when the signal strength of the interferer signal is high and the signal strength of the desired signal is low and the desired signal is larger than in the worst-case power dissipation conditions, causing the bias current of the circuit in the receiver signal path of the wireless transceiver to be reduced compared to the worst-case power dissipation condition, causing a reduction in power dissipation;

(ii) when the signal strength of the interferer signal is high and the signal strength of the desired signal is high, causing the impedance of the circuit in the receiver signal path of the wireless transceiver to be increased compared to the worst-case power dissipation condition, causing a reduction in power dissipation;

(iii) when the signal strength of the interferer signal is low and the signal strength of the desired signal is low, causing the bias current of the circuit in the receiver signal path of the wireless transceiver to be reduced compared to the worst-case power dissipation condition, causing a reduction in power dissipation;

(iv) when the signal strength of the interferer signal is low and the signal strength of the desired signal is high, causing the impedance of the circuit in the receiver signal path of the wireless transceiver to be increased compared to the worst-case power dissipation condition, causing a reduction in power dissipation; and

wherein increasing the impedance of the circuit reduces a drive current of the circuit and reduces the associated bias current of the circuit.

26. (new) A method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, and a corresponding reduction in power dissipation and an increase in battery life of the battery powered portable wireless device, the method comprising:

receiving a wireless signal having a desired signal and an interferer signal, by the wireless transceiver of the battery powered portable wireless device, the wireless transceiver having a receiver signal path comprising a plurality of circuits, wherein the plurality of circuits includes an amplifier, a filter, and a mixer, and wherein the wireless transceiver comprises a circuit for determining a signal strength of the interferer signal and a circuit for determining a signal strength of the desired signal;

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wherein a worst-case power dissipation condition from the battery results when the signal strength of the desired signal is low and the signal strength of the interferer signal is high; and

wherein the power dissipation reduction in the receiver is achieved by causing a bias current and an impedance to vary in one or more of the plurality of circuits in the receiver signal path of the wireless transceiver as the signal strength of the interferer signal and the signal strength of the desired signal vary, according to the following:

when the signal strength of the interferer signal is high and the signal strength of the desired signal is low, and the desired signal has a signal strength that is larger than in the worst-case power dissipation condition, causing:

(i) the bias current of the one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be decreased; and

(ii) an impedance of the one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be increased, thereby causing a drive current of the one or more of the plurality of circuits to be decreased.

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REMARKS/ARGUMENTS

In the present amendment, all prior claims have been cancelled and new claims 19-26 have been added. These new claims have been very carefully drafted to claim various aspects of the invention disclosed and combinations of such aspects using the exact terminology of the disclosure to the extent possible within the limitations of proper claim drafting.

New independent claim 25 generally corresponds to claim 29 of U.S. Patent No. 9,838,962, though presented in a somewhat different organization and again, very closely following the terminology used in the disclosure. Accordingly, it is believed that new claim 25 is allowable as filed.

New independent claim 19 generally claims "A method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device" … by "causing the bias current of the one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be decreased" using either of two criterion based on the signal strength of an interferer signal and the signal strength of the desired signal.

New independent claim 21 generally claims "A method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device" … by "causing the bias current of the one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be decreased" using a criterion based on the signal strength of an interferer signal and the signal strength of the desired signal.

New independent claim 23 generally claims "A method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device" … by "causing the bias current of the one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be decreased" using either of four criterion based on the signal strength of an interferer signal and the signal strength of the desired signal.

New independent claim 26 generally claims "A method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device" … by "causing a bias current and an impedance to vary in one or more of the plurality of circuits in the

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receiver signal path of the wireless transceiver" using a criterion based on the signal strength of an interferer signal and the signal strength of the desired signal.

In the outstanding final office action, the examiner acknowledges that "Clark does not specifically disclose wherein the bias current of the component in the receiver circuit is dynamically adjusted by one or both of, a changing of the value of an impedance across a voltage, a changing of the base voltage of a device whose emitter is connected to ground through a resistor, thereby optimizing the power drain from the battery" but goes on to say "However, Leifso et al. (figure 4) disclose varying a gain of an amplifier by variably a bias current of the component in the receiver circuit is dynamically adjusted by one or both of, a changing of the value of an impedance across a voltage, a changing of the base voltage of a device whose emitter is connected to ground through a resistor (column 6, line 26 – column 8, line 15)." While the last statement appears to be inadvertently scrambled and is not understood by the undersigned, the undersigned does not understand any relevance of Leifso to the present invention as claimed herein.

In particular, in Leifso "A gain control circuit that permits a variable gain amplifier circuit to operate with high input linearity and low power consumption is disclosed." (First sentence of the Abstract). "FIG. 2 shows a block diagram illustrating a Variable Bias Degeneration Automatic Gain Control system in accordance with an embodiment the present invention;" and "FIG. 3 shows a block diagram illustrating functional blocks of the gain control circuit shown in FIG. 2;" (Brief Description of the Drawings) Both Figs. show inputs of VREF (a reference voltage), VCTRL ("VCTRL is a user defined voltage level that sets the desired gain of VGA circuit 102 from FIG. 2. (Col. 6, lines 2-4)), and VBIAS (a bias voltage) Thus Leifso simply provides "A gain control circuit that permits a variable gain amplifier circuit to operate with high input linearity and low power consumption is disclosed" as the Abstract states. The Leifso circuit simply requires a user to input a control signal that tells the circuit what to do, and the circuit will do it efficiently. Accordingly the Leifso invention may well be useable in embodiments of the present invention that use or include the control of gain.

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However the present invention as claimed in the claims now under consideration is not directed to the detailed circuit design of a gain control circuit, or of a bias control circuit or of an impedance control circuit, but rather is directed to when, and how, such parameters, particularly bias and impedance, should be controlled based on the signal strength of an interferer signal and the signal strength of a desired signal. As stated before, the examiner acknowledges that "Clark does not specifically disclose wherein the bias current of the component in the receiver circuit is dynamically adjusted by one or both of, a changing of the value of an impedance across a voltage, a changing of the base voltage of a device whose emitter is connected to ground through a resistor, thereby optimizing the power drain from the battery". It is respectfully submitted that the examiner has also not pointed out any part of Leifso that suggests when, and how, such parameters, particularly bias or bias and impedance, should be controlled based on the signal strength of an interferer signal and the signal strength of the desired signal as now claimed.

Thus for the foregoing reasons, it is believed that all independent claims in the case are in condition for allowance.

The dependent claims, namely dependent claims 20, 22 and 24 add limitations regarding associated impedance changes to the independent claims, and are believed allowable as dependent on now allowable independent claims and as providing greater novelty and specificity to the overall claimed method.

Thus for the foregoing reasons, it is believed that all claims in the case are in condition for allowance.

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CONCLUSION

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 03/06/2018

By _____
Roger W. Blakely, Jr.
Reg. No. 25,831
Tel.: (714) 557-3800 (Pacific Coast)

1279 Oakmead Parkway
Sunnyvale, California 94085

CERTIFICATE OF TRANSMISSION (37 CFR 1.8A)

I hereby certify that this correspondence is being EFS Web transmitted to the USPTO on the date shown below.

Date: 03/06/2018

Jessica A Clark 3/6/2018
Jessica A. Clark *Date*

IPR2024-00817
Apple EX1002 Page 341

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application. No.	:	15/080,432	Confirmation No. 6094
Applicant	:	Yannis Tsividis	
Filed	:	03/24/2016	
TC/A.U.	:	2647	
Examiner	:	Vuong, Quochien B	
Docket No.	:	10037P007CC2	
Customer No.	:	8791	

Mail Stop AF
Commissioner for Patents
PO Box 1450
Alexandria VA 22313-1450

AUTHORIZATION FOR EXTENSION OF TIME, ALL REPLIES

Sir:

Authorization is given to treat any concurrent or future reply requiring a petition for an extension of time under 37 CFR §1.136(a) for its timely submission, as incorporating a petition for extension of time for the appropriate length of time. If any other petition is necessary for consideration of this paper, it is hereby so petitioned. Please charge any shortage in fees in connection with the filing of this paper, including extension of time fees, to Deposit Account 02-2666 and please credit any excess fees to such deposit account.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 03/06/2018

By _____
Roger W. Blakely, Jr.
Reg. No. 25,831
Tel.: (714) 557-3800 (Pacific Coast)

1279 Oakmead Parkway
Sunnyvale, California 94085

CERTIFICATE OF TRANSMISSION (37 CFR 1.8A)

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Date: 03/06/2018

Jessica A. Clark 3/6/2018
Jessica A. Clark *Date*

IPR2024-00817
Apple EX1002 Page 342

Electronic Patent Application Fee Transmittal

Application Number:	15080432
Filing Date:	24-Mar-2016
Title of Invention:	Power Dissipation Reduction in Wireless Transceivers
First Named Inventor/Applicant Name:	Yannis Tsividis
Filer:	Roger W. Blakely/Jessica Clark
Attorney Docket Number:	10037P007CC2

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension - 3 months with $0 paid	2253	1	700	700
Miscellaneous:				
RCE- 1st Request	2801	1	650	650
		Total in USD ($)		**1350**

Electronic Acknowledgement Receipt

EFS ID:	31977294
Application Number:	15080432
International Application Number:	
Confirmation Number:	6094
Title of Invention:	Power Dissipation Reduction in Wireless Transceivers
First Named Inventor/Applicant Name:	Yannis Tsividis
Customer Number:	8791
Filer:	Roger W. Blakely/Jessica Clark
Filer Authorized By:	Roger W. Blakely
Attorney Docket Number:	10037P007CC2
Receipt Date:	06-MAR-2018
Filing Date:	24-MAR-2016
Time Stamp:	18:57:47
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$1350
RAM confirmation Number	030718INTEFSW00006118090528
Deposit Account	090528
Authorized User	Jessica Clark

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

37 CFR 1.16 (National application filing, search, and examination fees)

37 CFR 1.17 (Patent application and reexamination processing fees)

37 CFR 1.19 (Document supply fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Extension of Time	10037P007CC2_20180306_Ext.pdf	30966 b22cbdcbf1ad522ca579bfedc409a0f750bdf4b8	no	1
Warnings:					
Information:					
2	Request for Continued Examination (RCE)	10037P007CC2_20180306_RCE.pdf	55109 b7a051081c28cc43d7403639da14984f2409e511	no	1
Warnings:					
This is not a USPTO supplied RCE SB30 form.					
Information:					
3		10037P007CC2_20180306_Amd.pdf	189545 15f8c98c82b7321fef849d0f72fcd93b23f32edf	yes	12

Multipart Description/PDF files in .zip description

Document Description	Start	End
Amendment Submitted/Entered with Filing of CPA/RCE	1	1
Claims	2	7
Applicant Arguments/Remarks Made in an Amendment	8	11
Authorization for Extension of Time all replies	12	12

Warnings:					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	32172 152c15054e19ccc9d224cd2cf2629873c9d8d38d	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	30272		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Docket No.: 10037P007CC2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of:

YANNIS TSIVIDIS

Application No.: 15/080,432

Filed: March 24, 2016

For: **Power Dissipation Reduction in Wireless Transceivers**

Art Group: 2647

Examiner: Vuong, Quochien B

PETITION FOR EXTENSION OF TIME PURSUANT TO 37 C.F.R. § 1.136(a)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with 37 C.F. R. §1.136(a), Applicant for the above-identified application respectfully Petitions the Commissioner for a three (3) month extension of time, extending the period for response to March 06, 2018, from the Final Office Action dated September 06, 2017. A Request for Continued Examination (RCE) and Amendment is/are attached. You are hereby authorized to charge our Deposit Account No. 090528 the amount of $700.00 (petition filing fee).

If it should be determined that a longer extension of time is required to prevent this application from being abandoned, please charge any additional fees to Deposit Account No. 090528.

Respectfully submitted,

Womble Bond Dickinson (US) LLP

Date: March 06, 2018

Roger W. Blakely, Jr., Reg. No. 25831

CERTIFICATE OF MAILING/TRANSMISSION

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.

Jessica A. Clark *03-06-18*

Jessica A. Clark *Date*

P.O. Box 7037
Atlanta, GA 30357-0037
Telephone: (714) 557-3800

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 15/080,432	Filing Date 03/24/2016	☐ To be Mailed

ENTITY: ☐ LARGE ☒ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	03/06/2018	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 8	Minus	** 20	= 0	X $50 =	0
	Independent (37 CFR 1.16(h))	* 5	Minus	***6	= 0	X $230 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

SLIE
LISA FULTON

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/080,432	03/24/2016	Yannis Tsividis	10037P007CC2	6094

8791 7590 04/13/2018

WOMBLE BOND DICKINSON (US) LLP
Attn: IP Docketing
P.O. Box 7037
Atlanta, GA 30357-0037

EXAMINER
VUONG, QUOCHIEN B

ART UNIT	PAPER NUMBER
2647	

NOTIFICATION DATE	DELIVERY MODE
04/13/2018	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

FIP_Group@bstz.com
PTO.MAIL@BSTZPTO.COM
PTO.MAIL@BSTZ.COM

Office Action Summary	Application No. 15/080,432	Applicant(s) TSIVIDIS, YANNIS	
	Examiner QUOCHIEN B. VUONG	Art Unit 2647	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03/06/2018*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *19-26* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *19-26* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

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The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 03/06/2018 has been entered.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*,

686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on nonstatutory double patenting provided the reference application or patent either is shown to be commonly owned with the examined application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. See MPEP § 717.02 for applications subject to examination under the first inventor to file provisions of the AIA as explained in MPEP § 2159. See MPEP §§ 706.02(l)(1) - 706.02(l)(3) for applications not subject to examination under the first inventor to file provisions of the AIA. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO Internet website contains terminal disclaimer forms which may be used. Please visit www.uspto.gov/patent/patents-forms. The filing date of the application in which the form is filed determines what form (e.g., PTO/SB/25, PTO/SB/26, PTO/AIA/25, or PTO/AIA/26) should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.

Claims 19-26 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-7 of U.S. Patent No. 9,838,962. Although the claims

at issue are not identical, they are not patentably distinct from each other because both are drawn to the same invention of a method for power dissipation reduction in a receiver of a wireless transceiver by varying an impedance and a bias current of one or more of the plurality of the plurality of circuits in the receiver path.

Regarding claims 19 and 20 of the present application, claims 1-7 of U.S. Patent No. 9,838,962 obviously encompass all the claimed limitation including a method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, and a corresponding increase in battery life of the battery powered portable wireless device, the method comprising: receiving a wireless signal having a desired signal and an interferer signal, by the wireless transceiver of the battery powered portable wireless device, the wireless transceiver having a receiver signal path comprising a plurality of circuits, wherein the plurality of circuits includes an amplifier, a filter, and a mixer, and wherein the wireless transceiver comprises a circuit for determining a signal strength of the interferer signal and a circuit for determining a signal strength of the desired signal; wherein a worst-case power dissipation condition results when the signal strength of the desired signal is low and the signal strength of the interferer signal is high; and wherein the power dissipation reduction in the receiver is achieved by causing a bias current to vary in one or more of the plurality of circuits in the receiver signal path of the wireless transceiver as the signal strength of the interferer signal and the signal strength of the desired signal vary according to the following: (i) when the signal strength of the interferer signal is high and the signal strength of the desired signal is low, and the desired signal is larger than in the worst-

case power dissipation condition, causing the bias current of the one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be reduced compared to the worst-case power dissipation condition, thereby saving power; and (ii) when the signal strength of the interferer signal is weak and the signal strength of the desired signal is weak, causing the bias current of the one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be decreased compared to the worst-case power dissipation condition, thereby saving power, wherein the change in the bias current of the one or more of the plurality of circuits in the receiver signal path is related to a change in an impedance in the one or more of the plurality of circuits in the receiver signal path and wherein the impedance comprises at least a resistor and a capacitor.

Regarding claims 21 and 22 of the present application, claims 1-7 of U.S. Patent No. 9,838,962 obviously encompass all the claimed limitation including a method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, and a corresponding increase in battery life of the battery powered portable wireless device, the method comprising: receiving a wireless signal having a desired signal and an interferer signal, by the wireless transceiver of the battery powered portable wireless device, the wireless transceiver having a receiver signal path comprising a plurality of circuits, wherein the plurality of circuits includes an amplifier, a filter, and a mixer, and wherein the wireless transceiver comprises a circuit for determining a signal strength of the interferer signal and a circuit for determining a signal strength of the desired signal; wherein a worst-case power dissipation condition

from the battery results when the signal strength of the desired signal is low and the signal strength of the interferer signal is high; and wherein the power dissipation reduction in the receiver is achieved by causing a bias current to vary in one or more of the plurality of circuits in the receiver signal path of the wireless transceiver as the signal strength of the interferer signal and the signal strength of the desired signal vary, according to the following: when the signal strength of the interferer signal is high and the signal strength of the desired signal is low, and the desired signal has a signal strength that is larger than in the worst- case power dissipation conditions, causing the bias current of the one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be decreased compared to the worst-case power dissipation condition, causing a reduction in power dissipation, wherein the change in the bias current of the one or more of the plurality of circuits in the receiver signal path is related to a change in an impedance in the one or more of the plurality of circuits in the receiver signal path; and wherein the impedance comprises at least a resistor and a capacitor.

Regarding claims 23 and 24 of the present application, claims 1-7 of U.S. Patent No. 9,838,962 obviously encompass all the claimed limitation including a method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, and a corresponding reduction in a drain on battery life of the battery powered portable wireless device, the method comprising: receiving a wireless signal having a desired signal and an interferer signal, by the wireless transceiver of the battery powered portable wireless device, the wireless transceiver having a receiver signal path comprising a plurality of circuits, wherein the plurality of circuits includes an

amplifier, a filter, and a mixer, and wherein the wireless transceiver comprises a circuit for determining a signal strength of the interferer signal and a circuit for determining a signal strength of the desired signal; wherein a worst-case power dissipation condition results when the signal strength of the desired signal is low and the signal strength of the interferer signal is high; and wherein the power dissipation reduction in the receiver is achieved by causing a bias current to vary in one or more of the plurality of circuits in the receiver signal path of the wireless transceiver as the signal strength of the interferer signal and the signal strength of the desired signal vary, according to the following: (i) when the signal strength of the interferer signal is high and the signal strength of the desired signal is weak, and the desired signal is larger than in the worst-case power dissipation condition, causing the bias current of the one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be reduced compared to the worst-case power dissipation condition, thereby saving power; (ii) when the signal strength of the interferer signal is high and the signal strength of the desired signal is high, causing the bias current of the one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be decreased compared to the worst-case 24 power dissipation condition, thereby saving power; (iii) when the signal strength of the interferer signal is weak and the signal strength of the desired signal is weak, causing the bias current of the one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be decreased compared to the worst-case power dissipation condition, thereby saving power; and (iv) when the signal strength of the interferer signal is weak and the signal strength of the desired signal is

high, causing the bias current of the one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be decreased compared to the worst-case power dissipation condition, thereby saving power, wherein the change in the bias current of the one or more of the plurality of circuits in the receiver signal path is related to a change in an impedance in the one or more of the plurality of circuits in the receiver signal path; and wherein the impedance comprises at least a resistor and a capacitor.

Regarding claim 25 of the present application, claims 1-7 of U.S. Patent No. 9,838,962 obviously encompass all the claimed limitation including a method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, and a corresponding reduction in a drain on battery life of the battery powered portable wireless device, the method comprising: receiving a wireless signal having a desired signal and an interferer signal, by the wireless transceiver of the battery powered portable wireless device, the wireless transceiver having a receiver signal path comprising a plurality of circuits, wherein the plurality of circuits includes an amplifier, a filter, and a mixer, and wherein the wireless transceiver comprises a circuit for determining a signal strength of the interferer signal and a signal strength of the desired signal in the receiver signal path; wherein a worst-case power dissipation condition in the receiver results when the signal strength of the desired signal is low and the signal strength of the interferer signal is high; and wherein the power dissipation reduction is achieved by causing an impedance and a bias current of one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to vary as the signal strength of the interferer signal and the signal strength of the desired signal to

vary according to the following: (i) when the signal strength of the interferer signal is high and the signal strength of the desired signal is low and the desired signal is larger than in the worst-case power dissipation conditions, causing the bias current of the circuit in the receiver signal path of the wireless transceiver to be reduced compared to the worst-case power dissipation condition, causing a reduction in power dissipation; (ii) when the signal strength of the interferer signal is high and the signal strength of the desired signal is high, causing the impedance of the circuit in the receiver signal path of the wireless transceiver to be increased compared to the worst-case power dissipation condition, causing a reduction in power dissipation; (iii) when the signal strength of the interferer signal is low and the signal strength of the desired signal is low, causing the bias current of the circuit in the receiver signal path of the wireless transceiver to be reduced compared to the worst-case power dissipation condition, causing a reduction in power dissipation; (iv) when the signal strength of the interferer signal is low and the signal strength of the desired signal is high, causing the impedance of the circuit in the receiver signal path of the wireless transceiver to be increased compared to the worst-case power dissipation condition, causing a reduction in power dissipation; and wherein increasing the impedance of the circuit reduces a drive current of the circuit and reduces the associated bias current of the circuit.

Regarding claim 26 of the present application, claims 1-7 of U.S. Patent No. 9,838,962 obviously encompass all the claimed limitation including a method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, and a corresponding reduction in power dissipation and an

increase in battery life of the battery powered portable wireless device, the method comprising: receiving a wireless signal having a desired signal and an interferer signal, by the wireless transceiver of the battery powered portable wireless device, the wireless transceiver having a receiver signal path comprising a plurality of circuits, wherein the plurality of circuits includes an amplifier, a filter, and a mixer, and wherein the wireless transceiver comprises a circuit for determining a signal strength of the interferer signal and a circuit for determining a signal strength of the desired signal; wherein a worst-case power dissipation condition from the battery results when the signal strength of the desired signal is low and the signal strength of the interferer signal is high; and wherein the power dissipation reduction in the receiver is achieved by causing a bias current and an impedance to vary in one or more of the plurality of circuits in the receiver signal path of the wireless transceiver as the signal strength of the interferer signal and the signal strength of the desired signal vary, according to the following: when the signal strength of the interferer signal is high and the signal strength of the desired signal is low, and the desired signal has a signal strength that is larger than in the worst- case power dissipation condition, causing: (i) the bias current of the one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be decreased; and (ii) an impedance of the one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be increased, thereby causing a drive current of the one or more of 24 the plurality of circuits to be decreased.

Response to Arguments

Applicant's arguments filed 03/06/2018 have been fully considered.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to QUOCHIEN B. VUONG whose telephone number is (571)272-7902. The examiner can normally be reached on M-F 9:30-18:00.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nay Maung can be reached on (571) 272-7882. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/QUOCHIEN B VUONG/
Primary Examiner, Art Unit 2647

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15080432	TSIVIDIS, YANNIS
	Examiner	Art Unit
	QUOCHIEN B VUONG	2647

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	10/28/2016	09/01/2017	04/10/2018						
	1	✓	✓	-						
	2	✓	✓	-						
	3	✓	✓	-						
	4	✓	✓	-						
	5	✓	✓	-						
	6	✓	✓	-						
	7	✓	✓	-						
	8	✓	✓	-						
	9	✓	✓	-						
	10	✓	✓	-						
	11	✓	✓	-						
	12	✓	✓	-						
	13	✓	✓	-						
	14	✓	✓	-						
	15	✓	✓	-						
	16	✓	✓	-						
	17	✓	✓	-						
	18	✓	✓	-						
	19			✓						
	20			✓						
	21			✓						
	22			✓						
	23			✓						
	24			✓						
	25			✓						
	26			✓						

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15080432	TSIVIDIS, YANNIS
	Examiner	Art Unit
	QUOCHIEN B VUONG	2647

CPC- SEARCHED		
Symbol	Date	Examiner
H04B 1/04, 1/16, 1/40, 1/109, 1/0457, 1/1607, 17/309, 17/318, 17/336,17/345, 2001/045, 2001/0416	10/27/2016	/QV/
H04W 52/52, 52/0261, 88/02	10/27/2016	/QV/
H03G 3/004, 3/20	10/27/2016	/QV/

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
455	63.1,67.13,127.1,127.2,127.5,226.1,226.2,232.1,234.1,250.1,251.1,295,296,343.1,572,574	10/27/2016	/QV/
370	442	10/27/2016	/QV/
330	127,134,144	10/27/2016	/QV/

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

SEARCH NOTES		
Search Notes	Date	Examiner
EAST search	10/27/2016	/QV/
Inventor name search	10/27/2016	/QV/
Search updated	08/30/2017	/QV/
Search updated	04/09/2018	/QV/

INTERFERENCE SEARCH

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US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

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Apple EX1002 Page 364

Doc Code: DIST.E.FILE Document Description: Electronic Terminal Disclaimer - Filed	PTO/SB/26 U.S. Patent and Trademark Office Department of Commerce

Electronic Petition Request	**TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT**
Application Number	15080432
Filing Date	24-Mar-2016
First Named Inventor	Yannis Tsividis
Attorney Docket Number	10037P007CC2
Title of Invention	Power Dissipation Reduction in Wireless Transceivers

☒ Filing of terminal disclaimer does not obviate requirement for response under 37 CFR 1.111 to outstanding Office Action

☒ This electronic Terminal Disclaimer is not being used for a Joint Research Agreement.

Owner	Percent Interest
Theta IP, LLC	100%

The owner(s) with percent interest listed above in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of prior patent number(s)

9838962

as the term of said prior patent is presently shortened by any terminal disclaimer. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the prior patent are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the owner does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the prior patent, "as the term of said prior patent is presently shortened by any terminal disclaimer," in the event that said prior patent later:
- expires for failure to pay a maintenance fee;
- is held unenforceable;
- is found invalid by a court of competent jurisdiction;
- is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
- has all claims canceled by a reexamination certificate;
- is reissued; or
- is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

◉ Terminal disclaimer fee under 37 CFR 1.20(d) is included with Electronic Terminal Disclaimer request.

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Apple EX1002 Page 365

○	I certify, in accordance with 37 CFR 1.4(d)(4), that the terminal disclaimer fee under 37 CFR 1.20(d) required for this terminal disclaimer has already been paid in the above-identified application.

Applicant claims the following fee status:

- (◉) Small Entity
- (○) Micro Entity
- (○) Regular Undiscounted

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

THIS PORTION MUST BE COMPLETED BY THE SIGNATORY OR SIGNATORIES

I certify, in accordance with 37 CFR 1.4(d)(4) that I am:

- (◉) An attorney or agent registered to practice before the Patent and Trademark Office who is of record in this application

  Registration Number 25831

- (○) A sole inventor
- (○) A joint inventor; I certify that I am authorized to sign this submission on behalf of all of the inventors as evidenced by the power of attorney in the application
- (○) A joint inventor; all of whom are signing this request

Signature	/RWB/
Name	Roger W. Blakely Jr.

*Statement under 37 CFR 3.73(b) is required if terminal disclaimer is signed by the assignee (owner).
Form PTO/SB/96 may be used for making this certification. See MPEP § 324.

Electronic Patent Application Fee Transmittal

Application Number:	15080432
Filing Date:	24-Mar-2016
Title of Invention:	Power Dissipation Reduction in Wireless Transceivers
First Named Inventor/Applicant Name:	Yannis Tsividis
Filer:	Roger W. Blakely/Jessica Clark
Attorney Docket Number:	10037P007CC2

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
STATUTORY OR TERMINAL DISCLAIMER	2814	1	160	160
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**160**

Doc Code: DISQ.E.FILE
Document Description: Electronic Terminal Disclaimer – Approved

Application No.: 15080432

Filing Date: 24-Mar-2016

Applicant/Patent under Reexamination: Tsividis

Electronic Terminal Disclaimer filed on June 1, 2018

☒ APPROVED

This patent is subject to a terminal disclaimer

☐ DISAPPROVED

Approved/Disapproved by: Electronic Terminal Disclaimer automatically approved by EFS-Web

U.S. Patent and Trademark Office

Electronic Acknowledgement Receipt

EFS ID:	32778886
Application Number:	15080432
International Application Number:	
Confirmation Number:	6094
Title of Invention:	Power Dissipation Reduction in Wireless Transceivers
First Named Inventor/Applicant Name:	Yannis Tsividis
Customer Number:	8791
Filer:	Roger W. Blakely/Jessica Clark
Filer Authorized By:	Roger W. Blakely
Attorney Docket Number:	10037P007CC2
Receipt Date:	01-JUN-2018
Filing Date:	24-MAR-2016
Time Stamp:	13:28:23
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$160
RAM confirmation Number	060118INTEFSW00010565090528
Deposit Account	090528
Authorized User	Jessica Clark

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

37 CFR 1.16 (National application filing, search, and examination fees)

37 CFR 1.17 (Patent application and reexamination processing fees)

37 CFR 1.19 (Document supply fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Terminal Disclaimer-Filed (Electronic)	eTerminal-Disclaimer.pdf	33467 85c4abf359ee8ba8080944907ba48e9588edf4f6	no	2
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30670 1d837c8b35f28021b0ab185766c072f922b3c12c	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	64137		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application. No.	:	15/080,432	Confirmation No. 6094
Applicant	:	Yannis Tsividis	
Filed	:	03/24/2016	
TC/A.U.	:	2647	
Examiner	:	Vuong, Quochien B	
Docket No.	:	10037P007CC2	
Customer No.	:	8791	

Mail Stop Amendment
Commissioner for Patents
PO Box 1450
Alexandria VA 22313-1450

RESPONSE

Sir:

In the office action dated April 13, 2018, claims 19-26 of the present application are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-7 of U.S. Patent No. 9,838,962. In response, a terminal disclaimer is filed concurrently herewith.

It is believed that the application is now in condition for allowance and applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

WOMBLE BOND DICKINSON (US) LLP

Dated: 06/01/2018

By _____
Roger W. Blakely, Jr.
Reg. No. 25,831
Tel.: (714) 557-3800 (Pacific Coast)

P.O. Box 7037
Atlanta, Georgia 30357-0037

CERTIFICATE OF TRANSMISSION (37 CFR 1.8A)

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.

Date: 06/01/2018

Jessica A. Clark 6/1/2018
Jessica A. Clark *Date*

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application. No.	:	15/080,432	Confirmation No. 6094
Applicant	:	Yannis Tsividis	
Filed	:	03/24/2016	
TC/A.U.	:	2647	
Examiner	:	Vuong, Quochien B	
Docket No.	:	10037P007CC2	
Customer No.	:	8791	

Mail Stop Amendment
Commissioner for Patents
PO Box 1450
Alexandria VA 22313-1450

AUTHORIZATION FOR EXTENSION OF TIME, ALL REPLIES

Sir:

Authorization is given to treat any concurrent or future reply requiring a petition for an extension of time under 37 CFR §1.136(a) for its timely submission, as incorporating a petition for extension of time for the appropriate length of time. If any other petition is necessary for consideration of this paper, it is hereby so petitioned. Please charge any shortage in fees in connection with the filing of this paper, including extension of time fees, to Deposit Account 090528 and please credit any excess fees to such deposit account.

Respectfully submitted,

WOMBLE BOND DICKINSON (US) LLP

Dated: 06/01/2018

By _____
Roger W. Blakely, Jr.
Reg. No. 25,831
Tel.: (714) 557-3800 (Pacific Coast)

P.O. Box 7037
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Date: 06/01/2018

Jessica A. Clark *6/1/2018*
Jessica A. Clark *Date*

IPR2024-00817
Apple EX1002 Page 373

Electronic Acknowledgement Receipt

EFS ID:	32781135
Application Number:	15080432
International Application Number:	
Confirmation Number:	6094
Title of Invention:	Power Dissipation Reduction in Wireless Transceivers
First Named Inventor/Applicant Name:	Yannis Tsividis
Customer Number:	8791
Filer:	Roger W. Blakely/Jessica Clark
Filer Authorized By:	Roger W. Blakely
Attorney Docket Number:	10037P007CC2
Receipt Date:	01-JUN-2018
Filing Date:	24-MAR-2016
Time Stamp:	13:31:46
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		10037P007CC2_20180601_Response.pdf	66405 834ba8e1cbdde79ff475d6a8b024053094ffcd97	yes	2

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Authorization for Extension of Time all replies	2	2
Warnings:			
Information:			
	Total Files Size (in bytes):	66405	

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New Applications Under 35 U.S.C. 111

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National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

8791 7590 07/18/2018

WOMBLE BOND DICKINSON (US) LLP
Attn: IP Docketing
P.O. Box 7037
Atlanta, GA 30357-0037
UNITED STATES OF AMERICA

EXAMINER
VUONG, QUOCHIEN B

ART UNIT	PAPER NUMBER
2647	

DATE MAILED: 07/18/2018

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/080,432	03/24/2016	Yannis Tsividis	10037P007CC2	6094

TITLE OF INVENTION: Power Dissipation Reduction in Wireless Transceivers

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$500	$0	$0	$500	10/18/2018

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

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Apple EX1002 Page 376

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

8791 7590 07/18/2018
WOMBLE BOND DICKINSON (US) LLP
Attn: IP Docketing
P.O. Box 7037
Atlanta, GA 30357-0037
UNITED STATES OF AMERICA

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/080,432	03/24/2016	Yannis Tsividis	10037P007CC2	6094

TITLE OF INVENTION: Power Dissipation Reduction in Wireless Transceivers

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$500	$0	$0	$500	10/18/2018

EXAMINER	ART UNIT	CLASS-SUBCLASS
VUONG, QUOCHIEN B	2647	455-574000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ Applicant certifying micro entity status. See 37 CFR 1.29 — NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ❑ Applicant asserting small entity status. See 37 CFR 1.27 — NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ❑ Applicant changing to regular undiscounted fee status. — NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/080,432	03/24/2016	Yannis Tsividis	10037P007CC2	6094

8791 7590 07/18/2018

WOMBLE BOND DICKINSON (US) LLP
Attn: IP Docketing
P.O. Box 7037
Atlanta, GA 30357-0037
UNITED STATES OF AMERICA

EXAMINER	
VUONG, QUOCHIEN B	
ART UNIT	PAPER NUMBER
2647	

DATE MAILED: 07/18/2018

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

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Apple EX1002 Page 378

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 15/080,432	Applicant(s) TSIVIDIS, YANNIS	
	Examiner QUOCHIEN B. VUONG	Art Unit 2647	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *06/01/2018*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *19-26*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/QUOCHIEN B VUONG/
Primary Examiner, Art Unit 2647

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15080432	TSIVIDIS, YANNIS
	Examiner	**Art Unit**
	QUOCHIEN B VUONG	2647

CPC							
Symbol						**Type**	**Version**
H04W		52	/	0209		F	2013-01-01
H04B		1	/	109		I	2013-01-01
Y02D		70	/	40		A	2018-01-01
Y02D		70	/	142		A	2018-01-01
Y02D		70	/	00		A	2018-01-01
			/				
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			/				
			/				
			/				

CPC Combination Sets							
Symbol					**Type**	**Set**	**Ranking**	**Version**
			/					
			/					

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	8	
/QUOCHIEN B VUONG/ Primary Examiner.Art Unit 2647		O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15080432	TSIVIDIS, YANNIS
	Examiner	**Art Unit**
	QUOCHIEN B VUONG	2647

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION	
CLASS	SUBCLASS	CLAIMED	NON-CLAIMED
455	574	H 0 4 B 1 / 38 (2015.01.01)	
		H 0 4 M 1 / 00 (2006.01.01)	

CROSS REFERENCE(S)					
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
455	234.1	251.1	343.1		

NONE (Assistant Examiner) (Date)	**Total Claims Allowed:** 8
/QUOCHIEN B VUONG/ Primary Examiner.Art Unit 2647 (Primary Examiner) (Date)	O.G. Print Claim(s): 1 O.G. Print Figure: 1

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15080432	TSIVIDIS, YANNIS
	Examiner	**Art Unit**
	QUOCHIEN B VUONG	2647

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☒ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		17												
	2		18												
	3	1	19												
	4	2	20												
	5	3	21												
	6	4	22												
	7	5	23												
	8	6	24												
	9	7	25												
	10	8	26												
	11														
	12														
	13														
	14														
	15														
	16														

NONE (Assistant Examiner) (Date)	**Total Claims Allowed:** 8	
/QUOCHIEN B VUONG/ Primary Examiner.Art Unit 2647 (Primary Examiner) (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 1

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	968	(RSSI (signal adj2 (strength level quality))) same ((chang$3 varr$4 adjsut$3 increas$3) with (bias near4 current))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/07/02 15:44
L2	159	1 same impedance	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/07/02 15:48
L3	38318	455/63.1,67.13,127.1,127.2,127.5,226.1,226.2,232.1,234.1,250.1,251.1,295,296,311,343.1,572,574.ccls. 370/442.ccls. 330/127,134,144.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/07/02 16:26
L4	14	2 and 3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/07/02 16:35
L5	67	2 and ((lower low reduce$3) near4 (power battery))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/07/02 17:38
L6	1290	(RSSI (signal adj2 (strength level quality))) same ((chang$3 varr$4 adjust$3 increas$3) with (bias near4 current))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/07/02 17:49
L7	189	6 same impedance	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/07/02 17:50
L8	14	7 and 3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/07/02 17:58

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L9	0	((RSSI (signal adj2 (strength level quality))) with ((chang$3 varr$4 adjust$3 increas$3) with (bias near4 current)) with impedance with((lower low reduce$3) near4 (power battery))).clm.	US-PGPUB; USPAT	OR	ON	2018/07/02 18:12

7/2/2018 6:28:41 PM

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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15080432	TSIVIDIS, YANNIS
	Examiner	**Art Unit**
	QUOCHIEN B VUONG	2647

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	10/28/2016	09/01/2017	04/10/2018	07/02/2018					
	1	✓	✓	-	-					
	2	✓	✓	-	-					
	3	✓	✓	-	-					
	4	✓	✓	-	-					
	5	✓	✓	-	-					
	6	✓	✓	-	-					
	7	✓	✓	-	-					
	8	✓	✓	-	-					
	9	✓	✓	-	-					
	10	✓	✓	-	-					
	11	✓	✓	-	-					
	12	✓	✓	-	-					
	13	✓	✓	-	-					
	14	✓	✓	-	-					
	15	✓	✓	-	-					
	16	✓	✓	-	-					
	17	✓	✓	-	-					
	18	✓	✓	-	-					
1	19			✓	=					
2	20			✓	=					
3	21			✓	=					
4	22			✓	=					
5	23			✓	=					
6	24			✓	=					
7	25			✓	=					
8	26			✓	=					

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15080432	TSIVIDIS, YANNIS
	Examiner	Art Unit
	QUOCHIEN B VUONG	2647

CPC- SEARCHED		
Symbol	Date	Examiner
H04B 1/04, 1/16, 1/40, 1/109, 1/0457, 1/1607, 17/309, 17/318, 17/336,17/345, 2001/045, 2001/0416	10/27/2016	/QV/
H04W 52/52, 52/0261, 88/02	10/27/2016	/QV/
H03G 3/004, 3/20	10/27/2016	/QV/

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
455	63.1,67.13,127.1,127.2,127.5,226.1,226.2,232.1,234.1,250.1,251.1,295,296,343.1,572,574	10/27/2016	/QV/
370	442	10/27/2016	/QV/
330	127,134,144	10/27/2016	/QV/

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

SEARCH NOTES		
Search Notes	Date	Examiner
EAST search	10/27/2016	/QV/
Inventor name search	10/27/2016	/QV/
Search updated	08/30/2017	/QV/
Search updated	04/09/2018	/QV/
Search updated	07/02/2018	/QV/

INTERFERENCE SEARCH

IPR2024-00817
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US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
455	234.1,251.1,343.1,574	07/02/2018	/QV/

IPR2024-00817

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Substitute for form 1449A/PTO	*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	15/080,432
	Filing Date	Mar 24, 2016
	First Named Inventor	Yannis Tsividis
	Group Art Unit	2647
	Examiner Name	Vuong, Quochien B
Sheet 1 of 1	Attorney Docket No: 10037P007CC2	

US PATENT DOCUMENTS					
Examiner Initial *	**Cite No [1]**	**USP Document Number**	**Publication or Issue Date YYYY-MM-DD**	**Name of Patentee or Applicant of cited Document**	**Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear**
		US-5854973	1998-12-29	Holtvoeth, Knud	
		US-7190935	2007-03-13	Hecht, James B.	

EXAMINER **DATE CONSIDERED**

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449) as modified by BSTZ 03/26/07

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional) [2] Applicant is to place a check mark here if English language Translation is attached

Electronic Patent Application Fee Transmittal

Application Number:	15080432
Filing Date:	24-Mar-2016
Title of Invention:	Power Dissipation Reduction in Wireless Transceivers
First Named Inventor/Applicant Name:	Yannis Tsividis
Filer:	Tri Cao Dang/Jessica Clark
Attorney Docket Number:	10037P007CC2

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
SUBMISSION- INFORMATION DISCLOSURE STMT	2806	1	120	120
		Total in USD ($)		**120**

Electronic Acknowledgement Receipt

EFS ID:	33924072
Application Number:	15080432
International Application Number:	
Confirmation Number:	6094
Title of Invention:	Power Dissipation Reduction in Wireless Transceivers
First Named Inventor/Applicant Name:	Yannis Tsividis
Customer Number:	8791
Filer:	Tri Cao Dang/Jessica Clark
Filer Authorized By:	Tri Cao Dang
Attorney Docket Number:	10037P007CC2
Receipt Date:	04-OCT-2018
Filing Date:	24-MAR-2016
Time Stamp:	18:36:23
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$120
RAM confirmation Number	100518INTEFSW00005232090528
Deposit Account	090528
Authorized User	Jessica Clark

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

37 CFR 1.16 (National application filing, search, and examination fees)

37 CFR 1.17 (Patent application and reexamination processing fees)

37 CFR 1.19 (Document supply fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	10037P007CC2_20181004_IDS Letter.pdf	154405 ab97179b317952b8ba98cbdf98df713a5c3a3f9c	no	1
Warnings:					
Information:					
2	Information Disclosure Statement (IDS) Form (SB08)	10037P007CC2_20181004_IDS.pdf	163911 df56482ded3a02f018e8a3a057e1b1cdedb1e47a	no	1
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
3	Fee Worksheet (SB06)	fee-info.pdf	30586 ebaf5146f29465a2b77f04d41be88f60ddeed995	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	348902		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application No.	15/080,432
Filing Date	March 24, 2016
First Inventor	Yannis Tsividis
Art Unit	2647
Examiner Name	Vuong, Quochien B
Attorney Docket No.	10037P007CC2 Conf. No. 6094

DUTY OF DISCLOSURE STATEMENT

In accordance with the duty of disclosure, enclosed is a copy of an Information Disclosure Statement (IDS) Citation Form PTO/SB/08 or PTO-1449, together with copies of the documents cited on that form, except for copies not required to be submitted (e.g., copies of U.S. patents and U.S. published patent applications need not be enclosed). This IDS and IDS Citation Form are being submitted before payment of the Issue Fee. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

The submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☒ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

OR

☐ None

☒ The IDS Filing Fee in the amount of $120.00 as set forth in 37 CFR 1.17(p) has been submitted herewith.

☒ It is requested that any requisite fees be debited from Deposit Account 090528.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of signature.

Signature	/ Tri C. Dang /	Date (MM-DD-YYYY)	10-04-2018
Name/Print	Tri C. Dang	Registration Number	71853

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.

Jessica A. Clark /Jessica A. Clark/ *Date* *10-04-18*

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

8791 7590 07/18/2018
WOMBLE BOND DICKINSON (US) LLP
Attn: IP Docketing
P.O. Box 7037
Atlanta, GA 30357-0037
UNITED STATES OF AMERICA

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Transmission
I hereby certify that this correspondence is being EFS Web transmitted to the USPTO on the date shown below.

Jessica A. Clark	(Depositor's name)
/Jessica A. Clark/	(Signature)
10/05/2018	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/080,432	03/24/2016	Yannis Tsividis	10037P007CC2	6094

TITLE OF INVENTION: Power Dissipation Reduction in Wireless Transceivers

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$500	$0	$0	$500	10/18/2018

EXAMINER	ART UNIT	CLASS-SUBCLASS
VUONG, QUOCHIEN B	2647	455-574000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Womble Bond Dickinson (US) LLP
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Theta IP, LLC

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Coppell, Texas

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
- ☒ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☒ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number 090528 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ☐ Applicant certifying micro entity status. See 37 CFR 1.29 — NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ☐ Applicant asserting small entity status. See 37 CFR 1.27 — NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ☐ Applicant changing to regular undiscounted fee status. — NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature / Tri C. Dang / Date 10/5/2018

Typed or printed name Tri C. Dang Registration No. 71853

IPR2024-00817
Apple EX1002 Page 394

Electronic Patent Application Fee Transmittal

Application Number:	15080432
Filing Date:	24-Mar-2016
Title of Invention:	Power Dissipation Reduction in Wireless Transceivers
First Named Inventor/Applicant Name:	Yannis Tsividis
Filer:	Tri Cao Dang/Jessica Clark
Attorney Docket Number:	10037P007CC2

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	2501	1	500	500

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**500**

Electronic Acknowledgement Receipt

EFS ID:	33935521
Application Number:	15080432
International Application Number:	
Confirmation Number:	6094
Title of Invention:	Power Dissipation Reduction in Wireless Transceivers
First Named Inventor/Applicant Name:	Yannis Tsividis
Customer Number:	8791
Filer:	Tri Cao Dang/Jessica Clark
Filer Authorized By:	Tri Cao Dang
Attorney Docket Number:	10037P007CC2
Receipt Date:	05-OCT-2018
Filing Date:	24-MAR-2016
Time Stamp:	17:17:46
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$500
RAM confirmation Number	100918INTEFSW00004316090528
Deposit Account	090528
Authorized User	Jessica Clark

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

37 CFR 1.16 (National application filing, search, and examination fees)

37 CFR 1.17 (Patent application and reexamination processing fees)

37 CFR 1.19 (Document supply fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	10037P007CC2_20181005_IssueFeeTrans.pdf	254979 08fce6afefac514707d7fc81d70d7c59d3b6bf87	no	1
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30247 b7b5404d37f39ecfaf7842a6abfcc59c3aee2fee	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	285226		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/080,432	03/24/2016	Yannis Tsividis	10037P007CC2	6094

8791 7590 10/15/2018

WOMBLE BOND DICKINSON (US) LLP
Attn: IP Docketing
P.O. Box 7037
Atlanta, GA 30357-0037

EXAMINER	
VUONG, QUOCHIEN B	

ART UNIT	PAPER NUMBER
2647	

NOTIFICATION DATE	DELIVERY MODE
10/15/2018	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

FIP_Group@bstz.com
PTO.MAIL@BSTZ.COM
PTO.MAIL@BSTZPTO.COM

Corrected ***Notice of Allowability***	**Application No.** 15/080,432	**Applicant(s)** Tsividis, Yannis	
	Examiner QUOCHIEN B VUONG	**Art Unit** 2647	**AIA Status** No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to 10/04/2018.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 19-26 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file areply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☑ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/QUOCHIEN B VUONG/
Primary Examiner, Art Unit 2647

Substitute for form 1449A/PTO	*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	15/080,432
	Filing Date	Mar 24, 2016
	First Named Inventor	Yannis Tsividis
	Group Art Unit	2647
	Examiner Name	Vuong, Quochien B
Sheet 1 of 1	Attorney Docket No: 10037P007CC2	

US PATENT DOCUMENTS					
Examiner Initial *	**Cite No [1]**	**USP Document Number**	**Publication or Issue Date YYYY-MM-DD**	**Name of Patentee or Applicant of cited Document**	**Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear**
/Q.B.V/		US-5854973	1998-12-29	Holtvoeth, Knud	
/Q.B.V/		US-7190935	2007-03-13	Hecht, James B.	

EXAMINER /QUOCHIEN B VUONG/ **DATE CONSIDERED** 10/10/2018

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449) as modified by BSTZ 03/26/07

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/080,432	11/13/2018	10129825	10037P007CC2	6094

8791 7590 10/24/2018

WOMBLE BOND DICKINSON (US) LLP
Attn: IP Docketing
P.O. Box 7037
Atlanta, GA 30357-0037

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Yannis Tsividis, New York, NY;
Theta IP, LLC, Coppell, TX;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court for the Western District of Texas, Waco Division on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
	2/28/2020	for the Western District of Texas, Waco Division

PLAINTIFF	DEFENDANT
Theta IP, LLC	Samsung Electronics Co., Ltd.; Samsung Electronics America, Inc.; Samsung Telecommunications America, LLC

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	9,838,962	12/5/2017	Theta IP, LLC
2	10,129,825	11/13/2018	Theta IP, LLC
3	10,524,202	12/31/2019	Theta IP, LLC
4			
5			

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director **Copy 3—Upon termination of action, mail this copy to Director**
Copy 2—Upon filing document adding patent(s), mail this copy to Director **Copy 4—Case file copy**

Print Save As...

AO 120 (Rev. 08/10)

TO:	Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Northern District of Illinois/Eastern Division on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
22cv3441	06/30/2022	Northern District of Illinois/Eastern Division

PLAINTIFF	DEFENDANT
Theta IP, LLC	Motorola Mobility LLC, Lenovo (United States) Inc., Lenovo Group Limited

PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 See Attached		
2		
3		
4		
5		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE
Thomas G. Bruton	David Jozwiak	07/05/2022

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

Case: 1:22-cv-03441 Document #: 1-1 Filed: 07/05/22 Page 16 of 626 PageID #:181

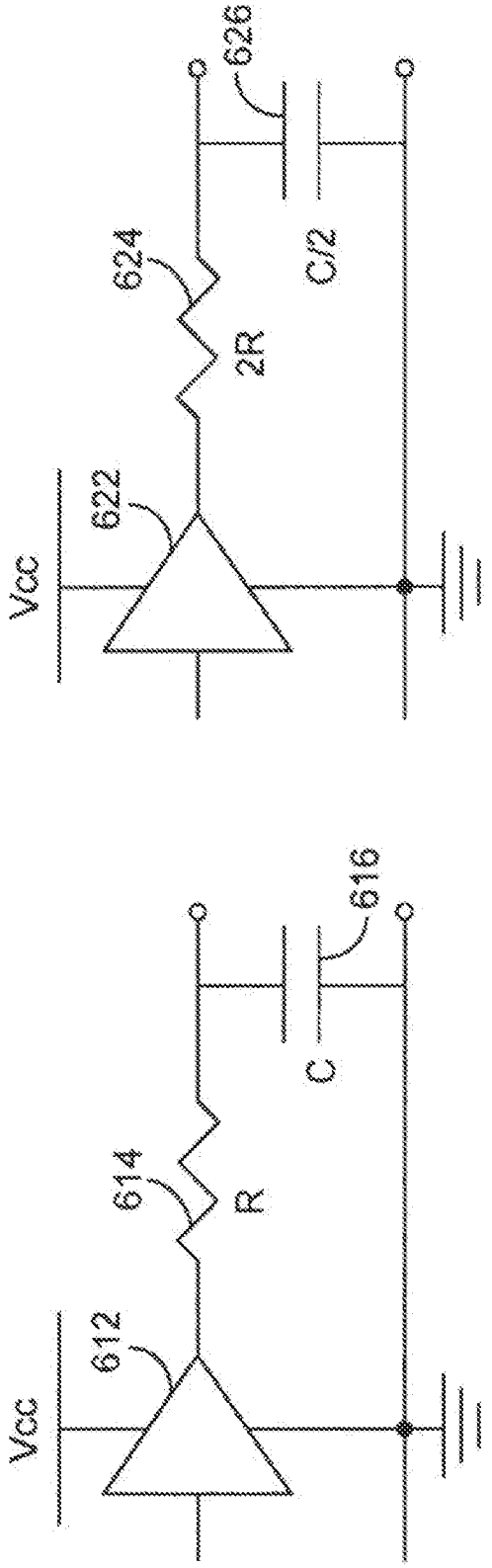
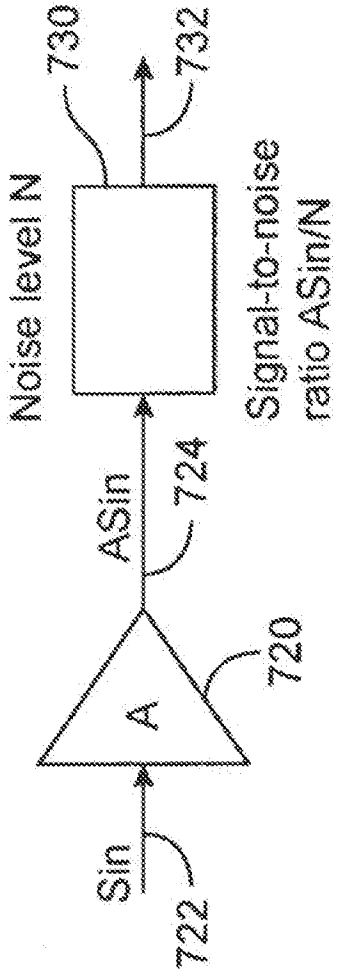


FIG. 6


730
732
Noise level N
Signal-to-noise ratio ASin/N
ASin
724
720
A
Sin
722

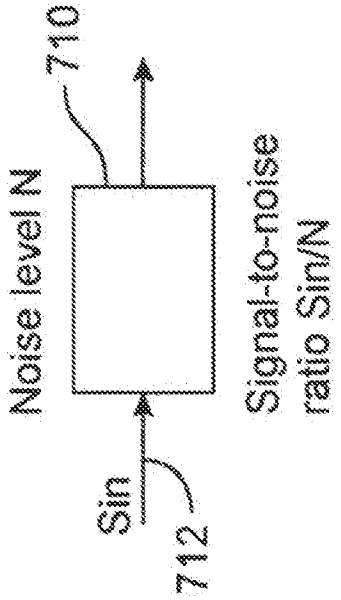

710
Noise level N
Signal-to-noise ratio Sin/N
Sin
712

FIG. 7

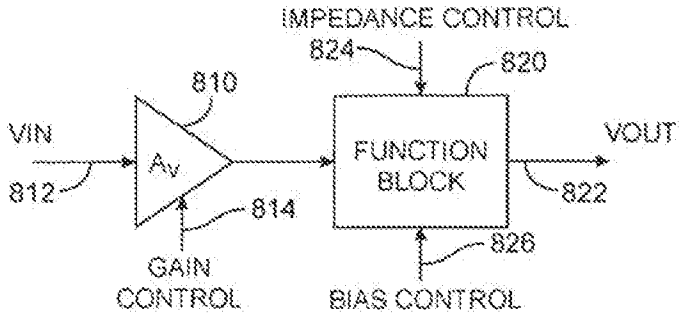


FIG. 8A

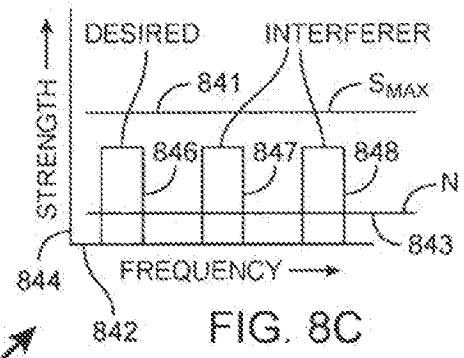


FIG. 8C

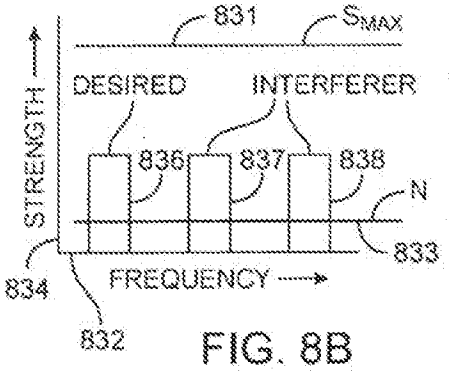


FIG. 8B

DECREASE BIASING

–AND/OR–

INCREASE GAIN AND IMPEDANCES

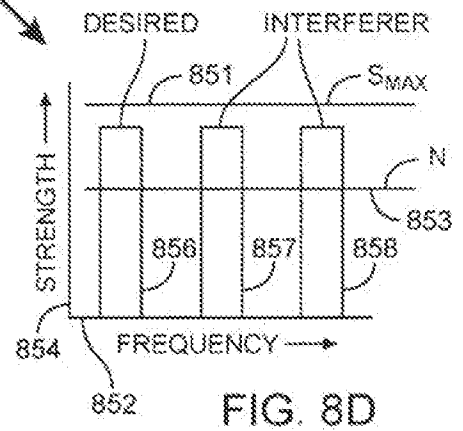


FIG. 8D

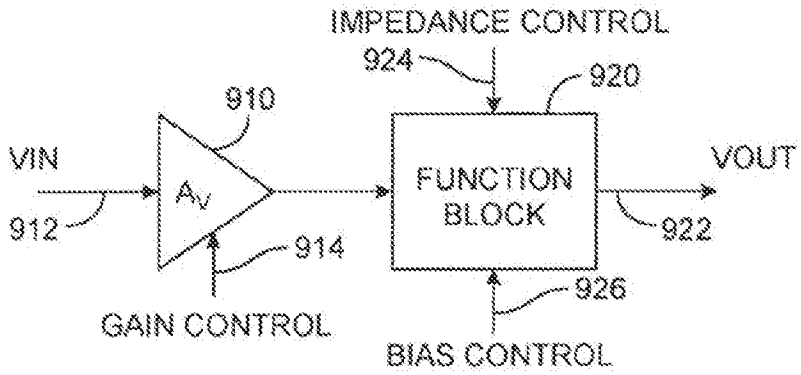


FIG. 9A

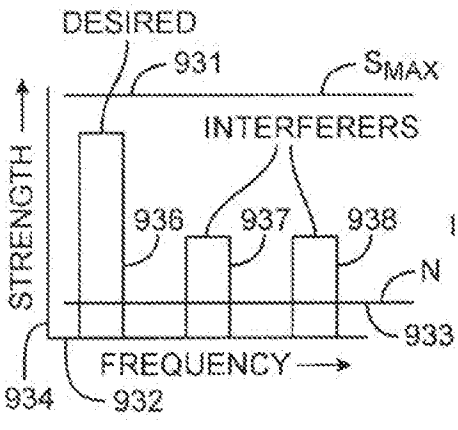


FIG. 9B

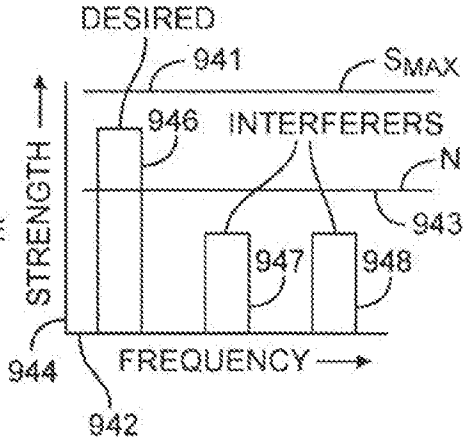


FIG. 9C

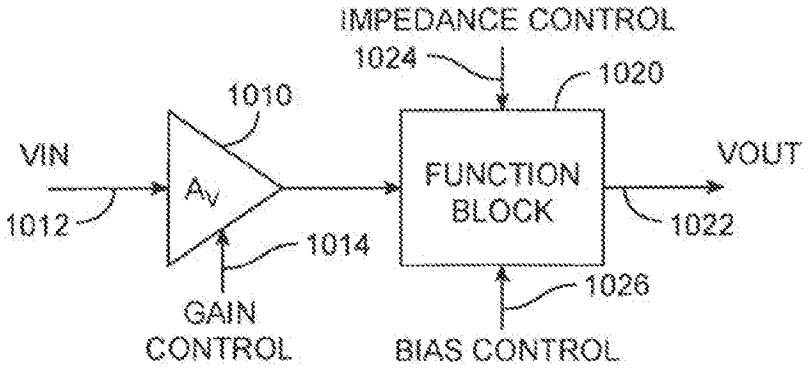


FIG. 10A

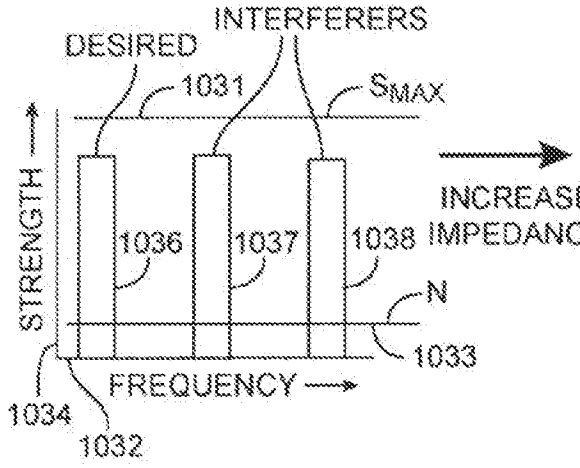


FIG. 10B

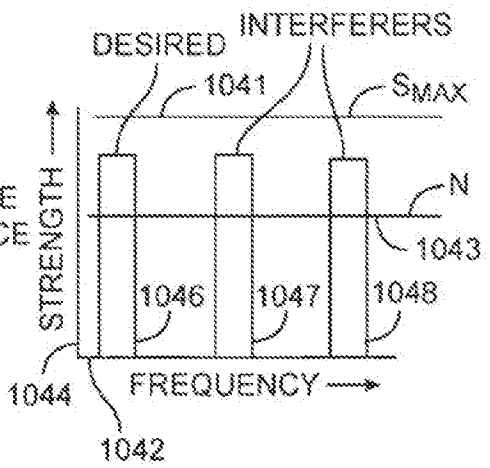


FIG. 10C

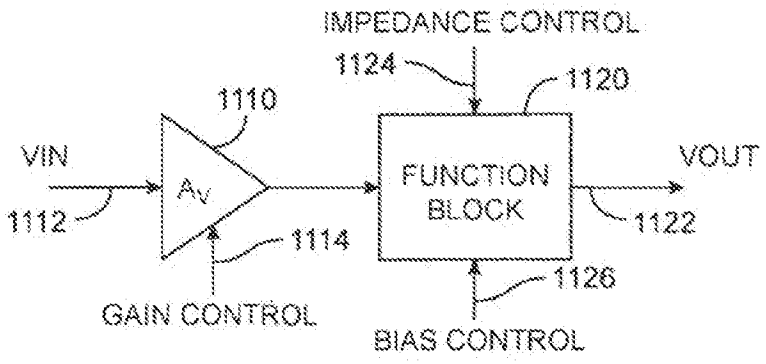


FIG. 11A

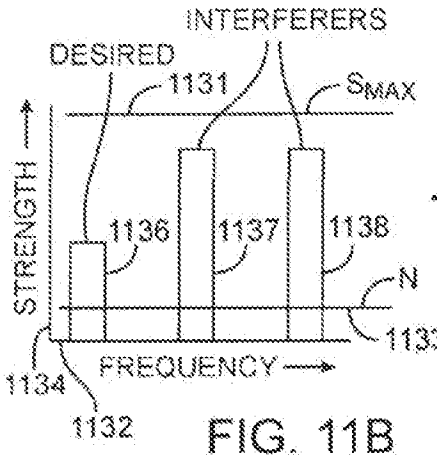


FIG. 11B

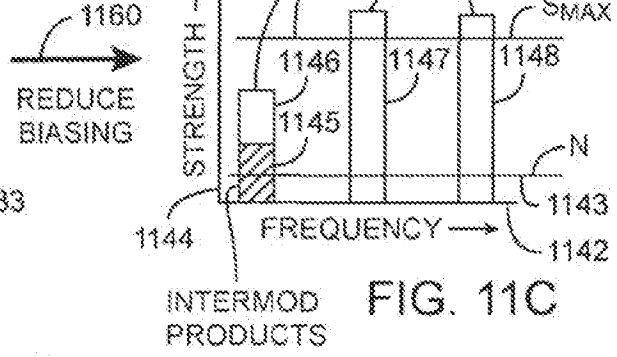


FIG. 11C

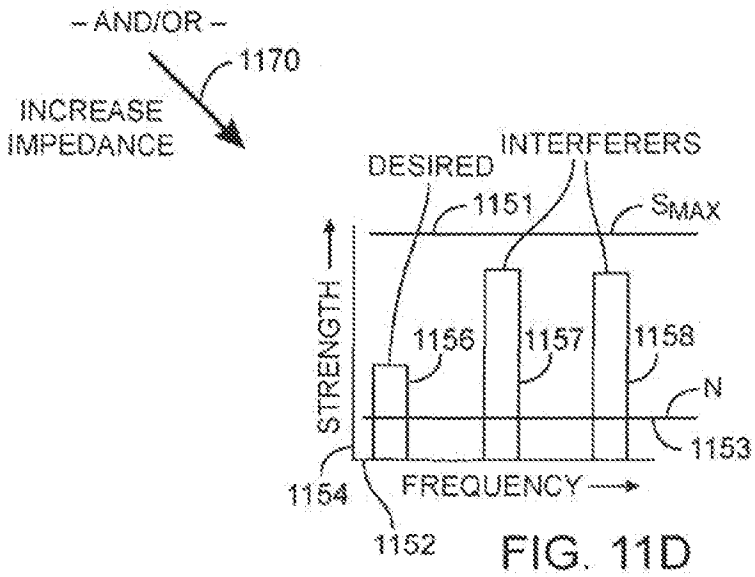


FIG. 11D

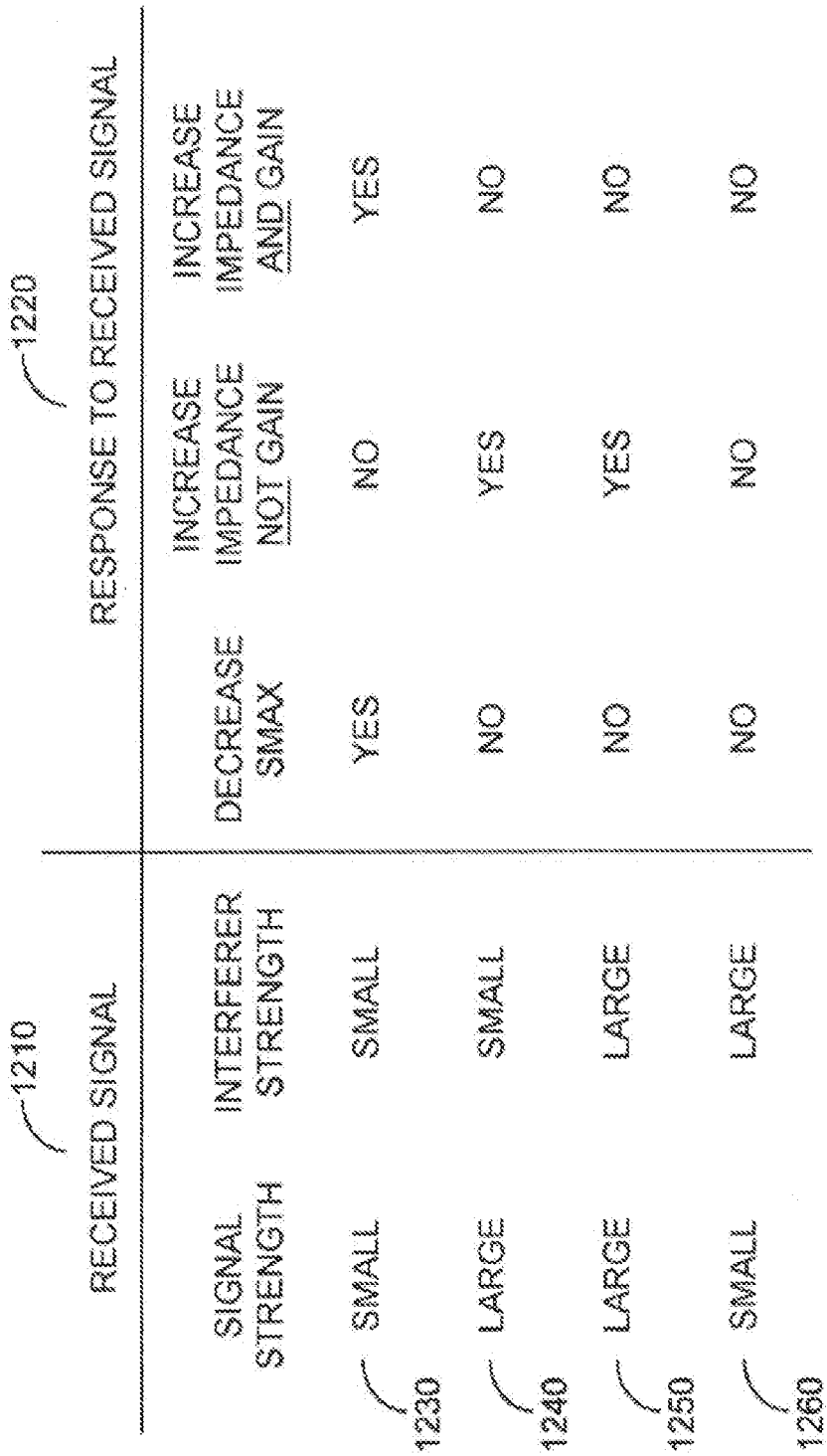

1210
RECEIVED SIGNAL
1220
RESPONSE TO RECEIVED SIGNAL
SIGNAL STRENGTH
INTERFERER STRENGTH
DECREASE SMAX
INCREASE IMPEDANCE NOT GAIN
INCREASE IMPEDANCE AND GAIN
SMALL
SMALL
YES
NO
YES
1230
LARGE
SMALL
NO
YES
NO
1240
LARGE
LARGE
NO
YES
NO
1250
SMALL
LARGE
NO
NO
NO
1260

FIG. 12

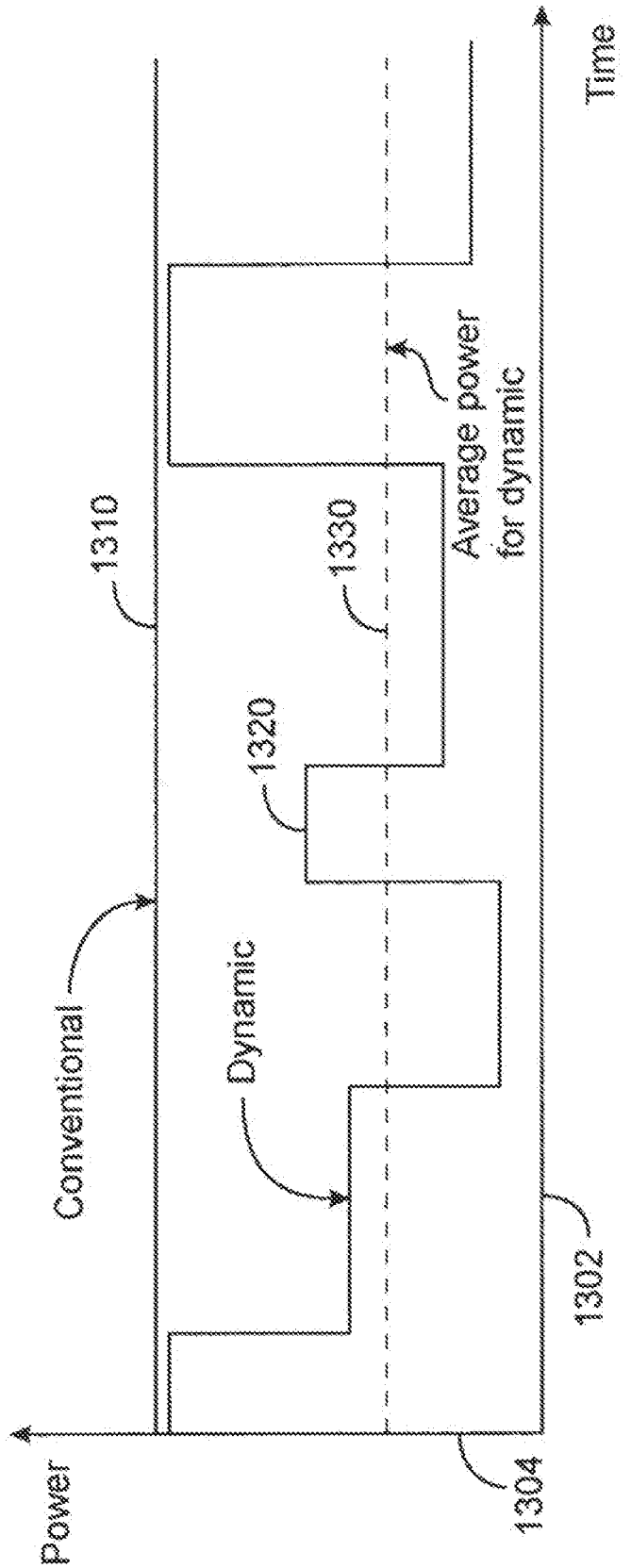

Time
Power
Conventional
Dynamic
Average power
for dynamic
1310
1320
1330
1302
1304

FIG. 13

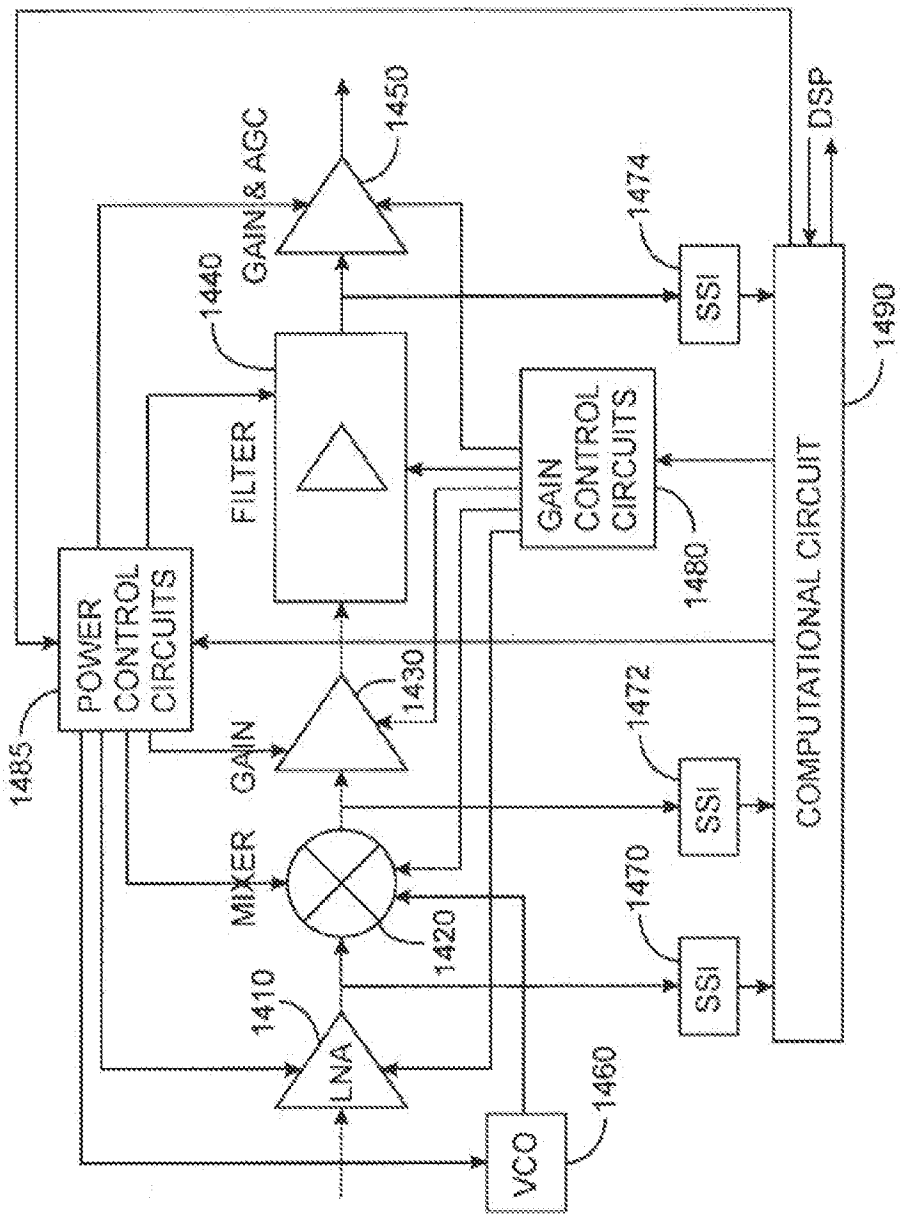

1450
GAIN & AGC
1440
FILTER
1474
SSI
DSP
1490
COMPUTATIONAL CIRCUIT
GAIN CONTROL CIRCUITS
1480
POWER CONTROL CIRCUITS
1485
1430
GAIN
1472
SSI
MIXER
1420
1470
SSI
1410
LNA
VCO
1460

FIG. 14

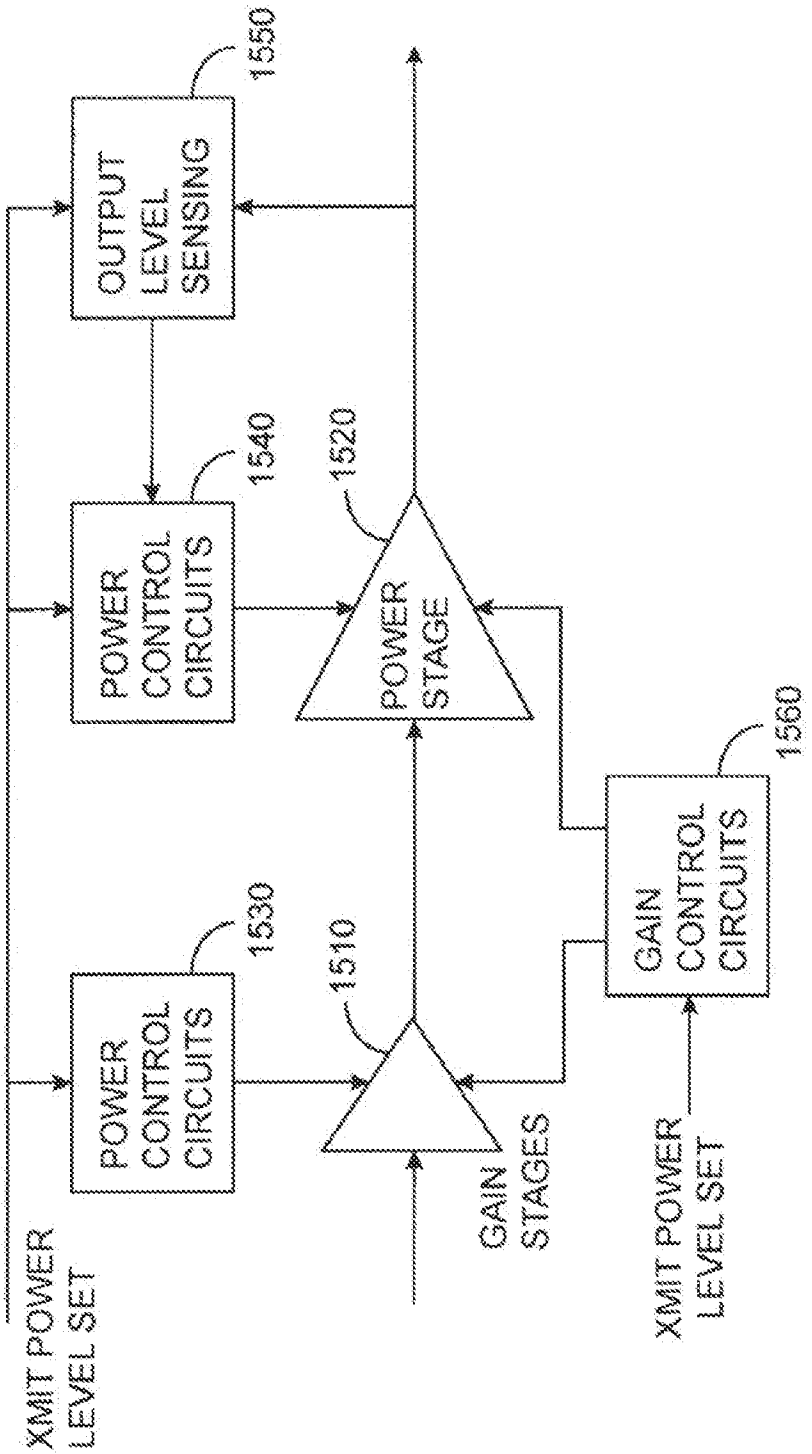

XMIT POWER LEVEL SET
POWER CONTROL CIRCUITS
1530
1510
GAIN STAGES
POWER CONTROL CIRCUITS
1540
1520
POWER STAGE
OUTPUT LEVEL SENSING
1550
XMIT POWER LEVEL SET
GAIN CONTROL CIRCUITS
1560

FIG. 15

Exhibit A

POWER DISSIPATION REDUCTION IN WIRELESS TRANSCEIVERS

CROSS-REFERENCES TO RELATED APPLICATIONS

This application claims the benefit of U.S. provisional application No. 60/451,229, filed Mar. 1, 2003, which is incorporated by reference.

This application is related to U.S. provisional application No. 60/451,230, filed Mar. 1, 2003, which is incorporated by reference.

BACKGROUND

The present invention relates to power dissipation reduction techniques for electronic circuits, for example wireless transceiver integrated circuits.

Wireless networking is quickly becoming ubiquitous, as desktop, notebook, and handheld computers are connected to share Internet access and files. Wireless networking cards compatible with PCMCIA and compact flash form factors are popular for laptops and handhelds respectively, particularly as mobile users connect to the Internet on the road at coffee shops, hotels, and airports.

A downside of this connectivity is a corresponding drain on battery life, especially for these portable devices. The power consumed by a wireless transmitter and receiver reduces the usefulness of a device and sends a user on a hunt for an electrical outlet for recharging.

One reason why this power drain is high is that electronic circuits are typically designed to function properly under worst-case operating conditions. For a wireless transceiver, the worst case condition is when a desired signal reception strength is low, while other transceivers or nearby electronic equipment generate interfering signals and other spurious noise.

But a wireless transceiver does not always operate in these worst-case conditions. For example, a base station, router or access point may be nearby such that the received signal is strong. Also, there may be no interfering signals, or they may be relatively weak. In these situations, receiver circuit currents can be reduced below what is necessary for the worst case condition. If this is done, power dissipation is reduced, and battery life is increased.

Thus, what is needed are circuits and methods that can adapt to a better-than-worst-case condition and reduce circuit currents and therefore power dissipation accordingly.

SUMMARY

Accordingly, embodiments of the present invention provide methods and circuits for reducing power dissipation in wireless transceivers and other electronic circuits and systems. Embodiments of the present invention use bias current reduction, impedance scaling, gain, and other dynamic changes either separately or in combination to reduce power dissipation in response to better-than-worst case conditions. For example, bias currents are reduced in response to a need for reduced signal handling capability, impedances are scaled thus reducing required drive and other bias currents in response to a strong received signal, or gain is varied and impedances are scaled in response to a low received signal in the presence of no or weak interfering signals. Alternately, currents may start low and be increased in response to worse-than-best-case conditions, or they may start at a point in between and vary up or down. These variations may be made to electronic systems generally, and are particularly suited and discussed below in the context of a wireless transceiver that may be used in networking devices, cellular telephones, and other wireless systems.

An exemplary embodiment of the present invention provides a method of receiving a signal using an integrated circuit. The integrated circuit includes a signal path having a low-noise amplifier configured to receive the signal, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer. The method itself includes determining a first signal strength at a first node in the signal path in the integrated circuit and dynamically changing an impedance of a component in the signal path based on the first signal strength.

A further exemplary embodiment of the present invention provides a method of receiving a signal using an integrated circuit. The integrated circuit includes a signal path having a low-noise amplifier configured to receive the signal, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer. The method itself includes determining a first signal strength at a first node in the signal path in the integrated circuit and dynamically changing a bias current in the signal path based on the first signal strength.

Another exemplary embodiment of the present invention provides a method of receiving a signal using an integrated circuit. The integrated circuit includes a signal path having a first circuit and a second circuit having an input coupled to an output of the first circuit. The method itself includes determining a first signal strength at a first node in the signal path in the integrated circuit. The first node is before the first circuit in the signal path. The method further includes dynamically changing a gain of the first circuit based on the first signal strength and dynamically changing an impedance of a component in the second circuit based on the first signal strength.

Still a further exemplary embodiment of the present invention provides a wireless transceiver integrated circuit including a receiver having a signal path, the signal path including a low-noise amplifier, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer, as well as a first signal strength indicator circuit coupled to the signal path and configured to determine a first signal strength. An impedance in the signal path is configured to be dynamically adjusted in response to the first signal strength.

Yet a further exemplary embodiment of the present invention provides a wireless transceiver integrated circuit. This integrated circuit includes a receiver comprising a signal path, the signal path having a low-noise amplifier, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer, as well as a first signal strength indicator circuit coupled to the signal path, and configured to determine a first signal strength. A bias current in the signal path is configured to be dynamically adjusted in response to the first signal strength.

Another exemplary embodiment of the present invention provides a wireless transceiver integrated circuit. This circuit includes a receiver comprising a signal path, the signal path having a first circuit; and a second circuit having an input coupled to an output of the first circuit; as well as a first signal strength indicator circuit coupled to the signal path, and configured to determine a first signal strength. A gain of the first circuit is configured to be dynamically adjusted in

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response to the first signal strength, and an impedance in the second circuit is configured to be dynamically adjusted in response to the first signal strength.

A better understanding of the nature and advantages of the present invention may be gained with reference to the following detailed description and the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram of a wireless transceiver that may benefit by incorporation of embodiments of the present invention;

FIGS. **2**A and **2**B illustrate examples of desired and interfering signals and noise that may be received by a circuit in a wireless receiver;

FIG. **3** illustrates what can occur as a maximum signal handling capability is reduced in the worst-case signal condition;

FIG. **4** illustrates a portion of a receiver consistent with an embodiment of the present invention;

FIG. **5** illustrates the relationship between a required bias current and a given output signal for a representative circuit;

FIG. **6** is an example of how a circuit's impedances may be scaled to reduce drive currents, and depending on the circuit configuration used, to reduce associated bias currents as well;

FIG. **7** illustrates how gain may be inserted in a signal path to improve a circuit's signal to noise ratio;

FIGS. **8**A–**8**D illustrate some of the possible power saving techniques that may be used when received desired and interferer signals are all at a low power level;

FIGS. **9**A–**9**C illustrate one of the possible power saving techniques that may be used when a received desired signal is strong while all interfering signals are at a low power level;

FIGS. **10**A–**10**C illustrate one of the possible power saving techniques that may be used when received desired and interferer signals are all at a high power level;

FIGS. **11**A–**11**D illustrate one of the possible power saving techniques that may be used when a received desired signal is weak while one or more interfering signals are strong;

FIG. **12** is a summary illustrating four different input conditions and some of the appropriate power-saving changes that may be made in response to those conditions;

FIG. **13** shows how power may be saved as a function of time by employing one or more of the power saving methods consistent with embodiments of the present invention;

FIG. **14** is a block diagram of a portion of a receiver consistent with an embodiment of the present invention; and

FIG. **15** is a block diagram of a portion of a transmitter consistent with an embodiment of the present invention.

DESCRIPTION OF EXEMPLARY EMBODIMENTS

FIG. **1** is a block diagram of a wireless transceiver that may benefit by incorporation of embodiments of the present invention. This wireless transceiver may be designed to send and receive signals consistent with the IEEE 802.11a, 802.11b, 802.11 g, or other signaling standard or combination of standards. This figure, as with all the included figures, is shown for illustrative purposes only and does not to limit either the possible embodiments of the present invention or the claims.

There are three main portions of this transceiver circuit, a receiver, transmitter, and synthesizer. This transceiver may be completely or partially integrated on a semiconductor chip, or it may be integrated onto multiple integrated circuits. In a specific embodiment, the circuitry bounded by dashed line **100** is integrated on a single chip coupled to one or more external components or circuits. The integrated circuit or circuits forming this wireless transceiver may incorporate various integrated circuit devices such as a bipolar, CMOS, or BiCMOS devices made using a silicon, silicon-germanium (SiGe), gallium arsenide or other III-V process, or other manufacturing process. Embodiments of the present invention may also be applicable to circuits manufactured using nanotechnology processing.

The receiver includes a signal path formed by low-noise amplifier **102**, I and Q mixers **104** and **106**, low pass filters **108** and **110**, and baseband amplifiers **114** and **116**. Other circuitry in the receiver includes received strength indicator **122**, automatic gain control circuit **166**, baseband gain control circuit **120**, tuning circuit **112**, and offset cancellation circuit **118**.

The transmitter includes input up-converter mixers **124** and **126**, summing node **176**, which may be conceptual rather than an actual circuit, transmit variable gain amplifier **128**, and power amplifier **130**.

The synthesizer includes a voltage-controlled oscillator **148**, which drives I and Q buffers **154** and **152**, prescaler **156**, reference clock buffer **142** and divider **158**, phase-frequency detector **160**, charge pump **162**, and loop filter **146**, which in a specific embodiment is formed by external components.

Signals are received on an antenna, not shown, and typically pass through an RF switch and bandpass filter before being received by the low-noise amplifier **102** on line **101**. The low noise amplifier gains the received signal and provides it to quadrature mixers **104** and **106**. I and Q mixers **104** and **106** down-convert the received signal to baseband by multiplying them with quadrature versions of the oscillator signal provided by buffers **152** and **154**. This down conversion also produces a high frequency component at a frequency that is equal to the sum of the frequencies of the received signal and the VCO. This unwanted signal is filtered by low pass filters **108** and **110**, which in turn drive baseband amplifiers **114** and **116**. The outputs of baseband amplifiers **114** and **116** are typically converted to digital signals by analog-to-digital converters at the front end of a digital signal processing block.

In the transmit mode, I and Q versions of the signal to be transmitted are provided on lines **121** and **123** to up-convert mixers **124** and **126**. These up-convert mixers multiply the I and Q portions of the transmit signal by quadrature versions of the VCO signal provided by buffers **152** and **154**. The outputs of the up-convert mixers **124** and **126** are summed, and amplified by transmit VGA **128**, which in turn drives power amplifier **130**. The output of power amplifier **130** is typically filtered, and passes through the RF switch to the antenna for transmission.

A reference clock is received and buffered by the reference buffer **142**. The VCO generates quadrature oscillatory signals that are divided by prescaler **156**. The reference clock is typically generated by a crystal or other stable periodic clock source. The phase-frequency detector **116** compares the phase or frequency (depending on whether the synthesizer is tracking or acquiring the correct frequency) of the divided VCO signal and the reference clock, or a divided version of the reference clock, and generates an error signal, which drives the charge pump **162**. The output signal of the

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charge pump **162** is filtered by the loop filter **146**, which is commonly a lead-lag filter, and which provides a tuning or correction signal to the VCO **148**.

Embodiments of the present invention may be used to reduce the power dissipation of one or more of these included circuits. For example, the power dissipation in the low-noise amplifier **102**, down-convert mixers **104** and **106**, low pass filters **108** and **110**, or baseband amplifiers **114** and **116** may be optimized. Also, power dissipation in up-convert mixers **124** **126**, variable gain amplifier **128**, and power amplifier **130** may also be optimized. Similarly, VCO **148** and prescaler **156** currents may be adjusted. Embodiments of the present invention may also be applied in other circuits which may be included in other integrated circuit receivers, transmitters, transceivers, or other electronic circuits or systems.

When a receiver is actively receiving a desired signal, each block in the signal path has at its input the desired signal as well as noise and possibly interfering signals. The desired signal is the useful, information-carrying portion of a received signal. The noise may be thermal, shot, or other noise generated on the integrated circuit, in addition to received noise generated by sources external to the chip. The noise at the input of a block may be referred to as the equivalent input noise. The interfering signal or signals, or interferers, may be generated by similar transceivers, or other electrical equipment, circuits, or systems.

FIGS. **2**A and **2**B illustrate examples of desired signals, interferers, and noise that may be received by one of the various circuits in a wireless receiver. In each of these figures, the signal strength is plotted along a Y-axis **204** or **254** as a function of frequency along an X-axis **202** or **252**. In the example of FIG. **2**A, a received desired signal **206** is large in comparison to interfering signals **208** and **210**. In these examples, two interfering signals are shown for illustrative purposes, though there may be no such signals, one such signal, or more than two such signals in the frequency range of interest. Also, while for these examples the interferers are shown as being at a higher frequency than the desired signal, there may be one or more interferers at higher or lower frequencies as the desired signal. In this specific example, the acceptable noise floor **214** is relatively high, while maximum signal handling capability Smax **212** (that is the maximum signal power that can be handled with an acceptably low distortion) needs only to be high enough to accommodate the desired signal. For this specific example, the circuit receiving this input spectrum only requires a relatively small dynamic range for proper operation, that is the range between Smax **212** and the noise floor **214** is relatively small.

Conversely, in the example shown in FIG. **2**B, the desired signal **256** is relatively weak compared to the large interferers **258** and **260**. In this example, the noise floor **264** should be relatively low so as to prevent an unacceptable level of error in the recovery the desired signal **256**. The maximum signal handling capability Smax **262** should be relatively high to accommodate the large interferers in order to avoid the creation of intermodulation products as described below. Accordingly, in this specific example, the circuit receiving this input spectrum should have a large dynamic range, particularly in comparison to the example of FIG. **2**A.

It should be noted that the noise level or noise floors shown in these and the other included figures is the noise density integrated over the bandwidth of interest. For simplicity and comparison, this level is shown as a horizontal line, and is not meant to imply noise density.

Often in wireless receivers, a circuit at different times will receive an input spectrum similar to those shown in FIGS. **2**A and **2**B. The input spectrum of FIG. **2**B is generally considered the worst-case input signal, and typical design methodology involves designing a receiver for this condition, specifically the weakest desired signal accompanied by largest interference level. Circuit impedances and currents are set such that the noise floor **264** is sufficiently low for an acceptable bit-error rate, while bias currents are set sufficiently high for the required Smax **262**.

Conversely, the input spectrum in FIG. **2**A is that of the best-case input signal, specifically, a robust desired signal accompanied by no or low-level interferers. In this case, the noise floor **214** may be allowed to rise, while the maximum signal handling capability Smax **212** may be reduced. When this is done, the receiver circuit may save significant power. For example, the circuit's impedances may be increased, thus reducing required drive currents. Similarly, bias currents may be lowered, thus reducing the maximum signal in handling capability.

The minimum power dissipation for a circuit is proportional to the required maximum signal-to-noise ratio, which is the ratio between Smax **212** or **262** and N **214** and **264**. Thus, a circuit receiving an input similar to the one shown in FIG. **2**A can dissipate less power than one receiving the input as shown in FIG. **2**B, while still achieving an acceptable bit-error rate.

FIG. **3** illustrates what can occur when the maximum signal handling capability Smax **314** is reduced in the worst-case condition, that is when a weak desired signal **306** is accompanied by large interferers **310** and **312**. Again, signal strength is plotted along a Y-axis **304** as a function of frequency along X-axis **302**. In this specific example, Smax **314** is reduced below the peak levels of the interferers **310** and **312**. Since Smax is low, the circuit cannot handle the interferers linearly. The resulting nonlinearities lead to a mixing of the interferers and the creation of intermodulation products **308** (for example, a third-order intermodulation distortion, IM3), one of which in this example occurs at the same frequency as the desired signal **306**. As can be seen, if the intermodulation products **308** become excessive, the received signal bit error rate may become excessive, and the desired signal **306** may be lost. Accordingly, while Smax may be lowered even under some unfavorable conditions in order to reduce power, care should be taken to avoid corruption of the received desired signal.

FIG. **4** illustrates a portion of a receiver consistent with an embodiment of the present invention. Included is a filter **430**. An optional gain element **420** is placed in front of the filter **430** in order to increase signal levels. Signal strength indicator circuits **440** and **450** are connected to input line **410** and output line **460**. In this specific example, the input signal spectrum on line **410** is shown as desired signal **412** and interferers **414** and **416**. The signal spectrum at the output line **460** is shown as desired signal **462** and interferers **464** and **466**. The signal strength indicators **440** and **450** do not provide information as to the relative sizes of the desired and interfering signals. Rather, a cumulative signal level is provided at their outputs. For example, the first signal strength indicator **440** outputs a level corresponding to the sum of desired signal **412** and interfering signals **414** and **416**, while the second signal strength indicator **450** provides a signal level corresponding to the sum of desired signal **462** and interfering signals **464** and **466**. In this specific example, the gain of the gain and filter circuit combinations is shown as approximately one, while the interfering signals **414** and **416** signal levels are reduced.

A comparison of the signal levels provided by the signal strength indicators **440** and **450** indicates that much of the combined received signal on line **410** has been filtered. Accordingly, it may be deduced that large interfering signals present at the input are being filtered by the filter **430**. From this information, as will be shown in greater detail below, the bias, impedance, and gain of the gain stage **420** and filter **430** combination may be optimized to reduce power dissipation.

There are several real world situations where the received signal is better than the worst-case condition such that power can be saved. For example, large interferers may be present only part of the time, that is, on a temporary or transient basis. The interfering equipment may be some distance from the transceiver, or it may be operating in the low power mode. Also, the desired signal may be very strong as compared to the noise and interferers, for example a hub, router, or access point may be nearby.

Some transceivers consistent with embodiments of the present invention are designed to work with more than one data transfer specification or standard. In this case, when a transceiver is operating in a mode having a lower data rate, the power saving techniques described here may be employed.

FIG. **5** illustrates the relationship between a required biased current **516** for a given output signal **514** for a representative circuit **510**. If the output signal current level is relatively low, such as the output current shown as **526**, the corresponding bias current **528** may be low. Conversely, if the output signal current level is larger as with the example **536**, the corresponding bias current level **538** should also be high. Accordingly, if a bias current is initially set high to handle large a large input signal, for example a large interferer, this current may be reduced if the input signal is smaller.

There are many ways by which these bias currents can be reduced. For example, the current may be generated by placing a voltage across a resistor by applying a bias voltage to the base of a device whose emitter is connected to ground through a resistance. In this case, the resistor may be increased by opening switches across portions of the resistance, or lowering the bias voltage applied at the base. Several ways in which this may be done will be readily understood by one skilled in the art.

FIG. **6** is an example of how a circuit's impedances may be scaled to reduce drive currents, and, depending on the circuit configuration used, associated bias currents as well. A driver **612** has a load R **614** and C **616**. The frequency response of this circuit is the same as that seen by driver **622**, which drives an impedance of 2R **624** and C/2 **626**. But the impedance of the load seen by driver **622** is double that seen by **612**, thus the output current required by the driver **622** is reduced by one-half.

As an example, the output stage of each of these drivers may be a Class A emitter follower formed by an emitter follower connected to a current source. When the outputs are driven high, the emitter of driver **622** need supply only one-half the drive current as driver **612**. In this way, an impedance can be scaled in order to decrease a circuit's required drive current.

Also, the discharge current for driver **622** is only one half that of driver **612** for a given negative-going slew rate. Thus, the current source of **622** may be reduced by the same factor of one-half as compared to driver **612**. In this example, the bias current, that is the current in the pull-down current source can be reduced. Many other examples where drive currents and possibly bias currents may be reduced will be appreciated by one skilled in the art.

FIG. **7** illustrates another degree of freedom that made be employed to reduce current levels in a transceiver. Specifically, a gain element **720** may be inserted in front of a circuit block **730** in order to improve the combined circuit's signal-to-noise ratio by a factor equal to the gain of the inserted gain block. This is particularly useful when large interferers are absent and the desired received signal is moderate or low. Specifically, gain is added to the signal while impedances are increased, which raise the noise floor. In this way, a given signal-to-noise ratio may be maintained while the power is decreased.

The gain of such an element may be varied by increasing a current in a differential pair or increasing a load resistance using switches. Many other examples where the gain of this element may be varied will be appreciated by one skilled in the art.

These variables, or degrees of freedom, specifically reducing bias currents, increasing impedances, and increasing gain may be used as in the following examples.

FIG. **8A** is a block diagram of a functional block **820** and optional gain element **810** in accordance with an embodiment of the present invention. Functional block **820**, like the functional blocks in the following diagrams, may be a filter, mixer, amplifier, or other circuit or circuits in a wireless transceiver or other electronic circuits or system. An input signal is received on line **812** by the optional gain element **814**. When the optional gain block **810** is not used, the input signal may be received directly by the function block **820**. The gain of the optional gain element **812** is controlled by a gain control signal on line **814**. The functional block receives an output signal from the optional gain element **810** and provides an output VOUT on line **822**. The lines in this and the other included figures may be one or more lines, depending on whether single-ended, differential, or other type of signaling is employed.

One or more impedances are under control of signals on impedance control lines **824**. Similarly, one or more bias currents in the function block are under control of one or more signals on bias control lines **826**. These various control lines may be logic signals, analog signals, voltage or currents lines, or other signal or bias lines. In other embodiments of the present invention, the gain control element **810** may be included in the function block **820**. Also, various embodiments may not incorporate either or both the impedance control and bias control.

FIG. **8B** is an example input that may be present on line VIN **812**. In this example, a desired signal **836** is relatively weak, as are interfering signals **837** and **838**. The initial bias and circuit configuration is such that the noise floor **833** and maximum signal handling capability Smax **831** are adjusted for worst case conditions. The circuit of FIG. **8A**, as with all the circuits described here, receives noise at its input which may be referred to as input equivalent noise or input referred noise. Additionally, the circuit of FIG. **8A** generates noise which is added to the input referred noise. Depending on the gain characteristics of the circuitry, the output noise at various frequencies may be greater than, equal to, or less than the input referred noise. For simplicity, the noise floor and maximum signal handling capability Smax, in this and the other figures, are shown as straight lines, though the noise and Smax are typically curved as a function of frequency.

That the input spectrum is as shown in FIG. **8B** can be determined, for example, by low signal strength indications on line VIN **812** and VOUT **822**. That is, a low level signal strength indication on line VIN **812** indicates that no portion of the input signal is particularly large.

For this exemplary input, there are at least two methods by which the power dissipation for this circuitry may be reduced. Depending on the exact circuits and structures used, one of these methods may be preferred.

In FIG. **8**C, the bias current is decreased, thereby lowering the maximum signal handling capability **841** as compared to **831**, closer to the desired and interfering signal levels. Again, the bias currents in the function block **820** may be reduced by switching impedances that appear across a voltage thereby changing a resulting bias current, by reducing a voltage at the gate of a MOS or base of a bipolar transistor, or by other methods.

In FIG. **8**D, a second method of reducing power dissipation in the function block **820** is employed. Specifically, Smax **851** is held constant as compared Smax **831**. The desired and interfering signals are amplified such that they are closer to the available signaling handling capability **851**. Also, the noise floor **853** is raised as compared to noise floor **833** in FIG. **8**B. Specifically, the noise contributed by the function block **820** is increased, such that the noise at its output is increased to noise floor **853**. This is done by increasing one or more impedance in function block **810**, such that drive currents inside that block are reduced. Depending on the exact configuration, this may also allow some biasing currents to be reduced, while maintaining the maximum signal handling capability **851** at a sufficient level. Alternately, these two methods of reducing power dissipation in function block **820** may be done in combination.

The included examples are explained for the exemplary situation where biasing and other parameters are set for worst-case conditions, and then changed to save power when it is discovered that the conditions are better-than-worst case. Alternately, the bias currents and other parameters may be set for maximum power savings, or an intermediate point, and the power can be adjusted from there.

FIG. **9**A illustrates a block diagram including an optional gain element **910** and function block **920**. Again, an input signal is received on line **912** by optional gain element **910** which in turn drives function block **920**. The function block provides an output VOUT on line **922**, and receives impedance and bias control signals on lines **924** and **926**.

FIG. **9**B shows the spectrum for what may be considered a best-case received signal. Specifically, the desired signal **936** is strong, while the interfering signals **937** and **938** are relatively weak. This may be determined, for example, by detecting a large signal level at the input line VIN **812** and a large signal level after a filter, since these readings would indicate that a large signal is received, but that it is at the desired signal frequency.

The maximum signaling capability **931** and noise floor **933** are shown as being set for the worst case conditions. In this case, the noise floor **933** is lower than the maximum allowed for proper signal reception. Accordingly, one or more impedance in the function block **920** may be increased, such that the noise floor **943** rises as shown in FIG. **9**C. In this way one or more the driving currents in the function block **920** may be reduced. Similarly, since the drive current is reduced, one or more bias current may also be reduced, depending on the exact circuit configuration.

FIG. **10**A illustrates a block diagram showing an optional gain element **1010** driving a function block **1020**. An input signal is received by the gain element **1010** on line **1012**, and an output is provided by function block **1020** on line VOUT **1022**. One or more gain control signals present on lines **1014** control the gain of gain control element **1010**, while one or more impedance and bias control signals are received by the function block **1020** on line to **1024** and **1026**.

FIG. **10**B illustrates a received signal that may be received on line VIN **1012**. In this example, the desired signal **1036** and interferers **1037** and **1038** are each relatively large. This may be determined, for example, by detecting a large signal level at the input line VIN **812** and a smaller signal level after a filter, since these readings would indicate that a large signal is received, but that interferers are being reduced.

As before, in this example, the noise floor **1033** and maximum signal handling capability **1031** are initially set for the worst case conditions. Since the desired signal is relatively large in this case, the noise floor may be allowed to rise, a shown by noise floor **1043** in FIG. **10**C. Since the desired signal **1046** and interferers **1047** are large, the maximum signal handling capability Smax **1041** remains constant. Again, the noise floor is increased by increasing impedances in the function block **1020**. This reduces the required drive current, and may also allow for a reduction in bias currents.

FIG. **11**A illustrates a block diagram including an optional gain element **1110** and function block **1120** in accordance with an embodiment of the present convention. An input signal is received on line **1112** by the optional gain control element **1110**, while an output signal is provided by the function block **1120** on line VOUT **1122**. Gain, impedance, and bias control signals are received on lines **1114**, **1124**, and **1126**.

FIG. **11**B is an exemplary input signal that may be received by the gain control element **1110** on line VIN **1112**. In this specific example, the desired signal **1136** is relatively low or weak while the interfering signals **1137** and **1138** are large. This may be determined, for example, by detecting a large signal level at the input line VIN **812** and a much smaller signal level after a filter, since these readings would indicate that a large signal is received and that large interferers are being reduced such that the resulting signal, the desired signal, is relatively weak.

Again, the maximum signal handling capability **1131** and noise floor **1133** are initially set for worst case conditions. If the desired signal is sufficiently low, while the interferers are sufficiently high, power savings may not be achievable over the worst case settings, since this is in fact the worst case condition. But, if the desired signal is somewhat larger than the worst case condition, then power may be saved in at least two different ways.

For example, FIG. **11**C shows the maximum signal handling capability **1141** being lowered. In this case, the interfering signals **1147** in **1148** began to clip and distort, thereby creating intermodulation products **1145**, which distort the desired signal **1146**. So long as care is taken to not corrupt the desired signal **1146** beyond an acceptable limit, typically measured by a bit-error rate, power may be reduced in this way.

Similarly, in FIG. **11**D, the noise floor **1153** is raised somewhat, thereby saving power. Again, this may be done so long as the noise floor is not sufficiently high that the system bit-error rate becomes unacceptable.

FIG. **12** is a summary of the above four examples. The received signal strengths are shown in column **1210**, while appropriate power saving responses are listed in column **1220**. Specifically, in row **1230**, the desired signal and interferer signal strengths are both weak or small. In this case, proper responses include decreasing Smax, or increasing one or more circuit impedances while increasing the circuit gain. Depending on the exact circuit configuration, one of these options may be preferred over the other. Alternately, they may be done in combination, or done in combination with other power saving techniques. Also, in

some specific embodiments, when both desired signal and interferer signal strengths are small, the gain may need to be increased while the impedance is maintained or not increased in order to keep the noise floor low.

In row **1240**, the desired signal strength is strong or large, while the interfering signals are small. In this case, an appropriate response is to increase one or more of the circuit impedances. Again, depending on the exact circuit in question, one or more of the bias currents may also be reduced.

In row **1250**, both the desired signals and interfering signal strengths are large. Again, in this case an appropriate response is to increase one or more of the circuit impedances.

In row **1260**, the received desired signal strength is weak or small, while the interfering signals are large. Since this is the worst case situation for which the circuit is designed, substantial power savings are difficult to achieve. However, again, if the received signal is above a minimum level necessary for proper operation, some distortion of the interferers or raising of the noise floor may be acceptable.

It should be noted that not all possible signal conditions are listed here. For example, either the signal or interferer may be of a relatively medium strength, or the interferer may be absent. Also, these terms are for exemplary purposes and are not meant to convey specific signal conditions, but rather are only qualitative. The proper response to a specific condition depends on the embodiment of the present invention, the particular circuit topology, the requirements of the signaling standard used, as well as other constraints.

FIG. **13** is an example shown how power may be saved as a function of time by employing one or more of these methods consistent with embodiments of the present invention. Power is plotted along a Y-axis **1304** as a function of time along X-axis **1302**. Conventional worst case design would fix power dissipation at line **1310**. As can be seen, dynamic power dissipation **1320** under the control of variable gains, impedances, biasing, or combination thereof, allows for a lower average power **1330** as compared to the power dissipated **1310** by the conventional design.

FIG. **14** is a block diagram of a portion of a receiver consistent with an embodiment of the present invention. Included are low-noise amplifier **1410**, mixer **1420**, gain stage **1430**, filter **1440**, AGC amplifier **1450**, and VCO **1460**. Signal strength detection is done at the output of the low-noise amplifier by signal strength indicator **1470**, at the output of the mixer by signal strength indicator **1472**, and at the output of the filter by signal strength indicator **1474**. The outputs of the signal strength indicator circuits are received by the computational circuit **1470**, which in turn controls gain and power control circuits **1480** and **1485**. Power and gain control circuits **1480** and **1485** control the gain, biasing, and impedance levels of the circuits in the receiver signal path. Also, the gain and power control circuits may control the same parameters in the VCO **1460**. This figure is greatly simplified for purposes of explanation. For example, the quadrature nature of the mixers and following circuits are not shown. Also, power-down and start-up circuits are not included.

The current level in the low-noise amplifier determines a multitude of parameters including voltage gain, linearity, input impedance matching, and noise figure. When conditions are better than worst-case, some of these parameters may be relaxed while maintaining an acceptable bit-error rate, thus saving power.

The bias current in the mixers effect that block's noise figure and linearity. Care is taken in reducing power in this block so as not to increase nonlinearities, particularly the third-order nonlinearity as measured by IP3, the third-order intercept point, beyond an acceptable limit.

A key parameter of the VCO is phase noise, an increase in which increases the sidebands on either side of the oscillation signal. During transmission, the phase noise should be kept low to avoid interference with adjacent channels and for preserving modulation information.

During reception however, if the conditions are better than worst case, the phase noise requirement for the VCO is relaxed, and power can be saved consistent with embodiments of the present invention. The achievable phase noise power spectral density is approximately inversely proportional to the bias current used. Thus, when low phase noise is not required during reception, bias current in the VCO can be reduced.

Most of the power savings in a transceiver in accordance with embodiments of the present invention is achieved in the receiver portion. Additional power may be saved in the transmitter section.

FIG. **15** is a block diagram of a transmitter portion consistent with an embodiment of the present invention. Included is a signal path formed by gain stage **1510** and power amplifier **1520**. The output power level is sensed by output level sensing circuit **1550**, which in turn adjusts the biasing of the power amplifier **1520** through the power control circuit **1540**. Additionally, a transmitter level control signal is received by power control circuits **1530** and **1540**, which in turn control the biasing of gain stage **1510** and power amplifier **1520**. Gain control circuit **1560** also adjusts the gain of gain stage **1510** and power amplifier **1520**. Additional circuitry that varies impedances in each of these circuits may also be included.

Since the gain, impedance and biasing of these blocks are being dynamically varied, care must be taken to not negatively affect the signal being processed. For example, specific embodiments of the present invention perform some or all of these variations during preamble. Also, as changes occur, the circuits in some embodiments are limited such that they may only adapt to an improvement in conditions after frames are completed. If conditions worsen, the circuits may be allowed to change in order to save the data. Alternately, a system may be manually calibrated, for example at set up, and when the network configuration is changed.

The above description of specific embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form described, and many modifications and variations are possible in light of the teaching above. The embodiments were chosen and described in order to best explain the principles of the invention and its practical applications to thereby enable others skilled in the art to best utilize the invention in various embodiments and with various modifications as are suited to the particular use contemplated.

What is claimed is:

1. A method of receiving a signal using an integrated circuit, the integrated circuit comprising a signal path including a low-noise amplifier configured to receive the signal, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer, the method comprising:

determining a first signal strength at a first node in the signal path in the integrated circuit; and

reducing a switching current in the signal path by dynamically changing an impedance of a component in the signal path based on the first signal strength.

2. The method of claim 1 wherein the signal comprises a preamble portion and a data portion, the impedance of a component is changed while receiving the preamble portion, and the method further comprises receiving the data portion of the signal.

3. The method of claim 2 further comprising:

determining a second signal strength at a second node in the signal path, wherein the second node in the signal path is after the first node in the signal path.

4. The method of claim 3 wherein the impedance of the component in the signal path is also changed based on the second signal strength.

5. The method of claim 2 wherein the component in the signal path comprises a MOS transistor.

6. The method of claim 2 wherein the component in the signal path comprises a resistor.

7. The method of claim 2 wherein the component in the signal path comprises a capacitor.

8. The method of claim 4 wherein the component in the signal path is included in the mixer.

9. The method of claim 4 wherein the component in the signal path is included in the low-pass filter.

10. A method of receiving a signal comprising a preamble portion and a data portion using an integrated circuit, the integrated circuit comprising a signal path including a low-noise amplifier configured to receive the signal, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer, the method comprising:

determining a first signal strength at a first node in the signal path in the integrated circuit; and

while receiving the preamble portion of the signal, dynamically changing a bias current in the signal path based on the first signal strength, and while receiving the data portion of the signal, maintaining the bias current in the signal path.

11. The method of claim 10 wherein the method further comprises receiving the data portion of the signal.

12. The method of claim 11 further comprising:

determining a second signal strength at a second node in the signal path, wherein the second node in the signal path is after the first node in the signal path.

13. The method of claim 12 wherein the bias current in the signal path is also changed based on the second signal strength.

14. The method of claim 11 wherein the bias current is a bias current for the low-noise amplifier.

15. The method of claim 11 wherein the bias current is a bias current for the mixer.

16. The method of claim 11 wherein the bias current is a bias current for the low-pass filter.

17. A method of receiving a signal using an integrated circuit, the integrated circuit comprising a signal path including a first circuit and a second circuit having an input coupled to an output of the first circuit, the method comprising:

determining a first signal strength at a first node in the signal path in the integrated circuit, wherein the first node is before the first circuit in the signal path;

dynamically changing a gain of the first circuit based on the first signal strength; and

dynamically changing an impedance of a component in the second circuit based on the first signal strength.

18. The method of claim 17 wherein the signal comprises a preamble portion and a data portion, the gain and impedance are changed while receiving the preamble portion, and the method further comprises receiving the data portion of the signal.

19. The method of claim 18 further comprising:

determining a second signal strength at a second node in the signal path, wherein the second node in the signal path is after the second circuit in the signal path.

20. The method of claim 19 wherein the gain of the first circuit and impedance of the component in the second circuit is also changed based on the second signal strength.

21. The method of claim 18 wherein the first circuit is a low-noise amplifier.

22. The method of claim 18 wherein the first circuit is a mixer.

23. A wireless transceiver integrated circuit comprising:

a receiver comprising a signal path, the signal path comprising:

a low-noise amplifier;

a mixer having an input coupled to an output of the low-noise amplifier; and

a low-pass filter having an input coupled to an output of the mixer; and

a first signal strength indicator circuit coupled to the signal path, and configured to determine a first signal strength;

wherein an impedance in the signal path is configured to be dynamically adjusted to reduce a switching current in response to the first signal strength.

24. The wireless transceiver of claim 23 further comprising:

a second signal strength indicator circuit coupled to the output of the mixer, and configured to determine a second signal strength,

wherein the first signal strength indicator is coupled to the output of the low-noise amplifier, and

wherein the impedance in the signal path is configured to be adjusted in response to the first and second signal strengths.

25. The wireless transceiver of claim 23 further comprising:

a second signal strength indicator circuit coupled to the output of the low-pass filter, and configured to determine a second signal strength,

wherein the first signal strength indicator is coupled to the output of the mixer, and

wherein the impedance in the signal path is configured to be adjusted in response to the first and second signal strengths.

26. A wireless transceiver integrated circuit comprising:

a receiver comprising a signal path, the signal path comprising:

a low-noise amplifier;

a mixer having an input coupled to an output of the low-noise amplifier; and

a low-pass filter having an input coupled to an output of the mixer; and

a first signal strength indicator circuit coupled to the signal path, and configured to determine a first signal strength, the first signal strength the strength of a signal comprising a preamble portion and a data portion;

wherein a bias current in the signal path is configured to be dynamically adjusted during the preamble portion of the signal in response to the first signal strength and further configured to be maintained during the data portion of the signal.

27. The wireless transceiver of claim 26 further comprising:

a second signal strength indicator circuit coupled to the output of the mixer, and configured to determine a second signal strength,

wherein the first signal strength indicator is coupled to the output of the low-noise amplifier, and

wherein the bias current in the signal path is configured to be adjusted in response to the first and second signal strengths.

28. The wireless transceiver of claim 26 further comprising:

a second signal strength indicator circuit coupled to the output of the low-pass filter, and configured to determine a second signal strength,

wherein the first signal strength indicator is coupled to the output of the mixer, and

wherein the bias current in the signal path is configured to be adjusted in response to the first and second signal strengths.

29. A wireless transceiver integrated circuit comprising:

a receiver comprising a signal path, the signal path comprising:

a first circuit; and

a second circuit having an input coupled to an output of the first circuit; and

a first signal strength indicator circuit coupled to the signal path, and configured to determine a first signal strength;

wherein a gain of the first circuit is configured to be dynamically adjusted in response to the first signal strength, and

wherein an impedance in the second circuit is configured to be dynamically adjusted in response to the first signal strength.

30. The wireless transceiver of claim 29 further comprising:

a transmitter comprising:

a power amplifier; and

an output-level-sensing circuit coupled to an output of the power amplifier,

wherein the output-level-sensing circuit is configured to dynamically adjust a gain of the power amplifier.

* * * * *

Exhibit B

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Tsividis

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(54) **POWER DISSIPATION REDUCTION IN WIRELESS TRANSCEIVERS**

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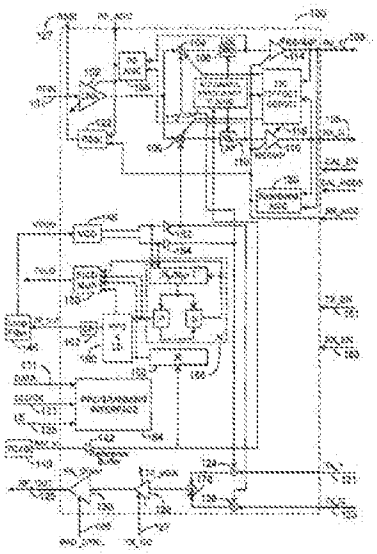
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(57) **ABSTRACT**

Processes, methods and circuits for improving battery life by reducing the battery power-drain of battery-powered devices using wireless transceivers is disclosed. Embodiments of the present invention provide for dynamically changing the bias current, impedance, and gain, either separately or in combination, during circuit operation to optimize or to reduce power dissipation. The dynamic variations may be implemented by varying the value of a resistance and/or a capacitance by opening switches across one or more portions of the resistance. Also, the dynamic variations may include setting any of the gain, bias current, or impedance parameters of the receiver circuit in between a high and low level, followed by adjusting the parameter up or down in response to a desired signal and an interferer signal.

8 Claims, 15 Drawing Sheets



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(12) **United States Patent**
Tsividis

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(54) **POWER DISSIPATION REDUCTION IN WIRELESS TRANSCEIVERS**

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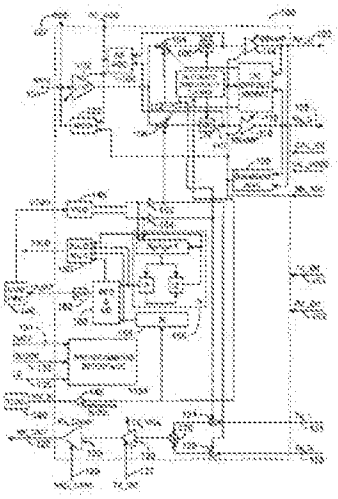
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(57) **ABSTRACT**

Methods and circuits for reducing power dissipation in wireless transceivers and other electronic circuits and systems. Embodiments of the present invention use bias current reduction, impedance scaling, and gain changes either separately or in combination to reduce power dissipation. For example, bias currents are reduced in response to a need for reduced signal handling capability, impedances are scaled thus reducing required drive and other bias currents in response to a strong received signal, or gain is increased and impedances are scaled in response to a low received signal in the presence of no or weak interfering signals.

30 Claims, 15 Drawing Sheets



Related U.S. Application Data

continuation of application No. 10/784,613, filed on Feb. 23, 2004, now Pat. No. 7,010,330.

(60) Provisional application No. 60/451,229, filed on Mar. 1, 2003, provisional application No. 60/451,230, filed on Mar. 1, 2003.

(51) **Int. Cl.**
H04W 52/02 (2009.01)
H04B 1/10 (2006.01)

(58) **Field of Classification Search**
CPC .. H04B 17/309; H04B 17/318; H04B 17/336; H04B 17/345; H04B 2001/045; H04B 2001/0416; H04W 52/52, H04W 52/0261; H04W 88/02; H03G 3/004; H03G 3/20
USPC 455/63.1, 67.13, 127.1, 127.2, 127.3, 455/226.1, 226.2, 232.1, 234.1, 250.1, 455/251.1, 295, 296, 343.1, 572, 574; 370/442; 330/127, 134, 144
See application file for complete search history.

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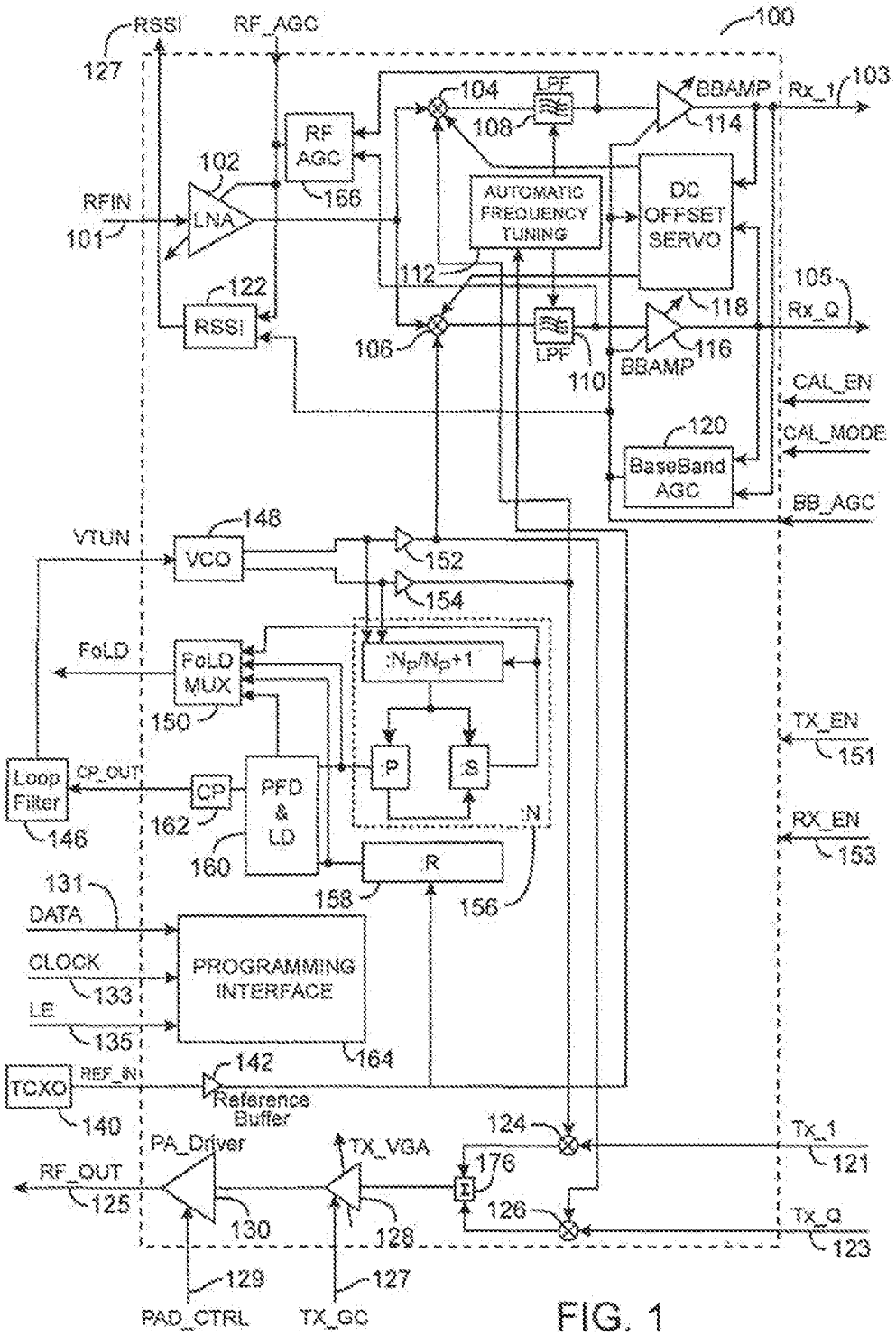

RSSI
127
RF_AGC
100
104
LPF
108
BBAMP
114
Rx_I
103
RF AGC
166
102
RFIN
101
LNA
AUTOMATIC FREQUENCY TUNING
DC OFFSET SERVO
118
112
105
Rx_Q
122
RSSI
106
LPF
110
BBAMP
116
CAL_EN
CAL_MODE
120
BaseBand AGC
BB_AGC
VTUN
148
VCO
152
154
FoLD
FoLD MUX
150
:Np/Np+1
TX_EN
151
Loop Filter
146
CP_OUT
CP
162
PFD & LD
160
:P
:S
:N
RX_EN
153
R
158
156
131
DATA
CLOCK
133
LE
135
PROGRAMMING INTERFACE
164
TCXO
140
REF_IN
142
Reference Buffer
124
Tx_I
121
PA_Driver
TX_VGA
176
RF_OUT
125
130
128
126
Tx_Q
123
129
PAD_CTRL
127
TX_GC

FIG. 1

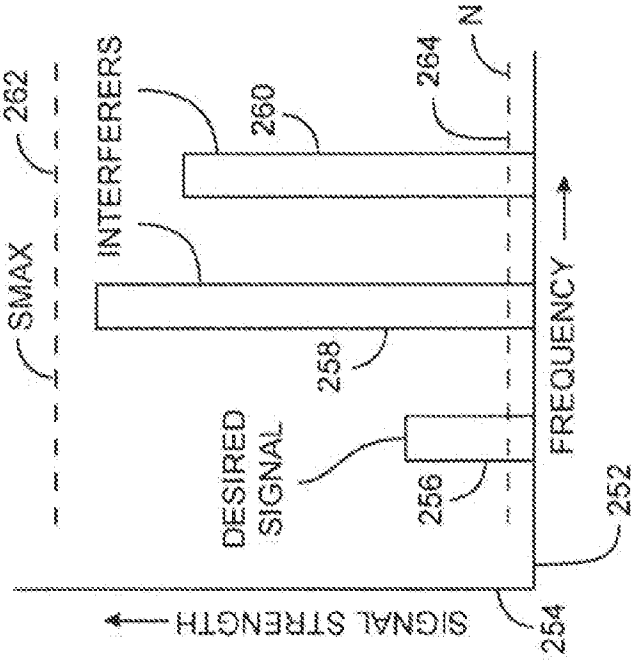

SMAX
262
INTERFERERS
260
264
N
258
DESIRED SIGNAL
256
FREQUENCY
252
SIGNAL STRENGTH
254

FIG. 2B

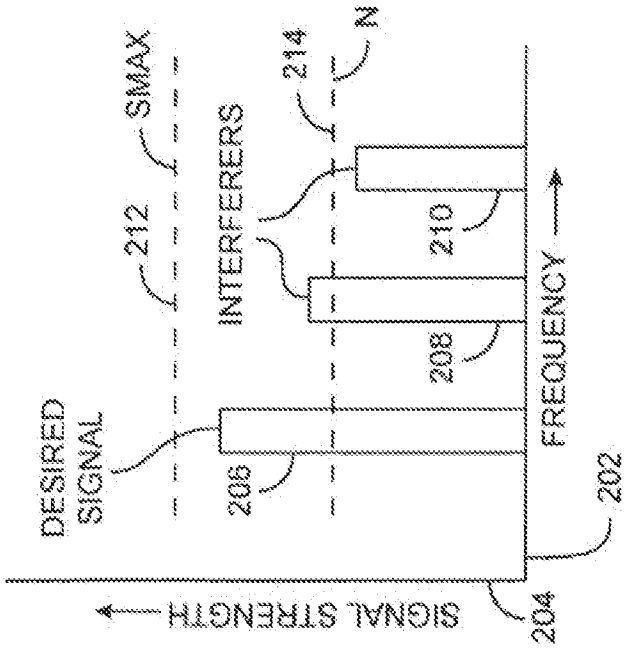

SMAX
212
214
N
INTERFERERS
210
208
DESIRED SIGNAL
206
FREQUENCY
202
SIGNAL STRENGTH
204

FIG. 2A

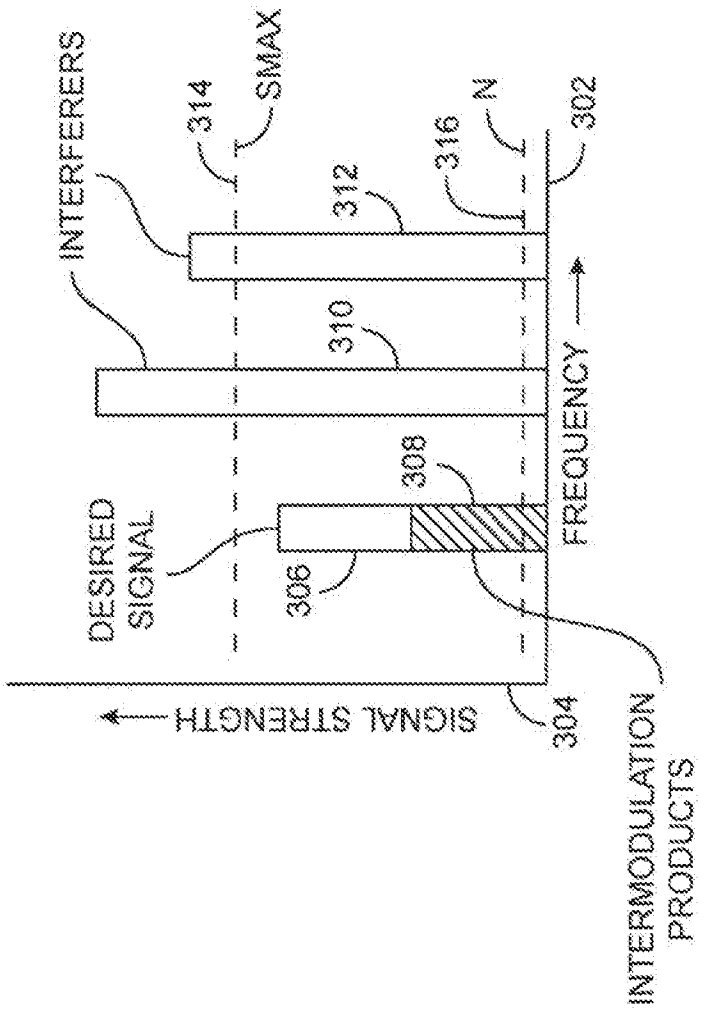

INTERFERERS
314
SMAX
312
316
N
302
310
DESIRED SIGNAL
308
306
FREQUENCY
SIGNAL STRENGTH
304
INTERMODULATION PRODUCTS

FIG. 3

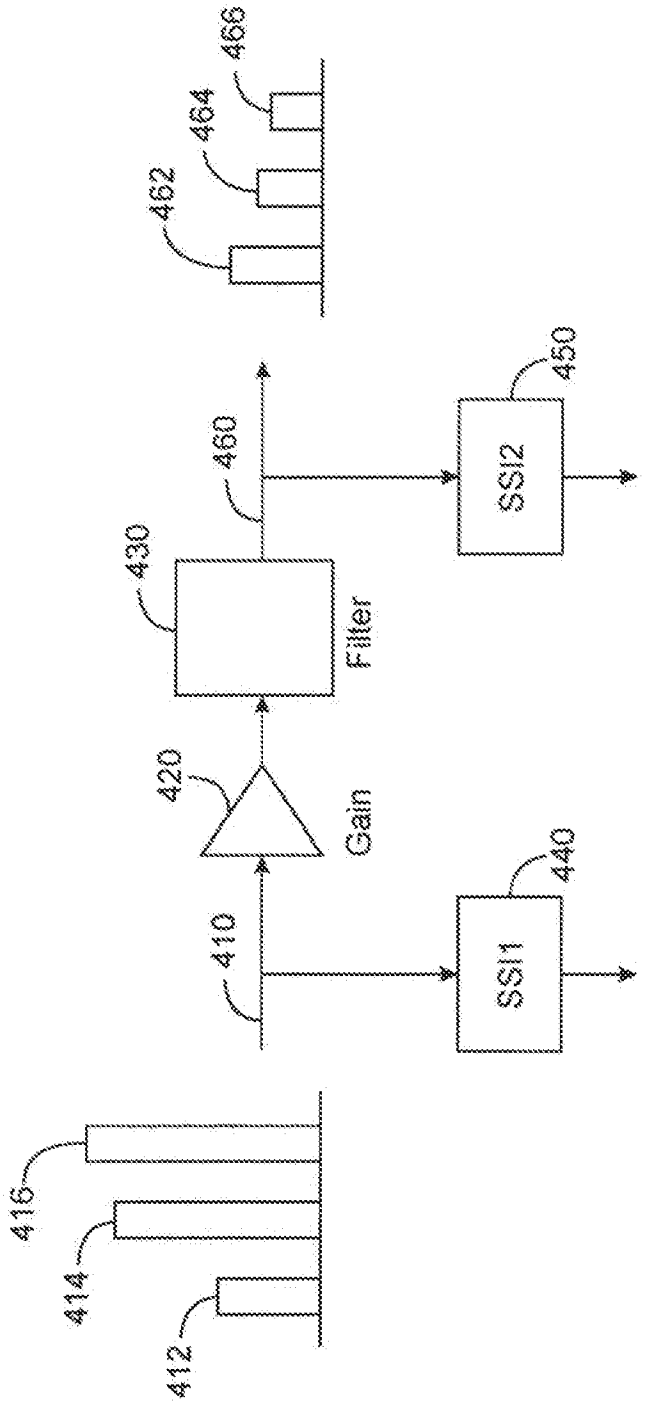

466
464
462
460
450
SSI2
430
Filter
420
Gain
410
440
SSI1
416
414
412

FIG. 4

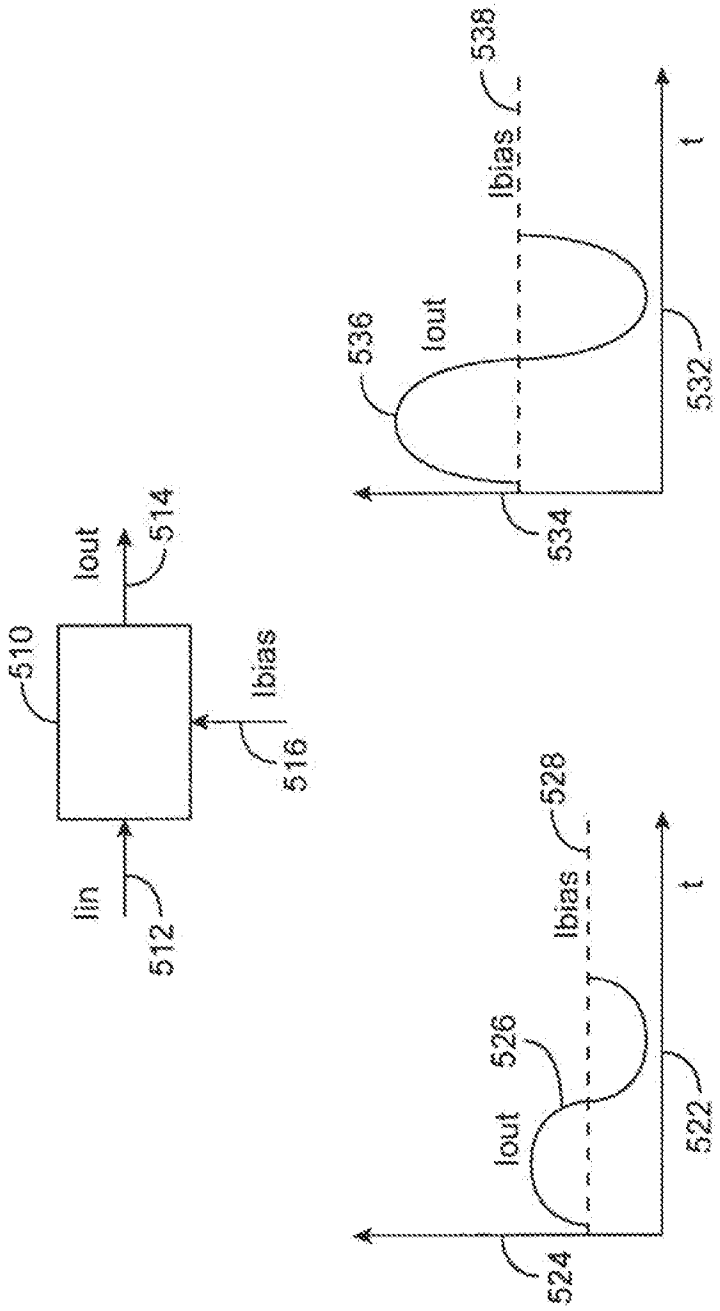

538
Ibias
t
536
Iout
532
534
514
Iout
510
Ibias
516
Iin
512
528
Ibias
t
526
Iout
522
524

FIG. 5

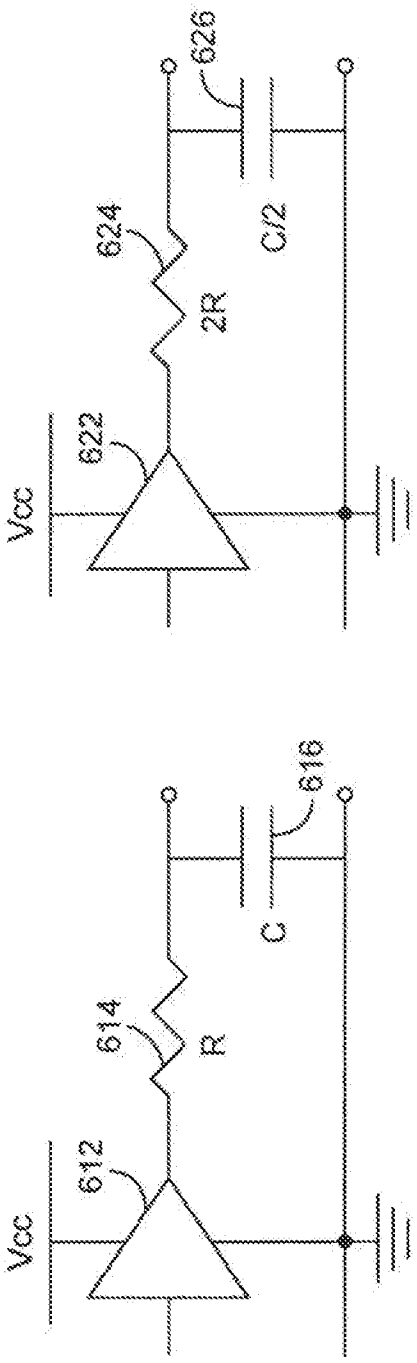


FIG. 6

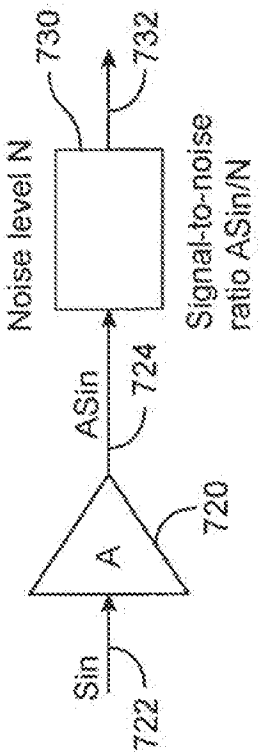

730
732
Noise level N
Signal-to-noise ratio ASin/N
ASin
724
720
A
Sin
722
710
Noise level N
Signal-to-noise ratio Sin/N
Sin
712

FIG. 7

Case: 1:22-cv-03441 Document #: 1-1 Filed: 07/05/22 Page 89 of 182 PageID #:89

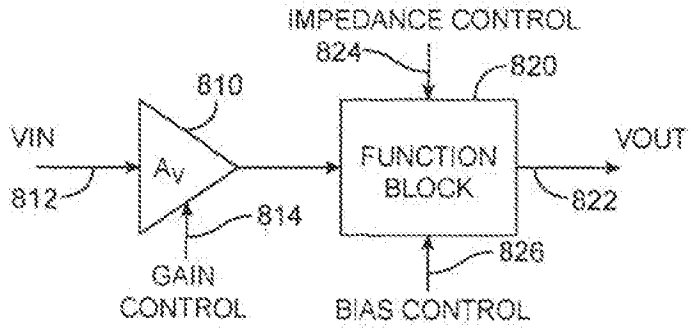


FIG. 8A

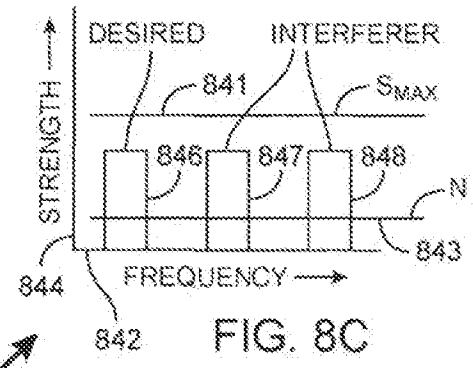


FIG. 8C

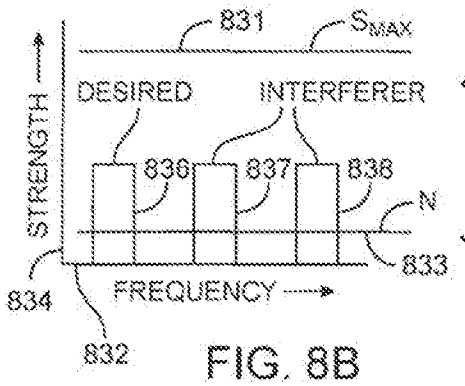


FIG. 8B

DECREASE BIASING

– AND/OR –

INCREASE GAIN AND IMPEDANCES

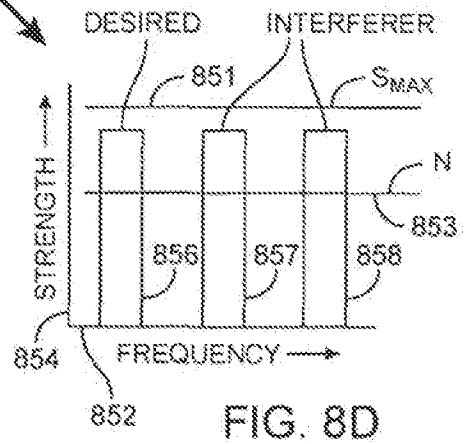


FIG. 8D

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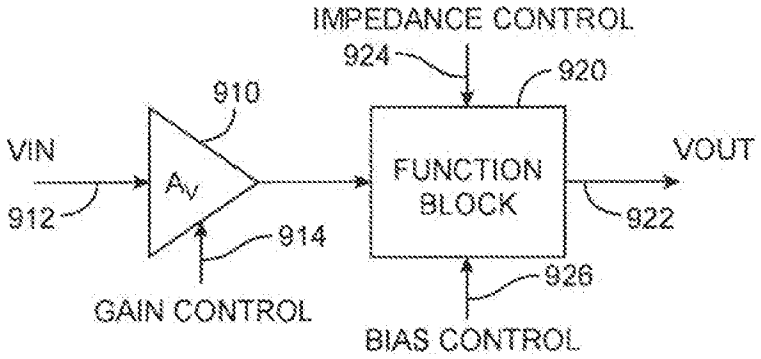


FIG. 9A

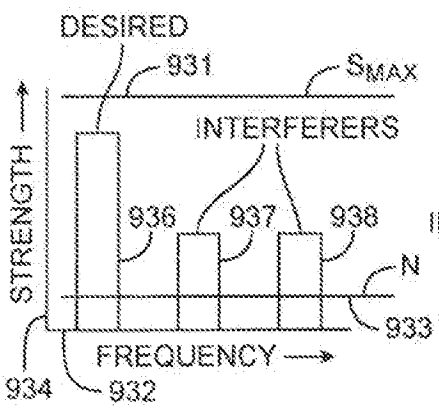


FIG. 9B

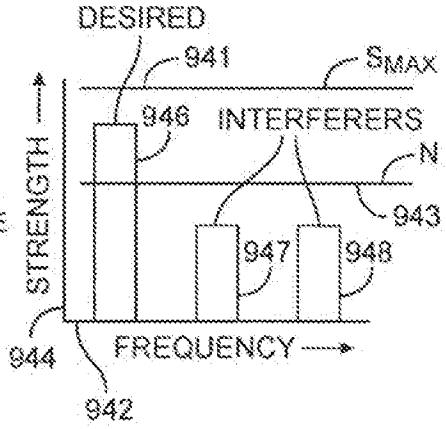


FIG. 9C

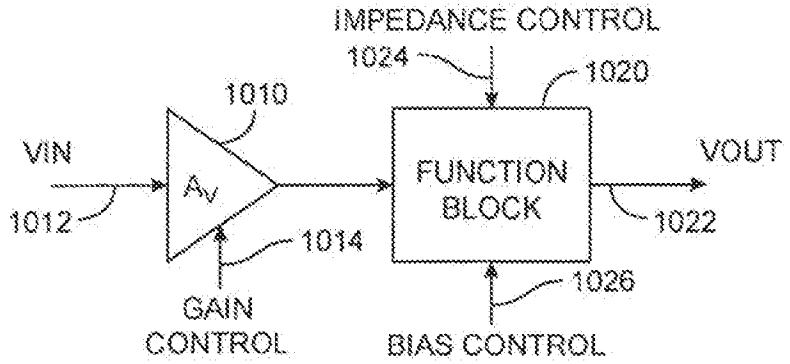


FIG. 10A

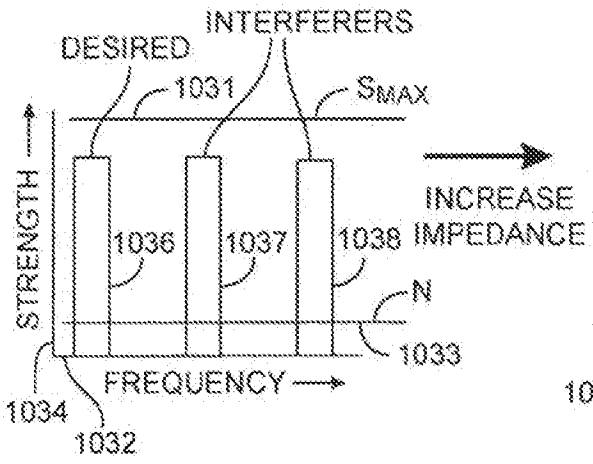


FIG. 10B

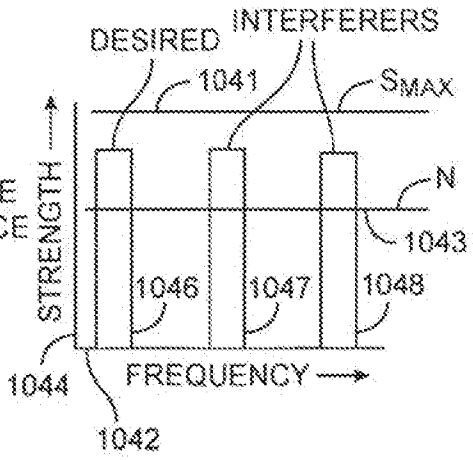


FIG. 10C

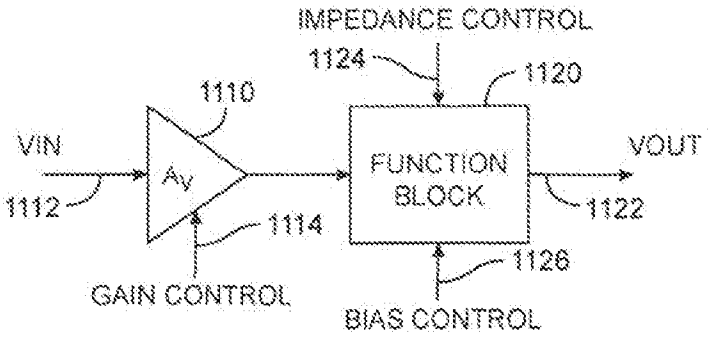


FIG. 11A

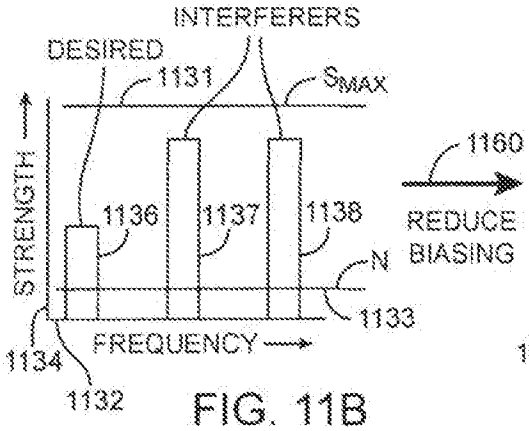


FIG. 11B

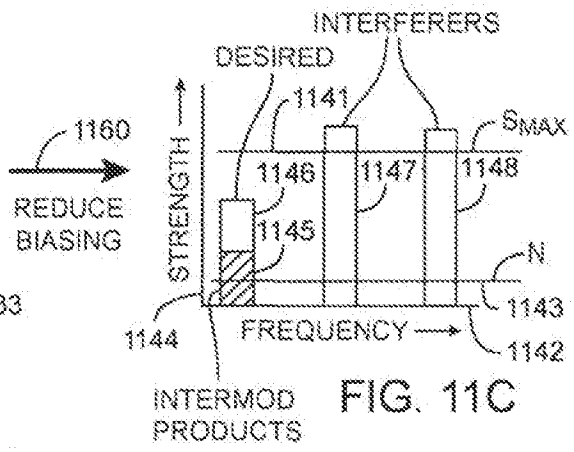


FIG. 11C

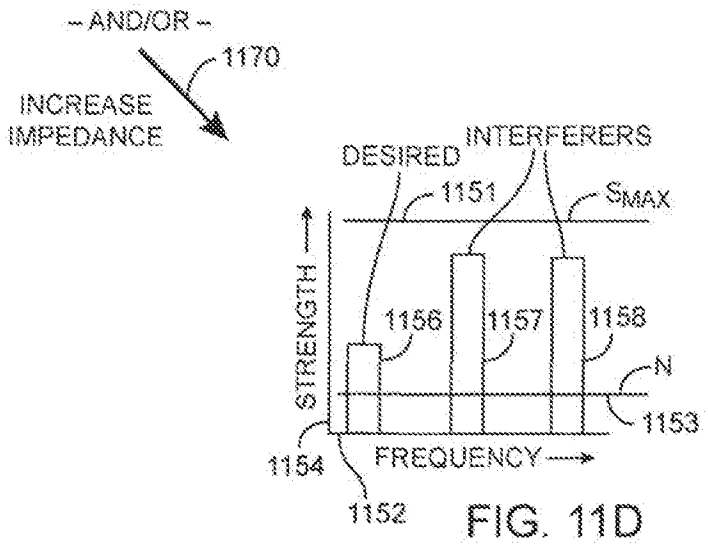


FIG. 11D

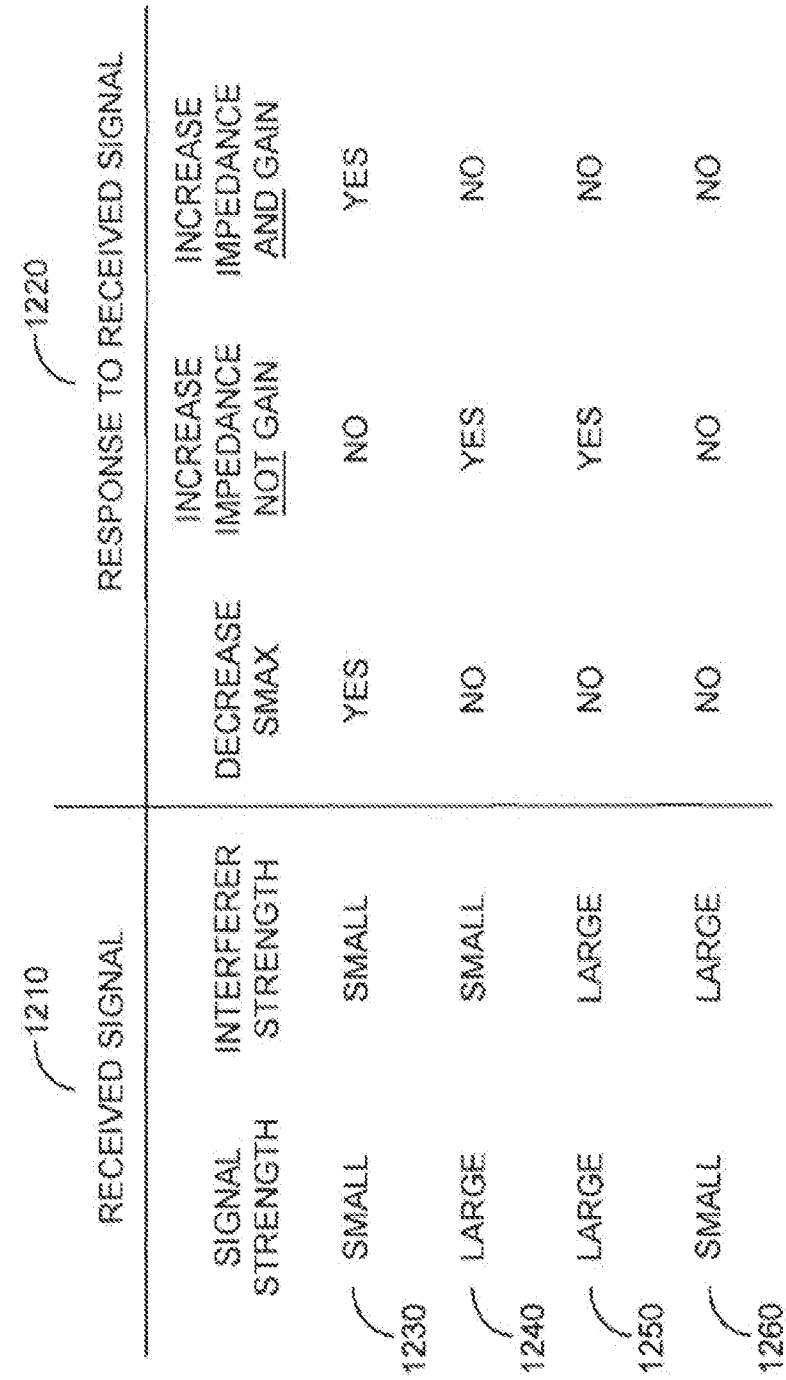

1210
RECEIVED SIGNAL
1220
RESPONSE TO RECEIVED SIGNAL
SIGNAL STRENGTH
INTERFERER STRENGTH
DECREASE SMAX
INCREASE IMPEDANCE NOT GAIN
INCREASE IMPEDANCE AND GAIN
SMALL
SMALL
YES
NO
YES
1230
LARGE
SMALL
NO
YES
NO
1240
LARGE
LARGE
NO
YES
NO
1250
SMALL
LARGE
NO
NO
NO
1260

FIG. 12

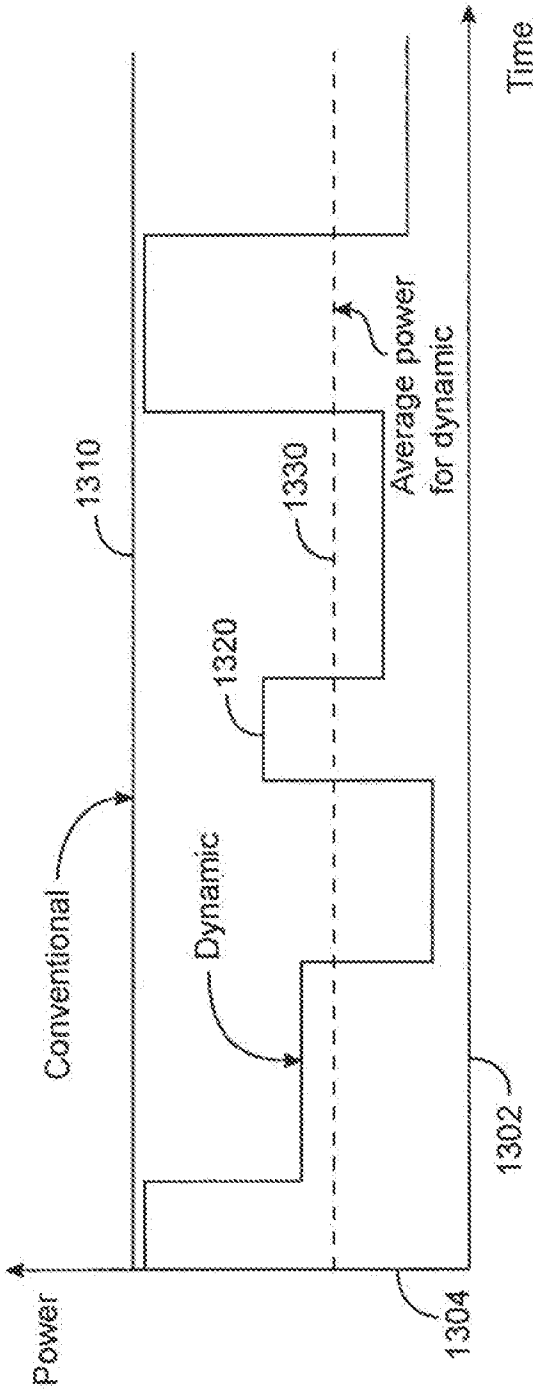

Power
Time
Conventional
Dynamic
1310
1320
1330
1302
1304
Average power for dynamic

FIG. 13

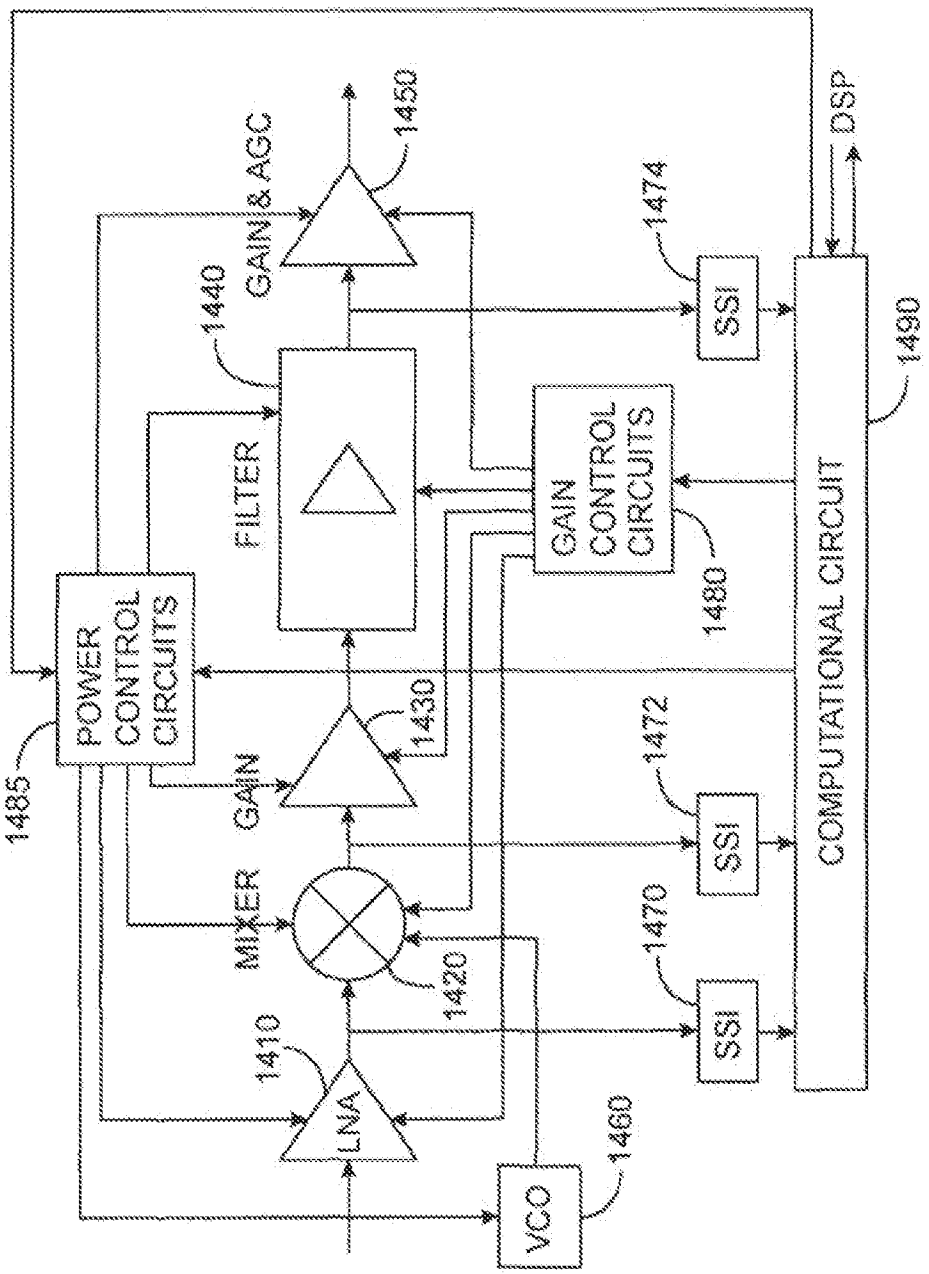

1485
POWER CONTROL CIRCUITS
1410
LNA
1420
MIXER
1430
GAIN
1440
FILTER
1450
GAIN & AGC
1460
VCO
1470
SSI
1472
SSI
1474
SSI
1480
GAIN CONTROL CIRCUITS
1490
COMPUTATIONAL CIRCUIT
DSP

FIG. 14

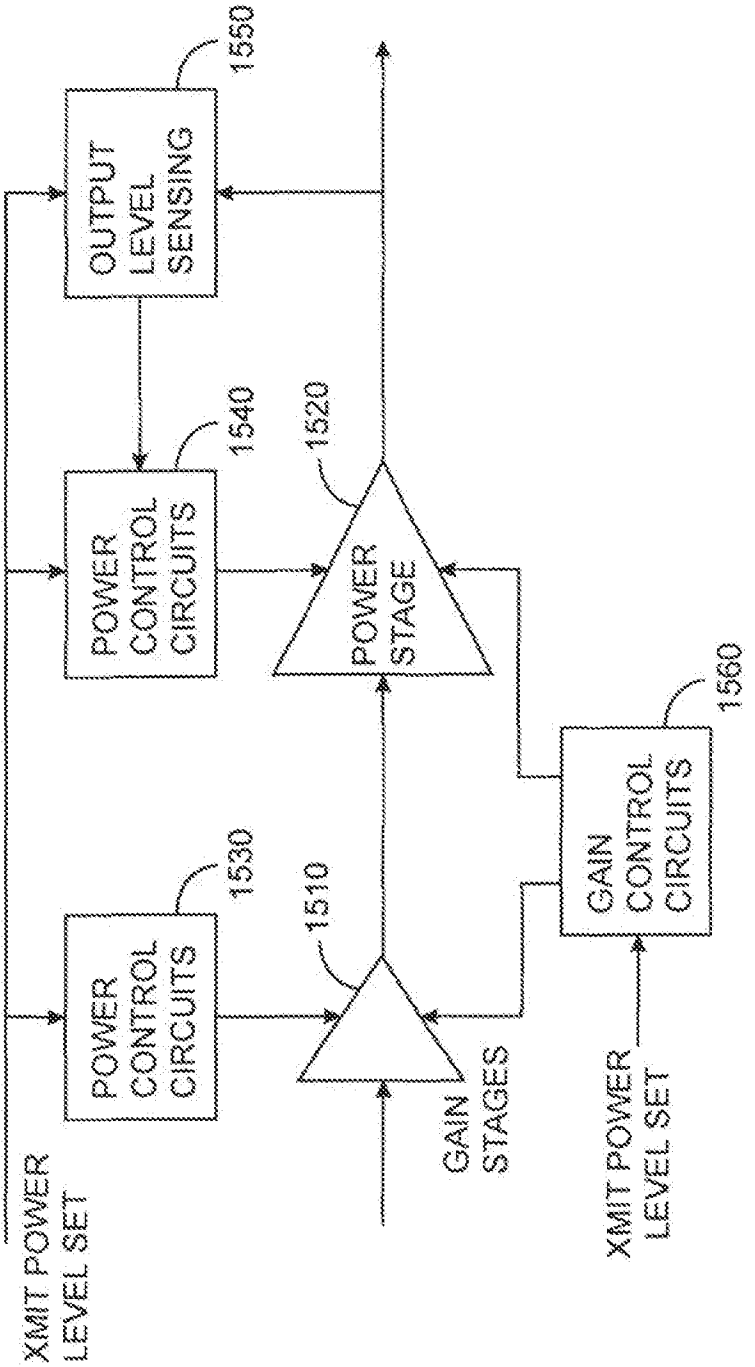

XMIT POWER LEVEL SET
POWER CONTROL CIRCUITS
1530
1510
GAIN STAGES
POWER CONTROL CIRCUITS
1540
1520
POWER STAGE
OUTPUT LEVEL SENSING
1550
GAIN CONTROL CIRCUITS
1560
XMIT POWER LEVEL SET

FIG. 15

POWER DISSIPATION REDUCTION IN WIRELESS TRANSCEIVERS

CROSS-REFERENCES TO RELATED APPLICATIONS

This application is a continuation of U.S. patent application Ser. No. 11/318,646, filed Dec. 27, 2005, which is a continuation of U.S. patent application Ser. No. 10/784,613, filed Feb. 23, 2004, which claims the benefit of U.S. provisional application No. 60/451,229, filed Mar. 1, 2003, which is incorporated by reference.

This application claims the benefit of U.S. provisional application No. 60/451,230, filed Mar. 1, 2003, which is incorporated by reference.

BACKGROUND

The present invention relates to power dissipation reduction techniques for electronic circuits, for example wireless transceiver integrated circuits.

Wireless networking is quickly becoming ubiquitous, as desktop, notebook, and handheld computers are connected to share Internet access and files. Wireless networking cards compatible with PCMCIA and compact flash form factors are popular for laptops and handhelds respectively, particularly as mobile users connect to the Internet on the road at coffee shops, hotels, and airports.

A downside of this connectivity is a corresponding drain on battery life, especially for these portable devices. The power consumed by a wireless transmitter and receiver reduces the usefulness of a device and sends a user on a hunt for an electrical outlet for recharging.

One reason why this power drain is high is that electronic circuits are typically designed to function properly under worst-case operating conditions. For a wireless transceiver, the worst case condition is when a desired signal reception strength is low, while other transceivers or nearby electronic equipment generate interfering signals and other spurious noise.

But a wireless transceiver does not always operate in these worst-case conditions. For example, a base station, router or access point may be nearby such that the received signal is strong. Also, there may be no interfering signals, or they may be relatively weak. In these situations, receiver circuit currents can be reduced below what is necessary for the worst case condition. If this is done, power dissipation is reduced, and battery life is increased.

Thus, what is needed are circuits and methods that can adapt to a better-than-worst-case condition and reduce circuit currents and therefore power dissipation accordingly.

SUMMARY

Accordingly, embodiments of the present invention provide methods and circuits for reducing power dissipation in wireless transceivers and other electronic circuits and systems. Embodiments of the present invention use bias current reduction, impedance scaling, gain, and other dynamic changes either separately or in combination to reduce power dissipation in response to better-than-worst case conditions. For example, bias currents are reduced in response to a need for reduced signal handling capability, impedances are scaled thus reducing required drive and other bias currents in response to a strong received signal, or gain is varied and impedances are scaled in response to a low received signal in the presence of no or weak interfering signals. Alternately, currents may start low and be increased in response to worse-than-best-case conditions, or they may start at a point in between and vary up or down. These variations may be made to electronic systems generally, and are particularly suited and discussed below in the context of a wireless transceiver that may be used in networking devices, cellular telephones, and other wireless systems.

An exemplary embodiment of the present invention provides a method of receiving a signal using an integrated circuit. The integrated circuit includes a signal path having a low-noise amplifier configured to receive the signal, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer. The method itself includes determining a first signal strength at a first node in the signal path in the integrated circuit and dynamically changing an impedance of a component in the signal path based on the first signal strength.

A further exemplary embodiment of the present invention provides a method of receiving a signal using an integrated circuit. The integrated circuit includes a signal path having a low-noise amplifier configured to receive the signal, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer. The method itself includes determining a first signal strength at a first node in the signal path in the integrated circuit and dynamically changing a bias current in the signal path based on the first signal strength.

Another exemplary embodiment of the present invention provides a method of receiving a signal using an integrated circuit. The integrated circuit includes a signal path having a first circuit and a second circuit having an input coupled to an output of the first circuit. The method itself includes determining a first signal strength at a first node in the signal path in the integrated circuit. The first node is before the first circuit in the signal path. The method further includes dynamically changing a gain of the first circuit based on the first signal strength and dynamically changing an impedance of a component in the second circuit based on the first signal strength.

Still a further exemplary embodiment of the present invention provides a wireless transceiver integrated circuit including a receiver having a signal path, the signal path including a low-noise amplifier, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer, as well as a first signal strength indicator circuit coupled to the signal path and configured to determine a first signal strength. An impedance in the signal path is configured to be dynamically adjusted in response to the first signal strength.

Yet a further exemplary embodiment of the present invention provides a wireless transceiver integrated circuit. This integrated circuit includes a receiver comprising a signal path, the signal path having a low-noise amplifier, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer, as well as a first signal strength indicator circuit coupled to the signal path, and configured to determine a first signal strength. A bias current in the signal path is configured to be dynamically adjusted in response to the first signal strength.

Another exemplary embodiment of the present invention provides a wireless transceiver integrated circuit. This circuit includes a receiver comprising a signal path, the signal path having a first circuit; and a second circuit having an input coupled to an output of the first circuit; as well as a first

signal strength indicator circuit coupled to the signal path, and configured to determine a first signal strength. A gain of the first circuit is configured to be dynamically adjusted in response to the first signal strength, and an impedance in the second circuit is configured to be dynamically adjusted in response to the first signal strength.

A better understanding of the nature and advantages of the present invention may be gained with reference to the following detailed description and the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram of a wireless transceiver that may benefit by incorporation of embodiments of the present invention;

FIGS. **2**A and **2**B illustrate examples of desired and interfering signals and noise that may be received by a circuit in a wireless receiver;

FIG. **3** illustrates what can occur as a maximum signal handling capability is reduced in the worst-case signal condition;

FIG. **4** illustrates a portion of a receiver consistent with an embodiment of the present invention;

FIG. **5** illustrates the relationship between a required bias current and a given output signal for a representative circuit;

FIG. **6** is an example of how a circuit's impedances may be scaled to reduce drive currents, and depending on the circuit configuration used, to reduce associated bias currents as well;

FIG. **7** illustrates how gain may be inserted in a signal path to improve a circuit's signal to noise ratio;

FIGS. **8**A-**8**D illustrate some of the possible power saving techniques that may be used when received desired and interferer signals are all at a low power level;

FIGS. **9**A-**9**C illustrate one of the possible power saving techniques that may be used when a received desired signal is strong while all interfering signals are at a low power level;

FIGS. **10**A-**10**C illustrate one of the possible power saving techniques that may be used when received desired and interferer signals are all at a high power level;

FIGS. **11**A-**11**D illustrate one of the possible power saving techniques that may be used when a received desired signal is weak while one or more interfering signals are strong;

FIG. **12** is a summary illustrating four different input conditions and some of the appropriate power-saving changes that may be made in response to those conditions;

FIG. **13** shows how power may be saved as a function of time by employing one or more of the power saving methods consistent with embodiments of the present invention;

FIG. **14** is a block diagram of a portion of a receiver consistent with an embodiment of the present invention; and

FIG. **15** is a block diagram of a portion of a transmitter consistent with an embodiment of the present invention.

DESCRIPTION OF EXEMPLARY EMBODIMENTS

FIG. **1** is a block diagram of a wireless transceiver that may benefit by incorporation of embodiments of the present invention. This wireless transceiver may be designed to send and receive signals consistent with the IEEE 802.11a, 802.11b, 802.11g, or other signaling standard or combination of standards. This figure, as with all the included figures, is shown for illustrative purposes only and does not to limit either the possible embodiments of the present invention or the claims.

There are three main portions of this transceiver circuit, a receiver, transmitter, and synthesizer. This transceiver may be completely or partially integrated on a semiconductor chip, or it may be integrated onto multiple integrated circuits. In a specific embodiment, the circuitry bounded by dashed line **100** is integrated on a single chip coupled to one or more external components or circuits. The integrated circuit or circuits forming this wireless transceiver may incorporate various integrated circuit devices such as a bipolar, CMOS, or BiCMOS devices made using a silicon, silicon-germanium (SiGe), gallium arsenide or other III-V process, or other manufacturing process. Embodiments of the present invention may also be applicable to circuits manufactured using nanotechnology processing.

The receiver includes a signal path formed by low-noise amplifier **102**, I and Q mixers **104** and **106**, low pass filters **108** and **110**, and baseband amplifiers **114** and **116**. Other circuitry in the receiver includes received strength indicator **122**, automatic gain control circuit **166**, baseband gain control circuit **120**, tuning circuit **112**, and offset cancellation circuit **118**.

The transmitter includes input up-converter mixers **124** and **126**, summing node **176**, which may be conceptual rather than an actual circuit, transmit variable gain amplifier **128**, and power amplifier **130**.

The synthesizer includes a voltage-controlled oscillator **148**, which drives I and Q buffers **154** and **152**, prescaler **156**, reference clock buffer **142** and divider **158**, phase-frequency detector **160**, charge pump **162**, and loop filter **146**, which in a specific embodiment is formed by external components.

Signals are received on an antenna, not shown, and typically pass through an RF switch and bandpass filter before being received by the low-noise amplifier **102** on line **101**. The low noise amplifier gains the received signal and provides it to quadrature mixers **104** and **106**. I and Q mixers **104** and **106** down-convert the received signal to baseband by multiplying them with quadrature versions of the oscillator signal provided by buffers **152** and **154**. This down conversion also produces a high frequency component at a frequency that is equal to the sum of the frequencies of the received signal and the VCO. This unwanted signal is filtered by low pass filters **108** and **110**, which in turn drive baseband amplifiers **114** and **116**. The outputs of baseband amplifiers **114** and **116** are typically converted to digital signals by analog-to-digital converters at the front end of a digital signal processing block.

In the transmit mode, I and Q versions of the signal to be transmitted are provided on lines **121** and **123** to up-convert mixers **124** and **126**. These up-convert mixers multiply the I and Q portions of the transmit signal by quadrature versions of the VCO signal provided by buffers **152** and **154**. The outputs of the up-convert mixers **124** and **126** are summed, and amplified by transmit VGA **128**, which in turn drives power amplifier **130**. The output of power amplifier **130** is typically filtered, and passes through the RF switch to the antenna for transmission.

A reference clock is received and buffered by the reference buffer **142**. The VCO generates quadrature oscillatory signals that are divided by prescaler **156**. The reference clock is typically generated by a crystal or other stable periodic clock source. The phase-frequency detector **116** compares the phase or frequency (depending on whether the synthesizer is tracking or acquiring the correct frequency) of

the divided VCO signal and the reference clock, or a divided version of the reference clock, and generates an error signal, which drives the charge pump **162**. The output signal of the charge pump **162** is filtered by the loop filter **146**, which is commonly a lead-lag filter, and which provides a tuning or correction signal to the VCO **148**.

Embodiments of the present invention may be used to reduce the power dissipation of one or more of these included circuits. For example, the power dissipation in the low-noise amplifier **102**, down-convert mixers **104** and **106**, low pass filters **108** and **110**, or baseband amplifiers **114** and **116** may be optimized. Also, power dissipation in up-convert mixers **124** **126**, variable gain amplifier **128**, and power amplifier **130** may also be optimized. Similarly, VCO **148** and prescaler **156** currents may be adjusted. Embodiments of the present invention may also be applied in other circuits which may be included in other integrated circuit receivers, transmitters, transceivers, or other electronic circuits or systems.

When a receiver is actively receiving a desired signal, each block in the signal path has at its input the desired signal as well as noise and possibly interfering signals. The desired signal is the useful, information-carrying portion of a received signal. The noise may be thermal, shot, or other noise generated on the integrated circuit, in addition to received noise generated by sources external to the chip. The noise at the input of a block may be referred to as the equivalent input noise. The interfering signal or signals, or interferers, may be generated by similar transceivers, or other electrical equipment, circuits, or systems.

FIGS. **2**A and **2**B illustrate examples of desired signals, interferers, and noise that may be received by one of the various circuits in a wireless receiver. In each of these figures, the signal strength is plotted along a Y-axis **204** or **254** as a function of frequency along an X-axis **202** or **252**. In the example of FIG. **2**A, a received desired signal **206** is large in comparison to interfering signals **208** and **210**. In these examples, two interfering signals are shown for illustrative purposes, though there may be no such signals, one such signal, or more than two such signals in the frequency range of interest. Also, while for these examples the interferers are shown as being at a higher frequency than the desired signal, there may be one or more interferers at higher or lower frequencies as the desired signal. In this specific example, the acceptable noise floor **214** is relatively high, while maximum signal handling capability Smax **212** (that is the maximum signal power that can be handled with an acceptably low distortion) needs only to be high enough to accommodate the desired signal. For this specific example, the circuit receiving this input spectrum only requires a relatively small dynamic range for proper operation, that is the range between Smax **212** and the noise floor **214** is relatively small.

Conversely, in the example shown in FIG. **2**B, the desired signal **256** is relatively weak compared to the large interferers **258** and **260**. In this example, the noise floor **264** should be relatively low so as to prevent an unacceptable level of error in the recovery the desired signal **256**. The maximum signal handling capability Smax **262** should be relatively high to accommodate the large interferers in order to avoid the creation of intermodulation products as described below. Accordingly, in this specific example, the circuit receiving this input spectrum should have a large dynamic range, particularly in comparison to the example of FIG. **2**A.

It should be noted that the noise level or noise floors shown in these and the other included figures is the noise density integrated over the bandwidth of interest. For simplicity and comparison, this level is shown as a horizontal line, and is not meant to imply noise density.

Often in wireless receivers, a circuit at different times will receive an input spectrum similar to those shown in FIGS. **2**A and **2**B. The input spectrum of FIG. **2**B is generally considered the worst-case input signal, and typical design methodology involves designing a receiver for this condition, specifically the weakest desired signal accompanied by largest interference level. Circuit impedances and currents are set such that the noise floor **264** is sufficiently low for an acceptable bit-error rate, while bias currents are set sufficiently high for the required Smax **262**.

Conversely, the input spectrum in FIG. **2**A is that of the best-case input signal, specifically, a robust desired signal accompanied by no or low-level interferers. In this case, the noise floor **214** may be allowed to rise, while the maximum signal handling capability Smax **212** may be reduced. When this is done, the receiver circuit may save significant power. For example, the circuit's impedances may be increased, thus reducing required drive currents. Similarly, bias currents may be lowered, thus reducing the maximum signal in handling capability.

The minimum power dissipation for a circuit is proportional to the required maximum signal-to-noise ratio, which is the ratio between Smax **212** or **262** and N **214** or **264**. Thus, a circuit receiving an input similar to the one shown in FIG. **2**A can dissipate less power than one receiving the input as shown in FIG. **2**B, while still achieving an acceptable bit-error rate.

FIG. **3** illustrates what can occur when the maximum signal handling capability Smax **314** is reduced in the worst-case condition, that is when a weak desired signal **306** is accompanied by large interferers **310** and **312**. Again, signal strength is plotted along a Y-axis **304** as a function of frequency along X-axis **302**. In this specific example, Smax **314** is reduced below the peak levels of the interferers **310** and **312**. Since Smax is low, the circuit cannot handle the interferers linearly. The resulting nonlinearities lead to a mixing of the interferers and the creation of intermodulation products **308** (for example, a third-order intermodulation distortion, IM3), one of which in this example occurs at the same frequency as the desired signal **306**. As can be seen, if the intermodulation products **308** become excessive, the received signal bit error rate may become excessive, and the desired signal **306** may be lost. Accordingly, while Smax may be lowered even under some unfavorable conditions in order to reduce power, care should be taken to avoid corruption of the received desired signal.

FIG. **4** illustrates a portion of a receiver consistent with an embodiment of the present invention. Included is a filter **430**. An optional gain element **420** is placed in front of the filter **430** in order to increase signal levels. Signal strength indicator circuits **440** and **450** are connected to input line **410** and output line **460**. In this specific example, the input signal spectrum on line **410** is shown as desired signal **412** and interferers **414** and **416**. The signal spectrum at the output line **460** is shown as desired signal **462** and interferers **464** and **466**. The signal strength indicators **440** and **450** do not provide information as to the relative sizes of the desired and interfering signals. Rather, a cumulative signal level is provided at their outputs. For example, the first signal strength indicator **440** outputs a level corresponding to the sum of desired signal **412** and interfering signals **414** and **416**, while the second signal strength indicator **450** provides a signal level corresponding to the sum of desired signal **462** and interfering signals **464** and **466**. In this specific example,

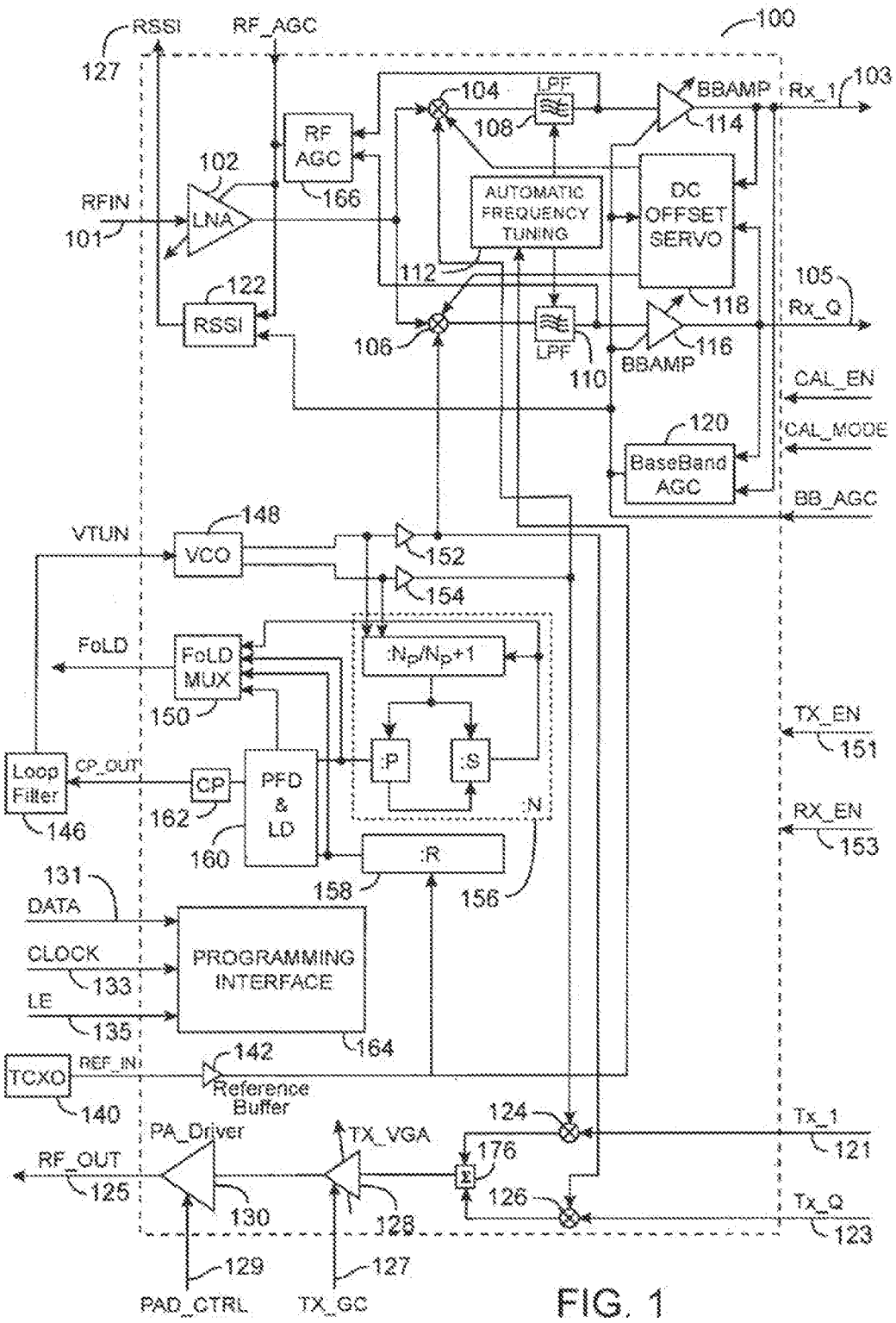

RSSI
127
RF_AGC
100
104
LPF
108
BBAMP
114
Rx_I
103
RF AGC
166
102
RFIN
101
LNA
AUTOMATIC FREQUENCY TUNING
DC OFFSET SERVO
112
122
RSSI
105
Rx_Q
118
106
LPF
110
BBAMP
116
CAL_EN
CAL_MODE
120
BaseBand AGC
BB_AGC
VTUN
148
VCO
152
154
FoLD
FoLD MUX
150
:Np/Np+1
TX_EN
151
Loop Filter
146
CP_OUT
CP
162
PFD & LD
160
:P
:S
:N
:R
158
156
RX_EN
153
131
DATA
CLOCK
133
LE
135
PROGRAMMING INTERFACE
164
TCXO
140
REF_IN
142
Reference Buffer
124
Tx_I
121
PA_Driver
TX_VGA
176
RF_OUT
125
130
128
126
Tx_Q
123
129
PAD_CTRL
127
TX_GC

FIG. 1

the gain of the gain and filter circuit combinations is shown as approximately one, while the interfering signals **414** and **416** signal levels are reduced.

A comparison of the signal levels provided by the signal strength indicators **440** and **450** indicates that much of the combined received signal on line **410** has been filtered. Accordingly, it may be deduced that large interfering signals present at the input are being filtered by the filter **430**. From this information, as will be shown in greater detail below, the bias, impedance, and gain of the gain stage **420** and filter **430** combination may be optimized to reduce power dissipation.

There are several real world situations where the received signal is better than the worst-case condition such that power can be saved. For example, large interferers may be present only part of the time, that is, on a temporary or transient basis. The interfering equipment may be some distance from the transceiver, or it may be operating in the low power mode. Also, the desired signal may be very strong as compared to the noise and interferers, for example a hub, router, or access point may be nearby.

Some transceivers consistent with embodiments of the present invention are designed to work with more than one data transfer specification or standard. In this case, when a transceiver is operating in a mode having a lower data rate, the power saving techniques described here may be employed.

FIG. **5** illustrates the relationship between a required biased current **516** for a given output signal **514** for a representative circuit **510**. If the output signal current level is relatively low, such as the output current shown as **526**, the corresponding bias current **528** may be low. Conversely, if the output signal current level is larger as with the example **536**, the corresponding bias current level **538** should also be high. Accordingly, if a bias current is initially set high to handle large a large input signal, for example a large interferer, this current may be reduced if the input signal is smaller.

There are many ways by which these bias currents can be reduced. For example, the current may be generated by placing a voltage across a resistor by applying a bias voltage to the base of a device whose emitter is connected to ground through a resistance. In this case, the resistor may be increased by opening switches across portions of the resistance, or lowering the bias voltage applied at the base. Several ways in which this may be done will be readily understood by one skilled in the art.

FIG. **6** is an example of how a circuit's impedances may be scaled to reduce drive currents, and, depending on the circuit configuration used, associated bias currents as well. A driver **612** has a load R **614** and C **616**. The frequency response of this circuit is the same as that seen by driver **622**, which drives an impedance of 2R **624** and C/2 **626**. But the impedance of the load seen by driver **622** is double that seen by **612**, thus the output current required by the driver **622** is reduced by one-half.

As an example, the output stage of each of these drivers may be a Class A emitter follower formed by an emitter follower connected to a current source. When the outputs are driven high, the emitter of driver **622** need supply only one-half the drive current as driver **612**. In this way, an impedance can be scaled in order to decrease a circuit's required drive current.

Also, the discharge current for driver **622** is only one half that of driver **612** for a given negative-going slew rate. Thus, the current source of **622** may be reduced by the same factor of one-half as compared to driver **612**. In this example, the bias current, that is the current in the pull-down current source can be reduced. Many other examples where drive currents and possibly bias currents may be reduced will be appreciated by one skilled in the art.

FIG. **7** illustrates another degree of freedom that made be employed to reduce current levels in a transceiver. Specifically, a gain element **720** may be inserted in front of a circuit block **730** in order to improve the combined circuit's signal-to-noise ratio by a factor equal to the gain of the inserted gain block. This is particularly useful when large interferers are absent and the desired received signal is moderate or low. Specifically, gain is added to the signal while impedances are increased, which raise the noise floor. In this way, a given signal-to-noise ratio may be maintained while the power is decreased.

The gain of such an element may be varied by increasing a current in a differential pair or increasing a load resistance using switches. Many other examples where the gain of this element may be varied will be appreciated by one skilled in the art.

These variables, or degrees of freedom, specifically reducing bias currents, increasing impedances, and increasing gain may be used as in the following examples.

FIG. **8A** is a block diagram of a functional block **820** and optional gain element **810** in accordance with an embodiment of the present invention. Functional block **820**, like the functional blocks in the following diagrams, may be a filter, mixer, amplifier, or other circuit or circuits in a wireless transceiver or other electronic circuits or system. An input signal is received on line **812** by the optional gain element **814**. When the optional gain block **810** is not used, the input signal may be received directly by the function block **820**. The gain of the optional gain element **812** is controlled by a gain control signal on line **814**. The functional block receives an output signal from the optional gain element **810** and provides an output VOUT on line **822**. The lines in this and the other included figures may be one or more lines, depending on whether single-ended, differential, or other type of signaling is employed.

One or more impedances are under control of signals on impedance control lines **824**. Similarly, one or more bias currents in the function block are under control of one or more signals on bias control lines **826**. These various control lines may be logic signals, analog signals, voltage or currents lines, or other signal or bias lines. In other embodiments of the present invention, the gain control element **810** may be included in the function block **820**. Also, various embodiments may not incorporate either or both the impedance control and bias control.

FIG. **8B** is an example input that may be present on line VIN **812**. In this example, a desired signal **836** is relatively weak, as are interfering signals **837** and **838**. The initial bias and circuit configuration is such that the noise floor **833** and maximum signal handling capability Smax **831** are adjusted for worst case conditions. The circuit of FIG. **8A**, as with all the circuits described here, receives noise at its input which may be referred to as input equivalent noise or input referred noise. Additionally, the circuit of FIG. **8A** generates noise which is added to the input referred noise. Depending on the gain characteristics of the circuitry, the output noise at various frequencies may be greater than, equal to, or less than the input referred noise. For simplicity, the noise floor and maximum signal handling capability Smax, in this and the other figures, are shown as straight lines, though the noise and Smax are typically curved as a function of frequency.

That the input spectrum is as shown in FIG. **8B** can be determined, for example, by low signal strength indications

on line VIN **812** and VOUT **822**. That is, a low level signal strength indication on line VIN **812** indicates that no portion of the input signal is particularly large.

For this exemplary input, there are at least two methods by which the power dissipation for this circuitry may be reduced. Depending on the exact circuits and structures used, one of these methods may be preferred.

In FIG. **8**C, the bias current is decreased, thereby lowering the maximum signal handling capability **841** as compared to **831**, closer to the desired and interfering signal levels. Again, the bias currents in the function block **820** may be reduced by switching impedances that appear across a voltage thereby changing a resulting bias current, by reducing a voltage at the gate of a MOS or base of a bipolar transistor, or by other methods.

In FIG. **8**D, a second method of reducing power dissipation in the function block **820** is employed. Specifically, Smax **851** is held constant as compared Smax **831**. The desired and interfering signals are amplified such that they are closer to the available signaling handling capability **851**. Also, the noise floor **853** is raised as compared to noise floor **833** in FIG. **8**B. Specifically, the noise contributed by the function block **820** is increased, such that the noise at its output is increased to noise floor **853**. This is done by increasing one or more impedance in function block **810**, such that drive currents inside that block are reduced. Depending on the exact configuration, this may also allow some biasing currents to be reduced, while maintaining the maximum signal handling capability **851** at a sufficient level. Alternately, these two methods of reducing power dissipation in function block **820** may be done in combination.

The included examples are explained for the exemplary situation where biasing and other parameters are set for worst-case conditions, and then changed to save power when it is discovered that the conditions are better-than-worst case. Alternately, the bias currents and other parameters may be set for maximum power savings, or an intermediate point, and the power can be adjusted from there.

FIG. **9**A illustrates a block diagram including an optional gain element **910** and function block **920**. Again, an input signal is received on line **912** by optional gain element **910** which in turn drives function block **920**. The function block provides an output VOUT on line **922**, and receives impedance and bias control signals on lines **924** and **926**.

FIG. **9**B shows the spectrum for what may be considered a best-case received signal. Specifically, the desired signal **936** is strong, while the interfering signals **937** and **938** are relatively weak. This may be determined, for example, by detecting a large signal level at the input line VIN **812** and a large signal level after a filter, since these readings would indicate that a large signal is received, but that it is at the desired signal frequency.

The maximum signaling capability **931** and noise floor **933** are shown as being set for the worst case conditions. In this case, the noise floor **933** is lower than the maximum allowed for proper signal reception. Accordingly, one or more impedance in the function block **920** may be increased, such that the noise floor **943** rises as shown in FIG. **9**C. In this way one or more of the driving currents in the function block **920** may be reduced. Similarly, since the drive current is reduced, one or more bias current may also be reduced, depending on the exact circuit configuration.

FIG. **10**A illustrates a block diagram showing an optional gain element **1010** driving a function block **1020**. An input signal is received by the gain element **1010** on line **1012**, and an output is provided by function block **1020** on line VOUT **1022**. One or more gain control signals present on lines **1014** control the gain of gain control element **1010**, while one or more impedance and bias control signals are received by the function block **1020** on line to **1024** and **1026**.

FIG. **10**B illustrates a received signal that may be received on line VIN **1012**. In this example, the desired signal **1036** and interferers **1037** and **1038** are each relatively large. This may be determined, for example, by detecting a large signal level at the input line VIN **812** and a smaller signal level after a filter, since these readings would indicate that a large signal is received, but that interferers are being reduced.

As before, in this example, the noise floor **1033** and maximum signal handling capability **1031** are initially set for the worst case conditions. Since the desired signal is relatively large in this case, the noise floor may be allowed to rise, a shown by noise floor **1043** in FIG. **10**C. Since the desired signal **1046** and interferers **1047** are large, the maximum signal handling capability Smax **1041** remains constant. Again, the noise floor is increased by increasing impedances in the function block **1020**. This reduces the required drive current, and may also allow for a reduction in bias currents.

FIG. **11**A illustrates a block diagram including an optional gain element **1110** and function block **1120** in accordance with an embodiment of the present convention. An input signal is received on line **1112** by the optional gain control element **1110**, while an output signal is provided by the function block **1120** on line VOUT **1122**. Gain, impedance, and bias control signals are received on lines **1114**, **1124**, and **1126**.

FIG. **11**B is an exemplary input signal that may be received by the gain control element **1110** on line VIN **1112**. In this specific example, the desired signal **1136** is relatively low or weak while the interfering signals **1137** and **1138** are large. This may be determined, for example, by detecting a large signal level at the input line VIN **812** and a much smaller signal level after a filter, since these readings would indicate that a large signal is received and that large interferers are being reduced such that the resulting signal, the desired signal, is relatively weak.

Again, the maximum signal handling capability **1131** and noise floor **1133** are initially set for worst case conditions. If the desired signal is sufficiently low, while the interferers are sufficiently high, power savings may not be achievable over the worst case settings, since this is in fact the worst case condition. But, if the desired signal is somewhat larger than the worst case condition, then power may be saved in at least two different ways.

For example, FIG. **11**C shows the maximum signal handling capability **1141** being lowered. In this case, the interfering signals **1147** in **1148** began to clip and distort, thereby creating intermodulation products **1145**, which distort the desired signal **1146**. So long as care is taken to not corrupt the desired signal **1146** beyond an acceptable limit, typically measured by a bit-error rate, power may be reduced in this way.

Similarly, in FIG. **11**D, the noise floor **1153** is raised somewhat, thereby saving power. Again, this may be done so long as the noise floor is not sufficiently high that the system bit-error rate becomes unacceptable.

FIG. **12** is a summary of the above four examples. The received signal strengths are shown in column **1210**, while appropriate power saving responses are listed in column **1220**. Specifically, in row **1230**, the desired signal and interferer signal strengths are both weak or small. In this case, proper responses include decreasing Smax, or increasing one or more circuit impedances while increasing the circuit gain. Depending on the exact circuit configuration,

one of these options may be preferred over the other. Alternately, they may be done in combination, or done in combination with other power saving techniques. Also, in some specific embodiments, when both desired signal and interferer signal strengths are small, the gain may need to be increased while the impedance is maintained or not increased in order to keep the noise floor low.

In row **1240**, the desired signal strength is strong or large, while the interfering signals are small. In this case, an appropriate response is to increase one or more of the circuit impedances. Again, depending on the exact circuit in question, one or more of the bias currents may also be reduced.

In row **1250**, both the desired signals and interfering signal strengths are large. Again, in this case an appropriate response is to increase one or more of the circuit impedances.

In row **1260**, the received desired signal strength is weak or small, while the interfering signals are large. Since this is the worst case situation for which the circuit is designed, substantial power savings are difficult to achieve. However, again, if the received signal is above a minimum level necessary for proper operation, some distortion of the interferers or raising of the noise floor may be acceptable.

It should be noted that not all possible signal conditions are listed here. For example, either the signal or interferer may be of a relatively medium strength, or the interferer may be absent. Also, these terms are for exemplary purposes and are not meant to convey specific signal conditions, but rather are only qualitative. The proper response to a specific condition depends on the embodiment of the present invention, the particular circuit topology, the requirements of the signaling standard used, as well as other constraints.

FIG. **13** is an example shown how power may be saved as a function of time by employing one or more of these methods consistent with embodiments of the present invention. Power is plotted along a Y-axis **1304** as a function of time along X-axis **1302**. Conventional worst case design would fix power dissipation at line **1310**. As can be seen, dynamic power dissipation **1320** under the control of variable gains, impedances, biasing, or combination thereof, allows for a lower average power **1330** as compared to the power dissipated **1310** by the conventional design.

FIG. **14** is a block diagram of a portion of a receiver consistent with an embodiment of the present invention. Included are low-noise amplifier **1410**, mixer **1420**, gain stage **1430**, filter **1440**, AGC amplifier **1450**, and VCO **1460**. Signal strength detection is done at the output of the low-noise amplifier by signal strength indicator **1470**, at the output of the mixer by signal strength indicator **1472**, and at the output of the filter by signal strength indicator **1474**. The outputs of the signal strength indicator circuits are received by the computational circuit **1470**, which in turn controls gain and power control circuits **1480** and **1485**. Power and gain control circuits **1480** and **1485** control the gain, biasing, and impedance levels of the circuits in the receiver signal path. Also, the gain and power control circuits may control the same parameters in the VCO **1460**. This figure is greatly simplified for purposes of explanation. For example, the quadrature nature of the mixers and following circuits are not shown. Also, power-down and start-up circuits are not included.

The current level in the low-noise amplifier determines a multitude of parameters including voltage gain, linearity, input impedance matching, and noise figure. When conditions are better than worst-case, some of these parameters may be relaxed while maintaining an acceptable bit-error rate, thus saving power.

The bias current in the mixers effect that block's noise figure and linearity. Care is taken in reducing power in this block so as not to increase nonlinearities, particularly the third-order nonlinearity as measured by IP3, the third-order intercept point, beyond an acceptable limit.

A key parameter of the VCO is phase noise, an increase in which increases the sidebands on either side of the oscillation signal. During transmission, the phase noise should be kept low to avoid interference with adjacent channels and for preserving modulation information.

During reception however, if the conditions are better than worst case, the phase noise requirement for the VCO is relaxed, and power can be saved consistent with embodiments of the present invention. The achievable phase noise power spectral density is approximately inversely proportional to the bias current used. Thus, when low phase noise is not required during reception, bias current in the VCO can be reduced.

Most of the power savings in a transceiver in accordance with embodiments of the present invention is achieved in the receiver portion. Additional power may be saved in the transmitter section.

FIG. **15** is a block diagram of a transmitter portion consistent with an embodiment of the present invention. Included is a signal path formed by gain stage **1510** and power amplifier **1520**. The output power level is sensed by output level sensing circuit **1550**, which in turn adjusts the biasing of the power amplifier **1520** through the power control circuit **1540**. Additionally, a transmitter level control signal is received by power control circuits **1530** and **1540**, which in turn control the biasing of gain stage **1510** and power amplifier **1520**. Gain control circuit **1560** also adjusts the gain of gain stage **1510** and power amplifier **1520**. Additional circuitry that varies impedances in each of these circuits may also be included.

Since the gain, impedance and biasing of these blocks are being dynamically varied, care must be taken to not negatively affect the signal being processed. For example, specific embodiments of the present invention perform some or all of these variations during preamble. Also, as changes occur, the circuits in some embodiments are limited such that they may only adapt to an improvement in conditions after frames are completed. If conditions worsen, the circuits may be allowed to change in order to save the data. Alternately, a system may be manually calibrated, for example at set up, and when the network configuration is changed.

The above description of specific embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form described, and many modifications and variations are possible in light of the teaching above. The embodiments were chosen and described in order to best explain the principles of the invention and its practical applications to thereby enable others skilled in the art to best utilize the invention in various embodiments and with various modifications as are suited to the particular use contemplated.

What is claimed is:

1. A method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, and a corresponding increase in battery life of the battery powered portable wireless device, the method comprising:

receiving a wireless signal having a desired signal and an interferer signal, by the wireless transceiver of the battery powered portable wireless device, the wireless

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transceiver having a receiver signal path comprising a plurality of circuits, wherein the plurality of circuits includes an amplifier, a filter, and a mixer, and wherein the wireless transceiver comprises a circuit for determining a signal strength of the interferer signal and a circuit for determining a signal strength of the desired signal;

wherein a worst-case power dissipation condition results when the signal strength of the desired signal is low and the signal strength of the interferer signal is high; and

wherein the power dissipation reduction in the receiver is achieved by causing a bias current to vary in one or more of the plurality of circuits in the receiver signal path of the wireless transceiver as the signal strength of the interferer signal and the signal strength of the desired signal vary according to the following:

(i) when the signal strength of the interferer signal is high and the signal strength of the desired signal is low, and the desired signal is larger than in the worst-case power dissipation condition, causing the bias current of the one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be reduced compared to the worst-case power dissipation condition, thereby saving power; and

(ii) when the signal strength of the interferer signal is weak and the signal strength of the desired signal is weak, causing the bias current of the one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be decreased compared to the worst-case power dissipation condition, thereby saving power.

2. The method of claim 1, wherein the change in the bias current of the one or more of the plurality of circuits in the receiver signal path is related to a change in an impedance in the one or more of the plurality of circuits in the receiver signal path and wherein the impedance comprises at least a resistor and a capacitor.

3. A method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, and a corresponding increase in battery life of the battery powered portable wireless device, the method comprising:

receiving a wireless signal having a desired signal and an interferer signal, by the wireless transceiver of the battery powered portable wireless device, the wireless transceiver having a receiver signal path comprising a plurality of circuits, wherein the plurality of circuits includes an amplifier, a filter, and a mixer, and wherein the wireless transceiver comprises a circuit for determining a signal strength of the interferer signal and a circuit for determining a signal strength of the desired signal;

wherein a worst-case power dissipation condition from the battery results when the signal strength of the desired signal is low and the signal strength of the interferer signal is high; and

wherein the power dissipation reduction in the receiver is achieved by causing a bias current to vary in one or more of the plurality of circuits in the receiver signal path of the wireless transceiver as the signal strength of the interferer signal and the signal strength of the desired signal vary, according to the following:

when the signal strength of the interferer signal is high and the signal strength of the desired signal is low, and the desired signal has a signal strength that is larger than in the worst-case power dissipation conditions, causing the bias current of the one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be decreased compared to the worst-case power dissipation condition, causing a reduction in power dissipation.

4. The method of claim 3, wherein the change in the bias current of the one or more of the plurality of circuits in the receiver signal path is related to a change in an impedance in the one or more of the plurality of circuits in the receiver signal path;

and wherein the impedance comprises at least a resistor and a capacitor.

5. A method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, and a corresponding reduction in a drain on battery life of the battery powered portable wireless device, the method comprising:

receiving a wireless signal having a desired signal and an interferer signal, by the wireless transceiver of the battery powered portable wireless device, the wireless transceiver having a receiver signal path comprising a plurality of circuits, wherein the plurality of circuits includes an amplifier, a filter, and a mixer, and wherein the wireless transceiver comprises a circuit for determining a signal strength of the interferer signal and a circuit for determining a signal strength of the desired signal;

wherein a worst-case power dissipation condition results when the signal strength of the desired signal is low and the signal strength of the interferer signal is high; and

wherein the power dissipation reduction in the receiver is achieved by causing a bias current to vary in one or more of the plurality of circuits in the receiver signal path of the wireless transceiver as the signal strength of the interferer signal and the signal strength of the desired signal vary, according to the following:

(i) when the signal strength of the interferer signal is high and the signal strength of the desired signal is weak, and the desired signal is larger than in the worst-case power dissipation condition, causing the bias current of the one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be reduced compared to the worst-case power dissipation condition, thereby saving power;

(ii) when the signal strength of the interferer signal is high and the signal strength of the desired signal is high, causing the bias current of the one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be decreased compared to the worst-case power dissipation condition, thereby saving power;

(iii) when the signal strength of the interferer signal is weak and the signal strength of the desired signal is weak, causing the bias current of the one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be decreased compared to the worst-case power dissipation condition, thereby saving power; and

(iv) when the signal strength of the interferer signal is weak and the signal strength of the desired signal is high, causing the bias current of the one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be decreased compared to the worst-case power dissipation condition, thereby saving power.

6. The method of claim 5, wherein the change in the bias current of the one or more of the plurality of circuits in the

receiver signal path is related to a change in an impedance in the one or more of the plurality of circuits in the receiver signal path;

and wherein the impedance comprises at least a resistor and a capacitor.

7. A method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, and a corresponding reduction in a drain on battery life of the battery powered portable wireless device, the method comprising:

receiving a wireless signal having a desired signal and an interferer signal, by the wireless transceiver of the battery powered portable wireless device, the wireless transceiver having a receiver signal path comprising a plurality of circuits, wherein the plurality of circuits includes an amplifier, a filter, and a mixer, and wherein the wireless transceiver comprises a circuit for determining a signal strength of the interferer signal and a signal strength of the desired signal in the receiver signal path;

wherein a worst-case power dissipation condition in the receiver results when the signal strength of the desired signal is low and the signal strength of the interferer signal is high; and

wherein the power dissipation reduction is achieved by causing an impedance and a bias current of one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to vary as the signal strength of the interferer signal and the signal strength of the desired signal to vary according to the following:

(i) when the signal strength of the interferer signal is high and the signal strength of the desired signal is low and the desired signal is larger than in the worst-case power dissipation conditions, causing the bias current of the circuit in the receiver signal path of the wireless transceiver to be reduced compared to the worst-case power dissipation condition, causing a reduction in power dissipation;

(ii) when the signal strength of the interferer signal is high and the signal strength of the desired signal is high, causing the impedance of the circuit in the receiver signal path of the wireless transceiver to be increased compared to the worst-case power dissipation condition, causing a reduction in power dissipation;

(iii) when the signal strength of the interferer signal is low and the signal strength of the desired signal is low, causing the bias current of the circuit in the receiver signal path of the wireless transceiver to be reduced compared to the worst-case power dissipation condition, causing a reduction in power dissipation;

(iv) when the signal strength of the interferer signal is low and the signal strength of the desired signal is high, causing the impedance of the circuit in the receiver signal path of the wireless transceiver to be increased compared to the worst-case power dissipation condition, causing a reduction in power dissipation; and

wherein increasing the impedance of the circuit reduces a drive current of the circuit and reduces the associated bias current of the circuit.

8. A method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, and a corresponding reduction in power dissipation and an increase in battery life of the battery powered portable wireless device, the method comprising:

receiving a wireless signal having a desired signal and an interferer signal, by the wireless transceiver of the battery powered portable wireless device, the wireless transceiver having a receiver signal path comprising a plurality of circuits, wherein the plurality of circuits includes an amplifier, a filter, and a mixer, and wherein the wireless transceiver comprises a circuit for determining a signal strength of the interferer signal and a circuit for determining a signal strength of the desired signal;

wherein a worst-case power dissipation condition from the battery results when the signal strength of the desired signal is low and the signal strength of the interferer signal is high; and

wherein the power dissipation reduction in the receiver is achieved by causing a bias current and an impedance to vary in one or more of the plurality of circuits in the receiver signal path of the wireless transceiver as the signal strength of the interferer signal and the signal strength of the desired signal vary, according to the following:

when the signal strength of the interferer signal is high and the signal strength of the desired signal is low, and the desired signal has a signal strength that is larger than in the worst-case power dissipation condition, causing:

(i) the bias current of the one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be decreased; and

(ii) an impedance of the one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be increased, thereby causing a drive current of the one or more of the plurality of circuits to be decreased.

* * * * *

Exhibit C

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Tsividis

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(54) **POWER DISSIPATION REDUCTION IN WIRELESS TRANSCEIVERS**

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H04M 1/00 (2006.01)
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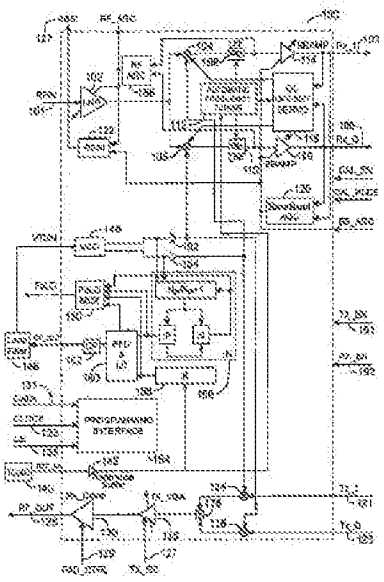
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(57) **ABSTRACT**

Methods and circuits for reducing power dissipation in wireless transceivers and other electronic circuits and systems. Embodiments of the present invention use bias current reduction, impedance scaling, and gain changes either separately or in combination to reduce power dissipation. For example, bias currents are reduced in response to a need for reduced signal handling capability, impedances are scaled thus reducing required drive and other bias currents in response to a strong received signal, or gain is increased and impedances are scaled in response to a low received signal in the presence of no or weak interfering signals.

23 Claims, 15 Drawing Sheets



Related U.S. Application Data

continuation of application No. 11/318,646, filed on Dec. 27, 2005, now Pat. No. 9,331,728, which is a continuation of application No. 10/784,613, filed on Feb. 23, 2004, now Pat. No. 7,010,330.

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See application file for complete search history.

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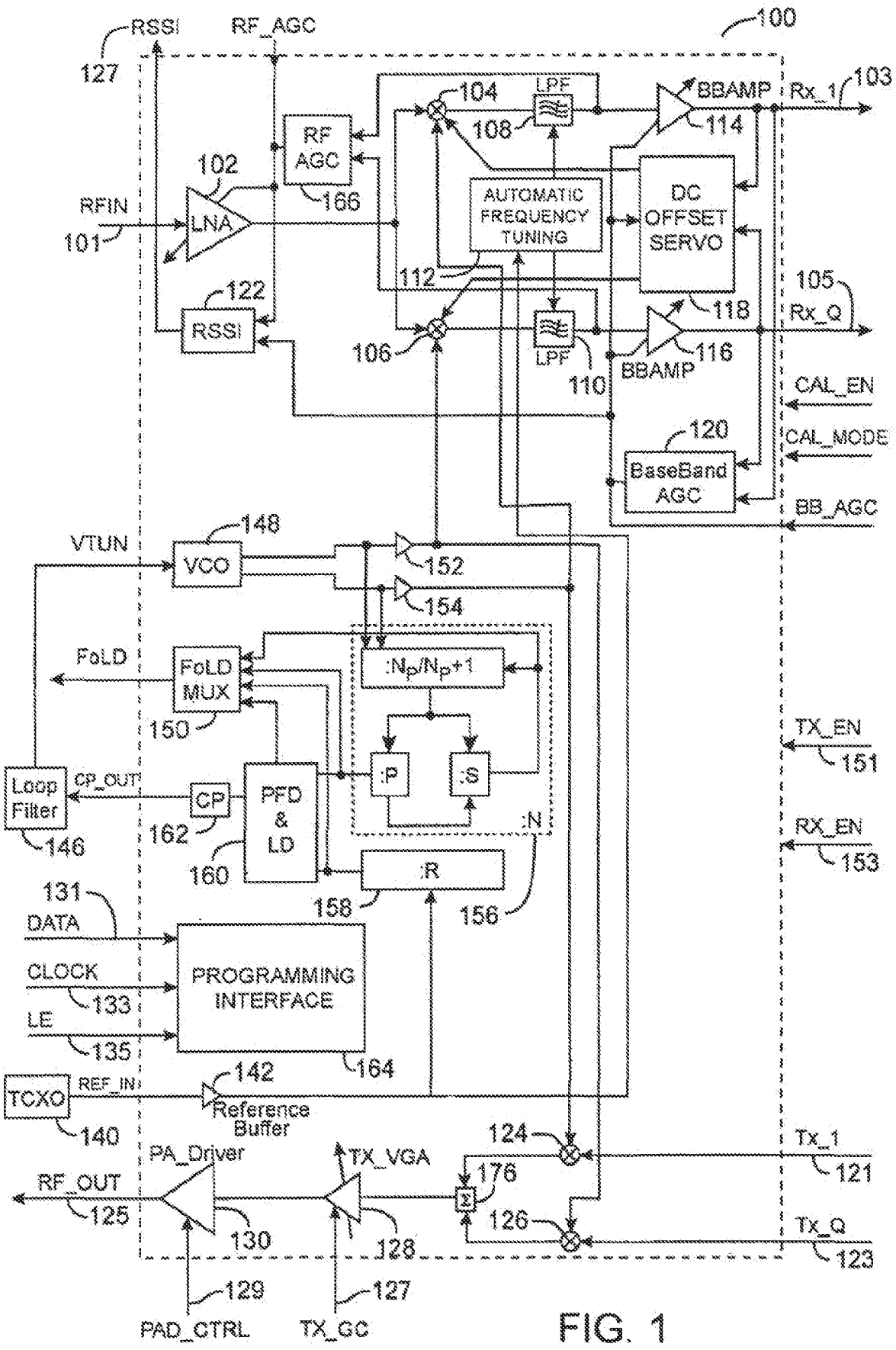

RSSI
RF_AGC
100
127
104
LPF
BBAMP
Rx_1
103
108
114
RF AGC
166
102
RFIN
LNA
101
AUTOMATIC FREQUENCY TUNING
DC OFFSET SERVO
112
105
Rx_Q
122
RSSI
118
106
LPF
BBAMP
116
110
CAL_EN
CAL_MODE
120
BaseBand AGC
BB_AGC
VTUN
148
VCO
152
154
FoLD
FoLD MUX
150
:Np/Np+1
TX_EN
151
Loop Filter
146
CP_OUT
CP
162
PFD & LD
160
:P
:S
:N
:R
158
156
RX_EN
153
131
DATA
CLOCK
133
LE
135
PROGRAMMING INTERFACE
164
TCXO
140
REF_IN
142
Reference Buffer
124
Tx_1
121
PA_Driver
TX_VGA
RF_OUT
125
176
2
126
Tx_Q
123
130
128
129
127
PAD_CTRL
TX_GC

FIG. 1

Case: 1:22-cv-03441 Document #: 1 Filed: 07/05/22 Page 6 of 62 PageID #:62

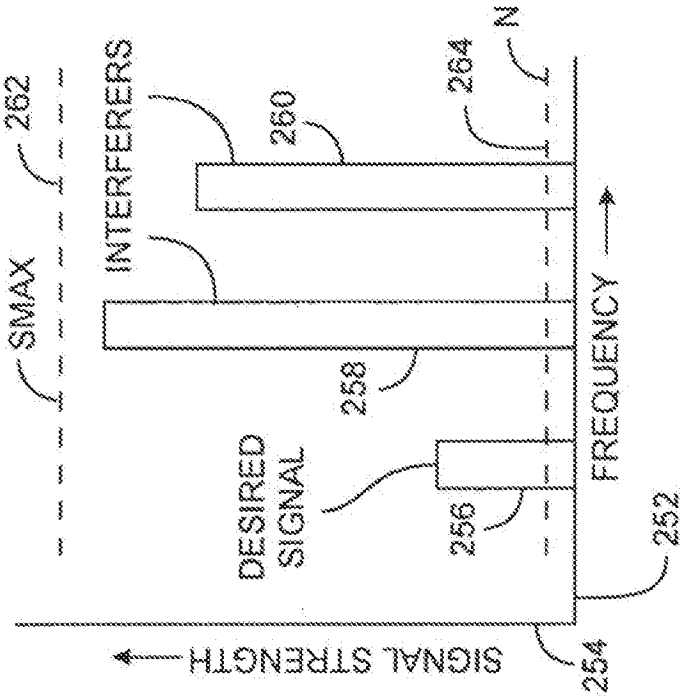


FIG. 2B

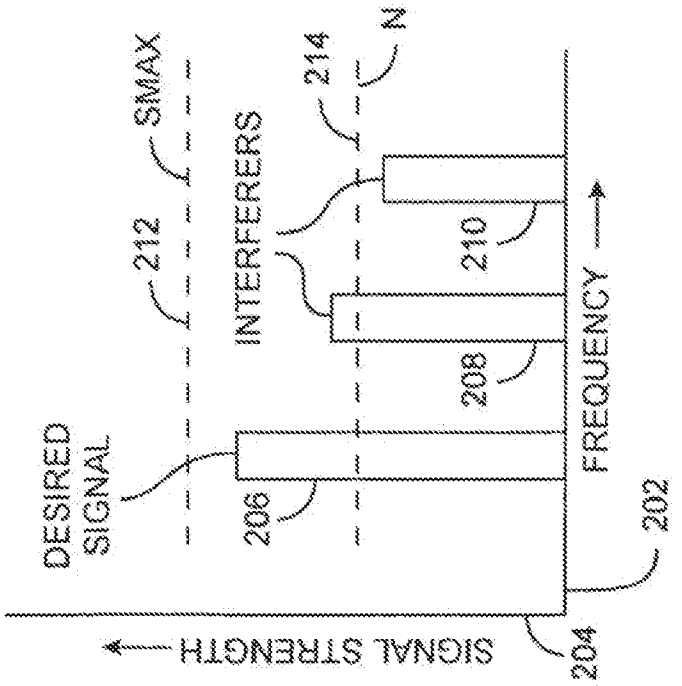


FIG. 2A

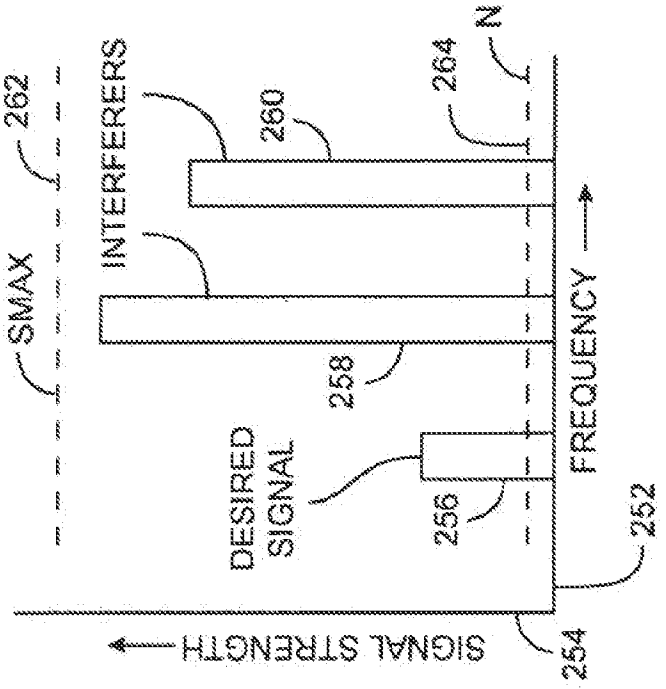

SMAX
262
INTERFERERS
260
264
N
258
DESIRED SIGNAL
256
FREQUENCY
252
SIGNAL STRENGTH
254

FIG. 2B

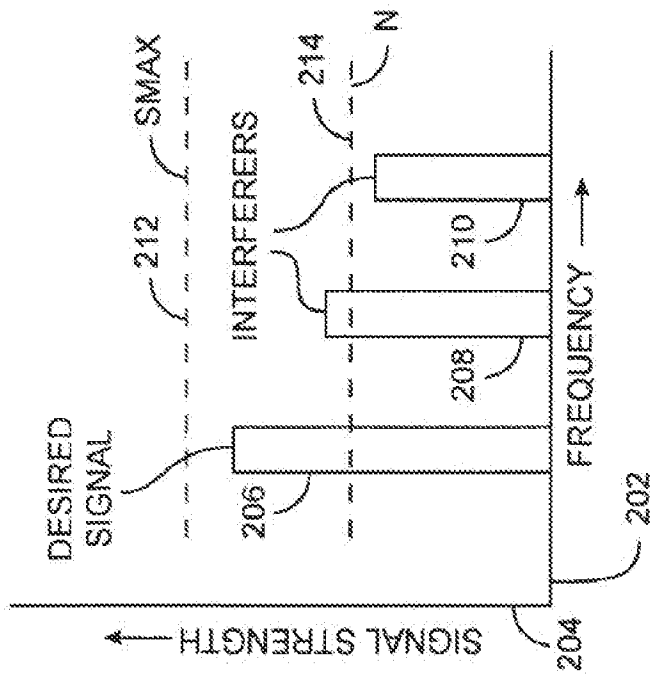

SMAX
212
214
N
INTERFERERS
210
208
DESIRED SIGNAL
206
FREQUENCY
202
SIGNAL STRENGTH
204

FIG 2A

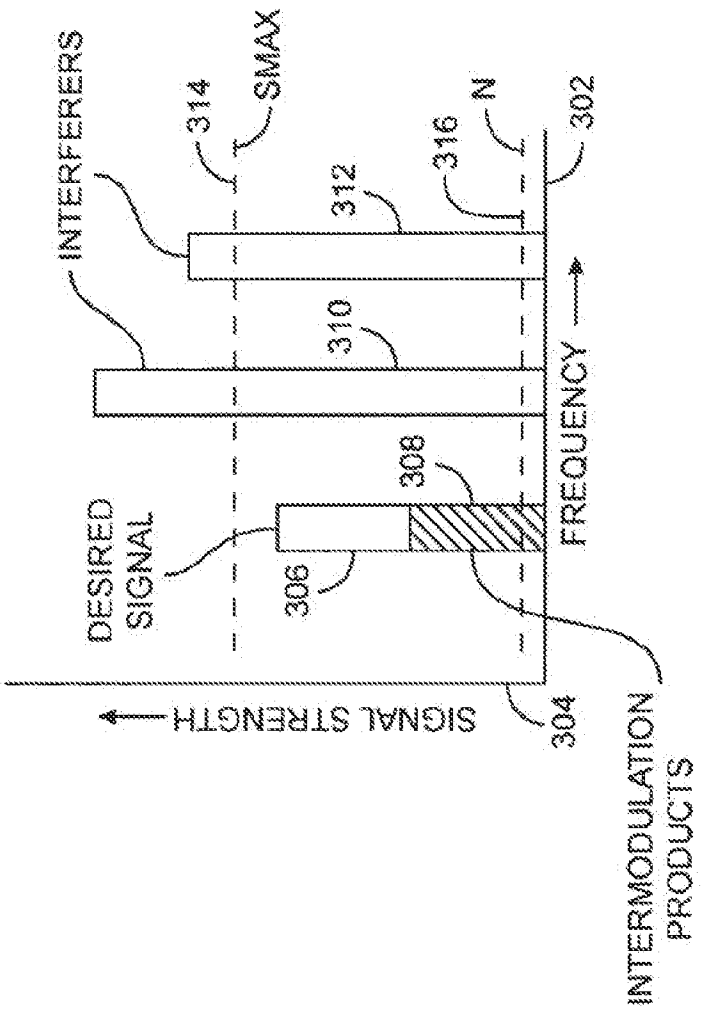

INTERFERERS
314
SMAX
312
316
N
302
310
308
DESIRED SIGNAL
306
FREQUENCY
SIGNAL STRENGTH
304
INTERMODULATION PRODUCTS

FIG. 3

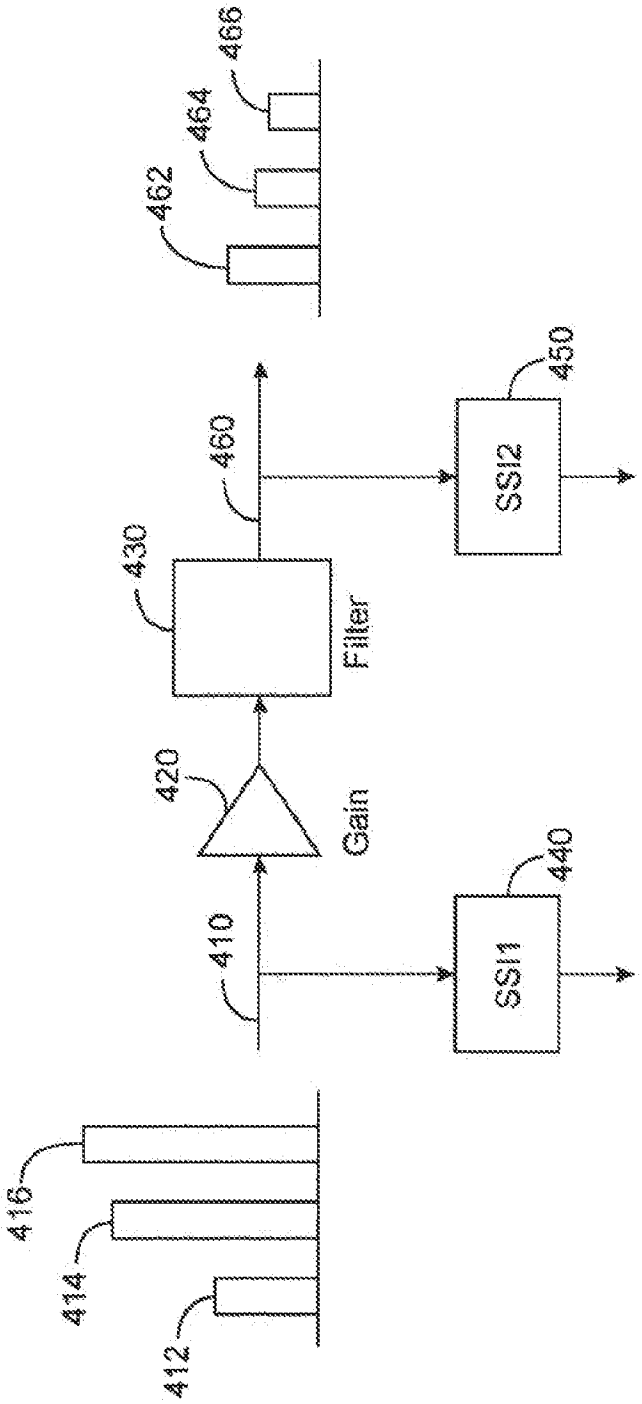

466
464
462
460
450
SSI2
430
Filter
420
Gain
410
440
SSI1
416
414
412

FIG. 4

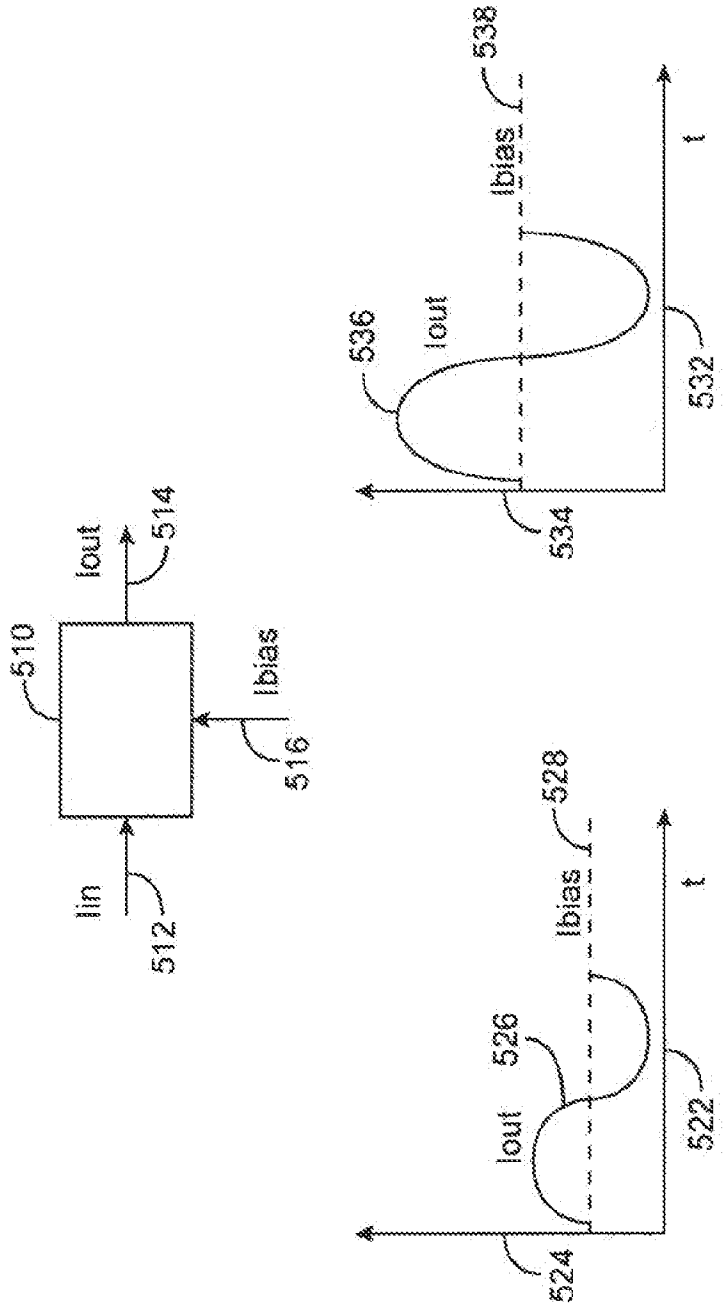

510
Iin
512
Iout
514
Ibias
516
524
Iout
526
Ibias
528
522
t
534
536
Iout
Ibias
538
532
t

FIG 5

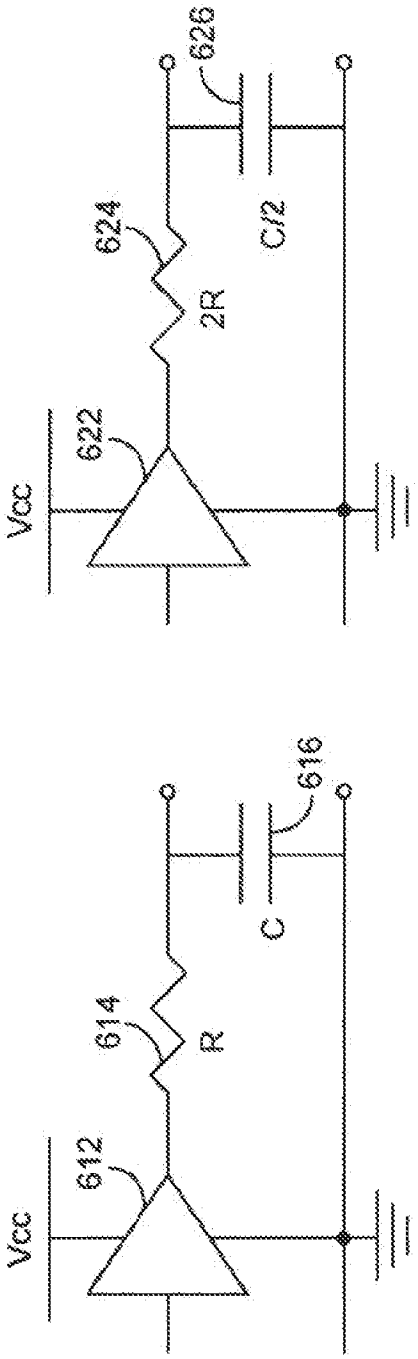


FIG 6

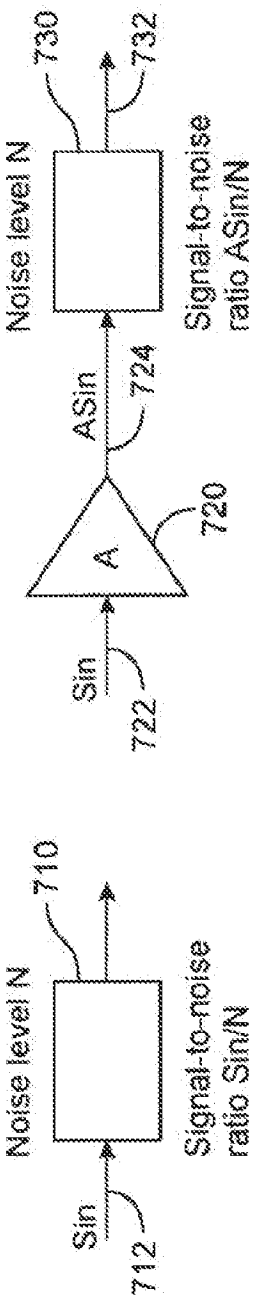

730
732
Noise level N
Signal-to-noise ratio ASin/N
ASin
724
A
720
Sin
722
710
Noise level N
Signal-to-noise ratio Sin/N
Sin
712

FIG. 7

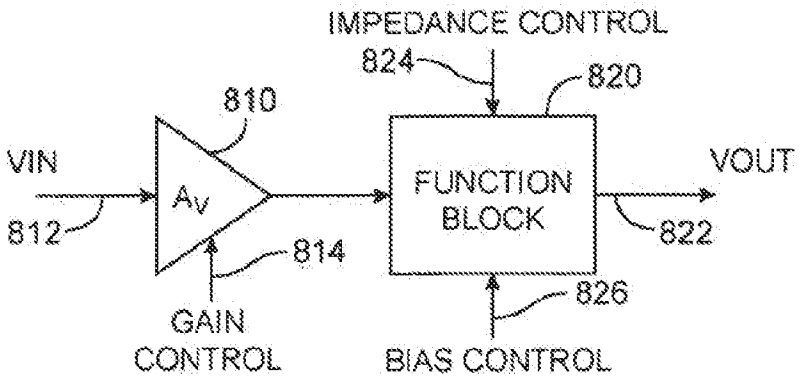


FIG. 8A

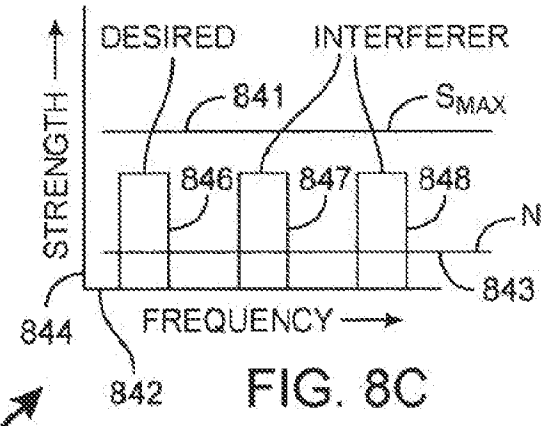


FIG. 8C

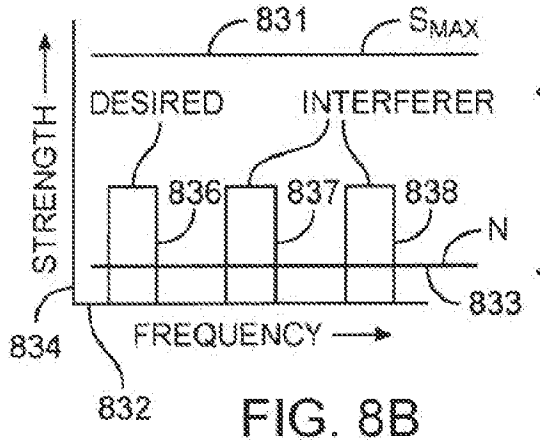


FIG. 8B

DECREASE BIASING

– AND/OR –

INCREASE GAIN AND IMPEDANCES

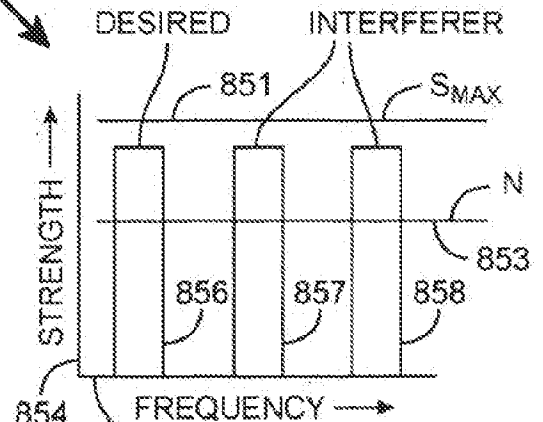


FIG. 8D

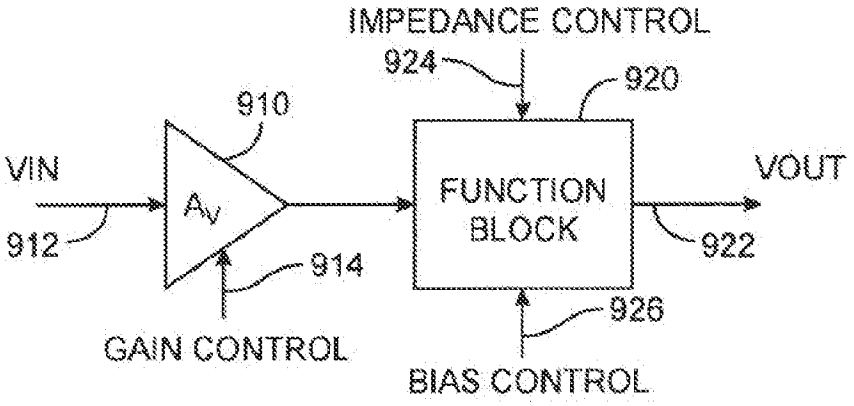


FIG. 9A

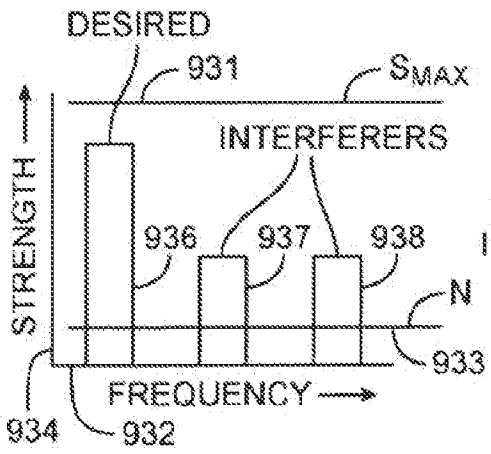


FIG. 9B

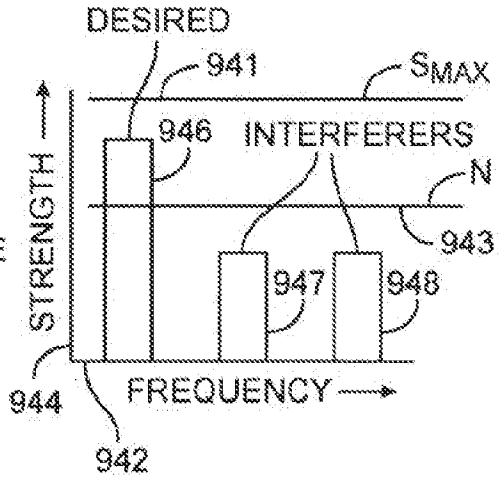


FIG. 9C

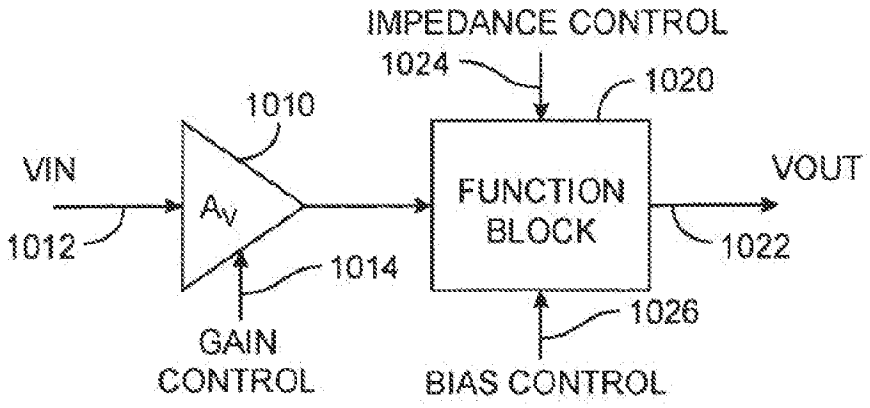


FIG. 10A

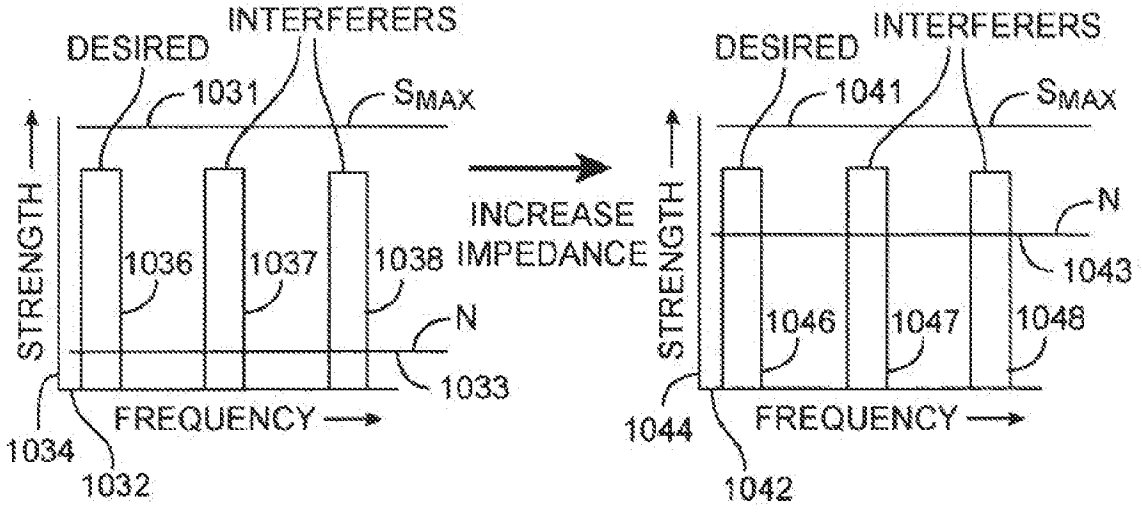


FIG. 10B

FIG. 10C

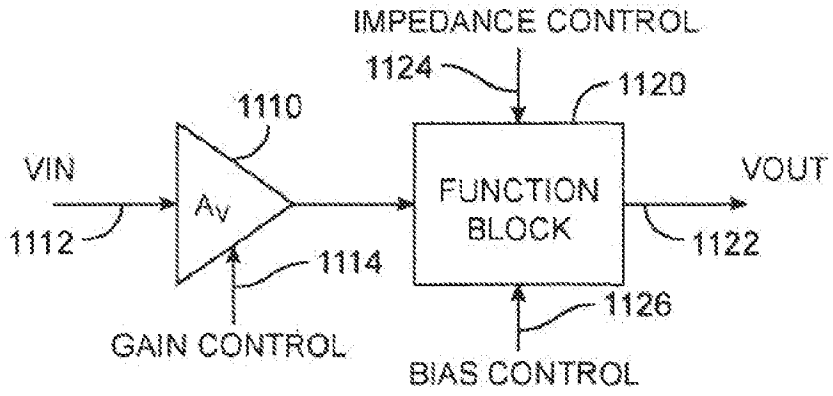


FIG. 11A

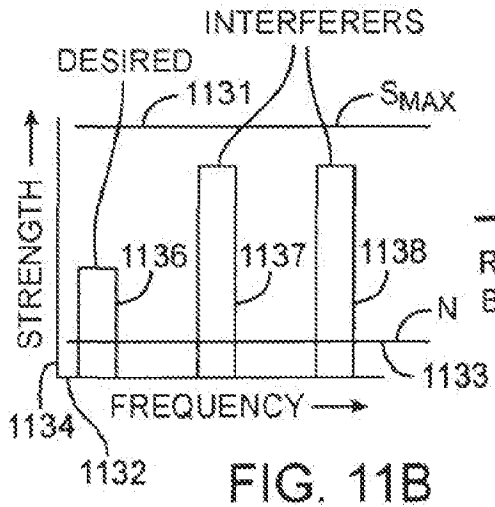


FIG. 11B

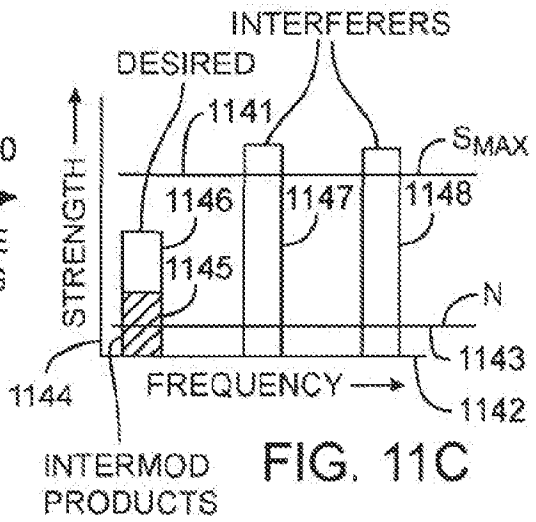


FIG. 11C

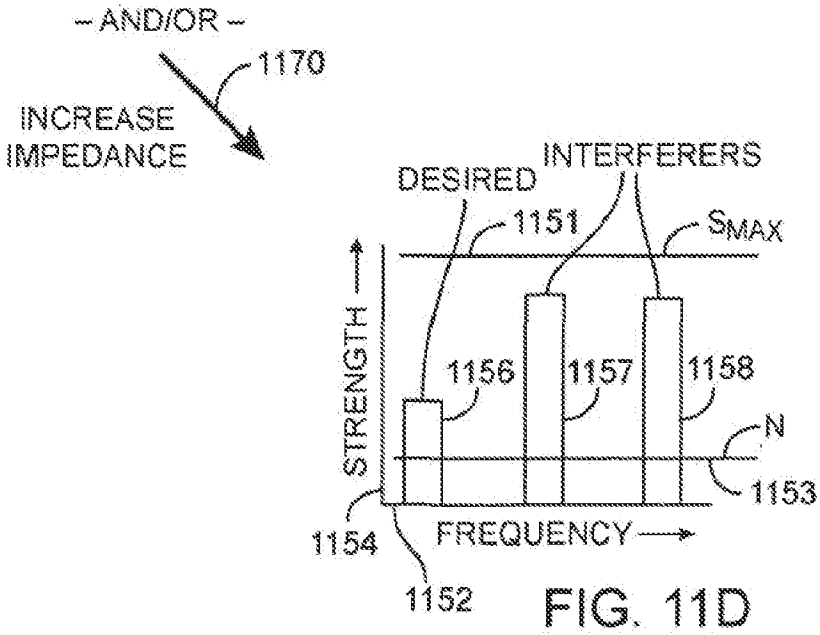


FIG. 11D

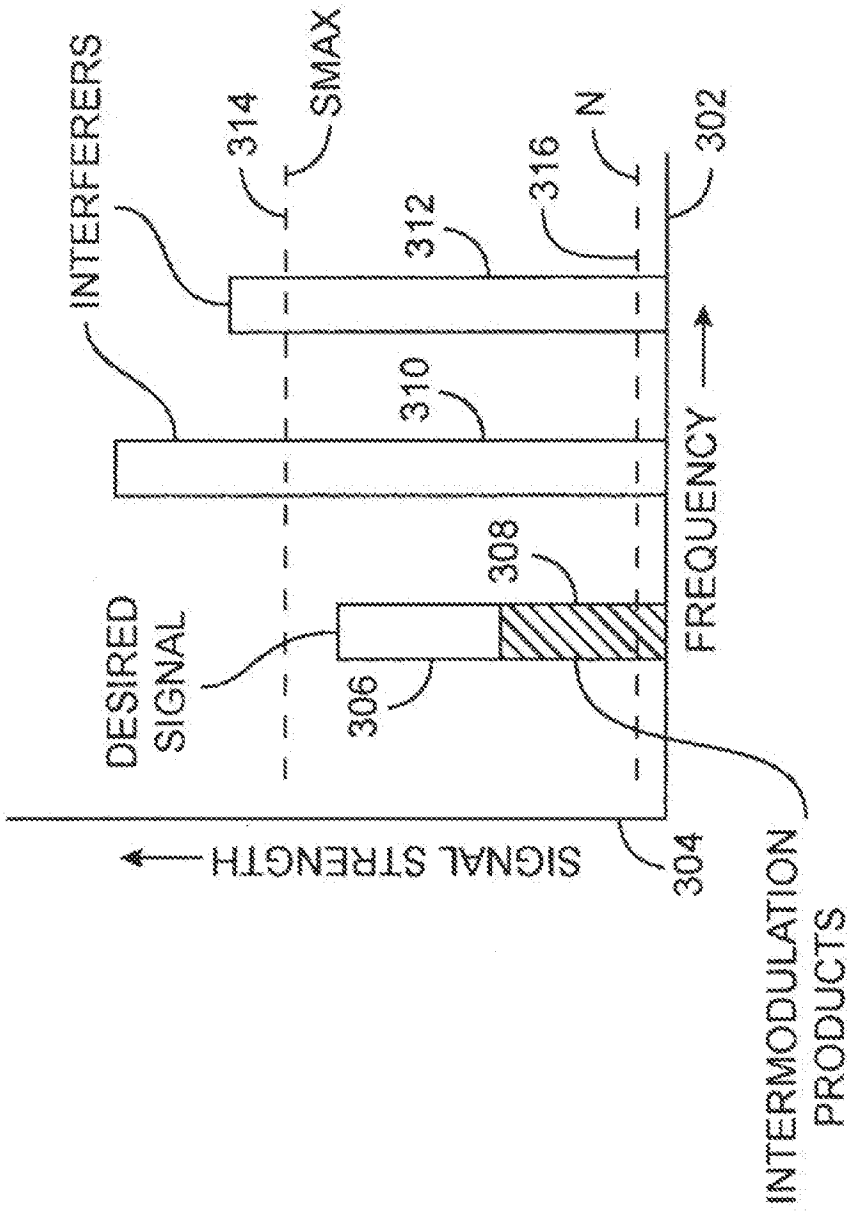

INTERFERERS
314
SMAX
312
316
N
302
310
308
DESIRED SIGNAL
306
FREQUENCY
SIGNAL STRENGTH
304
INTERMODULATION PRODUCTS

FIG. 3

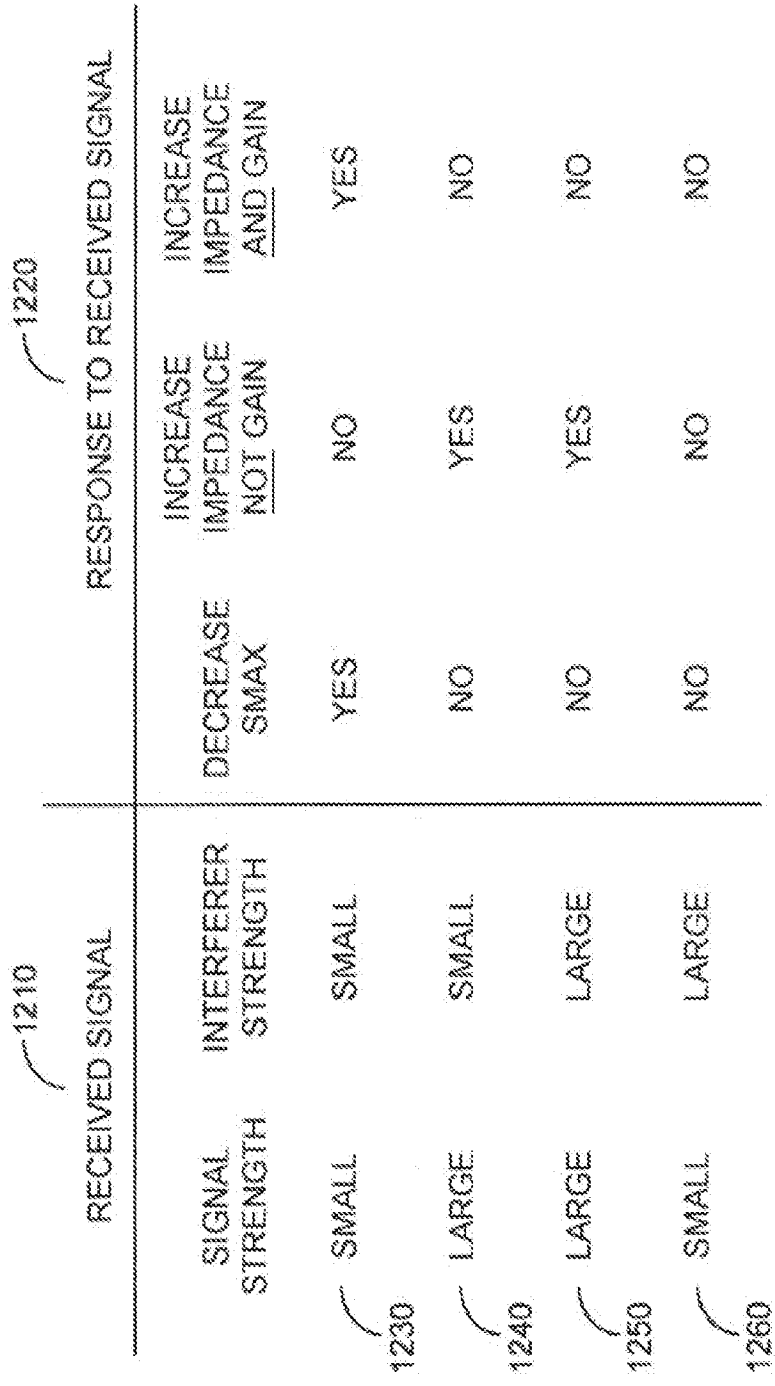

1210
RECEIVED SIGNAL
1220
RESPONSE TO RECEIVED SIGNAL
SIGNAL STRENGTH
INTERFERER STRENGTH
DECREASE SMAX
INCREASE IMPEDANCE NOT GAIN
INCREASE IMPEDANCE AND GAIN
SMALL
SMALL
YES
NO
YES
1230
LARGE
SMALL
NO
YES
NO
1240
LARGE
LARGE
NO
YES
NO
1250
SMALL
LARGE
NO
NO
NO
1260

FIG. 12

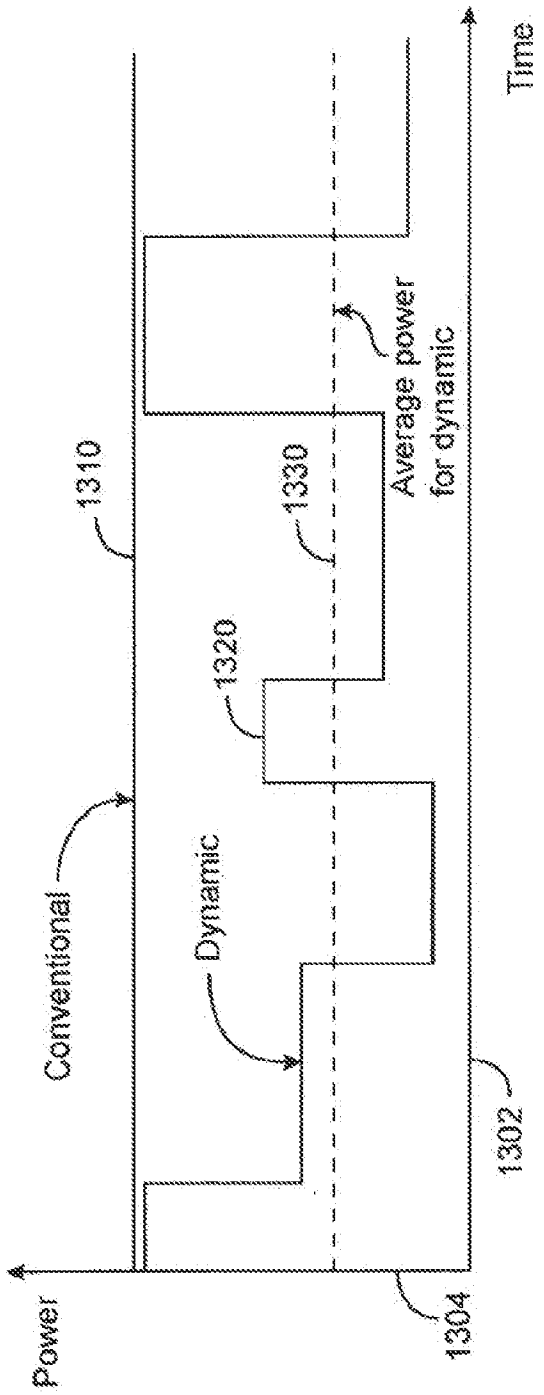

Power
Time
Conventional
Dynamic
1310
1320
1330
1302
1304
Average power for dynamic

FIG 13

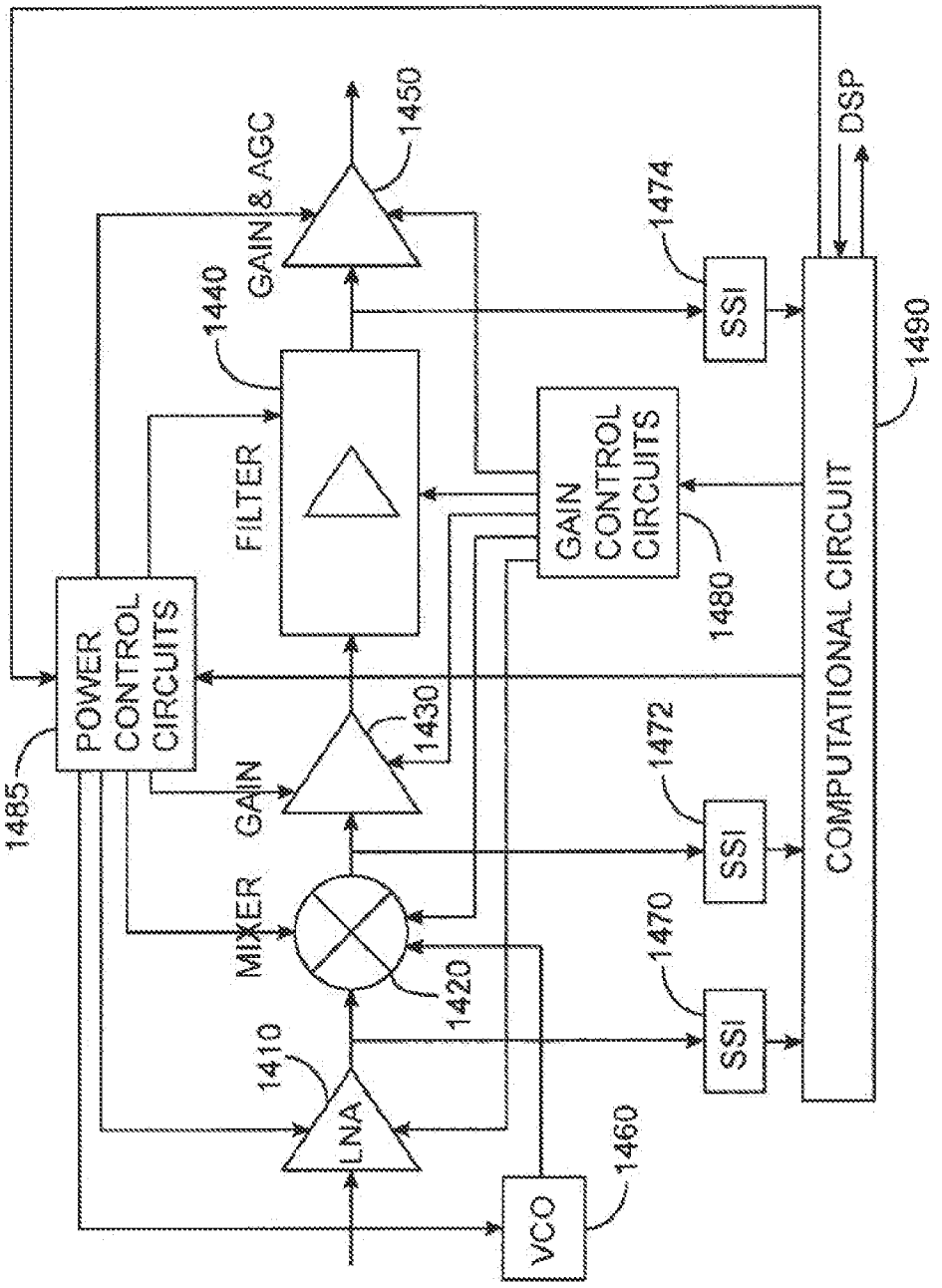

1485
POWER CONTROL CIRCUITS
1410
LNA
1420
MIXER
1430
GAIN
1440
FILTER
1450
GAIN & AGC
1460
VCO
1470
SSI
1472
SSI
1474
SSI
1480
GAIN CONTROL CIRCUITS
1490
COMPUTATIONAL CIRCUIT
DSP

FIG. 14

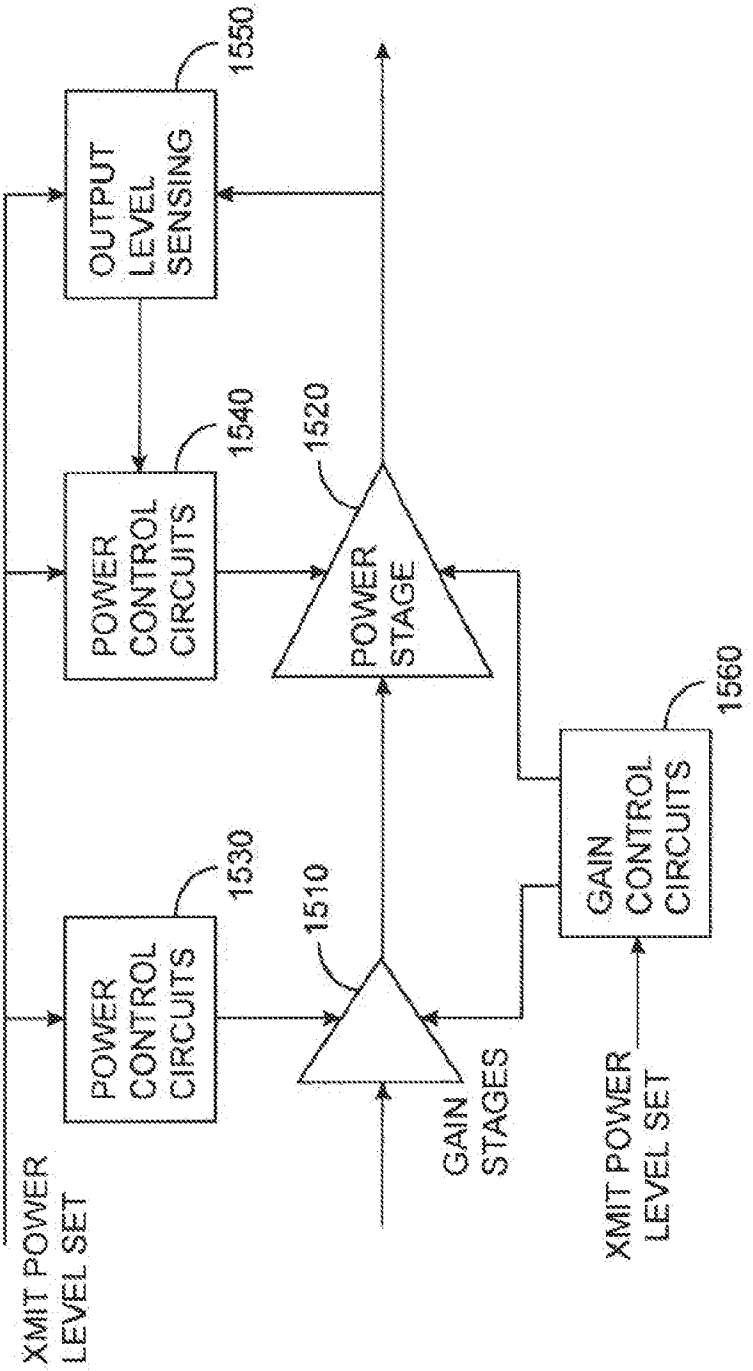

XMIT POWER LEVEL SET
POWER CONTROL CIRCUITS
1530
1510
GAIN STAGES
POWER CONTROL CIRCUITS
1540
1520
POWER STAGE
OUTPUT LEVEL SENSING
1550
XMIT POWER LEVEL SET
GAIN CONTROL CIRCUITS
1560

FIG. 15

POWER DISSIPATION REDUCTION IN WIRELESS TRANSCEIVERS

CROSS-REFERENCES TO RELATED APPLICATIONS

This application is a continuation of U.S. patent application Ser. No. 15/080,421, filed Mar. 24, 2016, which is a continuation of U.S. patent application Ser. No. 11/318,646, filed Dec. 27, 2005, which is a continuation of U.S. patent application Ser. No. 10/784,613, filed Feb. 23, 2004, which claims the benefit of U.S. provisional application No. 60/451,229, filed Mar. 1, 2003, which is incorporated by reference.

This application claims the benefit of U.S. provisional application No. 60/451,230, filed Mar. 1, 2003, which is incorporated by reference.

BACKGROUND

The present invention relates to power dissipation reduction techniques for electronic circuits, for example wireless transceiver integrated circuits.

Wireless networking is quickly becoming ubiquitous, as desktop, notebook, and handheld computers are connected to share Internet access and files. Wireless networking cards compatible with PCMCIA and compact flash form factors are popular for laptops and handhelds respectively, particularly as mobile users connect to the Internet on the road at coffee shops, hotels, and airports.

A downside of this connectivity is a corresponding drain on battery life, especially for these portable devices. The power consumed by a wireless transmitter and receiver reduces the usefulness of a device and sends a user on a hunt for an electrical outlet for recharging.

One reason why this power drain is high is that electronic circuits are typically designed to function properly under worst-case operating conditions. For a wireless transceiver, the worst case condition is when a desired signal reception strength is low, while other transceivers or nearby electronic equipment generate interfering signals and other spurious noise.

But a wireless transceiver does not always operate in these worst-case conditions. For example, a base station, router or access point may be nearby such that the received signal is strong. Also, there may be no interfering signals, or they may be relatively weak. In these situations, receiver circuit currents can be reduced below what is necessary for the worst case condition. If this is done, power dissipation is reduced, and battery life is increased.

Thus, what is needed are circuits and methods that can adapt to a better-than-worst-case condition and reduce circuit currents and therefore power dissipation accordingly.

SUMMARY

Accordingly, embodiments of the present invention provide methods and circuits for reducing power dissipation in wireless transceivers and other electronic circuits and systems. Embodiments of the present invention use bias current reduction, impedance scaling, gain, and other dynamic changes either separately or in combination to reduce power dissipation in response to better-than-worst case conditions. For example, bias currents are reduced in response to a need for reduced signal handling capability, impedances are scaled thus reducing required drive and other bias currents in response to a strong received signal, or gain is varied and impedances are scaled in response to a low received signal in the presence of no or weak interfering signals. Alternately, currents may start low and be increased in response to worse-than-best-case conditions, or they may start at a point in between and vary up or down. These variations may be made to electronic systems generally, and are particularly suited and discussed below in the context of a wireless transceiver that may be used in networking devices, cellular telephones, and other wireless systems.

An exemplary embodiment of the present invention provides a method of receiving a signal using an integrated circuit. The integrated circuit includes a signal path having a low-noise amplifier configured to receive the signal, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer. The method itself includes determining a first signal strength at a first node in the signal path in the integrated circuit and dynamically changing an impedance of a component in the signal path based on the first signal strength.

A further exemplary embodiment of the present invention provides a method of receiving a signal using an integrated circuit. The integrated circuit includes a signal path having a low-noise amplifier configured to receive the signal, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer. The method itself includes determining a first signal strength at a first node in the signal path in the integrated circuit and dynamically changing a bias current in the signal path based on the first signal strength.

Another exemplary embodiment of the present invention provides a method of receiving a signal using an integrated circuit. The integrated circuit includes a signal path having a first circuit and a second circuit having an input coupled to an output of the first circuit. The method itself includes determining a first signal strength at a first node in the signal path in the integrated circuit. The first node is before the first circuit in the signal path. The method further includes dynamically changing a gain of the first circuit based on the first signal strength and dynamically changing an impedance of a component in the second circuit based on the first signal strength.

Still a further exemplary embodiment of the present invention provides a wireless transceiver integrated circuit including a receiver having a signal path, the signal path including a low-noise amplifier, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer, as well as a first signal strength indicator circuit coupled to the signal path and configured to determine a first signal strength. An impedance in the signal path is configured to be dynamically adjusted in response to the first signal strength.

Yet a further exemplary embodiment of the present invention provides a wireless transceiver integrated circuit. This integrated circuit includes a receiver comprising a signal path, the signal path having a low-noise amplifier, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer, as well as a first signal strength indicator circuit coupled to the signal path, and configured to determine a first signal strength. A bias current in the signal path is configured to be dynamically adjusted in response to the first signal strength.

Another exemplary embodiment of the present invention provides a wireless transceiver integrated circuit. This circuit includes a receiver comprising a signal path, the signal

path having a first circuit; and a second circuit having an input coupled to an output of the first circuit, as well as a first signal strength indicator circuit coupled to the signal path, and configured to determine a first signal strength. A gain of the first circuit is configured to be dynamically adjusted in response to the first signal strength, and an impedance in the second circuit is configured to be dynamically adjusted in response to the first signal strength.

A better understanding of the nature and advantages of the present invention may be gained with reference to the following detailed description and the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram of a wireless transceiver that may benefit by incorporation of embodiments of the present invention;

FIGS. **2**A and **2**B illustrate examples of desired and interfering signals and noise that may be received by a circuit in a wireless receiver;

FIG. **3** illustrates what can occur as a maximum signal handling capability is reduced in the worst-case signal condition;

FIG. **4** illustrates a portion of a receiver consistent with an embodiment of the present invention;

FIG. **5** illustrates the relationship between a required bias current and a given output signal for a representative circuit;

FIG. **6** is an example of how a circuit's impedances may be scaled to reduce drive currents, and depending on the circuit configuration used, to reduce associated bias currents as well;

FIG. **7** illustrates how gain may be inserted in a signal path to improve a circuit's signal to noise ratio;

FIGS. **8**A-**8**D illustrate some of the possible power saving techniques that may be used when received desired and interferer signals are all at a low power level;

FIGS. **9**A-**9**C illustrate one of the possible power saving techniques that may be used when a received desired signal is strong while all interfering signals are at a low power level;

FIGS. **10**A-**10**C illustrate one of the possible power saving techniques that may be used when received desired and interferer signals are all at a high power level;

FIGS. **11**A-**11**D illustrate one of the possible power saving techniques that may be used when a received desired signal is weak while one or more interfering signals are strong;

FIG. **12** is a summary illustrating four different input conditions and some of the appropriate power-saving changes that may be made in response to those conditions;

FIG. **13** shows how power may be saved as a function of time by employing one or more of the power saving methods consistent with embodiments of the present invention;

FIG. **14** is a block diagram of a portion of a receiver consistent with an embodiment of the present invention; and

FIG. **15** is a block diagram of a portion of a transmitter consistent with an embodiment of the present invention.

DESCRIPTION OF EXEMPLARY EMBODIMENTS

FIG. **1** is a block diagram of a wireless transceiver that may benefit by incorporation of embodiments of the present invention. This wireless transceiver may be designed to send and receive signals consistent with the IEEE 802.11a, 802.11b, 802.11g, or other signaling standard or combination of standards. This figure, as with all the included figures, is shown for illustrative purposes only and does not to limit either the possible embodiments of the present invention or the claims.

There are three main portions of this transceiver circuit, a receiver, transmitter, and synthesizer. This transceiver may be completely or partially integrated on a semiconductor chip, or it may be integrated onto multiple integrated circuits. In a specific embodiment, the circuitry bounded by dashed line **100** is integrated on a single chip coupled to one or more external components or circuits. The integrated circuit or circuits forming this wireless transceiver may incorporate various integrated circuit devices such as a bipolar, CMOS, or BiCMOS devices made using a silicon, silicon-germanium (SiGe), gallium arsenide or other III-V process, or other manufacturing process. Embodiments of the present invention may also be applicable to circuits manufactured using nanotechnology processing.

The receiver includes a signal path formed by low-noise amplifier **102**, I and Q mixers **104** and **106**, low pass filters **108** and **110**, and baseband amplifiers **114** and **116**. Other circuitry in the receiver includes received strength indicator **122**, automatic gain control circuit **166**, baseband gain control circuit **120**, tuning circuit **112**, and offset cancellation circuit **118**.

The transmitter includes input up-converter mixers **124** and **126**, summing node **176**, which may be conceptual rather than an actual circuit, transmit variable gain amplifier **128**, and power amplifier **130**.

The synthesizer includes a voltage-controlled oscillator **148**, which drives I and Q buffers **154** and **152**, prescaler **156**, reference clock buffer **142** and divider **158**, phase-frequency detector **160**, charge pump **162**, and loop filter **146**, which in a specific embodiment is formed by external components.

Signals are received on an antenna, not shown, and typically pass through an RF switch and bandpass filter before being received by the low-noise amplifier **102** on line **101**. The low noise amplifier gains the received signal and provides it to quadrature mixers **104** and **106**. I and Q mixers **104** and **106** down-convert the received signal to baseband by multiplying them with quadrature versions of the oscillator signal provided by buffers **152** and **154**. This down conversion also produces a high frequency component at a frequency that is equal to the sum of the frequencies of the received signal and the VCO. This unwanted signal is filtered by low pass filters **108** and **110**, which in turn drive baseband amplifiers **114** and **116**. The outputs of baseband amplifiers **114** and **116** are typically converted to digital signals by analog-to-digital converters at the front end of a digital signal processing block.

In the transmit mode, I and Q versions of the signal to be transmitted are provided on lines **121** and **123** to up-convert mixers **124** and **126**. These up-convert mixers multiply the I and Q portions of the transmit signal by quadrature versions of the VCO signal provided by buffers **152** and **154**. The outputs of the up-convert mixers **124** and **126** are summed, and amplified by transmit VGA **128**, which in turn drives power amplifier **130**. The output of power amplifier **130** is typically filtered, and passes through the RF switch to the antenna for transmission.

A reference clock is received and buffered by the reference buffer **142**. The VCO generates quadrature oscillatory signals that are divided by prescaler **156**. The reference clock is typically generated by a crystal or other stable periodic clock source. The phase-frequency detector **116** compares the phase or frequency (depending on whether the

synthesizer is tracking or acquiring the correct frequency) of the divided VCO signal and the reference clock, or a divided version of the reference clock, and generates an error signal, which drives the charge pump **162**. The output signal of the charge pump **162** is filtered by the loop filter **146**, which is commonly a lead-lag filter, and which provides a tuning or correction signal to the VCO **148**.

Embodiments of the present invention may be used to reduce the power dissipation of one or more of these included circuits. For example, the power dissipation in the low-noise amplifier **102**, down-convert mixers **104** and **106**, low pass filters **108** and **110**, or baseband amplifiers **114** and **116** may be optimized. Also, power dissipation in up-convert mixers **124** **126**, variable gain amplifier **128**, and power amplifier **130** may also be optimized. Similarly, VCO **148** and prescaler **156** currents may be adjusted. Embodiments of the present invention may also be applied in other circuits which may be included in other integrated circuit receivers, transmitters, transceivers, or other electronic circuits or systems.

When a receiver is actively receiving a desired signal, each block in the signal path has at its input the desired signal as well as noise and possibly interfering signals. The desired signal is the useful, information-carrying portion of a received signal. The noise may be thermal, shot, or other noise generated on the integrated circuit, in addition to received noise generated by sources external to the chip. The noise at the input of a block may be referred to as the equivalent input noise. The interfering signal or signals, or interferers, may be generated by similar transceivers, or other electrical equipment, circuits, or systems.

FIGS. **2**A and **2**B illustrate examples of desired signals, interferers, and noise that may be received by one of the various circuits in a wireless receiver. In each of these figures, the signal strength is plotted along a Y-axis **204** or **254** as a function of frequency along an X-axis **202** or **252**. In the example of FIG. **2**A, a received desired signal **206** is large in comparison to interfering signals **208** and **210**. In these examples, two interfering signals are shown for illustrative purposes, though there may be no such signals, one such signal, or more than two such signals in the frequency range of interest. Also, while for these examples the interferers are shown as being at a higher frequency than the desired signal, there may be one or more interferers at higher or lower frequencies as the desired signal. In this specific example, the acceptable noise floor **214** is relatively high, while maximum signal handling capability Smax **212** (that is the maximum signal power that can be handled with an acceptably low distortion) needs only to be high enough to accommodate the desired signal. For this specific example, the circuit receiving this input spectrum only requires a relatively small dynamic range for proper operation, that is the range between Smax **212** and the noise floor **214** is relatively small.

Conversely, in the example shown in FIG. **2**B, the desired signal **256** is relatively weak compared to the large interferers **258** and **260**. In this example, the noise floor **264** should be relatively low so as to prevent an unacceptable level of error in the recovery the desired signal **256**. The maximum signal handling capability Smax **262** should be relatively high to accommodate the large interferers in order to avoid the creation of intermodulation products as described below. Accordingly, in this specific example, the circuit receiving this input spectrum should have a large dynamic range, particularly in comparison to the example of FIG. **2**A.

It should be noted that the noise level or noise floors shown in these and the other included figures is the noise density integrated over the bandwidth of interest. For simplicity and comparison, this level is shown as a horizontal line, and is not meant to imply noise density.

Often in wireless receivers, a circuit at different times will receive an input spectrum similar to those shown in FIGS. **2**A and **2**B. The input spectrum of FIG. **2**B is generally considered the worst-case input signal, and typical design methodology involves designing a receiver for this condition, specifically the weakest desired signal accompanied by largest interference level. Circuit impedances and currents are set such that the noise floor **264** is sufficiently low for an acceptable bit-error rate, while bias currents are set sufficiently high for the required Smax **262**.

Conversely, the input spectrum in FIG. **2**A is that of the best-case input signal, specifically, a robust desired signal accompanied by no or low-level interferers. In this case, the noise floor **214** may be allowed to rise, while the maximum signal handling capability Smax **212** may be reduced. When this is done, the receiver circuit may save significant power. For example, the circuit's impedances may be increased, thus reducing required drive currents. Similarly, bias currents may be lowered, thus reducing the maximum signal in handling capability.

The minimum power dissipation for a circuit is proportional to the required maximum signal-to-noise ratio, which is the ratio between Smax **212** or **262** and N **214** and **264**. Thus, a circuit receiving an input similar to the one shown in FIG. **2**A can dissipate less power than one receiving the input as shown in FIG. **2**B, while still achieving an acceptable bit-error rate.

FIG. **3** illustrates what can occur when the maximum signal handling capability Smax **314** is reduced in the worst-case condition, that is when a weak desired signal **306** is accompanied by large interferers **310** and **312**. Again, signal strength is plotted along a Y-axis **304** as a function of frequency along X-axis **302**. In this specific example, Smax **314** is reduced below the peak levels of the interferers **310** and **312**. Since Smax is low, the circuit cannot handle the interferers linearly. The resulting nonlinearities lead to a mixing of the interferers and the creation of intermodulation products **308** (for example, a third-order intermodulation distortion, IM3), one of which in this example occurs at the same frequency as the desired signal **306**. As can be seen, if the intermodulation products **308** become excessive, the received signal bit error rate may become excessive, and the desired signal **306** may be lost. Accordingly, while Smax may be lowered even under some unfavorable conditions in order to reduce power, care should be taken to avoid corruption of the received desired signal.

FIG. **4** illustrates a portion of a receiver consistent with an embodiment of the present invention. Included is a filter **430**. An optional gain element **420** is placed in front of the filter **430** in order to increase signal levels. Signal strength indicator circuits **440** and **450** are connected to input line **410** and output line **460**. In this specific example, the input signal spectrum on line **410** is shown as desired signal **412** and interferers **414** and **416**. The signal spectrum at the output line **460** is shown as desired signal **462** and interferers **464** and **466**. The signal strength indicators **440** and **450** do not provide information as to the relative sizes of the desired and interfering signals. Rather, a cumulative signal level is provided at their outputs. For example, the first signal strength indicator **440** outputs a level corresponding to the sum of desired signal **412** and interfering signals **414** and **416**, while the second signal strength indicator **450** provides

a signal level corresponding to the sum of desired signal **462** and interfering signals **464** and **466**. In this specific example, the gain of the gain and filter circuit combinations is shown as approximately one, while the interfering signals **414** and **416** signal levels are reduced.

A comparison of the signal levels provided by the signal strength indicators **440** and **450** indicates that much of the combined received signal on line **410** has been filtered. Accordingly, it may be deduced that large interfering signals present at the input are being filtered by the filter **430**. From this information, as will be shown in greater detail below, the bias, impedance, and gain of the gain stage **420** and filter **430** combination may be optimized to reduce power dissipation.

There are several real world situations where the received signal is better than the worst-case condition such that power can be saved. For example, large interferers may be present only part of the time, that is, on a temporary or transient basis. The interfering equipment may be some distance from the transceiver, or it may be operating in the low power mode. Also, the desired signal may be very strong as compared to the noise and interferers, for example a hub, router, or access point may be nearby.

Some transceivers consistent with embodiments of the present invention are designed to work with more than one data transfer specification or standard. In this case, when a transceiver is operating in a mode having a lower data rate, the power saving techniques described here may be employed.

FIG. **5** illustrates the relationship between a required biased current **516** for a given output signal **514** for a representative circuit **510**. If the output signal current level is relatively low, such as the output current shown as **526**, the corresponding bias current **528** may be low. Conversely, if the output signal current level is larger as with the example **536**, the corresponding bias current level **538** should also be high. Accordingly, if a bias current is initially set high to handle large a large input signal, for example a large interferer, this current may be reduced if the input signal is smaller.

There are many ways by which these bias currents can be reduced. For example, the current may be generated by placing a voltage across a resistor by applying a bias voltage to the base of a device whose emitter is connected to ground through a resistance. In this case, the resistor may be increased by opening switches across portions of the resistance, or lowering the bias voltage applied at the base. Several ways in which this may be done will be readily understood by one skilled in the art.

FIG. **6** is an example of how a circuit's impedances may be scaled to reduce drive currents, and, depending on the circuit configuration used, associated bias currents as well. A driver **612** has a load R **614** and C **616**. The frequency response of this circuit is the same as that seen by driver **622**, which drives an impedance of 2R **624** and C/2 **626**. But the impedance of the load seen by driver **622** is double that seen by **612**, thus the output current required by the driver **622** is reduced by one-half.

As an example, the output stage of each of these drivers may be a Class A emitter follower formed by an emitter follower connected to a current source. When the outputs are driven high, the emitter of driver **622** need supply only one-half the drive current as driver **612**. In this way, an impedance can be scaled in order to decrease a circuit's required drive current.

Also, the discharge current for driver **622** is only one half that of driver **612** for a given negative-going slew rate. Thus, the current source of **622** may be reduced by the same factor of one-half as compared to driver **612**. In this example, the bias current, that is the current in the pull-down current source can be reduced. Many other examples where drive currents and possibly bias currents may be reduced will be appreciated by one skilled in the art.

FIG. **7** illustrates another degree of freedom that made be employed to reduce current levels in a transceiver. Specifically, a gain element **720** may be inserted in front of a circuit block **730** in order to improve the combined circuit's signal-to-noise ratio by a factor equal to the gain of the inserted gain block. This is particularly useful when large interferers are absent and the desired received signal is moderate or low. Specifically, gain is added to the signal while impedances are increased, which raise the noise floor. In this way, a given signal-to-noise ratio may be maintained while the power is decreased.

The gain of such an element may be varied by increasing a current in a differential pair or increasing a load resistance using switches. Many other examples where the gain of this element may be varied will be appreciated by one skilled in the art.

These variables, or degrees of freedom, specifically reducing bias currents, increasing impedances, and increasing gain may be used as in the following examples.

FIG. **8A** is a block diagram of a functional block **820** and optional gain element **810** in accordance with an embodiment of the present invention. Functional block **820**, like the functional blocks in the following diagrams, may be a filter, mixer, amplifier, or other circuit or circuits in a wireless transceiver or other electronic circuits or system. An input signal is received on line **812** by the optional gain element **814**. When the optional gain block **810** is not used, the input signal may be received directly by the function block **820**. The gain of the optional gain element **812** is controlled by a gain control signal on line **814**. The functional block receives an output signal from the optional gain element **810** and provides an output VOUT on line **822**. The lines in this and the other included figures may be one or more lines, depending on whether single-ended, differential, or other type of signaling is employed.

One or more impedances are under control of signals on impedance control lines **824**. Similarly, one or more bias currents in the function block are under control of one or more signals on bias control lines **826**. These various control lines may be logic signals, analog signals, voltage or currents lines, or other signal or bias lines. In other embodiments of the present invention, the gain control element **810** may be included in the function block **820**. Also, various embodiments may not incorporate either or both the impedance control and bias control.

FIG. **8B** is an example input that may be present on line VIN **812**. In this example, a desired signal **836** is relatively weak, as are interfering signals **837** and **838**. The initial bias and circuit configuration is such that the noise floor **833** and maximum signal handling capability Smax **831** are adjusted for worst case conditions. The circuit of FIG. **8A**, as with all the circuits described here, receives noise at its input which may be referred to as input equivalent noise or input referred noise. Additionally, the circuit of FIG. **8A** generates noise which is added to the input referred noise. Depending on the gain characteristics of the circuitry, the output noise at various frequencies may be greater than, equal to, or less than the input referred noise. For simplicity, the noise floor and maximum signal handling capability Smax, in this and the other figures, are shown as straight lines, though the noise and Smax are typically curved as a function of frequency.

That the input spectrum is as shown in FIG. **8**B can be determined, for example, by low signal strength indications on line VIN **812** and VOUT **822**. That is, a low level signal strength indication on line VIN **812** indicates that no portion of the input signal is particularly large.

For this exemplary input, there are at least two methods by which the power dissipation for this circuitry may be reduced. Depending on the exact circuits and structures used, one of these methods may be preferred.

In FIG. **8**C, the bias current is decreased, thereby lowering the maximum signal handling capability **841** as compared to **831**, closer to the desired and interfering signal levels. Again, the bias currents in the function block **820** may be reduced by switching impedances that appear across a voltage thereby changing a resulting bias current, by reducing a voltage at the gate of a MOS or base of a bipolar transistor, or by other methods.

In FIG. **8**D, a second method of reducing power dissipation in the function block **820** is employed. Specifically, Smax **851** is held constant as compared Smax **831**. The desired and interfering signals are amplified such that they are closer to the available signaling handling capability **851**. Also, the noise floor **853** is raised as compared to noise floor **833** in FIG. **8**B. Specifically, the noise contributed by the function block **820** is increased, such that the noise at its output is increased to noise floor **853**. This is done by increasing one or more impedance in function block **810**, such that drive currents inside that block are reduced. Depending on the exact configuration, this may also allow some biasing currents to be reduced, while maintaining the maximum signal handling capability **851** at a sufficient level. Alternately, these two methods of reducing power dissipation in function block **820** may be done in combination.

The included examples are explained for the exemplary situation where biasing and other parameters are set for worst-case conditions, and then changed to save power when it is discovered that the conditions are better-than-worst case. Alternately, the bias currents and other parameters may be set for maximum power savings, or an intermediate point, and the power can be adjusted from there.

FIG. **9**A illustrates a block diagram including an optional gain element **910** and function block **920**. Again, an input signal is received on line **912** by optional gain element **910** which in turn drives function block **920**. The function block provides an output VOUT on line **922**, and receives impedance and bias control signals on lines **924** and **926**.

FIG. **9**B shows the spectrum for what may be considered a best-case received signal. Specifically, the desired signal **936** is strong, while the interfering signals **937** and **938** are relatively weak. This may be determined, for example, by detecting a large signal level at the input line VIN **812** and a large signal level after a filter, since these readings would indicate that a large signal is received, but that it is at the desired signal frequency.

The maximum signaling capability **931** and noise floor **933** are shown as being set for the worst case conditions. In this case, the noise floor **933** is lower than the maximum allowed for proper signal reception. Accordingly, one or more impedance in the function block **920** may be increased, such that the noise floor **943** rises as shown in FIG. **9**C. In this way one or more the driving currents in the function block **920** may be reduced. Similarly, since the drive current is reduced, one or more bias current may also be reduced, depending on the exact circuit configuration.

FIG. **10**A illustrates a block diagram showing an optional gain element **1010** driving a function block **1020**. An input signal is received by the gain element **1010** on line **1012**, and an output is provided by function block **1020** on line VOUT **1022**. One or more gain control signals present on lines **1014** control the gain of gain control element **1010**, while one or more impedance and bias control signals are received by the function block **1020** on line to **1024** and **1026**.

FIG. **10**B illustrates a received signal that may be received on line VIN **1012**. In this example, the desired signal **1036** and interferers **1037** and **1038** are each relatively large. This may be determined, for example, by detecting a large signal level at the input line VIN **812** and a smaller signal level after a filter, since these readings would indicate that a large signal is received, but that interferers are being reduced.

As before, in this example, the noise floor **1033** and maximum signal handling capability **1031** are initially set for the worst case conditions. Since the desired signal is relatively large in this case, the noise floor may be allowed to rise, a shown by noise floor **1043** in FIG. **10**C. Since the desired signal **1046** and interferers **1047** are large, the maximum signal handling capability Smax **1041** remains constant. Again, the noise floor is increased by increasing impedances in the function block **1020**. This reduces the required drive current, and may also allow for a reduction in bias currents.

FIG. **11**A illustrates a block diagram including an optional gain element **1110** and function block **1120** in accordance with an embodiment of the present convention. An input signal is received on line **1112** by the optional gain control element **1110**, while an output signal is provided by the function block **1120** on line VOUT **1122**. Gain, impedance, and bias control signals are received on lines **1114**, **1124**, and **1126**.

FIG. **11**B is an exemplary input signal that may be received by the gain control element **1110** on line VIN **1112**. In this specific example, the desired signal **1136** is relatively low or weak while the interfering signals **1137** and **1138** are large. This may be determined, for example, by detecting a large signal level at the input line VIN **812** and a much smaller signal level after a filter, since these readings would indicate that a large signal is received and that large interferers are being reduced such that the resulting signal, the desired signal, is relatively weak.

Again, the maximum signal handling capability **1131** and noise floor **1133** are initially set for worst case conditions. If the desired signal is sufficiently low, while the interferers are sufficiently high, power savings may not be achievable over the worst case settings, since this is in fact the worst case condition. But, if the desired signal is somewhat larger than the worst case condition, then power may be saved in at least two different ways.

For example, FIG. **11**C shows the maximum signal handling capability **1141** being lowered. In this case, the interfering signals **1147** in **1148** began to clip and distort, thereby creating intermodulation products **1145**, which distort the desired signal **1146**. So long as care is taken to not corrupt the desired signal **1146** beyond an acceptable limit, typically measured by a bit-error rate, power may be reduced in this way.

Similarly, in FIG. **11**D, the noise floor **1153** is raised somewhat, thereby saving power. Again, this may be done so long as the noise floor is not sufficiently high that the system bit-error rate becomes unacceptable.

FIG. **12** is a summary of the above four examples. The received signal strengths are shown in column **1210**, while appropriate power saving responses are listed in column **1220**. Specifically, in row **1230**, the desired signal and interferer signal strengths are both weak or small. In this case, proper responses include decreasing Smax, or increas-

ing one or more circuit impedances while increasing the circuit gain. Depending on the exact circuit configuration, one of these options may be preferred over the other. Alternately, they may be done in combination, or done in combination with other power saving techniques. Also, in some specific embodiments, when both desired signal and interferer signal strengths are small, the gain may need to be increased while the impedance is maintained or not increased in order to keep the noise floor low.

In row **1240**, the desired signal strength is strong or large, while the interfering signals are small. In this case, an appropriate response is to increase one or more of the circuit impedances. Again, depending on the exact circuit in question, one or more of the bias currents may also be reduced.

In row **1250**, both the desired signals and interfering signal strengths are large. Again, in this case an appropriate response is to increase one or more of the circuit impedances.

In row **1260**, the received desired signal strength is weak or small, while the interfering signals are large. Since this is the worst case situation for which the circuit is designed, substantial power savings are difficult to achieve. However, again, if the received signal is above a minimum level necessary for proper operation, some distortion of the interferers or raising of the noise floor may be acceptable.

It should be noted that not all possible signal conditions are listed here. For example, either the signal or interferer may be of a relatively medium strength, or the interferer may be absent. Also, these terms are for exemplary purposes and are not meant to convey specific signal conditions, but rather are only qualitative. The proper response to a specific condition depends on the embodiment of the present invention, the particular circuit topology, the requirements of the signaling standard used, as well as other constraints.

FIG. **13** is an example shown how power may be saved as a function of time by employing one or more of these methods consistent with embodiments of the present invention. Power is plotted along a Y-axis **1304** as a function of time along X-axis **1302**. Conventional worst case design would fix power dissipation at line **1310**. As can be seen, dynamic power dissipation **1320** under the control of variable gains, impedances, biasing, or combination thereof, allows for a lower average power **1330** as compared to the power dissipated **1310** by the conventional design.

FIG. **14** is a block diagram of a portion of a receiver consistent with an embodiment of the present invention. Included are low-noise amplifier **1410**, mixer **1420**, gain stage **1430**, filter **1440**, AGC amplifier **1450**, and VCO **1460**. Signal strength detection is done at the output of the low-noise amplifier by signal strength indicator **1470**, at the output of the mixer by signal strength indicator **1472**, and at the output of the filter by signal strength indicator **1474**. The outputs of the signal strength indicator circuits are received by the computational circuit **1470**, which in turn controls gain and power control circuits **1480** and **1485**. Power and gain control circuits **1480** and **1485** control the gain, biasing, and impedance levels of the circuits in the receiver signal path. Also, the gain and power control circuits may control the same parameters in the VCO **1460**. This figure is greatly simplified for purposes of explanation. For example, the quadrature nature of the mixers and following circuits are not shown. Also, power-down and start-up circuits are not included.

The current level in the low-noise amplifier determines a multitude of parameters including voltage gain, linearity, input impedance matching, and noise figure. When conditions are better than worst-case, some of these parameters may be relaxed while maintaining an acceptable bit-error rate, thus saving power.

The bias current in the mixers effect that block's noise figure and linearity. Care is taken in reducing power in this block so as not to increase nonlinearities, particularly the third-order nonlinearity as measured by IP3, the third-order intercept point, beyond an acceptable limit.

A key parameter of the VCO is phase noise, an increase in which increases the sidebands on either side of the oscillation signal. During transmission, the phase noise should be kept low to avoid interference with adjacent channels and for preserving modulation information.

During reception however, if the conditions are better than worst case, the phase noise requirement for the VCO is relaxed, and power can be saved consistent with embodiments of the present invention. The achievable phase noise power spectral density is approximately inversely proportional to the bias current used. Thus, when low phase noise is not required during reception, bias current in the VCO can be reduced.

Most of the power savings in a transceiver in accordance with embodiments of the present invention is achieved in the receiver portion. Additional power may be saved in the transmitter section.

FIG. **15** is a block diagram of a transmitter portion consistent with an embodiment of the present invention. Included is a signal path formed by gain stage **1510** and power amplifier **1520**. The output power level is sensed by output level sensing circuit **1550**, which in turn adjusts the biasing of the power amplifier **1520** through the power control circuit **1540**. Additionally, a transmitter level control signal is received by power control circuits **1530** and **1540**, which in turn control the biasing of gain stage **1510** and power amplifier **1520**. Gain control circuit **1560** also adjusts the gain of gain stage **1510** and power amplifier **1520**. Additional circuitry that varies impedances in each of these circuits may also be included.

Since the gain, impedance and biasing of these blocks are being dynamically varied, care must be taken to not negatively affect the signal being processed. For example, specific embodiments of the present invention perform some or all of these variations during preamble. Also, as changes occur, the circuits in some embodiments are limited such that they may only adapt to an improvement in conditions after frames are completed. If conditions worsen, the circuits may be allowed to change in order to save the data. Alternately, a system may be manually calibrated, for example at set up, and when the network configuration is changed.

The above description of specific embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form described, and many modifications and variations are possible in light of the teaching above. The embodiments were chosen and described in order to best explain the principles of the invention and its practical applications to thereby enable others skilled in the art to best utilize the invention in various embodiments and with various modifications as are suited to the particular use contemplated.

What is claimed is:

1. A method of reducing the power consumption of a receiver of a battery operated transceiver having a plurality of circuits, wherein the plurality of circuits comprise a receiver signal path comprising at least an amplifier, a mixer and a filter, wherein the plurality of circuits are designed to

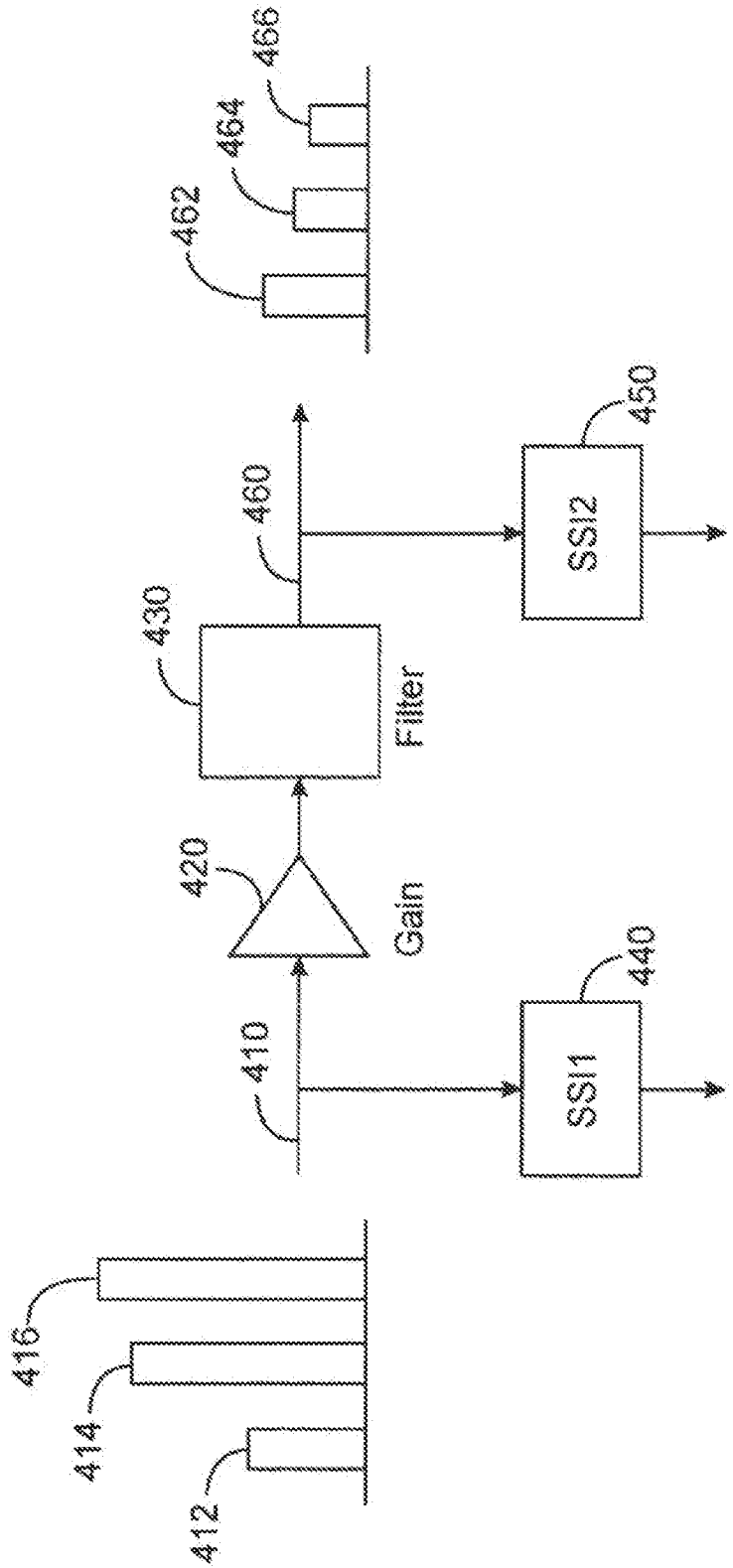

466
464
462
460
450
SSI2
430
Filter
420
Gain
410
440
SSI1
416
414
412

FIG. 4

function between a worst-case operating condition and a best case operating condition, wherein the worst-case operating condition is when a desired signal strength is low and an interferer signal strength is high and the receiver operates with a maximum power dissipation and the best-case operating condition is when the desired signal strength is high and the interferer signal strength is low and the receiver operates with a minimum power dissipation, the method comprising:

receiving a signal comprising a desired signal and an interferer signal;

determining a strength of the desired signal;

determining a strength of the interferer signal;

comparing the strength of the desired signal to the strength of the interfere signal; and

dynamically adjusting at least one of an impedance, a bias or a gain of at least one of the amplifier, filter or mixer in the receiver signal path, responsive to the comparing.

2. The method of claim 1, wherein when the strength of the interferer signal decreases over time, and the strength of the desired signal is low, dynamically decreasing the bias of at least one of the plurality of circuits in the receiver signal path.

3. The method of claim 1, wherein when the strength of the interferer signal is low, and the strength of the desired signal decreases over time, dynamically increasing a gain of at least one of a plurality of circuits in the receiver signal path and dynamically increasing the impedance of at least one of the plurality of circuits in the receiver signal path.

4. The method of claim 1 wherein when the strength of the interferer signal is low and the strength of the desired signal increases over time, dynamically increasing the impedance of one or more of the plurality of circuits in the receiver signal path.

5. The method of claim 1, wherein when the interferer signal is weak and the desired signal is low and the strength of the desired signal increases over time, dynamically decreasing the bias of one or more of the plurality of circuits in the receiver signal path.

6. A method for reducing power consumption in a receiver in a battery operated mobile device, wherein the receiver comprises a plurality of circuits, and wherein the plurality of circuits comprise a signal path including at least an amplifier, a mixer and a filter, the method comprising:

receiving a wireless signal comprising a desired signal and an interferer signal at the receiver;

determining a strength of the desired signal;

determining a strength of the interferer signal;

comparing the strength of the desired signal to the strength of the interferer signal; and

when the strength of the interferer signal is low and the relative strength of the desired signal is greater than the strength of the interferer signal, dynamically increasing an impedance of at least one of the amplifier, filter or mixer in the signal path of the receiver, thereby reducing power dissipation in the receiver.

7. A method for power dissipation control in a receiver of a wireless transceiver of a battery-powered portable wireless device, the receiver having a signal path comprising a plurality of circuits including at least an amplifier, a filter, and a mixer, wherein the receiver is configured to receive a wireless signal having a desired signal and an interferer signal, wherein the plurality of circuits are designed to function between a worst-case condition when a strength of the desired signal is low and a strength of the interferer signal is high, and a best-case condition when the strength of the desired signal is high and the strength of the interferer signal is low, the method comprising:

receiving the wireless signal having the desired signal and the interferer signal by the receiver;

determining the strength of the desired signal;

determining the strength of the interferer signal;

comparing the strength of the desired signal relative to the strength of the interferer signal; and

based on the comparison, when the plurality of circuits are functioning at better than the worst-case condition, dynamically adjusting one or more of an impedance, a bias or a gain of one or more of the plurality of circuits in the signal path, thereby controlling power dissipation.

8. The method of claim 7, wherein when the strength of the interferer signal is low and the relative strength of the desired signal with respect to the interferer signal increases, dynamically increasing the impedance of one or more of the plurality of circuits in the signal path to reduce the power dissipation and thereby save power.

9. The method of claim 7, wherein when the strength of the desired signal is low but the relative strength of the desired signal with respect to the interferer signal is better than the worst-case condition and the interferer signal reduces in strength, dynamically reducing the bias of one or more of the plurality of circuits in the signal path, thereby reducing power dissipation and saving power.

10. The method of claim 9, wherein reducing power dissipation reduces a power drain from a battery in the battery-powered portable wireless device.

11. A method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, the receiver having a signal path comprising a plurality of circuits including at least an amplifier, a filter, and a mixer, the plurality of circuits designed to function under at least a worst case condition when a strength of a received desired signal is low and a strength of a received interferer signal is high, the method comprising:

receiving a wireless signal having a desired signal and an interferer signal by the receiver;

determining a strength of the desired signal;

determining a strength of the interferer signal;

comparing the strength of the desired signal relative to the strength of the interferer signal;

based on the comparing, determining a functioning condition of the plurality of circuits; and

when the plurality of circuits are determined to function at a better than the worst case condition in which the strength of the interferer signal is low and the strength of the desired signal is low, causing a bias current of one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be dynamically decreased relative to the worst-case condition, thereby saving power.

12. A method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, the receiver configured to function under at least a worst case condition when a received desired signal strength is low and a received interferer signal strength is high, the receiver having a signal path comprising at least an amplifier, a filter, and a mixer, the method comprising:

receiving a wireless signal having a desired signal and an interferer signal by the receiver;

determining a strength of the desired signal;

determining a strength of the interferer signal;

comparing the strength of the desired signal relative to the strength of the interferer signal;

based on the comparing, determining a functioning condition of the plurality of circuits; and

when the plurality of circuits are determined to function at a better than the worst case condition in which the strength of the interferer signal is low and the strength of the desired signal is high, causing an impedance of one or more of amplifier, filter or the mixer in the receiver signal path of the wireless transceiver to be increased relative to the worst-case condition, thereby saving power.

13. A method for power dissipation control in a receiver of a wireless transceiver of a battery powered portable wireless device, the receiver having a signal path comprising a plurality of circuits including at least an amplifier, a filter, and a mixer, the method comprising:

receiving a wireless signal having a desired signal and an interferer signal by the receiver;

determining the strength of the desired signal;

determining the strength of the interferer signal;

comparing the strength of the desired signal relative to the strength of the interferer signal; and

when the interferer signal is high and the desired signal is low, causing a bias current of one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be dynamically increased, controlling the power dissipation of the receiver.

14. A method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device based on its operating signal conditions, wherein the receiver has a signal path comprising a plurality of circuits including at least an amplifier, a filter, and a mixer, the plurality of circuits designed to function under operating signal conditions that vary based on relative signal strengths of an interferer signal and a desired signal, wherein the operating signal conditions vary between a worst-case operating condition and a best-case operating condition, wherein the worst-case operating condition occurs when a desired signal strength is low and an interferer signal is high and the receiver operates with a maximum power dissipation, wherein the best-case operating condition occurs when the desired signal is high and the interferer signal strength is low and the receiver operates with a minimum power dissipation, the method comprising:

receiving a wireless signal having a desired signal and an interferer signal by the receiver;

determining the strength of the desired signal;

determining the strength of the interferer signal;

comparing the strength of the desired signal relative to the strength of the interferer signal strength;

based on the comparing, when the plurality of circuits are determined to be functioning at better than the worst-case operating signal condition, dynamically adjusting at least one of an impedance, a bias current or a gain of one or more of the amplifier, filter or mixer in the signal path of the receiver, thereby reducing power consumption to save power.

15. The method of claim 14, wherein when the desired signal strength is low and the receiver is operating at better than the worst-case operating signal condition by having the interferer strength lower than that in the worst case operating signal condition, dynamically reducing the bias of one or more of the plurality of circuits in the signal path of the receiver, thereby reducing power dissipation and saving power; and

wherein when the interferer signal strength is high and the receiver is operating at better than the worst-case operating signal condition by having the desired signal higher than that in the worst case operating signal condition, dynamically increasing the impedance of one or more of the plurality of circuits in the signal path of the receiver, thereby reducing power dissipation and saving power.

16. A method for power dissipation optimization in a receiver of a wireless transceiver of a battery powered portable wireless device, the receiver having a signal path comprising a plurality of circuits including at least an amplifier, a filter, and a mixer, wherein the plurality of circuits are designed to function between a worst-case operating condition and a best case operating condition, wherein the worst-case operating condition is when a desired signal strength is low and an interferer signal strength is high and the receiver operates with a maximum power dissipation and the best-case operating condition is when the desired signal strength is high and the interferer signal strength is low and the receiver operates with a minimum power dissipation, the method comprising:

receiving a wireless signal having a desired signal and an interferer signal by the receiver;

determining a strength of the desired signal;

determining a strength of the interferer signal;

comparing the strength of the desired signal relative to the strength of the interferer signal; and

based on the comparing, when the plurality of circuits are determined to be functioning at better than the worst-case operating condition, dynamically adjusting at least one of an impedance, a bias current or a gain of one or more of the amplifier, filter or mixer in the signal path of the receiver to optimize power dissipation and save power.

17. The method of claim 16, wherein when the desired signal strength is low and the operating signal condition of the receiver is better than the worst-case operating signal condition and the interferer signal strength is increasing, dynamically increasing a bias current of at least one of the plurality of circuits in the receiver signal path of the wireless transceiver, optimizing the power dissipation;

wherein when the desired signal strength is low and the operating signal condition of the receiver is better than the worst-case operating condition and the interferer signal strength reduces over time, dynamically decreasing a bias current of at least one of the plurality of circuits in the receiver signal path of the wireless transceiver, optimizing the power dissipation, and

wherein optimizing the power dissipation under better than the worst-case operating signal condition saves power with respect to the maximum power dissipation of the worst-case operating signal condition.

18. A method for controlling power dissipation in a receiver of a wireless transceiver of a battery powered portable wireless device, the receiver having a signal path comprising a plurality of circuits including at least an amplifier, a filter, and a mixer, wherein the plurality of circuits are designed to function between a worst-case operating condition and a best case operating condition, wherein the worst-case operating condition is when a desired signal strength is low and an interferer signal strength is high and the receiver operates with a maximum power dissipation and the best-case operating condition is when the desired signal strength is high and the interferer signal strength is low and the receiver operates with a minimum power dissipation, the method comprising:

receiving a wireless signal having a desired signal strength and an interferer signal by the receiver;

determining a strength of the desired signal;

determining a strength of the interferer signal;

comparing the strength of the desired signal relative to the strength of the interferer signal; and

wherein when the strength of the interferer signal is low and when the strength of the received desired signal is higher than the desired signal of the worst-case operating signal condition, dynamically adjusting an impedance of at least one of the plurality of circuits in the signal path to reduce power dissipation.

19. A method of power dissipation optimization in a receiver of a wireless transceiver of a wireless communication device based on its operating signal conditions, wherein the transceiver has a signal path comprising a plurality of circuits designed to function under operating signal conditions that vary based on relative signal strengths of an interferer signal and a desired signal in a received wireless signal, wherein operating conditions vary between a worst-case operating signal condition, wherein the receiver operates with a maximum power dissipation when a desired signal strength is low and an interferer signal strength is high and a best-case operating signal condition, wherein the receiver operates with minimum power dissipation when the desired signal strength is high and the interferer signal strength is low, the method comprising:

receiving the wireless signal having the desired signal and the interferer signal by the receiver;

determining the desired signal strength;

determining the interferer signal strength;

comparing the desired signal strength to the interferer signal strength to determine an operating signal condition of the receiver;

based on the comparing, when the receiver operating signal condition is better than the worst case operating signal condition, dynamically adjusting one or more of an impedance, a bias, or a gain of one or more of the plurality of circuits in the receiver signal path, thereby optimizing power consumption to save power.

20. The method of claim 19, wherein power saving occurs when the desired signal strength is low and the operating signal condition is better than the worst-case operating signal condition, by dynamically reducing the bias current of one or more of the plurality of circuits in the signal path of the receiver, thereby reducing power dissipation.

21. The method of claim 20, wherein power saving occurs when the operating signal condition improves when the strength of the interferer signal decreases over time, and the bias current is reduced by dynamically adjusting the bias current of one or more of the plurality of circuits in the signal path of the receiver.

22. A method of power dissipation optimization in a receiver of a wireless transceiver of a wireless communication device based on its operating signal conditions, wherein the transceiver has a signal path comprising a plurality of circuits designed to function under operating signal conditions that vary based on relative signal strengths of an interferer signal and a desired signal in a received wireless signal received, wherein the operating signal conditions vary between a worst-case operating signal condition and a best-case operating signal condition, wherein in the worst-case operating signal condition the receiver operates with a maximum power dissipation when a desired signal strength is low and an interferer signal strength is high, and wherein in the best-case operating signal condition the receiver operates with minimum power dissipation when the desired signal strength is high and the interferer signal strength is low, the method comprising:

receiving the wireless signal having the desired signal and the interferer signal by the receiver;

determining the desired signal strength;

determining the interferer signal strength;

comparing the desired signal strength to the interferer signal strength;

determining an operating signal condition of the receiver between the best and worst-case operating signal conditions based on the comparing;

when the interferer signal strength is high and the operating signal condition is better than the worst-case operating signal condition, dynamically increasing an impedance of one or more of the plurality of circuits in the signal path of the receiver, thereby reducing power dissipation.

23. The method of claim 22, wherein when the desired signal strength increases over time resulting in an improvement in the operating condition, dynamically adjusting the impedance of one or more of the plurality of circuits in the signal path of the receiver results in power saving.

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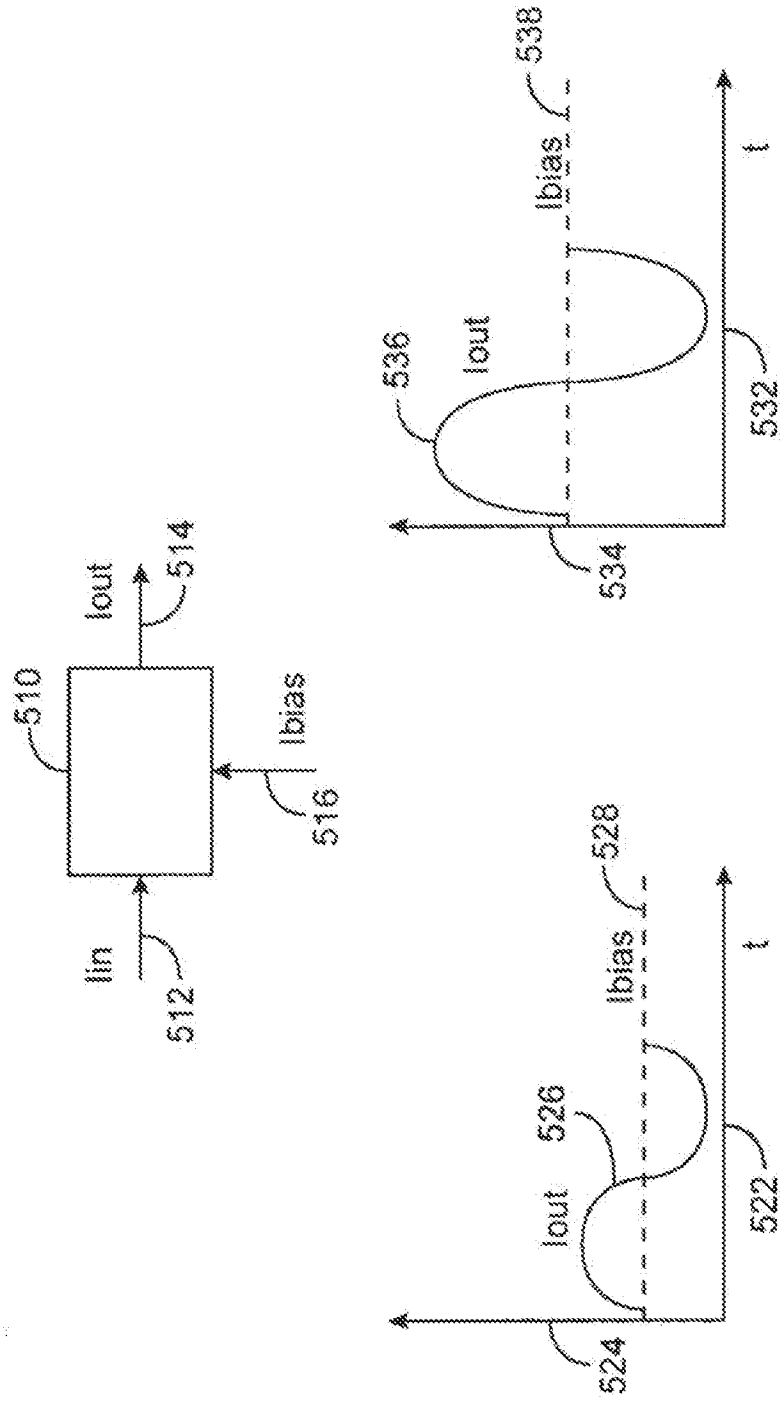

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FIG. 5