Adaptive Analog IF Signal Processor for a Wide-Band CMOS Wireless Receiver

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***Abstract*—An IF strip for a wireless receiver supports a variable baud rate by changing analog filter bandwidth. Sliding and step adaptive dynamic range are both used at IF to dissipate only the necessary power at prevailing channel conditions. A combination of VGA and PGA is developed for 64-QAM. The total signal processor draws an average of 16 mA from 3.3 V and a peak of 73 mA. The differential input noise is as low as $3.9\text{nV}/\sqrt{\text{Hz}}$, while maximum IIP3 is $+22$ dBm with respect to 100 ohms.**

***Index Terms*—Author, please supply index terms. E-mail keywords@ieee.org for info.**

I. Introduction

THE complexity of wireless systems increases with the growing power of digital signal processors (DSPs). As complexity grows, smaller form-factor and higher integration become more important, which leads inevitably to a fully integrated receiver (RX). Two main challenges are on-chip image-rejection and wide dynamic range. Image rejection is addressed in detail elsewhere [1], [2]. This paper focuses on the second challenge.

In a wireless RX, the communication channel conditions can vary largely. In most mobile systems, this large dynamic range (DR) must be absorbed by the analog radio; otherwise the A/D and the digital front-end must resolve a very large number of bits. Sigma–delta modulators have been used in narrow-band systems to obtain a very high DR [3]. However, they are not practical in wide-band systems. Therefore, wide DR *analog* circuits are key to the realization of low-power wide-band systems.

This receiver implements adaptive dynamic range in the IF section. Most wireless systems are designed for the worst case; that is, the dynamic range is specified for the desired signal at a minimum detectable level, accompanied by the largest anticipated interferers. In practice, the receiver only infrequently needs this high instant DR. DR is obtained at the expense of a disproportionate rise in power consumption: doubling the power consumed by a circuit lowers its noise floor by 3 dB with constant IP3, thus raising its spurious-free dynamic range (SFDR) by only 2 dB. An important idea here, which has also been noted elsewhere [4], is that providing no more than the required DR at any given time lowers the *average* power consumption.

Section II describes the system that the IF strip was designed for and Section III introduces the idea of adaptive DR. Circuit design of the programmable gain amplifier (PGA), variable gain amplifier (VGA), and filters is discussed in Sections IV and V. Measurements are given in Section VI.

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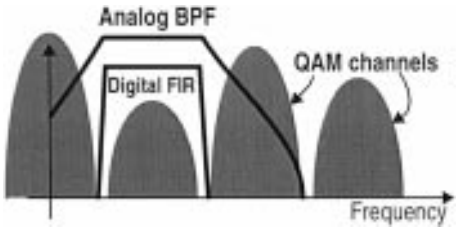

Fig. 1. Complete channel select filter is a combination of the analog BPF and a digital FIR filter.

II. System Description

The basic RX architecture has been described in detail elsewhere [5]. The IF section supports selectable bandwidths (BWs) of 625 kHz, 2.5 MHz, and 10 MHz. The modulation may be 4-QAM, 16-QAM, or 64-QAM. A receiver with adaptive BW requires a fully integrated bandpass filter (BPF). This system uses every channel in each cell [6] to increase the total number of users per cell. With the resulting very small guard-bands, a sharp channel select filter is necessary. It is impractical to implement this entirely as an analog circuit. Instead, following coarse analog filtering, a high-order FIR filter implemented in DSP isolates one channel (Fig. 1).

The 2.4-GHz ISM band does not regulate interferers. Microwave ovens emitting in the middle of the band are often the largest interferer for other users. These considerations call for an RX design with the largest possible DR. This is addressed at two levels: first, with circuits designed for the highest possible DR at a given power consumption, and second, by adaptive use of circuit blocks.

The front-end and image-reject downconversion sections of the RX are described in [5]. Fig. 2 is taken from [7] and shows a block diagram of the RX; the IF section is the main focus of this paper. This section of the receiver follows image rejection, and comprises a prefilter programmable gain amplifier (PGA), bandpass filter (BPF), a post-filter PGA, and finally a continuously variable gain amplifier (VGA). The BPF is usually the bottleneck to DR. The prefilter PGA (PGA1) trades off between the NF and the IIP3 of the IF strip. The BPF attenuates near-by channels and rejects far-away channels. The post-filter PGA + VGA amplifies the signal to 90% of the A/D full scale.

The following sections cover details of the circuit design.

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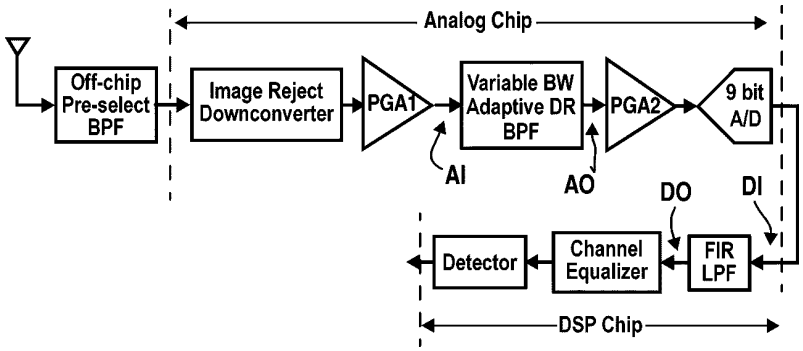

Fig. 2. Block diagram of complete WLAN receiver.

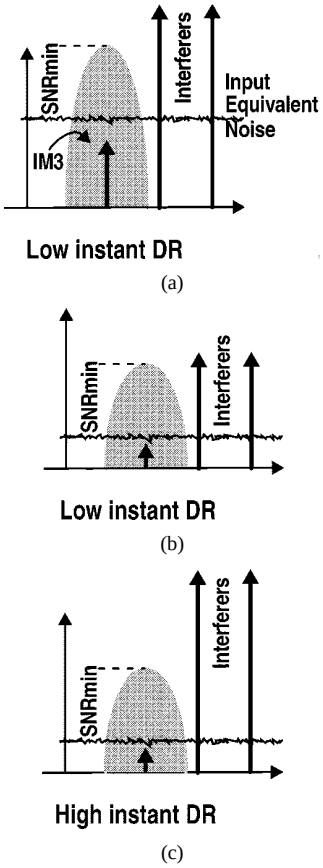

Fig. 3. Three different scenarios for received signals. (a) Strong desired signal. High noise can be tolerated. (b) Weak desired signal and weak interferers. Low linearity can be tolerated. (c) Weak desired signal and large interferers. Low noise and high linearity is required.

III. Adaptive Dynamic Range

In wireless systems, the minimum detectable signal (MDS) and spurious-free dynamic range (SFDR) together quantify the ability of the receiver to detect a very weak desired signal in the presence of strong interferers. A radio signal of interest is received in roughly different conditions. The desired signal may be strong enough to overcome large noise and intermodulation due to nearby interferers [Fig. 3(a)]. In this case, a high receiver NF is acceptable. Alternatively, the desired signal and the interferers are weak, so the signal-to-interference ratio (S/I) is still good (Fig. 3(b)), yet low IIP3 is acceptable. In both cases, the receiver dynamic range may be modest. The worst-case is when the desired signal is weak but the interferers strong (Fig. 3(c)). Now the instant receiver input signal DR is high, which requires high IIP3 and low NF.

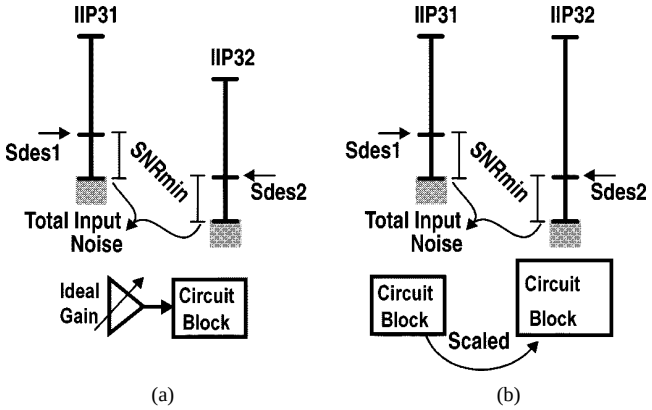

Fig. 4. An illustration of how to achieve: (a) slide DR with preamplification and (b) step DR by substitution of a scaled circuit block.

For least power consumption, the RX DR should adapt to the prevailing conditions. Two types of adaptive DR are possible, *sliding* and *step* [Fig. 4(a)]. In sliding DR, the *instant* DR of the RX is constant but slides to best accommodate the input signal conditions. Fig. 4(a) shows how, by adding a gain stage in front of a noisy and nonlinear circuit block, input referred noise and IIP3 drop by the gain of the amplifier. This *slides* down the entire DR and enables detection of a weaker signal accompanied by weak interferers.

Suppose that at some point the receiver needs higher DR. Scaling up all the transistors in a circuit keeping $V_{\rm GS} - V_{\rm t}$ constant and scaling down all resistors by the same factor lowers input mean square noise and raises bias current proportional to the scale factor, while IIP3 remains unchanged [Fig. 4(b)]. The scaled circuit can pass a weak desired signal accompanied by strong interferers. Thus, DR may be *stepped up* by substituting a scaled version of a nominal circuit.

The circuits comprising this receiver (Fig. 2) use both types of adaptive DR. Assume that the DR and linearity of PGA1 is higher than that of the BPF, while the filter contributes the largest noise at the input. Then the IF strip input IP3 (for interferers in the BPF stopband) can be expressed as

$$\mathrm{IIP3_{IF}\,(dBm)} = \mathrm{IIP3_{BPF}\,(dBm)} - \mathrm{Gain_{PGA1}\,(dBM)}. \quad (1)$$

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When the gain of PGA1 is lowered, $\mathrm{IIP3_{IF}}$ is higher. On the other hand, $\mathrm{NF_{IF}}$ also rises due to the dominant noise of the BPF. Thus, lowering gain in PGA1 slides up the DR.

The on-chip filter is usually the bottleneck to achievable DR in a fully integrated RX. In this design, the BPF adapts power dissipation to the instantaneous needs, as shown in Fig. 4(b). Two filters are implemented with the same topology, but one, scaled up to consume $10\times$ more power, offers $10\times$ lower mean square noise but the same linearity. An algorithm described below senses which of the previously described conditions is present. In the first two instances [Fig. 3(a) and (b)], a BPF dissipating low power is employed for nominal RX DR. However, in the worst-case scenario, the high-power scaled filter is switched in raising total DR. Since the worst-case scenario is infrequent, the low-power filter determines the average RX power consumption.

The algorithm to sense the input signal and determine instant DR is key. Signal power is sensed at four points along the IF strip (Fig. 2): input and output of the analog BPF and input and output of the digital channel select filter. These measured signal levels indicate how much of the received signal is being rejected, respectively, by the analog filter and the digital filter.

The signal at the output of the digital filter (point D_o in Fig. 2) is only the desired channel, with possibly some possible IM3 from adjacent interferers. By comparing the signal level at the output of the analog BPF (A_o) and at the input of the A/D (D_I), the post-filter gain is measured. Then, by comparing the signal level at the input and the output of the digital filter (D_I and D_o), the relative strength of the out-of-channel signal that passes through the analog filter is calculated. The signal level at A_I and A_o is a measure of the out-of-band interferers being rejected by the analog BPF. If the *desired* signal at the output of the analog BPF is strong, as measured by $\mathrm{Power_{Do}}$–$\mathrm{Gain_{Post\text{-}analog\text{-}filter}}$, the scenario is as shown in Fig. 3(a). If the total signal power is comparable at A_I and A_o, and at D_I and D_o, the condition is like Fig. 3(a) or (b). In both cases, the required instant DR is low. If the signal levels are significantly different at either of the above pairs of nodes (A_I and A_o and D_I and D_o) and there is a weak signal at D_o, the condition must be the one shown in Fig. 3(c).

An abrupt switch from the low-power to the high-power filter causes the BER to increase momentarily. However, as data transmitted in frames is preceded by a preamble and training sequence, the desired filter is switched during the preamble and settles during that time, eliminating increase in bit error rate (BER) during the data sector. If the interference increases abruptly during the data sector to the point that the BER exceeds the limit, that data frame is dropped. This frequency-hopping transceiver uses many adaptive algorithms at each hop, which necessitate a lengthy preamble of typically 300 symbols out of a frame that is 5000 symbols long. Therefore, the turn-around time of a few symbol periods can be tolerated. The actual number of symbols required for the system to settle depends on the channel conditions.

IV. Programmable and Variable Gain Amplifiers

As the received QAM waveform modulates carrier amplitude, it requires linear amplification in the receiver. Two sets of pre-filter and post-filter amplifiers are implemented, with different goals. The pre-BPF amplifier, PGA1, slides the input DR of the BPF to best fit the instant level of the input signal, as shown in Fig. 4(a). As mentioned before, for a weak desired signal where a low NF is needed, PGA1 is set to high gain to overcome the high NF of the filter. When the input signal is strong, PGA1 is set to low gain and high OIP3 to preserve the IIP3 of the BPF. The post-BPF amplifiers boost the signal to optimally load the ADC input (90% of the 1 V full scale). If the BPF could perfectly isolate the desired channel, intermodulation would no longer be a concern in the post-BPF circuits. However, when the analog BPF's selectivity is poor at low BW settings as well as the desired channel, it passes a few adjacent channels, thus, the need for a linear post-filter amplifier.

Amplifier gain may be controlled by varying: 1) transconductance (g_m); 2) load impedance; or 3) feedback factor. Bias current sets transconductance. When the input signals are large, the transconductance gain must be low, and simultaneously the intercept point must rise. However, lowering the bias current also lowers the intercept point, which is contrary to what is wanted. Furthermore, as the MOSFET transconductance is at best a square-root function of bias current, the current must change by $100\times$ for 20 dB of change in gain.

Next consider varying gain with the load resistance. If the load is linear, the transconductance amplifier determines both noise and linearity. Therefore, as in the case above, the amplifier DR does not improve when gain is lowered. However, if supply-limited clipping at the output node determines circuit nonlinearity, IP3 improves with lower gain.

Finally, gain may be changed with variable feedback factor. A noiseless feedback block does not affect the equivalent input noise of the amplifier but improves linearity by the loop gain. Therefore, feedback trades off the gain for DR. In this respect, feedback is superior to the methods described above and is used here. In practice, the feedback components add noise of their own that shrinks the improvement in the DR.

A programmable gain amplifier implementing a set of discrete gains may be realized by an array of switch-selectable amplifiers, each optimized for the best DR at fixed gain. By contrast, in a VGA, the gain changes continuously and cannot be optimum over the whole range. For this reason, at a given power consumption and gain range, the DR of a PGA is higher than that for a VGA. Therefore, the PGA should be used in a receiver whenever possible.

The constellation points are very close together in complex modulation schemes like 64-QAM. A sudden variation in gain can easily be mistaken for a change in signal level, and this increases the BER. To avoid this, gain must be stepped in small increments. Fig. 5 shows 64-QAM SNR with PGA gain step [6]. To ensure an SNR of above 40 dB, the gain must be accurate to 0.027 dB. With an 80-dB gain range, this requires 11-bit resolution of PGA gain, which is clearly impractical. On the other extreme, a simple VGA designed to cover 85 dB of gain range dissipates excessive power. The solution is to combine the two.

The best combination is found by exploiting certain features of the system. At the beginning of each hop, the frame starts with a training sequence during which algorithms, such as for carrier recovery, beam forming, clock recovery, and automatic

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gain control (AGC) [6], converge. A jump in gain in this training period does not degrade the BER. Furthermore, the channel does not vary much over the data sector of each frame. Thus, a PGA with a high DR can coarsely set the gain in this time, and during the data sector, VGAs can track the channel variations.

The required VGA range is determined using a channel model. The largest data frame is 5000 symbols, which lasts at most 8 ms at 625 kS/s. Assuming a maximum speed of 2 m/s for the indoor mobile transceiver, an indoor channel model [11] defines the VGA variation to be limited within -14 dB and $+6$ dB for 98% of the time. This needs 20 dB of gain variation in the VGA. The gain range is asymmetric because the system is more prone to ADC overload; thus, the attenuation range exceeds amplification.

A. PGA Circuit Design

The PGAs used in this work all consist of a degenerated differential pair with resistive load. Degeneration improves the linearity of the amplifier and the resistor load alleviates the nonlinearity due to the MOSFET output impedance. The ratio between the nonlinear MOSFET output impedance and the linear load resistor affects overall amplifier linearity, and here limits the maximum gain of each stage to about 15 dB.

As shown in Fig. 6, the local feedback loop gain is changed by switching the degeneration resistor. Although long channel devices do not suffer from excessive noise and their output impedance is large, their large $C_{\rm gd}$ strongly loads the preceding stage and limits the BW. For this reason, all MOSFETs are minimum channel length.

Control switches change the effective degeneration and thus the effective $G_{\rm m}$ of the stage

$$G_{\rm m} = \frac{g_{\rm m}}{1+g_{\rm m}R_{\rm s}} = \frac{g_{\rm m}}{1+\frac{2IR_{\rm s}}{V_{\rm GS}-V_{\rm t}}} = \frac{g_{\rm m}}{1+\frac{2V_{\rm Rs}}{V_{\rm GS}-V_{\rm t}}} \qquad (2)$$

where the term $2V_{\rm Rs}/(V_{\rm GS}-V_{\rm t})$ is the loop gain. With a given MOSFET size and bias current (i.e., the same $g_{\rm m}$ and $V_{\rm GS}-V_{\rm t}$), the headroom available for $V_{\rm Rs}$ limits the loop gain and therefore the gain range.

Gain is also changed with load impedance, but without tradeoff in linearity. Now headroom limits the maximum gain. In order to increase the gain, part of the dc current is supplied by the current sources to reduce the voltage drop on $R_{\rm L}$ [Fig. 7(a)]. This method has some advantages over supplying all the dc by current sources and inserting floating resistors reported before [12] [Fig. 7(b)]. With the current source MOSFETs biased at a certain $V_{\rm DS}$, their output noise current $(i_{\rm n}^2)$ is proportional to their dc current. Using $R_{\rm L}$ to supply the main part of the dc current reduces the total noise from the load current source. Furthermore, a lower bias current results in larger output impedance for the current sources and improves the output linearity. Common-mode feedback (CMFB) is applied to the gates of the current source FETs.

Fig. 8 shows the low-power fine-step PGA (LPWstep in Fig. 9) designed to drive the 0.4-pF input capacitance of the BPF. The gain of this stage varies from 3 to 15 dB in 3-dB steps. For 3-dB gain, all the degeneration switches are open (maximum degeneration) and all the load switches are closed (minimum load resistance), whereas for 15-dB gain

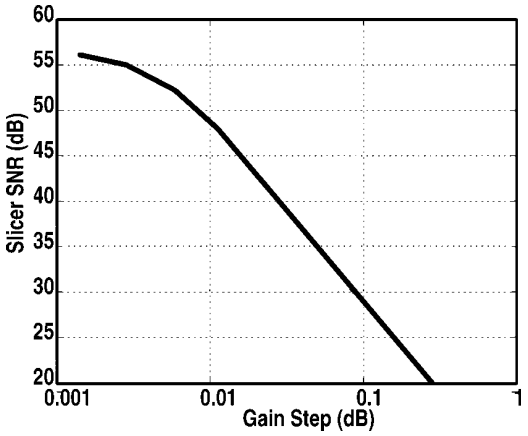

Fig. 5. Detected SNR of 64-QAM bitstream as a function of a gain jump during reception.

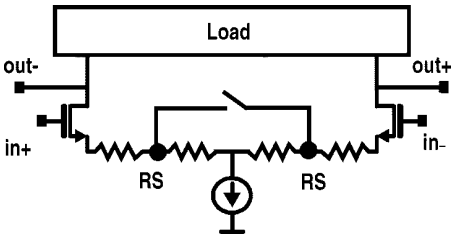

Fig. 6. Switched degeneration with a single tail current source. Voltage headroom limits loop gain.

the switches are in the opposite positions. The high-power low-noise fine-step PGA (HPW step) resembles the circuit of Fig. 8, except it is scaled by factor of 9. The gain of the coarse-step PGA (HPWfix) is 15 dB, and this defines the high gain portion of the fine-step PGA. For 0-dB gain, the amplifier bias current is shut off and its inputs are shorted to its outputs.

The total gain and the bias current of the PGA are set as follows. To overcome the input noise of the low-power BPF, the coarse PGA and two fine-step PGAs amplify the input by up to 30 dB (Fig. 9). The bias current of the PGA blocks is set by two parameters: the required input noise and the filter input capacitance, which is, respectively, 0.4 and 4 pF for the low-power and the high-power versions. The pole frequency associated with the load resistor of the PGA driving the LPF input lies beyond 40 MHz.

The post-filter PGA (PGA2) implements 60-dB gain variation in 3-dB steps, divided among three stages of low-power coarse PGAs and one low-power fine PGA. The HPF function is combined with the PGA function, as will be explained in Section V. Switches sized large enough to drop negligible voltage when in the ON state also contribute negligible noise and nonlinearity.

The gain and noise are related as follows:

$$\text{Gain} \propto G_{\rm m}, \quad \hat{\rm v}_{\rm n} \propto \sqrt{\frac{1}{G_{\rm m}}} \qquad (3)$$

where $G_{\rm m}$ is the degenerated transconductance. Equation (3) assumes that the noise of the input MOSFETs is dominant, which is usually the case in a highly linear low-voltage design. Thus, gain (in dB) decreases twice as fast as $v_{\rm n}$ increases (in dB).

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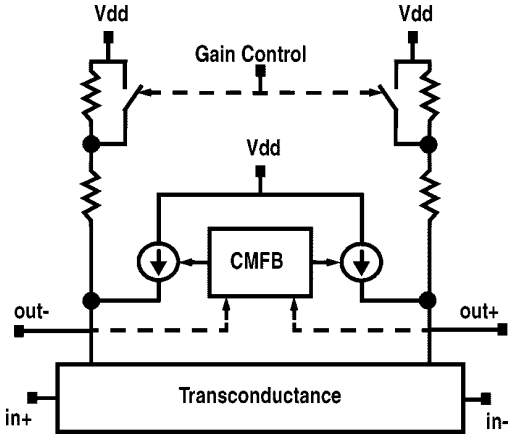
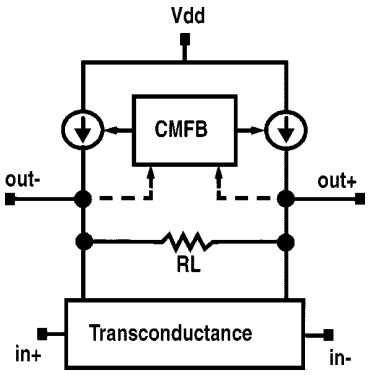


(a)



(b)

Fig. 7. Biaising alternatives with resistor loads. (a) RL connected to supply. A small part of current is supplied by the current sources. (b) Floating load resistor. All bias current is supplied by the current sources.

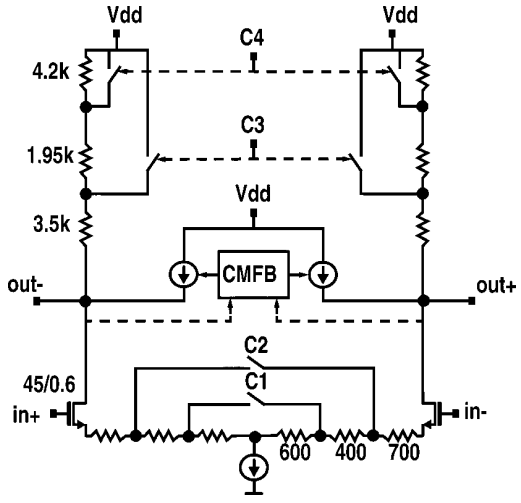


Fig. 8. Fine-step PGA, low-power version.

Short-channel MOSFETs are noisier than long —channel ones [13]. The higher the $G_{\rm m}$ (weaker degeneration), the higher the noise contributed by the MOSFETs, which leads to a weaker decrease in $v_{\rm n}$. On the other hand, as the load resistance is increased, the current sources in parallel with the load must be larger to maintain constant headroom. As a result, their noise contribution and thus $v_{\rm n}$ increase.

At a constant output swing, feedback lowers amplifier nonlinearity by the loop gain T [14] as

$$\begin{aligned} G_{\rm m} &= \frac{g_{\rm m}({\rm OL})}{1+T} \\ {\rm IM3(constant\ output\ level)} &= \frac{{\rm IM3(OL)}}{1+T} \\ {\rm OIP3(input\ limited)} &= {\rm OIP3(OL)} \cdot \sqrt{1+T} \\ {\rm IIP3(input\ limited)} &= \frac{\rm OIP3}{\rm Gain} \\ &= {\rm IIP3} \cdot (1+T)^{1.5} \end{aligned} \tag{4}$$

where OL is the open-loop case without feedback. Equation (4) is valid if the input dominates nonlinearity. However, nonlinearity in FET output impedance is not enclosed by the loop. If this is dominant, the resulting OIP3 will be constant. Now we have

$$\begin{aligned} {\rm OIP3} &= {\rm OIP3(OL)} \\ {\rm IIP3(output\ limited)} &= \frac{\rm OIP3}{\rm Gain} = \frac{\rm OIP3(OL)}{\rm Gain}(1+T). \end{aligned} \tag{5}$$

In practice, at large gains, nonlinearity in the output impedance dominates and produces a constant OIP3. This can be improved with the cascade topology [5].

B. VGA Circuit Design

To continuously vary the gain of the amplifier, a MOSFET in the triode region can be used as voltage-controlled resistor both for degeneration and as the load. However, a MOSFET resistor is nonlinear, especially at low $V_{\rm GS} - V_{\rm t}$, when a small-signal swing can force it into saturation. Linearity may be improved at the expense of range by padding it with linear resistors either in series or in parallel (Fig. 10).

With parallel padding [Fig. 10(b)], the linear resistor dominates when the MOS $r_{\rm ON}$ is at its maximum, which corresponds to low gain, large input signal, and therefore maximum nonlinearity. Thus, parallel padding is better than series. The correct choice of W/L balances linearity with the net variation in resistance. To achieve a wide range, padded stages are used as shown in the differential configuration of Fig. 11. The resulting structure has been termed soft switching [15]. In each stage, the worst-case linearity appears when the MOSFET is turned OFF. The resistors should be turned OFF one by one. In a previous circuit [15], a supply voltage of 5 V was dropped across the various nodes and one control ramp voltage applied to all the gates turned off the FETs successively. In a low-voltage design, however, the voltage drop is low and the MOSFETs will tend to turn off together. Here a resistor ladder generates six staggered voltages from a single control signal (Ext_cont). By properly selecting the resistor values, the decibel gain can be made linear with Ext_cont (V).

In addition to its use for degeneration, the soft-switched variable resistor (SSVR) may also be used for the load. Now ${\rm IIP3_{VGA}} = {\rm IP3_{SSVR}} - {\rm Gain_{VGA}}$ (dB). Since ${\rm Gain_{VGA}}$ is higher than 0 dB, this limits the ${\rm IIP3_{VGA}}$. If used as degeneration, the input signal is divided between the input transistors and the SSVR. Furthermore, at high gain settings, the input

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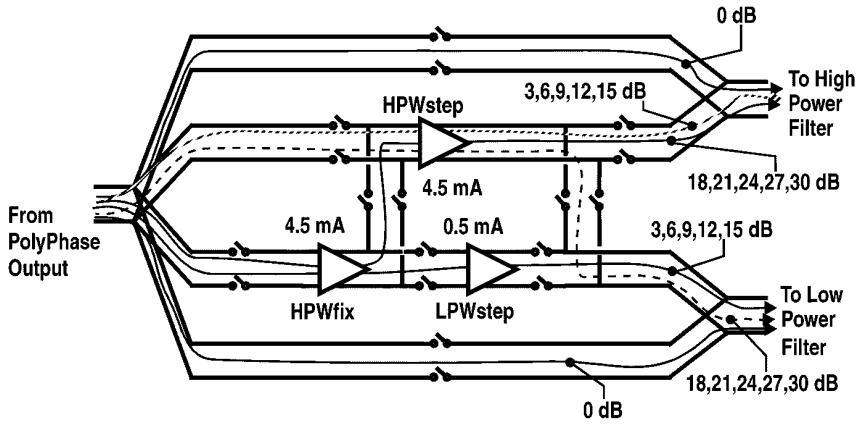

Fig. 9. Combination of PGA stages realizing PGA1.

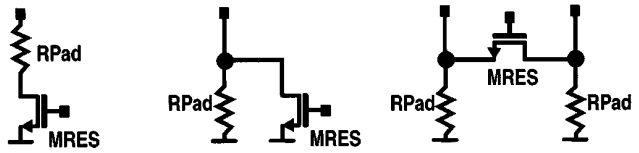

Fig. 10. Illustrating degeneration by: (a) serial resistor padding, (b) parallel padding and (c) parallel differential padding.

swing is lower than the output swing. Thus, on considerations of linearity, SSVR is better suited to degeneration.

This differential circuit does not use constant current bias. Simulations show that removing the tail current source improves linearity by up to 10 dB. The MOSFET resistor can be used floating or grounded. Although the floating SSVR has 0 dc voltage drop and higher linearity, with grounded SSVR, the dc path changes, and so does the dc current. For low-voltage applications, the change of bias due to the grounded MOSFET resistors is desirable. In this design, a combination of both has been used. In Fig. 11, as cont1 rises to increase the gain, the voltage of node 1 decreases, providing higher voltage drop on the other resistors.

The variable transconductance section of the VGA with SSVR degeneration is designed as follows. First, a bias voltage is chosen at the input ($V_{\rm IP}$ and $V_{\rm IN}$) as dictated by the preceding stage, or for highest linearity. Then the length of the input FETs is selected either from considerations of excess noise in short channel FETs, or from the maximum tolerable capacitance at the input. Next, the $V_{\rm GS}-V_{\rm t}$ is selected for the desired linearity by setting the fixed degeneration resistor. For a degeneration stage with constant input bias voltage, higher $V_{\rm GS}-V_{\rm t}$ results in weaker degeneration and lower linearity, but higher $G_{\rm m}/I_{\rm bias}$. The degeneration element consists of fixed linear resistors, in series with a floating differential MOSFET resistor. The FET W/L is chosen to be the largest that gives the required linearity. The worst-case scenario is when the MOSFET is close to the OFF. The top half resistor (the linear resistor between the MOSFET resistor and input FETs) is divided into two parts and another MOSFET resistor is inserted at the new middle node. This procedure is repeated until the required variation range is obtained.

The prototype circuit is scaled until the required input referred noise is obtained. The final VGA stage [Fig. 11(a)] provides a gain range from -1 to 8 dB. Three such stages in cascade give a gain variable from 0 to 20 dB with margin.

V. Bandpass Filter

The analog BPF partly selects the desired channel to lower the required DR for the A/D. Fig. 12 shows the SNR at the input of the demodulator for a 64-QAM constellation, with 90% A/D loading [6], for a single channel. A resolution of at least 8 bit is required. If the out-of-band channel power passing through the A/D (I) is comparable to or larger than the desired signal (S), then the A/D must resolve the following number of additional bits to accommodate the interferers, which is roughly:

$$N=\frac{\text{Int}\left(\frac{I}{S}+3\right)}{6\text{ dB}}.$$

A powerful digital channel equalizer used in the DSP, shown in Fig. 2, compensates for the BPF passband ripple and group delay [6]. This relaxes the specification of the analog filter. A $g_{\rm m}$–C realization is used for its good high-frequency performance.

A high-order LPF is cascaded with a low-order HPF for symmetric transition regions [7], which gives the minimum power consumption. To vary the BW of the resulting BPF, the lower cutoff is fixed at 5 MHz and only the higher cutoff frequency is tuned to define the filter passband. The HPF offers programmable gain of 0 to 45 dB. The details of the BPF design are presented elsewhere [7].

Fig. 13 shows the post-filter amplifiers. The first three blocks are a PGA-HPF, which give a coarse-gain variation of 0 to 45 dB in steps of 15 dB. Next, a fine-step PGA increments gain in 3-dB steps up to 15 dB. Finally, three VGA stages in cascade provide 27 dB of continuous gain variation prior to the A/D.

VI. Standalone IF Strip Implementation and Measurement Results

The IF strip was implemented in a 0.6-μm CMOS process and operates at a 3.3-V supply. First, the PGA blocks (Fig. 9) are

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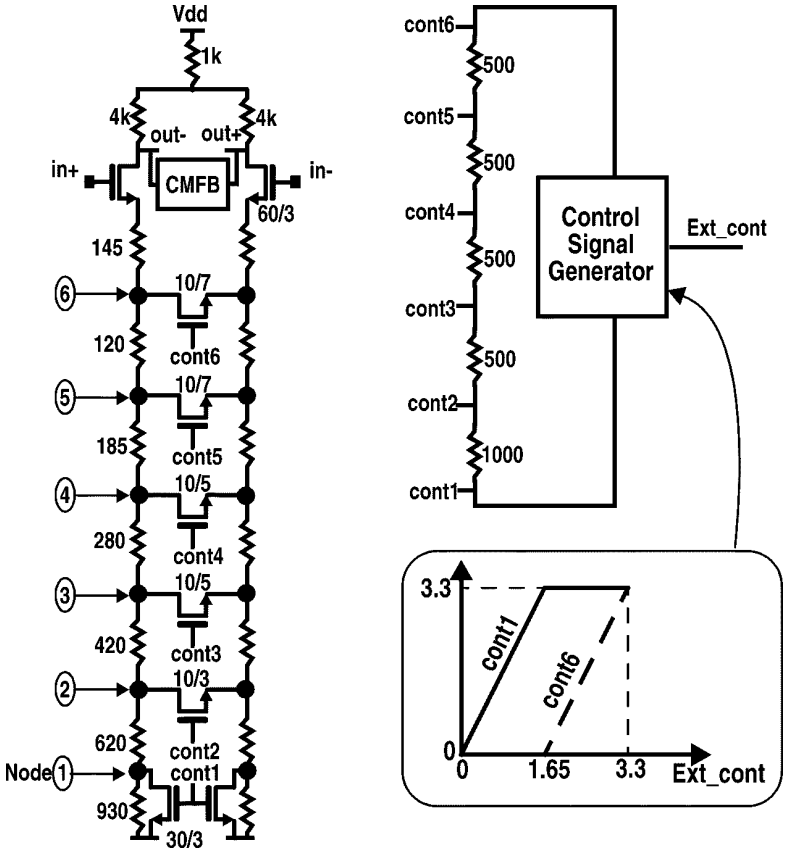

(a) (b)

Fig. 11. (a) VGA circuit using soft-switched degeneration. (b) Resistor ladder and control voltages.

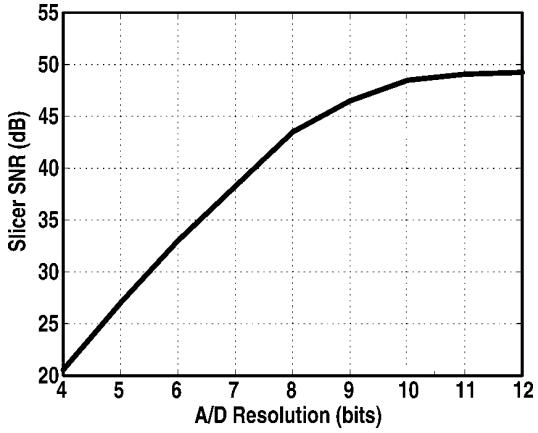

Fig. 12. Detected SNR of a 64-QAM signal versus A/D resolution, assuming signal loads A/D 90% at the peak.

experimentally characterized. Fig. 14 shows the OIP3 and the differential input referred noise of the PGA1. The low-power fine-step PGA (LPWstep) is the same one as in Fig. 8. Since the measured OIP3 versus gain is almost constant, it may be concluded that output impedance nonlinearity dominates. The input noise decreases due to the growing transconductance as the gain rises from 3 to 9 dB. For 12- and 15-dB gain settings, load resistance is stepped up, as is the current through the output current sources (Fig. 8). Now current source noise raises the total input-referred noise of the stage.

Fig. 15 plots the gain of one VGA stage biased at 0.6 mA versus the input control voltage. The gain (in dB) is fairly linear with $V_{\mathrm{Cont}}(\mathrm{V})$, with a peak deviation of 0.4 dB. The input noise and OIP3 of the VGA is shown in Fig. 16. The noise is very close to simulations, however, the OIP3 is about 4 dB lower than expected mainly due to the shortcomings of the BSIM2 models used. Table I compares the result of this design with recent published works. The characteristics of this work are scaled to match the gain and the power consumption of each reference circuit by cascading the required number of stages and scaling the resulting circuit for power. Except for the model in [16], the designed VGA and PGA surpass the others in DR. The circuit in [16] has lower noise due to high g_{m} bipolar transistors, but it requires a high supply voltage.

The low-power and high-power LPFs drain 6 mA and 60 mA from the supply, with $50\ \mathrm{nV}/\sqrt{\mathrm{Hz}}$ and $17\ \mathrm{nV}/\sqrt{\mathrm{Hz}}$ differential input noise, respectively. Since switched capacitors control filter bandwidth, the g_{m} variation is not very large. The input noise density is therefore almost independent of the BW. The in-band and stopband IIP3 of both LPFs are 18 and 22.5 dBm (referred to 100 Ω differential) respectively. They are measured for a BW of 10 MHz, with two tones of 10 and 11 MHz for in-band IIP3. For stopband IIP3, two sets of tones were used, 30/50 MHz and 40/70 MHz. Each stage of the PGA-HPF consumes 1.8 mA, with 40 and $7.9\ \mathrm{nV}/\sqrt{\mathrm{Hz}}$ noise for 0- and 15-dB gain respectively. The OIP3 of the PGA-HPF for in-band and out-of-band interferers is 28 and 24 dBm (referred to 100 Ω), respectively.

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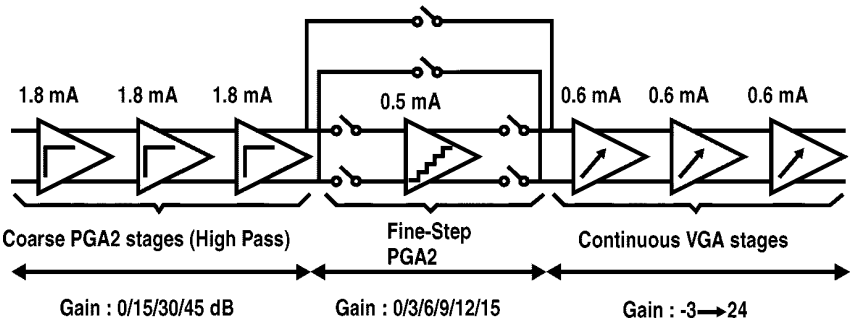

Fig. 13. Post-filter PGA2 with HPF, and VGA.

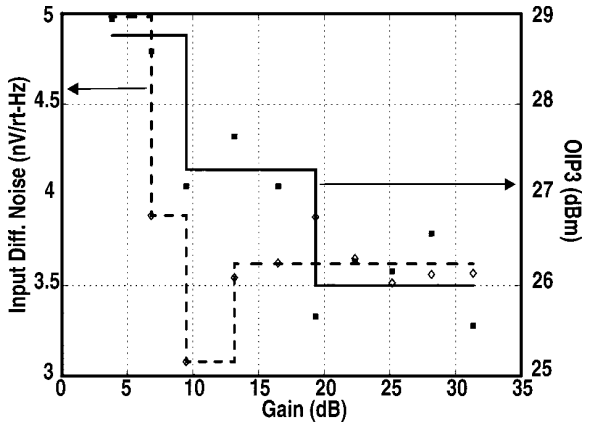

Fig. 14. Measured noise and output of IP3 of prefilter PGA (shown in Fig. 9) versus gain, when LPWstep is used.

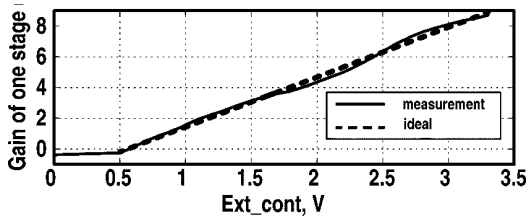

Fig. 15. Gain of one VGA stage versus control voltage.

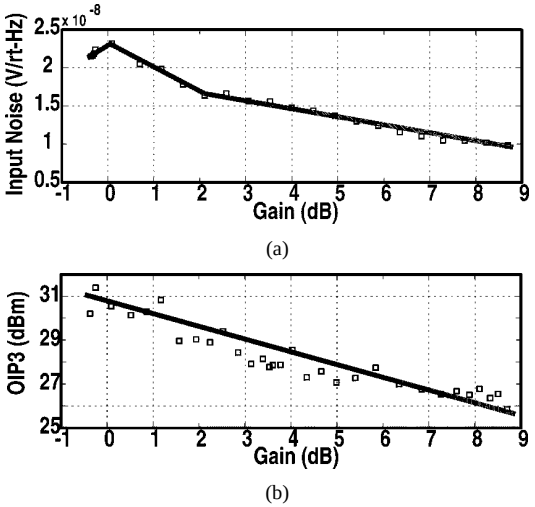

Fig. 16. (a) Noise and (b) output IP3 of one VGA stage versus gain.

Since the transconductance stages used in the filters do not have any common-mode rejection, mismatch between two sides of the transconductance stages causes common-mode to differential conversion. Now noise on the substrate and supply can appear differentially at the filter output. With post-filter gain as high as 83 dB, stability of the IF strip is an important concern. Very careful common-centroid layout of all blocks limits signal injection to the substrate, differential signal pickup from the substrate, and the conversion of common-mode signals to differential. Total post-filter gain was varied from 0 to 83 dB [Fig. 17(a)] on the packaged test chip with no instability. A small constant input is applied during this measurement on a network analyzer, and the filter stopband lies below the noise floor. Fig. 17(b) (from [7]) shows the variable BW in the IF strip. The passband ripple in the worst case of 10 MHz BW is less than 3 dB. For lower BW settings, the passband ripple is less than 1 dB.

Two sets of measurements are devised to show adaptivity in dynamic range and power consumption. First the output $\mathrm{SNR}_{\mathrm{min}}$ at 1.6 Vptp differential output is set to 14 dB for a 625-kHz-wide channel. As the BPF significantly attenuates interferers lying in its stopband, linearity of the post-filter blocks is not important. At minimum detectable input signal [Fig. 18(a)], the input NF should be as low as possible. With weak interferers, prefilter gain is set to maximum (30 dB) to overcome filter noise. Strong interferers will generate in-band IM3 products. The interferers are made stronger, the IM3 components rise, and, when the interferer tones are at -42 dBm, the distortion products are equal to the input equivalent noise. Since the filter limits overall IIP3, the gain of the prefilter amplifier is lowered to improve linearity. However, this increases the NF at the input and will degrade SNR of the desired signal, but

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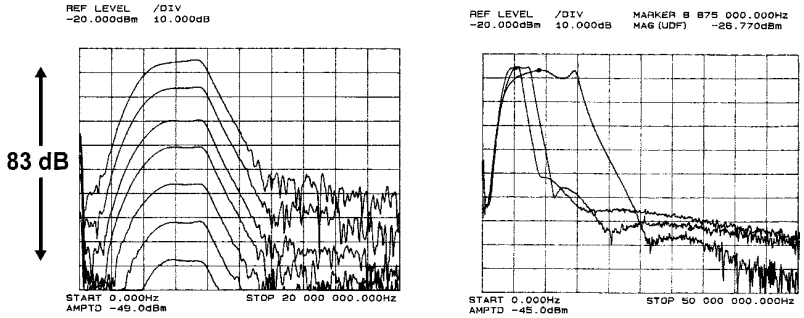
TABLE I
COMPARISON OF THE DESIGNED PGA AND VGA WITH OTHER PUBLISHED WORKS

		mA	MHz (Ours 50)	Noise (nV/rt-Hz)		Linearity (dBm wrt 100 ohm)		Rel SFDR (dB)
				Theirs	Ours	Theirs	Ours	
VGA [11]	0.6 µm CMOS	10	20	12.7	7	20	22	+4.8
VGA [16]	12 GHz BJT (5 V)	8	35	1.6	4.7	30	26	-8
						24	25.5	-5
VGA [17]	0.6 µm BiCMOS	12	200	1.9	5.1	-3	24	+12
VGA [18]	0.6 µm CMOS	10	10	25.8	4.2	28	26	+9
PGA [19]	0.6 µm CMOS	2	71	5.4	9.7	-3	14	+8



(a) (b)

Fig. 17. IF strip frequency response: (a) when changing post-filter gain by 85 dB and (b) at the three BW settings.

the high-power, low-noise LPF is now activated to improve the instant DR of the IF strip by about 6.5 dB.

When the desired input signal is larger, the DR must slide to the best level. Fig. 18(b) shows sliding DR for progressively larger input signals, when higher NF due to lower prefilter gain can be tolerated. For example, if the desired signal rises from -92 to -88 dBm, the NF can rise from 9.5 to 13.5 dB while maintaining the same detector SNR. Thus, for the low-power LPF, the prefilter gain can drop from 30 to 21 dB, which increases the IF strip IIP3 from –8.6 to 0.4 dBm. For the high-power LPF, gain can drop from 21 to 9 dB which raises the IF strip IIP3 from 0.4 to 12.4 dBm.

When the desired signal is higher than -70 dBm, a satisfactory SNR is obtained even with 0-dB prefilter gain. Now IIP3 is the highest possible (22.5 dBm). Using the low-power LPF, the receiver SFDR is higher than 70.5 dB. Two-tone interferers as large as -70 dBm $+$ 70.5 dB $=$ $+0.5$ dBm may be tolerated at the input to the IF strip. There is no need to switch in the high-power LPF.

Next, consider a desired channel of 625 kHz BW at the input to the IF strip, accompanied by strong nearby adjacent channel interferers which are only mildly attenuated in the analog filter. If the interferers are stronger than the desired signal, after amplification they will occupy the A/D input full scale. Since the quantization noise relative to the total peak signal at the input of the A/D is constant, this degrades the SNR for the smaller desired signal. In general, the signal-to-quantization-noise ratio is

$$\mathrm{SNR}\left(\frac{A}{D}\mathrm{Output}\right) = 6.02N + 1.8 - \text{Rel Crest Factor} - \text{Margin} + \mathrm{OSF} \quad (6)$$

where relative crest factor is with respect to a single tone. The two first terms represent Full scale$/N_{\mathrm{Quantization}}$ [20]. The maximum possible signal corresponds to a dc input at full scale. However, SNR is calculated with the rms signal, which is always less then the peak for non-dc waveforms. The Crest Factor, defined as the ratio between the peak value and the rms of a waveform, takes this into account. To avoid A/D overload, the peak signal is usually set less than the A/D full scale, which is the Margin. The quantization noise has a flat spectral density from DC to $f_s/2$. Increasing the sampling rate beyond the Nyquist rate by the oversampling factor (OSF) lowers the in-band quantization noise.

In the scenario being examined, two-tone interferers pass through the filter with little attenuation and are amplified by the AGC to 90% of the full scale of the 8-bit A/D. To avoid aliasing of the bandpass signal, the sampling frequency must

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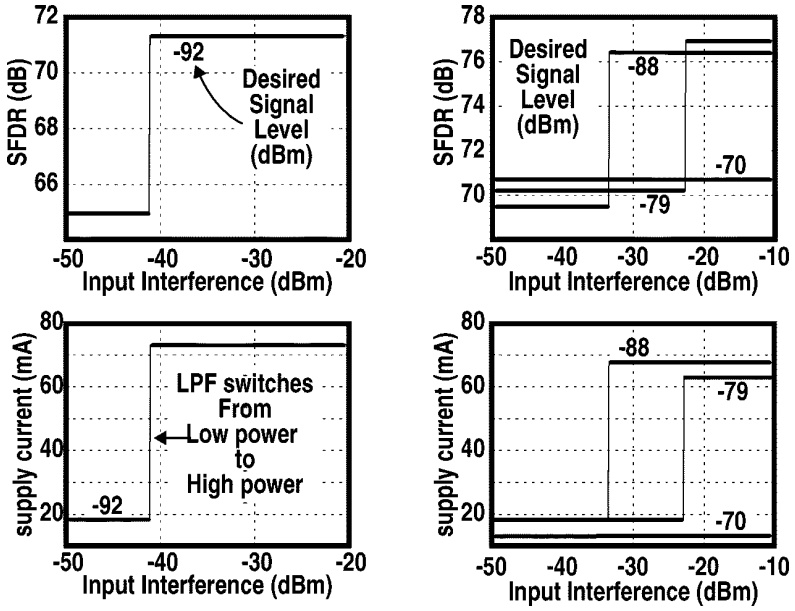
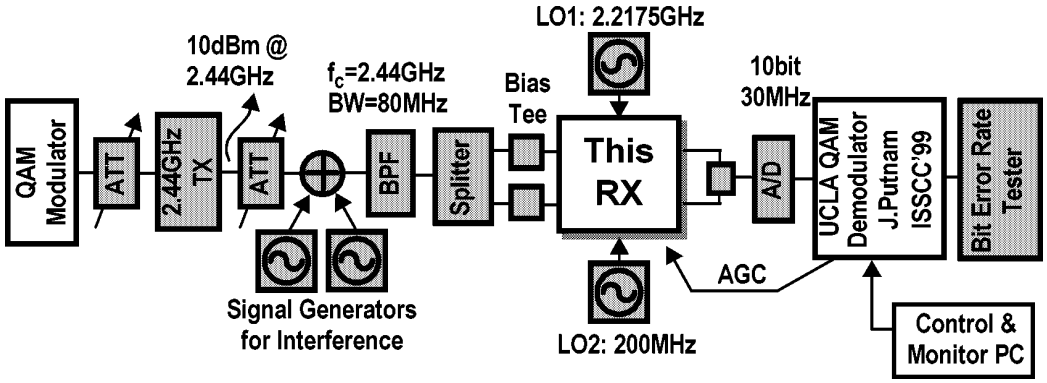
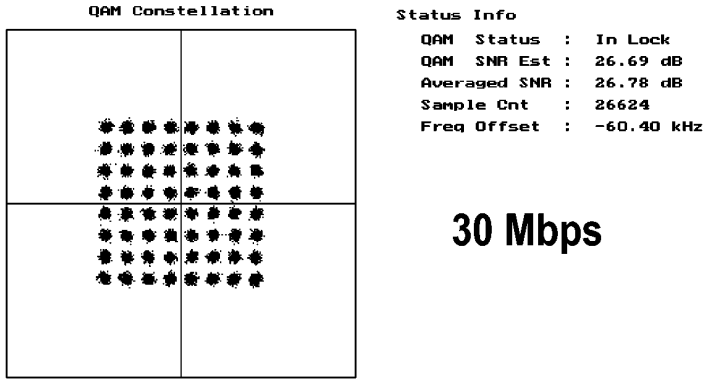


(a) (b)

Fig. 18. Adapting dynamic range to levels of interferer and desired signal. (a) Desired signal at the minimum level. (b) At three levels of the desired signal.



(a)



(b)

Fig. 19. (a) RX measurement setup. (b) Measured 64-QAM constellation at the baseband.

be $4 \times (5\ \text{MHz} + 625\ \text{kHz}/2) = 21.25\ \text{MHz}$. For two equal sinusoids at different frequencies, we have

$$\text{Rel Crest Factor} = 20\log\left(\frac{\text{Peak of Two Tones}}{\text{RMS of Two Tones}}\right) - 3\,\text{dB} = 3\,\text{dB}.$$

Thus,

$$\text{SNR}\left(\frac{A}{D}\text{Output}\right) = 6 \times 8 + 1.8 - 3 - 20\log(0.9) + 10\log\left(\frac{\frac{21.25}{2}}{0.625}\right) = 58.2\,\text{dB}.$$

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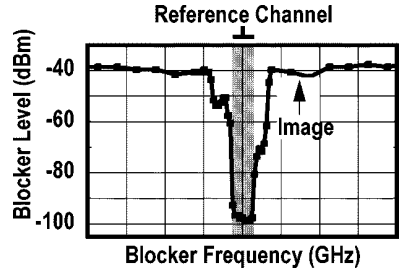
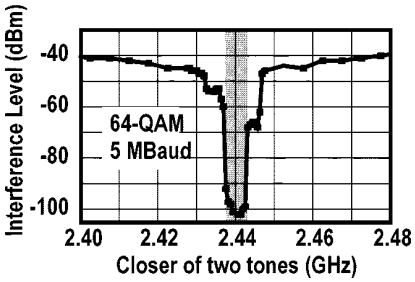
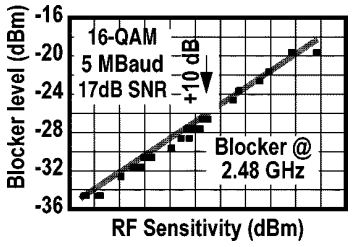


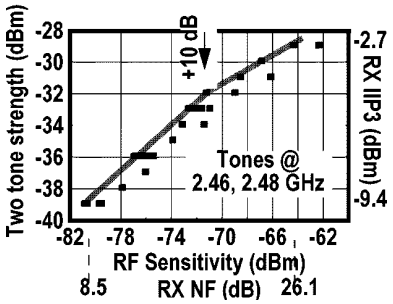
(a)



(b)



(c)



(d)

Fig. 20. Complete receiver measurements. (a) Single-tone blocker strength at various frequencies which desensitizes receiver by 3 dB. (b) Two-tone strength which desensitizes receiver by 3 dB because the intermodulation product lies on the reference channel. (c) Sensitivity versus blocker strength as the IF section adapts. (d) Sensitivity versus IIP3 as the IF section adapts to two in-band tones.

If the last VGA, whose OIP3 is 27 dBm, amplifies each tone to the maximum level of -1.5 dBM, the output node will dominate the nonlinearity. Thus, IM3 with respect to the peak power is $-2 \times (27 - (-1.5)) = 57$ dB. In this extreme case, the poor close-in rejection of the analog BW degrades the sensitivity of the IF strip by only $58.2 - 57 = 1.2$ dB. Assuming 4-QAM modulation with $\mathrm{SNR}_{\min} = 13.5$ dB, the DSP is able to demodulate a desired signal lying $57 - 13.5 = 43.5$ dB below the interferer level.

When the channel bandwidth is 2.5 MHz and 10 MHz, the SNR at the output of the A/D drops to 55.9 and 51.9 dB, respectively, due to the lower oversampling ratio. In these cases, the filter substantially attenuates adjacent and farther channels, the worst-case IM3 stays well in the quantization noise floor, and thus the linearity of the post-filter blocks does not limit the sensitivity of the IF strip.

TABLE II
COMPLETE RX PERFORMANCE

NF	8.5 dB, min
IIP3	-9.4 dBm to -2.7 dBm
Channel BW	625 kHz, 2.5 MHz, and 10 MHz
Max throughput	50 Mbps (with 64-QAM)
Inband ripple Stopband rejection	0.5 dB , 2.5 dB 53 dB , 65 dB
Image Rejection	>75 dB for RF mixer 60 dB for IF mixer
Max RX voltage gain	115 dB
Bias Current	50 mA, Average 100 mA, Peak
Supply Voltage	3.3 V
Process / Area	1P3M, 0.6 μm CMOS / 20 mm^2

VII. COMPLETE RX MEASUREMENT RESULTS

Fig. 19(a) shows the measurement setup for the whole RX. Separately developed QAM modulator and demodulator chips were used for end-to-end data transmission. Fig. 19(b) shows the received constellation at the baseband for 64-QAM, 5-Mbaud signal at a BER of 10^{-6}. In this case, with -71.5 dBM input power the total NF of the RX is deduced to be 8.5 dB.

Interferer measurement results are shown in Fig. 20. The interferer levels shown desensitize the receiver by 3 dB in the desired channel. Fig. 20(a) plots the blocker tolerance level. It shows that the on-chip filter largely suppresses the blocker. The blocker tolerance at image frequency is only 2 dB worse than the other side of the BPF, proving the effectiveness of the on-chip image rejection. Fig. 20(b) shows the two-tone test results and the frequency axis corresponds to the closer tone. Fig. 20(c) and (d) show the effect of the sliding DR in the RX. Dots are the measurements for various gain combinations of RF mixer, first IF amplifier [5], and prefilter PGA. By decreasing the gain in the path, the blocking immunity and linearity of the RX increases, and so does the NF. When the input signal is strong, the high NF can be tolerated. For instance, if the input desired signal is 10 dB higher than the sensitivity level, the blocking tolerance improves by 10 dB and the IIP3 improves by about 5 dB. The IIP3 of the RX ranges from -9.4 dBM to -2.7 dBM and the blocker may be as large as -20 dBM. Table II summarizes all the RX performance.

VIII. CONCLUSION

An IF strip is implemented in a 0.6-μm CMOS for a wireless RX. The active filter in the IF strip supports various baud rates. The dynamic range adapts to the prevailing channel condition by selecting one of the two versions of the BPF, low-power or

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low-noise. A BPF realized by an LPF in series with HPF lowers power consumption. A combined VGA and PGA provided the optimum solution for a packet 64-QAM modulation. Adaptation using a sensing algorithm that switches either gains or circuit blocks is shown to significantly improve the RX dynamic range without increasing average power consumption. A complete receiver consisting of the IF strip integrated with the RF front-end has been evaluated using end-to-end BER measurements with 64-QAM. Cascade NF of the receiver is 8.5 dB at maximum sensitivity, and cascade IP3 is -2.7 dBm with respect to 50 Ω at maximum linearity.

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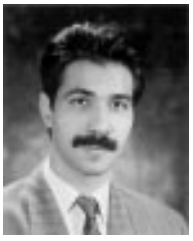
Dr. Behbahani was a corecipient of the second prize in the annual Iranian National Research Contest in 1996 and the IEEE Solid-State Circuits Society Pre-Doctoral Fellowship in 1997. He received the Young Scientist Award from the Association of Professors and Scholars of Iranian Heritage in California in 1999. He was also recognized as the outstanding Ph.D. in Electrical Engineering from UCLA in 2000.



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His area of interests include analog ICs for communications, wireless transceiver architecture and circuit design, and nonlinear circuit analysis.

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Dr. Abidi served as the Program Secretary for the International Solid-State Circuits Conference from 1984 to 1990, and as General Chairman of the Symposium on VLSI Circuits in 1992. He was Secretary of the IEEE Solid-State Circuits Council from 1990 to 1991, and from 1992 to 1995 he was Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS. He has received the 1988 TRW Award for Innovative Teaching and the 1997 IEEE Donald G. Fink Award, and is corecipient of the Best Paper Award at the 1995 European Solid-State Circuits Conference, the Jack Kilby Best Student Paper Award at the 1996 International Solid-State Circuits Conference (ISSCC), the Jack Raper Award for Outstanding Technology Directions Paper at the 1997 ISSCC, the Design Contest Award at the 1998 Design Automation Conference, and an Honorable Mention at the 2000 Design Automation Conference. He received an IEEE Millennium Medal.

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