A CMOS Limiting Amplifier and Signal-Strength Indicator

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Introduction

Mobile radio handsets require an on-chip circuit to measure the received signal-strength. This information is sent to the base station to regulate the transmitted power level, and to determine cell-handoff. As strong attenuation and fading may cause the received signal power to span 6 to 8 decades, the measurement circuit must have a semi-logarithmic input-output characteristic to encompass this dynamic range.

The design of logarithmic amplifiers is now a well-established, although specialized, art. Unlike older implementations, these amplifiers no longer derive a logarithmic characteristic from the PN junction I-V characteristic; instead, they use the *successive-detection* architecture [1], wherein the sum of equally-weighted taps along a cascade of identical clipping amplifiers approximates the logarithm as a piecewise-linear function (Fig.1). A DC measure of the amplitude of a bipolar signal such as a sinewave is obtained by rectifying each tap, and lowpass filtering the sum of the rectified taps. These measurements will be accurate to the degree the actual amplifier input-output characteristic conforms to the ideal logarithm, and how stable it remains over the operating temperature range. Both these qualities are captured by the deviation of the actual characteristics from the ideal logarithm, specified as a gain ripple in dB.

Although all commercially available monolithic log amps today are bipolar ICs [2-5], CMOS is equally well-suited to implement the successive-detection architecture. We report here on the design and performance of such a logarithmic amplifier, which is part of a monolithic all-CMOS spread-spectrum 900 MHz wireless transceiver [6]. In the intended use, a received 160 kb/s binary-FSK signal is amplified at RF, directly downconverted to DC, and applied to the logarithmic amplifier after channel-select filtering. The amplifier provides two useful outputs. First, the limited output from the cascade of clipping amplifiers contains the data encoded as signal *phase* in the zero-crossings. This is directly applied to a correlating 1-bit digital detector for binary-FSK [6], without need for AGC. Second, the circuit produces a logarithmic signal-strength measurement to an accuracy of 1 dB over a 80 dB dynamic range, which a slow 7-bit A/D converter digitizes for uplink to the base-station.

The salient features of this logarithmic amplifier are: operation to 2.7-V supply, 0.75 mA current drain with a 5 MHz bandwidth, 80 dB dynamic range, 84 dB limiting gain, and implementation in 1-μm CMOS.

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Circuit Design

The useful dynamic range of a successive-detection amplifier is limited on the upper end when the input causes the first stage in the cascade to clip, and on the lower end when all stages are in the linear region. In practice, if the amplifier noise causes the last stage to limit, it will determine the lower end. The amplifier characteristics will accurately conform to the logarithm over this dynamic range when a large number of clipping amplifier blocks, each with a relatively small gain, is cascaded. For instance, with a gain of 10 dB per stage and an ideal rectifier, the ripple in the DC logarithmic characteristic is 0.3 dB [4]. We use a cascade of 7 direct-coupled, balanced clipping amplifiers, each with 12 dB gain, and sum the output of 8 rectifiers along the cascade (Fig.1). Each stage consists of an NMOS differential pair with NMOS loads, and its gain, therefore, depends mainly on device-ratio, and to a large extent is process- and temperature-independent (Fig.2). The input and output common-mode levels are the same. A four-quadrant MOS multiplier rectifies the balanced signal at each tap in the cascade (Fig.3). Single-ended output currents taken from all 8 rectifiers are summed into an on-chip 10kΩ polysilicon resistor, and filtered by an off-chip 1-μF capacitor. All circuits are designed for operation at 2.7 V supply.

A well-designed bias source is important in attaining stable logarithmic characteristics. An on-chip replica circuit generates bias voltages for the current sources in the amplifier and rectifier (Fig.3).

Experimental Results

An off-chip *RC* circuit with a cutoff frequency of 3 Hz is connected in negative feedback between the limiting output and amplifier input, to stabilize the bias and suppress DC offsets. All measurements are made with a variable-amplitude 455 kHz sinewave capacitively-coupled into the amplifier. This is the standard 2nd IF in FM cellular telephones, and a sufficiently high frequency to cover the baseband spectrum of 160 kb/s binary-FSK.

The amplifier output is observed to limit on its own noise, as is customary in limiting amplifiers of high sensitivity. The signal-strength output conforms well to the logarithm over more than 80 dB, with a minimum detectable signal of -80 dBm (32 μV amplitude), which is also close to the equivalent input noise voltage (Fig.4). A ripple of ±0.5 dB is observed at all tempera-

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tures, but owing to a small temperature-dependence of gain, the error curve acquires a slope which exacerbates the total error to ±1 dB at 85°C relative to the room-temperature characteristic (Fig.4(b)). This is acceptable for the intended application, and a considerable improvement over the ±3 dB ripple in a previously published CMOS logarithmic amplifier [7].

A ±1V ptp differential square-wave with well-defined zero-crossings is observed at the limiting output across the entire dynamic range. The group-delay through the cascade must also stay relatively constant over this range [5], otherwise the detected SNR, which is sensitive to phase of the received signal, will suffer. We measure this to vary by less than 100 ns across all amplitudes (Fig.5), which the resultant 16° peak phase-error will cause only a 0.2 dB loss in SNR.

The 1-μm CMOS N-well IC occupies an active area of 1 sq mm, and drains a total current of 0.75 mA from 2.7 V.

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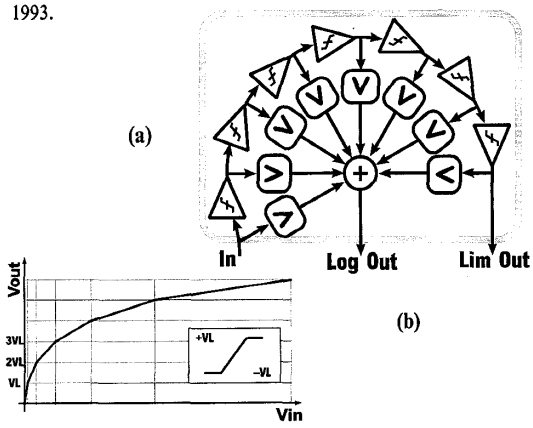

Fig.1. (a) Principle of successive-detection logarithmic amplifier. Yields both logarithmic and limited outputs. (b) Piecewise-linear approximation to log function. VL is clipping-level of each amplifier.

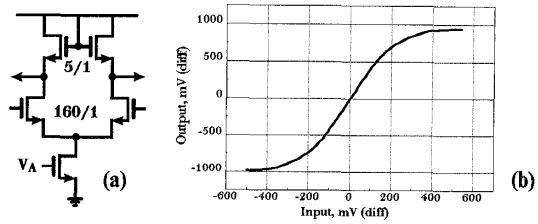

Fig.2. (a) Single clipping amplifier, and (b) its measured input-output characteristic.

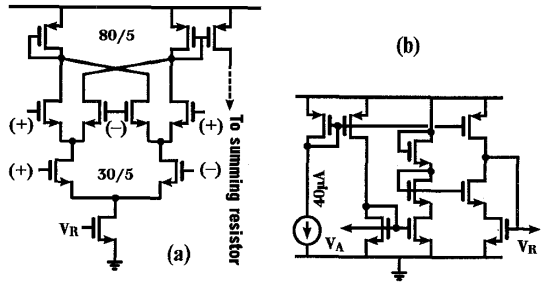

Fig.3. (a) Single full-wave rectifier. (b) Replica-bias circuit.

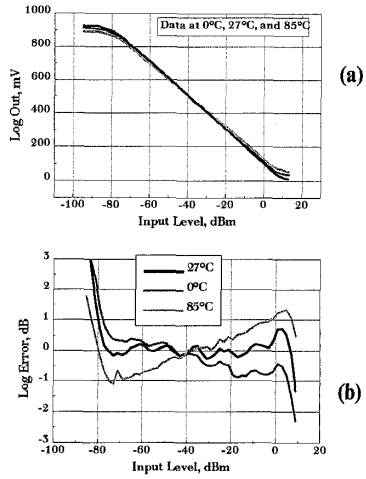

Fig.4. (a) Measured characteristic at Log Output, over temperature. (b) Measured deviation from ideal logarithm, with 27°C as reference.

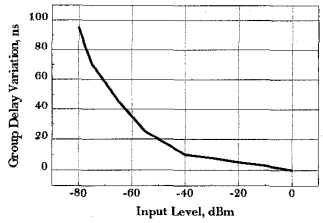

Fig.5. Variation in group-delay through Limiting Amplifier, over the complete dynamic range.

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