

DIGITAL SIGNAL  
PROCESSING IN  
COMMUNICATION  
SYSTEMS

# DIGITAL SIGNAL PROCESSING IN COMMUNICATION SYSTEMS

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**VNR** VAN NOSTRAND REINHOLD  
New York

IPR2024-00817

Apple EX1038 Page 1

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Library of Congress Catalog Card Number 93-25299  
ISBN 0-442-01616-6

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Printed in the United States of America

Van Nostrand Reinhold  
115 Fifth Avenue  
New York, NY 10003

ITP Germany  
Königswinterer Str. 418  
53227 Bonn  
Germany

International Thomson Publishing  
Berkshire House, 168-173  
High Holborn, London WC1V 7AA  
England

International Thomson Publishing Asia  
38 Kim Tian Rd., #0105  
Singapore 0316

Thomas Nelson Australia  
102 Dodds Street  
South Melbourne 3205  
Victoria, Australia

International Thomson Publishing Japan  
Kyowa Building, 3F  
2-2-1 Hirakawacho  
Chiyada-Ku, Tokyo 102  
Japan

Nelson Canada  
1120 Birchmount Road  
Scarborough, Ontario  
M1K 5G4, Canada

16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1

Library of Congress Cataloging in Publication Data

Frerking, Marvin E.

Digital signal processing in communication systems / Marvin E.

Frerking.

p. cm.

Includes index.

ISBN 0-442-01616-6

1. Signal processing—Digital techniques. 2. Digital communications. I. Title.

TK5102.9.F74 1993

621.382'2—dc20

93-25299  
CIP

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## Dedication

This book is dedicated to my wife, Shirley, who encouraged and supported the work and generously gave of her time to type the manuscript. The author would also like to thank Linda Frerking for the many hours she spent drawing illustrations.

The algorithm converges fairly quickly after an initial guess  $x_0$ . As an example, suppose we initially choose  $x_1 = 0.707$ , regardless of the value of  $E$ . The convergence sequence for  $1/(2E)$  for values of  $E = 0.5$  and  $1.0$  are given in Table 6.1. As can be seen, only three iterations are required to provide an accuracy better than 0.1 percent, if  $E$  is prescaled to the range  $0.5 < E < 1.0$ . The result, of course, must be adjusted by shifting as many places—but in the opposite direction, as were performed in the prescaling operation.

The second algorithm suggested for finding the value of  $1/E$  is to use a two-entry look table, as described earlier in the chapter for other functions. The value of the reciprocal can then be calculated using the equation

$$\frac{1}{E} = M_i E + C_i \quad (6.159)$$

where  $M_i$  and  $C_i$  are taken from the table. Good results can be obtained by using an eight-place table if  $E$  is prescaled so that  $0.5 \leq E \leq 1$ . The methods discussed in Eqs. (6.23) and (6.28) can be used to find the table values.

The adjustment range of a compressor theoretically can be made very large. However, for best results, it should be limited to 15 or 20 dB. If this is not done, the background noise may become objectionable when no one is speaking. This can be accomplished by checking the value of  $M(n+1)$  after each iteration of Eq. (6.147) and setting it equal to the maximum permissible value if a larger value is calculated.

## AUTOMATIC GAIN CONTROL

A function similar to the audio compressor is required in a radio receiver for regulation of the amplitude of the signal for varying input signal levels. The problem is more complex in the receiver, because the signal may vary over a large range, depending on the power level transmitted, the proximity of the transmitter to the receiver, the propagation conditions, the antennas used, and other factors. It is possible that a receiver that is required to receive a  $3 \mu\text{V}$  signal at one time, on

TABLE 6.1 Convergence of  $1/(2E)$  Algorithm

| Iteration Number | Reciprocal of $2E$ |           |
|------------------|--------------------|-----------|
|                  | $E = 0.5$          | $E = 1.0$ |
| 0                | 0.707              | 0.707     |
| 1                | 0.9142             | 0.5860    |
| 2                | 0.9926             | 0.4852    |
| 3                | 0.9999             | 0.4996    |
| 4                | 1.0000             | 0.5000    |

another occasion may be required to receive a 1 V signal from a nearby transmitter. Since both signals should produce the same audio output level, an adjustment range of more than 110 dB may be required. The problem is made more difficult because most of the amplifier stages in the receiver, and certainly the A/D converter, often have a dynamic range less than the total range of signal strength variations which must be accommodated by the receiver. It is, therefore, customary to turn down the gain in various parts of the receiver rather than at a single point. Thus, for a fairly weak signal, the gain is decreased near the A/D converter end of the receiver. Maximum gain is retained at the receiver front end and IF so the best overall noise figure is maintained.

For somewhat stronger signals, the gain may also be decreased in some of the intermediate stages as well as the A/D. This prevents overload at any point in the receiver that would cause distortion. Finally, for very strong signals, the gain of the receiver front end is decreased, in addition to the gain in the intermediate and final stages.

The AGC analysis is made here assuming that the gain is controlled at a single point. The designer should note, however, that the amount of turndown, in practice, must be distributed and applied to both the analog gain stages and to the digital path. As will be seen in the feedback algorithm, to be described, part of the gain turn down, in decibels, can be output to a D/A converter and applied to the analog amplifiers.

A block diagram of an AGC regulating circuit is shown in Fig. 6.55. Here, the incoming signal  $x(n)$  is scaled by multiplication by the gain factor  $M(n)$ . The output  $y(n)$  is envelope detected as shown, and the log of the envelope is compared to the desired reference,  $R$ . An error signal,  $\epsilon(n)$ , is then generated and processed to determine the multiplier,  $M(n)$ . If the envelope is too large, the multiplier is reduced; if the envelope is too small, the multiplier is increased.

The performance of the algorithm can be derived in a straightforward manner. For the analysis, we let

$x(n)$  = values of  $x$  at the sampling instants

$E_x(n)$  = values of the envelop of the input

$E_y(n)$  = envelop of the output  $y(n)$

$E_{yL}(n)$  = log of  $E_y(n)$

Clearly,  $E_y(n) = M(n)E_x(n)$  (6.160)

Taking the log of both sides gives

$$\log E_y(n) = \log M(n) + \log E_x(n) \quad (6.161)$$

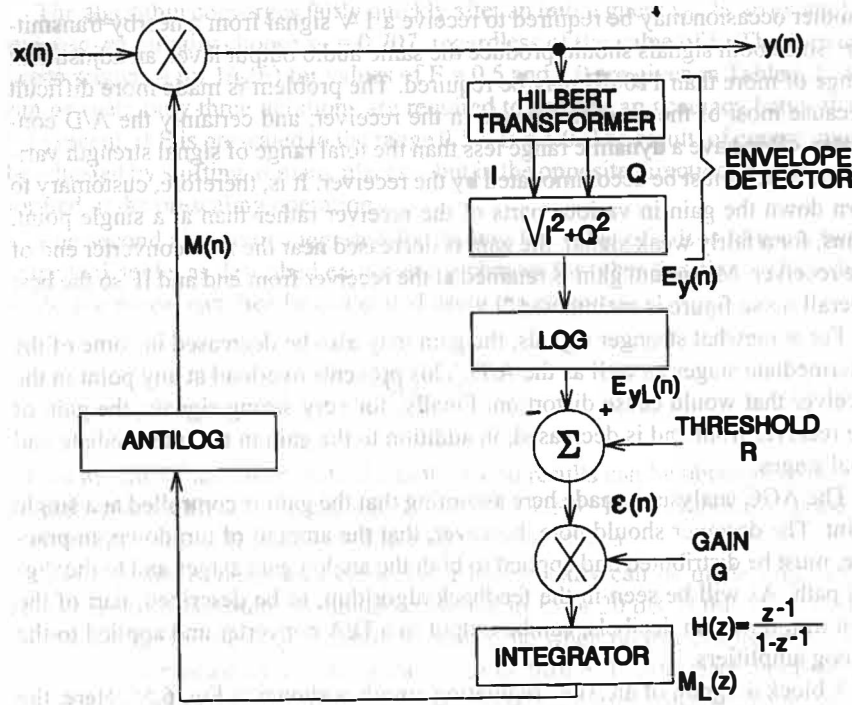


FIGURE 6.55 Block diagram of AGC regulator configuration

Writing this using the notation defined above,

$$E_{yL}(n) = M_L(n) + E_{xL}(n) \quad (6.162)$$

Taking the z-transform, we have

$$E_{yL}(z) = M_L(z) + E_{xL}(z) \quad (6.163)$$

Now, referring to Fig. 6.55, we may write

$$M_L(z) = [R(z) - E_{yL}(z)] G \left( \frac{z^{-1}}{1 - z^{-1}} \right) \quad (6.164)$$

where

$R(z)$  = the z-transform of the reference level

Substituting this into the previous equation gives

$$E_{yL}(z) = Gz^{-1} \left[ \frac{R(z) - E_{yL}(z)}{1 - z^{-1}} \right] + E_{xL}(z) \quad (6.165)$$

Factoring out the term  $E_{yL}(z)$  gives

$$E_{yL}(z) \left[ 1 + \frac{Gz^{-1}}{1 - z^{-1}} \right] = \frac{Gz^{-1}R(z)}{1 - z^{-1}} + E_{xL}(z) \quad (6.166)$$

Finally, solving for  $E_{yL}(z)$ , one obtains

$$E_{yL}(z) = \frac{Gz^{-1}R(z)}{1 + (G-1)z^{-1}} + \frac{E_{xL}(z)(1 - z^{-1})}{1 + (G-1)z^{-1}} \quad (6.167)$$

We now evaluate the response to a unit step function. This corresponds to the case when a signal suddenly appears due to the keying of a transmitter. To simplify the analysis, we also assume that the threshold,  $R$ , is a step function at  $t = 0$ . Then,

$$R(n) = Ru(n)$$

and

$$E_{xL}(n) = u(n)$$

Taking the z-transforms gives

$$R(z) = \frac{R}{1 - z^{-1}}$$

$$E_{xL}(z) = \frac{1}{1 - z^{-1}}$$

Substituting these into Eq. (6.167) gives

$$E_{yL}(z) = \frac{GRz^{-1}}{[1 + (G-1)z^{-1}][1 - z^{-1}]} + \frac{1}{1 + (G-1)z^{-1}} \quad (6.168)$$

$$E_{yL}(z) = \frac{1 + (GR - 1)z^{-1}}{[1 + (G - 1)z^{-1}][1 - z^{-1}]} \quad (6.169)$$

Using partial fraction expansion,

$$E_{yL}(z) = \frac{1 - R}{1 + (G - 1)z^{-1}} + \frac{R}{1 - z^{-1}} \quad (6.170)$$

The inverse z-transform may now be written as

$$E_{yL}(n) = (1 - R)(1 - G)^n + R \quad (6.171)$$

The initial value of the output envelope is  $E_{yL}(0) = 1$ , and the final value is

$$E_{yL}(\infty) = R$$

If we let

$$e^{-\frac{nt}{t_c}} = (1 - G)^n$$

we see that the time constant for the AGC response is given by

$$t_c = \frac{-T_s}{\ln(1 - G)} \quad (6.172)$$

where

$T_s$  = the sampling time

The closed-loop AGC has several advantages over the open-loop system described in connection with the compressor. Perhaps one of the most important is that the multiplier is available in log form as  $M_L(n)$ . Since many analog control circuits tend to have a logarithmic control function, a portion of  $M_L(n)$  can be output to the analog amplifiers to avoid saturation. It should be noted, however, that if an analog control point is selected before narrowband filters, the possibility of oscillations exists for very short time constants, and a compensating delay may have to be added.

A major disadvantage of the algorithm is, of course, that logs and antilogs must be calculated. In many applications, a reasonable size PROM can be used for this.

If base 2 logarithms are used, prescaling to the nearest power of 2 can be used to limit the size of the PROM.

## SQUELCH CIRCUITS

Many receivers used for general communications employ a squelch circuit to suppress the output noise when no signal is being received. Basically, the task of the squelch circuit is to determine when a signal of interest is present at the receiver. It is then a simple task to cut off the audio gain. Many different techniques have been tried to make the signal determination. Indeed, scores of patents have been issued for various techniques.

One of the oldest techniques, and one which is still frequently used, is to detect the signal level by setting a threshold on the AGC control voltage. The threshold is often adjustable by a control accessible to the operator. This circuit works well for AM modulation, except that the threshold tends to change as the receiver amplifier gain changes due to time and temperature variations.

It is beyond the scope of this book to discuss all (or even most) of the squelch techniques that have been used, and only a few will be described in detail. One technique that works effectively is to transmit a pilot tone with the desired signal, often in the region around 150 Hz. The squelch opens when tone's presence is detected. Since the tone is outside the normal voice band, it is filtered out of the signal and is unnoticed by the user. Obviously, different tone frequencies (or even combinations of tones) can be used to selectively open the receiver when the desired transmission is received. Since the system requires coordination between the receiver and the transmitter, it is unsatisfactory for a general coverage receiver.

Another type of squelch that can be used, particularly for FM, is to include an out-of-band noise detector. When a signal is present, even the out-of-band noise is quieted and can be used for the squelch. This system requires a fairly large bandwidth, since out-of-band noise in the 30 to 50 kHz range is sometimes used. Consequently, an analog implementation may be considered.

Another proposed squelch technique is to use the number of zero crossings per unit time in the detected signal to determine when a signal is present. Normally, in a voice signal, the number of zero crossings is less than that for noise—perhaps in the region below 500 per second. Unfortunately, this squelch is vulnerable to certain kinds of interference and may not work effectively by itself. Digital signal processing does, however, make it reasonable to use several conditions for the squelch decision.

A technique that has proven to be quite effective for single-sideband systems is to compare the energy in the lower part of the audio band with that in the upper part. When a voice signal is present, the energy will be concentrated in the lower part of the spectrum, while for noise alone, the energy is more evenly divided. A block diagram of this squelch is shown in Fig. 6.56. The LPF is designed to have

reduce the complexity of the main filter. In this case, the nearest integer divisible into 18 is 9.

Since M1 does not contain a factor of two, all the filter coefficients are required in two sets, and the program must alternate between them on alternate output samples. For this reason, it may still be reasonable to decimate by six rather than nine in the first stage. This does not result in a great increase in the computations required. It is interesting to compare the results of the two-stage decimation with a single filter followed by a decimation of 18. In this case, the filter parameters are

$$\delta_1 = \frac{10^{\frac{1}{20}} - 1}{10^{\frac{1}{20}} + 1} = 0.0575$$

$$\delta_2 = 10^{-4}$$

$$f_T = 1.2 \text{ kHz}$$

$$f_s = 86.4 \text{ ks/s}$$

This requires approximately 194 taps. The resulting computation rates, in terms of multiples and adds per second, are shown in Table 7.1 (if we do not take advantage of the fact that every other input sample is zero) and in Table 7.2 (if we use this simplification).

There are other advantages to two-stage decimation that may be important in certain cases. For example, the storage requirements are generally lower. There may be other instances where two-stage decimation is of value in partitioning the

**TABLE 7.1 Comparison of Computation Rate for Two-Stage and Single-Stage Decimation with Random Inputs to Filter Chain**

| Decimation |    | Taps in Filter |             | K Multiples/Second |       |       |
|------------|----|----------------|-------------|--------------------|-------|-------|
| M1         | M2 | Dec. Filter    | Main Filter | Dec.               | Main  | Total |
| 6          | 3  | 25             | 36          | 360                | 172.8 | 532.8 |
| 1          | 18 | 0              | 194         | 0                  | 931.2 | 931.2 |

**TABLE 7.2 Comparison of Computation Rate for Two-Stage and Single-Stage Decimation with Every Other Input to Filter System Zero**

| Decimation |    | Taps in Filter |             | K Multiples/Second |       |       |
|------------|----|----------------|-------------|--------------------|-------|-------|
| M1         | M2 | Dec. Filter    | Main Filter | Dec.               | Main  | Total |
| 9          | 2  | 43             | 25          | 206.4              | 120.0 | 326.4 |
| 1          | 18 | 0              | 194         | 0.0                | 465.6 | 465.6 |

workload between two processors. It is generally somewhat awkward to use two processors to perform as a single filter if one processor cannot handle the whole load. It becomes necessary to pass partial sums as well as data values between processors. An alternative may be to use a decimation filter executed in one processor, and a smaller main filter executed in the second processor.

### AGC Circuit

An AGC circuit similar to the system shown in Fig. 6.55 can be used to regulate the output amplitude of the receiver. Since the I and Q channels are already available in the receiver, the Hilbert transformer is not required. It is necessary, however, to split the gain reduction between the analog and the digital portions of the receiver. To see more clearly how this is accomplished, Table 7.3 gives the desired analog and digital gains as a function of the input signal values. It is assumed here that the desired output signal has an envelope value of 0.5. For fractional two-complement arithmetic, this gives a headroom of  $20 \log(1/0.5) = 6 \text{ dB}$ . Depending on the nature of the application and the type of signal being received, additional headroom may be desirable. In this example we will, however, use 6 dB. It is also assumed here for simplicity that the analog gain is reduced by attenuation at the antenna. In reality, this would not be done. The initial analog attenuation would be added at the last analog IF. For large signals, this would result in a better S/N ratio than shown in Table 7.3. This is important in a receiver used for analog signals so that a better ultimate S/N ratio results. With a digital receiver, an ultimate S/N ratio better than the 27 dB achieved here is of no particular benefit since the bit error rate is already near zero.

We have also assumed, for simplicity, that the first 20 dB of AGC turn-down is accomplished digitally, followed by analog gain reduction. This results in a decrease in the A/D converter headroom for a larger than minimum desired signal. If this characteristic is to be maximized, the initial AGC turn-down can be applied to the latter stages of the analog circuitry.

Using the AGC system developed in Fig. 6.55, the resulting AGC circuit is shown in Fig. 7.14. The threshold value  $R = \log_{10}(\text{desired envelope value})$  or, if base-two logarithms are used,  $R$  obviously becomes  $\log_2$  of the desired envelope.

**TABLE 7.3 Gain Distribution**

| Input Signal Level (dBW)    | Analog Gain (dB) | Digital Gain (dB) | S/N in 2.4 kHz Bandwidth (dB) | Headroom (dB) |
|-----------------------------|------------------|-------------------|-------------------------------|---------------|
| -155 (0.125 $\mu\text{V}$ ) | 63.1             | 65.9              | 7.2                           | 80            |
| -135                        | 63.1             | 45.9              | 27.2                          | 60            |
| -115                        | 43.1             | 45.9              | 27.2                          | 60            |
| -79.9                       | 8.0              | 45.9              | 27.2                          | 60            |
| -20.0                       | 8.0              | -14.0             | 27.2                          | 0             |

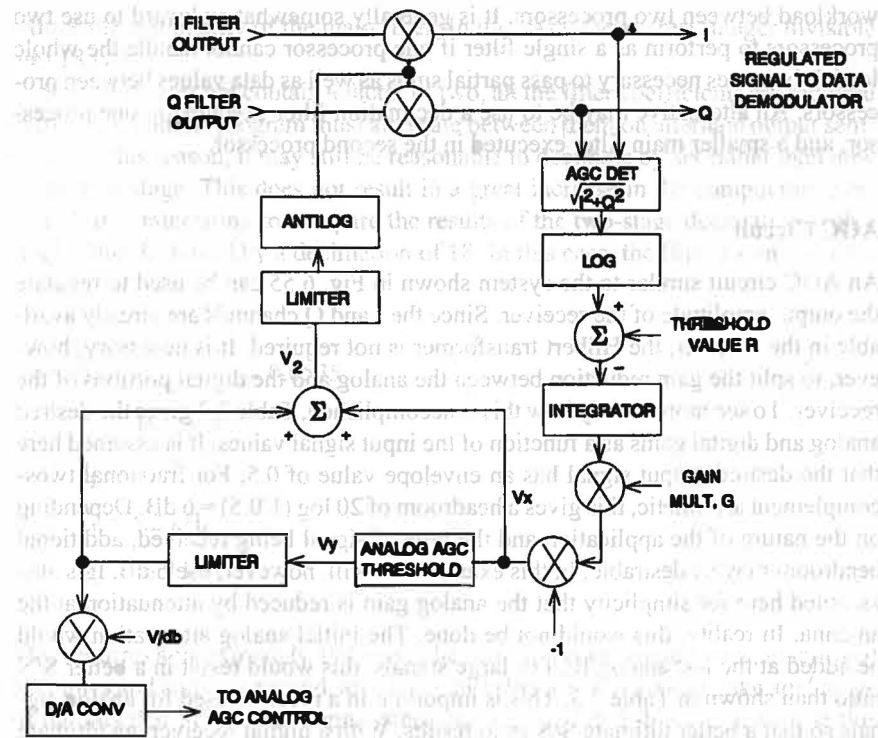


FIGURE 7.14 Block diagram of AGC circuit

The required gain of the circuit is found from the desired time constant using the relationship

$$G = 1 - e^{-\frac{T_s}{TC}} \quad (7.47)$$

where

$$T_s = \text{sample time [see Eq. (6.172)]}$$

For the data receiver, an attack time constant in the order of 20 to 50 ms may be appropriate, with a decay time constant around 1 s. For the present design, for an attack time  $TC = 50$  ms and sample time  $T_s = 1/4800 = 2.083 \times 10^{-4}$ , we have

$$G = 1 - \exp\left(\frac{-2.083 \times 10^{-4}}{50 \times 10^{-3}}\right) = 0.004157$$

For the decay, when the envelop is decreasing,  $G = 0.0002083$ .

We will now examine the analog vs. digital AGC voltage split. Using Table 7.3 as a basis, the desired analog gain as a function of input signal level is plotted in Fig. 7.15a. The corresponding digital gain is shown in Fig. 7.15b. Now consider the block labeled "analog AGC threshold" in Fig. 7.14. Basically, this block is an open circuit until  $V_x$  decreases to the point where the digital gain is 46 dB. For voltage less than this value, the AGC threshold block outputs a voltage,  $V_y = TH - V_x$ , for positive control voltage, to the D/A converter. The limiter in the path to the D/A converter does nothing until the analog circuit is producing maximum attenuation. The analog voltage  $V_y$  is added to  $V_x$  to produce the digital gain factor given by  $V_2 = V_x + [TH - V_x] = TH$ . The digital gain then holds constant at the threshold value until the analog limiter saturates. At that point, the digital gain again decreases for further increases in the input signal level.

The description of the AGC circuit covers the basic principles of operation. It should be noted, however, that AGC circuits in a modern receiver may incorporate

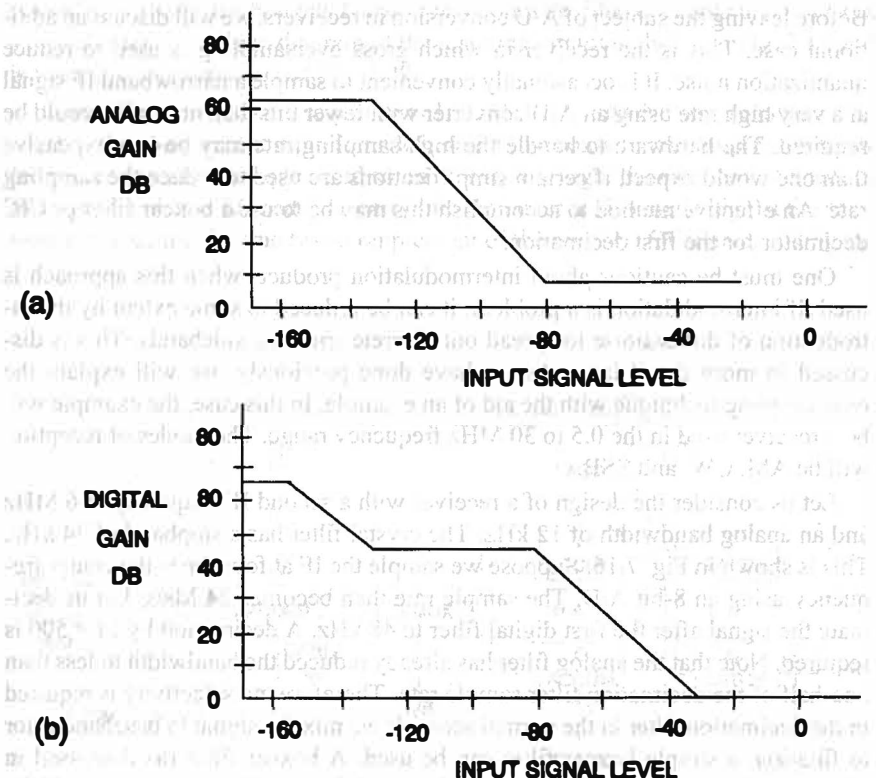


FIGURE 7.15 (a) Analog gain versus input signal level and (b) digital gain versus input signal level

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additional features such as different attack and decay time constants, hang timers, crowbars, and so on. As the attack time is made shorter, delays through the filters must also be dealt with or instability may result. The control afforded by an AGC circuit may be quite good, and the output can be held constant within 1 dB over a large signal input range.

This completes the design of the receiver specified at the onset of this chapter. Many of the principles involved in the design of an actual receiver have been illustrated. Several analytic relationships have also been derived or presented, such as the noise figure of the receiver, the noise figure of the A/D converter, and the optimum decimation ratios. The design of the data demodulator will be covered in connection with data transmission in Chapter 8. We will now proceed to an examination of the characteristics of some different receivers and a radio exciter.

### NARROWBAND RECEIVERS WITH HIGH-SPEED A/D CONVERTERS

Before leaving the subject of A/D conversion in receivers, we will discuss an additional case. This is the receiver in which gross oversampling is used to reduce quantization noise. It is occasionally convenient to sample a narrowband IF signal at a very high rate using an A/D converter with fewer bits than normally would be required. The hardware to handle the high sampling rate may be less expensive than one would expect, if certain simplifications are used to reduce the sampling rate. An effective method to accomplish this may be to use a boxcar filter or CIC decimator for the first decimation.

One must be cautious about intermodulation products when this approach is used. If intermodulation is a problem, it can be reduced to some extent by the introduction of dither noise to spread out discrete spurious sidebands. This is discussed in more detail later. As we have done previously, we will explain the oversampling technique with the aid of an example. In this case, the example will be a receiver used in the 0.5 to 30 MHz frequency range. The modes of reception will be AM, CW, and SSB.

Let us consider the design of a receiver with a second IF frequency at 6 MHz and an analog bandwidth of 12 kHz. The crystal filter has a stopband of 24 kHz. This is shown in Fig. 7.16. Suppose we sample the IF at four times the center frequency using an 8-bit A/D. The sample rate then becomes 24 Ms/s. Let us decimate the signal after the first digital filter to 48 kHz. A decimation by  $M = 500$  is required. Note that the analog filter has already reduced the bandwidth to less than one-half of the decimation filter sample rate. Therefore, no selectivity is required in the decimation filter in the normal sense. If we mix the signal to baseband prior to filtering, a simple boxcar filter can be used. A boxcar filter (as discussed in Chapter 5) is an FIR filter in which all the multiplier coefficients are unity. If the filter is followed by a decimation of the same factor as the number of taps (e.g.,

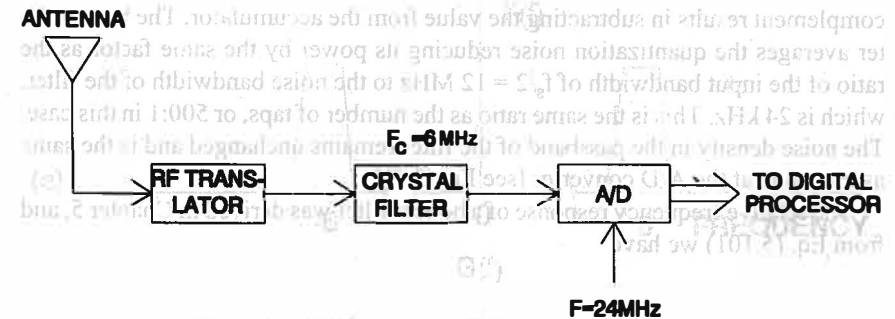


FIGURE 7.16 Block diagram of receiver with high-speed sampler

N), then each output point is the average of the previous N input points, scaled by a factor N. If the IF center frequency is one-fourth the sample rate, as we have discussed previously, the baseband mixers preceding the filters become inverters and a demultiplexer. A block diagram of the resulting circuit is shown in Fig. 7.17 and is basically an expression of Fig. 5.29.

Since the cosine mixing sequence is 1, 0, -1, 0, ..., and the sine sequence is 0, -1, 0, 1, the complement input is made high for two consecutive samples, then low for two consecutive samples, and so on. When it is high, the ones complement of the input number is formed. The carry into the adder is also made high at the sample time, forming the true two's complement of the number. Of course, adding the

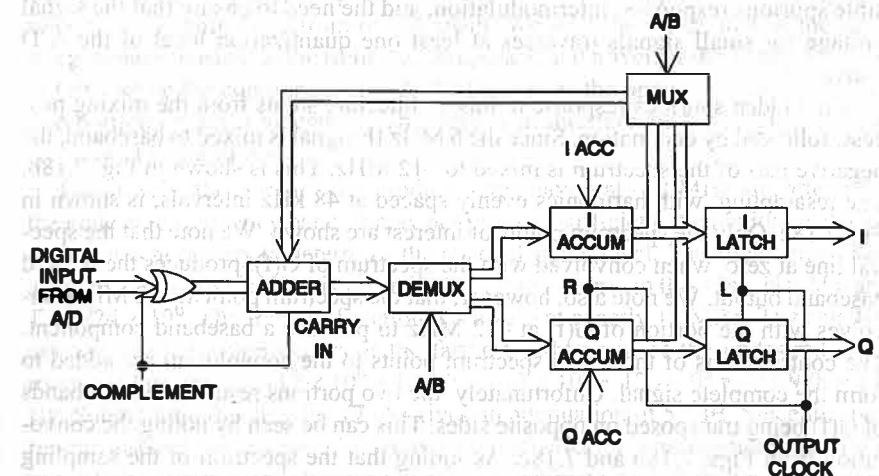


FIGURE 7.17 Block diagram of dual box filter