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Application Number	
Filing Date	
First Named Inventor	Yannis Tsividis
Title	Power Dissipation Reduction in Wireless Transceivers
Art Unit	
Examiner Name	
Attorney Docket Number	10037P007CCC

SIGNATURE of Applicant or Patent Practitioner

Signature	/RWB/	Date (Optional)	11/28/2017
Name	Roger W. Blakely, Jr.	Registration Number	25,831
Title (if Applicant is a juristic entity)			
Applicant Name (if Applicant is a juristic entity)			

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I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

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Name	Demetrios Papageorgiou		
Title	CEO, Theta IP, LLC		

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☒ Declaration Submitted with Initial Filing **OR** ☐ Declaration Submitted after Initial Filing (surcharge (37 CFR 1.16(f)) required)	**Attorney Docket Number**	10037P007CC
	First Named Inventor	Yannis Tsividis
	COMPLETE IF KNOWN	
	Application Number	
	Filing Date	
	Art Unit	
	Examiner Name	

Power Dissipation Reduction in Wireless Transceivers

(Title of the Invention)

As a below named inventor, I hereby declare that:

This declaration is directed to:

☒ The attached application,

OR

☐ United States Application Number or PCT International Application Number _____

filed on _____

The above-identified application was made or authorized to be made by me.

I believe I am the original inventor or an original joint inventor of a claimed invention in the application.

I have reviewed and understand the contents of the above-identified application, including the claim(s).

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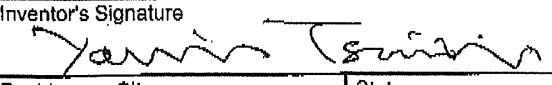
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Legal Name of Sole or First Inventor:

(*E.g.*, Given Name (first and middle (if any)) and Family Name or Surname)

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POWER DISSIPATION REDUCTION IN WIRELESS TRANSCEIVERS

ABSTRACT OF THE DISCLOSURE

Methods and circuits for reducing power dissipation in wireless transceivers and other electronic circuits and systems. Embodiments of the present invention use bias current reduction, impedance scaling, and gain changes either separately or in combination to reduce power dissipation. For example, bias currents are reduced in response to a need for reduced signal handling capability, impedances are scaled thus reducing required drive and other bias currents in response to a strong received signal, or gain is increased and impedances are scaled in response to a low received signal in the presence of no or weak interfering signals.

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CLAIMS

What is claimed is:

1. A method of controlling a battery power consumption of a transceiver apparatus, by controlling a power dissipation of a receiver of the transceiver apparatus when the receiver is receiving an input signal in a receiver signal path that includes a desired signal and an interferer signal, the method comprising:

determining at a first node of the receiver signal path a strength of the input signal;

filtering the desired signal and the interferer signal by a filter after the first node of the receiver signal path to reduce the interferer signal relative to the desired signal;

determining at a second node in the receiver signal path, after the filter, a signal strength that substantially represents the desired signal, with the interferer signal as reduced by filtering from the input signal;

performing a comparison where the signal strength at the first node is compared with the signal strength at the second node; and

as the comparison changes, changing a dynamic range and a noise floor of the receiver signal path by dynamically adjusting one or more of a bias current, an impedance, or a gain, in the receiver to control the power dissipation of the receiver of the transceiver apparatus and thereby control the battery power consumption of the transceiver apparatus.

2. The method of claim 1 wherein dynamically adjusting any one or more of the bias current, the impedance, or the gain, in the component in the receiver signal path occurs while the receiver is receiving the input signal.

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3. A method for power dissipation reduction in a wireless receiver of a transceiver of a battery powered wireless device and a corresponding improvement in a drain on battery life of the battery powered wireless device, the method comprising:

receiving a wireless input signal having a desired signal and an interferer signal, by the wireless receiver of the transceiver of the battery powered wireless device, the wireless receiver having a receiver signal path comprising a plurality of circuits, wherein the plurality of circuits comprise: an amplifier, a filter, and a mixer; wherein the receiver signal path of the wireless receiver is coupled to a circuit for determining a signal strength of a first signal at a first node in the receiver signal path;

determining the signal strength of the first signal at the first node in the receiver signal path;

dynamically adjusting a bias of a circuit in the receiver signal path of the wireless receiver responsive to the determined signal strength of the first signal; and

wherein the determined signal strength of the first signal is responsive to the signal strength of the interferer signal; and

wherein the bias of the circuit is dynamically adjusted as the determined signal strength of the first signal varies;

wherein adjusting one or more of a bias current, an impedance, or a gain of the circuit resulting in the optimization of the power dissipation of the wireless receiver; and

wherein the dynamically adjusting of the bias occurs while the wireless input signal is in the receiver signal path of the wireless receiver.

4. The method of claim 3, wherein the determined signal strength of the first signal also includes the signal strength of the desired signal.

5. The method of claim 3, further comprising using the determined signal strength of the first signal to determine a ratio of the strength of the interferer signal with respect to the

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wireless input signal, and wherein the bias of the circuit in the receiver signal path of the wireless receiver is dynamically adjusted responsive to the determined ratio.

6. The method of claim 3, further comprising using the determined signal strength of the first signal to determine a ratio of the strength of the interferer signal with respect to the desired signal, and wherein the bias of the circuit in the receiver signal path of the receiver is dynamically adjusted responsive to the determined ratio.

7. The method of claim 3, wherein the circuit in the receiver signal path whose bias is dynamically adjusted is the amplifier.

8. The method of claim 3, wherein the circuit in the receiver signal path whose bias is dynamically adjusted is the mixer.

9. The method of claim 3, wherein the circuit in the receiver signal path whose bias is dynamically adjusted is the filter.

10. The method of claim 3, wherein dynamically adjusting the bias comprises dynamically adjusting a bias current of the circuit by dynamically adjusting an impedance in a bias circuit providing the bias current to the circuit in the receiver signal path.

11. The method of claim 10 wherein the impedance in the bias circuit providing bias current to the circuit in the receiver signal path is a resistance.

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12. The method of claim 3, wherein dynamically adjusting the bias comprises reducing a bias current of the circuit in the receiver signal path by switching an impedance that appears across a voltage, thereby changing the bias current.

13. A method for power dissipation reduction in a receiver of a transceiver of a portable wireless device and a corresponding improvement in a drain on battery life of the portable wireless device, the method comprising:

receiving a wireless input signal having a desired signal and an interferer signal by the receiver of the transceiver of the portable wireless device, the receiver having a receiver signal path comprising a plurality of circuits, wherein the plurality of circuits include an amplifier, a filter, and a mixer, wherein the receiver signal path of the receiver is coupled to a circuit for determining a signal strength of a first signal at a first node in the receiver signal path;

dynamically adjusting an impedance of a circuit in the receiver signal path of the receiver responsive to the signal strength of the first signal;

wherein the signal strength of the first signal is responsive to the signal strength of the interferer signal;

wherein the impedance of the circuit is dynamically adjusted as the determined signal strength of the first signal varies; and

wherein the dynamically adjusting of the impedance occurs while the receiver is receiving the wireless input signal.

14. The method of claim 13, wherein the signal strength of the first signal also includes the signal strength of the desired signal.

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15. The method of claim 13, further comprising using the signal strength of the first signal to determine a ratio of the strength of the interferer signal with respect to the wireless input signal, and wherein the impedance in the circuit in the receiver signal path of the receiver is dynamically adjusted responsive to the determined ratio.

16. The method of claim 13, wherein the first signal strength is used to determine a ratio of the strength of the interferer signal with respect to the desired signal, and wherein the impedance of the circuit in the receiver signal path of the receiver is dynamically adjusted responsive to the determined ratio.

17. The method of claim 13, wherein the circuit in the receiver signal path of the receiver whose impedance is dynamically adjusted is the amplifier.

18. The method of claim 13, wherein the circuit in the receiver signal path of the receiver whose impedance is dynamically adjusted is the mixer.

19. The method of claim 13, wherein the circuit in the receiver signal path of the receiver whose impedance is dynamically adjusted is the filter.

20. The method of claim 13, wherein dynamically adjusting the impedance of the circuit in the receiver signal path of the receiver is affected by switching in and out of the circuit in the receiver signal path, the impedance in series with a load in response to the signal strength of the first signal.

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POWER DISSIPATION REDUCTION IN WIRELESS TRANSCEIVERS

CROSS-REFERENCES TO RELATED APPLICATIONS

[0001] This application is a continuation of U.S. Patent Application No. 15/080,421, filed March 24, 2016, which is a continuation of U.S. Patent Application No. 11/318,646, filed December 27, 2005, which is a continuation of U.S. Patent Application Number 10/784,613, filed February 23, 2004, which claims the benefit of United States provisional application number 60/451,229, filed March 1, 2003, which is incorporated by reference.

[0002] This application claims the benefit of United States provisional application number 60/451,230, filed March 1, 2003, which is incorporated by reference.

BACKGROUND

[0003] The present invention relates to power dissipation reduction techniques for electronic circuits, for example wireless transceiver integrated circuits.

[0004] Wireless networking is quickly becoming ubiquitous, as desktop, notebook, and handheld computers are connected to share Internet access and files. Wireless networking cards compatible with PCMCIA and compact flash form factors are popular for laptops and handhelds respectively, particularly as mobile users connect to the Internet on the road at coffee shops, hotels, and airports.

[0005] A downside of this connectivity is a corresponding drain on battery life, especially for these portable devices. The power consumed by a wireless transmitter and receiver reduces the usefulness of a device and sends a user on a hunt for an electrical outlet for recharging.

[0006] One reason why this power drain is high is that electronic circuits are typically designed to function properly under worst-case operating conditions. For a wireless transceiver, the worst case condition is when a desired signal reception strength is low, while other transceivers or nearby electronic equipment generate interfering signals and other spurious noise.

[0007] But a wireless transceiver does not always operate in these worst-case conditions. For example, a base station, router or access point may be nearby such that the received signal is strong. Also, there may be no interfering signals, or they may be relatively weak. In these situations, receiver circuit currents can be reduced below what is necessary for the worst case condition. If this is done, power dissipation is reduced, and battery life is increased.

[0008] Thus, what is needed are circuits and methods that can adapt to a better-than-worst-case condition and reduce circuit currents and therefore power dissipation accordingly.

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SUMMARY

[0009] Accordingly, embodiments of the present invention provide methods and circuits for reducing power dissipation in wireless transceivers and other electronic circuits and systems. Embodiments of the present invention use bias current reduction, impedance scaling, gain, and other dynamic changes either separately or in combination to reduce power dissipation in response to better-than-worst case conditions. For example, bias currents are reduced in response to a need for reduced signal handling capability, impedances are scaled thus reducing required drive and other bias currents in response to a strong received signal, or gain is varied and impedances are scaled in response to a low received signal in the presence of no or weak interfering signals. Alternately, currents may start low and be increased in response to worse-than-best-case conditions, or they may start at a point in between and vary up or down. These variations may be made to electronic systems generally, and are particularly suited and discussed below in the context of a wireless transceiver that may be used in networking devices, cellular telephones, and other wireless systems.

[0010] An exemplary embodiment of the present invention provides a method of receiving a signal using an integrated circuit. The integrated circuit includes a signal path having a low-noise amplifier configured to receive the signal, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer. The method itself includes determining a first signal strength at a first node in the signal path in the integrated circuit and dynamically changing an impedance of a component in the signal path based on the first signal strength.

[0011] A further exemplary embodiment of the present invention provides a method of receiving a signal using an integrated circuit. The integrated circuit includes a signal path having a low-noise amplifier configured to receive the signal, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer. The method itself includes determining a first signal strength at a first node in the signal path in the integrated circuit and dynamically changing a bias current in the signal path based on the first signal strength.

[0012] Another exemplary embodiment of the present invention provides a method of receiving a signal using an integrated circuit. The integrated circuit includes a signal path having

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a first circuit and a second circuit having an input coupled to an output of the first circuit. The method itself includes determining a first signal strength at a first node in the signal path in the integrated circuit. The first node is before the first circuit in the signal path. The method further includes dynamically changing a gain of the first circuit based on the first signal strength and dynamically changing an impedance of a component in the second circuit based on the first signal strength.

[0013] Still a further exemplary embodiment of the present invention provides a wireless transceiver integrated circuit including a receiver having a signal path, the signal path including a low-noise amplifier, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer, as well as a first signal strength indicator circuit coupled to the signal path and configured to determine a first signal strength. An impedance in the signal path is configured to be dynamically adjusted in response to the first signal strength.

[0014] Yet a further exemplary embodiment of the present invention provides a wireless transceiver integrated circuit. This integrated circuit includes a receiver comprising a signal path, the signal path having a low-noise amplifier, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer, as well as a first signal strength indicator circuit coupled to the signal path, and configured to determine a first signal strength. A bias current in the signal path is configured to be dynamically adjusted in response to the first signal strength.

[0015] Another exemplary embodiment of the present invention provides a wireless transceiver integrated circuit. This circuit includes a receiver comprising a signal path, the signal path having a first circuit; and a second circuit having an input coupled to an output of the first circuit; as well as a first signal strength indicator circuit coupled to the signal path, and configured to determine a first signal strength. A gain of the first circuit is configured to be dynamically adjusted in response to the first signal strength, and an impedance in the second circuit is configured to be dynamically adjusted in response to the first signal strength.

[0016] A better understanding of the nature and advantages of the present invention may be gained with reference to the following detailed description and the accompanying drawings.

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BRIEF DESCRIPTION OF THE DRAWINGS

[0017] Figure 1 is a block diagram of a wireless transceiver that may benefit by incorporation of embodiments of the present invention;

[0018] Figures 2A and 2B illustrate examples of desired and interfering signals and noise that may be received by a circuit in a wireless receiver;

[0019] Figure 3 illustrates what can occur as a maximum signal handling capability is reduced in the worst-case signal condition;

[0020] Figure 4 illustrates a portion of a receiver consistent with an embodiment of the present invention;

[0021] Figure 5 illustrates the relationship between a required bias current and a given output signal for a representative circuit;

[0022] Figure 6 is an example of how a circuit's impedances may be scaled to reduce drive currents, and depending on the circuit configuration used, to reduce associated bias currents as well;

[0023] Figure 7 illustrates how gain may be inserted in a signal path to improve a circuit's signal to noise ratio;

[0024] Figures 8A-8D illustrate some of the possible power saving techniques that may be used when received desired and interferer signals are all at a low power level;

[0025] Figures 9A-9C illustrate one of the possible power saving techniques that may be used when a received desired signal is strong while all interfering signals are at a low power level;

[0026] Figures 10A-10C illustrate one of the possible power saving techniques that may be used when received desired and interferer signals are all at a high power level;

[0027] Figures 11A-11D illustrate one of the possible power saving techniques that may be used when a received desired signal is weak while one or more interfering signals are strong;

[0028] Figure 12 is a summary illustrating four different input conditions and some of the appropriate power-saving changes that may be made in response to those conditions;

[0029] Figure 13 shows how power may be saved as a function of time by employing one or more of the power saving methods consistent with embodiments of the present invention;

[0030] Figure 14 is a block diagram of a portion of a receiver consistent with an embodiment of the present invention; and

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[0031] Figure 15 is a block diagram of a portion of a transmitter consistent with an embodiment of the present invention.

DESCRIPTION OF EXEMPLARY EMBODIMENTS

[0032] Figure 1 is a block diagram of a wireless transceiver that may benefit by incorporation of embodiments of the present invention. This wireless transceiver may be designed to send and receive signals consistent with the IEEE 802.11a, 802.11b, 802.11g, or other signaling standard or combination of standards. This figure, as with all the included figures, is shown for illustrative purposes only and does not to limit either the possible embodiments of the present invention or the claims.

[0033] There are three main portions of this transceiver circuit, a receiver, transmitter, and synthesizer. This transceiver may be completely or partially integrated on a semiconductor chip, or it may be integrated onto multiple integrated circuits. In a specific embodiment, the circuitry bounded by dashed line 100 is integrated on a single chip coupled to one or more external components or circuits. The integrated circuit or circuits forming this wireless transceiver may incorporate various integrated circuit devices such as a bipolar, CMOS, or BiCMOS devices made using a silicon, silicon-germanium (SiGe), gallium arsenide or other III-V process, or other manufacturing process. Embodiments of the present invention may also be applicable to circuits manufactured using nanotechnology processing.

[0034] The receiver includes a signal path formed by low-noise amplifier 102, I and Q mixers 104 and 106, low pass filters 108 and 110, and baseband amplifiers 114 and 116. Other circuitry in the receiver includes received strength indicator 122, automatic gain control circuit 166, baseband gain control circuit 120, tuning circuit 112, and offset cancellation circuit 118.

[0035] The transmitter includes input up-converter mixers 124 and 126, summing node 176, which may be conceptual rather than an actual circuit, transmit variable gain amplifier 128, and power amplifier 130.

[0036] The synthesizer includes a voltage-controlled oscillator 148, which drives I and Q buffers 154 and 152, prescaler 156, reference clock buffer 142 and divider 158, phase-frequency detector 160, charge pump 162, and loop filter 146, which in a specific embodiment is formed by external components.

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[0037] Signals are received on an antenna, not shown, and typically pass through an RF switch and bandpass filter before being received by the low-noise amplifier 102 on line 101. The low noise amplifier gains the received signal and provides it to quadrature mixers 104 and 106. I and Q mixers 104 and 106 down-convert the received signal to baseband by multiplying them with quadrature versions of the oscillator signal provided by buffers 152 and 154. This down conversion also produces a high frequency component at a frequency that is equal to the sum of the frequencies of the received signal and the VCO. This unwanted signal is filtered by low pass filters 108 and 110, which in turn drive baseband amplifiers 114 and 116. The outputs of baseband amplifiers 114 and 116 are typically converted to digital signals by analog-to-digital converters at the front end of a digital signal processing block.

[0038] In the transmit mode, I and Q versions of the signal to be transmitted are provided on lines 121 and 123 to up-convert mixers 124 and 126. These up-convert mixers multiply the I and Q portions of the transmit signal by quadrature versions of the VCO signal provided by buffers 152 and 154. The outputs of the up-convert mixers 124 and 126 are summed, and amplified by transmit VGA 128, which in turn drives power amplifier 130. The output of power amplifier 130 is typically filtered, and passes through the RF switch to the antenna for transmission.

[0039] A reference clock is received and buffered by the reference buffer 142. The VCO generates quadrature oscillatory signals that are divided by prescaler 156. The reference clock is typically generated by a crystal or other stable periodic clock source. The phase-frequency detector 116 compares the phase or frequency (depending on whether the synthesizer is tracking or acquiring the correct frequency) of the divided VCO signal and the reference clock, or a divided version of the reference clock, and generates an error signal, which drives the charge pump 162. The output signal of the charge pump 162 is filtered by the loop filter 146, which is commonly a lead-lag filter, and which provides a tuning or correction signal to the VCO 148.

[0040] Embodiments of the present invention may be used to reduce the power dissipation of one or more of these included circuits. For example, the power dissipation in the low-noise amplifier 102, down-convert mixers 104 and 106, low pass filters 108 and 110, or baseband amplifiers 114 and 116 may be optimized. Also, power dissipation in up-convert mixers 124 126, variable gain amplifier 128, and power amplifier 130 may also be optimized. Similarly, VCO 148 and prescaler 156 currents may be adjusted. Embodiments of the present invention

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may also be applied in other circuits which may be included in other integrated circuit receivers, transmitters, transceivers, or other electronic circuits or systems.

[0041] When a receiver is actively receiving a desired signal, each block in the signal path has at its input the desired signal as well as noise and possibly interfering signals. The desired signal is the useful, information-carrying portion of a received signal. The noise may be thermal, shot, or other noise generated on the integrated circuit, in addition to received noise generated by sources external to the chip. The noise at the input of a block may be referred to as the equivalent input noise. The interfering signal or signals, or interferers, may be generated by similar transceivers, or other electrical equipment, circuits, or systems.

[0042] Figures 2A and 2B illustrate examples of desired signals, interferers, and noise that may be received by one of the various circuits in a wireless receiver. In each of these figures, the signal strength is plotted along a Y-axis 204 or 254 as a function of frequency along an X-axis 202 or 252. In the example of Figure 2A, a received desired signal 206 is large in comparison to interfering signals 208 and 210. In these examples, two interfering signals are shown for illustrative purposes, though there may be no such signals, one such signal, or more than two such signals in the frequency range of interest. Also, while for these examples the interferers are shown as being at a higher frequency than the desired signal, there may be one or more interferers at higher or lower frequencies as the desired signal. In this specific example, the acceptable noise floor 214 is relatively high, while maximum signal handling capability Smax 212 (that is the maximum signal power that can be handled with an acceptably low distortion) needs only to be high enough to accommodate the desired signal. For this specific example, the circuit receiving this input spectrum only requires a relatively small dynamic range for proper operation, that is the range between Smax 212 and the noise floor 214 is relatively small.

[0043] Conversely, in the example shown in Figure 2B, the desired signal 256 is relatively weak compared to the large interferers 258 and 260. In this example, the noise floor 264 should be relatively low so as to prevent an unacceptable level of error in the recovery the desired signal 256. The maximum signal handling capability Smax 262 should be relatively high to accommodate the large interferers in order to avoid the creation of intermodulation products as described below. Accordingly, in this specific example, the circuit receiving this input spectrum should have a large dynamic range, particularly in comparison to the example of Figure 2A.

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[0044] It should be noted that the noise level or noise floors shown in these and the other included figures is the noise density integrated over the bandwidth of interest. For simplicity and comparison, this level is shown as a horizontal line, and is not meant to imply noise density.

[0045] Often in wireless receivers, a circuit at different times will receive an input spectrum similar to those shown in Figures 2A and 2B. The input spectrum of Figure 2B is generally considered the worst-case input signal, and typical design methodology involves designing a receiver for this condition, specifically the weakest desired signal accompanied by largest interference level. Circuit impedances and currents are set such that the noise floor 264 is sufficiently low for an acceptable bit-error rate, while bias currents are set sufficiently high for the required Smax 262.

[0046] Conversely, the input spectrum in Figure 2A is that of the best-case input signal, specifically, a robust desired signal accompanied by no or low-level interferers. In this case, the noise floor 214 may be allowed to rise, while the maximum signal handling capability Smax 212 may be reduced. When this is done, the receiver circuit may save significant power. For example, the circuit's impedances may be increased, thus reducing required drive currents. Similarly, bias currents may be lowered, thus reducing the maximum signal in handling capability.

[0047] The minimum power dissipation for a circuit is proportional to the required maximum signal-to-noise ratio, which is the ratio between Smax 212 or 262 and N 214 and 264. Thus, a circuit receiving an input similar to the one shown in Figure 2A can dissipate less power than one receiving the input as shown in Figure 2B, while still achieving an acceptable bit-error rate.

[0048] Figure 3 illustrates what can occur when the maximum signal handling capability Smax 314 is reduced in the worst-case condition, that is when a weak desired signal 306 is accompanied by large interferers 310 and 312. Again, signal strength is plotted along a Y-axis 304 as a function of frequency along X-axis 302. In this specific example, Smax 314 is reduced below the peak levels of the interferers 310 and 312. Since Smax is low, the circuit cannot handle the interferers linearly. The resulting nonlinearities lead to a mixing of the interferers and the creation of intermodulation products 308 (for example, a third-order intermodulation distortion, IM3), one of which in this example occurs at the same frequency as the desired signal 306. As can be seen, if the intermodulation products 308 become excessive, the received signal bit error rate may become excessive, and the desired signal 306 may be lost. Accordingly, while

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Smax may be lowered even under some unfavorable conditions in order to reduce power, care should be taken to avoid corruption of the received desired signal.

[0049] Figure 4 illustrates a portion of a receiver consistent with an embodiment of the present invention. Included is a filter 430. An optional gain element 420 is placed in front of the filter 430 in order to increase signal levels. Signal strength indicator circuits 440 and 450 are connected to input line 410 and output line 460. In this specific example, the input signal spectrum on line 410 is shown as desired signal 412 and interferers 414 and 416. The signal spectrum at the output line 460 is shown as desired signal 462 and interferers 464 and 466. The signal strength indicators 440 and 450 do not provide information as to the relative sizes of the desired and interfering signals. Rather, a cumulative signal level is provided at their outputs. For example, the first signal strength indicator 440 outputs a level corresponding to the sum of desired signal 412 and interfering signals 414 and 416, while the second signal strength indicator 450 provides a signal level corresponding to the sum of desired signal 462 and interfering signals 464 and 466. In this specific example, the gain of the gain and filter circuit combinations is shown as approximately one, while the interfering signals 414 and 416 signal levels are reduced.

[0050] A comparison of the signal levels provided by the signal strength indicators 440 and 450 indicates that much of the combined received signal on line 410 has been filtered. Accordingly, it may be deduced that large interfering signals present at the input are being filtered by the filter 430. From this information, as will be shown in greater detail below, the bias, impedance, and gain of the gain stage 420 and filter 430 combination may be optimized to reduce power dissipation.

[0051] There are several real world situations where the received signal is better than the worst-case condition such that power can be saved. For example, large interferers may be present only part of the time, that is, on a temporary or transient basis. The interfering equipment may be some distance from the transceiver, or it may be operating in the low power mode. Also, the desired signal may be very strong as compared to the noise and interferers, for example a hub, router, or access point may be nearby.

[0052] Some transceivers consistent with embodiments of the present invention are designed to work with more than one data transfer specification or standard. In this case, when a transceiver is operating in a mode having a lower data rate, the power saving techniques described here may be employed.

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[0053] Figure 5 illustrates the relationship between a required biased current 516 for a given output signal 514 for a representative circuit 510. If the output signal current level is relatively low, such as the output current shown as 526, the corresponding bias current 528 may be low. Conversely, if the output signal current level is larger as with the example 536, the corresponding bias current level 538 should also be high. Accordingly, if a bias current is initially set high to handle large a large input signal, for example a large interferer, this current may be reduced if the input signal is smaller.

[0054] There are many ways by which these bias currents can be reduced. For example, the current may be generated by placing a voltage across a resistor by applying a bias voltage to the base of a device whose emitter is connected to ground through a resistance. In this case, the resistor may be increased by opening switches across portions of the resistance, or lowering the bias voltage applied at the base. Several ways in which this may be done will be readily understood by one skilled in the art.

[0055] Figure 6 is an example of how a circuit's impedances may be scaled to reduce drive currents, and, depending on the circuit configuration used, associated bias currents as well. A driver 612 has a load R 614 and C 616. The frequency response of this circuit is the same as that seen by driver 622, which drives an impedance of 2R 624 and C/2 626. But the impedance of the load seen by driver 622 is double that seen by 612, thus the output current required by the driver 622 is reduced by one-half.

[0056] As an example, the output stage of each of these drivers may be a Class A emitter follower formed by an emitter follower connected to a current source. When the outputs are driven high, the emitter of driver 622 need supply only one-half the drive current as driver 612. In this way, an impedance can be scaled in order to decrease a circuit's required drive current.

[0057] Also, the discharge current for driver 622 is only one half that of driver 612 for a given negative-going slew rate. Thus, the current source of 622 may be reduced by the same factor of one-half as compared to driver 612. In this example, the bias current, that is the current in the pull-down current source can be reduced. Many other examples where drive currents and possibly bias currents may be reduced will be appreciated by one skilled in the art.

[0058] Figure 7 illustrates another degree of freedom that made be employed to reduce current levels in a transceiver. Specifically, a gain element 720 may be inserted in front of a circuit block 730 in order to improve the combined circuit's signal-to-noise ratio by a factor equal to the

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gain of the inserted gain block. This is particularly useful when large interferers are absent and the desired received signal is moderate or low. Specifically, gain is added to the signal while impedances are increased, which raise the noise floor. In this way, a given signal-to-noise ratio may be maintained while the power is decreased.

[0059] The gain of such an element may be varied by increasing a current in a differential pair or increasing a load resistance using switches. Many other examples where the gain of this element may be varied will be appreciated by one skilled in the art.

[0060] These variables, or degrees of freedom, specifically reducing bias currents, increasing impedances, and increasing gain may be used as in the following examples.

[0061] Figure 8A is a block diagram of a functional block 820 and optional gain element 810 in accordance with an embodiment of the present invention. Functional block 820, like the functional blocks in the following diagrams, may be a filter, mixer, amplifier, or other circuit or circuits in a wireless transceiver or other electronic circuits or system. An input signal is received on line 812 by the optional gain element 814. When the optional gain block 810 is not used, the input signal may be received directly by the function block 820. The gain of the optional gain element 812 is controlled by a gain control signal on line 814. The functional block receives an output signal from the optional gain element 810 and provides an output VOUT on line 822. The lines in this and the other included figures may be one or more lines, depending on whether single-ended, differential, or other type of signaling is employed.

[0062] One or more impedances are under control of signals on impedance control lines 824. Similarly, one or more bias currents in the function block are under control of one or more signals on bias control lines 826. These various control lines may be logic signals, analog signals, voltage or currents lines, or other signal or bias lines. In other embodiments of the present invention, the gain control element 810 may be included in the function block 820. Also, various embodiments may not incorporate either or both the impedance control and bias control.

[0063] Figure 8B is an example input that may be present on line VIN 812. In this example, a desired signal 836 is relatively weak, as are interfering signals 837 and 838. The initial bias and circuit configuration is such that the noise floor 833 and maximum signal handling capability Smax 831 are adjusted for worst case conditions. The circuit of Figure 8A, as with all the circuits described here, receives noise at its input which may be referred to as input equivalent noise or input referred noise. Additionally, the circuit of Figure 8A generates noise which is

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added to the input referred noise. Depending on the gain characteristics of the circuitry, the output noise at various frequencies may be greater than, equal to, or less than the input referred noise. For simplicity, the noise floor and maximum signal handling capability Smax, in this and the other figures, are shown as straight lines, though the noise and Smax are typically curved as a function of frequency.

[0064] That the input spectrum is as shown in Figure 8B can be determined, for example, by low signal strength indications on line VIN 812 and VOUT 822. That is, a low level signal strength indication on line VIN 812 indicates that no portion of the input signal is particularly large.

[0065] For this exemplary input, there are at least two methods by which the power dissipation for this circuitry may be reduced. Depending on the exact circuits and structures used, one of these methods may be preferred.

[0066] In Figure 8C, the bias current is decreased, thereby lowering the maximum signal handling capability 841 as compared to 831, closer to the desired and interfering signal levels. Again, the bias currents in the function block 820 may be reduced by switching impedances that appear across a voltage thereby changing a resulting bias current, by reducing a voltage at the gate of a MOS or base of a bipolar transistor, or by other methods.

[0067] In Figure 8D, a second method of reducing power dissipation in the function block 820 is employed. Specifically, Smax 851 is held constant as compared Smax 831. The desired and interfering signals are amplified such that they are closer to the available signaling handling capability 851. Also, the noise floor 853 is raised as compared to noise floor 833 in Figure 8B. Specifically, the noise contributed by the function block 820 is increased, such that the noise at its output is increased to noise floor 853. This is done by increasing one or more impedance in function block 810, such that drive currents inside that block are reduced. Depending on the exact configuration, this may also allow some biasing currents to be reduced, while maintaining the maximum signal handling capability 851 at a sufficient level. Alternately, these two methods of reducing power dissipation in function block 820 may be done in combination.

[0068] The included examples are explained for the exemplary situation where biasing and other parameters are set for worst-case conditions, and then changed to save power when it is discovered that the conditions are better-than-worst case. Alternately, the bias currents and other

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parameters may be set for maximum power savings, or an intermediate point, and the power can be adjusted from there.

[0069] Figure 9A illustrates a block diagram including an optional gain element 910 and function block 920. Again, an input signal is received on line 912 by optional gain element 910 which in turn drives function block 920. The function block provides an output VOUT on line 922, and receives impedance and bias control signals on lines 924 and 926.

[0070] Figure 9B shows the spectrum for what may be considered a best-case received signal. Specifically, the desired signal 936 is strong, while the interfering signals 937 and 938 are relatively weak. This may be determined, for example, by detecting a large signal level at the input line VIN 812 and a large signal level after a filter, since these readings would indicate that a large signal is received, but that it is at the desired signal frequency.

[0071] The maximum signaling capability 931 and noise floor 933 are shown as being set for the worst case conditions. In this case, the noise floor 933 is lower than the maximum allowed for proper signal reception. Accordingly, one or more impedance in the function block 920 may be increased, such that the noise floor 943 rises as shown in Figure 9C. In this way one or more the driving currents in the function block 920 may be reduced. Similarly, since the drive current is reduced, one or more bias current may also be reduced, depending on the exact circuit configuration.

[0072] Figure 10A illustrates a block diagram showing an optional gain element 1010 driving a function block 1020. An input signal is received by the gain element 1010 on line 1012, and an output is provided by function block 1020 on line VOUT 1022. One or more gain control signals present on lines 1014 control the gain of gain control element 1010, while one or more impedance and bias control signals are received by the function block 1020 on line to 1024 and 1026.

[0073] Figure 10B illustrates a received signal that may be received on line VIN 1012. In this example, the desired signal 1036 and interferers 1037 and 1038 are each relatively large. This may be determined, for example, by detecting a large signal level at the input line VIN 812 and a smaller signal level after a filter, since these readings would indicate that a large signal is received, but that interferers are being reduced.

[0074] As before, in this example, the noise floor 1033 and maximum signal handling capability 1031 are initially set for the worst case conditions. Since the desired signal is

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relatively large in this case, the noise floor may be allowed to rise, a shown by noise floor 1043 in Figure 10C. Since the desired signal 1046 and interferers 1047 are large, the maximum signal handling capability Smax 1041 remains constant. Again, the noise floor is increased by increasing impedances in the function block 1020. This reduces the required drive current, and may also allow for a reduction in bias currents.

[0075] Figure 11A illustrates a block diagram including an optional gain element 1110 and function block 1120 in accordance with an embodiment of the present convention. An input signal is received on line 1112 by the optional gain control element 1110, while an output signal is provided by the function block 1120 on line VOUT 1122. Gain, impedance, and bias control signals are received on lines 1114, 1124, and 1126.

[0076] Figure 11B is an exemplary input signal that may be received by the gain control element 1110 on line VIN 1112. In this specific example, the desired signal 1136 is relatively low or weak while the interfering signals 1137 and 1138 are large. This may be determined, for example, by detecting a large signal level at the input line VIN 812 and a much smaller signal level after a filter, since these readings would indicate that a large signal is received and that large interferers are being reduced such that the resulting signal, the desired signal, is relatively weak.

[0077] Again, the maximum signal handling capability 1131 and noise floor 1133 are initially set for worst case conditions. If the desired signal is sufficiently low, while the interferers are sufficiently high, power savings may not be achievable over the worst case settings, since this is in fact the worst case condition. But, if the desired signal is somewhat larger than the worst case condition, then power may be saved in at least two different ways.

[0078] For example, Figure 11C shows the maximum signal handling capability 1141 being lowered. In this case, the interfering signals 1147 in 1148 began to clip and distort, thereby creating intermodulation products 1145, which distort the desired signal 1146. So long as care is taken to not corrupt the desired signal 1146 beyond an acceptable limit, typically measured by a bit-error rate, power may be reduced in this way.

[0079] Similarly, in Figure 11D, the noise floor 1153 is raised somewhat, thereby saving power. Again, this may be done so long as the noise floor is not sufficiently high that the system bit-error rate becomes unacceptable.

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[0080] Figure 12 is a summary of the above four examples. The received signal strengths are shown in column 1210, while appropriate power saving responses are listed in column 1220. Specifically, in row 1230, the desired signal and interferer signal strengths are both weak or small. In this case, proper responses include decreasing Smax, or increasing one or more circuit impedances while increasing the circuit gain. Depending on the exact circuit configuration, one of these options may be preferred over the other. Alternately, they may be done in combination, or done in combination with other power saving techniques. Also, in some specific embodiments, when both desired signal and interferer signal strengths are small, the gain may need to be increased while the impedance is maintained or not increased in order to keep the noise floor low.

[0081] In row 1240, the desired signal strength is strong or large, while the interfering signals are small. In this case, an appropriate response is to increase one or more of the circuit impedances. Again, depending on the exact circuit in question, one or more of the bias currents may also be reduced.

[0082] In row 1250, both the desired signals and interfering signal strengths are large. Again, in this case an appropriate response is to increase one or more of the circuit impedances.

[0083] In row 1260, the received desired signal strength is weak or small, while the interfering signals are large. Since this is the worst case situation for which the circuit is designed, substantial power savings are difficult to achieve. However, again, if the received signal is above a minimum level necessary for proper operation, some distortion of the interferers or raising of the noise floor may be acceptable.

[0084] It should be noted that not all possible signal conditions are listed here. For example, either the signal or interferer may be of a relatively medium strength, or the interferer may be absent. Also, these terms are for exemplary purposes and are not meant to convey specific signal conditions, but rather are only qualitative. The proper response to a specific condition depends on the embodiment of the present invention, the particular circuit topology, the requirements of the signaling standard used, as well as other constraints.

[0085] Figure 13 is an example shown how power may be saved as a function of time by employing one or more of these methods consistent with embodiments of the present invention. Power is plotted along a Y-axis 1304 as a function of time along X-axis 1302. Conventional worst case design would fix power dissipation at line 1310. As can be seen, dynamic power

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dissipation 1320 under the control of variable gains, impedances, biasing, or combination thereof, allows for a lower average power 1330 as compared to the power dissipated 1310 by the conventional design.

[0086] Figure 14 is a block diagram of a portion of a receiver consistent with an embodiment of the present invention. Included are low-noise amplifier 1410, mixer 1420, gain stage 1430, filter 1440, AGC amplifier 1450, and VCO 1460. Signal strength detection is done at the output of the low-noise amplifier by signal strength indicator 1470, at the output of the mixer by signal strength indicator 1472, and at the output of the filter by signal strength indicator 1474. The outputs of the signal strength indicator circuits are received by the computational circuit 1470, which in turn controls gain and power control circuits 1480 and 1485. Power and gain control circuits 1480 and 1485 control the gain, biasing, and impedance levels of the circuits in the receiver signal path. Also, the gain and power control circuits may control the same parameters in the VCO 1460. This figure is greatly simplified for purposes of explanation. For example, the quadrature nature of the mixers and following circuits are not shown. Also, power-down and start-up circuits are not included.

[0087] The current level in the low-noise amplifier determines a multitude of parameters including voltage gain, linearity, input impedance matching, and noise figure. When conditions are better than worst-case, some of these parameters may be relaxed while maintaining an acceptable bit-error rate, thus saving power.

[0088] The bias current in the mixers effect that block's noise figure and linearity. Care is taken in reducing power in this block so as not to increase nonlinearities, particularly the third-order nonlinearity as measured by IP3, the third-order intercept point, beyond an acceptable limit.

[0089] A key parameter of the VCO is phase noise, an increase in which increases the sidebands on either side of the oscillation signal. During transmission, the phase noise should be kept low to avoid interference with adjacent channels and for preserving modulation information.

[0090] During reception however, if the conditions are better than worst case, the phase noise requirement for the VCO is relaxed, and power can be saved consistent with embodiments of the present invention. The achievable phase noise power spectral density is approximately inversely proportional to the bias current used. Thus, when low phase noise is not required during reception, bias current in the VCO can be reduced.

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[0091] Most of the power savings in a transceiver in accordance with embodiments of the present invention is achieved in the receiver portion. Additional power may be saved in the transmitter section.

[0092] Figure 15 is a block diagram of a transmitter portion consistent with an embodiment of the present invention. Included is a signal path formed by gain stage 1510 and power amplifier 1520. The output power level is sensed by output level sensing circuit 1550, which in turn adjusts the biasing of the power amplifier 1520 through the power control circuit 1540. Additionally, a transmitter level control signal is received by power control circuits 1530 and 1540, which in turn control the biasing of gain stage 1510 and power amplifier 1520. Gain control circuit 1560 also adjusts the gain of gain stage 1510 and power amplifier 1520. Additional circuitry that varies impedances in each of these circuits may also be included.

[0093] Since the gain, impedance and biasing of these blocks are being dynamically varied, care must be taken to not negatively affect the signal being processed. For example, specific embodiments of the present invention perform some or all of these variations during preamble. Also, as changes occur, the circuits in some embodiments are limited such that they may only adapt to an improvement in conditions after frames are completed. If conditions worsen, the circuits may be allowed to change in order to save the data. Alternately, a system may be manually calibrated, for example at set up, and when the network configuration is changed.

[0094] The above description of specific embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form described, and many modifications and variations are possible in light of the teaching above. The embodiments were chosen and described in order to best explain the principles of the invention and its practical applications to thereby enable others skilled in the art to best utilize the invention in various embodiments and with various modifications as are suited to the particular use contemplated.

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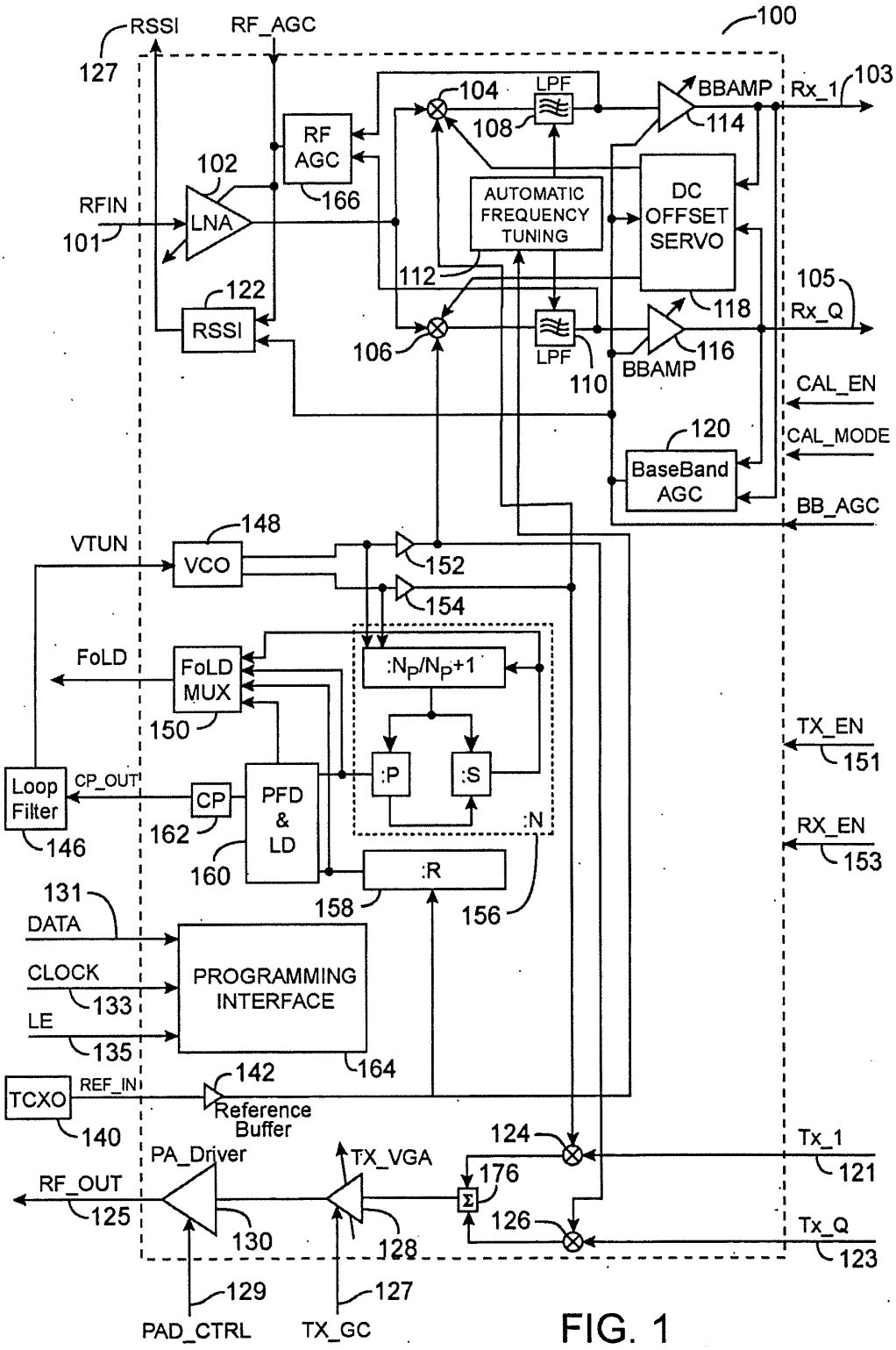

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DC OFFSET SERVO
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118
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RSSI
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LPF
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VCO
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FoLD
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:P
:S
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CP
162
PFD & LD
160
:R
158
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DATA
CLOCK
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LE
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TCXO
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FIG. 1

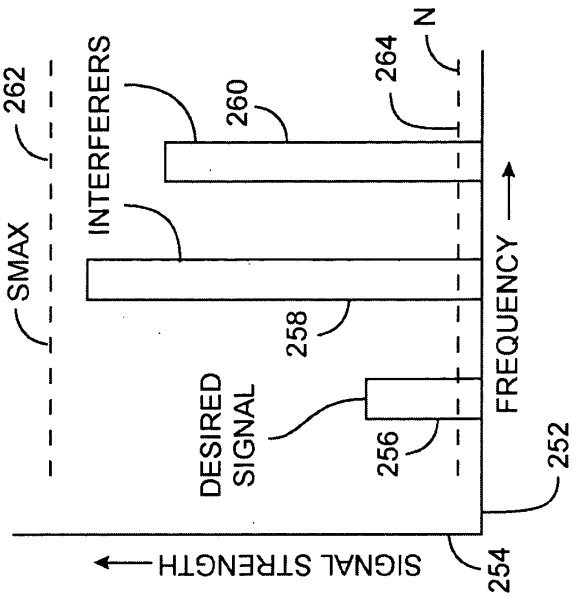

SMAX
262
INTERFERERS
260
264
N
258
DESIRED
SIGNAL
256
FREQUENCY
252
SIGNAL STRENGTH
254

FIG. 2B

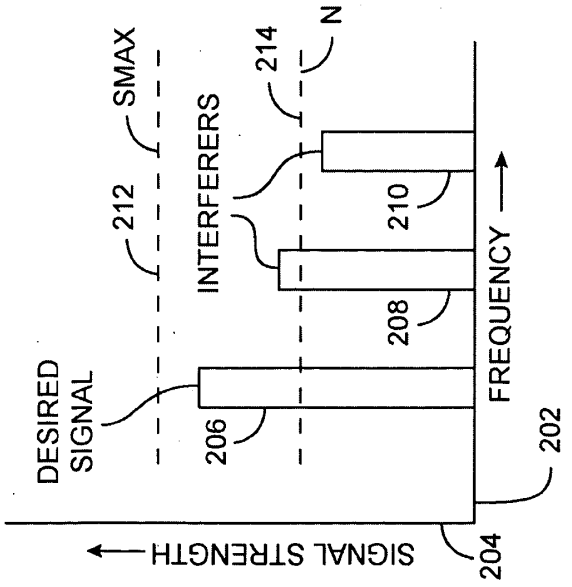

SMAX
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INTERFERERS
210
208
DESIRED
SIGNAL
206
FREQUENCY
202
SIGNAL STRENGTH
204

FIG. 2A

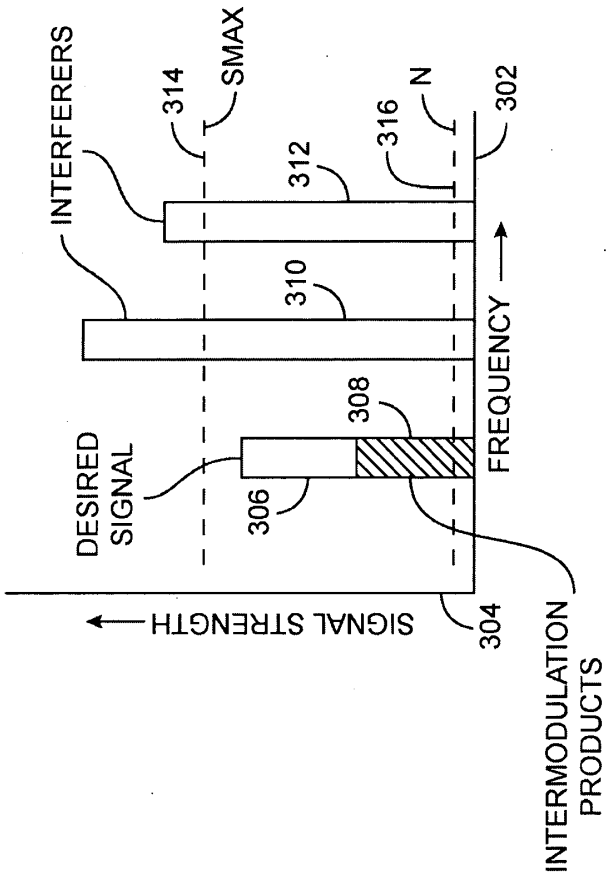

INTERFERERS
314
SMAX
312
316
N
302
310
308
DESIRED SIGNAL
306
FREQUENCY
SIGNAL STRENGTH
304
INTERMODULATION PRODUCTS

FIG. 3

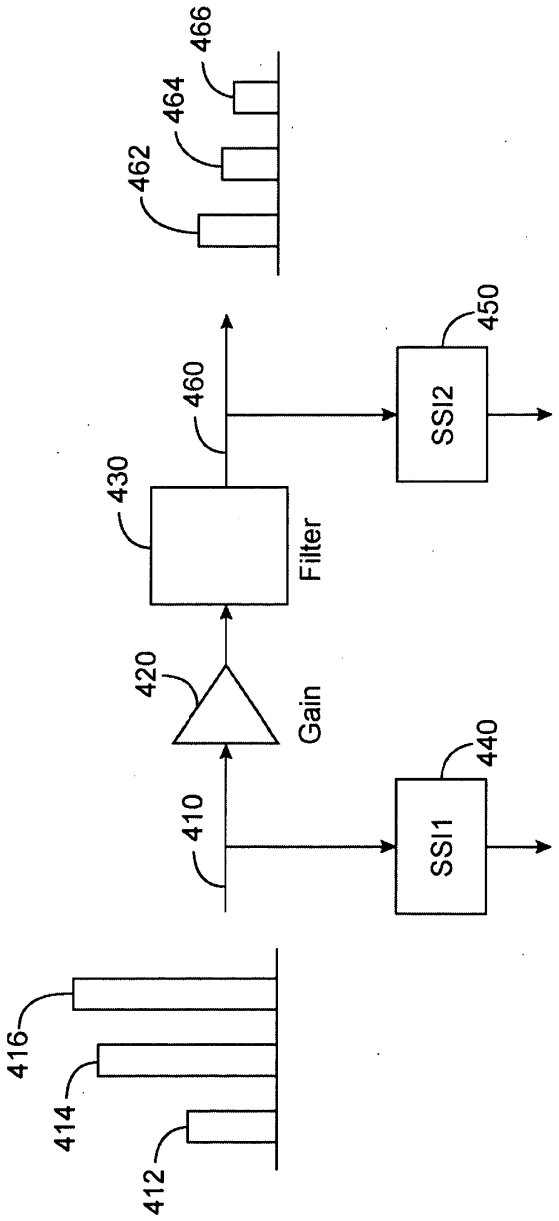

466
464
462
460
450
SSI2
430
Filter
420
Gain
410
440
SSI1
416
414
412

FIG. 4

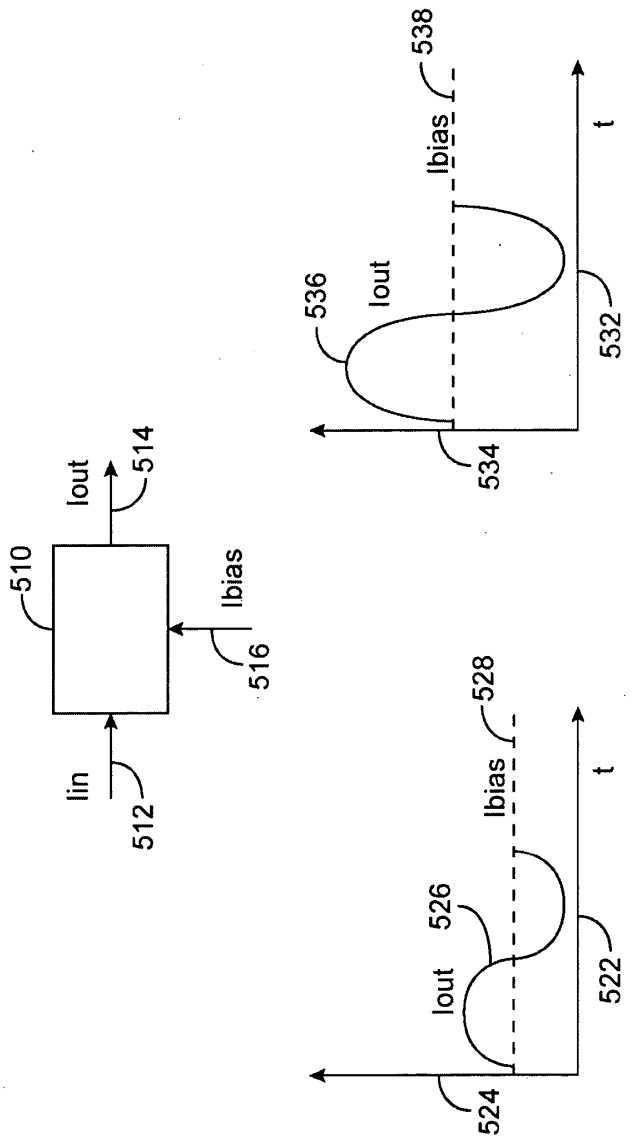

510
Iout
514
Ibias
516
Iin
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Iout
532
534
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Ibias
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526
Iout
522
524

FIG. 5

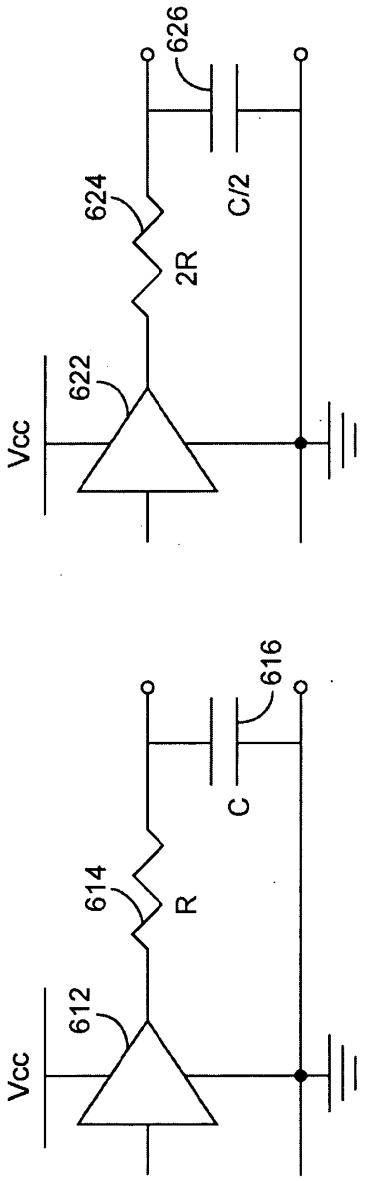


FIG. 6

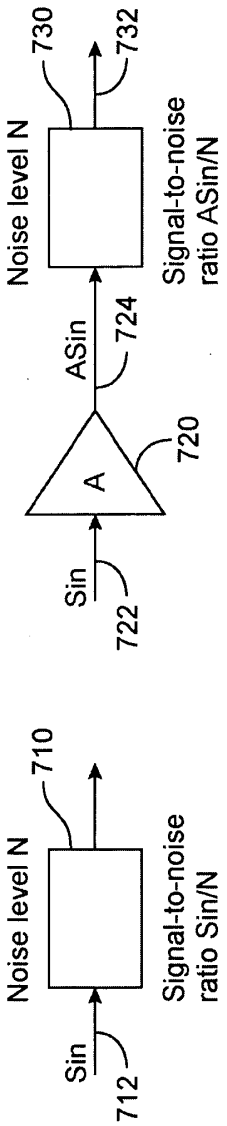

Noise level N
710
Sin
712
Signal-to-noise ratio Sin/N
Noise level N
730
732
Signal-to-noise ratio ASin/N
ASin
724
A
720
Sin
722

FIG. 7

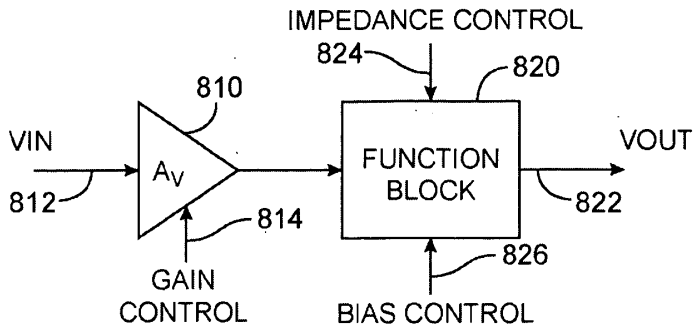


FIG. 8A

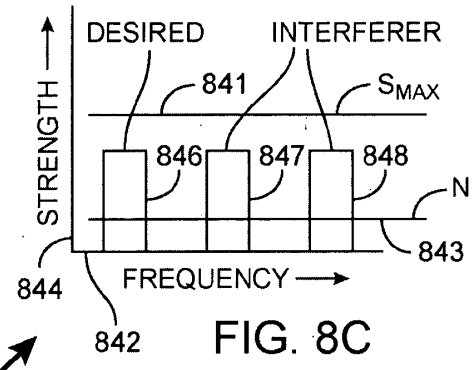


FIG. 8C

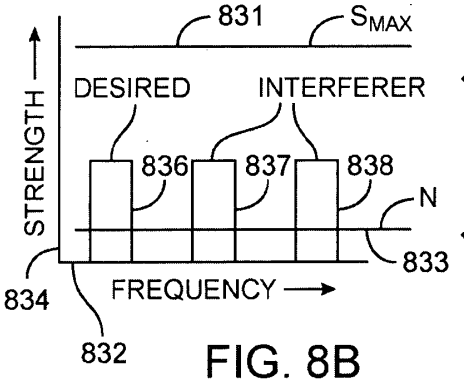


FIG. 8B

DECREASE BIASING

– AND/OR –

INCREASE GAIN AND IMPEDANCES

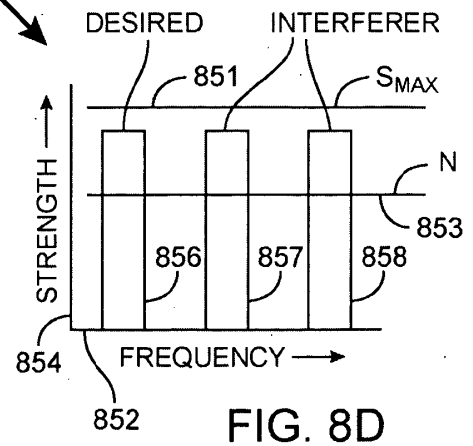


FIG. 8D

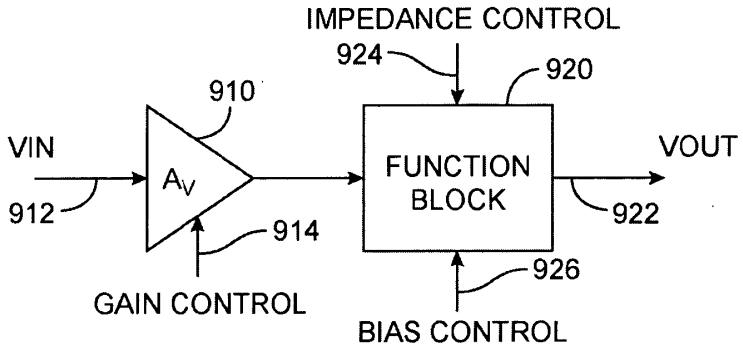


FIG. 9A

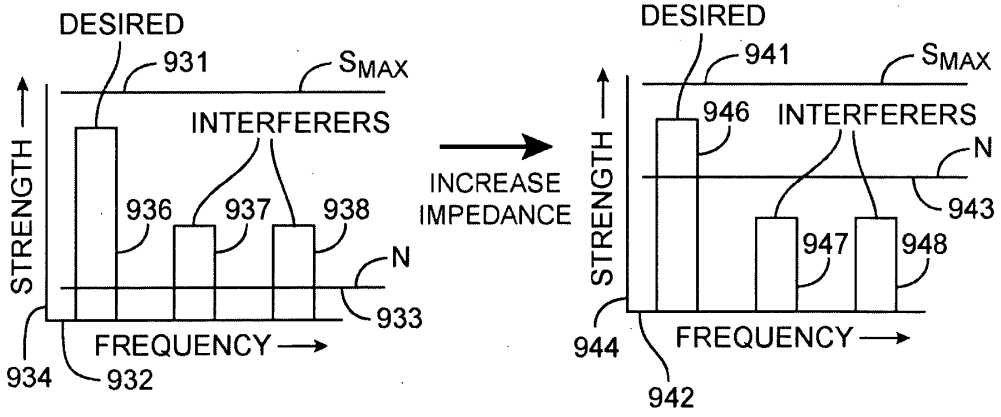


FIG. 9B

FIG. 9C

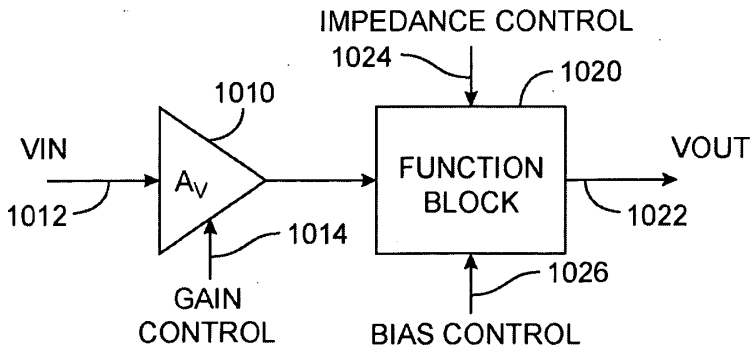


FIG. 10A

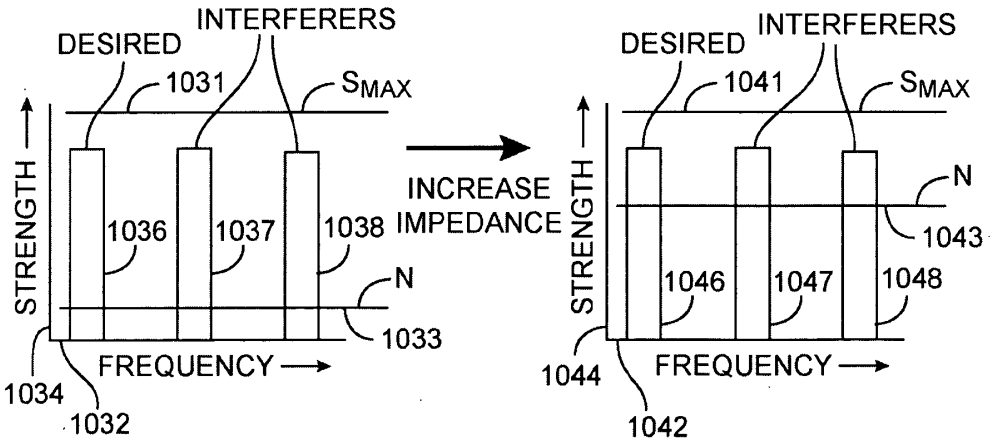


FIG. 10B

FIG. 10C

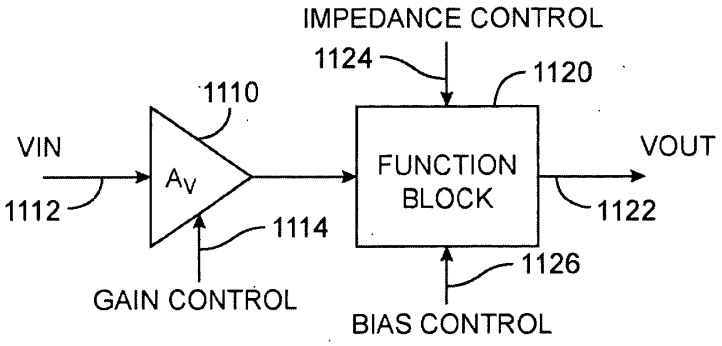


FIG. 11A

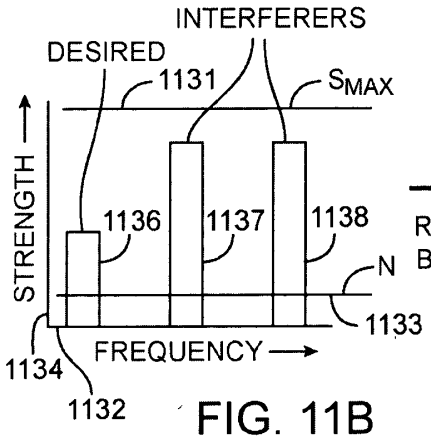


FIG. 11B

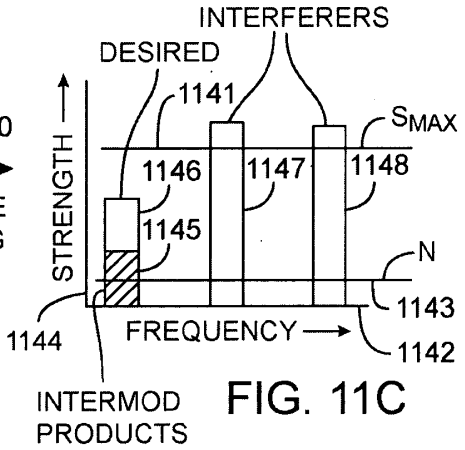
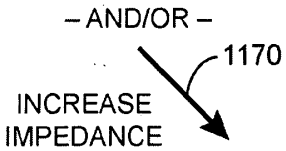


FIG. 11C



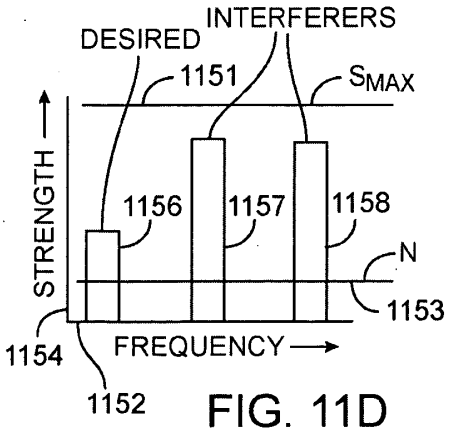


FIG. 11D

	1210 RECEIVED SIGNAL		1220 RESPONSE TO RECEIVED SIGNAL		
	SIGNAL STRENGTH	INTERFERER STRENGTH	DECREASE SMAX	INCREASE IMPEDANCE NOT GAIN	INCREASE IMPEDANCE AND GAIN
1230	SMALL	SMALL	YES	NO	YES
1240	LARGE	SMALL	NO	YES	NO
1250	LARGE	LARGE	NO	YES	NO
1260	SMALL	LARGE	NO	NO	NO

FIG. 12

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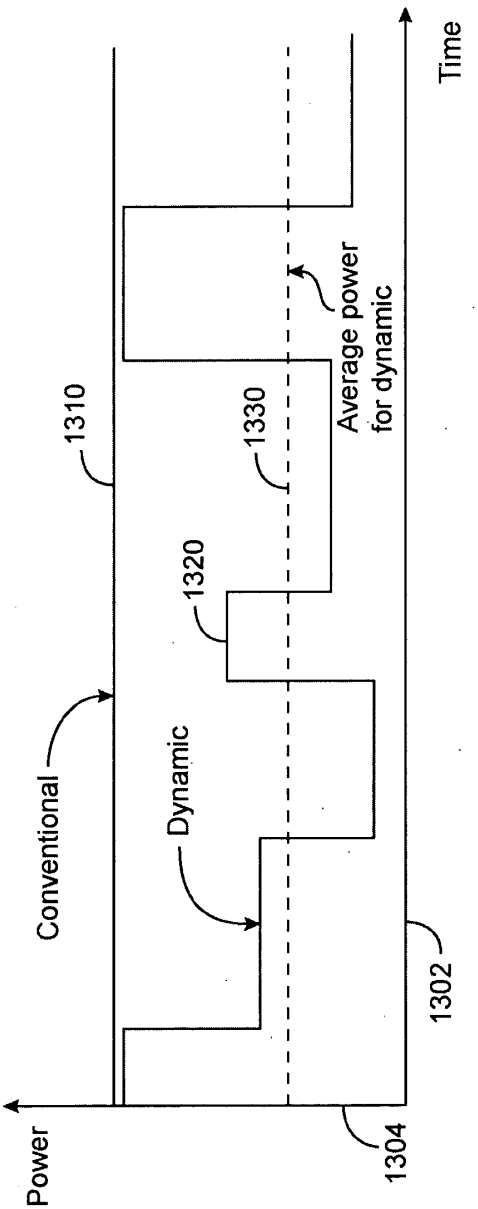

Time
Power
Conventional
Dynamic
1310
1320
1330
1302
1304
Average power
for dynamic

FIG. 13

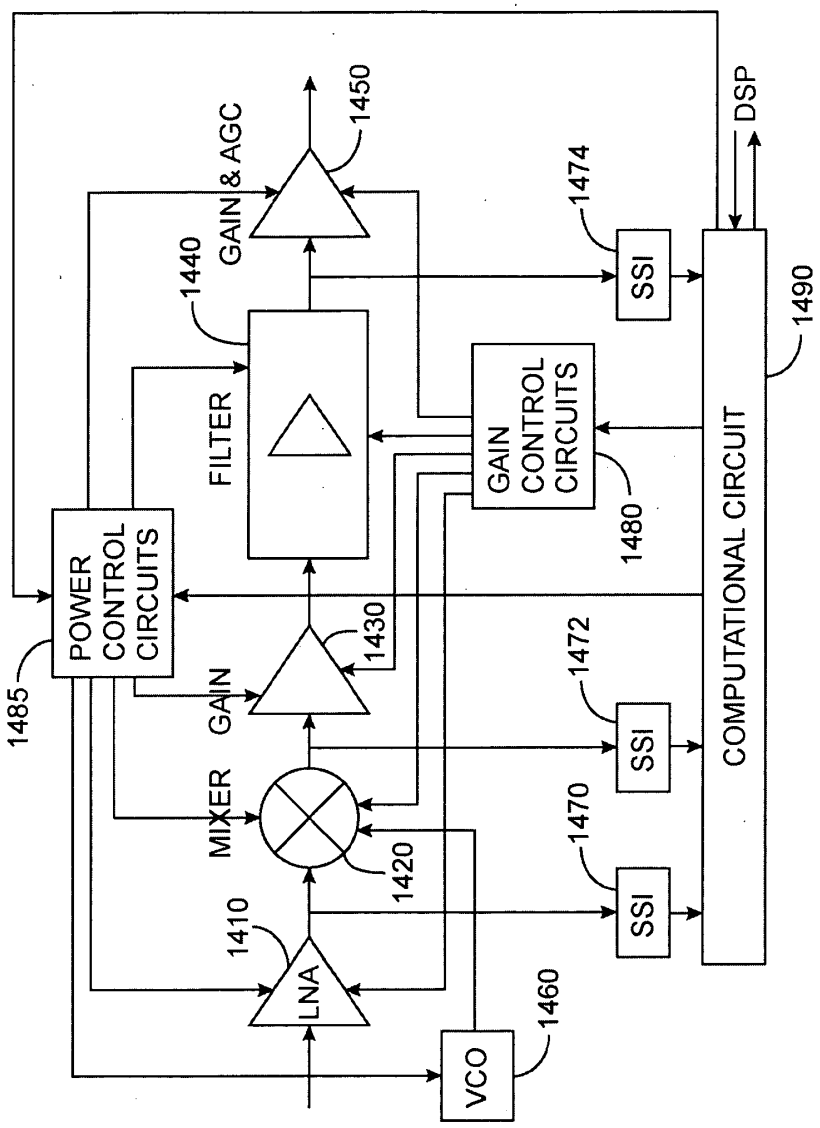

DSP
1450
GAIN & AGC
1474
SSI
1440
FILTER
GAIN CONTROL CIRCUITS
1480
1490
COMPUTATIONAL CIRCUIT
POWER CONTROL CIRCUITS
1485
1430
GAIN
1472
SSI
MIXER
1420
1470
SSI
1410
LNA
VCO
1460

FIG. 14

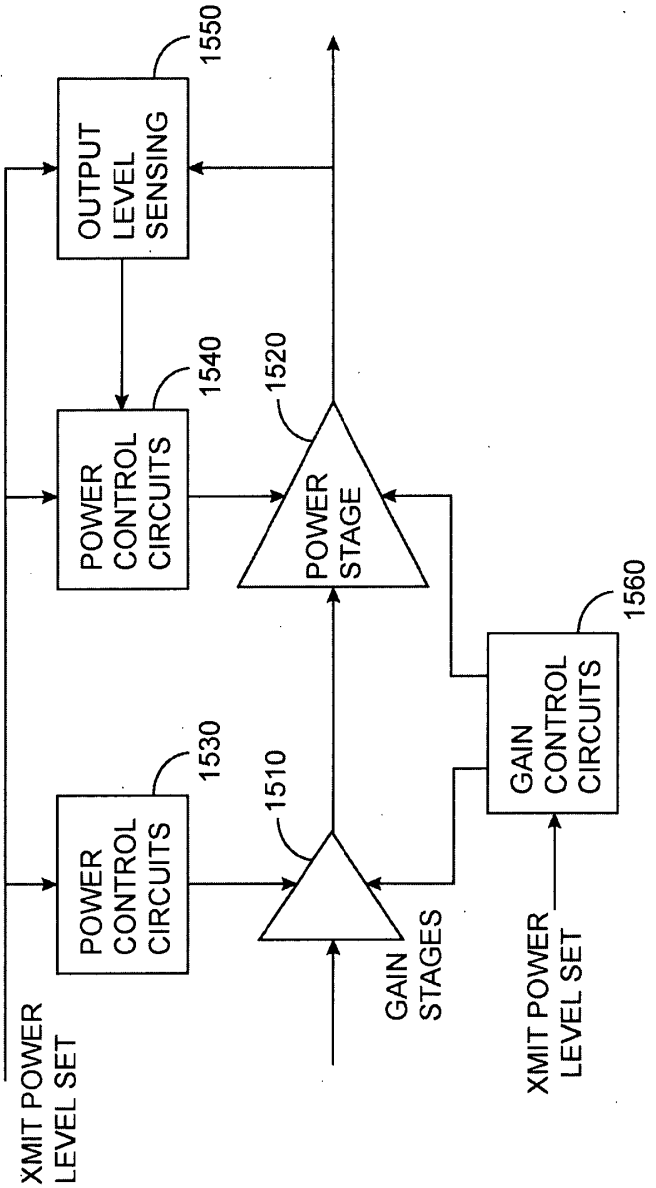

OUTPUT LEVEL SENSING
1550
POWER CONTROL CIRCUITS
1540
POWER STAGE
1520
POWER CONTROL CIRCUITS
1530
GAIN STAGES
1510
GAIN CONTROL CIRCUITS
1560
XMIT POWER LEVEL SET
XMIT POWER LEVEL SET

FIG. 15

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	Power Dissipation Reduction in Wireless Transceivers
First Named Inventor/Applicant Name:	Yannis Tsividis
Filer:	Roger W. Blakely/Jessica Clark
Attorney Docket Number:	10037P007CCC

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY FILING FEE (ELECTRONIC FILING)	4011	1	70	70
UTILITY SEARCH FEE	2111	1	300	300
UTILITY EXAMINATION FEE	2311	1	360	360
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**730**

Electronic Acknowledgement Receipt	
EFS ID:	31067468
Application Number:	15824841
International Application Number:	
Confirmation Number:	4819
Title of Invention:	Power Dissipation Reduction in Wireless Transceivers
First Named Inventor/Applicant Name:	Yannis Tsividis
Customer Number:	8791
Filer:	Roger W. Blakely/Jessica Clark
Filer Authorized By:	Roger W. Blakely
Attorney Docket Number:	10037P007CCC
Receipt Date:	28-NOV-2017
Filing Date:	
Time Stamp:	18:31:55
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$730
RAM confirmation Number	112917INTEFSW00006200022666
Deposit Account	022666
Authorized User	Jessica Clark
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.19 (Document supply fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	10037P007CCC_20171128_ADS.pdf	1793293 2b4aa9b1ebb915097e6242890c7bb24b61a82011	no	9
Warnings:					
Information:					
2	Power of Attorney	10037P007CCC_20171128_POAwTrans.pdf	1166442 5f6906e23259439b326d313929a6c275947c0914	no	2
Warnings:					
Information:					
3	Oath or Declaration filed	10037P007CCC_20171128_Decl.pdf	119365 2ab1e5030c92e9b20fa046db0aed5bcfbd808994	no	2
Warnings:					
Information:					
4		10037P007CCC_20171128_App.pdf	951292 cd8a5601eae0b186efcf15b38bff866f5fbcf417	yes	23

Multipart Description/PDF files in .zip description

Document Description	Start	End
Abstract	23	23
Claims	18	22
Specification	1	17

Warnings:					
Information:					
5	Drawings-only black and white line drawings	10037P007CCC_20171128_Figs.pdf	214194 1a4e163236876c42b1826961b0794349e91240c7	no	15

Warnings:					
Information:					
6	Fee Worksheet (SB06)	fee-info.pdf	35226 9db0708dcca370273e00856df5bc67adfefd6c2d	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	4279812	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	10037P007CCC
	Application Number	
Title of Invention	Power Dissipation Reduction in Wireless Transceivers	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 — Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Yannis		Tsividis	

Residence Information (Select One) ● US Residency Non US Residency Active US Military Service

City	New York	State/Province	NY	Country of Residence	US

Mailing Address of Inventor:

Address 1	Dept. of Electrical Engineering
Address 2	Columbia University

City	New York	State/Province	NY
Postal Code	10027	**Country**	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	08791		
Email Address		Add Email	Remove Email

Application Information:

Title of the Invention	Power Dissipation Reduction in Wireless Transceivers		
Attorney Docket Number	10037P007CCC	**Small Entity Status Claimed**	☒
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	15	**Suggested Figure for Publication (if any)**	8A

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	10037P007CCC
	Application Number	
Title of Invention	Power Dissipation Reduction in Wireless Transceivers	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	● Customer Number	US Patent Practitioner	◯ Limited Recognition (37 CFR 11.9)
Customer Number	08791		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Continuation of	15080421	2016-03-24

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	10037P007CCC
	Application Number	
Title of Invention	Power Dissipation Reduction in Wireless Transceivers	

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15080421	Continuation of	11318646	2005-12-27	9331728	2016-05-03
Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
11318646	Continuation of	10784613	2004-02-23	7010330	2006-03-07
Prior Application Status	Expired				Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
10784613	Claims benefit of provisional	60451229	2003-03-01		
Prior Application Status	Expired				Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
10784613	Claims benefit of provisional	60451230	2003-03-01		
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button.					Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

			Remove
Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)
Additional Foreign Priority Data may be generated within this form by selecting the **Add** button.			Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	10037P007CCC
	Application Number	
Title of Invention	Power Dissipation Reduction in Wireless Transceivers	

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	10037P007CCC
	Application Number	
Title of Invention	Power Dissipation Reduction in Wireless Transceivers	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	10037P007CCC
	Application Number	
Title of Invention	Power Dissipation Reduction in Wireless Transceivers	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1 — Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

● Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor
Person to whom the inventor is obligated to assign.	Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

Organization Name	Theta IP, LLC		
Mailing Address Information For Applicant:			
Address 1	710 Inglenook Court		
Address 2			
City	Coppell	**State/Province**	TX
Country	US	Postal Code	75019
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button. — Add

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	10037P007CCC
	Application Number	
Title of Invention	Power Dissipation Reduction in Wireless Transceivers	

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

Remove

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. Add

Signature:

Remove

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/RWB/			Date (YYYY-MM-DD)	2017-11-28
First Name	Roger	Last Name	Blakely	Registration Number	25831

Additional Signature may be generated within this form by selecting the Add button. Add

PTO/AIA/14 (11-15)
Approved for use through 04/30/2017. OMB 0651-0032
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Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	10037P007CCC
	Application Number	
Title of Invention	Power Dissipation Reduction in Wireless Transceivers	

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent CooperationTreaty.

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Apple EX1002 Page 56

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
15/824,841	11/28/2017	2422	730	10037P007CCC	20	3

CONFIRMATION NO. 4819

8791
BLAKELY SOKOLOFF TAYLOR & ZAFMAN
1279 Oakmead Parkway
Sunnyvale, CA 94085-4040

FILING RECEIPT

OC000000093997908

Date Mailed: 12/13/2017

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Yannis Tsividis, New York, NY;

Applicant(s)

Theta IP, LLC, Coppell, TX;

Power of Attorney: The patent practitioners associated with Customer Number 08791

Domestic Priority data as claimed by applicant

This application is a CON of 15/080,421 03/24/2016 PAT 9838962
which is a CON of 11/318,646 12/27/2005 PAT 9331728
which is a CON of 10/784,613 02/23/2004 PAT 7010330
which claims benefit of 60/451,229 03/01/2003
and claims benefit of 60/451,230 03/01/2003

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

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Apple EX1002 Page 57

If Required, Foreign Filing License Granted: 12/11/2017

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 15/824,841**

Projected Publication Date: 03/22/2018

Non-Publication Request: No

Early Publication Request: No
**** SMALL ENTITY ****
Title

Power Dissipation Reduction in Wireless Transceivers

Preliminary Class

348

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

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Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

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Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 15/824,841

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	70		N/A	
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	300		N/A	
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	360		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	20 minus 20 =	*	x 40 =	0.00	OR		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*	x 210 =	0.00			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			0.00			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				0.00			
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	730		TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/824,841	11/28/2017	Yannis Tsividis	10037P007CCC

CONFIRMATION NO. 4819

8791
WOMBLE BOND DICKINSON (US) LLP
Attn: IP Docketing
P.O. Box 7037
Atlanta, GA 30357-0037

PUBLICATION NOTICE

OC000000098229568

Title: Power Dissipation Reduction in Wireless Transceivers

Publication No.US-2018-0084492-A1
Publication Date:03/22/2018

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

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Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

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Apple EX1002 Page 61

Substitute for form 1449A/PTO	*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	15/824,841
	Filing Date	Nov 28, 2017
	First Named Inventor	Yannis Tsividis
	Group Art Unit	
	Examiner Name	
Sheet 1 of 6	Attorney Docket No: 10037P007CCC	

US PATENT DOCUMENTS					
Examiner Initial *	**Cite No [1]**	**USP Document Number**	**Publication or Issue Date YYYY-MM-DD**	**Name of Patentee or Applicant of cited Document**	**Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear**
		US-2002/0036519	2002-03-28	Krishnapura, Nagendra et al.	
		US-2002/0050861	2002-05-02	Nguyen, Thinh C., et al.	
		US-2002/0137478	2002-09-26	Masamura, Hitoshi	
		US-2002/0190796	2002-12-19	Park, Joonbae et al.	
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		US-2003/0124999	2003-07-03	Parssinen, Aarno et al.	
		US-2003/0169089	2003-09-11	Manku, Tajinder et al.	
		US-2004/0042572	2004-03-04	Palaskas, George et al.	
		US-2004/0077324	2004-04-22	Wieck, Christopher P.	
		US-2004/0091035	2004-05-13	Palaskas, George et al.	
		US-2004/0152429	2004-08-05	Haub, David et al.	
		US-3408587	1968-10-29	Lancaster, William W.	
		US-4270222	1981-05-26	Menant, Christophe	
		US-4355414	1982-10-19	Inoue, Shigeki	
		US-4894566	1990-01-16	Rush, Michael J.	
		US-5001776	1991-03-19	Clark, Edward T.	
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		US-5390357	1995-02-14	Nobusawa, Hideaki et al.	
		US-5392457	1995-02-21	Davis, Walter L., et al.	
		US-5406613	1995-04-11	Peponides, George M., et al.	
		US-5408697	1995-04-18	Price, J. M., et al.	
		US-5412498	1995-05-02	Arstein, David M., et al.	
		US-5564094	1996-10-08	Anderson, George C., et al.	
		US-5600271	1997-02-04	Erickson, Charles R., et al.	
		US-5638141	1997-06-10	Bae, Dae-sik et al.	
		US-5661437	1997-08-26	Nishikawa, Kenjiro et al.	
		US-5751148	1998-05-12	Kennedy, John F., et al.	

EXAMINER **DATE CONSIDERED**

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449) as modified by BSTZ 03/26/07

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Substitute for form 1449A/PTO	*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	15/824,841
	Filing Date	Nov 28, 2017
	First Named Inventor	Yannis Tsividis
	Group Art Unit	
	Examiner Name	
Sheet 2 of 6	Attorney Docket No: 10037P007CCC	

		US-5809400	1998-09-15	Abramsky, Victor A., et al.	
		US-5864760	1999-01-26	Gilhousen, Klein S., et al.	
		US-5867063	1999-02-02	Snider, James R., et al.	
		US-5886547	1999-03-23	Durec, Jeffrey C., et al.	
		US-5907798	1999-05-25	Abramsky, Victor A., et al.	
		US-5930692	1999-07-27	Peterzell, Paul E., et al.	
		US-5949286	1999-09-07	Jones, Mark A.	
		US-5995853	1999-11-30	Park, Hyung-Weon	
		US-6026288	2000-02-15	Bronner, Peter E.	
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		US-6259901	2001-07-10	Shinomiya, Yoshitaka et al.	
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		US-6298221	2001-10-02	Nguyen, Dien M.	
		US-6339711	2002-01-15	Otaka, Shoji et al.	
		US-6351172	2002-02-26	Ouyang, Paul H., et al.	
		US-6360085	2002-03-19	Walley, Kenneth S.	
		US-6370187	2002-04-09	Agah, Michael D.	
		US-6370210	2002-04-09	Yamamoto, Takeshi	
		US-6388525	2002-05-14	Bien, David E.	
		US-6389445	2002-05-14	Tsividis, Yannis	
		US-6400177	2002-06-04	Yoshizaki, Shoichi	
		US-6498926	2002-12-24	Ciccarelli, Steven C., et al.	
		US-6509796	2003-01-21	Nguyen, Thinh C., et al.	
		US-6529069	2003-03-04	Krishnapura, Nagendra et al.	
		US-6546058	2003-04-08	Gilhousen, Klein S., et al.	
		US-6577677	2003-06-10	Hara, Susumu	
		US-6621339	2003-09-16	Tripathi, Adya et al.	
		US-6633550	2003-10-14	Gardenfors, Karl H., et al.	
		US-6639447	2003-10-28	Manku, Tajinder et al.	
		US-6657498	2003-12-02	Park, Joonbae et al.	
		US-6668028	2003-12-23	Wieck, Christopher P.	
		US-6670901	2003-12-30	Brueske, Daniel E., et al.	
		US-6683492	2004-01-27	Krishnapura, Nagendra et al.	
		US-6687491	2004-02-03	Wieck, Christopher P.	
		US-6694129	2004-02-17	Peterzell, Paul E., et al.	

EXAMINER **DATE CONSIDERED**

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449) as modified by BSTZ 03/26/07

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Substitute for form 1449A/PTO	*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	15/824,841
	Filing Date	Nov 28, 2017
	First Named Inventor	Yannis Tsividis
	Group Art Unit	
	Examiner Name	
Sheet 3 of 6	Attorney Docket No: 10037P007CCC	

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Examiner Initials*	**Cite No [1]**	**Foreign Patent Document** Country Code/Number/Kind Code (if known)	**Publication Date** YYYY-MM-DD	**Name of Patentee or Applicant of cited Document**	**Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear**	**T[2]**
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EXAMINER **DATE CONSIDERED**

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449) as modified by BSTZ 03/26/07
* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

Substitute for form 1449A/PTO	*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	15/824,841
	Filing Date	Nov 28, 2017
	First Named Inventor	Yannis Tsividis
	Group Art Unit	
	Examiner Name	
Sheet 4 of 6	Attorney Docket No: 10037P007CCC	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	**Cite No [1]**	**Foreign Patent Document** Country Code/Number/Kind Code (if known)	**Publication Date** YYYY-MM-DD	**Name of Patentee or Applicant of cited Document**	**Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear**	**T[2]**
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		WO-2004/017589	2004-02-24	Palaskas, George et al.		

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	**Cite No [1]**	**Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.**	**T[2]**
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EXAMINER **DATE CONSIDERED**

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449) as modified by BSTZ 03/26/07

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Substitute for form 1449A/PTO	*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	15/824,841
	Filing Date	Nov 28, 2017
	First Named Inventor	Yannis Tsividis
	Group Art Unit	
	Examiner Name	
Sheet 5 of 6	Attorney Docket No: 10037P007CCC	

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	**Cite No [1]**	**Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.**	**T[2]**
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EXAMINER **DATE CONSIDERED**

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449) as modified by BSTZ 03/26/07

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Substitute for form 1449A/PTO	*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	15/824,841
	Filing Date	Nov 28, 2017
	First Named Inventor	Yannis Tsividis
	Group Art Unit	
	Examiner Name	
Sheet 6 of 6	Attorney Docket No: 10037P007CCC	

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	**Cite No [1]**	**Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.**	**T[2]**
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EXAMINER **DATE CONSIDERED**

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application. No.	:	15/824,841	Confirmation No. 4819
Inventor(s)	:	Yannis Tsividis	
Filed	:	11/28/2017	
TC/A.U.	:		
Examiner	:		
Docket No.	:	10037P007CCC	
Customer No.	:	08791	

Commissioner for Patents
PO Box 1450
Alexandria VA 22313-1450

NOTICE OF COPENDING U.S. PATENT APPLICATION

Sir:

In accordance with the duty of disclosure, Applicant hereby provides notice of the following copending application, which may have similar subject matter:

U.S. Patent Application No. 15/080,432, filed 03/24/2016

Respectfully submitted,

WOMBLE BOND DICKINSON (US) LLP

Dated: 05/03/2018

By _____
Roger W. Blakely, Jr.
Reg. No. 25,831
Tel.: (714) 557-3800 (Pacific Coast)

P.O. Box 7037
Atlanta, Georgia 30357-0037

CERTIFICATE OF TRANSMISSION (37 CFR 1.8A)

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.

Date: 05/03/2018

_____
Jessica A. Clark *Date*

IPR2024-00818
Apple EX1002 Page 68

Electronic Acknowledgement Receipt	
EFS ID:	32523263
Application Number:	15824841
International Application Number:	
Confirmation Number:	4819
Title of Invention:	Power Dissipation Reduction in Wireless Transceivers
First Named Inventor/Applicant Name:	Yannis Tsividis
Customer Number:	8791
Filer:	Roger W. Blakely/Jessica Clark
Filer Authorized By:	Roger W. Blakely
Attorney Docket Number:	10037P007CCC
Receipt Date:	03-MAY-2018
Filing Date:	28-NOV-2017
Time Stamp:	13:58:46
Application Type:	Utility under 35 USC 111(a)

Payment information:

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	10037P007CCC_20180503_IDS Letter.pdf	72851 d6649816b1723b84730e964a338967f14fa97be1	no	1
Warnings:					

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2	Information Disclosure Statement (IDS) Form (SB08)	10037P007CCC_20180503_IDS.pdf	213409 1488bd55f05c1b04d13338a4fc725d3247008c15	no	6
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3	Transmittal Letter	10037P007CCC_20180503_NoticeCopendingApp.pdf	28266 81f397971a2c752b4ffc2c6acc44abfb412699d10	no	1
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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application No.	15/824,841
Filing Date	November 28, 2017
First Inventor	Yannis Tsividis
Art Unit	
Examiner Name	
Attorney Docket No.	10037P007CCC Conf. No. 4819

DUTY OF DISCLOSURE STATEMENT

In accordance with the duty of disclosure, enclosed is a copy of an Information Disclosure Statement (IDS) Citation Form PTO/SB/08 or PTO-1449, together with copies of the documents cited on that form, except for copies not required to be submitted (e.g., copies of U.S. patents and U.S. published patent applications need not be enclosed). This IDS and IDS Citation Form are being submitted before the mailing of a first Office Action on the merits. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s). Some or all of the references listed on the enclosed PTO/SB/08 were previously identified in one or more prior applications as follows:
Application No. 10/784,613, filed February 23, 2004
Application No. 11/318,646, filed December 27, 2005
Application No. 15/080,421, filed March 24, 2016
and copies of the references were furnished at that time. Accordingly, per 37 CFR §1.98(d)(1) additional copies of those references are not submitted herewith.

The submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

OR

☒ None

☐ The IDS Filing Fee in the amount of $120.00 as set forth in 37 CFR 1.17(p) has been submitted herewith.

☒ It is requested that any requisite fees be debited from Deposit Account 090528.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of signature.

Signature	Roger W Blakely	Date (MM-DD-YYYY)	05-03-2018
Name/Print	Roger W. Blakely, Jr.	Registration Number	25831

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.

Jessica A. Clark Jessica A Clark *Date* *05-03-18*

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application. No.	:	15/824,841	Confirmation No. 4819
Inventor(s)	:	Yannis Tsividis	
Filed	:	11/28/2017	
TC/A.U.	:	2647	
Examiner	:	Vuong, Quochien B	
Docket No.	:	10037P007CCC	
Customer No.	:	8791	

Commissioner for Patents
PO Box 1450
Alexandria VA 22313-1450

PRE-EXAMINATION AMENDMENT

Sir:

Please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 8 of this paper.

IPR2024-00818
Apple EX1002 Page 72

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-20 (cancelled)

21. (New) A method of reducing the power consumption of a receiver of a battery operated transceiver having a plurality of circuits, wherein the plurality of circuits comprise a receiver signal path comprising at least an amplifier, a mixer and a filter, the plurality of circuits further comprise circuits for determining at least a signal strength indication in the signal path of the receiver; the method comprising:

receiving a signal comprising a desired signal and an interferer signal in the signal path of the receiver;

determining a first signal strength indication, wherein the first signal strength indication is relative to the strength of the received signal;

determining a second signal strength indication, wherein the second signal strength indication is relative to the strength of the signal after filtering the received signal to reduce the interferer signal;

comparing the first and second signal strength indication, and

adjusting at least one of an impedance, a bias or a gain of at least one of the amplifier, filter or mixer in the signal path, responsive to the changes in the strength of the first and second signal strength indication as below:

when the second signal strength indication increases, increasing the impedance of at least one of the plurality of circuits in the signal path.

22. (New) A method of reducing the power consumption of a receiver of a battery operated transceiver having a plurality of circuits, wherein the plurality of circuits comprise a receiver signal path comprising at least an amplifier, a mixer and a filter, the plurality of circuits

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Apple EX1002 Page 73

further comprising circuits for determining at least a signal strength indication in the signal path of the receiver; the method comprising:

receiving a signal comprising a desired signal and an interferer signal in the signal path of the receiver;

determining a first signal strength indication, wherein the first signal strength indication is relative to the strength of the received signal;

determining a second signal strength indication, wherein the second signal strength indication is relative to the strength of the signal after filtering the received signal to reduce the interferer signal;

comparing the first and second signal strength indication to determine a signal strength indication of a desired signal and a signal strength indication of an interferer signal; and

when the indicated interferer signal strength decreases, and the indicated strength of the desired signal decreases, decreasing the bias of at least one of the plurality of circuits in the signal path.

23. (New) A method of reducing the power consumption of a receiver of a battery operated transceiver having a plurality of circuits, wherein the plurality of circuits comprise a receiver signal path comprising at least an amplifier, a mixer and a filter, the plurality of circuits further comprising circuits for determining at least a signal strength indication in the signal path of the receiver; the method comprising:

receiving a signal comprising a desired signal and an interferer signal in the signal path of the receiver;

determining a first signal strength indication, wherein the first signal strength indication is relative to the strength of the received signal;

determining a second signal strength indication, wherein the second signal strength indication is relative to the strength of the signal after filtering the received signal to reduce the interferer signal;

comparing the first and second signal strength indications to determine a signal strength indication of the desired signal and a signal strength indication of the interferer signal; and

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Apple EX1002 Page 74

when the indicated interferer signal strength decreases, and the indicated strength of the desired signal decreases, increasing a gain of at least one of a plurality of circuits in the signal path and increasing an impedance of at least one of the plurality of circuits in the signal path.

24. (New) A method for reducing power consumption in a receiver in a battery operated mobile device where the receiver receives a wireless signal and comprises a plurality of circuits, the plurality of circuits comprising a signal path including at least an amplifier, a mixer and a filter, and wherein the receiver also comprises circuits for determining at least a signal strength at a one or more locations in the signal path, the method comprising:

filtering the received signal to determine a signal strength of a desired signal and a signal strength of an interferer signal; and

when the signal strength of the desired signal is greater than the signal strength of the interferer signal, increasing an impedance of at least one of the amplifier, filter or mixer in the signal path of the receiver, thereby reducing power dissipation in the receiver.

25. (New) A method for reducing power consumption in a receiver in a battery operated mobile device where the receiver receives a wireless signal and comprises a plurality of circuits, the plurality of circuits comprising a signal path including at least an amplifier, a mixer and a filter, and wherein the receiver also comprises circuits for determining signal strengths at a plurality of locations in the signal path, the method comprising:

filtering the received signal to determine a signal strength of a desired signal and a signal strength of an interferer signal; and

when the signal strength of the interferer signal is greater than the signal strength of the desired signal, reducing a bias of at least one of the plurality of circuits in the signal path of the receiver, thereby reducing power dissipation in the receiver.

26. (New) A method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, the method comprising:

receiving a wireless signal having a desired signal strength and an interferer signal strength by the receiver, the receiver having a plurality of circuits to function under a worst case

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condition when a received desired signal strength is low and a received interferer signal strength is high, the receiver having a signal path comprising a plurality of circuits including at least an amplifier, a filter, and a mixer, and wherein the receiver also comprises circuits determining a received desired signal strength and determining a received interferer signal strength; and

when the signal strength of the interferer signal is high and the signal strength of the desired signal is high, causing an impedance of one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be increased compared to the worst-case power dissipation condition, thereby saving power.

27. (New) A method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, the method comprising:

receiving a wireless signal having a desired signal strength and an interferer signal strength by the receiver, the receiver having a plurality of circuits to function under a worst case condition when a received desired signal strength is low and a received interferer signal strength is high, the receiver having a signal path comprising a plurality of circuits including at least an amplifier, a filter, and a mixer, and wherein the receiver also comprises circuits determining a received desired signal strength and determining a received interferer signal strength; and

when the signal strength of the interferer signal is low and the signal strength of the desired signal is low, causing a bias current of one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be decreased compared to the worst-case power dissipation condition, thereby saving power.

28. (New) A method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, the method comprising:

receiving a wireless signal having a desired signal strength and an interferer signal strength by the receiver, the receiver having a plurality of circuits to function under a worst case condition when a received desired signal strength is low and a received interferer signal strength is high, the receiver having a signal path comprising a plurality of circuits including at least an amplifier, a filter, and a mixer, and wherein the receiver also comprises circuits determining a received desired signal strength and determining a received interferer signal strength; and

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when the signal strength of the interferer signal is low and the signal strength of the desired signal is low, causing an impedance and a gain of one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be increased compared to the worst-case power dissipation condition, thereby saving power.

29. (New) A method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, the method comprising:

receiving a wireless signal having a desired signal strength and an interferer signal strength by the receiver, the receiver having a plurality of circuits to function under a worst case condition when a received desired signal strength is low and a received interferer signal strength is high, the receiver having a signal path comprising a plurality of circuits including at least an amplifier, a filter, and a mixer, and wherein the receiver also comprises circuits determining a received desired signal strength and determining a received interferer signal strength; and

when the signal strength of the interferer signal is low and the signal strength of the desired signal is high, causing an impedance of one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be increased compared to the worst-case power dissipation condition, thereby saving power.

30. (New) A method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, the method comprising:

receiving a wireless signal having a desired signal strength and an interferer signal strength by the receiver, the receiver having a plurality of circuits to function under a worst case condition when a received desired signal strength is low and a received interferer signal strength is high, the receiver having a signal path comprising a plurality of circuits including at least an amplifier, a filter, and a mixer, and wherein the receiver also comprises circuits determining a received desired signal strength and determining a received interferer signal strength; and

when the signal strength of the interferer signal is high and the signal strength of the desired signal is low, and the desired signal has a signal strength that is larger than in the worst-case power dissipation conditions, causing an impedance of one or more of the plurality of

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circuits in the receiver signal path of the wireless transceiver to be increased compared to the worst-case power dissipation condition, causing a reduction in power dissipation.

31. (New) A method for reducing power consumption in a receiver in a battery operated mobile device where the receiver receives a wireless signal and comprises a plurality of circuits, the plurality of circuits comprising a signal path including at least an amplifier, a mixer and a filter, and wherein the receiver also comprises circuits for determining a signal strength at least at a location in the signal path, the method comprising:

filtering the received signal to determine a signal strength of an interferer signal; and

when the signal strength of the interferer signal is high, increasing an impedance of at least one of the plurality of circuits in the signal path of the receiver, thereby reducing power dissipation in the receiver.

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Remarks/Arguments.

Prior to the examination of the claims currently on file in this RCE, Applicant presents new claims 21-31 for examination herein and cancels claims 1-20 previously on file. These new claims are being submitted in accordance with an agreement of the examiner that examination of this case would be conducted on these claims rather than the pending claims provided this pre-examination amendment was filed on or before July 3, 2018.

In this pre-examination amendment the new claims have been drafted to claim the invention in simplified and alternate forms as follows:

New Claim 21 claims the method of the present invention in accordance with Figures 9 and 10 and the corresponding descriptions thereof which may be found in paragraphs [0069] to [0074] of the application as filed.

New Claim 22 claims the invention in accordance with Figure 8C and the description thereof which may be found in paragraph [0066] of the application as originally filed.

New Claim 23 claims the invention disclosed at Figure 8D and as described in paragraph [0067] of the application as originally filed.

New Claim 24 claims the invention disclosed in Figures 9B and 9C as described in paragraphs [0070] and [0071] of the application as originally filed.

New Claim 25 claims the invention disclosed in Figure 11C as described in paragraph [0078] of the application as originally filed.

New Claim 26 claims the invention disclosed in Figures 10B and 10C and as described in paragraphs [0073] and [0074] of the application as originally filed.

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New Claim 27 claims the invention disclosed in the application as originally filed in Figure 8C in a form alternate to that of Figure 28 and again as disclosed in the paragraph [0066] of the application as originally filed.

New Claim 28 claims the invention disclosed in Figure 8D in the application as originally filed and described in paragraph [0067].

New Claim 29 claims the invention disclosed in Figure 9C and described in paragraph [0071] of the application as originally filed.

New Claim 30 claims the invention disclosed in Figure 11D as disclosed in paragraph [0079] of the application as original filed, the noise floor being dependent upon the impedance of one or more of the plurality of circuits in the receiver signal path as best illustrated in Figures 9B and 9C as well as Figures 10B and 10C of the application as originally filed.

New Claim 31 claims the invention of Figures 10C and 11D of the application as described in paragraphs [0074] and [0079] as originally filed, again the noise floor varying in response to an impedance of one or more of the plurality of circuits in the receiver signal path as illustrated in Figures 9B and 9C as well as Figures 10B and 10C.

Accordingly, Applicant believes that all claims in the case as filed herein are in condition for allowance.

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CONCLUSION

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 07/02/2018

By / RWB /
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CERTIFICATE OF TRANSMISSION (37 CFR 1.8A)

I hereby certify that this correspondence is being EFS Web transmitted to the USPTO on the date shown below.

Date: 07/03/2018

/Jessica A. Clark/ ***07/03/2018***
Jessica A. Clark *Date*

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Electronic Patent Application Fee Transmittal				
Application Number:	15824841			
Filing Date:	28-Nov-2017			
Title of Invention:	Power Dissipation Reduction in Wireless Transceivers			
First Named Inventor/Applicant Name:	Yannis Tsividis			
Filer:	Roger W. Blakely/Jessica Clark			
Attorney Docket Number:	10037P007CCC			
Filed as Small Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	**Fee Code**	**Quantity**	**Amount**	**Sub-Total in USD($)**
Basic Filing:				
Pages:				
Claims:				
INDEPENDENT CLAIMS IN EXCESS OF 3	2201	8	230	1840
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1840**

Electronic Acknowledgement Receipt	
EFS ID:	33084944
Application Number:	15824841
International Application Number:	
Confirmation Number:	4819
Title of Invention:	Power Dissipation Reduction in Wireless Transceivers
First Named Inventor/Applicant Name:	Yannis Tsividis
Customer Number:	8791
Filer:	Roger W. Blakely/Jessica Clark
Filer Authorized By:	Roger W. Blakely
Attorney Docket Number:	10037P007CCC
Receipt Date:	03-JUL-2018
Filing Date:	28-NOV-2017
Time Stamp:	16:54:05
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$1840
RAM confirmation Number	070518INTEFSW00005825090528
Deposit Account	090528
Authorized User	Jessica Clark
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.19 (Document supply fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		10037P007CCC_20180703_PreExamAmd.pdf	198750 f5a061ccb2021cd8a938d1faf41b1dc741616c37	yes	10

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Preliminary Amendment	1	1
	Claims	2	7
	Applicant Arguments/Remarks Made in an Amendment	8	10

Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30676 38ec54d7989b70c51716726017957e98704cc9d9	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	229426		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 15/824,841	Filing Date 11/28/2017	☐ To be Mailed

ENTITY: ☐ LARGE ☑ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $40 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $210 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

AMENDMENT	07/03/2018	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 11	Minus	** 20	= 0		x $50 =	0
	Independent (37 CFR 1.16(h))	* 11	Minus	*** 3	= 8		x $230 =	1840
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	1840

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	diana A bates
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/824,841	11/28/2017	Yannis Tsividis	10037P007CCC	4819

8791 7590 07/18/2018

WOMBLE BOND DICKINSON (US) LLP
Attn: IP Docketing
P.O. Box 7037
Atlanta, GA 30357-0037
UNITED STATES OF AMERICA

EXAMINER
VUONG, QUOCHIEN B

ART UNIT	PAPER NUMBER
2647	

NOTIFICATION DATE	DELIVERY MODE
07/18/2018	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

FIP_Group@bstz.com
PTO.MAIL@BSTZPTO.COM
PTO.MAIL@BSTZ.COM

Office Action Summary	Application No. 15/824,841	Applicant(s) TSIVIDIS, YANNIS	
	Examiner QUOCHIEN B. VUONG	Art Unit 2647	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07/03/2018*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *21-31* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *21-31* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *11/28/2017* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

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The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 05/03/2018 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 112

The following is a quotation of 35 U.S.C. 112(b):

> (b) CONCLUSION.—The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention.

The following is a quotation of 35 U.S.C. 112 (pre-AIA), second paragraph:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 26-30 are rejected under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor, or for pre-AIA the applicant regards as the invention.

Claim 26 recites the limitation "**the worst-case power dissipation condition**" in claim 26, lines 11-12. There is insufficient antecedent basis for this limitation in the claim.

Claim 27 recites the limitation "**the worst-case power dissipation condition**" in claim 27, lines 11-12. There is insufficient antecedent basis for this limitation in the claim.

Claim 28 recites the limitation "**the worst-case power dissipation condition**" in claim 28, lines 11-12. There is insufficient antecedent basis for this limitation in the claim.

Claim 29 recites the limitation "**the worst-case power dissipation condition**" in claim 29, lines 11-12. There is insufficient antecedent basis for this limitation in the claim.

Claim 30 recites the limitation "**the worst-case power dissipation condition**" in claim 30, lines 10-11. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 21-31 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Clark (US 5,001,776) in view of Leifso et al. (US 6,870,425).

Regarding claim 21, Clark (figure 1) discloses a method of reducing the power consumption of a receiver of a battery operated transceiver having a plurality of circuits,

wherein the plurality of circuits comprise a receiver signal path comprising at least an amplifier (108, 122), a mixer (110) and a filter (103), the plurality of circuits further comprise circuits for determining at least a signal strength indication in the signal path of the receiver; the method comprising: receiving a signal comprising a desired signal and an interferer signal in the signal path of the receiver; determining a first signal strength indication, wherein the first signal strength indication is relative to the strength of the received signal (127); determining a second signal strength indication, wherein the second signal strength indication is relative to the strength of the signal after filtering the received signal to reduce the interferer signal (127'); comparing the first and second signal strength indication, and adjusting at least one of an impedance, a bias or a gain of at least one of the amplifier, filter or mixer in the signal path, responsive to the changes in the strength of the first and second signal strength indication (via control lines 132, 134, 138 and 140); when the second signal strength indication increases, adjusting the gain of at least one of the plurality of circuits in the signal path (column 2, line 34 – column 4, line 66). Clark does not specifically disclose when the second signal strength indication increases, increasing the impedance of at least one of the plurality of circuits in the signal path. However, Leifso et al. (figure 4) disclose adjusting a gain of an amplifier by changing of the value of an impedance of at least one of the plurality of circuits in the signal path (column 6, line 26 – column 8, line 15). Therefore, it would have been obvious for one having ordinary skill in the art at the time the invention was made to adapt the teaching of adjusting the gain of the amplifier by adjusting the impedance of Leifso et al. to the method of Clark as a system design preference for

performing the same function as controlling and adjusting the gain of the amplifier and power consumption in the receiver.

Regarding claim 22, Clark (figure 1) discloses a method of reducing the power consumption of a receiver of a battery operated transceiver having a plurality of circuits, wherein the plurality of circuits comprise a receiver signal path comprising at least an amplifier (108, 122), a mixer (110) and a filter (120), the plurality of circuits further comprising circuits for determining at least a signal strength indication in the signal path of the receiver; the method comprising: receiving a signal comprising a desired signal and an interferer signal in the signal path of the receiver; determining a first signal strength indication, wherein the first signal strength indication is relative to the strength of the received signal (127); determining a second signal strength indication, wherein the second signal strength indication is relative to the strength of the signal after filtering the received signal to reduce the interferer signal (127'); comparing the first and second signal strength indication to determine a signal strength indication of a desired signal and a signal strength indication of an interferer signal; and when the indicated interferer signal strength decreases, and the indicated strength of the desired signal decreases, decreasing the gain of at least one of the plurality of circuits in the signal path (column 2, line 34 – column 4, line 66). Clark does not specifically disclose when the indicated interferer signal strength decreases, and the indicated strength of the desired signal decreases, decreasing the bias of at least one of the plurality of circuits in the signal path. However, Leifso et al. (figure 4) disclose adjusting a gain of an amplifier by changing a bias of at least one of the plurality of circuits in the signal path (column 6,

line 26 – column 8, line 15). Therefore, it would have been obvious for one having ordinary skill in the art at the time the invention was made to adapt the teaching of adjusting the gain of the amplifier by adjusting the bias of Leifso et al. to the method of Clark as a system design preference for performing the same function as controlling and adjusting the gain of the amplifier and power consumption in the receiver.

Regarding claim 23, Clark (figure 1) discloses a method of reducing the power consumption of a receiver of a battery operated transceiver having a plurality of circuits, wherein the plurality of circuits comprise a receiver signal path comprising at least an amplifier (108, 122), a mixer (110) and a filter (120), the plurality of circuits further comprising circuits for determining at least a signal strength indication in the signal path of the receiver; the method comprising: receiving a signal comprising a desired signal and an interferer signal in the signal path of the receiver; determining a first signal strength indication, wherein the first signal strength indication is relative to the strength of the received signal (127); determining a second signal strength indication, wherein the second signal strength indication is relative to the strength of the signal after filtering the received signal to reduce the interferer signal (127'); comparing the first and second signal strength indications to determine a signal strength indication of the desired signal and a signal strength indication of the interferer signal; and when the indicated interferer signal strength decreases, and the indicated strength of the desired signal decreases, increasing a gain of at least one of a plurality of circuits in the signal path (column 2, line 34 – column 4, line 66). Clark does not specifically disclose when the indicated strength of the desired signal decreases, increasing an impedance of at least one of the plurality

of circuits in the signal path. However, Leifso et al. (figure 4) disclose adjusting a gain of an amplifier by changing an impedance of at least one of the plurality of circuits in the signal path (column 6, line 26 – column 8, line 15). Therefore, it would have been obvious for one having ordinary skill in the art at the time the invention was made to adapt the teaching of adjusting the gain of the amplifier and adjusting the impedance of Leifso et al. to the method of Clark as a system design preference for performing the same function as controlling and adjusting the gain of the amplifier and power consumption in the receiver.

Regarding claim 24, Clark (figure 1) discloses a method for reducing power consumption in a receiver in a battery operated mobile device where the receiver receives a wireless signal and comprises a plurality of circuits, the plurality of circuits comprising a signal path including at least an amplifier (108, 122), a mixer (110) and a filter (120), and wherein the receiver also comprises circuits for determining at least a signal strength at a one or more locations in the signal path, the method comprising: filtering the received signal to determine a signal strength of a desired signal and a signal strength of an interferer signal; and when the signal strength of the desired signal (127') is greater than the signal strength of the interferer signal (127), adjusting a gain of at least one of the amplifier, filter or mixer in the signal path of the receiver, thereby reducing power dissipation in the receiver path (column 2, line 34 – column 4, line 66). Clark does not specifically disclose increasing an impedance of at least one of the amplifier, filter or mixer in the signal path of the receiver. However, Leifso et al. (figure 4) disclose adjusting a gain of an amplifier by changing an impedance of at least one of

the plurality of circuits in the signal path (column 6, line 26 – column 8, line 15). Therefore, it would have been obvious for one having ordinary skill in the art at the time the invention was made to adapt the teaching of adjusting the gain of the amplifier by adjusting the impedance of Leifso et al. to the method of Clark as a system design preference for performing the same function as controlling and adjusting the gain of the amplifier and power consumption in the receiver.al path of the receiver, thereby reducing power dissipation in the receiver.

Regarding claim 25, Clark (figure 1) discloses a method for reducing power consumption in a receiver in a battery operated mobile device where the receiver receives a wireless signal and comprises a plurality of circuits, the plurality of circuits comprising a signal path including at least an amplifier (108, 122), a mixer (110) and a filter (120), and wherein the receiver also comprises circuits for determining signal strengths at a plurality of locations in the signal path, the method comprising: filtering the received signal to determine a signal strength of a desired signal and a signal strength of an interferer signal; and when the signal strength of the interferer signal (127) is greater than the signal strength of the desired signal (127'), adjusting a gain of at least one of the plurality of circuits in the signal path of the receiver, thereby reducing power dissipation in the receiver path (column 2, line 34 – column 4, line 66). Clark does not specifically reducing a bias of at least one of the plurality of circuits in the signal path of the receiver. However, Leifso et al. (figure 4) disclose adjusting a gain of an amplifier by changing a bias of at least one of the plurality of circuits in the signal path (column 6, line 26 – column 8, line 15). Therefore, it would have been obvious for

one having ordinary skill in the art at the time the invention was made to adapt the teaching of adjusting the gain of the amplifier by adjusting the bias of Leifso et al. to the method of Clark as a system design preference for performing the same function as controlling and adjusting the gain of the amplifier and power consumption in the receiver.

Regarding claim 26, Clark (figure 1) discloses a method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, the method comprising: receiving a wireless signal having a desired signal strength and an interferer signal strength by the receiver, the receiver having a plurality of circuits to function under a worst case condition when a received desired signal strength is low and a received interferer signal strength is high, the receiver having a signal path comprising a plurality of circuits including at least an amplifier (108, 122), a filter (120), and a mixer (110), and wherein the receiver also comprises circuits determining a received desired signal strength (127') and determining a received interferer signal strength (127); and when the signal strength of the interferer signal is high and the signal strength of the desired signal is high, causing a gain of one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be increased compared to the worst-case power dissipation condition, thereby saving power (column 2, line 34 – column 4, line 66). Clark does not specifically disclose causing an impedance of one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be increased. However, Leifso et al. (figure 4) disclose adjusting a gain of an amplifier by changing an impedance of at least one of the plurality of

circuits in the signal path (column 6, line 26 – column 8, line 15). Therefore, it would have been obvious for one having ordinary skill in the art at the time the invention was made to adapt the teaching of adjusting the gain of the amplifier by adjusting the impedance of Leifso et al. to the method of Clark as a system design preference for performing the same function as controlling and adjusting the gain of the amplifier and power consumption in the receiver.

Regarding claim 27, Clark (figure 1) discloses a method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, the method comprising: receiving a wireless signal having a desired signal strength and an interferer signal strength by the receiver, the receiver having a plurality of circuits to function under a worst case condition when a received desired signal strength is low and a received interferer signal strength is high, the receiver having a signal path comprising a plurality of circuits including at least an amplifier (108, 122), a filter (120), and a mixer (110), and wherein the receiver also comprises circuits determining a received desired signal strength (127') and determining a received interferer signal strength (127); and when the signal strength of the interferer signal is low and the signal strength of the desired signal is low, causing a gain of one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be decreased compared to the worst-case power dissipation condition, thereby saving power (column 2, line 34 – column 4, line 66). Clark does not specifically disclose causing a bias current of one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be decreased. However, Leifso et al. (figure 4) disclose adjusting a gain of an amplifier

by changing a bias of at least one of the plurality of circuits in the signal path (column 6, line 26 – column 8, line 15). Therefore, it would have been obvious for one having ordinary skill in the art at the time the invention was made to adapt the teaching of adjusting the gain of the amplifier by adjusting the bias current of Leifso et al. to the method of Clark as a system design preference for performing the same function as controlling and adjusting the gain of the amplifier and power consumption in the receiver.

Regarding claim 28, Clark (figure 1) discloses a method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, the method comprising: receiving a wireless signal having a desired signal strength and an interferer signal strength by the receiver, the receiver having a plurality of circuits to function under a worst case condition when a received desired signal strength is low and a received interferer signal strength is high, the receiver having a signal path comprising a plurality of circuits including at least an amplifier (108, 122), a filter (120), and a mixer (110), and wherein the receiver also comprises circuits determining a received desired signal strength (127') and determining a received interferer signal strength (127); and when the signal strength of the interferer signal is low and the signal strength of the desired signal is low, causing a gain of one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be increased compared to the worst-case power dissipation condition, thereby saving power (column 2, line 34 – column 4, line 66). Clark does not specifically disclose causing an impedance and a gain of one or more of the plurality of circuits in the

receiver signal path of the wireless transceiver to be increased. However, Leifso et al. (figure 4) disclose adjusting a gain of an amplifier and changing an impedance of at least one of the plurality of circuits in the signal path (column 6, line 26 – column 8, line 15). Therefore, it would have been obvious for one having ordinary skill in the art at the time the invention was made to adapt the teaching of adjusting the gain of the amplifier and adjusting the impedance of Leifso et al. to the method of Clark as a system design preference for performing the same function as controlling and adjusting the gain of the amplifier and power consumption in the receiver.

Regarding claim 29, Clark (figure 1) discloses a method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, the method comprising: receiving a wireless signal having a desired signal strength and an interferer signal strength by the receiver, the receiver having a plurality of circuits to function under a worst case condition when a received desired signal strength is low and a received interferer signal strength is high, the receiver having a signal path comprising a plurality of circuits including at least an amplifier (108, 122), a filter (120), and a mixer (110), and wherein the receiver also comprises circuits determining a received desired signal strength and determining a received interferer signal strength; and when the signal strength of the interferer signal is low and the signal strength of the desired signal is high, causing a gain of one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be increased compared to the worst-case power dissipation condition, thereby saving power (column 2, line 34 – column 4, line 66). Clark does not specifically disclose causing an

impedance of one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be increased. However, Leifso et al. (figure 4) disclose adjusting a gain of an amplifier by changing an impedance of at least one of the plurality of circuits in the signal path (column 6, line 26 – column 8, line 15). Therefore, it would have been obvious for one having ordinary skill in the art at the time the invention was made to adapt the teaching of adjusting the gain of the amplifier by adjusting the impedance of Leifso et al. to the method of Clark as a system design preference for performing the same function as controlling and adjusting the gain of the amplifier and power consumption in the receiver.

Regarding claim 30, Clark (figure 1) discloses a method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, the method comprising: receiving a wireless signal having a desired signal strength and an interferer signal strength by the receiver, the receiver having a plurality of circuits to function under a worst case condition when a received desired signal strength is low and a received interferer signal strength is high, the receiver having a signal path comprising a plurality of circuits including at least an amplifier (108, 122), a filter (120), and a mixer (110), and wherein the receiver also comprises circuits determining a received desired signal strength and determining a received interferer signal strength; and when the signal strength of the interferer signal is high and the signal strength of the desired signal is low, and the desired signal has a signal strength that is larger than in the worst- case power dissipation conditions, causing a gain of one or more of the plurality of circuits in the receiver signal path of the wireless transceiver

to be increased compared to the worst-case power dissipation condition, causing a reduction in power dissipation (column 2, line 34 – column 4, line 66). Clark does not specifically disclose causing an impedance of one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be increased. However, Leifso et al. (figure 4) disclose adjusting a gain of an amplifier by changing an impedance of at least one of the plurality of circuits in the signal path (column 6, line 26 – column 8, line 15). Therefore, it would have been obvious for one having ordinary skill in the art at the time the invention was made to adapt the teaching of adjusting the gain of the amplifier and adjusting the impedance of Leifso et al. to the method of Clark as a system design preference for performing the same function as controlling and adjusting the gain of the amplifier and power consumption in the receiver.

Regarding claim 31, Clark (figure 1) discloses a method for reducing power consumption in a receiver in a battery operated mobile device where the receiver receives a wireless signal and comprises a plurality of circuits, the plurality of circuits comprising a signal path including at least an amplifier (108, 122), a mixer (110) and a filter (120), and wherein the receiver also comprises circuits for determining a signal strength at least at a location in the signal path, the method comprising: filtering the received signal to determine a signal strength of an interferer signal (by comparing the received signal strength (127) including interference signal before filtering with the desired signal quality (127') after filtering); and when the signal strength of the interferer signal is high, increasing an impedance of at least one of the plurality of circuits in the signal path of the receiver, thereby reducing power dissipation in the receiver (column 2,

line 34 – column 4, line 66). Clark does not specifically disclose increasing an impedance of at least one of the plurality of circuits in the signal path of the receiver. However, Leifso et al. (figure 4) disclose adjusting a gain of an amplifier by changing an impedance of at least one of the plurality of circuits in the signal path (column 6, line 26 – column 8, line 15). Therefore, it would have been obvious for one having ordinary skill in the art at the time the invention was made to adapt the teaching of adjusting the gain of the amplifier and adjusting the impedance of Leifso et al. to the method of Clark as a system design preference for performing the same function as controlling and adjusting the gain of the amplifier and power consumption in the receiver.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the “right to exclude” granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*,

686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on nonstatutory double patenting provided the reference application or patent either is shown to be commonly owned with the examined application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. See MPEP § 717.02 for applications subject to examination under the first inventor to file provisions of the AIA as explained in MPEP § 2159. See MPEP §§ 706.02(l)(1) - 706.02(l)(3) for applications not subject to examination under the first inventor to file provisions of the AIA. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO Internet website contains terminal disclaimer forms which may be used. Please visit www.uspto.gov/patent/patents-forms. The filing date of the application in which the form is filed determines what form (e.g., PTO/SB/25, PTO/SB/26, PTO/AIA/25, or PTO/AIA/26) should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.

Claims 21, 22, 24, 27, 29 and 31 are rejected on the ground of nonstatutory double patenting as being unpatentable over claim 1 of U.S. Patent No. 9,838,962.

Although the claims at issue are not identical, they are not patentably distinct from each other because both are drawn to the same invention of a method of reducing the power consumption of a receiver of a battery operated transceiver having a plurality of circuits by varying impedance, bias current or gain of one or more of the plurality of circuits in the receiver path based on at least a signal strength indication in the signal path of the receiver.

Regarding claim 21 of the present application, claim 1 U.S. Patent No. 9,838,962 encompasses all claimed limitation including a method of reducing the power consumption of a receiver of a battery operated transceiver having a plurality of circuits, wherein the plurality of circuits comprise a receiver signal path comprising at least an amplifier, a mixer and a filter, the plurality of circuits further comprise circuits for determining at least a signal strength indication in the signal path of the receiver; the method comprising: receiving a signal comprising a desired signal and an interferer signal in the signal path of the receiver; determining a first signal strength indication, wherein the first signal strength indication is relative to the strength of the received signal; determining a second signal strength indication, wherein the second signal strength indication is relative to the strength of the signal after filtering the received signal to reduce the interferer signal; comparing the first and second signal strength indication, and adjusting at least one of an impedance, a bias or a gain of at least one of the amplifier, filter or mixer in the signal path, responsive to the changes in the strength of the first and second signal strength indication as below: when the second signal

strength indication increases, increasing the impedance of at least one of the plurality of circuits in the signal path.

Regarding claim 22 of the present application, claim 1 U.S. Patent No. 9,838,962 encompasses all claimed limitation including a method of reducing the power consumption of a receiver of a battery operated transceiver having a plurality of circuits, wherein the plurality of circuits comprise a receiver signal path comprising at least an amplifier, a mixer and a filter, the plurality of circuits further comprising circuits for determining at least a signal strength indication in the signal path of the receiver; the method comprising: receiving a signal comprising a desired signal and an interferer signal in the signal path of the receiver; determining a first signal strength indication, wherein the first signal strength indication is relative to the strength of the received signal; determining a second signal strength indication, wherein the second signal strength indication is relative to the strength of the signal after filtering the received signal to reduce the interferer signal; comparing the first and second signal strength indication to determine a signal strength indication of a desired signal and a signal strength indication of an interferer signal; and when the indicated interferer signal strength decreases, and the indicated strength of the desired signal decreases, decreasing the bias of at least one of the plurality of circuits in the signal path.

Regarding claim 24 of the present application, claim 1 U.S. Patent No. 9,838,962 encompasses all claimed limitation including a method for reducing power consumption in a receiver in a battery operated mobile device where the receiver receives a wireless signal and comprises a plurality of circuits, the plurality of circuits comprising a signal

path including at least an amplifier, a mixer and a filter, and wherein the receiver also comprises circuits for determining at least a signal strength at a one or more locations in the signal path, the method comprising: filtering the received signal to determine a signal strength of a desired signal and a signal strength of an interferer signal; and when the signal strength of the desired signal is greater than the signal strength of the interferer signal, increasing an impedance of at least one of the amplifier, filter or mixer in the signal path of the receiver, thereby reducing power dissipation in the receiver.

Regarding claim 27 of the present application, claim 1 U.S. Patent No. 9,838,962 encompasses all claimed limitation including a method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, the method comprising: receiving a wireless signal having a desired signal strength and an interferer signal strength by the receiver, the receiver having a plurality of circuits to function under a worst case condition when a received desired signal strength is low and a received interferer signal strength is high, the receiver having a signal path comprising a plurality of circuits including at least an amplifier, a filter, and a mixer, and wherein the receiver also comprises circuits determining a received desired signal strength and determining a received interferer signal strength; and when the signal strength of the interferer signal is low and the signal strength of the desired signal is low, causing a bias current of one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be decreased compared to the worst-case power dissipation condition, thereby saving power.

Regarding claim 29 of the present application, claim 1 U.S. Patent No. 9,838,962 encompasses all claimed limitation including a method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, the method comprising: receiving a wireless signal having a desired signal strength and an interferer signal strength by the receiver, the receiver having a plurality of circuits to function under a worst case condition when a received desired signal strength is low and a received interferer signal strength is high, the receiver having a signal path comprising a plurality of circuits including at least an amplifier, a filter, and a mixer, and wherein the receiver also comprises circuits determining a received desired signal strength and determining a received interferer signal strength; and when the signal strength of the interferer signal is low and the signal strength of the desired signal is high, causing an impedance of one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be increased compared to the worst-case power dissipation condition, thereby saving power.

Regarding claim 31 of the present application, claim 1 U.S. Patent No. 9,838,962 encompasses all claimed limitation including a method for reducing power consumption in a receiver in a battery operated mobile device where the receiver receives a wireless signal and comprises a plurality of circuits, the plurality of circuits comprising a signal path including at least an amplifier, a mixer and a filter, and wherein the receiver also comprises circuits for determining a signal strength at least at a location in the signal path, the method comprising: filtering the received signal to determine a signal strength of an interferer signal; and when the signal strength of the interferer signal is high,

increasing an impedance of at least one of the plurality of circuits in the signal path of the receiver, thereby reducing power dissipation in the receiver.

Claims 21, 24, 26, and 29-31 are rejected on the ground of nonstatutory double patenting as being unpatentable over claim 2 of U.S. Patent No. 9,331,728. Although the claims at issue are not identical, they are not patentably distinct from each other because both are drawn to the same invention of a method of reducing the power consumption of a receiver of a battery operated transceiver having a plurality of circuits by varying impedance, bias current or gain of one or more of the plurality of circuits in the receiver path based on at least a signal strength indication in the signal path of the receiver.

Regarding claim 21 of the present application, claim 2 of U.S. Patent No. 9,331,728 encompasses all claimed limitation including a method of reducing the power consumption of a receiver of a battery operated transceiver having a plurality of circuits, wherein the plurality of circuits comprise a receiver signal path comprising at least an amplifier, a mixer and a filter, the plurality of circuits further comprise circuits for determining at least a signal strength indication in the signal path of the receiver; the method comprising: receiving a signal comprising a desired signal and an interferer signal in the signal path of the receiver; determining a first signal strength indication, wherein the first signal strength indication is relative to the strength of the received signal; determining a second signal strength indication, wherein the second signal strength indication is relative to the strength of the signal after filtering the received

signal to reduce the interferer signal; comparing the first and second signal strength indication, and adjusting at least one of an impedance, a bias or a gain of at least one of the amplifier, filter or mixer in the signal path, responsive to the changes in the strength of the first and second signal strength indication as below: when the second signal strength indication increases, increasing the impedance of at least one of the plurality of circuits in the signal path.

Regarding claim 24 of the present application, claim 2 of U.S. Patent No. 9,331,728 encompasses all claimed limitation including a method for reducing power consumption in a receiver in a battery operated mobile device where the receiver receives a wireless signal and comprises a plurality of circuits, the plurality of circuits comprising a signal path including at least an amplifier, a mixer and a filter, and wherein the receiver also comprises circuits for determining at least a signal strength at a one or more locations in the signal path, the method comprising: filtering the received signal to determine a signal strength of a desired signal and a signal strength of an interferer signal; and when the signal strength of the desired signal is greater than the signal strength of the interferer signal, increasing an impedance of at least one of the amplifier, filter or mixer in the signal path of the receiver, thereby reducing power dissipation in the receiver.

Regarding claim 26 of the present application, claim 2 of U.S. Patent No. 9,331,728 encompasses all claimed limitation including a method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, the method comprising: receiving a wireless signal having a desired signal

strength and an interferer signal strength by the receiver, the receiver having a plurality of circuits to function under a worst case condition when a received desired signal strength is low and a received interferer signal strength is high, the receiver having a signal path comprising a plurality of circuits including at least an amplifier, a filter, and a mixer, and wherein the receiver also comprises circuits determining a received desired signal strength and determining a received interferer signal strength; and when the signal strength of the interferer signal is high and the signal strength of the desired signal is high, causing an impedance of one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be increased compared to the worst-case power dissipation condition, thereby saving power.

Regarding claim 29 of the present application, claim 2 of U.S. Patent No. 9,331,728 encompasses all claimed limitation including a method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, the method comprising: receiving a wireless signal having a desired signal strength and an interferer signal strength by the receiver, the receiver having a plurality of circuits to function under a worst case condition when a received desired signal strength is low and a received interferer signal strength is high, the receiver having a signal path comprising a plurality of circuits including at least an amplifier, a filter, and a mixer, and wherein the receiver also comprises circuits determining a received desired signal strength and determining a received interferer signal strength; and when the signal strength of the interferer signal is low and the signal strength of the desired signal is high, causing an impedance of one or more of the plurality of circuits in the receiver

signal path of the wireless transceiver to be increased compared to the worst-case power dissipation condition, thereby saving power.

Regarding claim 30 of the present application, claim 2 of U.S. Patent No. 9,331,728 encompasses all claimed limitation including a method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, the method comprising: receiving a wireless signal having a desired signal strength and an interferer signal strength by the receiver, the receiver having a plurality of circuits to function under a worst case condition when a received desired signal strength is low and a received interferer signal strength is high, the receiver having a signal path comprising a plurality of circuits including at least an amplifier, a filter, and a mixer, and wherein the receiver also comprises circuits determining a received desired signal strength and determining a received interferer signal strength; and when the signal strength of the interferer signal is high and the signal strength of the desired signal is low, and the desired signal has a signal strength that is larger than in the worst-case power dissipation conditions, causing an impedance of one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be increased compared to the worst-case power dissipation condition, causing a reduction in power dissipation.

Regarding claim 31 of the present application, claim 2 of U.S. Patent No. 9,331,728 encompasses all claimed limitation including a method for reducing power consumption in a receiver in a battery operated mobile device where the receiver receives a wireless signal and comprises a plurality of circuits, the plurality of circuits

comprising a signal path including at least an amplifier, a mixer and a filter, and wherein the receiver also comprises circuits for determining a signal strength at least at a location in the signal path, the method comprising: filtering the received signal to determine a signal strength of an interferer signal; and when the signal strength of the interferer signal is high, increasing an impedance of at least one of the plurality of circuits in the signal path of the receiver, thereby reducing power dissipation in the receiver.

Claims 21-31 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 17, 19, 21, 22, and 26 -28 of U.S. Patent No. 7.010,330. Although the claims at issue are not identical, they are not patentably distinct from each other because both are drawn to the same invention of a method of reducing the power consumption of a receiver of a battery operated transceiver having a plurality of circuits by varying impedance, bias current or gain of one or more of the plurality of circuits in the receiver path based on at least a signal strength indication in the signal path of the receiver.

Regarding claim 21 of the present application, claims 17, 19, 26 and 28 of U.S. Patent No. 7.010,330 encompass all claimed limitation including a method of reducing the power consumption of a receiver of a battery operated transceiver having a plurality of circuits, wherein the plurality of circuits comprise a receiver signal path comprising at least an amplifier, a mixer and a filter, the plurality of circuits further comprise circuits for determining at least a signal strength indication in the signal path of the receiver; the

method comprising: receiving a signal comprising a desired signal and an interferer signal in the signal path of the receiver; determining a first signal strength indication, wherein the first signal strength indication is relative to the strength of the received signal; determining a second signal strength indication, wherein the second signal strength indication is relative to the strength of the signal after filtering the received signal to reduce the interferer signal; comparing the first and second signal strength indication, and adjusting at least one of an impedance, a bias or a gain of at least one of the amplifier, filter or mixer in the signal path, responsive to the changes in the strength of the first and second signal strength indication as below: when the second signal strength indication increases, increasing the impedance of at least one of the plurality of circuits in the signal path.

Regarding claim 22 of the present application, claims 17, 19, 26-28 of U.S. Patent No. 7.010,330 encompass all claimed limitation including a method of reducing the power consumption of a receiver of a battery operated transceiver having a plurality of circuits, wherein the plurality of circuits comprise a receiver signal path comprising at least an amplifier, a mixer and a filter, the plurality of circuits further comprising circuits for determining at least a signal strength indication in the signal path of the receiver; the method comprising: receiving a signal comprising a desired signal and an interferer signal in the signal path of the receiver; determining a first signal strength indication, wherein the first signal strength indication is relative to the strength of the received signal; determining a second signal strength indication, wherein the second signal strength indication is relative to the strength of the signal after filtering the received

signal to reduce the interferer signal; comparing the first and second signal strength indication to determine a signal strength indication of a desired signal and a signal strength indication of an interferer signal; and when the indicated interferer signal strength decreases, and the indicated strength of the desired signal decreases, decreasing the bias of at least one of the plurality of circuits in the signal path.

Regarding claim 23 of the present application, claims 17, 19, 26-28 of U.S. Patent No. 7.010,330 encompass all claimed limitation including a method of reducing the power consumption of a receiver of a battery operated transceiver having a plurality of circuits, wherein the plurality of circuits comprise a receiver signal path comprising at least an amplifier, a mixer and a filter, the plurality of circuits further comprising circuits for determining at least a signal strength indication in the signal path of the receiver; the method comprising: receiving a signal comprising a desired signal and an interferer signal in the signal path of the receiver; determining a first signal strength indication, wherein the first signal strength indication is relative to the strength of the received signal; determining a second signal strength indication, wherein the second signal strength indication is relative to the strength of the signal after filtering the received signal to reduce the interferer signal; comparing the first and second signal strength indications to determine a signal strength indication of the desired signal and a signal strength indication of the interferer signal; and when the indicated interferer signal strength decreases, and the indicated strength of the desired signal decreases, increasing a gain of at least one of a plurality of circuits in the signal path and increasing an impedance of at least one of the plurality of circuits in the signal path.

Regarding claim 24 of the present application, claims 17, 19, 26-28 of U.S. Patent No. 7.010,330 encompass all claimed limitation including a method for reducing power consumption in a receiver in a battery operated mobile device where the receiver receives a wireless signal and comprises a plurality of circuits, the plurality of circuits comprising a signal path including at least an amplifier, a mixer and a filter, and wherein the receiver also comprises circuits for determining at least a signal strength at a one or more locations in the signal path, the method comprising: filtering the received signal to determine a signal strength of a desired signal and a signal strength of an interferer signal; and when the signal strength of the desired signal is greater than the signal strength of the interferer signal, increasing an impedance of at least one of the amplifier, filter or mixer in the signal path of the receiver, thereby reducing power dissipation in the receiver.

Regarding claim 25 of the present application, claims 17, 19, 26-28 of U.S. Patent No. 7.010,330 encompass all claimed limitation including a method for reducing power consumption in a receiver in a battery operated mobile device where the receiver receives a wireless signal and comprises a plurality of circuits, the plurality of circuits comprising a signal path including at least an amplifier, a mixer and a filter, and wherein the receiver also comprises circuits for determining signal strengths at a plurality of locations in the signal path, the method comprising: filtering the received signal to determine a signal strength of a desired signal and a signal strength of an interferer signal; and when the signal strength of the interferer signal is greater than the signal

strength of the desired signal, reducing a bias of at least one of the plurality of circuits in the signal path of the receiver, thereby reducing power dissipation in the receiver.

Regarding claim 26 of the present application, claims 17, 19, 26-28 of U.S. Patent No. 7.010,330 encompass all claimed limitation including a method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, the method comprising: receiving a wireless signal having a desired signal strength and an interferer signal strength by the receiver, the receiver having a plurality of circuits to function under a worst case condition when a received desired signal strength is low and a received interferer signal strength is high, the receiver having a signal path comprising a plurality of circuits including at least an amplifier, a filter, and a mixer, and wherein the receiver also comprises circuits determining a received desired signal strength and determining a received interferer signal strength; and when the signal strength of the interferer signal is high and the signal strength of the desired signal is high, causing an impedance of one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be increased compared to the worst-case power dissipation condition, thereby saving power.

Regarding claim 27 of the present application, claims 17, 19, 26-28 of U.S. Patent No. 7.010,330 encompass all claimed limitation including a method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, the method comprising: receiving a wireless signal having a desired signal strength and an interferer signal strength by the receiver, the receiver

having a plurality of circuits to function under a worst case condition when a received desired signal strength is low and a received interferer signal strength is high, the receiver having a signal path comprising a plurality of circuits including at least an amplifier, a filter, and a mixer, and wherein the receiver also comprises circuits determining a received desired signal strength and determining a received interferer signal strength; and when the signal strength of the interferer signal is low and the signal strength of the desired signal is low, causing a bias current of one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be decreased compared to the worst-case power dissipation condition, thereby saving power.

Regarding claim 28 of the present application, claims 17, 19, 26-28 of U.S. Patent No. 7.010,330 encompass all claimed limitation including a method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, the method comprising: receiving a wireless signal having a desired signal strength and an interferer signal strength by the receiver, the receiver having a plurality of circuits to function under a worst case condition when a received desired signal strength is low and a received interferer signal strength is high, the receiver having a signal path comprising a plurality of circuits including at least an amplifier, a filter, and a mixer, and wherein the receiver also comprises circuits determining a received desired signal strength and determining a received interferer signal strength; and when the signal strength of the interferer signal is low and the signal strength of the desired signal is low, causing an impedance and a gain of one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to

be increased compared to the worst-case power dissipation condition, thereby saving power.

Regarding claim 29 of the present application, claims 17, 19, 26-28 of U.S. Patent No. 7.010,330 encompass all claimed limitation including a method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, the method comprising: receiving a wireless signal having a desired signal strength and an interferer signal strength by the receiver, the receiver having a plurality of circuits to function under a worst case condition when a received desired signal strength is low and a received interferer signal strength is high, the receiver having a signal path comprising a plurality of circuits including at least an amplifier, a filter, and a mixer, and wherein the receiver also comprises circuits determining a received desired signal strength and determining a received interferer signal strength; and when the signal strength of the interferer signal is low and the signal strength of the desired signal is high, causing an impedance of one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be increased compared to the worst-case power dissipation condition, thereby saving power.

Regarding claim 30 of the present application, claims 17, 19, 26-28 of U.S. Patent No. 7.010,330 encompass all claimed limitation including a method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, the method comprising: receiving a wireless signal having a desired signal strength and an interferer signal strength by the receiver, the receiver

having a plurality of circuits to function under a worst case condition when a received desired signal strength is low and a received interferer signal strength is high, the receiver having a signal path comprising a plurality of circuits including at least an amplifier, a filter, and a mixer, and wherein the receiver also comprises circuits determining a received desired signal strength and determining a received interferer signal strength; and when the signal strength of the interferer signal is high and the signal strength of the desired signal is low, and the desired signal has a signal strength that is larger than in the worst- case power dissipation conditions, causing an impedance of one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be increased compared to the worst-case power dissipation condition, causing a reduction in power dissipation.

Regarding claim 31 of the present application, claims 17, 19, 26-28 of U.S. Patent No. 7.010,330 encompass all claimed limitation including a method for reducing power consumption in a receiver in a battery operated mobile device where the receiver receives a wireless signal and comprises a plurality of circuits, the plurality of circuits comprising a signal path including at least an amplifier, a mixer and a filter, and wherein the receiver also comprises circuits for determining a signal strength at least at a location in the signal path, the method comprising: filtering the received signal to determine a signal strength of an interferer signal; and when the signal strength of the interferer signal is high, increasing an impedance of at least one of the plurality of circuits in the signal path of the receiver, thereby reducing power dissipation in the receiver.

Claims 21, 22, 24-27, and 29-31 are provisionally rejected on the ground of nonstatutory double patenting as being unpatentable over claims 25 and 26 of copending Application No. 15/080,432 (reference application). Although the claims at issue are not identical, they are not patentably distinct from each other because both are drawn to the same invention of a method of reducing the power consumption of a receiver of a battery operated transceiver having a plurality of circuits by varying impedance, bias current or gain of one or more of the plurality of circuits in the receiver path based on at least a signal strength indication in the signal path of the receiver.

This is a provisional nonstatutory double patenting rejection because the patentably indistinct claims have not in fact been patented.

Regarding claim 21 of the present application, claim 25 of copending Application No. 15/080,432 encompasses all claimed limitation including a method of reducing the power consumption of a receiver of a battery operated transceiver having a plurality of circuits, wherein the plurality of circuits comprise a receiver signal path comprising at least an amplifier, a mixer and a filter, the plurality of circuits further comprise circuits for determining at least a signal strength indication in the signal path of the receiver; the method comprising: receiving a signal comprising a desired signal and an interferer signal in the signal path of the receiver; determining a first signal strength indication, wherein the first signal strength indication is relative to the strength of the received signal; determining a second signal strength indication, wherein the second signal strength indication is relative to the strength of the signal after filtering the received

signal to reduce the interferer signal; comparing the first and second signal strength indication, and adjusting at least one of an impedance, a bias or a gain of at least one of the amplifier, filter or mixer in the signal path, responsive to the changes in the strength of the first and second signal strength indication as below: when the second signal strength indication increases, increasing the impedance of at least one of the plurality of circuits in the signal path.

Regarding claim 22 of the present application, claim 25 of copending Application No. 15/080,432 encompasses all claimed limitation including a method of reducing the power consumption of a receiver of a battery operated transceiver having a plurality of circuits, wherein the plurality of circuits comprise a receiver signal path comprising at least an amplifier, a mixer and a filter, the plurality of circuits further comprising circuits for determining at least a signal strength indication in the signal path of the receiver; the method comprising: receiving a signal comprising a desired signal and an interferer signal in the signal path of the receiver; determining a first signal strength indication, wherein the first signal strength indication is relative to the strength of the received signal; determining a second signal strength indication, wherein the second signal strength indication is relative to the strength of the signal after filtering the received signal to reduce the interferer signal; comparing the first and second signal strength indication to determine a signal strength indication of a desired signal and a signal strength indication of an interferer signal; and when the indicated interferer signal strength decreases, and the indicated strength of the desired signal decreases, decreasing the bias of at least one of the plurality of circuits in the signal path.

Regarding claim 24 of the present application, claim 25 of copending Application No. 15/080,432 encompasses all claimed limitation including a method for reducing power consumption in a receiver in a battery operated mobile device where the receiver receives a wireless signal and comprises a plurality of circuits, the plurality of circuits comprising a signal path including at least an amplifier, a mixer and a filter, and wherein the receiver also comprises circuits for determining at least a signal strength at a one or more locations in the signal path, the method comprising: filtering the received signal to determine a signal strength of a desired signal and a signal strength of an interferer signal; and when the signal strength of the desired signal is greater than the signal strength of the interferer signal, increasing an impedance of at least one of the amplifier, filter or mixer in the signal path of the receiver, thereby reducing power dissipation in the receiver.

Regarding claim 25 of the present application, claim 25 of copending Application No. 15/080,432 encompasses all claimed limitation including a method for reducing power consumption in a receiver in a battery operated mobile device where the receiver receives a wireless signal and comprises a plurality of circuits, the plurality of circuits comprising a signal path including at least an amplifier, a mixer and a filter, and wherein the receiver also comprises circuits for determining signal strengths at a plurality of locations in the signal path, the method comprising: filtering the received signal to determine a signal strength of a desired signal and a signal strength of an interferer signal; and when the signal strength of the interferer signal is greater than the signal

strength of the desired signal, reducing a bias of at least one of the plurality of circuits in the signal path of the receiver, thereby reducing power dissipation in the receiver.

Regarding claim 26 of the present application, claim 25 of copending Application No. 15/080,432 encompasses all claimed limitation including a method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, the method comprising: receiving a wireless signal having a desired signal strength and an interferer signal strength by the receiver, the receiver having a plurality of circuits to function under a worst case condition when a received desired signal strength is low and a received interferer signal strength is high, the receiver having a signal path comprising a plurality of circuits including at least an amplifier, a filter, and a mixer, and wherein the receiver also comprises circuits determining a received desired signal strength and determining a received interferer signal strength; and when the signal strength of the interferer signal is high and the signal strength of the desired signal is high, causing an impedance of one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be increased compared to the worst-case power dissipation condition, thereby saving power.

Regarding claim 27 of the present application, claim 25 of copending Application No. 15/080,432 encompasses all claimed limitation including a a method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, the method comprising: receiving a wireless signal having a desired signal strength and an interferer signal strength by the receiver, the receiver

having a plurality of circuits to function under a worst case condition when a received desired signal strength is low and a received interferer signal strength is high, the receiver having a signal path comprising a plurality of circuits including at least an amplifier, a filter, and a mixer, and wherein the receiver also comprises circuits determining a received desired signal strength and determining a received interferer signal strength; and when the signal strength of the interferer signal is low and the signal strength of the desired signal is low, causing a bias current of one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be decreased compared to the worst-case power dissipation condition, thereby saving power.

Regarding claim 29 of the present application, claim 25 of copending Application No. 15/080,432 encompasses all claimed limitation including a method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, the method comprising: receiving a wireless signal having a desired signal strength and an interferer signal strength by the receiver, the receiver having a plurality of circuits to function under a worst case condition when a received desired signal strength is low and a received interferer signal strength is high, the receiver having a signal path comprising a plurality of circuits including at least an amplifier, a filter, and a mixer, and wherein the receiver also comprises circuits determining a received desired signal strength and determining a received interferer signal strength; and when the signal strength of the interferer signal is low and the signal strength of the desired signal is high, causing an impedance of one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be

increased compared to the worst-case power dissipation condition, thereby saving power.

Regarding claim 30 of the present application, claim 26 of copending Application No. 15/080,432 encompasses all claimed limitation including a method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, the method comprising: receiving a wireless signal having a desired signal strength and an interferer signal strength by the receiver, the receiver having a plurality of circuits to function under a worst case condition when a received desired signal strength is low and a received interferer signal strength is high, the receiver having a signal path comprising a plurality of circuits including at least an amplifier, a filter, and a mixer, and wherein the receiver also comprises circuits determining a received desired signal strength and determining a received interferer signal strength; and when the signal strength of the interferer signal is high and the signal strength of the desired signal is low, and the desired signal has a signal strength that is larger than in the worst- case power dissipation conditions, causing an impedance of one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be increased compared to the worst-case power dissipation condition, causing a reduction in power dissipation.

Regarding claim 31 of the present application, claim 25 of copending Application No. 15/080,432 encompasses all claimed limitation including a method for reducing power consumption in a receiver in a battery operated mobile device where the receiver receives a wireless signal and comprises a plurality of circuits, the plurality of circuits

comprising a signal path including at least an amplifier, a mixer and a filter, and wherein the receiver also comprises circuits for determining a signal strength at least at a location in the signal path, the method comprising: filtering the received signal to determine a signal strength of an interferer signal; and when the signal strength of the interferer signal is high, increasing an impedance of at least one of the plurality of circuits in the signal path of the receiver, thereby reducing power dissipation in the receiver.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to QUOCHIEN B. VUONG whose telephone number is (571)272-7902. The examiner can normally be reached on M-F 9:30-18:00.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nay Maung can be reached on (571) 272-7882. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/QUOCHIEN B VUONG/
Primary Examiner, Art Unit 2647

Notice of References Cited	Application/Control No. 15/824,841	Applicant(s)/Patent Under Reexamination TSIVIDIS, YANNIS	
	Examiner QUOCHIEN B. VUONG	Art Unit 2647	Page 1 of 1

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	15/824,841
	Filing Date	Nov 28, 2017
	First Named Inventor	Yannis Tsividis
	Group Art Unit	2647
	Examiner Name	Quochien Vuong
Sheet 1 of 6	Attorney Docket No: 10037P007CCC	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	15/824,841
	Filing Date	Nov 28, 2017
	First Named Inventor	Yannis Tsividis
	Group Art Unit	
	Examiner Name	
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	15/824,841
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	First Named Inventor	Yannis Tsividis
	Group Art Unit	
	Examiner Name	
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	15/824,841
	Filing Date	Nov 28, 2017
	First Named Inventor	Yannis Tsividis
	Group Art Unit	
	Examiner Name	
Sheet 4 of 6	Attorney Docket No: 10037P007CCC	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	**Cite No [1]**	**Foreign Patent Document** Country Code/Number/Kind Code (if known)	**Publication Date** YYYY-MM-DD	**Name of Patentee or Applicant of cited Document**	**Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear**	**T[2]**
		WO-02/056470	2002-07-18	Palaskas, George et al.		
		WO-02/056558	2002-07-18	Palaskas, George et al.		
		WO-02/35756	2002-05-02	Yoshizawa, Atushi et al.		
		WO-2004/017589	2004-02-24	Palaskas, George et al.		

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	**Cite No [1]**	**Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.**	**T[2]**
		"Office Action Dated April 13, 2018; U.S. Patent Application No. 15/080,432", 4/13/2018	
		"Office Action Dated November 1, 2016; U.S. Patent Application No. 15/080,432", 11/1/2016	
		"Office Action Dated September 6, 2017; U.S. Patent Application No. 15/080,432", 9/6/2017	
		APARIN, VLADIMIR et al., "A Highly-Integrated Tri-Band/Quad-Mode SiGe BiCMOS RF-to-Baseband Receiver for Wireless CDMA/WCDMA/AMPS Applications with GPS Capability", 2002 IEEE International Solid-State Circuits Conference, Session 14, Cellular RF Wireless, 14.3, 2002,	
		BEHBAHANI, FARBOD et al., "A Broad-Band Tunable CMOS Channel-Select Filter for a Low-IF Wireless Receiver", IEEE Journal of Solid-State Circuits, Vol. 35, No. 4, April 2000, Pgs. 476-489	
		BEHBAHANI, FARBOD et al., "Adaptive Analog IF Signal Processor for a Wide-Band CMOS Wireless Receiver", IEEE Journal of Solid-State Circuits, Vol. 36, No. 8, August 2001, Pgs. 1205-1217	
		BEHBAHANI, FARBOD , "An Adaptive Scalable 2.4 GHz Frequency Hopping Receiver for Wideband Wireless LAN", A dissertation submitted in partial satisfaction of the requirements for the degree of Doctor of Philosophy in Electrical Engineering, University of California, Los Angeles, 1999,	
		BEHZAD, ARYA R. et al., "A 5-GHz Direct-Conversion CMOS Transceiver Utilizing Automatic Frequency Control for the IEEE 802.11a Wireless LAN Standard", IEEE Journal of Solid-State Circuits, Vol. 38, No. 12, December 2003, Pgs. 2209-2220	
		CHRISTENSEN, CRAIG L. , "A Low Power, Low Datarate Integrated 433MHz Wireless Transceiver in CMOS", Proceedings of the 15th Biennial University/Government/Industry Microelectronics Symposium, 2003, pp. 70-73	

EXAMINER /QUOCHIEN B VUONG/ **DATE CONSIDERED** 07/06/2018

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449) as modified by BSTZ 03/26/07

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional) [2] Applicant is to place a check mark here if English language Translation is attached

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /Q.B.V/

Substitute for form 1449A/PTO	*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	15/824,841
	Filing Date	Nov 28, 2017
	First Named Inventor	Yannis Tsividis
	Group Art Unit	
	Examiner Name	
Sheet 5 of 6	Attorney Docket No: 10037P007CCC	

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	**Cite No [1]**	**Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.**	**T[2]**
		DASGUPTA, UDAY et al., "A CMOS Transmit/Receive IF Chip-Set for WCDMA Mobiles", 2002 IEEE Radio Frequency Integrated Circuits Symposium, MO4A-4, 2002, pp. 195-198	
		GRAY, P. R. et al., "Future Directions in Silicon ICs for RF Personal Communications", IEEE 1995 Custom Integrated Circuits Conference, 1995, Pgs. 83-90	
		HOLLMAN, TUOMAS et al., "A 2.7-V CMOS Dual-Mode Baseband Filter for PDC and WCDMA", IEEE Journal of Solid-State Circuits, Vol. 36, No. 7, July 2001, Pgs. 1148-1153	
		LEE, KANG-YOON et al., "Full-CMOS 2-GHz WCDMA Direct Conversion Transmitter and Receiver", IEEE Journal of Solid-State Circuits, Vol. 38, No. 1, January 2003, pp. 43-53	
		LEUNG, VINCENT et al., "Digital-IF WCDMA Handset Transmitter IC in 0.25um SiGe BiCMOS", 2004 IEEE International Solid-State Circuits Conference, 2004, Pgs. 182-183	
		ORSATTI, PAOLO et al., "A 20-mA-Receive, 55-mA-Transmit, Single-Chip GSM Transceiver in 0.25-µm CMOS", IEEE Journal of Solid-State Circuits, Vol. 34, No. 12, December 1999, pp. 1869-1880	
		PARSSINEN, AARNO et al., "A 2-GHz Wide-Band Direct Conversion Receiver for WCDMA Applications", IEEE Journal of Solid-State Circuits, Vol. 34, No. 12, December 1999, Pgs. 1893-1903	
		REYNOLDS, S et al., "A Direct-Conversion Receiver IC for WCDMA Mobile Systems", Proceedings of the 2002 Bipolar/BiCMOS Circuits and Technology Meeting, 2002, pp. 61-64	
		RUDELL, JACQUES C. et al., "Recent Developments in High Integration Multi-Standard CMOS Transceivers for Personal Communication Systems", Proceedings of the 1998 International Symposium on Low Power Electronics and Design, Aug. 10-12, 1998, pp. 149-154	
		RYYNANEN, JUSSI et al., "RF Gain Control in Direct Conversion Receivers", IEEE, 2002, Pgs. IV-117 - IV-120	
		SANIELEVICI, SERGIO A. et al., "A 900-MHz Transceiver Chipset for Two-Way Paging Applications", IEEE Journal of Solid-State Circuits, Vol. 33, No. 12, December 1998, pp. 2160-2168	
		SCHUCHTER, WALTER et al., "A Single Chip FSK/ASK 900MHz Transceiver in a Standard 0.25um CMOS Technology", 2001 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, 2001, pp. 183-186	

EXAMINER	/QUOCHIEN B VUONG/	**DATE CONSIDERED**	07/06/2018

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449) as modified by BSTZ 03/26/07

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /Q.B.V/

Substitute for form 1449A/PTO	*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	15/824,841
	Filing Date	Nov 28, 2017
	First Named Inventor	Yannis Tsividis
	Group Art Unit	
	Examiner Name	
Sheet 6 of 6	Attorney Docket No: 10037P007CCC	

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	**Cite No [1]**	**Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.**	**T[2]**
		TADJPOUR, SHAHRZAD , "A 900 MHz Dual Conversion, Low-IF CMOS GSM Receiver", A dissertation submitted in partial satisfaction of the requirements for the degree Doctor of Philosophy in Electrical Engineering, University of California, Los Angeles, 2001,	
		TASIC, ALEKSANDAR et al., "Concept of Frequency-Transconductance Tuning of Bipolar Voltage-Controlled Oscillators", IEEE, 2002, Pgs. III-555 - III-558	
		TASIC, ALEKSANDAR et al., "Concept of Phase-Noise Tuning of Bipolar Voltage-Controlled Oscillators", IEEE, 2002, Pgs. V-161 - V-164	
		TSIVIDIS, Y , "Minimising power dissipation in analogue signal processors through syllabic companding", Electronic Letters, Vol. 35, No. 21, October 14, 1999, Pgs. 1805-1807	
		TSIVIDIS, Y. et al., "Internally Varying Analog Circuits Minimize Power Dissipation", IEEE Circuits & Devices Magazine, January 2003, Pgs. 63-72	
		VAN DEN BOS, CHRIS et al., "Architecture of a reconfigurable radio receiver front-end using overall feedback", Electronics Research Laboratory, Delft University of Technology, 2001,	
		XIONG, WEI et al., "An S-band Low-Noise Amplifier with Self-Adjusting Bias for Improved Power Consumption and Dynamic Range in a Mobile Environment", 1999 IEEE Radio Frequency Integrated Circuits Symposium, TUE5-4, 1999, pp. 193-196	
		YOSHIZAWA, ATSUSHI et al., "An Anti-Blocker Structure MOSFET-C Filter For a Direct Conversion Receiver", IEEE 2001 Custom Integrated Circuits Conference, 2001, Pgs. 5-8	
		ZARGARI, MASOUD et al., "A Single-Chip Dual-Band Tri-Mode CMOS Transceiver for IEEE 802.11a/b/g WLAN", 2004 IEEE International Solid-State Circuits Conference, 2004, Pgs. 96-97	

EXAMINER	/QUOCHIEN B VUONG/	**DATE CONSIDERED**	07/06/2018

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449) as modified by BSTZ 03/26/07

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	6524	((RSSI (signal adj2 (strength level quality))) same ((chang$3 varr$4 adjust$3 increas$3 decreas$3) with impedance)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/07/06 18:23
L3	112	2 same (gain (bias near4 current)) same ((low lower less reduc$3) near4 (power battery))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/07/06 18:30
L4	38318	455/63.1,67.13,127.1,127.2,127.5,226.1,226.2,232.1,234.1,250.1,251.1,295,296,311,343.1,572,574.ccls. 370/442.ccls. 330/127,134,144.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/07/06 18:35
L5	226	2 and 4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/07/06 18:35
L6	421	2 same ((low lower less reduc$3) near4 (power battery))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/07/06 19:04
L7	285	2 AND ((H03F2200/451 OR H03F2200/387 OR H03F1/56 OR H03F2200/27 OR H03F2200/78 OR H03F3/20 OR H04B17/318 OR H04B1/16 OR H04B1/1607 OR H04B1/40 OR H04W52/52).CPC.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/07/06 19:17
L10	8	"5001776".pn. "6870425".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/07/06 20:04

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L8	9208	"2" AND ((H03F2200/451 OR H03F2200/387 OR H03F1/56 OR H03F2200/27 OR H03F2200/78 OR H03F3/20 OR H04B17/318 OR H04B1/16 OR H04B1/1607 OR H04B1/40 OR H04W52/52).CPC.)	USPAT	OR	ON	2018/07/06 19:47
L9	73	tsividis-yannis.in.	US-PGPUB; USPAT	OR	ON	2018/07/06 19:48

7/6/2018 8:05:46 PM

IPR2024-00818
Apple EX1002 Page 136

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15824841	TSIVIDIS, YANNIS
	Examiner	Art Unit
	QUOCHIEN B VUONG	2647

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	07/06/2018								
	1	-								
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	28	✓								
	29	✓								
	30	✓								
	31	✓								

IPR2024-00818
Apple EX1002 Page 137

Bibliographic Data

Application No: 15/824,841

Foreign Priority claimed: ○ Yes ◉ No

35 USC 119 (a-d) conditions met: ☐ Yes ☑ No ☐ Met After Allowance

Verified and Acknowledged: /QUOCHIEN B VUONG/ (Examiner's Signature) | (Initials)

Title: Power Dissipation Reduction in Wireless Transceivers

FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
11/28/2017	455	2647	10037P007CCC
RULE			

APPLICANTS

Theta IP, LLC, Coppell, TX, UNITED STATES

INVENTORS

Yannis Tsividis New York, NY, UNITED STATES

CONTINUING DATA

This application is a CON of 15080421 03/24/2016 PAT 9838962

15080421 is a CON of 11318646 12/27/2005 PAT 9331728

11318646 is a CON of 10784613 02/23/2004 PAT 7010330

10784613 has PRO of 60451230 03/01/2003

10784613 has PRO of 60451229 03/01/2003

FOREIGN APPLICATIONS

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12/11/2017

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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15824841	TSIVIDIS, YANNIS
	Examiner	Art Unit
	QUOCHIEN B VUONG	2647

CPC- SEARCHED		
Symbol	Date	Examiner
H04B 1/16, 1/1607, 1/40, 17/318	07/06/2018	/QV/
H04W 52/52	07/06/2018	/QV/
H03F 1/56, 3/20, 2200/27, 2200/78, 2200/387, 2200/451	07/06/2018	/QV/

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
455	63.1,67.13,127.1,127.2,127.5,226.1,226.2,232.1,234.1,250.1,251.1,295,296,311,343.1,572,574	07/06/2018	/QV/
370	442	0706/2018	/QV/
330	127,134,144	07/06/2018	/QV/

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

SEARCH NOTES		
Search Notes	Date	Examiner
EAST search	07/06/2018	/QV/
Inventor name search	07/06/2018	/QV/

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

Substitute for form 1449A/PTO	*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	15/824,841
	Filing Date	Nov 28, 2017
	First Named Inventor	Yannis Tsividis
	Group Art Unit	2647
	Examiner Name	Vuong, Quochien B
Sheet 1 of 1	Attorney Docket No: 10037P007CCC	

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		"Notice of Allowance Dated July 18, 2018; U.S. Patent Application No. 15/080,432", 7/18/2018	

EXAMINER **DATE CONSIDERED**

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Electronic Acknowledgement Receipt

EFS ID:	34027461
Application Number:	15824841
International Application Number:	
Confirmation Number:	4819
Title of Invention:	Power Dissipation Reduction in Wireless Transceivers
First Named Inventor/Applicant Name:	Yannis Tsividis
Customer Number:	8791
Filer:	Tri Cao Dang/Jessica Clark
Filer Authorized By:	Tri Cao Dang
Attorney Docket Number:	10037P007CCC
Receipt Date:	16-OCT-2018
Filing Date:	28-NOV-2017
Time Stamp:	16:48:34
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	10037P007CCC_20181016_IDS Letter.pdf	154339 a2b2add9ce309c12631744 2e67612b6a0a5c8812	no	1
Warnings:					

Information:					
2	Information Disclosure Statement (IDS) Form (SB08)	10037P007CCC_20181016_IDS.pdf	164801 9723305a22407c7c5cd11f5f260fcb13e5f7e8b3	no	1
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
3	Other Reference-Patent/App/Search documents	10037P007CC2_20180718_NOA.pdf	353954 1ab7b275e905df93e452f2648508406a1e222fec	no	5
Warnings:					
Information:					
		Total Files Size (in bytes):	673094		

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<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application No.	15/824,841
Filing Date	November 28, 2017
First Inventor	Yannis Tsividis
Art Unit	2647
Examiner Name	Vuong, Quochien B
Attorney Docket No.	10037P007CCC Conf. No. 4819

DUTY OF DISCLOSURE STATEMENT

In accordance with the duty of disclosure, enclosed is a copy of an Information Disclosure Statement (IDS) Citation Form PTO/SB/08 or PTO-1449, together with copies of the documents cited on that form, except for copies not required to be submitted (e.g., copies of U.S. patents and U.S. published patent applications need not be enclosed). This IDS and IDS Citation Form are being submitted before the mailing of a final Office Action or Notice of Allowance. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

The submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☒ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

OR

☐ None

☐ The IDS Filing Fee in the amount of $120.00 as set forth in 37 CFR 1.17(p) has been submitted herewith.

☒ It is requested that any requisite fees be debited from Deposit Account 090528.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of signature.

Signature	/ Tri C. Dang /	Date (MM-DD-YYYY)	10-16-2018
Name/Print	Tri C. Dang	Registration Number	71853

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.

Jessica A. Clark /Jessica A. Clark/ *Date* *10-16-18*

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Document Description: Power of Attorney

PTO/AIA/82A (07-13)
Approved for use through 11/30/2014. OMB 0651-0051
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Application Number	15/824,841
Filing Date	November 28, 2017
First Named Inventor	Yannis TSIVIDIS
Title	POWER DISSIPATION REDUCTION IN WIRELESS TRANCEIVERS
Art Unit	2467
Examiner Name	Quochien B. VUONG
Attorney Docket Number	THETA-000002US00

SIGNATURE of Applicant or Patent Practitioner

Signature	/Jennifer Hayes/	Date (Optional)	
Name	Jennifer Hayes	Registration Number	50,845
Title (if Applicant is a juristic entity)			
Applicant Name (if Applicant is a juristic entity)			

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.

☑ *Total of 2 forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Application Number	Filing Date

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I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

THETA IP, LLC

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☑ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

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SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature		Date (Optional)	
Name	Demetris Paraskevopoulos		
Title	CEO, Theta IP, LLC		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☑ Total of 2 forms are submitted.

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Electronic Acknowledgement Receipt

EFS ID:	34843396
Application Number:	15824841
International Application Number:	
Confirmation Number:	4819
Title of Invention:	Power Dissipation Reduction in Wireless Transceivers
First Named Inventor/Applicant Name:	Yannis Tsividis
Customer Number:	8791
Filer:	Jennifer NMN Hayes/Cristene Amador
Filer Authorized By:	Jennifer NMN Hayes
Attorney Docket Number:	10037P007CCC
Receipt Date:	14-JAN-2019
Filing Date:	28-NOV-2017
Time Stamp:	12:46:10
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	POA_084820-002US0.pdf	2906163 35b1007ea0e944526ce292e7dd1f3f431fbd b93b	no	3

Warnings:

Information:	
Total Files Size (in bytes):	2906163

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National Stage of an International Application under 35 U.S.C. 371

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New International Application Filed with the USPTO as a Receiving Office

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PTO/SB/06 (09-11)
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 15/824,841	Filing Date 11/28/2017	☐ To be Mailed

ENTITY: ☐ LARGE ☑ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

	(Column 1)	(Column 2)			
FOR	NUMBER FILED	NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $40 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $210 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	01/17/2019	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 18	Minus	** 20	= 0		x $50 =	0
	Independent (37 CFR 1.16(h))	* 10	Minus	*** 11	= 0		x $230 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/STEPHEN W HOOVER/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Yannis TSIVIDIS	Confirmation No.:	4819
Application No.:	15/824,841	Examiner:	Quochien B. VUONG
Filing Date:	November 28, 2017	Art Unit:	2647
Title:	Power Dissipation Reduction in Wireless Transceivers		

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT AND RESPONSE TO OFFICE ACTION

Sir:

In response to the Office Action mailed July 18, 2018, please enter the following amendments and consider the accompanying remarks.

Amendments to the Claims, if any, are reflected in the Listing of Claims beginning on page **2**.

Remarks begin on page **11**.

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Amendments to the Claims

The following Listing of Claims replaces all prior versions in the application:

1-20. (Cancelled)

21. (Currently Amended) A method of reducing the power consumption of a receiver of a battery operated transceiver having a plurality of circuits, wherein the plurality of circuits comprise a receiver signal path comprising at least an amplifier, a mixer and a filter, the plurality of circuits further comprise circuits for determining at least a signal strength indication in the signal path of the receiver; the method comprising:

receiving a signal comprising a desired signal and an interferer signal in the receiver signal path ~~of the receiver~~;

determining a first signal strength indication, wherein the first signal strength indication is relative to the strength of the received signal;

determining a second signal strength indication, wherein the second signal strength indication is relative to the strength of the signal after filtering the received signal to reduce the interferer signal;

comparing the first and second signal strength indication to one another, and

adjusting at least one of an impedance, a bias or a gain of at least one of the amplifier, filter or mixer in the receiver signal path, responsive to ~~the~~ relative changes in the strength of the first and second signal strength indication ~~as below:~~

~~when the second signal strength indication increases, increasing the impedance of at least one of the plurality of circuits in the signal path.~~

22. (Currently Amended) The method of claim 21, ~~A method of reducing the power consumption of a receiver of a battery operated transceiver having a plurality of circuits, wherein the plurality of circuits comprise a receiver signal path comprising at least an amplifier, a mixer and a filter, the plurality of circuits further comprising circuits for determining at least a signal strength indication in the signal path of the receiver; the method comprising:~~

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~~receiving a signal comprising a desired signal and an interferer signal in the signal path of the receiver;~~

~~determining a first signal strength indication, wherein the first signal strength indication is relative to the strength of the received signal;~~

~~determining a second signal strength indication, wherein the second signal strength indication is relative to the strength of the signal after filtering the received signal to reduce the interferer signal;~~

~~comparing the first and second signal strength indication to determine a signal strength indication of a desired signal and a signal strength indication of an interferer signal; and~~

wherein when the indicated interferer signal strength decreases, and the indicated strength of the desired signal decreases, decreasing the bias of at least one of the plurality of circuits in the signal path.

23. (Currently Amended) ~~A method of reducing the power consumption of a receiver of a battery operated transceiver having a plurality of circuits, wherein the plurality of circuits comprise a receiver signal path comprising at least an amplifier, a mixer and a filter, the plurality of circuits further comprising circuits for determining at least a signal strength indication in the signal path of the receiver; the method comprising:~~

~~receiving a signal comprising a desired signal and an interferer signal in the signal path of the receiver;~~

~~determining a first signal strength indication, wherein the first signal strength indication is relative to the strength of the received signal;~~

~~determining a second signal strength indication, wherein the second signal strength indication is relative to the strength of the signal after filtering the received signal to reduce the interferer signal;~~

~~comparing the first and second signal strength indications to determine a signal strength indication of the desired signal and a signal strength indication of the interferer signal; and~~The method of claim 21, wherein when the indicated interferer signal strength decreases, and the indicated strength of the desired signal decreases, increasing a gain of at least one of a plurality of circuits in the signal path and increasing an impedance of at least one of the plurality of circuits in the signal path.

24. (Currently Amended) A method for reducing power consumption in a receiver in a battery operated mobile device where the receiver receives a wireless signal and comprises a plurality of circuits, the plurality of circuits comprising a signal path including at least an amplifier, a mixer and a filter, and wherein the receiver also comprises circuits for determining at least a signal strength at a one or more locations in the signal path, the method comprising:

filtering the received signal to determine a signal strength of a desired signal and a signal strength of an interferer signal;

comparing the signal strength of the desired signal to the signal strength of the interferer signal; and

when the signal strength of the desired signal is greater than the signal strength of the interferer signal, increasing an impedance of at least one of the amplifier, filter or mixer in the signal path of the receiver, thereby reducing power dissipation in the receiver.

25. (Currently Amended) A method for reducing power consumption in a receiver in a battery operated mobile device where the receiver receives a wireless signal and comprises a plurality of circuits, the plurality of circuits comprising a signal path including at least an amplifier, a mixer and a filter, and wherein the receiver also comprises circuits for determining signal strengths at a plurality of locations in the signal path, the method comprising:

filtering the received signal to determine a signal strength of a desired signal and a signal strength of an interferer signal;

comparing the signal strength of the desired signal to the signal strength of the interferer signal; and

when the signal strength of the interferer signal is ~~greater~~ smaller than the signal strength of the desired signal, reducing a bias of at least one of the plurality of circuits in the signal path of the receiver, thereby reducing power dissipation in the receiver.

26. (Currently Amended) A method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, the receiver having a signal path comprising a plurality of circuits including at least an amplifier, a filter, and a mixer, the receiver having a plurality of circuits to function under a worst-case condition when a received

desired signal strength is low and a received interferer signal strength is high, the method comprising:

receiving a wireless signal having a desired signal strength and an interferer signal strength by the receiver;, the receiver having a plurality of circuits to function under a worst case condition when a received desired signal strength is low and a received interferer signal strength is high; , the receiver having a signal path comprising a plurality of circuits including at least an amplifier, a filter, and a mixer, and wherein the receiver also comprises circuits

determining a the received desired signal strength;

and determining a the received interferer signal strength;

comparing the received desired signal strength relative to the received interferer signal strength; and

when the interferer signal strength of the interferer signal is high and the desired signal strength of the desired signal is high, causing an impedance of one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be increased compared relative to the impedance at the worst-case power dissipation condition, thereby saving power.

27. (Currently Amended) A method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, the receiver having a signal path comprising a plurality of circuits including at least an amplifier, a filter, and a mixer, the receiver having a plurality of circuits to function under a worst case condition when a received desired signal strength is low and a received interferer signal strength is high, the method comprising:

receiving a wireless signal having a desired signal strength and an interferer signal strength by the receiver, the receiver having a plurality of circuits to function under a worst case condition when a received desired signal strength is low and a received interferer signal strength is high;, the receiver having a signal path comprising a plurality of circuits including at least an amplifier, a filter, and a mixer, and wherein the receiver also comprises circuits

-determining a received desired signal strength;

and determining a received interferer signal strength;

comparing the received desired signal strength relative to the received interferer signal strength; and

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when the interferer signal strength ~~of the interferer signal~~ is low and the desired signal strength ~~of the desired signal~~ is low, causing a bias current of one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be decreased ~~compared~~ relative to the worst-case ~~power dissipation~~ condition, thereby saving power.

28. (Cancelled)

29. (Currently Amended) A method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, the receiver having a plurality of circuits to function under a worst case condition when a received desired signal strength is low and a received interferer signal strength is high, the receiver having a signal path comprising a plurality of circuits including at least an amplifier, a filter, and a mixer, the method comprising:

receiving a wireless signal having a desired signal strength and an interferer signal strength by the receiver; ~~, the receiver having a plurality of circuits to function under a worst case condition when a received desired signal strength is low and a received interferer signal strength is high, the receiver having a signal path comprising a plurality of circuits including at least an amplifier, a filter, and a mixer, and wherein the receiver also comprises circuits~~

determining a received desired signal strength ~~and~~ ;

determining a received interferer signal strength;

comparing the desired signal strength relative to the interferer signal strength; and

when the ~~signal strength of the~~ interferer signal strength is low and the desired signal strength ~~of the desired signal~~ is high, causing an impedance of one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be increased ~~compared~~ relative to the worst-case ~~power dissipation~~ condition, thereby saving power.

30. (Currently Amended) A method for power dissipation ~~reduction~~ control in a receiver of a wireless transceiver of a battery powered portable wireless device, the receiver having a signal path comprising a plurality of circuits including at least an amplifier, a filter, and a mixer, the method comprising:

receiving a wireless signal having a desired signal strength and an interferer signal strength by the receiver; ~~, the receiver having a plurality of circuits to function under a worst case~~

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~~condition when a received desired signal strength is low and a received interferer signal strength is high, the receiver having a signal path comprising a plurality of circuits including at least an amplifier, a filter, and a mixer, and wherein the receiver also comprises circuits~~

determining ~~a~~ the received desired signal strength; ~~and~~

determining ~~a~~ the received interferer signal strength;

comparing the received desired signal strength relative to the received interferer signal strength; and

when the ~~signal strength of the~~ received interferer signal strength is high and the received desired signal strength ~~of the desired signal~~ is low, ~~and the desired signal has a signal strength that is larger than in the worst-case power dissipation conditions~~, causing ~~an impedance~~ a bias current of one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be increased ~~compared to the worst-case power dissipation condition~~, causing an ~~reduction~~ increase in power dissipation.

31. (Currently Amended) A method for ~~reducing~~ power consumption control in a receiver in a battery operated mobile device where the receiver receives a wireless signal and comprises a plurality of circuits, the plurality of circuits comprising a signal path including at least an amplifier, a mixer and a filter, and wherein the receiver also comprises circuits for determining a signal strength at least at a location in the signal path, the method comprising:

filtering the received signal to determine a signal strength of an interferer signal and a signal strength of a desired signal; and

when the signal strength of the interferer signal is ~~high~~increasing, increasing ~~an impedance~~ a bias current of at least one of the plurality of circuits in the signal path of the receiver, thereby ~~reducing~~ increasing power dissipation in the receiver.

32. (New) A method for power dissipation optimization in a receiver of a wireless transceiver of a battery powered portable wireless device based on its operating conditions, wherein the receiver has a signal path comprising a plurality of circuits including at least an amplifier, a filter, and a mixer, the receiver having a plurality of circuits designed to function under operating conditions that vary based on relative signal strengths of the interferer signal and desired signal, wherein operating conditions vary between a worst-case operating condition and a

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best-case operating condition, wherein the worst-case operating condition occurs when a desired signal strength is low and an interferer signal strength is high and the receiver operates with a maximum bias current, wherein the best-case operating condition occurs when the desired signal strength is high and the interferer signal strength is very low or zero and the receiver operates with a minimum bias current, the method comprising:

receiving a wireless signal having a desired signal and an interferer signal by the receiver;

determining the received desired signal strength;

determining the received interferer signal strength;

comparing the received desired signal strength relative to the received interferer signal strength;

when the received desired signal strength relative to the received interferer signal strength is better than that the worst-case operating condition, reducing a bias current of one or more of the plurality of circuits in the signal path of the receiver, thereby reducing power dissipation and saving power.

33. (New) The method of claim 32, wherein the received desired signal strength relative to the received interferer signal strength is better than that the worst-case operating condition when the received desired signal strength is higher than the desired signal strength at the worst-case operating condition.

34. (New) The method of claim 32, wherein the received desired signal strength relative to the received interferer signal strength is better than that the worst-case operating condition when the received interfere signal strength is lower than the interferer signal strength at the worst case operating condition.

35. (New) The method of claim 32, wherein the received desired signal strength relative to the received interferer signal strength is better than that the worst-case operating condition when the received desired signal strength is higher than the desired signal strength of the worst-case operating condition and the received interferer signal strength is lower than the interferer signal strength at the worst case operating condition.

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36. (New) The method of claim 32, wherein the interferer signal is due to other transceivers or nearby electronic equipment generating interfering signals and other spurious noise.

37. (New) The method of claim 31, wherein the filtering the received signal to determine a signal strength of an interferer signal and a signal strength of a desired signal occurs over a period of time and further comprising comparing the signal strength of the interferer signal at a first period of time to the signal strength of the interferer signal at a second period of time to determine whether the signal strength of the interferer signal is increasing.

38. (New) A method for power dissipation control in a receiver of a wireless transceiver of a battery powered portable wireless device, the receiver having a signal path comprising a plurality of circuits including at least an amplifier, a filter, and a mixer, the method comprising:

receiving a wireless signal having a desired signal strength and an interferer signal strength by the receiver;

determining the received desired signal strength;

determining the received interferer signal strength;

comparing the received desired signal strength relative to the received interferer signal strength; and

when the received interferer signal strength is greater than the received desired signal strength, increasing a bias current of at least one of the plurality of circuits in the receiver signal path of the wireless transceiver, causing an increase in power dissipation.

39. (New) A method for controlling power dissipation in a receiver of a wireless transceiver of a battery powered portable wireless device, the receiver having a signal path comprising a plurality of circuits including at least an amplifier, a filter, and a mixer, the method comprising:

receiving a wireless signal having a desired signal strength and an interferer signal strength by the receiver;

determining the received desired signal strength;

determining the received interferer signal strength;

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comparing the received desired signal strength relative to the received interferer signal strength; and

wherein when the received desired signal strength is greater than the received interferer signal strength, decreasing a bias current of at least one of the plurality of circuits in the signal path.

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REMARKS

The Office Action mailed July 18, 2018 has been carefully considered. In this Amendment, claim 28 has been cancelled, claims 21-27, and 29-31 have been amended, and claims 32-39 have been added. Reconsideration in view of the following remarks is respectfully requested.

Rejection(s) Under 35 U.S.C. § 112, Second Paragraph

Claims 26-30 stand rejected under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. These rejections are traversed. Applicants have amended claims 26-27 and 29-30 and cancelled claim 28. Applicant accordingly requests withdrawal of the rejections under 35 U.S.C. § 112, second paragraph.

Rejection(s) under 35 U.S.C. § 103

Claims 21-31 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over U.S. Patent No. 5,001,776 to Clark (hereinafter, "Clark") in view of U.S. Patent No. 6,870,425 to Leifso et al. (hereinafter, "Leifso"). These rejections are traversed.

Clark generally discloses a method of controlling the power consumption of a receiver (of a transceiver) based on the level of the desired signal and the level of all signals received. However, Clark specifically discloses that a "first threshold" and a "second threshold" are used for controlling the power consumption of the receiver. See, for example, Fig. 2 and Claim 1 of Clark. In Clark, the desired signal is compared to the first threshold, which is determined after the received signal has been mixed. The received signal is compared to the second threshold,

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which is determined before the signal has been mixed. Additionally, in Clark, since each threshold causes two outcomes (high or low), there are four total outcomes of this controlling method, as shown in TABLE 1 of Clark. Thus, in Clark, there are only two Operating Mode Currents: High and Low. This is confirmed by Fig. 2 of Clark, which shows only a Low Current Mode and a High Current Mode.

The presently pending claims do not rely on a comparison of the desired and undesired (interferer) signals to thresholds; instead, in the method of claims 21-27 and 29-30, the receiver dynamically adjusts impedance or bias based on the relative comparison of the desired signal strength to the interferer signal strength. This allows for the receiver to operate at more than two operating mode currents, i.e., there are many more than four outcomes as described in Clark.

The Examiner admits that Clark fails to disclose the last limitation of each of the claims. See Office Action, pp. 4 – 15. The examiner points to Leifso as disclosing those limitations. Leifso generally describes a method for amplifier gain control. Leifso, however, does not disclose performing a comparison of desired signal strength and interferer signal strength or adjusting gain based on such a comparison. Accordingly, Leifso in combination with Clark fails to disclose all of the limitations of the claims.

Claim 31 differs from Clark in that the method requires increasing a bias current of at least one of the plurality of circuits in the signal path of the receiver, thereby increasing power dissipation in the receiver, when the signal strength of the interferer signal is *increasing*. As discussed above, Clark does not perform its control based on whether an interferer signal is increasing; it only does it based on a comparison of the pre-mixing and post-mixing signals to a threshold.

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Thus, the cited art fails to disclose all of the limitations of independent claims 21-27 and 29-32. Claims 33-36 depend, directly or indirectly, from one of the foregoing independent claims. Applicant accordingly requests withdrawal of the rejections under 35 U.S.C. § 102 and/or 35 U.S.C. § 103.

Double Patenting Rejections

Claims 21, 22, 24, 27, 29 and 31 stand rejected pursuant to the judicially-created doctrine of obviousness-type double patenting as allegedly being unpatentable over claim 1 of prior U.S. Patent No. 9,838,962. Claims 21, 24, 26 and 29-31 stand rejected pursuant to the judicially-created doctrine of obviousness-type double patenting as allegedly being unpatentable over claim 2 of prior U.S. Patent No. 9,331,728. Claims 21-31 stand rejected pursuant to the judicially-created doctrine of obviousness-type double patenting as allegedly being unpatentable over claims 17, 19, 21, 22 and 26-28 of prior U.S. Patent No. 7,010,330. Claims 21, 22, 24-27 and 29-31 stand rejected pursuant to the judicially-created doctrine of obviousness-type double patenting as allegedly being unpatentable over claims 25 and 26 of prior U.S. Application No. 15/080,432.

Applicants submit herewith a Terminal Disclaimer to overcome said double patenting rejections if the Examiner finds the subject matter of the claims allowable. Applicants accordingly request withdrawal of the double patenting rejections.

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New Claims

Claims 32-38 have been added to further particularly point out and distinctly claim the subject matter regarded as the invention and are patentable for at least the same reasons discussed above.

CONCLUSION

In view of the preceding discussion, Applicant respectfully urges that the claims of the present application define patentable subject matter and should be passed to allowance.

If the Examiner believes that a telephone call would help advance prosecution of the present invention, the Examiner is kindly invited to call the undersigned attorney at the number below.

The Commissioner is authorized to charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 50-4166.

Respectfully submitted,
NIXON PEABODY LLP

Dated: January 17, 2019

/Jennifer Hayes/
Jennifer Hayes
Reg. No. 50,845

ONE CALIFORNIA PLAZA
300 SOUTH GRAND AVENUE, SUITE 4100
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PHONE: (213) 629-6000
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Apple EX1002 Page 163

Electronic Patent Application Fee Transmittal

Application Number:	15824841
Filing Date:	28-Nov-2017
Title of Invention:	Power Dissipation Reduction in Wireless Transceivers
First Named Inventor/Applicant Name:	Yannis Tsividis
Filer:	Jennifer NMN Hayes/Diana Girgis
Attorney Docket Number:	THETA-000002US00

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension - 3 months with $0 paid	2253	1	700	700
Miscellaneous:				
		Total in USD ($)		**700**

Electronic Acknowledgement Receipt	
EFS ID:	34891149
Application Number:	15824841
International Application Number:	
Confirmation Number:	4819
Title of Invention:	Power Dissipation Reduction in Wireless Transceivers
First Named Inventor/Applicant Name:	Yannis Tsividis
Customer Number:	106303
Filer:	Jennifer NMN Hayes/Diana Girgis
Filer Authorized By:	Jennifer NMN Hayes
Attorney Docket Number:	THETA-000002US00
Receipt Date:	17-JAN-2019
Filing Date:	28-NOV-2017
Time Stamp:	18:07:38
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$700
RAM confirmation Number	011819INTEFSW00018573504166
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		2019-01-17-Response-to-OA-Amendment-084820-002US00.pdf	134799 8a46e7ab95fdf9e99e6b8a735b8f62dc55e45f48	yes	14

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Claims	2	10
	Applicant Arguments/Remarks Made in an Amendment	11	14

Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30603 71da8680769812f9f0a8234b90c12d9319d19f11	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	165402		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc Code: DIST.E.FILE **Document Description: Electronic Terminal Disclaimer - Filed**	PTO/SB/25 PTO/SB/26 U.S. Patent and Trademark Office Department of Commerce

Electronic Petition Request	**TERMINAL DISCLAIMER TO OBVIATE A PROVISIONAL DOUBLE PATENTING REJECTION OVER A PENDING "REFERENCE" APPLICATION AND TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT**
Application Number	15824841
Filing Date	28-Nov-2017
First Named Inventor	Yannis Tsividis
Attorney Docket Number	THETA-000002US00
Title of Invention	Power Dissipation Reduction in Wireless Transceivers

☒ Filing of terminal disclaimer does not obviate requirement for response under 37 CFR 1.111 to outstanding Office Action

☒ This electronic Terminal Disclaimer is not being used for a Joint Research Agreement.

Owner	Percent Interest
Theta IP, LLC	100 %

The owner(s) of percent interest listed above in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of any patent granted on pending reference Application Number(s)

15080432 filed on 03/24/2016

as the term of any patent granted on said reference application may be shortened by any terminal disclaimer filed prior to the grant of any patent on the pending reference application. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and any patent granted on the reference application are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the owner does not disclaim the terminal part of any patent granted on the instant application that would extend to the expiration date of the full statutory term of any patent granted on said reference application, "as the term of any patent granted on said reference application may be shortened by any terminal disclaimer filed prior to the grant of any patent on the pending reference application," in the event that any such patent granted on the pending reference application: expires for failure to pay a maintenance fee, is held unenforceable, is found invalid by a court of competent jurisdiction, is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321, has all claims canceled by a reexamination certificate, is reissued, or is in any manner terminated prior to the expiration of its full statutory term as shortened by any terminal disclaimer filed prior to its grant.

The owner(s) with percent interest listed above in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of prior patent number(s)

9838962

9331728

7010330

as the term of said prior patent is presently shortened by any terminal disclaimer. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the prior patent are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the owner does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the prior patent, "as the term of said prior patent is presently shortened by any terminal disclaimer," in the event that said prior patent later:
- expires for failure to pay a maintenance fee;
- is held unenforceable;
- is found invalid by a court of competent jurisdiction;
- is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
- has all claims canceled by a reexamination certificate;
- is reissued; or
- is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

(●) Terminal disclaimer fee under 37 CFR 1.20(d) is included with Electronic Terminal Disclaimer request.

( ) I certify, in accordance with 37 CFR 1.4(d)(4), that the terminal disclaimer fee under 37 CFR 1.20(d) required for this terminal disclaimer has already been paid in the above-identified application.

Applicants claims the following fee status:

(●) Small Entity

( ) Micro Entity

( ) Regular Undiscounted

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

THIS PORTION MUST BE COMPLETED BY THE SIGNATORY OR SIGNATORIES

I certify, in accordance with 37 CFR 1.4(d)(4) that I am:

(●) An attorney or agent registered to practice before the Patent and Trademark Office who is of record in this application

Registration Number 50845

( ) A sole inventor

( ) A joint inventor; I certify that I am authorized to sign this submission on behalf of all of the inventors as evidenced by the power of attorney in the application

( ) A joint inventor; all of whom are signing this request

Signature	/Jennifer Hayes/

Name	Jennifer Hayes

*Statement under 37 CFR 3.73(b) is required if terminal disclaimer is signed by the assignee (owner).
Form PTO/SB/96 may be used for making this certification. See MPEP § 324.

Electronic Patent Application Fee Transmittal

Application Number:	15824841
Filing Date:	28-Nov-2017
Title of Invention:	Power Dissipation Reduction in Wireless Transceivers
First Named Inventor/Applicant Name:	Yannis Tsividis
Filer:	Jennifer NMN Hayes/Diana Girgis
Attorney Docket Number:	THETA-000002US00

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
STATUTORY OR TERMINAL DISCLAIMER	2814	1	160	160
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**160**

Doc Code: DISQ.E.FILE
Document Description: Electronic Terminal Disclaimer – Approved

Application No.: 15824841

Filing Date: 28-Nov-2017

Applicant/Patent under Reexamination: Tsividis

Electronic Terminal Disclaimer filed on January 17, 2019

☒ APPROVED

This patent is subject to a terminal disclaimer

☐ DISAPPROVED

Approved/Disapproved by: Electronic Terminal Disclaimer automatically approved by EFS-Web

U.S. Patent and Trademark Office

Electronic Acknowledgement Receipt	
EFS ID:	34890569
Application Number:	15824841
International Application Number:	
Confirmation Number:	4819
Title of Invention:	Power Dissipation Reduction in Wireless Transceivers
First Named Inventor/Applicant Name:	Yannis Tsividis
Customer Number:	106303
Filer:	Jennifer NMN Hayes/Diana Girgis
Filer Authorized By:	Jennifer NMN Hayes
Attorney Docket Number:	THETA-000002US00
Receipt Date:	17-JAN-2019
Filing Date:	28-NOV-2017
Time Stamp:	18:10:26
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$160
RAM confirmation Number	011819INTEFSW00018618504166
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Terminal Disclaimer-Filed (Electronic)	eTerminal-Disclaimer.pdf	37011 76324bcafac7988979bb3a9937a6feea12f32c2c	no	3
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30566 122807b94fb99b8c4879bc3a13a5348edd4c9164	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	67577		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/824,841	11/28/2017	Yannis Tsividis	10037P007CCC

CONFIRMATION NO. 4819

8791
WOMBLE BOND DICKINSON (US) LLP
Attn: IP Docketing
P.O. Box 7037
Atlanta, GA 30357-0037

POWER OF ATTORNEY NOTICE

OC000000105175845

Date Mailed: 01/18/2019

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 01/14/2019.

- The Power of Attorney to you in this application has been revoked by the applicant. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/mteklemichael/

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/824,841	11/28/2017	Yannis Tsividis	THETA-000002US00

CONFIRMATION NO. 4819

106303
Nixon Peabody LLP
300 South Grand Avenue, Suite 4100
Los Angeles, CA 90071

POA ACCEPTANCE LETTER

OC000000105175898

Date Mailed: 01/18/2019

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 01/14/2019.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/mteklemichael/

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Apple EX1002 Page 178

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/824,841	11/28/2017	Yannis Tsividis	084820-000002US00	4819

106303 7590 04/12/2019

Nixon Peabody LLP
300 South Grand Avenue, Suite 4100
Los Angeles, CA 90071

EXAMINER	
VUONG, QUOCHIEN B	

ART UNIT	PAPER NUMBER
2649	

NOTIFICATION DATE	DELIVERY MODE
04/12/2019	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ipairlink@nixonpeabody.com
lapatentmb@nixonpeabody.com
slevy@nixonpeabody.com

Office Action Summary	**Application No.** 15/824,841	**Applicant(s)** Tsividis, Yannis	
	Examiner QUOCHIEN B VUONG	**Art Unit** 2649	**AIA (FITF) Status** No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 01/17/2019.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☑ This action is **FINAL.** 2b) ☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 21-27 and 29-39 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 21-27 and 29-39 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☑ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

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Apple EX1002 Page 180

DETAILED ACTION

Notice of Pre-AIA or AIA Status

The present application is being examined under the pre-AIA first to invent provisions.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 10/16/2018 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Terminal Disclaimer

The terminal disclaimer filed on 01/17/2019 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of U.S. Patent Application No. 15/080,432 and U.S. Patent No. 9,838,962 - 9,331,728 - 7,010,330 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Response to Arguments

Applicant's arguments, see Applicant's remarks, filed 01/17/2019, with respect to the rejection(s) of claim(s) 21-31 under 35 USC § 103 rejection have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Loke (US 6,311,048), Clark (US 5,001,776) and Leifso et al. (US 6,870,425).

In view of the terminal disclaimer above, the previous nonstatutory double patenting rejection has been withdrawn.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112(a):

> (a) IN GENERAL.—The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor or joint inventor of carrying out the invention.

The following is a quotation of the first paragraph of pre-AIA 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 31 and 37 are rejected under 35 U.S.C. 112(a) or 35 U.S.C. 112 (pre-AIA), first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor or a joint inventor, or for pre-AIA the inventor(s), at the time the application was filed, had possession of the claimed invention."

Claim 31 recites among other "*when the signal strength of the interferer signal is increasing, increasing an impedance a bias current of at least one of the plurality of circuits in the signal path of the receiver, thereby reducing increasing power dissipation in the receiver*." which is not described in the specification.

Claim 37 recites "*wherein the filtering the received signal to determine a signal strength of an interferer signal and a signal strength of a desired signal occurs over a period of time and further comprising comparing the signal strength of the interferer signal at a first period of time to the signal strength of the interferer signal at a second period of time to determine whether the signal strength of the interferer signal is increasing*." which is not described in the specification.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of pre-AIA 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 31, 32, 38 and 39 are rejected under pre-AIA 35 U.S.C. 102b as being anticipated by Loke (US 6,311,048).

Regarding claim 31, Loke (figures 1 and 2) disclose a method for reducing power consumption control in a receiver in a battery operated mobile device where the receiver receives a wireless signal and comprises a plurality of circuits, the plurality of circuits comprising a signal path including at least an amplifier (108), a mixer (110) and a filter (113), and wherein the receiver also comprises circuits for determining a signal strength at least at a location in the signal path, the method comprising: filtering the received signal to determine a signal strength of an interferer signal (RSSI) and a signal strength of a desired signal (EcIo); and when the signal strength of the interferer signal is increasing, increasing an impedance a bias current of at least one of the plurality of circuits in the signal path of the receiver, thereby reducing increasing power dissipation in the receiver (column 2, line 39 - column 4, line 40).

Regarding claim 32, Loke (figures 1 and 2) disclose a method for power dissipation optimization in a receiver of a wireless transceiver of a battery powered portable wireless device based on its operating conditions, wherein the receiver has a signal path comprising a plurality of circuits including at least an amplifier (108), a mixer (110) and a filter (113), the receiver having a plurality of circuits designed to function under operating conditions that vary based on relative signal strengths of the interferer signal and desired signal, wherein operating conditions vary between a worst-case operating

condition and a best-case operating condition, wherein the worst-case operating condition occurs when a desired signal strength is low and an interferer signal strength is high and the receiver operates with a maximum bias current, wherein the best-case operating condition occurs when the desired signal strength is high and the interferer signal strength is very low or zero and the receiver operates with a minimum bias current, the method comprising: receiving a wireless signal having a desired signal and an interferer signal by the receiver; determining the received desired signal strength (EcIo); determining the received interferer signal strength (RSSI); comparing the received desired signal strength relative to the received interferer signal strength; when the received desired signal strength relative to the received interferer signal strength is better than that the worst-case operating condition, reducing a bias current of one or more of the plurality of circuits in the signal path of the receiver, thereby reducing power dissipation and saving power (column 2, line 39 - column 4, line 40).

Regarding claim 38, Loke (figures 1 and 2) disclose a method for power dissipation control in a receiver of a wireless transceiver of a battery powered portable wireless device, the receiver having a signal path comprising a plurality of circuits including at least an amplifier (108), a mixer (110) and a filter (113), the method comprising: receiving a wireless signal having a desired signal strength and an interferer signal strength by the receiver; determining the received desired signal strength; determining the received interferer signal strength (RSSI); comparing the received desired signal strength (Ec/Io) relative to the received interferer signal strength; and when the received interferer signal strength is greater than the received desired signal strength, increasing a bias current of at least one of the plurality of circuits in the receiver signal path of the wireless transceiver, causing an increase in power dissipation (column 2, line 39 - column 4, line 40).

Regarding claim 39, Loke (figures 1 and 2) disclose a method for controlling power dissipation in a receiver of a wireless transceiver of a battery powered portable wireless device, the receiver having a signal path comprising a plurality of circuits including at least an amplifier (108), a mixer (110) and a

filter (113), the method comprising: receiving a wireless signal having a desired signal strength and an interferer signal strength by the receiver; determining the received desired signal strength (Ec/Io); determining the received interferer signal strength (RSSI); comparing the received desired signal strength relative to the received interferer signal strength; and wherein when the received desired signal strength is greater than the received interferer signal strength, decreasing a bias current of at least one of the plurality of circuits in the signal path (column 2, line 39 - column 4, line 40).

Claim Rejections - 35 USC § 103

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 21, 22, 25, 27, 30 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Clark (US 5,001,776) in view of Loke (US 6,311,048).

Regarding claim 21, Clark (figure 1) discloses a method of reducing the power consumption of a receiver of a battery operated transceiver having a plurality of circuits, wherein the plurality of circuits comprise a receiver signal path comprising at least an amplifier (108, 122), a mixer (110) and a filter (103), the plurality of circuits further comprise circuits for determining at least a signal strength indication in the signal path of the receiver; the method comprising: receiving a signal comprising a desired signal and an interferer signal in the receiver signal path; determining a first signal strength indication, wherein the first signal strength indication is relative to the strength of the received signal (127); determining a second signal strength indication, wherein the second signal strength indication is relative to the strength of the signal after filtering the received signal to reduce the

interferer signal (127'); comparing the first and second signal strength indication, and adjusting at least one of an impedance, a bias or a gain of at least one of the amplifier, filter or mixer in the signal path, responsive to the relative changes in the strength of the first and second signal strength indication (via control lines 132, 134, 138 and 140; column 2, line 34 - column 4, line 66). Clark does not specifically disclose comparing the first and second signal strength indication to one another. However, Loke (figures 1 and 2) disclose comparing a first signal strength indication, wherein the first signal strength indication is relative to the strength of the received signal (RSSI); determining a second signal strength indication, wherein the second signal strength indication is relative to the strength of the signal after reducing the interferer signal (Ec/Io) to one another, and adjusting at least one of an impedance, a bias or a gain of at least one of the amplifier, filter or mixer in the signal path, responsive to the relative changes in the strength of the first and second signal strength indication (column 2, line 39 - column 4, line 40). Therefore, it would have been obvious for one having ordinary skill in the art at the time the invention was made to adapt the teaching of comparing the first and second signal strength indications of Loke to the method of Clark as a system design preference for performing the same function as controlling and adjusting the bias of the amplifier to improve power consumption in the receiver.

Regarding claim 22, Clark and Loke discloses the method of claim 21 above. In addition, Clark discloses when the indicated interferer signal strength decreases, and the indicated strength of the desired signal decreases, decreasing the gain of at least one of the plurality of circuits in the signal path (low current operating mode) (column 2, line 34 - column 4, line 66). And Loke discloses decreasing a gain of an amplifier by decreasing a bias of at least one of the plurality of circuits in the signal path (column 4, lines 13-26).

Regarding claim 25, Clark (figure 1) discloses a method for reducing power consumption in a receiver in a battery operated mobile device where the receiver receives a wireless signal and comprises a plurality of circuits, the plurality of circuits comprising a signal path including at least an amplifier (108,

122), a mixer (110) and a filter (120), and wherein the receiver also comprises circuits for determining signal strengths at a plurality of locations in the signal path, the method comprising: filtering the received signal to determine a signal strength of a desired signal and a signal strength of an interferer signal; and when the signal strength of the interferer signal (127) is greater than the signal strength of the desired signal (127'), adjusting a gain of at least one of the plurality of circuits in the signal path of the receiver, thereby reducing power dissipation in the receiver path (column 2, line 34 - column 4, line 66). Clark does not specifically disclose comparing the signal strength of the desired signal to the signal strength of the interference signal and reducing a bias of at least one of the plurality of circuits in the signal path of the receiver. However, Loke (figures 1 and 2) disclose comparing the signal strength of the desired signal (Ec/Io) to the signal strength of the interference signal (RSSI), and adjusting a bias of at least one of the plurality of circuits in the signal path of the receiver (column 2, line 39 - column 4, line 40). Therefore, it would have been obvious for one having ordinary skill in the art at the time the invention was made to adapt the teaching of comparing the signal strength of the desired signal to the signal strength of the interference signal and adjusting the gain of the amplifier by adjusting the bias of Loke to the method of Clark as a system design preference for performing the same function as controlling and adjusting the bias of the amplifier to improve power consumption in the receiver.

Regarding claim 27, Clark (figure 1) discloses a method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, the receiver having a signal path comprising a plurality of circuits including at least an amplifier (108, 122), a filter (120), and a mixer (110), the receiver having a plurality of circuits to function under a worst case condition when a received desired signal strength is low and a received interferer signal strength is high, the method comprising: receiving a wireless signal having a desired signal strength and an interferer signal strength by the receive; determining a received desired signal strength (127') and determining a received interferer signal strength (127); and when the signal strength of the interferer signal is low and the

signal strength of the desired signal is low, causing a gain of one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be decreased compared to the worst-case power dissipation condition, thereby saving power (column 2, line 34 -column 4, line 66). Clark does not specifically disclose comparing the received desired signal strength relative to the received interferer signal strength; and causing a bias current of one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be decreased. However, Loke (figures 1 and 2) disclose comparing the signal strength of the desired signal (Ec/Io) to the signal strength of the interference signal (RSSI), and adjusting a bias of at least one of the plurality of circuits in the signal path of the receiver (column 2, line 39 - column 4, line 40). Therefore, it would have been obvious for one having ordinary skill in the art at the time the invention was made to adapt the teaching of comparing the signal strength of the desired signal to the signal strength of the interference signal and adjusting the gain of the amplifier by adjusting the bias of Loke to the method of Clark as a system design preference for performing the same function as controlling and adjusting the bias of the amplifier to improve power consumption in the receiver.

Regarding claim 30, Clark (figure 1) discloses a method for power dissipation control in a receiver of a wireless transceiver of a battery powered portable wireless device, the receiver having a signal path comprising a plurality of circuits including at least an amplifier (108, 122), a filter (120), and a mixer (110), the method comprising: receiving a wireless signal having a desired signal strength and an interferer signal strength by the receiver, determining the received desired signal strength, determining the received interferer signal strength; and when the received interferer signal strength is high and the signal strength of the received desired signal is low, causing a gain of one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be increased, causing a reduction in power dissipation (column 2, line 34 - column 4, line 66). Clark does not specifically disclose comparing the received desired signal strength relative to the received interferer signal strength; and causing a bias current of one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to

be increased. However, Loke (figures 1 and 2) disclose comparing the signal strength of the desired signal (Ec/Io) to the signal strength of the interference signal (RSSI), and adjusting a bias of at least one of the plurality of circuits in the signal path of the receiver (column 2, line 39 - column 4, line 40). Therefore, it would have been obvious for one having ordinary skill in the art at the time the invention was made to adapt the teaching of comparing the signal strength of the desired signal to the signal strength of the interference signal and adjusting the gain of the amplifier by adjusting the bias of Loke to the method of Clark as a system design preference for performing the same function as controlling and adjusting the bias of the amplifier to improve power consumption in the receiver.

Claims 23, 24, 26, 29, are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Clark (US 5,001,776) in view of Loke (US 6,311,048) and further in view of Leifso et al. (US 6,870,425).

Regarding claim 23, Clark and Loke discloses the method of claim 21 above. Clark does not specifically disclose when the indicated strength of the desired signal decreases, increasing an impedance of at least one of the plurality of circuits in the signal path. In addition, Clark discloses wherein when the indicated interferer signal strength decreases, and the indicated strength of the desired signal decreases, increasing a gain of at least one of a plurality of circuits in the signal path (column 2, line 34 – column 4, line 66). Clark and Loke do not specifically disclose wherein when the indicated interferer signal strength decreases, and the indicated strength of the desired signal decreases increasing an impedance of at least one of the plurality of circuits in the signal path. However, Leifso et al. (figure 4) disclose adjusting a gain of an amplifier by changing an impedance of at least one of the plurality of circuits in the signal path (column 6, line 26 - column 8, line 15). Therefore, it would have been obvious for one having ordinary skill in the art at the time the invention was made to adapt the teaching of adjusting the gain of the amplifier and adjusting the impedance of Leifso et al. to the method

of Clark and Loke as a system design preference for performing the same function as controlling and adjusting the gain of the amplifier and power consumption in the receiver.

Regarding claim 24, Clark (figure 1) discloses a method for reducing power consumption in a receiver in a battery operated mobile device where the receiver receives a wireless signal and comprises a plurality of circuits, the plurality of circuits comprising a signal path including at least an amplifier (108, 122), a mixer (110) and a filter (120), and wherein the receiver also comprises circuits for determining at least a signal strength at a one or more locations in the signal path, the method comprising: filtering the received signal to determine a signal strength of a desired signal and a signal strength of an interferer signal; and when the signal strength of the desired signal (127') is greater than the signal strength of the interferer signal (127), adjusting a gain of at least one of the amplifier, filter or mixer in the signal path of the receiver, thereby reducing power dissipation in the receiver path (column 2, line 34 - column 4, line 66). Clark does not specifically disclose comparing the signal strength of the desired signal to the signal strength of the interference signal and increasing an impedance of at least one of the amplifier, filter or mixer in the signal path of the receiver. However, Loke (figures 1 and 2) disclose comparing the signal strength of the desired signal (Ec/Io) to the signal strength of the interference signal (RSSI), and adjusting at least one of an impedance, a bias or a gain of at least one of the amplifier, filter or mixer in the signal path, responsive to the relative changes in the strength of the first and second signal strength indication (column 2, line 39 - column 4, line 40). Therefore, it would have been obvious for one having ordinary skill in the art at the time the invention was made to adapt the teaching of comparing the signal strength of the desired signal to the signal strength of the interference signal of Loke to the method of Clark as a system design preference for performing the same function as controlling and adjusting the bias of the amplifier to improve power consumption in the receiver. Clark and Loke do not specifically disclose increasing an impedance of at least one of the amplifier, filter or mixer in the signal path of the receiver. However, Leifso et al. (figure 4) disclose adjusting a gain of an amplifier by changing

an impedance of at least one of the plurality of circuits in the signal path (column 6, line 26 - column 8, line 15). Therefore, it would have been obvious for one having ordinary skill in the art at the time the invention was made to adapt the teaching of adjusting the gain of the amplifier by adjusting the impedance of Leifso et al. to the method of Clark and Loke as a system design preference for performing the same function as controlling and adjusting the gain of the amplifier and power consumption in the receiver path of the receiver, thereby reducing power dissipation in the receiver.

Regarding claim 26, Clark (figure 1) discloses a method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, the receiver having a signal path comprising a plurality of circuits including at least an amplifier (108, 122), a filter (120), and a mixer (110), the receiver having a plurality of circuits to function under a worst-case condition when a received desired signal strength is low and a received interferer signal strength is high, the method comprising: receiving a wireless signal having a desired signal strength and an interferer signal strength by the receiver; determining a received desired signal strength (127'); determining the received interference signal strength (127); and when the interference signal strength is high and the signal strength of the desired signal is high, causing a gain of one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be increased compared to the worst-case condition, thereby saving power (column 2, line 34 - column 4, line 66). Clark does not specifically disclose comparing the received desired signal strength relative to the received interferer signal strength; and causing an impedance of one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be increased. However, Loke (figures 1 and 2) disclose comparing the received desired signal strength (Ec/Io) relative to the received interferer signal strength (RSSI), and adjusting at least a bias or a gain of at least one of the amplifier, filter or mixer in the signal path, responsive to the relative changes in the strength of the first and second signal strength indication (column 2, line 39 - column 4, line 40). Therefore, it would have been obvious for one having ordinary

skill in the art at the time the invention was made to adapt the teaching of the received desired signal strength relative to the received interferer signal strength of Loke to the method of Clark as a system design preference for performing the same function as controlling and adjusting the bias of the amplifier to improve power consumption in the receiver. Clark and Loke do not specifically disclose increasing an impedance of at one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be increased relative to the impedance at the worst condition. However, Leifso et al. (figure 4) disclose adjusting a gain of an amplifier by changing an impedance of at least one of the plurality of circuits in the signal path (column 6, line 26 - column 8, line 15). Therefore, it would have been obvious for one having ordinary skill in the art at the time the invention was made to adapt the teaching of adjusting the gain of the amplifier by adjusting the impedance of Leifso et al. to the method of Clark and Loke as a system design preference for performing the same function as controlling and adjusting the gain of the amplifier and power consumption in the receiver.

Regarding claim 29, Clark (figure 1) discloses a method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, the receiver having a plurality of circuits to function under a worst case condition when a received desired signal strength is low and a received interferer signal strength is high, the receiver having a signal path comprising a plurality of circuits including at least an amplifier (108, 122), a filter (120), and a mixer (110), the method comprising: receiving a wireless signal having a desired signal strength and an interferer signal strength by the receiver, determining a received desired signal strength (127'), determining a received interferer signal strength (127); and when the signal strength of the interferer signal is low and the signal strength of the desired signal is high, causing a gain of one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be increased compared to the worst-case power dissipation condition, thereby saving power (column 2, line 34 - column 4, line 66). Clark does not specifically disclose comparing the desired signal strength relative to the interferer signal strength; and

causing an impedance of one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be increased. However, Loke (figures 1 and 2) disclose comparing the received desired signal strength (Ec/Io) relative to the received interferer signal strength (RSSI), and adjusting at least a bias or a gain of at least one of the amplifier, filter or mixer in the signal path, responsive to the relative changes in the strength of the first and second signal strength indication (column 2, line 39 - column 4, line 40). Therefore, it would have been obvious for one having ordinary skill in the art at the time the invention was made to adapt the teaching of the received desired signal strength relative to the received interferer signal strength of Loke to the method of Clark as a system design preference for performing the same function as controlling and adjusting the bias of the amplifier to improve power consumption in the receiver. Clark and Loke do not specifically disclose causing an impedance of one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be increased relative to the worst-case condition. However, Leifso et al. (figure 4) disclose adjusting a gain of an amplifier by changing an impedance of at least one of the plurality of circuits in the signal path (column 6, line 26 - column 8, line 15). Therefore, it would have been obvious for one having ordinary skill in the art at the time the invention was made to adapt the teaching of adjusting the gain of the amplifier by adjusting the impedance of Leifso et al. to the method of Clark and Loke as a system design preference for performing the same function as controlling and adjusting the gain of the amplifier and power consumption in the receiver.

Claims 33-35 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Loke (US 6,311,048) in view of Clark (US 5,001,776).

Regarding claim 33, Loke disclose the method of claim 32 above. Loke does not specifically disclose wherein the received desired signal strength relative to the received interferer signal strength is better than that the worst-case operating condition when the received desired signal strength is higher

than the desired signal strength at the worst- case operating condition. However, Clark (figure 1) disclose comparing the received desired signal strength and the received interferer signal strength with the threshold to adjust the gain for low current operating mode to save power (row 3 of TABLE 1 show the received desired signal strength (High) is higher than the desired signal strength at the worst- case operating condition (threshold); column 2, line 34 – column 4, line 30). Therefore, it would have been obvious for one having ordinary skill in the art at the time the invention was made to adapt the teaching of comparing the desired signal strength of Clark to the method of Loke as a system design preference for performing the same function as to determine the desired signal strength for adjusting the receiver to save power.

Regarding claim 34, Loke disclose the method of claim 32 above. Loke does not specifically disclose wherein the received desired signal strength relative to the received interferer signal strength is better than that the worst-case operating condition when the received interfere signal strength is lower than the interferer signal strength at the worst case operating condition. However, Clark (figure 1) disclose comparing the received desired signal strength and the received interferer signal strength with the threshold to adjust the gain for low current operating mode to save power (row 3 of TABLE 1 show the received interferer signal strength (Low) is lower than the interfere signal strength at the worst- case operating condition (threshold); column 2, line 34 – column 4, line 30). Therefore, it would have been obvious for one having ordinary skill in the art at the time the invention was made to adapt the teaching of comparing the interferer signal strength of Clark to the method of Loke as a system design preference for performing the same function as to determine the received interferer signal strength for adjusting the receiver to save power.

Regarding claim 35, Loke disclose the method of claim 32 above. Loke does not specifically disclose wherein the received desired signal strength relative to the received interferer signal strength is better than that the worst-case operating condition when the received desired signal strength is higher

than the desired signal strength of the worst- case operating condition and the received interferer signal strength is lower than the interferer signal strength at the worst case operating condition. However, Clark (figure 1) disclose comparing the received desired signal strength and the received interferer signal strength with the threshold to adjust the gain for low current operating mode to save power (row 3 of TABLE 1 show the received desired signal strength (High) is higher than the desired signal strength at the worst- case operating condition (threshold); and the received interferer signal strength (Low) is lower than the interferer signal strength at the worst case operating condition (threshold) ; column 2, line 34 – column 4, line 30). Therefore, it would have been obvious for one having ordinary skill in the art at the time the invention was made to adapt the teaching of comparing the desired signal strength and the interferer signal of Clark to the method of Loke as a system design preference for performing the same function as to determine the desired signal strength and received interferer signal strength for adjusting the receiver to save power.

Claim 36 is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Loke (US 6,311,048) in view of Official notice.

Regarding claim 36, Loke disclose the method of claim 32 above. Loke does not specifically disclose wherein the interferer signal is due to other transceivers or nearby electronic equipment generating interfering signals and other spurious noise. However, the examiner takes Official notice that interferer signal is due to other transceivers or nearby electronic equipment generating interfering signals and other spurious noise is well-known in the art. Therefore, it would have been obvious for one having ordinary skill in the art at the time the invention was made to adapt the well-known interferer signal due to other transceivers or nearby electronic equipment generating interfering signals and other spurious noise to the method of Loke for adjusting the receiver according to the well-known interferer signal to reduce power consumption without degradation of the received desired signal.

Claim 37 is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Loke (US 6,311,048) in view of Jarvinen (US 5,406,635).

Regarding claim 37, Loke disclose the method of claim 32 above. Loke does not specifically disclose wherein the filtering the received signal to determine a signal strength of an interferer signal and a signal strength of a desired signal occurs over a period of time and further comprising comparing the signal strength of the interferer signal at a first period of time to the signal strength of the interferer signal at a second period of time to determine whether the signal strength of the interferer signal is increasing. However, Jarvinen (figure 2) discloses filtering the received signal to determine a signal strength of an interferer signal and a signal strength of a desired signal occurs over a period of time (column 3, lines 5-43; and column 4, lines 25-55). Therefore, it would have been obvious for one having ordinary skill in the art at the time the invention was made to adapt the teaching of Jarvinen to the method of Loke for more proper determining of the signal strength over a period of time.

Loke and Jarvinen do not specifically disclose comparing the signal strength of the interferer signal at a first period of time to the signal strength of the interferer signal at a second period of time to determine whether the signal strength of the interferer signal is increasing. However, examiner takes Official notice that it is well-known in the art to determining whether the signal strength of the interferer signal is increasing by comparing the signal strength of the interferer signal at a first period of time to the signal strength of the interferer signal at a second period of time. Therefore, it would have been obvious for one having ordinary skill in the art at the time the invention was made to adapt the well-known comparison to the method of Jarvinen and Loke for more proper determining the increasing of the interferer signal.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to QUOCHIEN B VUONG whose telephone number is (571)272-7902. The examiner can normally be reached on 10:00-06:00PM M-F.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, EDWARD URBAN can be reached on 571-272-7899. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available

through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/QUOCHIEN B VUONG/
Primary Examiner, Art Unit 2649

Notice of References Cited	Application/Control No. 15/824,841	Applicant(s)/Patent Under Reexamination Tsividis, Yannis	
	Examiner QUOCHIEN B VUONG	Art Unit 2649	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-5406635-A	04-1995	Jarvinen;Kari J.	G10L21/0208	381/94.3
*	B	US-6311048-B1	10-2001	Loke; Aravind	H04B1/109	455/245.1
*	C	US-7656933-B2	02-2010	Klinke; Stefano Ambrosius	G10L21/02	455/63.1
	D					
	E					
	F					
	G					
	H					
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/824,841	Tsividis, Yannis
	Examiner	Art Unit
	QUOCHIEN B VUONG	2649

CPC - Searched*		
Symbol	**Date**	**Examiner**
H04B 1/16, 1/1607, 1/40, 17/318	07/06/2018	/QV/
H04W 52/52	07/06/2018	/QV/
H03F 1/56, 3/20, 2200/27, 2200/78, 2200/387, 2200/451	07/06/2018	/QV/

CPC Combination Sets - Searched*		
Symbol	**Date**	**Examiner**

US Classification - Searched*			
Class	**Subclass**	**Date**	**Examiner**
455	63.1,67.13,127.1,127.2,127.5,226.1,226.2,232.1,234.1, 250.1,251.1,295,296,311,343.1,572,574	07/06/2018	/QV/
370	442	0706/2018	/QV/
330	127,134,144	07/06/2018	/QV/

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	**Date**	**Examiner**
EAST search	07/06/2018	/QV/
Inventor name search	07/06/2018	/QV/
Search updated	04/04/2019	/QV/

Interference Search			
US Class/CPC Symbol	**US Subclass/CPC Group**	**Date**	**Examiner**

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	15/824,841	Tsividis, Yannis
	Examiner	Art Unit
	QUOCHIEN B VUONG	2649

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	07/06/2018	04/08/2019							
	1	-	-							
	2	-	-							
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	18	-	-							
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	20	-	-							
	21	✓	✓							
	22	✓	✓							
	23	✓	✓							
	24	✓	✓							
	25	✓	✓							
	26	✓	✓							
	27	✓	✓							
	28	✓	-							
	29	✓	✓							
	30	✓	✓							
	31	✓	✓							
	32		✓							
	33		✓							
	34		✓							
	35		✓							
	36		✓							
	37		✓							
	38		✓							
	39		✓							

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	7237	(second near4 (RSSI (signal near4 (strength level quality)))) same ((control$4 adjust$3) with (gain impedance bias))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/04/04 15:37
S2	1959	S1 same (receiver receiving)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/04/04 15:38
S3	153	S2 same (compar$3 near6 (RSSI (signal near4 (strength level quality))))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/04/04 15:39
S4	531	(compar$3 with (RSSI (signal near4 (strength level quality))) with (interference noise)) same ((control$4 adjust$3) with (gain impedance bias))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/04/04 15:55

EAST Search History (Interference)

< This search history is empty>

4/4/2019 7:09:11 PM

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Apple EX1002 Page 202

Substitute for form 1449A/PTO	*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	15/824,841
	Filing Date	Nov 28, 2017
	First Named Inventor	Yannis Tsividis
	Group Art Unit	2647
	Examiner Name	Vuong, Quochien B
Sheet 1 of 1	Attorney Docket No: 10037P007CCC	

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	**Cite No [1]**	**Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.**	**T [2]**
/Q.B.V/		"Notice of Allowance Dated July 18, 2018; U.S. Patent Application No. 15/080,432", 7/18/2018	

EXAMINER	/QUOCHIEN B VUONG/	**DATE CONSIDERED**	04/04/2019

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449) as modified by BSTZ 03/26/07

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

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Nixon Peabody LLP
300 South Grand Avenue, Suite 4100
Los Angeles, CA 90071

Courtesy Reminder for
Application Serial No: 15/824,841

Attorney Docket No: 084820-000002US00
Customer Number: 106303
Date of Electronic Notification: 04/12/2019

This is a courtesy reminder that new correspondence is available for this application. If you have not done so already, please review the correspondence. The official date of notification of the outgoing correspondence will be indicated on the form PTOL-90 accompanying the correspondence.

An email notification regarding the correspondence was sent to the following email address(es) associated with your customer number:

lapatentmb@nixonpeabody.com
ipairlink@nixonpeabody.com
slevy@nixonpeabody.com

To view your correspondence online or update your email addresses, please visit us anytime at **https://ppair-my.uspto.gov/pair/PrivatePair.**
If you have any questions, please email the Electronic Business Center (EBC) at EBC@uspto.gov or call 1-866-217-9197.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 15/824,841	Filing Date 11/28/2017	☐ To be Mailed

ENTITY: ☐ LARGE ☑ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $40 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $210 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
AMENDMENT	10/11/2019							
	Total (37 CFR 1.16(i))	* 23	Minus	** 20	= 3		x $50 =	150
	Independent (37 CFR 1.16(h))	* 11	Minus	*** 11	= 0		x $230 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	150

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
AMENDMENT								
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/KIMBERLY N PANNELL/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Doc code: RCEX
Doc description: Request for Continued Examination (RCE)

PTO/SB/30EFS (07-14)
Approved for use through 07/31/2016. OMB 0651-0031
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REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)

Application Number	15824841	Filing Date	2017-11-28	Docket Number (if applicable)	084820-000002US00	Art Unit	2647
First Named Inventor	Yannis TSIVIDIS			Examiner Name	Quochien B. VUONG		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, to any international application that does not comply with the requirements of 35 U.S.C. 371, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV.

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

- ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
- ☐ Other _____

☒ Enclosed

- ☒ Amendment/Reply
- ☐ Information Disclosure Statement (IDS)
- ☐ Affidavit(s)/ Declaration(s)
- ☐ Other _____

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____
(Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

☒ **The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.**
The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No 504166

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

Applicant Signature

EFS - Web 2.1.15

PTO/SB/30EFS (07-14)
Approved for use through 07/31/2016. OMB 0651-0031
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Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Signature of Registered U.S. Patent Practitioner			
Signature	/Jennifer Hayes/	Date (YYYY-MM-DD)	2019-10-11
Name	Jennifer Hayes	Registration Number	60845

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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Electronic Patent Application Fee Transmittal

Application Number:	15824841
Filing Date:	28-Nov-2017
Title of Invention:	Power Dissipation Reduction in Wireless Transceivers
First Named Inventor/Applicant Name:	Yannis Tsividis
Filer:	Jennifer NMN Hayes/Diana Girgis
Attorney Docket Number:	084820-000002US00

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
CLAIMS IN EXCESS OF 20	2202	3	50	150
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Extension - 3 months with $0 paid	2253	1	700	700
Miscellaneous:				
RCE- 1ST REQUEST	2801	1	650	650
		Total in USD ($)		**1500**

Electronic Acknowledgement Receipt	
EFS ID:	37441287
Application Number:	15824841
International Application Number:	
Confirmation Number:	4819
Title of Invention:	Power Dissipation Reduction in Wireless Transceivers
First Named Inventor/Applicant Name:	Yannis Tsividis
Customer Number:	106303
Filer:	Jennifer NMN Hayes/Diana Girgis
Filer Authorized By:	Jennifer NMN Hayes
Attorney Docket Number:	084820-000002US00
Receipt Date:	11-OCT-2019
Filing Date:	28-NOV-2017
Time Stamp:	20:01:42
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$1500
RAM confirmation Number	E20190AK02180780
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		2019-10-11-Response-to-OA-Amendment-084820-002US00.pdf	618282 33541150e785a30a6100382c454e7a3409a1cd05	yes	37
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Amendment Submitted/Entered with Filing of CPA/RCE		1	1	
	Claims		2	12	
	Amendment/Req. Reconsideration-After Non-Final Reject		13	37	
Warnings:					
Information:					
2	Request for Continued Examination (RCE)	2019-10-11-RCE-084820-002US00.pdf	1349874 228112e4593417d79f7821b66aa2f3a87e2ed62e	no	3
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	34094 577687f4198b7283e6e22d60850aef9eb0ea9ac1	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	2002250		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Yannis TSIVIDIS	Confirmation No.:	4819
Application No.:	15/824,841	Examiner:	Quochien B. VUONG
Filing Date:	November 28, 2017	Art Unit:	2647
Title:	Power Dissipation Reduction in Wireless Transceivers		

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT AND RESPONSE TO OFFICE ACTION

Sir:

In response to the Final Office Action mailed April 12, 2019, please enter the following amendments and consider the accompanying remarks.

Amendments to the Claims, if any, are reflected in the Listing of Claims beginning on page **2**.

Remarks begin on page **13**.

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Amendments to the Claims

The following Listing of Claims replaces all prior versions in the application:

1-20. (Cancelled)

21. (Currently Amended) A method of reducing the power consumption of a receiver of a battery operated transceiver having a plurality of circuits, wherein the plurality of circuits comprise a receiver signal path comprising at least an amplifier, a mixer and a filter, ~~the plurality of circuits further comprise circuits for determining at least a signal strength indication in the signal path of the receiver;~~ wherein the plurality of circuits are designed to function between a worst-case operating condition and a best case operating condition, wherein the worst-case operating condition is when a desired signal strength is low and an interferer signal strength is high and the receiver operates with a maximum power dissipation and the best-case operating condition is when the desired signal strength is high and the interferer signal strength is low and the receiver operates with a minimum power dissipation, the method comprising:

receiving a signal comprising a desired signal and an interferer signal ~~in the receiver signal path~~;

determining a ~~first signal~~ strength of the desired signal ~~indication, wherein the first signal strength indication is relative to the strength of the received signal~~;

determining a ~~second signal strength indication, wherein the second signal strength indication is relative to the~~ strength of the ~~signal after filtering the received signal to reduce the~~ interferer signal;

comparing the strength of the desired signal to the strength of the interfere signal~~first and second signal strength indication to one another~~;~~,~~ and

dynamically adjusting at least one of an impedance, a bias or a gain of at least one of the amplifier, filter or mixer in the receiver signal path, responsive to ~~relative changes in the strength of the first and second signal strength indication~~the comparing.

22. (Currently Amended) The method of claim 21, wherein when the ~~indicated~~ strength of the interferer signal ~~strength~~ decreases over time, and the ~~indicated~~ strength of the

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desired signal ~~decreases~~is low, dynamically decreasing the bias of at least one of the plurality of circuits in the receiver signal path.

23. (Currently Amended) The method of claim 21, wherein when the ~~indicated~~ strength of the interferer signal ~~strength decreases~~is low, and the ~~indicated~~ strength of the desired signal decreases over time, dynamically increasing a gain of at least one of a plurality of circuits in the receiver signal path and dynamically increasing ~~an~~ the impedance of at least one of the plurality of circuits in the receiver signal path.

24. (Currently Amended) A method for reducing power consumption in a receiver in a battery operated mobile device, wherein the receiver ~~receives a wireless signal and~~ comprises a plurality of circuits, and wherein the plurality of circuits compris~~e~~ing a signal path including at least an amplifier, a mixer and a filter~~, and wherein the receiver also comprises circuits for determining at least a signal strength at a one or more locations in the signal path~~, the method comprising:

receiving a wireless signal comprising a desired signal and an interferer signal at the receiver;

determining a strength of the desired signal;

determining a strength of the interferer signal;

~~filtering the received signal to determine a signal strength of a desired signal and a signal strength of an interferer signal;~~

comparing the ~~signal~~ strength of the desired signal to the ~~signal~~ strength of the interferer signal; and

when the strength of the interferer signal is low and the relative ~~signal~~ strength of the desired signal is greater than the ~~signal~~ strength of the interferer signal, dynamically increasing an impedance of at least one of the amplifier, filter or mixer in the signal path of the receiver, thereby reducing power dissipation in the receiver.

25. (Cancelled)

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26. (Currently Amended) A method for power dissipation ~~reduction~~ control in a receiver of a wireless transceiver of a battery--powered portable wireless device, the receiver having a signal path comprising a plurality of circuits including at least an amplifier, a filter, and a mixer, wherein the receiver is configured to receive a wireless signal having a desired signal and an interferer signal, ~~the receiver having a~~wherein the plurality of circuits are designed to function ~~under~~ between a worst-case condition when a ~~received~~ strength of the desired signal ~~strength~~ is low and a strength of the ~~received~~ interferer signal ~~strength~~ is high, and a best-case condition when the strength of the desired signal is high and the strength of the interferer signal is low, the method comprising:

receiving ~~a~~ the wireless signal having the~~a~~ desired signal ~~strength~~ and ~~an~~ the interferer signal ~~strength~~ by the receiver;

determining the strength of the ~~received~~ desired signal ~~strength~~;

determining the strength of the ~~received~~ interferer signal ~~strength~~;

comparing the ~~received~~ strength of the desired signal ~~strength~~ relative to the ~~received~~ strength of the interferer signal ~~strength~~; and

based on the comparison, when the plurality of circuits are functioning at better than the worst-case condition, ~~when the interferer signal strength is high and the desired signal strength is high, causing~~ dynamically adjusting one or more of an impedance, a bias or a gain of one or more of the plurality of circuits in the ~~receiver~~ signal path ~~of the wireless transceiver to be increased relative to the impedance at the worst-case condition~~, thereby ~~saving~~ controlling power dissipation.

27. (Currently Amended) A method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, the receiver having a signal path comprising a plurality of circuits including at least an amplifier, a filter, and a mixer, the ~~receiver having a~~ plurality of circuits designed to function under at least a worst case condition when a strength of a received desired signal ~~strength~~ is low and a strength of a received interferer signal ~~strength~~ is high, the method comprising:

receiving a wireless signal having a desired signal ~~strength~~ and an interferer signal ~~strength~~ by the receiver;

determining a strength of the ~~received~~ desired signal ~~strength~~;

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determining a strength of the ~~received~~ interferer signal ~~strength~~;

comparing the strength of the ~~received~~ desired signal ~~strength~~ relative to the strength of the ~~received~~ interferer signal ~~strength~~;

based on the comparing, determining a functioning condition of the plurality of circuits; and

when the plurality of circuits are determined to function at a better than the worst case condition in which the strength of the interferer signal ~~strength~~ is low and the strength of the desired signal ~~strength~~ is low, causing a bias current of one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be dynamically decreased relative to the worst-case condition, thereby saving power.

28. (Cancelled)

29. (Currently Amended) A method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, the receiver ~~having a plurality of circuits~~ configured to function under at least a worst case condition when a received desired signal strength is low and a received interferer signal strength is high, the receiver having a signal path comprising ~~a plurality of circuits including~~ at least an amplifier, a filter, and a mixer, the method comprising:

receiving a wireless signal having a desired signal ~~strength~~ and an interferer signal ~~strength~~ by the receiver;

determining a strength of the ~~received~~ desired signal ~~strength~~;

determining a strength of the ~~received~~ interferer signal ~~strength~~;

comparing the strength of the desired signal ~~strength~~ relative to the strength of the interferer signal ~~strength~~;

based on the comparing, determining a functioning condition of the plurality of circuits; and

when the plurality of circuits are determined to function at a better than the worst case condition in which the strength of the interferer signal ~~strength~~ is low and the strength of the desired signal ~~strength~~ is high, causing an impedance of one or more of ~~the plurality of circuits~~

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amplifier, filter or the mixer in the receiver signal path of the wireless transceiver to be increased relative to the worst-case condition, thereby saving power.

30. (Currently Amended) A method for power dissipation control in a receiver of a wireless transceiver of a battery powered portable wireless device, the receiver having a signal path comprising a plurality of circuits including at least an amplifier, a filter, and a mixer, the method comprising:

receiving a wireless signal having a desired signal ~~strength~~ and an interferer signal ~~strength~~ by the receiver;

determining the strength of the ~~received~~ desired signal ~~strength~~;

determining the strength of the ~~received~~ interferer signal ~~strength~~;

comparing the strength of the ~~received~~ desired signal ~~strength~~ relative to the strength of the ~~received~~ interferer signal ~~strength~~; and

when the ~~received~~ interferer signal strength is high and the ~~received~~ desired signal strength is low, causing a bias current of one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be dynamically increased, ~~causing an increase in~~ controlling the power dissipation of the receiver.

31. (Cancelled)

32. (Currently Amended) A method for power dissipation ~~optimization~~ reduction in a receiver of a wireless transceiver of a battery powered portable wireless device based on its operating signal conditions, wherein the receiver has a signal path comprising a plurality of circuits including at least an amplifier, a filter, and a mixer, the ~~receiver having a~~ plurality of circuits designed to function under operating signal conditions that vary based on relative signal strengths of ~~the~~ an interferer signal and a desired signal, wherein the operating signal conditions vary between a worst-case operating condition and a best-case operating condition, wherein the worst-case operating condition occurs when a desired signal strength is low and an interferer signal strength is high and the receiver operates with a maximum ~~bias current~~power dissipation, wherein the best-case operating condition occurs when the desired signal strength is high and the

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interferer signal strength is ~~very~~ low ~~or zero~~ and the receiver operates with a minimum ~~bias current~~power dissipation, the method comprising:

receiving a wireless signal having a desired signal and an interferer signal by the receiver;

determining the strength of the ~~received~~ desired signal ~~strength~~;

determining the strength of the ~~received~~ interferer signal ~~strength~~;

comparing the strength of the ~~received~~ desired signal ~~strength~~ relative to the strength of the ~~received~~ interferer signal strength;

based on the comparing, when the plurality of circuits are determined to be functioning at better than the worst-case operating signal condition, ~~when the received desired signal strength relative to the received interferer signal strength is better than that the worst-case operating condition~~, ~~reducing~~ dynamically adjusting at least one of an impedance, a bias current or a gain of one or more of the ~~plurality of circuits~~ amplifier, filter or mixer in the signal path of the receiver, thereby reducing power ~~dissipation and saving~~ consumption to save power.

33 - 37. (Cancelled)

38. (Currently Amended) A method for power dissipation ~~control~~ optimization in a receiver of a wireless transceiver of a battery powered portable wireless device, the receiver having a signal path comprising a plurality of circuits including at least an amplifier, a filter, and a mixer, wherein the plurality of circuits are designed to function between a worst-case operating condition and a best case operating condition, wherein the worst-case operating condition is when a desired signal strength is low and an interferer signal strength is high and the receiver operates with a maximum power dissipation and the best-case operating condition is when the desired signal strength is high and the interferer signal strength is low and the receiver operates with a minimum power dissipation, the method comprising:

receiving a wireless signal having a desired signal ~~strength~~ and an interferer signal ~~strength~~ by the receiver;

determining a strength of the ~~received~~ desired signal ~~strength~~;

determining a strength of the ~~received~~ interferer signal ~~strength~~;

comparing the strength of the ~~received~~ desired signal ~~strength~~ relative to the strength of the ~~received~~ interferer signal ~~strength~~; and

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based on the comparing, when the plurality of circuits are determined to be functioning at better than the worst-case operating condition, dynamically adjusting at least one of an impedance, a bias current or a gain of one or more of the amplifier, filter or mixer in the signal path of the receiver to optimize power dissipation and save power~~when the received interferer signal strength is greater than the received desired signal strength, increasing a bias current of at least one of the plurality of circuits in the receiver signal path of the wireless transceiver, causing an increase in power dissipation~~.

39. (Currently Amended) A method for controlling power dissipation in a receiver of a wireless transceiver of a battery powered portable wireless device, the receiver having a signal path comprising a plurality of circuits including at least an amplifier, a filter, and a mixer, wherein the plurality of circuits are designed to function between a worst-case operating condition and a best case operating condition, wherein the worst-case operating condition is when a desired signal strength is low and an interferer signal strength is high and the receiver operates with a maximum power dissipation and the best-case operating condition is when the desired signal strength is high and the interferer signal strength is low and the receiver operates with a minimum power dissipation, the method comprising:

receiving a wireless signal having a desired signal ~~strength~~ and an interferer signal ~~strength~~ by the receiver;

determining a strength of the ~~received~~ desired signal ~~strength~~;

determining a strength of the ~~received~~ interferer signal ~~strength~~;

comparing the strength of the ~~received~~ desired signal ~~strength~~ relative to the strength of the ~~received~~ interferer signal ~~strength~~; and

wherein when the strength of the received interferer signal is low and when the strength of the received desired signal ~~strength~~ is ~~greater~~ higher than the ~~received interferer signal strength~~desired signal strength of the worst-case operating signal condition, ~~decreasing~~ dynamically adjusting an impedance ~~a bias current~~ of at least one of the plurality of circuits in the signal path to reduce power dissipation.

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40. (New) The method of claim 21 wherein when the strength of the interferer signal is low and the strength of the desired signal increases over time, dynamically increasing the impedance of one or more of the plurality of circuits in the receiver signal path.

41. (New) The method of claim 21, wherein when the interferer signal is weak and the desired signal is low and the strength of the desired signal increases over time, dynamically decreasing the bias of one or more of the plurality of circuits in the receiver signal path.

42. (New) The method of claim 26, wherein when the strength of the interferer signal is low and the relative strength of the desired signal with respect to the interferer signal increases, dynamically increasing the impedance of one or more of the plurality of circuits in the signal path to reduce the power dissipation and thereby save power.

43. (New) The method of claim 26, wherein when the strength of the desired signal is low but the relative strength of the desired signal with respect to the interferer signal is better than the worst-case condition and the interferer signal reduces in strength, dynamically reducing the bias of one or more of the plurality of circuits in the signal path, thereby reducing power dissipation and saving power.

44. (New) The method of claim 43, wherein reducing power dissipation reduces a power drain from a battery in the battery-powered portable wireless device.

45. (New) The method of claim 32, wherein when the desired signal strength is low and the receiver is operating at better than the worst-case operating signal condition by having the interferer strength lower than that in the worst case operating signal condition, dynamically reducing the bias of one or more of the plurality of circuits in the signal path of the receiver, thereby reducing power dissipation and saving power; and

wherein when the interferer signal strength is high and the receiver is operating at better than the worst-case operating signal condition by having the desired signal higher than that in the worst case operating signal condition, dynamically increasing the impedance of one or more of

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the plurality of circuits in the signal path of the receiver, thereby reducing power dissipation and saving power.

46. (New) A method of power dissipation optimization in a receiver of a wireless transceiver of a wireless communication device based on its operating signal conditions, wherein the transceiver has a signal path comprising a plurality of circuits designed to function under operating signal conditions that vary based on relative signal strengths of an interferer signal and a desired signal in a received wireless signal, wherein operating conditions vary between a worst-case operating signal condition, wherein the receiver operates with a maximum power dissipation when a desired signal strength is low and an interferer signal strength is high and a best-case operating signal condition, wherein the receiver operates with minimum power dissipation when the desired signal strength is high and the interferer signal strength is low, the method comprising:

receiving the wireless signal having the desired signal and the interferer signal by the receiver;

determining the desired signal strength;

determining the interferer signal strength;

comparing the desired signal strength to the interferer signal strength to determine an operating signal condition of the receiver;

based on the comparing, when the receiver operating signal condition is better than the worst case operating signal condition, dynamically adjusting one or more of an impedance, a bias, or a gain of one or more of the plurality of circuits in the receiver signal path, thereby optimizing power consumption to save power.

47. (New) The method of claim 46, wherein power saving occurs when the desired signal strength is low and the operating signal condition is better than the worst-case operating signal condition, by dynamically reducing the bias current of one or more of the plurality of circuits in the signal path of the receiver, thereby reducing power dissipation.

48. (New) The method of claim 47, wherein power saving occurs when the operating signal condition improves when the strength of the interferer signal decreases over time, and the

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bias current is reduced by dynamically adjusting the bias current of one or more of the plurality of circuits in the signal path of the receiver.

49. (New) A method of power dissipation optimization in a receiver of a wireless transceiver of a wireless communication device based on its operating signal conditions, wherein the transceiver has a signal path comprising a plurality of circuits designed to function under operating signal conditions that vary based on relative signal strengths of an interferer signal and a desired signal in a received wireless signal received, wherein the operating signal conditions vary between a worst-case operating signal condition and a best-case operating signal condition, wherein in the worst-case operating signal condition the receiver operates with a maximum power dissipation when a desired signal strength is low and an interferer signal strength is high, and wherein in the best-case operating signal condition the receiver operates with minimum power dissipation when the desired signal strength is high and the interferer signal strength is low, the method comprising:

receiving the wireless signal having the desired signal and the interferer signal by the receiver;

determining the desired signal strength;

determining the interferer signal strength;

comparing the desired signal strength to the interferer signal strength;

determining an operating signal condition of the receiver between the best and worst-case operating signal conditions based on the comparing;

when the interferer signal strength is high and the operating signal condition is better than the worst-case operating signal condition, dynamically increasing an impedance of one or more of the plurality of circuits in the signal path of the receiver, thereby reducing power dissipation.

50. (New) The method of claim 49, wherein when the desired signal strength increases over time resulting in an improvement in the operating condition, dynamically adjusting the impedance of one or more of the plurality of circuits in the signal path of the receiver results in power saving.

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51. (New) The method of claim 38, wherein when the desired signal strength is low and the operating signal condition of the receiver is better than the worst-case operating signal condition and the interferer signal strength is increasing, dynamically increasing a bias current of at least one of the plurality of circuits in the receiver signal path of the wireless transceiver, optimizing the power dissipation;

wherein when the desired signal strength is low and the operating signal condition of the receiver is better than the worst-case operating condition and the interferer signal strength reduces over time, dynamically decreasing a bias current of at least one of the plurality of circuits in the receiver signal path of the wireless transceiver, optimizing the power dissipation, and

wherein optimizing the power dissipation under better than the worst-case operating signal condition saves power with respect to the maximum power dissipation of the worst-case operating signal condition.

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REMARKS

The Final Office Action mailed April 12, 2019 has been carefully considered. In this Amendment, claims 25, 31 and 33-37 have been cancelled, claims 21-24, 26-27, 29-30, 32, and 38-39 have been amended, and claims 40-51 have been added. Reconsideration in view of the following remarks is respectfully requested.

Rejection Under 35 U.S.C. § 112, First Paragraph

Claims 31 and 37 stand rejected under 35 U.S.C. § 112, first paragraph, as allegedly containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the art to which it pertains or with which it is mostly nearly connected, to make and/or use the invention. This rejection is traversed. Applicant disagrees with the Examiner's characterization. Nevertheless, Applicant has cancelled claims 31 and 37 to advance prosecution of the application. Applicant accordingly requests withdrawal of the rejections under 35 U.S.C. § 112, first paragraph.

Rejections under 35 U.S.C. § 102 and 35 U.S.C. § 103

Claims 31, 32, 38 and 39 stand rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by U.S. Patent No. 6,311,048 to Loke (hereinafter, "Loke"), Claims 21, 22, 25, 27 and 30 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over U.S. Patent No. 5,001,776 to Clark (hereinafter, "Clark") in view of Loke, Claims 23, 24, 26 and 29 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Clark in view of Loke and further in view of U.S. Patent No. 6,870,425 to Leifso et al. (hereinafter, "Leifso"), Claims 33-35 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Loke in view of Clark, Claim 36 stands rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over

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Loke in view of Official Notice, and Claim 37 stands stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Loke in view of U.S. Patent No. 5,406,635 to Jarvinen (hereinafter "Jarvinen"). These rejections are traversed.

As explained above, claims 25, 31 and 33-37 have been cancelled. Independent claims 21, 25, 26-27, 29-30, 32, and 38-39 are patentable over the cited art as set forth above.

None of the sited prior art teach or suggest dynamically adjusting, dynamically decreasing or dynamically increasing one or more of a bias, a gain, an impedance of one or more of the circuits in the receiver path, as claimed. In a related district court proceeding, the court construed "dynamically adjusted" to mean "adjust[ed] during operation without reliance upon a signal strength threshold." This limitation is not disclosed in the prior art.

Loke fails to teach or suggest "determining the strength of the received interferer signal; comparing the strength of the desired signal relative to the strength of the interferer signal strength; based on the comparing, when the plurality of circuits are determined to be functioning at better than the worst-case operating signal condition, dynamically adjusting at least one of an impedance, a bias current or a gain of one or more of the amplifier, filter or mixer in the signal path of the receiver, thereby reducing power consumption to save power" as required by claim 32. Loke fails to teach or suggest "determining a strength of the interferer signal; comparing the strength of the desired signal relative to the strength of the interferer signal; and based on the comparing, when the plurality of circuits are determined to be functioning at better than the worst-case operating condition, dynamically adjusting at least one of an impedance, a bias current or a gain of one or more of the amplifier, filter or mixer in the signal path of the receiver to optimize power dissipation and save power," as required by claim 38. Loke fails to teach or suggest determining a strength of the interferer signal; comparing the strength of the desired

signal relative to the strength of the interferer signal; and wherein when the strength of the interferer signal is low and when the strength of the desired signal is higher than the desired signal strength of the worst-case operating signal condition, dynamically adjusting an impedance of at least one of the plurality of circuits in the signal path to reduce power dissipation. as required by claim 39.

The examiner is incorrect in equating the RSSI described in Loke as the interferer signal of the claims. RSSI, "Received Signal Strength Indicator", is a common name for signal strength in a wireless network environment. RSSI is typically a measure of the total signal received (desired signal, interferer signal and noise). See Exhibit A. A measure of RSSI is not a determination of the strength of the interference signal *and* a determination of the strength of the desired signal, as claimed.

Further, in Loke, the control loop uses the transmit channel output power information from the TX automatic gain control (AGC) in addition to the mode of operation and received signal strength to selectively adjust the IP3 value and control linearity of the receiver. See Loke, col. 2 lines 6-11; col. 3, lines 19-29; Fig 1 (Tx power control input to decision logic 118 from CDMA processor 116); and, Fig 2 (control loop flow comprising blocks 214 to 224). In the present invention, the TX output power level information is not necessary for operation. In the present application, by contrast, the adjustment of the impedance, gain and/or bias is a result of a comparison of the strengths of the desired and interferer signals.

Loke also uses a threshold value to determine if interference mandates switching to a high bias condition. In Loke, the RSSI has to be greater than the Ec/Io value plus a "false alarm" threshold in order for Loke's control circuit to determine if interference is present and switch to a high linearity state. See Loke col. 3, lines 54-56; and Fig. 2 (block 210). Embodiments of the

invention do not rely on such thresholds. By contrast, embodiments of the invention determine the strength of the desired signal, determine the strength of the interference signal, and perform a comparison of the strengths of the desired and interference signals. No such comparison of the strength of the desired signal and the strength of the interference signal is disclosed in Loke.

Further, Loke changes the LP3 value of the LNA-mixer combination selectively based on the threshold or switches to different LNAs having different LP3 values based on the threshold. See Loke col. 3, lines 21-29. By contrast, embodiments of the present application require dynamically adjusting the bias, gain or impedance of at least one of the plurality of circuits in the signal path of the receiver based on the operating condition of the receiver as determined by the comparison of desired and interferer signals to optimally control the power dissipation without the need for threshold(s).

Clark in combination with Loke fails to teach or suggest "determining a strength of the desired signal; determining a strength of the interferer signal; comparing the strength of the desired signal to the strength of the interfere signal; and dynamically adjusting at least one of an impedance, a bias or a gain of at least one of the amplifier, filter or mixer in the receiver signal path, responsive to the comparing" as required by claim 21. Clark in combination with Loke fails to teach or suggest "determining a strength of the received desired signal; determining a strength of the received interferer signal; comparing the strength of the received desired signal relative to the strength of the received interferer signal; based on the comparing, determining a functioning condition of the plurality of circuits; and when the plurality of circuits are determined to function at a better than the worst case condition in which the strength of the interferer signal is low and the strength of the desired signal is low, causing a bias current of one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be

dynamically decreased relative to the worst-case condition, thereby saving power" as required by claim 27. Clark in combination with Loke fails to teach or suggest "determining the strength of the received desired signal; determining the strength of the received interferer signal; comparing the strength of the received desired signal relative to the strength of the received interferer signal; and when the received interferer signal strength is high and the received desired signal strength is low, causing a bias current of one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be dynamically increased, controlling the power dissipation of the receiver" as required by claim 30.

Clark generally discloses a method of controlling the power consumption of a receiver (of a transceiver) based on the level of the desired signal and the level of all signals received. However, Clark specifically discloses that a "first threshold" and a "second threshold" are used for controlling the power consumption of the receiver. See, for example, Fig. 2 and Claim 1 of Clark. In Clark, the desired signal is compared to the first threshold, which is determined after the received signal has been mixed. The received signal is compared to the second threshold, which is determined before the signal has been mixed. Additionally, in Clark, since each threshold causes two outcomes (high or low), there are four total outcomes of this controlling method, as shown in TABLE 1 of Clark. Thus, in Clark, there are only two Operating Mode Currents: High and Low. This is confirmed by Fig. 2 of Clark, which shows only a Low Current Mode and a High Current Mode.

The presently pending claims do not rely on a comparison of the desired and undesired (interferer) signals to thresholds; instead, the method requires dynamically adjusting impedance or bias based on the relative comparison of the desired signal strength to the interferer signal

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strength. This allows for the receiver to operate at more than two operating mode currents, i.e., there are many more than four outcomes described in Clark.

Clark describes the aim of its invention as:

> **Accordingly, it is an object of the present invention to provide an Rf communication system transceiving devices capable of adapting their operation to minimize intermodulation distortion.**

Clark describes varying the amplification of the signals by varying the gain of the circuit and by using a square wave of varying amplitude from the local oscillator at the mixer to reduce the intermodulation distortion. The use of high gain in the amplifiers and high value square wave generation by the local oscillator result in high current drain from the battery and reduce battery life. Hence, Clark uses a two-step gain control and a feed back to the transmitting unit to increase the power of the desired signal so that the gain and amplitude of the local oscillator signals can be reduced to save power.

This is completely different from what is described and claimed in the present application. In embodiments of the present invention, the aim is the optimization of the power drain from the battery based on the relationship between the strength of interferer and the strength of desired signal in the radio frequency section of the transceiver. The adjustment is a ***dynamic change*** that is based on continuous monitoring of the interferer signal levels and desired signal levels to optimize the changes in gain, bias and impedance of the devices and circuits in the receiver path of the RF signal.

Fig.2 of Clark is a flow chart that shows that the desired signal strength and the input signal strength are used to switch the receiver between a high current mode and a low current mode. See Clark, Fig.2 (blocks 200, 202,204 and 206). Clark, similar to Loke, uses strength of the input signal and the desired signal as well as threshold settings to switch between high gain levels and low gain states to conserve power.

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Clark does not disclose changing or the use of bias and impedance for power optimization. Clark only uses the term gain once at col 4, lines 34-37: "Also, the **amplification factors** (and thus the current drain) of the RF amplifier 108 and the IF amplifier 122 may be varied (via control lines 138 and 140 respectively) by the controller 130."

The Examiner admits Clark does not specifically disclose comparing the first and second signal strength indication to one another. The Examiner contends Loke (figures 1 and 2) disclose comparing a first signal strength indication, wherein the first signal strength indication is relative to the strength of the received signal (RSSI); determining a second signal strength indication, wherein the second signal strength indication is relative to the strength of the signal after reducing the interferer signal (Ec/lo) to one another, and adjusting at least one of an impedance, a bias or a gain of at least one of the amplifier, filter or mixer in the signal path, responsive to the relative changes in the strength of the first and second signal strength indication (column 2, line 39 - column 4, line 40). The Examiner contends it would have been obvious for one having ordinary skill in the art at the time the invention was made to adapt the teaching of comparing the first and second signal strength indications of Loke to the method of Clark as a system design preference for performing the same function as controlling and adjusting the bias of the amplifier to improve power consumption in the receiver. The Examiner provides no support for his contention that it would be a system design preference for performing the same function as controlling and adjusting the gain of the amplifier and power consumption in the receiver and has therefore failed to set forth a prima facie case of obviousness. The fact that the Examiner cannot point to support for the motivation to combine suggests the Examiner is relying on impermissible hindsight for the motivation.

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Clark in combination with Loke and Leifso fails to teach or suggest "determining the strength of the desired signal; determining the strength of the interferer signal; comparing the strength of the desired signal relative to the strength of the interferer signal; and based on the comparison, ***dynamically adjusting*** one or more of an impedance, a bias or a gain of one or more of the plurality of circuits in the signal path, thereby controlling power dissipation" as required by claim 26. Clark in combination with Loke and Leifso fails to teach or suggest "determining a strength of the desired signal; determining a strength of the interferer signal; comparing the strength of the desired signal relative to the strength of the interferer signal; based on the comparing, determining a functioning condition of the plurality of circuits; and when the plurality of circuits are determined to function at a better than the worst case condition in which the strength of the interferer signal is low and the strength of the desired signal is high, causing an impedance of one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be ***dynamically increased*** relative to the worst-case condition, thereby saving power" as required by claim 29.

The Examiner admits Clark does not disclose when the indicated strength of the desired signal decreases, increasing an impedance of at least one of the plurality of circuits in the signal path. The Examiner admits Clark and Loke do not specifically disclose wherein when the indicated interferer signal strength decreases, and the indicated strength of the desired signal decreases increasing an impedance of at least one of the plurality of circuits in the signal path. The Examiner contends that Leifso discloses adjusting a gain of an amplifier by changing an impedance of at least one of the plurality of circuits in the signal path (column 6, line 26 - column 8, line 15). The Examiner contends that it would have been obvious for one having ordinary skill in the art at the time the invention was made to adapt the teaching of adjusting the

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gain of the amplifier and adjusting the impedance of Leifso et al. to the method of Clark and Loke as a system design preference for performing the same function as controlling and adjusting the gain of the amplifier and power consumption in the receiver. Applicants respectfully disagree. The Examiner provides no support for his contention that it would be a system design preference for performing the same function as controlling and adjusting the gain of the amplifier and power consumption in the receiver and has therefore failed to set forth a prima facie case of obviousness. The fact that the Examiner cannot point to support for the motivation to combine suggests the Examiner is relying on impermissible hindsight for the motivation.

Leifso generally discloses amplifier gain control using variable bias and degeneration transistors. In Leifso, the aim is to provide a variable gain amplifier capable of providing a linear amplification with high dynamic range for even the small signals received. See column 2, line 28 of Leifso. The examiner contends that Leifso shows that impedance can be adjusted, pointing to Fig 4 of Leifso, which shows an impedance adjustment of a circuit. However, Leifso does not teach or disclose ***dynamically adjusting/changing*** impedance of at least one of the plurality of circuits of the signal path of a wireless receiver to reduce battery power consumption where ***dynamically adjusting*** an impedance in the current application is for changing a load impedance seen by the circuit and hence change an output current of the circuit, as claimed. Impedance change in the present application is not to cause a change in gain of an amplifier as described in Leifso. Furthermore, Leifso discusses only changes in the gain of the amplifier. In particular, Leifso discusses changing the bias or impedance to change the gain of an amplifier. This however does not change the impedance of the load circuit of the signal path of the receiver, as occurs in the present application.

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In addition, Leifso uses the pair of degeneration transistors to provide the variable bias control for controlling the gain of the RF or IF amplifier. Leifso does not disclose any relationship to the interferer signal strength or desired signal strength in deciding the gain control. Liefso does not disclose any determination of interferer signal strength or desired signal strength. And, embodiments of the present invention do not use degeneration circuitry as disclosed in Leifso.

Hence, combining Clark, which teaches gain switching in an amplifier between a high and low values, and Loke, which teaches changing IP3 status of a receiver based on threshold over desired signal strength, with Leifso, which teaches using a pair of regeneration transistors as part of the gain control, without any reference to the interferer signal strength and desired signal strength and their inter-relationship, does not disclose the claimed embodiments.

Moreover, Applicant respectfully traverses the Examiner's Official Notice. If the Examiner continues to rely on this unsupported contention, Applicants respectfully request the Examiner to provide support. See, *In re Zurko*, 258 F.3d 1379, 59 U.S.P.Q.2d 1693 (Fed. Cir. 2001) (holding that the USPTO must point to some concrete evidence in the record to support core factual findings in a determination of patentability); Memorandum by Stephen G. Kunin, Deputy Commissioner for Patent Examination Policy (February 21, 2002)(stating that it is never appropriate to rely on common knowledge without evidentiary support as sole or principal evidence on which to base rejection); 37 C.F.R. § 1.104 (providing that when a rejection in an application is based on facts within the personal knowledge of an Examiner, the data should be stated as specifically as possible, and the facts must be supported, when called for by the applicant, by an affidavit from the Examiner); MPEP § 2144.03 (providing that the Examiner may only take official notice of facts outside of the record which are capable of instant and

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unquestionable demonstration as being "well-known" in the art and, if the Applicant traverses such an assertion, the Examiner should cite a reference in support of his or her position.).

Thus, the cited art fails to disclose all of the limitations of independent claims 21, 24, 26-27 and 29-30, 32 and 38-39. Claims 22-23 depend, directly or indirectly, from one of the foregoing independent claims. Applicant accordingly requests withdrawal of the rejections under 35 U.S.C. § 102 and/or 35 U.S.C. § 103.

New Claims

Claims 40-51 have been added to further particularly point out and distinctly claim the subject matter regarded as the invention. New claims 40-45 and new claim 51 depend, directly or indirectly, from one of the independent claims addressed above and are patentable for at least the same reasons discussed above. New claims 46-50 are also patentable over the cited art. Applicant accordingly submits new claims 40-51 are patentable for at least the same reasons discussed above.

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CONCLUSION

In view of the preceding discussion, Applicant respectfully urges that the claims of the present application define patentable subject matter and should be passed to allowance.

If the Examiner believes that a telephone call would help advance prosecution of the present invention, the Examiner is kindly invited to call the undersigned attorney at the number below.

The Commissioner is authorized to charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 50-4166.

Respectfully submitted,
NIXON PEABODY LLP

Dated: October 11, 2019

/Jennifer Hayes/
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EXHIBIT A

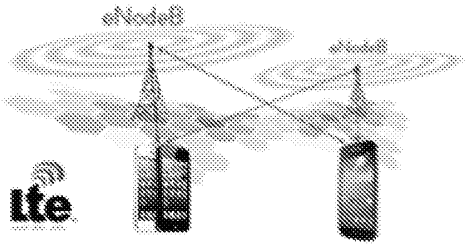
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LTE RSSI, RSRP and RSRQ Measurement

RSRP and RSRQ Measurement in LTE

RSRP and RSRQ are key measures of signal level and quality for modern LTE networks. In cellular networks, when a mobile moves from cell to cell and performs cell selection/reselection and handover, it has to measure the signal strength/quality of the neighbor



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cell.

In LTE network, a UE measures two parameters on reference signal: RSRP (Reference Signal Received Power) and RSRQ (Reference Signal Received Quality).

In LTE network, a UE measures two parameters on reference signal:

RSSI – Received Signal Strength Indicator: The carrier RSSI (Received Signal Strength Indicator) measures the average total received power observed only in OFDM symbols containing reference symbols for antenna port 0 (i.e., OFDM symbol 0 & 4 in a slot) in the measurement bandwidth over N resource blocks.

The total received power of the carrier RSSI includes the power from co-channel serving & non-serving cells, adjacent channel interference, thermal noise, etc. Total measured over 12-subcarriers including RS from Serving Cell, Traffic in the Serving Cell

RSRP – Reference Signal Received Power: RSRP is a RSSI type of measurement, as follows there are some definition of it and some details as well.
It is the power of the LTE Reference Signals spread over the full bandwidth and narrowband.
A minimum of -20 dB SINR (of the S-Synch channel) is needed to detect RSRP/RSRQ

RSRQ – Reference Signal Received Quality: *Quality considering also RSSI and the number of used Resource Blocks (N) RSRQ = (N * RSRP) / RSSI measured over the same bandwidth. RSRQ is a C/I type of measurement and it indicates the quality of the received reference signal. The RSRQ measurement provides additional information when RSRP is not sufficient to make a reliable handover or cell reselection decision.*

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In the procedure of handover, the LTE specification provides the flexibility of using RSRP, RSRQ, or both.

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It must to be measured over the same bandwidth:

- Narrowband N = 62 Sub Carriers (6 Resource Blocks)
- Wideband N = full bandwidth (up to 100 Resource Blocks / 20 MHz)

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RSRP 3GPP Definition

__Reference Signal Received Power (RSRP)__, is defined as the linear average over the power contributions (in [W]) of the resource elements that carry cell-specific reference signals within the considered measurement frequency bandwidth.

For RSRP determination the cell-specific reference signals R0 according to TS 36.211 [3] shall be used. If the UE can reliably detect addition to R0 to determine RSRP.

The reference point for the RSRP shall be the antenna connector of the UE.

Or, even better, __Reference Signal Received Quality__ is defined as the ratio N×RSRP/(E-UTRA carrier RSSI), where N is the number of RB's of the E-UTRA carrier RSSI measurement bandwidth. __The measurements in the numerator and denominator shall be made over the same set of resource blocks.__

If receiver diversity is in use by the UE, the reported value shall not be lower than the corresponding RSRP of any of the individual diversity branches.

***Applicable for:** RRC_IDLE intra-frequency, RRC_IDLE inter-frequency, RRC_CONNECTED intra-frequency, RRC_CONNECTED inter-frequency*

***Note1:** The number of resource elements within the considered measurement frequency bandwidth and within the measurement period that are used by the UE to determine RSRP is left up to the UE implementation with the limitation that corresponding measurement accuracy requirements have to be fulfilled.*

***Note 2:** The power per resource element is determined from the energy received during the useful part of the symbol, excluding the CP.*

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In other words RSRP (Reference Signal Receive Power) is the average power of Resource Elements (RE) that carry cell specific Reference Signals (RS) over the entire bandwidth, so RSRP is only measured in the symbols carrying RS.

- RSRP is the average received power of a single RS resource element.
- UE measures the power of multiple resource elements used to transfer the reference signal but then takes an average of them rather than summing them.
- Reporting range -44...-140 dBm

RSRP does a better job of measuring signal power from a specific sector while potentially excluding noise and interference from other sectors.

RSRP levels for usable signal typically range from about -75 dBm close in to an LTE cell site to -120 dBm at the edge of LTE coverage.

RSRP mapping 3GPP TS 36.133 V8.9.0 (2010-03)

The reporting range of RSRP is defined from -140 dBm to – 44 dBm with 1 dB resolution.

The mapping of measured quantity is defined in the table.

Reported value	Measured quantity value	Unit
RSRP_00	RSRP < -140	dBm
RSRP_01	-140 ≤ RSRP < -139	dBm
RSRP_02	-139 ≤ RSRP < -138	dBm
...	...	...
RSRP_95	-46 ≤ RSRP < -45	dBm
RSRP_96	-45 ≤ RSRP < -44	dBm
RSRP_97	-44 ≤ RSRP	dBm

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RSRQ 3GPP Definition *Reference Signal Received Quality (RSRQ) is defined as the ratio NxRSRP/(E-UTRA carrier RSSI), where N is the number of RB's of the E-UTRA carrier RSSI measurement bandwidth. The measurements in the numerator and denominator shall be made over the same set of resource blocks.*

E-UTRA Carrier Received Signal Strength Indicator (RSSI), comprises the total received power (in [W]) observed only in OFDM symbols containing reference symbols for antenna port 0, in the measurement bandwidth, over N number of resource blocks by the UE from all sources, including co-channel serving and non-serving cells, adjacent channel interference, thermal noise etc.

The reference point for the RSRQ shall be the antenna connector of the UE. If receiver diversity is in use by the UE, the reported value shall not be lower than the corresponding RSRQ of any of the individual diversity branches.

Applicable for: *RRC_CONNECTED intra-frequency, RRC_CONNECTED inter-frequency*

RSRQ

In formula:

RSRQ = N x RSRP / RSSI

- N is the number of Physical Resource Blocks (PRBs) over which the RSSI is measured, typically equal to system bandwidth

Reported value	Measured quantity value	Unit
RSRQ_00	RSRQ < -19.5	dB
RSRQ_01	-19.5 ≤ RSRQ < -19	dB
RSRQ_02	-19 ≤ RSRQ < -18.5	dB
...	...	...
RSRQ_32	-4 ≤ RSRQ < -3.5	dB
RSRQ_33	-3.5 ≤ RSRQ < -3	dB
RSRQ_34	-3 ≤ RSRQ	dB

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- RSSI is pure wideband power measurement including intracell power, interference and noise
- RSRQ is defined from -3...-19.5dB

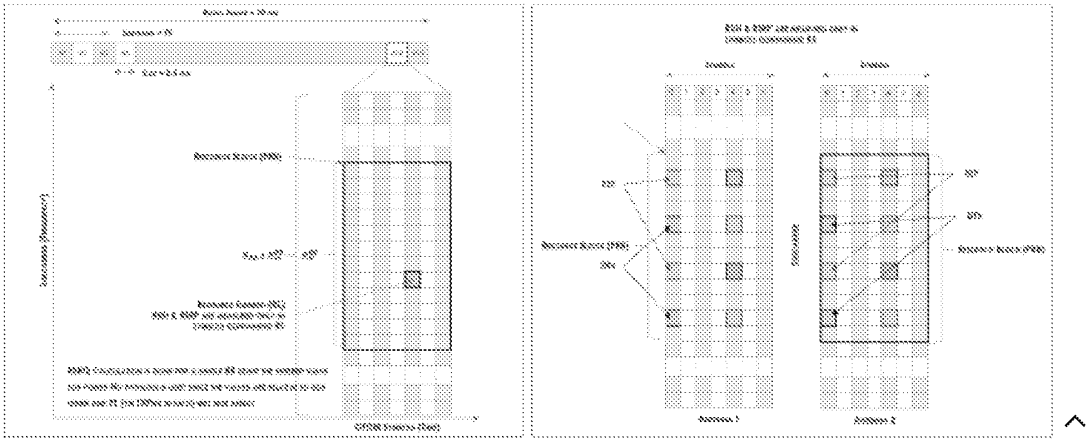
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Reference Signals recap: OFDMA Channel Estimation

In simple terms the Reference Signal (RS) is mapped to Resource Elements (RE). This mapping follows a specific pattern (see to below).

So at any point in time the UE will measure all the REs that carry the RS and average the measurements to obtain an RSRP reading.

- Channel estimation in LTE is based on reference signals (like CPICH functionality in WCDMA)
- Reference signals position in time domain is fixed (0 and 4 for Type 1 Frame) whereas in frequency domain it depends on the Cell ID
- In case more than one antenna is used (e.g. MIMO) the Resource elements allocated to reference signals on one antenna are DTX on the other antennas
- Reference signals are modulated to identify the cell to which they belong.



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RSSI (Received Signal Strength Indicator) is a parameter which provides information about total received wide-band power (measure in all symbols) including interference and thermal noise.

RSSI is not reported to Node B by UE. It can simply be computed from RSRQ and RSRP that are reported by UE.

RSSI = wideband power = noise + serving cell power + interference power

So, without noise and interference, we have that 100% DL PRB activity: **RSSI=12*N*RSRP**

Where:

- **RSRP is the received power of 1 RE (3GPP definition)** average of power levels received across all Reference Signal symbols within the considered measurement frequency bandwidth
- **RSSI is measured over the entire bandwidth**
- **N: number of RBs across the RSSI** is measured and depends on the BW

Based on the above, under full load and high:

SNR: RSRP (dBm)= RSSI (dBm) -10*log (12*N)

So we have:

RSRQ = RSRP / (RSSI/N)

- **N = Number of PRBs (Physical Resource Blocks)**

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RSSI = noise + serving cell power + interference power during RS symbol

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So we see that RSRQ depends on serving cell power and the number of Tx antennas

Impact of serving cell power to RSRQ:

Example for noise limited case (no interference): If all resource elements are active and are transmitted with equal power, then Q

RSRQ = N / 12N = -10.8 dB for 1Tx

RSRQ = N / 20N = -13 dB for 2Tx taking DTX into account

(because RSRP is measured over 1 resource element and RSSI per resource block is measured over 12 resource elements).

Remember that RSSI is only measured at those symbol times during which RS REs are transmitted – We do not have to take into the count DTx!!!

So, when there is no traffic, and assuming only the reference symbols are transmitted (there are 2 of them within the same symbol of a resource block) from a single Tx antenna then the RSSI is generated by only the 2 reference symbols so the result becomes

RSRQ = N / 2N = -3 dB for 1Tx

RSRQ = -6dB for 2Tx

SINR DefinitionSINR is the reference value used in the system simulation and can be defined:

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2. SINR for a specific subcarriers (or for a specific resource elements)

SINR = S/(I+N), all measured over the same bandwidth

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SNR vs. RSRP

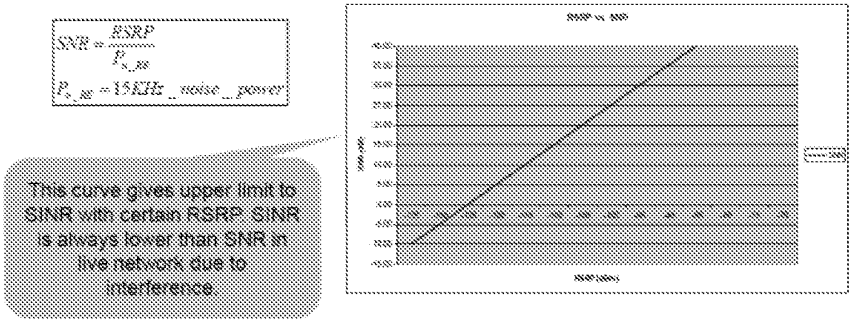
RSRP is measured for a single subcarrier, noisepower for 15KHz= -125.2dBm

1. *Noise figure = 7 dB*
2. *Temperature = 290 K*

Assumption: RSRP doesn't contain noise power

$$SNR = \frac{RSRP}{P_{n\_RE}}$$

$$P_{n\_RE} = 15KHz\_noise\_power$$



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EXAMINER
VUONG, QUOCHIEN B

ART UNIT	PAPER NUMBER
2649	

DATE MAILED: 11/13/2019

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/824,841	11/28/2017	Yannis Tsividis	084820-000002US10	4819

TITLE OF INVENTION: Power Dissipation Reduction in Wireless Transceivers

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$500	$0.00	$0.00	$500	02/13/2020

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

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(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/824,841	11/28/2017	Yannis Tsividis	084820-000002US10	4819

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nonprovisional	SMALL	$500	$0.00	$0.00	$500	02/13/2020

EXAMINER	ART UNIT	CLASS-SUBCLASS
VUONG, QUOCHIEN B	2649	455-574000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

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Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

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5. **Change in Entity Status** (from status indicated above)

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❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

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EXAMINER	
VUONG, QUOCHIEN B	
ART UNIT	PAPER NUMBER
2649	

DATE MAILED: 11/13/2019

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

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OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	**Application No.** 15/824,841	**Applicant(s)** Tsividis, Yannis	
	Examiner QUOCHIEN B VUONG	**Art Unit** 2649	**AIA (FITF) Status** No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to 10/11/2019.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 21-24,26-27,29-30,32 and 38-51 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☑ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/QUOCHIEN B VUONG/
Primary Examiner, Art Unit 2649

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Notice of References Cited	Application/Control No. 15/824,841	Applicant(s)/Patent Under Reexamination Tsividis, Yannis	
	Examiner QUOCHIEN B VUONG	Art Unit 2649	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-6690922-B1	02-2004	Lindemann; Brian	H03G3/3047	455/67.11
*	B	US-9350313-B2	05-2016	Wilhelmsson; Leif	H03G3/3078	1/1
	C					
	D					
	E					
	F					
	G					
	H					
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/824,841	Tsividis, Yannis
	Examiner	**Art Unit**
	QUOCHIEN B VUONG	2649

CPC						
Symbol					**Type**	**Version**
H04W	/	52	/	0209	F	2013-01-01
H04B	/	1	/	109	I	2013-01-01
Y02D	/	70	/	40	A	2018-01-01
Y02D	/	70	/	142	A	2018-01-01
Y02D	/	70	/	00	A	2018-01-01

CPC Combination Sets							
Symbol					**Type**	**Set**	**Ranking**	**Version**
	/		/					

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	23	
/QUOCHIEN B VUONG/ Primary Examiner, Art Unit 2649	05 November 2019	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1

U.S. Patent and Trademark Office — Part of Paper No.: 20191105

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Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/824,841	Tsividis, Yannis
	Examiner	**Art Unit**
	QUOCHIEN B VUONG	2649

INTERNATIONAL CLASSIFICATION					
CLAIMED					
H04B	/	1	/	38	
H04M	/	1	/	00	
NON-CLAIMED					
	/		/		

US ORIGINAL CLASSIFICATION	
CLASS	**SUBCLASS**
455	574

CROSS REFERENCES(S)						
CLASS	**SUBCLASS (ONE SUBCLASS PER BLOCK)**					
455	234.1	251.1	343.1			

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	23	
/QUOCHIEN B VUONG/ Primary Examiner, Art Unit 2649	05 November 2019	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1

U.S. Patent and Trademark Office — Part of Paper No.: 20191105

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Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/824,841	Tsividis, Yannis
	Examiner	**Art Unit**
	QUOCHIEN B VUONG	2649

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☑ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		10		19		28		37	19	46				
	2		11		20	12	29	16	38	20	47				
	3		12	1	21	13	30	18	39	21	48				
	4		13	2	22		31	4	40	22	49				
	5		14	3	23	14	32	5	41	23	50				
	6		15	6	24		33	8	42	17	51				
	7		16		25		34	9	43						
	8		17	7	26		35	10	44						
	9		18	11	27		36	15	45						

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 23	
/QUOCHIEN B VUONG/ Primary Examiner, Art Unit 2649 (Primary Examiner)	05 November 2019 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 1

U.S. Patent and Trademark Office — Part of Paper No.: 20191105

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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/824,841	Tsividis, Yannis
	Examiner	**Art Unit**
	QUOCHIEN B VUONG	2649

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☑ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	07/06/2018	04/08/2019	11/05/2019						
	1	-	-	-						
	2	-	-	-						
	3	-	-	-						
	4	-	-	-						
	5	-	-	-						
	6	-	-	-						
	7	-	-	-						
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	20	-	-	-						
1	21	✓	✓	=						
2	22	✓	✓	=						
3	23	✓	✓	=						
6	24	✓	✓	=						
	25	✓	✓	-						
7	26	✓	✓	=						
11	27	✓	✓	=						
	28	✓	-	-						
12	29	✓	✓	=						
13	30	✓	✓	=						
	31	✓	✓	-						
14	32		✓	=						
	33		✓	-						
	34		✓	-						
	35		✓	-						
	36		✓	-						
	37		✓	-						
16	38		✓	=						
18	39		✓	=						
4	40			=						
5	41			=						
8	42			=						

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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/824,841	Tsividis, Yannis
	Examiner	Art Unit
	QUOCHIEN B VUONG	2649

CLAIM		DATE								
Final	Original	07/06/2018	04/08/2019	11/05/2019						
9	43			=						
10	44			=						
15	45			=						
19	46			=						
20	47			=						
21	48			=						
22	49			=						
23	50			=						
17	51			=						

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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/824,841	Tsividis, Yannis
	Examiner	Art Unit
	QUOCHIEN B VUONG	2649

CPC - Searched*		
Symbol	Date	Examiner
H04B 1/16, 1/1607, 1/40, 17/318	07/06/2018	/QV/
H04W 52/52	07/06/2018	/QV/
H03F 1/56, 3/20, 2200/27, 2200/78, 2200/387, 2200/451	07/06/2018	/QV/

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner
455	63.1,67.13,127.1,127.2,127.5,226.1,226.2,232.1,234.1, 250.1,251.1,295,296,311,343.1,572,574	07/06/2018	/QV/
370	442	0706/2018	/QV/
330	127,134,144	07/06/2018	/QV/

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
EAST search	07/06/2018	/QV/
Inventor name search	07/06/2018	/QV/
Search updated	04/04/2019	/QV/
Search updated	11/04/2019	/QV/

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
455	234.1,574	11/04/2019	/QV/

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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/824,841	Tsividis, Yannis
	Examiner	Art Unit
	QUOCHIEN B VUONG	2649

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	12	"6311048".pn. "5001776".pn. "6870425".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/11/04 15:18
L2	550	(compar$3 with (RSSI (signal near4 (strength level quality))) with (interference noise)) same ((control$4 adjust$3) with (gain impedance bias))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/11/04 16:11
L3	68	2 and ((dynamic dynamically) with (control$4 adjust$3) with (gain impedance bias))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/11/04 16:55
L4	32	2 AND ((H03F2200/451 OR H03F2200/372 OR H03F2200/78 OR H03F3/20 OR H04B17/318 OR H04B17/345 OR H04B1/16).CPC.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/11/04 18:16
L5	37818	(signal-to-noise signal-to-interference (signal near6 (interference noise))) same ((adjust$3 control$4) near4 (gain impedance bias))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/11/04 19:06
L6	1386	5 same (compar$3 with signal with (noise interference))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/11/04 19:19
L7	1176	6 and (receiv$3 transceiver)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/11/04 19:20

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L9	0	(((reduc$3 sav$3) near6 (power battery)) with (receiver tranceiver) with (compar$3 with (RSSI (signal near4 (strength level quality))) with (interference noise)) with ((control$4 adjust$3) with (gain impedance bias)) with ((dynamic dynamically) near4 (control$4 adjust$3)) with (gain impedance bias)).clm.	US-PGPUB; USPAT	OR	ON	2019/11/04 20:15

11/4/2019 8:18:35 PM

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Yannis TSIVIDIS	Examiner:	Quochien B. VUONG
Application No.:	15/824,841	Art Unit:	2649
Filing Date:	November 28, 2017	Confirmation No.:	4819

Title: POWER DISSIPATION REDUCTION IN WIRELESS TRANSCEIVERS

Commissioner for Patents – MS Issue Fee
P.O. Box 1450
Alexandria, VA 22313-1450

APPLICANT'S COMMENTS ON REASONS FOR ALLOWANCE

These comments are responsive to the Notice of Allowance, mailed on November 13, 2019.

Applicant gratefully acknowledges the indication of allowance of Claims 21-24, 26-27, 29-30, 32 and 38-51. Applicant respectfully urges that additional and/or alternative reasons for allowance may exist apart from those advanced by the Examiner and the Applicants, and these reasons may each be independently sufficient to establish the patentability of the allowed claims.

Applicant respectfully reserves the right to introduce, articulate, or otherwise comment on any such additional reasons for allowance as may be appropriate in any future proceedings concerning the one or more claimed embodiments.

Please charge any additional required fee or credit any overpayment to our Deposit Account number 50-4166.

Respectfully submitted,

NIXON PEABODY LLP

Dated: November 21, 2019

/Jennifer Hayes/
Jennifer Hayes
Reg. No. 50,845

300 South Grand Avenue, Suite 4100
Los Angeles, CA 90071-3151
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Fax (213) 629-6001

4841-5137-8605.1
084820-000002US10

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Electronic Patent Application Fee Transmittal

Application Number:	15824841
Filing Date:	28-Nov-2017
Title of Invention:	Power Dissipation Reduction in Wireless Transceivers
First Named Inventor/Applicant Name:	Yannis Tsividis
Filer:	Jennifer NMN Hayes/Diana Girgis
Attorney Docket Number:	084820-000002US10

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	2501	1	500	500

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**500**

Electronic Acknowledgement Receipt	
EFS ID:	37823680
Application Number:	15824841
International Application Number:	
Confirmation Number:	4819
Title of Invention:	Power Dissipation Reduction in Wireless Transceivers
First Named Inventor/Applicant Name:	Yannis Tsividis
Customer Number:	106303
Filer:	Jennifer NMN Hayes/Diana Girgis
Filer Authorized By:	Jennifer NMN Hayes
Attorney Docket Number:	084820-000002US10
Receipt Date:	21-NOV-2019
Filing Date:	28-NOV-2017
Time Stamp:	17:15:59
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$500
RAM confirmation Number	E2019AKH16158818
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	2019-11-21-Issue-Fee-Transmittal-084820-002US10.pdf	88525 3ee45ba5c6eef98a45fd39352833c92ca1daebde	no	1
Warnings:					
Information:					
2	Miscellaneous Incoming Letter	2019-11-21-Comments-on-Allowance-084820-002US10.pdf	91175 18754abc787817f0a65916177129de68ca88f85a	no	1
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	30187 f9cbe312594b6851c3d30d2b042024695af692e6	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	209887		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

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106303 7590 11/13/2019
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/824,841	11/28/2017	Yannis Tsividis	084820-000002US10	4819

TITLE OF INVENTION: Power Dissipation Reduction in Wireless Transceivers

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$500	$0.00	$0.00	$500	02/13/2020

EXAMINER	ART UNIT	CLASS-SUBCLASS
VUONG, QUOCHIEN B	2649	455-574000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
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1 Jennifer Hayes
2 Nixon Peabody LLP
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: THETA IP, LLC

(B) RESIDENCE: (CITY and STATE OR COUNTRY): COPPELL, TEXAS

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ☒ Corporation or other private group entity ❑ Government

4a. Fees submitted: ☒ Issue Fee ❑ Publication Fee (if required) ❑ Advance Order - # of Copies _____

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5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

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NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
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Authorized Signature /Jennifer Hayes/ Date November 21, 2019

Typed or printed name Jennifer Hayes Registration No. 50,845

PTOL-85 Part B (08-18) Approved for use through 01/31/2020 OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

IPR2024-00818
Apple EX1002 Page 271

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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/824,841	12/31/2019	10524202	084820-000002US10	4819

106303 7590 12/11/2019

Nixon Peabody LLP
300 South Grand Avenue, Suite 4100
Los Angeles, CA 90071

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Yannis Tsividis, New York, NY;
Theta IP, LLC, Coppell, TX;

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AO 120 (Rev. 08/10)

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Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

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☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
	2/28/2020	for the Western District of Texas, Waco Division

PLAINTIFF	DEFENDANT
Theta IP, LLC	Samsung Electronics Co., Ltd.; Samsung Electronics America, Inc.; Samsung Telecommunications America, LLC

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	9,838,962	12/5/2017	Theta IP, LLC
2	10,129,825	11/13/2018	Theta IP, LLC
3	10,524,202	12/31/2019	Theta IP, LLC
4			
5			

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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3		
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AO 120 (Rev. 08/10)

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☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
22cv3441	06/30/2022	Northern District of Illinois/Eastern Division

PLAINTIFF	DEFENDANT
Theta IP, LLC	Motorola Mobility LLC, Lenovo (United States) Inc., Lenovo Group Limited

PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 See Attached		
2		
3		
4		
5		

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PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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3		
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DECISION/JUDGEMENT

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Thomas G. Bruton	David Jozwiak	07/05/2022

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Copy 2—Upon filing document adding patent(s), mail this copy to Director **Copy 4—Case file copy**

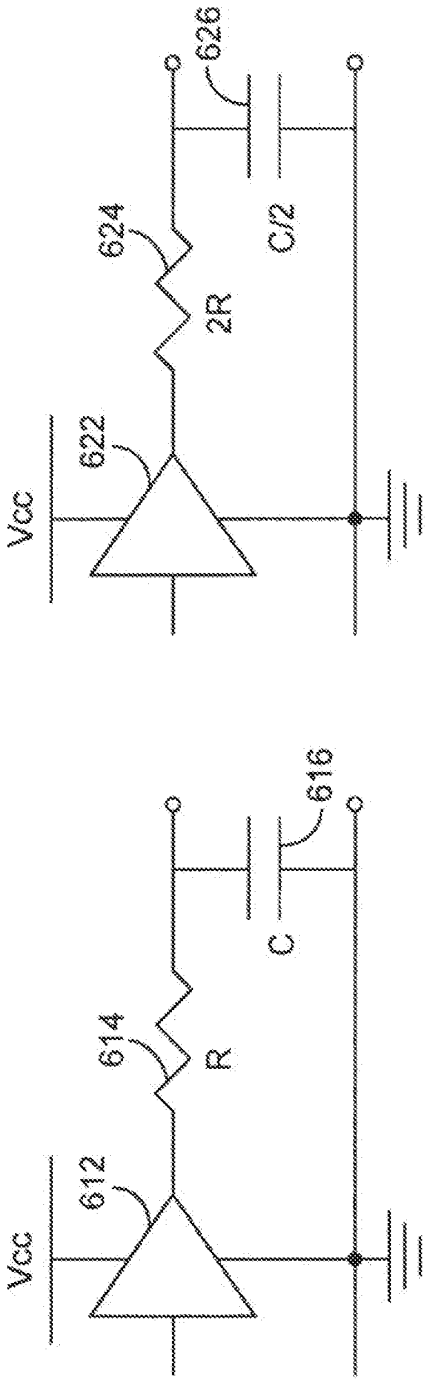


FIG. 6

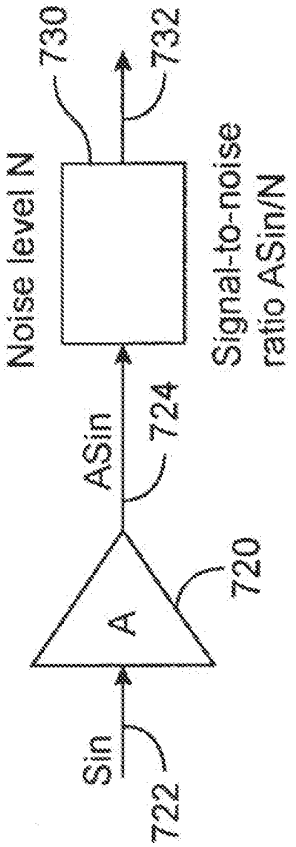

730
732
Noise level N
Signal-to-noise ratio ASin/N
ASin
724
A
720
Sin
722
710
Noise level N
Signal-to-noise ratio Sin/N
Sin
712

FIG. 7

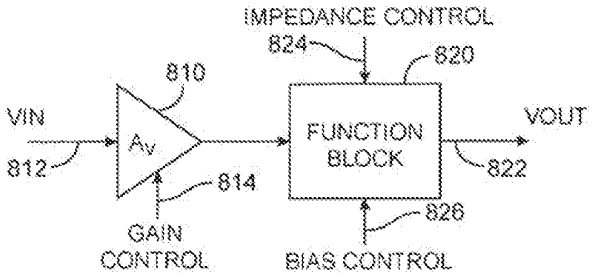


FIG. 8A

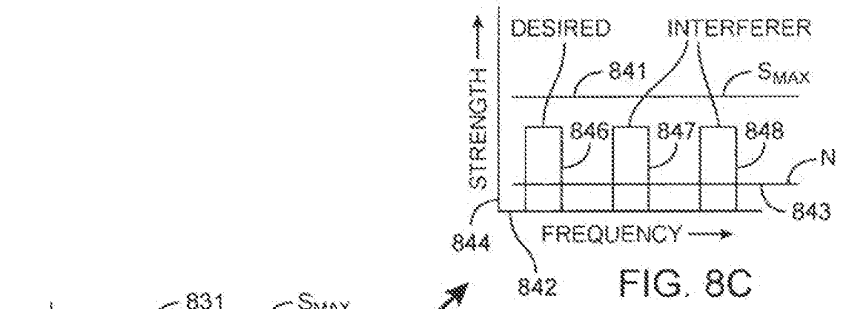


FIG. 8C

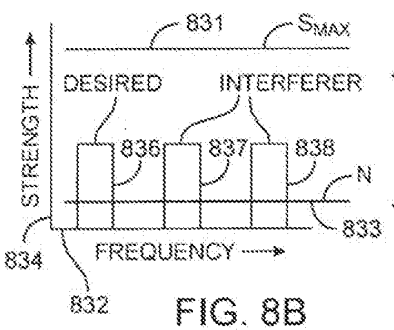


FIG. 8B

DECREASE BIASING

– AND/OR –

INCREASE GAIN AND IMPEDANCES

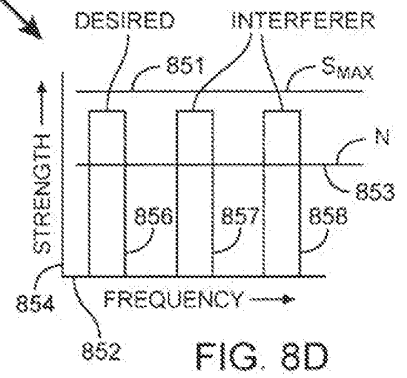


FIG. 8D

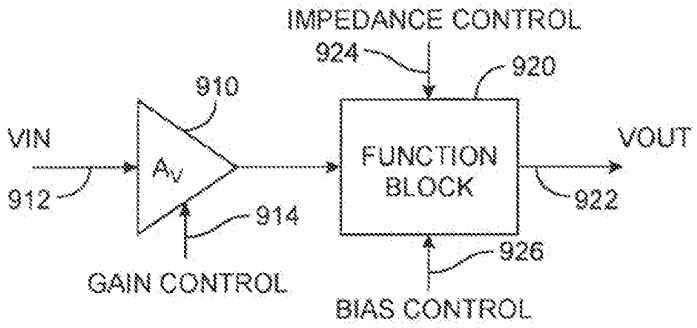


FIG. 9A

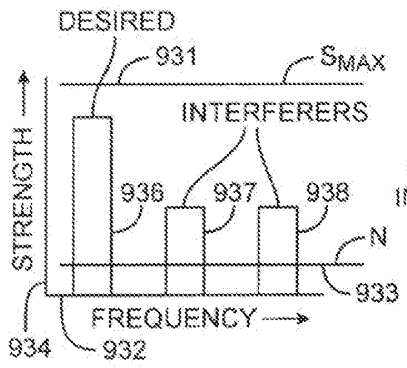


FIG. 9B

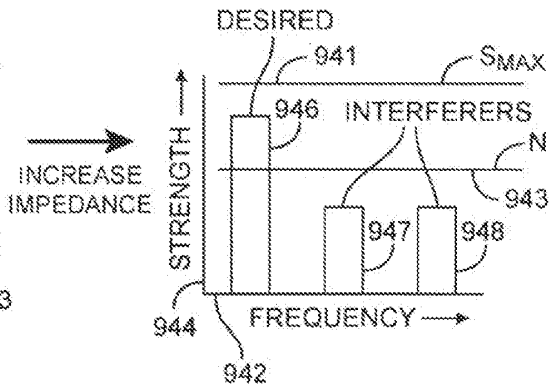


FIG. 9C

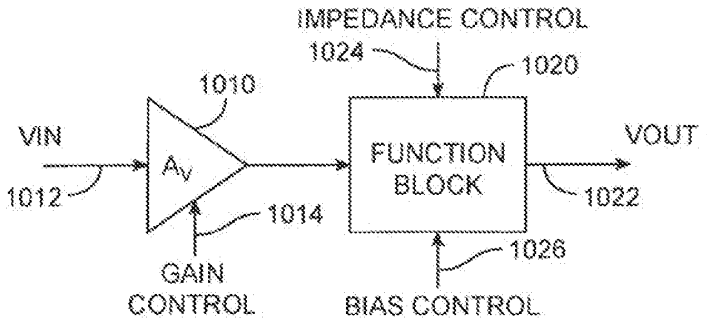


FIG. 10A

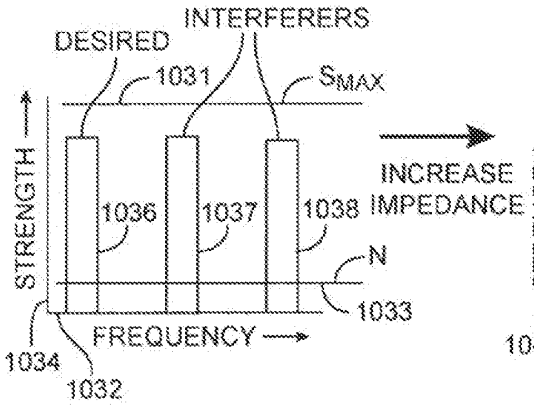


FIG. 10B

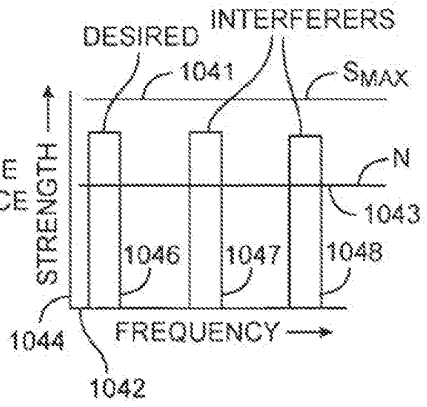


FIG. 10C

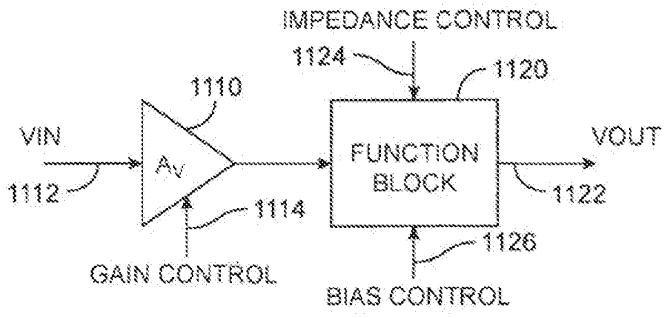


FIG. 11A

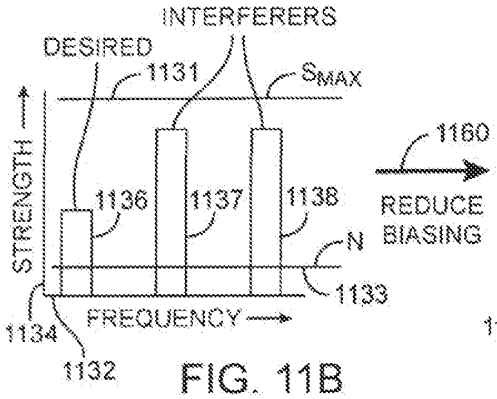


FIG. 11B

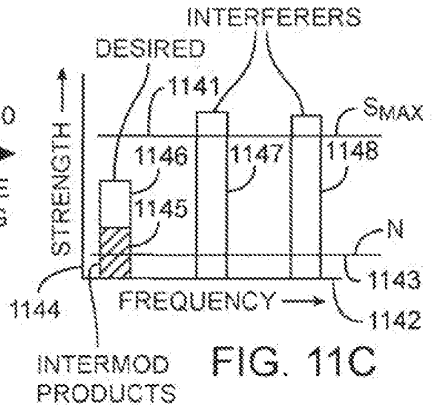


FIG. 11C

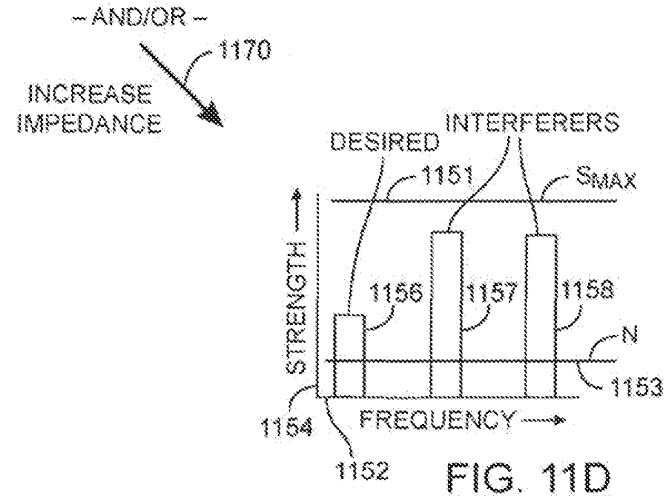


FIG. 11D

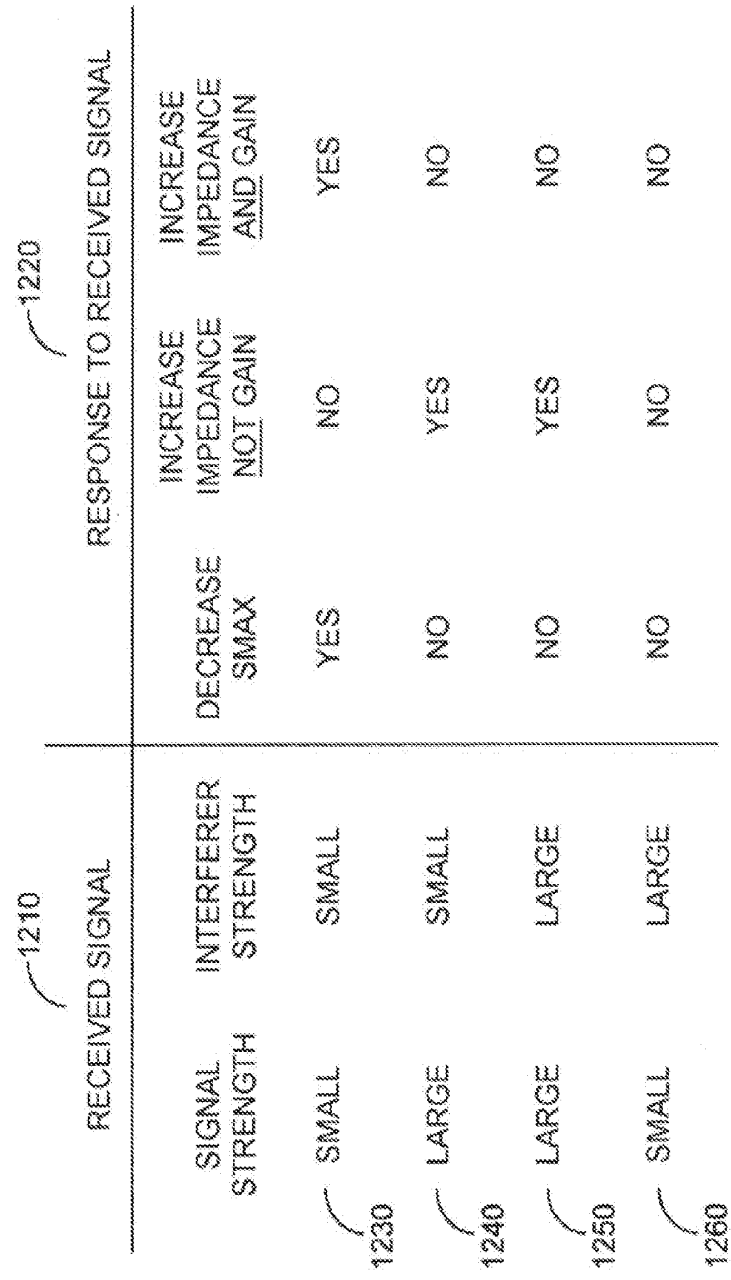

1210
RECEIVED SIGNAL
1220
RESPONSE TO RECEIVED SIGNAL
SIGNAL STRENGTH
INTERFERER STRENGTH
DECREASE SMAX
INCREASE IMPEDANCE NOT GAIN
INCREASE IMPEDANCE AND GAIN
SMALL
SMALL
YES
NO
YES
1230
LARGE
SMALL
NO
YES
NO
1240
LARGE
LARGE
NO
YES
NO
1250
SMALL
LARGE
NO
NO
NO
1260

FIG. 12

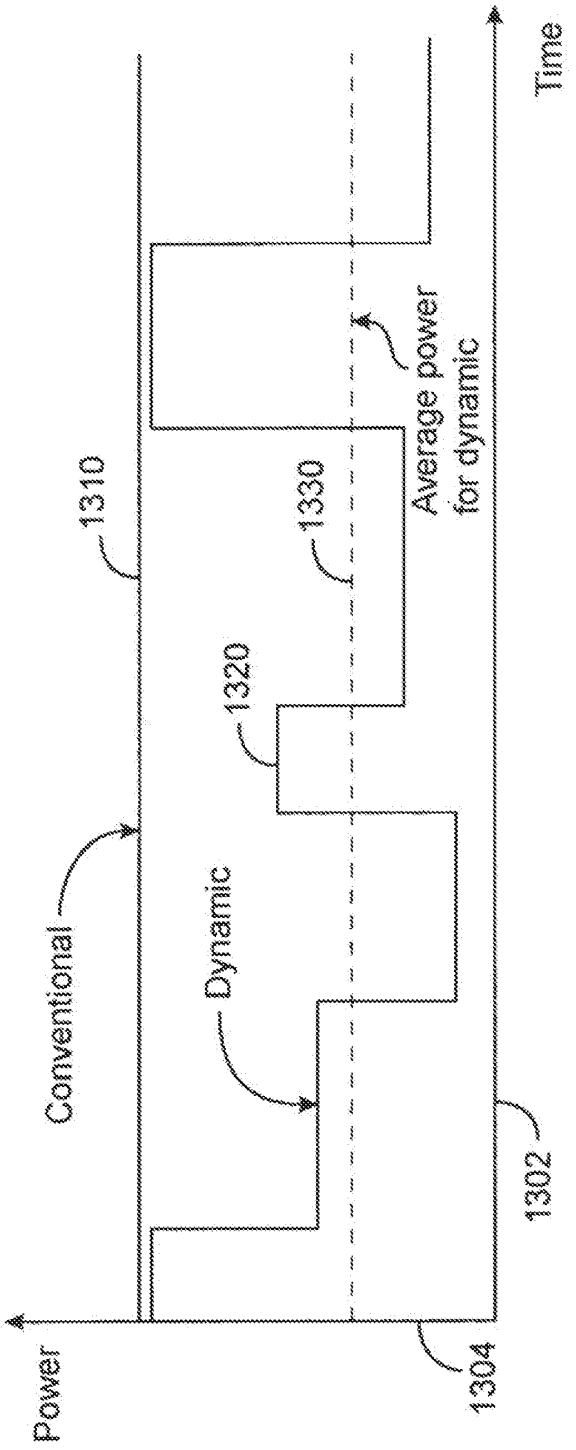

Power
Time
Conventional
Dynamic
1310
1320
1330
1302
1304
Average power
for dynamic

FIG. 13

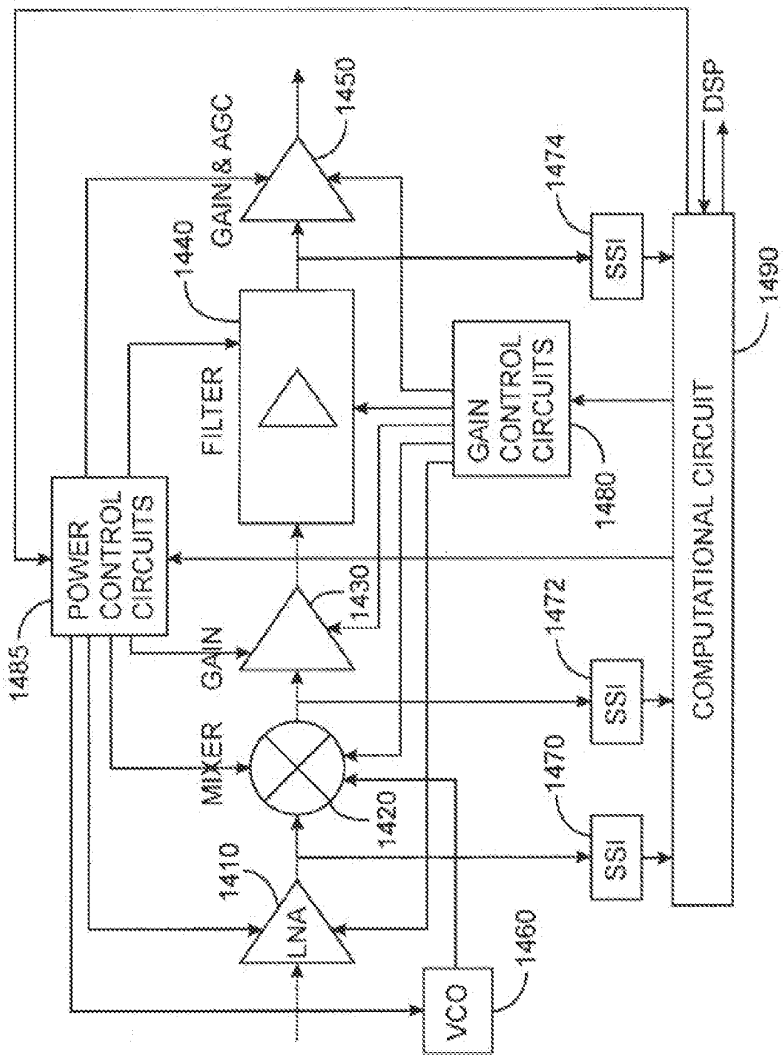

1450
GAIN & AGC
1440
FILTER
1474
SSI
DSP
1490
COMPUTATIONAL CIRCUIT
GAIN CONTROL CIRCUITS
1480
POWER CONTROL CIRCUITS
1485
1430
GAIN
1472
SSI
MIXER
1420
1470
SSI
1410
LNA
VCO
1460

FIG. 14

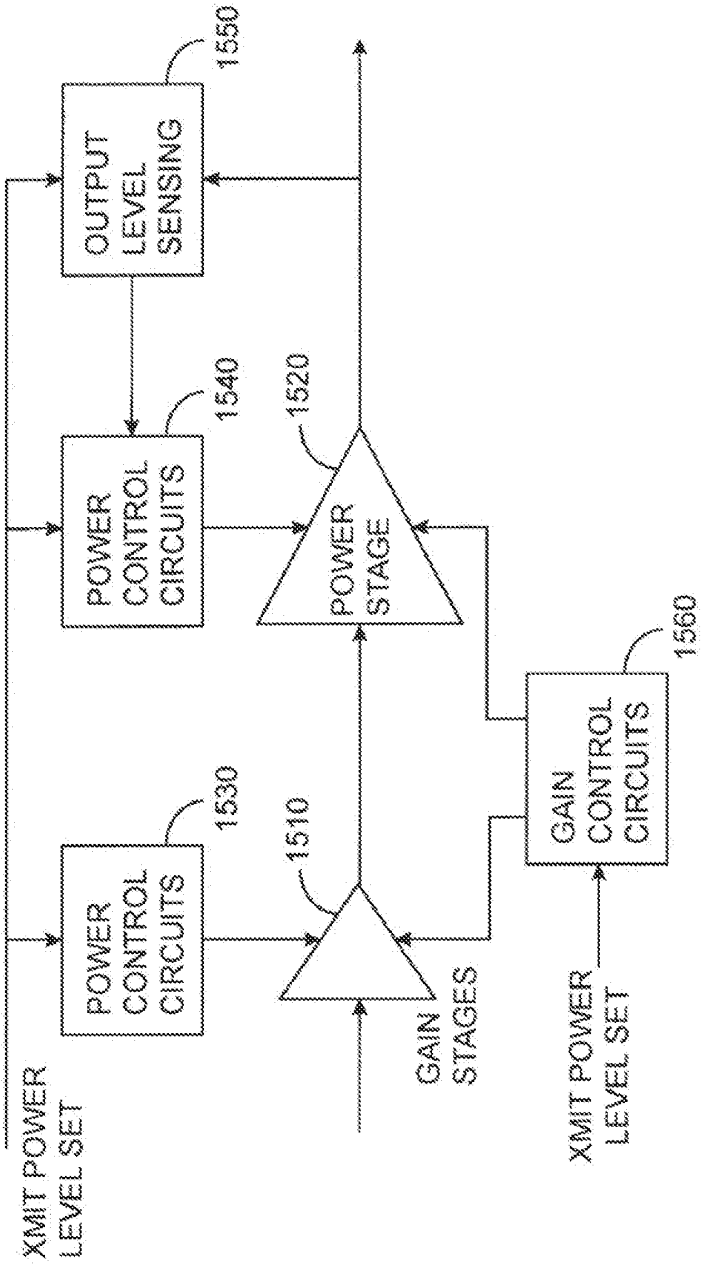

1550
OUTPUT LEVEL SENSING
1540
1520
POWER CONTROL CIRCUITS
POWER STAGE
1530
1510
1560
POWER CONTROL CIRCUITS
GAIN CONTROL CIRCUITS
XMIT POWER LEVEL SET
GAIN STAGES
XMIT POWER LEVEL SET

FIG. 15

Exhibit A

POWER DISSIPATION REDUCTION IN WIRELESS TRANSCEIVERS

CROSS-REFERENCES TO RELATED APPLICATIONS

This application claims the benefit of U.S. provisional application No. 60/451,229, filed Mar. 1, 2003, which is incorporated by reference.

This application is related to U.S. provisional application No. 60/451,230, filed Mar. 1, 2003, which is incorporated by reference.

BACKGROUND

The present invention relates to power dissipation reduction techniques for electronic circuits, for example wireless transceiver integrated circuits.

Wireless networking is quickly becoming ubiquitous, as desktop, notebook, and handheld computers are connected to share Internet access and files. Wireless networking cards compatible with PCMCIA and compact flash form factors are popular for laptops and handhelds respectively, particularly as mobile users connect to the Internet on the road at coffee shops, hotels, and airports.

A downside of this connectivity is a corresponding drain on battery life, especially for these portable devices. The power consumed by a wireless transmitter and receiver reduces the usefulness of a device and sends a user on a hunt for an electrical outlet for recharging.

One reason why this power drain is high is that electronic circuits are typically designed to function properly under worst-case operating conditions. For a wireless transceiver, the worst case condition is when a desired signal reception strength is low, while other transceivers or nearby electronic equipment generate interfering signals and other spurious noise.

But a wireless transceiver does not always operate in these worst-case conditions. For example, a base station, router or access point may be nearby such that the received signal is strong. Also, there may be no interfering signals, or they may be relatively weak. In these situations, receiver circuit currents can be reduced below what is necessary for the worst case condition. If this is done, power dissipation is reduced, and battery life is increased.

Thus, what is needed are circuits and methods that can adapt to a better-than-worst-case condition and reduce circuit currents and therefore power dissipation accordingly.

SUMMARY

Accordingly, embodiments of the present invention provide methods and circuits for reducing power dissipation in wireless transceivers and other electronic circuits and systems. Embodiments of the present invention use bias current reduction, impedance scaling, gain, and other dynamic changes either separately or in combination to reduce power dissipation in response to better-than-worst case conditions. For example, bias currents are reduced in response to a need for reduced signal handling capability, impedances are scaled thus reducing required drive and other bias currents in response to a strong received signal, or gain is varied and impedances are scaled in response to a low received signal in the presence of no or weak interfering signals. Alternately, currents may start low and be increased in response to worse-than-best-case conditions, or they may start at a point in between and vary up or down. These variations may be made to electronic systems generally, and are particularly suited and discussed below in the context of a wireless transceiver that may be used in networking devices, cellular telephones, and other wireless systems.

An exemplary embodiment of the present invention provides a method of receiving a signal using an integrated circuit. The integrated circuit includes a signal path having a low-noise amplifier configured to receive the signal, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer. The method itself includes determining a first signal strength at a first node in the signal path in the integrated circuit and dynamically changing an impedance of a component in the signal path based on the first signal strength.

A further exemplary embodiment of the present invention provides a method of receiving a signal using an integrated circuit. The integrated circuit includes a signal path having a low-noise amplifier configured to receive the signal, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer. The method itself includes determining a first signal strength at a first node in the signal path in the integrated circuit and dynamically changing a bias current in the signal path based on the first signal strength.

Another exemplary embodiment of the present invention provides a method of receiving a signal using an integrated circuit. The integrated circuit includes a signal path having a first circuit and a second circuit having an input coupled to an output of the first circuit. The method itself includes determining a first signal strength at a first node in the signal path in the integrated circuit. The first node is before the first circuit in the signal path. The method further includes dynamically changing a gain of the first circuit based on the first signal strength and dynamically changing an impedance of a component in the second circuit based on the first signal strength.

Still a further exemplary embodiment of the present invention provides a wireless transceiver integrated circuit including a receiver having a signal path, the signal path including a low-noise amplifier, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer, as well as a first signal strength indicator circuit coupled to the signal path and configured to determine a first signal strength. An impedance in the signal path is configured to be dynamically adjusted in response to the first signal strength.

Yet a further exemplary embodiment of the present invention provides a wireless transceiver integrated circuit. This integrated circuit includes a receiver comprising a signal path, the signal path having a low-noise amplifier, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer, as well as a first signal strength indicator circuit coupled to the signal path, and configured to determine a first signal strength. A bias current in the signal path is configured to be dynamically adjusted in response to the first signal strength.

Another exemplary embodiment of the present invention provides a wireless transceiver integrated circuit. This circuit includes a receiver comprising a signal path, the signal path having a first circuit, and a second circuit having an input coupled to an output of the first circuit, as well as a first signal strength indicator circuit coupled to the signal path, and configured to determine a first signal strength. A gain of the first circuit is configured to be dynamically adjusted in

Case: 1:22-cv-03441 Document #: 1-Filed: 07/05/22 Page 210 of 28 PageID #:492

response to the first signal strength, and an impedance in the second circuit is configured to be dynamically adjusted in response to the first signal strength.

A better understanding of the nature and advantages of the present invention may be gained with reference to the following detailed description and the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram of a wireless transceiver that may benefit by incorporation of embodiments of the present invention;

FIGS. **2**A and **2**B illustrate examples of desired and interfering signals and noise that may be received by a circuit in a wireless receiver;

FIG. **3** illustrates what can occur as a maximum signal handling capability is reduced in the worst-case signal condition;

FIG. **4** illustrates a portion of a receiver consistent with an embodiment of the present invention;

FIG. **5** illustrates the relationship between a required bias current and a given output signal for a representative circuit;

FIG. **6** is an example of how a circuit's impedances may be scaled to reduce drive currents, and depending on the circuit configuration used, to reduce associated bias currents as well;

FIG. **7** illustrates how gain may be inserted in a signal path to improve a circuit's signal to noise ratio;

FIGS. **8**A–**8**D illustrate some of the possible power saving techniques that may be used when received desired and interferer signals are all at a low power level;

FIGS. **9**A–**9**C illustrate one of the possible power saving techniques that may be used when a received desired signal is strong while all interfering signals are at a low power level;

FIGS. **10**A–**10**C illustrate one of the possible power saving techniques that may be used when received desired and interferer signals are all at a high power level;

FIGS. **11**A–**11**D illustrate one of the possible power saving techniques that may be used when a received desired signal is weak while one or more interfering signals are strong;

FIG. **12** is a summary illustrating four different input conditions and some of the appropriate power-saving changes that may be made in response to those conditions;

FIG. **13** shows how power may be saved as a function of time by employing one or more of the power saving methods consistent with embodiments of the present invention;

FIG. **14** is a block diagram of a portion of a receiver consistent with an embodiment of the present invention; and

FIG. **15** is a block diagram of a portion of a transmitter consistent with an embodiment of the present invention.

DESCRIPTION OF EXEMPLARY EMBODIMENTS

FIG. **1** is a block diagram of a wireless transceiver that may benefit by incorporation of embodiments of the present invention. This wireless transceiver may be designed to send and receive signals consistent with the IEEE 802.11a, 802.11b, 802.11 g, or other signaling standard or combination of standards. This figure, as with all the included figures, is shown for illustrative purposes only and does not to limit either the possible embodiments of the present invention or the claims.

There are three main portions of this transceiver circuit, a receiver, transmitter, and synthesizer. This transceiver may be completely or partially integrated on a semiconductor chip, or it may be integrated onto multiple integrated circuits. In a specific embodiment, the circuitry bounded by dashed line **100** is integrated on a single chip coupled to one or more external components or circuits. The integrated circuit or circuits forming this wireless transceiver may incorporate various integrated circuit devices such as a bipolar, CMOS, or BiCMOS devices made using a silicon, silicon-germanium (SiGe), gallium arsenide or other III-V process, or other manufacturing process. Embodiments of the present invention may also be applicable to circuits manufactured using nanotechnology processing.

The receiver includes a signal path formed by low-noise amplifier **102**, I and Q mixers **104** and **106**, low pass filters **108** and **110**, and baseband amplifiers **114** and **116**. Other circuitry in the receiver includes received strength indicator **122**, automatic gain control circuit **166**, baseband gain control circuit **120**, tuning circuit **112**, and offset cancellation circuit **118**.

The transmitter includes input up-converter mixers **124** and **126**, summing node **176**, which may be conceptual rather than an actual circuit, transmit variable gain amplifier **128**, and power amplifier **130**.

The synthesizer includes a voltage-controlled oscillator **148**, which drives I and Q buffers **154** and **152**, prescaler **156**, reference clock buffer **142** and divider **158**, phase-frequency detector **160**, charge pump **162**, and loop filter **146**, which in a specific embodiment is formed by external components.

Signals are received on an antenna, not shown, and typically pass through an RF switch and bandpass filter before being received by the low-noise amplifier **102** on line **101**. The low noise amplifier gains the received signal and provides it to quadrature mixers **104** and **106**. I and Q mixers **104** and **106** down-convert the received signal to baseband by multiplying them with quadrature versions of the oscillator signal provided by buffers **152** and **154**. This down conversion also produces a high frequency component at a frequency that is equal to the sum of the frequencies of the received signal and the VCO. This unwanted signal is filtered by low pass filters **108** and **110**, which in turn drive baseband amplifiers **114** and **116**. The outputs of baseband amplifiers **114** and **116** are typically converted to digital signals by analog-to-digital converters at the front end of a digital signal processing block.

In the transmit mode, I and Q versions of the signal to be transmitted are provided on lines **121** and **123** to up-convert mixers **124** and **126**. These up-convert mixers multiply the I and Q portions of the transmit signal by quadrature versions of the VCO signal provided by buffers **152** and **154**. The outputs of the up-convert mixers **124** and **126** are summed, and amplified by transmit VGA **128**, which in turn drives power amplifier **130**. The output of power amplifier **130** is typically filtered, and passes through the RF switch to the antenna for transmission.

A reference clock is received and buffered by the reference buffer **142**. The VCO generates quadrature oscillatory signals that are divided by prescaler **156**. The reference clock is typically generated by a crystal or other stable periodic clock source. The phase-frequency detector **116** compares the phase or frequency (depending on whether the synthesizer is tracking or acquiring the correct frequency) of the divided VCO signal and the reference clock, or a divided version of the reference clock, and generates an error signal, which drives the charge pump **162**. The output signal of the

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charge pump **162** is filtered by the loop filter **146**, which is commonly a lead-lag filter, and which provides a tuning or correction signal to the VCO **148**.

Embodiments of the present invention may be used to reduce the power dissipation of one or more of these included circuits. For example, the power dissipation in the low-noise amplifier **102**, down-convert mixers **104** and **106**, low pass filters **108** and **110**, or baseband amplifiers **114** and **116** may be optimized. Also, power dissipation in up-convert mixers **124** **126**, variable gain amplifier **128**, and power amplifier **130** may also be optimized. Similarly, VCO **148** and prescaler **156** currents may be adjusted. Embodiments of the present invention may also be applied in other circuits which may be included in other integrated circuit receivers, transmitters, transceivers, or other electronic circuits or systems.

When a receiver is actively receiving a desired signal, each block in the signal path has at its input the desired signal as well as noise and possibly interfering signals. The desired signal is the useful, information-carrying portion of a received signal. The noise may be thermal, shot, or other noise generated on the integrated circuit, in addition to received noise generated by sources external to the chip. The noise at the input of a block may be referred to as the equivalent input noise. The interfering signal or signals, or interferers, may be generated by similar transceivers, or other electrical equipment, circuits, or systems.

FIGS. **2**A and **2**B illustrate examples of desired signals, interferers, and noise that may be received by one of the various circuits in a wireless receiver. In each of these figures, the signal strength is plotted along a Y-axis **204** or **254** as a function of frequency along an X-axis **202** or **252**. In the example of FIG. **2**A, a received desired signal **206** is large in comparison to interfering signals **208** and **210**. In these examples, two interfering signals are shown for illustrative purposes, though there may be no such signals, one such signal, or more than two such signals in the frequency range of interest. Also, while for these examples the interferers are shown as being at a higher frequency than the desired signal, there may be one or more interferers at higher or lower frequencies as the desired signal. In this specific example, the acceptable noise floor **214** is relatively high, while maximum signal handling capability Smax **212** (that is the maximum signal power that can be handled with an acceptably low distortion) needs only to be high enough to accommodate the desired signal. For this specific example, the circuit receiving this input spectrum only requires a relatively small dynamic range for proper operation, that is the range between Smax **212** and the noise floor **214** is relatively small.

Conversely, in the example shown in FIG. **2**B, the desired signal **256** is relatively weak compared to the large interferers **258** and **260**. In this example, the noise floor **264** should be relatively low so as to prevent an unacceptable level of error in the recovery the desired signal **256**. The maximum signal handling capability Smax **262** should be relatively high to accommodate the large interferers in order to avoid the creation of intermodulation products as described below. Accordingly, in this specific example, the circuit receiving this input spectrum should have a large dynamic range, particularly in comparison to the example of FIG. **2**A.

It should be noted that the noise level or noise floors shown in these and the other included figures is the noise density integrated over the bandwidth of interest. For simplicity and comparison, this level is shown as a horizontal line, and is not meant to imply noise density.

Often in wireless receivers, a circuit at different times will receive an input spectrum similar to those shown in FIGS. **2**A and **2**B. The input spectrum of FIG. **2**B is generally considered the worst-case input signal, and typical design methodology involves designing a receiver for this condition, specifically the weakest desired signal accompanied by largest interference level. Circuit impedances and currents are set such that the noise floor **264** is sufficiently low for an acceptable bit-error rate, while bias currents are set sufficiently high for the required Smax **262**.

Conversely, the input spectrum in FIG. **2**A is that of the best-case input signal, specifically, a robust desired signal accompanied by no or low-level interferers. In this case, the noise floor **214** may be allowed to rise, while the maximum signal handling capability Smax **212** may be reduced. When this is done, the receiver circuit may save significant power. For example, the circuit's impedances may be increased, thus reducing required drive currents. Similarly, bias currents may be lowered, thus reducing the maximum signal in handling capability.

The minimum power dissipation for a circuit is proportional to the required maximum signal-to-noise ratio, which is the ratio between Smax **212** or **262** and N **214** and **264**. Thus, a circuit receiving an input similar to the one shown in FIG. **2**A can dissipate less power than one receiving the input as shown in FIG. **2**B, while still achieving an acceptable bit-error rate.

FIG. **3** illustrates what can occur when the maximum signal handling capability Smax **314** is reduced in the worst-case condition, that is when a weak desired signal **306** is accompanied by large interferers **310** and **312**. Again, signal strength is plotted along a Y-axis **304** as a function of frequency along X-axis **302**. In this specific example, Smax **314** is reduced below the peak levels of the interferers **310** and **312**. Since Smax is low, the circuit cannot handle the interferers linearly. The resulting nonlinearities lead to a mixing of the interferers and the creation of intermodulation products **308** (for example, a third-order intermodulation distortion, IM3), one of which in this example occurs at the same frequency as the desired signal **306**. As can be seen, if the intermodulation products **308** become excessive, the received signal bit error rate may become excessive, and the desired signal **306** may be lost. Accordingly, while Smax may be lowered even under some unfavorable conditions in order to reduce power, care should be taken to avoid corruption of the received desired signal.

FIG. **4** illustrates a portion of a receiver consistent with an embodiment of the present invention. Included is a filter **430**. An optional gain element **420** is placed in front of the filter **430** in order to increase signal levels. Signal strength indicator circuits **440** and **450** are connected to input line **410** and output line **460**. In this specific example, the input signal spectrum on line **410** is shown as desired signal **412** and interferers **414** and **416**. The signal spectrum at the output line **460** is shown as desired signal **462** and interferers **464** and **466**. The signal strength indicators **440** and **450** do not provide information as to the relative sizes of the desired and interfering signals. Rather, a cumulative signal level is provided at their outputs. For example, the first signal strength indicator **440** outputs a level corresponding to the sum of desired signal **412** and interfering signals **414** and **416**, while the second signal strength indicator **450** provides a signal level corresponding to the sum of desired signal **462** and interfering signals **464** and **466**. In this specific example, the gain of the gain and filter circuit combinations is shown as approximately one, while the interfering signals **414** and **416** signal levels are reduced.

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A comparison of the signal levels provided by the signal strength indicators **440** and **450** indicates that much of the combined received signal on line **410** has been filtered. Accordingly, it may be deduced that large interfering signals present at the input are being filtered by the filter **430**. From this information, as will be shown in greater detail below, the bias, impedance, and gain of the gain stage **420** and filter **430** combination may be optimized to reduce power dissipation.

There are several real world situations where the received signal is better than the worst-case condition such that power can be saved. For example, large interferers may be present only part of the time, that is, on a temporary or transient basis. The interfering equipment may be some distance from the transceiver, or it may be operating in the low power mode. Also, the desired signal may be very strong as compared to the noise and interferers, for example a hub, router, or access point may be nearby.

Some transceivers consistent with embodiments of the present invention are designed to work with more than one data transfer specification or standard. In this case, when a transceiver is operating in a mode having a lower data rate, the power saving techniques described here may be employed.

FIG. **5** illustrates the relationship between a required biased current **516** for a given output signal **514** for a representative circuit **510**. If the output signal current level is relatively low, such as the output current shown as **526**, the corresponding bias current **528** may be low. Conversely, if the output signal current level is larger as with the example **536**, the corresponding bias current level **538** should also be high. Accordingly, if a bias current is initially set high to handle large a large input signal, for example a large interferer, this current may be reduced if the input signal is smaller.

There are many ways by which these bias currents can be reduced. For example, the current may be generated by placing a voltage across a resistor by applying a bias voltage to the base of a device whose emitter is connected to ground through a resistance. In this case, the resistor may be increased by opening switches across portions of the resistance, or lowering the bias voltage applied at the base. Several ways in which this may be done will be readily understood by one skilled in the art.

FIG. **6** is an example of how a circuit's impedances may be scaled to reduce drive currents, and, depending on the circuit configuration used, associated bias currents as well. A driver **612** has a load R **614** and C **616**. The frequency response of this circuit is the same as that seen by driver **622**, which drives an impedance of 2R **624** and C/2 **626**. But the impedance of the load seen by driver **622** is double that seen by **612**, thus the output current required by the driver **622** is reduced by one-half.

As an example, the output stage of each of these drivers may be a Class A emitter follower formed by an emitter follower connected to a current source. When the outputs are driven high, the emitter of driver **622** need supply only one-half the drive current as driver **612**. In this way, an impedance can be scaled in order to decrease a circuit's required drive current.

Also, the discharge current for driver **622** is only one half that of driver **612** for a given negative-going slew rate. Thus, the current source of **622** may be reduced by the same factor of one-half as compared to driver **612**. In this example, the bias current, that is the current in the pull-down current source can be reduced. Many other examples where drive currents and possibly bias currents may be reduced will be appreciated by one skilled in the art.

FIG. **7** illustrates another degree of freedom that made be employed to reduce current levels in a transceiver. Specifically, a gain element **720** may be inserted in front of a circuit block **730** in order to improve the combined circuit's signal-to-noise ratio by a factor equal to the gain of the inserted gain block. This is particularly useful when large interferers are absent and the desired received signal is moderate or low. Specifically, gain is added to the signal while impedances are increased, which raise the noise floor. In this way, a given signal-to-noise ratio may be maintained while the power is decreased.

The gain of such an element may be varied by increasing a current in a differential pair or increasing a load resistance using switches. Many other examples where the gain of this element may be varied will be appreciated by one skilled in the art.

These variables, or degrees of freedom, specifically reducing bias currents, increasing impedances, and increasing gain may be used as in the following examples.

FIG. **8A** is a block diagram of a functional block **820** and optional gain element **810** in accordance with an embodiment of the present invention. Functional block **820**, like the functional blocks in the following diagrams, may be a filter, mixer, amplifier, or other circuit or circuits in a wireless transceiver or other electronic circuits or system. An input signal is received on line **812** by the optional gain element **814**. When the optional gain block **810** is not used, the input signal may be received directly by the function block **820**. The gain of the optional gain element **812** is controlled by a gain control signal on line **814**. The functional block receives an output signal from the optional gain element **810** and provides an output VOUT on line **822**. The lines in this and the other included figures may be one or more lines, depending on whether single-ended, differential, or other type of signaling is employed.

One or more impedances are under control of signals on impedance control lines **824**. Similarly, one or more bias currents in the function block are under control of one or more signals on bias control lines **826**. These various control lines may be logic signals, analog signals, voltage or currents lines, or other signal or bias lines. In other embodiments of the present invention, the gain control element **810** may be included in the function block **820**. Also, various embodiments may not incorporate either or both the impedance control and bias control.

FIG. **8B** is an example input that may be present on line VIN **812**. In this example, a desired signal **836** is relatively weak, as are interfering signals **837** and **838**. The initial bias and circuit configuration is such that the noise floor **833** and maximum signal handling capability Smax **831** are adjusted for worst case conditions. The circuit of FIG. **8A**, as with all the circuits described here, receives noise at its input which may be referred to as input equivalent noise or input referred noise. Additionally, the circuit of FIG. **8A** generates noise which is added to the input referred noise. Depending on the gain characteristics of the circuitry, the output noise at various frequencies may be greater than, equal to, or less than the input referred noise. For simplicity, the noise floor and maximum signal handling capability Smax, in this and the other figures, are shown as straight lines, though the noise and Smax are typically curved as a function of frequency.

That the input spectrum is as shown in FIG. **8B** can be determined, for example, by low signal strength indications on line VIN **812** and VOUT **822**. That is, a low level signal strength indication on line VIN **812** indicates that no portion of the input signal is particularly large.

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For this exemplary input, there are at least two methods by which the power dissipation for this circuitry may be reduced. Depending on the exact circuits and structures used, one of these methods may be preferred.

In FIG. 8C, the bias current is decreased, thereby lowering the maximum signal handling capability **841** as compared to **831**, closer to the desired and interfering signal levels. Again, the bias currents in the function block **820** may be reduced by switching impedances that appear across a voltage thereby changing a resulting bias current, by reducing a voltage at the gate of a MOS or base of a bipolar transistor, or by other methods.

In FIG. 8D, a second method of reducing power dissipation in the function block **820** is employed. Specifically, Smax **851** is held constant as compared Smax **831**. The desired and interfering signals are amplified such that they are closer to the available signaling handling capability **851**. Also, the noise floor **853** is raised as compared to noise floor **833** in FIG. 8B. Specifically, the noise contributed by the function block **820** is increased, such that the noise at its output is increased to noise floor **853**. This is done by increasing one or more impedance in function block **810**, such that drive currents inside that block are reduced. Depending on the exact configuration, this may also allow some biasing currents to be reduced, while maintaining the maximum signal handling capability **851** at a sufficient level. Alternately, these two methods of reducing power dissipation in function block **820** may be done in combination.

The included examples are explained for the exemplary situation where biasing and other parameters are set for worst-case conditions, and then changed to save power when it is discovered that the conditions are better-than-worst case. Alternately, the bias currents and other parameters may be set for maximum power savings, or an intermediate point, and the power can be adjusted from there.

FIG. 9A illustrates a block diagram including an optional gain element **910** and function block **920**. Again, an input signal is received on line **912** by optional gain element **910** which in turn drives function block **920**. The function block provides an output VOUT on line **922**, and receives impedance and bias control signals on lines **924** and **926**.

FIG. 9B shows the spectrum for what may be considered a best-case received signal. Specifically, the desired signal **936** is strong, while the interfering signals **937** and **938** are relatively weak. This may be determined, for example, by detecting a large signal level at the input line VIN **812** and a large signal level after a filter, since these readings would indicate that a large signal is received, but that it is at the desired signal frequency.

The maximum signaling capability **931** and noise floor **933** are shown as being set for the worst case conditions. In this case, the noise floor **933** is lower than the maximum allowed for proper signal reception. Accordingly, one or more impedance in the function block **920** may be increased, such that the noise floor **943** rises as shown in FIG. 9C. In this way one or more the driving currents in the function block **920** may be reduced. Similarly, since the drive current is reduced, one or more bias current may also be reduced, depending on the exact circuit configuration.

FIG. **10**A illustrates a block diagram showing an optional gain element **1010** driving a function block **1020**. An input signal is received by the gain element **1010** on line **1012**, and an output is provided by function block **1020** on line VOUT **1022**. One or more gain control signals present on lines **1014** control the gain of gain control element **1010**, while one or more impedance and bias control signals are received by the function block **1020** on line to **1024** and **1026**.

FIG. **10**B illustrates a received signal that may be received on line VIN **1012**. In this example, the desired signal **1036** and interferers **1037** and **1038** are each relatively large. This may be determined, for example, by detecting a large signal level at the input line VIN **812** and a smaller signal level after a filter, since these readings would indicate that a large signal is received, but that interferers are being reduced.

As before, in this example, the noise floor **1033** and maximum signal handling capability **1031** are initially set for the worst case conditions. Since the desired signal is relatively large in this case, the noise floor may be allowed to rise, a shown by noise floor **1043** in FIG. **10**C. Since the desired signal **1046** and interferers **1047** are large, the maximum signal handling capability Smax **1041** remains constant. Again, the noise floor is increased by increasing impedances in the function block **1020**. This reduces the required drive current, and may also allow for a reduction in bias currents.

FIG. **11**A illustrates a block diagram including an optional gain element **1110** and function block **1120** in accordance with an embodiment of the present convention. An input signal is received on line **1112** by the optional gain control element **1110**, while an output signal is provided by the function block **1120** on line VOUT **1122**. Gain, impedance, and bias control signals are received on lines **1114**, **1124**, and **1126**.

FIG. **11**B is an exemplary input signal that may be received by the gain control element **1110** on line VIN **1112**. In this specific example, the desired signal **1136** is relatively low or weak while the interfering signals **1137** and **1138** are large. This may be determined, for example, by detecting a large signal level at the input line VIN **812** and a much smaller signal level after a filter, since these readings would indicate that a large signal is received and that large interferers are being reduced such that the resulting signal, the desired signal, is relatively weak.

Again, the maximum signal handling capability **1131** and noise floor **1133** are initially set for worst case conditions. If the desired signal is sufficiently low, while the interferers are sufficiently high, power savings may not be achievable over the worst case settings, since this is in fact the worst case condition. But, if the desired signal is somewhat larger than the worst case condition, then power may be saved in at least two different ways.

For example, FIG. **11**C shows the maximum signal handling capability **1141** being lowered. In this case, the interfering signals **1147** in **1148** began to clip and distort, thereby creating intermodulation products **1145**, which distort the desired signal **1146**. So long as care is taken to not corrupt the desired signal **1146** beyond an acceptable limit, typically measured by a bit-error rate, power may be reduced in this way.

Similarly, in FIG. **11**D, the noise floor **1153** is raised somewhat, thereby saving power. Again, this may be done so long as the noise floor is not sufficiently high that the system bit-error rate becomes unacceptable.

FIG. **12** is a summary of the above four examples. The received signal strengths are shown in column **1210**, while appropriate power saving responses are listed in column **1220**. Specifically, in row **1230**, the desired signal and interferer signal strengths are both weak or small. In this case, proper responses include decreasing Smax, or increasing one or more circuit impedances while increasing the circuit gain. Depending on the exact circuit configuration, one of these options may be preferred over the other. Alternately, they may be done in combination, or done in combination with other power saving techniques. Also, in

some specific embodiments, when both desired signal and interferer signal strengths are small, the gain may need to be increased while the impedance is maintained or not increased in order to keep the noise floor low.

In row **1240**, the desired signal strength is strong or large, while the interfering signals are small. In this case, an appropriate response is to increase one or more of the circuit impedances. Again, depending on the exact circuit in question, one or more of the bias currents may also be reduced.

In row **1250**, both the desired signals and interfering signal strengths are large. Again, in this case an appropriate response is to increase one or more of the circuit impedances.

In row **1260**, the received desired signal strength is weak or small, while the interfering signals are large. Since this is the worst case situation for which the circuit is designed, substantial power savings are difficult to achieve. However, again, if the received signal is above a minimum level necessary for proper operation, some distortion of the interferers or raising of the noise floor may be acceptable.

It should be noted that not all possible signal conditions are listed here. For example, either the signal or interferer may be of a relatively medium strength, or the interferer may be absent. Also, these terms are for exemplary purposes and are not meant to convey specific signal conditions, but rather are only qualitative. The proper response to a specific condition depends on the embodiment of the present invention, the particular circuit topology, the requirements of the signaling standard used, as well as other constraints.

FIG. **13** is an example shown how power may be saved as a function of time by employing one or more of these methods consistent with embodiments of the present invention. Power is plotted along a Y-axis **1304** as a function of time along X-axis **1302**. Conventional worst case design would fix power dissipation at line **1310**. As can be seen, dynamic power dissipation **1320** under the control of variable gains, impedances, biasing, or combination thereof, allows for a lower average power **1330** as compared to the power dissipated **1310** by the conventional design.

FIG. **14** is a block diagram of a portion of a receiver consistent with an embodiment of the present invention. Included are low-noise amplifier **1410**, mixer **1420**, gain stage **1430**, filter **1440**, AGC amplifier **1450**, and VCO **1460**. Signal strength detection is done at the output of the low-noise amplifier by signal strength indicator **1470**, at the output of the mixer by signal strength indicator **1472**, and at the output of the filter by signal strength indicator **1474**. The outputs of the signal strength indicator circuits are received by the computational circuit **1470**, which in turn controls gain and power control circuits **1480** and **1485**. Power and gain control circuits **1480** and **1485** control the gain, biasing, and impedance levels of the circuits in the receiver signal path. Also, the gain and power control circuits may control the same parameters in the VCO **1460**. This figure is greatly simplified for purposes of explanation. For example, the quadrature nature of the mixers and following circuits are not shown. Also, power-down and start-up circuits are not included.

The current level in the low-noise amplifier determines a multitude of parameters including voltage gain, linearity, input impedance matching, and noise figure. When conditions are better than worst-case, some of these parameters may be relaxed while maintaining an acceptable bit-error rate, thus saving power.

The bias current in the mixers effect that block's noise figure and linearity. Care is taken in reducing power in this block so as not to increase nonlinearities, particularly the third-order nonlinearity as measured by IP3, the third-order intercept point, beyond an acceptable limit.

A key parameter of the VCO is phase noise, an increase in which increases the sidebands on either side of the oscillation signal. During transmission, the phase noise should be kept low to avoid interference with adjacent channels and for preserving modulation information.

During reception however, if the conditions are better than worst case, the phase noise requirement for the VCO is relaxed, and power can be saved consistent with embodiments of the present invention. The achievable phase noise power spectral density is approximately inversely proportional to the bias current used. Thus, when low phase noise is not required during reception, bias current in the VCO can be reduced.

Most of the power savings in a transceiver in accordance with embodiments of the present invention is achieved in the receiver portion. Additional power may be saved in the transmitter section.

FIG. **15** is a block diagram of a transmitter portion consistent with an embodiment of the present invention. Included is a signal path formed by gain stage **1510** and power amplifier **1520**. The output power level is sensed by output level sensing circuit **1550**, which in turn adjusts the biasing of the power amplifier **1520** through the power control circuit **1540**. Additionally, a transmitter level control signal is received by power control circuits **1530** and **1540**, which in turn control the biasing of gain stage **1510** and power amplifier **1520**. Gain control circuit **1560** also adjusts the gain of gain stage **1510** and power amplifier **1520**. Additional circuitry that varies impedances in each of these circuits may also be included.

Since the gain, impedance and biasing of these blocks are being dynamically varied, care must be taken to not negatively affect the signal being processed. For example, specific embodiments of the present invention perform some or all of these variations during preamble. Also, as changes occur, the circuits in some embodiments are limited such that they may only adapt to an improvement in conditions after frames are completed. If conditions worsen, the circuits may be allowed to change in order to save the data. Alternately, a system may be manually calibrated, for example at set up, and when the network configuration is changed.

The above description of specific embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form described, and many modifications and variations are possible in light of the teaching above. The embodiments were chosen and described in order to best explain the principles of the invention and its practical applications to thereby enable others skilled in the art to best utilize the invention in various embodiments and with various modifications as are suited to the particular use contemplated.

What is claimed is:

1. A method of receiving a signal using an integrated circuit, the integrated circuit comprising a signal path including a low-noise amplifier configured to receive the signal, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer, the method comprising:

determining a first signal strength at a first node in the signal path in the integrated circuit; and

reducing a switching current in the signal path by dynamically changing an impedance of a component in the signal path based on the first signal strength.

2. The method of claim 1 wherein the signal comprises a preamble portion and a data portion, the impedance of a component is changed while receiving the preamble portion, and the method further comprises receiving the data portion of the signal.

3. The method of claim 2 further comprising:

determining a second signal strength at a second node in the signal path, wherein the second node in the signal path is after the first node in the signal path.

4. The method of claim 3 wherein the impedance of the component in the signal path is also changed based on the second signal strength.

5. The method of claim 2 wherein the component in the signal path comprises a MOS transistor.

6. The method of claim 2 wherein the component in the signal path comprises a resistor.

7. The method of claim 2 wherein the component in the signal path comprises a capacitor.

8. The method of claim 4 wherein the component in the signal path is included in the mixer.

9. The method of claim 4 wherein the component in the signal path is included in the low-pass filter.

10. A method of receiving a signal comprising a preamble portion and a data portion using an integrated circuit, the integrated circuit comprising a signal path including a low-noise amplifier configured to receive the signal, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer, the method comprising:

determining a first signal strength at a first node in the signal path in the integrated circuit; and

while receiving the preamble portion of the signal, dynamically changing a bias current in the signal path based on the first signal strength, and while receiving the data portion of the signal, maintaining the bias current in the signal path.

11. The method of claim 10 wherein the method further comprises receiving the data portion of the signal.

12. The method of claim 11 further comprising:

determining a second signal strength at a second node in the signal path, wherein the second node in the signal path is after the first node in the signal path.

13. The method of claim 12 wherein the bias current in the signal path is also changed based on the second signal strength.

14. The method of claim 11 wherein the bias current is a bias current for the low-noise amplifier.

15. The method of claim 11 wherein the bias current is a bias current for the mixer.

16. The method of claim 11 wherein the bias current is a bias current for the low-pass filter.

17. A method of receiving a signal using an integrated circuit, the integrated circuit comprising a signal path including a first circuit and a second circuit having an input coupled to an output of the first circuit, the method comprising:

determining a first signal strength at a first node in the signal path in the integrated circuit, wherein the first node is before the first circuit in the signal path;

dynamically changing a gain of the first circuit based on the first signal strength; and

dynamically changing an impedance of a component in the second circuit based on the first signal strength.

18. The method of claim 17 wherein the signal comprises a preamble portion and a data portion, the gain and impedance are changed while receiving the preamble portion, and the method further comprises receiving the data portion of the signal.

19. The method of claim 18 further comprising:

determining a second signal strength at a second node in the signal path, wherein the second node in the signal path is after the second circuit in the signal path.

20. The method of claim 19 wherein the gain of the first circuit and impedance of the component in the second circuit is also changed based on the second signal strength.

21. The method of claim 18 wherein the first circuit is a low-noise amplifier.

22. The method of claim 18 wherein the first circuit is a mixer.

23. A wireless transceiver integrated circuit comprising:

a receiver comprising a signal path, the signal path comprising:

a low-noise amplifier;

a mixer having an input coupled to an output of the low-noise amplifier; and

a low-pass filter having an input coupled to an output of the mixer; and

a first signal strength indicator circuit coupled to the signal path, and configured to determine a first signal strength;

wherein an impedance in the signal path is configured to be dynamically adjusted to reduce a switching current in response to the first signal strength.

24. The wireless transceiver of claim 23 further comprising:

a second signal strength indicator circuit coupled to the output of the mixer, and configured to determine a second signal strength,

wherein the first signal strength indicator is coupled to the output of the low-noise amplifier, and

wherein the impedance in the signal path is configured to be adjusted in response to the first and second signal strengths.

25. The wireless transceiver of claim 23 further comprising:

a second signal strength indicator circuit coupled to the output of the low-pass filter, and configured to determine a second signal strength,

wherein the first signal strength indicator is coupled to the output of the mixer, and

wherein the impedance in the signal path is configured to be adjusted in response to the first and second signal strengths.

26. A wireless transceiver integrated circuit comprising:

a receiver comprising a signal path, the signal path comprising:

a low-noise amplifier;

a mixer having an input coupled to an output of the low-noise amplifier; and

a low-pass filter having an input coupled to an output of the mixer; and

a first signal strength indicator circuit coupled to the signal path, and configured to determine a first signal strength, the first signal strength the strength of a signal comprising a preamble portion and a data portion;

wherein a bias current in the signal path is configured to be dynamically adjusted during the preamble portion of the signal in response to the first signal strength and further configured to be maintained during the data portion of the signal.

27. The wireless transceiver of claim 26 further comprising:

a second signal strength indicator circuit coupled to the output of the mixer, and configured to determine a second signal strength,

wherein the first signal strength indicator is coupled to the output of the low-noise amplifier, and

wherein the bias current in the signal path is configured to be adjusted in response to the first and second signal strengths.

28. The wireless transceiver of claim 26 further comprising:

a second signal strength indicator circuit coupled to the output of the low-pass filter, and configured to determine a second signal strength,

wherein the first signal strength indicator is coupled to the output of the mixer, and

wherein the bias current in the signal path is configured to be adjusted in response to the first and second signal strengths.

29. A wireless transceiver integrated circuit comprising:

a receiver comprising a signal path, the signal path comprising:

a first circuit; and

a second circuit having an input coupled to an output of the first circuit; and

a first signal strength indicator circuit coupled to the signal path, and configured to determine a first signal strength,

wherein a gain of the first circuit is configured to be dynamically adjusted in response to the first signal strength, and

wherein an impedance in the second circuit is configured to be dynamically adjusted in response to the first signal strength.

30. The wireless transceiver of claim 29 further comprising:

a transmitter comprising:

a power amplifier; and

an output-level-sensing circuit coupled to an output of the power amplifier,

wherein the output-level-sensing circuit is configured to dynamically adjust a gain of the power amplifier.

* * * * *

Exhibit B

US010129825B2

(12) **United States Patent**
Tsividis

(10) **Patent No.: US 10,129,825 B2**
(45) **Date of Patent: *Nov. 13, 2018**

(54) **POWER DISSIPATION REDUCTION IN WIRELESS TRANSCEIVERS**

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(72) Inventor: **Yannis Tsividis**, New York, NY (US)

(73) Assignee: **Theta IP, LLC**, Coppell, TX (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

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(22) Filed: **Mar. 24, 2016**

(65) **Prior Publication Data**

US 2016/0212701 A1 Jul. 21, 2016

Related U.S. Application Data

(63) Continuation of application No. 11/318,646, filed on Dec. 27, 2005, now Pat. No. 9,331,728, which is a (Continued)

(51) **Int. Cl.**
H04B 1/38 (2015.01)
H04M 1/00 (2006.01)
(Continued)

(52) **U.S. Cl.**
CPC ***H04W 52/0209*** (2013.01); ***H04B 1/109*** (2013.01); *Y02D 70/00* (2018.01); *Y02D 70/142* (2018.01); *Y02D 70/40* (2018.01)

(58) **Field of Classification Search**
CPC ... H04B 1/04; H04B 1/16; H04B 1/40; H04B 1/109; H04B 1/0457; H04B 1/1607;
(Continued)

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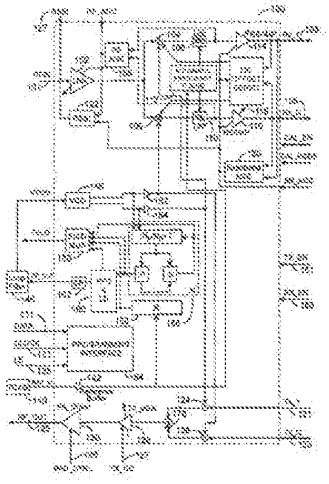
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Primary Examiner — Quochien B Vuong
(74) *Attorney, Agent, or Firm* — Womble Bond Dickinson (US) LLP

(57) **ABSTRACT**

Processes, methods and circuits for improving battery life by reducing the battery power-drain of battery-powered devices using wireless transceivers is disclosed. Embodiments of the present invention provide for dynamically changing the bias current, impedance, and gain, either separately or in combination, during circuit operation to optimize or to reduce power dissipation. The dynamic variations may be implemented by varying the value of a resistance and/or a capacitance by opening switches across one or more portions of the resistance. Also, the dynamic variations may include setting any of the gain, bias current, or impedance parameters of the receiver circuit in between a high and low level, followed by adjusting the parameter up or down in response to a desired signal and an interferer signal.

8 Claims, 15 Drawing Sheets



US007010330B1

(12) **United States Patent**
Tsividis

(10) **Patent No.: US 7,010,330 B1**
(45) **Date of Patent: Mar. 7, 2006**

(54) **POWER DISSIPATION REDUCTION IN WIRELESS TRANSCEIVERS**

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(73) Assignee: **Theta Microelectronics, Inc.**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/784,613**

(22) Filed: **Feb. 23, 2004**

Related U.S. Application Data

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(51) **Int. Cl.**
H04B 1/38 (2006.01)
H04M 1/00 (2006.01)

(52) **U.S. Cl.** **455/574**; 455/234.1; 455/251.1; 455/343.1

(58) **Field of Classification Search** 455/63.1, 455/67.13, 226.1, 226.2, 232.1, 234.1, 250.1, 455/251.1, 295, 296, 311, 333, 343.1, 127.1, 455/127.2, 127.5, 574, 572; 370/442; 330/127, 330/129, 134, 136, 144
See application file for complete search history.

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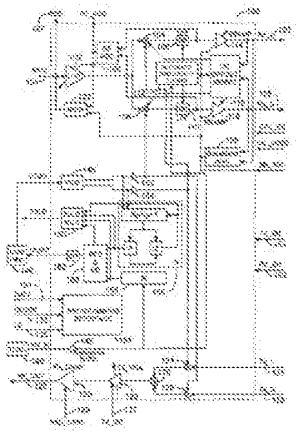
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(57) **ABSTRACT**

Methods and circuits for reducing power dissipation in wireless transceivers and other electronic circuits and systems. Embodiments of the present invention use bias current reduction, impedance scaling, and gain changes either separately or in combination to reduce power dissipation. For example, bias currents are reduced in response to a need for reduced signal handling capability, impedances are scaled thus reducing required drive and other bias currents in response to a strong received signal, or gain is increased and impedances are scaled in response to a low received signal in the presence of no or weak interfering signals.

30 Claims, 15 Drawing Sheets



Related U.S. Application Data

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H04W 52/02	(2009.01)
H04B 1/10	(2006.01)

(58) **Field of Classification Search**

CPC .. H04B 17/309; H04B 17/318; H04B 17/336; H04B 17/345; H04B 2001/045; H04B 2001/0416; H04W 52/52; H04W 52/0261; H04W 88/02; H03G 3/004; H03G 3/20

USPC 455/63.1, 67.13, 127.1, 127.2, 127.5, 455/226.1, 226.2, 232.1, 234.1, 250.1, 455/251.1, 295, 296, 343.1, 572, 574; 370/442; 330/127, 134, 144

See application file for complete search history.

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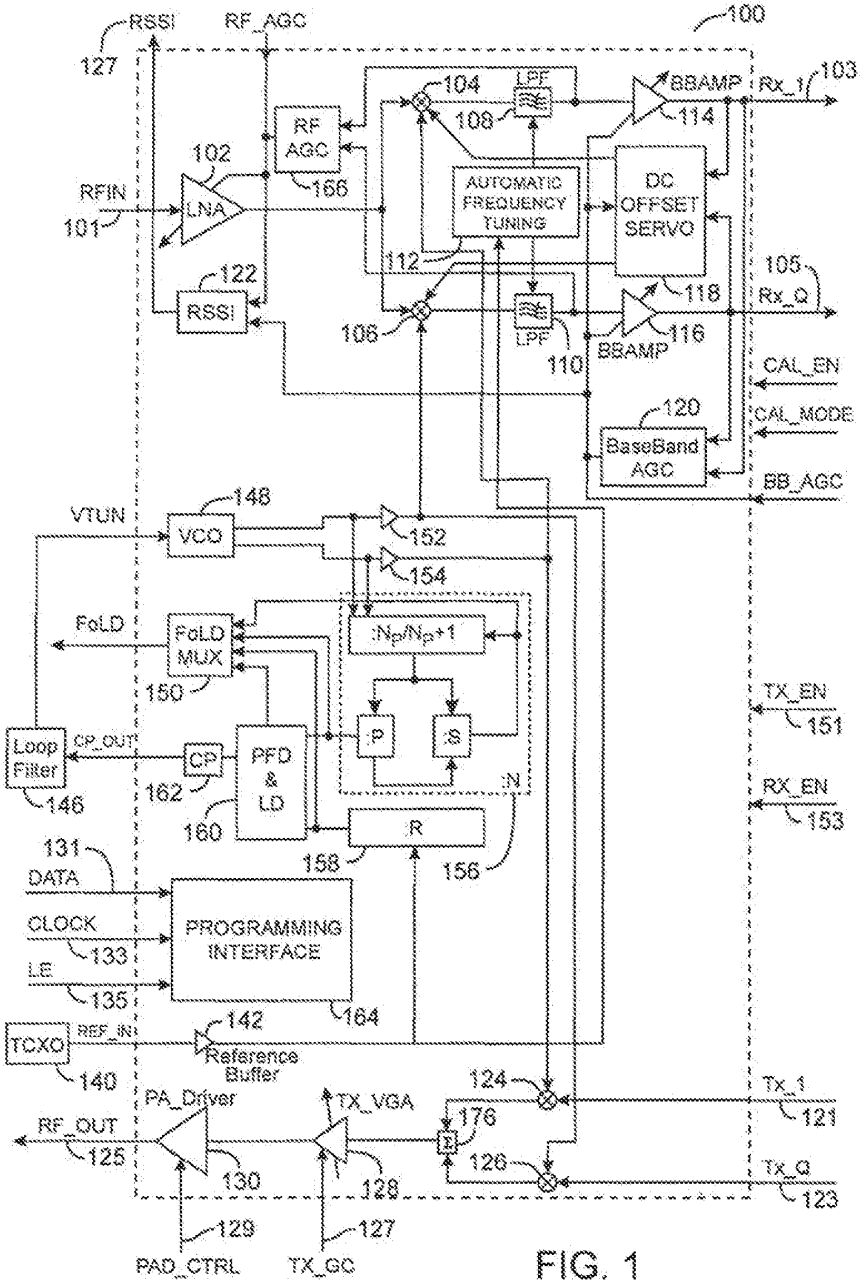

RSSI
RF_AGC
100
127
104
LPF
BBAMP
Rx_I
103
108
114
RF AGC
166
102
AUTOMATIC FREQUENCY TUNING
DC OFFSET SERVO
RFIN
101
LNA
112
105
Rx_Q
122
RSSI
118
106
LPF
110
BBAMP
116
CAL_EN
CAL_MODE
120
BaseBand AGC
BB_AGC
VTUN
148
VCO
152
154
FoLD
FoLD MUX
150
:N_P/N_P+1
TX_EN
151
Loop Filter
146
CP_OUT
CP
162
PFD & LD
160
P
:S
:N
RX_EN
153
R
158
156
131
DATA
CLOCK
133
LE
135
PROGRAMMING INTERFACE
164
TCXO
140
REF_IN
142
Reference Buffer
124
Tx_I
121
PA_Driver
TX_VGA
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RF_OUT
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130
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Tx_Q
123
129
127
PAD_CTRL
TX_GC

FIG. 1

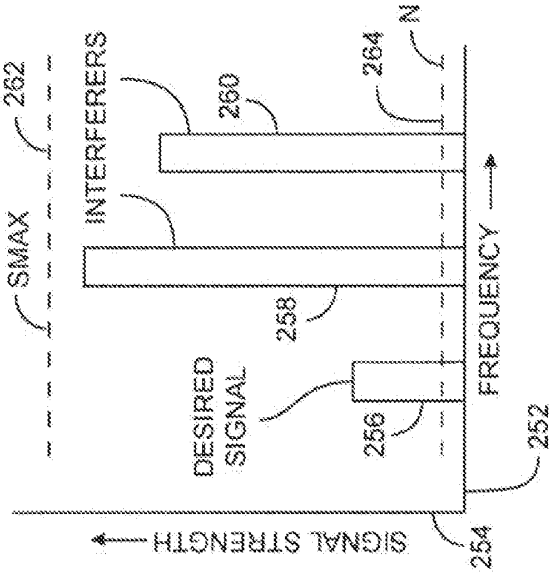

SMAX
262
INTERFERERS
260
264
N
258
DESIRED SIGNAL
256
FREQUENCY
252
SIGNAL STRENGTH
254

FIG. 2B

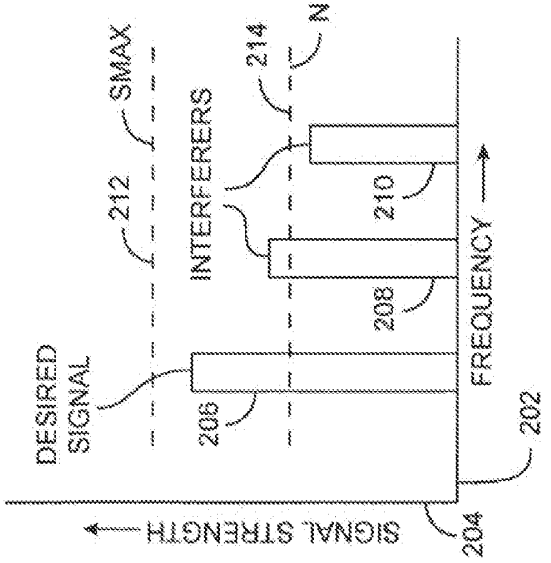

SMAX
212
214
N
INTERFERERS
210
208
DESIRED SIGNAL
206
FREQUENCY
202
SIGNAL STRENGTH
204

FIG. 2A

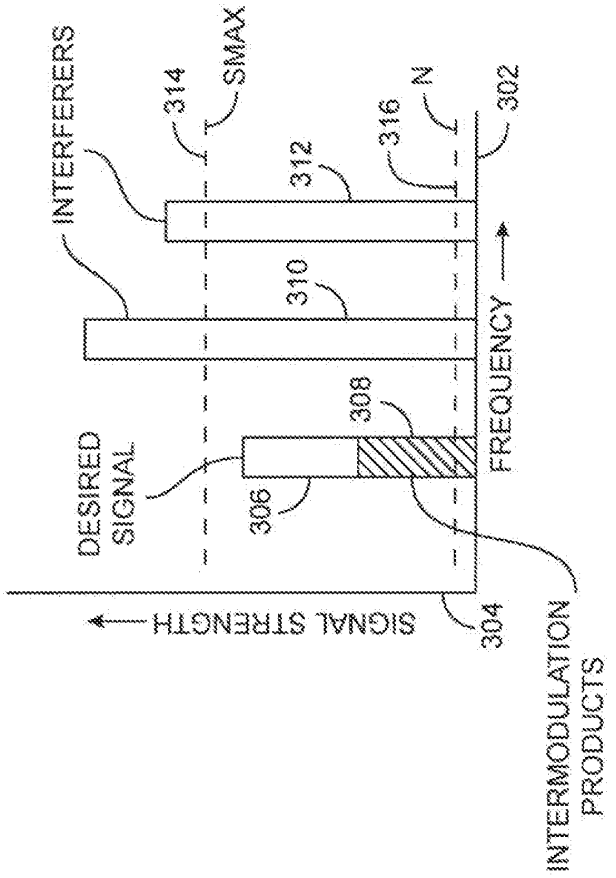

INTERFERERS
314
SMAX
312
316
N
302
310
FREQUENCY
308
DESIRED SIGNAL
306
SIGNAL STRENGTH
304
INTERMODULATION PRODUCTS

FIG. 3

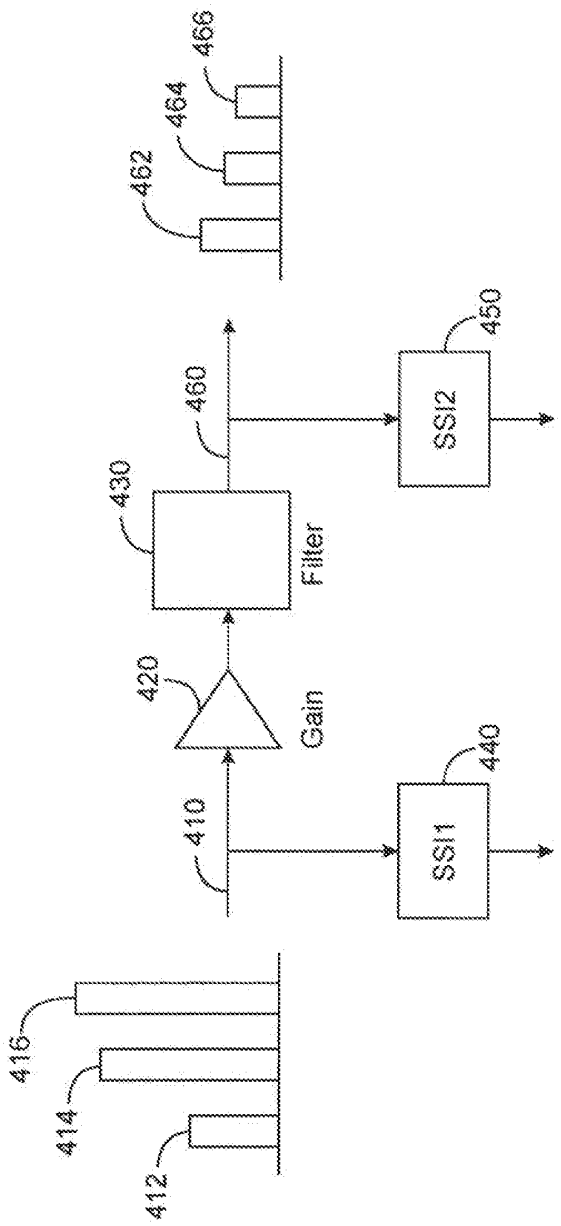

466
464
462
460
450
SSI2
430
Filter
420
Gain
410
440
SSI1
416
414
412

FIG. 4

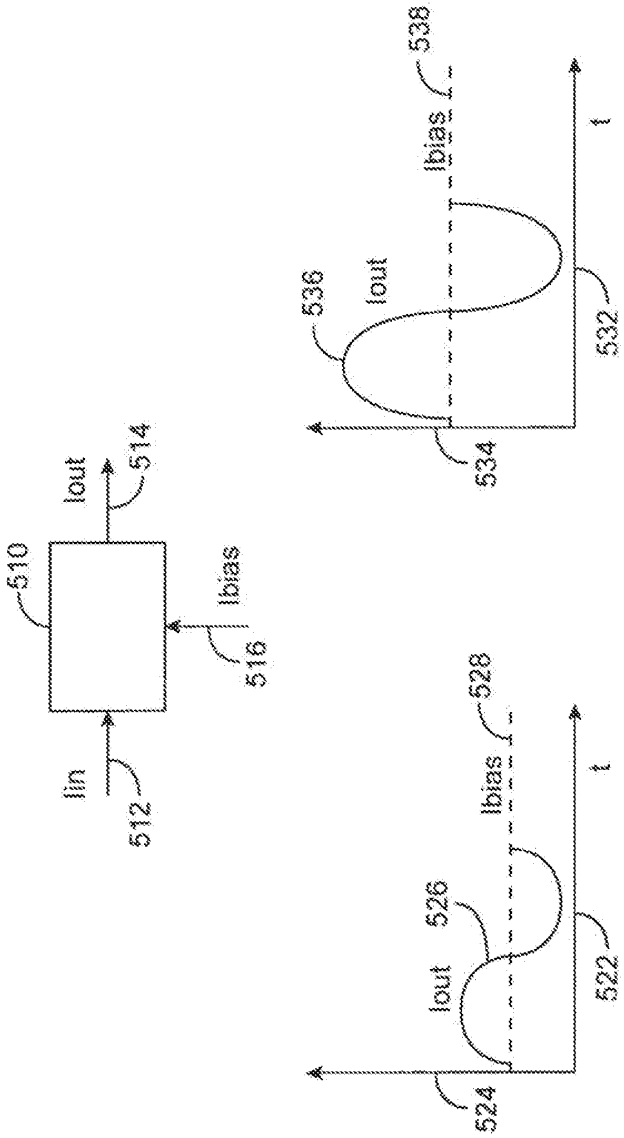

510
Iout
514
Ibias
516
Iin
512
538
Ibias
t
536
Iout
532
534
528
Ibias
t
526
Iout
522
524

FIG. 5

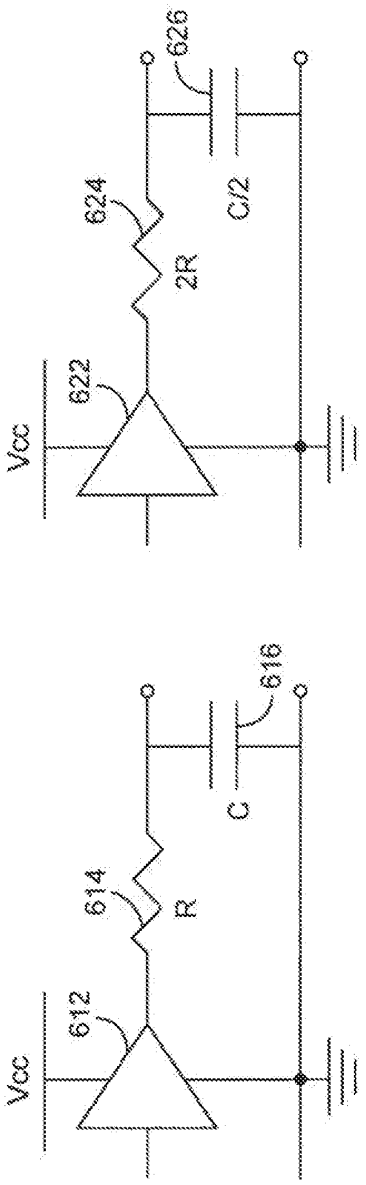


FIG. 6

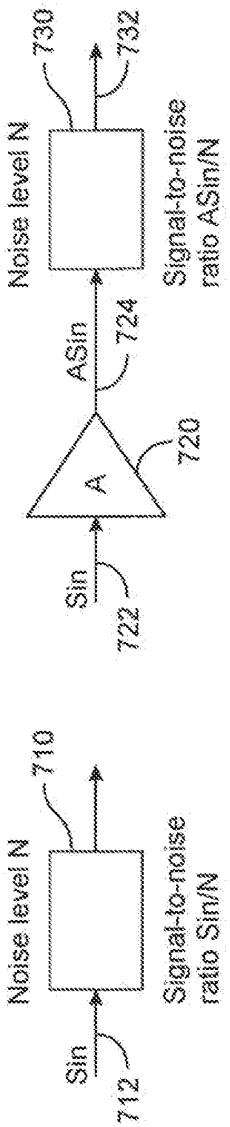

730
732
Noise level N
Signal-to-noise ratio ASin/N
ASin
724
A
720
Sin
722
710
Noise level N
Signal-to-noise ratio Sin/N
Sin
712

FIG. 7

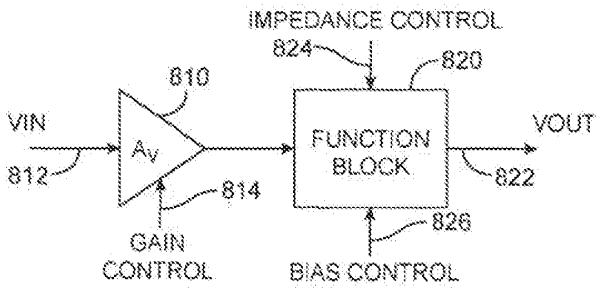


FIG. 8A

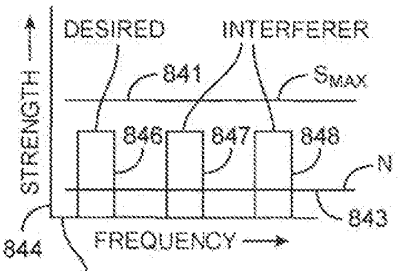


FIG. 8C

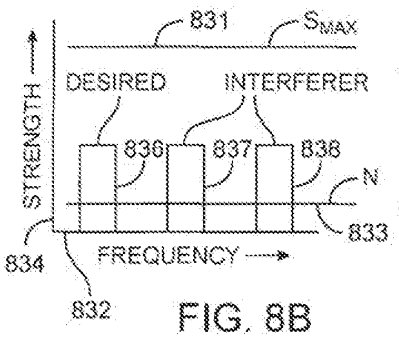


FIG. 8B

DECREASE BIASING

– AND/OR –

INCREASE GAIN AND IMPEDANCES

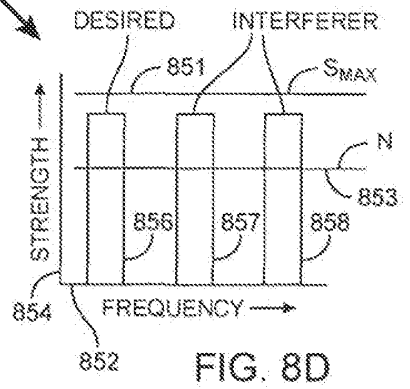


FIG. 8D

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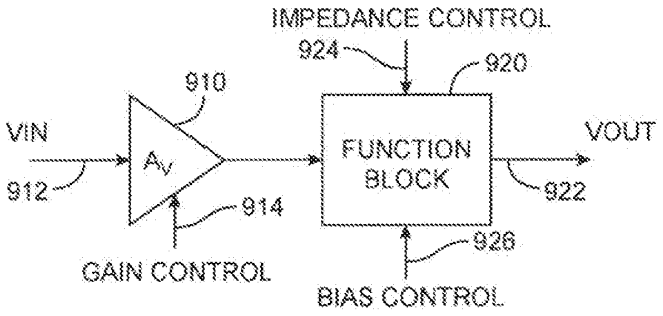


FIG. 9A

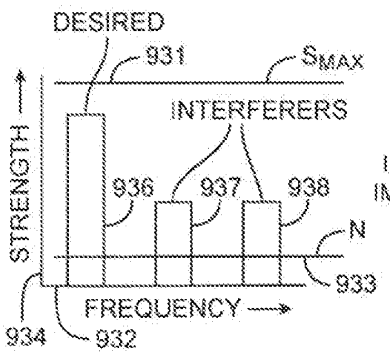


FIG. 9B

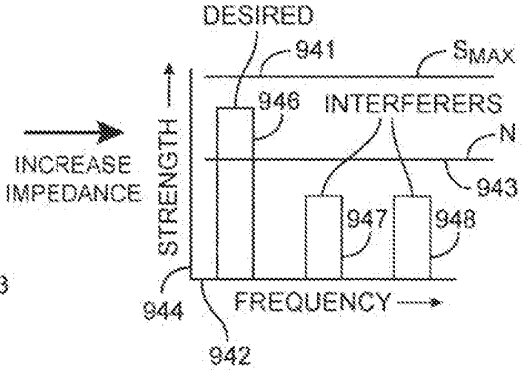


FIG. 9C

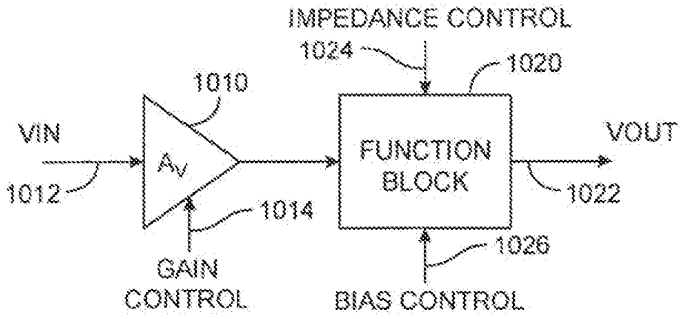


FIG. 10A

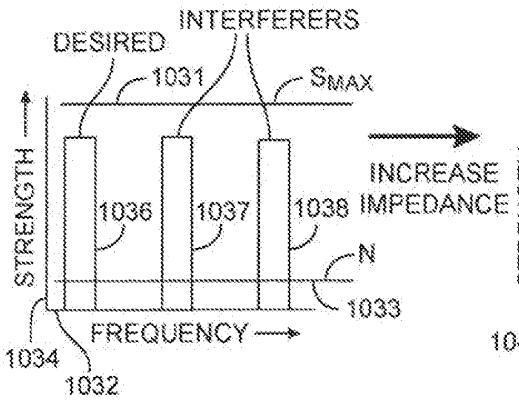


FIG. 10B

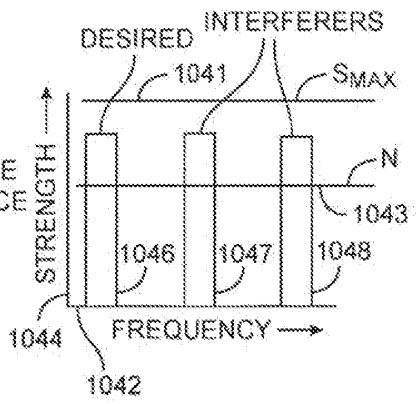


FIG. 10C

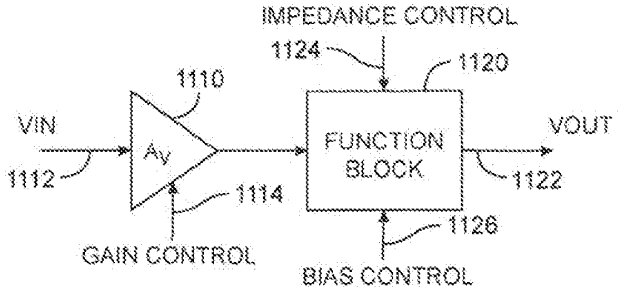


FIG. 11A

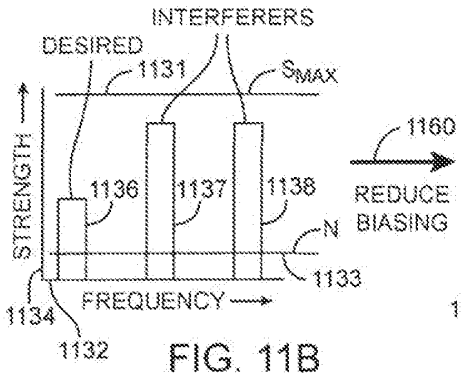


FIG. 11B

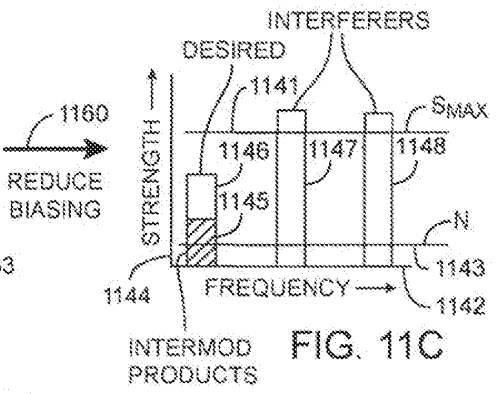


FIG. 11C

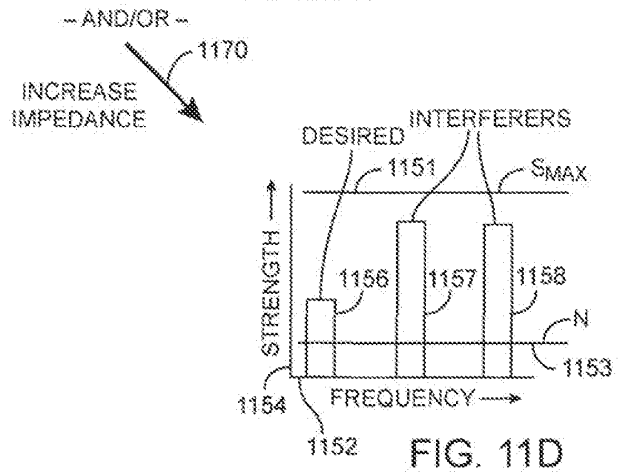


FIG. 11D

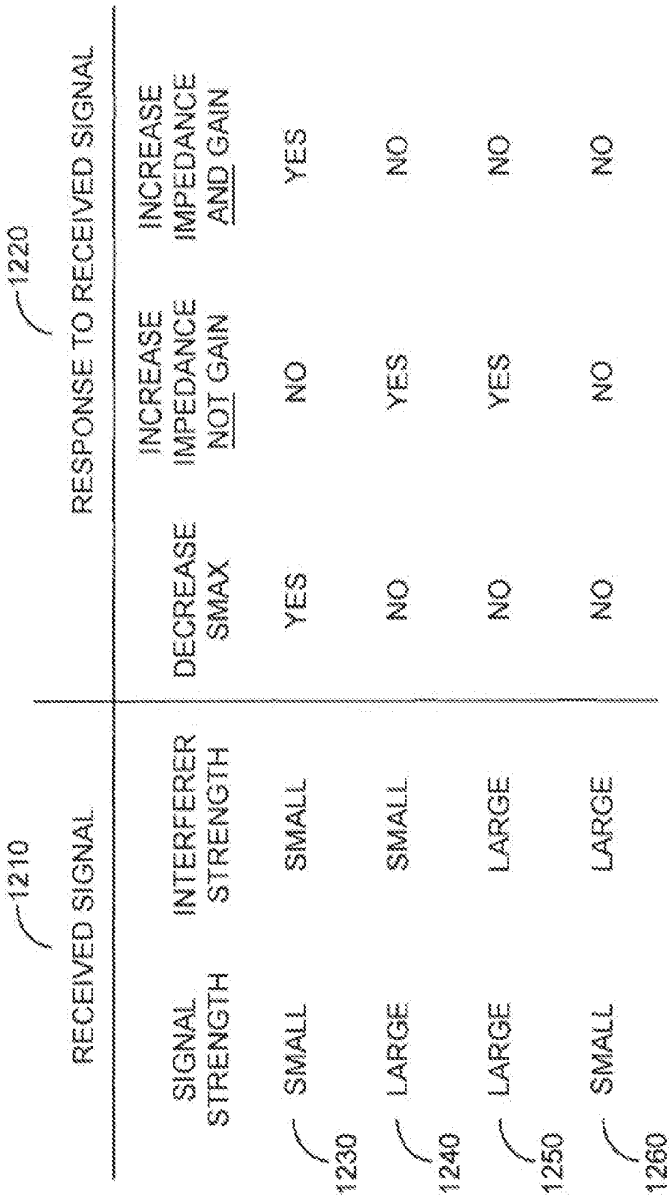

1210
RECEIVED SIGNAL
1220
RESPONSE TO RECEIVED SIGNAL
SIGNAL STRENGTH
INTERFERER STRENGTH
DECREASE SMAX
INCREASE IMPEDANCE NOT GAIN
INCREASE IMPEDANCE AND GAIN
SMALL
SMALL
YES
NO
YES
1230
LARGE
SMALL
NO
YES
NO
1240
LARGE
LARGE
NO
YES
NO
1250
SMALL
LARGE
NO
NO
NO
1260

FIG. 12

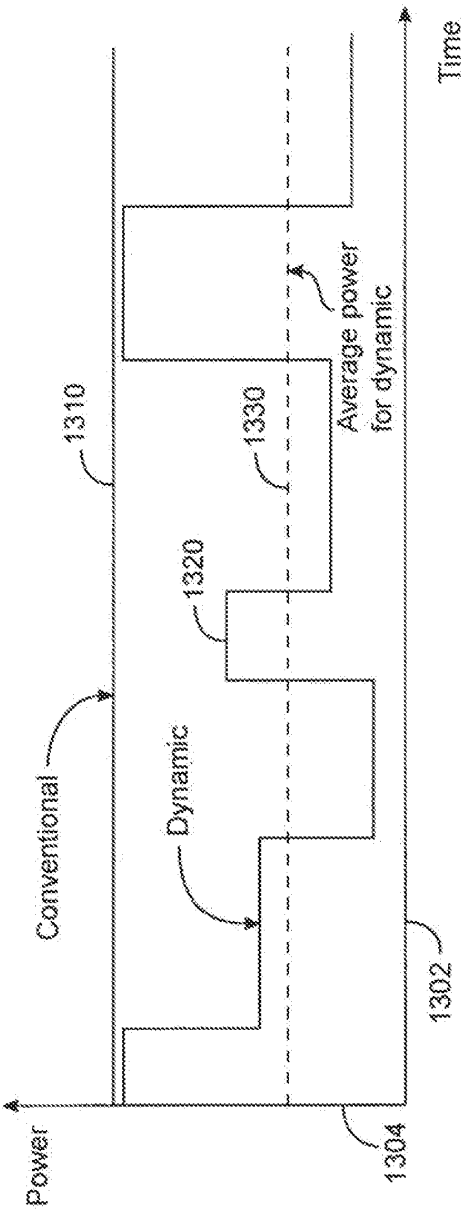

Power
Time
Conventional
Dynamic
1310
1320
1330
1302
1304
Average power for dynamic

FIG. 13

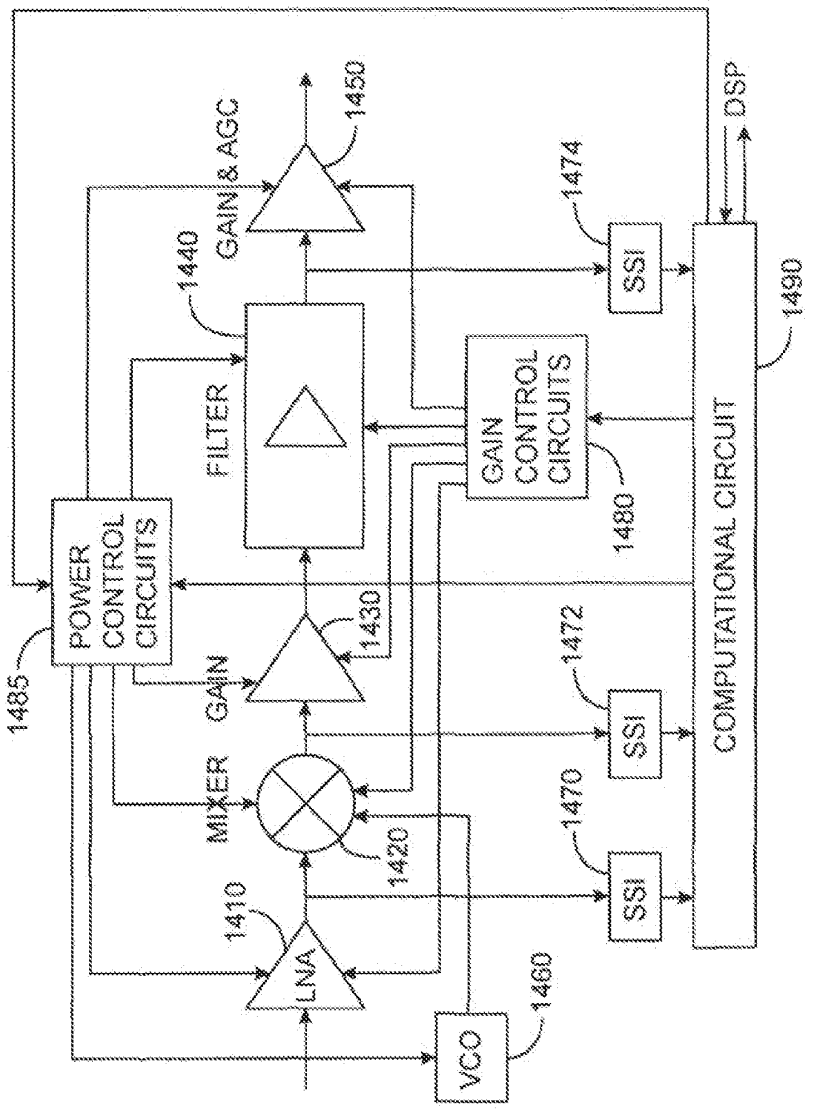

1485
POWER CONTROL CIRCUITS
1410
LNA
MIXER
1420
GAIN
1430
FILTER
1440
GAIN& AGC
1450
VCO
1460
1470
SSI
1472
SSI
1474
SSI
COMPUTATIONAL CIRCUIT
1490
DSP
GAIN CONTROL CIRCUITS
1480

FIG. 14

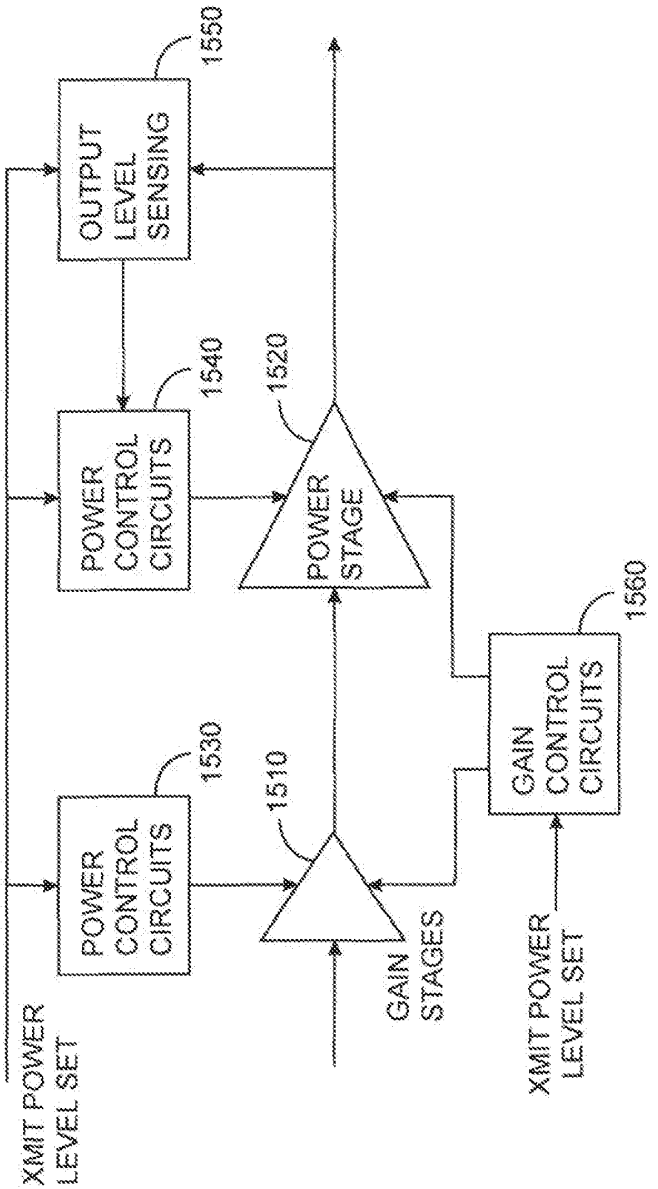

1550
OUTPUT LEVEL SENSING
1540
POWER CONTROL CIRCUITS
1520
POWER STAGE
1530
POWER CONTROL CIRCUITS
1510
GAIN STAGES
1560
GAIN CONTROL CIRCUITS
XMIT POWER LEVEL SET
XMIT POWER LEVEL SET

FIG. 15

POWER DISSIPATION REDUCTION IN WIRELESS TRANSCEIVERS

CROSS-REFERENCES TO RELATED APPLICATIONS

This application is a continuation of U.S. patent application Ser. No. 11/318,646, filed Dec. 27, 2005, which is a continuation of U.S. patent application Ser. No. 10/784,613, filed Feb. 23, 2004, which claims the benefit of U.S. provisional application No. 60/451,229, filed Mar. 1, 2003, which is incorporated by reference.

This application claims the benefit of U.S. provisional application No. 60/451,230, filed Mar. 1, 2003, which is incorporated by reference.

BACKGROUND

The present invention relates to power dissipation reduction techniques for electronic circuits, for example wireless transceiver integrated circuits.

Wireless networking is quickly becoming ubiquitous, as desktop, notebook, and handheld computers are connected to share Internet access and files. Wireless networking cards compatible with PCMCIA and compact flash form factors are popular for laptops and handhelds respectively, particularly as mobile users connect to the Internet on the road at coffee shops, hotels, and airports.

A downside of this connectivity is a corresponding drain on battery life, especially for these portable devices. The power consumed by a wireless transmitter and receiver reduces the usefulness of a device and sends a user on a hunt for an electrical outlet for recharging.

One reason why this power drain is high is that electronic circuits are typically designed to function properly under worst-case operating conditions. For a wireless transceiver, the worst case condition is when a desired signal reception strength is low, while other transceivers or nearby electronic equipment generate interfering signals and other spurious noise.

But a wireless transceiver does not always operate in these worst-case conditions. For example, a base station, router or access point may be nearby such that the received signal is strong. Also, there may be no interfering signals, or they may be relatively weak. In these situations, receiver circuit currents can be reduced below what is necessary for the worst case condition. If this is done, power dissipation is reduced, and battery life is increased.

Thus, what is needed are circuits and methods that can adapt to a better-than-worst-case condition and reduce circuit currents and therefore power dissipation accordingly.

SUMMARY

Accordingly, embodiments of the present invention provide methods and circuits for reducing power dissipation in wireless transceivers and other electronic circuits and systems. Embodiments of the present invention use bias current reduction, impedance scaling, gain, and other dynamic changes either separately or in combination to reduce power dissipation in response to better-than-worst case conditions. For example, bias currents are reduced in response to a need for reduced signal handling capability, impedances are scaled thus reducing required drive and other bias currents in response to a strong received signal, or gain is varied and impedances are scaled in response to a low received signal in the presence of no or weak interfering signals. Alternately, currents may start low and be increased in response to worse-than-best-case conditions, or they may start at a point in between and vary up or down. These variations may be made to electronic systems generally, and are particularly suited and discussed below in the context of a wireless transceiver that may be used in networking devices, cellular telephones, and other wireless systems.

An exemplary embodiment of the present invention provides a method of receiving a signal using an integrated circuit. The integrated circuit includes a signal path having a low-noise amplifier configured to receive the signal, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer. The method itself includes determining a first signal strength at a first node in the signal path in the integrated circuit and dynamically changing an impedance of a component in the signal path based on the first signal strength.

A further exemplary embodiment of the present invention provides a method of receiving a signal using an integrated circuit. The integrated circuit includes a signal path having a low-noise amplifier configured to receive the signal, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer. The method itself includes determining a first signal strength at a first node in the signal path in the integrated circuit and dynamically changing a bias current in the signal path based on the first signal strength.

Another exemplary embodiment of the present invention provides a method of receiving a signal using an integrated circuit. The integrated circuit includes a signal path having a first circuit and a second circuit having an input coupled to an output of the first circuit. The method itself includes determining a first signal strength at a first node in the signal path in the integrated circuit. The first node is before the first circuit in the signal path. The method further includes dynamically changing a gain of the first circuit based on the first signal strength and dynamically changing an impedance of a component in the second circuit based on the first signal strength.

Still a further exemplary embodiment of the present invention provides a wireless transceiver integrated circuit including a receiver having a signal path, the signal path including a low-noise amplifier, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer, as well as a first signal strength indicator circuit coupled to the signal path and configured to determine a first signal strength. An impedance in the signal path is configured to be dynamically adjusted in response to the first signal strength.

Yet a further exemplary embodiment of the present invention provides a wireless transceiver integrated circuit. This integrated circuit includes a receiver comprising a signal path, the signal path having a low-noise amplifier, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer, as well as a first signal strength indicator circuit coupled to the signal path, and configured to determine a first signal strength. A bias current in the signal path is configured to be dynamically adjusted in response to the first signal strength.

Another exemplary embodiment of the present invention provides a wireless transceiver integrated circuit. This circuit includes a receiver comprising a signal path, the signal path having a first circuit; and a second circuit having an input coupled to an output of the first circuit; as well as a first

signal strength indicator circuit coupled to the signal path, and configured to determine a first signal strength. A gain of the first circuit is configured to be dynamically adjusted in response to the first signal strength, and an impedance in the second circuit is configured to be dynamically adjusted in response to the first signal strength.

A better understanding of the nature and advantages of the present invention may be gained with reference to the following detailed description and the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram of a wireless transceiver that may benefit by incorporation of embodiments of the present invention;

FIGS. **2**A and **2**B illustrate examples of desired and interfering signals and noise that may be received by a circuit in a wireless receiver;

FIG. **3** illustrates what can occur as a maximum signal handling capability is reduced in the worst-case signal condition;

FIG. **4** illustrates a portion of a receiver consistent with an embodiment of the present invention;

FIG. **5** illustrates the relationship between a required bias current and a given output signal for a representative circuit;

FIG. **6** is an example of how a circuit's impedances may be scaled to reduce drive currents, and depending on the circuit configuration used, to reduce associated bias currents as well;

FIG. **7** illustrates how gain may be inserted in a signal path to improve a circuit's signal to noise ratio;

FIGS. **8**A-**8**D illustrate some of the possible power saving techniques that may be used when received desired and interferer signals are all at a low power level;

FIGS. **9**A-**9**C illustrate one of the possible power saving techniques that may be used when a received desired signal is strong while all interfering signals are at a low power level;

FIGS. **10**A-**10**C illustrate one of the possible power saving techniques that may be used when received desired and interferer signals are all at a high power level;

FIGS. **11**A-**11**D illustrate one of the possible power saving techniques that may be used when a received desired signal is weak while one or more interfering signals are strong;

FIG. **12** is a summary illustrating four different input conditions and some of the appropriate power-saving changes that may be made in response to those conditions;

FIG. **13** shows how power may be saved as a function of time by employing one or more of the power saving methods consistent with embodiments of the present invention;

FIG. **14** is a block diagram of a portion of a receiver consistent with an embodiment of the present invention; and

FIG. **15** is a block diagram of a portion of a transmitter consistent with an embodiment of the present invention.

DESCRIPTION OF EXEMPLARY EMBODIMENTS

FIG. **1** is a block diagram of a wireless transceiver that may benefit by incorporation of embodiments of the present invention. This wireless transceiver may be designed to send and receive signals consistent with the IEEE 802.11a, 802.11b, 802.11g, or other signaling standard or combination of standards. This figure, as with all the included figures, is shown for illustrative purposes only and does not to limit either the possible embodiments of the present invention or the claims.

There are three main portions of this transceiver circuit, a receiver, transmitter, and synthesizer. This transceiver may be completely or partially integrated on a semiconductor chip, or it may be integrated onto multiple integrated circuits. In a specific embodiment, the circuitry bounded by dashed line **100** is integrated on a single chip coupled to one or more external components or circuits. The integrated circuit or circuits forming this wireless transceiver may incorporate various integrated circuit devices such as a bipolar, CMOS, or BiCMOS devices made using a silicon, silicon-germanium (SiGe), gallium arsenide or other III-V process, or other manufacturing process. Embodiments of the present invention may also be applicable to circuits manufactured using nanotechnology processing.

The receiver includes a signal path formed by low-noise amplifier **102**, I and Q mixers **104** and **106**, low pass filters **108** and **110**, and baseband amplifiers **114** and **116**. Other circuitry in the receiver includes received strength indicator **122**, automatic gain control circuit **166**, baseband gain control circuit **120**, tuning circuit **112**, and offset cancellation circuit **118**.

The transmitter includes input up-converter mixers **124** and **126**, summing node **176**, which may be conceptual rather than an actual circuit, transmit variable gain amplifier **128**, and power amplifier **130**.

The synthesizer includes a voltage-controlled oscillator **148**, which drives I and Q buffers **154** and **152**, prescaler **156**, reference clock buffer **142** and divider **158**, phase-frequency detector **160**, charge pump **162**, and loop filter **146**, which in a specific embodiment is formed by external components.

Signals are received on an antenna, not shown, and typically pass through an RF switch and bandpass filter before being received by the low-noise amplifier **102** on line **101**. The low noise amplifier gains the received signal and provides it to quadrature mixers **104** and **106**. I and Q mixers **104** and **106** down-convert the received signal to baseband by multiplying them with quadrature versions of the oscillator signal provided by buffers **152** and **154**. This down conversion also produces a high frequency component at a frequency that is equal to the sum of the frequencies of the received signal and the VCO. This unwanted signal is filtered by low pass filters **108** and **110**, which in turn drive baseband amplifiers **114** and **116**. The outputs of baseband amplifiers **114** and **116** are typically converted to digital signals by analog-to-digital converters at the front end of a digital signal processing block.

In the transmit mode, I and Q versions of the signal to be transmitted are provided on lines **121** and **123** to up-convert mixers **124** and **126**. These up-convert mixers multiply the I and Q portions of the transmit signal by quadrature versions of the VCO signal provided by buffers **152** and **154**. The outputs of the up-convert mixers **124** and **126** are summed, and amplified by transmit VGA **128**, which in turn drives power amplifier **130**. The output of power amplifier **130** is typically filtered, and passes through the RF switch to the antenna for transmission.

A reference clock is received and buffered by the reference buffer **142**. The VCO generates quadrature oscillatory signals that are divided by prescaler **156**. The reference clock is typically generated by a crystal or other stable periodic clock source. The phase-frequency detector **116** compares the phase or frequency (depending on whether the synthesizer is tracking or acquiring the correct frequency) of

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the divided VCO signal and the reference clock, or a divided version of the reference clock, and generates an error signal, which drives the charge pump **162**. The output signal of the charge pump **162** is filtered by the loop filter **146**, which is commonly a lead-lag filter, and which provides a tuning or correction signal to the VCO **148**.

Embodiments of the present invention may be used to reduce the power dissipation of one or more of these included circuits. For example, the power dissipation in the low-noise amplifier **102**, down-convert mixers **104** and **106**, low pass filters **108** and **110**, or baseband amplifiers **114** and **116** may be optimized. Also, power dissipation in up-convert mixers **124** **126**, variable gain amplifier **128**, and power amplifier **130** may also be optimized. Similarly, VCO **148** and prescaler **156** currents may be adjusted. Embodiments of the present invention may also be applied in other circuits which may be included in other integrated circuit receivers, transmitters, transceivers, or other electronic circuits or systems.

When a receiver is actively receiving a desired signal, each block in the signal path has at its input the desired signal as well as noise and possibly interfering signals. The desired signal is the useful, information-carrying portion of a received signal. The noise may be thermal, shot, or other noise generated on the integrated circuit, in addition to received noise generated by sources external to the chip. The noise at the input of a block may be referred to as the equivalent input noise. The interfering signal or signals, or interferers, may be generated by similar transceivers, or other electrical equipment, circuits, or systems.

FIGS. **2**A and **2**B illustrate examples of desired signals, interferers, and noise that may be received by one of the various circuits in a wireless receiver. In each of these figures, the signal strength is plotted along a Y-axis **204** or **254** as a function of frequency along an X-axis **202** or **252**. In the example of FIG. **2**A, a received desired signal **206** is large in comparison to interfering signals **208** and **210**. In these examples, two interfering signals are shown for illustrative purposes, though there may be no such signals, one such signal, or more than two such signals in the frequency range of interest. Also, while for these examples the interferers are shown as being at a higher frequency than the desired signal, there may be one or more interferers at higher or lower frequencies as the desired signal. In this specific example, the acceptable noise floor **214** is relatively high, while maximum signal handling capability Smax **212** (that is the maximum signal power that can be handled with an acceptably low distortion) needs only to be high enough to accommodate the desired signal. For this specific example, the circuit receiving this input spectrum only requires a relatively small dynamic range for proper operation, that is the range between Smax **212** and the noise floor **214** is relatively small.

Conversely, in the example shown in FIG. **2**B, the desired signal **256** is relatively weak compared to the large interferers **258** and **260**. In this example, the noise floor **264** should be relatively low so as to prevent an unacceptable level of error in the recovery the desired signal **256**. The maximum signal handling capability Smax **262** should be relatively high to accommodate the large interferers in order to avoid the creation of intermodulation products as described below. Accordingly, in this specific example, the circuit receiving this input spectrum should have a large dynamic range, particularly in comparison to the example of FIG. **2**A.

It should be noted that the noise level or noise floors shown in these and the other included figures is the noise density integrated over the bandwidth of interest. For simplicity and comparison, this level is shown as a horizontal line, and is not meant to imply noise density.

Often in wireless receivers, a circuit at different times will receive an input spectrum similar to those shown in FIGS. **2**A and **2**B. The input spectrum of FIG. **2**B is generally considered the worst-case input signal, and typical design methodology involves designing a receiver for this condition, specifically the weakest desired signal accompanied by largest interference level. Circuit impedances and currents are set such that the noise floor **264** is sufficiently low for an acceptable bit-error rate, while bias currents are set sufficiently high for the required Smax **262**.

Conversely, the input spectrum in FIG. **2**A is that of the best-case input signal, specifically, a robust desired signal accompanied by no or low-level interferers. In this case, the noise floor **214** may be allowed to rise, while the maximum signal handling capability Smax **212** may be reduced. When this is done, the receiver circuit may save significant power. For example, the circuit's impedances may be increased, thus reducing required drive currents. Similarly, bias currents may be lowered, thus reducing the maximum signal in handling capability.

The minimum power dissipation for a circuit is proportional to the required maximum signal-to-noise ratio, which is the ratio between Smax **212** or **262** and N **214** or **264**. Thus, a circuit receiving an input similar to the one shown in FIG. **2**A can dissipate less power than one receiving the input as shown in FIG. **2**B, while still achieving an acceptable bit-error rate.

FIG. **3** illustrates what can occur when the maximum signal handling capability Smax **314** is reduced in the worst-case condition, that is when a weak desired signal **306** is accompanied by large interferers **310** and **312**. Again, signal strength is plotted along a Y-axis **304** as a function of frequency along X-axis **302**. In this specific example, Smax **314** is reduced below the peak levels of the interferers **310** and **312**. Since Smax is low, the circuit cannot handle the interferers linearly. The resulting nonlinearities lead to a mixing of the interferers and the creation of intermodulation products **308** (for example, a third-order intermodulation distortion, IM3), one of which in this example occurs at the same frequency as the desired signal **306**. As can be seen, if the intermodulation products **308** become excessive, the received signal bit error rate may become excessive, and the desired signal **306** may be lost. Accordingly, while Smax may be lowered even under some unfavorable conditions in order to reduce power, care should be taken to avoid corruption of the received desired signal.

FIG. **4** illustrates a portion of a receiver consistent with an embodiment of the present invention. Included is a filter **430**. An optional gain element **420** is placed in front of the filter **430** in order to increase signal levels. Signal strength indicator circuits **440** and **450** are connected to input line **410** and output line **460**. In this specific example, the input signal spectrum on line **410** is shown as desired signal **412** and interferers **414** and **416**. The signal spectrum at the output line **460** is shown as desired signal **462** and interferers **464** and **466**. The signal strength indicators **440** and **450** do not provide information as to the relative sizes of the desired and interfering signals. Rather, a cumulative signal level is provided at their outputs. For example, the first signal strength indicator **440** outputs a level corresponding to the sum of desired signal **412** and interfering signals **414** and **416**, while the second signal strength indicator **450** provides a signal level corresponding to the sum of desired signal **462** and interfering signals **464** and **466**. In this specific example,

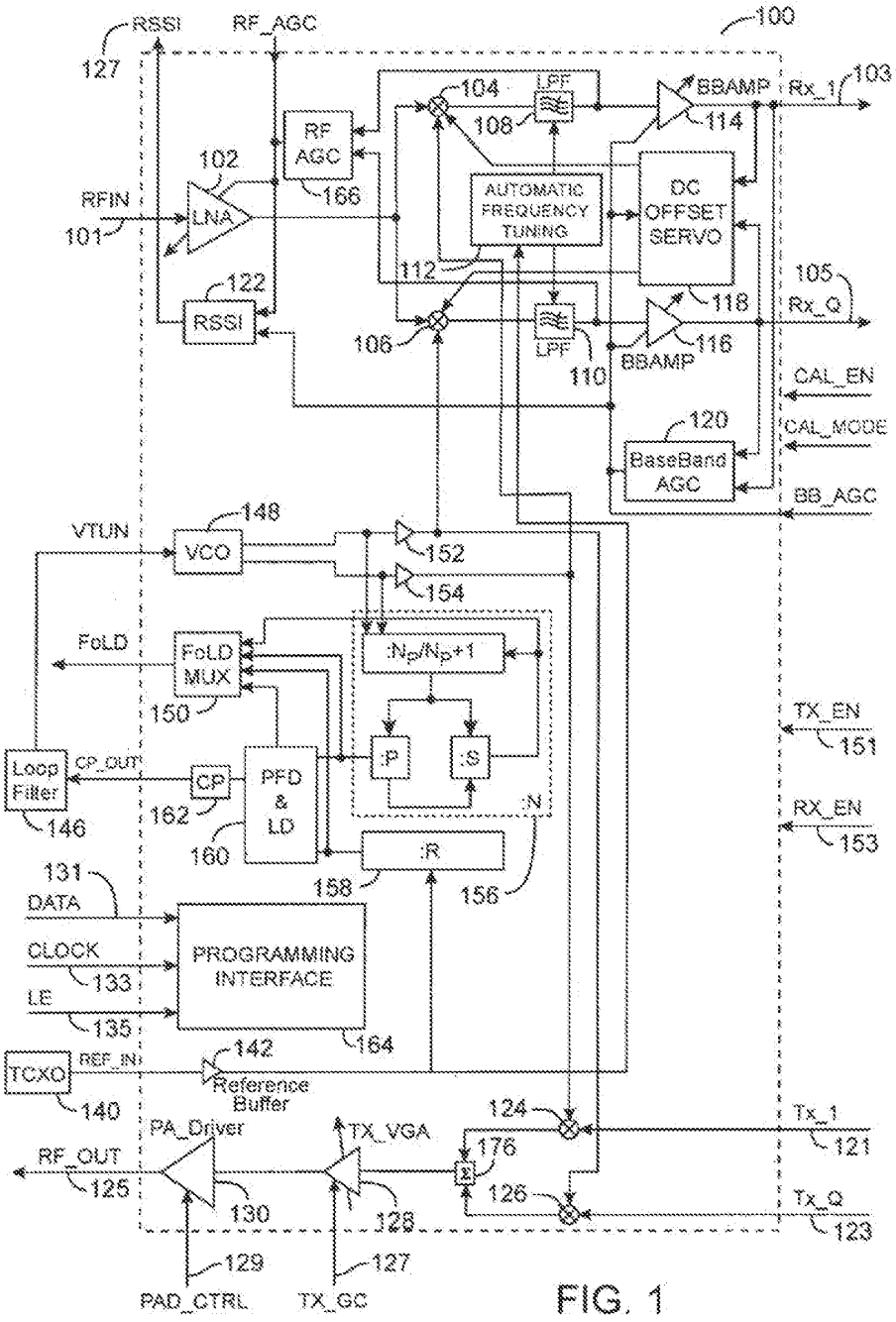

RSSI
RF_AGC
100
127
104
LPF
BBAMP
Rx_1
103
108
114
RF AGC
102
166
RFIN
101
LNA
AUTOMATIC FREQUENCY TUNING
DC OFFSET SERVO
112
105
Rx_Q
118
122
RSSI
106
LPF
110
BBAMP
116
CAL_EN
CAL_MODE
120
BaseBand AGC
BB_AGC
VTUN
148
VCO
152
154
FoLD
FoLD MUX
150
:Np/Np+1
:P
:S
:N
TX_EN
151
Loop Filter
CP_OUT
CP
162
PFD & LD
160
:R
158
156
RX_EN
153
131
DATA
CLOCK
133
LE
135
PROGRAMMING INTERFACE
164
TCXO
REF_IN
142
Reference Buffer
140
124
Tx_1
121
PA_Driver
TX_VGA
RF_OUT
125
176
126
Tx_Q
123
130
128
129
127
PAD_CTRL
TX_GC

FIG. 1

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the gain of the gain and filter circuit combinations is shown as approximately one, while the interfering signals **414** and **416** signal levels are reduced.

A comparison of the signal levels provided by the signal strength indicators **440** and **450** indicates that much of the combined received signal on line **410** has been filtered. Accordingly, it may be deduced that large interfering signals present at the input are being filtered by the filter **430**. From this information, as will be shown in greater detail below, the bias, impedance, and gain of the gain stage **420** and filter **430** combination may be optimized to reduce power dissipation.

There are several real world situations where the received signal is better than the worst-case condition such that power can be saved. For example, large interferers may be present only part of the time, that is, on a temporary or transient basis. The interfering equipment may be some distance from the transceiver, or it may be operating in the low power mode. Also, the desired signal may be very strong as compared to the noise and interferers, for example a hub, router, or access point may be nearby.

Some transceivers consistent with embodiments of the present invention are designed to work with more than one data transfer specification or standard. In this case, when a transceiver is operating in a mode having a lower data rate, the power saving techniques described here may be employed.

FIG. **5** illustrates the relationship between a required biased current **516** for a given output signal **514** for a representative circuit **510**. If the output signal current level is relatively low, such as the output current shown as **526**, the corresponding bias current **528** may be low. Conversely, if the output signal current level is larger as with the example **536**, the corresponding bias current level **538** should also be high. Accordingly, if a bias current is initially set high to handle large a large input signal, for example a large interferer, this current may be reduced if the input signal is smaller.

There are many ways by which these bias currents can be reduced. For example, the current may be generated by placing a voltage across a resistor by applying a bias voltage to the base of a device whose emitter is connected to ground through a resistance. In this case, the resistor may be increased by opening switches across portions of the resistance, or lowering the bias voltage applied at the base. Several ways in which this may be done will be readily understood by one skilled in the art.

FIG. **6** is an example of how a circuit's impedances may be scaled to reduce drive currents, and, depending on the circuit configuration used, associated bias currents as well. A driver **612** has a load R **614** and C **616**. The frequency response of this circuit is the same as that seen by driver **622**, which drives an impedance of 2R **624** and C/2 **626**. But the impedance of the load seen by driver **622** is double that seen by **612**, thus the output current required by the driver **622** is reduced by one-half.

As an example, the output stage of each of these drivers may be a Class A emitter follower formed by an emitter follower connected to a current source. When the outputs are driven high, the emitter of driver **622** need supply only one-half the drive current as driver **612**. In this way, an impedance can be scaled in order to decrease a circuit's required drive current.

Also, the discharge current for driver **622** is only one half that of driver **612** for a given negative-going slew rate. Thus, the current source of **622** may be reduced by the same factor of one-half as compared to driver **612**. In this example, the bias current, that is the current in the pull-down current source can be reduced. Many other examples where drive currents and possibly bias currents may be reduced will be appreciated by one skilled in the art.

FIG. **7** illustrates another degree of freedom that made be employed to reduce current levels in a transceiver. Specifically, a gain element **720** may be inserted in front of a circuit block **730** in order to improve the combined circuit's signal-to-noise ratio by a factor equal to the gain of the inserted gain block. This is particularly useful when large interferers are absent and the desired received signal is moderate or low. Specifically, gain is added to the signal while impedances are increased, which raise the noise floor. In this way, a given signal-to-noise ratio may be maintained while the power is decreased.

The gain of such an element may be varied by increasing a current in a differential pair or increasing a load resistance using switches. Many other examples where the gain of this element may be varied will be appreciated by one skilled in the art.

These variables, or degrees of freedom, specifically reducing bias currents, increasing impedances, and increasing gain may be used as in the following examples.

FIG. **8**A is a block diagram of a functional block **820** and optional gain element **810** in accordance with an embodiment of the present invention. Functional block **820**, like the functional blocks in the following diagrams, may be a filter, mixer, amplifier, or other circuit or circuits in a wireless transceiver or other electronic circuits or system. An input signal is received on line **812** by the optional gain element **814**. When the optional gain block **810** is not used, the input signal may be received directly by the function block **820**. The gain of the optional gain element **812** is controlled by a gain control signal on line **814**. The functional block receives an output signal from the optional gain element **810** and provides an output VOUT on line **822**. The lines in this and the other included figures may be one or more lines, depending on whether single-ended, differential, or other type of signaling is employed.

One or more impedances are under control of signals on impedance control lines **824**. Similarly, one or more bias currents in the function block are under control of one or more signals on bias control lines **826**. These various control lines may be logic signals, analog signals, voltage or currents lines, or other signal or bias lines. In other embodiments of the present invention, the gain control element **810** may be included in the function block **820**. Also, various embodiments may not incorporate either or both the impedance control and bias control.

FIG. **8**B is an example input that may be present on line VIN **812**. In this example, a desired signal **836** is relatively weak, as are interfering signals **837** and **838**. The initial bias and circuit configuration is such that the noise floor **833** and maximum signal handling capability Smax **831** are adjusted for worst case conditions. The circuit of FIG. **8**A, as with all the circuits described here, receives noise at its input which may be referred to as input equivalent noise or input referred noise. Additionally, the circuit of FIG. **8**A generates noise which is added to the input referred noise. Depending on the gain characteristics of the circuitry, the output noise at various frequencies may be greater than, equal to, or less than the input referred noise. For simplicity, the noise floor and maximum signal handling capability Smax, in this and the other figures, are shown as straight lines, though the noise and Smax are typically curved as a function of frequency.

That the input spectrum is as shown in FIG. **8**B can be determined, for example, by low signal strength indications

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on line VIN **812** and VOUT **822**. That is, a low level signal strength indication on line VIN **812** indicates that no portion of the input signal is particularly large.

For this exemplary input, there are at least two methods by which the power dissipation for this circuitry may be reduced. Depending on the exact circuits and structures used, one of these methods may be preferred.

In FIG. **8**C, the bias current is decreased, thereby lowering the maximum signal handling capability **841** as compared to **831**, closer to the desired and interfering signal levels. Again, the bias currents in the function block **820** may be reduced by switching impedances that appear across a voltage thereby changing a resulting bias current, by reducing a voltage at the gate of a MOS or base of a bipolar transistor, or by other methods.

In FIG. **8**D, a second method of reducing power dissipation in the function block **820** is employed. Specifically, Smax **851** is held constant as compared Smax **831**. The desired and interfering signals are amplified such that they are closer to the available signaling handling capability **851**. Also, the noise floor **853** is raised as compared to noise floor **833** in FIG. **8**B. Specifically, the noise contributed by the function block **820** is increased, such that the noise at its output is increased to noise floor **853**. This is done by increasing one or more impedance in function block **810**, such that drive currents inside that block are reduced. Depending on the exact configuration, this may also allow some biasing currents to be reduced, while maintaining the maximum signal handling capability **851** at a sufficient level. Alternately, these two methods of reducing power dissipation in function block **820** may be done in combination.

The included examples are explained for the exemplary situation where biasing and other parameters are set for worst-case conditions, and then changed to save power when it is discovered that the conditions are better-than-worst case. Alternately, the bias currents and other parameters may be set for maximum power savings, or an intermediate point, and the power can be adjusted from there.

FIG. **9**A illustrates a block diagram including an optional gain element **910** and function block **920**. Again, an input signal is received on line **912** by optional gain element **910** which in turn drives function block **920**. The function block provides an output VOUT on line **922**, and receives impedance and bias control signals on lines **924** and **926**.

FIG. **9**B shows the spectrum for what may be considered a best-case received signal. Specifically, the desired signal **936** is strong, while the interfering signals **937** and **938** are relatively weak. This may be determined, for example, by detecting a large signal level at the input line VIN **812** and a large signal level after a filter, since these readings would indicate that a large signal is received, but that it is at the desired signal frequency.

The maximum signaling capability **931** and noise floor **933** are shown as being set for the worst case conditions. In this case, the noise floor **933** is lower than the maximum allowed for proper signal reception. Accordingly, one or more impedance in the function block **920** may be increased, such that the noise floor **943** rises as shown in FIG. **9**C. In this way one or more of the driving currents in the function block **920** may be reduced. Similarly, since the drive current is reduced, one or more bias current may also be reduced, depending on the exact circuit configuration.

FIG. **10**A illustrates a block diagram showing an optional gain element **1010** driving a function block **1020**. An input signal is received by the gain element **1010** on line **1012**, and an output is provided by function block **1020** on line VOUT **1022**. One or more gain control signals present on lines **1014** control the gain of gain control element **1010**, while one or more impedance and bias control signals are received by the function block **1020** on line to **1024** and **1026**.

FIG. **10**B illustrates a received signal that may be received on line VIN **1012**. In this example, the desired signal **1036** and interferers **1037** and **1038** are each relatively large. This may be determined, for example, by detecting a large signal level at the input line VIN **812** and a smaller signal level after a filter, since these readings would indicate that a large signal is received, but that interferers are being reduced.

As before, in this example, the noise floor **1033** and maximum signal handling capability **1031** are initially set for the worst case conditions. Since the desired signal is relatively large in this case, the noise floor may be allowed to rise, a shown by noise floor **1043** in FIG. **10**C. Since the desired signal **1046** and interferers **1047** are large, the maximum signal handling capability Smax **1041** remains constant. Again, the noise floor is increased by increasing impedances in the function block **1020**. This reduces the required drive current, and may also allow for a reduction in bias currents.

FIG. **11**A illustrates a block diagram including an optional gain element **1110** and function block **1120** in accordance with an embodiment of the present convention. An input signal is received on line **1112** by the optional gain control element **1110**, while an output signal is provided by the function block **1120** on line VOUT **1122**. Gain, impedance, and bias control signals are received on lines **1114**, **1124**, and **1126**.

FIG. **11**B is an exemplary input signal that may be received by the gain control element **1110** on line VIN **1112**. In this specific example, the desired signal **1136** is relatively low or weak while the interfering signals **1137** and **1138** are large. This may be determined, for example, by detecting a large signal level at the input line VIN **812** and a much smaller signal level after a filter, since these readings would indicate that a large signal is received and that large interferers are being reduced such that the resulting signal, the desired signal, is relatively weak.

Again, the maximum signal handling capability **1131** and noise floor **1133** are initially set for worst case conditions. If the desired signal is sufficiently low, while the interferers are sufficiently high, power savings may not be achievable over the worst case settings, since this is in fact the worst case condition. But, if the desired signal is somewhat larger than the worst case condition, then power may be saved in at least two different ways.

For example, FIG. **11**C shows the maximum signal handling capability **1141** being lowered. In this case, the interfering signals **1147** in **1148** began to clip and distort, thereby creating intermodulation products **1145**, which distort the desired signal **1146**. So long as care is taken to not corrupt the desired signal **1146** beyond an acceptable limit, typically measured by a bit-error rate, power may be reduced in this way.

Similarly, in FIG. **11**D, the noise floor **1153** is raised somewhat, thereby saving power. Again, this may be done so long as the noise floor is not sufficiently high that the system bit-error rate becomes unacceptable.

FIG. **12** is a summary of the above four examples. The received signal strengths are shown in column **1210**, while appropriate power saving responses are listed in column **1220**. Specifically, in row **1230**, the desired signal and interferer signal strengths are both weak or small. In this case, proper responses include decreasing Smax, or increasing one or more circuit impedances while increasing the circuit gain. Depending on the exact circuit configuration,

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one of these options may be preferred over the other. Alternately, they may be done in combination, or done in combination with other power saving techniques. Also, in some specific embodiments, when both desired signal and interferer signal strengths are small, the gain may need to be increased while the impedance is maintained or not increased in order to keep the noise floor low.

In row **1240**, the desired signal strength is strong or large, while the interfering signals are small. In this case, an appropriate response is to increase one or more of the circuit impedances. Again, depending on the exact circuit in question, one or more of the bias currents may also be reduced.

In row **1250**, both the desired signals and interfering signal strengths are large. Again, in this case an appropriate response is to increase one or more of the circuit impedances.

In row **1260**, the received desired signal strength is weak or small, while the interfering signals are large. Since this is the worst case situation for which the circuit is designed, substantial power savings are difficult to achieve. However, again, if the received signal is above a minimum level necessary for proper operation, some distortion of the interferers or raising of the noise floor may be acceptable.

It should be noted that not all possible signal conditions are listed here. For example, either the signal or interferer may be of a relatively medium strength, or the interferer may be absent. Also, these terms are for exemplary purposes and are not meant to convey specific signal conditions, but rather are only qualitative. The proper response to a specific condition depends on the embodiment of the present invention, the particular circuit topology, the requirements of the signaling standard used, as well as other constraints.

FIG. **13** is an example shown how power may be saved as a function of time by employing one or more of these methods consistent with embodiments of the present invention. Power is plotted along a Y-axis **1304** as a function of time along X-axis **1302**. Conventional worst case design would fix power dissipation at line **1310**. As can be seen, dynamic power dissipation **1320** under the control of variable gains, impedances, biasing, or combination thereof, allows for a lower average power **1330** as compared to the power dissipated **1310** by the conventional design.

FIG. **14** is a block diagram of a portion of a receiver consistent with an embodiment of the present invention. Included are low-noise amplifier **1410**, mixer **1420**, gain stage **1430**, filter **1440**, AGC amplifier **1450**, and VCO **1460**. Signal strength detection is done at the output of the low-noise amplifier by signal strength indicator **1470**, at the output of the mixer by signal strength indicator **1472**, and at the output of the filter by signal strength indicator **1474**. The outputs of the signal strength indicator circuits are received by the computational circuit **1470**, which in turn controls gain and power control circuits **1480** and **1485**. Power and gain control circuits **1480** and **1485** control the gain, biasing, and impedance levels of the circuits in the receiver signal path. Also, the gain and power control circuits may control the same parameters in the VCO **1460**. This figure is greatly simplified for purposes of explanation. For example, the quadrature nature of the mixers and following circuits are not shown. Also, power-down and start-up circuits are not included.

The current level in the low-noise amplifier determines a multitude of parameters including voltage gain, linearity, input impedance matching, and noise figure. When conditions are better than worst-case, some of these parameters may be relaxed while maintaining an acceptable bit-error rate, thus saving power.

The bias current in the mixers effect that block's noise figure and linearity. Care is taken in reducing power in this block so as not to increase nonlinearities, particularly the third-order nonlinearity as measured by IP3, the third-order intercept point, beyond an acceptable limit.

A key parameter of the VCO is phase noise, an increase in which increases the sidebands on either side of the oscillation signal. During transmission, the phase noise should be kept low to avoid interference with adjacent channels and for preserving modulation information.

During reception however, if the conditions are better than worst case, the phase noise requirement for the VCO is relaxed, and power can be saved consistent with embodiments of the present invention. The achievable phase noise power spectral density is approximately inversely proportional to the bias current used. Thus, when low phase noise is not required during reception, bias current in the VCO can be reduced.

Most of the power savings in a transceiver in accordance with embodiments of the present invention is achieved in the receiver portion. Additional power may be saved in the transmitter section.

FIG. **15** is a block diagram of a transmitter portion consistent with an embodiment of the present invention. Included is a signal path formed by gain stage **1510** and power amplifier **1520**. The output power level is sensed by output level sensing circuit **1550**, which in turn adjusts the biasing of the power amplifier **1520** through the power control circuit **1540**. Additionally, a transmitter level control signal is received by power control circuits **1530** and **1540**, which in turn control the biasing of gain stage **1510** and power amplifier **1520**. Gain control circuit **1560** also adjusts the gain of gain stage **1510** and power amplifier **1520**. Additional circuitry that varies impedances in each of these circuits may also be included.

Since the gain, impedance and biasing of these blocks are being dynamically varied, care must be taken to not negatively affect the signal being processed. For example, specific embodiments of the present invention perform some or all of these variations during preamble. Also, as changes occur, the circuits in some embodiments are limited such that they may only adapt to an improvement in conditions after frames are completed. If conditions worsen, the circuits may be allowed to change in order to save the data. Alternately, a system may be manually calibrated, for example at set up, and when the network configuration is changed.

The above description of specific embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form described, and many modifications and variations are possible in light of the teaching above. The embodiments were chosen and described in order to best explain the principles of the invention and its practical applications to thereby enable others skilled in the art to best utilize the invention in various embodiments and with various modifications as are suited to the particular use contemplated.

What is claimed is:

1. A method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, and a corresponding increase in battery life of the battery powered portable wireless device, the method comprising:

receiving a wireless signal having a desired signal and an interferer signal, by the wireless transceiver of the battery powered portable wireless device, the wireless

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transceiver having a receiver signal path comprising a plurality of circuits, wherein the plurality of circuits includes an amplifier, a filter, and a mixer, and wherein the wireless transceiver comprises a circuit for determining a signal strength of the interferer signal and a circuit for determining a signal strength of the desired signal;

wherein a worst-case power dissipation condition results when the signal strength of the desired signal is low and the signal strength of the interferer signal is high; and

wherein the power dissipation reduction in the receiver is achieved by causing a bias current to vary in one or more of the plurality of circuits in the receiver signal path of the wireless transceiver as the signal strength of the interferer signal and the signal strength of the desired signal vary according to the following:

(i) when the signal strength of the interferer signal is high and the signal strength of the desired signal is low, and the desired signal is larger than in the worst-case power dissipation condition, causing the bias current of the one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be reduced compared to the worst-case power dissipation condition, thereby saving power; and

(ii) when the signal strength of the interferer signal is weak and the signal strength of the desired signal is weak, causing the bias current of the one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be decreased compared to the worst-case power dissipation condition, thereby saving power.

2. The method of claim 1, wherein the change in the bias current of the one or more of the plurality of circuits in the receiver signal path is related to a change in an impedance in the one or more of the plurality of circuits in the receiver signal path and wherein the impedance comprises at least a resistor and a capacitor.

3. A method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, and a corresponding increase in battery life of the battery powered portable wireless device, the method comprising:

receiving a wireless signal having a desired signal and an interferer signal, by the wireless transceiver of the battery powered portable wireless device, the wireless transceiver having a receiver signal path comprising a plurality of circuits, wherein the plurality of circuits includes an amplifier, a filter, and a mixer, and wherein the wireless transceiver comprises a circuit for determining a signal strength of the interferer signal and a circuit for determining a signal strength of the desired signal;

wherein a worst-case power dissipation condition from the battery results when the signal strength of the desired signal is low and the signal strength of the interferer signal is high; and

wherein the power dissipation reduction in the receiver is achieved by causing a bias current to vary in one or more of the plurality of circuits in the receiver signal path of the wireless transceiver as the signal strength of the interferer signal and the signal strength of the desired signal vary, according to the following:

when the signal strength of the interferer signal is high and the signal strength of the desired signal is low, and the desired signal has a signal strength that is larger than in the worst-case power dissipation conditions, causing the bias current of the one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be decreased compared to the worst-case power dissipation condition, causing a reduction in power dissipation.

4. The method of claim 3, wherein the change in the bias current of the one or more of the plurality of circuits in the receiver signal path is related to a change in an impedance in the one or more of the plurality of circuits in the receiver signal path;

and wherein the impedance comprises at least a resistor and a capacitor.

5. A method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, and a corresponding reduction in a drain on battery life of the battery powered portable wireless device, the method comprising:

receiving a wireless signal having a desired signal and an interferer signal, by the wireless transceiver of the battery powered portable wireless device, the wireless transceiver having a receiver signal path comprising a plurality of circuits, wherein the plurality of circuits includes an amplifier, a filter, and a mixer, and wherein the wireless transceiver comprises a circuit for determining a signal strength of the interferer signal and a circuit for determining a signal strength of the desired signal;

wherein a worst-case power dissipation condition results when the signal strength of the desired signal is low and the signal strength of the interferer signal is high; and

wherein the power dissipation reduction in the receiver is achieved by causing a bias current to vary in one or more of the plurality of circuits in the receiver signal path of the wireless transceiver as the signal strength of the interferer signal and the signal strength of the desired signal vary, according to the following:

(i) when the signal strength of the interferer signal is high and the signal strength of the desired signal is weak, and the desired signal is larger than in the worst-case power dissipation condition, causing the bias current of the one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be reduced compared to the worst-case power dissipation condition, thereby saving power;

(ii) when the signal strength of the interferer signal is high and the signal strength of the desired signal is high, causing the bias current of the one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be decreased compared to the worst-case power dissipation condition, thereby saving power;

(iii) when the signal strength of the interferer signal is weak and the signal strength of the desired signal is weak, causing the bias current of the one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be decreased compared to the worst-case power dissipation condition, thereby saving power; and

(iv) when the signal strength of the interferer signal is weak and the signal strength of the desired signal is high, causing the bias current of the one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be decreased compared to the worst-case power dissipation condition, thereby saving power.

6. The method of claim 5, wherein the change in the bias current of the one or more of the plurality of circuits in the

receiver signal path is related to a change in an impedance in the one or more of the plurality of circuits in the receiver signal path;

and wherein the impedance comprises at least a resistor and a capacitor.

7. A method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, and a corresponding reduction in a drain on battery life of the battery powered portable wireless device, the method comprising:

receiving a wireless signal having a desired signal and an interferer signal, by the wireless transceiver of the battery powered portable wireless device, the wireless transceiver having a receiver signal path comprising a plurality of circuits, wherein the plurality of circuits includes an amplifier, a filter, and a mixer, and wherein the wireless transceiver comprises a circuit for determining a signal strength of the interferer signal and a signal strength of the desired signal in the receiver signal path;

wherein a worst-case power dissipation condition in the receiver results when the signal strength of the desired signal is low and the signal strength of the interferer signal is high; and

wherein the power dissipation reduction is achieved by causing an impedance and a bias current of one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to vary as the signal strength of the interferer signal and the signal strength of the desired signal to vary according to the following:

(i) when the signal strength of the interferer signal is high and the signal strength of the desired signal is low and the desired signal is larger than in the worst-case power dissipation conditions, causing the bias current of the circuit in the receiver signal path of the wireless transceiver to be reduced compared to the worst-case power dissipation condition, causing a reduction in power dissipation;

(ii) when the signal strength of the interferer signal is high and the signal strength of the desired signal is high, causing the impedance of the circuit in the receiver signal path of the wireless transceiver to be increased compared to the worst-case power dissipation condition, causing a reduction in power dissipation;

(iii) when the signal strength of the interferer signal is low and the signal strength of the desired signal is low, causing the bias current of the circuit in the receiver signal path of the wireless transceiver to be reduced compared to the worst-case power dissipation condition, causing a reduction in power dissipation;

(iv) when the signal strength of the interferer signal is low and the signal strength of the desired signal is high, causing the impedance of the circuit in the receiver signal path of the wireless transceiver to be increased compared to the worst-case power dissipation condition, causing a reduction in power dissipation; and

wherein increasing the impedance of the circuit reduces a drive current of the circuit and reduces the associated bias current of the circuit.

8. A method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, and a corresponding reduction in power dissipation and an increase in battery life of the battery powered portable wireless device, the method comprising:

receiving a wireless signal having a desired signal and an interferer signal, by the wireless transceiver of the battery powered portable wireless device, the wireless transceiver having a receiver signal path comprising a plurality of circuits, wherein the plurality of circuits includes an amplifier, a filter, and a mixer, and wherein the wireless transceiver comprises a circuit for determining a signal strength of the interferer signal and a circuit for determining a signal strength of the desired signal;

wherein a worst-case power dissipation condition from the battery results when the signal strength of the desired signal is low and the signal strength of the interferer signal is high; and

wherein the power dissipation reduction in the receiver is achieved by causing a bias current and an impedance to vary in one or more of the plurality of circuits in the receiver signal path of the wireless transceiver as the signal strength of the interferer signal and the signal strength of the desired signal vary, according to the following:

when the signal strength of the interferer signal is high and the signal strength of the desired signal is low, and the desired signal has a signal strength that is larger than in the worst-case power dissipation condition, causing:

(i) the bias current of the one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be decreased; and

(ii) an impedance of the one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be increased, thereby causing a drive current of the one or more of the plurality of circuits to be decreased.

* * * * *

Exhibit C

US010524202B2

(12) **United States Patent**
Tsividis

(10) **Patent No.: US 10,524,202 B2**
(45) **Date of Patent: *Dec. 31, 2019**

(54) **POWER DISSIPATION REDUCTION IN WIRELESS TRANSCEIVERS**

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(72) Inventor: **Yannis Tsividis**, New York, NY (US)

(73) Assignee: **THETA IP, LLC**, Coppell, TX (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **15/824,841**

(22) Filed: **Nov. 28, 2017**

(65) **Prior Publication Data**

US 2018/0084492 A1 Mar. 22, 2018

Related U.S. Application Data

(63) Continuation of application No. 15/080,421, filed on Mar. 24, 2016, now Pat. No. 9,838,962, which is a (Continued)

(51) **Int. Cl.**
H04B 1/38 (2015.01)
H04M 1/00 (2006.01)
(Continued)

(52) **U.S. Cl.**
CPC ***H04W 52/0209*** (2013.01); ***H04B 1/109*** (2013.01); *Y02D 70/00* (2018.01); *Y02D 70/142* (2018.01); *Y02D 70/40* (2018.01)

(58) **Field of Classification Search**
CPC H04B 1/16; H04B 1/1607; H04B 1/40; H04B 17/318; H04W 52/52; H03F 1/56;
(Continued)

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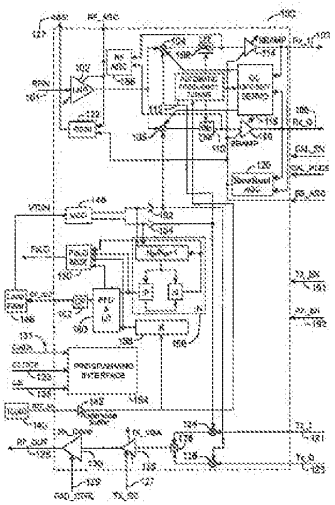
US 6,529,069 B2, 03/2003, Krishnapura et al. (withdrawn)
(Continued)

Primary Examiner — Quochien B Vuong
(74) *Attorney, Agent, or Firm* — Jennifer Hayes; Nixon Peabody LLP

(57) **ABSTRACT**

Methods and circuits for reducing power dissipation in wireless transceivers and other electronic circuits and systems. Embodiments of the present invention use bias current reduction, impedance scaling, and gain changes either separately or in combination to reduce power dissipation. For example, bias currents are reduced in response to a need for reduced signal handling capability, impedances are scaled thus reducing required drive and other bias currents in response to a strong received signal, or gain is increased and impedances are scaled in response to a low received signal in the presence of no or weak interfering signals.

23 Claims, 15 Drawing Sheets



Related U.S. Application Data

continuation of application No. 11/318,646, filed on Dec. 27, 2005, now Pat. No. 9,331,728, which is a continuation of application No. 10/784,613, filed on Feb. 23, 2004, now Pat. No. 7,010,330.

(60) Provisional application No. 60/451,220, filed on Mar. 1, 2003, provisional application No. 60/451,230, filed on Mar. 1, 2003.

(51) **Int. Cl.**
H04W 52/02 (2009.01)
H04B 1/10 (2006.01)

(58) **Field of Classification Search**
CPC ... H03F 3/20; H03F 2200/27; H03F 2200/78; H03F 2200/387; H03F 2200/451
USPC 455/63.1, 67.13, 127.1, 127.2, 127.5, 455/226.1, 226.2, 232.1, 234.1, 250.1, 455/251.1, 295, 296, 311, 343.1, 572, 455/574; 370/442; 330/127, 134, 144
See application file for complete search history.

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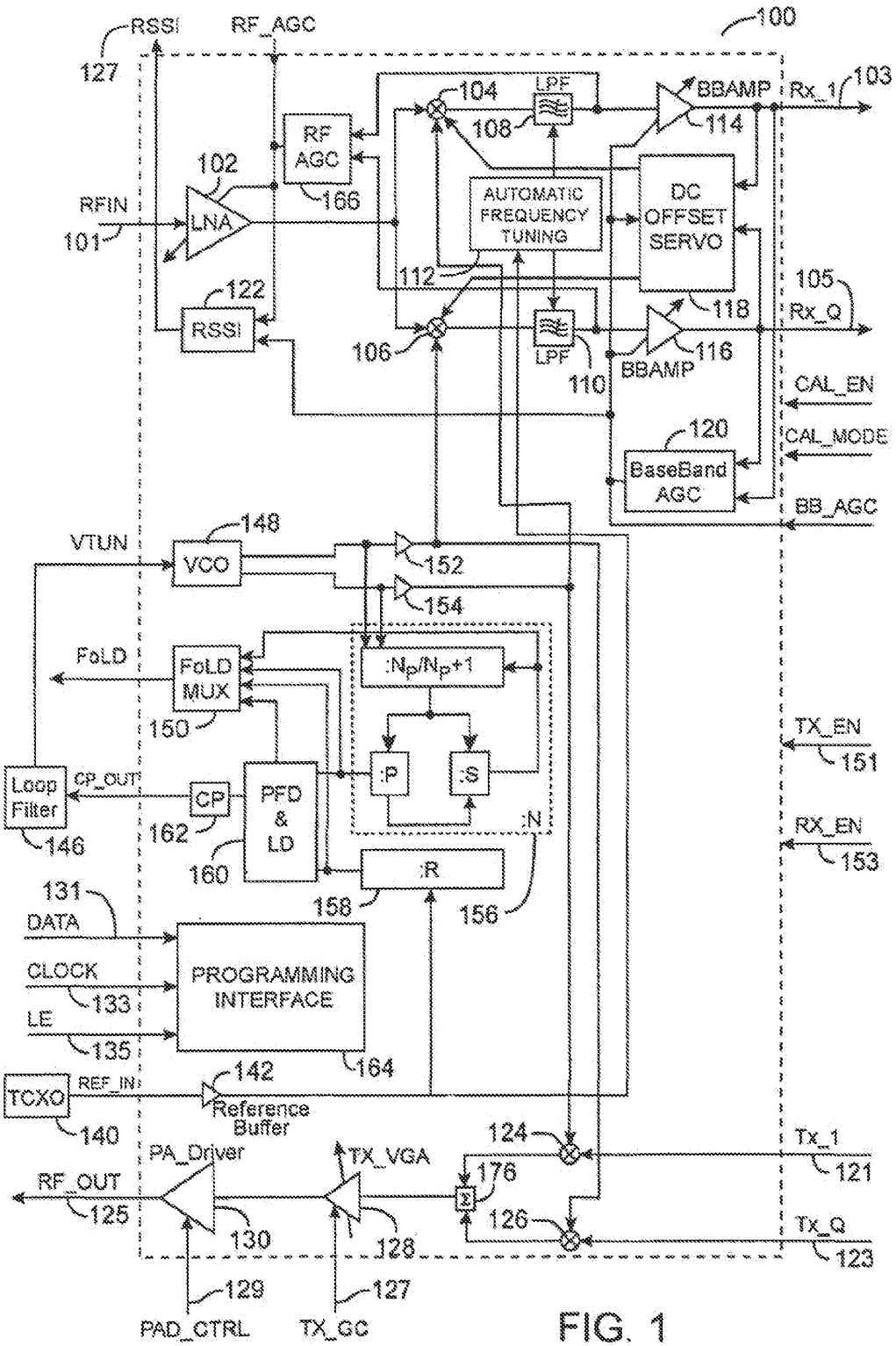

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AUTOMATIC FREQUENCY TUNING
DC OFFSET SERVO
112
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Rx_Q
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RSSI
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:S
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:R
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TX_EN
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RX_EN
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Loop Filter
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PFD & LD
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CLOCK
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LE
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PROGRAMMING INTERFACE
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FIG. 1

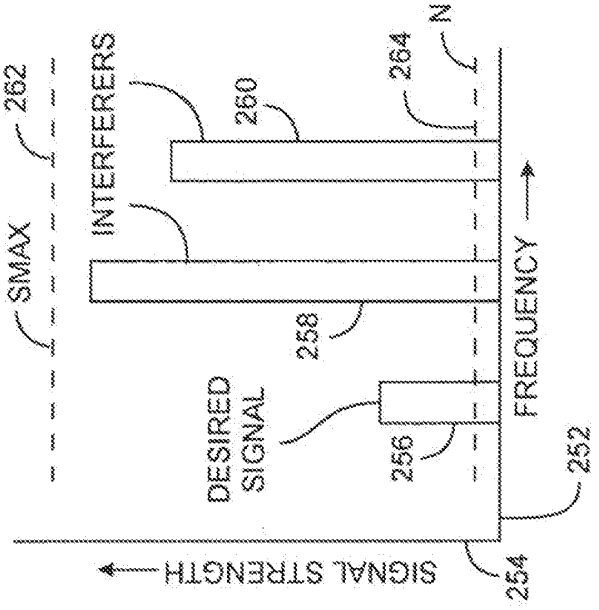

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DESIRED SIGNAL
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FREQUENCY
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SIGNAL STRENGTH
254

FIG. 2B

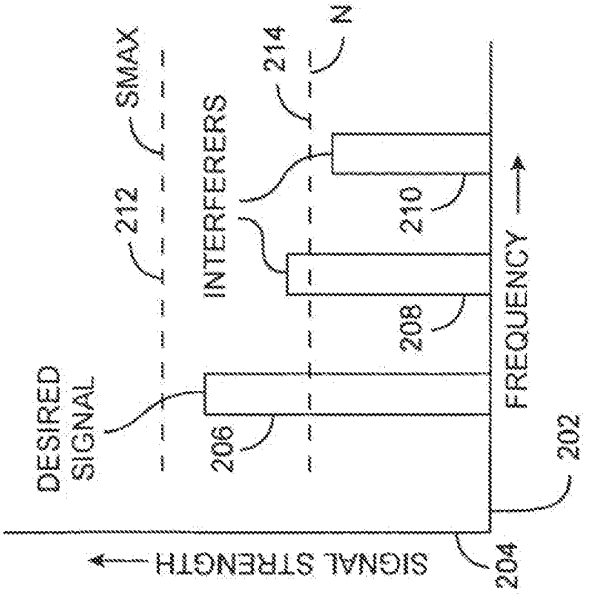

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SIGNAL STRENGTH
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FIG. 2A

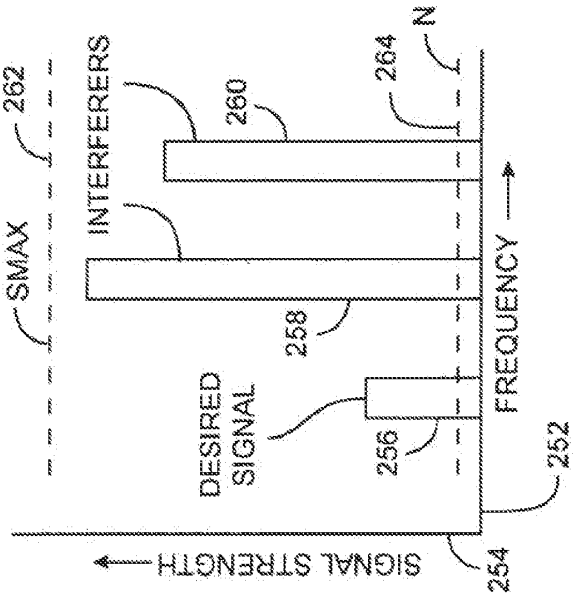

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FIG. 2B

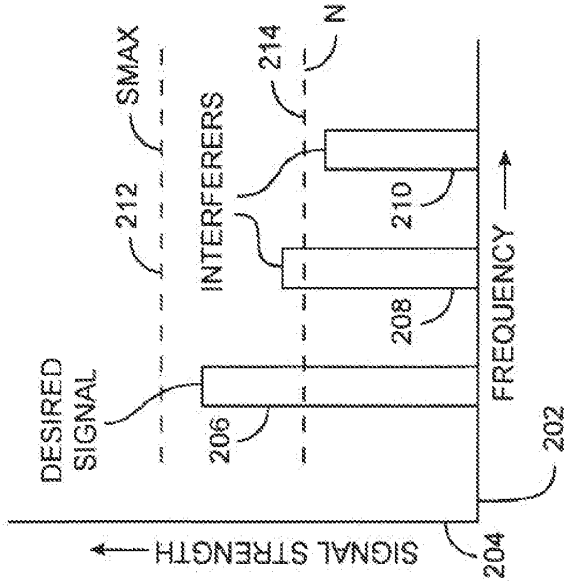

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DESIRED SIGNAL
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FREQUENCY
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SIGNAL STRENGTH
204

FIG 2A

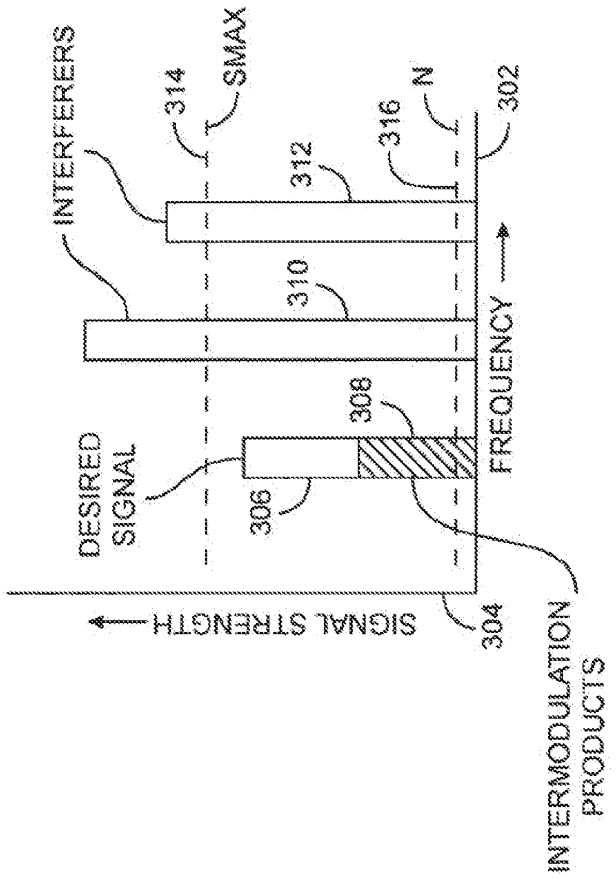

INTERFERERS
314
SMAX
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316
N
302
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FREQUENCY
308
DESIRED SIGNAL
306
SIGNAL STRENGTH
304
INTERMODULATION PRODUCTS

FIG. 3

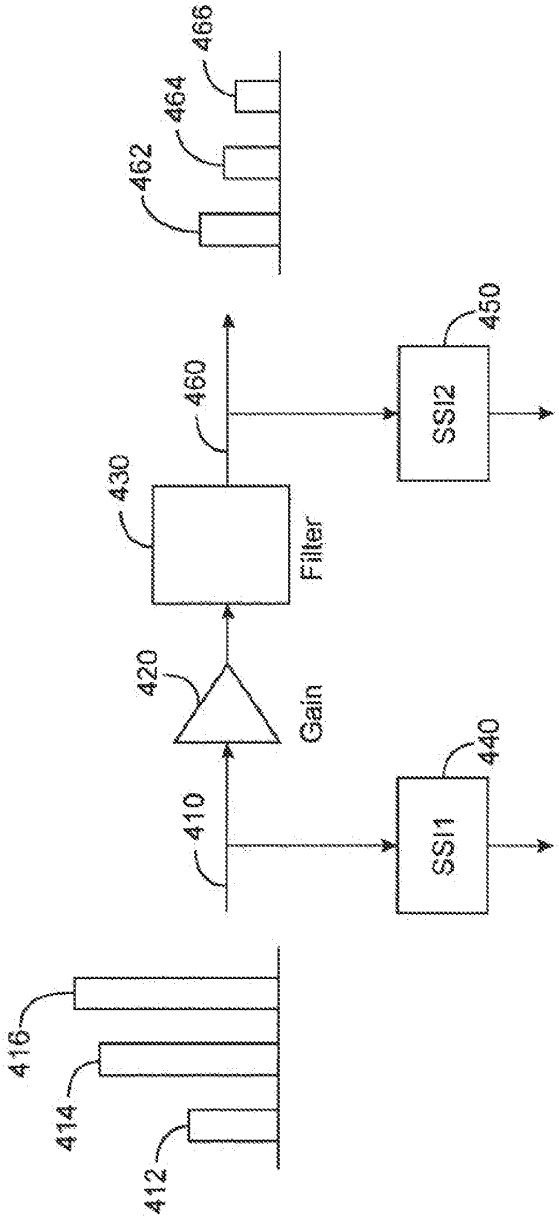

466
464
462
460
450
SSI2
430
Filter
420
Gain
410
440
SSI1
416
414
412

FIG. 4

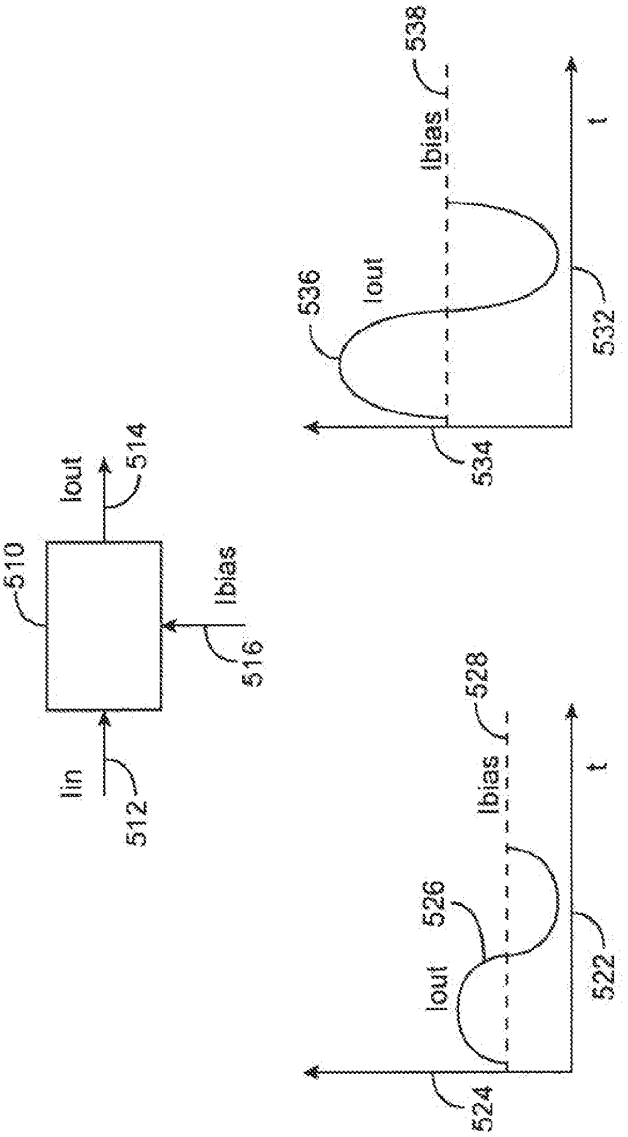

Iout
514
510
Ibias
516
Iin
512
538
Ibias
t
536
Iout
532
534
528
Ibias
t
526
Iout
522
524

FIG 5

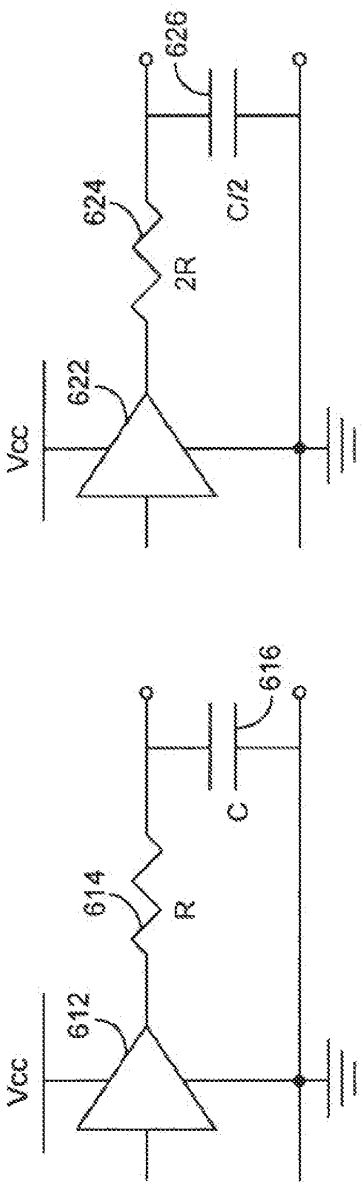


FIG 6

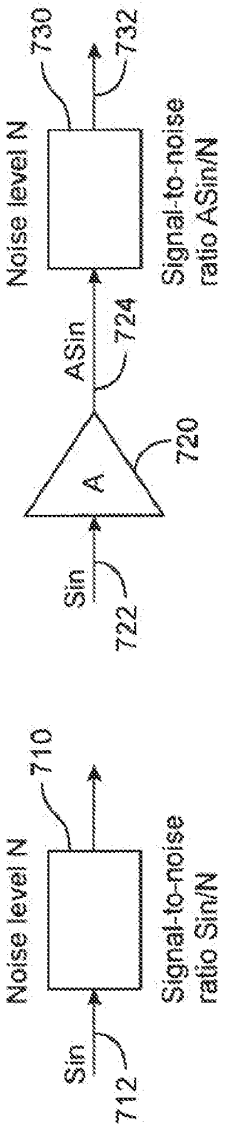

730
732
Noise level N
Signal-to-noise ratio ASin/N
ASin
724
A
720
Sin
722
710
Noise level N
Signal-to-noise ratio Sin/N
Sin
712

FIG. 7

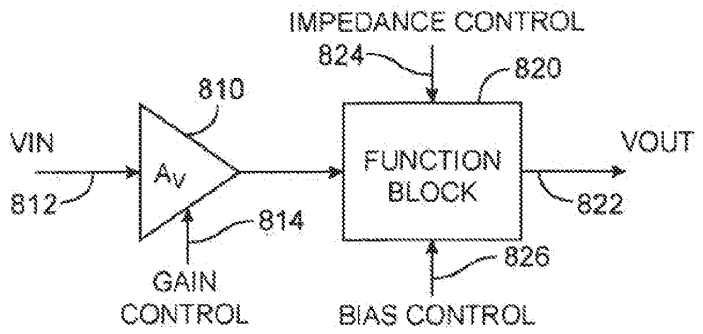


FIG. 8A

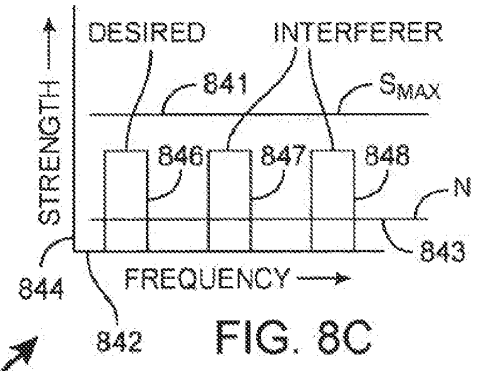


FIG. 8C

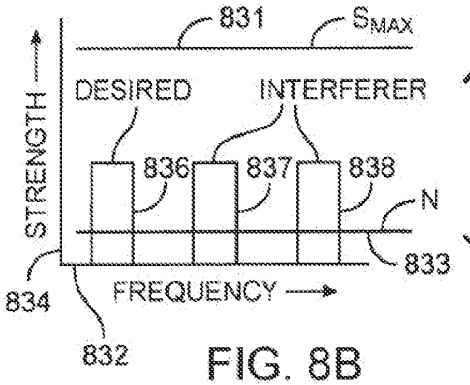


FIG. 8B

DECREASE BIASING

– AND/OR –

INCREASE GAIN AND IMPEDANCES

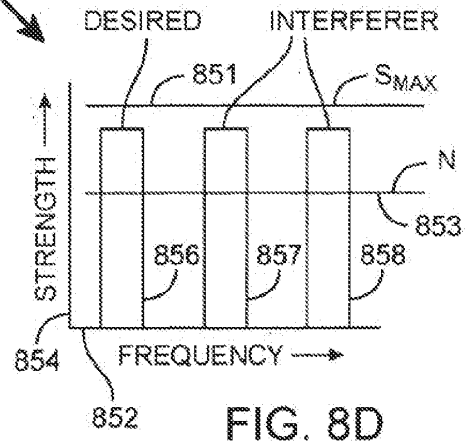


FIG. 8D

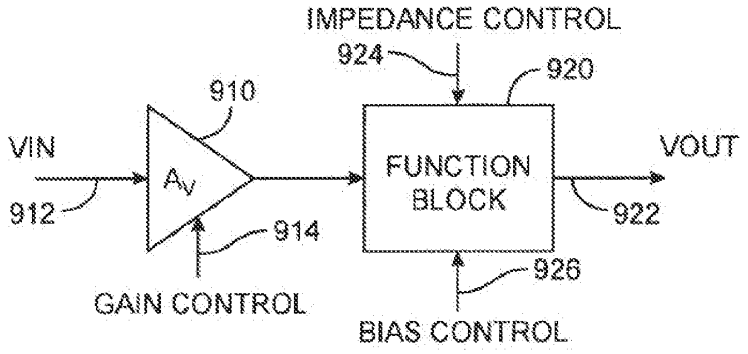


FIG. 9A

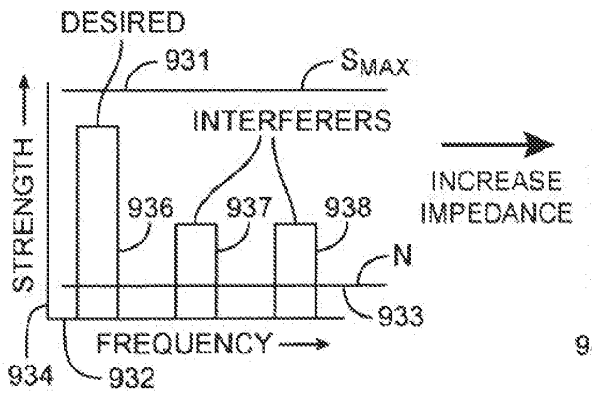


FIG. 9B

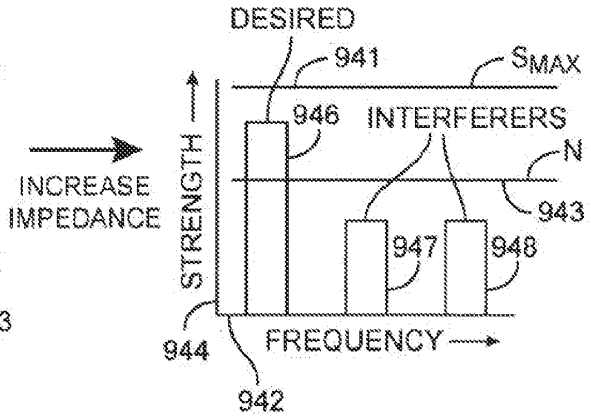


FIG. 9C

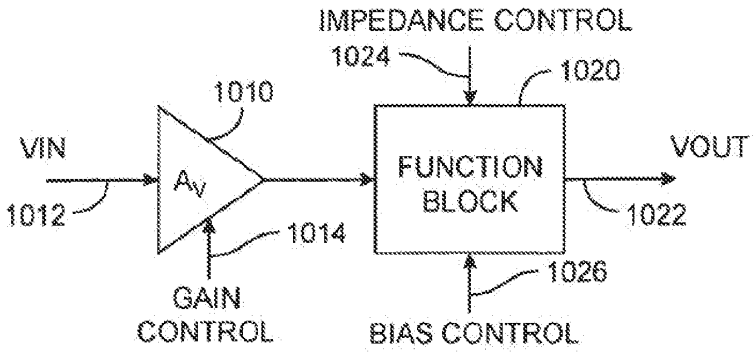


FIG. 10A

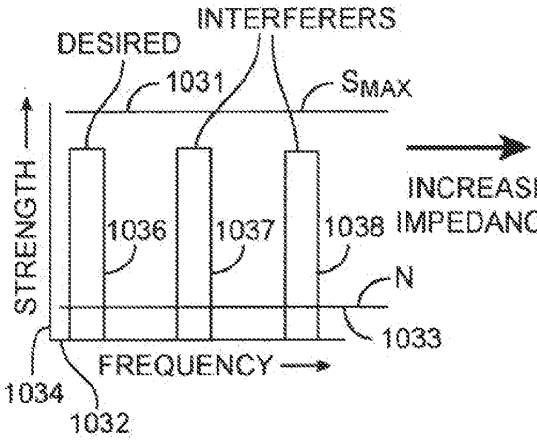


FIG. 10B

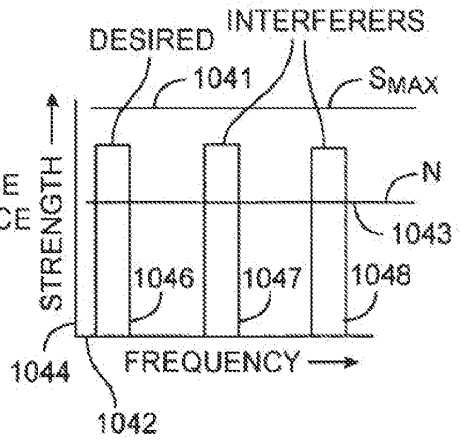


FIG. 10C

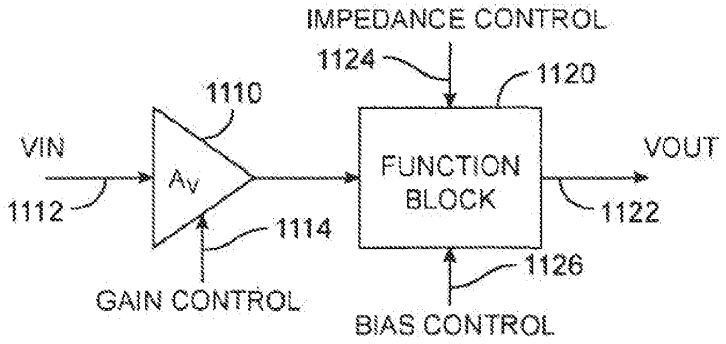


FIG. 11A

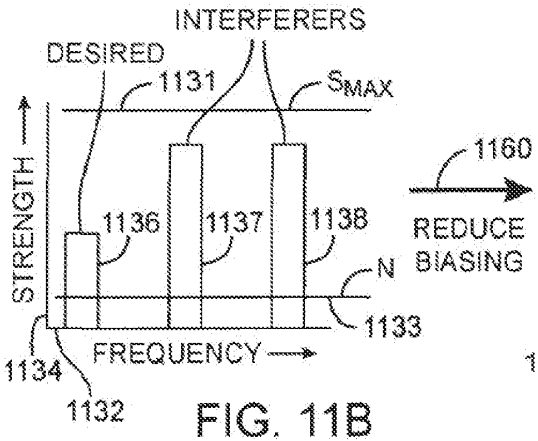


FIG. 11B

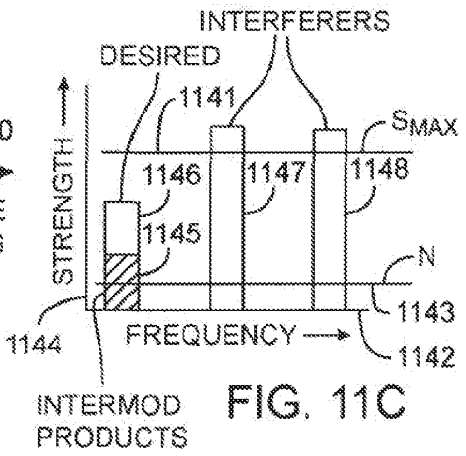
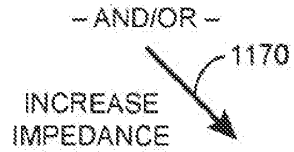


FIG. 11C



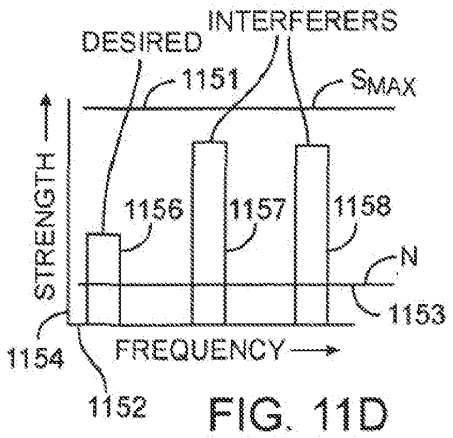


FIG. 11D

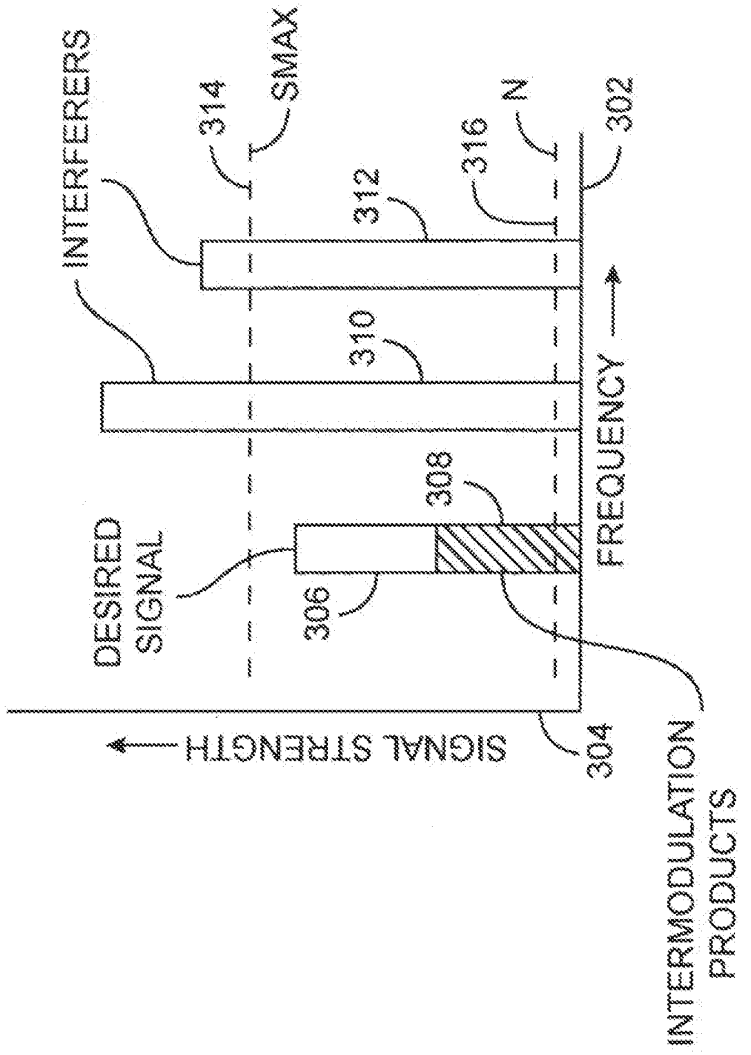

INTERFERERS
314
SMAX
312
316
N
302
310
308
DESIRED SIGNAL
306
FREQUENCY
SIGNAL STRENGTH
304
INTERMODULATION PRODUCTS

FIG. 3

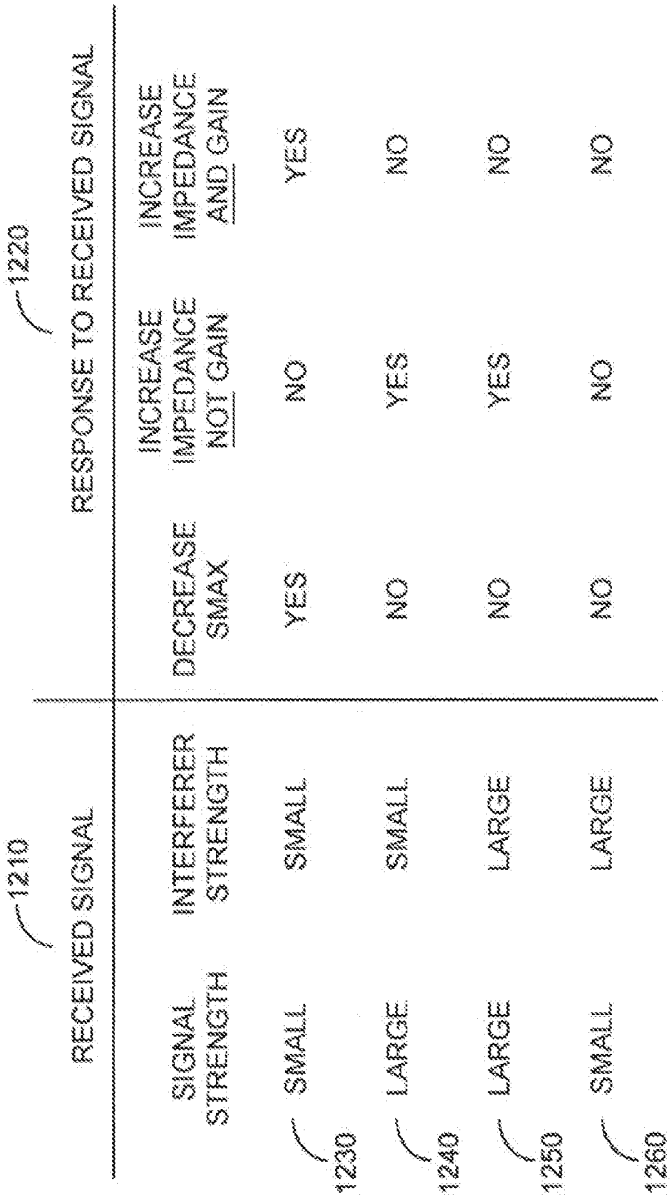

1210
RECEIVED SIGNAL
1220
RESPONSE TO RECEIVED SIGNAL
SIGNAL STRENGTH
INTERFERER STRENGTH
DECREASE SMAX
INCREASE IMPEDANCE NOT GAIN
INCREASE IMPEDANCE AND GAIN
SMALL
SMALL
YES
NO
YES
1230
LARGE
SMALL
NO
YES
NO
1240
LARGE
LARGE
NO
YES
NO
1250
SMALL
LARGE
NO
NO
NO
1260

FIG. 12

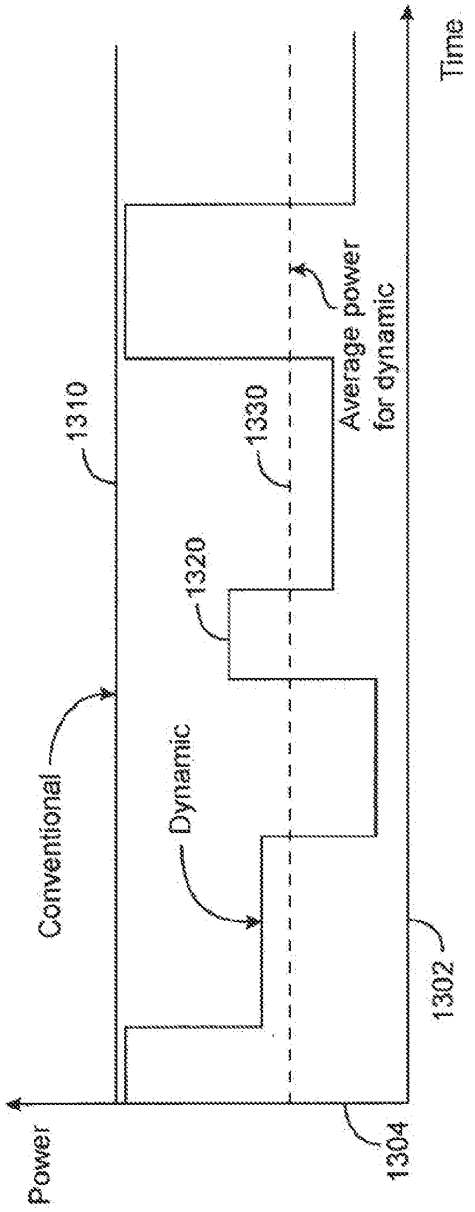

Power
Time
Conventional
Dynamic
1310
1320
1330
1302
1304
Average power
for dynamic

FIG 13

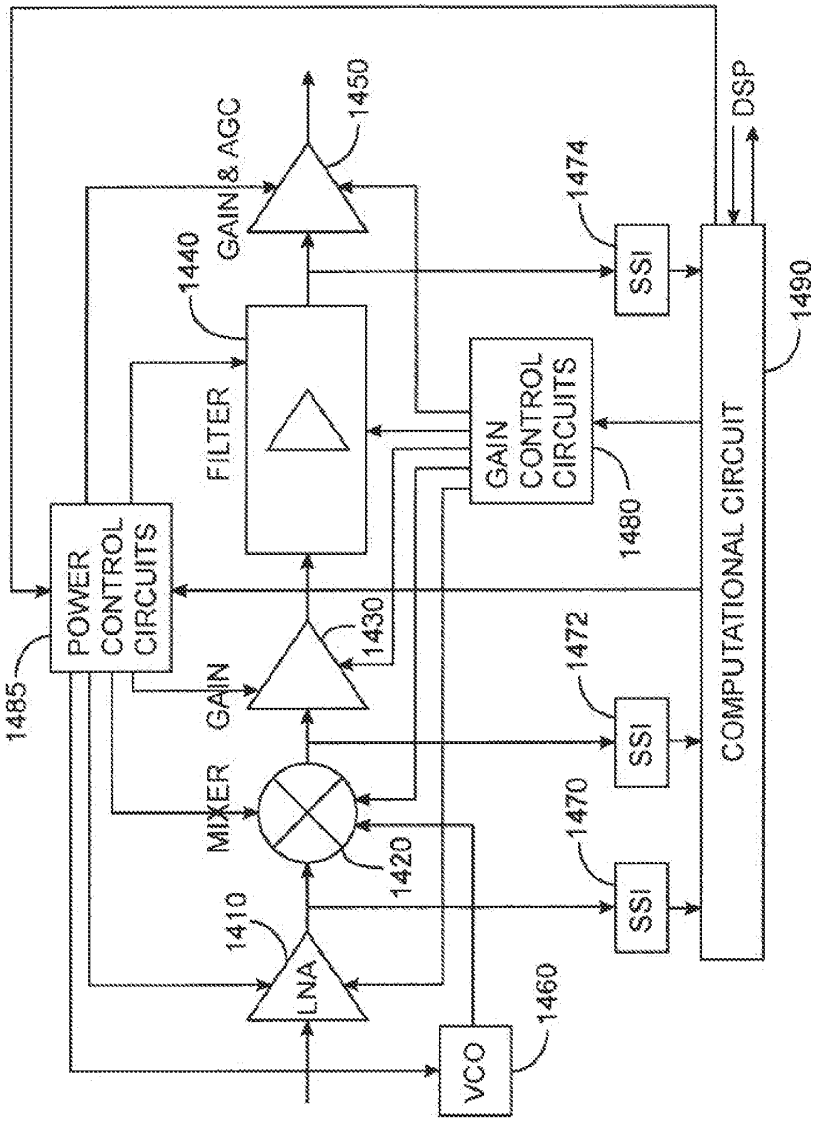

1485
POWER CONTROL CIRCUITS
1410
LNA
1420
MIXER
1430
GAIN
1440
FILTER
1450
GAIN & AGC
1460
VCO
1470
SSI
1472
SSI
1474
SSI
1480
GAIN CONTROL CIRCUITS
1490
COMPUTATIONAL CIRCUIT
DSP

FIG. 14

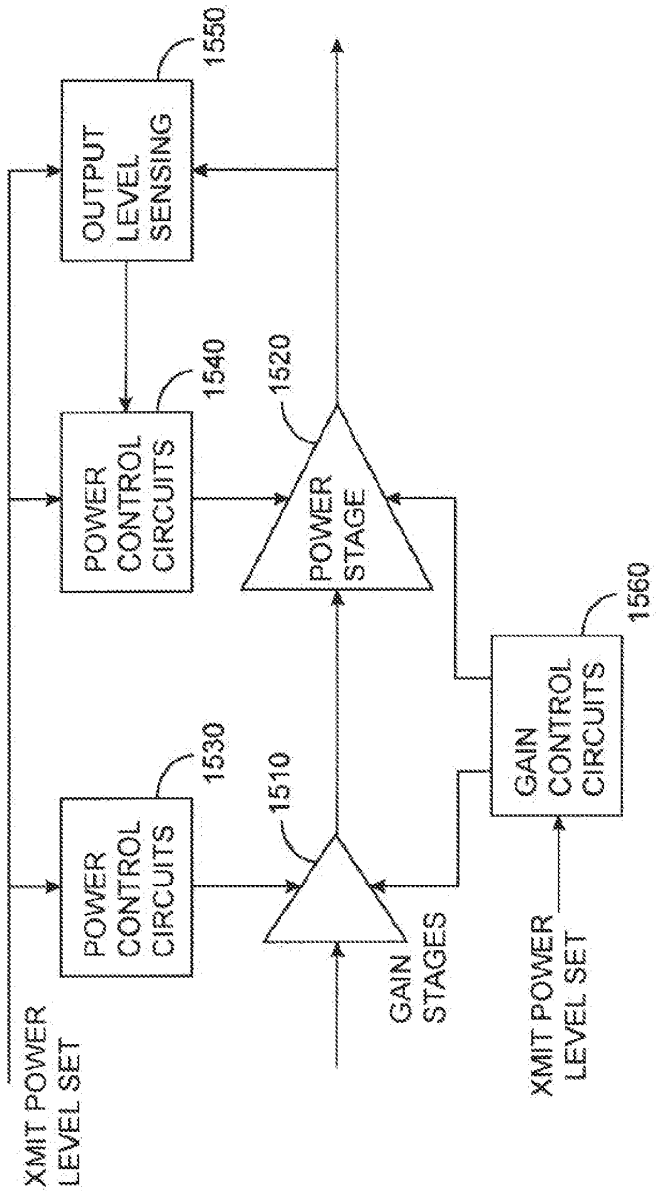

1550
OUTPUT LEVEL SENSING
1540
1520
POWER CONTROL CIRCUITS
POWER STAGE
1560
GAIN CONTROL CIRCUITS
1530
1510
POWER CONTROL CIRCUITS
GAIN STAGES
XMIT POWER LEVEL SET
XMIT POWER LEVEL SET

FIG. 15

POWER DISSIPATION REDUCTION IN WIRELESS TRANSCEIVERS

CROSS-REFERENCES TO RELATED APPLICATIONS

This application is a continuation of U.S. patent application Ser. No. 15/080,421, filed Mar. 24, 2016, which is a continuation of U.S. patent application Ser. No. 11/318,646, filed Dec. 27, 2005, which is a continuation of U.S. patent application Ser. No. 10/784,613, filed Feb. 23, 2004, which claims the benefit of U.S. provisional application No. 60/451,229, filed Mar. 1, 2003, which is incorporated by reference.

This application claims the benefit of U.S. provisional application No. 60/451,230, filed Mar. 1, 2003, which is incorporated by reference.

BACKGROUND

The present invention relates to power dissipation reduction techniques for electronic circuits, for example wireless transceiver integrated circuits.

Wireless networking is quickly becoming ubiquitous, as desktop, notebook, and handheld computers are connected to share Internet access and files. Wireless networking cards compatible with PCMCIA and compact flash form factors are popular for laptops and handhelds respectively, particularly as mobile users connect to the Internet on the road at coffee shops, hotels, and airports.

A downside of this connectivity is a corresponding drain on battery life, especially for these portable devices. The power consumed by a wireless transmitter and receiver reduces the usefulness of a device and sends a user on a hunt for an electrical outlet for recharging.

One reason why this power drain is high is that electronic circuits are typically designed to function properly under worst-case operating conditions. For a wireless transceiver, the worst case condition is when a desired signal reception strength is low, while other transceivers or nearby electronic equipment generate interfering signals and other spurious noise.

But a wireless transceiver does not always operate in these worst-case conditions. For example, a base station, router or access point may be nearby such that the received signal is strong. Also, there may be no interfering signals, or they may be relatively weak. In these situations, receiver circuit currents can be reduced below what is necessary for the worst case condition. If this is done, power dissipation is reduced, and battery life is increased.

Thus, what is needed are circuits and methods that can adapt to a better-than-worst-case condition and reduce circuit currents and therefore power dissipation accordingly.

SUMMARY

Accordingly, embodiments of the present invention provide methods and circuits for reducing power dissipation in wireless transceivers and other electronic circuits and systems. Embodiments of the present invention use bias current reduction, impedance scaling, gain, and other dynamic changes either separately or in combination to reduce power dissipation in response to better-than-worst case conditions. For example, bias currents are reduced in response to a need for reduced signal handling capability, impedances are scaled thus reducing required drive and other bias currents in response to a strong received signal, or gain is varied and

impedances are scaled in response to a low received signal in the presence of no or weak interfering signals. Alternately, currents may start low and be increased in response to worse-than-best-case conditions, or they may start at a point in between and vary up or down. These variations may be made to electronic systems generally, and are particularly suited and discussed below in the context of a wireless transceiver that may be used in networking devices, cellular telephones, and other wireless systems.

An exemplary embodiment of the present invention provides a method of receiving a signal using an integrated circuit. The integrated circuit includes a signal path having a low-noise amplifier configured to receive the signal, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer. The method itself includes determining a first signal strength at a first node in the signal path in the integrated circuit and dynamically changing an impedance of a component in the signal path based on the first signal strength.

A further exemplary embodiment of the present invention provides a method of receiving a signal using an integrated circuit. The integrated circuit includes a signal path having a low-noise amplifier configured to receive the signal, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer. The method itself includes determining a first signal strength at a first node in the signal path in the integrated circuit and dynamically changing a bias current in the signal path based on the first signal strength.

Another exemplary embodiment of the present invention provides a method of receiving a signal using an integrated circuit. The integrated circuit includes a signal path having a first circuit and a second circuit having an input coupled to an output of the first circuit. The method itself includes determining a first signal strength at a first node in the signal path in the integrated circuit. The first node is before the first circuit in the signal path. The method further includes dynamically changing a gain of the first circuit based on the first signal strength and dynamically changing an impedance of a component in the second circuit based on the first signal strength.

Still a further exemplary embodiment of the present invention provides a wireless transceiver integrated circuit including a receiver having a signal path, the signal path including a low-noise amplifier, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer, as well as a first signal strength indicator circuit coupled to the signal path and configured to determine a first signal strength. An impedance in the signal path is configured to be dynamically adjusted in response to the first signal strength.

Yet a further exemplary embodiment of the present invention provides a wireless transceiver integrated circuit. This integrated circuit includes a receiver comprising a signal path, the signal path having a low-noise amplifier, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer, as well as a first signal strength indicator circuit coupled to the signal path, and configured to determine a first signal strength. A bias current in the signal path is configured to be dynamically adjusted in response to the first signal strength.

Another exemplary embodiment of the present invention provides a wireless transceiver integrated circuit. This circuit includes a receiver comprising a signal path, the signal

path having a first circuit; and a second circuit having an input coupled to an output of the first circuit, as well as a first signal strength indicator circuit coupled to the signal path, and configured to determine a first signal strength. A gain of the first circuit is configured to be dynamically adjusted in response to the first signal strength, and an impedance in the second circuit is configured to be dynamically adjusted in response to the first signal strength.

A better understanding of the nature and advantages of the present invention may be gained with reference to the following detailed description and the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram of a wireless transceiver that may benefit by incorporation of embodiments of the present invention;

FIGS. **2**A and **2**B illustrate examples of desired and interfering signals and noise that may be received by a circuit in a wireless receiver;

FIG. **3** illustrates what can occur as a maximum signal handling capability is reduced in the worst-case signal condition;

FIG. **4** illustrates a portion of a receiver consistent with an embodiment of the present invention;

FIG. **5** illustrates the relationship between a required bias current and a given output signal for a representative circuit;

FIG. **6** is an example of how a circuit's impedances may be scaled to reduce drive currents, and depending on the circuit configuration used, to reduce associated bias currents as well;

FIG. **7** illustrates how gain may be inserted in a signal path to improve a circuit's signal to noise ratio;

FIGS. **8**A-**8**D illustrate some of the possible power saving techniques that may be used when received desired and interferer signals are all at a low power level;

FIGS. **9**A-**9**C illustrate one of the possible power saving techniques that may be used when a received desired signal is strong while all interfering signals are at a low power level;

FIGS. **10**A-**10**C illustrate one of the possible power saving techniques that may be used when received desired and interferer signals are all at a high power level;

FIGS. **11**A-**11**D illustrate one of the possible power saving techniques that may be used when a received desired signal is weak while one or more interfering signals are strong;

FIG. **12** is a summary illustrating four different input conditions and some of the appropriate power-saving changes that may be made in response to those conditions;

FIG. **13** shows how power may be saved as a function of time by employing one or more of the power saving methods consistent with embodiments of the present invention;

FIG. **14** is a block diagram of a portion of a receiver consistent with an embodiment of the present invention; and

FIG. **15** is a block diagram of a portion of a transmitter consistent with an embodiment of the present invention.

DESCRIPTION OF EXEMPLARY EMBODIMENTS

FIG. **1** is a block diagram of a wireless transceiver that may benefit by incorporation of embodiments of the present invention. This wireless transceiver may be designed to send and receive signals consistent with the IEEE 802.11a, 802.11b, 802.11g, or other signaling standard or combination of standards. This figure, as with all the included figures, is shown for illustrative purposes only and does not to limit either the possible embodiments of the present invention or the claims.

There are three main portions of this transceiver circuit, a receiver, transmitter, and syathesizer. This transceiver may be completely or partially integrated on a semiconductor chip, or it may be integrated onto multiple integrated circuits. In a specific embodiment, the circuitry bounded by dashed line **100** is integrated on a single chip coupled to one or more external components or circuits. The integrated circuit or circuits forming this wireless transceiver may incorporate various integrated circuit devices such as a bipolar, CMOS, or BiCMOS devices made using a silicon, silicon-germanium (SiGe), gallium arsenide or other III-V process, or other manufacturing process. Embodiments of the present invention may also be applicable to circuits manufactured using nanotechnology processing.

The receiver includes a signal path formed by low-noise amplifier **102**, I and Q mixers **104** and **106**, low pass filters **108** and **110**, and baseband amplifiers **114** and **116**. Other circuitry in the receiver includes received strength indicator **122**, automatic gain control circuit **166**, baseband gain control circuit **120**, tuning circuit **112**, and offset cancellation circuit **118**.

The transmitter includes input up-converter mixers **124** and **126**, summing node **176**, which may be conceptual rather than an actual circuit, transmit variable gain amplifier **128**, and power amplifier **130**.

The synthesizer includes a voltage-controlled oscillator **148**, which drives I and Q buffers **154** and **152**, prescaler **156**, reference clock buffer **142** and divider **158**, phase-frequency detector **160**, charge pump **162**, and loop filter **146**, which in a specific embodiment is formed by external components.

Signals are received on an antenna, not shown, and typically pass through an RF switch and bandpass filter before being received by the low-noise amplifier **102** on line **101**. The low noise amplifier gains the received signal and provides it to quadrature mixers **104** and **106**. I and Q mixers **104** and **106** down-convert the received signal to baseband by multiplying them with quadrature versions of the oscillator signal provided by buffers **152** and **154**. This down conversion also produces a high frequency component at a frequency that is equal to the sum of the frequencies of the received signal and the VCO. This unwanted signal is filtered by low pass filters **108** and **110**, which in turn drive baseband amplifiers **114** and **116**. The outputs of baseband amplifiers **114** and **116** are typically converted to digital signals by analog-to-digital converters at the front end of a digital signal processing block.

In the transmit mode, I and Q versions of the signal to be transmitted are provided on lines **121** and **123** to up-convert mixers **124** and **126**. These up-convert mixers multiply the I and Q portions of the transmit signal by quadrature versions of the VCO signal provided by buffers **152** and **154**. The outputs of the up-convert mixers **124** and **126** are summed, and amplified by transmit VGA **128**, which in turn drives power amplifier **130**. The output of power amplifier **130** is typically filtered, and passes through the RF switch to the antenna for transmission.

A reference clock is received and buffered by the reference buffer **142**. The VCO generates quadrature oscillatory signals that are divided by prescaler **156**. The reference clock is typically generated by a crystal or other stable periodic clock source. The phase-frequency detector **116** compares the phase or frequency (depending on whether the

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synthesizer is tracking or acquiring the correct frequency) of the divided VCO signal and the reference clock, or a divided version of the reference clock, and generates an error signal, which drives the charge pump **162**. The output signal of the charge pump **162** is filtered by the loop filter **146**, which is commonly a lead-lag filter, and which provides a tuning or correction signal to the VCO **148**.

Embodiments of the present invention may be used to reduce the power dissipation of one or more of these included circuits. For example, the power dissipation in the low-noise amplifier **102**, down-convert mixers **104** and **106**, low pass filters **108** and **110**, or baseband amplifiers **114** and **116** may be optimized. Also, power dissipation in up-convert mixers **124** **126**, variable gain amplifier **128**, and power amplifier **130** may also be optimized. Similarly, VCO **148** and prescaler **156** currents may be adjusted. Embodiments of the present invention may also be applied in other circuits which may be included in other integrated circuit receivers, transmitters, transceivers, or other electronic circuits or systems.

When a receiver is actively receiving a desired signal, each block in the signal path has at its input the desired signal as well as noise and possibly interfering signals. The desired signal is the useful, information-carrying portion of a received signal. The noise may be thermal, shot, or other noise generated on the integrated circuit, in addition to received noise generated by sources external to the chip. The noise at the input of a block may be referred to as the equivalent input noise. The interfering signal or signals, or interferers, may be generated by similar transceivers, or other electrical equipment, circuits, or systems.

FIGS. **2**A and **2**B illustrate examples of desired signals, interferers, and noise that may be received by one of the various circuits in a wireless receiver. In each of these figures, the signal strength is plotted along a Y-axis **204** or **254** as a function of frequency along an X-axis **202** or **252**. In the example of FIG. **2**A, a received desired signal **206** is large in comparison to interfering signals **208** and **210**. In these examples, two interfering signals are shown for illustrative purposes, though there may be no such signals, one such signal, or more than two such signals in the frequency range of interest. Also, while for these examples the interferers are shown as being at a higher frequency than the desired signal, there may be one or more interferers at higher or lower frequencies as the desired signal. In this specific example, the acceptable noise floor **214** is relatively high, while maximum signal handling capability Smax **212** (that is the maximum signal power that can be handled with an acceptably low distortion) needs only to be high enough to accommodate the desired signal. For this specific example, the circuit receiving this input spectrum only requires a relatively small dynamic range for proper operation, that is the range between Smax **212** and the noise floor **214** is relatively small.

Conversely, in the example shown in FIG. **2**B, the desired signal **256** is relatively weak compared to the large interferers **258** and **260**. In this example, the noise floor **264** should be relatively low so as to prevent an unacceptable level of error in the recovery the desired signal **256**. The maximum signal handling capability Smax **262** should be relatively high to accommodate the large interferers in order to avoid the creation of intermodulation products as described below. Accordingly, in this specific example, the circuit receiving this input spectrum should have a large dynamic range, particularly in comparison to the example of FIG. **2**A.

It should be noted that the noise level or noise floors shown in these and the other included figures is the noise density integrated over the bandwidth of interest. For simplicity and comparison, this level is shown as a horizontal line, and is not meant to imply noise density.

Often in wireless receivers, a circuit at different times will receive an input spectrum similar to those shown in FIGS. **2**A and **2**B. The input spectrum of FIG. **2**B is generally considered the worst-case input signal, and typical design methodology involves designing a receiver for this condition, specifically the weakest desired signal accompanied by largest interference level. Circuit impedances and currents are set such that the noise floor **264** is sufficiently low for an acceptable bit-error rate, while bias currents are set sufficiently high for the required Smax **262**.

Conversely, the input spectrum in FIG. **2**A is that of the best-case input signal, specifically, a robust desired signal accompanied by no or low-level interferers. In this case, the noise floor **214** may be allowed to rise, while the maximum signal handling capability Smax **212** may be reduced. When this is done, the receiver circuit may save significant power. For example, the circuit's impedances may be increased, thus reducing required drive currents. Similarly, bias currents may be lowered, thus reducing the maximum signal in handling capability.

The minimum power dissipation for a circuit is proportional to the required maximum signal-to-noise ratio, which is the ratio between Smax **212** or **262** and N **214** and **264**. Thus, a circuit receiving an input similar to the one shown in FIG. **2**A can dissipate less power than one receiving the input as shown in FIG. **2**B, while still achieving an acceptable bit-error rate.

FIG. **3** illustrates what can occur when the maximum signal handling capability Smax **314** is reduced in the worst-case condition, that is when a weak desired signal **306** is accompanied by large interferers **310** and **312**. Again, signal strength is plotted along a Y-axis **304** as a function of frequency along X-axis **302**. In this specific example, Smax **314** is reduced below the peak levels of the interferers **310** and **312**. Since Smax is low, the circuit cannot handle the interferers linearly. The resulting nonlinearities lead to a mixing of the interferers and the creation of intermodulation products **308** (for example, a third-order intermodulation distortion, IM3), one of which in this example occurs at the same frequency as the desired signal **306**. As can be seen, if the intermodulation products **308** become excessive, the received signal bit error rate may become excessive, and the desired signal **306** may be lost. Accordingly, while Smax may be lowered even under some unfavorable conditions in order to reduce power, care should be taken to avoid corruption of the received desired signal.

FIG. **4** illustrates a portion of a receiver consistent with an embodiment of the present invention. Included is a filter **430**. An optional gain element **420** is placed in front of the filter **430** in order to increase signal levels. Signal strength indicator circuits **440** and **450** are connected to input line **410** and output line **460**. In this specific example, the input signal spectrum on line **410** is shown as desired signal **412** and interferers **414** and **416**. The signal spectrum at the output line **460** is shown as desired signal **462** and interferers **464** and **466**. The signal strength indicators **440** and **450** do not provide information as to the relative sizes of the desired and interfering signals. Rather, a cumulative signal level is provided at their outputs. For example, the first signal strength indicator **440** outputs a level corresponding to the sum of desired signal **412** and interfering signals **414** and **416**, while the second signal strength indicator **450** provides

a signal level corresponding to the sum of desired signal **462** and interfering signals **464** and **466**. In this specific example, the gain of the gain and filter circuit combinations is shown as approximately one, while the interfering signals **414** and **416** signal levels are reduced.

A comparison of the signal levels provided by the signal strength indicators **440** and **450** indicates that much of the combined received signal on line **410** has been filtered. Accordingly, it may be deduced that large interfering signals present at the input are being filtered by the filter **430**. From this information, as will be shown in greater detail below, the bias, impedance, and gain of the gain stage **420** and filter **430** combination may be optimized to reduce power dissipation.

There are several real world situations where the received signal is better than the worst-case condition such that power can be saved. For example, large interferers may be present only part of the time, that is, on a temporary or transient basis. The interfering equipment may be some distance from the transceiver, or it may be operating in the low power mode. Also, the desired signal may be very strong as compared to the noise and interferers, for example a hub, router, or access point may be nearby.

Some transceivers consistent with embodiments of the present invention are designed to work with more than one data transfer specification or standard. In this case, when a transceiver is operating in a mode having a lower data rate, the power saving techniques described here may be employed.

FIG. **5** illustrates the relationship between a required biassal current **516** for a given output signal **514** for a representative circuit **510**. If the output signal current level is relatively low, such as the output current shown as **526**, the corresponding bias current **528** may be low. Conversely, if the output signal current level is larger as with the example **536**, the corresponding bias current level **538** should also be high. Accordingly, if a bias current is initially set high to handle large a large input signal, for example a large interferer, this current may be reduced if the input signal is smaller.

There are many ways by which these bias currents can be reduced. For example, the current may be generated by placing a voltage across a resistor by applying a bias voltage to the base of a device whose emitter is connected to ground through a resistance. In this case, the resistor may be increased by opening switches across portions of the resistance, or lowering the bias voltage applied at the base. Several ways in which this may be done will be readily understood by one skilled in the art.

FIG. **6** is an example of how a circuit's impedances may be scaled to reduce drive currents, and, depending on the circuit configuration used, associated bias currents as well. A driver **612** has a load R **614** and C **616**. The frequency response of this circuit is the same as that seen by driver **622**, which drives an impedance of 2R **624** and C/2 **626**. But the impedance of the load seen by driver **622** is double that seen by **612**, thus the output current required by the driver **622** is reduced by one-half.

As an example, the output stage of each of these drivers may be a Class A emitter follower formed by an emitter follower connected to a current source. When the outputs are driven high, the emitter of driver **622** need supply only one-half the drive current as driver **612**. In this way, an impedance can be scaled in order to decrease a circuit's required drive current.

Also, the discharge current for driver **622** is only one half that of driver **612** for a given negative-going slew rate. Thus, the current source of **622** may be reduced by the same factor of one-half as compared to driver **612**. In this example, the bias current, that is the current in the pull-down current source can be reduced. Many other examples where drive currents and possibly bias currents may be reduced will be appreciated by one skilled in the art.

FIG. **7** illustrates another degree of freedom that made be employed to reduce current levels in a transceiver. Specifically, a gain element **720** may be inserted in front of a circuit block **730** in order to improve the combined circuit's signal-to-noise ratio by a factor equal to the gain of the inserted gain block. This is particularly useful when large interferers are absent and the desired received signal is moderate or low. Specifically, gain is added to the signal while impedances are increased, which raise the noise floor. In this way, a given signal-to-noise ratio may be maintained while the power is decreased.

The gain of such an element may be varied by increasing a current in a differential pair or increasing a load resistance using switches. Many other examples where the gain of this element may be varied will be appreciated by one skilled in the art.

These variables, or degrees of freedom, specifically reducing bias currents, increasing impedances, and increasing gain may be used as in the following examples.

FIG. **8**A is a block diagram of a functional block **820** and optional gain element **810** in accordance with an embodiment of the present invention. Functional block **820**, like the functional blocks in the following diagrams, may be a filter, mixer, amplifier, or other circuit or circuits in a wireless transceiver or other electronic circuits or system. An input signal is received on line **812** by the optional gain element **814**. When the optional gain block **810** is not used, the input signal may be received directly by the function block **820**. The gain of the optional gain element **812** is controlled by a gain control signal on line **814**. The functional block receives an output signal from the optional gain element **810** and provides an output VOUT on line **822**. The lines in this and the other included figures may be one or more lines, depending on whether single-ended, differential, or other type of signaling is employed.

One or more impedances are under control of signals on impedance control lines **824**. Similarly, one or more bias currents in the function block are under control of one or more signals on bias control lines **826**. These various control lines may be logic signals, analog signals, voltage or currents lines, or other signal or bias lines. In other embodiments of the present invention, the gain control element **810** may be included in the function block **820**. Also, various embodiments may not incorporate either or both the impedance control and bias control.

FIG. **8**B is an example input that may be present on line VIN **812**. In this example, a desired signal **836** is relatively weak, as are interfering signals **837** and **838**. The initial bias and circuit configuration is such that the noise floor **833** and maximum signal handling capability Smax **831** are adjusted for worst case conditions. The circuit of FIG. **8**A, as with all the circuits described here, receives noise at its input which may be referred to as input equivalent noise or input referred noise. Additionally, the circuit of FIG. **8**A generates noise which is added to the input referred noise. Depending on the gain characteristics of the circuitry, the output noise at various frequencies may be greater than, equal to, or less than the input referred noise. For simplicity, the noise floor and maximum signal handling capability Smax, in this and the other figures, are shown as straight lines, though the noise and Smax are typically curved as a function of frequency.

That the input spectrum is as shown in FIG. **8**B can be determined, for example, by low signal strength indications on line VIN **812** and VOUT **822**. That is, a low level signal strength indication on line VIN **812** indicates that no portion of the input signal is particularly large.

For this exemplary input, there are at least two methods by which the power dissipation for this circuitry may be reduced. Depending on the exact circuits and structures used, one of these methods may be preferred.

In FIG. **8**C, the bias current is decreased, thereby lowering the maximum signal handling capability **841** as compared to **831**, closer to the desired and interfering signal levels. Again, the bias currents in the function block **820** may be reduced by switching impedances that appear across a voltage thereby changing a resulting bias current, by reducing a voltage at the gate of a MOS or base of a bipolar transistor, or by other methods.

In FIG. **8**D, a second method of reducing power dissipation in the function block **820** is employed. Specifically, Smax **851** is held constant as compared Smax **831**. The desired and interfering signals are amplified such that they are closer to the available signaling handling capability **851**. Also, the noise floor **853** is raised as compared to noise floor **833** in FIG. **8**B. Specifically, the noise contributed by the function block **820** is increased, such that the noise at its output is increased to noise floor **853**. This is done by increasing one or more impedance in function block **810**, such that drive currents inside that block are reduced. Depending on the exact configuration, this may also allow some biasing currents to be reduced, while maintaining the maximum signal handling capability **851** at a sufficient level. Alternately, these two methods of reducing power dissipation in function block **820** may be done in combination.

The included examples are explained for the exemplary situation where biasing and other parameters are set for worst-case conditions, and then changed to save power when it is discovered that the conditions are better-than-worst case. Alternately, the bias currents and other parameters may be set for maximum power savings, or an intermediate point, and the power can be adjusted from there.

FIG. **9**A illustrates a block diagram including an optional gain element **910** and function block **920**. Again, an input signal is received on line **912** by optional gain element **910** which in turn drives function block **920**. The function block provides an output VOUT on line **922**, and receives impedance and bias control signals on lines **924** and **926**.

FIG. **9**B shows the spectrum for what may be considered a best-case received signal. Specifically, the desired signal **936** is strong, while the interfering signals **937** and **938** are relatively weak. This may be determined, for example, by detecting a large signal level at the input line VIN **812** and a large signal level after a filter, since these readings would indicate that a large signal is received, but that it is at the desired signal frequency.

The maximum signaling capability **931** and noise floor **933** are shown as being set for the worst case conditions. In this case, the noise floor **933** is lower than the maximum allowed for proper signal reception. Accordingly, one or more impedance in the function block **920** may be increased, such that the noise floor **943** rises as shown in FIG. **9**C. In this way one or more the driving currents in the function block **920** may be reduced. Similarly, since the drive current is reduced, one or more bias current may also be reduced, depending on the exact circuit configuration.

FIG. **10**A illustrates a block diagram showing an optional gain element **1010** driving a function block **1020**. An input signal is received by the gain element **1010** on hue **1012**, and an output is provided by function block **1020** on line VOUT **1022**. One or more gain control signals present on lines **1014** control the gain of gain control element **1010**, while one or more impedance and bias control signals are received by the function block **1020** on line to **1024** and **1026**.

FIG. **10**B illustrates a received signal that may be received on line VIN **1012**. In this example, the desired signal **1036** and interferers **1037** and **1038** are each relatively large. This may be determined, for example, by detecting a large signal level at the input line VIN **812** and a smaller signal level after a filter, since these readings would indicate that a large signal is received, but that interferers are being reduced.

As before, in this example, the noise floor **1033** and maximum signal handling capability **1031** are initially set for the worst case conditions. Since the desired signal is relatively large in this case, the noise floor may be allowed to rise, a shown by noise floor **1043** in FIG. **10**C. Since the desired signal **1046** and interferers **1047** are large, the maximum signal handling capability Smax **1041** remains constant. Again, the noise floor is increased by increasing impedances in the function block **1020**. This reduces the required drive current, and may also allow for a reduction in bias currents.

FIG. **11**A illustrates a block diagram including an optional gain element **1110** and function block **1120** in accordance with an embodiment of the present convention. An input signal is received on line **1112** by the optional gain control element **1110**, while an output signal is provided by the function block **1120** on line VOUT **1122**. Gain, impedance, and bias control signals are received on lines **1114**, **1124**, and **1126**.

FIG. **11**B is an exemplary input signal that may be received by the gain control element **1110** on line VIN **1112**. In this specific example, the desired signal **1136** is relatively low or weak while the interfering signals **1137** and **1138** are large. This may be determined, for example, by detecting a large signal level at the input line VIN **812** and a much smaller signal level after a filter, since these readings would indicate that a large signal is received and that large interferers are being reduced such that the resulting signal, the desired signal, is relatively weak.

Again, the maximum signal handling capability **1131** and noise floor **1133** are initially set for worst case conditions. If the desired signal is sufficiently low, while the interferers are sufficiently high, power savings may not be achievable over the worst case settings, since this is in fact the worst case condition. But, if the desired signal is somewhat larger than the worst case condition, then power may be saved in at least two different ways.

For example, FIG. **11**C shows the maximum signal handling capability **1141** being lowered. In this case, the interfering signals **1147** in **1148** began to clip and distort, thereby creating intermodulation products **1145**, which distort the desired signal **1146**. So long as care is taken to not corrupt the desired signal **1146** beyond an acceptable limit, typically measured by a bit-error rate, power may be reduced in this way.

Similarly, in FIG. **11**D, the noise floor **1153** is raised somewhat, thereby saving power. Again, this may be done so long as the noise floor is not sufficiently high that the system bit-error rate becomes unacceptable.

FIG. **12** is a summary of the above four examples. The received signal strengths are shown in column **1210**, while appropriate power saving responses are listed in column **1220**. Specifically, in row **1230**, the desired signal and interferer signal strengths are both weak or small. In this case, proper responses include decreasing Smax, or increas-

ing one or more circuit impedances while increasing the circuit gain. Depending on the exact circuit configuration, one of these options may be preferred over the other. Alternately, they may be done in combination, or done in combination with other power saving techniques. Also, in some specific embodiments, when both desired signal and interferer signal strengths are small, the gain may need to be increased while the impedance is maintained or not increased in order to keep the noise floor low.

In row **1240**, the desired signal strength is strong or large, while the interfering signals are small. In this case, an appropriate response is to increase one or more of the circuit impedances. Again, depending on the exact circuit in question, one or more of the bias currents may also be reduced.

In row **1250**, both the desired signals and interfering signal strengths are large. Again, in this case an appropriate response is to increase one or more of the circuit impedances.

In row **1260**, the received desired signal strength is weak or small, while the interfering signals are large. Since this is the worst case situation for which the circuit is designed, substantial power savings are difficult to achieve. However, again, if the received signal is above a minimum level necessary for proper operation, some distortion of the interferers or raising of the noise floor may be acceptable.

It should be noted that not all possible signal conditions are listed here. For example, either the signal or interferer may be of a relatively medium strength, or the interferer may be absent. Also, these terms are for exemplary purposes and are not meant to convey specific signal conditions, but rather are only qualitative. The proper response to a specific condition depends on the embodiment of the present invention, the particular circuit topology, the requirements of the signaling standard used, as well as other constraints.

FIG. **13** is an example shown how power may be saved as a function of time by employing one or more of these methods consistent with embodiments of the present invention. Power is plotted along a Y-axis **1304** as a function of time along X-axis **1302**. Conventional worst case design would fix power dissipation at line **1310**. As can be seen, dynamic power dissipation **1320** under the control of variable gains, impedances, biasing, or combination thereof, allows for a lower average power **1330** as compared to the power dissipated **1310** by the conventional design.

FIG. **14** is a block diagram of a portion of a receiver consistent with an embodiment of the present invention. Included are low-noise amplifier **1410**, mixer **1420**, gain stage **1430**, filter **1440**, AGC amplifier **1450**, and VCO **1460**. Signal strength detection is done at the output of the low-noise amplifier by signal strength indicator **1470**, at the output of the mixer by signal strength indicator **1472**, and at the output of the filter by signal strength indicator **1474**. The outputs of the signal strength indicator circuits are received by the computational circuit **1470**, which in turn controls gain and power control circuits **1480** and **1485**. Power and gain control circuits **1480** and **1485** control the gain, biasing, and impedance levels of the circuits in the receiver signal path. Also, the gain and power control circuits may control the same parameters in the VCO **1460**. This figure is greatly simplified for purposes of explanation. For example, the quadrature nature of the mixers and following circuits are not shown. Also, power-down and start-up circuits are not included.

The current level in the low-noise amplifier determines a multitude of parameters including voltage gain, linearity, input impedance matching, and noise figure. When conditions are better than worst-case, some of these parameters may be relaxed while maintaining an acceptable bit-error rate, thus saving power.

The bias current in the mixers effect that block's noise figure and linearity. Care is taken in reducing power in this block so as not to increase nonlinearities, particularly the third-order nonlinearity as measured by IP3, the third-order intercept point, beyond an acceptable limit.

A key parameter of the VCO is phase noise, an increase in which increases the sidebands on either side of the oscillation signal. During transmission, the phase noise should be kept low to avoid interference with adjacent channels and for preserving modulation information.

During reception however, if the conditions are better than worst case, the phase noise requirement for the VCO is relaxed, and power can be saved consistent with embodiments of the present invention. The achievable phase noise power spectral density is approximately inversely proportional to the bias current used. Thus, when low phase noise is not required during reception, bias current in the VCO can be reduced.

Most of the power savings in a transceiver in accordance with embodiments of the present invention is achieved in the receiver portion. Additional power may be saved in the transmitter section.

FIG. **15** is a block diagram of a transmitter portion consistent with an embodiment of the present invention. Included is a signal path formed by gain stage **1510** and power amplifier **1520**. The output power level is sensed by output level sensing circuit **1550**, which in turn adjusts the biasing of the power amplifier **1520** through the power control circuit **1540**. Additionally, a transmitter level control signal is received by power control circuits **1530** and **1540**, which in turn control the biasing of gain stage **1510** and power amplifier **1520**. Gain control circuit **1560** also adjusts the gain of gain stage **1510** and power amplifier **1520**. Additional circuitry that varies impedances in each of these circuits may also be included.

Since the gain, impedance and biasing of these blocks are being dynamically varied, care must be taken to not negatively affect the signal being processed. For example, specific embodiments of the present invention perform some or all of these variations during preamble. Also, as changes occur, the circuits in some embodiments are limited such that they may only adapt to an improvement in conditions after frames are completed. If conditions worsen, the circuits may be allowed to change in order to save the data. Alternately, a system may be manually calibrated, for example at set up, and when the network configuration is changed.

The above description of specific embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form described, and many modifications and variations are possible in light of the teaching above. The embodiments were chosen and described in order to best explain the principles of the invention and its practical applications to thereby enable others skilled in the art to best utilize the invention in various embodiments and with various modifications as are suited to the particular use contemplated.

What is claimed is:

1. A method of reducing the power consumption of a receiver of a battery operated transceiver having a plurality of circuits, wherein the plurality of circuits comprise a receiver signal path comprising at least an amplifier, a mixer and a filter, wherein the plurality of circuits are designed to

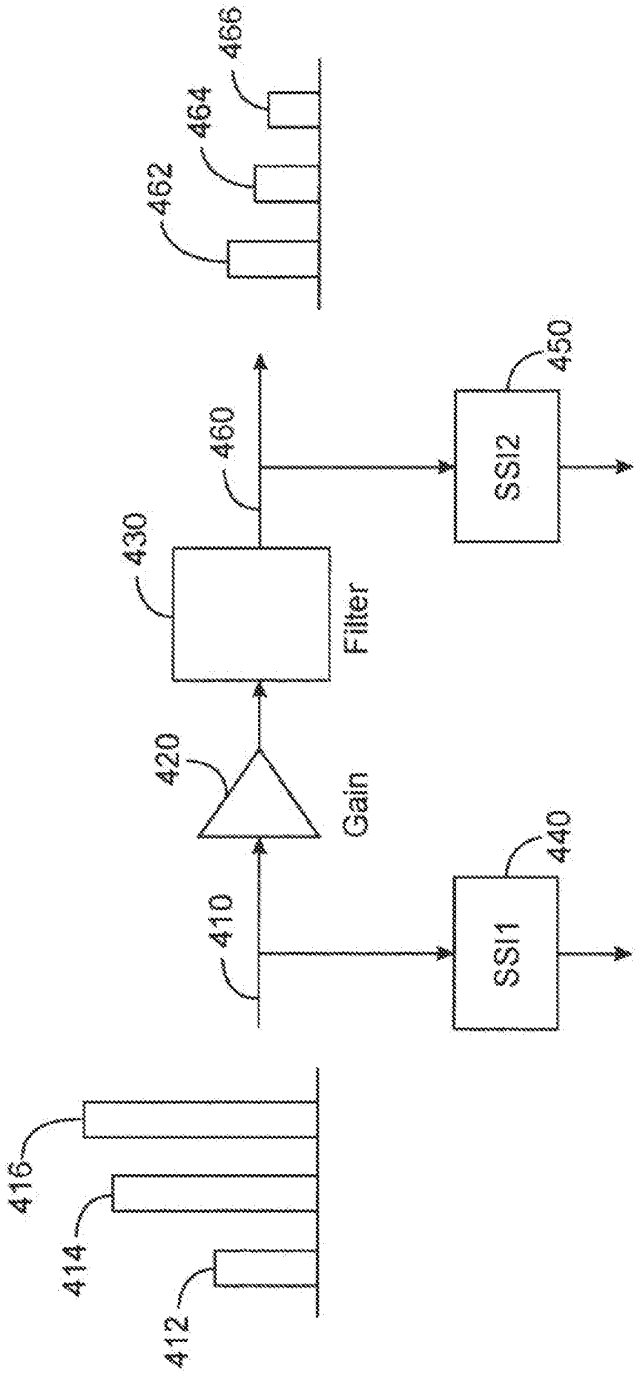

466
464
462
460
450
SSI2
430
Filter
420
Gain
410
440
SSI1
416
414
412

FIG. 4

function between a worst-case operating condition and a best case operating condition, wherein the worst-case operating condition is when a desired signal strength is low and an interferer signal strength is high and the receiver operates with a maximum power dissipation and the best-case operating condition is when the desired signal strength is high and the interferer signal strength is low and the receiver operates with a minimum power dissipation, the method comprising:

receiving a signal comprising a desired signal and an interferer signal;

determining a strength of the desired signal;

determining a strength of the interferer signal;

comparing the strength of the desired signal to the strength of the interfere signal; and

dynamically adjusting at least one of an impedance, a bias or a gain of at least one of the amplifier, filter or mixer in the receiver signal path, responsive to the comparing.

2. The method of claim 1, wherein when the strength of the interferer signal decreases over time, and the strength of the desired signal is low, dynamically decreasing the bias of at least one of the plurality of circuits in the receiver signal path.

3. The method of claim 1, wherein when the strength of the interferer signal is low, and the strength of the desired signal decreases over time, dynamically increasing a gain of at least one of a plurality of circuits in the receiver signal path and dynamically increasing the impedance of at least one of the plurality of circuits in the receiver signal path.

4. The method of claim 1 wherein when the strength of the interferer signal is low and the strength of the desired signal increases over time, dynamically increasing the impedance of one or more of the plurality of circuits in the receiver signal path.

5. The method of claim 1, wherein when the interferer signal is weak and the desired signal is low and the strength of the desired signal increases over time, dynamically decreasing the bias of one or more of the plurality of circuits in the receiver signal path.

6. A method for reducing power consumption in a receiver in a battery operated mobile device, wherein the receiver comprises a plurality of circuits, and wherein the plurality of circuits comprise a signal path including at least an amplifier, a mixer and a filter, the method comprising:

receiving a wireless signal comprising a desired signal and an interferer signal at the receiver;

determining a strength of the desired signal;

determining a strength of the interferer signal;

comparing the strength of the desired signal to the strength of the interferer signal; and

when the strength of the interferer signal is low and the relative strength of the desired signal is greater than the strength of the interferer signal, dynamically increasing an impedance of at least one of the amplifier, filter or mixer in the signal path of the receiver, thereby reducing power dissipation in the receiver.

7. A method for power dissipation control in a receiver of a wireless transceiver of a battery-powered portable wireless device, the receiver having a signal path comprising a plurality of circuits including at least an amplifier, a filter, and a mixer, wherein the receiver is configured to receive a wireless signal having a desired signal and an interferer signal, wherein the plurality of circuits are designed to function between a worst-case condition when a strength of the desired signal is low and a strength of the interferer signal is high, and a best-case condition when the strength of the desired signal is high and the strength of the interferer signal is low, the method comprising:

receiving the wireless signal having the desired signal and the interferer signal by the receiver;

determining the strength of the desired signal;

determining the strength of the interferer signal;

comparing the strength of the desired signal relative to the strength of the interferer signal; and

based on the comparison, when the plurality of circuits are functioning at better than the worst-case condition, dynamically adjusting one or more of an impedance, a bias or a gain of one or more of the plurality of circuits in the signal path, thereby controlling power dissipation.

8. The method of claim 7, wherein when the strength of the interferer signal is low and the relative strength of the desired signal with respect to the interferer signal increases, dynamically increasing the impedance of one or more of the plurality of circuits in the signal path to reduce the power dissipation and thereby save power.

9. The method of claim 7, wherein when the strength of the desired signal is low but the relative strength of the desired signal with respect to the interferer signal is better than the worst-case condition and the interferer signal reduces in strength, dynamically reducing the bias of one or more of the plurality of circuits in the signal path, thereby reducing power dissipation and saving power.

10. The method of claim 9, wherein reducing power dissipation reduces a power drain from a battery in the battery-powered portable wireless device.

11. A method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, the receiver having a signal path comprising a plurality of circuits including at least an amplifier, a filter, and a mixer, the plurality of circuits designed to function under at least a worst case condition when a strength of a received desired signal is low and a strength of a received interferer signal is high, the method comprising:

receiving a wireless signal having a desired signal and an interferer signal by the receiver;

determining a strength of the desired signal;

determining a strength of the interferer signal;

comparing the strength of the desired signal relative to the strength of the interferer signal;

based on the comparing, determining a functioning condition of the plurality of circuits; and

when the plurality of circuits are determined to function at a better than the worst case condition in which the strength of the interferer signal is low and the strength of the desired signal is low, causing a bias current of one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be dynamically decreased relative to the worst-case condition, thereby saving power.

12. A method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, the receiver configured to function under at least a worst case condition when a received desired signal strength is low and a received interferer signal strength is high, the receiver having a signal path comprising at least an amplifier, a filter, and a mixer, the method comprising:

receiving a wireless signal having a desired signal and an interferer signal by the receiver;

determining a strength of the desired signal;

determining a strength of the interferer signal;

comparing the strength of the desired signal relative to the strength of the interferer signal;

based on the comparing, determining a functioning condition of the plurality of circuits; and

when the plurality of circuits are determined to function at a better than the worst case condition in which the strength of the interferer signal is low and the strength of the desired signal is high, causing an impedance of one or more of amplifier, filter or the mixer in the receiver signal path of the wireless transceiver to be increased relative to the worst-case condition, thereby saving power.

13. A method for power dissipation control in a receiver of a wireless transceiver of a battery powered portable wireless device, the receiver having a signal path comprising a plurality of circuits including at least an amplifier, a filter, and a mixer, the method comprising:

receiving a wireless signal having a desired signal and an interferer signal by the receiver;

determining the strength of the desired signal;

determining the strength of the interferer signal;

comparing the strength of the desired signal relative to the strength of the interferer signal; and

when the interferer signal is high and the desired signal is low, causing a bias current of one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be dynamically increased, controlling the power dissipation of the receiver.

14. A method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device based on its operating signal conditions, wherein the receiver has a signal path comprising a plurality of circuits including at least an amplifier, a filter, and a mixer, the plurality of circuits designed to function under operating signal conditions that vary based on relative signal strengths of an interferer signal and a desired signal, wherein the operating signal conditions vary between a worst-case operating condition and a best-case operating condition, wherein the worst-case operating condition occurs when a desired signal strength is low and an interferer signal is high and the receiver operates with a maximum power dissipation, wherein the best-case operating condition occurs when the desired signal is high and the interferer signal strength is low and the receiver operates with a minimum power dissipation, the method comprising:

receiving a wireless signal having a desired signal and an interferer signal by the receiver;

determining the strength of the desired signal;

determining the strength of the interferer signal;

comparing the strength of the desired signal relative to the strength of the interferer signal strength;

based on the comparing, when the plurality of circuits are determined to be functioning at better than the worst-case operating signal condition, dynamically adjusting at least one of an impedance, a bias current or a gain of one or more of the amplifier, filter or mixer in the signal path of the receiver, thereby reducing power consumption to save power.

15. The method of claim **14**, wherein when the desired signal strength is low and the receiver is operating at better than the worst-case operating signal condition by having the interferer strength lower than that in the worst case operating signal condition, dynamically reducing the bias of one or more of the plurality of circuits in the signal path of the receiver, thereby reducing power dissipation and saving power; and

wherein when the interferer signal strength is high and the receiver is operating at better than the worst-case operating signal condition by having the desired signal higher than that in the worst case operating signal condition, dynamically increasing the impedance of one or more of the plurality of circuits in the signal path of the receiver, thereby reducing power dissipation and saving power.

16. A method for power dissipation optimization in a receiver of a wireless transceiver of a battery powered portable wireless device, the receiver having a signal path comprising a plurality of circuits including at least an amplifier, a filter, and a mixer, wherein the plurality of circuits are designed to function between a worst-case operating condition and a best case operating condition, wherein the worst-case operating condition is when a desired signal strength is low and an interferer signal strength is high and the receiver operates with a maximum power dissipation and the best-case operating condition is when the desired signal strength is high and the interferer signal strength is low and the receiver operates with a minimum power dissipation, the method comprising:

receiving a wireless signal having a desired signal and an interferer signal by the receiver;

determining a strength of the desired signal;

determining a strength of the interferer signal;

comparing the strength of the desired signal relative to the strength of the interferer signal; and

based on the comparing, when the plurality of circuits are determined to be functioning at better than the worst-case operating condition, dynamically adjusting at least one of an impedance, a bias current or a gain of one or more of the amplifier, filter or mixer in the signal path of the receiver to optimize power dissipation and save power.

17. The method of claim **16**, wherein when the desired signal strength is low and the operating signal condition of the receiver is better than the worst-case operating signal condition and the interferer signal strength is increasing, dynamically increasing a bias current of at least one of the plurality of circuits in the receiver signal path of the wireless transceiver, optimizing the power dissipation;

wherein when the desired signal strength is low and the operating signal condition of the receiver is better than the worst-case operating condition and the interferer signal strength reduces over time, dynamically decreasing a bias current of at least one of the plurality of circuits in the receiver signal path of the wireless transceiver, optimizing the power dissipation, and

wherein optimizing the power dissipation under better than the worst-case operating signal condition saves power with respect to the maximum power dissipation of the worst-case operating signal condition.

18. A method for controlling power dissipation in a receiver of a wireless transceiver of a battery powered portable wireless device, the receiver having a signal path comprising a plurality of circuits including at least an amplifier, a filter, and a mixer, wherein the plurality of circuits are designed to function between a worst-case operating condition and a best case operating condition, wherein the worst-case operating condition is when a desired signal strength is low and an interferer signal strength is high and the receiver operates with a maximum power dissipation and the best-case operating condition is when the desired signal strength is high and the interferer signal strength is low and the receiver operates with a minimum power dissipation, the method comprising:

receiving a wireless signal having a desired signal strength and an interferer signal by the receiver;

determining a strength of the desired signal;

determining a strength of the interferer signal;

comparing the strength of the desired signal relative to the strength of the interferer signal; and

wherein when the strength of the interferer signal is low and when the strength of the received desired signal is higher than the desired signal of the worst-case operating signal condition, dynamically adjusting an impedance of at least one of the plurality of circuits in the signal path to reduce power dissipation.

19. A method of power dissipation optimization in a receiver of a wireless transceiver of a wireless communication device based on its operating signal conditions, wherein the transceiver has a signal path comprising a plurality of circuits designed to function under operating signal conditions that vary based on relative signal strengths of an interferer signal and a desired signal in a received wireless signal, wherein operating conditions vary between a worst-case operating signal condition, wherein the receiver operates with a maximum power dissipation when a desired signal strength is low and an interferer signal strength is high and a best-case operating signal condition, wherein the receiver operates with minimum power dissipation when the desired signal strength is high and the interferer signal strength is low, the method comprising:

receiving the wireless signal having the desired signal and the interferer signal by the receiver;

determining the desired signal strength;

determining the interferer signal strength;

comparing the desired signal strength to the interferer signal strength to determine an operating signal condition of the receiver;

based on the comparing, when the receiver operating signal condition is better than the worst case operating signal condition, dynamically adjusting one or more of an impedance, a bias, or a gain of one or more of the plurality of circuits in the receiver signal path, thereby optimizing power consumption to save power.

20. The method of claim 19, wherein power saving occurs when the desired signal strength is low and the operating signal condition is better than the worst-case operating signal condition, by dynamically reducing the bias current of one or more of the plurality of circuits in the signal path of the receiver, thereby reducing power dissipation.

21. The method of claim 20, wherein power saving occurs when the operating signal condition improves when the strength of the interferer signal decreases over time, and the bias current is reduced by dynamically adjusting the bias current of one or more of the plurality of circuits in the signal path of the receiver.

22. A method of power dissipation optimization in a receiver of a wireless transceiver of a wireless communication device based on its operating signal conditions, wherein the transceiver has a signal path comprising a plurality of circuits designed to function under operating signal conditions that vary based on relative signal strengths of an interferer signal and a desired signal in a received wireless signal received, wherein the operating signal conditions vary between a worst-case operating signal condition and a best-case operating signal condition, wherein in the worst-case operating signal condition the receiver operates with a maximum power dissipation when a desired signal strength is low and an interferer signal strength is high, and wherein in the best-case operating signal condition the receiver operates with minimum power dissipation when the desired signal strength is high and the interferer signal strength is low, the method comprising:

receiving the wireless signal having the desired signal and the interferer signal by the receiver;

determining the desired signal strength;

determining the interferer signal strength;

comparing the desired signal strength to the interferer signal strength;

determining an operating signal condition of the receiver between the best and worst-case operating signal conditions based on the comparing;

when the interferer signal strength is high and the operating signal condition is better than the worst-case operating signal condition, dynamically increasing an impedance of one or more of the plurality of circuits in the signal path of the receiver, thereby reducing power dissipation.

23. The method of claim 22, wherein when the desired signal strength increases over time resulting in an improvement in the operating condition, dynamically adjusting the impedance of one or more of the plurality of circuits in the signal path of the receiver results in power saving.

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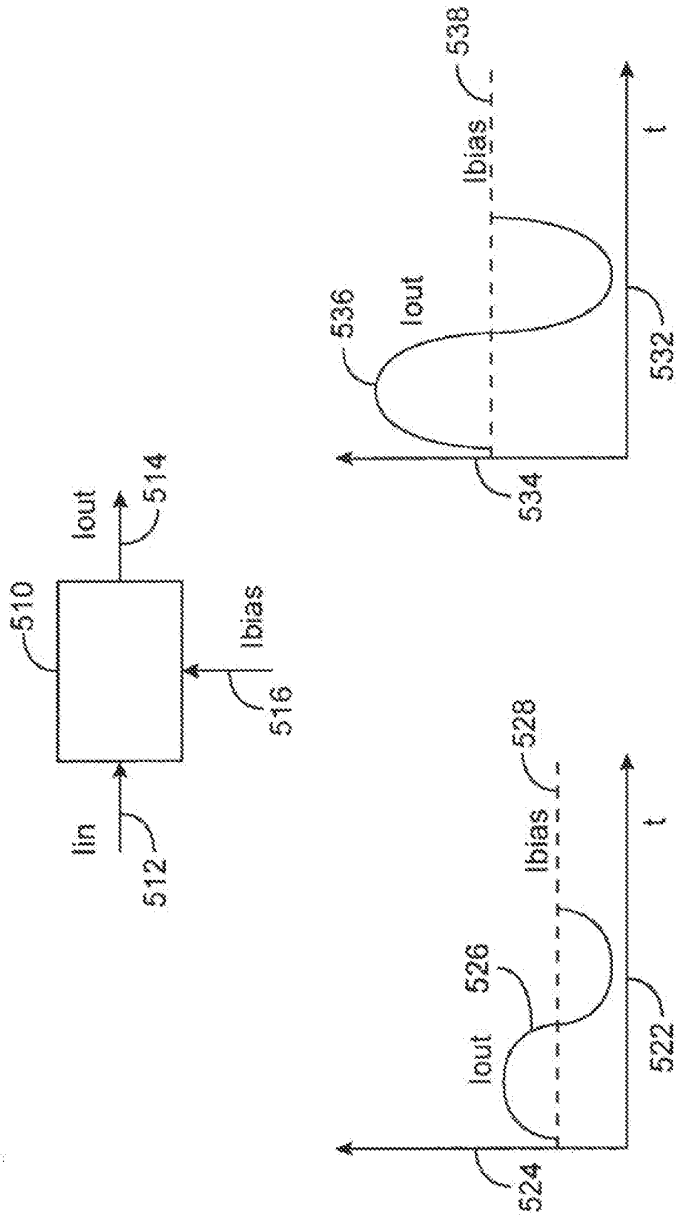

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FIG. 5