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(12) **United States Patent**
Tsividis

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(45) **Date of Patent:** ***Jan. 24, 2023**

(54) **POWER DISSIPATION REDUCTION IN WIRELESS TRANSCEIVERS**

(56) **References Cited**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

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(Continued)

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(63) Continuation of application No. 16/714,629, filed on Dec. 13, 2019, now Pat. No. 11,129,097, which is a (Continued)

(57) **ABSTRACT**

Methods and circuits for reducing power dissipation in wireless transceivers and other electronic circuits and systems. Embodiments of the present invention use bias current reduction, impedance scaling, and gain changes either separately or in combination to reduce power dissipation. For example, bias currents are reduced in response to a need for reduced signal handling capability, impedances are scaled thus reducing required drive and other bias currents in response to a strong received signal, or gain is increased and impedances are scaled in response to a low received signal in the presence of no or weak interfering signals.

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H04W 52/02
H04B 1/38
H04B 1/10

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(2006.01)

(52) **U.S. Cl.**

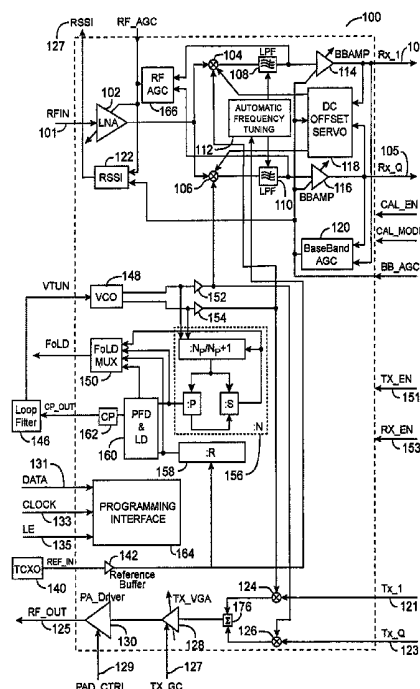
CPC **H04W 52/0209** (2013.01); **H04B 1/109** (2013.01); **Y02D 30/70** (2020.08)

(58) **Field of Classification Search**

CPC H04W 52/02; H04W 52/0209; H04W 52/0225; H04W 52/0229; H04W 52/0238;

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20 Claims, 15 Drawing Sheets



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continuation of application No. 15/824,841, filed on Nov. 28, 2017, now Pat. No. 10,524,202, which is a continuation of application No. 15/080,421, filed on Mar. 24, 2016, now Pat. No. 9,838,962, which is a continuation of application No. 11/318,646, filed on Dec. 27, 2005, now Pat. No. 9,331,728, which is a continuation of application No. 10/784,613, filed on Feb. 23, 2004, now Pat. No. 7,010,330.

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(58) **Field of Classification Search**

CPC H04W 52/0245; H04W 52/0261; H04W 52/0274; H04W 52/082; H04W 52/52; H04W 52/241; H04W 52/243; H04W 52/245; H04W 72/082; H04W 72/085; H04B 1/04; H04B 1/10; H04B 1/16; H04B 1/109; H04B 1/1036; H04B 1/7097; H04B 1/715; H04B 10/40; H04B 10/60; H04B 17/309; H04B 17/318; H04B 17/336; H04B 17/345; H03F 1/56; H03F 2200/27; H03F 2200/78; H03F 2200/378; H03F 2200/451; H03F 2200/294

See application file for complete search history.

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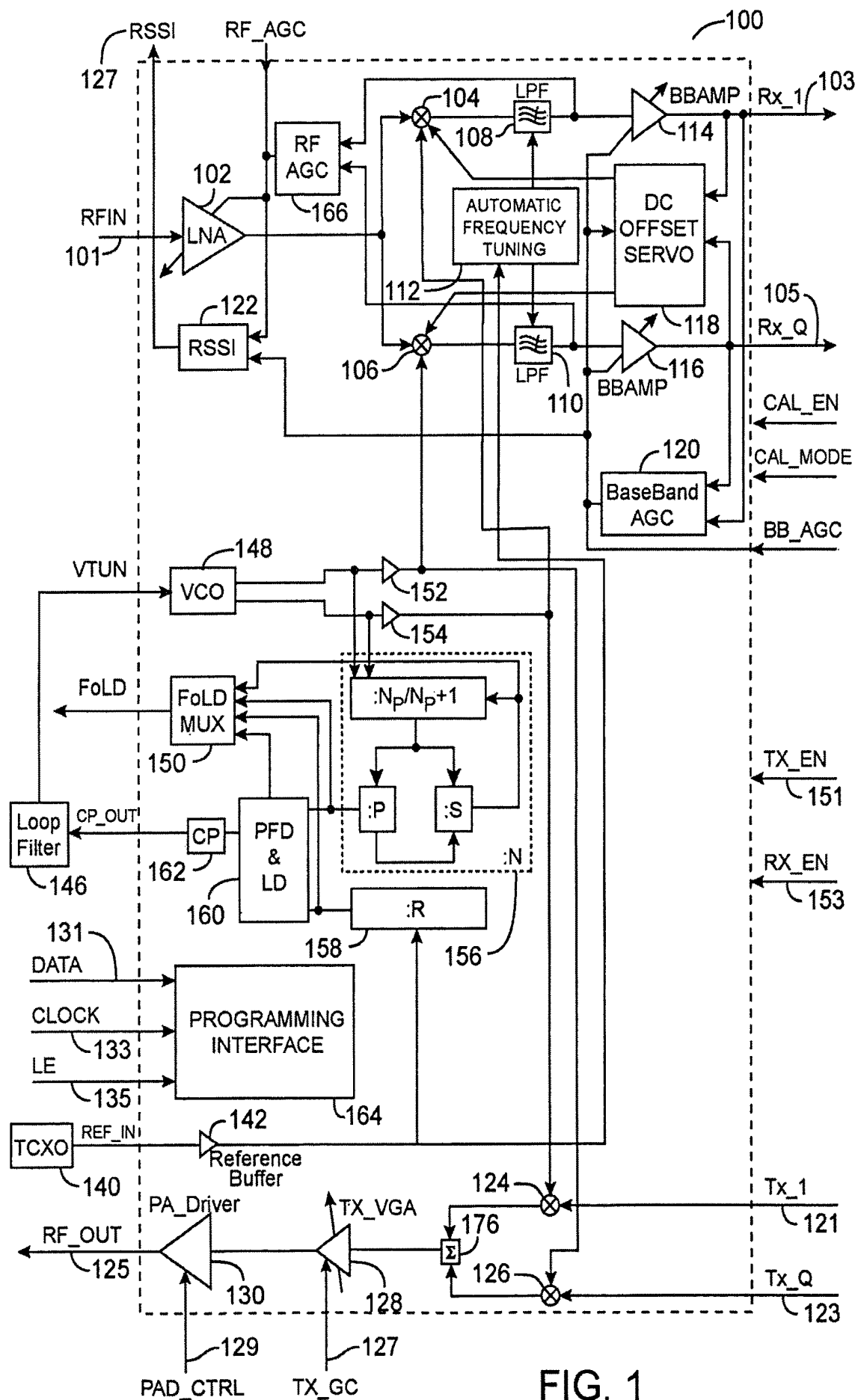


FIG. 1

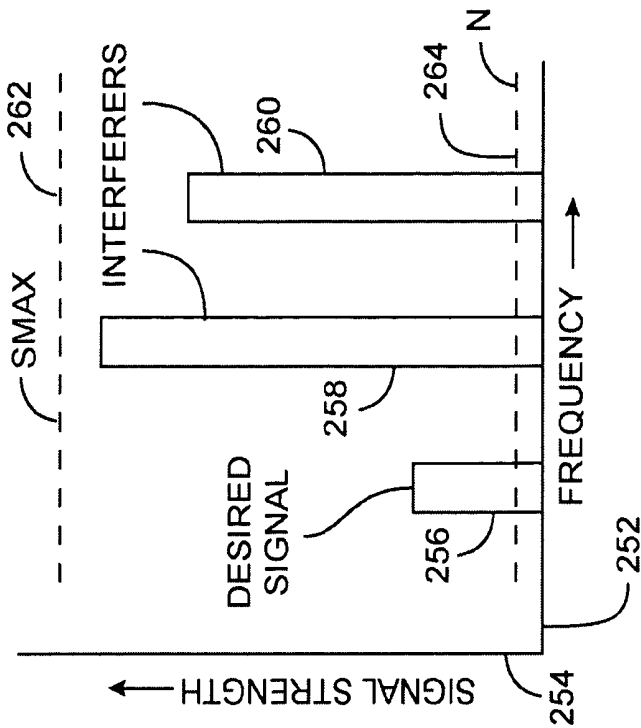


FIG. 2A

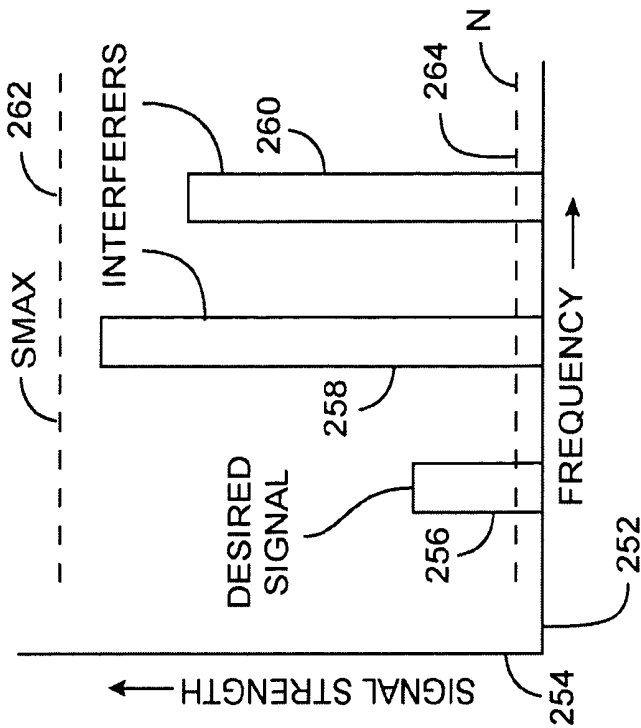


FIG. 2B

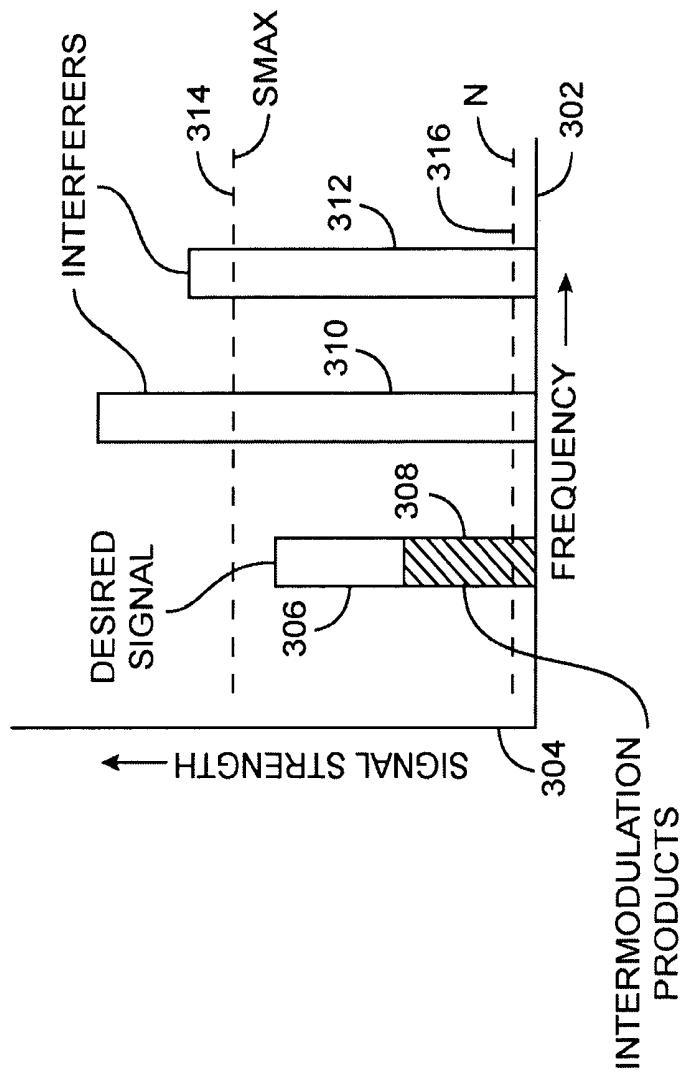


FIG. 3

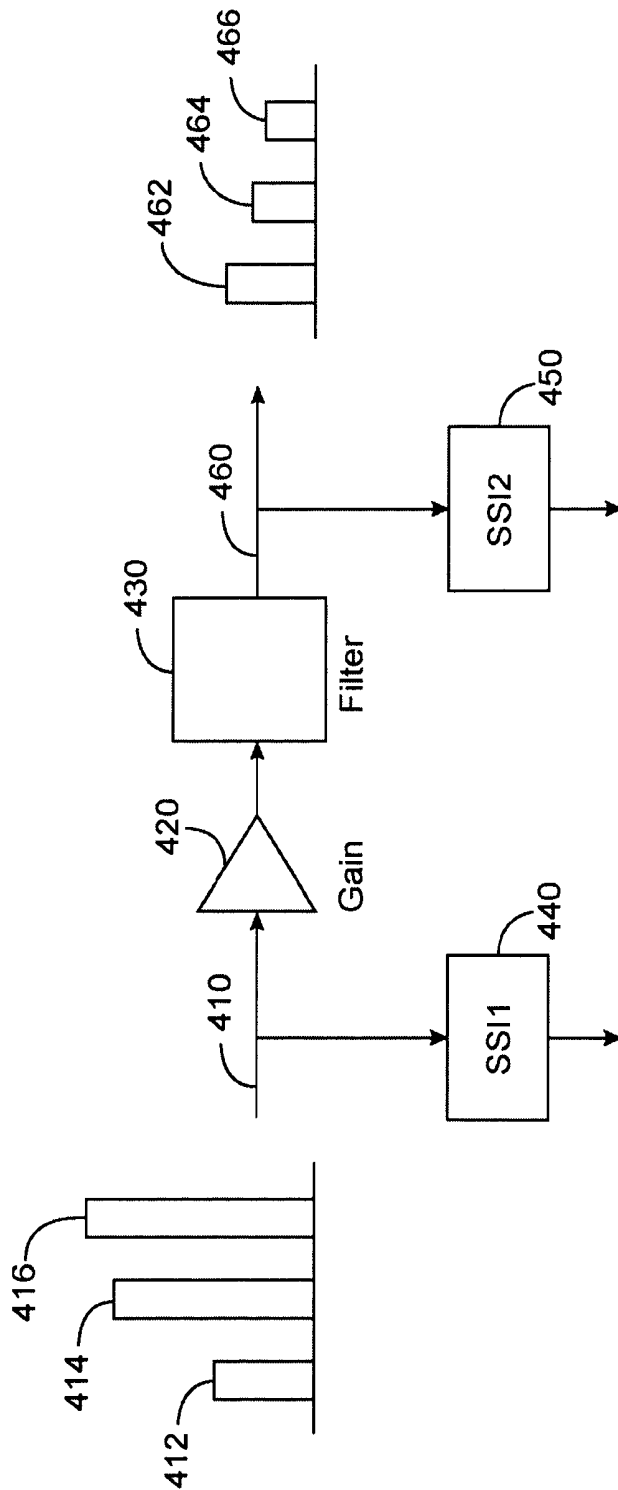


FIG. 4

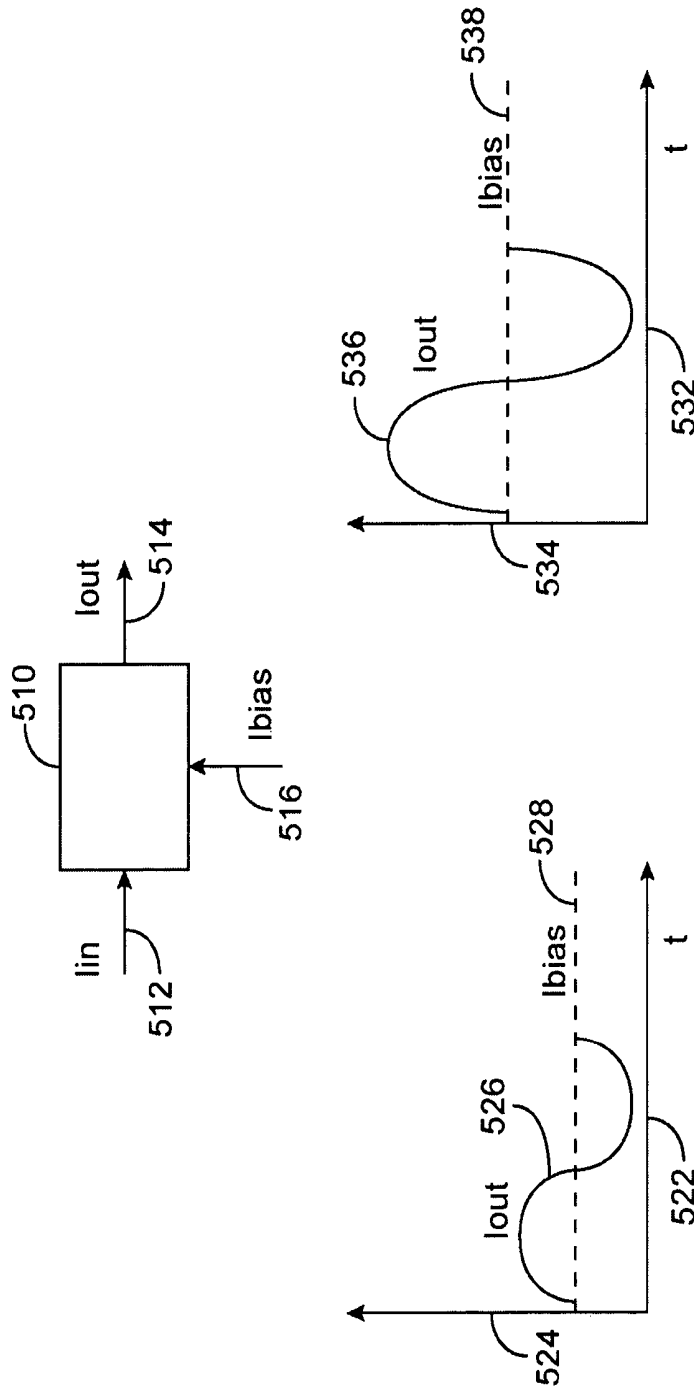


FIG. 5

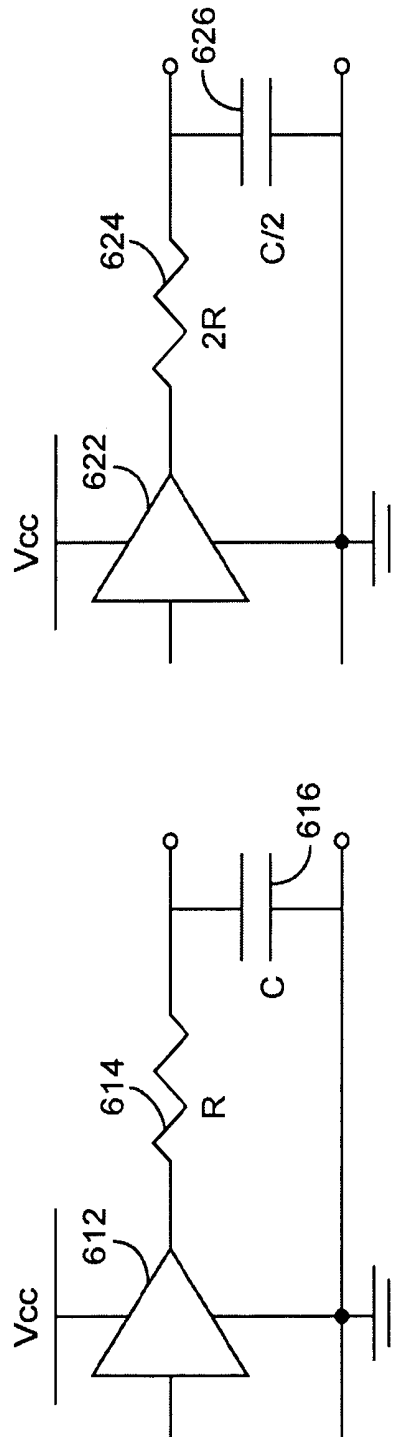


FIG. 6

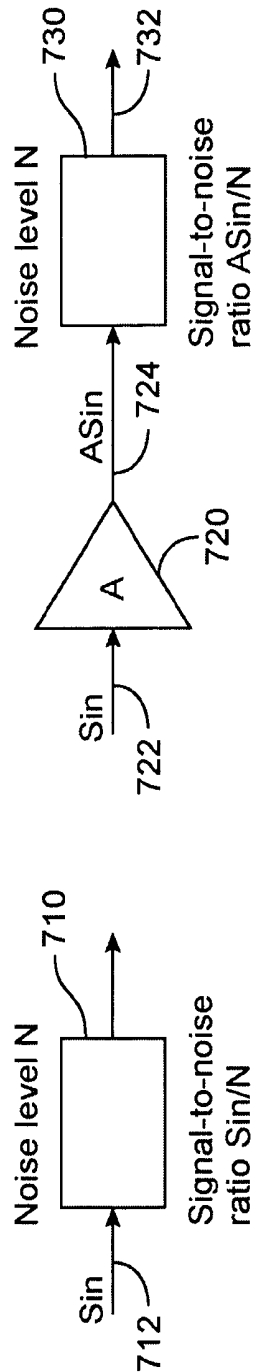


FIG. 7

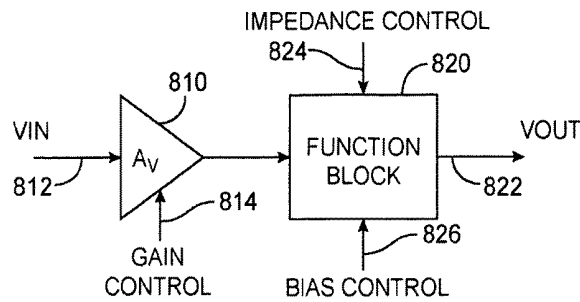


FIG. 8A

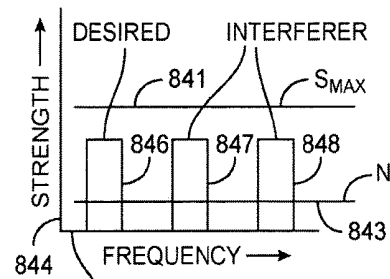


FIG. 8C

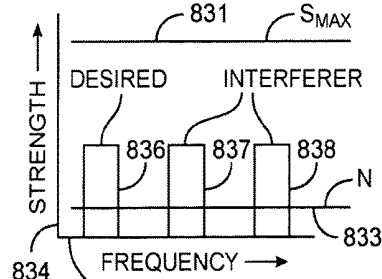


FIG. 8B

DECREASE
BIASING
- AND/OR -

INCREASE GAIN AND IMPEDANCES

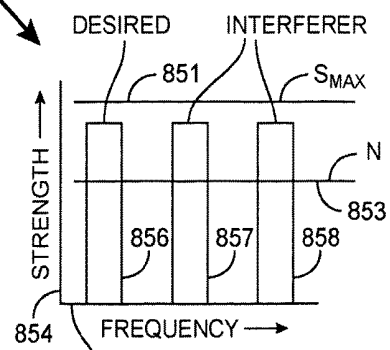


FIG. 8D

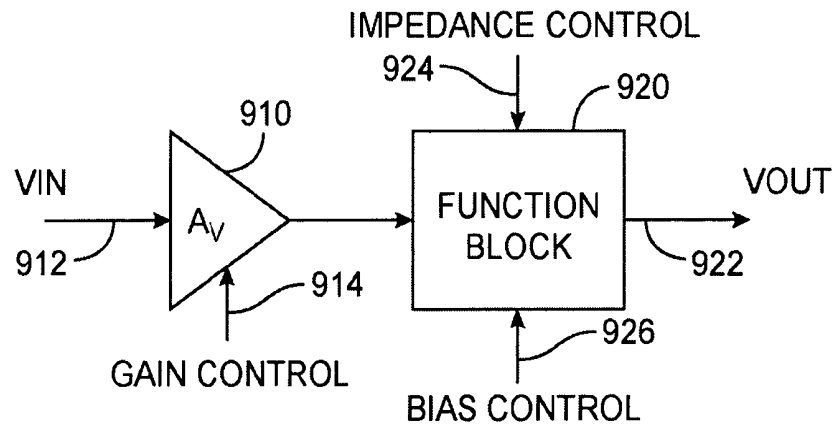


FIG. 9A

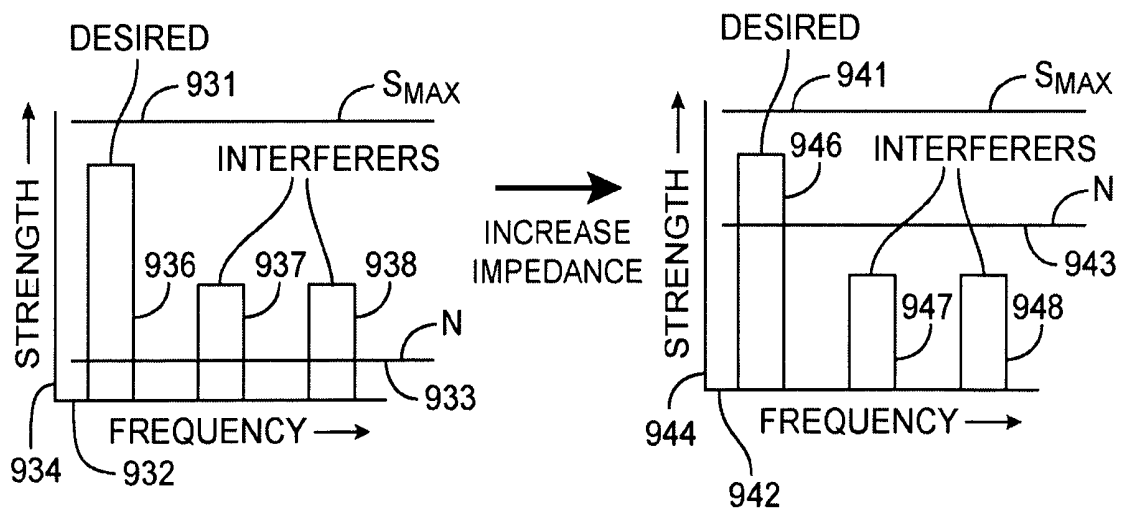


FIG. 9B

FIG. 9C

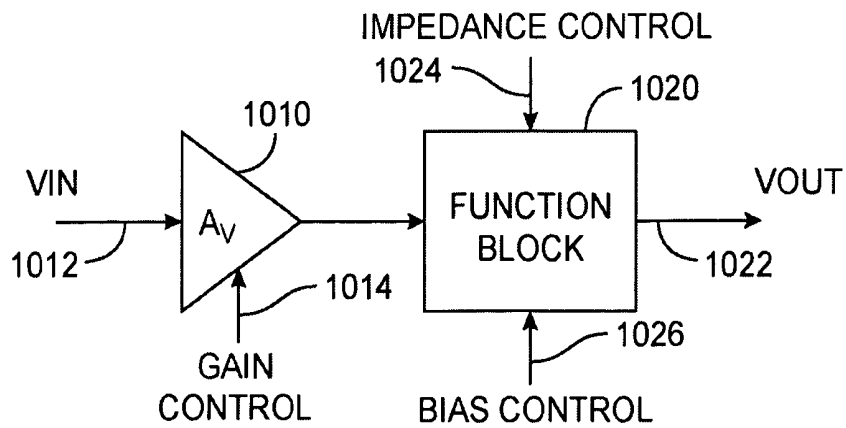


FIG. 10A

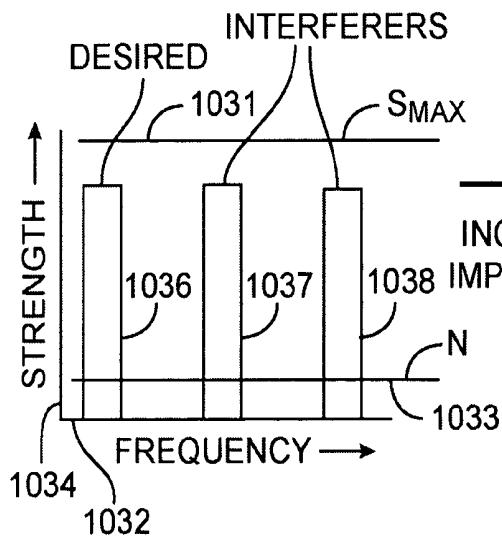


FIG. 10B

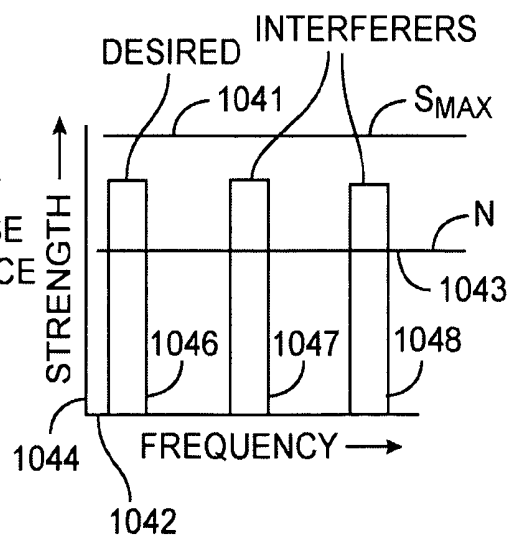


FIG. 10C

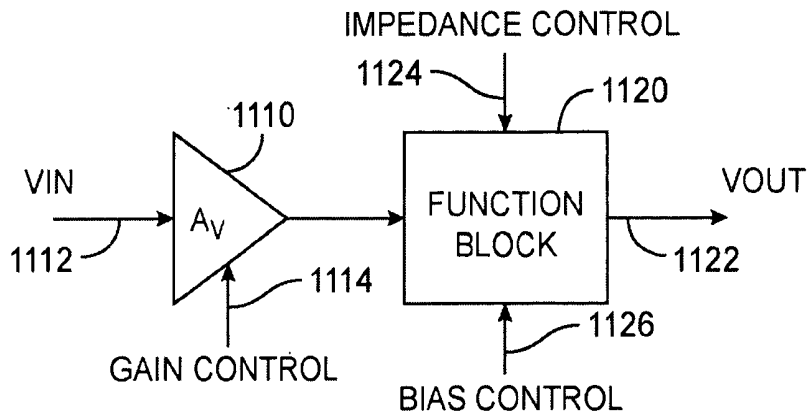


FIG. 11A

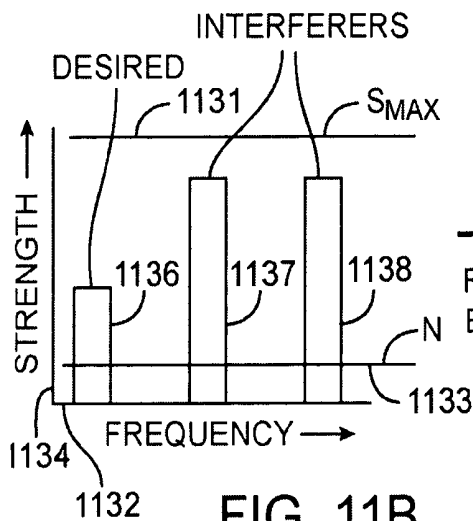


FIG. 11B

1160
REDUCE
BIASING

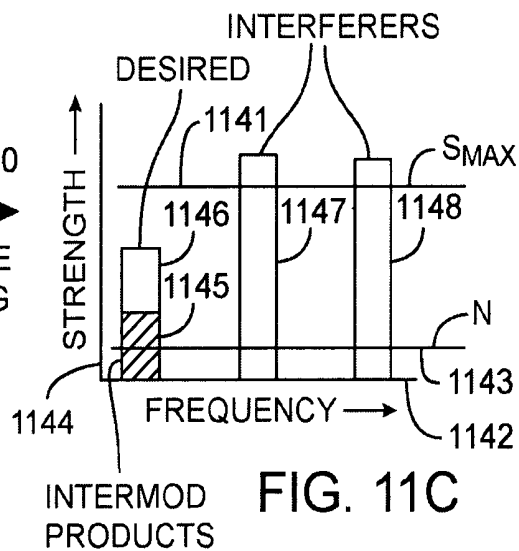


FIG. 11C

- AND/OR -

1170
INCREASE
IMPEDANCE

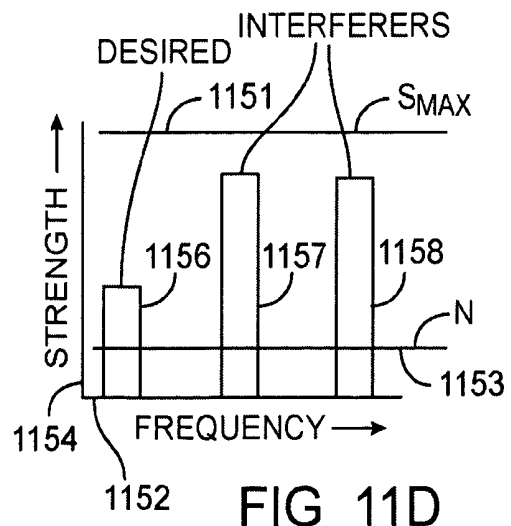


FIG. 11D

RECEIVED SIGNAL		RESPONSE TO RECEIVED SIGNAL		
SIGNAL STRENGTH	INTERFERER STRENGTH	DECREASE SMAX	INCREASE IMPEDANCE NOT GAIN	INCREASE IMPEDANCE AND GAIN
1230 SMALL	SMALL	YES	NO	YES
1240 LARGE	SMALL	NO	YES	NO
1250 LARGE	LARGE	NO	YES	NO
1260 SMALL	LARGE	NO	NO	NO

FIG. 12

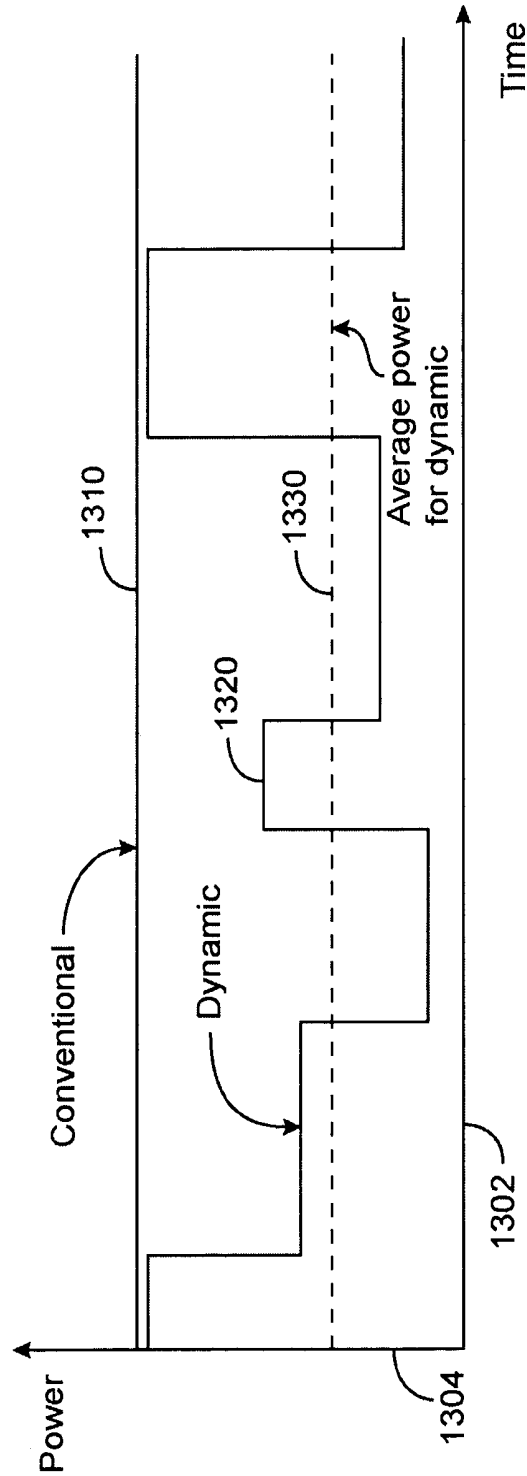


FIG 13

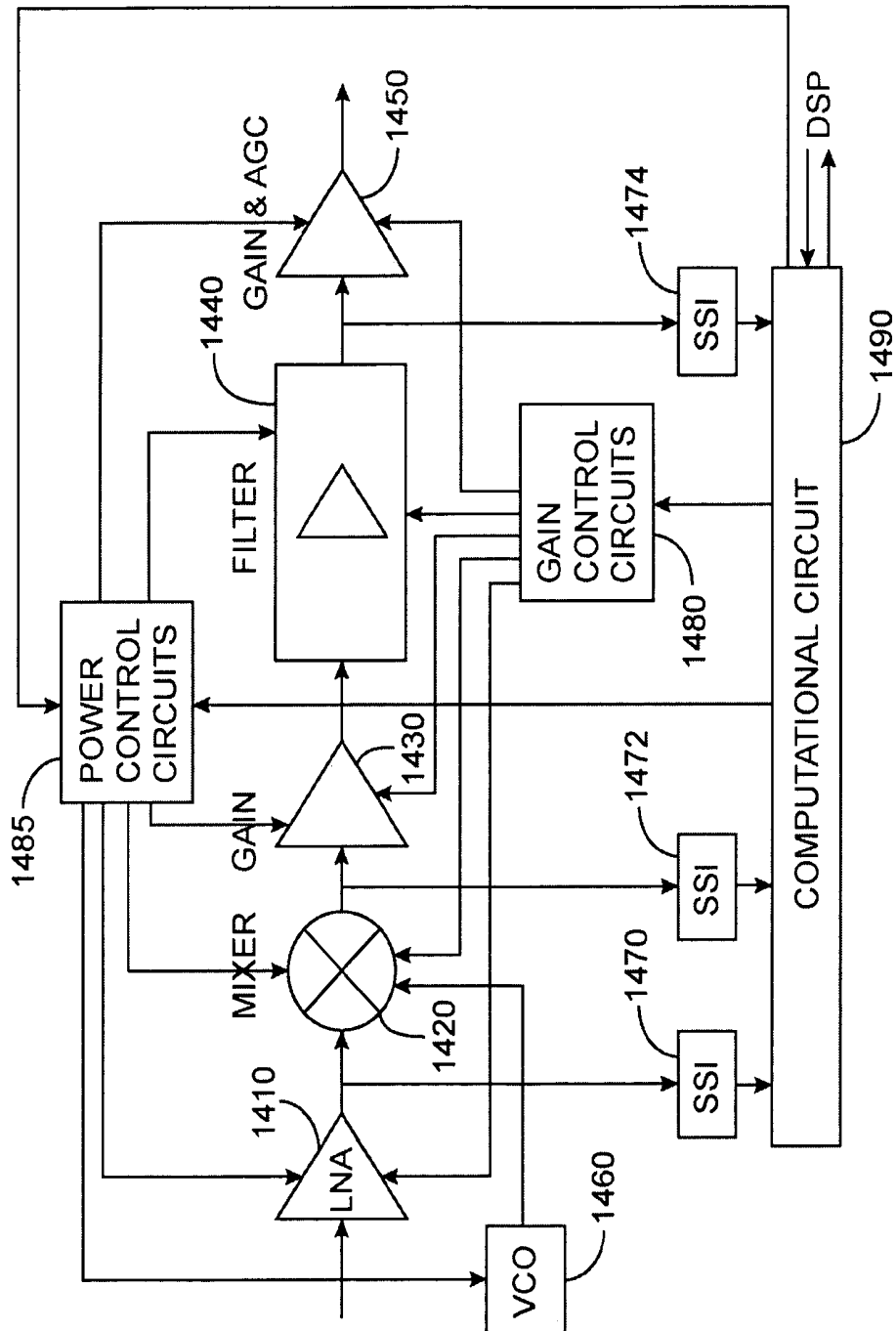


FIG. 14

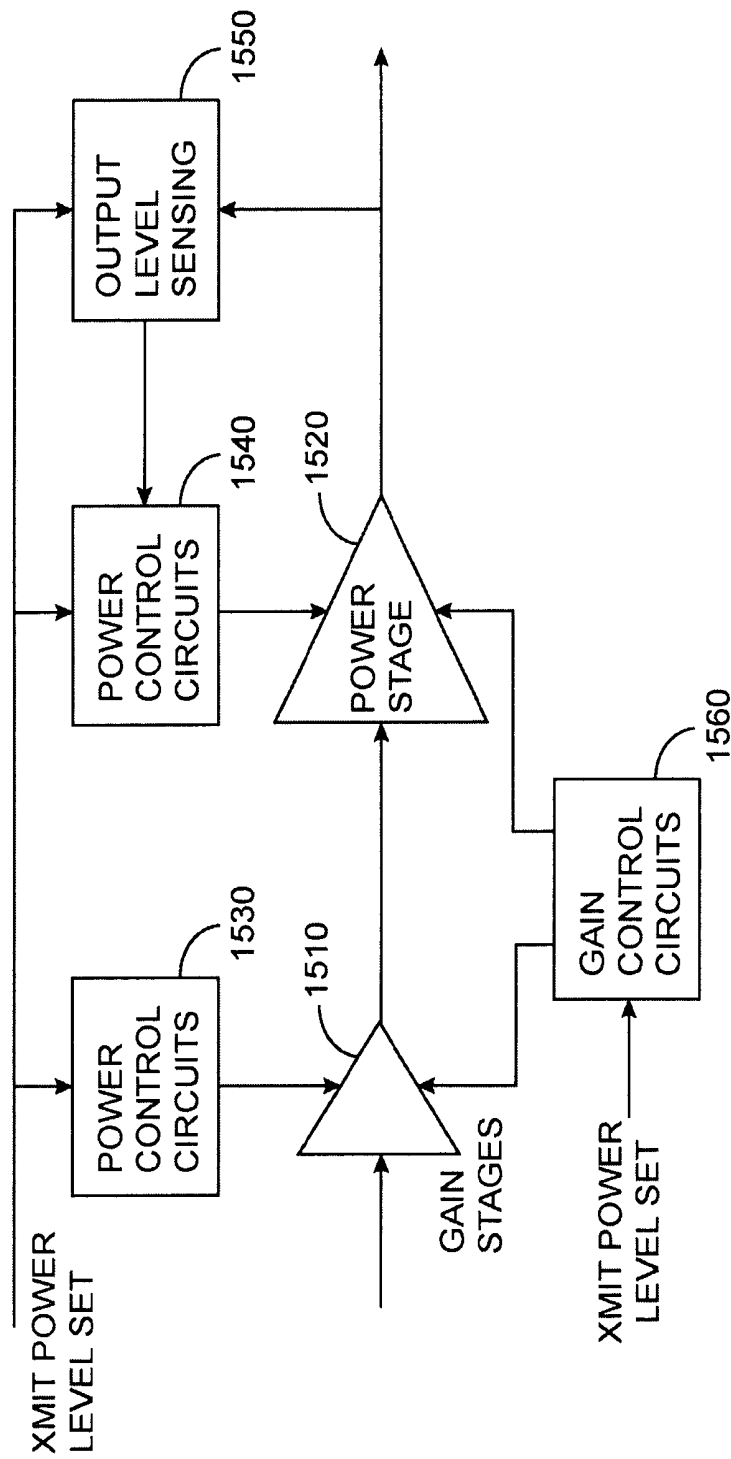


FIG. 15

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**POWER DISSIPATION REDUCTION IN
WIRELESS TRANSCEIVERS****CROSS-REFERENCES TO RELATED
APPLICATIONS**

This application is a continuation of U.S. patent application Ser. No. 16/714,629, filed Dec. 13, 2019, which is a continuation of U.S. patent application Ser. No. 15/824,841, filed Nov. 28, 2017, now U.S. Pat. No. 10,524,202, which is a continuation of U.S. patent application Ser. No. 15/080,421, filed Mar. 24, 2016, now U.S. Pat. No. 9,838,962, which is a continuation of U.S. patent application Ser. No. 11/318,646, filed Dec. 27, 2005, now U.S. Pat. No. 9,331,728, which is a continuation of U.S. patent application Ser. No. 10/784,613, filed Feb. 23, 2004, now U.S. Pat. No. 7,010,330, which claims the benefit of U.S. Provisional Application Nos. 60/451,229, filed Mar. 1, 2003 and 60/451,230, filed Mar. 1, 2003, the disclosures of which are hereby incorporated herein by reference in their entireties.

BACKGROUND

The present invention relates to power dissipation reduction techniques for electronic circuits, for example wireless transceiver integrated circuits.

Wireless networking is quickly becoming ubiquitous, as desktop, notebook, and handheld computers are connected to share Internet access and files. Wireless networking cards compatible with PCMCIA and compact flash form factors are popular for laptops and handhelds respectively, particularly as mobile users connect to the Internet on the road at coffee shops, hotels, and airports.

A downside of this connectivity is a corresponding drain on battery life, especially for these portable devices. The power consumed by a wireless transmitter and receiver reduces the usefulness of a device and sends a user on a hunt for an electrical outlet for recharging.

One reason why this power drain is high is that electronic circuits are typically designed to function properly under worst-case operating conditions. For a wireless transceiver, the worst case condition is when a desired signal reception strength is low, while other transceivers or nearby electronic equipment generate interfering signals and other spurious noise.

But a wireless transceiver does not always operate in these worst-case conditions. For example, a base station, router or access point may be nearby such that the received signal is strong. Also, there may be no interfering signals, or they may be relatively weak. In these situations, receiver circuit currents can be reduced below what is necessary for the worst case condition. If this is done, power dissipation is reduced, and battery life is increased.

Thus, what is needed are circuits and methods that can adapt to a better-than-worst-case condition and reduce circuit currents and therefore power dissipation accordingly.

SUMMARY

Accordingly, embodiments of the present invention provide methods and circuits for reducing power dissipation in wireless transceivers and other electronic circuits and systems. Embodiments of the present invention use bias current reduction, impedance scaling, gain, and other dynamic changes either separately or in combination to reduce power dissipation in response to better-than-worst case conditions. For example, bias currents are reduced in response to a need

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for reduced signal handling capability, impedances are scaled thus reducing required drive and other bias currents in response to a strong received signal, or gain is varied and impedances are scaled in response to a low received signal in the presence of no or weak interfering signals. Alternately, currents may start low and be increased in response to worse-than-best-case conditions, or they may start at a point in between and vary up or down. These variations may be made to electronic systems generally, and are particularly suited and discussed below in the context of a wireless transceiver that may be used in networking devices, cellular telephones, and other wireless systems.

An exemplary embodiment of the present invention provides a method of receiving a signal using an integrated circuit. The integrated circuit includes a signal path having a low-noise amplifier configured to receive the signal, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer. The method itself includes determining a first signal strength at a first node in the signal path in the integrated circuit and dynamically changing an impedance of a component in the signal path based on the first signal strength.

A further exemplary embodiment of the present invention provides a method of receiving a signal using an integrated circuit. The integrated circuit includes a signal path having a low-noise amplifier configured to receive the signal, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer. The method itself includes determining a first signal strength at a first node in the signal path in the integrated circuit and dynamically changing a bias current in the signal path based on the first signal strength.

Another exemplary embodiment of the present invention provides a method of receiving a signal using an integrated circuit. The integrated circuit includes a signal path having a first circuit and a second circuit having an input coupled to an output of the first circuit. The method itself includes determining a first signal strength at a first node in the signal path in the integrated circuit. The first node is before the first circuit in the signal path. The method further includes dynamically changing a gain of the first circuit based on the first signal strength and dynamically changing an impedance of a component in the second circuit based on the first signal strength.

Still a further exemplary embodiment of the present invention provides a wireless transceiver integrated circuit including a receiver having a signal path, the signal path including a low-noise amplifier, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer, as well as a first signal strength indicator circuit coupled to the signal path and configured to determine a first signal strength. An impedance in the signal path is configured to be dynamically adjusted in response to the first signal strength.

Yet a further exemplary embodiment of the present invention provides a wireless transceiver integrated circuit. This integrated circuit includes a receiver comprising a signal path, the signal path having a low-noise amplifier, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer, as well as a first signal strength indicator circuit coupled to the signal path, and configured to determine a first signal strength. A bias current in the signal path is configured to be dynamically adjusted in response to the first signal strength.

Another exemplary embodiment of the present invention provides a wireless transceiver integrated circuit. This circuit includes a receiver comprising a signal path, the signal path having a first circuit; and a second circuit having an input coupled to an output of the first circuit; as well as a first signal strength indicator circuit coupled to the signal path, and configured to determine a first signal strength. A gain of the first circuit is configured to be dynamically adjusted in response to the first signal strength, and an impedance in the second circuit is configured to be dynamically adjusted in response to the first signal strength.

A better understanding of the nature and advantages of the present invention may be gained with reference to the following detailed description and the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a wireless transceiver that may benefit by incorporation of embodiments of the present invention;

FIGS. 2A and 2B illustrate examples of desired and interfering signals and noise that may be received by a circuit in a wireless receiver;

FIG. 3 illustrates what can occur as a maximum signal handling capability is reduced in the worst-case signal condition;

FIG. 4 illustrates a portion of a receiver consistent with an embodiment of the present invention;

FIG. 5 illustrates the relationship between a required bias current and a given output signal for a representative circuit;

FIG. 6 is an example of how a circuit's impedances may be scaled to reduce drive currents, and depending on the circuit configuration used, to reduce associated bias currents as well;

FIG. 7 illustrates how gain may be inserted in a signal path to improve a circuit's signal to noise ratio;

FIGS. 8A-8D illustrate some of the possible power saving techniques that may be used when received desired and interferer signals are all at a low power level;

FIGS. 9A-9C illustrate one of the possible power saving techniques that may be used when a received desired signal is strong while all interfering signals are at a low power level;

FIGS. 10A-10C illustrate one of the possible power saving techniques that may be used when received desired and interferer signals are all at a high power level;

FIGS. 11A-11D illustrate one of the possible power saving techniques that may be used when a received desired signal is weak while one or more interfering signals are strong;

FIG. 12 is a summary illustrating four different input conditions and some of the appropriate power-saving changes that may be made in response to those conditions;

FIG. 13 shows how power may be saved as a function of time by employing one or more of the power saving methods consistent with embodiments of the present invention;

FIG. 14 is a block diagram of a portion of a receiver consistent with an embodiment of the present invention; and

FIG. 15 is a block diagram of a portion of a transmitter consistent with an embodiment of the present invention.

DESCRIPTION OF EXEMPLARY EMBODIMENTS

FIG. 1 is a block diagram of a wireless transceiver that may benefit by incorporation of embodiments of the present

invention. This wireless transceiver may be designed to send and receive signals consistent with the IEEE 802.11a, 802.11b, 802.11g, or other signaling standard or combination of standards. This figure, as with all the included figures, is shown for illustrative purposes only and does not to limit either the possible embodiments of the present invention or the claims.

There are three main portions of this transceiver circuit, a receiver, transmitter, and synthesizer. This transceiver may be completely or partially integrated on a semiconductor chip, or it may be integrated onto multiple integrated circuits. In a specific embodiment, the circuitry bounded by dashed line 100 is integrated on a single chip coupled to one or more external components or circuits. The integrated circuit or circuits forming this wireless transceiver may incorporate various integrated circuit devices such as a bipolar, CMOS, or BiCMOS devices made using a silicon, silicon-germanium (SiGe), gallium arsenide or other III-V process, or other manufacturing process. Embodiments of the present invention may also be applicable to circuits manufactured using nanotechnology processing.

The receiver includes a signal path formed by low-noise amplifier 102, I and Q mixers 104 and 106, low pass filters 108 and 110, and baseband amplifiers 114 and 116. Other circuitry in the receiver includes received strength indicator 122, automatic gain control circuit 166, baseband gain control circuit 120, tuning circuit 112, and offset cancellation circuit 118.

The transmitter includes input up-converter mixers 124 and 126, summing node 176, which may be conceptual rather than an actual circuit, transmit variable gain amplifier 128, and power amplifier 130.

The synthesizer includes a voltage-controlled oscillator 148, which drives I and Q buffers 154 and 152, prescaler 156, reference clock buffer 142 and divider 158, phase-frequency detector 160, charge pump 162, and loop filter 146, which in a specific embodiment is formed by external components.

Signals are received on an antenna, not shown, and typically pass through an RF switch and bandpass filter before being received by the low-noise amplifier 102 on line 101. The low noise amplifier gains the received signal and provides it to quadrature mixers 104 and 106. I and Q mixers 104 and 106 down-convert the received signal to baseband by multiplying them with quadrature versions of the oscillator signal provided by buffers 152 and 154. This down conversion also produces a high frequency component at a frequency that is equal to the sum of the frequencies of the received signal and the VCO. This unwanted signal is filtered by low pass filters 108 and 110, which in turn drive baseband amplifiers 114 and 116. The outputs of baseband amplifiers 114 and 116 are typically converted to digital signals by analog-to-digital converters at the front end of a digital signal processing block.

In the transmit mode, I and Q versions of the signal to be transmitted are provided on lines 121 and 123 to up-convert mixers 124 and 126. These up-convert mixers multiply the I and Q portions of the transmit signal by quadrature versions of the VCO signal provided by buffers 152 and 154. The outputs of the up-convert mixers 124 and 126 are summed, and amplified by transmit VGA 128, which in turn drives power amplifier 130. The output of power amplifier 130 is typically filtered, and passes through the RF switch to the antenna for transmission.

A reference clock is received and buffered by the reference buffer 142. The VCO generates quadrature oscillatory signals that are divided by prescaler 156. The reference

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clock is typically generated by a crystal or other stable periodic clock source. The phase-frequency detector **116** compares the phase or frequency (depending on whether the synthesizer is tracking or acquiring the correct frequency) of the divided VCO signal and the reference clock, or a divided version of the reference clock, and generates an error signal, which drives the charge pump **162**. The output signal of the charge pump **162** is filtered by the loop filter **146**, which is commonly a lead-lag filter, and which provides a tuning or correction signal to the VCO **148**.

Embodiments of the present invention may be used to reduce the power dissipation of one or more of these included circuits. For example, the power dissipation in the low-noise amplifier **102**, down-convert mixers **104** and **106**, low pass filters **108** and **110**, or baseband amplifiers **114** and **116** may be optimized. Also, power dissipation in up-convert mixers **124** **126**, variable gain amplifier **128**, and power amplifier **130** may also be optimized. Similarly, VCO **148** and prescaler **156** currents may be adjusted. Embodiments of the present invention may also be applied in other circuits which may be included in other integrated circuit receivers, transmitters, transceivers, or other electronic circuits or systems.

When a receiver is actively receiving a desired signal, each block in the signal path has at its input the desired signal as well as noise and possibly interfering signals. The desired signal is the useful, information-carrying portion of a received signal. The noise may be thermal, shot, or other noise generated on the integrated circuit, in addition to received noise generated by sources external to the chip. The noise at the input of a block may be referred to as the equivalent input noise. The interfering signal or signals, or interferers, may be generated by similar transceivers, or other electrical equipment, circuits, or systems.

FIGS. **2A** and **2B** illustrate examples of desired signals, interferers, and noise that may be received by one of the various circuits in a wireless receiver. In each of these figures, the signal strength is plotted along a Y-axis **204** or **254** as a function of frequency along an X-axis **202** or **252**. In the example of FIG. **2A**, a received desired signal **206** is large in comparison to interfering signals **208** and **210**. In these examples, two interfering signals are shown for illustrative purposes, though there may be no such signals, one such signal, or more than two such signals in the frequency range of interest. Also, while for these examples the interferers are shown as being at a higher frequency than the desired signal, there may be one or more interferers at higher or lower frequencies as the desired signal. In this specific example, the acceptable noise floor **214** is relatively high, while maximum signal handling capability S_{max} **212** (that is the maximum signal power that can be handled with an acceptably low distortion) needs only to be high enough to accommodate the desired signal. For this specific example, the circuit receiving this input spectrum only requires a relatively small dynamic range for proper operation, that is the range between S_{max} **212** and the noise floor **214** is relatively small.

Conversely, in the example shown in FIG. **2B**, the desired signal **256** is relatively weak compared to the large interferers **258** and **260**. In this example, the noise floor **264** should be relatively low so as to prevent an unacceptable level of error in the recovery the desired signal **256**. The maximum signal handling capability S_{max} **262** should be relatively high to accommodate the large interferers in order to avoid the creation of intermodulation products as described below. Accordingly, in this specific example, the

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circuit receiving this input spectrum should have a large dynamic range, particularly in comparison to the example of FIG. **2A**.

It should be noted that the noise level or noise floors shown in these and the other included figures is the noise density integrated over the bandwidth of interest. For simplicity and comparison, this level is shown as a horizontal line, and is not meant to imply noise density.

Often in wireless receivers, a circuit at different times will receive an input spectrum similar to those shown in FIGS. **2A** and **2B**. The input spectrum of FIG. **2B** is generally considered the worst-case input signal, and typical design methodology involves designing a receiver for this condition, specifically the weakest desired signal accompanied by largest interference level. Circuit impedances and currents are set such that the noise floor **264** is sufficiently low for an acceptable bit-error rate, while bias currents are set sufficiently high for the required S_{max} **262**.

Conversely, the input spectrum in FIG. **2A** is that of the best-case input signal, specifically, a robust desired signal accompanied by no or low-level interferers. In this case, the noise floor **214** may be allowed to rise, while the maximum signal handling capability S_{max} **212** may be reduced. When this is done, the receiver circuit may save significant power. For example, the circuit's impedances may be increased, thus reducing required drive currents. Similarly, bias currents may be lowered, thus reducing the maximum signal in handling capability.

The minimum power dissipation for a circuit is proportional to the required maximum signal-to-noise ratio, which is the ratio between S_{max} **212** or **262** and N **214** and **264**. Thus, a circuit receiving an input similar to the one shown in FIG. **2A** can dissipate less power than one receiving the input as shown in FIG. **2B**, while still achieving an acceptable bit-error rate.

FIG. **3** illustrates what can occur when the maximum signal handling capability S_{max} **314** is reduced in the worst-case condition, that is when a weak desired signal **306** is accompanied by large interferers **310** and **312**. Again, signal strength is plotted along a Y-axis **304** as a function of frequency along X-axis **302**. In this specific example, S_{max} **314** is reduced below the peak levels of the interferers **310** and **312**. Since S_{max} is low, the circuit cannot handle the interferers linearly. The resulting nonlinearities lead to a mixing of the interferers and the creation of intermodulation products **308** (for example, a third-order intermodulation distortion, IM3), one of which in this example occurs at the same frequency as the desired signal **306**. As can be seen, if the intermodulation products **308** become excessive, the received signal bit error rate may become excessive, and the desired signal **306** may be lost. Accordingly, while S_{max} may be lowered even under some unfavorable conditions in order to reduce power, care should be taken to avoid corruption of the received desired signal.

FIG. **4** illustrates a portion of a receiver consistent with an embodiment of the present invention. Included is a filter **430**. An optional gain element **420** is placed in front of the filter **430** in order to increase signal levels. Signal strength indicator circuits **440** and **450** are connected to input line **410** and output line **460**. In this specific example, the input signal spectrum on line **410** is shown as desired signal **412** and interferers **414** and **416**. The signal spectrum at the output line **460** is shown as desired signal **462** and interferers **464** and **466**. The signal strength indicators **440** and **450** do not provide information as to the relative sizes of the desired and interfering signals. Rather, a cumulative signal level is provided at their outputs. For example, the first signal

strength indicator **440** outputs a level corresponding to the sum of desired signal **412** and interfering signals **414** and **416**, while the second signal strength indicator **450** provides a signal level corresponding to the sum of desired signal **462** and interfering signals **464** and **466**. In this specific example, the gain of the gain and filter circuit combinations is shown as approximately one, while the interfering signals **414** and **416** signal levels are reduced.

A comparison of the signal levels provided by the signal strength indicators **440** and **450** indicates that much of the combined received signal on line **410** has been filtered. Accordingly, it may be deduced that large interfering signals present at the input are being filtered by the filter **430**. From this information, as will be shown in greater detail below, the bias, impedance, and gain of the gain stage **420** and filter **430** combination may be optimized to reduce power dissipation.

There are several real world situations where the received signal is better than the worst-case condition such that power can be saved. For example, large interferers may be present only part of the time, that is, on a temporary or transient basis. The interfering equipment may be some distance from the transceiver, or it may be operating in the low power mode. Also, the desired signal may be very strong as compared to the noise and interferers, for example a hub, router, or access point may be nearby.

Some transceivers consistent with embodiments of the present invention are designed to work with more than one data transfer specification or standard. In this case, when a transceiver is operating in a mode having a lower data rate, the power saving techniques described here may be employed.

FIG. **5** illustrates the relationship between a required biased current **516** for a given output signal **514** for a representative circuit **510**. If the output signal current level is relatively low, such as the output current shown as **526**, the corresponding bias current **528** may be low. Conversely, if the output signal current level is larger as with the example **536**, the corresponding bias current level **538** should also be high. Accordingly, if a bias current is initially set high to handle large a large input signal, for example a large interferer, this current may be reduced if the input signal is smaller.

There are many ways by which these bias currents can be reduced. For example, the current may be generated by placing a voltage across a resistor by applying a bias voltage to the base of a device whose emitter is connected to ground through a resistance. In this case, the resistor may be increased by opening switches across portions of the resistance, or lowering the bias voltage applied at the base. Several ways in which this may be done will be readily understood by one skilled in the art.

FIG. **6** is an example of how a circuit's impedances may be scaled to reduce drive currents, and, depending on the circuit configuration used, associated bias currents as well. A driver **612** has a load **R 614** and **C 616**. The frequency response of this circuit is the same as that seen by driver **622**, which drives an impedance of $2R$ **624** and $C/2$ **626**. But the impedance of the load seen by driver **622** is double that seen by **612**, thus the output current required by the driver **622** is reduced by one-half.

As an example, the output stage of each of these drivers may be a Class A emitter follower formed by an emitter follower connected to a current source. When the outputs are driven high, the emitter of driver **622** need supply only one-half the drive current as driver **612**. In this way, an impedance can be scaled in order to decrease a circuit's required drive current.

Also, the discharge current for driver **622** is only one half that of driver **612** for a given negative-going slew rate. Thus, the current source of **622** may be reduced by the same factor of one-half as compared to driver **612**. In this example, the bias current, that is the current in the pull-down current source can be reduced. Many other examples where drive currents and possibly bias currents may be reduced will be appreciated by one skilled in the art.

FIG. **7** illustrates another degree of freedom that made be employed to reduce current levels in a transceiver. Specifically, a gain element **720** may be inserted in front of a circuit block **730** in order to improve the combined circuit's signal-to-noise ratio by a factor equal to the gain of the inserted gain block. This is particularly useful when large interferers are absent and the desired received signal is moderate or low. Specifically, gain is added to the signal while impedances are increased, which raise the noise floor. In this way, a given signal-to-noise ratio may be maintained while the power is decreased.

The gain of such an element may be varied by increasing a current in a differential pair or increasing a load resistance using switches. Many other examples where the gain of this element may be varied will be appreciated by one skilled in the art.

These variables, or degrees of freedom, specifically reducing bias currents, increasing impedances, and increasing gain may be used as in the following examples.

FIG. **8A** is a block diagram of a functional block **820** and optional gain element **810** in accordance with an embodiment of the present invention. Functional block **820**, like the functional blocks in the following diagrams, may be a filter, mixer, amplifier, or other circuit or circuits in a wireless transceiver or other electronic circuits or system. An input signal is received on line **812** by the optional gain element **814**. When the optional gain block **810** is not used, the input signal may be received directly by the function block **820**. The gain of the optional gain element **812** is controlled by a gain control signal on line **814**. The functional block receives an output signal from the optional gain element **810** and provides an output VOUT on line **822**. The lines in this and the other included figures may be one or more lines, depending on whether single-ended, differential, or other type of signaling is employed.

One or more impedances are under control of signals on impedance control lines **824**. Similarly, one or more bias currents in the function block are under control of one or more signals on bias control lines **826**. These various control lines may be logic signals, analog signals, voltage or currents lines, or other signal or bias lines. In other embodiments of the present invention, the gain control element **810** may be included in the function block **820**. Also, various embodiments may not incorporate either or both the impedance control and bias control.

FIG. **8B** is an example input that may be present on line VIN **812**. In this example, a desired signal **836** is relatively weak, as are interfering signals **837** and **838**. The initial bias and circuit configuration is such that the noise floor **833** and maximum signal handling capability **Smax 831** are adjusted for worst case conditions. The circuit of FIG. **8A**, as with all the circuits described here, receives noise at its input which may be referred to as input equivalent noise or input referred noise. Additionally, the circuit of FIG. **8A** generates noise which is added to the input referred noise. Depending on the gain characteristics of the circuitry, the output noise at various frequencies may be greater than, equal to, or less than the input referred noise. For simplicity, the noise floor and maximum signal handling capability **Smax**, in this and

the other figures, are shown as straight lines, though the noise and Smax are typically curved as a function of frequency.

That the input spectrum is as shown in FIG. 8B can be determined, for example, by low signal strength indications on line VIN **812** and VOUT **822**. That is, a low level signal strength indication on line VIN **812** indicates that no portion of the input signal is particularly large.

For this exemplary input, there are at least two methods by which the power dissipation for this circuitry may be reduced. Depending on the exact circuits and structures used, one of these methods may be preferred.

In FIG. 8C, the bias current is decreased, thereby lowering the maximum signal handling capability **841** as compared to **831**, closer to the desired and interfering signal levels. Again, the bias currents in the function block **820** may be reduced by switching impedances that appear across a voltage thereby changing a resulting bias current, by reducing a voltage at the gate of a MOS or base of a bipolar transistor, or by other methods.

In FIG. 8D, a second method of reducing power dissipation in the function block **820** is employed. Specifically, Smax **851** is held constant as compared Smax **831**. The desired and interfering signals are amplified such that they are closer to the available signaling handling capability **851**. Also, the noise floor **853** is raised as compared to noise floor **833** in FIG. 8B. Specifically, the noise contributed by the function block **820** is increased, such that the noise at its output is increased to noise floor **853**. This is done by increasing one or more impedance in function block **810**, such that drive currents inside that block are reduced. Depending on the exact configuration, this may also allow some biasing currents to be reduced, while maintaining the maximum signal handling capability **851** at a sufficient level. Alternately, these two methods of reducing power dissipation in function block **820** may be done in combination.

The included examples are explained for the exemplary situation where biasing and other parameters are set for worst-case conditions, and then changed to save power when it is discovered that the conditions are better-than-worst case. Alternately, the bias currents and other parameters may be set for maximum power savings, or an intermediate point, and the power can be adjusted from there.

FIG. 9A illustrates a block diagram including an optional gain element **910** and function block **920**. Again, an input signal is received on line **912** by optional gain element **910** which in turn drives function block **920**. The function block provides an output VOUT on line **922**, and receives impedance and bias control signals on lines **924** and **926**.

FIG. 9B shows the spectrum for what may be considered a best-case received signal. Specifically, the desired signal **936** is strong, while the interfering signals **937** and **938** are relatively weak. This may be determined, for example, by detecting a large signal level at the input line VIN **812** and a large signal level after a filter, since these readings would indicate that a large signal is received, but that it is at the desired signal frequency.

The maximum signaling capability **931** and noise floor **933** are shown as being set for the worst case conditions. In this case, the noise floor **933** is lower than the maximum allowed for proper signal reception. Accordingly, one or more impedance in the function block **920** may be increased, such that the noise floor **943** rises as shown in FIG. 9C. In this way one or more the driving currents in the function block **920** may be reduced. Similarly, since the drive current is reduced, one or more bias current may also be reduced, depending on the exact circuit configuration.

FIG. 10A illustrates a block diagram showing an optional gain element **1010** driving a function block **1020**. An input signal is received by the gain element **1010** on line **1012**, and an output is provided by function block **1020** on line VOUT **1022**. One or more gain control signals present on lines **1014** control the gain of gain control element **1010**, while one or more impedance and bias control signals are received by the function block **1020** on line to **1024** and **1026**.

FIG. 10B illustrates a received signal that may be received on line VIN **1012**. In this example, the desired signal **1036** and interferers **1037** and **1038** are each relatively large. This may be determined, for example, by detecting a large signal level at the input line VIN **812** and a smaller signal level after a filter, since these readings would indicate that a large signal is received, but that interferers are being reduced.

As before, in this example, the noise floor **1033** and maximum signal handling capability **1031** are initially set for the worst case conditions. Since the desired signal is relatively large in this case, the noise floor may be allowed to rise, as shown by noise floor **1043** in FIG. 10C. Since the desired signal **1046** and interferers **1047** are large, the maximum signal handling capability Smax **1041** remains constant. Again, the noise floor is increased by increasing impedances in the function block **1020**. This reduces the required drive current, and may also allow for a reduction in bias currents.

FIG. 11A illustrates a block diagram including an optional gain element **1110** and function block **1120** in accordance with an embodiment of the present convention. An input signal is received on line **1112** by the optional gain control element **1110**, while an output signal is provided by the function block **1120** on line VOUT **1122**. Gain, impedance, and bias control signals are received on lines **1114**, **1124**, and **1126**.

FIG. 11B is an exemplary input signal that may be received by the gain control element **1110** on line VIN **1112**. In this specific example, the desired signal **1136** is relatively low or weak while the interfering signals **1137** and **1138** are large. This may be determined, for example, by detecting a large signal level at the input line VIN **812** and a much smaller signal level after a filter, since these readings would indicate that a large signal is received and that large interferers are being reduced such that the resulting signal, the desired signal, is relatively weak.

Again, the maximum signal handling capability **1131** and noise floor **1133** are initially set for worst case conditions. If the desired signal is sufficiently low, while the interferers are sufficiently high, power savings may not be achievable over the worst case settings, since this is in fact the worst case condition. But, if the desired signal is somewhat larger than the worst case condition, then power may be saved in at least two different ways.

For example, FIG. 11C shows the maximum signal handling capability **1141** being lowered. In this case, the interfering signals **1147** in **1148** began to clip and distort, thereby creating intermodulation products **1145**, which distort the desired signal **1146**. So long as care is taken to not corrupt the desired signal **1146** beyond an acceptable limit, typically measured by a bit-error rate, power may be reduced in this way.

Similarly, in FIG. 11D, the noise floor **1153** is raised somewhat, thereby saving power. Again, this may be done so long as the noise floor is not sufficiently high that the system bit-error rate becomes unacceptable.

FIG. 12 is a summary of the above four examples. The received signal strengths are shown in column **1210**, while appropriate power saving responses are listed in column

1220. Specifically, in row 1230, the desired signal and interferer signal strengths are both weak or small. In this case, proper responses include decreasing Smax, or increasing one or more circuit impedances while increasing the circuit gain. Depending on the exact circuit configuration, one of these options may be preferred over the other. Alternately, they may be done in combination, or done in combination with other power saving techniques. Also, in some specific embodiments, when both desired signal and interferer signal strengths are small, the gain may need to be increased while the impedance is maintained or not increased in order to keep the noise floor low.

In row 1240, the desired signal strength is strong or large, while the interfering signals are small. In this case, an appropriate response is to increase one or more of the circuit impedances. Again, depending on the exact circuit in question, one or more of the bias currents may also be reduced.

In row 1250, both the desired signals and interfering signal strengths are large. Again, in this case an appropriate response is to increase one or more of the circuit impedances.

In row 1260, the received desired signal strength is weak or small, while the interfering signals are large. Since this is the worst case situation for which the circuit is designed, substantial power savings are difficult to achieve. However, again, if the received signal is above a minimum level necessary for proper operation, some distortion of the interferers or raising of the noise floor may be acceptable.

It should be noted that not all possible signal conditions are listed here. For example, either the signal or interferer may be of a relatively medium strength, or the interferer may be absent. Also, these terms are for exemplary purposes and are not meant to convey specific signal conditions, but rather are only qualitative. The proper response to a specific condition depends on the embodiment of the present invention, the particular circuit topology, the requirements of the signaling standard used, as well as other constraints.

FIG. 13 is an example shown how power may be saved as a function of time by employing one or more of these methods consistent with embodiments of the present invention. Power is plotted along a Y-axis 1304 as a function of time along X-axis 1302. Conventional worst case design would fix power dissipation at line 1310. As can be seen, dynamic power dissipation 1320 under the control of variable gains, impedances, biasing, or combination thereof, allows for a lower average power 1330 as compared to the power dissipated 1310 by the conventional design.

FIG. 14 is a block diagram of a portion of a receiver consistent with an embodiment of the present invention. Included are low-noise amplifier 1410, mixer 1420, gain stage 1430, filter 1440, AGC amplifier 1450, and VCO 1460. Signal strength detection is done at the output of the low-noise amplifier by signal strength indicator 1470, at the output of the mixer by signal strength indicator 1472, and at the output of the filter by signal strength indicator 1474. The outputs of the signal strength indicator circuits are received by the computational circuit 1470, which in turn controls gain and power control circuits 1480 and 1485. Power and gain control circuits 1480 and 1485 control the gain, biasing, and impedance levels of the circuits in the receiver signal path. Also, the gain and power control circuits may control the same parameters in the VCO 1460. This figure is greatly simplified for purposes of explanation. For example, the quadrature nature of the mixers and following circuits are not shown. Also, power-down and start-up circuits are not included.

The current level in the low-noise amplifier determines a multitude of parameters including voltage gain, linearity, input impedance matching, and noise figure. When conditions are better than worst-case, some of these parameters may be relaxed while maintaining an acceptable bit-error rate, thus saving power.

The bias current in the mixers effect that block's noise figure and linearity. Care is taken in reducing power in this block so as not to increase nonlinearities, particularly the third-order nonlinearity as measured by 1133, the third-order intercept point, beyond an acceptable limit.

A key parameter of the VCO is phase noise, an increase in which increases the sidebands on either side of the oscillation signal. During transmission, the phase noise should be kept low to avoid interference with adjacent channels and for preserving modulation information.

During reception however, if the conditions are better than worst case, the phase noise requirement for the VCO is relaxed, and power can be saved consistent with embodiments of the present invention. The achievable phase noise power spectral density is approximately inversely proportional to the bias current used. Thus, when low phase noise is not required during reception, bias current in the VCO can be reduced.

Most of the power savings in a transceiver in accordance with embodiments of the present invention is achieved in the receiver portion. Additional power may be saved in the transmitter section.

FIG. 15 is a block diagram of a transmitter portion consistent with an embodiment of the present invention. Included is a signal path formed by gain stage 1510 and power amplifier 1520. The output power level is sensed by output level sensing circuit 1550, which in turn adjusts the biasing of the power amplifier 1520 through the power control circuit 1540. Additionally, a transmitter level control signal is received by power control circuits 1530 and 1540, which in turn control the biasing of gain stage 1510 and power amplifier 1520. Gain control circuit 1560 also adjusts the gain of gain stage 1510 and power amplifier 1520. Additional circuitry that varies impedances in each of these circuits may also be included.

Since the gain, impedance and biasing of these blocks are being dynamically varied, care must be taken to not negatively affect the signal being processed. For example, specific embodiments of the present invention perform some or all of these variations during preamble. Also, as changes occur, the circuits in some embodiments are limited such that they may only adapt to an improvement in conditions after frames are completed. If conditions worsen, the circuits may be allowed to change in order to save the data. Alternately, a system may be manually calibrated, for example at set up, and when the network configuration is changed.

The above description of specific embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form described, and many modifications and variations are possible in light of the teaching above. The embodiments were chosen and described in order to best explain the principles of the invention and its practical applications to thereby enable others skilled in the art to best utilize the invention in various embodiments and with various modifications as are suited to the particular use contemplated.

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What is claimed is:

1. A system for power dissipation reduction in a battery powered portable wireless communication device, the system comprising:

- a battery powered portable wireless communication device, the wireless communication device comprising:
 - a battery configured to supply power for the battery powered portable wireless communication device;
 - a wireless receiver configured to receive a wireless signal, wherein the wireless signal has a desired signal and an interferer signal, the wireless receiver having a plurality of circuits that includes circuits in a receiver signal path, the plurality of circuits designed to operate under a worst-case operating condition where the corresponding power drain from the battery is a maximum, thereby consuming maximum power from the battery; and
 - a monitoring circuit associated with the battery powered portable communication wireless device configured to monitor the signal strength of the interferer signal,

wherein a power dissipation control circuit in the wireless receiver causes a bias current to be dynamically adjusted in one or more of the circuits in the receiver signal path as the monitored signal strength of the interferer signal varies during operation when the operating condition is better than the worst-case operating condition, enabling a power dissipation reduction in the wireless receiver, providing a corresponding reduction in a power consumption from the battery of the battery powered portable wireless communication device.

2. The system of claim 1, wherein the power dissipation control circuit is configured to dynamically adjust the bias current at least in part by a change in an impedance of one or more of the plurality of circuits.

3. The system of claim 1, wherein the power dissipation control circuit is configured to dynamically adjust the bias current at least in part by a change in gain of one or more of the plurality of circuits.

4. The system of claim 1, wherein the reduction in the power consumption from the battery increases a time interval between required recharging of the battery.

5. A control system to improve a power dissipation from a battery in a receiver of a wireless transceiver of a battery powered portable wireless device, the system comprising:

- a wireless receiver in the wireless transceiver of the portable device configured to receive a wireless signal having a desired signal and an interferer signal, the wireless receiver comprising a plurality of circuits including a signal path comprising at least an amplifier, a filter, and a mixer, and wherein the wireless transceiver comprises at least a circuit configured to determine a signal strength of the interferer signal;

wherein the wireless receiver is designed to function under a worst-case operating condition with a worst-case power dissipation,

wherein one or more of the plurality of circuits in the receiver signal path is configured to enable power dissipation control by dynamically varying a bias current, reducing the power dissipation of one or more of the plurality of circuits in the receiver signal path responsive to a better than worst case operating condition, and

wherein the dynamically varying the bias current results in a corresponding change, reducing the power con-

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sumption from the battery of the battery powered portable wireless device when the operating condition is better than worst case.

6. The system of claim 5, wherein an impedance of one or more of the plurality of circuits of the wireless receiver is configured to be increased to dynamically decrease the bias current.

7. The system of claim 5, wherein an impedance of one or more of the plurality of circuits of the wireless receiver is configured to be varied to dynamically vary the bias current.

8. The system of claim 5, wherein a gain of one or more of the plurality of circuits of the wireless receiver is configured to be changed to dynamically vary the bias current.

9. The system of claim 5, wherein reducing a power consumption from the battery increases a time interval between required recharging of the battery.

10. A system of controlling the power consumption from a battery of a wireless receiver, of a battery-operated transceiver comprising a plurality of circuits, wherein the plurality of circuits comprises at least a signal path and the plurality of circuits are designed to function at a worst-case operating condition, wherein the wireless receiver operates with a maximum power dissipation resulting in maximum power consumption from the battery, wherein to control the power consumption, the system:

receives a signal comprising a desired signal and an interferer signal by the wireless receiver and determines at least a signal strength by at least a circuit of the wireless receiver;

determines a relative strength of the desired signal and the interferer signal; and

responds to a change in the relative strength of the desired signal and the interferer signal by dynamically adjusting a bias current of one or more of the circuits of the wireless receiver when the wireless receiver is functioning at a better than worst case operating condition.

11. The system of claim 10, wherein a bias current of one or more of the circuits in the receiver signal path is dynamically adjusted to result in a reduction in power dissipation in the wireless receiver and a corresponding reduction in the power consumption from the battery.

12. The system of claim 10, wherein a bias current is dynamically adjusted by changing an impedance of one or more of the plurality of circuits of the wireless receiver.

13. The system of claim 10, wherein a bias current is dynamically adjusted by changing a gain of one or more of the plurality of circuits of the wireless receiver.

14. The system of claim 10, wherein controlling power dissipation of the wireless receiver reduces a power consumption from the battery and increases a time interval between required recharging of the battery.

15. A system for power dissipation control in a battery powered portable wireless communication device, comprising:

- a wireless receiver configured to receive a wireless signal comprising a desired signal and an interferer, the wireless receiver comprising a signal path comprising a plurality of circuits designed to operate under a worst-case operating condition when the signal strength of the desired signal is low and the signal strength of the interferer signal is high, wherein the power drain from the battery is maximum;

wherein one or more of the plurality of circuits in the signal path is configured such that a bias current is configured to be dynamically adjusted as the received signal strengths of the desired and interferer signals vary during operation resulting in operating conditions

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that are better than the worst-case operating condition to control the power dissipation in the wireless receiver and to provide a corresponding reduction in a power consumption from the battery of the wireless communication device.

16. The system of claim 15, wherein the bias current is dynamically adjusted by changing an impedance of one or more of the plurality of circuits of the wireless receiver.

17. The system of claim 15, wherein the bias current is dynamically adjusted by changing a gain of one or more of the plurality of circuits of the wireless receiver.

18. The system of claim 15, wherein operating conditions that are better than the worst-case operating condition result when the received signals vary to increase the relative strength of the desired signal with respect to the interferer signal during operation.

19. The system of claim 15, wherein reduction in power consumption from the battery increases a time interval between required recharging of the battery.

20. A battery-powered portable wireless device, comprising:

a wireless transceiver comprising circuits for determining signal strengths of signals received;
the wireless transceiver of the battery-powered portable wireless device further comprising a wireless receiver

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having a signal path comprising a plurality of circuits including at least an amplifier, a filter, and a mixer; wherein the wireless transceiver is configured to receive a wireless signal comprising a desired signal and an interferer signal;

wherein the plurality of circuits of the wireless receiver are designed to function between a worst-case condition when a strength of the desired signal is low and a strength of the interferer signal is high, and a best-case condition when the strength of the desired signal is high and the strength of the interferer signal is low;

wherein the wireless transceiver is configured to determine signal strengths of the desired signal and the interferer signal;

wherein the wireless transceiver is configured to compare the strength of the desired signal relative to the strength of the interferer signal; and

based on the comparison, when the plurality of circuits are functioning at better than the worst-case condition, the wireless receiver is configured to dynamically adjust a bias of one or more of the plurality of circuits in the signal path, thereby controlling power dissipation.

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