A Broad-Band Tunable CMOS Channel-Select Filter for a Low-IF Wireless Receiver

Farbod Behbahani, Weeguan Tan, Ali Karimi-Sanjaani, *Student Member, IEEE*, Andreas Roithmeier, and Asad A. Abidi, *Fellow, IEEE*

***Abstract*—This paper presents a broad-band bandpass filter (BPF) designed as a channel-select filter for wireless applications. It is implemented as a low-pass filter (LPF) in series with a high-pass filter (HPF) for lower power consumption compared to true BPF. Semiscaling of the filter nodes is superior in the wireless receiver over traditional full scaling. The HPF is built with low-pass feedback of an amplifier. The bandwidth is selectable from 625 kHz, 2.5 MHz, or 10 MHz. The filter stopband loss is more than 50 dB extending beyond 100 MHz, and passband ripple less than 2.5 dB. Fabricated in a 0.6-μm CMOS process, it provides a minimum input noise of 16 nV/$\sqrt{\text{Hz}}$ noise with 22.5-dBm out-of-band IIP3, while draining an average 14 mA from 3.3 V.**

***Index Terms*—Bandpass filters, CMOS analog integrated circuits, radio receivers, transconductance-capacitor filters, wireless LAN.**

I. Introduction

FREQUENCY-DIVISION multiple access wireless systems allocate different frequency bands to various applications [1]. Each band contains many channels, from which a given user is assigned one channel. The preselect radio-frequency (RF) filter before the receiver passes all these channels. Then, a sharper channel-select filter in the intermediate-frequency (IF) section isolates the desired channel for demodulation or detection. An off-chip passive filter may be used for this purpose for its high selectivity and wide dynamic range, but at the expense of power consumption in the driving circuits. Also, the receiver (RX) is no longer fully integrated, and one or more filters take precious board space. Furthermore, the fixed bandwidth in a passive filter precludes bandwidth (BW) adaptation.

On-chip active filters, on the other hand, consume power and chip area and limit overall RX dynamic range. Nevertheless, they enable high integration and BW adaptation. The main specifications of an on-chip active filter in a wireless receiver are: 1) its frequency response, including the passband ripple, stopband attenuation, selectivity, and group delay; 2) its dynamic range, including the noise and the linearity; 3) its current drain or power consumption; and 4) the chip area. The linearity of wireless building blocks is usually defined by the third-order intercept point of the (IP3) rather than total harmonic distortion.

Manuscript received December 7, 1999.

F. Behbahani is with Valence Semiconductor Inc., Irvine, CA.

W. Tan, A. Karimi-Sanjaani, A. Roithmeier, and A. A. Abidi are with the Electrical Engineering Department, University of California, Los Angeles CA 90095-1594 USA (e-mail: abidi@icsl.ucla.edu).

Publisher Item Identifier S 0018-9200(00)02659-7.

The channel-select filter must suppress adjacent and all other channels sufficiently to pass only the desired signal to the detector. In most modern wireless systems, it is realized with some combination of analog and digital filters. If there were no analog filtering, the desired signal at the input of the analog-to-digital converter (A/D) will be accompanied by all the other channels in the band, in particular large adjacent channels, which will later be removed in the digital filter. The large interferers, which are eventually of no interest, raise the required resolution of the A/D. In the special case of narrow channels, it is possible to digitize a wide band with a large dynamic range using a bandpass $\Sigma\Delta$ A/D and a large oversampling factor [2], [3]. For example, in [2], an 8-kHz desired channel and adjacent channels are sampled at 16.8 MHz with a peak signal-to-(noise + distortion) ratio of 98 dB. However, for wide-band applications, a large oversampling factor requires impractically high clock rates and is not feasible. Therefore, most interferers must be removed prior to A/D conversion. On the other hand, the sharper the analog filter, the higher the required pole-Q's, and the lower its dynamic range at a given power consumption [4]. An important design tradeoff is how to divide the total required filtering between the analog and the digital sections for best performance. In applications requiring very high selectivity, the optimum lies with partial channel selection in the analog section, followed by a highly selective digital filter.

This paper describes the design and implementation of a variable-BW bandpass filter (BPF). Section II describes the filter structure and Section III covers the optimum transconductance design for our application. Low-pass filter (LPF) and high-pass filter (HPF) design are discussed in Sections IV and V, and Section VI describes solutions to some common-mode feedback problems. The frequency and Q control loops are explained in Section VII. Last, the experimental results are given in Section VIII.

II. Filter Structure

This paper presents a variable BW BPF designed for a fully adaptive wireless local-area network (WLAN) system. The main concern was to integrate as many functions as possible. Fig. 1 shows the block diagram of the RX. The passband is selectable as one of 625 kHz, 2.5 MHz, and 10 MHz, with a stopband that exceeds 100 MHz. The RF preselect filter attenuates incoming signals farther than 100 MHz away from the desired channel. An attenuation of at least 50 dB is desired across the filter stopband. Unlike many wireless systems which use every other channel in a cell, our system uses every channel

0018–9200/00$10.00 © 2000 IEEE

Authorized licensed use limited to: University of Missouri Libraries. Downloaded on January 16,2024 at 20:47:54 UTC from IEEE Xplore. Restrictions apply.

IPR2024-00819
Apple EX1006 Page 1

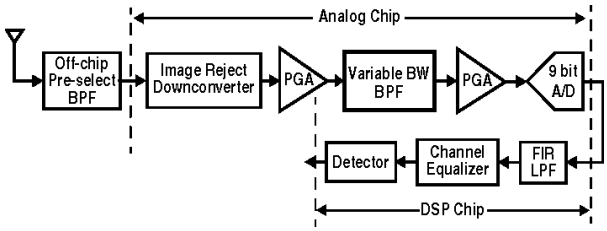


Fig. 1. Block diagram of receiver, showing location of analog filter.

[5] for maximum capacity. To adequately reject the adjacent channel, the filter must be of high order, very likely with high-Q poles. These poles boost filter noise and limit the dynamic range (DR) of the entire RX [4]. Therefore, the analog filter is implemented for partial channel selection, mainly to relax the required A/D DR. A high-order finite impulse response (FIR) digital filter, itself consuming a reasonable power and chip area in the baseband digital signal processor, subsequently isolates the desired channel [5].

With the same BW and selectivity, the higher the filter center frequency, the larger the pole Q's. This translates to higher power consumption for a given dynamic range [4]. Therefore, the filter center frequency should be the lowest possible. A center frequency of 10 MHz was chosen for a bandwidth of up to 10 MHz, which results in a passband spanning 5–15 MHz. A polyphase filter preceding the BPF rejects the image after downconversion over this band [7]. The lower its bandwidth, the more selective an LPF in absolute frequency. Therefore, the lower edge of the filter passband is fixed at 5 MHz for all bandwidths. This also positions the channel of interest beyond the $1/f$ noise corner in the filter. The filter center frequency, which defines the receiver IF, now changes with channel bandwidth.

G_m-C filters are well suited to high frequencies. Accurately modeled parasitic capacitances may be absorbed in the natural grounded capacitors in the filter. This filter is realized as a G_m-C circuit. Like every integrated continuous-time filter, it too requires a tuning loop.

The textbook approach prescribes synthesis of a bandpass (BP) filter from a low-pass (LP) prototype using the bilinear transform. This works well for narrow-band filters [6]. However, when the BW is comparable to the center frequency, such as here, the LP to BP transformation results in a much sharper lower transition (Fig. 2(a)). This is disadvantageous in an active filter, because the associated high-Q poles boost the filter noise at the lower end of the passband. As interferers entering a wireless receiver are equally likely to lie above or below the channel of interest, the upper and lower transition bands should be symmetric. This is realized with an LPF in cascade with an HPF [8], implemented here as a fifth-order elliptic and a third-order Chebychev filter, respectively, to obtain the desired characteristics. Whereas the textbook LP to BP transformation results in an eighth-order bandpass elliptic filter with two conjugate pole pairs of $Q = 7.8$, the largest pole Q in the LPF is 6.9, and 1.3 in the HPF. For a given noise floor, this saves 40% in power consumption compared to a true bandpass filter.

The lower and upper cutoff frequencies may be independently adjusted in the cascade. The HPF fixes the lower edge of the passband to 5 MHz, while the LPF adjusts the overall BW with it upper cutoff [Fig. 2(b)]. If the LPF is designed for the desired selectivity at maximum bandwidth, then selectivity will worsen at lower BW's. For instance, in Fig. 2(b), at a BW of 10 MHz, the transition band of the LPF is equal to the passband. When the LPF poles are scaled to a BW of 2.5 MHz, the transition band expands to twice the passband, worsening selectivity by a factor of two. In the extreme case of 625-kHz BW, the transition band expands to 5.625 MHz, which is 9× the BW. As explained later, the transition band in the actual filter is sharper than this.

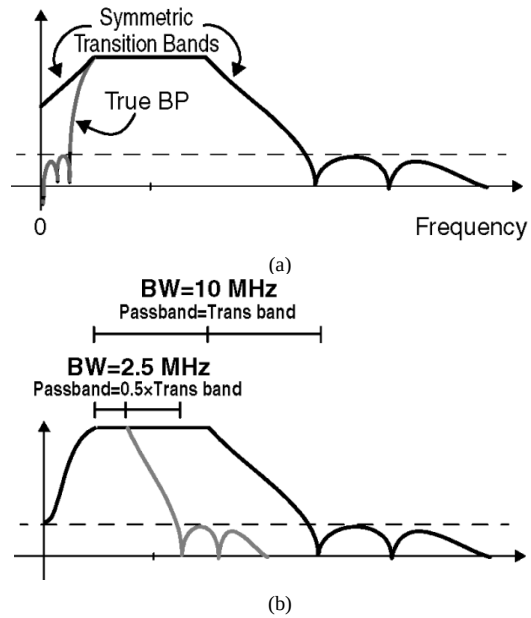


Fig. 2. (a) Broad-band bandpass filter synthesized from cascade of low-pass and high-pass, compared with true bandpass (gray). (b) Selectivity of cascade BPF is worse at lower bandwidths.

III. Transconductors with Wide Dynamic Range

The electrical characteristics of the G_m-C filter strongly depend on the G_m circuit. These characteristics are: noise factor, current efficiency $G_m/I_{\rm bias}$, linearity as measured by intercept point, tuning range, frequency response, maximum signal swing at the input and the output, and dc gain. Limited dc gain generates a pole at the output of a simple G_m-C integrator, which introduces parasitic loss and restricts the maximum pole-Q the filter can implement. Poles and zeros in the G_m stage may generate excess loss or peaking in the filter response [4].

Various transconductor circuits are reported in the literature. The transconductance of a MOS differential pair may be changed with bias current [9]. This method usually does not provide a high linearity, and the tuning range is limited. A MOS resistor may be used as voltage-controlled degeneration [10]. Degeneration improves the linearity of a simple differential pair, but the available triode region of the MOS resistor limits tuning range. At low $V_{\rm GS} - V_t$, small signals can push the degeneration MOSFET into saturation. For higher linearity, the MOS resistor may be padded with a fixed linear resistor, which now limits the range of G_m variation. An improved version of padded MOS degeneration is called soft switching, first

Authorized licensed use limited to: University of Missouri Libraries. Downloaded on January 16,2024 at 20:47:54 UTC from IEEE Xplore. Restrictions apply.

IPR2024-00819
Apple EX1006 Page 2

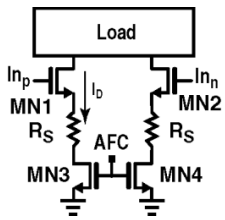


Fig. 3. Variable transconductor (simplified) based on degenerated differential pair.

presented in [11]. In this technique, a ladder of padded MOS degeneration widens G_m tuning range while maintaining good linearity. However, now noise changes with G_m variation, which is not desirable in our application.

Transconductors also use nonlinearity cancellation to improve the dynamic range of the filter [12]–[14]. This requires good modeling of the MOS devices, and cancellation depends on process, temperature, and bias. Transconductors can also be linearized with high loop gain feedback [15], [16], [20]. However, loop gain usually drops at high frequencies and linearity degrades. As the filter may have to remove strong interferers far away from the passband, the resulting poorer IP3 at high frequencies is undesirable.

A. Transconductance Core

The transconductor used in this filter employs variable wide-band resistor degeneration (Fig. 3). MOS resistors MN3 and MN4 operate in the triode region as voltage-controlled degeneration, and are padded with linear resistors in series to improve linearity. To understand this circuit, first consider a MOSFET degenerated by a linear resistor R_s. With constant output signal, the linearity improves by the loop gain $(1+T)$

$$\begin{aligned} 1+T &= 1+g_{mN}\cdot R_S = 1+\frac{2\cdot I_D}{(V_{\rm GS}-V_t)_N}\times R_S \\ &= 1+\frac{2\cdot V_{R_S}}{(V_{\rm GS}-V_t)_N} = \frac{2\cdot(V_G-V_t)}{V_G-V_t-V_{\rm Rs}}-1 \end{aligned} \quad (1)$$

where $V_{\rm Rs}$ is the bias voltage across the resistor. This shows that the linearity of the G_m stage is a function of V_G, the input bias voltage. The total available headroom, set by the supply voltage, is divided across the input stage (transconductance core, MN1-4 and Rs) and the load. The higher the voltage drop across the input stage, the higher the linearity. At constant V_G, a larger $V_{\rm Rs}$ results in stronger feedback (higher T), and therefore better linearity. On the other hand, the current efficiency of the G_m stage is

$$\begin{aligned} \frac{G_m}{I_d} &= \frac{1}{I_d}\cdot\frac{g_{mN}}{1+R_S\cdot g_{mN}} \\ &= \frac{1}{I_d}\cdot\frac{(2I_d)/(V_{\rm GS}-V_t)_N}{1+(2I_dR_S)/(V_{\rm GS}-V_t)_N} \\ &= \frac{1}{\frac{(V_{\rm GS}-V_t)}{2}+V_{\rm Rs}}. \end{aligned} \quad (2)$$

Strong feedback (large $V_{\rm Rs}$) raises the bias current necessary for the same transconductance. Fig. 4 plots the simulated tradeoff between the current efficiency $(G_m/I_{\rm bias})$ and linearity of the G_m stage. In the first case, $V_{\rm GS}-V_t$ is kept constant at 0.6 V and

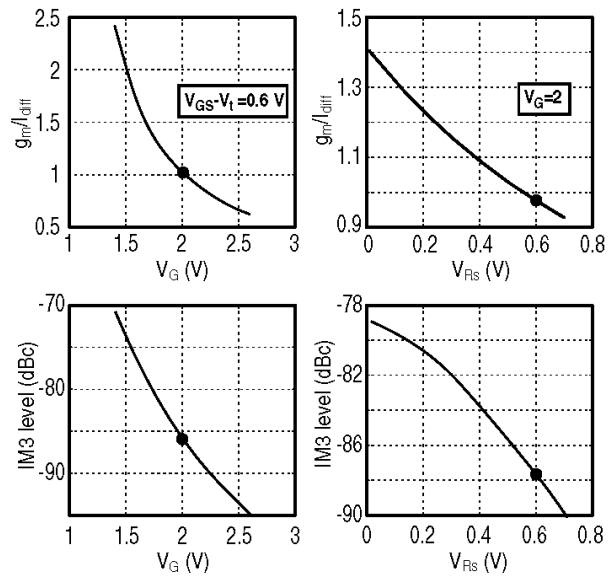


Fig. 4. Current efficiency and linearity of transconductor versus bias voltage and degeneration. Dots show the bias values used.

V_G is swept. In the second case, V_G is constant at 2 V and $V_{\rm Rs}$ is swept. Linearity is simulated with two tones, each 0.2 $V_{\rm pp,diff}$. This design is centered at V_G of 2 V and $V_{\rm Rs}$ of 0.6 V. It should be noted that as the dc degeneration voltage gets larger, the body bias of the field-effect transistor (FET) increases and its $V_{\rm GS}-V_t$ is lowered. Both latter effects create more nonlinearity in the circuit. Therefore, output linearity improves less than the increase in loop gain.

For greater voltage headroom, the bias current source is removed from under the transconductance differential pair. Simulations show that this improves linearity by up to 10 dB. However, the G_m stage now amplifies a common-mode input with the same gain as a differential-mode input. Eventually, true differential sensing of the filter output will strip off the common mode. However, imbalance in the differential circuits due to dc offsets or mismatch causes common-mode to differential conversion. This is precarious, because now parasitic common-mode feedback through the substrate and supply lines may induce differential oscillation in the high gain IF strip. The IF circuits were laid out with great care to symmetrically position individual transistors, and even entire circuit blocks on a center line. This minimizes systematic offsets, and symmetrically couples both halves of differential circuits to the substrate.

B. Active Load

The filter simulates inductors with gyrators, which consist of pairs of transconductors in differential negative feedback. The transconductor inputs and outputs bias at the same voltage. Assuming this is 2 V, and allowing for signal swing of 0.8 $V_{\rm PP}$, the headroom for the active load with 3.3 V supply is

$$\begin{aligned} \text{Load headroom} &= V_{\rm DD}-\left(V_{\rm Out,bias}+\frac{V_{O,\rm pp}}{2}+V_{\rm margin}\right) \\ &= 3.3-\left(2+\frac{0.8}{2}+0.3\right)=0.6\ \text{V}. \end{aligned}$$

Authorized licensed use limited to: University of Missouri Libraries. Downloaded on January 16,2024 at 20:47:54 UTC from IEEE Xplore. Restrictions apply.

IPR2024-00819
Apple EX1006 Page 3

The active load consists of a single PMOSFET biased with $V_{\rm DS}$ equal to the full 0.6-V headroom. For an acceptable impedance, the PMOSFET length is chosen as 4.5 μm and the NMOSFET length as 3 μm. In contrast, the PMOS in a cascode load fitted into the same bias voltage would contribute 50% higher noise spectral density.

C. Noise, Linearity, and Power Consumption

With the above bias voltages, the $G_m/I_{\rm bias}$ of the transconductance is about 1 (Fig. 4). The noise performance of the transconductor circuit is specified by an excess noise factor Γ defined as follows:

$$\hat{i}_{\rm nO}^2 = 4kTT \times G_m. \tag{3}$$

An expression for the output noise in the transconductor circuit is

$$\hat{i}_{\rm nO}^2 = 4kT \times \left\{ \left(\frac{1 + g_{mN} \cdot R_S - \frac{\gamma}{2}}{g_{mN}} \right) \cdot \left(\frac{g_{mN}}{1 + g_{mN} \cdot R_S} \right)^2 + \gamma \times g_{mP} \right\} \tag{4}$$

where $\gamma = 2/3$ is the noise factor of a long-channel FET.

Since $1 + g_{mN} \cdot R_S > \gamma/2 = 1/3$, then

$$\hat{i}_{\rm nO}^2 \cong 4kTG_m \times \left(1 + \gamma \times \frac{g_{mP}}{G_m}\right). \tag{5}$$

Therefore

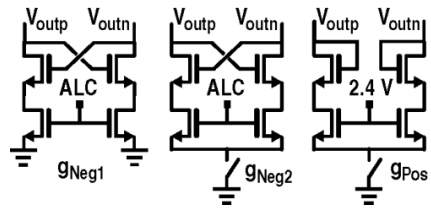
$$\Gamma = 1 + \gamma \times \frac{g_{mP}}{G_m} = 1 + \gamma \times \frac{g_{mP}/I_d}{G_m/I_d} = 1 + \gamma \times \frac{1}{G_m/I_d} \times \frac{2}{(V_{\rm GS} - V_t)_P}. \tag{6}$$

For more linearity, the loop gain must be higher, which means lower G_m/I_d. Now the noise overhead of the active load is significant. Furthermore, the lower the headroom on the active load transistor, the higher its noise. An interesting alternative is the CMOS inverter-type transconductor [17], which lowers excess noise because both sources of noise (NMOS and PMOS) also contribute signal transconductance. However, at low supply voltages, this transconductor is not linear enough for this filter.

D. Parasitic Capacitances

The large FET's in the transconductor impose a large gate capacitance, with two adverse effects. First, the $C_{\rm gate}$, which appears in parallel with the filter tuning capacitors, can cause large deviations in the filter frequency response. Second, $C_{\rm gd}$ generates a zero in the right-half s-plane at frequencies close to the passband edge of the LPF, and the resulting phase shift may peak the frequency response in the passband

$$\omega_Z = G_m/C_{{\rm gd},N} = \frac{g_{mN}}{C_{{\rm gs},N}} \times \frac{1}{1 + g_{mN} \cdot R_S} \times \frac{C_{{\rm gs},N}}{C_{{\rm gd},N}} = \frac{\omega_{T,N}}{\text{Loop Gain}} \times \frac{C_{{\rm gs},N}}{C_{{\rm gd},N}}. \tag{7}$$



(a) (b) (c)

Fig. 5. (a) Negative conductance stage. (b) Auxiliary switched negative conductance. (c) Switched positive conductance.

TABLE I
RANGE OF TOTAL NEGATIVE CONDUCTANCE AT THE OUTPUT

N_{Pos}	N_{neg2}	Range
on	off	$0 \rightarrow -1.5\times G_m/40$
off	off	$-G_m/40 \rightarrow -G_m/16$
off	on	$-G_m/20 \rightarrow -G_m/8$

Long channel devices suffers from low ω_T. In addition, higher loop gain lowers the zero frequency. Nevertheless, $\omega_Z = 2\pi \times 2.2$ GHz in this transconductor lies more than two decades higher than the passband edge, causing negligible parasitic phase shift.

E. Increasing dc Gain

Simulations show that the dc voltage gain of the basic G_m stage is about 20 when driving a capacitor load. As the output impedance in the HSPICE BSIM2 MOS models at the time of the design was not trustworthy, the design allows for a spread of 50% in output impedance. A gain as low as ten would produce unacceptable passband loss in the filter frequency response. To compensate this, a negative conductance stage, implemented by a cross-coupled transconductor, is put in parallel with the output of the main transconductor [Fig. 5(a)]. Using $|g_{\rm Neg}| = |-G_m/8|$ can compensate a dc gain as low as eight. An auxiliary switchable negative conductance $g_{\rm Neg2}$ is in parallel with this [Fig. 5(b)]. At the other extreme, if the net output impedance becomes negative due to overcompensation, it should be possible to set $g_{\rm Neg}$ to zero. However, sweeping the control voltage ($V_{\rm ALC}$) over its full range from 2.4 to 3.2 V changes $g_{\rm Neg}$ by a maximum of 2.5×. To obtain a net output $g_{\rm Neg}$ of zero, a switchable positive conductance stage is inserted in parallel [Fig. 5(c)]. $g_{\rm Pos}$ is constant and equal to $G_m/40$. Each $g_{\rm Neg}$ stage varies between $-G_m/40$ and $-G_m/16$. Table I shows the range of total negative conductance at the output for various switch positions. Simulations show that $g_{\rm Neg1}$ alone covers the nominal case. At the price of a slightly more complicated control loop, this approach consumes about 3× less power and is less nonlinear and noisy than if of one $g_{\rm Neg}$ and one $g_{\rm Pos}$ were required to cover the full range of process variations.

F. Final G_m Circuit

The final G_m stage shown in Fig. 6(a) is designed for a low-noise version ($G_{m,H}$) of the LPF. The total filter consumes 50 mA from 3.3 V. The receiver also uses another LPF with the

Authorized licensed use limited to: University of Missouri Libraries. Downloaded on January 16,2024 at 20:47:54 UTC from IEEE Xplore. Restrictions apply.

IPR2024-00819
Apple EX1006 Page 4

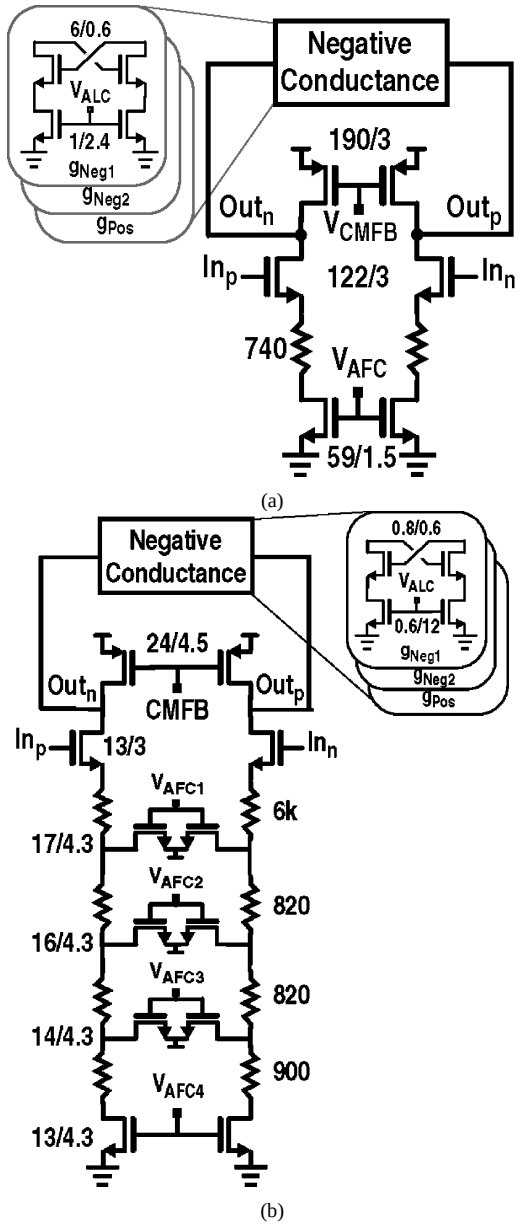


Fig. 6. Variable transconductor (actual), as used in (a) low-noise LPF and (b) low-power LPF and HPF.

same frequency response and linearity, which consumes 10× lower power $(G_{m,L})$ but with a 10-dB higher noise floor. All the transconductances and capacitors in this filter are scaled down by a factor of ten. The low power transconductance is shown in Fig. 6(b). For a reason that will be explained later, $G_{m,L}$ should be tunable by more than 50%, while the $G_{m,H}$ need only vary by 13%. Compared to the high power transconductor, $G_{m,L}$ includes several stages of variable degeneration to expand range without giving up linearity. At any time, only one of the degeneration MOSFET's is on, and its gain control voltage varies from 1.6 to 3.3 V. The range of degenerated transconductance overlaps across the MOSFET's in the ladder. This guarantees continuous sweep of 50% in transconductance. Table II summarizes the important characteristics of the final transconductors.

TABLE II
CHARACTERISTICS OF THE FILTER TRANSCONDUCTANCE

	Hi/Low Power
G_m nominal	660/66 (μS)
g_m/I_{diff}	1
Noise factor, γ	2.3
g_m variation	13%/50%
Input/Output swing	1.6 Vpp,diff
IIP3 (ref. 100 Ω)	29 (dBm)

IV. LOW-PASS FILTER DESIGN

The low-pass filter's cutoff frequency, which defines the upper edge of the bandpass filter, is selectable as 5.65, 7.5, and 15 MHz. A passband ripple as large as 3 dB is tolerable, but the stopband attenuation should be higher than 50 dB. Depending on the channel conditions, either the low-power or the low-noise LPF is selected. Each LPF is based on a doubly terminated LC ladder, which is more forgiving of deviations in component values from the ideal. This property is particularly valuable because in this filter, the transconductor FET's themselves contribute substantial but poorly modeled capacitance, with a different dependence on process variations than the linear capacitors.

A. Filter Structure

The prototype filter is designed for 1-dB passband ripple, 60-dB stopband attenuation, 15-MHz passband edge frequency, and a transition band narrower than the passband. A fifth-order elliptic filter meets these specifications. The floating inductors are replaced with gyrator-C circuits. The capacitances and transconductors of the filter are built from unit capacitors (C_u) and unit G_m stages $(G_{\rm mu})$ [6]. The ratio between the filter node capacitors and the transconductors should be ideally constant over temperature and process. Parasitic capacitors at the nodes arise mainly from the drain junctions and the NMOS gates. They vary differently with fabrication process than the main linear capacitors. In the ith node, the parasitic capacitance from the transconductors $C_{\rm Pi}$ is absorbed in the total node capacitance C_i

$$C_i = C_{\rm Pi} + n_i \cdot C_u. \tag{8}$$

Since the ratio $C_{\rm Pi}/n_i \cdot C_u$ varies from node to node, if $C_{\rm Pi}$ is a significant part of C_i it disturbs the designed ratio of node capacitors, and thus the filter frequency response. At high bandwidth settings, $C_{\rm Pi}/n_i \cdot C_u$ is largest. C_P comprises the input and output capacitance of G_m, which are 1.2 and 0.5 pF for $G_{m,H}$, respectively. Table III shows the standard deviation of the different types of the capacitance. These spreads cause two problems. First, the passband ripple increases. This happens to be not very important in the intended use. Second, the master control loop and slave filter do not match well. The consequences of this are discussed later.

Authorized licensed use limited to: University of Missouri Libraries. Downloaded on January 16,2024 at 20:47:54 UTC from IEEE Xplore. Restrictions apply.

TABLE III
STANDARD DEVIATION OF THE DIFFERENT TYPES OF THE CAPACITANCE OVER VARIOUS RUNS IN OUR PROCESS

	Lin. Cap.	$C_{G,PMOS}$	$C_{G,NMOS}$	$C_{D,PMOS}$	$C_{D,NMOS}$	Gate Cap./ Lin. Cap.
Average (fF)	2264	3392	3577	932	536	
Rel. σ (%)	2.3	3.2	3.5	4.9	3.8	1.8

TABLE IV
PEAK GAIN TO THE INTERNAL NODES, AND THE POWER MERIT FOR THREE TYPES OF SCALING

	Node Max. gain (dB)				Power merit
	1	2	3	4	Relative $I_{bias}.V^2_N$ (dB)
No Scaling	4	8.7	8.2	4.5	0
Full Scaling	0	0	0	0	6.5
Semi Scaling	4	5.1	4.5	4.7	1.4

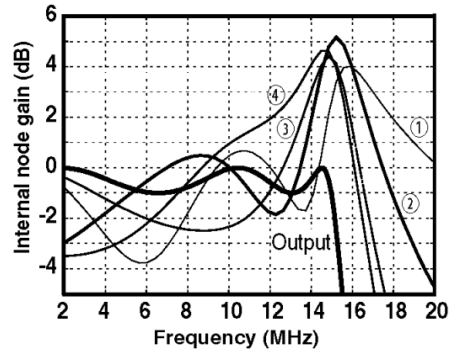


Fig. 7. Gain versus frequency to the filter internal nodes (shown numbered) after semiscaling.

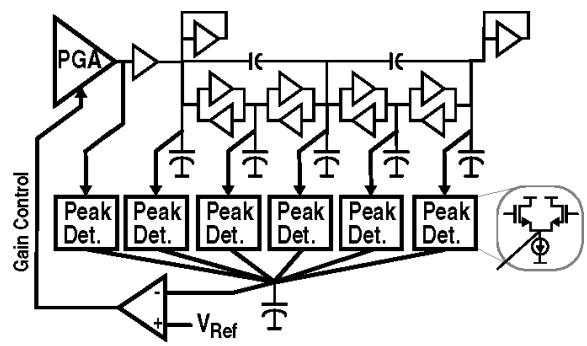


Fig. 8. Prefilter AGC prevents saturation at internal nodes.

B. Filter Amplitude Scaling

There are two steps in scaling an active filter to maximize dynamic range: amplitude scaling, and noise scaling. In an unscaled filter, the input signal may be amplified more to internal nodes than to the filter output, the peak gain at a frequency close to the passband edge. An input signal with strong power spectral density at this frequency can drive the internal transconductors into saturation. The textbook solution is to scale the filter by the $\mathbb{L}_\infty$ norm. That is, all node impedances are scaled so as to make the peak gain from the input to all the filter nodes to 0 dB across the entire passband [6]. As a consequence, gain from the major noise sources in the filter to the output also rises, increasing the input-referred noise of the filter. In a wireless receiver, the higher in-band noise of an $\mathbb{L}_\infty$-scaled filter always weakens the signal-to-noise ratio of the desired channel, whereas in an unscaled filter, only an interferer that happens to lie close to the passband edge, or a very strong desired signal drives internal nodes into saturation. In practice, strong interferers appear with equal likelihood across the band, and only sometimes lie close to the passband edge. Furthermore, a prefilter automatic gain control (AGC) can lower a strong in-band signal. Therefore, a partly scaled filter may be preferred in a wireless receiver because its lower noise is always desirable.

This filter is scaled as follows. While scaling gain to the internal filter nodes, Σg_m, which represents the power consumption, and the output noise are monitored. Initially, scaling lowers the peak gain to the internal nodes faster than it causes noise to rise. With further scaling, however, noise increases substantially. Table IV shows the peak gain to the internal nodes, and the power figure-of-merit for three stages in scaling. Discussion in the next section justifies choice of this figure of merit. To begin with, in the unscaled filter the largest gain to an internal node is 8.7 dB, while the end-to-end filter peak gain is 0 dB in the passband. Scaling the peak down to 5.1 dB lowers the figure of merit by 1.4 dB, which means that dynamic range improves. Further scaling to level all the peak gains to 0 dB lowers the figure of merit $(I_{\text{bias}} \cdot V^2_{O,n})$ by 5.1 dB, which is almost the same as the decrease in peak gain. However, the resulting higher noise always degrades sensitivity. With full scaling, therefore, average dynamic range is worse.

As a result of these trends, this filter is only partly scaled. Fig. 7 shows the frequency response of the filter nodes after semiscaling. To prevent premature saturation of G_m stages, the scheme in Fig. 8 detects signal peaks at all the nodes. If the peak value exceeds some limit, the prefilter variable-gain amplifier lowers the input signal.

C. Filter Noise Scaling

Following scaling for gain, the filter is scaled for the noise. Scaling up all the G_m stages and the filter capacitors together increases the bias current but proportionally lowers output noise spectral density $(V^2_{O,n})$. The power merit and frequency response of all nodes remain unchanged. This is why $I_{\text{bias}} \times V^2_{O,n}$ is a fundamental figure of merit. The procedure for noise scaling starts by identifying those filter nodes that contribute significantly to total noise but whose associated

Authorized licensed use limited to: University of Missouri Libraries. Downloaded on January 16,2024 at 20:47:54 UTC from IEEE Xplore. Restrictions apply.

IPR2024-00819
Apple EX1006 Page 6

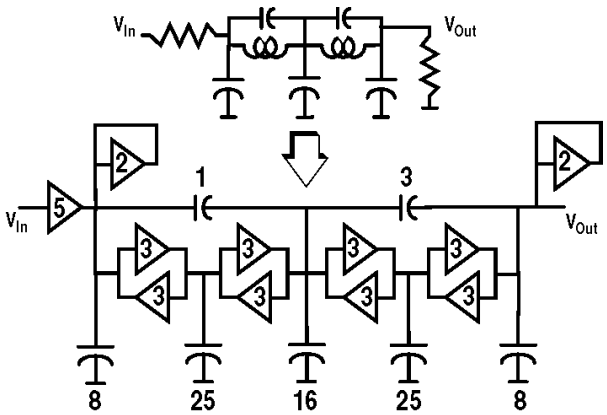


Fig. 9. LPF ladder prototype and its active G_m-C realization. Transconductors and capacitors are scaled to small multiples of unit values.

transconductors drain relatively small bias current. Scaling up these nodes does not impact power consumption much, but it lowers noise significantly.

Noise scaling is optimized as follows. $N_{\rm Tot}$, the total output noise power spectral density, is calculated, where $N_{\rm Oi}$ is the noise that the ith G_m stage contributes to the filter output

$$N_{\rm Tot} = \sum_{i=1}^{K} N_{\rm Oi}. \tag{9}$$

As all G_m stages use the same circuit, then

$$N_{\rm Oi} \propto \frac{1}{G_{\rm mi}} \propto \frac{1}{I_i} \rightarrow N_{\rm Oi} \cdot I_i = \alpha_i \tag{10}$$

where $G_{\rm mi}$ and I_i are the transconductance and the bias current of the ith stage and α_i is a constant set by the circuit topology and $V_{\rm GS} - V_t$. Noise scaling aims to minimize the noise with a constant total bias $I_{\rm Tot}$

$$N_{\rm Tot} = \sum_{i=1}^{K} \frac{\alpha_i}{I_i} = \sum_{i=1}^{K-1} \frac{\alpha_i}{I_i} + \frac{\alpha_K}{I_{\rm Tot} - \sum_{i=1}^{K-1} I_i} \tag{11}$$

$$\frac{\partial N_{\rm Tot}}{\partial I_i} = 0 \rightarrow \frac{N_{\rm Oi}}{I_i} = \frac{N_{\rm Tot}}{I_{\rm Tot}} = \text{Constant}. \tag{12}$$

Thus, for the lowest $N_{\rm Tot}$ at a fixed $I_{\rm Tot}$, all the G_m stages should be scaled to the contribute the same noise to the filter output per unit bias current. However, G_m stages whose outputs connect together are not independent and must be scaled together. Ideally, the optimum scale factor β_i for the ith G_m stage is

$$\beta_i = \sqrt{\frac{N_{\rm Oi}/I_i}{N_{\rm Tot}/I_{\rm Tot}}}. \tag{13}$$

In this way, the filter is scaled for both gain and noise. Fig. 9 shows the final component sizes after scaling and roundoff to small integers.

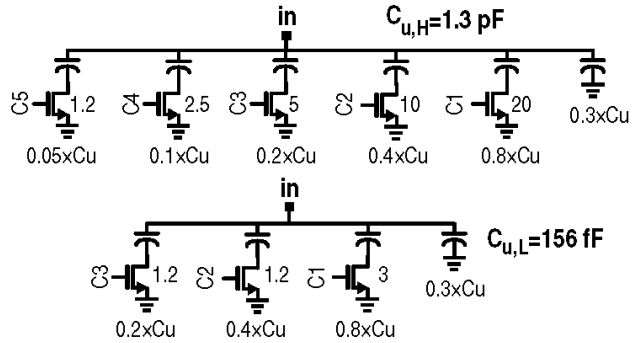


Fig. 10. Grounded unit capacitor in low-noise and low-power LPF. Switch widths are shown; all lengths are minimum. Floating capacitors (not shown) consist of same array, activated by complimentary switches.

D. Switched Capacitor Array

The cutoff frequency of the adaptive LPF must vary from 5.7 to 15 MHz. Allowing an additional ±25% to compensate for process and temperature variations, the tuning range encompasses 3.8–18.8 MHz, requiring $G_{\rm mu}/C_u$ to vary by 5×. If $G_{\rm mu}$ alone is tuned over this range, the passband noise spectral density rises by 7 dB at the lowest frequency. On the other hand, if C_u is varied, the noise spectral density stays constant.

Each capacitor consists of a subarray of switched capacitors. The switch on-resistance introduces some loss in the circuit, lowering the effective Q of the capacitor (Q_c). Filters with higher Q poles require higher Q_c. Since $Q_c = 1/(r_{\rm on}\omega C)$, high-frequency poles need larger switches. Switch sizes were chosen by modeling resistors in series with C_u, and exploring the impact of limited Q_c on filter response. Fig. 10 shows the C_u for grounded and floating capacitors used in high-power and low-power LPF's. The low-power LPF uses fewer switched capacitors, because the nominal capacitance is 10× smaller and even the smallest switch now introduces a parasitic, which compresses the capacitance swing between switch ON and OFF. The switched capacitor ratio is about 8% for the high-power capacitors, and 30% for the low power. To guarantee continuous coverage of G_m/C, G_m must span a wider range than the switched capacitor ratio. Therefore, the G_m variation for the high power and the low power was chosen to be 13% and 50%, respectively.

V. High-Pass Filter Design

The HPF transition band should be similar to the LPF transition band. A third-order Chebychev high-pass satisfies this condition. However, there is a practical problem in a direct implementation of the HPF. Although no filter capacitor connects to ground, inevitable parasitics to ground produce rolloff at high frequencies. When using this G_m stage, the parasitic upper cutoff in the HPF lies close to the highest designed cutoff in the LPF (15 MHz). This is unacceptable.

This HPF is implemented by applying low-pass feedback to 45-dB switchable gain stage [Fig. 11(a)]. This follows the LPF. A transconductance stage (G_L) with input connected to its output through a low-pass biquad is inserted in parallel with a fixed load resistor. At high frequencies, there is no feedback, and G_L produces no signal current. As G_L's output resistance is much higher than R_L, the gain at high frequency is $G_{\rm mA} \times R_L$.

Authorized licensed use limited to: University of Missouri Libraries. Downloaded on January 16,2024 at 20:47:54 UTC from IEEE Xplore. Restrictions apply.

IPR2024-00819
Apple EX1006 Page 7

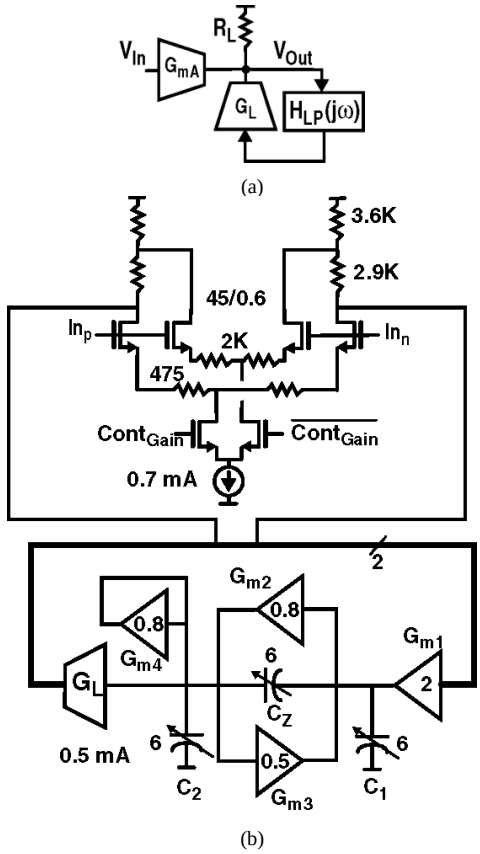


Fig. 11. (a) HPF consists of amplifier with low-pass feedback at output load. (b) Details of HPF, showing switched gain transconductor and LPF biquad in feedback with feedforward compensation capacitor.

At low frequencies, however, the biquad applies unity gain feedback causing the transconductor to appear as a resistance $1/G_L$. When $R_L \gg 1/G_L$, overall dc gain G_{mA}/G_L is smaller. In the actual design, the gain varies from 0 dB at dc to 15 dB beyond 5 MHz, implementing a high-pass amplifier. The passband gain is switchable between 0 and 15 dB with the degeneration resistors in G_{mA}.

The feedback loop's noise contribution is only important for in-band signals, that is, for signals lying in the stopband of the low-pass feedback. The feedback elements generate an output noise with a spectral density proportional to G_L. In the high gain mode, with dc gain of 0 dB, $G_{\mathrm{mA},H} = G_L$. As the output current noise of these two blocks is proportional to their transconductance, G_L adds 3 dB to the input noise of the amplifier. In the low gain mode, $G_{\mathrm{mA},L}$ is 15 dB lower, and now G_L contributes most of the output noise. However, low postfilter gain is only selected when the signal is large, in which case the higher noise is not much of concern.

Now consider nonlinearity due to loop components. The LPF and G_L give rise to in-band third-order intermodulation (IM3).

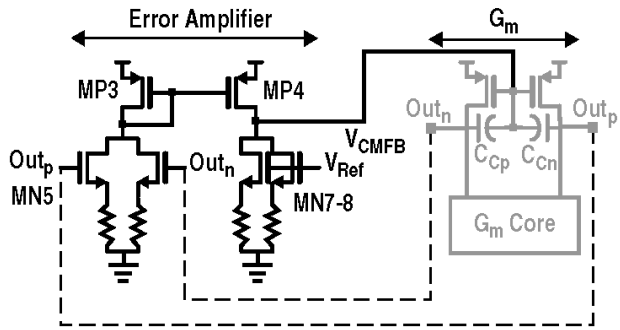


Fig. 12. Common-mode feedback amplifier.

The BW of the feedback LPF is 1 MHz. To generate IM3 at frequencies higher than 5 MHz, at least one of the tones must lie in the transition band of the low-pass feedback, and this is significantly attenuated before it reaches the input of G_L. Hence, G_L itself cannot generate significant IM3 at frequencies above 5 MHz. Any in-band IM3 that the low-pass feedback generates lies in its stopband and is attenuated. Thus, loop nonlinearity does not affect the overall HPF.

Next consider stability. The low-pass biquad induces large phase shift in the loop. Although a high-order feedback filter would sharpen the HPF transition band, it makes loop compensation impossible. This is why a second-order LPF is used. Fig. 11(b) shows the block diagram of this HPF biquad stage. Feedforward capacitor C_Z creates a transmission zero to compensate the loop with better than 60° phase margin. The transfer function is shown in (14) at the bottom of the page. Three identical stages in cascade produce a comparable transition band to the main LPF. The HPF uses the same G_{mu} stage and C_u as the low-power LPF. Taking into account the zero, the final HPF is of third order.

VI. Common-Mode Feedback

A common-mode feedback (CMFB) sets the input and output bias in a fully differential transconductor. Associated with each transconductor is the CMFB circuit (Fig. 12). MN5-8 form the common mode detector and error amplifier, and MN5-6 generate a sum current at their drains, which depends on the G_m stage output CM voltage. MN7-8 compare this with the current generated by V_{REF}. The output voltage (V_{CMFB}) feeds back to the gates of the PMOS load transistors in the main transconductor, driving the output bias of the G_m stage to V_{REF}. Resistor degeneration linearizes the error amplifier to suppress bias shifts caused by a large differential sinewave at the G_m output due to second-order distortion in the FET's.

There are some special problems of CMFB in multiple differential transconductors connected in a filter. At many places in the LPF, the outputs of G_m stages connect together. Independent CMFB in each stage will create multiple feedback loops

$$\frac{V_O}{V_I}(s) = \frac{G_{m1} \cdot G_{m2} \cdot \left(1 + \frac{C_Z}{G_{m2}} s\right)}{[(C_1 + C_2)(C_2 + C_Z) - C_Z^2] \cdot s^2 + [G_{m4}(C_1 + C_Z) + (G_{m3} - G_{m2})C_Z] \cdot s + G_{m2} \cdot G_{m3}} \tag{14}$$

Authorized licensed use limited to: University of Missouri Libraries. Downloaded on January 16,2024 at 20:47:54 UTC from IEEE Xplore. Restrictions apply.

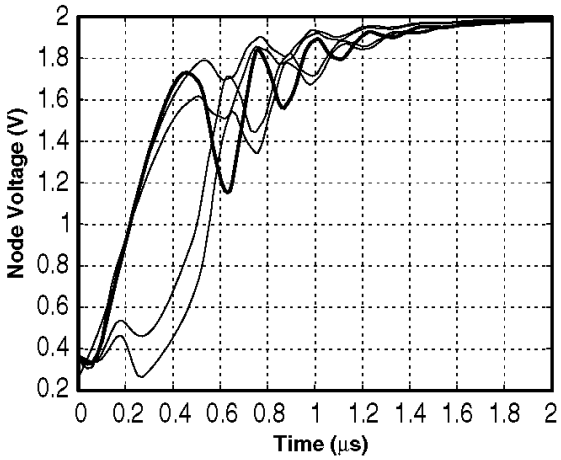


Fig. 13. Common-mode step response at filter's internal nodes.

competing to force the same CM voltage at the shared node. In the presence of mismatch or offsets, this may drive some of the active load PMOSFET's into triode or cutoff. To prevent this, all active loads connecting to an output node are merged and driven by a single CMFB.

Two comparable poles in the two-stage loop amplifier erode phase margin. Miller multiplied capacitors $C_{\rm Cp}$ and $C_{\rm Cn}$ between $V_{\rm OUT}$ and $V_{\rm CMFB}$ in Fig. 12 compensate the loop. To differential transconductor inputs, the node CMFB is at a virtual ground, so that these C_C's are connected between the output and ground and absorbed into the actual grounded capacitor which sets the filter poles.

The large common-mode gain in this transconductor poses a problem in gyrator loops. Although the loop is connected in negative feedback for differential signals, it is always in positive feedback for common mode. This can only be guaranteed stable if the negative CMFB gain overcomes the positive feedback gain in the gyrator loop. Due to the local CMFB, the CM closed loop output impedance presented to the G_m stage is

$$R_{O,C} = \frac{R_{O,O}}{(1 + g_{m,P} \cdot R_{O,O} \times \text{Gain}_{\text{ErrAmp}})} \tag{15}$$

where $R_{O,O}$ is the open-loop output impedance of G_m, $R_{O,O} = r_{\rm op}||(1 + g_{mN} \cdot R_s)r_{\rm on}$. The net common-mode loop gain is

$$T_{\text{Global}} = G_m \cdot R_{O,C} \approx \frac{1}{g_{m,P} \cdot R_s \times \text{Gain}_{\text{ErrAmp}}}. \tag{16}$$

This quantity is always less than one, which means that at dc the global loop is always stable. At high frequencies, the Miller-multiplied C_C shorts the input and the output of the PMOS active load devices, lowering the output impedance to $1/g_{\rm mP}$. Since $G_m < g_{\rm mP}$ (as explained in Section III), the positive feedback loop gain remains less than one. In the actual circuit, stability of the gyrator loops requires C_C to be 3× value required for stability of the local CMFB loops.

It is difficult to simulate the phase margin for this multiple loop circuit using only ac analysis in SPICE. Transient analysis of, for instance, the response to a large step in CM $V_{\rm REF}$ from 0 to 2 V gives more insight. Fig. 13 shows the simulated step response test for all the filter nodes in the worst case, when G_m is maximum and C_u minimum.

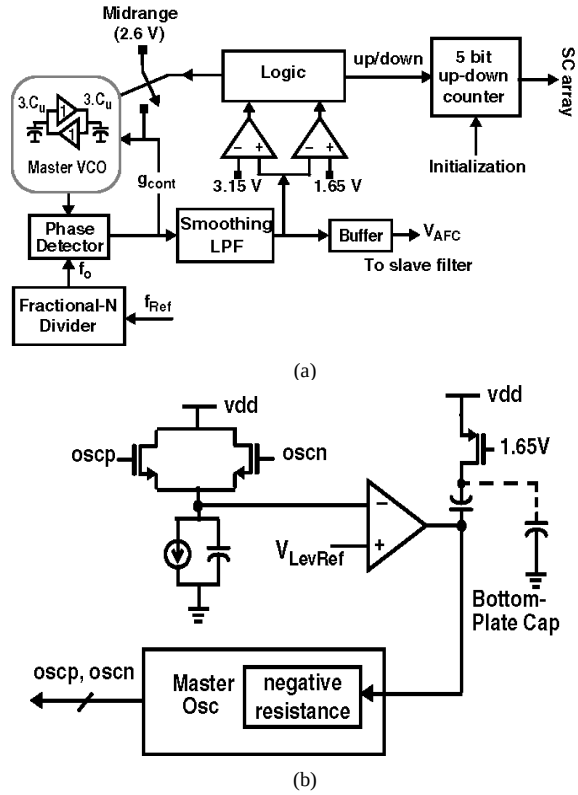


Fig. 14. (a) Automatic frequency control loop. (b) Automatic level control loop.

VII. Frequency and Q-Tuning Loops

Tuning loops set the ratio $G_{\rm mu}/C_u$ (for frequency response) and the output negative resistance (for pole Q). The literature covers many different methods for the design of these loops [18]. This filter uses a master–slave vector-locked loop (VLL). With the desired value of $G_{\rm mu}/C_u$, a voltage-controlled oscillator (VCO) consisting of an undamped gyrator-based resonator oscillates at a known frequency f_0 enforced by an automatic frequency control (AFC) loop. The VCO also controls Q. In the event of a net negative resistance at the output of the G_m, the amplitude of oscillation grows until it pushes the transistors into triode region. On the other hand, the amplitude decays if the net resistance is positive. Only a zero net output conductance produces stable linear oscillation at a known amplitude. An automatic level control (ALC) adjusts the negative resistance. As all control loops operate similarly, only the phase-locked loop (PLL) for the high-power filter is described below.

A. AFC Loop

The AFC [Fig. 14(a)] is a mixed analog–digital loop, consisting of an analog phase detector and smoothing filter, digital comparator block, logic, reset circuits, and the 5-bit up–down counter.

$V_{\rm AFC}$, the continuous output of the AFC loop, biases the gates of the active degeneration FET's in the G_m block (Fig. 6)

Authorized licensed use limited to: University of Missouri Libraries. Downloaded on January 16,2024 at 20:47:54 UTC from IEEE Xplore. Restrictions apply.

IPR2024-00819
Apple EX1006 Page 9

and sets the transconductance. The digital word from the 5-bit counter selects the switches in C_u (Fig. 10). In the low-power filter, the digital section routes $V_{\rm AFC}$ to one of the active degeneration MOSFET's for coarse discrete tuning.

The PLL consists of a conventional phase frequency detector and a charge pump, with a simple series RC filter for compensation. As $V_{\rm AFC}$ changes from 1.65 to 3.15 V, it raises the transconductance and the VCO frequency by 13%. However, as mentioned in Section IV-D, a 500% range is required for G_m/C_u. Switching the capacitors in C_u gives the rest.

The AFC works as follows. Assume that the frequency of VCO $(f_{\rm VCO})$ is initially much lower than the frequency at the output of the divider (f_0). To increase f_0, the PLL drives up $V_{\rm AFC}$ until it hits the upper limit of 3.15 V. This trips a comparator, which decrements the counter. This switches C_u to a lower value, causing a jump up in the frequency of oscillation. The reverse happens when $f_{\rm VCO}$ is initially higher than f_0, and $V_{\rm AFC}$ crosses the lower threshold of 1.65 V. Since the PLL is second-order and slightly underdamped, the control voltage rings as it approaches the final value. Although $V_{\rm AFC}$ finally settles to some value between 1.65 and 3.15 V, it might overshoot this range at the peaks of the ringing waveform. An LPF smooths the PLL control voltage before comparison with the trip levels.

Feedback from the counter to the comparator/logic prevents overflow (underflow) when the C_u is minimum (maximum), corresponding to the word 00 000 (11111). To lower settling time, the counter is initialized with the steady-state value expected from simulations. Then, the control voltage is initialized midway between the upper and lower limits. This guarantees a short settling time for the PLL.

B. Tuning AFC Loop to Three Different BW's

The AFC must be able to tune the filter to three widely separated frequencies. One possibility is to scale the $G_{m,\rm VCO}$ relative to $G_{\rm mu}$, so that the oscillator remains locked to a fixed reference frequency while G_m/C in the filter steps to the desired values. This approach is not practical if the G_m stage, as here, suffers from significant parasitics, which will upset the ratio accuracy between master and slave over the wide range of filter settings. Instead, the VCO replicates the $G_{\rm mu}$ and C_u in the main filter, and is locked to synthesized reference frequency proportional to the filter BW (Fig. 20).

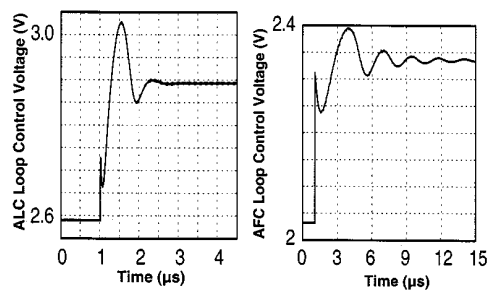
As in any master–slave scheme, the main concern is how accurately the VCO oscillation frequency tracks the filter BW. To simulate this, the capacitors in an ideal G_m-C filter and VCO are expressed as combinations of C_i (at the G_m input), C_o (at the G_m output), and C_u (unit linear capacitors). Then, based on the data in Table III, each capacitor is skewed from nominal to simulate mismatch among different capacitor types (this does not simulate random mismatch between capacitors of the same type). Table V shows that filter BW follows the VCO oscillation frequency with an accuracy better than ±1%, for 3σ deviations in the various capacitors.

C. ALC Loop

The ALC is very similar to the AFC, except that it controls amplitude of oscillation instead of frequency [Fig. 14(b)]. A 2-bit counter selects the three discrete states of the negative conductance circuit. Comparators with trip points at 2.4 and 3.2 V define the valid range of control voltage. Initially, both $g_{\rm Pos}$ and $g_{\rm Neg2}$ are off and the control voltage is set midscale to 2.8 V. If the transconductor output conductance is net positive, the peak detector senses zero. The ALC now raises the negative conductance by increasing $V_{\rm ALC}$. In steady state, the net output conductance is zero, and the amplitude of oscillation is 200 mV.

TABLE V
VARIATION IN VCO FREQUENCY AND FILTER BW

BW (MHz)	Parameter Variation	C_o (±15%)	C_i (±10%)	C_u (±7%)
15	ΔVCO (f_0)	±1.45%	±3.51%	±3.9%
	ΔFilter (BW)	±1.87%	±2.75%	±4.7%
	$\lvert\Delta BW-\Delta f_0\rvert$	0.42%	0.76%	0.8%
5.7	ΔVCO (f_0)	±0.75%	±1.4%	±6.65%
	ΔFilter (BW)	±0.35%	±0.86%	±6.1%
	$\lvert\Delta BW-\Delta f_0\rvert$	0.35%	0.54%	0.65%



(a) (b)

Fig. 15. Simulated response to a 300-mV step in (a) ALC loop, with AFC inactive and (b) AFC loop, with ALC inactive.

D. Simultaneous Compensation of AFC and ALC

At power up, the ALC induces oscillation. As a result the AFC loop becomes active and changes G_m, but as there is no tail current source, this also changes the FET bias current. Since the output conductance depends on bias, the ALC reacts by adjusting the negative conductance to compensate for the new output conductance. In this way, the two loops interact and can possibly oscillate in a limit cycle. The solution is to substantially slow down the AFC loop compared to the ALC. Fig. 15(a) shows that with AFC inactive, the ALC loop settles in about 1.5 μs in response to a 300-mV step. Fig. 15(b) shows that with ALC inactive, the AFC loop settling time is about 15 μs, which is considerably slower than the ALC. Sufficient phase margin may be deduced from the small overshoot in the settling transient.

VIII. EXPERIMENTAL RESULTS

The variable-gain BPF IC (Fig. 16) was implemented in a 3M1P 0.6-μm CMOS technology. The linear degeneration resistors consume the largest area in the low-power G_m stage and

Authorized licensed use limited to: University of Missouri Libraries. Downloaded on January 16,2024 at 20:47:54 UTC from IEEE Xplore. Restrictions apply.

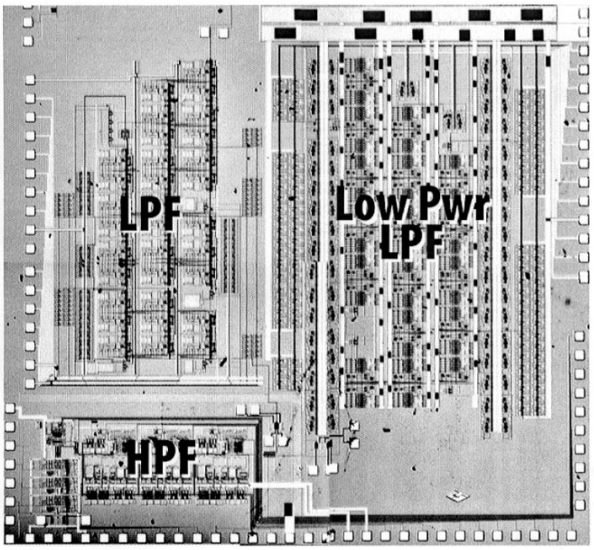
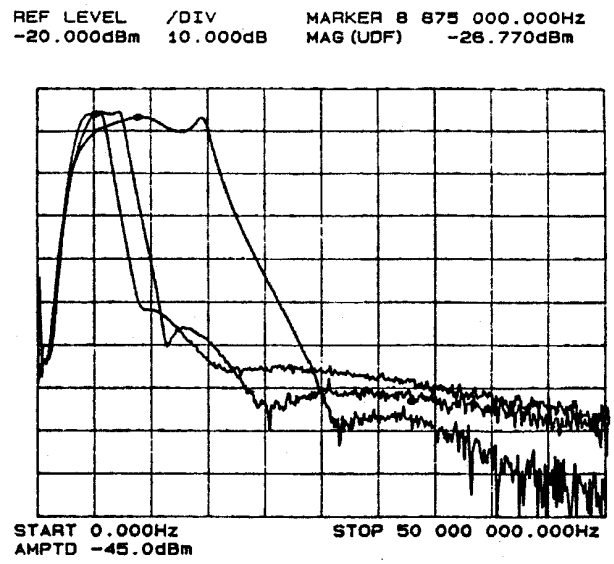


Fig. 16. Chip microphotograph.

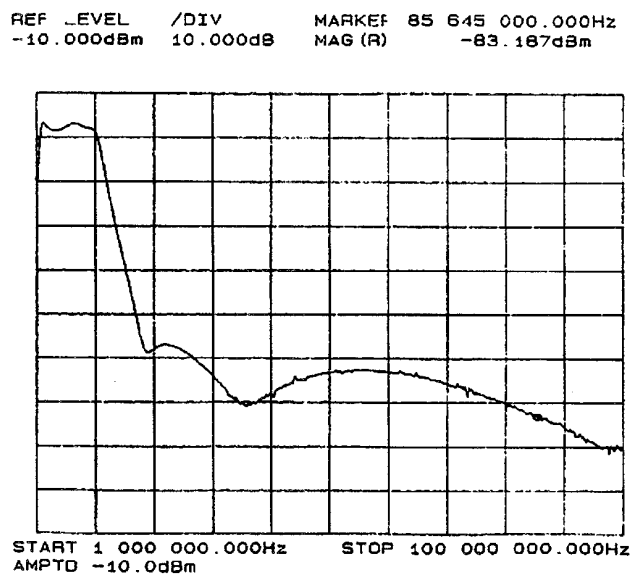
the large PMOS load in the high power G_m stage. The LPF cutoff is tunable between 4–18 MHz, and for the HPF between 3–8 MHz. Fig. 17(a) shows the composite frequency response. At the highest BW, the passband suffers from 2.5-dB ripple, but the stopband loss is more than 60 dB. At lower BW, the ripple decreases to 1 dB (as initially designed), but the stopband attenuation worsens to 50 dB. At high BW, most of the linear capacitors are turned off, and parasitic capacitors significantly alter the pole-zero constellation, worsening the passband ripple. At lower BW, the filter response is closer to designed because the linear capacitors dominate the parasitics. As the LPF is tuned down in frequency, the floating capacitors, which generate nulls in the elliptic filter's magnitude response, appear larger relative to the grounded capacitors, causing the first null to decrease faster than the corner pole frequency. Thus, the transition region becomes sharper, which is desirable, but at the expense of 10-dB-worse stopband loss. Fig. 17(b) shows that the stopband of the filter extends to 100 MHz, beyond which the RF preselect filter at the receiver input strongly attenuates out-of-band signals. The measured passband gain ranges over 47 dB in three steps of 15.7 dB each.

The low-power LPF and low-noise LPF drain 5.4 and 56 mA from 3.3 V, respectively. Input-referred average passband differential noise density is 50 nV/$\sqrt{}$Hz and 15.2 nV/$\sqrt{}$Hz, respectively. In-band IIP3, measured with two tones at 10 and 11 MHz for 15-MHz BW, is +18.5 dBm (referred to 100-Ω differential). This is unchanged for close-in out-of-band tones at 20 and 30 MHz. However, the out-of-band IIP3 with two sets of tones at 30 and 50 MHz and 40 and 70 MHz is +22.5 dBm. As the LPF input stage, where out-of-band tones experience little filtering, dominates the distortion, the IIP3 is not much changed.

The three-stage HPF consumes a total of 5.4 mA at all gains from 0 to 45 dB. The lower cutoff frequency is adjustable from 3 to 10 MHz. Output IP3 specifies linearity for a circuit with variable gain, and for one HPF stage this is found to remain almost constant at +28 dBm (referred to 100-Ω diff), limited by



(a)



(b)

Fig. 17. Measured filter frequency response. (a) Various BW settings, passband, and transition band. (b) Stopband.

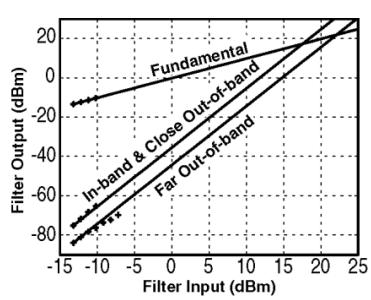
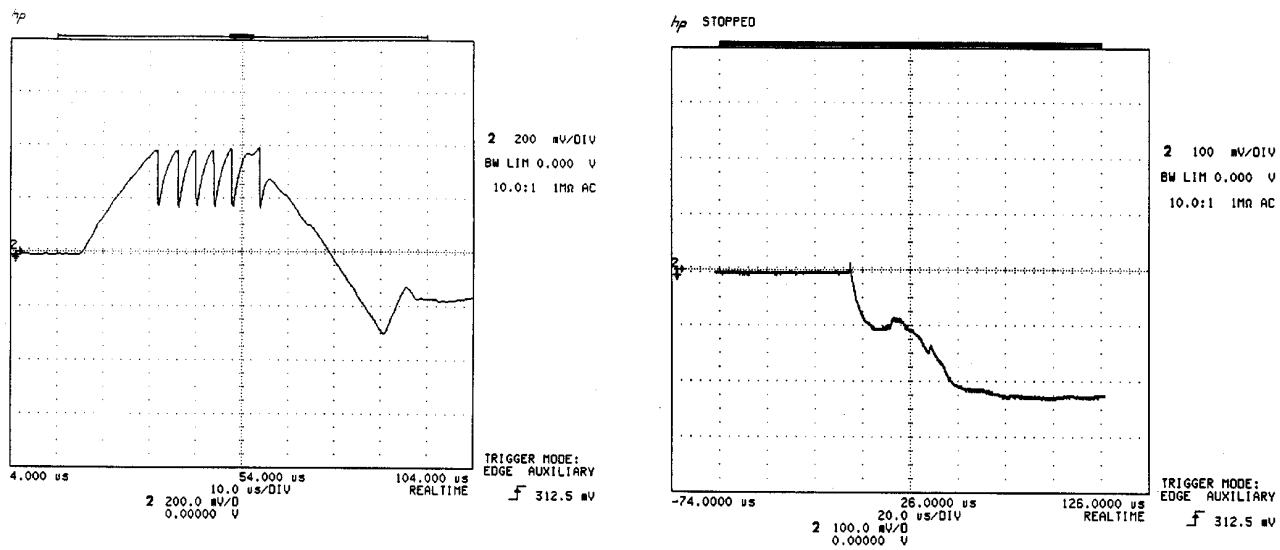


Fig. 18. Measured filter input IP3 at 0-dB passband gain, for two tones in-band and out-of-band.

Authorized licensed use limited to: University of Missouri Libraries. Downloaded on January 16,2024 at 20:47:54 UTC from IEEE Xplore. Restrictions apply.



(a) (b)

Fig. 19. Measured settling transient following reset for: (a) AFC and (b) ALC loop.

TABLE VI
COMPARISON OF THE PERFORMANCE OF THIS WORK WITH RECENT PUBLISHED WORKS

Source	Filter order	Technology	cutoff	I/Pole (mA)	Noise (nV/rt-Hz)		Linearity (IIP3, dBm)		Our relative DR (dB)	Their test conditions
					Theirs	Ours	Theirs	Ours		
[21]	6th elliptic+2nd Butterwoth	1μm CMOS	230 kHz	0.74	70	61	30	22.5	-6.3	24 dB gain in filter; Stopband IIP3
[22]	3rd elliptic	0.5μm CMOS	5.5 MHz	1.2	114	48	17.4	20	+10	
[23]	5th elliptic	0.5μm CMOS	2 Mhz	0.77	32.3	60	7	22.5	+10.1	IIP3 ref. to diff. 50 ohms
[24]	6th elliptic	0.5μm CMOS	700 kHz	1.6	30	41.5	30	22.5	-10	AGC within filter. Noise at max. gain. IIP3 at min. gain.
[25]	7th elliptic	1μm BiCMOS	150 kHz--1.5MHz	1.48	140	43	26.7	20	+3.5	IP3 converted from THD
[26]	3rd Buttherworth	BJT	192 kHz	0.33	273	91.2	22.6	20	+6.9	IP3 converted from THD
[27]	5th elliptic	0.8μm CMOS	4 kHz	0.66	130	64	10.8	20	+15.3	

the main amplifier transconductance (G_{mA} in Fig. 6). Average input in-band noise at 0-dB gain is 40 nV/$\sqrt{\mathrm{Hz}}$, dropping to 7.9 nV/$\sqrt{\mathrm{Hz}}$ at gains of 15 dB and higher.

Fig. 18 shows that total IIP3 for the BPF is +18 dBm for in-band tones and out-of-band tones at 20 and 30 MHz. For far out-of-band interferers, namely 30/50 MHz and 30/70 MHz, the IIP3 is +22.5 dBm. As the LPF strongly attenuates interferers in its stopband prior to the following HPF, it (the LPF) governs total filter IP3.

The measured settling behavior of the ALC and AFC loop after applying reset signal is shown in Fig. 26. In Fig. 19(a), the filter capacitance was initially too high. V_{AFC} increases, driving G_{mu} higher until it trips the comparator. At that point the AFC logic switches off a capacitor and resets V_{AFC}. This

Authorized licensed use limited to: University of Missouri Libraries. Downloaded on January 16,2024 at 20:47:54 UTC from IEEE Xplore. Restrictions apply.

IPR2024-00819
Apple EX1006 Page 12

process continues until the correct capacitor is found. Then $V_{\rm AFC}$ reaches equilibrium. Fig. 19(b) shows how the ALC settles to the final value.

Table VI compares the performance of the LPF designed in the work with other filters. The bias current and noise of this LPF are scaled according to match $I_{\rm bias}$/pole in each case (Noise power $\propto I_{\rm bias}$). Since many of the other filters are not designed for wireless applications, their linearity is specified by single-tone total harmonic distortion (THD) rather than IP3. In this case, it is assumed that the third-order nonlinearity is dominant, and the IP3 is estimated from the THD. The LPF described here surpasses all the other filters, except those interleaving filtering and amplification.

IX. Conclusion

This paper has described the architecture and circuit of a broad-band CMOS BPF for partial channel selection in a low-IF wireless receiver. It is implemented as a LPF in cascade with a HPF for lower power consumption than a true bandpass filter. The bandwidth is selectable from 625 kHz, 2.5 MHz, and 10 MHz, with the lower passband edge fixed at 5 MHz. By careful design of the transconductor, the optimum linearity and dynamic range is obtained for a given power consumption. The HPF is implemented by using a low-pass feedback. This overcomes the HPF sensitivity to the parasitic capacitances to ground.

We show two low-power and high-power versions of the LPF drain 5.4 and 56 mA from a 3.3-V supply, with input noise of 50 and 15.2 nV/$\sqrt{\rm Hz}$, respectively. The HPF drains 5.8 mA with 7.9 nV/$\sqrt{\rm Hz}$ input noise, when it has gain higher than 15 dB. The gain of HPF is variable from 0 to 45 dB in 15-dB steps. The BPF provides better than 50-dB stopband rejection and less than 2.5-dB passband ripple.

References

[1] R. Carson, *Radio Communications Concepts: Analog*. New York: Wiley, 1990.

[2] T. Paulus, S. S. Somayajula, T. A. Miller, B. Trotter, C. Kyong, and D. A. Kerth, "A CMOS IF transceiver with reduced analog complexity," *IEEE J. Solid-State Circuits*, vol. 33, pp. 2154–2159, Dec. 1998.

[3] A. R. Feldman, B. E. Boser, and P. R. Gray, "A 13-bit, 1.4-MS/s sigma-delta modulator for RF baseband channel applications," *IEEE J. Solid-State Circuits*, vol. 33, pp. 1462–1469, Oct. 1998.

[4] Y.-T. Wang and A. A. Abidi, "CMOS active filter design at very high frequencies," *IEEE J. Solid-State Circuits*, vol. 25, pp. 1562–1574, Dec. 1990.

[5] J. Putnam and H. Samueli, "A 4-channel diversity QAM receiver for broadband wireless communications," in *Proc. Int. Solid-State Circuits Conf. (ISSCC'99)*, San Francisco, CA, Feb. 15–17, 1999, pp. 338–339.

[6] R. Gregorian and G. Temes, *Analog MOS Integrated Circuits for Signal Processing*. New York: Wiley, 1986.

[7] F. Behbahani, Y. Kishigami, J. Leete, and A. A. Abidi, "CMOS 10 MHz-IF downconverter with on-chip broadband circuits for large image-suppression," in *Proc. Symp. VLSI Circuits*, Kyoto, Japan, 1999.

[8] W. K. Chen, *The Circuits and Filters Handbook*. New York: IEEE Press, 1995.

[9] H. Khorramabadi and P. R. Gray, "High-frequency CMOS continuous-time filters," *IEEE J. Solid-State Circuits*, vol. SC-19, pp. 939–948, Dec. 1984.

[10] A. Kaiser, "A micropower CMOS continuous-time low-pass filter," *IEEE J. Solid-State Circuits*, vol. 24, pp. 736–743, June 1989.

[11] C. H. J. Mensink, B. Nauta, and H. Wallinga, "A CMOS "soft-switched" transconductor and its application in gain control and filters," *IEEE J. Solid-State Circuits*, vol. 32, pp. 989–998, July 1997.

[12] F. Krummenacher and N. Joehl, "A 4-MHz CMOS continuous-time filter with on-chip automatic tuning," *IEEE J. Solid-State Circuits*, vol. 23, pp. 750–758, June 1988.

[13] S. Szczepanski, J. Jakusz, and R. Schaumann, "A linear fully balanced CMOS OTA for VHF filtering applications," *IEEE Trans. Circuits Syst. II*, vol. 44, pp. 174–187, Mar. 1997.

[14] K. Ono, N. Fujii, S. Takagi, and M. Hotta, "Design of low-distortion MOS OTA based on cross-coupled differential amplifier and its application for active filters," *IEICE Trans. Fund. Electron., Commun. Comput. Sci.*, vol. E77-A, no. 2, pp. 363–370, Feb. 1994.

[15] S. D. Willingham, K. W. Martin, and A. Ganesan, "A BiCMOS low-distortion 8-MHz low-pass filter," *IEEE J. Solid-State Circuits*, vol. 28, pp. 1234–1245, Dec. 1993.

[16] T. Inoue, F. Ueno, M. Kawasaki, and Y. Aramaki *et al.*, "A new MOS linear operational transconductance amplifier and its application to OTA-C filters," *IEICE Trans. Electron.*, vol. E75-C, no. 1, pp. 81–89, Jan. 1992.

[17] B. Nauta, "A CMOS transconductance-C filter technique for very high frequencies," *IEEE J. Solid-State Circuits*, vol. 27, pp. 142–153, Feb. 1992.

[18] R. Schaumann, "Design of continuous-time fully integrated filters: A review," *Proc. Inst. Elect. Eng.*, vol. 136, no. 4, pp. 184–190, Aug. 1989.

[19] B. Razavi, *RF Microelectronics*. Upper Saddle River, NJ: Prentice-Hall, 1998.

[20] D. K. Shaeffer, A. R. Shahani, S. S. Mohan, and H. Samavati *et al.*, "A 115-mW, 0.5-μm CMOS GPS receiver with wide dynamic-range active filters," *IEEE J. Solid-State Circuits*, vol. 33, pp. 2219–2231, Dec. 1998.

[21] P. J. Chang, A. Rofougaran, and A. A. Abidi, "A CMOS channel-select filter for a direct-conversion wireless receiver," *IEEE J. Solid-State Circuits*, vol. 32, pp. 722–729, May 1997.

[22] C. H. J. Mensink, B. Nauta, and H. Wallinga, "A CMOS "soft-switched" transconductor and its application in gain control and filters," *IEEE J. Solid-State Circuits*, vol. 32, pp. 989–998, July 1997.

[23] D. K. Shaeffer, A. R. Shahani, and T. H. Lee, "A 115-mW, 0.5 um CMOS GPS receiver with wide dynamic-range active filters," *IEEE J. Solid-State Circuits*, vol. 33, pp. 2219–2232, Dec. 1998.

[24] T. B. Cho, G. Chien, F. Brianti, and P. R. Gray, "A power-optimized CMOS baseband channel filter and ADC for cordless application," in *Symp. VLSI Circuits Dig. Tech.*, Honolulu, HI, June 13–15, 1996, pp. 64–65.

[25] Y. F. Yang and C. C. Enz, "A low-distortion BiCMOS seventh-order Bessel filter operating at 2.5 V supply," *IEEE J. Solid-State Circuits*, vol. 31, pp. 321–330, Mar. 1996.

[26] M. Koyama, T. Arai, H. Tanimoto, and Y. Yoshida, "A 2.5-V active low-pass filter using all-n-p-n Gilbert cells with a 1-$V_{\rm pp}$ range," *IEEE J. Solid-State Circuits*, vol. 28, pp. 1246–1253, Dec. 1993.

[27] C. Yoo, S. Lee, and W. Kim, "A $\pm$1.5-V, 4 MHz CMOS continous-time filter with a single-integrator based tuning," *IEEE J. Solid-State Circuits*, vol. 33, pp. 18–27, Jan. 1998.

[28] D. Cheung, K. Bult, and A. Buchwald, "10-MHz 60-dB dynamic-range 4th-order Butterworth lowpass filter," in *Proc. 23rd Eur. Solid-State Circuits Conf. (ESSCIRC'97)*, Southampton, U.K., 1997, pp. 248–251.

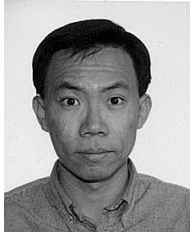
Farbod Behbahani was born in Tehran, Iran, in 1967. He received the B.S. and M.S. degrees (with honors) in electrical engineering from Sharif University of Technology, Tehran, Iran, in 1990 and 1993, respectively, and the Ph.D. degree from the University of California, Los Angeles (UCLA), in 1999.

From 1992 to 1995, he worked for Philips Semiconductors as an RF and Analog Integrated Circuit Designer. From 1995 to 1999, he was a Research Assistant at UCLA. Since 1999, he has been with Valence Semiconductor Inc., Irvine, CA, where he is the Director of Engineering, RF & wireless. His research interests include RF CMOS and adaptive architecture for wireless radio. He has received two U.S. patents and is an author or co-author of more than 25 technical papers in the area of integrated circuit design and communication systems.

Dr. Behbahani was a corecipient of the second prize in the annual Iranian national research contest in 1996 and the IEEE Solid-State Circuits Society predoctoral Fellowship in 1997. He received the Young Scientist Award from the Association of Professors and Scholars of Iranian Heritage in California in 1999.

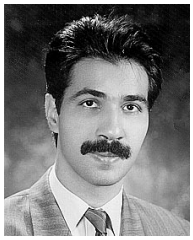
Authorized licensed use limited to: University of Missouri Libraries. Downloaded on January 16,2024 at 20:47:54 UTC from IEEE Xplore. Restrictions apply.

IPR2024-00819
Apple EX1006 Page 13



Weeguan Tan was born in Singapore in 1970. He received the Bachelor degree in electrical engineering from the University of California at Berkeley in 1994 and the Masters degree in electrical engineering from UCLA in 1999.

Currently, he is a design engineer at Newport Communications, Irvine, CA.



Ali Karimi-Sanjaani (S'98) was born in Tehran, Iran, in March 1974. He received the B.S. and M.S. (highest honors) degrees in electrical engineering from SHARIF University of Technology, Tehran, Iran, in 1995 and 1997, respectively. He is currently pursuing his Ph.D. degree by focusing on a fully integrated WCDMA receiver for 3rd generation mobile radio.

He joined the Electrical Engineering Department of UCLA in January 1998 where he worked on the design of a wireless local area network analog receiver. His area of interests include analog IC's for communications, wireless transceiver architecture and curcuit design, and nonlinerar circuit analysis.

Andreas Roithmeier, photograph and biography not available at the time of publication.

Asad A. Abidi (S'75–M'80–SM'95–F'96) received the B.Sc. (Hons.) degree from Imperial College, London, U.K., in 1976 and the M.S. and Ph.D. degrees in electrical engineering from the University of California, Berkeley, in 1978 and 1981.

He was at Bell Laboratories, Murray Hill, NJ, from 1981 to 1984 as a Member of Technical Staff in the Advanced LSI Development Laboratory. Since 1985, he has been w ith the Electrical Engineering Department of the University of California, Los Angeles, where he is Professor. He was a Visiting Faculty Researcher at Hewlett Packard Laboratories during 1989. His research interests are in CMOS RF design, high-speed analog integrated circuit design, data conversion, and other techniques of analog signal processing.

Dr. Abidi was the Program Secretary for the International Solid-State Circuits Conference from 1984 to 1990 and General Chairman of the Symposium on VLSI Circuits in 1992. He was Secretary of the IEEE Solid-State Circuits Council from 1990 to 1991. From 1992 to 1995, he was Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS. He has received the 1988 TRW Award for Innovative Teaching and the 1997 IEEE Donald G. Fink Award. He was a corecipient of the Best Paper Award at the 1995 European Solid-State Circuits Conference, the Jack Kilby Best Student Paper Award at the 1996 International Solid-State Circuits Conference (ISSCC), the Jack Raper Award for Outstanding Technology Directions Paper at the 1997 ISSCC, and the Design Contest Award at the 1998 Design Automation Conference.

Authorized licensed use limited to: University of Missouri Libraries. Downloaded on January 16,2024 at 20:47:54 UTC from IEEE Xplore. Restrictions apply.