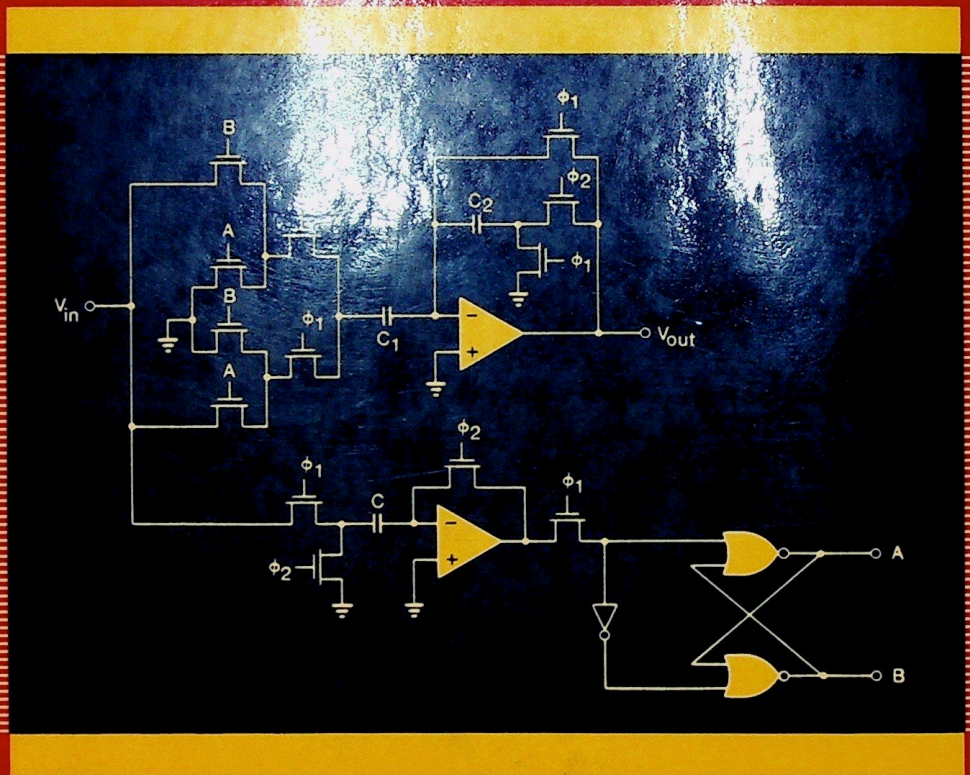


Analog MOS Integrated Circuits

FOR SIGNAL PROCESSING



ROUBIK GREGORIAN

GABOR C. TEMES

A volume in the Wiley Series on Filters: Design, Manufacturing and Applications; Robert A. Johnson & George Szentirmai, Editors

This book is both a reference for industry and a textbook. It is both theoretical and practical. It covers analog MOS integrated circuits. *MOS Integrated Circuits for Signal Processing* both explains the operating principles and shows professional and advanced student engineers how to design them. Only a minimum of mathematics, electronic conductor physics, and analog MOS integrated circuit design are required. The theoretical design is not restricted to the practical design. A number of design examples are available to compare the book focuses on the most widely tested one.

The first three chapters of *MOS Integrated Circuits* give a basic description of the circuits, and necessary background mathematics (Laplace transforms) and device physics. The rest of the book is devoted to the operation and design of circuits as switches, analog-to-digital converters, log converters, and oscillators, and also discusses the problems encountered and provides solutions, and examples of actual applications. To enhance reference, *Analog Circuits* includes numerical design and step-by-step procedures and exercises that test the reader's understanding of the book.

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Analog MOS Integrated Circuits for Signal Processing

Roubik Gregorian and Gabor C. Temes

ANALOG MOS INTEGRATED CIRCUITS FOR SIGNAL PROCESSING

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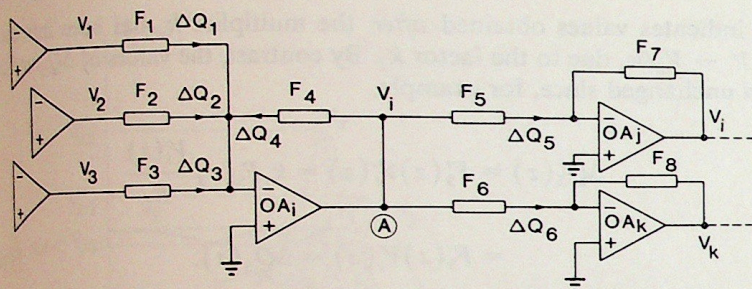


FIGURE 5.40. SC filter section.

For very narrow-band bandpass filters (say, with relative bandwidths of 1% or less) none of the design techniques described in this chapter are very effective, since they result in circuits which are too sensitive to finite op-amp gain effects, strays, and element-value variations. Then, design based on the *N-path filter concept* may be used. This concept, and the corresponding design techniques, are discussed in Section 5.8.

5.6. THE SCALING OF SWITCHED-CAPACITOR FILTERS^{19,36}

The actual performance of an SCF can be improved, and the area which it occupies on its silicon chip reduced, by scaling operations. To understand how such operations can be carried out, consider a segment of an SCF containing the i th op-amp OA_i and all branches connected to it. This is schematically illustrated in Fig. 5.40, in which the coupling branches may contain capacitors and switches in any arrangement. Each coupling branch in a stray-insensitive SCF is connected between an op-amp output and a virtual ground; each can be described by a transfer function $F_k(z) = \Delta Q_k(z)/V_i(z)$. Here, $\Delta Q_k(z)$ is the z -domain representation of the charge-per-clock-period sequence $q_k(nT)$ (i.e., $q_k(nT - T)$), and $V_i(z)$ is the z -transform of the voltage sequence $v_i(nT)$ at the input of the branch.

Now let all branches connected to the *output* terminal of OA_i be modified such that their $\Delta Q/V$ transfer functions (F_4, F_5, F_6) are multiplied by a positive real constant factor k_i . This can be achieved simply by multiplying all capacitors in these branches by k_i , since (for given voltages connected across these branches) their charges are proportional to these capacitances.

Since the input branches and their voltages were left unchanged, the charge flowing in the feedback branch

$$\Delta Q_4(z) = -\Delta Q_1(z) - \Delta Q_2(z) - \Delta Q_3(z) \quad (5.93)$$

remains at its original value. The output voltage of OA_i (assuming ideal op-amps) thus becomes $V'_i(z) = \Delta Q_4(z)/[k_i F_4(z)] = V_i(z)/k_i$, where the

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prime indicates values obtained *after* the multiplier k_i has been introduced. Thus, $V_i \rightarrow V_i/k_i$ due to the factor k_i . By contrast, the values of ΔQ_5 and ΔQ_6 remain unchanged since, for example,

$$\begin{aligned}\Delta Q'_5(z) &= F'_5(z)V'_i(z) = k_i F_5(z) \frac{V_i(z)}{k_i} \\ &= F_5(z)V_i(z) = \Delta Q_5(z).\end{aligned}\quad (5.94)$$

In conclusion, multiplying all capacitors which are connected (or switched) to the output terminal of the i th op-amp OA_i changes its output voltage V_i to V_i/k_i , while leaving all charges flowing from (and to) OA_i to (and from) the rest of the circuit unchanged. Thus, by this operation we can increase or decrease V_i by a constant scale factor without affecting any other voltages or charges in the SCF.

The described scaling operation is useful in improving the dynamic range of SC circuits. As defined in Section 4.1 of Chapter 4, the dynamic range is $20 \log_{10} (v_{in, \max}/v_{in, \min})$. Here, $v_{in, \max}$ is the maximum input signal which the SCF can handle without excessive nonlinear distortion; in an SCF, $v_{in, \max}$ is usually limited by the saturation of the op-amps. The minimum useful input signal $v_{in, \min}$ is the smallest value for which the SCF output voltage v_{out} can be distinguished from the output noise $v_{n, out}$.

In the following discussions it will be assumed that the dynamic range of the SCF is to be optimized using scaling. Consider the SC circuit schematically illustrated in Fig. 5.41. Let the amplitude of the largest output signal which the op-amps in the filter (assumed, for simplicity, to be identical) can handle be $V_{\max}$. Also, let the passband gain of the filter be A_p . Since v_{out} (produced by the output op-amp OA_n) is at most $V_{\max}$, we have

$$v_{in, \max} \leq V_{\max}/A_p. \quad (5.95)$$

Let the frequency responses of all op-amp outputs $V_1, V_2, \dots, V_i, \dots, V_n$ be as shown in Fig. 5.42, where a fifth-order low-pass filter is assumed. Then, as the amplitude of v_{in} is increased from a small value to $V_{\max}/A_p$ at a frequency near ω_2 (the peak frequency of V_2), OA_2 will saturate before OA_5 does since

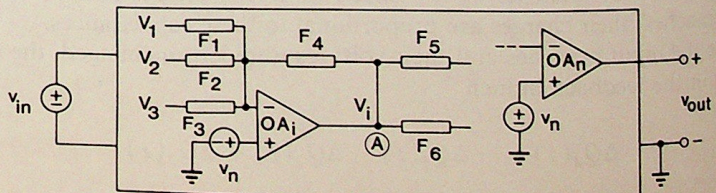


FIGURE 5.41. SC filter with noisy internal op-amp.

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