PTO/SB/05 (01-04)

16562 U.S.PTO 022304

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	021673-000210US
First Inventor	Tsividis, Yannis
Title	POWER DISSIPATION REDUCTION IN WIRELESS TRANSCEIVERS
Express Mail Label No.	EV 369 118 824 US

22278 U.S.PTO 10/784613 022304

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. ☒ Fee Transmittal Form (e.g., PTO/SB/17) *(Submit an original and a duplicate for fee processing)*
2. ☒ Applicant claims small entity status. See 37 CFR 1.27.
3. ☒ Specification [*Total Pages* 25] *(preferred arrangement set forth below)*
   - Descriptive title of the Invention
   - Cross Reference to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to sequence listing, a table, or a computer program listing appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
4. ☒ Drawing(s) *(35 U.S.C.113)* [*Total Sheets* 15]
5. Oath or Declaration [*Total Pages* 1]
   a. ☒ Newly executed (original or copy)
   b. ☐ Copy from a prior application (37 CFR 1.63 (d)) *(for a continuation/divisional with Box 18 completed)*
      i. ☐ DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
6. ☒ Application Data Sheet. See 37 CFR 1.76

ADDRESS TO

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7. ☐ CD-ROM or CD-R in duplicate, large table or Computer Program *(Appendix)*
8. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. ☐ Computer Readable Form (CRF)
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      i. ☐ CD-ROM or CD-R (2 copies); or
      ii. ☐ Paper number of pages
   c. ☐ Statements verifying identity of above copies

ACCOMPANYING APPLICATIONS PARTS

9. ☐ Assignment Papers (cover sheet & document(s))
10. ☐ 37 CFR 3.73(b) Statement ☐ Power of Attorney *(when there is an assignee)*
11. ☐ English Translation Document *(if applicable)*
12. ☐ Information Disclosure Statement (IDS)/PTO-1449 ☐ Copies of IDS Citations
13. ☐ Preliminary Amendment
14. ☒ Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
15. ☐ Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
16. ☒ Nonpublication Request under 35 U.S.C. 122 (b)(2)(B)(i). Applicant must attach form PTO/SB/35 or its equivalent
17. ☐ Other:

18. If a CONTINUING APPLICATION, *check appropriate box, and supply the requisite information below and in the first sentence of the specification following the title, or in an Application Data Sheet under 37 CFR 1.76:*

☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No: _____

Prior application information: *Examiner* _____ *Art Unit:* _____

For CONTINUATION OF DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 5b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

19. CORRESPONDENCE ADDRESS

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Signature		*Date*	February 23, 2004

60142384 v1

FEE TRANSMITTAL for FY 2004

Effective 10/01/2003. Patent fees are subject to annual revision.

☒ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 604

Complete if Known	
Application Number	
Filing Date	
First Named Inventor	Tsividis, Yannis
Examiner Name	
Art Unit	
Attorney Docket No.	021673-000210US

METHOD OF PAYMENT *(check all that apply)*

☐ Check ☐ Credit Card ☐ Money Order ☐ Other ☐ None

☒ Deposit Account:

Deposit Account Number: 20-1430

Deposit Account Name: Townsend and Townsend and Crew LLP

The Director is authorized to: *(check all that apply)*

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FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	770	2001	385	Utility filing fee	385
1002	340	2002	170	Design filing fee	
1003	530	2003	265	Plant filing fee	
1004	770	2004	385	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($)385

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

			Extra Claims	Fee from below	Fee Paid
Total Claims	30	-20** =	10	X$9 =	$90
Independent Claims	6	-3** =	3	X$43 =	$129
Multiple Dependent				X =	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	86	2201	43	Independent claims in excess of 3
1203	290	2203	145	Multiple dependent claim, if not paid
1204	86	2204	43	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($)219

***or number previously paid, if greater; For Reissues, see above*

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet.	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	420	2252	210	Extension for reply within second month	
1253	950	2253	475	Extension for reply within third month	
1254	1,480	2254	740	Extension for reply within fourth month	
1255	2,010	2255	1,005	Extension for reply within fifth month	
1401	330	2401	165	Notice of Appeal	
1402	330	2402	165	Filing a brief in support of an appeal	
1403	290	2403	145	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive – unavoidable	
1453	1,330	2453	665	Petition to revive – unintentional	
1501	1,330	2501	665	Utility issue fee (or reissue)	
1502	480	2502	240	Design issue fee	
1503	640	2503	320	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Petitions related to provisional applications	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	770	2809	385	Filing a submission after final rejection (37 CFR § 1.129(a))	
1810	770	2810	385	For each additional invention to be examined (37 CFR § 1.129(b))	
1801	770	2801	385	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	
				Other fee (specify) ----------	

*Reduced by Basic Filing Fee Paid **SUBTOTAL (3)** ($)

SUBMITTED BY				Complete *(if applicable)*	
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60142388 v1

PTO/SB/35 (02-01)

NONPUBLICATION REQUEST CERTIFICATION UNDER 35 U.S.C. 122(b)(2)(B)(i)		
	First Named Inventor	Yannis Tsividis
	Title	POWER DISSIPATION REDUCTION IN WIRELESS TRANSCEIVERS
	Atty Docket Number	021673-000210US

I hereby certify that the invention disclosed in the attached application **has not and will not be** the subject of an application filed in another country, or under a multilateral agreement, that requires publication at eighteen months after filing.

I hereby request that the attached application not be published under 35 U.S.C. 122(b).

February 23, 2004
Date


Signature

Reg. No. 44,005

J. Matthew Zigmant
Typed or printed name

This request must be signed in compliance with 37 CFR 1.33(b) and submitted with the application **upon filing.**

Applicant may rescind this nonpublication request at any time. If applicant rescinds a request that an application not be published under 35 U.S.C. 122(b), the application will be scheduled for publication at eighteen months from the earliest claimed filing date for which a benefit is claimed.

If applicant subsequently files an application directed to the invention disclosed in the attached application in another country, or under a multilateral international agreement, that requires publication of applications eighteen months after filing, the applicant **must** notify the United States Patent and Trademark Office of such filing within forty-five (45) days after the date of the filing of such foreign or international application. **Failure to do so will result in abandonment of this application (35 U.S.C. 122(b)(2)(B)(iii)).**

60142391 v1

Attorney Docket No.: 021673-000210US

PATENT APPLICATION

POWER DISSIPATION REDUCTION IN WIRELESS TRANSCEIVERS

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POWER DISSIPATION REDUCTION IN WIRELESS TRANSCEIVERS

CROSS-REFERENCES TO RELATED APPLICATIONS

[0001] This application claims the benefit of United States provisional application number 60/451,229, filed March 1, 2003, which is incorporated by reference.

[0002] This application is related to United States provisional application number 60/451,230, filed March 1, 2003, which is incorporated by reference.

BACKGROUND

[0003] The present invention relates to power dissipation reduction techniques for electronic circuits, for example wireless transceiver integrated circuits.

[0004] Wireless networking is quickly becoming ubiquitous, as desktop, notebook, and handheld computers are connected to share Internet access and files. Wireless networking cards compatible with PCMCIA and compact flash form factors are popular for laptops and handhelds respectively, particularly as mobile users connect to the Internet on the road at coffee shops, hotels, and airports.

[0005] A downside of this connectivity is a corresponding drain on battery life, especially for these portable devices. The power consumed by a wireless transmitter and receiver reduces the usefulness of a device and sends a user on a hunt for an electrical outlet for recharging.

[0006] One reason why this power drain is high is that electronic circuits are typically designed to function properly under worst-case operating conditions. For a wireless transceiver, the worst case condition is when a desired signal reception strength is low, while other transceivers or nearby electronic equipment generate interfering signals and other spurious noise.

[0007] But a wireless transceiver does not always operate in these worst-case conditions. For example, a base station, router or access point may be nearby such that the received signal is strong. Also, there may be no interfering signals, or they may be relatively weak. In these situations, receiver circuit currents can be reduced below what is necessary for the worst case condition. If this is done, power dissipation is reduced, and battery life is increased.

[0008] Thus, what is needed are circuits and methods that can adapt to a better-than-worst-case condition and reduce circuit currents and therefore power dissipation accordingly.

SUMMARY

[0009] Accordingly, embodiments of the present invention provide methods and circuits for reducing power dissipation in wireless transceivers and other electronic circuits and systems. Embodiments of the present invention use bias current reduction, impedance scaling, gain, and other dynamic changes either separately or in combination to reduce power dissipation in response to better-than-worst case conditions. For example, bias currents are reduced in response to a need for reduced signal handling capability, impedances are scaled thus reducing required drive and other bias currents in response to a strong received signal, or gain is varied and impedances are scaled in response to a low received signal in the presence of no or weak interfering signals. Alternately, currents may start low and be increased in response to worse-than-best-case conditions, or they may start at a point in between and vary up or down. These variations may be made to electronic systems generally, and are particularly suited and discussed below in the context of a wireless transceiver that may be used in networking devices, cellular telephones, and other wireless systems.

[0010] An exemplary embodiment of the present invention provides a method of receiving a signal using an integrated circuit. The integrated circuit includes a signal path having a low-noise amplifier configured to receive the signal, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer. The method itself includes determining a first signal strength at a first node in the signal path in the integrated circuit and dynamically changing an impedance of a component in the signal path based on the first signal strength.

[0011] A further exemplary embodiment of the present invention provides a method of receiving a signal using an integrated circuit. The integrated circuit includes a signal path having a low-noise amplifier configured to receive the signal, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer. The method itself includes determining a first signal strength at a first node in the signal path in the integrated circuit and dynamically changing a bias current in the signal path based on the first signal strength.

[0012] Another exemplary embodiment of the present invention provides a method of receiving a signal using an integrated circuit. The integrated circuit includes a signal path having

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a first circuit and a second circuit having an input coupled to an output of the first circuit. The method itself includes determining a first signal strength at a first node in the signal path in the integrated circuit. The first node is before the first circuit in the signal path. The method further includes dynamically changing a gain of the first circuit based on the first signal strength and dynamically changing an impedance of a component in the second circuit based on the first signal strength.

[0013] Still a further exemplary embodiment of the present invention provides a wireless transceiver integrated circuit including a receiver having a signal path, the signal path including a low-noise amplifier, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer, as well as a first signal strength indicator circuit coupled to the signal path and configured to determine a first signal strength. An impedance in the signal path is configured to be dynamically adjusted in response to the first signal strength.

[0014] Yet a further exemplary embodiment of the present invention provides a wireless transceiver integrated circuit. This integrated circuit includes a receiver comprising a signal path, the signal path having a low-noise amplifier, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer, as well as a first signal strength indicator circuit coupled to the signal path, and configured to determine a first signal strength. A bias current in the signal path is configured to be dynamically adjusted in response to the first signal strength.

[0015] Another exemplary embodiment of the present invention provides a wireless transceiver integrated circuit. This circuit includes a receiver comprising a signal path, the signal path having a first circuit; and a second circuit having an input coupled to an output of the first circuit; as well as a first signal strength indicator circuit coupled to the signal path, and configured to determine a first signal strength. A gain of the first circuit is configured to be dynamically adjusted in response to the first signal strength, and an impedance in the second circuit is configured to be dynamically adjusted in response to the first signal strength.

[0016] A better understanding of the nature and advantages of the present invention may be gained with reference to the following detailed description and the accompanying drawings.

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BRIEF DESCRIPTION OF THE DRAWINGS

[0017] Figure 1 is a block diagram of a wireless transceiver that may benefit by incorporation of embodiments of the present invention;

[0018] Figures 2A and 2B illustrate examples of desired and interfering signals and noise that may be received by a circuit in a wireless receiver;

[0019] Figure 3 illustrates what can occur as a maximum signal handling capability is reduced in the worst-case signal condition;

[0020] Figure 4 illustrates a portion of a receiver consistent with an embodiment of the present invention;

[0021] Figure 5 illustrates the relationship between a required bias current and a given output signal for a representative circuit;

[0022] Figure 6 is an example of how a circuit's impedances may be scaled to reduce drive currents, and depending on the circuit configuration used, to reduce associated bias currents as well;

[0023] Figure 7 illustrates how gain may be inserted in a signal path to improve a circuit's signal to noise ratio;

[0024] Figures 8A-8D illustrate some of the possible power saving techniques that may be used when received desired and interferer signals are all at a low power level;

[0025] Figures 9A-9C illustrate one of the possible power saving techniques that may be used when a received desired signal is strong while all interfering signals are at a low power level;

[0026] Figures 10A-10C illustrate one of the possible power saving techniques that may be used when received desired and interferer signals are all at a high power level;

[0027] Figures 11A-11D illustrate one of the possible power saving techniques that may be used when a received desired signal is weak while one or more interfering signals are strong;

[0028] Figure 12 is a summary illustrating four different input conditions and some of the appropriate power-saving changes that may be made in response to those conditions;

[0029] Figure 13 shows how power may be saved as a function of time by employing one or more of the power saving methods consistent with embodiments of the present invention;

[0030] Figure 14 is a block diagram of a portion of a receiver consistent with an embodiment of the present invention; and

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[0031] Figure 15 is a block diagram of a portion of a transmitter consistent with an embodiment of the present invention.

DESCRIPTION OF EXEMPLARY EMBODIMENTS

[0032] Figure 1 is a block diagram of a wireless transceiver that may benefit by incorporation of embodiments of the present invention. This wireless transceiver may be designed to send and receive signals consistent with the IEEE 802.11a, 802.11b, 802.11g, or other signaling standard or combination of standards. This figure, as with all the included figures, is shown for illustrative purposes only and does not to limit either the possible embodiments of the present invention or the claims.

[0033] There are three main portions of this transceiver circuit, a receiver, transmitter, and synthesizer. This transceiver may be completely or partially integrated on a semiconductor chip, or it may be integrated onto multiple integrated circuits. In a specific embodiment, the circuitry bounded by dashed line 100 is integrated on a single chip coupled to one or more external components or circuits. The integrated circuit or circuits forming this wireless transceiver may incorporate various integrated circuit devices such as a bipolar, CMOS, or BiCMOS devices made using a silicon, silicon-germanium (SiGe), gallium arsenide or other III-V process, or other manufacturing process. Embodiments of the present invention may also be applicable to circuits manufactured using nanotechnology processing.

[0034] The receiver includes a signal path formed by low-noise amplifier 102, I and Q mixers 104 and 106, low pass filters 108 and 110, and baseband amplifiers 114 and 116. Other circuitry in the receiver includes received strength indicator 122, automatic gain control circuit 166, baseband gain control circuit 120, tuning circuit 112, and offset cancellation circuit 118.

[0035] The transmitter includes input up-converter mixers 124 and 126, summing node 176, which may be conceptual rather than an actual circuit, transmit variable gain amplifier 128, and power amplifier 130.

[0036] The synthesizer includes a voltage-controlled oscillator 148, which drives I and Q buffers 154 and 152, prescaler 156, reference clock buffer 142 and divider 158, phase-frequency detector 160, charge pump 162, and loop filter 146, which in a specific embodiment is formed by external components.

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[0037] Signals are received on an antenna, not shown, and typically pass through an RF switch and bandpass filter before being received by the low-noise amplifier 102 on line 101. The low noise amplifier gains the received signal and provides it to quadrature mixers 104 and 106. I and Q mixers 104 and 106 down-convert the received signal to baseband by multiplying them with quadrature versions of the oscillator signal provided by buffers 152 and 154. This down conversion also produces a high frequency component at a frequency that is equal to the sum of the frequencies of the received signal and the VCO. This unwanted signal is filtered by low pass filters 108 and 110, which in turn drive baseband amplifiers 114 and 116. The outputs of baseband amplifiers 114 and 116 are typically converted to digital signals by analog-to-digital converters at the front end of a digital signal processing block.

[0038] In the transmit mode, I and Q versions of the signal to be transmitted are provided on lines 121 and 123 to up-convert mixers 124 and 126. These up-convert mixers multiply the I and Q portions of the transmit signal by quadrature versions of the VCO signal provided by buffers 152 and 154. The outputs of the up-convert mixers 124 and 126 are summed, and amplified by transmit VGA 128, which in turn drives power amplifier 130. The output of power amplifier 130 is typically filtered, and passes through the RF switch to the antenna for transmission.

[0039] A reference clock is received and buffered by the reference buffer 142. The VCO generates quadrature oscillatory signals that are divided by prescaler 156. The reference clock is typically generated by a crystal or other stable periodic clock source. The phase-frequency detector 116 compares the phase or frequency (depending on whether the synthesizer is tracking or acquiring the correct frequency) of the divided VCO signal and the reference clock, or a divided version of the reference clock, and generates an error signal, which drives the charge pump 162. The output signal of the charge pump 162 is filtered by the loop filter 146, which is commonly a lead-lag filter, and which provides a tuning or correction signal to the VCO 148.

[0040] Embodiments of the present invention may be used to reduce the power dissipation of one or more of these included circuits. For example, the power dissipation in the low-noise amplifier 102, down-convert mixers 104 and 106, low pass filters 108 and 110, or baseband amplifiers 114 and 116 may be optimized. Also, power dissipation in up-convert mixers 124 126, variable gain amplifier 128, and power amplifier 130 may also be optimized. Similarly, VCO 148 and prescaler 156 currents may be adjusted. Embodiments of the present invention

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may also be applied in other circuits which may be included in other integrated circuit receivers, transmitters, transceivers, or other electronic circuits or systems.

[0041] When a receiver is actively receiving a desired signal, each block in the signal path has at its input the desired signal as well as noise and possibly interfering signals. The desired signal is the useful, information-carrying portion of a received signal. The noise may be thermal, shot, or other noise generated on the integrated circuit, in addition to received noise generated by sources external to the chip. The noise at the input of a block may be referred to as the equivalent input noise. The interfering signal or signals, or interferers, may be generated by similar transceivers, or other electrical equipment, circuits, or systems.

[0042] Figures 2A and 2B illustrate examples of desired signals, interferers, and noise that may be received by one of the various circuits in a wireless receiver. In each of these figures, the signal strength is plotted along a Y-axis 204 or 254 as a function of frequency along an X-axis 202 or 252. In the example of Figure 2A, a received desired signal 206 is large in comparison to interfering signals 208 and 210. In these examples, two interfering signals are shown for illustrative purposes, though there may be no such signals, one such signal, or more than two such signals in the frequency range of interest. Also, while for these examples the interferers are shown as being at a higher frequency than the desired signal, there may be one or more interferers at higher or lower frequencies as the desired signal. In this specific example, the acceptable noise floor 214 is relatively high, while maximum signal handling capability Smax 212 (that is the maximum signal power that can be handled with an acceptably low distortion) needs only to be high enough to accommodate the desired signal. For this specific example, the circuit receiving this input spectrum only requires a relatively small dynamic range for proper operation, that is the range between Smax 212 and the noise floor 214 is relatively small.

[0043] Conversely, in the example shown in Figure 2B, the desired signal 256 is relatively weak compared to the large interferers 258 and 260. In this example, the noise floor 264 should be relatively low so as to prevent an unacceptable level of error in the recovery the desired signal 256. The maximum signal handling capability Smax 262 should be relatively high to accommodate the large interferers in order to avoid the creation of intermodulation products as described below. Accordingly, in this specific example, the circuit receiving this input spectrum should have a large dynamic range, particularly in comparison to the example of Figure 2A.

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[0044] It should be noted that the noise level or noise floors shown in these and the other included figures is the noise density integrated over the bandwidth of interest. For simplicity and comparison, this level is shown as a horizontal line, and is not meant to imply noise density.

[0045] Often in wireless receivers, a circuit at different times will receive an input spectrum similar to those shown in Figures 2A and 2B. The input spectrum of Figure 2B is generally considered the worst-case input signal, and typical design methodology involves designing a receiver for this condition, specifically the weakest desired signal accompanied by largest interference level. Circuit impedances and currents are set such that the noise floor 264 is sufficiently low for an acceptable bit-error rate, while bias currents are set sufficiently high for the required Smax 262.

[0046] Conversely, the input spectrum in Figure 2A is that of the best-case input signal, specifically, a robust desired signal accompanied by no or low-level interferers. In this case, the noise floor 214 may be allowed to rise, while the maximum signal handling capability Smax 212 may be reduced. When this is done, the receiver circuit may save significant power. For example, the circuit's impedances may be increased, thus reducing required drive currents. Similarly, bias currents may be lowered, thus reducing the maximum signal in handling capability.

[0047] The minimum power dissipation for a circuit is proportional to the required maximum signal-to-noise ratio, which is the ratio between Smax 212 or 262 and N 214 and 264. Thus, a circuit receiving an input similar to the one shown in Figure 2A can dissipate less power than one receiving the input as shown in Figure 2B, while still achieving an acceptable bit-error rate.

[0048] Figure 3 illustrates what can occur when the maximum signal handling capability Smax 314 is reduced in the worst-case condition, that is when a weak desired signal 306 is accompanied by large interferers 310 and 312. Again, signal strength is plotted along a Y-axis 304 as a function of frequency along X-axis 302. In this specific example, Smax 314 is reduced below the peak levels of the interferers 310 and 312. Since Smax is low, the circuit cannot handle the interferers linearly. The resulting nonlinearities lead to a mixing of the interferers and the creation of intermodulation products 308 (for example, a third-order intermodulation distortion, IM3), one of which in this example occurs at the same frequency as the desired signal 306. As can be seen, if the intermodulation products 308 become excessive, the received signal bit error rate may become excessive, and the desired signal 306 may be lost. Accordingly, while

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Smax may be lowered even under some unfavorable conditions in order to reduce power, care should be taken to avoid corruption of the received desired signal.

[0049] Figure 4 illustrates a portion of a receiver consistent with an embodiment of the present invention. Included is a filter 430. An optional gain element 420 is placed in front of the filter 430 in order to increase signal levels. Signal strength indicator circuits 440 and 450 are connected to input line 410 and output line 460. In this specific example, the input signal spectrum on line 410 is shown as desired signal 412 and interferers 414 and 416. The signal spectrum at the output line 460 is shown as desired signal 462 and interferers 464 and 466. The signal strength indicators 440 and 450 do not provide information as to the relative sizes of the desired and interfering signals. Rather, a cumulative signal level is provided at their outputs. For example, the first signal strength indicator 440 outputs a level corresponding to the sum of desired signal 412 and interfering signals 414 and 416, while the second signal strength indicator 450 provides a signal level corresponding to the sum of desired signal 462 and interfering signals 464 and 466. In this specific example, the gain of the gain and filter circuit combinations is shown as approximately one, while the interfering signals 414 and 416 signal levels are reduced.

[0050] A comparison of the signal levels provided by the signal strength indicators 440 and 450 indicates that much of the combined received signal on line 410 has been filtered. Accordingly, it may be deduced that large interfering signals present at the input are being filtered by the filter 430. From this information, as will be shown in greater detail below, the bias, impedance, and gain of the gain stage 420 and filter 430 combination may be optimized to reduce power dissipation.

[0051] There are several real world situations where the received signal is better than the worst-case condition such that power can be saved. For example, large interferers may be present only part of the time, that is, on a temporary or transient basis. The interfering equipment may be some distance from the transceiver, or it may be operating in the low power mode. Also, the desired signal may be very strong as compared to the noise and interferers, for example a hub, router, or access point may be nearby.

[0052] Some transceivers consistent with embodiments of the present invention are designed to work with more than one data transfer specification or standard. In this case, when a transceiver is operating in a mode having a lower data rate, the power saving techniques described here may be employed.

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[0053] Figure 5 illustrates the relationship between a required biased current 516 for a given output signal 514 for a representative circuit 510. If the output signal current level is relatively low, such as the output current shown as 526, the corresponding bias current 528 may be low. Conversely, if the output signal current level is larger as with the example 536, the corresponding bias current level 538 should also be high. Accordingly, if a bias current is initially set high to handle large a large input signal, for example a large interferer, this current may be reduced if the input signal is smaller.

[0054] There are many ways by which these bias currents can be reduced. For example, the current may be generated by placing a voltage across a resistor by applying a bias voltage to the base of a device whose emitter is connected to ground through a resistance. In this case, the resistor may be increased by opening switches across portions of the resistance, or lowering the bias voltage applied at the base. Several ways in which this may be done will be readily understood by one skilled in the art.

[0055] Figure 6 is an example of how a circuit's impedances may be scaled to reduce drive currents, and, depending on the circuit configuration used, associated bias currents as well. A driver 612 has a load R 614 and C 616. The frequency response of this circuit is the same as that seen by driver 622, which drives an impedance of 2R 624 and C/2 626. But the impedance of the load seen by driver 622 is double that seen by 612, thus the output current required by the driver 622 is reduced by one-half.

[0056] As an example, the output stage of each of these drivers may be a Class A emitter follower formed by an emitter follower connected to a current source. When the outputs are driven high, the emitter of driver 622 need supply only one-half the drive current as driver 612. In this way, an impedance can be scaled in order to decrease a circuit's required drive current.

[0057] Also, the discharge current for driver 622 is only one half that of driver 612 for a given negative-going slew rate. Thus, the current source of 622 may be reduced by the same factor of one-half as compared to driver 612. In this example, the bias current, that is the current in the pull-down current source can be reduced. Many other examples where drive currents and possibly bias currents may be reduced will be appreciated by one skilled in the art.

[0058] Figure 7 illustrates another degree of freedom that made be employed to reduce current levels in a transceiver. Specifically, a gain element 720 may be inserted in front of a circuit block 730 in order to improve the combined circuit's signal-to-noise ratio by a factor equal to the

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gain of the inserted gain block. This is particularly useful when large interferers are absent and the desired received signal is moderate or low. Specifically, gain is added to the signal while impedances are increased, which raise the noise floor. In this way, a given signal-to-noise ratio may be maintained while the power is decreased.

[0059] The gain of such an element may be varied by increasing a current in a differential pair or increasing a load resistance using switches. Many other examples where the gain of this element may be varied will be appreciated by one skilled in the art.

[0060] These variables, or degrees of freedom, specifically reducing bias currents, increasing impedances, and increasing gain may be used as in the following examples.

[0061] Figure 8A is a block diagram of a functional block 820 and optional gain element 810 in accordance with an embodiment of the present invention. Functional block 820, like the functional blocks in the following diagrams, may be a filter, mixer, amplifier, or other circuit or circuits in a wireless transceiver or other electronic circuits or system. An input signal is received on line 812 by the optional gain element 814. When the optional gain block 810 is not used, the input signal may be received directly by the function block 820. The gain of the optional gain element 812 is controlled by a gain control signal on line 814. The functional block receives an output signal from the optional gain element 810 and provides an output VOUT on line 822. The lines in this and the other included figures may be one or more lines, depending on whether single-ended, differential, or other type of signaling is employed.

[0062] One or more impedances are under control of signals on impedance control lines 824. Similarly, one or more bias currents in the function block are under control of one or more signals on bias control lines 826. These various control lines may be logic signals, analog signals, voltage or currents lines, or other signal or bias lines. In other embodiments of the present invention, the gain control element 810 may be included in the function block 820. Also, various embodiments may not incorporate either or both the impedance control and bias control.

[0063] Figure 8B is an example input that may be present on line VIN 812. In this example, a desired signal 836 is relatively weak, as are interfering signals 837 and 838. The initial bias and circuit configuration is such that the noise floor 833 and maximum signal handling capability Smax 831 are adjusted for worst case conditions. The circuit of Figure 8A, as with all the circuits described here, receives noise at its input which may be referred to as input equivalent noise or input referred noise. Additionally, the circuit of Figure 8A generates noise which is

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added to the input referred noise. Depending on the gain characteristics of the circuitry, the output noise at various frequencies may be greater than, equal to, or less than the input referred noise. For simplicity, the noise floor and maximum signal handling capability Smax, in this and the other figures, are shown as straight lines, though the noise and Smax are typically curved as a function of frequency.

[0064] That the input spectrum is as shown in Figure 8B can be determined, for example, by low signal strength indications on line VIN 812 and VOUT 822. That is, a low level signal strength indication on line VIN 812 indicates that no portion of the input signal is particularly large.

[0065] For this exemplary input, there are at least two methods by which the power dissipation for this circuitry may be reduced. Depending on the exact circuits and structures used, one of these methods may be preferred.

[0066] In Figure 8C, the bias current is decreased, thereby lowering the maximum signal handling capability 841 as compared to 831, closer to the desired and interfering signal levels. Again, the bias currents in the function block 820 may be reduced by switching impedances that appear across a voltage thereby changing a resulting bias current, by reducing a voltage at the gate of a MOS or base of a bipolar transistor, or by other methods.

[0067] In Figure 8D, a second method of reducing power dissipation in the function block 820 is employed. Specifically, Smax 851 is held constant as compared Smax 831. The desired and interfering signals are amplified such that they are closer to the available signaling handling capability 851. Also, the noise floor 853 is raised as compared to noise floor 833 in Figure 8B. Specifically, the noise contributed by the function block 820 is increased, such that the noise at its output is increased to noise floor 853. This is done by increasing one or more impedance in function block 810, such that drive currents inside that block are reduced. Depending on the exact configuration, this may also allow some biasing currents to be reduced, while maintaining the maximum signal handling capability 851 at a sufficient level. Alternately, these two methods of reducing power dissipation in function block 820 may be done in combination.

[0068] The included examples are explained for the exemplary situation where biasing and other parameters are set for worst-case conditions, and then changed to save power when it is discovered that the conditions are better-than-worst case. Alternately, the bias currents and other

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parameters may be set for maximum power savings, or an intermediate point, and the power can be adjusted from there.

[0069] Figure 9A illustrates a block diagram including an optional gain element 910 and function block 920. Again, an input signal is received on line 912 by optional gain element 910 which in turn drives function block 920. The function block provides an output VOUT on line 922, and receives impedance and bias control signals on lines 924 and 926.

[0070] Figure 9B shows the spectrum for what may be considered a best-case received signal. Specifically, the desired signal 936 is strong, while the interfering signals 937 and 938 are relatively weak. This may be determined, for example, by detecting a large signal level at the input line VIN 812 and a large signal level after a filter, since these readings would indicate that a large signal is received, but that it is at the desired signal frequency.

[0071] The maximum signaling capability 931 and noise floor 933 are shown as being set for the worst case conditions. In this case, the noise floor 933 is lower than the maximum allowed for proper signal reception. Accordingly, one or more impedance in the function block 920 may be increased, such that the noise floor 943 rises as shown in Figure 9C. In this way one or more the driving currents in the function block 920 may be reduced. Similarly, since the drive current is reduced, one or more bias current may also be reduced, depending on the exact circuit configuration.

[0072] Figure 10A illustrates a block diagram showing an optional gain element 1010 driving a function block 1020. An input signal is received by the gain element 1010 on line 1012, and an output is provided by function block 1020 on line VOUT 1022. One or more gain control signals present on lines 1014 control the gain of gain control element 1010, while one or more impedance and bias control signals are received by the function block 1020 on line to 1024 and 1026.

[0073] Figure 10B illustrates a received signal that may be received on line VIN 1012. In this example, the desired signal 1036 and interferers 1037 and 1038 are each relatively large. This may be determined, for example, by detecting a large signal level at the input line VIN 812 and a smaller signal level after a filter, since these readings would indicate that a large signal is received, but that interferers are being reduced.

[0074] As before, in this example, the noise floor 1033 and maximum signal handling capability 1031 are initially set for the worst case conditions. Since the desired signal is

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relatively large in this case, the noise floor may be allowed to rise, a shown by noise floor 1043 in Figure 10C. Since the desired signal 1046 and interferers 1047 are large, the maximum signal handling capability Smax 1041 remains constant. Again, the noise floor is increased by increasing impedances in the function block 1020. This reduces the required drive current, and may also allow for a reduction in bias currents.

[0075] Figure 11A illustrates a block diagram including an optional gain element 1110 and function block 1120 in accordance with an embodiment of the present convention. An input signal is received on line 1112 by the optional gain control element 1110, while an output signal is provided by the function block 1120 on line VOUT 1122. Gain, impedance, and bias control signals are received on lines 1114, 1124, and 1126.

[0076] Figure 11B is an exemplary input signal that may be received by the gain control element 1110 on line VIN 1112. In this specific example, the desired signal 1136 is relatively low or weak while the interfering signals 1137 and 1138 are large. This may be determined, for example, by detecting a large signal level at the input line VIN 812 and a much smaller signal level after a filter, since these readings would indicate that a large signal is received and that large interferers are being reduced such that the resulting signal, the desired signal, is relatively weak.

[0077] Again, the maximum signal handling capability 1131 and noise floor 1133 are initially set for worst case conditions. If the desired signal is sufficiently low, while the interferers are sufficiently high, power savings may not be achievable over the worst case settings, since this is in fact the worst case condition. But, if the desired signal is somewhat larger than the worst case condition, then power may be saved in at least two different ways.

[0078] For example, Figure 11C shows the maximum signal handling capability 1141 being lowered. In this case, the interfering signals 1147 in 1148 began to clip and distort, thereby creating intermodulation products 1145, which distort the desired signal 1146. So long as care is taken to not corrupt the desired signal 1146 beyond an acceptable limit, typically measured by a bit-error rate, power may be reduced in this way.

[0079] Similarly, in Figure 11D, the noise floor 1153 is raised somewhat, thereby saving power. Again, this may be done so long as the noise floor is not sufficiently high that the system bit-error rate becomes unacceptable.

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[0080] Figure 12 is a summary of the above four examples. The received signal strengths are shown in column 1210, while appropriate power saving responses are listed in column 1220. Specifically, in row 1230, the desired signal and interferer signal strengths are both weak or small. In this case, proper responses include decreasing Smax, or increasing one or more circuit impedances while increasing the circuit gain. Depending on the exact circuit configuration, one of these options may be preferred over the other. Alternately, they may be done in combination, or done in combination with other power saving techniques. Also, in some specific embodiments, when both desired signal and interferer signal strengths are small, the gain may need to be increased while the impedance is maintained or not increased in order to keep the noise floor low.

[0081] In row 1240, the desired signal strength is strong or large, while the interfering signals are small. In this case, an appropriate response is to increase one or more of the circuit impedances. Again, depending on the exact circuit in question, one or more of the bias currents may also be reduced.

[0082] In row 1250, both the desired signals and interfering signal strengths are large. Again, in this case an appropriate response is to increase one or more of the circuit impedances.

[0083] In row 1260, the received desired signal strength is weak or small, while the interfering signals are large. Since this is the worst case situation for which the circuit is designed, substantial power savings are difficult to achieve. However, again, if the received signal is above a minimum level necessary for proper operation, some distortion of the interferers or raising of the noise floor may be acceptable.

[0084] It should be noted that not all possible signal conditions are listed here. For example, either the signal or interferer may be of a relatively medium strength, or the interferer may be absent. Also, these terms are for exemplary purposes and are not meant to convey specific signal conditions, but rather are only qualitative. The proper response to a specific condition depends on the embodiment of the present invention, the particular circuit topology, the requirements of the signaling standard used, as well as other constraints.

[0085] Figure 13 is an example shown how power may be saved as a function of time by employing one or more of these methods consistent with embodiments of the present invention. Power is plotted along a Y-axis 1304 as a function of time along X-axis 1302. Conventional worst case design would fix power dissipation at line 1310. As can be seen, dynamic power

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dissipation 1320 under the control of variable gains, impedances, biasing, or combination thereof, allows for a lower average power 1330 as compared to the power dissipated 1310 by the conventional design.

[0086] Figure 14 is a block diagram of a portion of a receiver consistent with an embodiment of the present invention. Included are low-noise amplifier 1410, mixer 1420, gain stage 1430, filter 1440, AGC amplifier 1450, and VCO 1460. Signal strength detection is done at the output of the low-noise amplifier by signal strength indicator 1470, at the output of the mixer by signal strength indicator 1472, and at the output of the filter by signal strength indicator 1474. The outputs of the signal strength indicator circuits are received by the computational circuit 1470, which in turn controls gain and power control circuits 1480 and 1485. Power and gain control circuits 1480 and 1485 control the gain, biasing, and impedance levels of the circuits in the receiver signal path. Also, the gain and power control circuits may control the same parameters in the VCO 1460. This figure is greatly simplified for purposes of explanation. For example, the quadrature nature of the mixers and following circuits are not shown. Also, power-down and start-up circuits are not included.

[0087] The current level in the low-noise amplifier determines a multitude of parameters including voltage gain, linearity, input impedance matching, and noise figure. When conditions are better than worst-case, some of these parameters may be relaxed while maintaining an acceptable bit-error rate, thus saving power.

[0088] The bias current in the mixers effect that block's noise figure and linearity. Care is taken in reducing power in this block so as not to increase nonlinearities, particularly the third-order nonlinearity as measured by IP3, the third-order intercept point, beyond an acceptable limit.

[0089] A key parameter of the VCO is phase noise, an increase in which increases the sidebands on either side of the oscillation signal. During transmission, the phase noise should be kept low to avoid interference with adjacent channels and for preserving modulation information.

[0090] During reception however, if the conditions are better than worst case, the phase noise requirement for the VCO is relaxed, and power can be saved consistent with embodiments of the present invention. The achievable phase noise power spectral density is approximately inversely proportional to the bias current used. Thus, when low phase noise is not required during reception, bias current in the VCO can be reduced.

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[0091] Most of the power savings in a transceiver in accordance with embodiments of the present invention is achieved in the receiver portion. Additional power may be saved in the transmitter section.

[0092] Figure 15 is a block diagram of a transmitter portion consistent with an embodiment of the present invention. Included is a signal path formed by gain stage 1510 and power amplifier 1520. The output power level is sensed by output level sensing circuit 1550, which in turn adjusts the biasing of the power amplifier 1520 through the power control circuit 1540. Additionally, a transmitter level control signal is received by power control circuits 1530 and 1540, which in turn control the biasing of gain stage 1510 and power amplifier 1520. Gain control circuit 1560 also adjusts the gain of gain stage 1510 and power amplifier 1520. Additional circuitry that varies impedances in each of these circuits may also be included.

[0093] Since the gain, impedance and biasing of these blocks are being dynamically varied, care must be taken to not negatively affect the signal being processed. For example, specific embodiments of the present invention perform some or all of these variations during preamble. Also, as changes occur, the circuits in some embodiments are limited such that they may only adapt to an improvement in conditions after frames are completed. If conditions worsen, the circuits may be allowed to change in order to save the data. Alternately, a system may be manually calibrated, for example at set up, and when the network configuration is changed.

[0094] The above description of specific embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form described, and many modifications and variations are possible in light of the teaching above. The embodiments were chosen and described in order to best explain the principles of the invention and its practical applications to thereby enable others skilled in the art to best utilize the invention in various embodiments and with various modifications as are suited to the particular use contemplated.

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WHAT IS CLAIMED IS:

1. A method of receiving a signal using an integrated circuit, the integrated circuit comprising a signal path including a low-noise amplifier configured to receive the signal, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer, the method comprising:

determining a first signal strength at a first node in the signal path in the integrated circuit; and

dynamically changing an impedance of a component in the signal path based on the first signal strength.

2. The method of claim 1 wherein the signal comprises a preamble portion and a data portion, the impedance of a component is changed while receiving the preamble portion, and the method further comprises receiving the data portion of the signal.

3. The method of claim 2 further comprising:

determining a second signal strength at a second node in the signal path, wherein the second node in the signal path is after the first node in the signal path.

4. The method of claim 3 wherein the impedance of the component in the signal path is also changed based on the second signal strength.

5. The method of claim 2 wherein the component in the signal path comprises a MOS transistor.

6. The method of claim 2 wherein the component in the signal path comprises a resistor.

7. The method of claim 2 wherein the component in the signal path comprises a capacitor.

8. The method of claim 4 wherein the component in the signal path is included in the mixer.

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9. The method of claim 4 wherein the component in the signal path is included in the low-pass filter.

10. A method of receiving a signal comprising a preamble portion and a data portion using an integrated circuit, the integrated circuit comprising a signal path including a low-noise amplifier configured to receive the signal, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer, the method comprising:

determining a first signal strength at a first node in the signal path in the integrated circuit; and

while receiving the preamble portion of the signal, dynamically changing a bias current in the signal path based on the first signal strength.

11. The method of claim 10 wherein the method further comprises receiving the data portion of the signal.

12. The method of claim 11 further comprising:

determining a second signal strength at a second node in the signal path, wherein the second node in the signal path is after the first node in the signal path.

13. The method of claim 12 wherein the bias current in the signal path is also changed based on the second signal strength.

14. The method of claim 11 wherein the bias current is a bias current for the low-noise amplifier.

15. The method of claim 11 wherein the bias current is a bias current for the mixer.

16. The method of claim 11 wherein the bias current is a bias current for the low-pass filter.

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17. A method of receiving a signal using an integrated circuit, the integrated circuit comprising a signal path including a first circuit and a second circuit having an input coupled to an output of the first circuit, the method comprising:

determining a first signal strength at a first node in the signal path in the integrated circuit, wherein the first node is before the first circuit in the signal path;

dynamically changing a gain of the first circuit based on the first signal strength; and

dynamically changing an impedance of a component in the second circuit based on the first signal strength.

18. The method of claim 17 wherein the signal comprises a preamble portion and a data portion, the gain and impedance are changed while receiving the preamble portion, and the method further comprises receiving the data portion of the signal.

19. The method of claim 18 further comprising:

determining a second signal strength at a second node in the signal path, wherein the second node in the signal path is after the second circuit in the signal path.

20. The method of claim 19 wherein the gain of the first circuit and impedance of the component in the second circuit is also changed based on the second signal strength.

21. The method of claim 18 wherein the first circuit is a low-noise amplifier.

22. The method of claim 18 wherein the first circuit is a mixer.

23. A wireless transceiver integrated circuit comprising:

a receiver comprising a signal path, the signal path comprising:

a low-noise amplifier;

a mixer having an input coupled to an output of the low-noise amplifier; and

a low-pass filter having an input coupled to an output of the mixer; and

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a first signal strength indicator circuit coupled to the signal path, and configured to determine a first signal strength;

wherein an impedance in the signal path is configured to be dynamically adjusted in response to the first signal strength.

24. The wireless transceiver of claim 23 further comprising:

a second signal strength indicator circuit coupled to the output of the mixer, and configured to determine a second signal strength,

wherein the first signal strength indicator is coupled to the output of the low-noise amplifier, and

wherein the impedance in the signal path is configured to be adjusted in response to the first and second signal strengths.

25. The wireless transceiver of claim 23 further comprising:

a second signal strength indicator circuit coupled to the output of the low-pass filter, and configured to determine a second signal strength,

wherein the first signal strength indicator is coupled to the output of the mixer, and

wherein the impedance in the signal path is configured to be adjusted in response to the first and second signal strengths.

26. A wireless transceiver integrated circuit comprising:

a receiver comprising a signal path, the signal path comprising:

a low-noise amplifier;

a mixer having an input coupled to an output of the low-noise amplifier; and

a low-pass filter having an input coupled to an output of the mixer; and

a first signal strength indicator circuit coupled to the signal path, and configured to determine a first signal strength, the first signal strength the strength of a signal comprising a preamble portion and a data portion;

wherein a bias current in the signal path is configured to be dynamically adjusted during the preamble portion of the signal in response to the first signal strength.

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27. The wireless transceiver of claim 26 further comprising:

a second signal strength indicator circuit coupled to the output of the mixer, and configured to determine a second signal strength,

wherein the first signal strength indicator is coupled to the output of the low-noise amplifier, and

wherein the bias current in the signal path is configured to be adjusted in response to the first and second signal strengths.

28. The wireless transceiver of claim 26 further comprising:

a second signal strength indicator circuit coupled to the output of the low-pass filter, and configured to determine a second signal strength,

wherein the first signal strength indicator is coupled to the output of the mixer, and

wherein the bias current in the signal path is configured to be adjusted in response to the first and second signal strengths.

29. A wireless transceiver integrated circuit comprising:

a receiver comprising a signal path, the signal path comprising:

a first circuit; and

a second circuit having an input coupled to an output of the first circuit; and

a first signal strength indicator circuit coupled to the signal path, and configured to determine a first signal strength;

wherein a gain of the first circuit is configured to be dynamically adjusted in response to the first signal strength, and

wherein an impedance in the second circuit is configured to be dynamically adjusted in response to the first signal strength.

30. The wireless transceiver of claim 29 further comprising:

a transmitter comprising:

a power amplifier; and

an output-level-sensing circuit coupled to an output of the power amplifier,

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wherein the output-level-sensing circuit is configured to dynamically adjust a gain of the power amplifier.

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POWER DISSIPATION REDUCTION IN WIRELESS TRANSCEIVERS

ABSTRACT OF THE DISCLOSURE

Methods and circuits for reducing power dissipation in wireless transceivers and other electronic circuits and systems. Embodiments of the present invention use bias current reduction, impedance scaling, and gain changes either separately or in combination to reduce power dissipation. For example, bias currents are reduced in response to a need for reduced signal handling capability, impedances are scaled thus reducing required drive and other bias currents in response to a strong received signal, or gain is increased and impedances are scaled in response to a low received signal in the presence of no or weak interfering signals.

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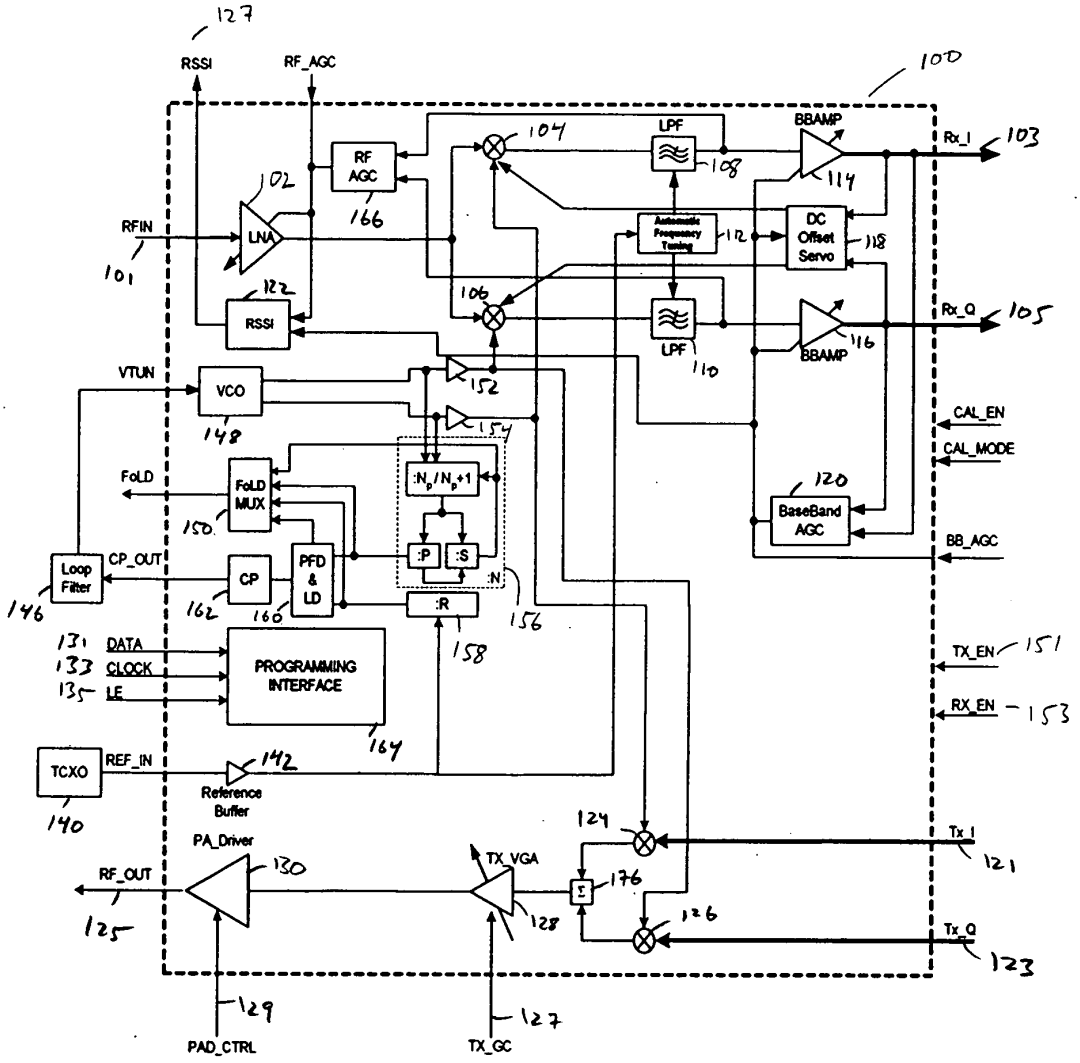

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Automatic Frequency Tuning
112
DC Offset Servo
118
122
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LPF
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BBAMP
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VTUN
VCO
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152
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BB_AGC
CP_OUT
Loop Filter
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:P
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:N
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:R
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133 CLOCK
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PA_Driver
130
RF_OUT
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Tx_Q
123
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PAD_CTRL
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TX_GC

FIGURE 1

FIGURE 2B

FIGURE 2A

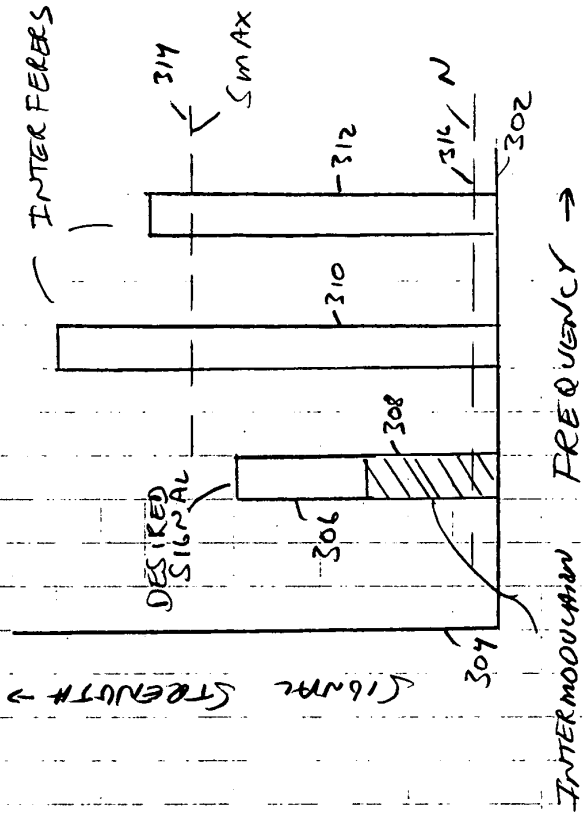

INTERFERERS
314
SMAX
312
316
N
302
310
308
306
304
DESIRED SIGNAL
FREQUENCY →
INTERMODULATION PRODUCTS
LINEAR STRENGTH →

FIGURE 3

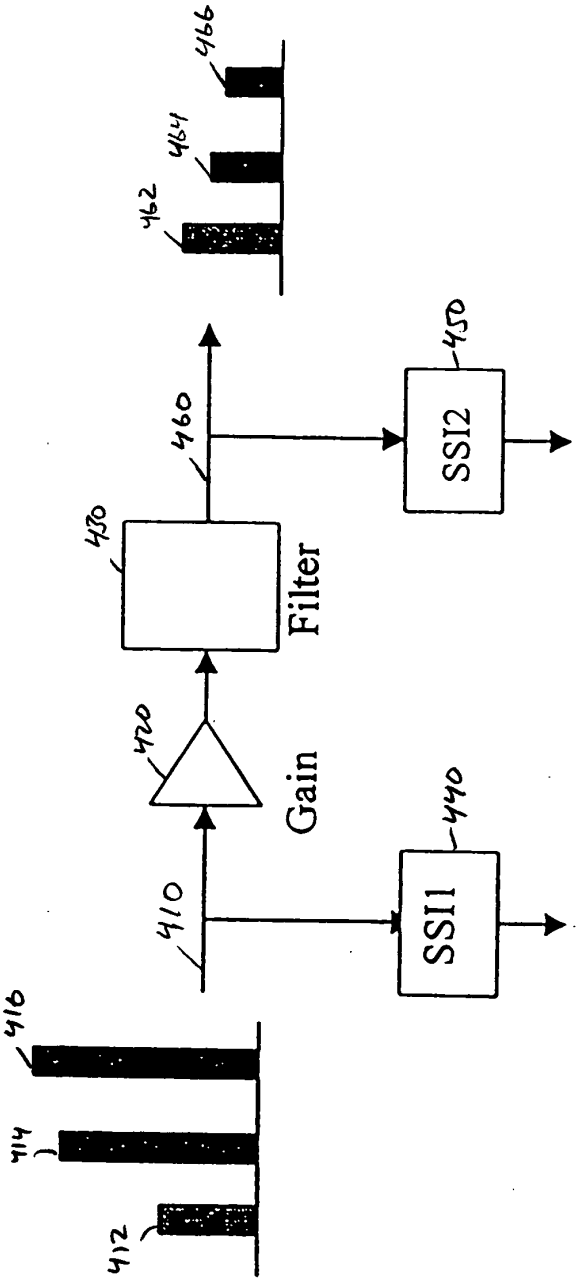

416
414
412
410
SSI1
440
420
Gain
430
Filter
460
SSI2
450
466
464
462

Figure 4

Iout
514
510
Ibias
516
Iin
512
Ibias
528
Iout
526
522
524
Ibias
538
Iout
536
532
534
t
t

FIGURE 5

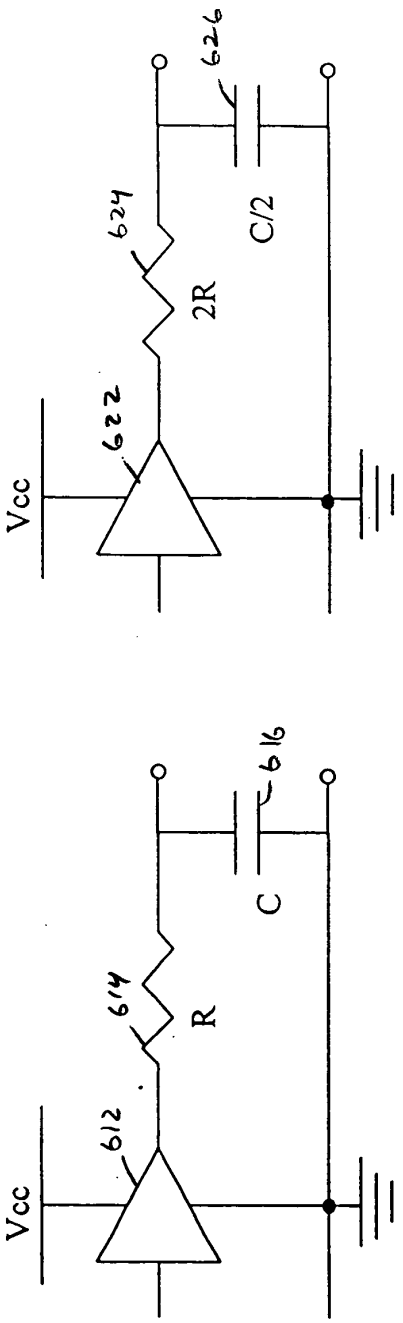


FIGURE 6

Noise level N
710
Sin
712
Signal-to-noise ratio Sin/N
Noise level N
730
732
ASin
724
A
720
Sin
722
Signal-to-noise ratio ASin/N

Figure 7

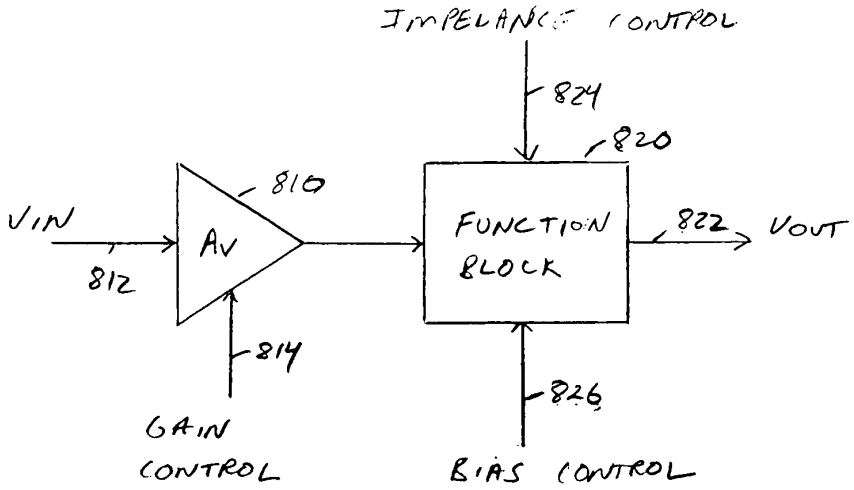


FIGURE 8A

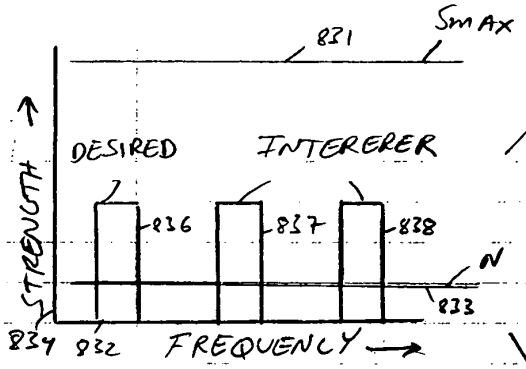


FIGURE 8B

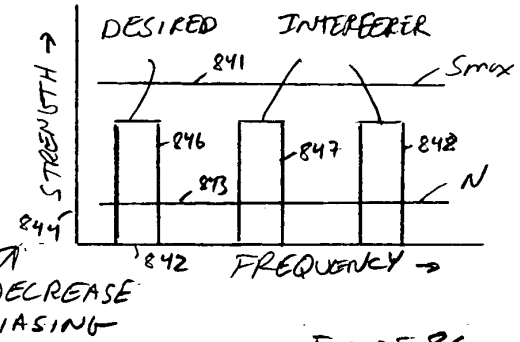


FIGURE 8C

DECREASE BIASING

-AND/OR-

INCREASE GAIN AND IMPEDANCES

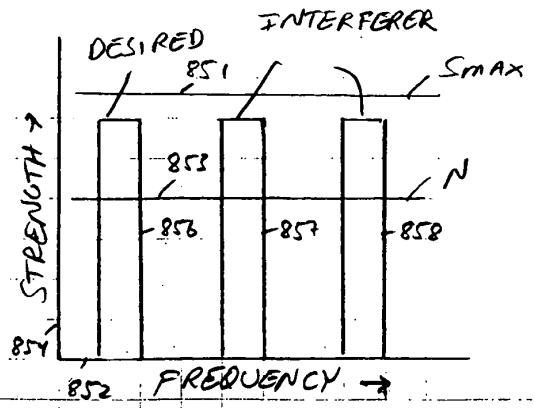


FIGURE 8D

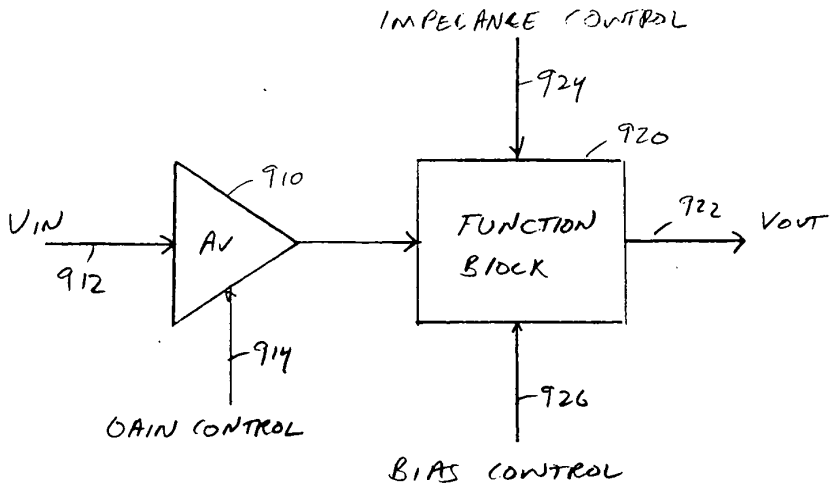


FIGURE 9A

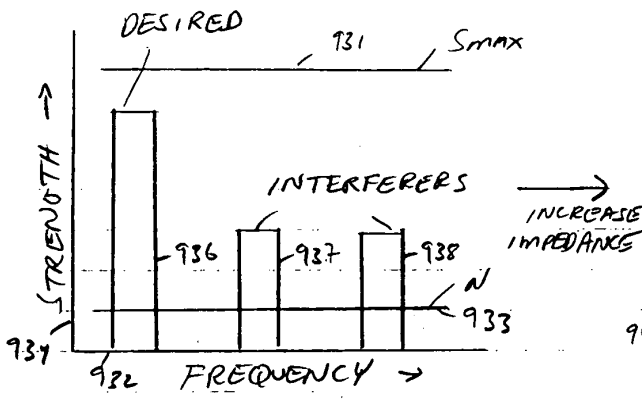


FIGURE 9B

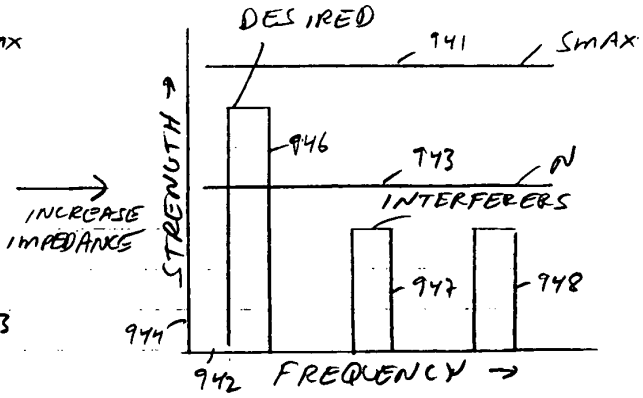


FIGURE 9C

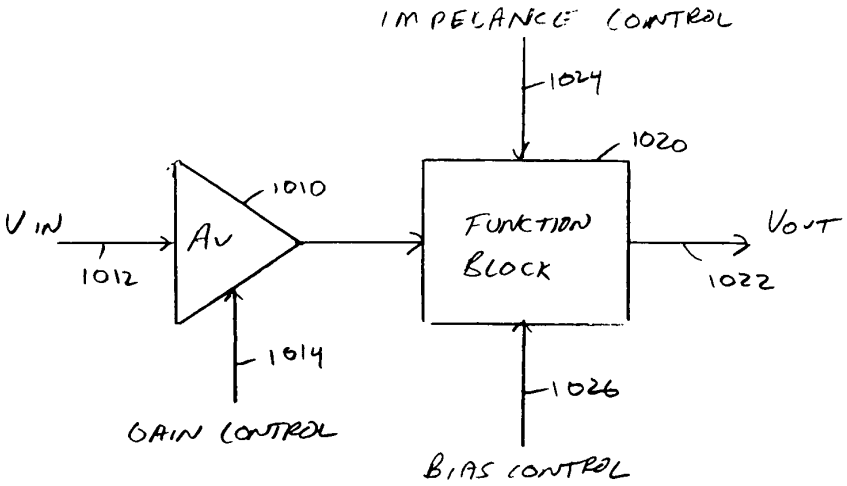


FIGURE 10A

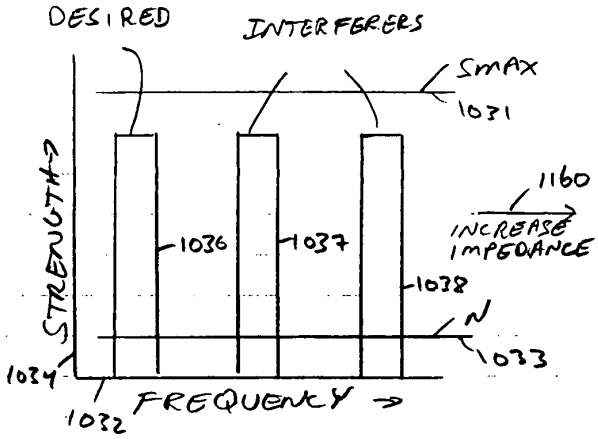


FIGURE 10B

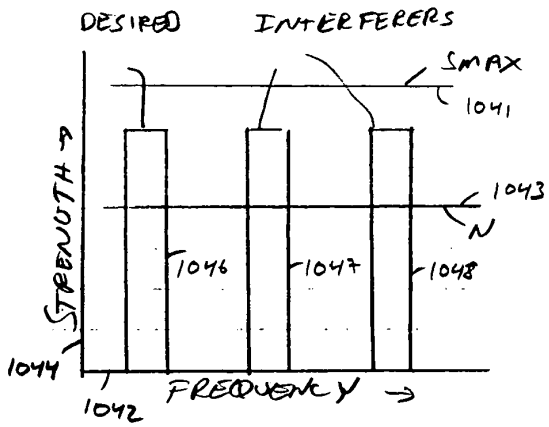


FIGURE 10C

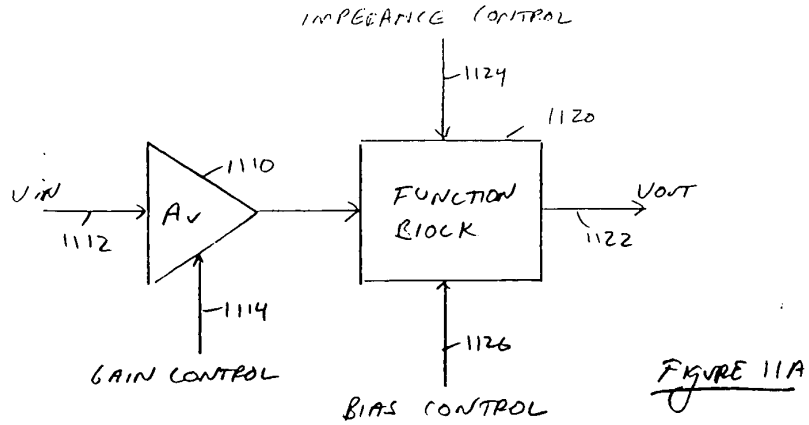


FIGURE 11A

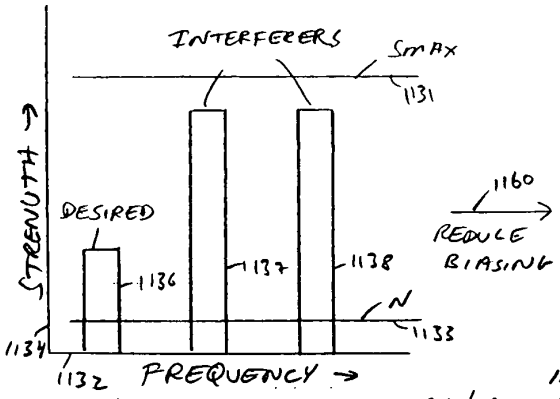


FIGURE 11B

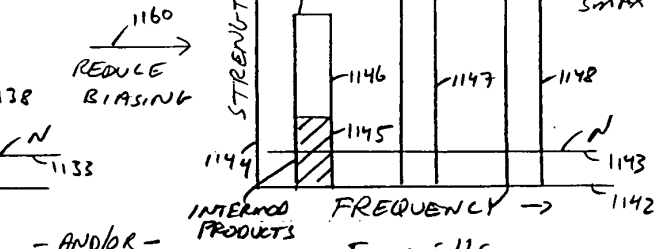


FIGURE 11C

- AND/OR -

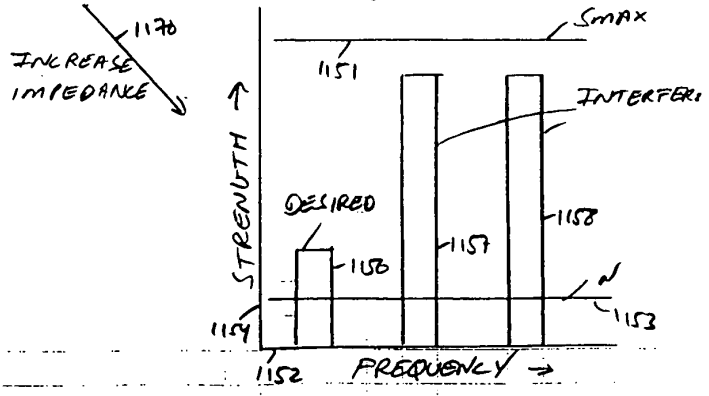


FIGURE 11D

	1210 RECEIVED SIGNAL		1220 RESPONSE TO RECEIVED SIGNAL		
	SIGNAL STRENGTH	INTERFERER STRENGTH	DECREASE SMAX	INCREASE IMPEDANCE NOT GAIN	INCREASE IMPEDANCE AND GAIN
1230	SMALL	SMALL	YES	NO	YES
1240	LARGE	SMALL	NO	YES	NO
1250	LARGE	LARGE	NO	YES	NO
1260	SMALL	LARGE	NO	NO	NO

Figure 12

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IPR2023-00819
Theta EX2019

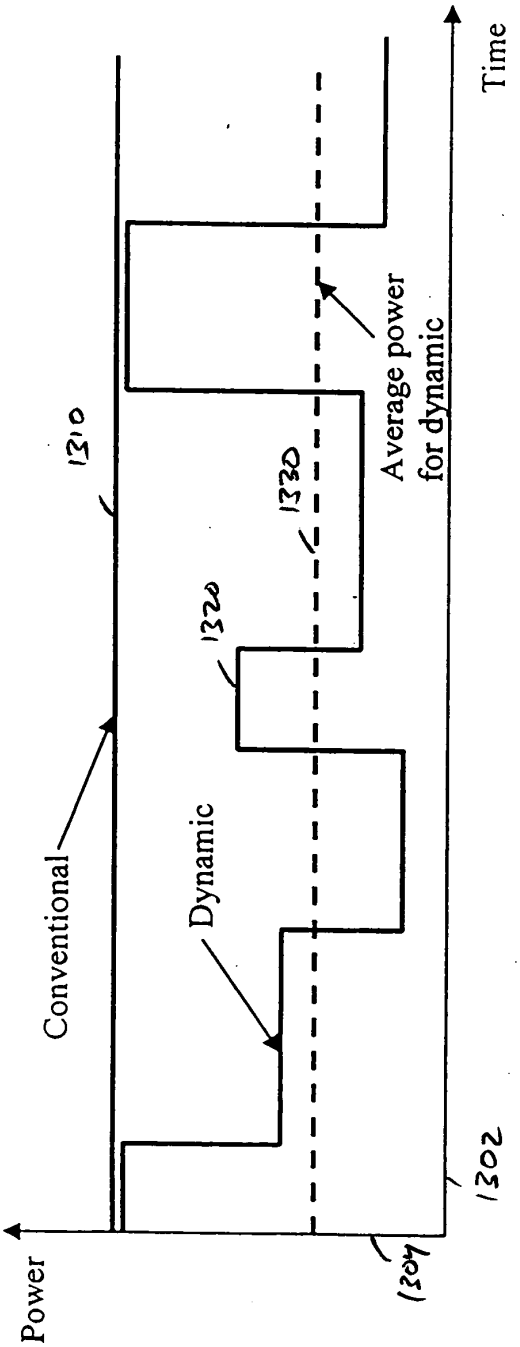

Power
Time
Conventional
Dynamic
Average power
for dynamic
1310
1320
1330
1302
1304

Figure 13

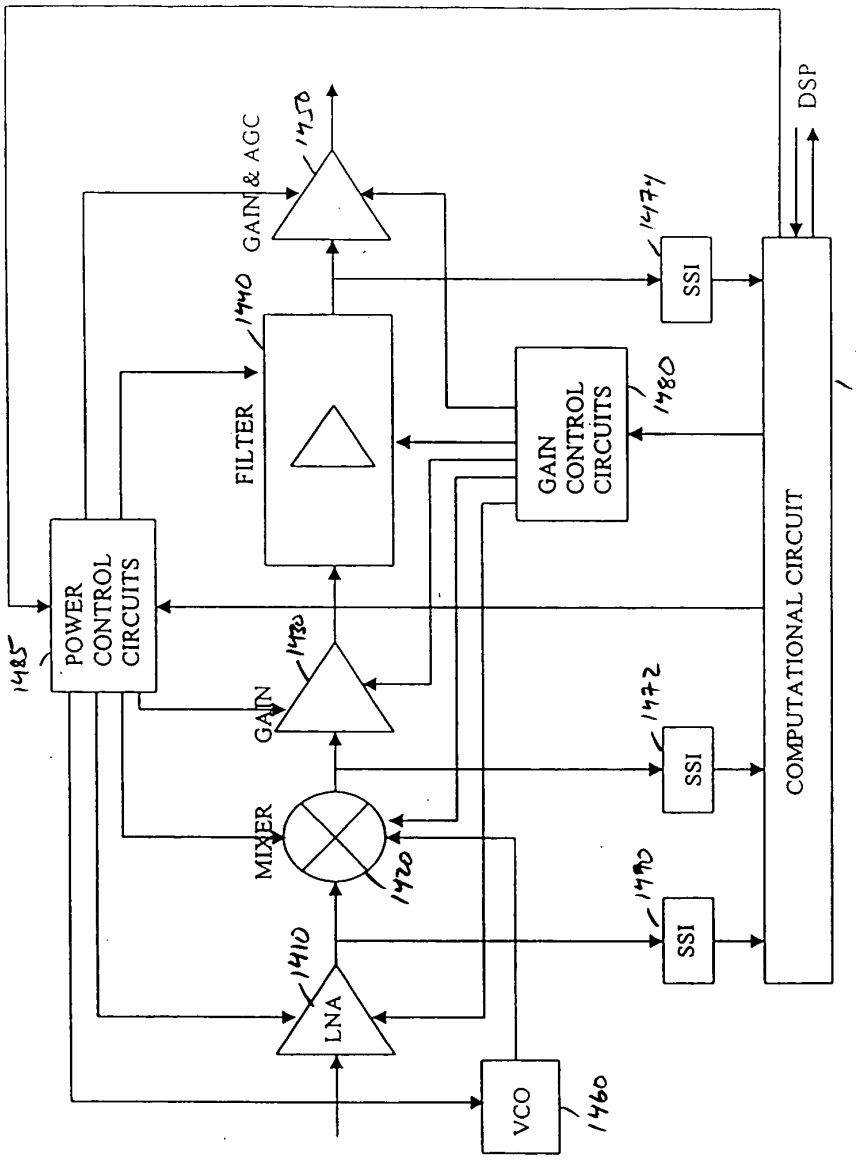

DSP
GAIN & AGC
1450
1471
SSI
1440
FILTER
1480
GAIN CONTROL CIRCUITS
1490
COMPUTATIONAL CIRCUIT
1485
POWER CONTROL CIRCUITS
1430
GAIN
1472
SSI
MIXER
1420
1470
SSI
1410
LNA
VCO
1460

FIGURE 14

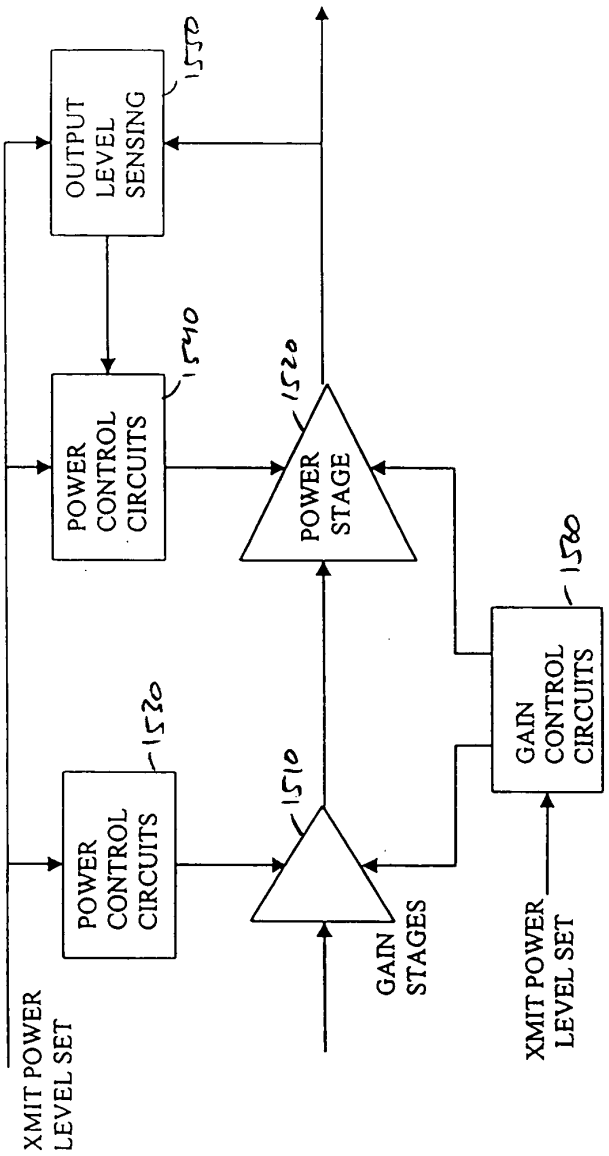

OUTPUT LEVEL SENSING
1530
POWER CONTROL CIRCUITS
1540
POWER STAGE
1520
POWER CONTROL CIRCUITS
1550
GAIN CONTROL CIRCUITS
1580
GAIN STAGES
1510
XMIT POWER LEVEL SET
XMIT POWER LEVEL SET

Figure 15

Attorney Docket No.: 021673-000210US
Client Ref. No.:

PTO/SB/01A (08-03)

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention POWER DISSIPATION REDUCTION IN WIRELESS TRANSCEIVERS

As the below named inventor(s), I/we declare that:

This declaration is directed to:

☒ The attached application, or

☐ Application No. , filed on ,

☐ as amended on _____ (if applicable);

I/we believe that I/we am/are the original and first inventor(s) of the subject matter which is claimed and for which a patent is sought;

I/we have reviewed and understand the contents of the above-identified application, including the claims, as amended by any amendment specifically referred to above;

I/we acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me/us to be material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

All statements made herein of my/our own knowledge are true, all statements made herein on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001, and may jeopardize the validity of the application or any patent issuing thereon.

FULL NAME OF INVENTOR(S)

Inventor 1	Yannis Tsividis	Date:	2-13-2004
Signature:	Yannis Tsividis	Citizen of:	Greece
Inventor 2		Date:	
Signature:		Citizen of:	
Inventor 3		Date:	
Signature:		Citizen of:	
Inventor 4		Date:	
Signature:		Citizen of:	

☐ Additional inventors are being named on additional form(s) attached hereto.

60139606 v1

BEST AVAILABLE COPY

Application Data Sheet

Application Information

Application number::	
Filing Date::	
Application Type::	Regular
Subject Matter::	Utility
Suggested classification::	
Suggested Group Art Unit::	
CD-ROM or CD-R??::	
Number of CD disks::	
Number of copies of CDs::	
Sequence Submission::	
Computer Readable Form (CRF)?::	
Number of copies of CRF::	
Title::	POWER DISSIPATION REDUCTION IN WIRELESS TRANSCEIVERS
Attorney Docket Number::	021673-000210US
Request for Early Publication::	No
Request for Non-Publication::	Yes
Suggested Drawing Figure::	
Total Drawing Sheets::	15
Small Entity?::	Yes
Latin name::	
Variety denomination name::	
Petition included?::	No
Petition Type::	
Licensed US Govt. Agency::	
Contract or Grant Numbers One::	
Secrecy Order in Parent Appl.::	No

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IPR2023-00819
Theta EX2019

Applicant Information

Applicant Authority Type::	Inventor
Primary Citizenship Country::	Greece
Status::	Full Capacity
Given Name::	Yannis
Middle Name::	
Family Name::	Tsividis
Name Suffix::	
City of Residence::	New York
State or Province of Residence::	NY
Country of Residence::	US
Street of Mailing Address::	410 Riverside Drive, Apt. 52A
City of Mailing Address::	New York
State or Province of mailing address::	NY
Country of mailing address::	US
Postal or Zip Code of mailing address::	10025

Correspondence Information

Correspondence Customer Number::	20350

Representative Information

Representative Customer Number::	20350

Domestic Priority Information

Application::	Continuity Type::	Parent Application::	Parent Filing Date::
This Application	An Appn claiming benefit under 35 USC 119(e) of	60/451,229	03/01/03

Foreign Priority Information

Country::	Application number::	Filing Date::

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Apple EX1002 Page 46
IPR2023-00819
Theta EX2019

Assignee Information

Assignee Name::	Theta Microelectronics Inc.
Street of mailing address::	2232 North First Street
City of mailing address::	San Jose
State or Province of mailing address::	CA
Country of mailing address::	US
Postal or Zip Code of mailing address::	95131

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IPR2023-00819
Theta EX2019

PATENT APPLICATION SERIAL NO. _____

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

02/27/2004 HDEMESS1 00000051 201430 10784613

01 FC:2001 385.00 DA
02 FC:2201 129.00 DA
03 FC:2202 90.00 DA

PTO-1556
(5/87)

*U.S. Government Printing Office: 2001 — 481-697/59173

PATENT APPLICATION FEE DETERMINATION RECORD
Effective October 1, 2003

Application or Docket Number: 10784613

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	30	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	30 minus 20=	* 10
INDEPENDENT CLAIMS	6 minus 3 =	* 3
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐ OR OTHER THAN SMALL ENTITY

RATE	FEE		RATE	FEE
BASIC FEE	385.00	OR	BASIC FEE	770.00
X$ 9=	90	OR	X$18=	
X43=	129	OR	X86=	
+145=		OR	+290=	
TOTAL	604	OR	TOTAL	

CLAIMS AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐				

SMALL ENTITY OR OTHER THAN SMALL ENTITY

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐				

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐				

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
***If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

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IPR2023-00819
Theta EX2019

16562 U.S.PTO 022304

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	021673-000210US
First Inventor	Tsividis, Yannis
Title	POWER DISSIPATION REDUCTION IN WIRELESS TRANSCEIVERS
Express Mail Label No.	EV 369 118 824 US

22278 U.S.PTO 10/784613 022304

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. ☒ Fee Transmittal Form (e.g., PTO/SB/17) *(Submit an original and a duplicate for fee processing)*
2. ☒ Applicant claims small entity status. See 37 CFR 1.27.
3. ☒ Specification [*Total Pages* 25] *(preferred arrangement set forth below)*
   - Descriptive title of the Invention
   - Cross Reference to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to sequence listing, a table, or a computer program listing appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
4. ☒ Drawing(s) *(35 U.S.C.113)* [*Total Sheets* 15]
5. Oath or Declaration [*Total Pages* 1]
   a. ☒ Newly executed (original or copy)
   b. ☐ Copy from a prior application (37 CFR 1.63 (d)) *(for a continuation/divisional with Box 18 completed)*
      i. ☐ DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
6. ☒ Application Data Sheet. See 37 CFR 1.76

ADDRESS TO

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

7. ☐ CD-ROM or CD-R in duplicate, large table or Computer Program *(Appendix)*
8. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. ☐ Computer Readable Form (CRF)
   b. Specification Sequence Listing on:
      i. ☐ CD-ROM or CD-R (2 copies); or
      ii. ☐ Paper number of pages
   c. ☐ Statements verifying identity of above copies

ACCOMPANYING APPLICATIONS PARTS

9. ☐ Assignment Papers (cover sheet & document(s))
10. ☐ 37 CFR 3.73(b) Statement *(when there is an assignee)* ☐ Power of Attorney
11. ☐ English Translation Document *(if applicable)*
12. ☐ Information Disclosure Statement (IDS)/PTO-1449 ☐ Copies of IDS Citations
13. ☐ Preliminary Amendment
14. ☒ Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
15. ☐ Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
16. ☒ Nonpublication Request under 35 U.S.C. 122 (b)(2)(B)(i). Applicant must attach form PTO/SB/35 or its equivalent
17. ☐ Other:

18. If a CONTINUING APPLICATION, *check appropriate box, and supply the requisite information below and in the first sentence of the specification following the title, or in an Application Data Sheet under 37 CFR 1.76:*

☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No: _____

Prior application information: *Examiner* _____ *Art Unit:* _____

For CONTINUATION OF DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 5b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

19. CORRESPONDENCE ADDRESS

☒ Customer Number **20350** *OR* ☐ Correspondence address below

Name					
Address					
City		*State*		*Zip Code*	
Country		*Telephone*		*Fax*	

Name (Print/Type)	J. Matthew Zigmant	*Registration No. (Attorney/Agent)*	44,005
Signature		*Date*	February 23, 2004

60142384 v1

PTO/SB/17 (10-03)

FEE TRANSMITTAL for FY 2004

Effective 10/01/2003. Patent fees are subject to annual revision.

☒ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 604

Complete if Known	
Application Number	
Filing Date	
First Named Inventor	Tsividis, Yannis
Examiner Name	
Art Unit	
Attorney Docket No.	021673-000210US

METHOD OF PAYMENT *(check all that apply)*

☐ Check ☐ Credit Card ☐ Money Order ☐ Other ☐ None

☒ Deposit Account:

Deposit Account Number: 20-1430

Deposit Account Name: Townsend and Townsend and Crew LLP

The Director is authorized to: *(check all that apply)*

☒ Charge fee(s) indicated below ☒ Credit any overpayments

☒ Charge any additional fee(s) or any underpayment of fee(s)

☐ Charge fee(s) indicated below, **except for the filing fee** to the above-identified deposit account.

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	770	2001	385	Utility filing fee	385
1002	340	2002	170	Design filing fee	
1003	530	2003	265	Plant filing fee	
1004	770	2004	385	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($)385

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

			Extra Claims	Fee from below	Fee Paid
Total Claims	30	-20** =	10	X $9 =	$90
Independent Claims	6	-3** =	3	X $43 =	$129
Multiple Dependent				X =	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	86	2201	43	Independent claims in excess of 3
1203	290	2203	145	Multiple dependent claim, if not paid
1204	86	2204	43	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($)219

***or number previously paid, if greater; For Reissues, see above*

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet.	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	420	2252	210	Extension for reply within second month	
1253	950	2253	475	Extension for reply within third month	
1254	1,480	2254	740	Extension for reply within fourth month	
1255	2,010	2255	1,005	Extension for reply within fifth month	
1401	330	2401	165	Notice of Appeal	
1402	330	2402	165	Filing a brief in support of an appeal	
1403	290	2403	145	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive – unavoidable	
1453	1,330	2453	665	Petition to revive – unintentional	
1501	1,330	2501	665	Utility issue fee (or reissue)	
1502	480	2502	240	Design issue fee	
1503	640	2503	320	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Petitions related to provisional applications	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	770	2809	385	Filing a submission after final rejection (37 CFR § 1.129(a))	
1810	770	2810	385	For each additional invention to be examined (37 CFR § 1.129(b))	
1801	770	2801	385	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	
				Other fee (specify) ----------	

*Reduced by Basic Filing Fee Paid **SUBTOTAL (3)** ($)

SUBMITTED BY				Complete *(if applicable)*	
Name (Print/Type)	J. Matthew Zigmant	*Registration No (Attorney/Agent)*	44,005	*Telephone*	650-326-2400
Signature				*Date*	February 23, 2004

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

60142388 v1

PTO/SB/35 (02-01)

NONPUBLICATION REQUEST CERTIFICATION UNDER 35 U.S.C. 122(b)(2)(B)(i)		
	First Named Inventor	Yannis Tsividis
	Title	POWER DISSIPATION REDUCTION IN WIRELESS TRANSCEIVERS
	Atty Docket Number	021673-000210US

I hereby certify that the invention disclosed in the attached application **has not and will not be** the subject of an application filed in another country, or under a multilateral agreement, that requires publication at eighteen months after filing.

I hereby request that the attached application not be published under 35 U.S.C. 122(b).

February 23, 2004
Date


Signature

Reg. No. 44,005

J. Matthew Zigmant
Typed or printed name

This request must be signed in compliance with 37 CFR 1.33(b) and submitted with the application **upon filing.**

Applicant may rescind this nonpublication request at any time. If applicant rescinds a request that an application not be published under 35 U.S.C. 122(b), the application will be scheduled for publication at eighteen months from the earliest claimed filing date for which a benefit is claimed.

If applicant subsequently files an application directed to the invention disclosed in the attached application in another country, or under a multilateral international agreement, that requires publication of applications eighteen months after filing, the applicant **must** notify the United States Patent and Trademark Office of such filing within forty-five (45) days after the date of the filing of such foreign or international application. **Failure to do so will result in abandonment of this application (35 U.S.C. 122(b)(2)(B)(iii)).**

60142391 v1

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
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APPLICATION NUMBER	FILING OR 371 (c) DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
10/784,613	02/23/2004	Yannis Tsividis	021673-000210US

CONFIRMATION NO. 8357

20350
TOWNSEND AND TOWNSEND AND CREW, LLP
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EIGHTH FLOOR
SAN FRANCISCO, CA 94111-3834

FORMALITIES LETTER

OC000000012717551

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NOTICE TO FILE CORRECTED APPLICATION PAPERS

Filing Date Granted

An application number and filing date have been accorded to this application. The application is informal since it does not comply with the regulations for the reason(s) indicated below. Applicant is given TWO MONTHS from the date of this Notice within which to correct the informalities indicated below. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

The required item(s) identified below must be timely submitted to avoid abandonment:

- Replacement drawings in compliance with 37 CFR 1.84 and 37 CFR 1.121 are required. The drawings submitted are not acceptable because:
  - The drawings must be made on paper that has a white background (see 37 CFR 1.84 (e)). For example, drawings on graph paper, lined paper, or paper that has a non-white background are not acceptable. See Figure(s) 2A,3,8B,8D,11D.

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PTO/SB/21 (02-04)

TRANSMITTAL FORM

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Application Number	10/784,613
Filing Date	February 23, 2004
First Named Inventor	Tsividis, Yannis
Art Unit	2681
Examiner Name	
Attorney Docket Number	021673-000210US

Total Number of Pages in This Submission: 5 w/7 refs

ENCLOSURES *(Check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment/Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☒ **Supplemental IDS w/PTO/SB/08B** (3pgs)
- ☐ Certified Copy of Priority Document(s)
- ☐ Response to Missing Parts/ Incomplete Application
  - ☐ Response to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
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- ☐ Status Letter
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Firm or Individual name	Townsend and Townsend and Crew LLP J. Matthew Zigmant Reg. No. 44,005
Signature	J. Matthew Zig
Date	July 2, 2004

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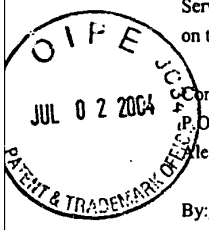
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By: _____
Daniel Miranda

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Yannis Tsividis

Application No.: 10/784,613

Filed: February 23, 2004

For: POWER DISSIPATION REDUCTION IN WIRELESS TRANSCEIVERS

Customer No.: 20350

Confirmation No.: 8357

Examiner:

Art Unit: 2681

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR §1.97 and §1.98

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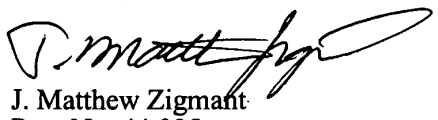
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Respectfully submitted,



J. Matthew Zigmant
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Substitute for form 1449B/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	10/784,613
Filing Date	February 23, 2004
First Named Inventor	Tsividis, Yannis
Art Unit	
Examiner Name	
Attorney Docket Number	021673-000210US

U.S. PATENT DOCUMENTS+

Examiner Initials*	Cite No.[1]	Document Number Number Kind Code[2] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	AA	US-2002/0036519	03-28-2002	Krishnapura et al.	
	AB	US-2003/0112059	06-19-2003	Krishnapura et al.	
	AC	US-2004/0042572	03-04-2004	Palaskas et al.	
	AD	US-2004/0091035	05-13-2004	Palaskas et al.	
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns; Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
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	AG					☐

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	AH	ARYA R. BEHZAD et al., "A 5-GHz Direct-Conversion CMOS Transceiver Utilizing Automatic Frequency Control for the IEEE 802.11a Wireless LAN Standard", IEEE Journal of Solid-State Circuits, Vol. 38, No. 12, December 2003	
	AI	VINCENT LEUNG et al., "Digital-IF WCDMA Handset Transmitter IC in 0.25um SiGe BiCMOS", 2004 IEEE International Solid-State Circuits Conference	
	AJ	MASOUD ZARGARI et al., "A Single-Chip Dual-Band Tri-Mode CMOS Transceiver for IEEE 802.11a/b/g WLAN", 2004 IEEE International Solid-State Circuits Conference	
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Application Number	10/784,613
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Attorney Docket Number	021673-000210US

Total Number of Pages in This Submission: 6 w/29 refs

ENCLOSURES *(Check all that apply)*

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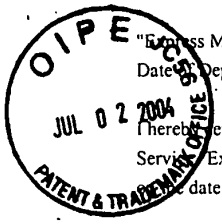
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PATENT
Attorney Docket No.: 021673-000210US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Yannis Tsividis Application No.: 10/784,613 Filed: February 23, 2004 For: POWER DISSIPATION REDUCTION IN WIRELESS TRANSCEIVERS Customer No. 20350	Confirmation No. 8357 Examiner: Art Unit: 2681 INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR §1.97 and §1.98

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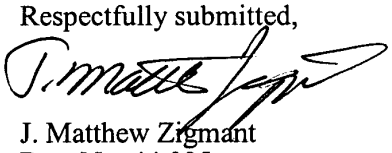
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Respectfully submitted,



J. Matthew Zigmant
Reg. No. 44,005

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Sheet 1 of 2

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Application Number	
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First Named Inventor	Tsividis, Yannis
Art Unit	
Examiner Name	
Attorney Docket Number	021673-000210US

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	AA	US-4,270,222	05-26-1981	Menant	
	AB	US-5,001,776	03-19-1991	Clark	
	AC	US-5,390,357	02-14-1995	Nobusawa	
	AD	US-5,392,457	02-21-1995	Davis et al.	
	AE	US-5,406,613	04-11-1995	Peponides et al.	
	AF	US-5,564,094	10-08-1996	Anderson et al.	
	AG	US-5,600,271	02-04-1997	Erickson et al.	
	AH	US-6,026,288	02-15-2000	Bronner	
	AI	US-6,389,445	05-14-2002	Tsividis	
	AJ	US-6,400,177	06-04-2002	Yoshizaki	
	AK	US-6,529,069	03-04-2003	Krishnapura et al.	
	AL	US-20030112060	06-19-2003	Krishnapura et al.	
	AM	US-20030117212	06-26-2003	Krishnapura et al.	
	AN	US-6,683,492	01-27-2004	Krishnapura et al.	
	AO	US-			

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	AP	PCT	WO 02/35756		05-02-2002	Yoshizawa et al.		☐
	AQ	PCT	WO 02/056558		07-18-2002	Palaskas et al.		☐
	AR	PCT	WO 02/056470		07-18-2002	Palaskas et al.		☐
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	AT	P.R. GRAY et al., "Future Directions in Silicon ICs for RF Personal Communications", IEEE 1995 Custom Integrated Circuits Conference	
	AU	Y. TSIVIDIS, "Minimising power dissipation in analogue signal processors through syllabic companding", Electronic Letters, Vol. 35, No. 21, October 14, 1999	
	AV	AARNO PARSSINEN et al., "A 2-GHz Wide-Band Direct Conversion Receiver for WCDMA Applications", IEEE Journal of Solid-State Circuits, Vol. 34, No. 12, December 1999	
	AW	FARBOD BEHBAHANI et al., "A Broad-Band Tunable CMOS Channel-Select Filter for a Low-IF Wireless Receiver", IEEE Journal of Solid-State Circuits, Vol. 35, No. 4, April 2000	
	AX	TUOMAS HOLLMAN et al., "A 2.7-V CMOS Dual-Mode Baseband Filter for PDC and WCDMA", IEEE Journal of Solid-State Circuits, Vol. 36, No. 7, July 2001	
	AY	FARBOD BEHBAHANI et al., "Adaptive Analog IF Signal Processor for a Wide-Band CMOS Wireless Receiver", IEEE Journal of Solid-State Circuits, Vol. 36, No. 8, August 2001	
	AZ	ATUSHI YOSHIZAWA et al., "An Anti-Blocker Structure MOSFET-C Filter for a Direct Conversion Receiver", IEEE 2001 Custom Integrated Circuits Conference	
	BA	JUSSI RYYNANEN et al., "RF Gain Control in Direct Conversion Receivers", 2002 IEEE	
	BB	ALEKSANDAR TASIC et al., "Concept of Frequency-Transconductance Tuning of Bipolar Voltage-Controlled Oscillators", 2002 IEEE	
	BC	ALEKSANDER TASIC et al., "Concept of Phase-Noise Tuning of Bipolar Voltage-Controlled Oscillators", 2002 IEEE	
	BD	Y. TSIVIDIS et al., "Internally Varying Analog Circuits Minimize Power Dissipation", IEEE Circuits & Devices Magazine, January 2003	
	BE	CHRIS VAN DEN BOS et al., "Architecture of a Reconfigurable Radio Receiver Front-End Using Overall Feedback", Electronic Research Laboratory, Delft University of Technology	

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PCT

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(25) Filing Language: English

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60/243,939 27 October 2000 (27.10.2000) US

(71) Applicant *(for all designated States except US)*: **THE TRUSTEES OF COLUMBIA UNIVERSITY IN THE CITY OF NEW YORK** [US/US]; 116th Street and Broadway, New York, NY 10027 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **YOSHIZAWA, Atushi** [JP/JP]; 1-8-15 Konan Minato-Ku, Tokyo 108-0075 (JP). **TSIVIDS, Yannis** [GR/US]; 410 Riverside Drive, Apt. 52A, New York, NY 10025 (US).

(74) Agent: **TANG, Henry**; Baker & Botts, LLP, 30 Rockefeller Plaza, New York, NY 10112-0228 (US).

(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

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WO 02/35756 A2

(54) Title: ACTIVE CONTINUOUS-TIME FILTER WITH INCREASED DYNAMIC RANGE IN THE PRESENCE OF BLOCKER SIGNALS

(57) Abstract: An active filter is disclosed with improved blocker signal rejection characteristics. Linear resistors, such as fixed value resistors are used at the input stage of the filter to suppress any blocker signal. A gain compensation stage is added to the output stage using resistors fabricated with the same technology used to fabricate the input resistors in order to offset any gain changes associated with the input fixed value resistors. In an exemplary embodiment, the fixed value resistors are fabricated using polysilicon.

IPR2024-00816
Apple EX1002 Page 64
IPR2023-00819
Theta EX2019

ACTIVE CONTINUOUS-TIME FILTER WITH INCREASED DYNAMIC RANGE IN THE PRESENCE OF BLOCKER SIGNALS

SPECIFICATION

RELATED APPLICATION

This application claims priority from provisional U.S. Application No. 60/243,939 filed October 27, 2000, which is incorporated herein by reference.

BACKGROUND OF INVENTION

Radio communication receivers must receive desired signals at predetermined frequencies while filtering out undesired signals at other frequencies. The undesired signals can have a much larger signal strength than the desired signals. These undesired signals are called "blockers" and are problematic because the filter that removes them must operate in its linear region to avoid distortion. Therefore, the maximum amplitude of all signals applied to the filter input must be limited so that the blocker signals do not cause saturation, clipping or subtler forms of distortion such as intermodulation (a typical measure of which is out-of-band third order input intercept point or IIP3) in the filter. Consequently, the strength of the entire range of signals to be processed, including the blocker signal and the desired signal, must be appropriately limited. This means that the desired signal, which can be orders of magnitude smaller than the blocker signals, will be limited to an extremely small amplitude and can fall below the noise floor of the filter.

To keep the signal-to-noise ratio within a reasonable range, the noise of the filter, which is advantageously implemented as an integrator circuit, must be kept extremely low which can result in a large chip area and have large power dissipation. Accordingly, it is difficult to implement these filters on an integrated circuit chip, necessitating the use of other technologies which can have penalties in terms of cost and size.

One technique known in the prior art to construct a radio communication receiver is the active RC technique as described in Mihai Banu &

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Yannis Tsividis, An Elliptic Continuous-Time CMOS Filter with On-Chip Automatic Tuning, SC-20 IEEE Journal of Solid-State Circuits, 1114, 1114-1121 (Dec. 1985). This technique employs fully-balanced integrator stages, each stage consisting of resistors, capacitors and operational amplifiers. Fully-balanced operation, which means that each integrator has two output terminals where the signals at each output terminal are identical in magnitude to one another, but have opposite polarity, improves the filter's common-mode interference rejection performance. Because the frequency response of an active filter designed in this fashion depend on the resistance and capacitance values of the chip components, and because those values may vary due to fabrication tolerances and temperature variations, a technique was described for making the resistors in the active filter tunable to compensate for unwanted variations in the frequency response of the filter. Specifically, the prior art describes all of the resistance element in the active filter being embodied as MOSFETs operating in their triode or nonsaturation region, designed and biased to function as variable resistors whose resistance is tuned by the gate voltage applied to the MOSFETs. This technique suffers from the disadvantage that large blocker signals present at the input of the active filter may force the MOSFETs that are functioning as variable resistors into a non-linear region of operation, thereby causing distortion in the signals present at the output of the active filter, as previously described.

SUMMARY OF THE INVENTION

It is an object of the present invention to process the desired signal and reject blocker signals without excessive power dissipation or chip area. The object is achieved by the introduction of linear resistance elements to the input stage of the active filter. The response of the fixed-value resistors at the input stage remains linear despite the large blocker signals at the input of the filter. The blocker signals are sufficiently attenuated by the input stage so that subsequent MOSFETs are not forced into a non-linear region of operation by the blocker signals. A gain compensation stage is added to the active filter to offset any changes to the gain of the filter caused by the use of both the linear resistance and the variable MOSFET resistance elements.

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In one exemplary embodiment of the present invention, an active filter is provided having a first fully balanced active integrator with linear resistance elements such as fixed value resistors at the input stage, at least one intermediate fully balanced active integrator with variable value resistors at the input stage and a variable gain output stage compensating for the gain variation caused by the mismatch of the fixed value resistors to the variable value resistors.

In another exemplary embodiment, the fixed resistors are polysilicon resistors.

In another exemplary embodiment, the variable resistors are tunable metal oxide silicon field effect transistors (MOSFETs).

In a further exemplary embodiment, the gain of the variable gain output stage corresponds to the ratio of the resistances of the linear resistors and the variable value resistors.

In a still further exemplary embodiment, the active filter includes a phase equalizer circuit connected to the filter output.

In yet another exemplary embodiment, the active filter includes coupling capacitors interconnecting the various integrator stages.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a circuit diagram illustrating an exemplary embodiment of the present invention.

Fig. 2 is a circuit diagram illustrating an implementation of a fully balanced amplifier useful in the embodiment illustrated in Fig. 1.

Fig. 3 is a block diagram of a circuit useful as a gate voltage source for the variable resistors illustrated in Fig. 1.

Fig. 4 is a circuit diagram of a one-quarter frequency divider useful in the circuit of Fig. 3.

Fig. 4A is a circuit diagram of a voltage converter useful in the circuit of Fig. 3.

Fig. 5 is a circuit diagram of a reference filter useful in the circuit of Fig. 3.

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Fig. 6 is a circuit diagram of a voltage multiplier useful in the circuit of Fig. 3.

Fig. 7 is a circuit diagram of a low-pass filter useful in the circuit of Fig. 3.

Fig. 8 is a circuit diagram of a charge pump useful in the circuit of Fig. 3.

Fig. 9 is a circuit diagram of a phase equalizer circuit useful at the output of the circuit illustrated in Fig. 1.

DESCRIPTION OF THE EXEMPLARY EMBODIMENTS

In Fig. 1 an exemplary embodiment of a low-pass filter in accordance with the invention for a direct conversion or zero intermediate frequency receiver is illustrated. The embodiment described has a cut-off frequency of 1.92 MHz, in-band gain of 8.5 dB and out-of-band rejection at 10 MHz of 64 dB.

In operation, fully balanced input signals are applied at input terminals 1 and 2 of the filter. For purposes of this specification and claims, fully balanced means the signals at each input terminal of a circuit are identical in magnitude to one another except have opposite polarity (i.e. the signals are 180° out of phase with respect to one another), and the signals at each output terminal of the circuit are identical to one another except have opposite polarity. The input signals pass through first fully balanced integrator 72 which consists of linear (e.g. fixed value) resistors 3 and 4, fully differential amplifier 8, linear capacitors 7 and 9, variable resistors 37, 38, 39 and 40. Fully differential amplifier 8 has a non-inverting input 5, an inverting input 6, a inverting output 10 and a non-inverting output 11. Fully differential amplifier 8 is described in detail herein with reference to Fig. 2. Linear capacitor 7 and variable resistor 39 are connected in parallel between the non-inverting input 5 and the inverting output 10 of amplifier 8. Similarly, linear capacitor 9 and variable resistor 40 are connected in parallel between the inverting input 6 and the non-inverting output 11 of amplifier 8. Linear resistors 3 and 4 are preferably polysilicon resistors with nominal resistance of 5 kΩ. Variable resistors 37, 38, 39 and 40 are preferably MOSFETs operating in the triode or nonsaturation region each designed and biased at its gate terminal to have a nominal resistance of 5 kΩ. The gate voltage V_G of the

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MOSFET transistors controls the channel resistance of the MOSFET devices, causing them to function as voltage controlled resistors. Gate voltage V_G of variable MOSFET resistors 37, 38, 39 and 40 is discussed in detail herein with respect to Figs. 3-8. Linear capacitors 7 and 9 are preferably composed of polysilicon plates and each have a capacitance of 17.7 pF.

After passing through integrator 72, the blocker signal is partially attenuated in the fully balanced output signals present at output nodes 10 and 11. The output signals of the integrator 72 are then applied to a first intermediate fully balanced active integrator 71, first passing through variable resistors 12 and 13. Variable MOSFET resistors 12 and 13 are implemented identically to variable MOSFET resistors 39 and 40. The signals then pass through balanced amplifier 17 and linear capacitors 16 and 18. Fully balanced amplifier 17 is identical to fully balanced amplifier 8. Linear capacitors 16 and 18, like linear capacitors 7 and 9, are preferably formed with polysilicon plates, each having a capacitance of 23.7 pF.

The first intermediate integrator stage 71 provides fully balanced output signals at terminals 19 and 20 with the blocker signal further attenuated. The signals then enter a second intermediate integrator 21, identical to the first intermediate integrator 71 but with linear feedback capacitors 65 and 66 each having a capacitance of 35.3 pF. The signals at terminals 19 and 20 are applied to the second intermediate integrator 21 at variable MOSFET input resistors 77 and 78, respectively, which are connected to the inverted input 82 and the non-inverted input 81 of fully balanced amplifier 89 of the second intermediate integrator 21, respectively. The second intermediate integrator 21 provides fully balanced output signals at terminals 51 and 52 with the blocker signal further attenuated. The signals at terminals 51 and 52 are the applied to a third intermediate integrator stage 22, identical to second intermediate integrator stage 21. The signals at terminals 51 and 52 are received by the third intermediate integrator 22 through variable MOSFET input resistors 85 and 86, respectively, which are connected to the inverted input 87 and the non-inverted input 88 of fully balanced amplifier 90 of the integrator 22, respectively. The third intermediate integrator 22 provides fully balanced output signals at terminals 53 and 54 with the blocker signal further attenuated.

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The signals at terminals 53 and 54 are applied to a final integrator 23 through variable MOSFET resistors 56 and 55, respectively, which are connected to the inverted input 60 and the non-inverted input 59 of the fully balanced amplifier 91 of the integrator 23, respectively. The final integrator 23 is identical to the initial integrator 72, but with variable MOSFET resistors 55 and 56 at the input stage rather than fixed value resistors 3 and 4 and with feedback linear capacitors 70 and 71 each having a capacitance of 17.7 pF. The signals provided by the final integrator stage are fully balanced signals present at terminals 26 and 27. At this stage, the blocker signal will be nearly completely eliminated from the output signal. However, because linear resistors 3 and 4 have a different physical structure than that of the MOSFETs, there is no correlation between the values of the fixed resistors and the values of the variable resistors (i.e. the MOSFETs) over fabrication tolerances and temperature variations, which can cause undesired variations of filter gain. Consequently, a variable gain output stage 57 is utilized to compensate for the undesired gain variation.

The signals at terminals 26 and 27 enter variable gain output stage 57 through variable MOSFET resistors 28 and 29, each having a nominal resistance of 5 kΩ. The signals then pass through amplifier 33 having linear feedback resistors 32 and 34. Linear resistors 32 and 34 are selected to offset the effect variation caused by linear resistors 3 and 4. In the exemplary embodiment illustrated in Fig. 1, it can be shown that the gain of the active filter 100 is proportional to the resistance of the linear output resistors 32 and 34 and inversely proportional to twice the resistance of the linear input resistors 3 and 4. Accordingly, resistors 32 and 34 are preferably polysilicon resistors with nominal resistance of 10 kΩ which ensures the nominal gain of the filter is 0 dB. The non-inverting and inverting outputs of amplifier 33 are connected to the non-inverting and inverting outputs 36 and 35 of the active filter 100.

As can be seen in Fig. 1, the exemplary embodiment utilizes four coupling capacitors 43A, 43B, 43C, 43D connected between terminals 6 and 44, 5 and 45, 11 and 46, and 10 and 47, respectively, and four coupling capacitors 58A, 58B, 58C, 58D connected between terminals 44 and 60, 45 and 59, 46 and 27, and 47 and 26 respectively. Adjusting the capacitance of these coupling capacitors

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correspondingly adjusts placement of the transmission zeros on the frequency response plot of the filter. In an exemplary embodiment, the two groups of coupling capacitors 43A, 43B, 43C and 43D, and 58A, 58B, 58C and 58D each consist of polysilicon plate capacitors, where the capacitors of the first group 43A, 43B, 43C and 43D each have a capacitance of 2.46 pF and the capacitors of the second group 58A, 58B, 58C and 58D each have a capacitance of 0.904 pF.

Additionally, as can be seen from Fig. 1, the integrators 72, 71, 21 and 22 each have a second set of signal inputs for accepting the feedback signal from the output of the subsequent integrator. Specifically, variable MOSFET resistors 37 and 38 connect the inverted and non-inverted output of the second integrator 71 at terminals 19 and 20, respectively, to the non-inverting and inverting inputs of the first fully balanced amplifier 8 at terminals 5 and 6, respectively. Consequently, the signals present at the inverted and non-inverted output terminals 10, 11 of the fully balanced amplifier 8 of the integrator 72 represent the integral of the sum of the two input signals (i.e. the balanced primary input signals present at terminals 1, 2 and the balanced feedback input signal present at terminals 19, 20). In a similar fashion, variable MOSFET resistors 41 and 42 connect the inverted and non-inverted outputs of the amplifier 89 of the third integrator 21 at terminals 51 and 52, respectively, to the non-inverting and inverting inputs of the amplifier 17 of the second integrator 71 at terminals 14 and 15, respectively. Further, the inverted and non-inverted outputs of amplifier 90 of integrator 22 at terminals 53 and 54, respectively, are fed back through variable MOSFET resistors 79 and 80, respectively, into the non-inverted and inverted inputs 81 and 82 of fully balanced amplifier 89 of integrator 21, respectively, and the inverted and non-inverted outputs of fully balanced amplifier 91 of integrator 23 at terminals 26 and 27, respectively are fed back through variable MOSFET resistors 83 and 84, respectively, into the non-inverted and inverted inputs 88 and 89 of the fully balanced amplifier 90 of integrator 22, respectively. All MOSFET variable resistors 12, 13, 24, 25, 28, 29, 37, 38, 39, 40, 41, 42, 55, 56, 77, 78, 79, 80, 83, 84, 85 and 86, in circuit 100 are preferably identical. In the exemplary embodiment shown in Fig. 1, all variable resistors are n-channel MOSFETS.

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Referring now to Fig. 2, an exemplary embodiment of the fully balanced amplifier 8 used in the filter 100 illustrated in Fig. 1 is shown. Other amplifiers 17, 89, 90, 91 and 93 illustrated in Fig. 1 have identical structures. The operation of fully balanced amplifier 8 will be apparent to one of ordinary skill in the art.

Input signals are is applied to the non-inverting and inverting inputs of the fully balanced amplifier 8 at terminals 101 and 103, respectively, which voltages are in turn applied to the base terminals of npn bipolar junction transistors (BJT) 113 and 115. The emitter terminals of transistors 113 and 115 are tied together at node 117 and connected to the drain of an n-channel MOSFET current source 109 having its source terminal connected to ground 105. The collector terminals of transistors 113 and 115 are tied to the drain terminals of p-channel MOSFETs 127 and 129 respectively at nodes 131 and 133. The gate terminals of transistors 127 and 129 are connected together at node 135.

Node 131 is connected to the base terminal of npn BJT 123. The emitter terminal 112 of transistor 123 is tied to the drain terminal of a MOSFET current source 107, which in turn has its source terminal connected to ground node 105. Terminal 112 also serves as a first (non-inverted) fully balanced output terminal. Similarly, node 133 is connected to the base terminal of npn BJT 125. The emitter terminal 114 of transistor 125 is tied to the drain terminal of an n-channel MOSFET current source 111, having its source terminal connected to ground node 105. Terminal 114 also serves as a second (inverted) fully balanced output terminal of the amplifier 8.

The source terminals of transistors 127 and 129 are tied together at supply voltage node 137. The collector terminals of transistors 123 and 125 are also connected to supply voltage node 137.

Amplifier 8 employs a common mode feedback servo circuit 160. Two npn BJTs 145 and 149 have their emitter terminals tied together at node 151 which is connected to the drain terminal of an n-channel MOSFET current source 110, which has its source terminal connected to ground node 105. The base terminal 153 of transistor 145 is connected to the juncture of resistors 141 and 143, each with a

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nominal resistance of 40 kΩ. Resistor 141 is connected between base terminal 153 of transistor 145 and inverted output terminal 114 of amplifier 8, while resistor 143 is connected between base terminal 153 of transistor 145 and non-inverted output terminal 112 of amplifier 8. The collector terminal of transistor 145 is connected to supply voltage node 137.

The base terminal 155 of transistor 149 is connected to an external voltage source, not shown. The collector terminal of transistor 149 is connected to the drain terminal of p-channel MOSFET 147. The drain terminal of transistor 147 is also tied to gate terminal 135 which, as previously noted, is tied to the commonly connected gate terminals of transistor pair 127 and 129. The source terminal of transistor 147 is connected to voltage supply node 137. Voltage source 139 is connected between ground node 105 and voltage supply node 137.

During operation, the amplifier 8, amplifies the fully balanced input signals present at terminals 101 and 103, and provides fully balanced amplified signals at terminals 112 and 114 respectively. The non-inverted and inverted output signals at terminals 112 and 114 are preferably identical in magnitude but have opposite polarity (i.e. the output signals are 180° out of phase with respect to one another). The average of the signals present at terminals 112 and 114 at any time is set by the voltage present at terminal 155, which in an exemplary embodiment is 1.5V.

To ensure that the MOSFETs of the filter 100 of Fig. 1 are operating deep within their triode regions of operation and are thus acting as linear gate voltage controlled variable resistors in the circuit of Fig. 1, it is necessary for the gate voltage V_G applied to the MOSFETs acting as variable resistors to be approximately 4V when the nominal channel resistance of the variable MOSFET resistors is 5 kΩ, the channel width is 18μm, the channel length is 10 μm and source and drain voltages are 1.5V using a common 0.8 μm BiCMOS technology. Because the supply source available in most low-power wireless applications is a low voltage battery cell, such as a lithium-ion cell that provides a supply voltage of 2.7V, a circuit is needed to boost the control voltage which drives the gates of MOSFETs in the filter. Additionally, the circuit supplying V_G will also control the frequency response of the overall active filter by

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adjusting the resistance of the MOSFET variable resistors, consequently a tuning circuit is needed to control V_G and thereby the cutoff frequency. Fig. 3 shows a tuning circuit suitable for controlling the gate voltage of the variable MOSFET resistors shown in Fig. 1.

Referring to Fig. 3, an external reference clock 180 supplies a signal to a ¼ frequency divider 181, which buffers the rest of the tuning circuit from the clock, thus making the tuning circuit insensitive to the reference clock voltage level. The ¼ frequency divider 181 is discussed in detail herein with reference to Fig. 4. The output of the ¼ frequency divider 187 is supplied to a reference filter 182, a voltage multiplier 183 and a voltage level conversion circuit 189, the output of which is fed into charge pump circuit 186. In an exemplary embodiment, the reference filter 182 selected is a second order MOSFET-C Butterworth low-pass filter with a cut off frequency of 3.84 MHz, which ensures that the frequency comparison is performed outside the passband of the active filter the circuit is intended to tune. The reference filter 182 is described in detail herein with reference to Fig. 5.

The output of the reference filter 182 is also supplied to voltage multiplier 183. The output of voltage multiplier 183 is passed through a loop filter 184, which removes high frequency signals generated by the voltage multiplication and allows a DC voltage to pass to charge pump 186. The voltage multiplier and low-pass filter are discussed in detail herein with reference to Fig. 6 and Fig. 7, respectively. Charge pump 186, described in detail below with reference to Fig. 8, boosts the voltage present at its input 185 to generate a sufficient V_G at terminal 188 to tune the MOSFETs acting as variable resistors in the active filter 100 shown in Fig. 1. The output of the charge pump 188 is fed back to the reference filter 182, ensuring the V_G output 188 will vary with temperature changes so as to maintain the desired frequency response of the main active filter 100 shown in Fig. 1.

Referring to Fig. 4, an exemplary embodiment of the ¼ frequency divider 181 of Fig. 3 is illustrated. The output of reference clock 180 of Fig. 3 is applied to non-inverting and inverting input terminals 404 and 406, respectively, of the ¼ frequency divider. In the exemplary embodiment, reference clock 180 of Fig. 3 is set to output a clock signal with frequency 15.36 MHz at 100 mV_{pp}. The input

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clock signal enters a first flip-flop based digital divider 400. The operation of digital divider 400 is well known to one of ordinary skill in the art. The input clock signals at terminals 404 and 406 are divided in frequency by digital divider stage 400, and the non-inverted and inverted outputs of the divider stage 400 are provided at terminals 410 and 412, respectively. The frequency of the output signals at terminals 410 and 412 are one half the frequency of the input clock signals at terminals 404 and 406. The balanced signals at terminals 410 and 412 then enter a second digital divider stage 402, identical to first digital divider stage 400. The second digital divider stage 402 provides non-inverted and inverted output signals at terminals 414 and 416, respectively, where the output signal frequency is ¼ of the frequency of the input clock signals present at terminals 404 and 406. In the exemplary embodiment, Vcc is 2.7 V and the output signal amplitude will typically be 400mVpp.

In Fig. 4A, an exemplary embodiment of a level conversion circuit is shown. The signals present at the non-inverted and inverted outputs 414 and 416 of the ¼ frequency divider of Fig. 4., respectively, enter the level conversion circuit at input terminals 418 and 420. The signals at input terminals 418 and 420 are applied to the gate terminals of two p-channel MOSFET transistors 436 and 434, respectively. The drain terminals of transistors 436 and 434 are connected to the drain terminals of two n-channel MOSFET transistors 438 and 440, respectively, each having its substrate and source terminals connected to ground node 424. Additionally, the gate terminals of the transistors 438 and 440 are both connected to the drain terminal of transistor 438. The substrate terminals of input transistors 434 and 436 are each connected to supply voltage node V_{dd} 428, while the source terminals of both input transistors 434 and 436 are tied to the drain terminal of p-channel MOSFET 430. The source and substrate terminals of transistor 430 are, in turn, connected to V_{dd} supply voltage node 428, while the gate terminal of transistor 430 is connected to received a bias voltage V_{bias} at terminal 426. The respective drain terminals of transistors 440 and 436 both are tied to the gate terminal of n-channel MOSFET 442, which has its source and substrate terminals tied to ground node 424. The drain terminal of transistor 442 is tied to the drain terminal of p-channel MOSFET 432, which, in turn, has its substrate and source terminals tied to V_{dd} supply voltage node 428 and its gate

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terminal tied to V_{bias} terminal 426. The voltage at the V_{bias} terminal 426 may be generated by a voltage divider circuit between V_{dd} supply voltage node 428 and ground node 424. The voltage at V_{bias} terminal 426 is selected to ensure that approximately 10μA of current flows through MOSFET 430. The junction of the drain terminals of transistors 442 and 432 serves as an output terminal 422 of the voltage level converter. This signal present at this output terminal serves as the clock for the charge pump described herein with reference to Fig. 8.

In Fig. 5 an exemplary embodiment of the second order MOSFET-C Butterworth low-pass reference filter 182 shown in Fig. 3 is illustrated. The respective output signals from the ¼ frequency divider 181 shown in Fig. 3 and Fig. 4 are present at the non-inverting and inverting input terminals 500 and 501 of reference filter 182. The input signal at the non-inverting input terminal 500 passes through a variable n-channel MOSFET resistor 502 and is applied at node 508, while the input signal at the inverting input terminal 501 passes through a variable n-channel MOSFET resistor 504 and is applied at node 506. The respective resistances of the MOSFET resistors 502 and 504 are both controlled by voltage V_G applied to their respective gates as previously described. The signal then enters fully differential amplifier 514, feedback capacitors 512 and 516 and variable n-channel MOSFET feedback resistors 510 and 518. Capacitors 512 and 516 are preferably fabricated in the same manner as the linear capacitors in the active filer 100 shown in Fig. 1, and each has a capacitance of 5.62 pF. Differential amplifier 514 is identical to the amplifiers used in the active filter 100 illustrated in Fig. 1.

The signal present at nodes 506 and 508 are also connected to variable n-channel MOSFET feedback resistors 522 and 524, respectively. MOSFET feedback resistor 522 is connected between node 506 and inverted output terminal 538 of reference filter 182, while MOSFET feedback resistor 524 is connected between node 508 and non-inverted output terminal 539 of reference filter 182.

After passing through the first integrator stage, the signal present at node 520 passes through variable n-channel MOSFET resistor 528 to node 530, while the signal present at node 521 passes through variable n-channel MOSFET resistor 526 to node 531. The balanced signal then enters differential amplifier 535 and linear

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feedback capacitors 533 and 534. Capacitors 533 and 534 are also preferably fabricated in the same manner as the linear capacitors in the active filter 100 shown in Fig. 1, and each has a capacitance of 11.25 pF. The fully differential amplifier 535 provides its inverted and non-inverted outputs at nodes 536 and 537, respectively. Nodes 536 and 537 are tied to output terminals 538 and 539 of the reference filter 182, respectively.

In Fig. 6, an exemplary embodiment of the voltage multiplier 183 for use in the circuit of Fig. 3 is illustrated. The operation of the voltage multiplier is well known to one of ordinary skill in the art. The non-inverted and inverted signal outputs from the MOSFET-C reference filter 182 shown in Fig. 3 and Fig. 5 enters the voltage multiplier at terminals 552 and 553, respectively. The non-inverted and inverted output signals from the ¼ frequency divider 181 shown in Fig. 3 and Fig. 4 enters the voltage multiplier at terminals 550 and 551, respectively. The respective products of the two non-inverted and the two inverted input voltage signals are provided at output terminals 554 and 555, respectively.

In Fig. 7, an exemplary embodiment of the loop filter 184 for use in the circuit of Fig. 3 is illustrated. The loop filter is a common one pole low-pass filter, well known to one of ordinary skill in the art. The non-inverted and inverted output signals from the voltage multiplier 183 shown in Fig. 3 and Fig. 6 are present at input terminals 600 and 601, respectively. The low-pass filter shown in Fig. 7 filters the input signals to remove unwanted high frequency components generated by the voltage multiplier and to leave a DC voltage V_G required for tuning the MOSFET variable resistors shown in Fig. 1. The filtered signal appears at a single ended output terminal V_{in} 185 as shown in Figs. 3 and 8.

Referring to Fig. 8, an exemplary embodiment of a charge pump circuit useful in the tuning system of Fig. 3 is shown. The charge pump is based on the Dickson multiplier well known to one of ordinary skill in the art. See J.F. Dickson, On-Chip High Voltage Generation in NMOS Integrated Circuits Using an Improved Voltage Multiplier Technique, IEEE Journal of Solid-State Circuits, June 1976, at 374, which is incorporated herein by reference. The voltage signal at terminal 185 from the output of the low-pass filter 184 shown in Fig. 3 and Fig. 7 is

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applied to the non-inverting input terminal of a conventional opamp 207. The inverting input terminal of opamp 207 is tied to its output terminal 205, which is in turn connected to the emitter terminal of diode-connected npn BJT 211 and to the input terminal of an inverter 255 whose output is connected to the gate terminal 256 of p-channel MOSFET 257. The base and collector terminals of transistor 211 are connected to the drain terminal of p-channel MOSFET 257. The gate terminal 256 of MOSFET 257 is biased with the inverse of the DC feed-back voltage of opamp 207 via inverter 255, which turns on MOSFET 257 to provide a current for the diode connected transistor 211, the drain and substrate terminals of MOSFET 257 being connected to V_{CC} supply voltage node 258, which is nominally at 2.7 V. The currents leaving the emitter terminal of transistor 211 and output terminal 205 of opamp 207 pass through a resistor 203 to the ground node 201. This arrangement produces approximately 20 μA of current through the drain terminal of MOSFET 257 when node 205 is nominally set to 0.5V and resistor 203 is 25 kΩ.

The voltage at node 213 is applied to the collector and base terminals of diode-connected npn BJT 233. The emitter of transistor 233 is connected to first charge pump stage consisting of a diode connected BJT 235 and a capacitor 243. Node 213 is also connected to source terminals of p-channel MOSFETs 223 and 231 of inverters formed by n-channel and p-channel MOSFETs pairs 221, 223 and 227, 231, respectively. The gate terminals 422 of MOSFETs 221 and 223 are connected to the output of voltage level converter 189 shown in Fig. 3 and Fig. 4A. The amplitude of the signal entering terminal 422 from the voltage converter 189 is CMOS level, and the frequency of the signal is 3.84 MHz. The drain terminal of p-channel MOSFET 223 is connected to the drain terminal of n-channel MOSFET 221 at node 225. Node 225 is tied to the gate terminals of n-channel and p-channel MOSFET transistors 227 and 231, respectively. The drain terminal of p-channel MOSFET 231 is connected to the drain terminal of n-channel MOSFET 227 at node 229. The source terminals of n-channel MOSFETs 221 and 227 are each tied to the ground node 201.

MOSFETs 221, 223 and 227 and 231 function as two inverter circuits connected in series which work as an amplitude regulator to control the amplitude of the input signal applied to node 422 so that the resulting charge-pump output voltage

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can be defined by the formula: $V_G=(n+1)V_{in}$, where V_G is the gate voltage applied to the gate terminals of the variable MOSFET resistors shown in Fig. 1, n is the number of charge pump stages plus one and V_{in} is the signal present at input terminal 185.

Node 225 is connected to the capacitors of the odd numbered charge pump stages. Thus, in the exemplary embodiment where n equals seven and there are six charge pump stages, node 225 is connected to capacitors C_1 243, C_3 (not shown), and C_5 245. In contrast, node 229 is connected to the capacitors of the even numbered charge pump stages. Thus, in the exemplary embodiment described, terminal 229 is connected to capacitors C_2 244, C_4 (not shown), and C_6 247. Each charge pump stage capacitor 243, 244, 245 and 247 has a capacitance of 0.5 pF.

The charge pump capacitors in turn are also connected to the collector and base terminals of the diode connected BJTs 235, 237, 239, and 241. Thus, C_1 243, is connected to node 261, C_2 is connected to node 259, C_3 and C_4 and their associated diode connected BJTs are not shown, C_5 245 is connected to node 257 and C_6 is connected to node 255. The diode connected BJTs are connected in series, with emitter terminal of BJT 235 connected to collector and base terminals 259 of BJT 237 and so on with the emitter terminal of final stage BJT 241 connected to terminal 253 which provides the desired V_G output voltage. Output voltage terminal 253 is also connected to capacitor C_7 249, having a capacitance of 10 pF, and the drain terminal of an n-channel MOSFET active load 251, which provides a discharge path for the pull-down operation of the charge-pump. The source terminal of the MOSFET load 251 is connected to the ground node 201. The gate terminal of transistor 251 is connected to the gate and drain terminals of an n-channel MOSFET 270 at node 271. Node 271, in turn, is connected to terminal 272 for receiving V_{bias} through a resistor 272.. The voltage V_{bias} may be generated by a voltage divider circuit between the V_{cc} voltage supply node 258 and ground node 201. The voltage V_{bias} is selected to ensure that approximately 10μA of current flows through MOSFET transistor 270

In the exemplary embodiment of the charge pump shown in Fig. 8, polysilicon to polysilicon or metal to metal capacitors are employed, which reduces the parasitic capacitance in the circuit. Accordingly, the output voltage V_G is related to the input V_{in} voltage by the formula: $V_G=(n+1)V_{in}$, where n is the number of charge

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pump stages plus one. Consequently, in the exemplary embodiment, where n is seven and V_{in} generated by the low-pass filter 184 shown in Fig. 3 and Fig. 7 is approximately 0.5 V, V_G is 4 V, which is sufficient to guarantee operation in the triode region for the tunable MOSFET resistors in the circuit illustrated in Fig. 1.

In Fig. 9, a phase equalization circuit for use in the active filter of Fig. 1 is illustrated. Such a circuit is well known to one of ordinary skill in the art. The circuit is useful to linearize the group delay characteristic of the fifth order filter of the exemplary embodiment illustrated in Fig. 1. The output signals from output terminals 35 and 36 of the active filter 100 illustrated in Fig. 1 are supplied to the input terminals 303 and 301 of the phase equalization circuit, respectively. The signals then enter through two circuit paths. In the first path, the signals received at input terminals 303, 301 are applied to capacitors 305 and 307, respectively. The signal then enters fully balanced amplifier 318, feedback capacitors 319 and 321 and variable n-channel MOSFET feedback resistors 325 and 323 connected between amplifier input terminals 315 and 317 and amplifier output terminals 329 and 327, respectively. The signals at amplifier output terminals 329 and 327 are fed to the second circuit path, first to variable n-channel MOSFET resistors 331 and 337, then to a second fully balanced amplifier 348, feedback capacitors 347 and 349 connected between amplifier input terminals 345 and 343 and amplifier output terminals 351 and 353, respectively.

In the second circuit path, the input signal present at input terminal 301 is coupled through variable MOSFET resistor 335 and capacitor 339 to inputs 345 and 343, respectively of fully balanced amplifier 348. The input signal present at terminal 303 is coupled through variable MOSFET resistor 333 and capacitor 341 to inputs 345 and 343, respectively of fully balanced amplifier 348. The balanced output signals from amplifier 348 present at nodes 351 and 353 are fed through variable MOSFET resistors 313, 311, to the input terminals 315, 317, respectively, of fully balanced amplifier 318.

In the exemplary embodiment illustrated, the fully balanced amplifiers 318, 348, capacitors 305, 307, 319, 321, 339, 341, 347 and 349, and variable MOSFET resistors 311, 313, 323, 325, 331, 333, 335 and 337 are respectively

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identical in construction to those in the fully balanced amplifiers, linear capacitors and variable MOSFET resistors of the integrators 72, 71, 21, 22 and 23 of the active filter 100 shown in Fig. 1, except the variable MOSFET resistors are each designed to have a nominal resistance of 10 kΩ at the same gate voltage used in the filter 100 of Fig. 1, and capacitors 339, 341, 347 and 349 each has a capacitance of 21.3 pF while capacitors 205, 307, 319 and 321 each has a capacitance of 8.3 pF. The gate voltage controlling the variable MOSFET resistors in the circuit of Fig. 9 is the same as that controlling the variable MOSFET resistors in the circuit 100 of Fig. 1 and is generated by the circuit shown in Fig. 3.

The foregoing merely illustrates the principles of the invention in an exemplary embodiment. Various modifications and alterations to the described embodiments will be apparent to those skilled in the art in view of the teachings herein. Particularly, the invention can be used in filters with numerous frequency response shapes, not simply the low-pass filter for a direct conversion or zero intermediate frequency receiver illustrated. Moreover, numerous deviations from the circuit topology shown in the attached drawings are possible. By way of example, it is possible to eliminate the coupling capacitors 43A, 43B, 43C and 43D, and 58A, 58B, 58C and 58D in the circuit 100 shown in Fig. 1. It will thus be fully appreciated that those skilled in the art will be able to devise numerous systems and methods which, although not explicitly shown or described, embody the principles of the invention and are thus within the spirit and scope of the invention as defined by the appended claims.

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CLAIMS

1. An active filter having a first filter input terminal, a second filter input terminal, a first filter output terminal and a second filter output terminal, comprising:

a first fully balanced integrator comprising a first fully balanced amplifier having a first non-inverting input, a first inverting input, a first inverting output and a first non-inverting output, a first capacitance element and a first variable value resistance element coupled in parallel between said first non-inverting input and said first inverting output, a second capacitance element and a second variable value resistance element coupled in parallel between said first inverting input and said first non-inverting output, a first linear resistance element coupled between said first filter input terminal and said first non-inverting input, a second linear resistance element coupled between said second filter input terminal and said first inverting input, a third variable resistance element having a first and second end, said first end coupled to said first non-inverting input terminal, and a fourth variable resistance element having a first and second end, said first end coupled to said first inverting input terminal;

a last fully balanced integrator comprising a second fully balanced amplifier having a second non-inverting input, a second inverting input, a second inverting output and a second non-inverting output, a third capacitance element and a fifth variable value resistance element coupled in parallel between said second non-inverting input and said second inverting output, a fourth capacitance element and a sixth variable value resistance element coupled in parallel between said second inverting input and said second non-inverting output, a seventh variable value resistance element having a first end and a second end, said first end coupled to said second non-inverting input, and an eighth variable value resistance element having a first end and a second end, said first end coupled to said second inverting input;

a filter gain compensation stage comprising a third fully balanced amplifier having a third non-inverting input, a third inverting input, a third inverting output coupled to said first filter output terminal and a third non-

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inverting output coupled to said second filter output terminal, a third linear resistance element coupled between said third non-inverting input and said third inverting output, a fourth linear resistance element coupled between said third inverting input and said third non-inverting output, a ninth variable value resistance element coupled between said third non-inverting input and said second non-inverting output, and a tenth variable value resistance element coupled between said third inverting input and said second inverting output;

at least one intermediate fully balanced integrator coupled in succession between said first and last fully balanced integrator, each intermediate fully balanced integrator comprising a fourth fully balanced amplifier having a fourth non-inverting input, a fourth inverting input, a fourth inverting output and a fourth non-inverting output, a fifth capacitance element coupled between said fourth non-inverting input and said fourth inverting output, a sixth capacitance element coupled between said fourth inverting input and said fourth non-inverting output, an eleventh variable value resistance element coupled between said fourth non-inverting input and the non-inverting output of the amplifier of a respective one of the fully balanced integrator coupled to immediately precede said intermediate fully balanced integrator, a twelfth variable value resistance element coupled between said fourth inverting input and the inverting output of the amplifier of a respective one of the fully balanced integrator coupled to immediately precede said intermediate fully balanced integrator, a thirteenth variable value resistance element coupled between said fourth non-inverting input and the inverting output of the amplifier of a respective one of the fully balanced integrator coupled to immediately succeed said intermediate fully balanced integrator, and a fourteenth variable value resistance element coupled between said fourth inverting input and the non-inverting output of the amplifier of a respective one of the fully balanced integrator coupled to immediately succeed said intermediate fully balanced integrator; and

wherein said second end of said third variable resistance element is coupled to the inverting output of the amplifier of a respective one of the at

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least one of the intermediate fully balanced integrator coupled to immediately succeed said first fully balanced integrator, said second end of said fourth variable resistance element is coupled to the non-inverting output of the amplifier of a respective one of the at least one intermediate fully balanced integrator coupled to immediately succeed said first fully balanced integrator, said second end of said seventh variable value resistance element is coupled to the non-inverting output of the amplifier of a respective one of the at least one intermediate fully balanced integrator coupled to immediate precede said last fully balanced amplifier and said second end of said eighth variable value resistance element is coupled to the inverting output of the amplifier of a respective one of the at least one intermediate fully balanced integrator coupled to immediately precede said last fully balanced amplifier.

2. The active filter of claim 1, wherein said first and second linear resistance elements are fixed value polysilicon resistors.

3. The active filter of claim 1, wherein said first and second variable value resistance elements are metal oxide semiconductor field effect transistors each having a source, drain and gate terminal, wherein the resistance between said source and drain terminals may be tuned by a voltage applied to said gate terminal.

4. The active filter of claim 1, wherein the gain of said filter gain compensation stage corresponds to the ratio of the resistance of said first linear resistance element to the resistance of said first variable value resistance element.

5. The active filter of claim 1, wherein the resistance of said third linear resistance element is proportional to twice the resistance of said first linear resistance element..

6. The active filter of claim 1, further comprising a phase equalizer coupled to said first and second filter output terminals.

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7. The active filter of claim 1, wherein said at least one intermediate fully balanced integrator comprises at least a first, second and third intermediate fully balanced integrator, further comprising:

a seventh capacitance element, coupled between said first inverting input and said fourth inverting output of the fourth fully balanced amplifier of said second intermediate fully balanced integrator;

an eighth capacitance element, coupled between said first non-inverting input and said fourth non-inverting output of the fourth fully balanced amplifier of said second intermediate fully balanced integrator;

a ninth capacitance element, coupled between said first non-inverting output and said fourth non-inverting input of the fourth fully balanced amplifier of said second intermediate fully balanced integrator;

a tenth capacitance element, coupled between said first inverting output and said fourth inverting input of the fourth fully balanced amplifier of said second intermediate fully balanced integrator;

an eleventh capacitance element, coupled between said second inverting input and said fourth inverting output of the fourth fully balanced amplifier of said second intermediate fully balanced integrator;

a twelfth capacitance element, coupled between said second non-inverting input and said fourth non-inverting output of the fourth fully balanced amplifier of said second intermediate fully balanced integrator;

a thirteenth capacitance element, coupled between said second non-inverting output and said fourth non-inverting input of the fourth fully balanced amplifier of said second intermediate fully balanced integrator; and

a fourteenth capacitance element, coupled between said second inverting output and said fourth inverting input of the fourth fully balanced amplifier of said second intermediate fully balanced integrator.

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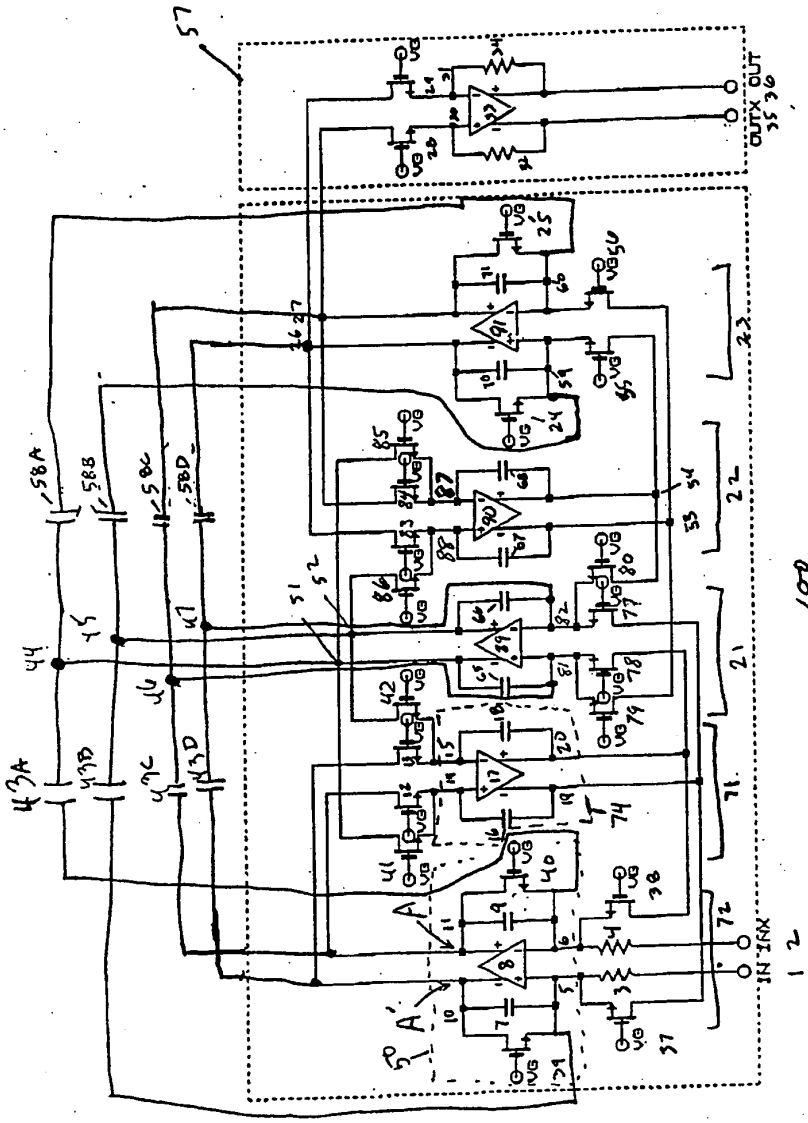


Fig. 1

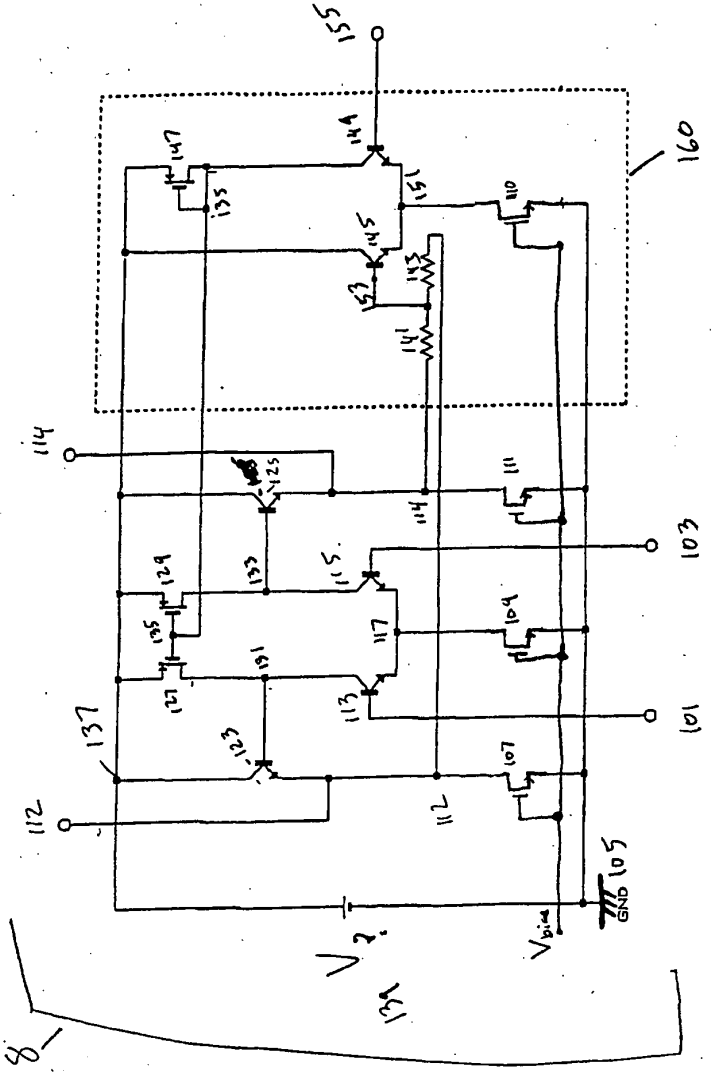

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127
131
113
101
137
123
107
112
105
GND
V_{bias}
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8

Fig. 2

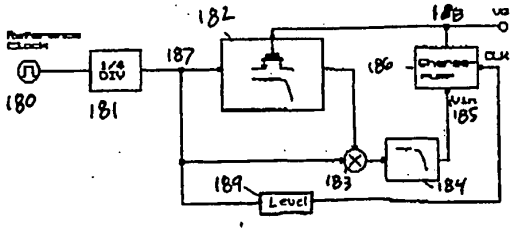

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Level
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Fig. 3

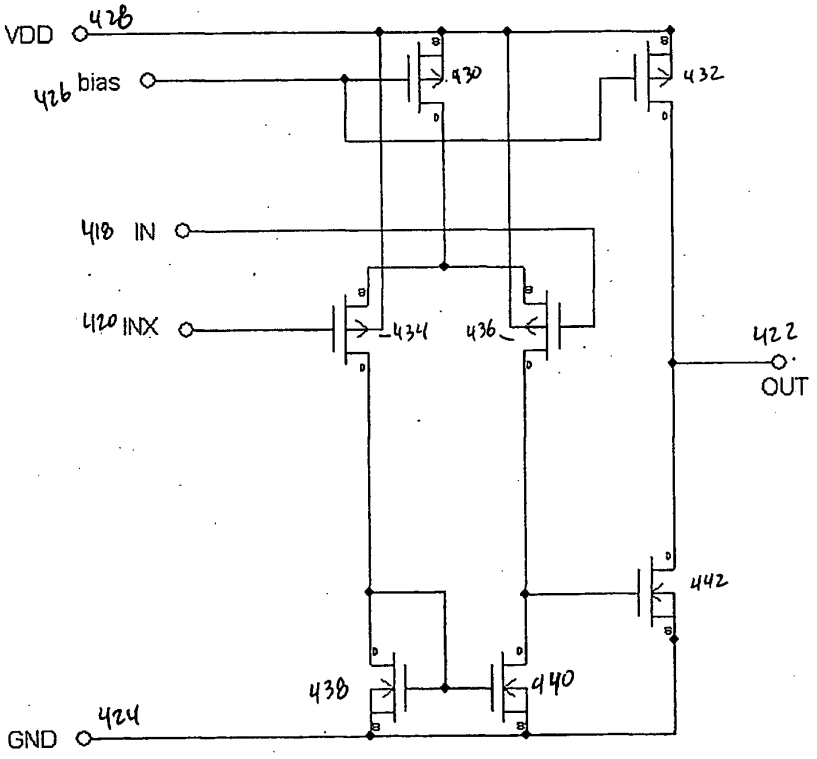

VDD
428
426 bias
430
432
418 IN
420 INX
434
436
422
OUT
442
438
440
424
GND

Fig. 4A

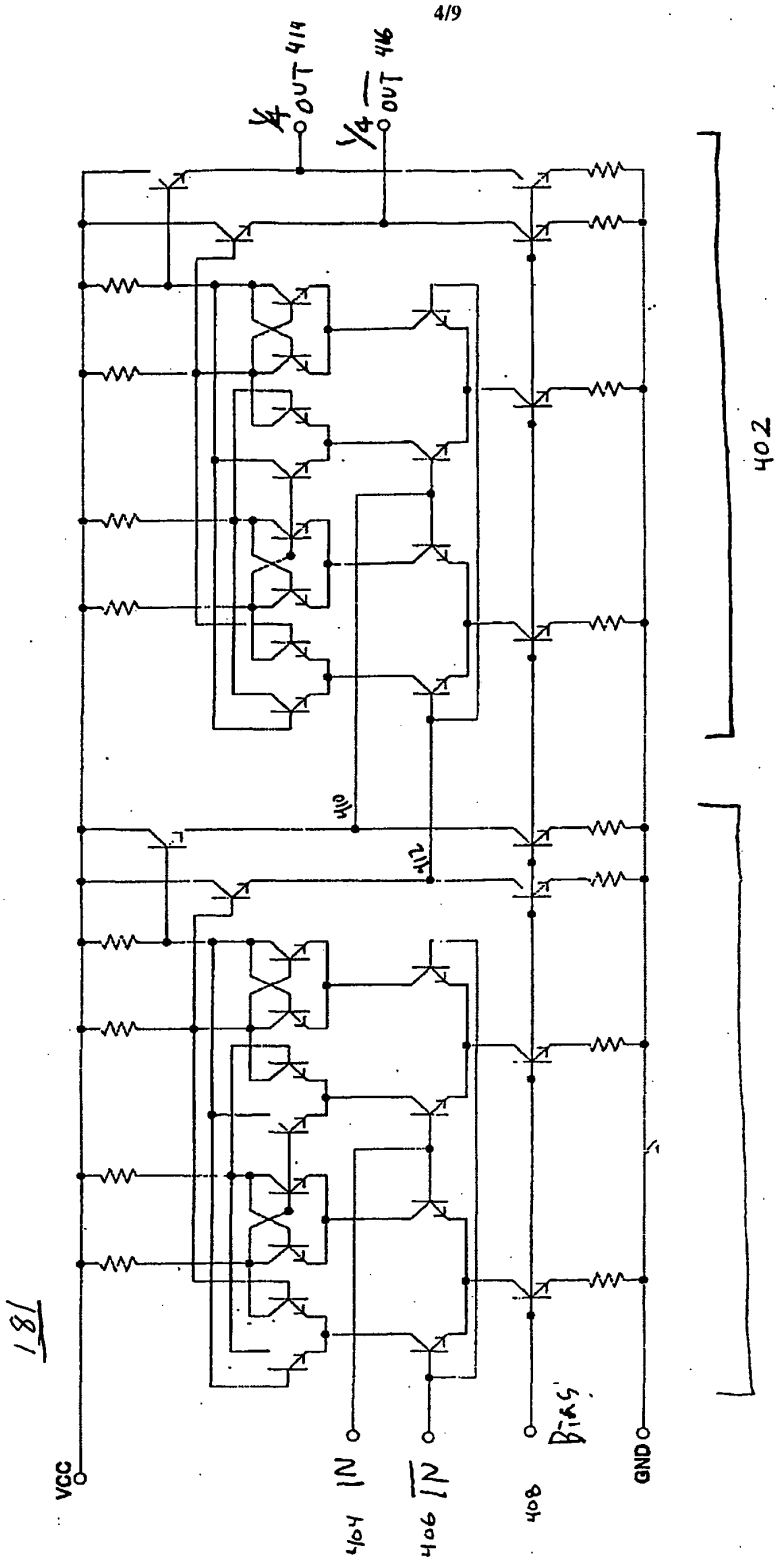

1/4 OUT 414
1/4 OUT 416
402
410
412
400
181
VCC
IN 404
IN 406
Bias 408
GND

Fig. 4

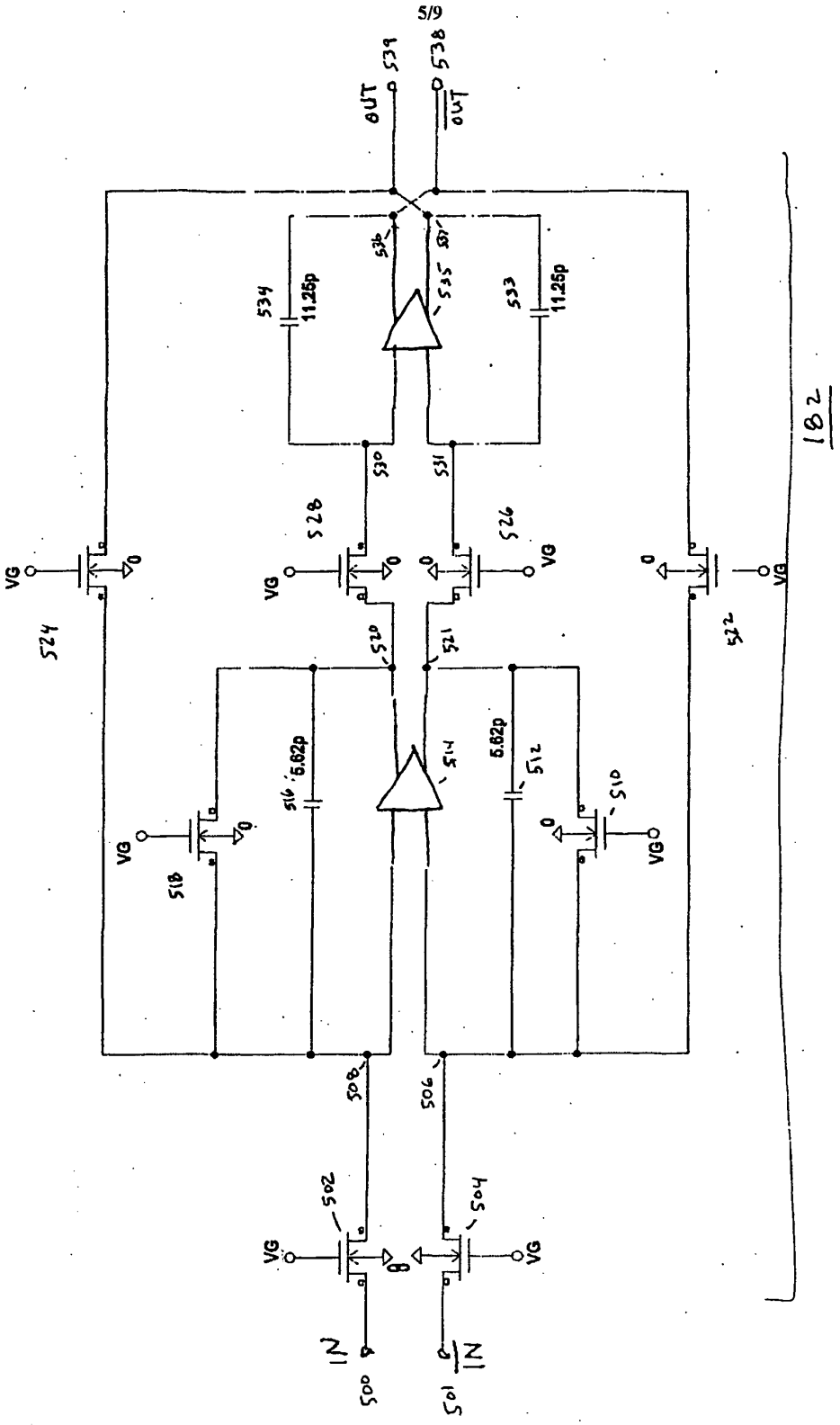

OUT
539
538
OUT
534
11.25p
533
11.25p
530
531
528
526
524
522
520
521
516
6.62p
514
512
6.62p
518
510
502
504
506
508
VG
0
IN
500
501
102

Fig. 5

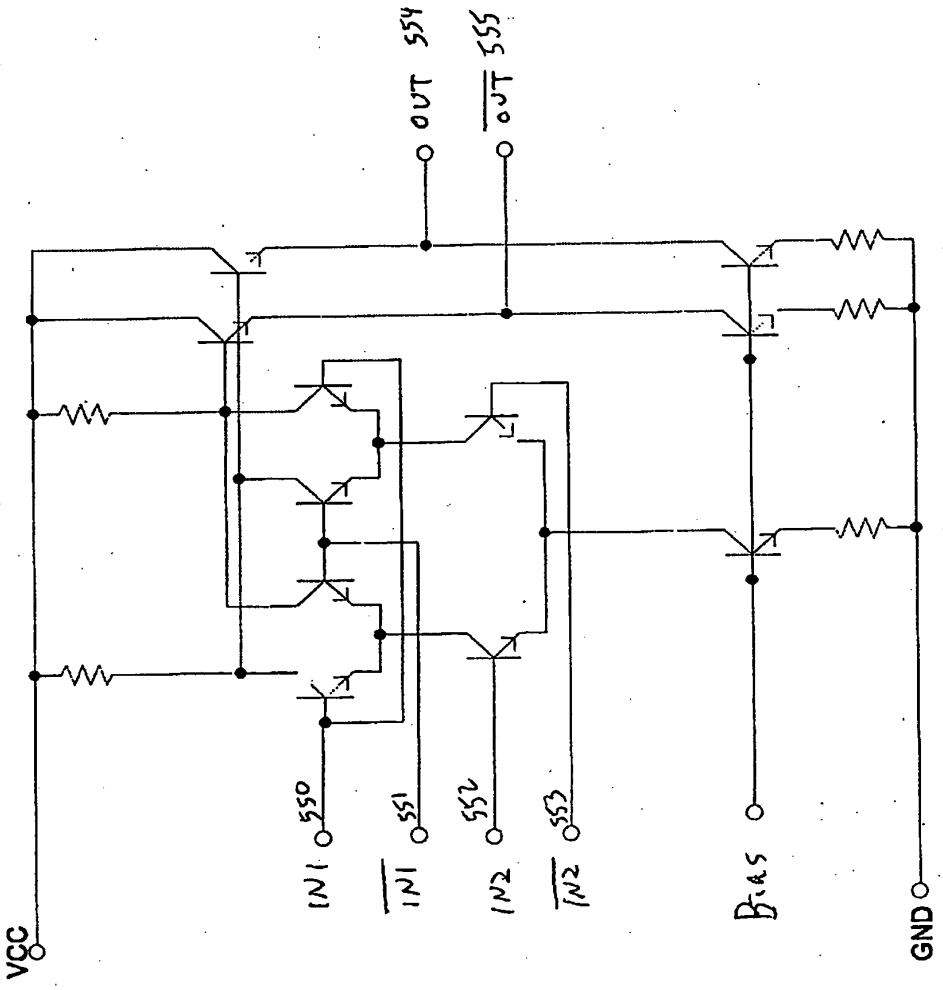


Fig 6

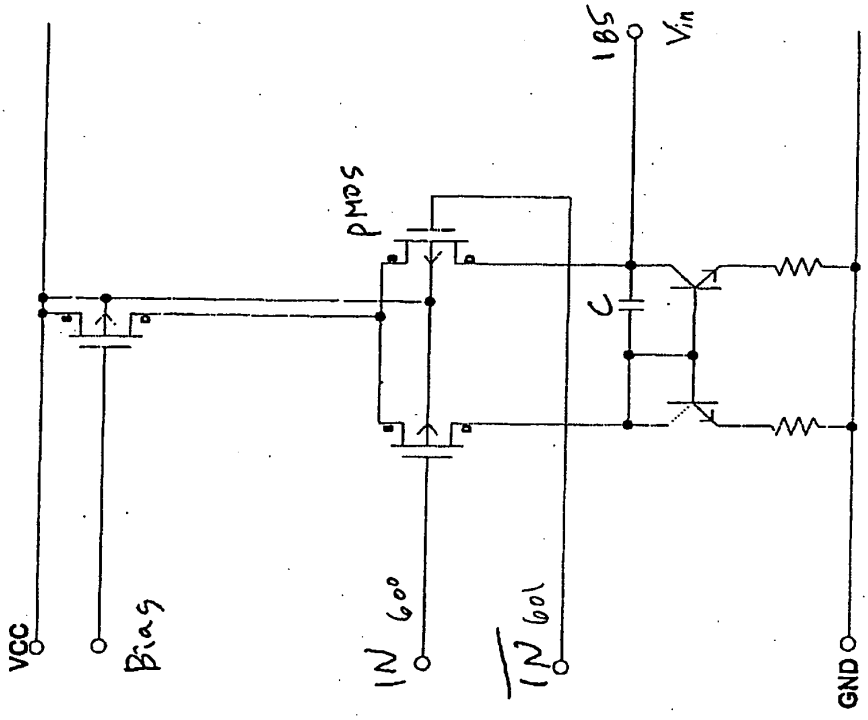


Fig. 7

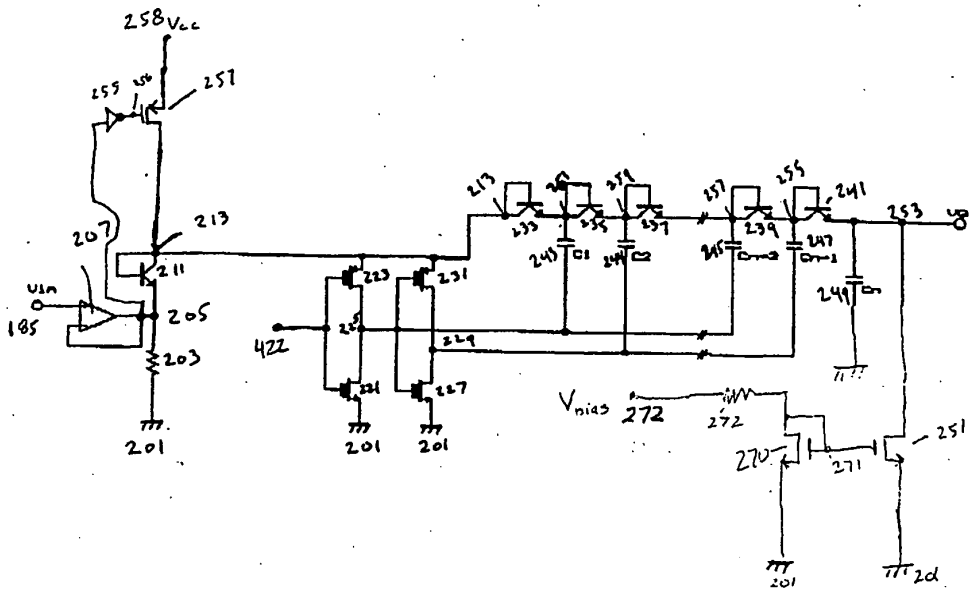

258 V_{cc}
257
255
207
213
211
205
203
185
201
422
V_{bias}
272
270
271
251
253
241
249

Fig. 8

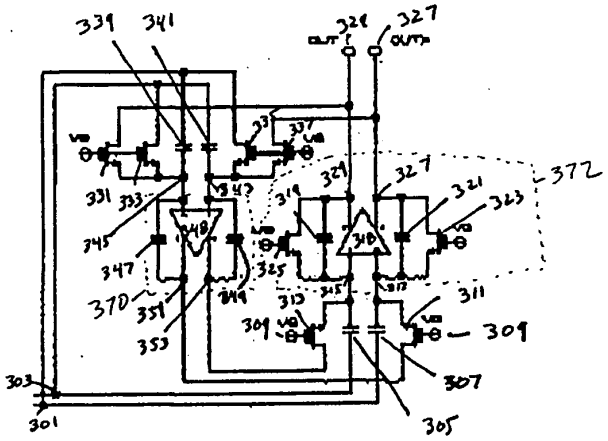

339
341
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327
OUT+
OUT-
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323
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Fig. 9

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(54) Title: ACTIVE FILTER CIRCUIT WITH DYNAMICALLY MODIFIABLE INTERNAL GAIN

(57) Abstract: Techniques are provided for the implementation of a signal processing circuit which expands the dynamic range of the signal processing circuit without interrupting the output of the circuit. The techniques can receive an input signal, process the signal through one of a plurality of dynamically modifiable signal processing circuits, and switch to processing the signal through another of the plurality of signal processing circuits without disturbing the output of the system.

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ACTIVE FILTER CIRCUIT WITH DYNAMICALLY MODIFIABLE INTERNAL GAIN

SPECIFICATION

This application claims priority to U.S. Provisional Application Serial Number 60/260,722 filed January 10, 2001, and U.S. Provisional Application Serial Number 60/288,976 filed May 4, 2001, each of which is incorporated by reference herein in its entirety.

BACKGROUND OF THE INVENTION

The present invention relates to signal processors and, more particularly, to signal processors that are dynamically modifiable for optimal performance and reduced power dissipation.

In order to expand the dynamic range of a signal processing system, companding signal processors can be used. A companding signal processor uses an input amplifier to amplify or attenuate a signal before it is provided to a signal processor, and an output amplifier is used to amplify or attenuate the signal provided by the signal processor. A signal processing circuit or signal processor includes an active filter. The gain of the output amplifier is the inverse of the gain of the input amplifier, thus conserving the overall gain of the signal processor. Ideally, the gains of the input amplifier and output amplifier should be dynamically variable. A signal strength detector can be used to measure the strength of the input signal and provide a processor appropriate gain control signal to the input amplifier and the output amplifier. See Y. Tsividis, "Externally linear, time-invariant systems and their application to companding signal processors," IEEE Transactions on Circuits and Systems II, Vol. 44, No. 2, February 1997. The gain control signal sets the amplification factors of the input amplifier and the output amplifier. However, this approach has the problem in that because the signal processor has memory, distortion in the output of the signal processor occurs whenever the amplification factors of the input amplifier and the output amplifier are changed.

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The analog floating point technique addresses the problem of distortion in the output whenever the amplification factors change. See E. Blumenkrantz, "The analog floating point technique," Proc. IEEE Symposium on Low Power Electronics, p. 72-73, 1995. This technique avoids distortion by altering the state variables of the signal processor when the amplification factors change. However, implementation of the analog floating point technique is complicated, and is sensitive to parasitics and component mismatch. Accordingly, there is a need for circuits which expand the dynamic range of a signal processor without interrupting the output of the system or causing distortion.

SUMMARY OF THE INVENTION

It is therefore an object of this invention to provide a circuit which has a large dynamic range and which operates in an energy-efficient manner without interrupting the output of the circuit or causing distortion.

In accordance with the present invention, there is provided an active filter system including a system input for receiving a system input signal, a system output for providing a system output signal, a main filter, a strength detector, a zero crossing detector and a gain control unit. The main filter having at least one successive filter stage having an input and an output, including a first filter stage, each filter stage having an associated input amplification stage including a signal input, a signal output coupled to the input of the associated filter stage and a gain control input for receiving a gain control signal that determines the amplification factor of the associated input amplification stage, the input of the input amplification stage associated with each filter stage, except for the input amplification stage associated with the first filter stage, being coupled to the output of a preceding filter stage, if any, the input of the amplification stage associated with the first filter stage being coupled to the system input, each filter stage having an associated output amplification stage including a signal input coupled to the output of the associated filter stage, a signal output and a gain control input for receiving a gain control signal that determines the amplification factor of the associated output amplification stage, the signal output of the output amplification stage associated with a selected one of the at least one filter

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stage being coupled to the system output. The strength detector having an input coupled to the output of the first filter stage, and having a first output and a second output for providing respective output signals indicative of whether the first filter stage is approaching saturation or is providing an output signal having less than a minimum acceptable signal to noise ratio. The zero crossing detector having at least one input coupled to respective ones of the at least one output of the at least one filter stage of the main filter, and having at least one output for providing at least one signal indicative of when a successive one of the at least one filter stage of the main filter provides a signal at its output that is approximately equal to zero. The gain control unit having a first input and a second input respectively coupled to the output of the strength detector and coupled to the at least one output of the zero crossing detector, and having a multiplicity of outputs for providing respective gain control signals to the gain control input of each input amplification stage and each output amplification stage associated with the at least one filter stage of the main filter, the gain control unit being responsive to signals provided initially by the strength detector indicative of the first filter stage approaching saturation or providing an output signal having less than the minimum acceptable signal to noise ratio, and a signal from the zero crossing detector indicative of the output signal provided by the first filter stage being approximately equal to zero for providing a gain control signal to the gain control input of the input amplification stage associated with the first filter stage so that the input amplification stage associated with the first filter stage has an amplification factor that results in a signal strength at its signal output which avoids saturation of the first filter stage and avoids the first filter stage providing a signal having less than the minimum acceptable signal to noise ratio, and for providing a gain control signal to the gain control input of the output amplification stage associated with the first filter stage so that the output amplification stage associated with the first filter stage has an amplification factor which is the reciprocal of the amplification factor of the input amplification stage associated with the first filter stage, the gain control unit being thereafter responsive to signals provided initially by the strength detector indicative of the first filter stage of the main filter approaching saturation or providing an output having less than the minimum acceptable signal to noise ratio, and to a

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signal from the zero crossing detector indicating that an output signal at the output of a successive filter stage, if any, being approximately equal to zero for providing a gain control signal to the gain control input of the input amplification stage associated with the successive filter stage so that the input amplification stage associated with the successive filter stage has an amplification factor that results in a signal strength at its signal output that avoids saturation of the successive filter stage and avoids the successive filter stage providing a signal having less than the minimum acceptable signal to noise ratio, and for providing a gain control signal to the gain control input of the output amplification stage associated with the successive filter stage so that the output amplification stage associated with the successive filter stage has an amplification factor which is a reciprocal of the amplification factor of the input amplification stage associated with the successive filter stage.

BRIEF DESCRIPTION OF THE DRAWINGS

Further objects, features, and advantages of the invention will become apparent from the following detailed description taken in conjunction with the accompanying figures showing illustrative embodiments of the invention, in which:

Fig. 1 is a block diagram illustrating a prior art signal processing system;

Fig. 2 is a block diagram illustrating a signal processing system in accordance with the present invention;

Fig. 3 is a circuit diagram illustrating the main filter of a signal processing system in accordance with the present invention;

Fig. 4 is a circuit diagram illustrating a switching unit of a signal processing system in accordance with the present invention;

Fig. 5 is a circuit diagram illustrating a shift register usable in a signal processing system in accordance with the present invention;

Fig. 6 is a circuit diagram illustrating a strength detector of a signal processing system in accordance with the present invention;

Fig. 7 is a circuit diagram illustrating a peak detector of a signal processing system in accordance with the present invention;

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Fig. 8 is a circuit diagram illustrating a threshold detector of a signal processing system in accordance with the present invention;

Figs. 9(a) and 9(b) are circuit diagrams illustrating a gain control unit of a signal processing system in accordance with the present invention;

Fig. 10 is a circuit diagram illustrating a comparator of a signal processing system in accordance with the present invention; and

Fig. 11 is a circuit diagram illustrating a transconductor of a signal processing system in accordance with the present invention.

Throughout the figures, unless otherwise stated, the same reference numerals and characters are used to denote like features, elements, components, or portions of the illustrated embodiments. Moreover, while the subject invention will now be described in detail with reference to the figures, and in connection with the illustrative embodiments, various changes and modifications to the described embodiments will be apparent to those skilled in the art without departing from the true scope and spirit of the subject invention as defined by the appended claims.

DETAILED DESCRIPTION OF THE INVENTION

Figure 1 illustrates an example of a prior art signal processing system 10. The signal processing system 10 is a companding filter. A companding filter amplifies or attenuates an input signal that is applied to a filter circuit, and attenuates or amplifies the output signal from the circuit. The prior art companding filter 10 includes an input 12, a signal strength detector 14, an input variable gain amplifier 16, a main filter 18, an output variable gain amplifier 20, and an output 22.

The input 12 of the signal processing system 10 is coupled to input 11 of the signal strength detector 14 and an input 30 of a variable gain input amplifier 16. The variable gain input amplifier 16 amplifies or attenuates the signal received by the input 30 depending on a gain control input signal received at a gain control input 13 of the variable gain input amplifier 16 and provides the resulting signal at its output 15. The output 15 of the variable gain input amplifier 16 is coupled to input 17 of a main filter 18. The main filter 18 processes the signal received at its input 17 and produces a processed output signal at its output 19. The output 19 of the main filter

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18 is coupled to input 21 of a variable gain output amplifier 20. The variable gain output amplifier 20 amplifies or attenuates the signal received at its input 21 depending on a gain control signal received at a gain control input 23 of the variable gain output amplifier 20 and provides a resulting signal at its output 24. The gain of the variable gain output amplifier 20 is the inverse of the gain of the variable gain input amplifier 16. The output 24 of the variable gain output amplifier 20 is connected to the output 22 of the signal processing system 10.

The signal strength detector 14 measures the strength (e.g., the voltage envelope) of the signal applied to the input 11 of the signal strength detector 14 and provides a gain control signal at its output 25, which is connected to the gain control inputs 13 and 23 of the variable gain input amplifier 16 and the variable gain output amplifier 20, respectively. Depending on the strength of the signal at the input 11 of the signal strength detector 14, different gain control signals are provided at the output 25 of the signal strength detector 14. If the signal applied to the input 12 of the signal processing system 10 is small, the strength detector 11 provides a gain control signal that causes the variable gain input amplifier 16 to have a relatively high gain, thereby causing the signal applied to the input 12 of the signal processing system 10 to be amplified before it is applied to the main filter 18, such that the signal is above the noise floor of the filter 18, *i.e.*, the noise generated by the filter. If the signal applied to the input 12 of the signal processing system 10, the strength deflector 14 provides a gain control signal that causes the variable gain input amplifier 16 to have a relatively low gain, thereby causing the signal applied to the input 12 of the signal processing system 10 to be slightly amplified or even attenuated before it is applied to the main filter 18 to avoid saturating the main filter 18.

Fig. 2 illustrates an exemplary signal processing system 100 in accordance with the present invention. The signal processing system 100 generates a processed signal with a strong in channel component well above the filter noise. The signal processing system 100 includes a system input 102, a main filter 106, a switching unit 130, a comparator 136, a shift register 144, a strength detector 154, a gain control unit 172, and a system output 190.

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A signal received by the system input 102 of the signal processing system 100, which typically includes an in-band component and an out-band component, is applied to an input 104 of the main filter 106. In the present embodiment, the main filter 106 is a second order filter, which includes two integrators (not shown in Fig. 2). Preferably, the main filter 106 has enough linear range to accommodate the in-band component and the out-band component of the signal without saturating. Each of the first and second integrators has a variable input gain stage and a variable output gain stage associated with it (not shown in Fig. 2). The main filter 106 processes the signal received at its input 104 as controlled by respective signals received at inputs 108, 110, 112, 114 and 116. These signals control the gain of the variable input gain stage and the variable output gain stage for each of the first and second integrators. The gain of the variable input gain stage and variable output gain stages associated with the first integrator should only be changed when the output of the first integrator is at or near zero. By changing the gain of the variable input gain stage and the variable output gain stage associated with the first integrator when the output of the first integrator is at or near zero, little or no transients are created in the signal produced at the output of the first integrator. Likewise, the gain of the variable input gain stage and the variable output gain stage associated with the second integrator should only be changed when the output of the second integrator is at or near zero. The main filter 106 produces a processed signal at each of its outputs 118, 120 and 122. The signal produced at the output 118 of the main filter 106 is the output of the first integrator of the main filter 106. The output 118 of the main filter 106 is connected to an input 124 of the switching unit 130, and an input 152 of the strength detector 154. The signal produced at the output 120 of the main filter 106 is the output of the second integrator of the main filter 106. The output 120 of the main filter 106 is connected to another input 126 of the switching unit 130. The signal produced at the output 122 of the main filter 106 is the output of the variable gain output stage associated with the first integrator of the main filter 106. The output 122 of the main filter 106 is connected to the system output 190 of the signal processing system 100. The structure and operation of the main filter 106 is described in greater detail hereinbelow with reference to Fig. 3.

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The switching unit 130 applies one of the signals received at its inputs 124, 126 to its output 132 in response to a signal received at an input 128. If a logical one voltage level (*i.e.*, 5 V) is received at the input 128, the switching unit 130 connects the input 124 and the output 132, and disconnects the input 120 from the output 132. If a logical zero voltage level (*i.e.*, ground potential) is received at the input 128, the switching unit 130 connects the input 126 to the output 132 and disconnects the input 124 from the output 132. The output 132 is connected to an input 134 of the comparator 136.

The comparator 136 compares a signal received at the input 134 against a reference voltage. If the voltage of the signal received at the input 134 is approximately equal to the reference voltage, the comparator 136 produces a signal equal to a logical one voltage level at an output 138 of the comparator 136. If the voltage of the signal received at the input 134 is not approximately equal to the reference voltage, the comparator 136 produces a signal equal to a logical zero voltage level at the output 138 of the comparator 136. The output 138 of the comparator 136 is connected to a clock input 140 of the shift register 144. In the present embodiment, the reference voltage may be zero.

The shift register 144 determines which of the outputs of the integrators of the main filter 106 the comparator 136 should measure against the reference voltage. A reset/enable input 142 of the shift register 144 is connected to an output 176 of the gain control unit 172. Outputs 146, 148, 150 of the shift register 144 are connected to inputs 166, 168, 170, respectively, of the gain control unit 172. If a logical one voltage level is received at the reset/enable input 142, the shift register 144 provides a logical one voltage level signal at the output 146, a logical zero voltage level signal at the output 148 and a logical zero voltage level signal at the output 150. If a logical zero voltage level signal is received at the reset/enable input 142 and a positive edge (*i.e.*, a logical zero voltage level changing to a logical one voltage level) is received at the input 140, the shift register 144 produces a logical zero voltage level signal on the output 146, produces a signal on the output 148 equal to the signal formerly on the output 146, and produces a signal on the output 150 equal to a logical OR of the signal formerly on the output 148 and the signal formerly

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on the output 150. The structure and operation of the shift register will be described in greater detail hereinbelow with reference to Fig. 5.

The signal strength detector 154 selects an amplification factor that is the most suitable for processing the signal received by the system input 102 of the signal processing system 100. The input 152 of the signal strength detector 154 is connected to the output 118 of the main filter 106, and outputs 156 and 158 of the signal strength detector 154 are connected to inputs 160 and 162, respectively, of the gain control unit 164. The signal strength detector 154 detects the voltage envelope of a signal received at the input 152 of the signal strength detector 154. A combination of a rectifier and a low-pass filter, well-known for use in many other applications, is one example of a circuit which can be used as an envelope detector of the signal strength detector 154. The signal strength detector 154 determines if the voltage envelope of the signal provided by the output 118 of the main filter 106 is below a first threshold whereby the signal to noise ratio of the output signal of the main filter 106 is approaching a minimum tolerable value with the main filter 106 having the present amplification factors, or exceeds a second threshold whereby the main filter 106 is entering saturation with the present amplification factors.

If the signal strength detector 154 detects that the voltage envelope of the signal received at its input 152 is not below the first threshold or does not exceed the second threshold, the signal strength detector 154 produces a signal equal to a logical zero voltage level on the output 156, and a signal equal to a logical zero voltage level on the output 158. For purposes of the specification and claims, positive logic is assumed. If the signal strength detector 154 detects that the voltage envelope of the signal received at its input 152 falls below the first threshold and does not exceed the second threshold, the signal strength detector 154 produces a logical one voltage level signal on its output 158, and a logical zero voltage level signal on its output 156. If the signal strength detector 154 detects that the voltage envelope of the signal received at its input 152 exceeds the first threshold and exceeds the second threshold, the signal strength detector produces a logical zero voltage level signal on its output 158, and a logical one voltage level signal on its output 156.

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The gain control unit 172, responsive to signals received at its inputs 160, 162, 166, 168, 170, provides signals at its output 176 to control the preset/enable input 142 of the shift register 144, and provides signals at its outputs 178, 180, 182, 184, 186 to control the respective amplification factors of the variable gain input stage associated with the first integrator, the variable gain output stage associated with the first integrator, the variable gain input stage associated with the second integrator, and the variable gain output stage associated with the second integrator. The outputs 178, 180, 182, 184, 186 of the gain control unit 172 are connected to the inputs 108, 110, 112, 114, 116, respectively, of the main filter 106. The output 176 of the gain control unit 172 is connected to the preset/enable input 142 of the shift register 144.

The gain control unit 172 provides signals to the main filter 106 and the shift register 144 that allow the amplification factors of the amplifiers within the main filter 106 to vary without causing transients to appear on signals at the system output 190 of the signal processing system 100. The gain control unit 172 begins the process of changing the amplification factors of the amplifiers of the main filter 106 by providing the preset/enable input 142 of the shift register 144 with a logical one voltage level signal to enable the shift register, which in turn provides a logical one voltage level signal to the input 128 of the switching unit 130. Once the comparator 136 senses that the signal received at the input 124 is equal to the reference voltage, the shift register 144 shifts the signals at its outputs 146, 148, 150, and causes a logical zero voltage level signal to be provided to the input 128 of the switching unit. This causes the gain control unit 172 to provide the main filter 106 with appropriate signals on its inputs 108, 110, 112, 114 to change the amplification factors of the variable gain input stage and the variable gain output stage associated with the first integrator, and the variable gain input stage associated with the second integrator of main filter 106 to the desired values. The amplification factor of the variable gain input stage associated with the second integrator must be changed at this point to compensate for the amplification factor change of the variable gain input stage associated with the first integrator. Then, once the comparator 136 senses that the signal received at the input 124 is equal to the reference voltage again, the shift register 144 shifts the signals at its outputs 146, 148, 150, causing the gain control

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unit 172 to provide the main filter 106 with the appropriate signals on its inputs 112, 114, 116 to change the amplification factors of the variable gain input stage and the variable gain output stage associated with the second integrator.

Fig. 3 illustrates the main filter 106 as shown in Fig. 2. The main filter 106 is a second order filter, and includes two integrators, a first integrator and a second integrator. Each of the integrators is associated with a respective variable gain input stage and a respective variable gain output stage. The variable gain input stage associated with the first integrator consists of resistors 216, 210, 204, 252, switches 232, 224, a capacitor 246, and an operational amplifier 240. The first integrator consists of the operational amplifier 240, the capacitor 246 and the resistor 252. The variable gain output stage associated with the first integrator consists of an operational amplifier 376, resistors 360, 384, 390, 205, and switches 213, 398. The variable gain input stage associated with the second integrator consists of resistors 258, 264, 278, switches 272, 286, a capacitor 334, and an operational amplifier 328. The second integrator consists of the operational amplifier 328, and the capacitor 334. The variable gain output amplification stage associated with the second integrator includes resistors 252, 292, 298, 312, 340, 354, switches 306, 320, operational amplifiers 240, 348, and the capacitor 246. A signal received at the input 104 is applied to a terminal 202 of the resistor 204, a terminal 208 of the resistor 210, and a terminal 214 of the resistor 216; a signal received at the input 108 is applied to a switch control terminal 230 of the switch 232, and a switch control terminal 211 of the switch 213; a signal received at the input 110 is applied to a switch control terminal 222 of the switch 224 and switch control terminal 396 of switch 398; a signal received at the input 112 is applied to a switch control terminal 284 of the switch 286; a signal received at the input 114 is applied to a switch control terminal 304 of the switch 306, and a switch control terminal 270 of the switch 272; and a signal received at the input 116 is applied to a switch control terminal 318 of the switch 320. Switches 222, 232, 213, 398, 320 and 306 may each be implemented as a CMOS transmission gate, in which an NMOS transistor and a PMOS transistor are connected in parallel with each other, the gate of the PMOS transistor is connected to the output of an inverter, the input of the inverter and the gate of the NMOS transistor are connected to each other and serve

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as the switch control terminal, and the source and drain of each transistor serve as the switch terminals. When a CMOS transmission gate is closed, the NMOS transistor and the PMOS transistor are active, such that a signal received on one terminal of the CMOS transmission gate is conveyed to the other terminal of the CMOS transmission gate. When a CMOS transmission gate is open, the NMOS transistor and the PMOS transistor are not active, such that a signal received on one terminal of the CMOS transmission gate is not conveyed to the other terminal of the CMOS transmission gate.

The variable gain input stage associated with the first integrator may amplify the signal received at the input 104 by one of three amplification factors and produce an output signal at a node 217. If the signals received at the inputs 108 and 110 are a logical zero voltage level (*i.e.*, ground potential) and a logical zero voltage level, respectively, the variable gain input stage amplifies the signal received at the input 104 by a relatively low amplification factor. In the present embodiment, the relatively low amplification factor may be one-tenth. If the signals received at the inputs 108 and 110 are a logical zero voltage level and a logical one voltage level (*i.e.*, 5V), respectively, the variable gain input stage amplifies the signal received at the input 104 by a relatively moderate amplification factor. In the present embodiment, the relatively moderate amplification factor is one. If the signals received at the inputs 108 and 110 are a logical one voltage level and a logical zero voltage level, respectively, the variable gain input stage amplifies the signal received at the input 104 by a relatively high amplification factor. In the present embodiment, the relatively high amplification factor is ten. In the present embodiment, the signals received at the inputs 108 and 110 should never both be a logical one voltage level.

The other terminal 206 of the resistor 204 is coupled to a terminal 226 of the switch 224, a terminal 234 of the switch 232, an inverted input 236 of the operational amplifier 240, a terminal 244 of the capacitor 246, a terminal 250 of the resistor 252, a terminal 290 of the resistor 292, a terminal 296 of the resistor 298 and a terminal 310 of the resistor 312, all of which form a node 217. In the present embodiment, the resistor 204 has a resistance of 200 kΩ.

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The other terminal 212 of the resistor 210 is connected to a terminal 220 of the switch 224. In the present embodiment, the resistor 210 has a resistance of 22.22 kΩ. The terminal 226 of the switch 224 is connected to the node 217. The switch 224 closes to connect its terminal 220 to its other terminal 226 if the signal received at the switch control terminal 222 is a logical one voltage level. If the signal at the switch control terminal 222 is at a logical zero voltage level, the switch 224 opens to disconnect its other terminal 220 from its terminal 226 resulting in an open circuit between those terminals.

The other terminal 218 of the resistor 216 is connected to a terminal 228 of the switch 232. In the present embodiment, the resistor 216 has a resistance of 2.02 kΩ. The terminal 234 of the switch 232 is connected to the node 217. The switch 232 closes to connect its terminal 228 to its other terminal 234 if the signal received at its switch control terminal 230 is a logical one voltage level. If the signal at the switch control terminal 230 is a logical zero voltage level, the switch 232 opens to disconnect its terminal 228 from its other terminal 234 resulting in an open circuit between those terminals.

The first integrator filters the signal received at the node 217 and produces a signal at a node 219, which is formed by the common connection of the other terminal 254 of the resistor 252, an output 242 of the operational amplifier 240, the other terminal 248 of the capacitor 246, the terminal 256 of the resistor 258, the terminal 262 of the resistor 264, the terminal 276 of the resistor 278, the terminal 358 of the resistor 360 and the output 118. The other terminal 254 of the resistor 252 is connected to the node 219. In the present embodiment, the resistor 254 has a resistance of 20 kΩ. The other terminal 248 of the capacitor 246 is connected to the node 219. In the present embodiment, the capacitor 246 has a capacitance of 80 pF. In the present embodiment, the operational amplifier 240 is a model LF347 operational amplifier available from National Semiconductor Corporation of Santa Clara, California.

The variable gain output stage associated with the first integrator may amplify the signal received at the node 219 by one of three factors and produce an amplified signal at the output 122. If the signals received at the inputs 108 and 110

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are a logical zero voltage level and a logical zero voltage level, respectively, the variable gain output stage amplifies the signal received at the node 219 by a relatively high amplification factor. In the present embodiment, the relatively high amplification factor may be ten. If the signals received at the inputs 108 and 110 are a logical zero voltage level and a logical one voltage level, respectively, the variable gain output stage amplifies the signal received at the node 219 by a relatively moderate amplification factor. In the present embodiment, the relatively moderate amplification factor is one. If the signals received at the inputs 108 and 110 are a logical one and a logical zero voltage level, respectively, the variable output gain stage amplifies the signal received at the node 219 by a relatively low amplification factor. In the present embodiment, the relatively low amplification factor is one-tenth. In the present embodiment, the signals received at the inputs 108 and 110 should never both be a logical one voltage level.

The other terminal 370 of the resistor 360 is connected to an inverted input 374 of the operational amplifier 376, a terminal 382 of the resistor 384, a terminal 388 of the resistor 390, and a terminal 203 of the resistor 205. The common connection of the other terminal 370 of the resistor 360, the inverted input 374 of the operational amplifier 376, the terminal 382 of the resistor 384, the terminal 388 of the resistor 390, and the terminal 203 of the resistor 205 form a node 225. In the present embodiment, the resistor 360 has a resistance of 20 kΩ. In the present embodiment, the operational amplifier 376 is a model LF347 operational amplifier available from National Semiconductor Corporation of Santa Clara, California. The other terminal 386 of the resistor 384 is connected to the output 122 of the main filter 106. In the present embodiment, the resistor 384 has a resistance of 200 kΩ.

The other terminal 392 of the resistor 390 is connected to a terminal 394 of the switch 398. In the present embodiment, the resistor 390 has a resistance of 22.22 kΩ. The other terminal 201 of the switch 398 is connected to the output 122 of the main filter 106. The switch 398 closes to connect its terminal 394 to its other terminal 201 if the signal received at the switch control terminal 396 is a logical one voltage level. If the signal at the switch control terminal 396 is a logical zero voltage

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level, the switch 398 opens to disconnect its terminal 394 from its other terminal 201 resulting in an open circuit between those terminals.

The other terminal 207 of the resistor 205 is connected to a terminal 209 of the switch 213. In the present embodiment, the resistor 205 has a resistance of 2.02 kΩ. The other terminal 215 of the switch 213 is connected to the output 122 of the main filter 106. The switch 213 closes to connect its terminal 209 to its other terminal 215 if the signal received at the switch control terminal 211 is a logical one voltage level. If the signal at the switch control terminal 211 is a logical zero voltage level, the switch 213 opens to disconnect its terminal 209 from its other terminal 215 resulting in an open circuit between those terminals.

The variable gain input stage associated with the second integrator may amplify the signal received at the node 219 by one of three factors and produce an output signal at a node 221, at which the other terminal 288 of the switch 286, the other terminal 274 of the switch 272, the other terminal 260 of resistor 258, one terminal 332 of the capacitor 334 and the inverting impact of the operational amplifier 328 are commonly connected. If the signals received at the inputs 112 and 114 are a logical zero voltage level and a logical zero voltage level, respectively, the variable gain input stage amplifies the signal received at the node 221 by a relatively low amplification factor. In the present embodiment, the relatively low factor is one-tenth. If the signals received at the inputs 112 and 114 are a logical zero voltage level and a logical one voltage level, respectively, the variable gain input stage amplifies the signal received at the node 221 by a relatively moderate amplification factor. In the present embodiment, the relatively moderate amplification factor is one. If the signals received at the inputs 112 and 114 are a logical one voltage level and a logical zero voltage level, respectively, the variable gain input stage amplifies the signal received at the node 221 by a relatively high amplification factor. In the present embodiment, the relatively high amplification factor is ten. In the present embodiment, the signals received at the inputs 112 and 114 should never both be a logical one voltage level. The other terminal 260 of the resistor 258 is connected to node 221. In the present embodiment, the resistor 258 has a resistance of 10 kΩ.

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The other terminal 266 of the resistor 264 is connected to one terminal 268 of the switch 272. In the present embodiment, the resistor 264 has a resistance of 1.11 kΩ. The other terminal 274 of the switch 272 is connected to the node 221. The switch 272 closes to connect its terminal 268 to its other terminal 274 if the signal received at the switch control terminal 270 is a logical one voltage level. If the signal at the switch control terminal 270 is a logical zero voltage level, the switch 272 opens to disconnect its terminal 268 from its other terminal 274 resulting in an open circuit between those terminals.

The other terminal 280 of the resistor 278 is connected to one terminal 282 of the switch 286. In the present embodiment, the resistor 278 has a resistance of 0.10 kΩ. The other terminal 288 of the switch 286 is connected to the node 221. The switch 286 closes to connect its terminal 282 to its other terminal 288 if the signal received at the switch control terminal 284 is a logical one voltage level. If the signal at the switch control terminal 284 is a logical zero voltage level, the switch 286 opens to disconnect its terminal 282 from its other terminal 288 resulting in an open circuit between those terminals.

The second integrator filters the signal received at the node 221 and produces a filtered signal at the output 120 of the main filter 106. The other terminal 336 of the capacitor 334 is connected to the output 120. In the present embodiment, the capacitor 334 has a capacitance of 80 pF.

The output 330 of the operational amplifier 328 is connected to the output 120 of the main filter 106. In the present embodiment, the operational amplifier 328 may be implemented using a model LF347 operational amplifier available from National Semiconductor Corporation of Santa Clara, California.

The variable gain output stage associated with the second integrator may amplify the signal received at terminal 338 of the resistor 340 by one of three factors and produce an amplified signal at the node 217. If the signals received at the inputs 116 and 114 are a logical zero voltage level and a logical zero voltage level, respectively, the variable gain output stage amplifies the signal received at terminal 338 of the resistor 340 by a relatively low amplification factor. In the present embodiment, the relatively low amplification factor is one-tenth. If the signals

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received at the inputs 116 and 114 are a logical zero voltage level and a logical one voltage level, respectively, the variable gain output stage amplifies the signal received at terminal 338 of the resistor 340 by a relatively moderate amplification factor. In the present embodiment, the relatively moderate amplification factor is one. If the signals received at the inputs 116 and 114 are a logical one voltage level and a logical zero voltage level, respectively, the variable gain output stage amplifies the signal received at terminal 338 of the resistor 340 by a relatively high amplification factor. In the present embodiment, the relatively high amplification factor is ten. In the present embodiment, the signals received at the inputs 116 and 114 should never both be a logical one voltage level.

The terminal 338 of the resistor 340 is coupled to the output 120. The other terminal 342 of the resistor 340 corresponds with an inverted input 344 of the operational amplifier 348 and the other terminal 352 of the resistor 354. In the present embodiment, the resistor 340 has a resistance of 10 kΩ.

The terminal 356 of the resistor 354 is connected to the node 223, at which the terminal 356 of resistor 354, the output 350 of the operational amplifier 348, the other terminal 394 of the resistor 292, the other terminal 308 of the switch 306 and the other terminal 322 of the switch 320 are commonly connected. In the present embodiment, the resistor 354 has a resistance of 10 kΩ.

The output 350 of the operational amplifier 348 is connected to the node 223. In the present embodiment, the operational amplifier 348 is implemented using the model LF347 operational amplifier available from National Semiconductor Corporation of Santa Clara, California. In the present embodiment, the resistor 292 has a resistance of 10 kΩ.

The other terminal 300 of the resistor 298 is connected to terminal 302 of the switch 306. In the present embodiment, the resistor 298 has a resistance of 1.11 kΩ. The other terminal 308 of the switch 306 is connected to the node 223. The switch 306 closes to connect its terminal 302 to its other terminal 308 if the signal received at the switch control terminal 304 is a logical one voltage level. If the signal at the switch control terminal 304 is a logical zero voltage level, the switch 306 opens

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to disconnect its terminal 302 from its other terminal 308 resulting in an open circuit between those terminals.

The other terminal 314 of the resistor 312 is connected to a terminal 316 of the switch 320. In the present embodiment, the resistor 312 has a resistance of 0.10 kΩ. The other terminal 322 of the switch 320 is connected to the node 223. The switch 320 closes to connect its terminal 316 to its other terminal 322 if the signal received at the switch control terminal 318 is a logical one voltage level. If the signal at the switch control terminal 318 is a logical zero voltage level, the switch 320 opens to disconnect its terminal 316 from its other terminal 322 resulting in an open circuit between those terminals.

Fig. 4 illustrates an exemplary embodiment of the switching unit 130 as shown in Fig. 2. The switching unit 130 includes an input 124, an input 126, an input 128, a first switch 406, a second switch 416 and an output 132. The switching unit 130 provides one of the signals received at the inputs 124, 126 to the output 132 in response to a signal received at the input 128.

A signal received at the input 124 is applied to one terminal 402 of the first switch 406; a signal received at the input 126 is applied to one terminal 412 of the second switch 416; and a signal received at the input 128 is applied to a switch control terminal 404 of the first switch 406 and an inverting switch control terminal 414 of the second switch 416. The first switch 406 closes to connect its terminal 402 to its other terminal 408 if the signal received at the switch control terminal 404 is a logical one voltage level (*i.e.*, 5 V). If the signal at the switch control terminal 404 is a logical zero voltage level (*i.e.*, ground potential), the first switch 406 opens to disconnect its terminal 402 from its other terminal 408 resulting in an open circuit between those terminals. The other terminal 408 of the first switch 406 is connected to the output 132 of the switching unit 130.

The second switch 416 closes to connect its terminal 412 to its other terminal 418 if the signal received at the inverting switch control terminal 414 is a logical one voltage level. If the signal at the inverting switch control terminal 414 is a logical zero voltage level, the second switch 416 opens to disconnect its terminal 412 from its other terminal 418 resulting in an open circuit between those terminals. The

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other terminal 418 of the first switch 416 is connected to the output 132 of the switching unit 130.

Fig. 10 illustrates the comparator 136. The comparator 136 includes an input 134, an output 138, a comparator circuit 1006, and a reference voltage 1003. The comparator circuit 1006 has an input 1002, an input 1004, and an output 1008. In the present embodiment, the comparator 136 may be implemented using a model LM219 comparator available from National Semiconductor Corporation of Santa Clara, California. The input 1002 is connected to the input 134, the input 1004 is connected to the reference voltage 1003, and the output 1008 is connected to the output 138. In the present embodiment, the reference voltage 1003 is ground. The comparator circuit 1006 measures a signal received at the input 1002 against the reference voltage 1003 received at the input 1004. If the voltage of the signal received at the input 1002 is approximately equal to the reference voltage 1003 received at the input 1004, the comparator circuit 1006 produces a logical one voltage level signal at the output 1008. If the voltage of the signal received at the input 1002 is not approximately equal to the reference voltage 1003, the comparator circuit 1006 produces a logical zero voltage level signal at the output 1008. The output 138 of the comparator 136 is connected to the clock input 140 of the shift register 144.

Fig. 5 illustrates an exemplary embodiment of the shift register 144 as shown in Fig. 2. The shift register 144 includes an clock input 140, an input 142, a first positive edge triggered D-type flip flop 508, a second positive edge triggered D-type flip flop 518, a third positive edge triggered D-type flip flop 528, a two input OR gate 532, an output 146, an output 148 and an output 150. The shift register 144 indicates which of the first and second integrators have reached the reference voltage. A signal received at the clock input 140 is applied to a clock input 506 of the first positive edge triggered D-type flip flop 508, a clock input 516 of the second positive edge triggered D-type flip flop 518, and a clock input 526 of the third positive edge triggered D-type flip flop 528; and a signal received at the input 142 is applied to a preset/enable input 504 of the first positive edge triggered D-type flip flop 508, a reset/enable input 514 of the second positive edge triggered D-type flip flop 518, and a reset/enable input 524 of the third positive edge triggered D-type flip flop 528.

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The first positive edge triggered D-type flip flop 508 produces a logical zero voltage level signal (*i.e.*, ground potential) on its data output 510 if a signal received at the preset/enable input 504 is equal to a logical one voltage level (*i.e.*, 5 V). If the signal received at the preset/enable input 504 is equal to a logical zero voltage level, the first positive edge triggered D-type flip flop 508 causes a signal received at its data input 502, which is connected to ground, to be provided at its data output 510 each time a positive transition of a signal from a logical zero voltage level to a logical one voltage level is received by its clock input 506. The output 510 is connected to the data input 512 of the second positive edge triggered D-type flip flop 518, and the output 146.

The second positive edge triggered D-type flip flop 518 produces a logical zero voltage level signal on its data output 520 if a signal received at the reset/enable input 514 is equal to a logical one voltage level. If the signal received at the reset/enable input 514 is equal to a logical zero voltage level, the second positive edge triggered D-type flip flop 518 causes a signal received at its data input 512 to be provided at its data output 520 at each time a positive transition of a signal from a logical zero voltage level to a logical one voltage level is received by its clock input 516. The data input 512 of the second positive edge triggered D-type flip-flop 518 is connected to the data output 510 of the first positive edge triggered D-type flip flop 508 and the output 146 of the shift register 144. The data output 520 is connected to one input of the two input OR gate 532 and the output 148 of the shift register 144.

The third positive edge triggered D-type flip flop 528 produces a logical zero voltage level signal on its data output 530 if a signal received at its reset/enable input 524 is equal to a logical one voltage level. If the signal received at the reset/enable input 524 is equal to a logical zero voltage level, the third positive edge triggered D-type flip flop 528 causes a signal received at its data input 522 to be provided at its data output 530 each time a positive transition of a signal from a logical zero voltage level to a logical one voltage level is received by its clock input 526. The data input 522 of the third positive edge triggered D-type flip-flop 528 is connected to the output of the two input OR gate 532. The data output 530 of the third positive edge triggered D-type flip-flop 528 is connected to the other input of the

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two input OR gate 532 and the output 150 of the shift register 144 provide more explanation of how the shift register determines which of the outputs of the integrators of the main filter 106 the comparator should measure against the reference voltage.

Referring to Fig. 6, there is shown an exemplary embodiment of the strength detector 154 as shown in Fig. 2. The strength detector 160 includes an input 152, a peak detector 604, a first threshold detector 610, a second threshold detector 616, a first inverter gate 622, a second inverter gate 628, a third inverter gate 634, a first output 156, and a second output 158. The peak detector 604 and the first threshold detector 610 are described in more detail below with reference to Fig. 7 and Fig. 8, respectively. The strength detector 154 senses the voltage envelope of the signal received at the input 152, and decides whether it would be appropriate to change amplification factors of the variable gain stages of the main filter 106. The saturation threshold represents the strength of the input signal received by the main filter 106 at which the main filter 106 approaches saturation given the present amplification factors of the main filter 106. The noise floor threshold represents the strength of the input signal received by the main filter 106 at which the output signal of the main filter 106 has a minimum acceptable signal-to-noise ratio given the present amplification factors of the main filter 106.

A signal received at the input 152 of the strength detector 154 is applied to an input 602 of the peak detector 604. The peak detector 604 receives an input voltage signal at its input 602 and provides a current signal representative of the peak of the voltage envelope of the input signal at its output 606. The output 606 of the peak detector 604 is coupled to an input 608 of the first threshold detector 610 and an input 614 of the second threshold detector 616. The first threshold detector 610 provides a logical one voltage level on its output 612 if the signal at its input 608 has a voltage envelope peak greater than the saturation threshold, and provides a logical zero voltage level on its output 612 if the signal at the input 608 has a voltage envelope peak less than the saturation threshold limit. The output 612 of the first threshold detector 610 is coupled to an input 620 of the first inverter gate 622. The second threshold detector 616 provides a logical one voltage level on its output 618 if

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the signal at its input 614 has a voltage envelope peak greater than the noise floor threshold, and provides a logical zero voltage level on its output 618 if the signal at its input 614 has a voltage envelope peak less than the noise floor threshold. The output 618 of the second threshold detector 616 is coupled to the input 632 of the third inverter gate 634.

The inverter gate 622 inverts the signal received at its input 620 and provides the inverted signal at its output 624. The output 624 is connected to the input 626 of the second inverter gate 628. The second inverter gate 628 inverts the signal received at its input 626 and provides the inverted signal at the output 630. The output 630 is couple to the first output 156 of the strength detector 154. The third inverter gate 634 inverts the signal received at its input 632 and provides the inverted signal at its output 636. The output 636 is connected to the second output 158 of the strength detector 154.

Fig. 7 illustrates an exemplary embodiment of the peak detector 604 of the strength detector 154 of Fig. 6. The peak detector 604 includes an NMOS transistor Q_1, a PMOS transistor Q_3, an NMOS transistor Q_4, a PMOS transistor Q_5, a PMOS transistor Q_6, a capacitor 750, a resistor 758, and a transconductor 742.

A signal received by the input 602 of the peak detector 604 is applied to a positive input 744 of the transconductor 742. The transconductor 742 provides at its output 748 a signal which is equal to the difference in the signal received by its positive input 744 and the signal received by the negative input 746, which is connected to ground, scaled by a transconductance G_{in} of the transconductor 742. In the present embodiment the transconductor 742 has a transconductance G_{in} of 1 microampere per volt. The current signal provided at the output 748 of the transconductor 742 is applied to the gate 710 of the PMOS transistor Q_3 and the gate 724 of the NMOS transistor Q_4, which are connected to form an inverter, the gate 726 and the drain 732 of the diode connected PMOS transistor Q_5, the drain 736 and the backgate 738 of the PMOS transistor Q_6, and the drain 702 of the NMOS transistor Q_1. The inverter formed by the PMOS transistor Q_3 and the NMOS transistor Q_4 are connected between supply voltages V_{DD} and V_{SS}, and the commonly connected drains of PMOS transistor Q_3 and NMOS transistor Q_4 are connected to the source 728 of

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the diode connected PMOS transistor Q_5 and the gate 734 of PMOS transistor Q_6. The back gates 714 and 720 of the PMOS transistor Q_3 and the NMOS transistor Q_4 are connected to supply voltages V_{DD} and V_{SS}, respectively. The commonly connected gate 726 and drain 732 of the diode connected PMOS transistor Q_5 are connected to the drain 736 and backgate 738 of PMOS transistor Q_6. The back gate 730 of diode connected PMOS transistor is connected to supply voltage V_{DD}. The source 740 of the PMOS transistor Q_6 is connected to the gate 748 of NMOS transistor Q_1, one terminal of capacitor 750, one terminal 756 of the resistor 758 and the output terminal 606 of the peak detector 606. The other terminal 754 of the capacitor 750 and the other terminal 1060 of the resistor 758 are connected to supply voltage V_{SS}. The drain 702 of NMOS transistor Q_1 is connected to the output 748 of the transconductor 742, the drain 736 and the backgate 738 of PMOS transistor Q_6, the commonly connected gate 726 and drain 732 of the diode connected PMOS transistor Q_5, and the commonly connected gates 710 and 724 of the PMOS transistor Q_3 and the NMOS transistor Q_4 forming the inverter. The source 706 of the NMOS transistor Q_1 is connected to supply voltage V_{SS}.

The NMOS transistor Q_1 of the peak detector 604 forms half of a NMOS current mirror. The other half of the current mirror consists of an NMOS transistor Q_2 of the threshold detector 610 (shown in Fig. 8). Thus, when the output 606 of the peak detector 604 is connected to the input 608 of the threshold detector 610, a complete NMOS current mirror is formed which acts as a current memory storing the peak current, *i.e.*, the current that represents the voltage envelope peak of input signal of the main filter. The CMOS inverter formed by PMOS transistor Q_3 and NMOS transistor Q_4 acts as a current comparator which compares the current provided by the output 748 of the transconductor 742 with the drain current of NMOS transistor Q_1.

When the drain current of NMOS transistor Q_1 is larger that the current provided by the output 748 of the transconductor 742, the commonly connected gates 710 and 724 of the PMOS transistor Q_3 and the NMOS transistor Q_4 forming the inverter are at a logical zero voltage level (*i.e.*, V_{SS}) and the commonly connected drains 716 and 718 of those transistors are at a logical one voltage level (*i.e.*, V_{DD}).

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Because the gate 734 of PMOS transistor Q_6 is connected to the commonly connected drains 716 and 718 of the inverter transistors Q_3 and Q_4, it is also at the logical one voltage level, and the PMOS transistor Q_6 is turned off. If the current provided by the output 748 of the transconductor 742 becomes larger than the drain current of NMOS transistor Q_1, the commonly connected gates 710 and 724 of PMOS transistor Q_3 and NMOS transistor Q_4 switches to a logical one voltage level, and the commonly connected drains 716 and 718 of those transistors switches to a logical zero voltage level; this causes the gate 734 of the PMOS transistor Q_6 to go to the logical zero voltage level and the PMOS transistor Q_6 to turn on. In this manner, PMOS transistor Q_6 connects the gates 708 and 802 (shown in Fig. 8) of NMOS transistors Q_1 and Q_2, terminal 752 of capacitor 750 and terminal 756 of the resistor 758 to the output 748 of the transconductor 742, and the current mirror follows the current provided by the output 748 of transconductor 742. When the current provided by the output 748 of the transconductor 742 starts to fall below the new peak current, the commonly connected gates 710 and 724 of PMOS transistor Q_3 and NMOS transistor Q_4 switch back to the logical zero voltage level and the commonly connected drains of those transistors to switch back to a logical one voltage level. This causes the PMOS transistor Q_6 to turn off leaving the gates 708 and 802 (shown in Fig. 8) of NMOS transistors at the voltage on the terminal 752 of the capacitor 750, thus allowing the NMOS current mirror to hold the new peak current, though the new peak current degrades as the capacitor 750 discharges through the resistor 758. Thereafter, the diode connected PMOS transistor Q_5 starts to supply the difference between the current provided by the output 748 of the transconductor 742 and the drain current of the NMOS transistor Q_1 to the node formed by the output 748 of the transconductor 743, the drain of NMOS transistor Q_1 and the commonly connected gates 710 and 724 of the PMOS transistor Q_3 and the NMOS transistor Q_4.

Fig. 8 illustrates an exemplary embodiment of the first threshold detector 610 of the strength detector 160 of Fig. 6. The first threshold detector 610 compares the current representing of the voltage envelope peak of a signal received at the input 602 of the peak detector 604 to a reference current supplied by a current source 826. The first threshold detector 610 includes an NMOS transistor Q_2, a

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PMOS transistor Q_7, a PMOS transistor Q_8, the current source 826 and an output 612 of the first threshold detector 610. Any number of threshold detectors can be connected to the peak detector 604 to derive a corresponding number of signal strength detector outputs.

As explained above in connection with Fig. 7, the NMOS transistor Q_2 of the first threshold detector 610 forms half of an NMOS current mirror that acts as a current memory which stores the peak current corresponding to the voltage envelope peak of the signal received at the input 602 of the peak detector 604. The other half of the NMOS current mirror that acts as a current memory consists of the NMOS transistor Q_1 of the peak detector 604, shown in Fig. 7, which has its gate 708 connected (via the output 606 of the peak detector 604) to the input 608 of the first threshold detector 610. The input 608 is connected to the gate 802 of NMOS transistor Q_2 to form a complete NMOS current mirror. The source 808 and the backgate 806 of the NMOS transistor Q_2 are connected to supply voltage V_{ss}. The drain 804 of the NMOS transistor Q_2 is connected to the drain 810 of the PMOS transistor Q_7.

The NMOS transistor Q_7, the NMOS transistor Q_8 and the current source 826 form a current mirror that causes a current to flow through the NMOS transistor Q_7 that mirrors the current of the current source 826. The gate 814 of the NMOS transistor Q_7 is connected to the gate 818 of the NMOS transistor Q_8, the drain 820 of the NMOS transistor Q_8, and the positive terminal 822 of the current source 826. The source 812 of the NMOS transistor Q_7 and the source 816 of NMOS transistor are connected to supply voltage V_{DD}. The drain 810 of the NMOS transistor Q_7 is connected to the drain 804 of the NMOS transistor Q_2 and the output 612 of the threshold detector 610. The negative terminal 824 of the current source 826 is connected to ground.

The current source 826 produces a reference current that represents the threshold voltage of the first threshold detector 610. The reference current can be any value, for example 100 uA, and the transistors Q_7, Q_8 of the first threshold detector 610 are scaled to cause the desired current to flow through the transistor Q_7. The preferred form of a current source is a resistance connected between the drain 820 of

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NMOS transistor Q_8 and ground. In the present example the reference current generated by the current source in the first threshold detector 610 is 5.5 mA.

The output 612 of the first threshold detector 610 indicates whether the respective amplification factors of the main filter 106 should be decreased given the voltage envelope of the signal received at the input 602 of the peak detector 604. If the current flowing through the transistor Q_2, which represents the voltage envelope peak of the signal received at the input 602 of the peak detector 604 (shown in Fig. 7), exceeds the current flowing through the transistor Q_7, which is related to the reference current of the current source 826, the output 612 of the first threshold detector 610 will be at a logical zero voltage level. If the current flowing through the transistor Q_2 does not exceed the current flowing through the transistor Q_7, the output 612 of the first threshold detector 610 will be at a logical one voltage level. In this manner, the saturation threshold limit of the signal strength detector 154 is represented by the amount of current generated by the current source 826.

In an exemplary embodiment the second threshold detector 616 (not shown in Fig. 8) is similar to the first threshold detector 610 shown in Fig. 8. It has a counterpart to NMOS transistor Q_2 of the first threshold detector 610, with the gate of the counterpart transistor connected to the output 606 of the peak detector 604. The second threshold detector 616 also has its counterpart to the current mirror, which in the first threshold detector 610 consists of NMOS transistors Q_7 and Q_8, and reference current source 826. The counterpart to the current source 826 of the second threshold detector 616 would produce a reference current that represents the noise floor threshold limit. In the present example, the counterpart to the current source 826 generates 55 micro-amperes.

Figs. 9(a) and 9(b) illustrate an exemplary embodiment of the gain control unit 172. The gain control unit 172 provides signals that control the various variable gain stages of the main filter 106, the switching unit 130, and the shift register 144. The gain control unit 172 includes AND gates, OR gates, a positive edge triggered D-type flip flop 972, a positive edge triggered D-type flip flop 980, a positive edge triggered D-type flip flop 988, a positive edge triggered D-type flip flop 996, and an N-bit binary counter 911. The gain control unit 172 receives control

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signals at its inputs 160, 162, 166, 168, 170, which are applied to an array of AND gates, and a clock signal at the input 985, which is applied to clock inputs 970, 978, 986, and 994 of the positive edge triggered D-type flip flops 972, 980, 988, and 996, respectively, and clock input 909 of the N-bit counter 911.

When the signal received at the system input 102 changes from a relatively small signal, needing a relatively large amount of amplification to be processed effectively (i.e., without saturation of the main filter 106 or having the main filter 106 provide an output signal having greater than the minimum acceptable signal to noise ratio), to a relatively medium strength signal, needing a relatively moderate amount of amplification to be processed effectively, the gain control unit 172 changes the respective amplification factors of the variable gain stages of the main filter 106 accordingly. If the signal processing system 100 is adapted to process a relatively small input signal, logical one voltage level signals are be produced on the outputs 178 and 184 of the gain control unit 172, and logical zero voltage level signals are produced on outputs 176, 180, 182, and 186 of the gain control unit 172. This corresponds to the application of logical one voltage level signals on inputs 108 and 114 of the main filter 106 of Fig. 3, and the application of logical zero voltage level signals on inputs 110, 112 and 116 of the main filter 106 of Fig. 3. In addition, a logical zero voltage level signal is applied to input 142 of the shift register 144 of Fig. 5. If these conditions exist, and the signal received at the input 162 of the gain control unit 172 is a logical one voltage level signal, the gain control unit 172 changes the respective amplification factors of the variable gain stages of the main filter 106. The logical one voltage level signal at the input 162 of the gain control unit 172 is provided by output 158 of the strength detector 154 to indicate that the main filter 160 is approaching saturation. The gain control unit 172 begins the process of changing the respective amplification factors of variable gain stages of the main filter 106 by providing a logical one voltage level signal on the output 176, without changing any other output signals. Providing a logical one voltage level signal on the output 176 of the gain control unit 172 corresponds to applying a logical one voltage level signal to reset/enable input 142 of the shift register 144, which enables the shift register 144. Once the gain control unit 172 receives a logical one voltage level signal at the input

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168, it produces logical one voltage level signals on the outputs 176, 180, 182, and produces logical zero voltage level signals on the outputs 178, 184, 186. The gain control unit 172 receives a logical one voltage level signal at its input 168 when the comparator 136 determines that the output of the first integrator of the main filter 106 (output 118), as provided to the comparator 136 by the switching unit 130, is approximately equal to zero volts, and the comparator 136 provides a logical zero to logical one voltage level transition at its output 138 to the clock input 140 of the shift register 144 causing the shift register 144 to change from the "100" state to the "010" state. Changing the respective amplification factors of the variable gain stages of the main filter 106 while the output of the first integrator is approximately equal to zero volts avoids or minimizes the occurrence of transients in the signal produced at the output of the first integrator caused by the change in the amplification factors. Accordingly, once it receives a logical one voltage level signal at its input 168, the gain control unit 172 provides logical one voltage level signals on its outputs 176, 180 and 182 to keep the shift register enabled, and to cause switches 224, 398 and 286 (shown in Fig. 3) to close, and provides logical zero voltage level signals on its outputs 178, 184 and 186 to cause switches 232, 213, 272, 320 and 306 to open. In this manner, the amplification factor of the variable gain input stage associated with the first integrator is changed from a relatively large value to a relatively moderate value, and the amplification factor of the variable gain output stage associated with the first integrator is changed to be the reciprocal of that of the variable gain input stage associated with the first integrator. At the same time, the amplification factor of the variable gain input stage associated with the second integrator is changed from a relatively moderate value to a relatively large value, and the amplification factor of the variable gain output stage associated with the second integrator is changed to be the reciprocal of that of the variable gain input stage associated with the second integrator. And then once the gain control unit 172 receives a logical one voltage level signal at the input 170, the gain control unit 172 produces logical one voltage level signals on the outputs 180, 184, and produces logical zero voltage level signals on the outputs 176, 178, 182, 186. The gain control unit 172 receives a logical one voltage level signal at its input 170 when the comparator 136 determines that the

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output of the second integrator of the main filter 106 (output 120), as provided to the comparator 136 by the switching unit 130, is approximately equal to zero volts, and the comparator 136 provides a logical zero to logical one voltage level transition at its output 138 to the clock input 140 of the shift register 144 causing the shift register 144 to change from the "010" state to the "001" state. Changing the respective amplification factors of the variable gain stages of the main filter 106 while the output of the second integrator is approximately equal to zero volts avoids or minimizes the occurrence of transients in the signal produced at the output of the second integrator caused by the change in the amplification factors. Accordingly, once it receives a logical one voltage level signal at its input 170, the gain control unit 172 provides logical one voltage level signals on its outputs 180 and 184 to cause switches 224, 398, 272 and 306 (shown in Fig. 3) to close, and provides logical zero voltage level signals on its outputs 176, 178, 182 and 186 to cause the shift register 144 to reset and switches 232, 213, 286 and 320 to open. In this manner, the amplification factor of the variable gain input stage associated with the first integrator remains the same, and the amplification factor of the variable gain output stage associated with the first integrator remains the same. At the same time, the amplification factor of the variable gain input stage associated with the second integrator is changed from a relatively large value to a relatively moderate value, and the amplification factor of the variable gain output stage associated with the second integrator is changed to be the reciprocal of that of the variable gain input stage associated with the second integrator. Once this is completed, the gain control unit 172 has completed a desired change of the respective amplification factors of the variable gain stages of the main filter 106.

When the signal received at the system input 102 changes from a relatively medium strength signal, needing a relatively moderate amount of amplification to be processed effectively, to a relatively large signal, needing a relatively small amount of amplification to be processed effectively, the gain control unit 172 changes the respective amplification factors of the variable gain stages of the main filter 106 accordingly. If the signal processing system 100 is adapted to process a relatively medium strength input signal, logical one voltage level signals are produced on the outputs 180 and 184 of the gain control unit 172, and logical zero

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voltage level signals are produced on outputs 176, 178, 182, and 186 of the gain control unit 172. This corresponds to the application of logical one voltage level signals on inputs 110 and 114 of the main filter 106 of Fig. 3, and the application of logical zero voltage level signals on inputs 108, 112 and 116 of the main filter 106 of Fig. 3. In addition, a logical zero voltage level signal is applied to input 142 of the shift register 144 of Fig. 5. If these conditions exist, and the signal received at the input 162 of the gain control unit 172 is a logical one voltage level signal, and the signal received at the input 160 of the gain control unit 172 is a logical zero voltage level signal, the gain control unit 172 changes the respective amplification factors of the variable gain stages of the main filter 106. The logical one voltage level signal at the input 162 of the gain control unit 172 is provided by output 158 of the strength detector 154 to indicate that the main filter 160 is approaching saturation. The gain control unit 172 begins the process of changing the respective amplification factors of the variable gain stages of the main filter 106 by providing a logical one voltage level signal on the output 176, while all other outputs remain unchanged. Providing a logical one voltage level signal on the output 176 of the gain control unit 172 corresponds to applying a logical one voltage level signal to reset/enable input 142 of the shift register 144, which enables the shift register 144. Once the gain control unit 172 receives a logical one voltage level signal at the input 168, the gain control unit 172 produces logical one voltage level signals on the outputs 176, 182, and produces logical zero voltage level signals on the outputs 178, 180, 184, 186. The gain control unit 172 receives a logical one voltage level signal at its input 168 when the comparator 136 determines that the output of the first integrator of the main filter 106 (output 118), as provided to the comparator 136 by the switching unit 130, is approximately equal to zero volts, and the comparator 136 provides a logical zero to logical one voltage level transition at its output 138 to the clock input 140 of the shift register 144 causing the shift register 144 to change from the "100" state to the "010" state. Changing the respective amplification factors of the variable gain stages of the main filter 106 while the output of the first integrator is approximately equal to zero volts avoids or minimizes the occurrence of transients in the signal produced at the output of the first integrator caused by the change in the amplification factors.

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Accordingly, once it receives a logical one voltage level signal at its input 168, the gain control unit 172 provides logical one voltage level signals on its outputs 176 and 182 to keep the shift register enabled, and to cause the switch 286 (shown in Fig. 3) to close, and provides logical zero voltage level signals on its outputs 178, 180, 184 and 186 to cause switches 232, 213, 224, 398, 272, 306 and 320 to open. In this manner, the amplification factor of the variable gain input stage associated with the first integrator is changed from a relatively moderate value to a relatively small value, and the amplification factor of the variable gain output stage associated with the first integrator is changed to be the reciprocal of that of the variable gain input stage associated with the first integrator. At the same time, the amplification factor of the variable gain input stage associated with the second integrator is changed from a relatively moderate value to a relatively large value, and the amplification factor of the variable gain output stage associated with the second integrator is changed to be the reciprocal of that of the variable gain input stage associated with the second integrator. And then once the gain control unit 172 receives a logical one voltage level signal at the input 170, it produces a logical one voltage level signal on the output 184, and produces logical zero voltage level signals on the outputs 176, 178, 180, 182, 186. The gain control unit 172 receives a logical one voltage level signal at its input 170 when the comparator 136 determines that the output of the second integrator of the main filter 106 (output 120), as provided to the comparator 136 by the switching unit 130, is approximately equal to zero volts, and the comparator 136 provides a logical zero to logical one voltage level transition at its output 138 to the clock input 140 of the shift register 144 causing the shift register 144 to change from the "010" state to the "001" state. Changing the respective amplification factors of the variable gain stages of the main filter 106 while the output of the second integrator is approximately equal to zero volts avoids or minimizes the occurrence of transients in the signal produced at the output of the second integrator caused by the change in the amplification factors. Accordingly, once it receives a logical one voltage level signal at its input 170, the gain control unit 172 provides a logical one voltage level signal on its output 184 to cause switches 272 and 306 (shown in Fig. 3) to close, and provides logical zero voltage level signals on its outputs 176, 178, 180, 182 and 186

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to cause the shift register 144 to reset and switches 232, 213, 224, 398, 286 and 320 to open. In this manner, the amplification factor of the variable gain input stage associated with the first integrator remains the same, and the amplification factor of the variable gain output stage associated with the first integrator remains the same. At the same time, the amplification factor of the variable gain input stage associated with the second integrator is changed from a relatively large value to a relatively moderate value, and the amplification factor of the variable gain output stage associated with the second integrator is changed to be the reciprocal of that of the variable gain input stage associated with the second integrator. Once this is completed, the gain control unit 172 has completed the desired change of the respective amplification factors of the variable gain stages of the main filter 106.

When the signal received at the system input 102 changes from a relatively large signal, needing a relatively small amount of amplification to be processed effectively, to a relatively medium strength signal, needing a relatively moderate amount of amplification to be processed effectively, the gain control unit 172 changes the respective amplification factors of the variable gain stages of the main filter 106 accordingly. If the signal processing system 100 is adapted to process a relatively large input signal, a logical one voltage level signal is produced on the output 184 of the gain control unit 172, and logical zero voltage level signals will be produced on outputs 176, 178, 180, 182, and 186 of the gain control unit 172. This corresponds to the application of logical one voltage level signals on inputs 114 of the main filter 106 of Fig. 3, and the application of logical zero voltage level signals on inputs 108, 110, 112 and 116 of the main filter 106 of Fig. 3. In addition, a logical zero voltage level signal is applied to input 142 of the shift register 144 of Fig. 5. If these conditions exist, and the signal received at the input 162 of the gain control unit 172 is a logical zero voltage level signal, and the signal received at the input 160 of the gain control unit 172 is a logical one voltage level signal, the gain control unit 172 changes the respective amplification factors of the variable gain stages of the main filter 106. The logical one voltage level signal at the input 160 of the gain control unit 172 is provided by output 156 of the strength detector 154 to indicate that the signal produced by the main filter 160 is approaching the noise floor of the main filter 160.

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The gain control unit 172 begins the process of changing the respective amplification factors of the variable gain stages of the main filter 106 by waiting a specified period of time equal to the time it would take, given a worst case input signal, for the main filter 106 to recover from a rapid change in the input signal before increasing the respective amplification factors of the variable gain stages of the main filter 106 will not overload any of the internal nodes of the main filter 106. Once the specified period of time has elapsed, the gain control unit 172 provides a logical one voltage level signal on the output 176, while all other outputs remain unchanged. Providing a logical one voltage level signal on the output 176 of the gain control unit 172 corresponds to applying a logical one voltage level signal to reset/enable input 142 of the shift register 144, which enables the shift register 144. Once the gain control unit 172 receives a logical one voltage level signal at the input 168, the gain control unit 172 produces logical one voltage level signals on the outputs 176, 180, 186, and produces logical zero voltage level signals on the outputs 178, 182, 184. The gain control unit 172 receives a logical one voltage level signal at its input 168 when the comparator 136 determines that the output of the first integrator of the main filter 106 (output 118), as provided to the comparator 136 by the switching unit 130, is approximately equal to zero volts, and the comparator 136 provides a logical zero to logical one voltage level transition at its output 138 to the clock input 140 of the shift register 144 causing the shift register 144 to change from the "100" state to the "010" state. Changing the respective amplification factors of the variable gain stages of the main filter 106 while the output of the first integrator is approximately equal to zero volts avoids or minimizes the occurrence of transients in the signal produced at the output of the first integrator caused by the change in the amplification factors. Accordingly, once it receives a logical one voltage level signal at its input 168, the gain control unit 172 provides logical one voltage level signals on its outputs 176, 180 and 186 to keep the shift register enabled, and to cause switches 224, 398 and 320 (shown in Fig. 3) to close, and provides logical zero voltage level signals on its outputs 178, 182 and 184 to cause switches 232, 213, 286, 272 and 306 to open. In this manner, the amplification factor of the variable gain input stage associated with the first integrator is changed from a relatively small value to a relatively moderate

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value, and the amplification factor of the variable gain output stage associated with the first integrator is changed to be the reciprocal of that of the variable gain input stage associated with the first integrator. At the same time, the amplification factor of the variable gain input stage associated with the second integrator is changed from a relatively moderate value to a relatively small value, and the amplification factor of the variable gain output stage associated with the second integrator is changed to be the reciprocal of that of the variable gain input stage associated with the second integrator. And then once the gain control unit 172 receives a logical one voltage level signal at the input 170, it produces logical one voltage level signals on the outputs 180, 184, and produces logical zero voltage level signals on the outputs 176, 178, 182, 186. The gain control unit 172 receives a logical one voltage level signal at its input 170 when the comparator 136 determines that the output of the second integrator of the main filter 106 (output 120), as provided to the comparator 136 by the switching unit 130, is approximately equal to zero volts, and the comparator 136 provides a logical zero to logical one voltage level transition at its output 138 to the clock input 140 of the shift register 144 causing the shift register 144 to change from the "010" state to the "001" state. Changing the respective amplification factors of the variable gain stages of the main filter 106 while the output of the second integrator is approximately equal to zero volts avoids or minimizes the occurrence of transients in the signal produced at the output of the second integrator caused by the change in the amplification factors. Accordingly, once it receives a logical one voltage level signal at its input 170, the gain control unit 172 provides logical one voltage level signals on its outputs 180 and 184 to cause switches 224, 398, 272 and 306 (shown in Fig. 3) to close, and provides logical zero voltage level signals on its outputs 176, 178, 182 and 186 to cause the shift register 144 to reset and switches 232, 213, 286 and 320 to open. In this manner, the amplification factor of the variable gain input stage associated with the first integrator remains the same, and the amplification factor of the variable gain output stage associated with the first integrator remains the same. At the same time, the amplification factor of the variable gain input stage associated with the second integrator is changed from a relatively small value to a relatively moderate value, and the amplification factor of the variable gain output

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stage associated with the second integrator is changed to be the reciprocal of that of the variable gain input stage associated with the second integrator. Once this is completed, the gain control unit 172 has completed the desired change of the respective amplification factors of the variable gain stages of the main filter 106.

When the signal received at the system input 102 changes from a relatively medium strength signal, needing a relatively moderate amount of amplification to be processed effectively, to a relatively small signal, needing a relatively large amount of amplification to be processed effectively, the gain control unit 172 changes the respective amplification factors of the variable gain stages of the main filter 106 accordingly. If the signal processing system 100 is adapted to process a relatively medium strength input signal, logical one voltage level signals are produced on the outputs 180, 184 of the gain control unit 172, and logical zero voltage level signals are produced on outputs 176, 178, 182, and 186 of the gain control unit 172. This corresponds to the application of logical one voltage level signals on inputs 110 and 114 of the main filter 106 of Fig. 3, and the application of logical zero voltage level signals on inputs 108, 112 and 116 of the main filter 106 of Fig. 3. In addition, a logical zero voltage level signal is applied to input 142 of the shift register 144 of Fig. 5. If these conditions exist, and the signal received at the input 162 of the gain control unit 172 is a logical zero voltage level signal, and the signal received at the input 160 of the gain control unit 172 is a logical one voltage level signal, the gain control unit 172 changes the respective amplification factors of the variable gain stages of the main filter 106. The logical one voltage level signal at the input 160 of the gain control unit 172 is provided by output 156 of the strength detector 154 to indicate that the signal produced by the main filter 160 is approaching the noise floor of the main filter 160. The gain control unit 172 begins the process of changing the respective amplification factors of the variable gain stages of the main filter 106 by waiting a specified period of time equal to the time it would take, given a worst case rapidly changing input signal, for the main filter 106 to recover from a rapid change in the input signal before increasing the respective amplification factors of the variable gain stages of the main filter 106 will not overload any of the internal nodes of the main filter 106. Once the specified period of time has elapsed, the gain

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control unit 172 provides a logical one voltage level signal on the output 176, while all other outputs remain unchanged. Providing a logical one voltage level signal on the output 176 of the gain control unit 172 corresponds to applying a logical one voltage level signal to reset/enable input 142 of the shift register 144, which enables the shift register 144. Once the gain control unit 172 receives a logical one voltage level signal at the input 168, it produces logical one voltage level signals on the outputs 176, 178, 186, and produces logical zero voltage level signals on the outputs 180, 182, 184. The gain control unit 172 receives a logical one voltage level signal at its input 168 when the comparator 136 determines that the output of the first integrator of the main filter 106 (output 118), as provided to the comparator 136 by the switching unit 130, is approximately equal to zero volts, and the comparator 136 provides a logical zero to logical one voltage level transition at its output 138 to the clock input 140 of the shift register 144 causing the shift register 144 to change from the "100" state to the "010" state. Changing the respective amplification factors of the variable gain stages of the main filter 106 while the output of the first integrator is approximately equal to zero volts avoids or minimizes the occurrence of transients in the signal produced at the output of the first integrator caused by the change in the amplification factors. Accordingly, once it receives a logical one voltage level signal at its input 168, the gain control unit 172 provides logical one voltage level signals on its outputs 176, 178 and 186 to keep the shift register enabled, and to cause switches 232, 213 and 320 (shown in Fig. 3) to close, and provides logical zero voltage level signals on its outputs 180, 182 and 184 to cause switches 224, 398, 286, 272 and 306 to open. In this manner, the amplification factor of the variable gain input stage associated with the first integrator is changed from a relatively moderate value to a relatively large value, and the amplification factor of the variable gain output stage associated with the first integrator is changed to be the reciprocal of that of the variable gain input stage associated with the first integrator. At the same time, the amplification factor of the variable gain input stage associated with the second integrator is changed from a relatively moderate value to a relatively small value, and the amplification factor of the variable gain output stage associated with the second integrator is changed to be the reciprocal of that of the variable gain input stage

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associated with the second integrator. And then once the gain control unit 172 receives a logical one voltage level signal at the input 170, the gain control unit 172 produces logical one voltage level signals on the output 178, 184, and produces logical zero voltage level signals on the outputs 176, 180, 182, 186. The gain control unit 172 receives a logical one voltage level signal at its input 170 when the comparator 136 determines that the output of the second integrator of the main filter 106 (output 120), as provided to the comparator 136 by the switching unit 130, is approximately equal to zero volts, and the comparator 136 provides a logical zero to logical one voltage level transition at its output 138 to the clock input 140 of the shift register 144 causing the shift register 144 to change from the "010" state to the "001" state. Changing the respective amplification factors of the variable gain stages of the main filter 106 while the output of the second integrator is approximately equal to zero volts avoids or minimizes the occurrence of transients in the signal produced at the output of the second integrator caused by the change in the amplification factors. Accordingly, once it receives a logical one voltage level signal at its input 170, the gain control unit 172 provides logical one voltage level signals on its outputs 178 and 184 to cause switches 232, 213, 272 and 306 (shown in Fig. 3) to close, and provides logical zero voltage level signals on its outputs 176, 180, 182 and 186 to cause the shift register 144 to reset and switches 224, 398, 286 and 320 to open. In this manner, the amplification factor of the variable gain input stage associated with the first integrator remains the same, and the amplification factor of the variable gain output stage associated with the first integrator remains the same. At the same time, the amplification factor of the variable gain input stage associated with the second integrator is changed from a relatively small value to a relatively moderate value, and the amplification factor of the variable gain output stage associated with the second integrator is changed to be the reciprocal of that of the variable gain input stage associated with the second integrator. Once this is completed, the gain control unit 172 has completed the desired change of the respective amplification factors of the variable gain stages of the main filter 106.

The N-bit counter 911 receives a signal at an enable/reset input 907, and a signal at a clock input 909, and provides an output at a counter overflow output

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913. If the signal received at the input 907 is a logical one voltage level signal, the N-bit counter 911 increments on the positive edge (i.e., a transition from a logical zero voltage level to a logical one voltage level) of each clock cycle, and the signal produced at the counter overflow output 913 is a logical zero, until the N-bit counter 911 reaches a specified maximum value. On the clock cycle after the N-bit counter 911 reaches its specified maximum value, the signal produced at the counter overflow output 913 is a logical one voltage level signal. If the signal received at the input 907 is a logical zero voltage level signal, the N-bit counter 911 is reset to a predetermined state, and the signal produced at the counter overflow output 913 is a logical zero voltage level signal. In a certain embodiment, the predetermined state is selected such that once the signal received at the enable/reset input 907 changes from a logical zero voltage level signal to a logical one voltage level signal, the counter overflow output 913 will not change to a logical one voltage level signal until a time equal to the time it would take, given a worst case rapidly changing input signal, for the main filter 106 to recover from a rapid change in the input signal before increasing the respective amplification factors of the variable gain stages of the main filter 106 will not overload any of the internal nodes of the main filter 106.

A five input AND gate 902 receives the inverse of a signal from a data output 974 of the positive edge triggered D-type flip flop 972, a signal from a data output 982 of the positive edge triggered D-type flip flop 980, a signal from a data output 990 of the positive edge triggered D-type flip flop 988, a signal from a data output 998 of the positive edge triggered D-type flip flop 996, and a signal received from the counter overflow output 913. The output of the AND gate 902 is connected to one input of a two input OR gate 906. A five input AND gate 904 receives a signal from the data output 974 of the positive edge triggered D-type flip flop 972, the inverse of a signal from the data output 982 of the positive edge triggered D-type flip flop 980, the inverse of a signal from the data output 990 of the positive edge triggered D-type flip flop 988, the inverse of a signal from the data output 998 of the positive edge triggered D-type flip flop 996, and the inverse of a signal received from the counter overflow output 913. The output of the AND gate 904 is connected to the

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other input of a two input OR gate 906. The output of the two input OR gate 906 is connected to the data input 968 of the positive edge triggered D-type flip flop 972.

A six input AND gate 908 receives the inverse of a signal from the data output 974 of the positive edge triggered D-type flip flop 972, the inverse of a signal from the data output 982 of the positive edge triggered D-type flip flop 980, a signal from the data output 990 of the positive edge triggered D-type flip flop 988, the inverse of a signal from the data output 998 of the positive edge triggered D-type flip flop 996, the inverse of a signal received by the input 162, and a signal received by the input 160. The AND gate 908 provides its output to a first input of a nine input OR gate 926. A five input AND gate 910 receives the inverse of a signal from the data output 974 of the positive edge triggered D-type flip flop 972, the inverse of a signal from the data output 982 of the positive edge triggered D-type flip flop 980, a signal from the data output 990 of the positive edge triggered D-type flip flop 988, a signal from the data output 998 of the positive edge triggered D-type flip flop 996, and a signal received by the input 170. The output of the AND gate 908 is provided to a second input of the nine input OR gate 926. A five input AND gate 912 receives the inverse of a signal from the data output 974 of the positive edge triggered D-type flip flop 972, a signal from the data output 982 of the positive edge triggered D-type flip flop 980, the inverse of a signal from the data output 990 of the positive edge triggered D-type flip flop 988, the inverse of a signal from the data output 998 of the positive edge triggered D-type flip flop 996, and the inverse of a signal received by the input 160. The output of the AND gate 914 is provided to a fourth input of the nine input OR gate 926. A five input AND gate 914 receives the inverse of a signal from the data output 974 of the positive edge triggered D-type flip flop 972, a signal from the data output 982 of the positive edge triggered D-type flip flop 980, the inverse of a signal from the data output 990 of the positive edge triggered D-type flip flop 988, the inverse of a signal from the data output 998 of the positive edge triggered D-type flip flop 996, and a signal received by the input 160. The output of the AND gate 914 is provided to a fourth input of the nine input OR gate 926. A five input AND gate 916 receives the inverse of a signal from the data output 974 of the positive edge triggered D-type flip flop 972, a signal from the data output 982 of the

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positive edge triggered D-type flip flop 980, the inverse of a signal from the data output 990 of the positive edge triggered D-type flip flop 988, a signal from the data output 998 of the positive edge triggered D-type flip flop 996, and the inverse of a signal received from the overflow output 913 of the counter 911. The output of the AND gate 916 is provided to a fifth input of the nine input OR gate 926. A five input AND gate 918 receives the inverse of a signal from the data output 974 of the positive edge triggered D-type flip flop 972, a signal from the data output 982 of the positive edge triggered D-type flip flop 980, the inverse of a signal from the data output 990 of the positive edge triggered D-type flip flop 988, a signal from the data output 998 of the positive edge triggered D-type flip flop 996, and a signal received from the overflow output 913 of the counter 911. The AND gate 918 is provided to a sixth input of the nine input OR gate 926. A five input AND gate 920 receives the inverse of a signal from the data output 974 of the positive edge triggered D-type flip flop 972, a signal from the data output 982 of the positive edge triggered D-type flip flop 980, a signal from the data output 990 of the positive edge triggered D-type flip flop 988, the inverse of a signal from the data output 998 of the positive edge triggered D-type flip flop 996, and the inverse of a signal received by the input 170. The output of the AND gate 920 is provided to a seventh input of the nine input OR gate 926. A five input AND gate 922 receives the inverse of a signal from the data output 974 of the positive edge triggered D-type flip flop 972, a signal from the data output 982 of the positive edge triggered D-type flip flop 980, a signal from the data output 990 of the positive edge triggered D-type flip flop 988, the inverse of a signal from the data output 998 of the positive edge triggered D-type flip flop 996, and a signal received by the input 170. The output of the AND gate 922 is provided to an eighth input of the nine input OR gate 926. A five input AND gate 924 receives the inverse of a signal from the data output 974 of the positive edge triggered D-type flip flop 972, a signal from the data output 982 of the positive edge triggered D-type flip flop 980, a signal from the data output 990 of the positive edge triggered D-type flip flop 988, a signal from the data output 998 of the positive edge triggered D-type flip flop 996, and the inverse of a signal received from the overflow output 913 of the counter 911. The output of AND gate 924 is provided to the ninth input of the nine input OR gate

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926. The output of the nine input OR gate 926 is provided to a data input 976 of the positive edge triggered D-type flip flop 980.

A five input AND gate 928 receives the inverse of a signal from the data output 974 of the positive edge triggered D-type flip flop 972, the inverse of a signal from the data output 982 of the positive edge triggered D-type flip flop 980, the inverse of a signal from the data output 990 of the positive edge triggered D-type flip flop 988, a signal from the data output 998 of the positive edge triggered D-type flip flop 996, and a signal received by the input 170. The output of the AND gate 928 is provided to a first input of a nine input OR gate 946. A six input AND gate 930 receives the inverse of a signal from the data output 974 of the positive edge triggered D-type flip flop 972, the inverse of a signal from the data output 982 of the positive edge triggered D-type flip flop 980, a signal from the data output 990 of the positive edge triggered D-type flip flop 988, the inverse of a signal from the data output 998 of the positive edge triggered D-type flip flop 996, the inverse of a signal received by the input 160, and the inverse of a signal received by the input 162. The output of the AND gate 930 is provided to a second input of the nine input OR gate 946. A six input AND gate 932 receives the inverse of a signal from the data output 974 of the positive edge triggered D-type flip flop 972, the inverse of a signal from the data output 982 of the positive edge triggered D-type flip flop 980, a signal from the data output 990 of the positive edge triggered D-type flip flop 988, the inverse of a signal from the data output 998 of the positive edge triggered D-type flip flop 996, a signal received by the input 160, and the inverse of a signal received by the input 162. The output of the AND gate 932 is provided to a third input of the nine input OR gate 946. A six input AND gate 934 receives the inverse of a signal from the data output 974 of the positive edge triggered D-type flip flop 972, the inverse of a signal from the data output 982 of the positive edge triggered D-type flip flop 980, a signal from the data output 990 of the positive edge triggered D-type flip flop 988, the inverse of a signal from the data output 998 of the positive edge triggered D-type flip flop 996, a signal received by the input 160, and the inverse of a signal received by the input 162. The output of the AND gate 934 is provided to a fourth input of the nine input OR gate 946. A five input AND gate 936 receives the inverse of a signal from the data output

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974 of the positive edge triggered D-type flip flop 972, the inverse of a signal from the data output 982 of the positive edge triggered D-type flip flop 980, a signal from the data output 990 of the positive edge triggered D-type flip flop 988, a signal from the data output 998 of the positive edge triggered D-type flip flop 996, and the inverse of a signal received by the input 170. The output of the AND gate 936 is provided to a fifth input of the nine input OR gate 946. A five input AND gate 938 receives the inverse of a signal from the data output 974 of the positive edge triggered D-type flip flop 972, a signal from the data output 982 of the positive edge triggered D-type flip flop 980, the inverse of a signal from the data output 990 of the positive edge triggered D-type flip flop 988, a signal from the data output 998 of the positive edge triggered D-type flip flop 996, and a signal from the overflow output 913 of the counter 911. The output of the AND gate 938 is provided to a sixth input of the nine input OR gate 946. A five input AND gate 940 receives the inverse of a signal from the data output 974 of the positive edge triggered D-type flip flop 972, a signal from the data output 982 of the positive edge triggered D-type flip flop 980, a signal from the data output 990 of the positive edge triggered D-type flip flop 988, the inverse of a signal from the data output 998 of the positive edge triggered D-type flip flop 996, and the inverse of a signal received by the input 170. The output of the AND gate 940 is provided to a seventh input of the nine input OR gate 946. A five input AND gate 942 receives the inverse of a signal from the data output 974 of the positive edge triggered D-type flip flop 972, a signal from the data output 982 of the positive edge triggered D-type flip flop 980, a signal from the data output 990 of the positive edge triggered D-type flip flop 988, the inverse of a signal from the data output 998 of the positive edge triggered D-type flip flop 996, and a signal received by the input 170. The output of the AND gate 942 is provided to an eighth input of the nine input OR gate 946. A five input AND gate 944 receives the inverse of a signal from the data output 974 of the positive edge triggered D-type flip flop 972, a signal from the data output 982 of the positive edge triggered D-type flip flop 980, a signal from the data output 990 of the positive edge triggered D-type flip flop 988, a signal from the data output 998 of the positive edge triggered D-type flip flop 996, and the inverse of a signal from the overflow output 913 of the counter 911. The output of the AND gate

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944 is provided to a ninth input of the nine input OR gate 946. The output of the nine input OR gate 946 is provided to a data input 984 of the positive edge triggered D-type flip flop 988.

A five input AND gate 948 receives the inverse of a signal from the data output 974 of the positive edge triggered D-type flip flop 972, the inverse of a signal from the data output 982 of the positive edge triggered D-type flip flop 980, the inverse of a signal from the data output 990 of the positive edge triggered D-type flip flop 988, the inverse of a signal from the data output 998 of the positive edge triggered D-type flip flop 996, and a signal received by the input 162. The output of the AND gate 948 is provided to a first input of a nine input OR gate 966. A five input AND gate 950 receives the inverse of a signal from the data output 974 of the positive edge triggered D-type flip flop 972, the inverse of a signal from the data output 982 of the positive edge triggered D-type flip flop 980, the inverse of a signal from the data output 990 of the positive edge triggered D-type flip flop 988, a signal from the data output 998 of the positive edge triggered D-type flip flop 996, and the inverse of a signal received by the input 170. The output of the AND gate 950 is provided to a second input of the nine input OR gate 966. A six input AND gate 952 receives the inverse of a signal from the data output 974 of the positive edge triggered D-type flip flop 972, the inverse of a signal from the data output 982 of the positive edge triggered D-type flip flop 980, a signal from the data output 990 of the positive edge triggered D-type flip flop 988, the inverse of a signal from the data output 998 of the positive edge triggered D-type flip flop 996, a signal received by the input 162, and the inverse of a signal received by the input 160. The output of the AND gate 952 is provided to a third input of the nine input OR gate 966. A six input AND gate 954 receives the inverse of a signal from the data output 974 of the positive edge triggered D-type flip flop 972, the inverse of a signal from the data output 982 of the positive edge triggered D-type flip flop 980, a signal from the data output 990 of the positive edge triggered D-type flip flop 988, the inverse of a signal from the data output 998 of the positive edge triggered D-type flip flop 996, the inverse of a signal received by the input 162, and a signal received by the input 160. The output of the AND gate 954 is provided to a fourth input of the nine input OR gate 966. A five

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input AND gate 956 receives the inverse of a signal from the data output 974 of the positive edge triggered D-type flip flop 972, the inverse of a signal from the data output 982 of the positive edge triggered D-type flip flop 980, a signal from the data output 990 of the positive edge triggered D-type flip flop 988, a signal from the data output 998 of the positive edge triggered D-type flip flop 996, and the inverse of a signal received by the input 170. The output of the AND gate 956 is provided to a fifth input of the nine input OR gate 966. A five input AND gate 958 receives the inverse of a signal from the data output 974 of the positive edge triggered D-type flip flop 972, a signal from the data output 982 of the positive edge triggered D-type flip flop 980, the inverse of a signal from the data output 990 of the positive edge triggered D-type flip flop 988, the inverse of a signal from the data output 998 of the positive edge triggered D-type flip flop 996, and a signal received by the input 160. The output of the AND gate 958 is provided to a sixth input of the nine input OR gate 966. A five input AND gate 960 receives the inverse of a signal from the data output 974 of the positive edge triggered D-type flip flop 972, a signal from the data output 982 of the positive edge triggered D-type flip flop 980, the inverse of a signal from the data output 990 of the positive edge triggered D-type flip flop 988, a signal from the data output 998 of the positive edge triggered D-type flip flop 996, and the inverse of a signal received from the overflow output 913 of the counter 911. The output of the AND gate 960 is provided to a seventh input of the nine input OR gate 966. A five input AND gate 962 receives the inverse of a signal from the data output 974 of the positive edge triggered D-type flip flop 972, a signal from the data output 982 of the positive edge triggered D-type flip flop 980, a signal from the data output 990 of the positive edge triggered D-type flip flop 988, the inverse of a signal from the data output 998 of the positive edge triggered D-type flip flop 996, and a signal received by the input 170. The output of the AND gate 962 if provided to an eighth input of the nine input OR gate 966. A five input AND gate 964 receives the inverse of a signal from the data output 974 of the positive edge triggered D-type flip flop 972, a signal from the data output 982 of the positive edge triggered D-type flip flop 980, a signal from the data output 990 of the positive edge triggered D-type flip flop 988, a signal from the data output 998 of the positive edge triggered D-type flip flop 996,

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and the inverse of a signal received from the overflow output 913 of the counter 911. The output of the AND gate 964 is provided to a ninth input of the nine input OR gate 966. The output of the nine input OR gate 966 is provided to a data input 992 of the positive edge triggered D-type flip flop 996.

The first D-type flip-flop 972 holds the most significant bit of the current state of the gain control unit 172 until the next positive edge of the clock signal is received at the clock input 985 of the gain control unit 172, at which time the most significant bit of the current state is provided at the data output 974 of the first D-type flip-flop 972. The output 974 is coupled to a terminal 915. The second D-type flip-flop 980 holds the second most significant bit of the current state of the gain control unit 172 until the next positive edge of the clock signal is received at the clock input 985 of the gain control unit 172, at which time the second most significant bit of the current state is provided at the data output 982 of the second D-type flip-flop 980. The output 982 is coupled to a terminal 917. The third D-type flip-flop 988 holds the third most significant bit of the current state of the gain control unit 172 until the next positive edge of the clock signal is received at the clock input 985 of the gain control unit 172, at which time the third most significant bit of the current state is provided at the data output 990 of the third D-type flip-flop 988. The output 990 is coupled to a terminal 919. The fourth D-type flip-flop 996 holds the least significant bit of the current state of the gain control unit 172 until the next positive edge of the clock signal is received at the clock input 985 of the gain control unit 172, at which time the least significant bit of the current state is provided at the data output 998 of the fourth D-type flip-flop 996. The output 998 is coupled to a terminal 921.

A four input AND gate 901 receives the inverse of a signal from the data output 974 of the positive edge triggered D-type flip flop 972, a signal from the data output 982 of the positive edge triggered D-type flip flop 980, the inverse of a signal from the data output 990 of the positive edge triggered D-type flip flop 988, and a signal from the data output 998 of the positive edge triggered D-type flip flop 996. The output of the AND gate 901 is provided to one input of a two input OR gate 905. A four input AND gate 903 receives the inverse of a signal from the data output 974 of the positive edge triggered D-type flip flop 972, a signal from the data output

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982 of the positive edge triggered D-type flip flop 980, a signal from the data output 990 of the positive edge triggered D-type flip flop 988, and a signal from the data output 998 of the positive edge triggered D-type flip flop 996. The output of the AND gate 903 is provided to the other input of the two input OR gate 905. The output of the two input OR gate 905 is provided to the enable/reset input 907 of the N-bit counter 911.

A four input AND gate 923 receives the inverse of a signal received by the input 915, the inverse of a signal received by the input 917, the inverse of a signal received by the input 919, and the inverse of a signal received by the input 921. The output of the AND gate 923 is provided to a first input of a four input OR gate 931. A seven input AND gate 925 receives the inverse of a signal received by the input 915, the inverse of a signal received by the input 917, the inverse of a signal received by the input 919, a signal received by the input 921, a signal received by the input 166, the inverse of a signal received by the input 168, and the inverse of a signal received by the input 170. The output of the AND gate 925 is provided to a second input of the four input OR gate 931. A seven input AND gate 927 receives a signal received by the input 915, the inverse of a signal received by the input 917, the inverse of a signal received by the input 919, the inverse of a signal received by the input 921, the inverse of a signal received by the input 166, a signal received by the input 168, and the inverse of a signal received by the input 170. The output of the AND gate 927 is provided to a third input of the four input OR gate 931. A seven input AND gate 929 receives a signal received by the input 915, the inverse of a signal received by the input 917, the inverse of a signal received by the input 919, the inverse of a signal received by the input 921, the inverse of a signal received by the input 166, the inverse of a signal received by the input 168, and a signal received by the input 170. The output of the AND gate 926 is provided to a fourth input of the four input OR gate 931. The output of the four input OR gate 931 is provided to the output 178.

A four input AND gate 933 receives the inverse of a signal received by the input 915, the inverse of a signal received by the input 917, a signal received by the input 919, and the inverse of a signal received by the input 921. The output of the AND gate 933 is provided to a first input of an eight input OR gate 949. A four input

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AND gate 935 receives the inverse of a signal received by the input 915, a signal received by the input 917, a signal received by the input 919, and a signal received by the input 921. The output of the AND gate 935 is provided to a second input of the eight input OR gate 949. A seven input AND gate 937 receives the inverse of a signal received by the input 915, the inverse of a signal received by the input 917, a signal received by the input 919, a signal received by the input 921, a signal received by the input 166, the inverse of a signal received by the input 168, and the inverse of a signal received by the input 170. The output of the AND gate 937 is provided to a third input of the eight input OR gate 949. A seven input AND gate 939 receives a signal received by the input 915, the inverse of a signal received by the input 917, the inverse of a signal received by the input 919, the inverse of a signal received by the input 921, a signal received by the input 166, the inverse of a signal received by the input 168, and the inverse of a signal received by the input 170. The output of the AND gate 939 is provided to a fourth input of the eight input OR gate 949. A seven input AND gate 941 receives the inverse of a signal received by the input 915, the inverse of a signal received by the input 917, the inverse of a signal received by the input 919, a signal received by the input 921, the inverse of a signal received by the input 166, a signal received by the input 168, and the inverse of a signal received by the input 170. The output of the AND gate 941 is provided to a fifth input of the eight input OR gate 949. A seven input AND gate 943 receives the inverse of a signal received by the input 915, the inverse of a signal received by the input 917, the inverse of a signal received by the input 919, a signal received by the input 921, the inverse of a signal received by the input 166, the inverse of a signal received by the input 168, and a signal received by the input 170. The output of the AND gate 943 is provided to a sixth input of the eight input OR gate 949. A seven input AND gate 945 receives the inverse of a signal received by the input 915, a signal received by the input 917, a signal received by the input 919, the inverse of a signal received by the input 921, the inverse of a signal received by the input 166, a signal received by the input 168, and the inverse of a signal received by the input 170. The output of the AND gate 945 is provided to a seventh input of the eight input OR gate 949. A seven input AND gate 947 receives the inverse of a signal received by the input 915, a

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signal received by the input 917, a signal received by the input 919, the inverse of a signal received by the input 921, the inverse of a signal received by the input 166, the inverse of a signal received by the input 168, and a signal received by the input 170. The output of the AND gate 947 is provided to an eighth input of the eight input OR gate 949. The output of the eight input OR gate 949 is provided to the output 180 of the gain control unit 172.

A seven input AND gate 951 receives the inverse of a signal received by the input 915, the inverse of a signal received by the input 917, the inverse of a signal received by the input 919, a signal received by the input 921, the inverse of a signal received by the input 166, a signal received by the input 168, and the inverse of a signal received by the input 170. The output of the AND gate 951 is provided to one input of a two input OR gate 955. A seven input AND gate 953 receives the inverse of a signal received by the input 915, the inverse of a signal received by the input 917, a signal received by the input 919, a signal received by the input 921, the inverse of a signal received by the input 166, a signal received by the input 168, and the inverse of a signal received by the input 170. The output of the AND gate 953 is provided to the other input of the two input OR gate 955. The output of the two input OR gate 955 is provided to the output 182 of the gain control unit 172.

A seven input AND gate 957 receives the inverse of a signal received by the input 915, the inverse of a signal received by the input 917, the inverse of a signal received by the input 919, a signal received by the input 921, the inverse of a signal received by the input 166, a signal received by the input 168, and the inverse of a signal received by the input 170. The output of the AND gate 957 is provided to a first input of a four input NOR gate 965. A seven input AND gate 959 receives the inverse of a signal received by the input 915, the inverse of a signal received by the input 917, a signal received by the input 919, a signal received by the input 921, the inverse of a signal received by the input 166, a signal received by the input 168, and the inverse of a signal received by the input 170. The output of the AND gate 959 is provided to a second input of the four input NOR gate 965. A seven input AND gate 961 receives the inverse of a signal received by the input 915, a signal received by the input 917, a signal received by the input 919, the inverse of a signal received by the

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input 921, the inverse of a signal received by the input 166, a signal received by the input 168, and the inverse of a signal received by the input 170. The output of the AND gate 961 is provided to a third input of the four input NOR gate 965. A seven input AND gate 963 receives a signal received by the input 915, the inverse of a signal received by the input 917, the inverse of a signal received by the input 919, the inverse of a signal received by the input 921, the inverse of a signal received by the input 166, a signal received by the input 168, and the inverse of a signal received by the input 170. The output of the AND gate 963 is provided to a fourth input of the four input NOR gate 965. The output of the four input NOR gate 965 is provided to the output 184 of the gain control unit 172.

A seven input AND gate 967 receives a signal received by the input 915, the inverse of a signal received by the input 917, the inverse of a signal received by the input 919, the inverse of a signal received by the input 921, the inverse of a signal received by the input 166, a signal received by the input 168, and the inverse of a signal received by the input 170. The output of the AND gate 967 is provided to one input of a two input OR gate 971. A seven input AND gate 969 receives the inverse of a signal received by the input 915, a signal received by the input 917, a signal received by the input 919, the inverse of a signal received by the input 921, the inverse of a signal received by the input 166, a signal received by the input 168, and the inverse of a signal received by the input 170. The output of the AND gate 969 is provided to the other input of the two input OR gate 971. The output of the two input OR gate 971 is provided to the output 186 of the gain control unit 172.

A four input AND gate 973 receives the inverse of a signal received by the input 915, the inverse of a signal received by the input 917, the inverse of a signal received by the input 919, and the inverse of a signal received by the input 921. The output of the AND gate 973 is provided to a first input of a five input OR gate 983. A four input AND gate 975 receives the inverse of a signal received by the input 915, the inverse of a signal received by the input 917, a signal received by the input 919, and the inverse of a signal received by the input 921. The output of the AND gate 975 is provided to a second input of the five input OR gate 983. A four input AND gate 977 receives the inverse of a signal received by the input 915, a signal received

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by the input 917, the inverse of a signal received by the input 919, and the inverse of a signal received by the input 921. The output of the AND gate 977 is provided to a third input of the five input OR gate 983. A four input AND gate 979 receives the inverse of a signal received by the input 915, a signal received by the input 917, the inverse of a signal received by the input 919, and a signal received by the input 921. The output of the AND gate 979 is provided to a fourth input of the five input OR gate 983. A four input AND gate 981 receives the inverse of a signal received by the input 915, a signal received by the input 917, a signal received by the input 919, and a signal received by the input 921. The output of the AND gate 981 is provided to a fifth input of the five input OR gate 983. The output of the five input OR gate 983 is provided to the output 176 of the gain control unit 172.

Fig. 11 illustrates an exemplary embodiment of the transconductor 742 in the peak detector 604 depicted in Fig. 7 in greater detail. The transconductor 742 includes an NMOS transistor Q_1, an NMOS transistor Q_2, a PMOS transistor Q_3, a PMOS transistor Q_4, an NMOS transistor Q_5, an NMOS transistor Q_6, and a current source 1124.

A signal received by the positive input 744 of the transconductor 742 is applied to the gate 1105 of the NMOS transistor Q_1. The NMOS transistor Q_1 allows current to flow from its source 1107 to its drain 1106, or vice versa, depending on the signal at the gate 1105 and the relative voltages at its source 1107 and at its drain 1106. The drain 1106 of the NMOS transistor Q_1 is connected to the drain 1113 and the gate 1111 of the PMOS transistor Q_3, and the gate 1114 of the PMOS transistor Q_4. The source 1107 of the NMOS transistor Q_1 is connected to the drain 1118 of the NMOS transistor Q_5 and the source 1110 of the NMOS transistor Q_2.

A signal received by the negative input 746 of the transconductor 742 is applied to the gate 1108 of the NMOS transistor Q_2. The drain 1109 of the NMOS transistor Q_2 is connected to the drain 1116 of the PMOS transistor Q_4 and the output 748 of the transconductor 742. The source 1110 of the NMOS transistor Q_2 is connected to the drain 1118 of the NMOS transistor Q_5, and the source 1107 of the NMOS transistor Q_1.

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The drain 1113 of the PMOS transistor Q_3 is connected to the drain 1106 of the NMOS transistor Q_1, the gate 1111 of the PMOS transistor Q_3, and the gate 1114 of the PMOS transistor Q_4. The source 1112 of the PMOS transistor Q_3 is connected to supply voltage V_{dd}.

The source 1115 of the PMOS transistor Q_4 is connected to supply voltage V_{dd}.

The drain 1118 of the NMOS transistor Q_5 is connected to the source 1107 of the NMOS transistor Q_1 and the source 1110 of the NMOS transistor Q_2. The source 1119 of the NMOS transistor Q_5 is connected to supply voltage V_{ss}. The gate 1117 of the NMOS transistor Q_5 is connected to the gate 1120 and the drain 1121 of the NMOS transistor Q_6, and the negative terminal 1125 of the current source 1124.

The source 1122 of the NMOS transistor Q_6 is connected to supply voltage V_{ss}.

The current source 1124 produces a bias current I_{bias} for the transconductor 332. The bias current I_{bias} produced by the current source 1124 is adjusted to give a stable center frequency in the presence of fabrication tolerances and temperature variations. The bias current I_{bias} can be any value, for example 100 micro-amperes, and the transistors Q_1, Q_2, Q_3, Q_4, Q_5, Q_6 of the transconductor 742 are scaled to yield the desired transconductances. The transconductance for the transconductors is calculated using the equation:

$$G_m = I_{tail} / (V_{GS} - V_T), \quad (3)$$

where I_{tail} is the current passing through the transistor Q_5, V_T is the threshold voltage of transistors Q_5 and Q_6, and V_{GS} is the gate-source voltage of the transistors Q_5, Q_6. The linear range of the transconductor is related to the quantity $V_{GS} - V_T$. Once the bias current I_{bias} has been set, the transistors Q_5, Q_6 are scaled such that, the following equation is satisfied:

$$(W_{Q5} / L_{Q5}) / (W_{Q6} / L_{Q6}) = I_{tail} / I_{bias}, \quad (4)$$

where W_{Q5} and L_{Q5} are the width and length of the channel of NMOS transistor Q_5, respectively, and W_{Q6} and L_{Q6} are the width and length of the channel of NMOS transistor Q_6, respectively. The positive terminal of the current source 1124 is connected to supply voltage V_{dd}. The preferred form of the current source 1124 is a

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resistor connected to the between the supply voltage V_{dd} and the drain 1121 and the gate 1120 of the NMOS transistor Q_6.

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CLAIMS

1. An active filter system comprising:

a system input for receiving a system input signal;

a system output for providing a system output signal;

a main filter having at least one successive filter stage having an input and an output, including a first filter stage, each filter stage having an associated input amplification stage including a signal input, a signal output coupled to the input of the associated filter stage and a gain control input for receiving a gain control signal that determines the amplification factor of the associated input amplification stage, the input of the input amplification stage associated with each filter stage, except for the input amplification stage associated with the first filter stage, being coupled to the output of a preceding filter stage, if any, the input of the amplification stage associated with the first filter stage being coupled to the system input, each filter stage having an associated output amplification stage including a signal input coupled to the output of the associated filter stage, a signal output and a gain control input for receiving a gain control signal that determines the amplification factor of the associated output amplification stage, the signal output of the output amplification stage associated with a selected one of the at least one filter stage being coupled to the system output;

a strength detector having an input coupled to the output of the first filter stage, and having a first output and a second output for providing respective output signals indicative of whether the first filter stage is approaching saturation or is providing an output signal having less than a minimum acceptable signal to noise ratio;

a zero crossing detector having at least one input coupled to respective ones of the at least one output of the at least one filter stage of the main filter, and having at least one output for providing at least one signal indicative of when a successive one of the at least one filter stage of the main filter provides a signal at its output that is approximately equal to zero; and

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a gain control unit having a first input and a second input respectively coupled to the output of the strength detector and coupled to the at least one output of the zero crossing detector, and having a multiplicity of outputs for providing respective gain control signals to the gain control input of each input amplification stage and each output amplification stage associated with the at least one filter stage of the main filter, the gain control unit being responsive to signals provided initially by the strength detector indicative of the first filter stage approaching saturation or providing an output signal having less than the minimum acceptable signal to noise ratio, and a signal from the zero crossing detector indicative of the output signal provided by the first filter stage being approximately equal to zero for providing a gain control signal to the gain control input of the input amplification stage associated with the first filter stage so that the input amplification stage associated with the first filter stage has an amplification factor that results in a signal strength at its signal output which avoids saturation of the first filter stage and avoids the first filter stage providing a signal having less than the minimum acceptable signal to noise ratio, and for providing a gain control signal to the gain control input of the output amplification stage associated with the first filter stage so that the output amplification stage associated with the first filter stage has an amplification factor which is the reciprocal of the amplification factor of the input amplification stage associated with the first filter stage, the gain control unit being thereafter responsive to signals provided initially by the strength detector indicative of the first filter stage of the main filter approaching saturation or providing an output having less than the minimum acceptable signal to noise ratio, and to a signal from the zero crossing detector indicating that an output signal at the output of a successive filter stage, if any, being approximately equal to zero for providing a gain control signal to the gain control input of the input amplification stage associated with the successive filter stage so that the input amplification stage associated with the successive filter stage has an amplification factor that results in a signal strength at its signal output that avoids saturation of the successive filter stage and avoids the successive filter stage providing a signal having less than the minimum acceptable signal to noise ratio, and for providing a gain control signal to the gain control input of the output amplification

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stage associated with the successive filter stage so that the output amplification stage associated with the successive filter stage has an amplification factor which is a reciprocal of the amplification factor of the input amplification stage associated with the successive filter stage.

2. An active filter system according to claim 1, wherein the at least one filter stage of the main filter comprises a first filter stage and a second filter stage, and the zero crossing detector comprising:

a switching unit having a first signal input coupled to the output of the first filter stage, a second signal input coupled to the output of the second filter stage, a switch control input, and a signal output, the switching unit being responsive to a first switch control signal received by the switch control terminal for connecting the first signal input to the signal output and disconnecting the second signal input from the signal output, and being responsive to a second switch control signal received by the switch control terminal for connecting the second signal input to the signal output and disconnecting the first signal input from the signal output;

a comparator having a signal input coupled to the signal output of the switching unit, and a signal output for providing an output signal, the comparator providing a first logical signal on the signal output if the signal received at the signal input is approximately equal to zero, and providing a second logical signal on the signal output if the signal received at the signal input is not approximately equal to zero; and

a three-stage shift register having a clock input coupled to the signal output of the comparator, a reset/enable input, a first stage output, a second stage output and a third stage output, the shift register being responsive to a first logical signal received at the reset/enable input for producing a first logical signal at the first stage output, a second logical signal at the second stage output and a second logical signal at the third stage output, and being responsive to receiving the second logical signal at the reset/enable input and a signal changing from the second logical signal to the first logical signal at the clock input while having the first logical signal at the first stage output, the second logical signal at the second stage output and the second logical signal at the third stage output for providing the second logical signal at the

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first stage output, the first logical signal at the second stage output and the second logical signal at the third stage output, the shift register being responsive to the first logical signal received at the reset/enable input and a signal changing from the second logical signal to the first logical signal at the clock input while having the second logical signal at the first stage output, the first logical signal at the second stage output and the second logical signal at the third stage output for providing the second logical signal at the first stage output, the second logical signal at the second stage output and the first logical signal at the third stage output, and being responsive to the first logical signal received at the reset/enable input and a signal changing from the second logical signal to the first logical signal at the clock input while having the second logical signal at the first stage output, the second logical signal at the second stage output and the first logical signal at the third stage output for providing the second logical signal at the first stage output, the second logical signal at the second stage output and the first logical signal at the third stage output, and wherein the first stage output, the second stage output and the third stage output are the output signals of the zero crossing detector provided to the gain control unit, and the first stage output is also the switch control terminal of the switching unit.

3. The active filter system of claim 2, wherein the gain control unit has a first zero cross input coupled to the first stage output of the shift register and the switch control input of the switching unit, a second zero cross input coupled to the second stage output of the shift register, a third zero cross input coupled to the third stage output of the shift register, a reset/enable output for providing a reset/enable signal to the reset/enable input of the shift register, a first gain control output terminal, a second gain control output terminal, a third gain control output terminal, a fourth gain control output terminal and a fifth gain control output terminal;

the gain control unit being responsive to receiving a first signal from the strength detector indicative of the first filter stage providing a signal having less than the minimum acceptable signal to noise ratio when the first gain control terminal is providing a second logical signal, the second gain control terminal is providing the second logical signal, the third gain control terminal is providing the second logical signal, the fourth gain control terminal is providing a first logical signal and the fifth

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gain control terminal is providing the second logical signal, for providing the second logical signal on the reset/enable output, and being thereafter responsive to receiving the second logical signal on the first zero cross input, the first logical signal on the second zero cross input and the second logical signal on the third zero cross input for providing the second logical signal on the reset/enable output, the second logical signal on the first gain control output terminal, the first logical signal on the second gain control output terminal, the second logical signal on the third gain control output terminal, the second logical signal on the fourth gain control output terminal and the first logical signal on the fifth gain control output terminal, and being thereafter responsive to receiving the second logical signal on the first zero cross input, the second logical signal on the second zero cross input and the first logical signal on the third zero cross input for providing the second logical signal on the reset/enable output, the first logical signal on the first gain control output terminal, the second logical signal on the second gain control output terminal, the second logical signal on the third gain control output terminal, the first logical signal on the fourth gain control output terminal and the second logical signal on the fifth gain control output terminal;

the gain control unit being responsive to receiving a signal from the signal strength detector indicative of the first filter stage providing a signal having less than the minimum acceptable signal to noise ratio while the first gain control output terminal is providing the first logical signal, the second gain control output terminal is providing the second logical signal, the third gain control output terminal is providing the second logical signal, the fourth gain control output terminal is providing the first logical signal and the fifth gain control output is providing the second logical signal, for providing after a particular time delay the second logical signal on the reset/enable output, and being thereafter responsive to receiving the second logical signal on the first zero cross input, the first logical signal on the second zero cross input and the second logical signal on the third zero cross input for providing the second logical signal on the reset/enable output, the second logical signal on the first gain control output terminal, the first logical signal on the second gain control output terminal, the first logical signal on the third gain control output terminal, the second logical signal on the fourth gain control output terminal and the

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second logical signal on the fifth gain control output terminal, and being thereafter responsive to receiving the second logical signal on the first zero cross input, the second logical signal on the second zero cross input and the first logical signal on the third zero cross input for providing the second logical signal on the reset/enable output, the second logical signal on the first gain control output terminal, the first logical terminal on the second gain control output terminal, the second logical signal on the third gain control output terminal, the first logical signal on the fourth gain control output terminal and the second logical signal on the fifth gain control output terminal;

the gain control unit being responsive to receiving a signal from the strength detector indicative of the first filter stage approaching saturation while the first gain control output is providing the second logical signal, the second gain control output is providing the first logical signal, the third gain control output terminal is providing the second logical signal, the fourth gain control output is providing the second logical signal and the fifth gain control output terminal is providing the second logical signal, for providing after a particular time delay the second logical signal on the reset/enable output, and being thereafter responsive to receiving the second logical signal on the first zero cross input, the first logical signal on the second zero cross input and the second logical signal on the third zero cross input for providing the second logical signal on the reset/enable output, the second logical signal on the first gain control output terminal, the second logical signal on the second gain control output terminal, the first logical signal on the third gain control output terminal, the second logical signal on the fourth gain control output terminal and the second logical signal on the fifth gain control output terminal, and being thereafter responsive to receiving the second logical signal on the first zero cross input, the second logical signal on the second zero cross input and the first logical signal on the third zero cross input for providing the second logical signal on the reset/enable output, the second logical signal on the first gain control output terminal, the second logical signal on the second gain control output terminal, the second logical signal on the third gain control output terminal, the first logical signal on the fourth gain control output terminal and the second logical signal on the fifth gain control output terminal, and wherein:

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the gain control input of the input amplification stage associated with the first filter stage comprises a first gain control terminal and a second grain control terminal, the first gain control terminal of the input amplification stage associated with the first filter stage of the main filter being coupled to the first gain control output terminal of the gain control unit, and the second gain control terminal of the input amplification stage associated with the first filter stage of the main filter is coupled to the second gain control output terminal of the gain control unit, the input amplification stage associated with the first filter stage being responsive to receiving the second logical signal on its first gain control terminal and the second logical signal on its second gain control terminal for amplifying the input signal by a first amplification factor, and being responsive to receiving the second logical signal on the first gain control terminal and the first logical signal on the second gain control terminal for amplifying the input signal by a second amplification factor which is greater than the first amplification factor, and being responsive to receiving the first logical signal on the first gain control terminal and the second logical signal on the second gain control terminal for amplifying the input signal by a third amplification factor which is greater than the second amplification factor;

the gain control input of the output amplification stage associated with the first filter stage comprises a first gain control terminal and a second gain control terminal, the first gain control terminal of the output amplification stage associated with the first filter stage being coupled to the first gain control output terminal of the gain control unit, the second gain control terminal of the output amplification stage associated with the first filter stage is coupled to the second gain control output terminal of the gain control unit, the output amplification stage associated with the first filter stage being responsive to receiving the second logical signal on its first gain control terminal and the second logical signal on its second gain control terminal for amplifying a signal provided by the output of the first filter stage by the third amplification factor, and being responsive to receiving the second logical signal on its first gain control terminal and the first logical signal on its second gain control terminal for amplifying the signal provided by the output of the first filter stage by the second amplification factor, and being responsive to receiving the first logical signal

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on the first gain control terminal and the second logical signal on the second gain control terminal for amplifying the signal provided by the output of the first filter stage by the first amplification factor;

the gain control input of the input amplification stage associated with the second filter stage comprises a third grain control terminal and a fourth gain control terminal, the third gain control terminal of the input amplification stage associated with the second filter stage being coupled to the third gain control output terminal of the gain control unit, and the fourth gain control terminal of the input amplification stage associated with the second filter stage is coupled to the fourth gain control output terminal of the gain control unit, the input amplification stage associated with the second filter stage being responsive to receiving the first logical signal on its third gain control terminal and the second logical signal on its fourth gain control terminal for amplifying a signal provided by the output of the first filter stage by a fourth amplification factor, and being responsive to receiving the second logical signal on its third gain control terminal and the first logical signal on its fourth gain control terminal for amplifying the signal provided by the output of the first filter stage by a fifth amplification factor which is greater than the fourth amplification factor, and being responsive to receiving the first logical signal on its third gain control terminal and the second logical signal on its fourth gain control terminal for amplifying the signal provided by the output of the first filter stage by a sixth amplification factor which is greater than the fifth amplification factor; and

the gain control input of the output amplification stage associated with the second filter stage comprises a fourth gain control terminal and a fifth gain control terminal, the fourth gain control terminal of the output amplification stage associated with the second filter stage being coupled to the fourth gain control output terminal of the gain control unit, the fifth gain control terminal of the amplification stage associated with the second filter stage being coupled to the fifth gain control unit, the output amplification stage associated with the second filter stage being responsive to receiving the second logical signal on its fourth gain control terminal and the second logical signal on its fifth gain control terminal for amplifying a signal provided by the output of the second filter stage by the fourth amplification factor, and being

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responsive to receiving the second logical signal on its fourth gain control terminal and the first logical signal on its fifth gain control terminal for amplifying the signal provided by the output of the second filter stage by the sixth amplification factor, and being responsive to receiving the first logical signal on its fourth gain control terminal and the second logical signal on its fifth gain control terminal for amplifying the signal provided by the output of the second filter stage by the fifth amplification factor.

4. The active filter system of claim 3, wherein the signal strength detector comprises:

a peak detector having an input coupled to the output of the first filter stage of the main filter and an output, the peak detector detecting a voltage envelope peak of the signal provided by the output of the first filter stage and providing a signal representative of the voltage envelope peak at its output;

a first threshold detector having an input coupled to the output of the peak detector and an output, the first threshold detector comparing the signal provided by the peak detector with a first threshold representative of a signal strength at the input of the first filter stage that would cause the first filter stage to approach saturation, the first threshold detector providing the first logical signal at its output if the signal received from the peak detector is less than the first threshold, and providing the second logical signal at its output if the signal received from the peak detector is greater than or equal to the first threshold; and

a second threshold detector having an input coupled to the output of the peak detector and an output, the second threshold detector comparing the signal from the peak detector with a second threshold representative of an input signal strength at the input of the first filter stage that would cause a signal provided by the output of the first filter to have less than a minimum acceptable signal to noise ratio, the second threshold detector providing the first logical signal at its output if the signal from the peak detector is greater than or equal to the second threshold, and for providing the second logical signal at its output if the signal from the peak detector is

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less than the second threshold, wherein the output of the first threshold detector and the output of the second threshold detector comprise the first and second outputs of the strength detector, respectively.

5. The active filter system of claim 3, wherein the first filter stage comprises a first integrator having an input and an output, and the second filter stage comprises a second integrator having an input and an output.

6. The active filter system of claim 2, wherein the input of the output amplification stage associated with the second filter stage is coupled to the output of the second filter stage, and the output of the output amplification stage associated with the second filter stage is coupled to the signal input of the input amplification stage associated with the second filter stage, and wherein the signal output of the output amplification stage associated with the first filter stage is coupled to the system output.

7. The active filter system of claim 2, wherein the input amplification stage associated with the first filter stage includes circuitry for clamping an output signal provided by the input amplification stage so as to prevent saturation of the first filter stage.

8. The active filter system of claim 2, wherein the input amplification stage associated with the second filter stage includes circuitry for clamping an output signal provided by the input amplification stage so as to prevent saturation of the second filter stage.

9. The active filter system of claim 6, wherein the output amplification stage associated with the second filter stage includes circuitry for clamping an output signal provided by the output amplification stage so as to prevent saturation of the second filter stage.

10. An active filter system according to claim 5, wherein the input amplification stage associated with the first filter stage includes: a first resistor; a second resistor; a third resistor; a fourth resistor; a capacitor; a first switch having a

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first terminal, a second terminal and a switch control terminal; a second switch having a first terminal, a second terminal and a switch control terminal; and an operational amplifier having an inverted input, a normal input and an output, the first resistor being connected between the system input and the inverting input of the operational amplifier, the second resistor being connected between the system input and the first terminal of the first switch, the third resistor being connected between the system input and the first terminal of the second switch, the second terminal of the first switch being coupled to the inverting input of the operational amplifier, the second terminal of the second switch being coupled to the inverting input of the operational amplifier, the fourth resistor being coupled between the output and the inverting input of the operational amplifier, the capacitor being coupled between the output and the inverting input of the operational amplifier, the normal input of the operational amplifier being coupled to ground, the switch control terminal of the first switch being coupled to the second gain control terminal, the switch control terminal of the second switch being coupled to the first gain control terminal, wherein each of the first switch and the second switch is responsive to receiving the first logical signal on its switch control terminal for connecting its first terminal to its second terminal, and is responsive to receiving the second logical signal on its switch control terminal for disconnecting its first terminal from its second terminal.

11. The active filter system of claim 10, wherein the first resistor has a resistance of 200 kΩ, the second resistor has a resistance of 22.22 kΩ, the third resistor has a resistance of 2.02 kΩ has a resistance of 20 kΩ, and the capacitor 80 pF.

12. The active filter system of claim 5, wherein the first integrator comprises: a resistor; a capacitor; and an operational amplifier having an inverting input, a normal input and an output, the resistor being coupled between the output and the inverting input of the operational amplifier, the capacitor being coupled between the output and the inverting input of the operational amplifier, the normal input of the operational amplifier being coupled to ground, the inverting input of the operational amplifier being coupled to the input of the first integrator, and the output of the operational amplifier being coupled to the output of the first integrator.

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13. The active filter system of claim 12, wherein the resistor has a resistance of 20 kΩ and the capacitor has a capacitance of 80 pF.

14. The active filter system of claim 5, wherein the output amplification stage associated with the first filter stage comprises: a first resistor; a second resistor; a third resistor; a fourth resistor; a first switch having a first terminal, a second terminal and a switch control terminal; a second switch having a first terminal, a second terminal and a switch control terminal; and an operational amplifier having a normal input, an inverting input and an output, the first resistor being coupled between the output of the first integrator and the inverting input of the operational amplifier, the second resistor being coupled between the output and the inverting input of the operational amplifier, the third resistor being coupled between the inverting input of the operational amplifier and the first terminal of the first switch, the fourth resistor being coupled between the inverting input of the operational amplifier and the first terminal of the second switch, the second terminal of the first switch being coupled to the output of the operational amplifier, the second terminal of the second switch being coupled to the output of the operational amplifier, the normal input of the operational amplifier being coupled to ground, the switch control terminal of the first switch being coupled to the second gain control input terminal and the switch control terminal of the second switch being coupled to the first gain control terminal, wherein each of the first switch and the second switch is responsive to receiving the first logical signal on its switch control terminal for connecting its first terminal to its second terminal, and is responsive to receiving the second logical signal on its switch control terminal for disconnecting its first terminal from its second terminal.

15. The active filter system according to claim 14, wherein the first resistor has a resistance of 20 kΩ, the second resistor has a resistance of 200 kΩ, the third resistor has a resistance of 22.22 kΩ and the fourth resistor has a resistance of 2.02 kΩ.

16. The active filter system of claim 5, wherein the input amplifier stage associated with the second filter stage comprises: a first resistor; a second resistor; a

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third resistor; a capacitor; a first switch having a first terminal, a second terminal and a switch control terminal; a second switch having a first terminal, a second terminal and a switch control terminal; and an operational amplifier having a normal input, an inverting input and an output, the first resistor being coupled between the output of the first integrator and the inverting input of the operational amplifier, the second resistor being coupled between the output of the first integrator and the first terminal of the first switch, the third resistor being coupled between the output of the first integrator and the first input of the second switch, the second terminal of the first switch being coupled to the inverting input of the operational amplifier, the second terminal of the second switch being coupled to the inverting input of the operational amplifier, the capacitor being coupled between the output and the inverting input of the operational amplifier, the normal input of the operational amplifier being coupled to ground, the switch control terminal of the first switch being coupled to the fourth gain control terminal and the switch control terminal of the second switch being coupled to the third gain control terminal, wherein each of the first switch and the second switch is responsive to receiving a first logical signal on its switch control terminal for connecting its first terminal to its second terminal, and is responsive to receiving the second logical signal on its switch control terminal for disconnecting its first terminal from its second terminal.

17. The active filter system of claim 16, wherein the first resistor has a resistance of 10 kΩ, the second resistor has a resistance of 1.01 kΩ, the third resistor has a resistance of .10 kΩ and the capacitor has a capacitance of 80 pF.

18. The active filter system of claim 5, wherein the second integrator comprises a capacitor, and an operational amplifier having a normal input, an inverting input and an output, the capacitor being coupled between the output and the inverting input of the operational amplifier, the inverting input of the operational amplifier being coupled to the input of the second integrator, the output of the operational amplifier being coupled to the output of the second integrator, the normal input of the operational amplifier being coupled to ground.

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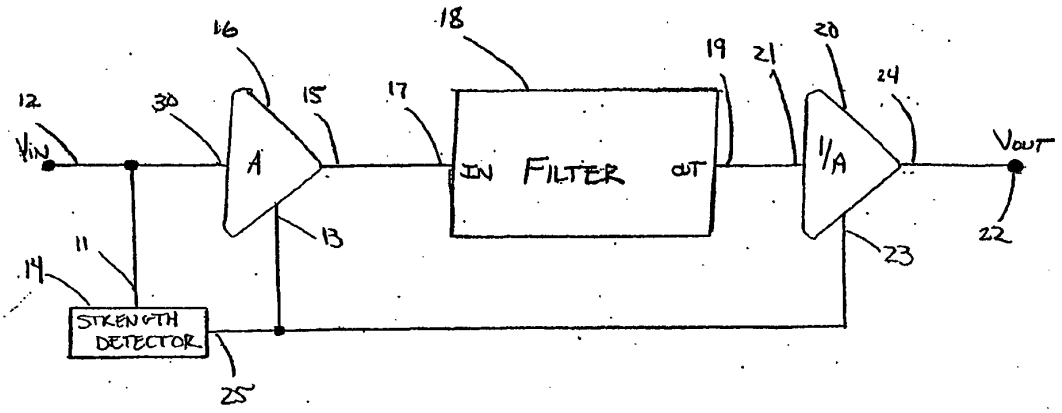
19. The active filter system of claim 6, wherein the output amplification stage associated with the second filter stage comprises: a first resistor; a second resistor; a third resistor; a fourth resistor; a fifth resistor; a sixth resistor; a capacitor; a first switch having a first terminal, a second terminal and a switch control terminal; a second switch having a first terminal, a second terminal and a switch control terminal; a first operational amplifier having a normal input, an inverting input and an output; and a second operational amplifier having a normal input, an inverting input and an output, the first resistor being coupled between the output of the second integrator and the inverting input of the first operational amplifier, the second resistor being coupled between the output and the inverting input of the first operational amplifier, the third resistor being coupled between the output of the first operational amplifier and the inverting input of the second operational amplifier, the fourth resistor being coupled between the inverting input of the second operational amplifier and the first terminal of the first switch, the fifth resistor being coupled between the inverting input of the second operational amplifier and the first terminal of the second switch, the second terminal of the first switch being coupled to the output of the first operational amplifier, the second terminal of the second switch being coupled to the output of the first operational amplifier, the normal output of the first operational amplifier being coupled to ground, the sixth resistor being coupled between the output and the inverting input of the second operational amplifier, the capacitor being coupled between the output and the inverting input of the second operational amplifier and the normal input of the second operational amplifier being coupled to ground, wherein each of the first switch and the second switch is responsive to receiving the first logical signal on its switch control terminal for connecting its first terminal to its second terminal, and is responsive to receiving the second logical signal on its switch control terminal for disconnecting its first terminal from its second terminal.

20. The active filter system of claim 19, wherein the first resistor has a resistance of 10 kΩ, the second resistor has a resistance of 10 kΩ, the third resistor has a resistance of 10 kΩ, the fourth resistor has a resistance of 1.11 kΩ, the fifth resistor has a resistance of .10 kΩ, the sixth resistor has a resistance of 20 kΩ, and the capacitor has a capacitance of 80 pF.

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21. The active filter system of claim 4, wherein the gain control unit comprises a multiple state logic circuit responsive to the signals provided by the first and second threshold detectors of the strength detector, and the signals received at the first zero cross input, the second zero cross input and the third zero cross input for deriving respective signals on the first gain control output terminal, the second gain control output terminal, the third gain control output terminal, the fourth gain control output terminal and the fifth gain control output terminal.

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FIG. 1
(Prior Art)

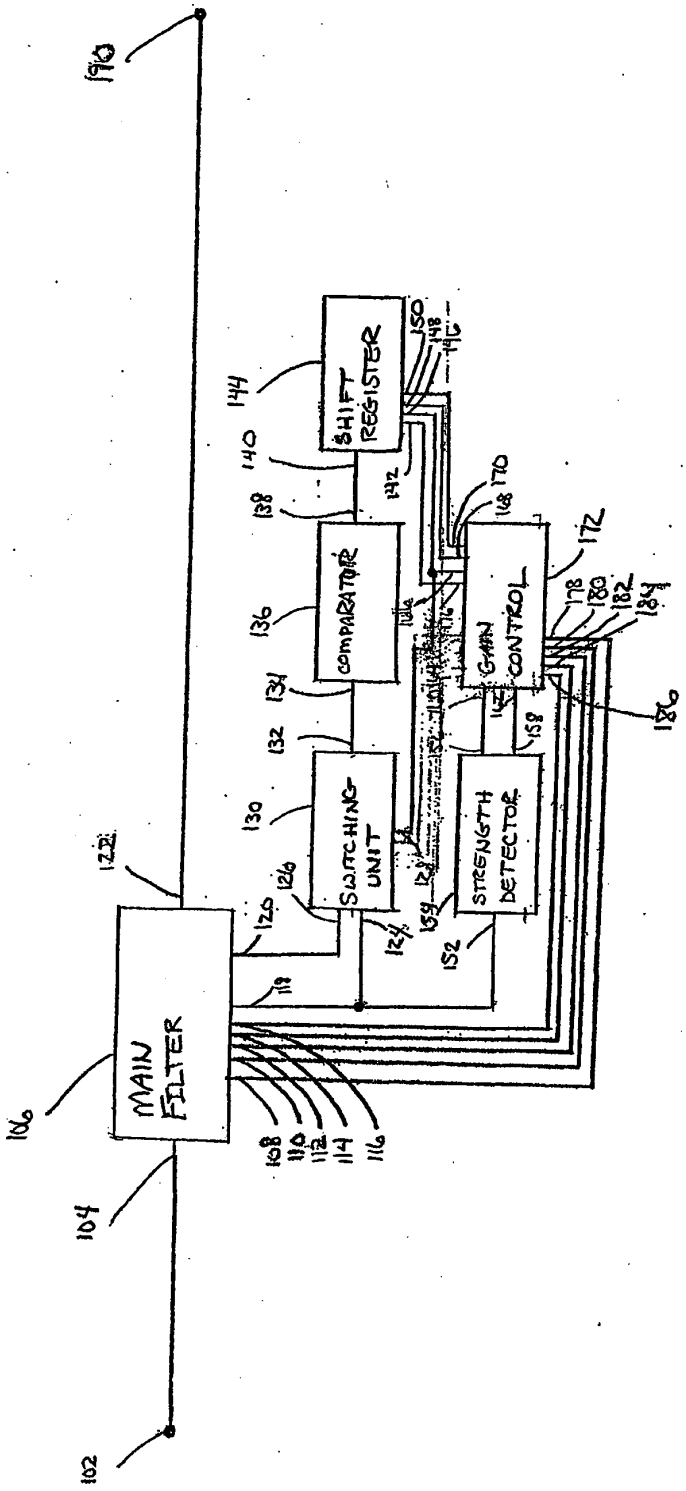
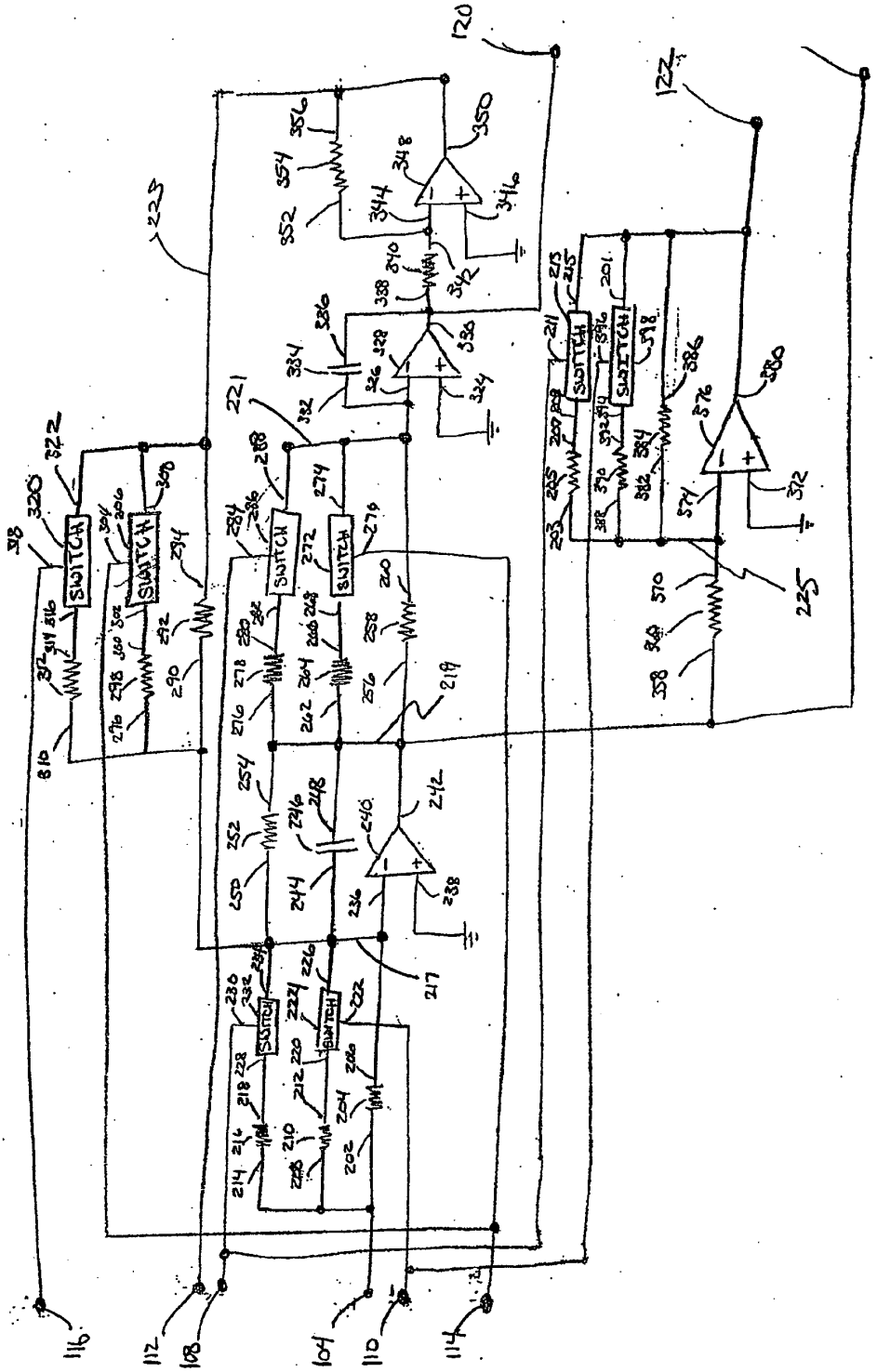

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SHIFT REGISTER
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COMPARATOR
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134
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SWITCHING UNIT
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120
118
MAIN FILTER
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104
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110
112
114
116
GAIN CONTROL
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172
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STRENGTH DETECTOR
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FIG. 2



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FIG. 3

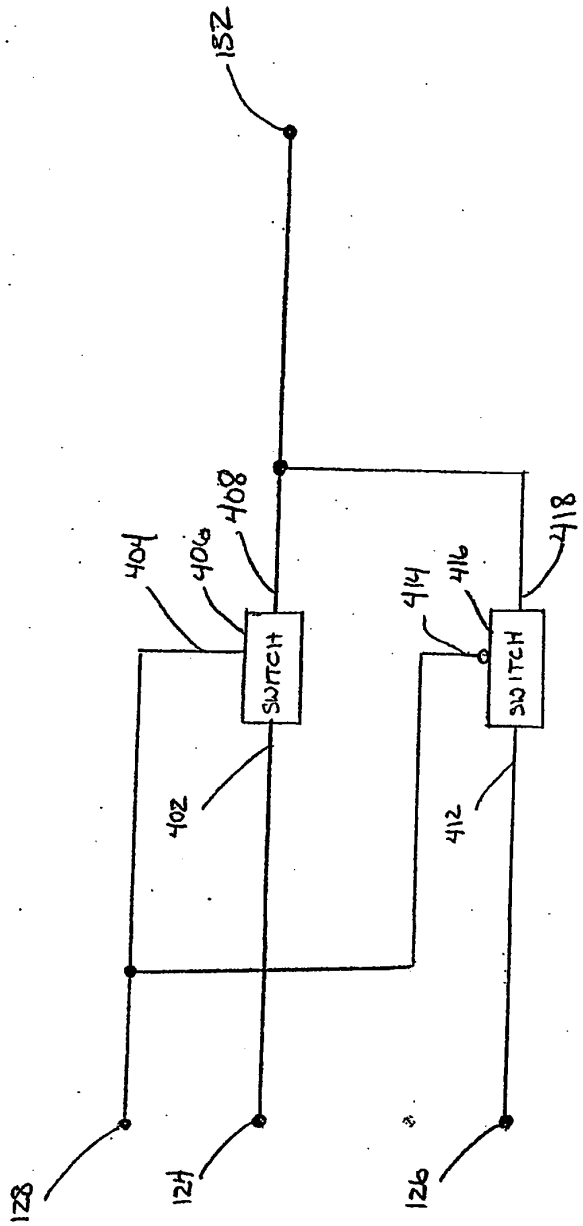
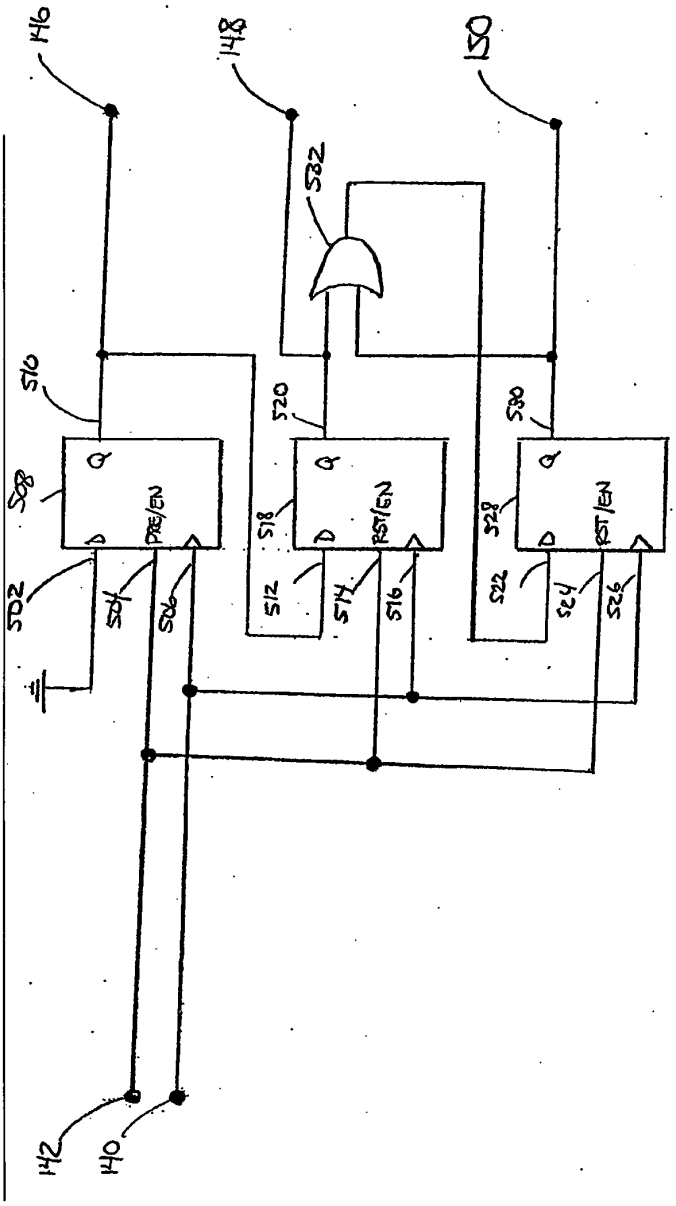
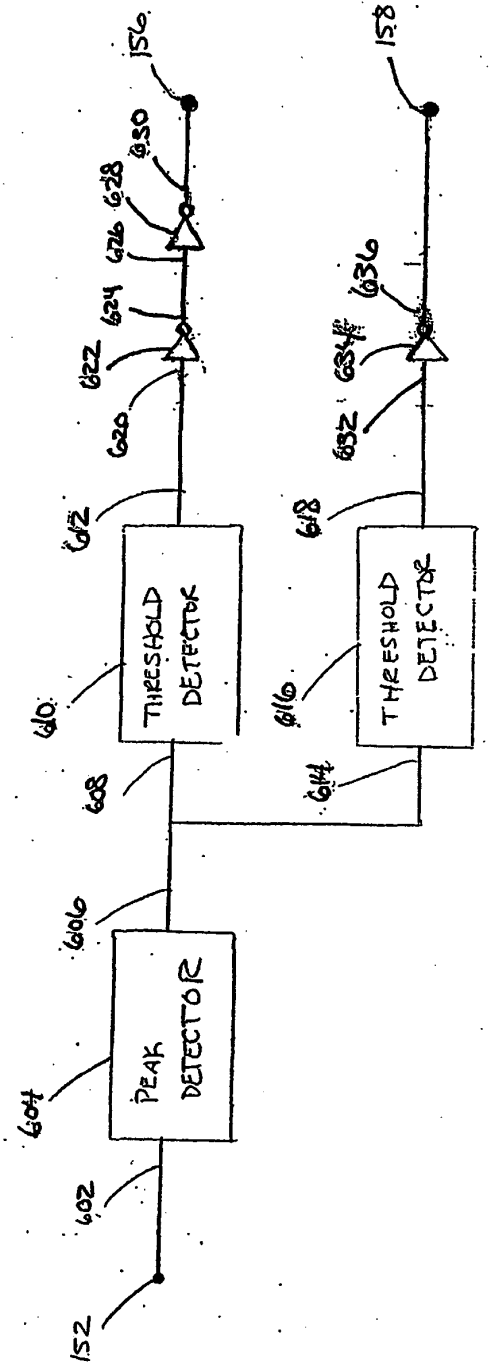

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SWITCH
SWITCH
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FIG. 4

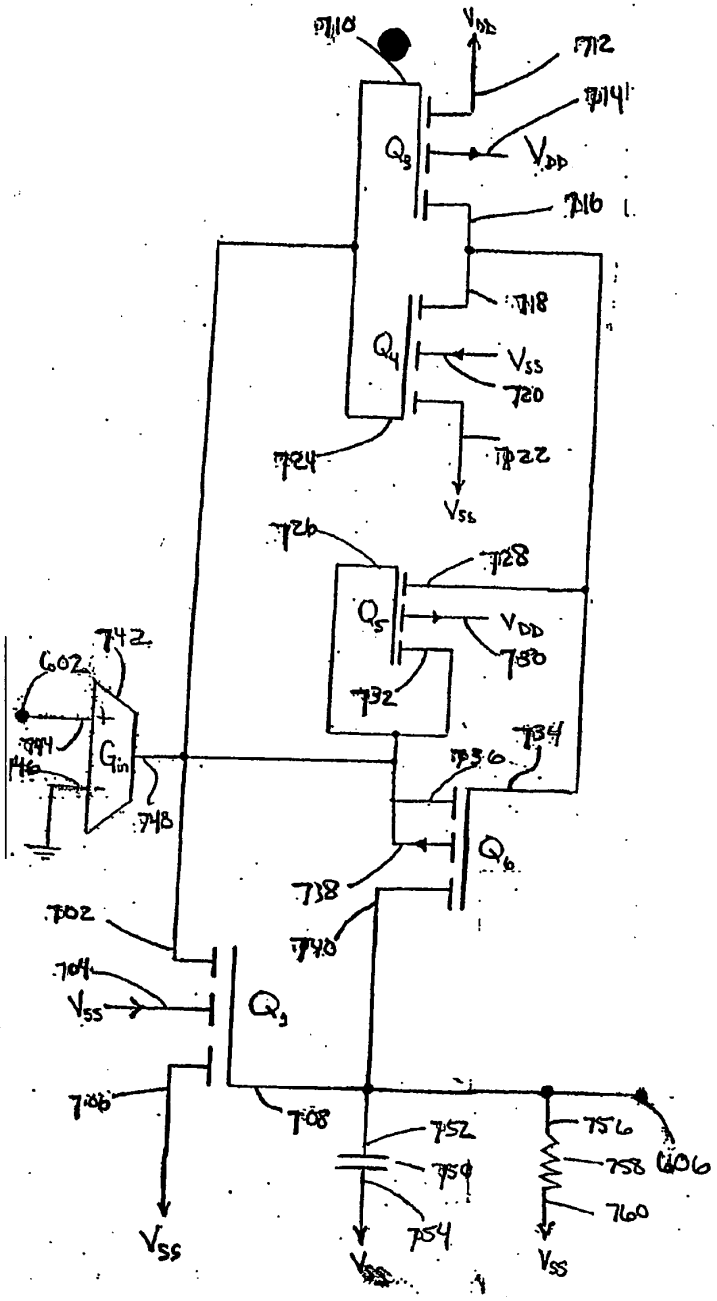

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RST/EN
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FIG. 5

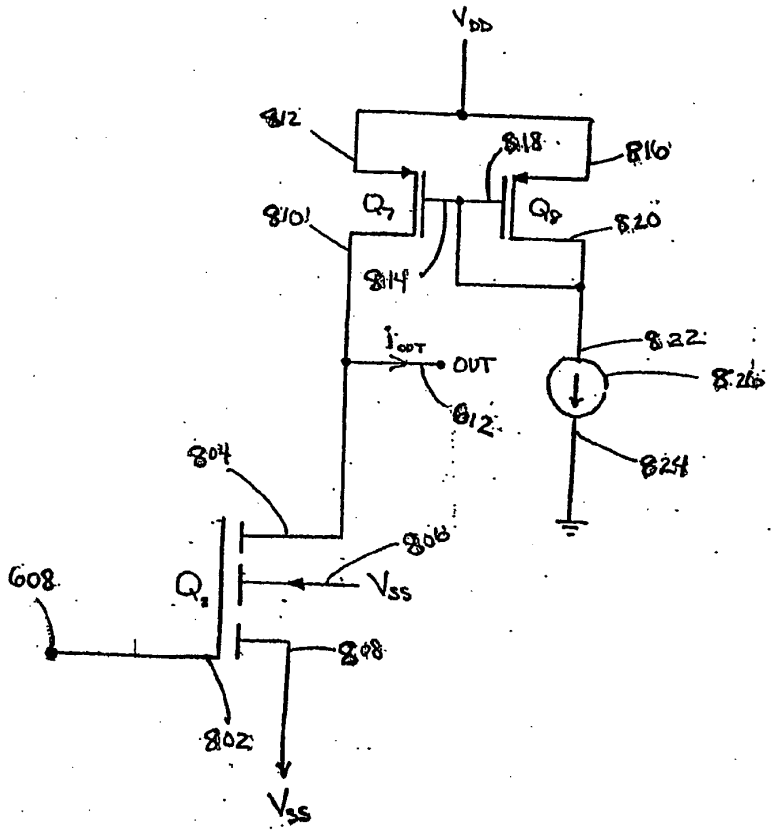

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THRESHOLD DETECTOR
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PEAK DETECTOR
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Fig. 6


710
712
714
Q_3
V_{DD}
716
718
Q_4
V_{SS}
720
722
724
V_{SS}
726
728
Q_5
V_{DD}
730
732
734
736
Q_6
738
740
742
602
744
746
G_{in}
748
702
704
V_{SS}
Q_3
706
708
752
754
V_{SS}
756
758
760
V_{SS}
606

604

Fig. 7


V_{DD}
812
818
810'
Q_7
Q_8
810
820
814
I_{OUT}
OUT
822
826
824
804
806
608
Q_2
V_{SS}
808
802
V_{SS}

610

Fig. 8

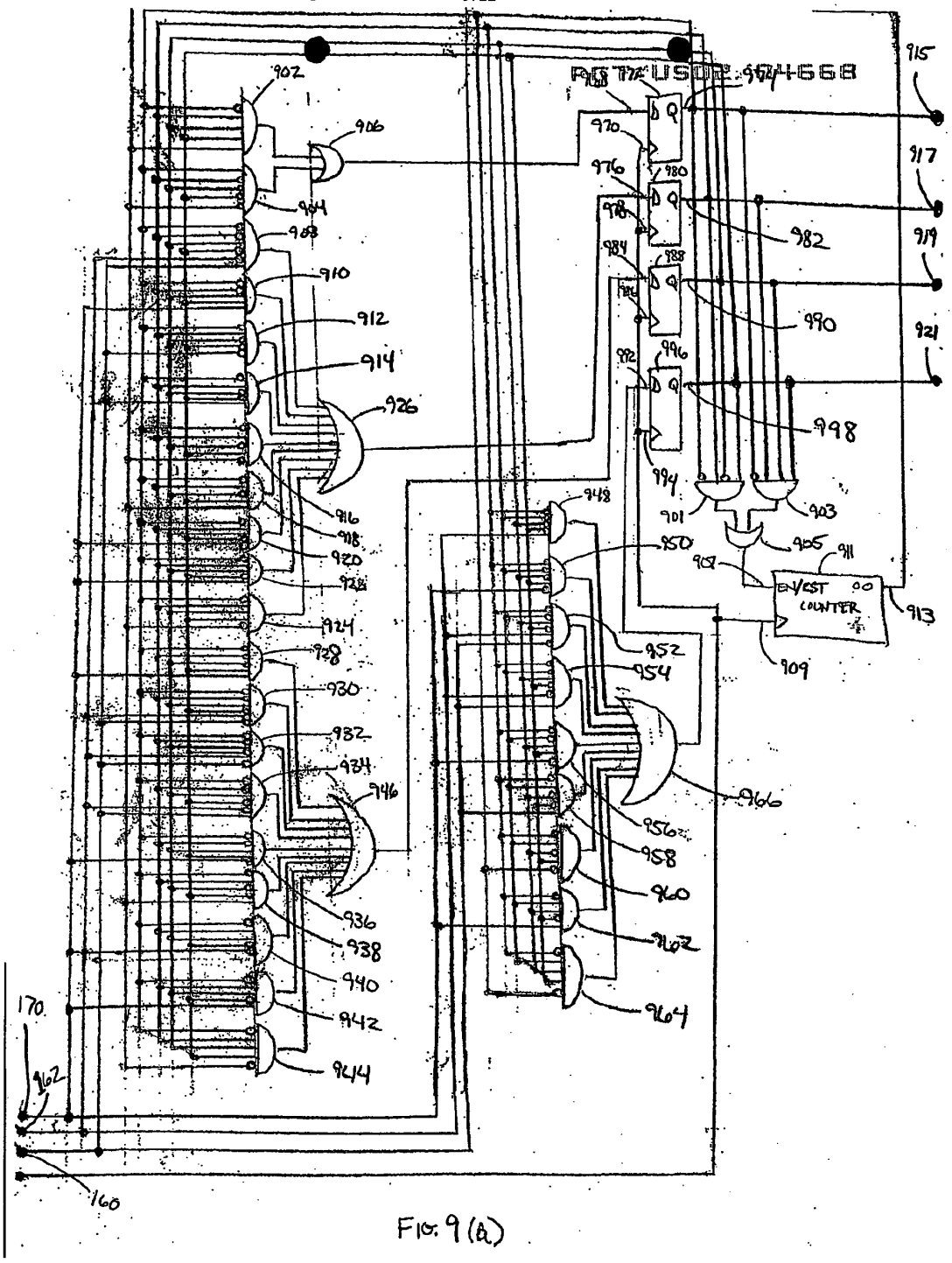

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EN/DST COUNTER
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FIG. 9(a)

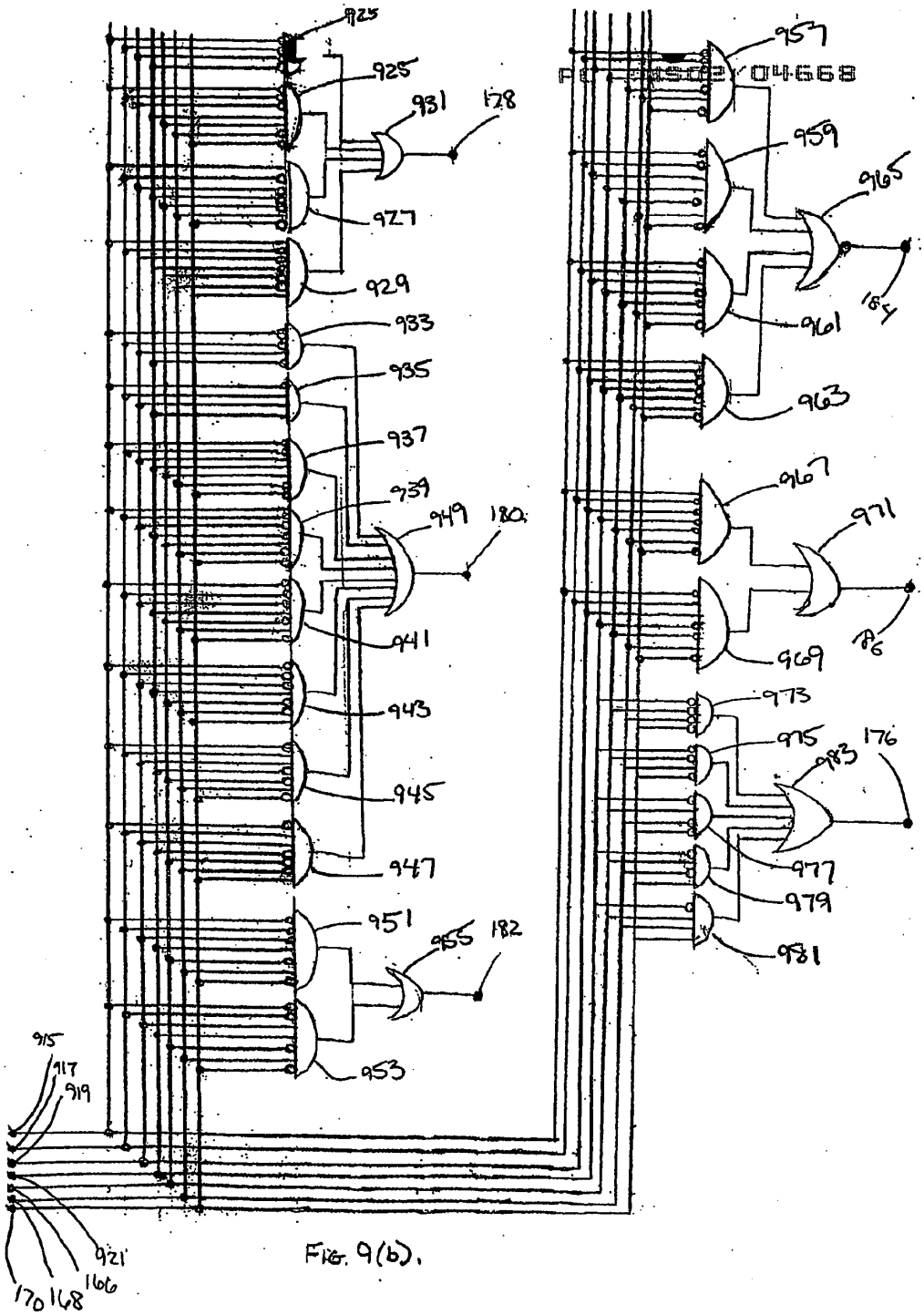
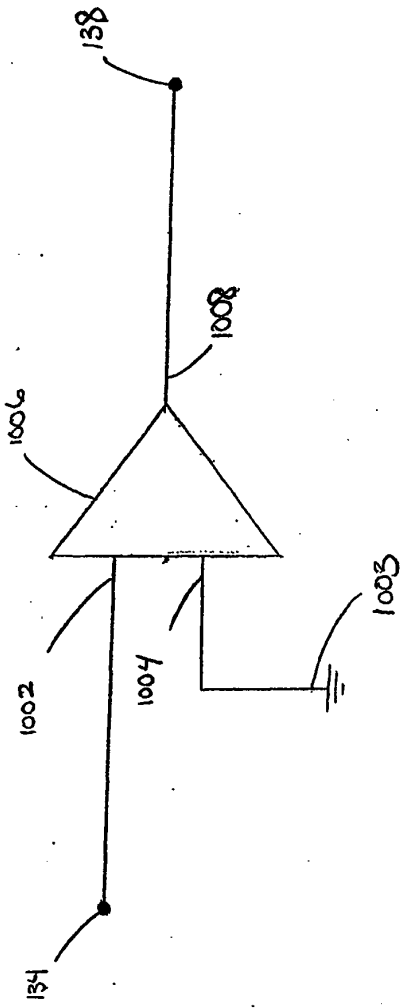
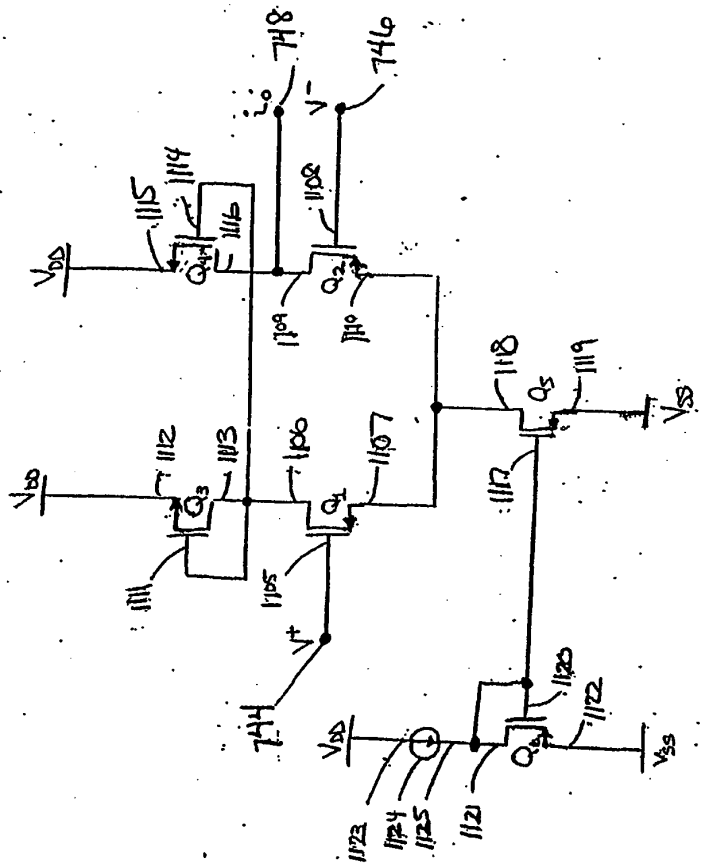

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Fig. 9(b).



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Fig. 10


748
746
V-
1114
1115
1116
1108
VSS
Q1
Q2
1109
1110
1118
1119
Q5
VSS
1112
1113
1106
1107
B
Q3
Q4
1117
1111
1105
V+
744
1120
1122
VSS
Q6
VSS
1123
1124
1125
1121

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Fig. 11

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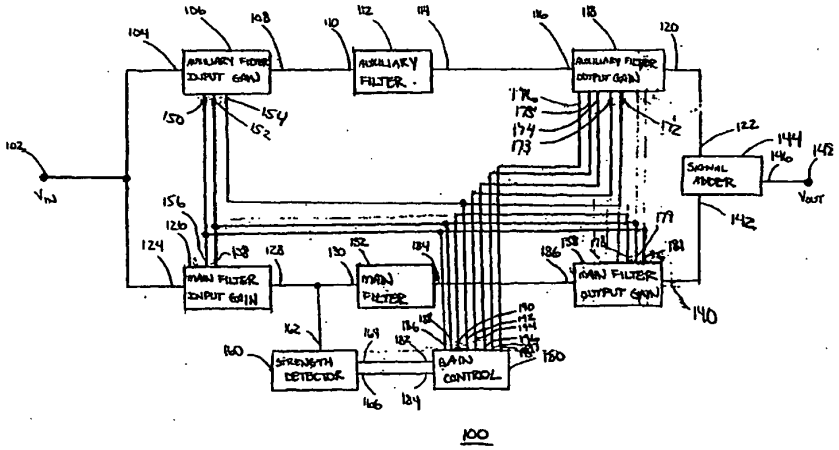
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[Continued on next page]

(54) Title: ACTIVE FILTER CIRCUIT WITH DYNAMICALLY MODIFIABLE GAIN



(57) Abstract: A signal processing system (100) comprises an input terminal (102), and a main path having a main filter input gain unit (126) coupled to said input terminal (102), a main filter (132) and an output gain unit (138). An auxiliary path includes an auxiliary filter input gain unit (106) coupled to the input terminal (102), an auxiliary filter (112) and an auxiliary filter output gain unit (118). An adder (144) is coupled to the output gain units (118, 138) for generating an output signal to an output terminal (148). The gains of the gain units are adjusted by a control unit (18) responsive to a detecting signal from a detector (160).

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ACTIVE FILTER CIRCUIT WITH DYNAMICALLY MODIFIABLE GAIN

SPECIFICATION

This application claims priority to U.S. Provisional Application Serial Number 60/260,722 filed January 10, 2001, and U.S. Provisional Application Serial Number 60/288,976 filed May 4, 2001, each of which is incorporated by reference herein in its entirety.

BACKGROUND OF THE INVENTION

The present invention relates to signal processors and, more particularly, to signal processors that are dynamically modifiable for optimal performance and reduced power dissipation.

In order to expand the dynamic range of a signal processing system, companding signal processors can be used. A companding signal processor uses an input amplifier to amplify or attenuate a signal before it is provided to the signal processor, and an output amplifier is used to amplify or attenuate the signal provided by the signal processor. A signal processor or signal processing circuit includes an active filter. The gain of the output amplifier is the inverse of the gain of the input amplifier, thus conserving the overall gain of the signal processor. Ideally, the gains of the input amplifier and output amplifier can be varied dynamically. A signal strength detector can be used to measure the strength of the input signal and provide a corresponding gain control signal. See Y. Tsividis, "Externally linear, time-invariant systems and their application to companding signal processors," IEEE Transactions on Circuits and Systems II, Vol. 44, No. 2, February 1997. The gain control signal sets the amplification factors of the input amplifier and the output amplifier. However, this approach has the problem in that because the signal processor has memory, distortion in the output of the signal processor occurs whenever the amplification factors of the input amplifier and the output amplifier are changed.

The analog floating point technique addresses the problem of distortion in the output whenever the amplification factors change. See E. Blumenkrantz, "The analog floating point technique," Proc. IEEE Symposium on Low Power Electronics, p. 72-73, 1995. This technique avoids distortion by altering the state variables of the signal processor when the amplification factors change. However, implementation of the analog floating point technique is complicated, and is sensitive to parasitics and component mismatch. Accordingly, there is a need for circuits which expand the

dynamic range of a signal processor without interrupting the output of the system or causing distortion.

SUMMARY OF THE INVENTION

It is therefore an object of this invention to provide a circuit which has a large dynamic range and which operates in an energy-efficient manner without interrupting the output of the circuit or causing distortion.

In accordance with the present invention, there is provided an active filter system including a system input for receiving a system input signal, a system output for providing a system output signal, a first input gain circuit, a first filter circuit, a first output gain circuit, a second input gain circuit, a second filter circuit, a second output gain circuit and a signal adding circuit. The first input gain circuit having a signal input coupled to the system input for receiving the system input signal, a gain control input and an output for providing a first amplified system input signal, the first input gain circuit being responsive to a first gain control signal received by the gain control input for amplifying the system input signal by a first amplification factor to obtain the first amplified system input signal, and being responsive to a second gain control signal received by the gain control input for amplifying the system input signal by a second amplification factor to obtain the first amplified system input signal. The first filter circuit having an input coupled to the output of the first input gain circuit, and an output, the first filter circuit being responsive to the first amplified system input signal received at its input for providing a first processed signal at its output. The first output gain circuit having a signal input coupled to the output of the first filter circuit for receiving the first processed signal, a gain control input and an output for providing a first amplified processed signal, the first output gain circuit being responsive to the first gain control signal received by its gain control input for amplifying the first processed signal received at its signal input by a third amplification factor to obtain the first amplified processed signal and responsive to a second gain control signal received by its gain control input for amplifying the first processed output signal received at its signal input by a fourth amplification factor to obtain the first amplified processed signal. The second input gain circuit having a signal input coupled to the system input for receiving the system input signal, a gain control input, an output control input, and an output for providing

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a second amplified system input signal, the second input gain circuit being responsive to the first gain control signal received by its gain control input for amplifying the system input signal by the first amplification factor to obtain the second amplified system input signal and being responsive to the second gain control signal received by its gain control input for amplifying the system input signal by the second amplification factor to obtain the second amplified system input signal, and the second input gain circuit being responsive to a first output control signal received by its output control input for providing the second amplified system input signal to its output and responsive to a second output control signal for causing its output to be an open circuit. The second filter circuit having an input coupled to the output of the second input gain circuit, and an output, the second signal processing circuit being responsive to the second amplified system input signal received by its input for providing a second processed signal at its output. The second output gain circuit having a signal input coupled to the output of the second filter circuit for receiving the second processed signal, a gain control input, a polarity control input, an output control input, and an output for providing one of an auxiliary output signal and ground, the second output gain circuit being responsive to a third gain control signal received by its gain control input for amplifying the second processed signal by a fifth amplification factor to obtain an amplified second processed signal, and being responsive to a fourth gain control signal received by its gain control input for amplifying the second processed signal by a sixth amplification factor to obtain the amplified second processed signal, the second output gain circuit being responsive to a first polarity gain control signal received by its polarity control input for inverting the amplified second processed signal to obtain the auxiliary output signal, and being responsive to a second polarity gain control signal received by its polarity control input for amplifying the amplified second processed signal by a unity gain to obtain the auxiliary output signal, the second output gain circuit being responsive to a first output control signal received by its output control input for connecting its output to ground, and being responsive to a second output control signal received by its output control input for providing the auxiliary output signal at its output. The signal adding circuit having a first input coupled to the output of the first output gain circuit, a second input coupled to the output of the second output gain circuit, and an output coupled to the system output, the signal adding circuit combining the first amplified

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processed signal provided by the output of the first output gain circuit, and one of the auxiliary output signal and ground provided by the output of the second output gain circuit to provide the system output signal at the output of the signal adding circuit.

According to another embodiment of the invention, there is provided an active filter system including a system input for receiving a system input signal, a system output for providing a system output signal, a first input gain circuit, a first filter circuit, a second input gain circuit, a second filter circuit, a signal adding circuit, a first output gain circuit. The first input gain circuit having a signal input coupled to the system input for receiving the system input signal, a gain control input and an output for providing a first amplified system input signal, the first input gain circuit being responsive to a first gain control signal received by the gain control input for amplifying the system input signal by a first amplification factor to obtain the first amplified system input signal and responsive to a second gain control signal received by the gain control input for amplifying the system input signal by a second amplification factor to obtain the first amplified system input signal. The first filter circuit having an input coupled to the output of the first input gain circuit and an output, the first filter circuit being responsive to a first amplified system input signal received at its input for providing a first processed signal at its output. The second input gain circuit having a signal input coupled to the system input for receiving the system input signal, a gain control input, an output control input and an output for providing a second amplified system input signal, the second input gain circuit being responsive to the first gain control signal received by its gain control input for amplifying the system input signal by the first amplification factor to obtain the second amplified system input signal and responsive to the second gain control signal received by its gain control input for amplifying the system input signal by the second amplification factor to obtain the second amplified system input signal, the second input gain circuit being responsive to a first output control signal received by its output control input for providing the second amplified system input signal to its output and responsive to a second output control signal for causing its output to be an open circuit. The second filter circuit having a signal input coupled to the output of the second input gain circuit, a gain control input and an output for providing a second amplified processed signal, the second filter circuit being responsive to the second amplified system input signal received by its input for providing a second processed

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signal, and being responsive to a third gain control signal received by its gain control input for amplifying the second processed signal by a fifth amplification factor to obtain the second amplified processed signal and being responsive to a fourth gain control signal received by its gain control input for amplifying the second processed signal by a sixth amplification factor to obtain the second amplified processed signal. The signal adding circuit having a first input coupled to the output of the first filter circuit, a second input coupled to the output of the second filter circuit and an output for providing a combined processed signal, the signal adding circuit combining the first processed output signal provided by the output of the first filter circuit and the second amplified processed signal provided by the output of the second filter circuit to provide the combined processed signal. The first output gain circuit having a signal input coupled to the output of the signal adding circuit, a gain control input and an output coupled to the system output, the first output gain circuit being responsive to the first gain control signal received by its gain control input for amplifying the combined processed signal received at its signal input by a third amplification factor to obtain the system output signal at its output and being responsive to a second gain control signal received by its gain control input for amplifying the combined processed signal received at its signal input by a fourth amplification factor to obtain the system output signal at its output.

According to another embodiment of the invention, there is provided a filter system including a system input for receiving a system input signal, a system output for providing a system output signal, a first input gain circuit, a first filter circuit, a second input gain circuit, a second filter circuit, a signal adding circuit, a first output gain circuit, and a signal switching circuit. The first input gain circuit having a signal input coupled to the system input for receiving the system input signal, a gain control input and an output for providing a first amplified system input signal, the first input gain circuit being responsive to a first gain control signal received by the gain control input for amplifying the system input signal by a first amplification factor to obtain the first amplified system input signal and responsive to a second gain control signal received by the gain control input for amplifying the system input signal by a second amplification factor to obtain the first amplified system input signal. The first filter circuit having an input coupled to the output of the first input gain circuit, a first output for providing a first processed signal, and a

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second output for providing a buffered first processed signal, the first filter circuit being responsive to a first amplified system input signal received at its input for providing the first processed signal at its first output, and for providing the buffered first processed signal at its second output. The second input gain circuit having a signal input coupled to the system input for receiving the system input signal, a gain control input, an output control input and an output for producing a second amplified system input signal, the second input gain circuit being responsive to the first gain control signal received by its gain control input for amplifying the system input signal by the first amplification factor to obtain the second amplified system input signal and being responsive to the second gain control signal received by its gain control input for amplifying the system input signal by the second amplification factor to obtain the second amplified system input signal, and the second input gain circuit being responsive to a first output control signal received by its output control input for providing the second amplified system input signal to its output and being responsive to a second output control signal received by its output control input for causing its output to be an open circuit. The second filter circuit having a signal input coupled to the output of the second input gain circuit, a gain control input and an output for providing a second amplified processed signal, the second filter circuit being responsive to the second amplified system input signal received by its input for providing a second processed signal, and being responsive to a third gain control signal received by its gain control input for amplifying the second processed signal by a fifth amplification factor to obtain the second amplified processed output signal and being responsive to a fourth gain control signal received by its gain control input for amplifying the second processed signal by a sixth amplification factor to obtain the second amplified processed output signal. The signal adding circuit having a first input coupled to the first output of the first filter circuit, a second input coupled to the output of the second filter circuit and an output for providing a combined processed signal, the signal adding circuit combining the first processed output signal provided by the output of the first filter circuit and the second amplified processed signal provided by the output of the second filter circuit to provide the combined processed signal. The first output gain circuit having a signal input coupled to the output of the signal adding circuit, a gain control input and an output for providing an amplified combined processed signal, the first output gain circuit being responsive to the first

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gain control signal received by its gain control input for amplifying the combined processed signal received at its signal input by a third amplification factor to obtain the amplified combined processed signal and being responsive to a second gain control signal received by its gain control input for amplifying the combined processed signal received at its signal input by a fourth amplification factor to obtain the amplified combined processed signal. The signal switching circuit having a first signal input coupled to the output of the first output gain circuit, a second signal input coupled to the second output of the first filter circuit, a switch control input and an output coupled to the system output, the signal switching circuit being responsive to receiving a first switching signal at the switch control input for providing the amplified combined processed signal received at the first signal input to the output, and being responsive to receiving a second switching signal at the switch control input for providing the buffered first processed output signal received at the second signal input to the output.

BRIEF DESCRIPTION OF THE DRAWINGS

Further objects, features, and advantages of the invention will become apparent from the following detailed description taken in conjunction with the accompanying figures showing illustrative embodiments of the invention, in which:

Fig. 1 is a block diagram illustrating a prior art signal processing system;

Fig. 2 is a block diagram illustrating a signal processing system in accordance with the present invention;

Fig. 3 is a circuit diagram illustrating a main filter input gain unit in accordance with the present invention;

Fig. 4 is a circuit diagram illustrating a main filter in accordance with the present invention;

Fig. 5 is a circuit diagram illustrating a main filter output gain unit in accordance with the present invention;

Fig. 6 is a circuit diagram illustrating an auxiliary filter input gain unit in accordance with the present invention;

Fig. 7 is a circuit diagram illustrating an auxiliary filter output gain unit in accordance with the present invention;

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Fig. 8 is a circuit diagram illustrating a signal adder in accordance with the present invention;

Fig. 9 is a block diagram illustrating a strength detector in accordance with the present invention;

Fig. 10 is a circuit diagram illustrating a peak detector in accordance with the present invention;

Fig. 11 is a circuit diagram illustrating a threshold detector in accordance with the present invention;

Fig. 12 is a circuit diagram illustrating a gain control unit in accordance with the present invention;

Fig. 13 is a circuit diagram illustrating a transconductor in accordance with the present invention;

Fig. 14 is a circuit diagram illustrating an on/off transconductor in accordance with the present invention;

Fig. 15 is a block diagram illustrating a signal processing system in accordance with the present invention;

Fig. 16 is a circuit diagram illustrating a modified auxiliary filter in accordance with the present invention;

Fig. 17 is a block diagram illustrating a signal processing system in accordance with the present invention;

Fig. 18 is a circuit diagram illustrating a multi-output main filter in accordance with the present invention;

Fig. 19 is a circuit diagram illustrating a comparison circuit in accordance with the present invention; and

Fig. 20 is a circuit diagram illustrating a switching unit in accordance with the present invention.

Throughout the figures, unless otherwise stated, the same reference numerals and characters are used to denote like features, elements, components, or portions of the illustrated embodiments. Moreover, while the subject invention will now be described in detail with reference to the figures, and in connection with the illustrative embodiments, various changes and modifications to the described embodiments will be apparent to those skilled in the art without departing from the true scope and spirit of the subject invention as defined by the appended claims.

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DETAILED DESCRIPTION OF THE INVENTION

Figure 1 illustrates an example of a prior art signal processing system 10. The signal processing system 10 is a companding filter. A companding filter amplifies or attenuates an input signal that is applied to a filter circuit, and attenuates or amplifies the output signal from the circuit. The prior art companding filter 10 includes an input 12, a signal strength detector 14, an input variable gain amplifier 16, a main filter 18, an output variable gain amplifier 20, and an output 22.

The input 12 of the signal processing system 10 is coupled to input 11 of the signal strength detector 14 and an input 30 of an input variable gain amplifier 16. The input variable gain amplifier 16 amplifies or attenuates the signal received by the input 30 depending on a gain control input signal received at a gain control input 13 of the input variable gain amplifier 16 and outputs the resultant signal at its output 15. The output 15 of the input variable gain amplifier 16 is coupled to input 17 of a main filter 18. The main filter 18 processes the signal received at its input 17 and produces a processed output signal at its output 19. The output 19 of the main filter 18 is coupled to input 21 of an output variable gain amplifier 20. The output variable gain amplifier 20 amplifies or attenuates the signal received at its input 21 depending on a gain control signal received at a gain control input 23 of the output variable gain amplifier 20 and outputs the resultant signal at its output 24. The gain of the output variable gain amplifier 20 is the inverse of the gain of the input variable gain amplifier 16. The output 24 of the output variable gain amplifier 20 is connected to the output 22 of the signal processing system 10.

The signal strength detector 14 measures the strength (e.g., the voltage envelope) of the signal applied to the input 11 of the signal strength detector 14 and outputs a gain control signal at its output 25, which is connected to the gain control inputs 13 and 23 of the input variable gain amplifier 16 and the output variable gain amplifier 20, respectively. Depending on the strength of the signal at the input 11 of the signal strength detector 14, different gain control signals are provided at the output 25 of the signal strength detector 14. If the signal applied to the input 11 of the signal strength detector 14 is small, the gain control signal causes the input variable gain amplifier 16 to have a relatively high gain, thereby causing the signal applied to the input 12 of the signal processing system 10 to be amplified before it is applied to the

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main filter 18, such that the signal is large compared to the filter noise, i.e. the noise generated by the filter. If the signal applied to the input 11 of the signal strength detector 14 is large, the gain control signal causes the input variable gain amplifier 16 to have a relatively low gain, thereby causing the signal applied to the input 12 of the signal processing system 10 to be slightly amplified or even attenuated before it is applied to the main filter 18 to avoid saturating the main filter 18.

Fig. 2 illustrates a signal processing system 100. The signal processing system 100 includes a system input 102, a main filter input gain unit 126, a main filter 132, a main filter output gain unit 138, an auxiliary filter input gain unit 106, an auxiliary filter 112, an auxiliary filter output gain unit 118, a signal adder 144, a system output 148, a strength detector 160, and a gain control unit 180. The signal processing system 100 generates a processed signal provided to the system output 148 with a strong in channel component well above the filter noise, which is not disturbed when internal states of the signal processing system 100 are changed. The signal processing system 100 accomplishes this by combining a signal processed by the auxiliary filter output gain unit 118 and a signal processed by the main filter output gain unit 138 whenever there is a change in an amplification factor of the main filter input gain unit 126 and an amplification factor of the main filter output gain unit 138. The signal processed by the auxiliary filter output gain unit 118 is combined with the signal processed by the main filter output gain unit 138 for a period of time at least as long as the amount of time it takes for transients in the signal processed by the main filter output gain unit 138 to die out. The transients in the signal processed by the auxiliary filter output gain unit 118 offset the transients in the signal processed by the main filter output gain unit 138. Therefore by combining the signal produced by the auxiliary filter output gain unit 118 with the signal produced by the main filter output gain unit 138, transients in the signal at the system output 148 of the signal processing system 100 are avoided when the amplification factor of the main filter input gain unit 126 and the amplification factor of the main filter output gain unit 138 are changed.

A signal received at system input 102 is applied to an input 124 of the main filter input gain unit 126 and an input 104 of the auxiliary filter input gain unit 106. The main filter input gain unit 126 amplifies the signal received at its input 124 as controlled by the signals received at its gain control inputs 156, 158. The main filter input gain unit 126 amplifies the signal received at its input 124 by one of three

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amplification factors. If the signal received at the input 158 represents a logical zero and the signal received at the input 156 represents a logical one, the main filter input gain unit 126 amplifies the signal received at the input 124 by a relatively large factor, here a factor of ten, and produces the amplified signal at its output 128. If the signal received at the input 158 represents a logical zero and the signal received at the input 156 represents a logical zero, the main filter input gain unit 126 amplifies the signal received at the input 124 by a relatively moderate factor, here a factor of one, and produces the amplified signal at its output 128. If the signal received at the input 158 represents a logical one and the signal received at the input 156 represents a logical zero, the main filter input gain unit 126 amplifies the signal received at the input 124 by a relatively small factor, here a factor of one tenth, and produces the amplified signal at its output 128. The output 128 of the main filter input gain unit 126 is coupled to an input 130 of the main filter 132 and an input 162 of the strength detector 160.

The main filter 132 processes the signal received at its input 130, which typically includes an in-band component and an out-band component, and outputs a processed signal at its output 134. Preferably, the main filter 132 has enough linear range to accommodate the in-band component and the out-band component of the signal without saturating. The output 134 of the main filter 132 is coupled to input 136 of the main filter output gain unit 138.

A signal received at an input 136 of the main filter output gain unit 138 is amplified under the control of the signals received at its gain control inputs 178, 179, 181. The main filter output gain unit 138 amplifies the signal received at its input 136 by one of three amplification factors. If the signal received at the input 178 represents a logical zero, the signal received at the input 179 represents a logical zero and the signal received at the input 181 represents a logical one, the main filter output gain unit 138 amplifies the signal received at the input 136 by a relatively small factor, here a factor of one tenth, and produces the amplified signal at its output 140. If the signal received at the input 178 represents a logical one, the signal received at the input 179 represents a logical zero, and the signal received at the input 181 represents a logical zero, the main filter input gain unit 138 amplifies the signal received at the input 136 by a relatively moderate factor, here a factor of one, and produces the amplified signal at its output 140. If the signal received at the input 178

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represents a logical zero, the signal received at the input 179 represents a logical one, and the signal received at the input 181 represents a logical zero, the main filter input gain unit 138 amplifies the signal received at the input 136 by a relatively large factor, here a factor of ten, and produces the amplified signal at its output 140. The output 140 of the main filter output gain unit 138 is coupled to an input 142 of the signal adder 144.

The auxiliary filter input gain unit 106 amplifies the signal received at its input 104 under the control of the signals received at its gain control inputs 150, 152, 154. The auxiliary filter input gain unit 106 amplifies the signal received at its input 104 by one of three amplification factors, and produces the amplified signal at its output 108. If the signal received at the input 154 represents a logical zero, the output 108 of the auxiliary filter input gain unit 106 provides an open circuit and the output 108 of the auxiliary filter input gain unit 106 is allowed to float. If the signal received at the input 154 represents a logical one, the signal received at the input 158 represents a logical zero and the signal received at the input 156 represents a logical one, the auxiliary filter input gain unit 106 amplifies the signal received at the input 104 by a relatively large factor, here a factor of ten, and produces the amplified signal at its output 108. If the signal received at the input 154 represents logical one, the signal received at the input 158 represents a logical zero and the signal received at the input 156 represents a logical zero, the auxiliary filter input gain unit 106 amplifies the signal received at its input 104 by a relatively moderate factor, here a factor of one, and produces the amplified signal at the output 108. If the signal received at the input 154 represents a logical one, the signal received at the input 158 represents a logical one and the signal received at the input 156 is a logical zero, the auxiliary filter input gain unit 106 amplifies the signal received at the input 104 by a relatively small factor, here a factor of one tenth, and produces the amplified processed signal at its output 108. The output 108 of the auxiliary filter input gain unit 106 is coupled to an input 110 of the auxiliary filter 112.

The auxiliary filter 112 processes the signal received at its input 110, which typically includes an in-band component and an out-band component, and outputs a processed signal at its output 114. Preferably, the auxiliary filter 112 has enough linear range to accommodate the in-band component and the out-band

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component of the signal without saturating. The output 114 of the auxiliary filter 112 is coupled to input 116 of the auxiliary filter output gain unit 118.

A signal received at an input 116 of the auxiliary filter output gain unit 118 is amplified under the control of signals received at gain control inputs 172, 173, 174, 175, 176. The auxiliary filter output gain unit 118 amplifies the signal received at its input 116 by one of three amplification factors, and provides the amplified signal to an output 120. If the signal received at the input 172 represents a logical one, the output 120 of the auxiliary filter output gain unit 106 is connected to ground. If the signal received at the input 172 represents a logical zero, the signal received at the input 173 represents a logical one, the signal received at the input 174 represents a logical zero, the signal received at the input 175 represents a logical zero and the signal received at the input 176 represents a logical one, the auxiliary filter input gain unit 118 amplifies the signal received at the input 116 by a relatively large positive amplification factor, here a factor of nine, and produces the amplified signal at its output 120. If the signal received at the input 172 represents a logical zero, the signal received at the input 173 represents a logical one, the signal received at the input 174 represents a logical zero, the signal received at the input 175 represents a logical one and the signal received at the input 176 represents a logical zero, the auxiliary filter input gain unit 118 amplifies the signal received at the input 116 by a relatively small positive amplification factor, here a factor of nine tenths, and produces the amplified signal at its output 120. If the signal received at the input 172 represents a logical zero, the signal received at the input 173 represents a logical zero, the signal received at the input 174 represents a logical one, the signal received at the input 175 represents a logical one and the signal received at the input 176 represents a logical zero, the auxiliary filter input gain unit 118 amplifies the signal received at the input 116 by a relatively large negative amplification factor, here a factor of minus nine tenths, and produces the amplified signal at its output 120. If the signal received at the input 172 represents a logical zero, the signal received at the input 173 represents a logical zero, the signal received at the input 174 represents a logical one, the signal received at the input 175 represents a logical zero and the signal received at the input 176 represents a logical one, the auxiliary filter input gain unit 118 amplifies the signal received at the input 116 by a relatively small negative factor, here a factor of

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minus nine, and produces the amplified signal at its output 120. The output 120 of the auxiliary filter output gain unit 118 is coupled to an input 122 of the signal adder 144.

The strength detector 160 measures the strength (e.g., the voltage envelope) of the signal applied to its input 162 and produces an up control signal at its output 166 and a down control signal at its output 164. Depending on the strength of the signal at its input 162, the strength detector 160 produces different signals at its two outputs 166, 164. If the signal applied to the input 162 of the strength detector 160 is below the noise floor threshold level of the main filter 132, which indicates that the amplification factor of the main filter input gain unit 126 should be increased, the strength detector 160 produces a logical one level signal on its output 166 and a logical zero level signal on its output 164. If the signal applied to the input 162 of the strength detector 160 is above the saturation threshold level of the main filter 132, which indicate that the amplification factor of the main filter input gain unit 126 should be decreased, the strength detector 160 produces a logical zero level signal on its output 166 and a logical one level signal on its output 164. If the signal applied to the input 162 of the strength detector 160 is above the noise floor threshold level and below the saturation threshold level of the main filter 132, which indicates that the amplification factor of the main filter input gain unit 126 should remain unchanged, the strength detector 160 produces a logical zero level signal on its output 166 and a logical zero level signal on its output 164. The outputs 166 and 164 are coupled to inputs 184 and 182, respectively, of the gain control unit 180.

The gain control unit 180, responsive to signals received at its inputs 182, 184, provides signals at its outputs 186, 188, 190, 192, 194, 195, 196, 197 to control the respective amplification factors of the main filter input gain unit 126, the main filter output gain unit 138, the auxiliary filter input gain unit 106 and the auxiliary filter output gain unit 118, as well as to selectively connect and disconnect the input 104 of the auxiliary filter input gain unit 106 to and from the system input 102, and to selectively connect and disconnect the output 120 of the auxiliary filter input gain unit 118 to and from the input 122 of the signal adder 144. The outputs 186 and 188 of the gain control unit 180 are connected to the inputs 156 and 158, respectively, of the main filter input gain unit 126. The outputs 186, 188 and 192, are connected to the inputs 150, 152 and 154, respectively, of the auxiliary filter input gain unit 106. The outputs 186, 188 and 190 are connected to the inputs 181, 179 and

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178, respectively, of the main filter output gain unit 138. The outputs 192, 194, 196, 197 and 195 are connected to the inputs 172, 173, 174, 175 and 176, respectively, of the auxiliary filter output gain 118.

The gain control unit 180 provides signals to the main filter input gain unit 126, the main filter output gain unit 138, the auxiliary filter input gain unit 106 and the auxiliary filter output gain unit 118 that allow their respective amplification factors to vary without causing transients to appear at the output 148 of the signal processing system 100. The gain control unit 180 begins the process of changing the amplification factors of the main filter input gain unit 126 and the main filter output gain unit 138 by providing the main filter input gain unit 126, the main filter output gain unit 138, the auxiliary filter input gain unit 106 and the auxiliary filter output gain unit 118 with the appropriate signals to change their respective amplification factors to desired values. At the same time, the gain control unit 180 provides an appropriate signal to the auxiliary filter input gain unit 106 to cause its input 104 to disconnect from the system input 102, and provides an appropriate signal to the auxiliary filter output gain unit 118 to connect its output 120 to the input 122 of the signal adder 144. The gain control unit 180 keeps the input 104 of the auxiliary filter input gain 106 disconnected from the system input 102 and keeps the output 120 of the auxiliary filter output gain unit 118 connected to the input 122 of the signal adder 144 for a period of time at least equal to the amount of time it takes for transients in the signal produced by the main filter output gain unit 138 caused by the change in its amplification factor to die out. Once that period of time has lapsed, the gain control unit 180 provides an appropriate signal to the auxiliary filter input gain 106 to cause its input 104 to connect to the system input 102, and provides an appropriate signal to the auxiliary filter output gain unit 118 to cause its output 120 to disconnect from the input 122 of the signal adder 144

The signal adder 144 combines the signals received at its inputs 122, 142 in the current domain and provides the combined signal at its output 146. The output 146 of the signal adder 144 is coupled to the output 148 of the signal processing system 100.

Fig. 3 illustrates an exemplary embodiment of the main filter input gain unit 126. The main filter input gain unit 126 amplifies the signal received at its input 124 by one of three amplification factors as controlled the gain control signals

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received by the inputs 156, 158. The main filter input gain unit 126 includes a first switch 312, a second switch 324, a first resistor 304, a second resistor 318, a transconductor 332 and an on/off transconductor 342. The first switch 312 and the second switch 324 may each be implemented as a CMOS transmission gate, in which an NMOS transistor and a PMOS transistor are connected in parallel with each other, the gate of the PMOS transistor is connected to the output of an inverter, the input of the inverter and the gate of the NMOS transistor are connected to each other and serve as the switch control terminal, and the source and drain of each transistor serve as the switch terminals. When a CMOS transmission gate is closed, the NMOS transistor and the PMOS transistor are active, such that a signal received on one terminal of the CMOS transmission gate is conveyed to the other terminal of the CMOS transmission gate. When a CMOS transmission gate is open, the NMOS transistor and the PMOS transistor are not active, such that a signal received on one terminal of the CMOS transmission gate is not conveyed to the other terminal of the CMOS transmission gate.

A signal received at gain control input 158 of the main filter input gain unit 126 is applied to an inverted switch control terminal 310 of the first switch 312 and one terminal 323 of the second switch 324; a signal received at the input 124 is applied to one terminal 302 of the first resistor 304 and terminal 308 of the first switch 312; and a signal received at gain control input 156 is applied to an on/off input 340 of the on/off transconductor 342, which is described in more detail in relation to Fig. 14. The first switch 312 closes to connect its terminal 308 to its other terminal 314 if the signal received at the inverted switch control terminal 310 is at a logical zero voltage level. If the signal at the inverted switch control terminal 310 is at a logical one voltage level, the first switch 312 opens to disconnect its terminal 308 from its other terminal 314 resulting in an open circuit between terminals 308 and 314. The first resistor 304 is connected between terminal 308 and terminal 314 of the first switch 312. The first resistor 304 may have a resistance of 90 kΩ. The terminal 314 of the first switch 312 and the other terminal 306 of the first resistor 304 are connected to one terminal 316 of the second resistor 318, a positive input 328 of the transconductor 332, and a positive input 336 of the on/off transconductor 342.

The other terminal 320 of the second resistor 318 is coupled to terminal 322 of the second switch 324. The second resistor 318 may have a resistance

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of 10 kΩ. Terminal 326 of the second switch 324 is connected to ground. The second switch 324 closes by connecting its terminal 322 to its other terminal 326 if the signal received at the switch control terminal 323 is at a logical one voltage level. If the signal at the switch control terminal 323 is at a logical zero voltage level, the second switch 324 opens by disconnecting its terminal 322 from its other terminal 326 resulting in an open circuit. The first switch 312 and the first resistor 304 form one half of a voltage divider, while the second switch 324 and the second resistor 318 form the other half of the voltage divider for the signal received at the input 124. The voltage divider causes the main amplifier gain unit to have a relatively small amplification factor when the signal applied to the gain control input 158 is at a logical or voltage level and the signal applied to the gain control input 156 is at a logical zero voltage level. A main filter input gain unit 126 having a relatively small amplification factor causes the signal process system to be effective for processing relatively large input signals.

The transconductor 332 operates on the difference between the signal received at its positive input 328 and the signal received at its negative input 330, which is connected to ground, and provides a signal at its output 334. The signal at the output 334 of the transconductor 332 is equal to the difference in the signal received by the positive input 328 of the transconductor 332 and the signal received by its negative input 330 scaled by a transconductance G_m of the transconductor 332. The output 334 of the transconductor 332 is coupled to the output 344 of the on/off transconductor 342, and the output 128 of the main filter input gain unit 126. When the first switch 312 is closed (as a result of a logical one voltage level signal applied to its switch control terminal 310), the switch 324 is open (as a result of a large logical zero voltage level signal applied to its switch control terminal terminal 323), and the on/off transconductor 342 is off (as a result of a logical zero voltage level signal received at its control input 340), the main filter input gain unit 126 has a relatively moderate amplification factor, and therefore the signal processing system 100 is effective for processing relatively moderate sized input signals.

If a logical one level voltage signal is received at the control terminal 340 of the on/off transconductor 342, the on/off transconductor 342 operates on the difference between the signal received at its positive input 336 and the signal received at its negative input 338, which is connected to ground, and provides a signal at its

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output 344. If the signal at its control input terminal 340 is at a logical zero voltage level, the on/off transconductor 342 acts as an open circuit between its input 336 and its output 344. If the signal at the control input terminal 340 is at a logical one voltage level, the signal at the output 344 of the on/off transconductor 342 is equal to the difference in the signal received by its positive input 336 and the signal received by its negative input 338 scaled by a transconductance $9G_m$ of the on/off transconductor 342. The output 344 of the on/off transconductor 342 is coupled to the output 334 of the transconductor 332 and to the output 128 of the main filter input gain unit 126. When the on/off transconductor 342 is on, i.e. when the signal at its control input 340 is at a logical one voltage level, the voltage output of the on/off transconductor 342 combines with the voltage output of the transconductor 332 causing the main filter input gain unit 129 to have a relatively large amplification factor, which in turn causes the signal processing system 129 to be effective for processing relatively small input signals.

Fig. 4 illustrates an exemplary embodiment of the main filter 132 which is in the form of a standard Tow-Thomas biquad. The main filter 132 includes a transconductor 412, a transconductor 420, a transconductor 428, a transconductor 442, a capacitor 404, and a capacitor 434. The center frequency ω_0 of the main filter 132 can be calculated by the equation:

$$\omega_0 = Q\, G_m / C \qquad (1)$$

where Q is the quality factor of the main filter 132. The absolute value of the transconductors and capacitors can be scaled by the same factor, i.e., impedance scaling, without affecting the transfer function of the main filter 132, since the transfer function depends on the ratios between these values. Impedance scaling does not change the transfer function of the main filter 132, however it does change the power dissipation and the noise level of the main filter 132.

A signal received by the input 130 of the main filter 132 is applied to a terminal 402 of the capacitor 404, a negative input 408 of the transconductor 412, an output 414 of the transconductor 412, a positive input 416 of the transconductor 420, and an output 430 of the transconductor 428. These connections form a node 450. The other terminal 406 of the capacitor 404 is connected to ground. The capacitor

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404 integrates the current signals provided to node 450 by the outputs of transconductors.

The transconductor 412 operates on the difference between the voltage signal received at a positive input 410, which is connected to ground and the voltage signal received at the negative input 408, and provides a current signal at its output 414. The signal at the current output 414 of the transconductor 412 is equal to the difference between the voltage signal received by its positive input 410, which is connected to ground, and the signal received by its negative input 408, which is the voltage at terminal 402 of the capacitor 404, scaled by its transconductance G_m. As explained above, the output 414 of the transconductor 412 together with one terminal 402 of the capacitor 404, the negative input 408 of the transconductor 412, the input 130, the positive input 416 of the transconductor 420 and the output 430 of the transconductor 428 form node 450. The transconductor 412 forms a feedback loop with the node 450.

The transconductor 420 operates on the difference between the voltage signal received at its positive input 416, which is the voltage at terminal 402 of the capacitor 404, and the voltage signal received at its negative input 418, which is connected to ground, and provides a current signal at its output 422. The current signal at the output 422 is equal to the difference between the voltage signal received by the positive input 416, which is node 450, and the voltage signal received by the negative input 418, scaled by a transconductance QG_m. The output 422 of the transconductor 420 together with one terminal 432 of a capacitor 434, a positive input 438 of the transconductor 442, and a negative input 424 of the transconductor 428 form node 451. The other terminal 436 of the capacitor 434 is connected to ground. The capacitor 434 integrates the current provided to node 451 by the output 422 of transconductor 420.

The transconductor 428 operates on the difference between the voltage signal received at its positive input 426, which is connected to ground and the voltage signal received at its negative input 424, which is voltage at terminal 432 of the capacitor 434, and provides a signal at its output 430 which is node 450. The current signal at the output 430, which is node 450, is equal to the difference in the signal received by the positive input 426 and the signal received by the negative input 424, which is node 451, of the transconductor 428, scaled by a transconductance QG_m.

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The transconductor 442 operates on the difference between the signal received at its positive input 438, which is the voltage at terminal 432 of the capacitor 434, and the voltage signal received at its negative input 440, which is connected to ground, and provides a current signal at an output 444. The signal at the output 444 is equal to the difference between the voltage signal received by the positive input 438, which is node 451, and the signal received by the negative input 440 of the transconductor 442, scaled by a transconductance G_m. The output 444 of the transconductor 442 is coupled to the output 134 of the main filter 132. In an exemplary embodiment of the main filter 132, the capacitance of the capacitors 404 and 434 are each 80v |. the quality factor, Q, is 20, and the transconductance G_m is 50.

In another exemplary embodiment of the main filter 132, a first diode (not shown) and a second diode (not shown) are connected to the node 450. The cathode of the first diode is connected to the node 450 and an anode of the first diode is connected to ground. The anode of the second diode is connected to the node 450 and a cathode of the second diode is connected to ground. This arrangement limits the voltage swing at the node 450 to approximately ± 0.7 volts.

In still another exemplary embodiment of the main filter 132, a first diode (not shown) and a second diode (not shown) are connected to the input 130. The cathode of the first diode is connected to the input 130 and an anode of the first diode is connected to ground. The anode of the second diode is connected to the input 130 and a cathode of the second diode is connected to ground. This arrangement limits the voltage swing at the input 130 to approximately ± 0.7 volts.

In yet another exemplary embodiment of the main filter 132, a first diode (not shown) and a second diode (not shown) are connected to the output 134. The cathode of the first diode is connected to the output 134 and an anode of the first diode is connected to ground. The anode of the second diode is connected to the output 134 and a cathode of the second diode is connected to ground. This arrangement limits the voltage swing at the output 134 to approximately ± 0.7 volts.

Fig. 5 illustrates an exemplary embodiment of the main filter output gain unit 138. The main filter output gain unit 138 provides a dynamically alterable output gain for the output of the main filter 132. The main filter output gain unit 138 includes a first switch 520, a second switch 532, a third switch 546, a first resistor

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512, a second resistor 526, a third resistor 538, and an operational amplifier 506. In the present embodiment, the operational amplifier 506 may be a model LF347 operational amplifier available from National Semiconductor Corporation in Santa Clara, California. Switches 520, 532 and 546 may each be implemented as a CMOS transmission gate.

A signal received at the input 136 of the main filter input gain unit 126 is applied to a negative input 502 of the operational amplifier 506, one terminal 510 of the first resistor 512, one terminal 524 of the second resistor 526 and one terminal 536 of the third resistor 538; a first gain control signal received at the input 181 is applied to a switch control terminal 518 of the first switch 520; a second gain control signal received at the input 178 is applied to a switch control terminal 531 of the second switch 532; and a third gain control signal received at the input 179 is applied to a switch control terminal 544 of the third switch 546. The other terminal 514 of the first resistor 512 is connected to one terminal 516 of the first switch 520. The first resistor 512 may have a relatively low resistance value. In the present example, the first resistor 512 has a value of $1/10G_m$, where G_m is in the transconductance of the transconductor 332 of the main filter input gain unit 126 depicted in Fig. 3. The other terminal 528 of the second resistor 526 is connected to one terminal 530 of the second switch 532. The second resistor 526 may have a relatively high resistance value. In the present example, the second resistor 526 has a value of $10/G_m$. The other terminal 540 of the third resistor 538 is connected to one terminal 542 of the third switch 546. The third resistor 538 may relatively moderate resistance value. In the present example, the third resistor 538 has a value of $1/G_m$.

Terminal 522 of the first switch 520 is connected to terminal 534 of the second switch 532, terminal 548 of the third switch 546, the output 508 of the operational amplifier 506, and the output 140 of the main filter output gain unit 138. The first switch 520 closes to connect its terminal 516 to its other terminal 522 if the signal received at the switch control terminal 518 is at a logical one voltage level. If the signal at the switch control terminal 518 of the first switch 520 is at a logical zero voltage level, the first switch 520 opens to disconnect its terminal 516 from its other terminal 522 resulting in an open circuit between the terminals.

Terminal 534 of the second switch 532 is connected to terminal 522 of the first switch 520, terminal 548 of the third switch 546, the output 508 of the

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operational amplifier 506, and the output 140 of the main filter output gain unit 138. The second switch 532 closes to connect its terminal 530 to its other terminal 534 if the signal received at the switch control terminal 531 of the second switch 532 is at a logical one voltage level. If the signal at the switch control terminal 531 is at a logical zero voltage level, the second switch 532 opens to disconnect its terminal 530 from its other terminal 534 resulting in an open circuit between the two terminals.

Terminal 548 of the third switch 546 is connected to terminal 522 of the first switch 520, terminal 534 of the second switch 532, the output 508 of the operational amplifier 506, and the output 140 of the main filter output gain unit 138. The third switch 546 closes to connect its terminal 542 to its other terminal 548 if the signal received at the switch control terminal 544 of the third switch 546 is at a logical one voltage level. If the signal at the switch control terminal 544 is at a logical zero voltage level, the second switch 546 opens to disconnect its terminal 542 from its other terminal 548 resulting in an open circuit between the two terminals.

The operational amplifier 506 amplifies the difference between the signal received at its positive input 504, which is connected to ground, and the signal received at its negative input 502 by an amplification factor and provides the amplified signal at its output 508. The signal produced at the output 508 is conveyed to the output 140 of the main filter output gain unit 138.

Fig. 6 illustrates an exemplary embodiment of the auxiliary filter input gain unit 106. The auxiliary filter input gain unit 106 amplifies the signal received at its input 104 by one of three amplification factors, and provides an appropriate amplified signal to its output 108. The auxiliary filter input gain unit 106 includes the main filter input gain unit 126, a first switch 614, and a second switch 622. Switches 614, 622 may each be implemented as a CMOS transmission gate.

A signal received at the input 104 of the auxiliary filter input gain unit 106 is applied to an input 602 of the main filter input gain unit 126; a signal received at the input 152 of the auxiliary filter input gain unit 106 is applied to an input 604 of the main filter input gain unit 126; a signal received at the input 150 of the auxiliary filter input gain unit 106 is applied to an input 606 of the main filter input gain unit 126; and a signal received at an input 154 is applied to an inverted switch control terminal 612 of the first switch 614 and a switch control terminal 620 of the second switch 622. The main filter input gain unit 126 amplifies the signal received at its

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input 602 by an amplification factor that depends on the signals received at its inputs 604, 606, as described above in relation to Fig. 3, and produces a signal at its output 608. The inputs 602, 604, 606 of the main filter input gain unit 126 correspond to the inputs 124, 158, 156, shown in Fig. 3, respectively, and the output 608 correspond to the output 128, shown in Fig. 3. The output 608 of the main filter input gain unit 126 is connected to a terminal 610 of the first switch 614, and a terminal 618 of the second switch 622.

One terminal 616 of the first switch 614 is connected to ground. The first switch 614 closes to connect its terminal 610 to its other terminal 616 if the signal received at the inverted switch control terminal 612 is at a logical zero voltage level. If the signal at the inverted switch control terminal 612 is at a logical one voltage level, the first switch 614 opens to disconnect its terminal 610 from its other terminal 616 resulting in an open circuit between the two terminals.

One terminal 624 of the second switch 622 is connected to the output 108 of the auxiliary filter input gain unit 106. The second switch 622 closes to connect its terminal 618 to its other terminal 624 if the signal received at its switch control terminal 620 is at a logical one voltage level. If the signal at the switch control terminal 620 is at a logical zero voltage level, the second switch 622 opens to disconnect its terminal 618 from its other terminal 624 resulting in an open circuit between the two terminals.

Fig. 21 illustrates an exemplary embodiment of the auxiliary filter 112. The auxiliary filter 112 includes the input 110, the main filter 132 and the output 114. A signal received by the input 110 of the auxiliary filter 112 is applied to the input 130 of the main filter 132. The structure and function of the main filter 132 is described above in relation to Fig. 3. The main filter 132 produces a processed signal at its output 134, which is connected to the output 114.

Fig. 7 illustrates an exemplary embodiment of the auxiliary filter output gain unit 118. The auxiliary filter output gain unit 118 provides a selectively enabled, dynamically alterable output gain for the auxiliary filter 106. The auxiliary filter output gain unit 118 includes a first operational amplifier 734, a second operational amplifier 762, a first resistor 704, a second resistor 718, a third resistor 748, a fourth resistor 754, a first switch 712, a second switch 726, a third switch 742, a fourth switch 770, and a fifth switch 778. In the present embodiment, the first

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operational amplifier 734 and the second operational amplifier 762 are model LF347 operational amplifiers available from National Semiconductor Corporation of Santa Clara, California. Switches 712, 726, 742, 770 and 778 may be each be implemented as CMOS transmission gates.

A signal received at the input 116 of the auxiliary filter output gain unit 118 is applied to a negative input 730 of the first operational amplifier 734, one terminal 702 of the first resistor 704, and one terminal 716 of the second resistor 718; a signal received at the input 175 of the auxiliary filter output gain unit 118 is applied to the switch control terminal 710 of the first switch 712; a signal received at the input 176 of the auxiliary filter output gain unit 118 is applied to the switch control terminal 724 of the second switch 726; a signal received at the input 173 of the auxiliary filter output gain unit 118 is applied to the switch control terminal 740 of the third switch 742; a signal received at the input 174 of the auxiliary filter output gain unit 118 is applied to the switch control terminal 768 of the fourth switch 770; and a signal received at the input 172 of the auxiliary filter output gain unit 118 is applied to the switch control terminal 776 of the fifth switch 778. The other terminal 706 of the first resistor 704 is connected to one terminal 708 of the first switch 712. The first resistor 704 has a relatively low resistance value. In the present example, the resistance of the first resistor 704 is $9/10G_m$ where G_m is the transconductance of transconductors 332 of the main filter input gain unit 126 depicted in Fig. 3. The other terminal 720 of the second resistor 718 is connected to one terminal 722 of the second switch 726. The second resistor 718 has a relatively high resistance value. In the present example, the resistance of the second resistor 718 is $9/G_m$.

Terminal 714 of the first switch 712 is connected to terminal 728 of the second switch 726, an output 736 of the first operational amplifier 734, one terminal 738 of the third switch 742, and one terminal 746 of the third resistor 748. The first switch 712 closes to connect its terminal 708 to its other terminal 714 if the signal received at its switch control terminal 710 is a logical one voltage level. If the signal at the switch control terminal 710 is at a logical zero voltage level, the first switch 712 opens to disconnect its terminal 708 from its other terminal 714 resulting in an open circuit between the two terminals.

Terminal 728 of the second switch 726 is connected to the terminal 714 of the first switch 712, the output 736 of the operational amplifier 734, terminal

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738 of the third switch 742, and one terminal 746 of the third resistor 748. The second switch 726 closes to connect its terminal 722 to its other terminal 728 if the signal received at its switch control terminal 724 is a logical one voltage level. If the signal at the switch control terminal 724 is at a logical zero voltage level, the second switch 726 opens to disconnect its terminal 722 from its other terminal 728 resulting in an open circuit between the two terminals.

The first resistor 704, the first switch 712, the second resistor 718, the second switch 726 and the operational amplifier 736 form an amplifier having a variable amplification factor. If input 175 receives a logical one voltage level signal and input 176 receives a logical zero level signal so that the first switch 712 is closed and the second switch 726 is open, the amplification factor between input 116 and the output 736 of the operational amplifier 734 is in the present example –9/10. If input 175 receives a logical zero voltage level signal and input 176 receives a logical one voltage level signal so that the first switch 712 is open and the second switch 726 is closed, the amplification factor between the input 116 and the output 736 of the operational amplifier 736 is –9.

Terminal 744 of the third switch 742 is connected to terminal 772 of the fourth switch 770, terminal 780 of the fifth switch 778, and the output 120 of the auxiliary filter output gain unit 118. The third switch 742 closes to connect its terminal 738 to its other terminal 744 if the signal received at its switch control terminal 740 is at a logical one voltage level. If the signal at the switch control terminal 740 is a logical zero voltage level, the third switch 742 opens to disconnect its terminal 738 from its other terminal 744 resulting in an open circuit between the two terminals.

The other terminal 750 of the third resistor 748 is connected to one terminal 752 of the fourth resistor 754, and the negative input 758 of the second operational amplifier 762. The third resistor 748, the fourth resistor 754, and the operational amplifier 762 form an inverting amplifier having an amplification factor serial to the negative ratio of the resistance of the fourth resistor 754 to the resistance of the third resistor 748. The inverting amplifier amplifies the signal received at terminal 746 of the third resistor 748 by such amplification factor and provides the amplified signal at its output 764. The signal produced at the output 764 is applied to terminal 766 of the fourth switch 770.

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The other terminal 772 of the fourth switch 770 is connected to terminal 744 of the third switch 742, the terminal 780 of the fifth switch 778 and the output 120 of the auxiliary filter output gain unit 118. The fourth switch 770 closes to connect its terminal 766 to its other terminal 772 if the signal received at its switch control terminal 768 is at a logical one voltage level. If the signal at the switch control terminal 768 is at a logical zero voltage level, the fourth switch 770 opens to disconnect its terminal 766 from its other terminal 772 resulting in an open circuit between the two terminals.

Terminal 774 of the fifth switch 778 is connected to ground. The other terminal 780 of the fifth switch 778 is connected to terminal 744 of the third switch 742, terminal 772 of the fifth switch 770, and the output 120 of the auxiliary filter output gain unit 118. The fifth switch 778 closes to connect its terminal 774 to its other terminal 780 if the signal received at its switch control terminal 776 is at a logical one voltage level. If the signal at the switch control terminal 776 is at a logical zero voltage level, the fifth switch 778 opens to disconnect its terminal 774 from its other terminal 780 resulting in an open circuit between the two terminals operation of the auxiliary filter output gain unit is not adequately described.

Fig. 8 illustrates an exemplary embodiment of the signal adder unit 144. The signal adder unit 144 combines the signals received at the input 122 and the input 142. The signal adder unit 144 includes an operational amplifier 824, a first resistor 804, a second resistor 810, and a third resistor 816. In the present embodiment, the operational amplifier 824 is model LF347 operational amplifier available from National Semiconductor Corporation of Santa Clara, California.

A signal received at the input 122 of the signal adder unit 144 is applied to one terminal 802 of the first resistor 804; a signal received at the input 142 of the signal adder unit 144 is applied to one terminal 808 of the second resistor 810. The other terminal 806 of the first resistor 804 is connected to the other terminal 812 of the second resistor 810, one terminal 814 of the third resistor 816 and the negative input 820 of the operational amplifier 824. The other terminal 818 of the third resistor 816 is connected to an output 826 of the operational amplifier 824 and the output 148 of the signal adder unit 144.

If the signal received at input 122 is V_P, the signal received at input 142 is V_Q and the signal at the output 148 is V_{ont}, then V_{ont} may be expressed as [EQ]

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where R_1 is the resistance of the first resistor 804, R_2 is the resistance of the second resistor 810 and R_F is the resistance of the third resistor 816.

Referring to Fig. 9, there is shown an exemplary embodiment of the strength detector 160 as shown in Fig. 2. The strength detector 160 includes an input 162, a peak detector 904, a first threshold detector 910, a second threshold detector 916, a first inverter gate 922, a second inverter gate 928, a third inverter gate 934, a first output 164, and a second output 166. The peak detector 904 and the first threshold detector 910 are described in more detail below in relation to Fig. 10 and Fig. 11, respectively. The strength detector 160 senses the voltage envelope of the signal received at the input 162, and decides whether it would be appropriate to change amplification factors of the main filter input gain unit 126, the main filter output gain unit 138, the auxiliary filter input gain unit 106 and the auxiliary filter output gain unit 118. The saturation threshold limit represents the input signal strength at which the main filter 132 approaches saturation. The noise floor threshold limit represents the input signal strength at which the output signal of the main filter 132 has a minimum acceptable signal-to-noise ratio.

A signal received at the input 162 of the strength detector 160 is applied to an input 902 of the peak detector 904. The peak detector 904 receives an input voltage signal at its input 902 and provides a current signal representative of the peak of the voltage envelope of the input signal at an output 906 of the peak detector 904. The output 906 of the peak detector 904 is coupled to an input 908 of the first threshold detector 910 and an input 914 of the second threshold detector 916. The first threshold detector 910 provides a logical one voltage level on its output 912 if the signal at its input 908 represents an input signal voltage envelope peak greater than the saturation threshold limit, and provides a logical zero voltage level on its output 912 if the signal at the input 908 represents an input signal voltage envelope peak less than the saturation threshold limit. The output 912 of the first threshold detector 910 is coupled to an input 920 of the first inverter gate 922. The second threshold detector 916 provides a logical one voltage level on its output 918 if the signal at its input 914 represents an input signal voltage envelope peak greater than the noise floor threshold limit, and provides a logical zero voltage level on its output 918 if the signal at its input 914 represents an input signal voltage envelope peak less than the noise floor

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threshold limit. The output 918 of the second threshold detector 916 is coupled to the input 932 of the third inverter gate 934.

The inverter gate 922 inverts the signal received at its input 920, and provides the inverted signal at its output 924. The output 924 is connected to the input 926 of the second inverter gate 928. The second inverter gate 928 inverts the signal received at its input 926, and provides the inverted signal at the output 930. The output 930 is couple, first to the output 164 of the strength detector 160. The third inverter gate 934 inverts the signal received at its input 932, and provides the inverted signal at its output 936. The output 936 is connected to the second output 166 of the strength detector 160.

Fig. 10 illustrates an exemplary embodiment of the peak detector 904 of the strength detector 160 of Fig. 9 in greater detail. The peak detector 904 includes an NMOS transistor Q_1, a PMOS transistor Q_3, an NMOS transistor Q_4, a PMOS transistor Q_5, a PMOS transistor Q_6, a capacitor 1050, a resistor 1058 and a transconductor 1042.

A signal received by the input 902 of the peak detector 904 is applied to a positive input 1044 of the transconductor 1042. The transconductor 1042 provide at its output 1048 a signal which is equal to the difference in the signal received by its positive input 1044 and the signal received by the negative input 1046, which is connected to ground, scaled by a transconductance G_{in} of the transconductor 1042. In the present embodiment the transconductor 1042 has a transconductance G_{in} of 1 microampere per volt. The signal provided at the output 1048 of the transconductor 1042 is applied to the gate 1010 of the PMOS transistor Q_3 and the gate 1024 of the NMOS transistor Q_4, which form an inverter, the gate 1026 and the drain 1032 of the diode connected PMOS transistor Q_5, the source 1036 and the backgate 1038 of the PMOS transistor Q_6, and the drain 1002 of the NMOS transistor Q_1. The inverter formed by the PMOS transistor Q_3 and the NMOS transistor Q_4 are connected between supply voltages V_{DD} and V_{SS}, and the commonly connected drains of PMOS transistor Q_3 and NMOS transistor Q_4 are connected to the source 1028 of diode connected PMOS transistor Q_5 and the gate 1034 of PMOS transistor Q_6. The back gates 1014 and 1020 of the PMOS transistor Q_3 and the NMOS transistor Q_4 are connected to supply voltage V_{DD} and V_{SS}, respectively. The commonly connected gate 1026 and drain 1032 of the diode connected PMOS transistor Q_5 are connected to

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the drain 1036 and backgate 1038 of PMOS transistor Q_6. The back gate 1030 of diode connected PMOS transistor is connected to supply voltage Q_{DD}. The source 1040 of the PMOS transistor Q_6 is connected to the gate 1048 of NMOS transistor Q_1, one terminal of capacitor 1050, one terminal 1056 of the resistor 1058 and output terminal 906. The other terminal of capacitor 1050 and the other terminal 1060 of the resistor 1058 are connected to supply voltage Q_{SS}. The drain 1002 of NMOS transistor Q_1 is connected to the output 1048 of the transconductor 1048 transconductor 1042, the drain 1036 and the backgate 1038 of PMOS transistor Q_6, the commonly connected gate 1026 and drain 1032 of diode connected PMOS transistor Q_5, and commonly connected gates 1010 and 1024 of the PMOS transistor Q_3 and the NMOS transistor Q_4 of the inverter. The source 1006 of the NMOS transistor Q_1 is connected to supply voltage Q_{SS}.

The NMOS transistor Q_1 of the peak detector 904 forms half of a NMOS current mirror. The other half of the current mirror consists of an NMOS transistor Q_2 of the threshold detector 910 (shown in Fig. 11). Thus, when the output 906 of the peak detector 904 is connected to the input 908 of the threshold detector 910, a complete NMOS current mirror is formed which acts as a current memory storing the peak current, *i.e.*, the current that represents the voltage envelope peak of input signal of the main filter. The CMOS inverter formed by PMOS transistor Q_3 and NMOS transistor Q_4 acts as a current comparator which compares the current provided by the output 1048 of the transconductor 1042 with the drain current of NMOS transistor Q_1.

When the drain current of NMOS transistor Q_1 is larger that the current provided by the output 1048 of the transconductor 1042, the commonly connected gates 1010 and 1024 of the PMOS transistor Q_3 and the NMOS transistor Q_4 forming the inverter is at a logical low voltage level (*i.e.*, V_{SS}) and the commonly connected drains 1016 and 1018 of those transistors are at a logical one voltage level (*i.e.*, V_{DD}). Because the gate 1034 of PMOS transistor Q_6 is connected to the commonly connected drains 1016 and 1018 of the inverter, it is also at the logical one voltage level, PMOS transistor Q_6 is turned off. If the current provided by the output 1048 of the transconductor 1042 becomes larger than the drain current of NMOS transistor Q_1, the commonly connected gates 1010 and 1024 of PMOS transistor Q_3 and NMOS transistor Q_4 switches to a logical one voltage level and the commonly connected

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drains 1016 and 1018 of those transistors switches to a logical zero voltage level; this causes the gate 1034 of the PMOS transistor Q_6 to go to the logical zero voltage level and PMOS transistor Q_6 to turn on. In this manner, PMOS transistor Q_6 connects the gates 1008 and 1102 (shown in Fig. 11) of NMOS transistors Q_1 and Q_2, one terminal 1052 of capacitor 1050 and terminal 1056 of the resistor 1058 to the output 1048 of the transconductor 1042, and the current mirror follows the current provided by the output 1048 of transconductor 1042. When the current provided by the output 1048 of the transconductor 1042 starts to fall below the new peak current, the commonly connected drains 1016 and 1018 of PMOS transistor Q_3 and NMOS transistor Q_4 switches back to a logical one voltage level causing PMOS transistor Q_6 to turn off leaving the gates 1008 and 1102 (shown in Fig. 11) of NMOS transistors at the voltage on the terminal 1052 of the capacitor 1050, thus allowing the NMOS current mirror to hold the new peak current, though the new peak current degrades as the capacitor 1050 discharges through the resistor 1058. Thereafter, the diode connected PMOS transistor Q_5 starts to supply the difference between the output of 1048 of the transconductor 1042 and the drain current provided by the current of the NMOS transistor Q_1 to the node formed by the output 1048 of the transconductor 1043, the drain of NMOS transistor Q_1 and the commonly connected gates 1010 and 1024 of PMOS transistor Q_3 and NMOS transistor Q_4.

Fig. 11 illustrates the first threshold detector 910 of the strength detector 160 of Fig. 9 in greater detail. The first threshold detector 910 compares the current representing of the voltage envelope of a signal received at the input 902 of the peak detector 904 to a reference current supplied by a current source 1126. The first threshold detector 910 includes an NMOS transistor Q_2, a PMOS transistor Q_7, a PMOS transistor Q_8, and the current source 1126. Any number of threshold detectors can be connected to the peak detector 904 to derive a corresponding number of signal strength detector outputs. A signal received by the input 908 of the first threshold detector 910 is applied to the gate 1102 of the NMOS transistor Q_2.

As explained above in connection with Fig. 10, the NMOS transistor Q_2 of the first threshold detector 910 forms half of an NMOS current mirror that acts as a current memory which stores the peak current corresponding to the peak voltage envelope of the signal received at the input 902 of the peak detector 904. The other half of the NMOS current mirror that acts as a current memory consists of the NMOS

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transistor Q_1 of the peak detector 904, shown in Fig. 10, which is connected to the input 908 of the first threshold detector 910. The source 1108 of the NMOS transistor Q_2 is connected to supply voltage V_{ss}. The drain 1104 of the NMOS transistor Q_2 is connected to the drain 1110 of the PMOS transistor Q_7. The gate 1102 of the NMOS transistor Q_2 is connected to the input 908 of the first threshold detector 910. The backgate 1106 of the NMOS transistor Q_2 is connected to supply voltage V_{ss}.

The NMOS transistor Q_7, the NMOS transistor Q_8 and the current source 1126 form a current mirror that causes a current to flow through the NMOS transistor Q_7 that mirrors the current of the current source 1126. The gate 1114 of the NMOS transistor Q_7 is connected to the gate 1118 of the NMOS transistor Q_8, the drain 1120 of the NMOS transistor Q_8, and the positive terminal 1122 of the current source 1126. The source 1112 of the NMOS transistor Q_7 is connected to supply voltage V_{dd} and the source 1116 of the NMOS transistor Q_8. The drain 1110 of the NMOS transistor Q_7 is connected to the drain 1104 of the NMOS transistor Q_2 and the output 912 of the threshold detector 910. The gate 1118 of NMOS transistor Q_8 is connected to the drain 1120 of the NMOS transistor Q_8 , the gate 1114 of the NMOS transistor Q_7 and the positive terminal 1122 of the current source 1126. The source 1116 of the NMOS transistor Q_8 is connected to the source 1112 of the NMOS transistor Q_7 and supply voltage V_{dd}. The negative terminal 1124 of the current source 1126 is connected to ground.

The current source 1126 produces a reference current that represents the threshold voltage of the first threshold detector 910. The reference current can be any value, for example 100 uA, and the transistors Q_7, Q_8 of the first threshold detector 910 are scaled to cause the desired current to flow through the transistor Q_7. The preferred form of a current source is a resistance connected between the drain 1120 of NMOS transistor Q_8 and ground. In the present example the reference current generated by the current source in the first threshold detector 910 is 5.5 MA.

The output 912 of the first threshold detector 910 indicates whether the respective amplification factors of the main filter input gain unit 126 and the auxiliary filter input gain unit 106 should be decreased given the voltage envelope of the signal received at the input 902 of the peak detector 904. If the current flowing through the transistor Q_2, which represents the voltage envelope peak of the signal received at the input 902 of the peak detector 904, exceeds the current flowing through the transistor

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Q_7, which is related to the reference current of the current source 1126, the output 912 of the first threshold detector 910 will be at a logical zero voltage level. If the current flowing through the transistor Q_2 does not exceed the current flowing through the transistor Q_7, the output 912 of the first threshold detector 910 will be at a logical one voltage level. In this manner, the saturation threshold limit of the signal strength detector 160 is represented by the amount of current generated by the current source 1126.

In an exemplary embodiment the second threshold detector 916 (not shown in Fig. 11) is similar to the first threshold detector 910 shown in Fig. 11. It has a counterpart to NMOS transistor Q_2 of the first threshold detector 910, with the gate of the counterpart transistor connected to the output 906 of the peak detector 904. The second threshold detector 916 also has its counterpart to the current mirror, which in the first threshold detector 910 consists of NMOS transistors Q_7 and Q_8, and reference current source 1126. The counterpart to the current source 1126 of the second threshold detector 916 would produce a reference current that represents the noise floor threshold limit. In the present example, the counterpart to the current source 1126 generates 55 micro-amperes.

Fig. 12 illustrates an exemplary embodiment of the gain control unit 180 of the block diagram of Fig. 2 in more detail. The gain control unit 180 controls the gain of the auxiliary filter input gain unit 106, the auxiliary filter output gain unit 118, the main filter input gain unit 126, and the main filter output gain unit 138. The gain control unit 180 is implemented with AND gates, OR gates, a positive edge triggered D-type flip flop 1209, a positive edge triggered D-type flip flop 1219, a positive edge triggered D-type flip flop 1229 and an N-bit counter 1268. The gain control unit 180 receives control signals at inputs 164, 166, which are applied to an array of AND gates, and a clock signal at the input 1201, which is conveyed to clock inputs 1208, 1218 and 1228 of the positive edge triggered D-type flip flops 1209, 1219 and 1229, respectively, and clock input 1266 of the N-bit counter 1268.

The N-bit counter 1268 receives a signal at an enable/reset input 1264, and a signal at a clock input 1266, and provides an output at the counter overflow output 1270. If the signal received at the input 1264 is a logical one, the N-bit counter 1268 increments on the positive edge of each clock cycle, and the signal produced at the counter overflow output 1270 is a logical zero, until it gets to a specified

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maximum value. On the clock cycle after the N-bit counter 1268 reaches its specified maximum value, the signal produced at the counter overflow output 1270 is a logical one.

If the signal received at the input 1264 is a logical zero, the N-bit counter 1268 is reset to a predetermined state, and the signal produced at the counter overflow output 1270 is a logical zero. In the exemplary embodiment, the predetermined state is selected such that once the signal received at the enable/reset input 1264 changes from a logical zero to a logical one, the counter overflow output 1270 will not change to a logical one until a time required for the largest possible transient on the outpost of the main filter die out has passed.

A four input AND gate 1202 receives the inverse of a signal from the data output 1210 of the positive edge triggered D-type flip flop 1209, a signal from the data output 1220 of the positive edge triggered D-type flip flop 1219, a signal from the data output 1230 of the positive edge triggered D-type flip flop 1229 and a signal from the counter overflow output 1270 of the counter 1268. The output of the four input AND gate 1202 is provided to a one input of a two input OR gate 1206. A four input AND gate 1204 receives a signal from a data output 1210 of the positive edge triggered D-type flip flop 1209, the inverse of a signal from the data output 1220 of the positive edge triggered D-type flip flop 1219, the inverse of a signal from the data output 1230 of the positive edge triggered D-type flip flop 1229, and a signal received by the input 164. The output of the four input AND gate 1204 is provided to its other input of the two input OR gate 1206. The output of the two input OR gate 1206 is provided to the data input 1207 of the positive edge triggered D-type flip flop 1209.

A four input AND gate 1212 receives the inverse of a signal from a data output 1210 of the positive edge triggered D-type flip flop 1209, the inverse of a signal from the data output 1220 of the positive edge triggered D-type flip flop 1219, a signal from the data output 1230 of the positive edge triggered D-type flip flop 1229, and a signal from the counter overflow output 1270 of the counter 1268. The output of the four input AND gate 1212 is provided to one input of a three input OR gate 1216. A four input AND gate 1214 receives the inverse of a signal from a data output 1210 of the positive edge triggered D-type flip flop 1209, a signal from the data output 1220 of the positive edge triggered D-type flip flop 1219, the inverse of a

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signal from the data output 1230 of the positive edge triggered D-type flip flop 1229 and a signal received by the input 166. The output of the four input AND gate 1214 is provided to another input of the three input OR gate 1216. A four input AND gate 1215 receives a signal from a data output 1210 of the positive edge triggered D-type flip flop 1209, the inverse of a signal from the data output 1220 of the positive edge triggered D-type flip flop 1219, a signal from the data output 1230 of the positive edge triggered D-type flip flop 1229, and a signal from the counter overflow output 1270 of the counter 1268. The output of the four input AND gate 1215 is provided to the remaining input of the three input OR gate 1216. The three input OR gate 1216 provides its output to the data input 1217 of the positive edge triggered D-type flip flop 1219.

A four input AND gate 1222 receives the inverse of a signal from a data output 1210 of the positive edge triggered D-type flip flop 1209, the inverse of a signal from the data output 1220 of the positive edge triggered D-type flip flop 1219, the inverse of a signal from the data output 1230 of the positive edge triggered D-type flip flop 1229, and a signal received by the input 166. The output of the four input AND gate 1222 is provided to one input of a three input OR gate 1226. A four input AND gate 1224 receives the inverse of a signal from a data output 1210 of the positive edge triggered D-type flip flop 1209, a signal from the data output 1220 of the positive edge triggered D-type flip flop 1219, the inverse of a signal from the data output 1230 of the positive edge triggered D-type flip flop 1229, and a signal received by the input 166. The output of the four input AND gate 1224 is provided to another input of the three input OR gate 1226. A four input AND gate 1225 receives a signal from a data output 1210 of the positive edge triggered D-type flip flop 1209, the inverse of a signal from the data output 1220 of the positive edge triggered D-type flip flop 1219, the inverse of a signal from the data output 1230 of the positive edge triggered D-type flip flop 1229, and a signal received by the input 164. The output of the four input AND gate 1225 is provided to the remaining input of the three input OR gate 1226. The three input OR gate 1226 provides its output to the data input 1227 of the positive edge triggered D-type flip flop 1229.

The first D-type flip-flop 1209 holds the most significant bit of the current state of the gain control unit 180 until the next positive edge of the clock signal received at the clock input 1201 of the gain control unit 180, at which time the

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most significant bit of the current state is provided at the output 1210 of flip-flop 1209. The second D-type flip-flop 1219 holds the second most significant bit of the current state of the gain control unit 180 until the next positive edge of the clock signal received at the clock input 1201 of the gain control unit 180, at which time the second most significant bit of the current state is provided at the output 1220 of flip-flop 1219. The third D-type flip-flop 1229 holds the least significant bit of the current state of the gain control unit 180 until the next positive edge of the clock signal received at the clock input 1201 of the gain control unit 180, at which time the least significant bit of the current state is provided at the output 1230 of flip-flop 1229.

A three input AND gate 1232 receives the inverse of a signal from the data output 1210 of the positive edge triggered D-type flip flop 1209, the inverse of a signal from the data output 1220 of the positive edge triggered D-type flip flop 1219, and the inverse of a signal from the data output 1230 of the positive edge triggered D-type flip flop 1229. The output of the three input AND gate 1232 is provided to one respective input of a two input OR gate 1246 and to one input of a three input OR gate 1252. A three input AND gate 1234 receives the inverse of a signal from the data output 1210 of the positive edge triggered D-type flip flop 1209, the inverse of a signal from the data output 1220 of the positive edge triggered D-type flip flop 1219 and a signal from the data output 1230 of the positive edge triggered D-type flip flop 1229. The output of the three input AND gate 1234 is provided to one respective input of a three input OR gate 1248 one input of a two input OR gate 1256, one input of a two input OR gate 1258, one input of a two input NOR gate 1260 and a first input of a four input OR gate 1262. A three input AND gate 1236 receives the inverse of a signal from the data output 1210 of the positive edge triggered D-type flip flop 1209, a signal from the data output 1220 of the positive edge triggered D-type flip flop 1219 and the inverse of a signal from the data output 1230 of the positive edge triggered D-type flip flop 1229. The output of the three input AND gate 1236 is provided to another input of the three input OR gate 1248, and another input of the three input OR gate 1252. A three input AND gate 1238 receives the inverse of a signal from the data output 1210 of the positive edge triggered D-type flip flop 1209, a signal from the data output 1220 of the positive edge triggered D-type flip flop 1219 and a signal from the data output 1230 of the positive edge triggered D-type flip flop 1229. The output of the three input AND gate 1238 is provided to one input of a two input OR

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gate 1250, the other input of the two input OR gate 1256 and a second input of the four input OR gate 1262. A three input AND gate 1240 receives a signal from the data output 1210 of the positive edge triggered D-type flip flop 1209, the inverse of a signal from the data output 1220 of the positive edge triggered D-type flip flop 1219, and the inverse of a signal from the data output 1230 of the positive edge triggered D-type flip flop 1229. The output of the three input AND gate 1240 is provided to the other input of the two input OR gate 1250 and the remaining input of the three input OR gate 1252. A three input AND gate 1242 receives a signal from the data output 1210 of the positive edge triggered D-type flip flop 1209, the inverse of a signal from the data output 1220 of the positive edge triggered D-type flip flop 1219 and a signal from the data output 1230 of the positive edge triggered D-type flip flop 1229, the output of the three input AND gate 1242 is provided to the remaining input of the three input OR gate 1248, one input of a two input OR gate 1254 and a third input of the four input OR gate 1262. A three input AND gate 1244 receives a signal from the data output 1210 of the positive edge triggered D-type flip flop 1209, a signal from the data output 1220 of the positive edge triggered D-type flip flop 1219 and the inverse of a signal from the data output 1230 of the positive edge triggered D-type flip flop 1229. The output of the three input AND gate 1244 is provided to the other input of the two input OR gate 1246, the other input of the two input OR gate 1254, the other input of the two input OR gate 1258, the other input of the two input NOR gate 1260 and a fourth input of the four input OR gate 1262.

The two input OR gate 1246 provides its output to an output terminal 186 The three input OR gate 1248 provides its output to output terminal 190. The two input OR gate 1250 provides its output to output terminal 188. The three input OR gate 1252 provides its output to output terminal 192. The two input OR gate 1254 provides its output to output terminal 194. The two input OR gate 1256 provides its output to output terminal 196. The two input OR gate 1258 provides its output to output terminal 197. The two input NOR gate 1260 provides its output to output terminal 195. The four input OR gate 1262 provides its output to the input 1264 of the counter 1268.

Fig. 13 illustrates an exemplary embodiment of the transconductor 332 in the main filter input gain unit 126 depicted in Fig. 3 in greater detail. The transconductors 412, 420, 428 and 442 used in the Tow-Thomas biquad 132 depicted

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in Fig. 4, and 1042 used in peak detection 904 depicted in Fig. 10 are similar in construction. The transconductor 332 includes an NMOS transistor Q_1, an NMOS transistor Q_2, a PMOS transistor Q_3, a PMOS transistor Q_4, an NMOS transistor Q_5, an NMOS transistor Q_6, and a current source 1324.

A signal received by the positive input 328 of the transconductor 332 is applied to the gate 1305 of the NMOS transistor Q_1. The NMOS transistor Q_1 allows current to flow from its source 1307 to its drain 1306, or vice versa, depending on the signal at the gate 1305 and the relative voltages at its source 1307 and at its drain 1306. The drain 1306 of the NMOS transistor Q_1 is connected to the drain 1313 and the gate 1311 of the PMOS transistor Q_3, and the gate 1314 of the PMOS transistor Q_4. The source 1307 of the NMOS transistor Q_1 is connected to the drain 1318 of the NMOS transistor Q_5 and the source 1310 of the NMOS transistor Q_2.

A signal received by the negative input 330 of the transconductor 332 is applied to the gate 1308 of the NMOS transistor Q_2. The drain 1309 of the NMOS transistor Q_2 is connected to the drain 1316 of the PMOS transistor Q_4 and the output 334 of the transconductor 332. The source 1310 of the NMOS transistor Q_2 is connected to the drain 1318 of the NMOS transistor Q_5, and the source 1307 of the NMOS transistor Q_1.

The drain 1313 of the PMOS transistor Q_3 is connected to the drain 1306 of the NMOS transistor Q_1, the gate 1311 of the PMOS transistor Q_3, and the gate 1314 of the PMOS transistor Q_4. The source 1312 of the PMOS transistor Q_3 is connected to supply voltage V_{dd}.

The source 1315 of the PMOS transistor Q_4 is connected to supply voltage V_{dd}.

The drain 1318 of the NMOS transistor Q_5 is connected to the source 1307 of the NMOS transistor Q_1 and the source 1310 of the NMOS transistor Q_2. The source 1319 of the NMOS transistor Q_5 is connected to supply voltage V_{ss}. The gate 1317 of the NMOS transistor Q_5 is connected to the gate 1320 and the drain 1321 of the NMOS transistor Q_6, and the negative terminal 1325 of the current source 1324.

The source 1322 of the NMOS transistor Q_6 is connected to supply voltage V_{ss}.

The current source 1324 produces a bias current I_{bias} for the transconductor 332. The bias current I_{bias} produced by the current source 1324

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controls the center frequency of the filter. The bias current I_{bias} of the transconductor 332 is adjusted to give a stable center frequency in the presence of fabrication tolerances and temperature variations. The bias current I_{bias} can be any value, for example 100 micro-amperes, and the transistors Q_1, Q_2, Q_3, Q_4, Q_5, Q_6 of the transconductor 332 are scaled to yield the desired transconductances. The transconductance for the transconductors is calculated using the equation:

$$G_m = I_{tail} / (V_{GS} - V_T), \quad (3)$$

where I_{tail} is the current passing through the transistor Q_5, V_T is the threshold voltage of transistors Q_5 and Q_6, and V_{GS} is the gate-source voltage of the transistors Q_5, Q_6. The linear range of the transconductor is related to the quantity $V_{GS} - V_T$. Once the bias current I_{bias} has been set, the transistors Q_5, Q_6 are scaled such that, the following equation is satisfied:

$$(W_{Q5} / L_{Q5}) / (W_{Q6} / L_{Q6}) = I_{tail} / I_{bias}, \quad (4)$$

where W_{Q5} and L_{Q5} are the width and length of the channel of NMOS transistor Q_5, respectively, and W_{Q6} and L_{Q6} are the width and length of the channel of NMOS transistor Q_6, respectively. The positive terminal of the current source 1324 is connected to supply voltage V_{dd}. The preferred form of the current source 1324 is a resistor connected to the between the supply voltage V_{dd} and the drain 1321 and the gate 1320 of the NMOS transistor Q_6. Each transconductor of the signal processing system 100 may have the configuration of the transconductor 332.

Referring to Fig. 14, there is shown an exemplary on/off transconductor 342. The on/off transconductor 342 is identical to the transconductor 332 shown in Fig. 13, except for the addition of a PMOS transistor Q_7 and an NMOS transistor Q_8. The PMOS transistor Q_7 is connected between the gate 1317 of the NMOS transistor Q_5 and ground. The NMOS transistor Q_8 connected in series between the gate 1320 of the NMOS transistor Q_6 and the gate 1317 of the NMOS transistor Q_5. The gate 1404 of NMOS transistor Q8 and the gate 1405 of the PMOS transistor are both connected to the on/off input 340 of the on/off transconductor 342. If the PMOS transistor Q_7 is turned off and the NMOS transistor Q_8 is turned on by the application of a logical one voltage level to their respective gate terminals 1404

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and 1405 via the on/off input 340, the on/off transconductor 342 operates in essentially the same manner as the transconductor 332 shown in Fig. 13. However, if the PMOS transistor Q_7 is turned on and the NMOS transistor Q_8 is turned off by the application of a logical zero voltage to the gate terminal 1404, the on/off transconductor 342 is disabled and the output 344 of the on/off transconductor 342 acts as an open circuit.

Referring now to Fig. 2, if the successive amplification factors of the main filter input gain unit 126, the main filter output gain unit 138, the auxiliary filter input gain unit 106, and the auxiliary filter output gain unit 118 of the signal processing system have a constant ratio to one another (i.e. if the main filter input gain unit 106 has amplification factors of 10, 1 and 1/10), the signal processing system 100 may be simplified. Signal processing system 1500 shown in Fig. 15 is one such system. In the signal processing system 100 of Fig. 2 the auxiliary filter output gain unit 118 amplifies a signal produced by the auxiliary filter 112 and produces an output signal which is combined with the signal produced by the main filter output gain unit 138 which amplifies a signal produced by the main filter 132. If the successive amplification factors have a constant ratio, the signals produced by the main filter 132 and the auxiliary filter 112 are amplified by common factors and the signal from the auxiliary filter 112 is scaled by some additional factors. In the signal processing system 1500 of Fig. 15, the signals produced by the modified auxiliary filter 1510 and the main filter 132 are amplified by the main filter output gain unit 138, and the modified auxiliary filter 1510 internally amplifies the processed signal by various amplification factors. The main filter output gain unit 138 is moved from its location in the signal processing system 100 from between the main filter 132 and the signal adder 144, as shown in Fig. 2, to between the signal adder 144 and the system output 1514, as shown in Fig. 15. Moving the main filter output gain unit 138 causes it to amplify the signal produced by the modified auxiliary filter 1510 and the signal produced by the main filter 132. This simplified signal processing system 1500 is illustrated in Fig. 15.

Referring to Fig. 15, the signal processing system 1500 includes a system input 1502, a main filter input gain unit 126, a main filter 132, a main filter output gain unit 138, an auxiliary filter input gain unit 106, a modified auxiliary filter 1510, a signal adder 144, a system output 1514, a strength detector 160, and a gain

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control unit 180. The signal processing system 1500 generates a processed signal provided to the system output 1514 with a strong in channel component well above the filter noise, which is not disturbed when internal states of the signal processing system 1500 are changed. The signal processing system 1500 accomplishes this in a manner similar to the signal processing system 100. The signal processing system 1500 combines a signal processed by the modified auxiliary filter 1510 and a signal processed by the main filter 132 whenever there is a change in an amplification factor of the main filter input gain unit 126 and a change in an amplification factor of the main filter output gain unit 138. The signal processed by the modified auxiliary filter 1510 is combined with the signal processed by the main filter 132 for a period of time at least as long as the amount of time it takes for transients in the signal processed by the main filter 132 to die out. The transients in the signal processed by the modified auxiliary filter 1510 offset the transients in the signal processed by the main filter 132. Therefore by combining the signal produced by the modified auxiliary filter 1510 with the signal produced by the main filter 132, transients in the signal at the system output 1514 of the signal processing system 1500 are avoided when the amplification factor of the main filter input gain unit 126 and the amplification factor of the main filter output gain unit 138 are changed.

A signal received at system input 1502 is applied to an input 124 of the main filter input gain unit 126, as described above in relation to Figs. 2 and 3, and an input 104 of the auxiliary filter input gain unit 106, described above in relation to Figs. 2 and 6. The output 128 of the main filter input gain unit 126 is coupled to an input 130 of the main filter 132, as described above in relation to Figs. 2 and 4, and an input 162 of the strength detector 160, as described above in relation to Figs. 2, 9, 10 and 11. The output 134 of the main filter 132 is connected to the input 142 of the signal adder 144, as described above in relation to Figs. 2 and 8.

The output 108 of the auxiliary filter input gain unit 106 is connected to an input 1504 of the modified auxiliary filter 1510. The modified auxiliary filter 1510 incorporates the functionality of the auxiliary filter 112 and some of the functionality of the auxiliary filter output gain unit 118. The modified auxiliary filter 1510 processes the signal in the same manner as the auxiliary filter 112, described above with reference to Figs. 2 and 4, and it amplifies the processed signal by one of two amplification factors. The modified auxiliary filter 1510 will be discussed in

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more detail below with reference to Fig. 16. An output 1512 of the modified auxiliary filter 1510 is connected to the input 122 of the signal adder 144, as described above in relation to Figs. 2 and 8. The output 146 of the signal adder 144 is connected to the input 136 of the main filter output gain unit 138, as described above in relation to Figs. 2 and 5. The output 140 of the main filter output gain unit 138 is connected to the system output 1514.

The outputs 164, 166 of the strength detector 160 are connected to the inputs 182, 184, respectively, of the gain control unit 180, as described above in relation to Figs. 2 and 12. The outputs 186, 188 of the gain control unit 180 are connected to the inputs 156, 158, respectively, of the main filter input gain unit 126. The outputs 186, 188, 192 of the gain control unit 180 are connected to the inputs 150, 152, 154, respectively, of the auxiliary filter input gain unit 106. The outputs 194, 196 of the gain control unit 180 are connected to the inputs 1506, 1508, respectively, of the modified auxiliary filter 1510. And the outputs 186, 188, 190 of the gain control unit 180 are connected to the inputs 181, 179, 178, respectively, of the main filter output gain unit 138.

Fig. 16 illustrates an exemplary embodiment of the modified auxiliary filter 1510 which is in the form of a modified standard Tow-Thomas biquad. The standard Tow-Thomas biquad is modified to incorporate output amplification. The modified auxiliary filter 1510 includes an input 1504, a gain control input 1506, a gain control input 1508, a signal output 1512, a transconductor 1612, a transconductor 1620, a transconductor 1628, a transconductor 1642, a transconductor 1655, a capacitor 1604, a capacitor 1634, a switch 1662, a switch 1670, a switch 1678, and a switch 1686. Switches 1662, 1670, 1678 and 1686 may be implemented as CMOS transmission gates. The center frequency ω_0 of the modified auxiliary filter 1510 can be calculated by the equation:

$$\omega_0 = Q\, G_m / C \qquad (1)$$

where Q is the quality factor of the modified auxiliary filter 1510 and G_m is the transconductance of transconductor 1612. The absolute values of the transconductances and capacitances of the modified auxiliary filter 1310 can be scaled by the same factor, i.e., impedance scaling, without affecting the transfer function of the modified auxiliary filter 1510, since the transfer function depends on the ratios of

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these values. Impedance scaling does not change the transfer function of the modified auxiliary filter 1510; however, it does change the power dissipation and the noise level of the modified auxiliary filter 1510. In addition to filtering the signal received at the input 1504, the modified auxiliary filter 1510 amplifies the signal according to the signals received at the inputs 1506, 1508. If the input 1506 receives a logical zero voltage level signal and the input 1508 receives a logical zero voltage level signal, which cause switches 1662 and 1672 to both open, and switches 1670 and 1686 to both close, the output 1512 of the auxiliary filter is an open circuit, and therefore the modified auxiliary filter 1510 does not contribute anything to the output signal produced at the system output 1514. If the input 1506 receives a logical one voltage level signal and the input 1508 receives a logical zero voltage level signal, which causes switches 1662 and 1686 to both close and, switches 1678 and 1670 to both open, the output signal is amplified by $9G_m$. If the input 1506 receives a logical zero voltage level signal and the input 1508 receives a logical one voltage level signal, which causes switches 1662 and 1686 to both open, and switches 1678 and 1670 to both close, the output signal is amplified by $-9/10\ G_m$. The inputs 1506 and 1508 should not both receive logical one voltage level signals at the same time.

A signal received by the input 1504 of the modified auxiliary filter 1510 is applied to a terminal 1602 of the capacitor 1604, a negative input 1608 of the transconductor 1612, an output 1614 of the transconductor 1612, a positive input 1616 of the transconductor 1620, and an output 1630 of the transconductor 1628. These connections form a node 1650. The other terminal 1606 of the capacitor 1604 is connected to ground. The capacitor 1604 integrates the current signals provided to node 1650 by the outputs of transconductors 1612 and 1628.

The transconductor 1612 operates on the difference between the voltage signal received at a positive input 1610, which is connected to ground, and the voltage signal received at the negative input 1608, and provides a current signal at its output 1614. The signal at the current output 1614 of the transconductor 1612 is equal to the difference between the voltage signal received by its positive input 1610, which is connected to ground, and the signal received by its negative input 1608, which is the voltage at terminal 1602 of the capacitor 1604, scaled by its transconductance G_m. As explained above, the output 1614 of the transconductor 1612 together with one terminal 1602 of the capacitor 1604, the negative input 1608

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of the transconductor 1612, the input 1504, the positive input 1616 of the transconductor 1620 and the output 1630 of the transconductor 1628 form node 1650. The transconductor 1612 forms a feedback loop at at the node 1650.

The transconductor 1620 operates on the difference between the voltage signal received at its positive input 1616, which is the voltage at terminal 1602 of the capacitor 1604, and the voltage signal received at its negative input 1618, which is connected to ground, and provides a current signal at its output 1622. The current signal at the output 1622 is equal to the difference between the voltage signal received by the positive input 1616, which is node 1650, and the voltage signal received by the negative input 1618, scaled by a transconductance QG_m. The output 1622 of the transconductor 1620 together with one terminal 1632 of a capacitor 1634, a positive input 1638 of the transconductor 1642, the positive input 1652 of the transconductor 1655 and a negative input 1624 of the transconductor 1628 form node 1651. The other terminal 1636 of the capacitor 1634 is connected to ground. The capacitor 1634 integrates the current provided to node 1651 by the output 1622 of transconductor 1620.

The transconductor 1628 operates on the difference between the voltage signal received at its positive input 1626, which is connected to ground and the voltage signal received at its negative input 1624, which is voltage at terminal 1632 of the capacitor 1634, and provides a signal at its output 1630 which is connected to node 1650. The current signal at the output 1630, which is connected to node 1650, is equal to the difference in the signal received by the positive input 1626 and the signal received by the negative input 1624, which is connected to node 1651, of the transconductor 1628, scaled by a transconductance QG_m.

The transconductor 1642 operates on the difference between the positive input 1640, which is connected to ground, and the signal received at its negative input 1638, which is the voltage at terminal 1632 of the capacitor 1634, and provides a current signal at an output 1644. The signal at the output 1644 is equal to the difference between the voltage signal received by the positive input 1638, which is node 1651, and the signal received by the negative input 1640 of the transconductor 1642, scaled by a transconductance 9/10 G_m. The output 1644 of the transconductor 1642 is coupled to a signal input 1674 of the switch 1678 and a terminal 1682 of the switch 1686. A signal output 1680 of the switch 1678 is connected to the signal

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output 1512. A terminal 1688 of the switch 1686 is connected to ground. The switch control terminal 1676 of the switch 1678 and the inverted switch control terminal 1684 of the switch 1686 are connected to the input 1508. If the input 1508 receives a logical one voltage level signal, the switch 1678 connects its signal input 1674 and its signal output 1680, which connects the output 1644 of the transconductor 1642 to the output 1512, and the switch 1686 disconnects its terminal 1682 from its terminal 1688. If the input 1508 receives a logical zero voltage level signal, the switch 1678 disconnects its signal input 1674 and its signal output 1680, and the switch 1686 connects its terminal 1682 to its terminal 1688, which connects the output 1644 of the transconductor 1642 to ground.

The transconductor 1655 operates on the difference between the positive input 1652, which is the voltage at terminal 1632 of the capacitor 1634, and the signal received at its negative input 1653, which is connected to ground, and provides a current signal at an output 1656. The signal at the output 1656 is equal to the difference between the voltage signal received by the positive input 1652, which is node 1651, and the signal received by the negative input 1653 of the transconductor 1655, scaled by a transconductance 9 G_m. The output 1656 of the transconductor 1655 is coupled to a signal input 1658 of the switch 1662 and a terminal 1666 of the switch 1670. A signal output 1664 of the switch 1662 is connected to the signal output 1512. A terminal 1672 of the switch 1670 is connected to ground. The switch control terminal 1660 of the switch 1662 and the inverted switch control terminal 1668 of the switch 1670 are connected to the input 1506. If the input 1506 receives a logical one voltage level signal, the switch 1662 connects its signal input 1658 and its signal output 1664, which connects the output 1656 of the transconductor 1655 to the output 1512, and the switch 1670 disconnects its terminal 1666 from its terminal 1672. If the input 1506 receives a logical zero voltage level signal, the switch 1662 disconnects its signal input 1658 and its signal output 1664, and the switch 1670 connects its terminal 1666 and its terminal 1672, which connects the output 1656 of the transconductor 1655 to ground.

In an exemplary embodiment of the modified auxiliary filter 1510, the capacitance of the capacitors 1604 and 1634 are each 80v |. the quality factor, Q, is 20, and the transconductance G_m is 50.

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In another exemplary embodiment of the modified auxiliary filter 1510, a first diode (not shown) and a second diode (not shown) are connected to the node 1650. The cathode of the first diode is connected to the node 1650 and an anode of the first diode is connected to ground. The anode of the second diode is connected to the node 1650 and a cathode of the second diode is connected to ground. This arrangement limits the voltage swing at the node 1650 to approximately ± 0.7 volts.

In still another exemplary embodiment of the modified auxiliary filter 1510, a first diode (not shown) and a second diode (not shown) are connected to the input 1504. The cathode of the first diode is connected to the input 1504 and an anode of the first diode is connected to ground. The anode of the second diode is connected to the input 1504 and a cathode of the second diode is connected to ground. This arrangement limits the voltage swing at the input 1504 to approximately ± 0.7 volts.

In yet another exemplary embodiment of the modified auxiliary filter 1510, a first diode (not shown) and a second diode (not shown) are connected to the output 1510. The cathode of the first diode is connected to the output 1510 and an anode of the first diode is connected to ground. The anode of the second diode is connected to the output 1510 and a cathode of the second diode is connected to ground. This arrangement limits the voltage swing at the output 134 to approximately ± 0.7 volts.

Fig. 17 illustrates a signal processing system 1700. If the signal processing system 1500, shown in Fig. 15, processes a signal with an out-band component which is large as compared to the in-band component it may be desirable to take the output of the main filter output gain unit 138 as the system output, however, if the signal processing system 1500 processes a signal with an out-band component which is not large as compared to the in-band component of the signal it may be desirable to take the system output from another location. The signal processing system 1700 is configured to take the output of the main filter output gain unit 138 as the system output 1718 when the signal received at the input 1702 has a large out-band component relative to the in-band component, and take the system output from another location, here an output 1710 of a multi-output main filter 1708, if the signal received at the input 1702 does not have a large out-band component

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relative to the in-band component. In the present embodiment, the out-band component is large compared to the in-band component of the signal received at the input 1702 if the voltage envelope of the signal received at an input 1704 of the multi-output main filter 1706 is at least 10 dB greater than the voltage envelope of the signal produced at the output 1710 of the multi-output main filter 1706.

The signal processing system 1700 includes a system input 1702, a main filter input gain unit 126, a multi-output main filter 1706, a main filter output gain unit 138, an auxiliary filter input gain unit 106, a modified auxiliary filter 1510, a signal adder 144, a switching unit 1716, a system output 1718, a first peak detector 904, a second peak detector 904, a threshold detector 910, a threshold detector 916, an inverter 922, an inverter 928, an inverter 934, a comparison circuit 1724, and a gain control unit 180. The signal processing system 1700 generates a processed signal provided to the system output 1718 with a strong in channel component well above the filter noise, which is not disturbed when internal states of the signal processing system 1700 are changed. The signal processing system 1700 accomplishes this in a manner similar to the signal processing systems 100 and 1500 if the out-band component of the signal received at the system input 1702 is large compared to the in-band component. If the out-band component of the signal received at the system input 1702 is large compared to the in-band component, the signal processing system 1700 combines a signal processed by the modified auxiliary filter 1510 and a signal processed by the multi-output main filter 1706 whenever there is a change in an amplification factor of the main filter input gain unit 126 and an amplification factor of the main filter output gain unit 138. The signal processed by the modified auxiliary filter 1510 is combined with the signal processed by the multi-output main filter 1706 for a period of time at least as long as the amount of time it takes for transients in the signal processed by the multi-output main filter 1706 to die out. The transients in the signal processed by the modified auxiliary filter 1510 offset the transients in the signal processed by the multi-output main filter 1706. Therefore by combining the signal produced by the modified auxiliary filter 1510 with the signal produced by the multi-output main filter 1706, transients in the signal at the system output 1718 of the signal processing system 1700 are avoided when the amplification factor of the main filter input gain unit 126 and the amplification factor of the main filter output gain unit 138 are changed. If the out-band component of the signal received at the system

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input 1702 is not large compared to the in-band component, the signal processing system 1700 produces the output 1710 of the multi-output main filter 1706 at the system output 1718, because the transients present in the signal produced at the output 1710 of the multi-output main filter 1706 are relatively minor, and the voltage amplitude of the signal produced at the output 1710 remains large whether the signal at the system input 1702 has a large or small voltage envelope.

A signal received at system input 1702 is applied to an input 124 of the main filter input gain unit 126, as described above in relation to Figs. 2 and 3, and an input 104 of the auxiliary filter input gain unit 106, described above in relation to Figs. 2 and 6. The output 128 of the main filter input gain unit 126 is coupled to the input 1704 of the multi-output main filter 1706 and an input 902A of the first peak detector 904, as described above in relation to Figs. 2, 9 and 10. An output 1708 of the multi-output main filter 1706 is connected to the input 142 of the signal adder 144, as described above in relation to Figs. 2 and 8. An output 1710 of the multi-output main filter 1706 is connected to an input 1714 of the switching unit 1716 and an input 902B of the second peak detector 904, as described above in relation to Figs. 2, 9 and 10.

The output 108 of the auxiliary filter input gain unit 106 is connected to an input 1504 of the modified auxiliary filter 1510, as described above in relation to Figs. 15 and 16. An output 1512 of the modified auxiliary filter 1510 is connected to the input 122 of the signal adder 144, as described above in relation to Figs. 2 and 8. The output 146 of the signal adder 144 is connected to the input 136 of the main filter output gain unit 138, as described above in relation to Figs. 2 and 5. The output 140 of the main filter output gain unit 138 is connected to an input 1712 of the switching unit 1716.

The output 906B of the first peak detector 904 is connected to the input 908 of the threshold detector 910, the input 914 of the threshold detector 916, and an input 1720 of the comparison circuit 1724. The output 912 of the threshold detector 910, as described above in relation to Figs. 2, 9 and 11, is connected to the input 920 of the inverter 922. The output 924 of the inverter 922 is connected to the input 926 of the inverter 928. The output 930 of the inverter 928 is connected to the input 182 of the gain control unit 180, as described above in relation to Figs. 2 and 12. The output 918 of the threshold detector 916, as described above in relation to Figs. 2, 9

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and 11, is connected to the input 932 of the inverter 934. The output 936 of the inverter 934 is connected to the input 184 of the gain control unit 180, as described above in relation to Figs. 2 and 12.

The output 906B of the second peak detector 904 is connected to an input 1722 of the comparison circuit 1724. An output 1726 of the comparison circuit 1724 is connected to a switch control terminal 1715 of the switching unit 1716. An output 1719 of the switching unit 1716 is connected to the system output 1718. If the signal received at the switch control terminal 1715 is a logical one voltage level the switching unit connects the input 1712 to the output 1719. Receiving a logical one voltage level signal at the input 1715 indicates that the voltage envelope of the signal received at the input 1704 of the multi-output main filter 1706 as determined by the first peak detector 904 is within 10 dB of the voltage envelope of the signal produced at the output 1710 of the multi-output main filter 1706 as determined by the second peak detector 904, as compared by comparison circuit 1724. If the signal received at the switch control terminal 1715 is a logical zero voltage level the switching unit connects the input 1714 to the output 1719. Receiving a logical zero voltage level signal at the input 1715 indicates that the voltage envelope of the signal received at the input 1704 of the multi-output main filter 1706, as determined by the first peak detector 904, is not within 10 dB of the voltage envelope of the signal produced at the output 1710 of the multi-output main filter 1706 as determined by the second peak detector 904, as compared by the comparison circuit 1724.

The outputs 186, 188 of the gain control unit 180 are connected to the inputs 156, 158, respectively, of the main filter input gain unit 126. The outputs 186, 188, 192 of the gain control unit 180 are connected to the inputs 150, 152, 154, respectively, of the auxiliary filter input gain unit 106. The outputs 194, 196 of the gain control unit 180 are connected to the inputs 1506, 1508, respectively, of the modified auxiliary filter 1510. And the outputs 186, 188, 190 of the gain control unit 180 are connected to the inputs 181, 179, 178, respectively, of the main filter output gain unit 138. In the signal processing system 1700, the outputs 195 and 197 of the gain control unit 180 shown in Fig. 12 are not necessary, and are therefore not connected.

Fig. 18 illustrates an exemplary embodiment of the multi-output main filter 1706 which is in the form of a slightly altered standard Tow-Thomas biquad.

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The multi-output main filter 1706 differs from the main filter 132 in that the multi-output main filter 1706 includes an additional output 1710. The output 1710 follows the voltage that is presented at a node 1851 of the multi-output main filter 1706. The node 1851 provides an output signal that has undergone input amplification but no output amplification. The multi-output main filter 1706 includes an input 1704, a transconductor 1812, a transconductor 1820, a transconductor 1828, a transconductor 1842, an operational amplifier 1852, a capacitor 1804, a capacitor 1834, an output 1708, and an output 1710. The center frequency ω_0 of the multi-output main filter 1706 can be calculated by the equation:

$$\omega_0 = Q\, G_m / C \qquad (2)$$

where Q is the quality factor of the multi-output main filter 1706 and G_m is the transconductance of transconductor 1812. The absolute value of the transconductances and capacitances can be scaled by the same factor, i.e., impedance scaling, without affecting the transfer function of the multi-output main filter 1706, since the transfer function depends on the ratios of these values. Impedance scaling does not change the transfer function of the multi-output main filter 1706; however, it does change the power dissipation and the noise level of the multi-output main filter 1706.

A signal received by the input 1704 of the multi-output main filter 1706 is applied to a terminal 1802 of the capacitor 1804, a negative input 1808 of the transconductor 1812, an output 1814 of the transconductor 1812, a positive input 1816 of the transconductor 1820, and an output 1830 of the transconductor 1828. These connections form a node 1850. The other terminal 1806 of the capacitor 1804 is connected to ground. The capacitor 1804 integrates the current signals provided to node 1850 by the outputs of transconductors.

The transconductor 1812 operates on the difference between the voltage signal received at its positive input 1810, which is connected to ground, and the voltage signal received at its negative input 1808, and provides a current signal at its output 1814. The signal at the current output 1814 of the transconductor 1812 is equal to the difference between the voltage signal received by its positive input 1810, which is connected to ground, and the signal received by its negative input 1808, which is the voltage at terminal 1802 of the capacitor 1804, scaled by its

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transconductance G_m. As explained above, the output 1814 of the transconductor 1812 together with one terminal 1802 of the capacitor 1804, the negative input 1808 of the transconductor 1812, the input 1704, the positive input 1816 of the transconductor 1820 and the output 1830 of the transconductor 1828 form node 1850. The transconductor 1812 forms a feedback loop with the node 1850.

The transconductor 1820 operates on the difference between the voltage signal received at its positive input 1816, which is the voltage at terminal 1802 of the capacitor 1804, and the voltage signal received at its negative input 1818, which is connected to ground, and provides a current signal at its output 1822. The current signal at the output 1822 is equal to the difference between the voltage signal received by the positive input 1816, which is connected to node 1850, and the voltage signal received by the negative input 1818, scaled by a transconductance QG_m. The common connection of the output 1822 of the transconductor 1820 together with one terminal 1832 of a capacitor 1834, a positive input 1838 of the transconductor 1842, a negative input 1824 of the transconductor 1828, and a positive input 1846 of the operational amplifier 1852 form node 1851. The other terminal 1836 of the capacitor 1834 is connected to ground. The capacitor 1834 integrates the current provided to node 1851 by the output 1822 of transconductor 1820.

The transconductor 1828 operates on the difference between the voltage signal received at its positive input 1826, which is connected to ground, and the voltage signal received at its negative input 1824, which is voltage at terminal 1832 of the capacitor 1834, and provides a signal at its output 1830, which is connected to node 1850. The current signal at the output 1830, which is connected to node 1850, is equal to the difference in the signal received by the positive input 1826 and the signal received by the negative input 1824, which is connected to node 1851, of the transconductor 1828, scaled by a transconductance QG_m.

The transconductor 1842 operates on the difference between the signal received at its positive input 1838, which is the voltage at terminal 1832 of the capacitor 1834, and the voltage signal received at its negative input 1840, which is connected to ground, and provides a current signal at an output 1844. The signal at the output 1844 is equal to the difference between the voltage signal received by the positive input 1838, which is connected to node 1851, and the signal received by the negative input 1840 of the transconductor 1842, scaled by a transconductance G_m.

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The output 1844 of the transconductor 1842 is coupled to the output 1708 of the multi-output main filter 1706.

The operational amplifier acts as a buffer between the node 1851 and the output 1710. The voltage at the output 1710 will follow the voltage at the terminal 1832 of the capacitor 1834. An output 1854 of the operational amplifier 1852 is connected to a inverting input 1848 of the operational amplifier 1852 and the output 1710.

In an exemplary embodiment of the multi-output main filter 1706, the capacitance of the capacitors 1804 and 1834 are each 80 pf. the quality factor, Q, is 20, and the transconductance G_m is 50.

In another exemplary embodiment of the multi-output main filter 1706, a first diode (not shown) and a second diode (not shown) are connected to the node 1850. The cathode of the first diode is connected to the node 1850 and an anode of the first diode is connected to ground. The anode of the second diode is connected to the node 1850 and a cathode of the second diode is connected to ground. This arrangement limits the voltage swing at the node 1850 to approximately ± 0.7 volts.

In still another exemplary embodiment of the multi-output main filter 1706, a first diode (not shown) and a second diode (not shown) are connected to the input 1704. The cathode of the first diode is connected to the input 1704 and an anode of the first diode is connected to ground. The anode of the second diode is connected to the input 1704 and a cathode of the second diode is connected to ground. This arrangement limits the voltage swing at the input 1704 to approximately ± 0.7 volts.

In yet another exemplary embodiment of the multi-output main filter 1706, a first diode (not shown) and a second diode (not shown) are connected to the output 1708. The cathode of the first diode is connected to the output 1708 and an anode of the first diode is connected to ground. The anode of the second diode is connected to the output 1708 and a cathode of the second diode is connected to ground. This arrangement limits the voltage swing at the output 1708 to approximately ± 0.7 volts.

Fig. 19 illustrates an exemplary embodiment of the comparison circuit 1724 shown in Fig. 17 in greater detail. The comparison circuit 1724 determines

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whether the voltage signal received at its input 1720, which is representative of the voltage envelope of the signal received at the input 1704 of the multi-output main filter 1706 as determined by the first peak detector 904, is more than 10 dB greater than the voltage signal received at its input 1722. The voltage signal at input 1722 is representative of the voltage envelope of the signal produced at the output 1710 of the multi-output main filter 1706 as determined by the second peak detector 904. The comparison circuit 1724 includes an NMOS transistor Q_1, an NMOS transistor Q_2, a PMOS transistor Q_3, a PMOS transistor Q_4, an inverter 1942, and an inverter 1948. A signal received by the input 1722 of the comparison circuit 1724 is applied to the gate 1902 of the NMOS transistor Q_1; and a signal received by the input 1720 of the comparison circuit 1724 is applied to the gate 1912 of the NMOS transistor Q_2.

The PMOS transistor Q_3 and the PMOS transistor Q_4 form a current mirror. The source 1924 of the PMOS transistor Q_3, and the source 1934 of the PMOS transistor Q_4 are both connected to supply voltage V_{dd}. The gate 1922 of the PMOS transistor Q_3 is connected to the gate 1932 of the PMOS transistor Q_4, the drain 1926 of the PMOS transistor Q_3, and the drain 1906 of the NMOS transistor Q_1. The drain 1936 of the PMOS transistor Q_4 is connected to the drain 1916 of the NMOS transistor Q_2 and an input 1940 of the inverter 1942. And the source 1904 of the NMOS transistor Q_1 and the source 1914 of the NMOS transistor Q_2 is connected to supply voltage V_{ss}.

The voltage of the signal received at the input 1722, which is representative of the voltage envelope of the signal produced at the output 1710 of the multi-output main filter 1706, as determined by the second peak detector 904, causes a current to flow through the NMOS transistor Q_1. Likewise, the voltage of the signal received at the input 1720, which is representative of the voltage envelope of the signal received at the input 1704 of the multi-output main filter 1706, as determined by the first peak detector 904, will cause a current to flow through the NMOS transistor Q_2. The PMOS transistor Q_4 is dimensioned such that the width to length ratio of the transistor is 3 times that of the PMOS transistor Q_3. Therefore, the current mirror will create a current flowing from the source 1934 to the drain 1936 of the PMOS transistor Q_4 that is 10 dB greater than the current flowing through the NMOS transistor Q_1. If the current flowing through the PMOS transistor Q_4 is greater than the current flowing through the NMOS transistor Q_2, the voltage envelope of the

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signal received at the input 1704 of the multi-output main filter 1706 is not more than 10 dB larger than the voltage of the signal produced at the output 1710 of the multi-output main filter 1706. Therefore, charge will collect at the input 1940 of the inverter 1942, and an output 1944 of the inverter 1942 will be driven to a logical zero voltage level. If the current flowing through the PMOS transistor Q_4 is less than the current flowing through the NMOS transistor Q_2, the voltage envelope of the signal received at the input 1704 of the multi-output main filter 1706 is more than 10 dB larger than the voltage of the signal produced at the output 1710 of the multi-output main filter 1706. Therefore, transistor Q_2 will sink charge from the input 1940 of the inverter 1942, and the output 1944 of the inverter 1942 will be driven to a logical one voltage level.

The output 1944 of the inverter 1942 is connected to an input 1946 of the inverter 1948. An output 1950 of the inverter 1948 is connected to the output 1726. The inverters 1942 and 1948 serve to "clean up" (i.e. make the logical zero to logical one voltage level signal transitions and the logical one to logical zero voltage level signal transitions more abrupt) the signal produced by the drain 1936 of the PMOS transistor Q_4.

Fig. 20 illustrates an exemplary embodiment of the switching unit 1716 as shown in Fig. 17. The switching unit 1716 includes an input 1712, an input 1714, an input 1715, a first switch 2006, a second switch 2014 and an output 1719. The switching unit 1716 provides one of the signals received at the inputs 1712, 1714 to the output 1719 in response to a signal received at the input 1715. If the signal received at the input 1715 is a logical one voltage level (i.e., 5 V), switch 2014 closes while switch 2006 opens, and the signal received at the input 1714 is provided to the output 1719. A logical one voltage level signal received at the input 1715 is representative of the voltage envelope of the signal received at the input 1704 of the multi-output main filter 1706, as determined by the first peak detector 904, being not more than 10 dB greater than the voltage signal received at its input 1722. The voltage signal received at the input 1722 is representative of the voltage envelope of the signal produced at the output 1710 of the multi-output main filter 1706, as determined by the second peak detector 904 and as compared by the comparison circuit 1724. If the signal received at the input 1715 is a logical zero voltage level, switch 2014 opens while switch 2006 closes, and the signal received at the input 1712

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is provided to the output 1719. A logical zero voltage level signal received at the input 1715 is representative of the voltage envelope of the signal received at the input 1704 of the multi-output main filter 1706, as determined by the first peak detector 904, being more than 10 dB greater than the voltage signal received at its input 1722. The voltage signed received at the input 1722 is representative of the voltage envelope of the signal produced at the output 1710 of the multi-output main filter 1706 as determined by the second peak detector 904 and as compared by the comparison circuit 1724. Switches 2006 and 2014 may each be implemented as CMOS transmission gates.

A signal received at the input 1712 is applied to one terminal 2002 of the first switch 2006; a signal received at the input 1714 is applied to one terminal 2010 of the second switch 2014; and a signal received at the input 1715 is applied to the switch control terminal 2012 of the second switch 2014 and the inverting switch control terminal 2004 of the first switch 2006. The first switch 2006 closes to connect its terminal 2002 to its other terminal 2008 if the signal received at the inverting switch control terminal 2004 is a logical zero voltage level (*i.e.*, ground potential). If the signal at the inverting switch control terminal 2004 is a logical one voltage level (*i.e.*, 5 V), the first switch 2006 opens to disconnect its terminal 2002 from its other terminal 2008 resulting in an open circuit between those terminals. The other terminal 2008 of the first switch 2006 is connected to the output 1719 of the switching unit 1716.

The second switch 2014 closes to connect its terminal 2010 to its other terminal 2016 if the signal received at the switch control terminal 2012 is a logical one voltage level. If the signal at the switch control terminal 2012 is a logical zero voltage level, the second switch 2014 opens to disconnect its terminal 2010 from its other terminal 2016 resulting in an open circuit between those terminals. The other terminal 2016 of the second switch 2014 is connected to the output 1719 of the switching unit 1716.

It should be appreciated that in an alternate embodiment, the main filter output gain unit 138 may be implemented in the digital domain, by using an analog to digital converter to create a digital representation of the analog signal and a multiplier and multiplying a digitized representation of the signal received at the input 136 by a digitized representation of one of the amplification factors.

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CLAIMS

1. An active filter system comprising:

a system input for receiving a system input signal ;

a system output for providing a system output signal;

a first input gain circuit having a signal input coupled to the system input for receiving the system input signal, a gain control input and an output for providing a first amplified system input signal, the first input gain circuit being responsive to a first gain control signal received by the gain control input for amplifying the system input signal by a first amplification factor to obtain the first amplified system input signal, and being responsive to a second gain control signal received by the gain control input for amplifying the system input signal by a second amplification factor to obtain the first amplified system input signal;

a first filter circuit having an input coupled to the output of the first input gain circuit, and an output, the first filter circuit being responsive to the first amplified system input signal received at its input for providing a first processed signal at its output;

a first output gain circuit having a signal input coupled to the output of the first filter circuit for receiving the first processed signal, a gain control input and an output for providing a first amplified processed signal, the first output gain circuit being responsive to the first gain control signal received by its gain control input for amplifying the first processed signal received at its signal input by a third amplification factor to obtain the first amplified processed signal and responsive to a second gain control signal received by its gain control input for amplifying the first processed output signal received at its signal input by a fourth amplification factor to obtain the first amplified processed signal;

a second input gain circuit having a signal input coupled to the system input for receiving the system input signal, a gain control input, an output control input, and an output for providing a second amplified system input signal, the second input gain circuit being responsive to the first gain control signal received by its gain control input for amplifying the system input signal by the first amplification factor to obtain the second amplified system input signal and being responsive to the second gain control signal received by its gain control input for amplifying the system input

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signal by the second amplification factor to obtain the second amplified system input signal, and the second input gain circuit being responsive to a first output control signal received by its output control input for providing the second amplified system input signal to its output and responsive to a second output control signal for causing its output to be an open circuit;

a second filter circuit having an input coupled to the output of the second input gain circuit, and an output, the second signal processing circuit being responsive to the second amplified system input signal received by its input for providing a second processed signal at its output;

a second output gain circuit having a signal input coupled to the output of the second filter circuit for receiving the second processed signal, a gain control input, a polarity control input, an output control input, and an output for providing one of an auxiliary output signal and ground, the second output gain circuit being responsive to a third gain control signal received by its gain control input for amplifying the second processed signal by a fifth amplification factor to obtain an amplified second processed signal, and being responsive to a fourth gain control signal received by its gain control input for amplifying the second processed signal by a sixth amplification factor to obtain the amplified second processed signal, the second output gain circuit being responsive to a first polarity gain control signal received by its polarity control input for inverting the amplified second processed signal to obtain the auxiliary output signal, and being responsive to a second polarity gain control signal received by its polarity control input for amplifying the amplified second processed signal by a unity gain to obtain the auxiliary output signal, the second output gain circuit being responsive to a first output control signal received by its output control input for connecting its output to ground, and being responsive to a second output control signal received by its output control input for providing the auxiliary output signal at its output;

a signal adding circuit having a first input coupled to the output of the first output gain circuit, a second input coupled to the output of the second output gain circuit, and an output coupled to the system output, the signal adding circuit combining the first amplified processed signal provided by the output of the first output gain circuit, and one of the auxiliary output signal and ground provided by the

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output of the second output gain circuit to provide the system output signal at the output of the signal adding circuit.

2. The active filter system of claim 1 further comprising:

a signal strength detector having an input coupled to the input of the first filter circuit and an output, the signal strength detector being responsive to a signal strength of the first amplified system input signal at the input of the first filter circuit being equal to or greater than a first threshold for providing a first signal strength signal at the output of the signal strength detector, and being responsive to a signal strength of the first amplified system input signal at the input of the first filter circuit being less than a second threshold for providing a second signal strength signal at the output of the signal strength detetor; and

a gain control circuit having an input coupled to the output of the strength detector, and a multiplicity of outputs respectively coupled to the gain control input of the first input gain circuit, to the gain control input of the first output gain circuit, to the gain control input and the output control input of the second input gain circuit, and to the gain control input, the polarity control input and the output control input of the second output gain circuit, the gain control circuit being responsive to the first signal strength signal received at its input for providing the second gain control signal to the gain control input of the first input gain circuit, the second gain control signal to the gain control input of the first output gain circuit, the second gain control signal to the gain control input of the second input gain circuit, the second output control signal to the output control input of the second input gain circuit, the third gain control signal to the gain control input of the second output gain circuit, the first polarity gain control signal to the polarity control input of the second output gain circuit, the second output control signal to the output control input of the second output gain circuit, and, after a predetermined delay, for providing the first output control signal to the output control input of the second input gain circuit and the first output control signal to the output control input of the second output gain circuit, the gain control circuit being responsive to the second signal strength signal received by its input for providing the first gain control signal to the gain control input of the first input gain circuit, the first gain control signal to the gain control input of the first output gains circuit, the first gain control signal to the gain control input of the second

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input gain circuit, the second output control signal to the output control input of the second input gain circuit, the third gain control signal to the gain control input of the second output gain circuit, the second polarity gain control signal to the output control input of the second output gain circuit and, after a predetermined delay, for providing the first output control signal to the output control input of the second input gain circuit and the first output control signal to the output control input of the second output gain circuit.

3. The active filter system of claim 1, wherein the first filter circuit and the second filter circuit are each a Tow-Thomas biquad having an input terminal, an output terminal, first, second, third and fourth transconductors each having a normal input, an inverting input and an output, a first capacitor, and a second capacitor, the first transconductor having a first transconductance and having its inverting input and output connected to the input terminal and its normal input connected to ground, the second transconductor having a second transconductance equal to the product of the first transconductance and a quality factor of the Tow-Thomas biquad and having its inverting input connected to ground, its normal input connected to the input terminal and its output connected to a first node, the third transconductor having the second transconductance and having its inverting input connected to the first node, its normal input connected to ground and its output connected to the input terminal, the fourth transconductor having the first transconductance and having its normal input connected to the first node, its inverting input connected to ground and its output connected to the output terminal, the first capacitor being connected between the input terminal and the ground, and the second capacitor being connected between the first node and ground.

4. The active filter system of claim 2, wherein the signal strength detector comprises:

a peak detector having an input coupled to the input of the first filter circuit and an output, the peak detector being responsive to the first amplified system input signal received by the input of the first filter circuit for providing a voltage envelope peak of the first amplified system input signal at the output of the peak detector;

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a threshold detector having an input coupled to the output of the peak detector, and an output, the threshold detector comparing the voltage envelope peak of the first amplified system input signal received at its input with the first threshold and providing the first signal strength signal at its output if the voltage envelope peak of the first amplified system input signal is equal to or greater than the first threshold, the threshold detector providing the second signal strength signal at its output if the voltage envelope peak of first amplified system input signal is less than the second threshold.

5. The signal processing system of claim 2, wherein the gain control circuit includes a multiple state logic circuit responsive to the first signal strength signal and the second signal strength signal for deriving respective signals provided by the multiplicity of outputs of the gain control circuit.

6. The signal processing system of claim1, wherein the first input gain circuit and the second input gain circuit each include circuitry for clamping their respective output signals so as to prevent saturation of the first filter circuit and the second filter circuit.

7. The signal processing system of claim 2, wherein the first threshold is a voltage envelope signal strength level of the first amplified system input signal that causes the first filter circuit to approach saturation, and the second threshold is a voltage envelope signal strength level of the first amplified system input signal that causes the first filter circuit to provide a signal at its output having a minimum tolerable signal-to-noise ratio.

8. An active filter system comprising:

a system input for receiving a system input signal;

a system output for providing a system output signal;

a first input gain circuit having a signal input coupled to the system input for receiving the system input signal, a gain control input and an output for providing a first amplified system input signal, the first input gain circuit being responsive to a first gain control signal received by the gain control input for amplifying the system input signal by a first amplification factor to obtain the first

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amplified system input signal and responsive to a second gain control signal received by the gain control input for amplifying the system input signal by a second amplification factor to obtain the first amplified system input signal;

a first filter circuit having an input coupled to the output of the first input gain circuit and an output, the first filter circuit being responsive to a first amplified system input signal received at its input for providing a first processed signal at its output;

a second input gain circuit having a signal input coupled to the system input for receiving the system input signal, a gain control input, an output control input and an output for providing a second amplified system input signal, the second input gain circuit being responsive to the first gain control signal received by its gain control input for amplifying the system input signal by the first amplification factor to obtain the second amplified system input signal and responsive to the second gain control signal received by its gain control input for amplifying the system input signal by the second amplification factor to obtain the second amplified system input signal, the second input gain circuit being responsive to a first output control signal received by its output control input for providing the second amplified system input signal to its output and responsive to a second output control signal for causing its output to be an open circuit;

a second filter circuit having a signal input coupled to the output of the second input gain circuit, a gain control input and an output for providing a second amplified processed signal, the second filter circuit being responsive to the second amplified system input signal received by its input for providing a second processed signal, and being responsive to a third gain control signal received by its gain control input for amplifying the second processed signal by a fifth amplification factor to obtain the second amplified processed signal and being responsive to a fourth gain control signal received by its gain control input for amplifying the second processed signal by a sixth amplification factor to obtain the second amplified processed signal;

a signal adding circuit having a first input coupled to the output of the first filter circuit, a second input coupled to the output of the second filter circuit and an output for providing a combined processed signal, the signal adding circuit combining the first processed output signal provided by the output of the first filter

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circuit and the second amplified processed signal provided by the output of the second filter circuit to provide the combined processed signal;

a first output gain circuit having a signal input coupled to the output of the signal adding circuit, a gain control input and an output coupled to the system output, the first output gain circuit being responsive to the first gain control signal received by its gain control input for amplifying the combined processed signal received at its signal input by a third amplification factor to obtain the system output signal at its output and being responsive to a second gain control signal received by its gain control input for amplifying the combined processed signal received at its signal input by a fourth amplification factor to obtain the system output signal at its output.

9. The system of claim 8 further comprising:

a signal strength detector circuit having an input coupled to the output of the first active filter circuit and an output, the signal strength detector circuit being responsive to a signal strength of the first amplified system input signal at the input of the first filter circuit being equal to or greater than a first threshold for providing a first signal strength signal at its output, the signal strength circuit being responsive to a signal strength of the first amplified system input signal at the input of the first filter circuit being less than a second threshold for providing a second strength signal at its output;

a gain control circuit having an input coupled to the output of the strength detector circuit and a plurality of outputs respectively coupled to the gain control input of the first input gain circuit, to the gain control input of the first output gain circuit, to the gain control input and the output control input of the second input gain circuit, and to the gain control input of the second filter circuit, the gain control circuit being responsive to the first signal strength signal received at its input for providing the second gain control signal to the gain control of the first input gain circuit, the second gain control signal to the gain control input of the first output gain circuit, the second gain control signal to the gain control input of the second input gain circuit, the second output control signal to the output control input of the second input gain circuit, the fourth gain control signal to the gain control input of the second filter circuit, and after a predetermined delay for providing the first output control signal to the output control input of the second input gain circuit and the third gain

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control signal to the gain control input of the second filter circuit, and the gain control circuit being responsive to the second signal strength signal received at its input for providing the first gain control signal to the gain control of the first input gain circuit, the first gain control signal to the gain control input of the first output gain circuit, the first gain control signal to the gain control input of the second input gain circuit, the second output control signal to the output control input of the second input gain circuit, the fourth gain control signal to the gain control input of the second filter circuit, and after a predetermined delay for providing the first output control signal to the output control input of the second input gain circuit and the third gain control signal to the gain control input of the second filter circuit.

10. The filter system of claim 9, wherein the active filter circuit has an input terminal, a first gain control terminal, a second gain control terminal and an output terminal, first, second, third, fourth and fifth transconductors each having a normal input, an inverting input and an output, a first capacitor, a second capacitor, a first and third switch, each having a first signal terminal, a second signal terminal and a switch control terminal, and a second and fourth switch having a first signal terminal, a second signal terminal, and an inverting switch control terminal, the first transconductor having a first transconductance and having its inverting input and output connected to the input terminal and its normal input connected to ground, the second transconductor having a second transconductance equal to the product of the first transconductance and a quality factor of the active filter and having its inverting input connected to ground, its normal input connected to the input terminal and its output terminal connected to a first node, the third transconductor having the second transconductance and having its inverting input connected to the first node, its normal input connected to ground and its output connected to the input terminal, the first capacitor being connected between the input terminal and the ground, the second capacitor being connected between the first node and ground, the fourth transconductor having a third transconductance equal to nine-tenths of the first transconductance and having its normal input connected to ground, its inverting input connected to the first node and its output connected to the first signal terminal of the first switch and the first signal terminal of the second switch, the second signal terminal of the first switch being connected to the output terminal, the switch control

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terminal of the first switch being connected to the first gain control terminal, the second signal terminal of the second switch being connected to ground, the switch control terminal of the second switch being connected to the first gain control terminal, the second terminal of the first switch connected to the output terminal, the active filter circuit being responsive to a logical one voltage level signal at the first gain control terminal providing the signal received at the first signal terminal of the first switch to the second signal terminal of the first switch, and being responsive to a logical zero voltage level signal at the first gain control terminal providing the signal received at the first signal terminal of the second switch to the second signal terminal of the second switch, the fifth transconductor having a fifth transconductance equal to nine times the first transconductance and having its normal input connected to the first node, its inverting input connected to ground and its output connected to the first signal terminal of the third switch and the first signal terminal of the fourth switch, the second signal terminal of the third switch being connected to the output terminal, the switch control terminal of the third switch being connected to the second gain control terminal, the second signal terminal of the fourth switch being connected to ground, the switch control terminal of the fourth switch being connected to the second gain control terminal, the second terminal of the third switch connected to the output terminal, the active filter circuit responsive to a logical one voltage level signal at the second gain control terminal providing the signal received at the first signal terminal of the third switch to the second signal terminal of the third switch, and responsive to a logical zero voltage level signal at the gain control terminal of the third switch providing the signal received at the first signal terminal of the fourth switch to the second signal terminal of the fourth switch.

11. A filter system comprising:

a system input for receiving a system input signal;

a system output for providing a system output signal;

a first input gain circuit having a signal input coupled to the system input for receiving the system input signal, a gain control input and an output for providing a first amplified system input signal, the first input gain circuit being responsive to a first gain control signal received by the gain control input for amplifying the system input signal by a first amplification factor to obtain the first

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amplified system input signal and responsive to a second gain control signal received by the gain control input for amplifying the system input signal by a second amplification factor to obtain the first amplified system input signal;

a first filter circuit having an input coupled to the output of the first input gain circuit, a first output for providing a first processed signal, and a second output for providing a buffered first processed signal, the first filter circuit being responsive to a first amplified system input signal received at its input for providing the first processed signal at its first output, and for providing the buffered first processed signal at its second output;

a second input gain circuit having a signal input coupled to the system input for receiving the system input signal, a gain control input, an output control input and an output for producing a second amplified system input signal, the second input gain circuit being responsive to the first gain control signal received by its gain control input for amplifying the system input signal by the first amplification factor to obtain the second amplified system input signal and being responsive to the second gain control signal received by its gain control input for amplifying the system input signal by the second amplification factor to obtain the second amplified system input signal, and the second input gain circuit being responsive to a first output control signal received by its output control input for providing the second amplified system input signal to its output and being responsive to a second output control signal received by its output control input for causing its output to be an open circuit;

a second filter circuit having a signal input coupled to the output of the second input gain circuit, a gain control input and an output for providing a second amplified processed signal, the second filter circuit being responsive to the second amplified system input signal received by its input for providing a second processed signal, and being responsive to a third gain control signal received by its gain control input for amplifying the second processed signal by a fifth amplification factor to obtain the second amplified processed output signal and being responsive to a fourth gain control signal received by its gain control input for amplifying the second processed signal by a sixth amplification factor to obtain the second amplified processed output signal;

a signal adding circuit having a first input coupled to the first output of the first filter circuit, a second input coupled to the output of the second filter circuit

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and an output for providing a combined processed signal, the signal adding circuit combining the first processed output signal provided by the output of the first filter circuit and the second amplified processed signal provided by the output of the second filter circuit to provide the combined processed signal;

a first output gain circuit having a signal input coupled to the output of the signal adding circuit, a gain control input and an output for providing an amplified combined processed signal, the first output gain circuit being responsive to the first gain control signal received by its gain control input for amplifying the combined processed signal received at its signal input by a third amplification factor to obtain the amplified combined processed signal and being responsive to a second gain control signal received by its gain control input for amplifying the combined processed signal received at its signal input by a fourth amplification factor to obtain the amplified combined processed signal; and

a signal switching circuit having a first signal input coupled to the output of the first output gain circuit, a second signal input coupled to the second output of the first filter circuit, a switch control input and an output coupled to the system output, the signal switching circuit being responsive to receiving a first switching signal at the switch control input for providing the amplified combined processed signal received at the first signal input to the output, and being responsive to receiving a second switching signal at the switch control input for providing the buffered first processed output signal received at the second signal input to the output.

12. The system of claim 11 further comprising:

a first peak detector circuit having an input coupled to the output of the input gain of the first active filter and an output, the first peak detector being responsive to the first amplified system input signal for providing a voltage envelope peak of the first amplified system input signal at its output;

a first threshold detector circuit having an input coupled to the output of the first peak detector and an output, the first threshold detector for comparing the voltage envelope peak of the first amplified system input signal received at its input with a first threshold, and providing the first signal strength signal at its output if the voltage envelope peak of the first amplified system input signal is equal to or greater than the first threshold;

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a second threshold detector circuit having an input coupled to the output of the first peak detector and an output, the second threshold detector for comparing the voltage envelope peak of the first amplified system input signal received at its input with a second threshold, and providing the second signal strength signal at its output if the voltage envelope peak of the first amplified system input signal is less than the first threshold;

a gain control circuit having first and second inputs coupled to the outputs of first and second threshold detector circuits, respectively, and a multiplicity of outputs respectively coupled to the gain control input of the first input gain circuit, to the gain control input of the first output gain circuit, to the gain control input and the output control input of the second input gain circuit, and to the gain control input of the second filter circuit, the gain control circuit being responsive to the first signal strength signal received at its first input for providing the second gain control signal to the gain control of the first input gain circuit, the second gain control signal to the gain control input of the first output gain circuit, the second gain control signal to the gain control input of the second input gain circuit, the second output control signal to the output control input of the second input gain circuit, the fourth gain control signal to the gain control input of the second filter circuit, and, after a predetermined delay, for providing the first output control signal to the output control input of the second input gain circuit and the third gain control signal to the gain control input of the second filter circuit, and the gain control circuit being responsive to the second signal strength signal received at its second input for providing the first gain control signal to the gain control of the first input gain circuit, the first gain control signal to the gain control input of the first output gain circuit, the first gain control signal to the gain control input of the second input gain circuit, the second output control signal to the output control input of the second input gain circuit, the fourth gain control signal to the gain control input of the second filter circuit, and after a predetermined delay for providing the first output control signal to the output control input of the second input gain circuit and the third gain control signal to the gain control input of the second filter circuit;

a second peak detector circuit having an input coupled to the output of the first active filter circuit and an output, the second peak detector being responsive

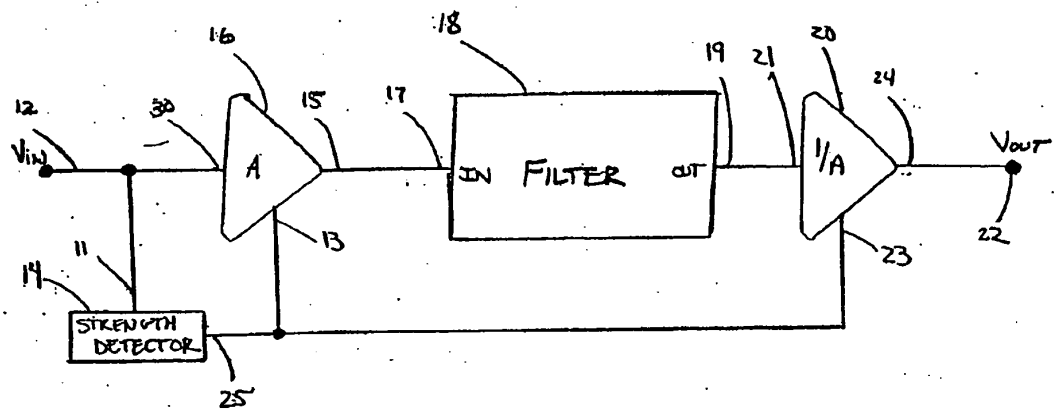
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to the first processed signal for providing a voltage envelope peak of the first processed signal at its output;

a comparison circuit having a first signal input coupled to the output of the first peak detector, a second signal input coupled to the output of the second peak detector, and an output, the comparison circuit being responsive to the voltage envelope peak of the first amplified system input signal and the voltage envelope peak of the first processed signal for providing a first switching signal to its output if the voltage envelope peak of the first amplified system input signal is greater than the voltage envelope peak of the first processed signal by a specified threshold, and for providing a second switching signal to its output if the voltage envelope peak of the first amplified system input signal is not greater than the voltage envelope peak of the first processed output signal by the specified threshold.

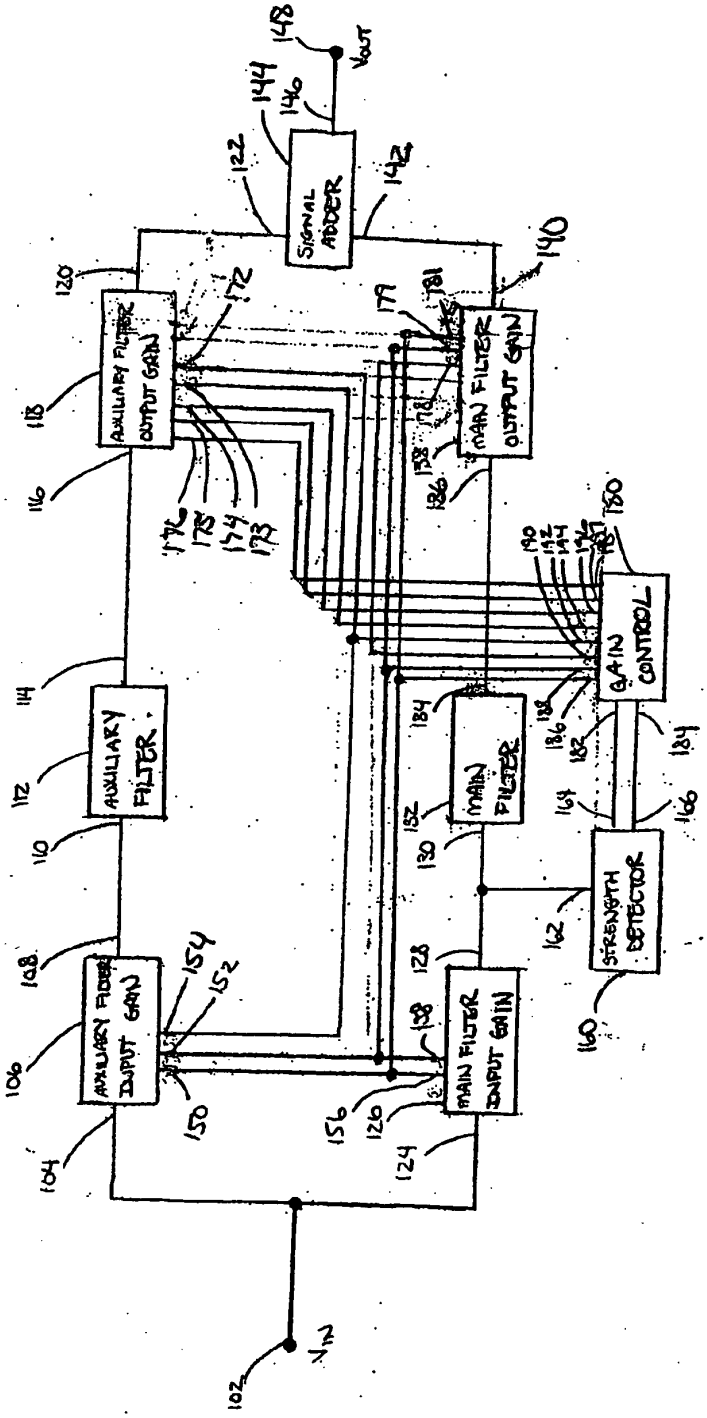
13. The filter system of claim 12, wherein the first active filter circuit is a multi-output Tow-Thomas biquad having an input terminal, a first output terminal, a second output terminal, first, second, third and fourth transconductors each having a normal input, an inverting input and an output, an operational amplifier having a normal input, an inverting input and an output, a first capacitor, and a second capacitor, the first transconductor having a first transconductance and having its inverting input and output connected to the input terminal and its normal input connected to ground, the second transconductor having a second transconductance equal to the product of the first transconductance and a quality factor of the multi-output Tow-Thomas biquad and having its inverting input connected to ground, its normal input connected to the input terminal and its output terminal connected to a first node, the third transconductor having the second transconductance and having its inverting input connected to the first node, its normal input connected to ground and its output connected to the input terminal, the fourth transconductor having the first transconductance and having its normal input connected to the first node, its inverting input connected to ground and its output connected to the first output terminal, the operational amplifier having its normal input connected to the first node and its inverting input and its output connected to the second output terminal, the first capacitor being connected between the input terminal and the ground, and the second capacitor being connected between the first node and ground.

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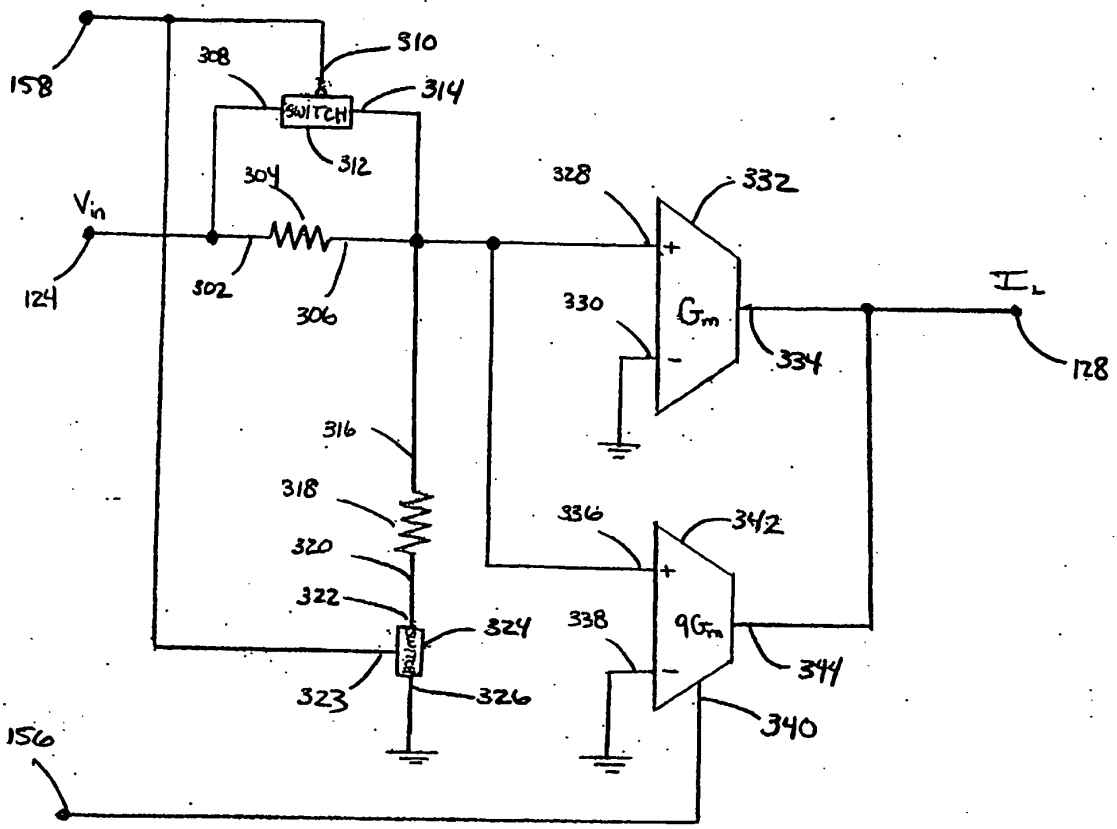
10

FIG. 1
(Prior Art)


SIGNAL ADDER
AUXILIARY FILTER OUTPUT GAIN
MAIN FILTER OUTPUT GAIN
GAIN CONTROL
AUXILIARY FILTER
MAIN FILTER
STRENGTH DETECTOR
AUXILIARY FILTER INPUT GAIN
MAIN FILTER INPUT GAIN

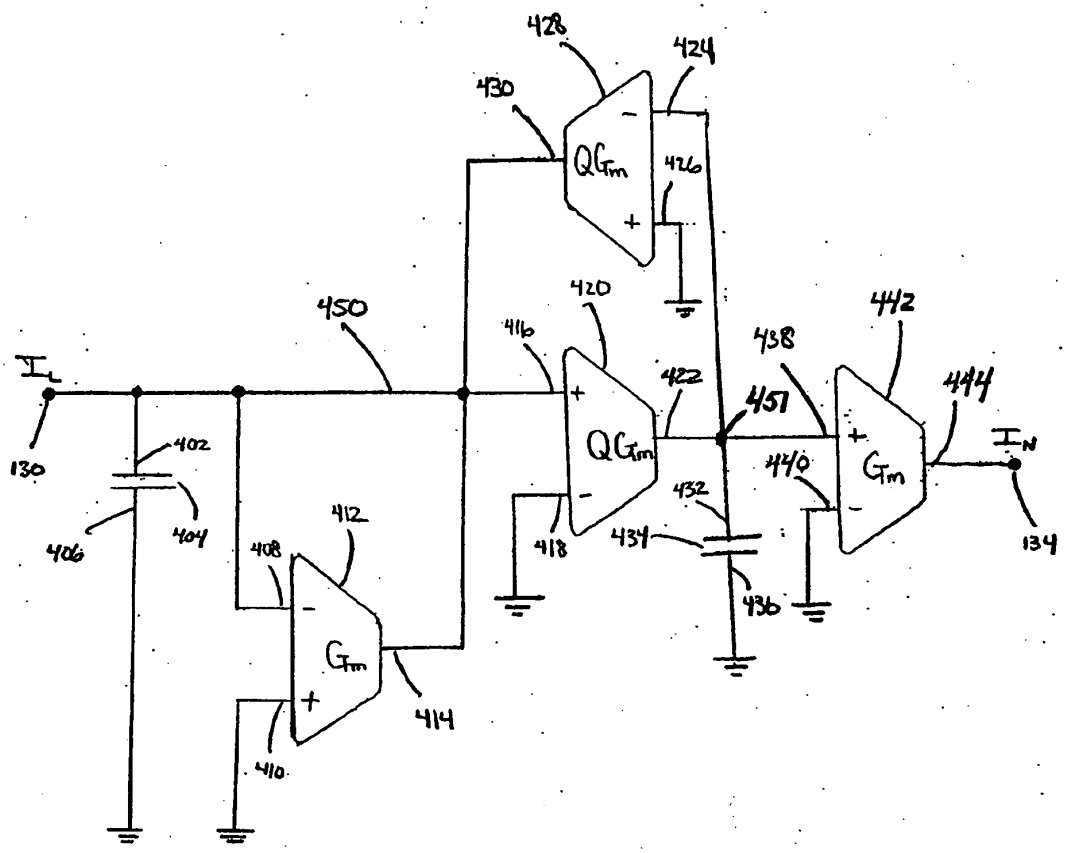
100

Fig. 2


158
308
310
314
SWITCH
312
304
328
332
V_{in}
124
302
306
330
G_m
334
I_L
178
316
318
336
342
320
322
338
$9G_m$
324
344
323
326
340
156

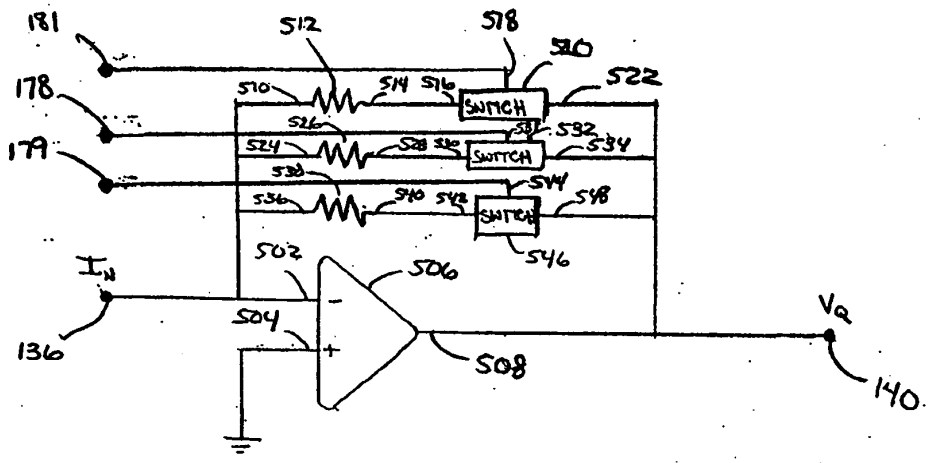
126

FIG. 3


428
424
430
QG_m
426
420
450
416
422
438
442
444
I_L
130
402
406
404
QGm
451
I_N
440
Gm
432
434
436
418
134
412
408
Gm
414
410

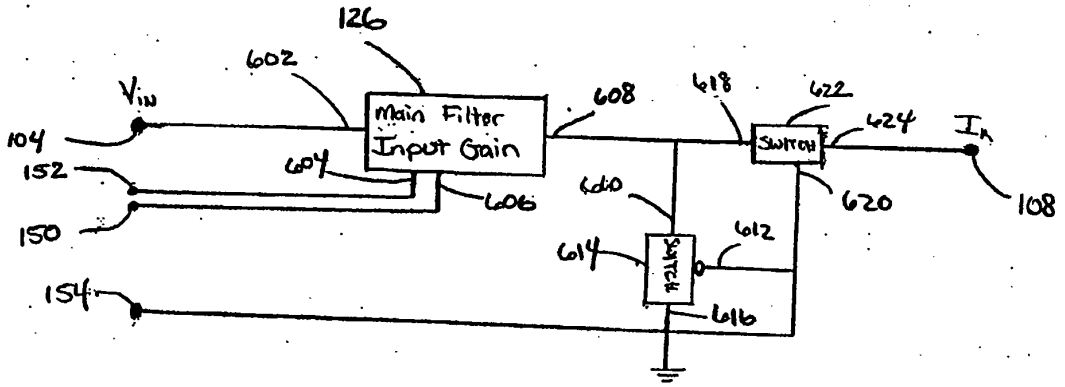
132

FIG. 4


181
178
179
512
518
510
522
514
516
SWITCH
526
524
528
530
532
534
536
540
542
544
548
546
502
506
504
508
I_N
136
V_Q
140

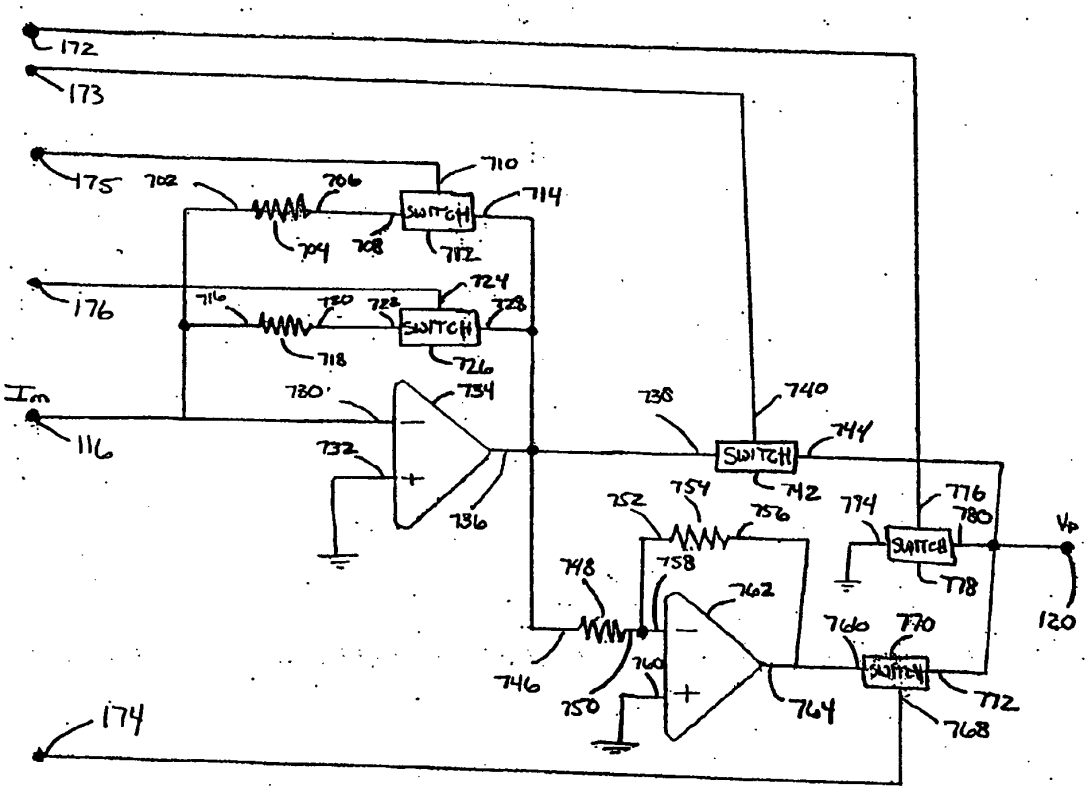
138

FIG. 5


126
602
V_{in}
104
152
150
154
Main Filter
Input Gain
604
606
608
610
612
614
616
618
622
624
Switch
620
I_A
108

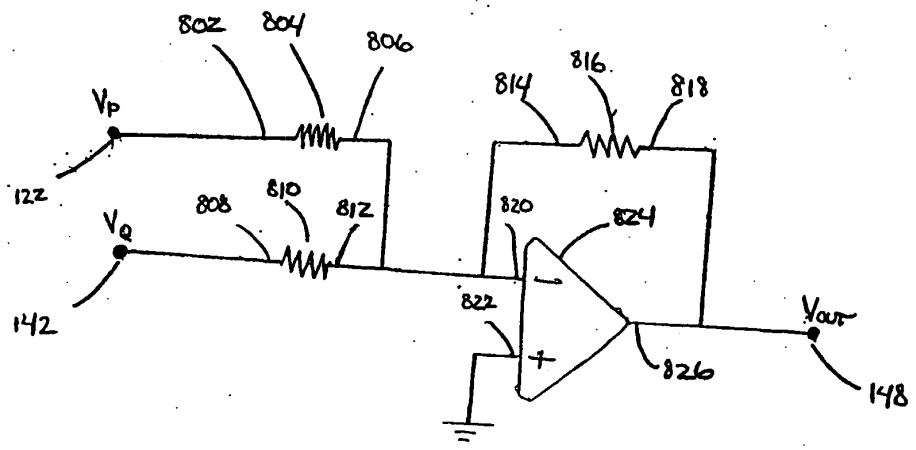
106

FIG. 6


172
173
175
702
706
710
SWITCH
714
704
708
712
176
716
720
722
724
SWITCH
728
718
726
Im
116
730
734
732
736
738
740
SWITCH
744
742
752
754
756
774
776
780
SWITCH
778
Vp
120
748
758
762
760
746
750
764
766
770
SWITCH
772
768
174

1.18

FIG. 7


802
804
806
814
816
818
V_P
122
808
810
812
820
824
V_Q
142
822
V_{OUT}
826
148

144

FIG. 8

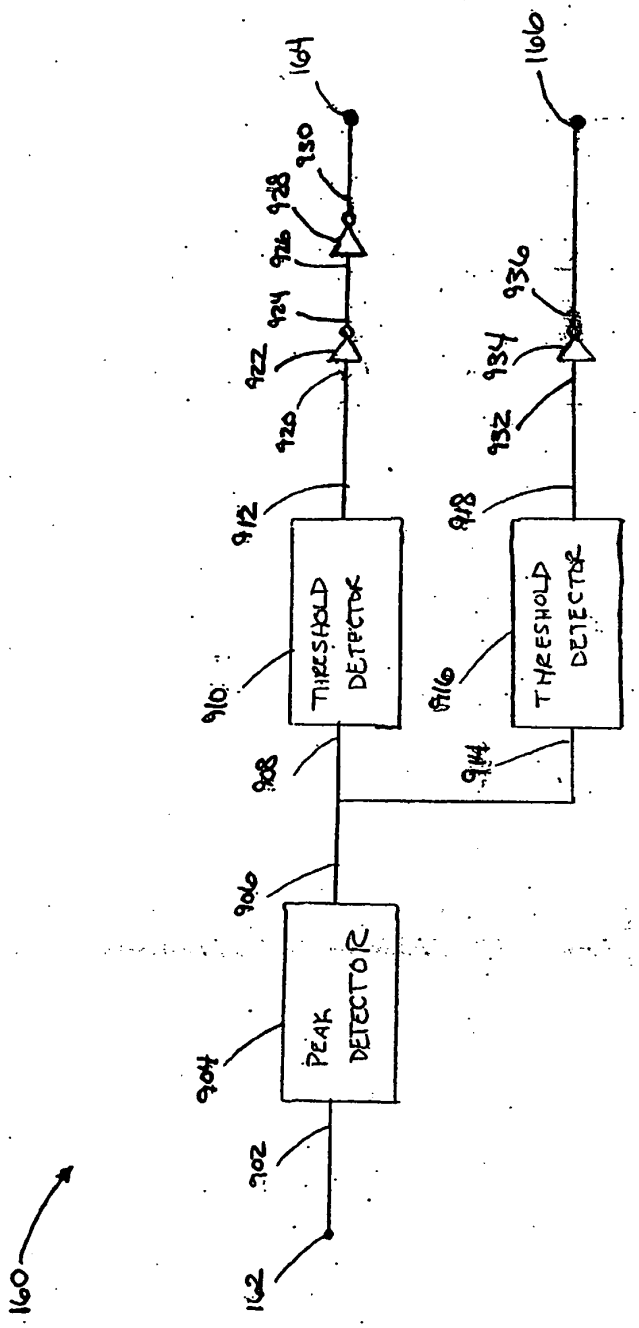
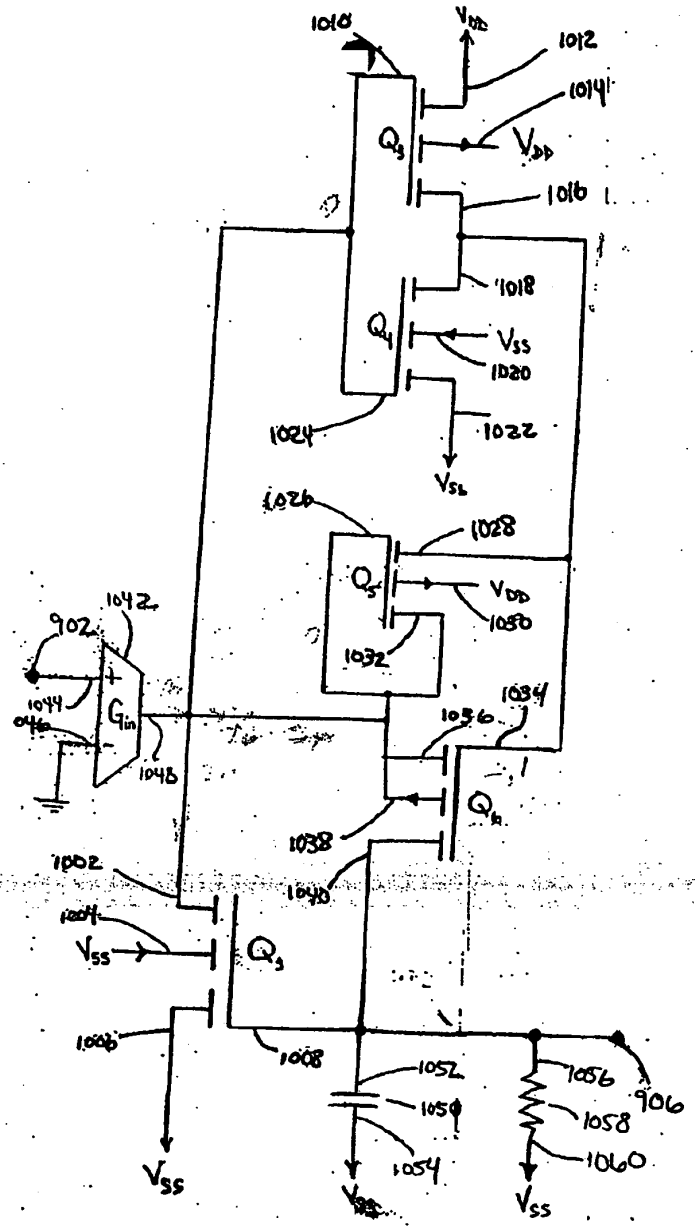
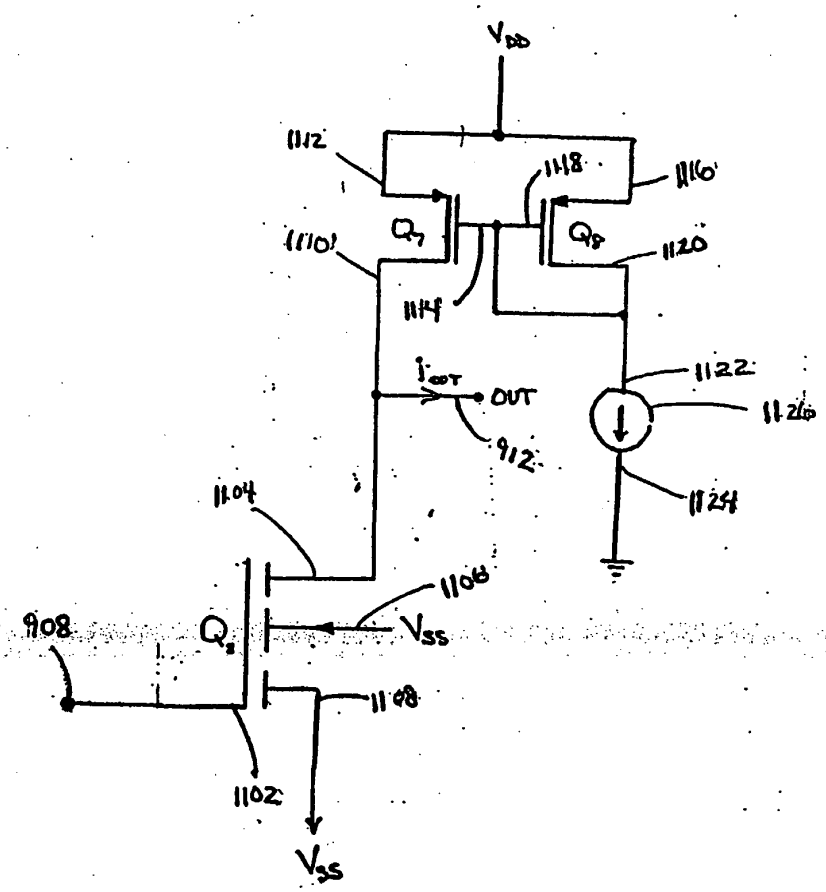

160
162
164
166
902
904
906
908
910
912
914
916
918
920
922
924
926
928
930
932
934
936
PEAK DETECTOR
THRESHOLD DETECTOR
THRESHOLD DETECTOR

Fig. 9


1010
1012
1014
Q_3
V_{DD}
1016
1018
Q_4
V_{SS}
1020
1022
1024
V_{SS}
1026
1028
Q_5
V_{DD}
1030
1032
1034
1036
Q_6
1038
1040
1042
902
1044
G_{in}
1046
1048
1002
1004
V_{SS}
Q_1
1006
1008
1052
1050
1054
V_{SS}
1056
1058
1060
V_{SS}
906

904

Fig. 10


V_{DD}
1112
1118
1116
Q_7
Q_8
1110
1120
1114
i_{OUT}
OUT
912
1122
1124
1104
1106
908
Q_9
V_{SS}
1108
1102
V_{SS}

910

Fig. 11

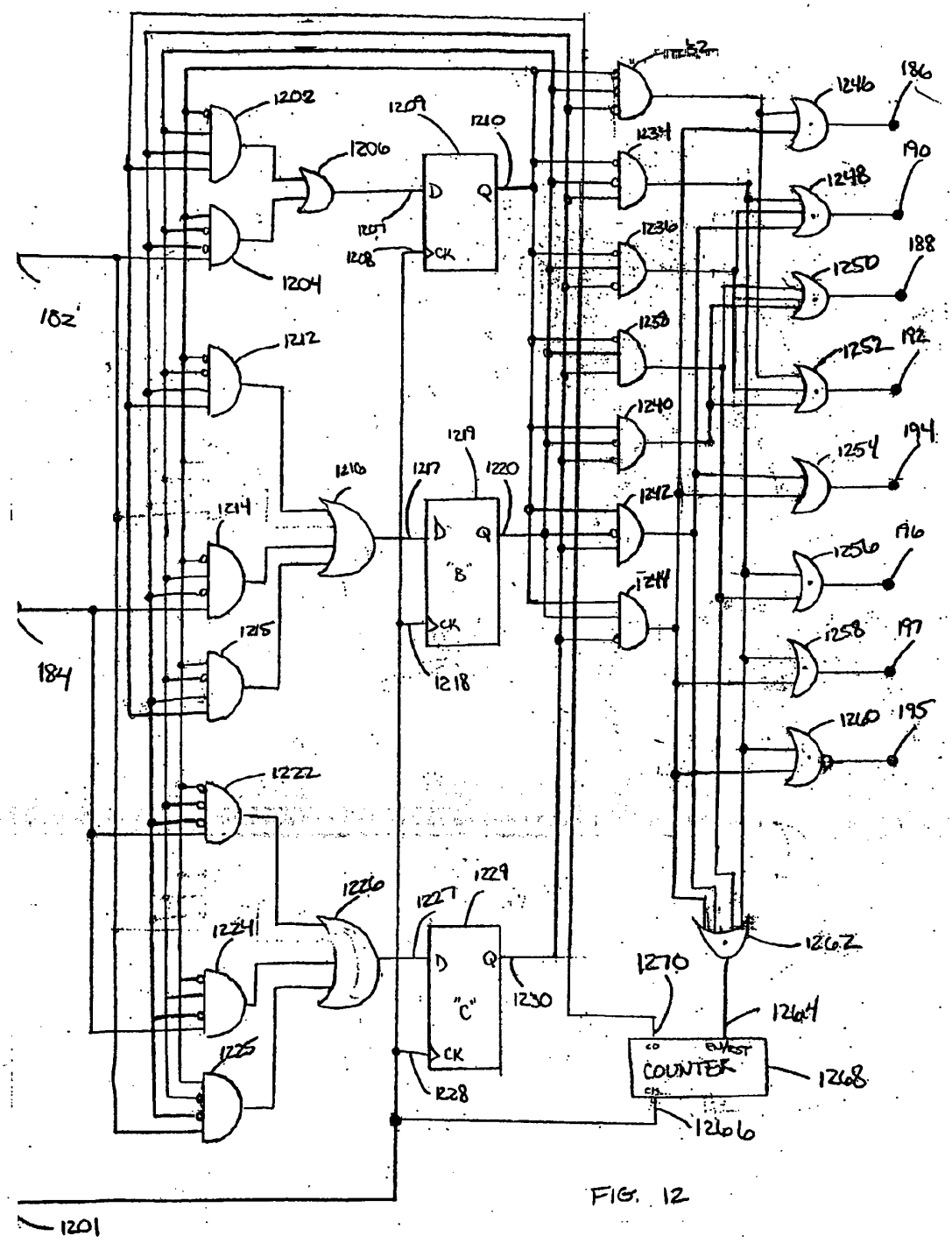
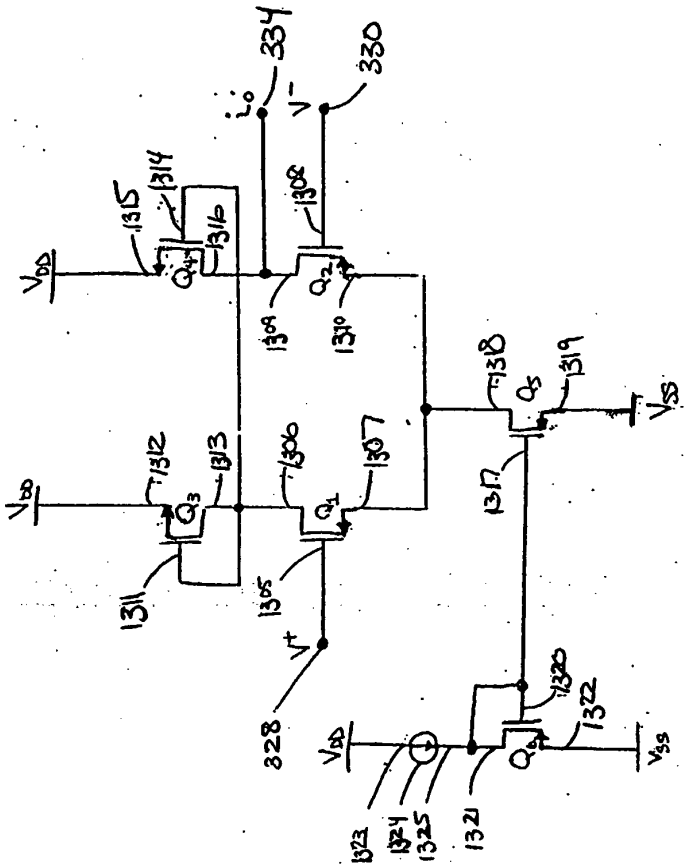
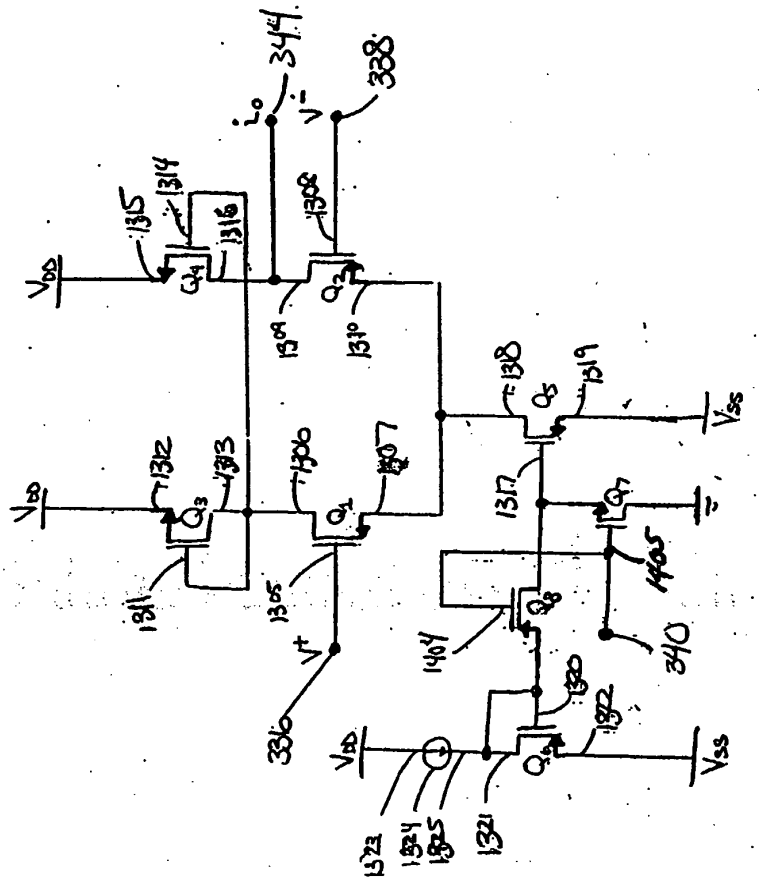

182
184
1201
1202
1204
1206
1207
1208
1209
1210
1212
1214
1215
1216
1217
1218
1219
1220
"B"
1222
1224
1225
1226
1227
1228
1229
1230
"C"
1232
1234
1236
1238
1240
1242
1244
1246
1248
1250
1252
1254
1256
1258
1260
1262
1264
1266
1268
1270
COUNTER
CO
EVENT
CLR
186
190
188
192
194
196
197
195

FIG. 12


334
330
i_0
V^-
1315
1314
1316
1308
V_{DD}
Q_4
Q_2
1309
1310
1318
1319
Q_5
V_{SS}
1312
1313
1306
1307
V_{DD}
Q_3
Q_1
1317
1311
1305
V^+
328
1320
1322
V_{DD}
Q_6
V_{SS}
1323
1324
1325
1321

332 FIG. 13


i0
V-
344
338
1315
1314
1316
1308
VDD
Q4
Q3
1309
1310
1318
Q5
1319
VSS
1312
1313
1306
1307
VB
Q6
Q2
1317
Q7
1311
1305
V+
1404
Q8
340
MOS
330
1322
336
VDD
Q9
VSS
1323
1324
1325
1321

342
FIG. 14

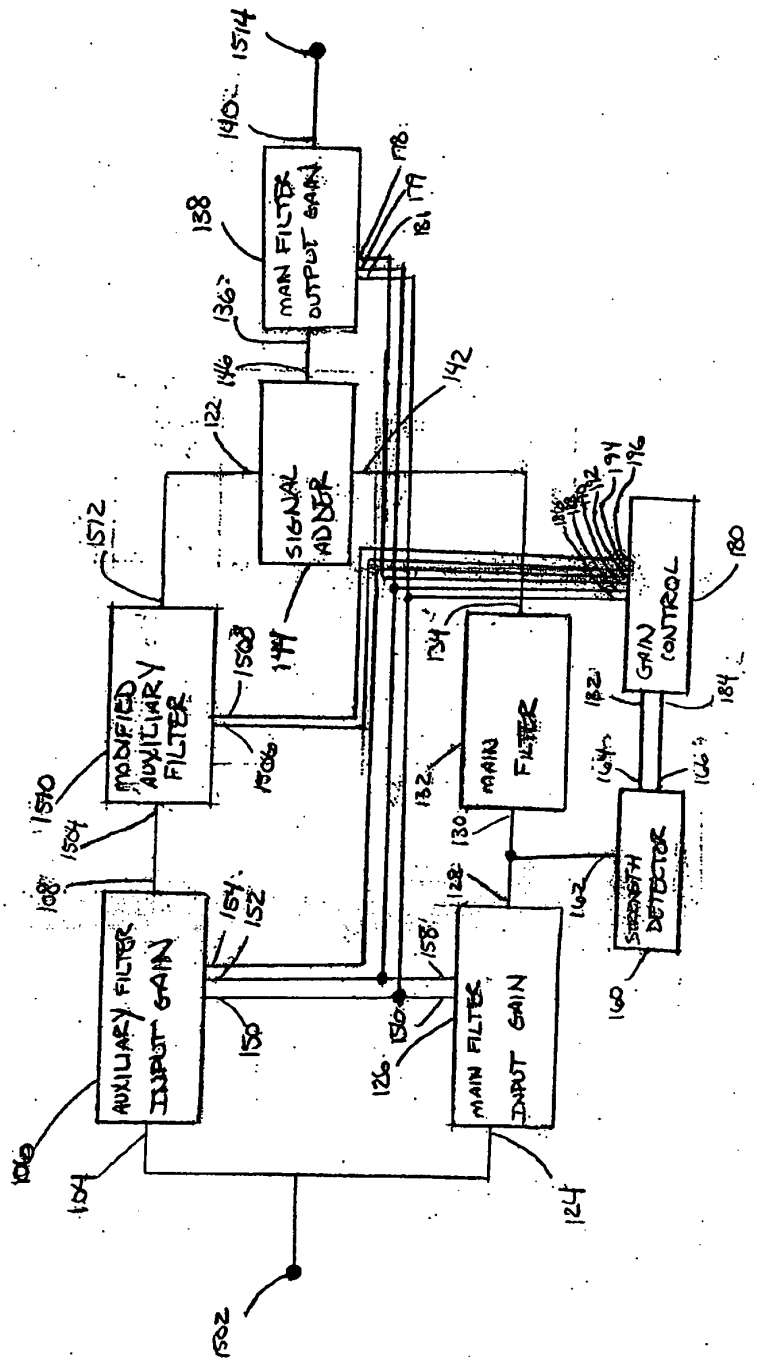
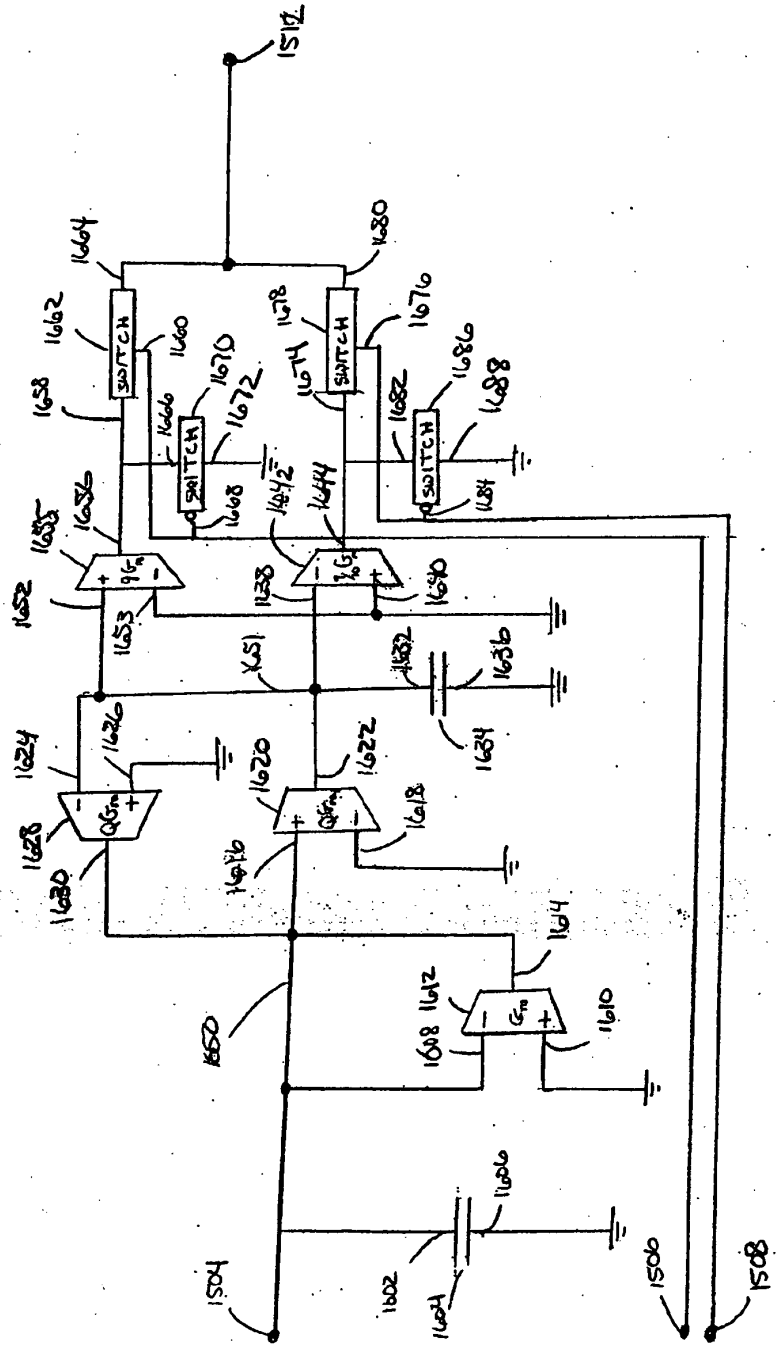
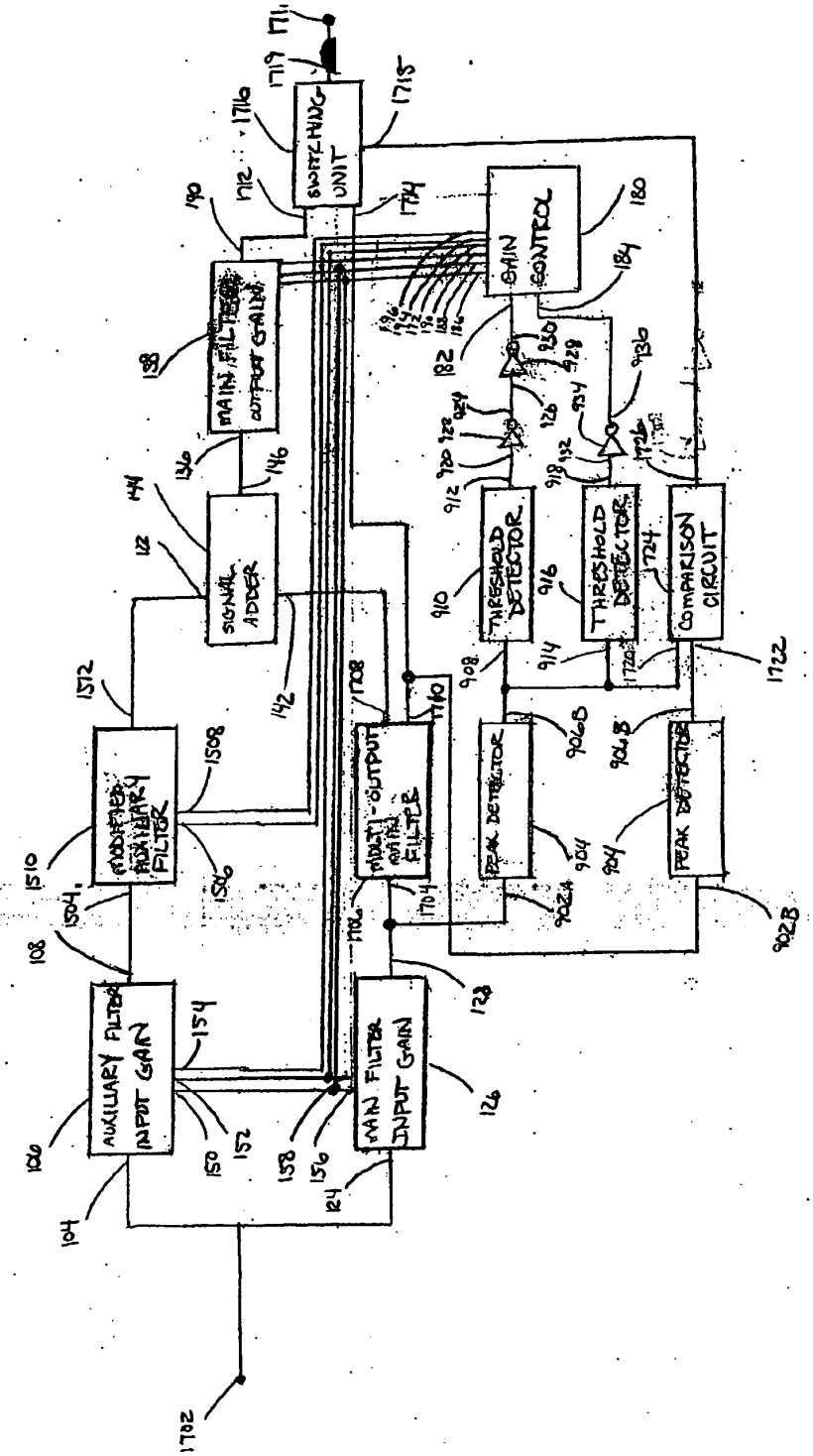

MAIN FILTER OUTPUT GAIN
SIGNAL ADDER
MODIFIED AUXILIARY FILTER
MAIN FILTER
GAIN CONTROL
STRENGTH DETECTOR
AUXILIARY FILTER INPUT GAIN
MAIN FILTER INPUT GAIN

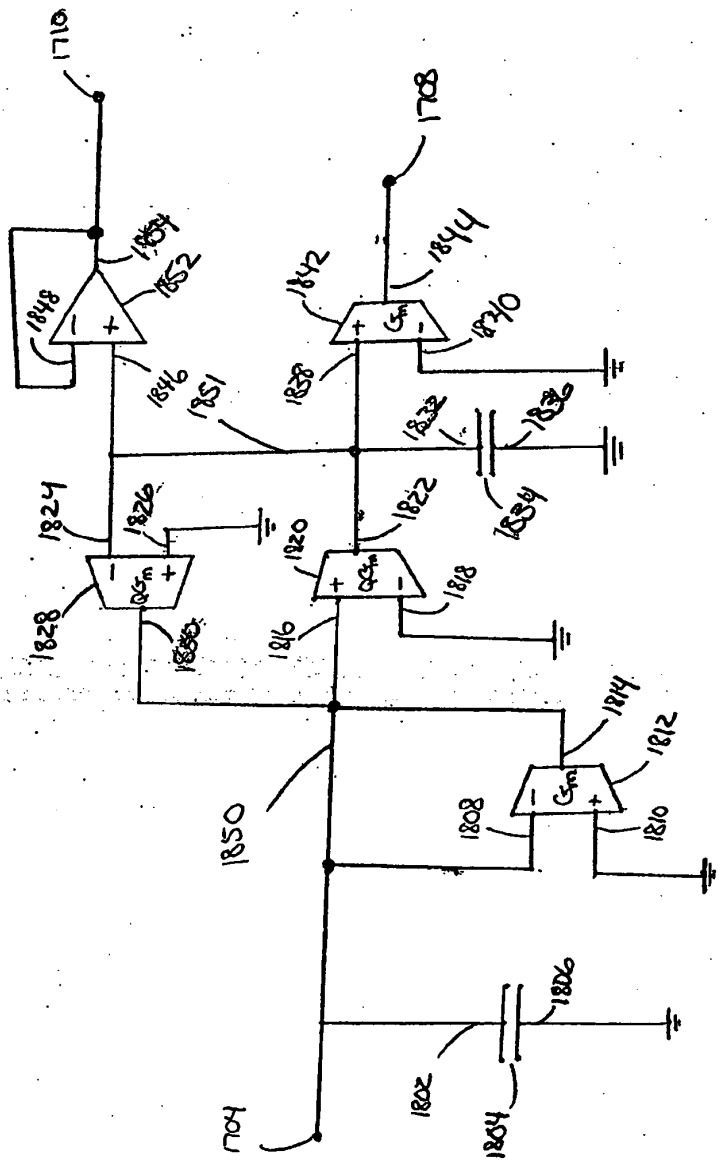
Fig. 15


1512
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SWITCH
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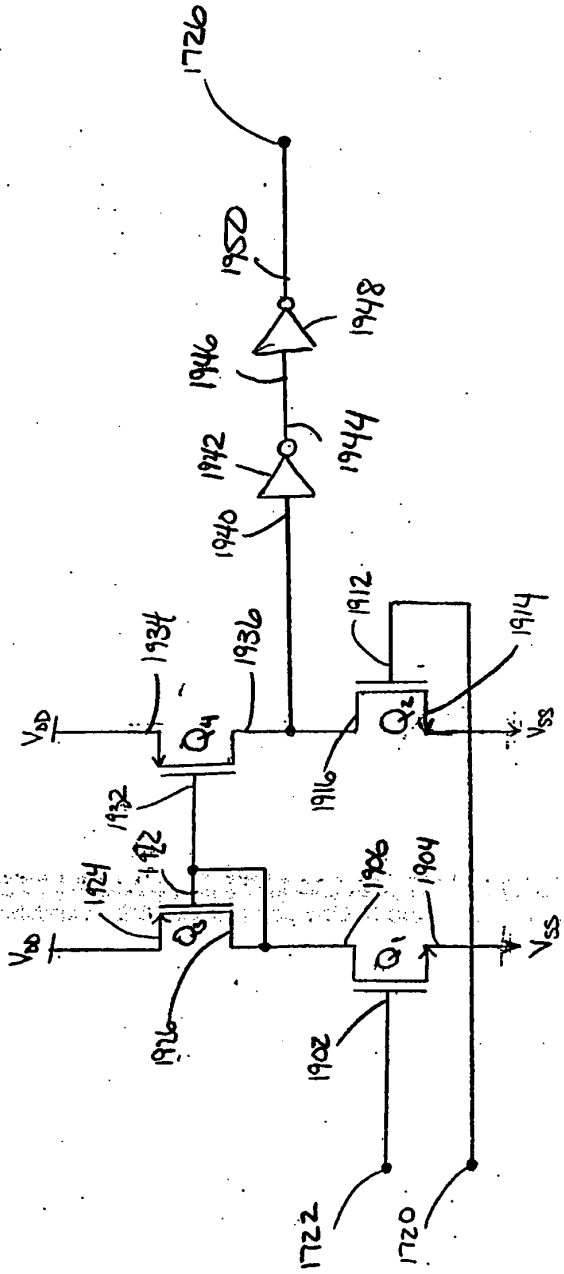
1510
Fig. 16


SWITCHING UNIT
GAIN CONTROL
MAIN FILTER OUTPUT GAIN
SIGNAL ADDER
MODIFIED AUXILIARY FILTER
MAIN OUTPUT FILTER
AUXILIARY FILTER INPUT GAIN
MAIN FILTER INPUT GAIN
THRESHOLD DETECTOR
THRESHOLD DETECTOR
COMPARISON CIRCUIT
PEAK DETECTOR
PEAK DETECTOR

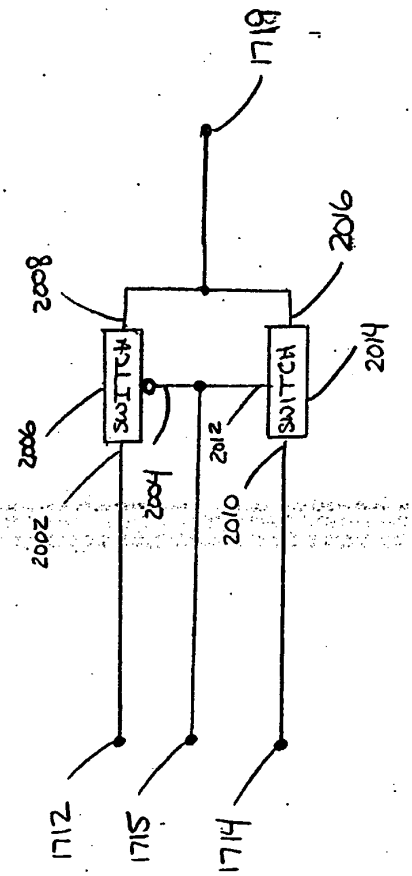
1700
Fig. 17


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1704

1706
Fig. 18

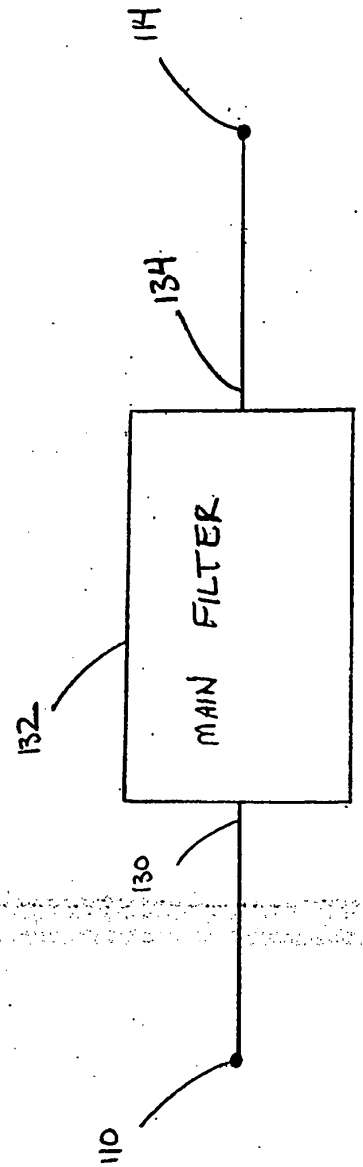

1726
1950
1948
1946
1944
1942
1940
1912
1914
1934
1936
V_{DD}
Q_4
Q_2
V_{SS}
1916
1932
1922
1924
1926
1906
1904
V_{DD}
Q_3
Q_1
V_{SS}
1902
1722
1720

1724
FIG. 19


1718
2006
2008
SWITCH
SWITCH
2014
2004
2012
2002
2010
1712
1715
1714

1716

FIG. 20



112

Fig. 21

07-21-04

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TC1110

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UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NUMBER	FILING OR 371 (c) DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
10/784,613	02/23/2004	Yannis Tsividis	021673-000210US

CONFIRMATION NO. 8357

20350
TOWNSEND AND TOWNSEND AND CREW, LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO, CA 94111-3834

FORMALITIES LETTER

OC000000012717551

Date Mailed: 05/20/2004

NOTICE TO FILE CORRECTED APPLICATION PAPERS

Filing Date Granted

An application number and filing date have been accorded to this application. The application is informal since it does not comply with the regulations for the reason(s) indicated below. Applicant is given TWO MONTHS from the date of this Notice within which to correct the informalities indicated below. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

The required item(s) identified below must be timely submitted to avoid abandonment:

- Replacement drawings in compliance with 37 CFR 1.84 and 37 CFR 1.121 are required. The drawings submitted are not acceptable because:
  - The drawings must be made on paper that has a white background (see 37 CFR 1.84 (e)). For example, drawings on graph paper, lined paper, or paper that has a non-white background are not acceptable. See Figure(s) 2A,3,8B,8D,11D.

Replies should be mailed to: Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

A copy of this notice MUST be returned with the reply.

Y. G

Customer Service Center
Initial Patent Examination Division (703) 308-1202
PART 2 - COPY TO BE RETURNED WITH RESPONSE

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JUL 19 2004
PATENT & TRADEMARK OFFICE

PTO/SB/21 (04-04)

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	10/784,613
Filing Date	February 23, 2004
First Named Inventor	Tsividis, Yannis
Art Unit	2681
Examiner Name	
Total Number of Pages in This Submission: 18	Attorney Docket Number: 021673-000210US

ENCLOSURES *(Check all that apply)*

- ☐ Fee Transmittal Form
- ☐ Fee Attached
- ☐ Amendment/Reply
- ☐ After Final
- ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Response to Missing Parts/ Incomplete Application
- ☒ **Notice to File Corrected Application Papers** (1pg)
- ☒ **FORMAL Drawings** (15pgs)
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
- ☐ Request for Refund
- ☐ CD, Number of CD(s) _____
- ☐ After Allowance Communication to Technology Center (TC)
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☐ Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- ☐ Proprietary Information
- ☐ Status Letter
- ☒ Other Enclosure(s) (please identify below):
  1. **This PTO/SB/21 Transmittal Form** (1pg)
  2. **Return Postcard** (1pg)

Remarks: The Commissioner is authorized to charge any additional fees to Deposit Account 20-1430.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Townsend and Townsend and Crew LLP J. Matthew Zigmant Reg. No. 44,005
Signature	J. Matthew Zigmant
Date	July 19, 2004

CERTIFICATE OF TRANSMISSION/MAILING

Express Mail Label: **EV 323 383 709 US**

I hereby certify that this correspondence is being deposited with the United States Postal Service with "Express Mail Post Office to Address" service under 37 CFR 1.10 on this date **July 19, 2004** and is addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below.

Typed or printed name	Ron Anton		
Signature	Ron Anton	Date	July 19, 2004

60263324 v1

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JUL 1 9 2004
PATENT & TRADEMARK OFFICE

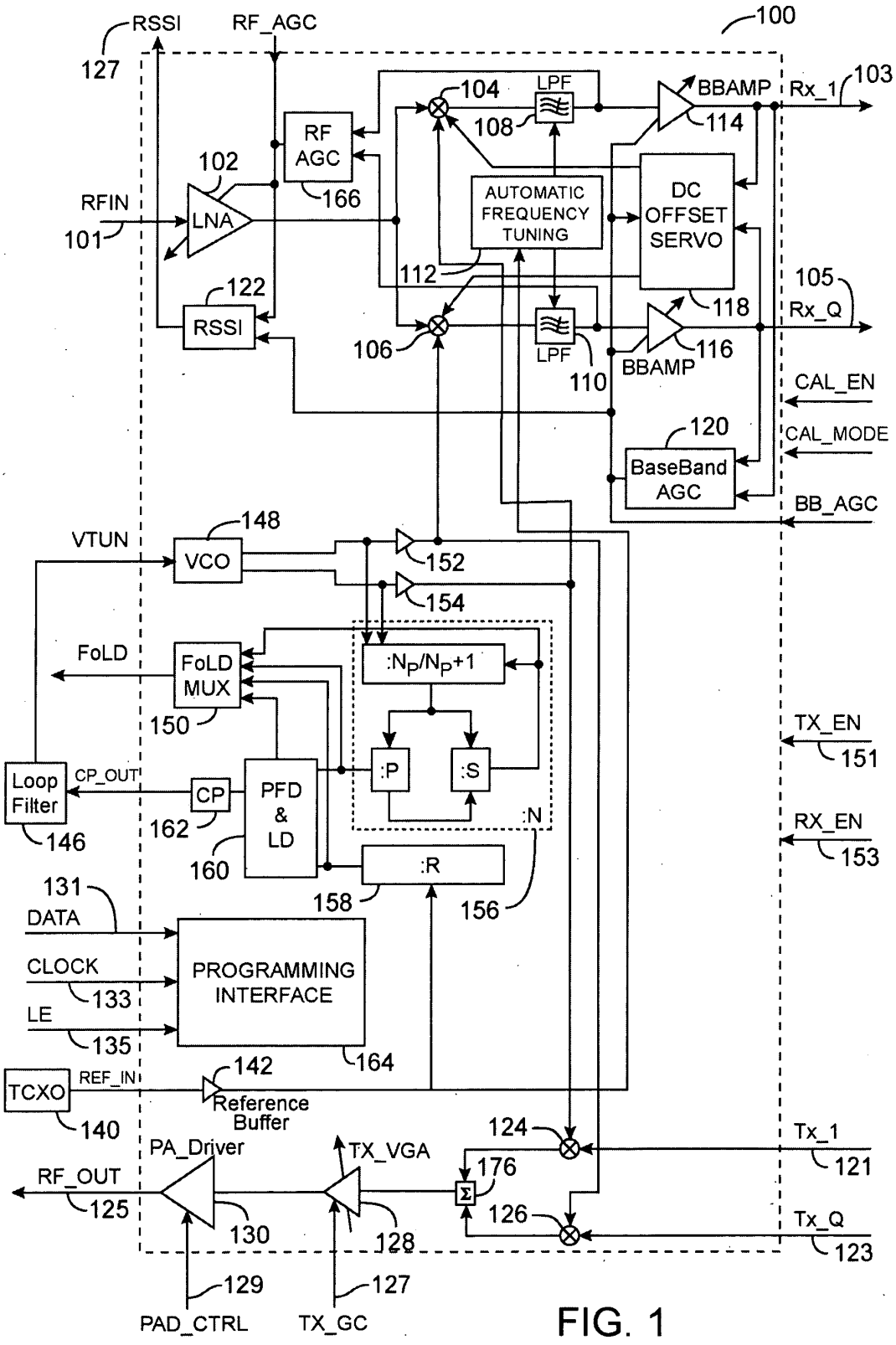


FIG. 1

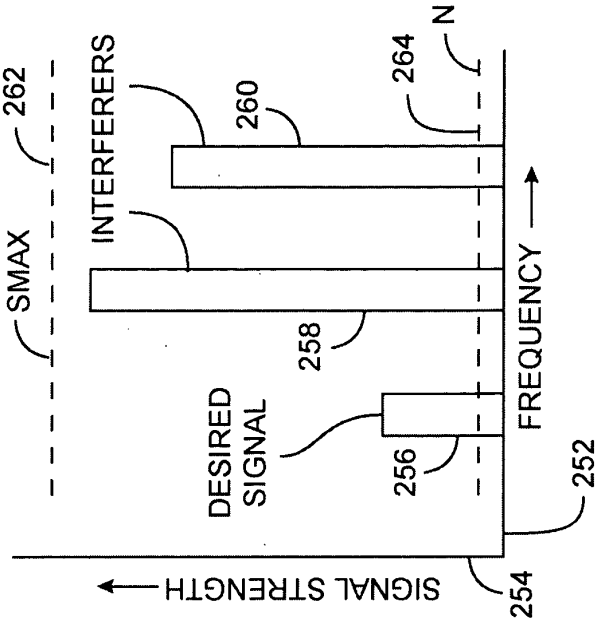

SIGNAL STRENGTH
FREQUENCY
DESIRED SIGNAL
INTERFERERS
SMAX
N
252
254
256
258
260
262
264

FIG. 2B

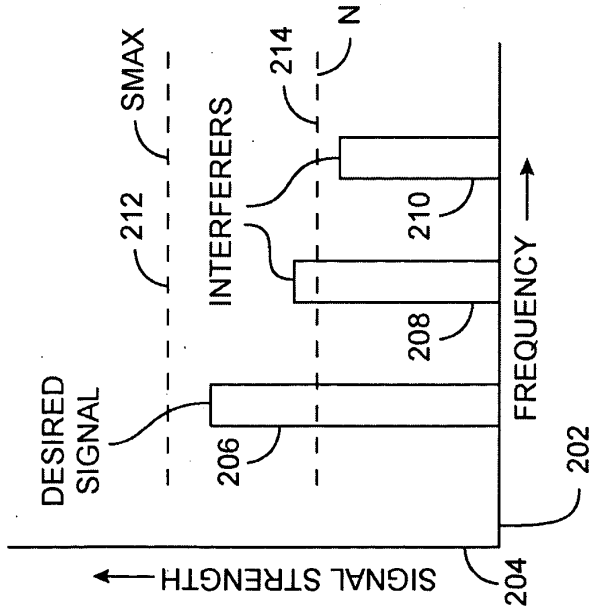

SIGNAL STRENGTH
FREQUENCY
DESIRED SIGNAL
INTERFERERS
SMAX
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202
204
206
208
210
212
214

FIG. 2A

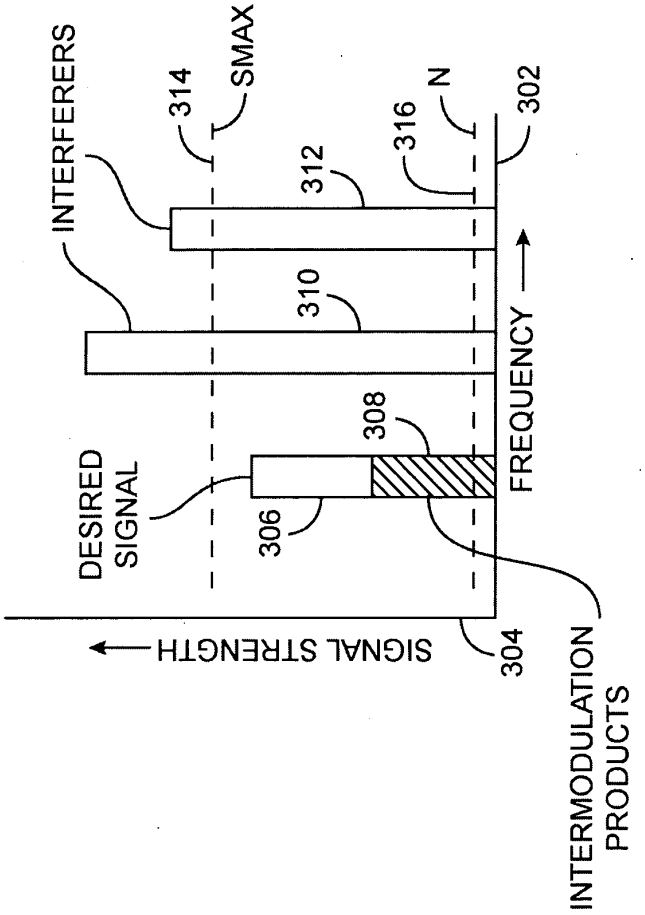

INTERFERERS
314
SMAX
312
316
N
302
310
FREQUENCY
308
DESIRED SIGNAL
306
SIGNAL STRENGTH
304
INTERMODULATION PRODUCTS

FIG. 3

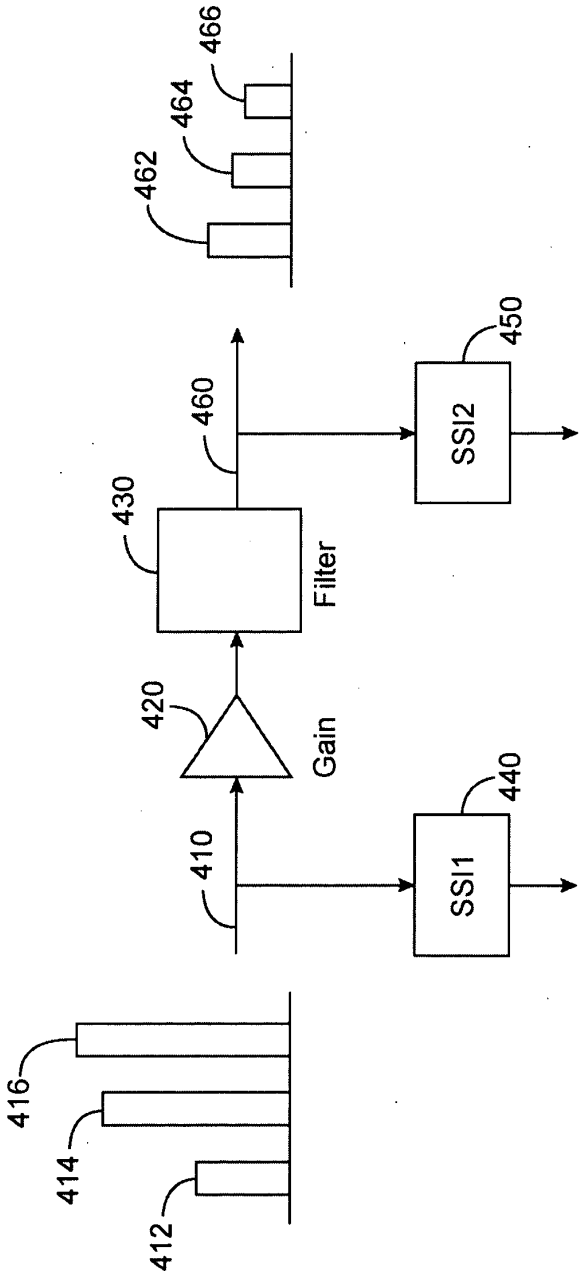

466
464
462
450
460
SSI2
430
Filter
420
Gain
440
410
SSI1
416
414
412

FIG. 4

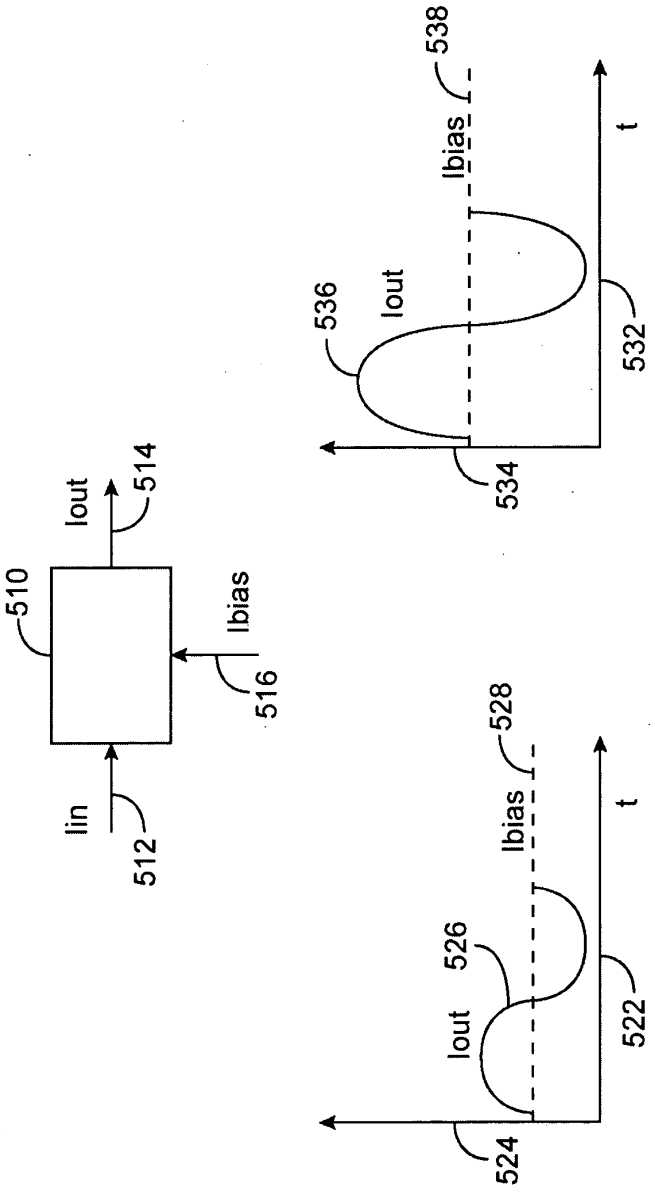

538
Ibias
t
536
Iout
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534
Iout
514
510
Ibias
516
Iin
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528
Ibias
t
526
Iout
522
524

FIG. 5

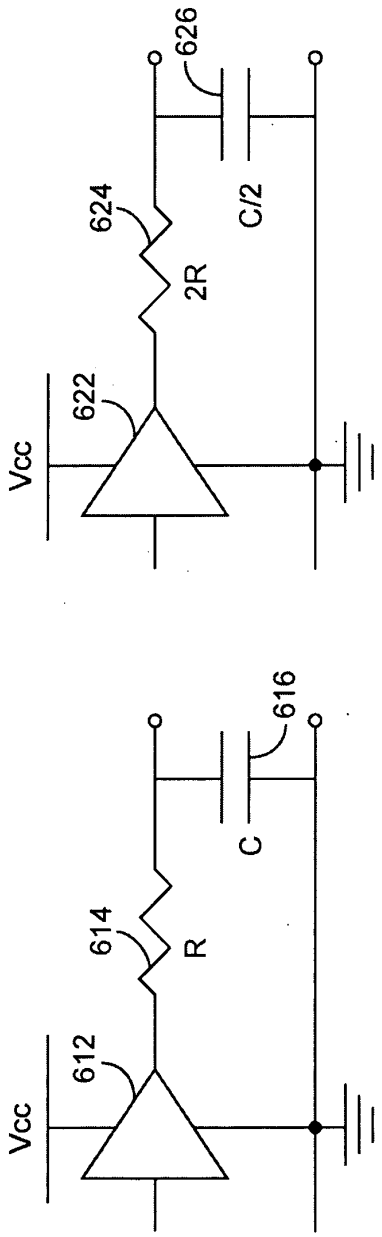


FIG. 6

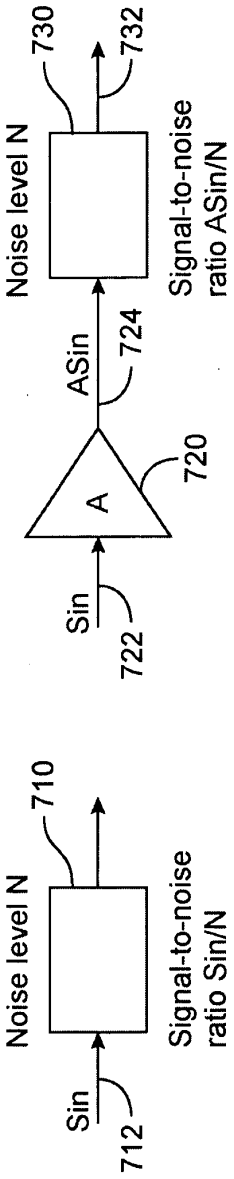

Noise level N
710
Signal-to-noise ratio Sin/N
Sin
712
Noise level N
730
732
Signal-to-noise ratio ASin/N
ASin
724
A
720
Sin
722

FIG. 7

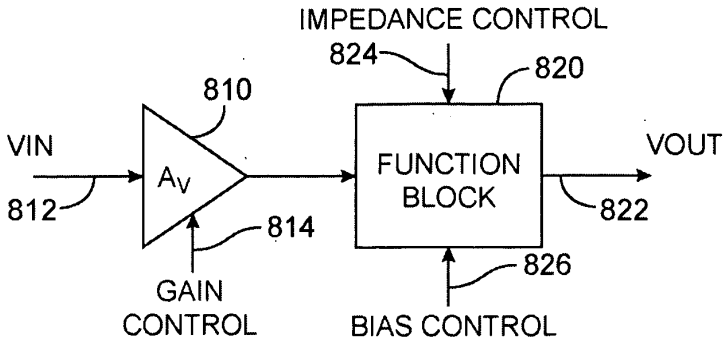


FIG. 8A

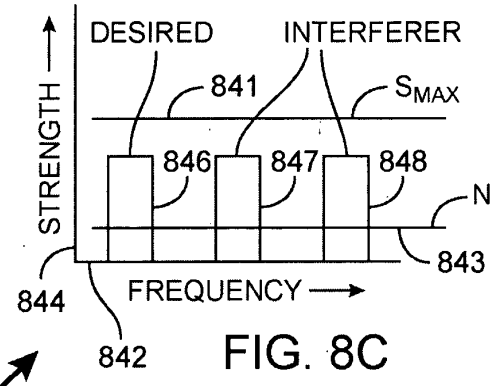


FIG. 8C

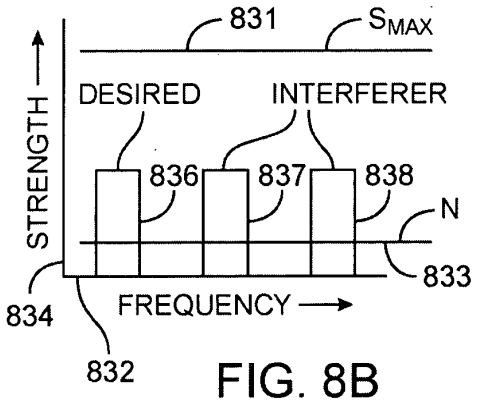


FIG. 8B

DECREASE BIASING

– AND/OR –

INCREASE GAIN AND IMPEDANCES

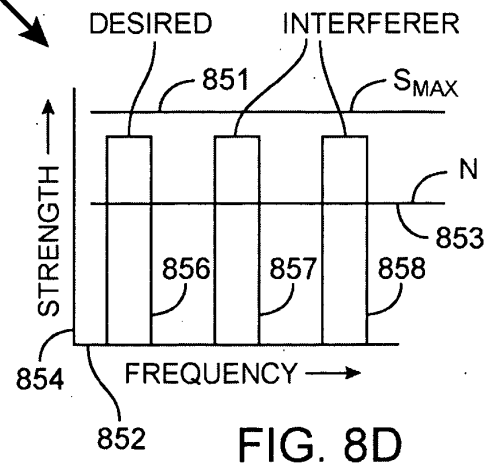


FIG. 8D

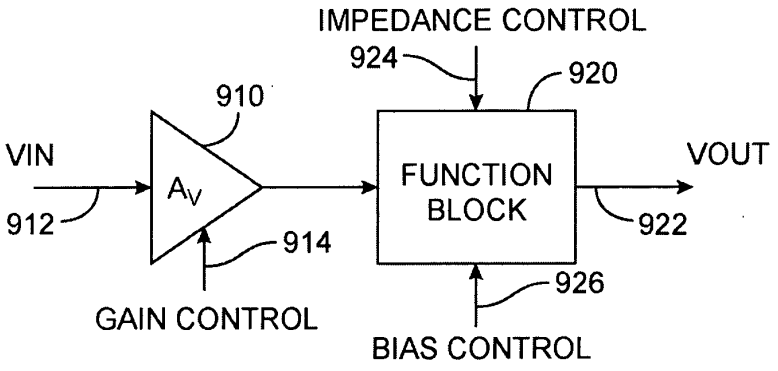


FIG. 9A

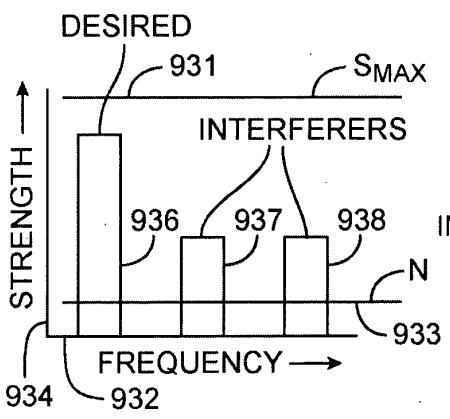


FIG. 9B

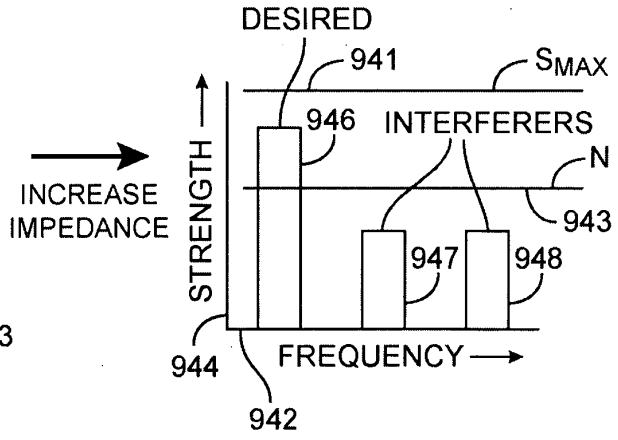


FIG. 9C

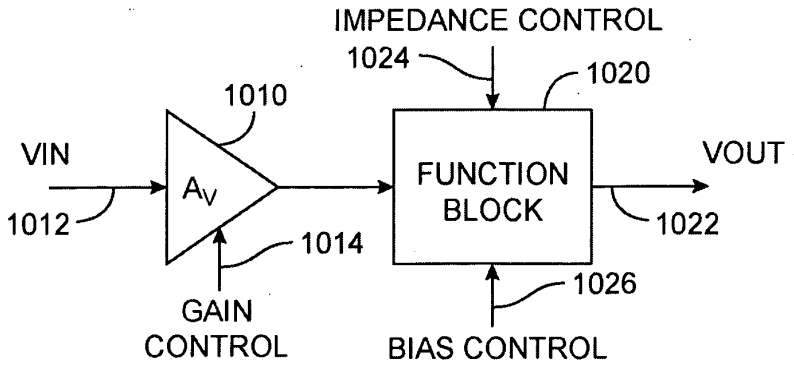


FIG. 10A

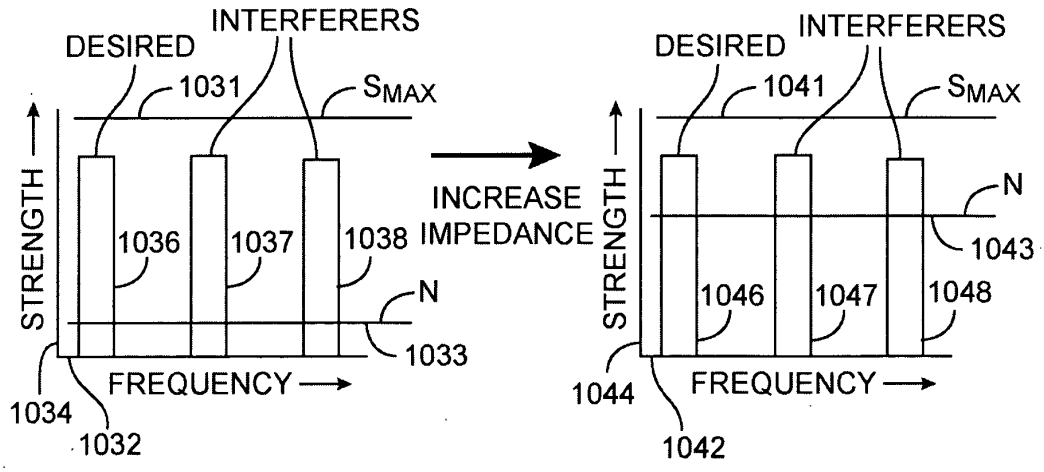


FIG. 10B

FIG. 10C

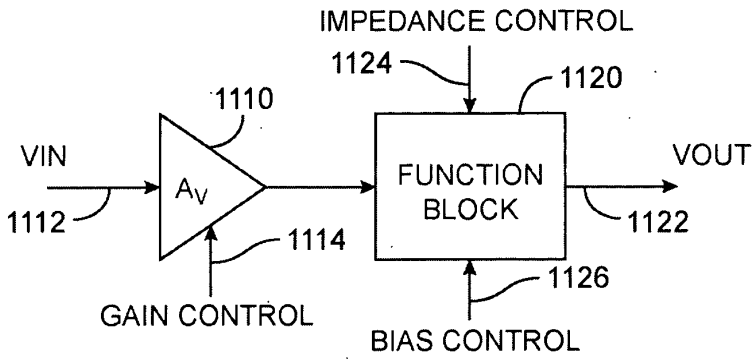


FIG. 11A

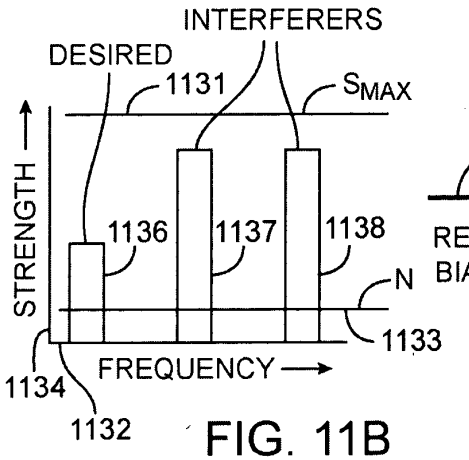


FIG. 11B

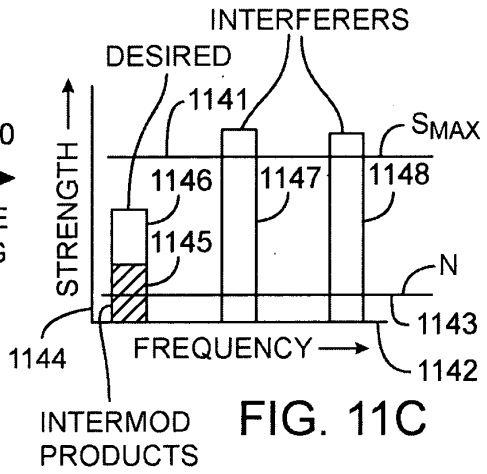
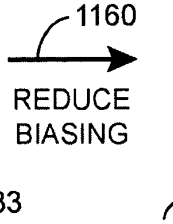
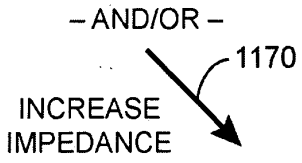


FIG. 11C





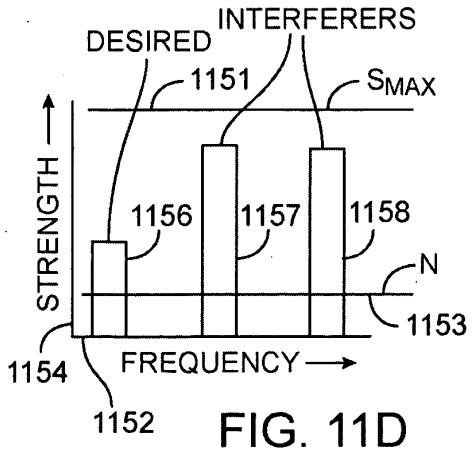


FIG. 11D

	1210 RECEIVED SIGNAL		1220 RESPONSE TO RECEIVED SIGNAL		
	SIGNAL STRENGTH	INTERFERER STRENGTH	DECREASE SMAX	INCREASE IMPEDANCE NOT GAIN	INCREASE IMPEDANCE AND GAIN
1230	SMALL	SMALL	YES	NO	YES
1240	LARGE	SMALL	NO	YES	NO
1250	LARGE	LARGE	NO	YES	NO
1260	SMALL	LARGE	NO	NO	NO

FIG. 12

IPR2024-00816
Apple EX1002 Page 280
IPR2023-00819
Theta EX2019

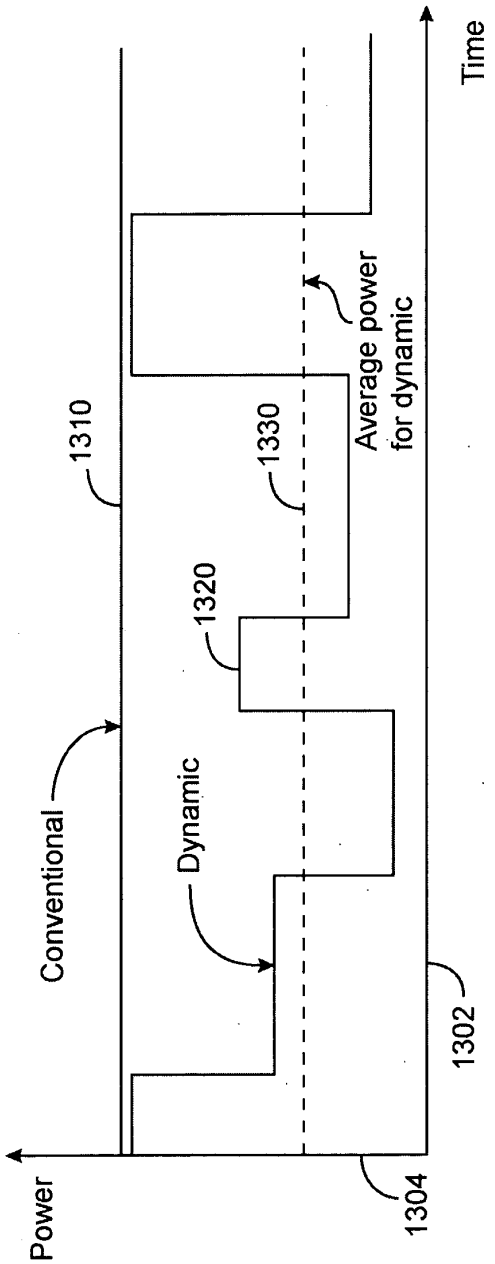

Time
Power
Conventional
Dynamic
1310
1320
1330
1302
1304
Average power
for dynamic

FIG. 13

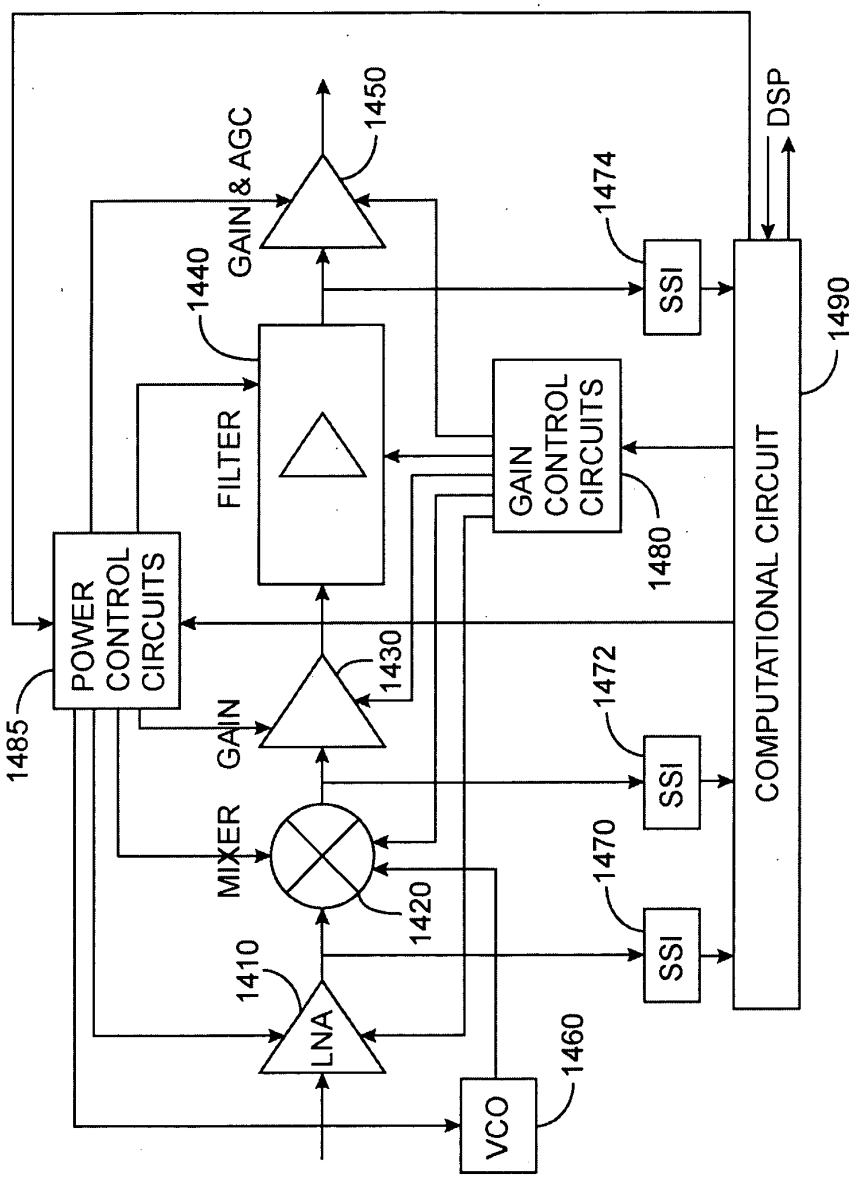

1450
GAIN & AGC
1440
FILTER
1430
GAIN
MIXER
1420
1410
LNA
1460
VCO
1485
POWER CONTROL CIRCUITS
GAIN CONTROL CIRCUITS
1480
1474
1472
1470
SSI
SSI
SSI
1490
COMPUTATIONAL CIRCUIT
DSP

FIG. 14

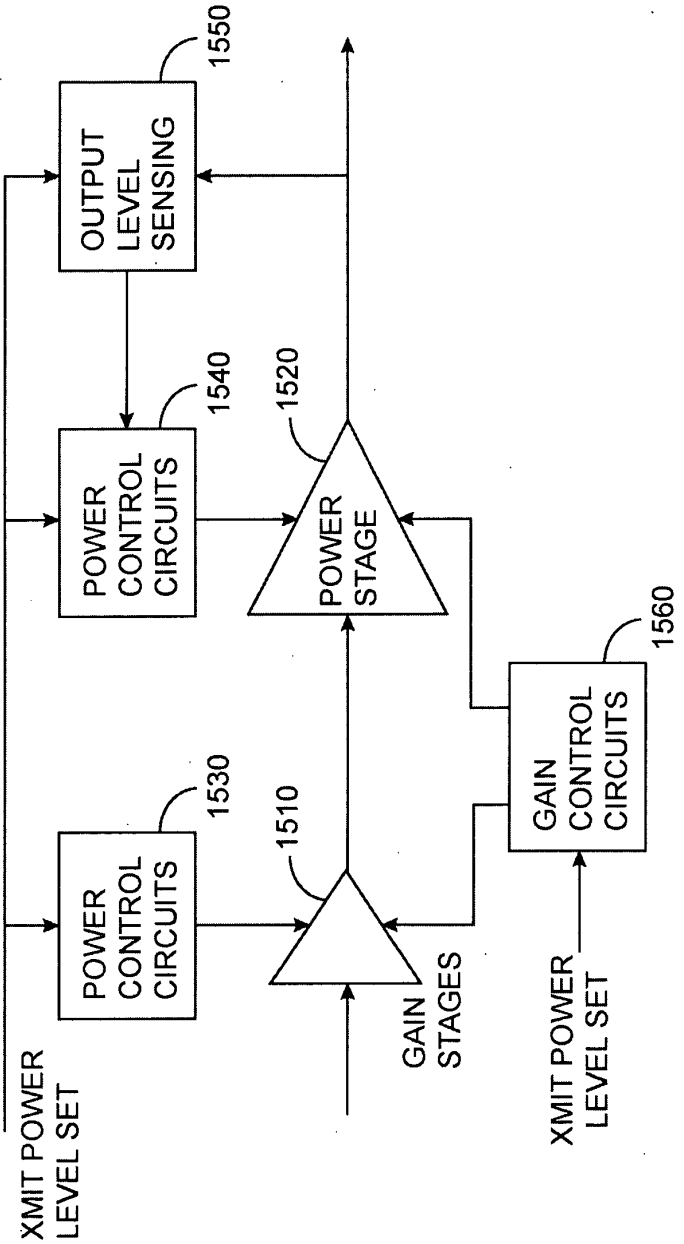

1550
OUTPUT LEVEL SENSING
1540
POWER CONTROL CIRCUITS
1520
POWER STAGE
1530
POWER CONTROL CIRCUITS
1510
GAIN STAGES
1560
GAIN CONTROL CIRCUITS
XMIT POWER LEVEL SET
XMIT POWER LEVEL SET

FIG. 15

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United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/784,613	02/23/2004	Yannis Tsividis	021673-000210US	8357

20350 7590 01/05/2005

TOWNSEND AND TOWNSEND AND CREW, LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO, CA 94111-3834

EXAMINER	
VUONG, QUOCHIEN B	

ART UNIT	PAPER NUMBER
2685	

DATE MAILED: 01/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/784,613	TSIVIDIS, YANNIS	
	Examiner	Art Unit	
	Quochien B Vuong	2685	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/02/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

IPR2024-00816
Apple EX1002 Page 285
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Theta EX2019

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 07/02/2004 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 17, 23-25, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Clark (US 5,001,776) in view of Okanobu (US 5,020,147).

Regarding claims 1 and 23, Clark (figure 1) discloses a wireless transceiver circuit and a method of receiving a signal using a circuit, the circuit comprising a signal path including a low-noise amplifier (108) configured to receive the signal, a mixer (110) having an input coupled to an output of the low-noise amplifier, and a low-pass filter (120) having an input coupled to an output of the mixer, the method comprising: determining a first signal strength (126) at a first node in the signal path in the circuit; and dynamically changing a peak-to-peak voltage and current consumption of component (mixer 110) in the signal path based on the first signal strength (column 2, line 34 – column 4, line 66). Clark does not specifically disclose the circuit is an

integrated circuit, and dynamically changing an impedance of the component in the signal path. However, since Clark disclose dynamically changing the peak-to-peak voltage and current consumption of component in the signal path based on the first signal strength, therefore, it would be obvious for the transceiver and method of Clark to dynamically change the impedance of the component as well in order to reduce signal interference or distortion. In addition, Okanobu discloses a circuit formed on an integrated circuit (see figure 1, column 7, lines 30-32). Therefore, it would have been obvious for one having ordinary skill in the art at the time the invention was made to adapt the teaching of Okanobu to the transceiver and method of Clark in order to reduce the size of the circuit for compact design.

Regarding claims 17 and 29, Clark (figure 1) discloses a wireless transceiver circuit and a method of receiving a signal using a circuit, the circuit comprising a signal path including a first circuit (including 104, 108) and a second circuit (the rest of the transceiver in figure 1) having an input coupled to an output of the first circuit, the method comprising: determining a first signal strength (126) at a first node in the signal path in the circuit, wherein the first node is before the first circuit in the signal path; and dynamically changing a gain of the first circuit (108) based on the first signal strength (column 4, lines 30-43) (column 2, line 34 – column 4, line 66). Clark does not specifically disclose the circuit is an integrated circuit, and dynamically changing an impedance of the second circuit. However, since Clark disclose dynamically changing the peak-to-peak voltage and current consumption of the second circuit based on the first signal strength (column 3, line 58 – column 4, line 3), therefore, it would be obvious

for the transceiver and method of Clark to dynamically change the impedance of the second circuit as well in order to reduce signal interference or distortion. In addition, Okanobu discloses a circuit formed on an integrated circuit (see figure 1, column 7, lines 30-32). Therefore, it would have been obvious for one having ordinary skill in the art at the time the invention was made to adapt the teaching of Okanobu to the transceiver and method of Clark in order to reduce the size of the circuit for compact design.

As to claims 24 and 25, Clark discloses a second signal strength indicator circuit (126') coupled to the output of the mixer (110) or low-pass filter (120), and configured to determined s second signal strength, wherein the impedance in the signals path is configured to be adjusted in response to the first and second signal strength (column 3, lines 6-49).

4. Claims 2-16, 18-22, and 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Clark (US 5,001,776) in view of Okanobu (US 5,020,147) and further in view of Smith et al. (US 6,714,557).

Regarding claim 2, the combination of Clark and Okanobu does not disclose the signal comprises a preamble portion and a data portion, the impedance of a component is changed while receiving the preamble portion, and the method further comprises receiving the data portion of the signal. However, Smith et al. (figure 1) disclose a signal comprising a preamble portion (112) and a data portion (114, 204, 206) (column 5, lines 29-45). Therefore, it would have been obvious to adapt the signal of Smith et al. to the

method of Clark and Okanobu to adjust the setting of the component during receiving the preample portion in order to properly receive the data portion.

As to claims 3 and 4, Clark (figure 1) discloses determining a second signal strength (126') at a second node in the signal path, wherein the second node in the signal path is after the first node, wherein the impedance of the component in the signal path is also changed based on the second signal strength (column 3, lines 6-49).

As to claims 5-9, Clark discloses the component in the signal path is included in the mixer (110), and it would be obvious for the component in the signal path to comprise a MOS transistor, resistor, capacitor, or a low-pass filter, since these components are well known in the transceiver circuit.

Regarding claims 10 and 26, Clark (figure 1) discloses a wireless transceiver circuit and a method of receiving a signal using a circuit, the circuit comprising a signal path including a low-noise amplifier (108) configured to receive the signal, a mixer (110) having an input coupled to an output of the low-noise amplifier, and a low-pass filter (120) having an input coupled to an output of the mixer, the method comprising: determining a first signal strength (126) at a first node in the signal path in the circuit; and dynamically changing a peak-to-peak voltage and current consumption in the signal path based on the first signal strength (column 2, line 34 – column 4, line 66). Clark does not specifically disclose the circuit is an integrated circuit; dynamically changing a bias current in the signal path while receiving a preample portion of the signal. However, since Clark disclose dynamically changing the peak-to-peak voltage and current consumption of component in the signal path based on the first signal strength,

therefore, it would be obvious for the transceiver and method of Clark to dynamically change the bias current as well in order to reduce signal interference or distortion. In addition, Okanobu discloses a circuit formed on an integrated circuit (see figure 1, column 7, lines 30-32). Therefore, it would have been obvious for one having ordinary skill in the art at the time the invention was made to adapt the teaching of Okanobu to the transceiver and method of Clark in order to reduce the size of the circuit for compact design. The combination of Clark and Okanobu does not disclose the signal comprises a preamble portion and a data portion, the impedance of a component is changed while receiving the preamble portion, and the method further comprises receiving the data portion of the signal. However, Smith et al. (figure 1) disclose a signal comprising a preamble portion (112) and a data portion (114, 204, 206) (column 5, lines 29-45). Therefore, it would have been obvious to adapt the signal of Smith et al. to the method of Clark and Okanobu to adjust the setting of the component during receiving the preample portion in order to properly receive the data portion.

As to claim 11, Smith et al. disclose the method further comprises receiving the data portion of the signal (column 5, lines 29-45).

As to claims 12 and 13, Clark (figure 1) discloses determining a second signal strength (126') at a second node in the signal path, wherein the second node in the signal path is after the first node, wherein the bias current in the signal path is also changed based on the second signal strength (column 3, lines 6-49).

As to claims 14-16, Clark discloses the component in the signal path is included in the mixer (110), and it would be obvious for the component in the signal path to

comprise a low-noise amplifier or a low-pass filter, since these components are well known in the transceiver circuit.

As to claim 18, the combination of Clark and Okanobu does not disclose the signal comprises a preamble portion and a data portion, the impedance of a component is changed while receiving the preamble portion, and the method further comprises receiving the data portion of the signal. However, Smith et al. (figure 1) disclose a signal comprising a preamble portion (112) and a data portion (114, 204, 206) (column 5, lines 29-45). Therefore, it would have been obvious to adapt the signal of Smith et al. to the method of Clark and Okanobu to adjust the setting of the component during receiving the preample portion in order to properly receive the data portion.

As to claims 19 and 20, Clark (figure 1) discloses determining a second signal strength (126') at a second node in the signal path, wherein the second node in the signal path is after the first node, wherein the impedance of the component in the signal path is also changed based on the second signal strength (column 3, lines 6-49).

As to claims 27 and 28, Clark discloses a second signal strength indicator circuit (126') coupled to the output of the mixer (110) or low-pass filter (120), and configured to determined s second signal strength, wherein the impedance in the signals path is configured to be adjusted in response to the first and second signal strength (column 3, lines 6-49).

5. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Clark (US 5,001,776) in view of Okanobu (US 5,020,147) and further in view of Park (US 5,995,853).

Regarding claim 30, Clark further discloses the transceiver comprising a transmitter (figure 1, transmitter 144). The combination of Clark and Okanobu does not disclose the transmitter comprising a power amplifier and an output-level-sensing circuit coupled to an output of the power amplifier, wherein the output-level-sensing circuit is configured to dynamically adjust a gain of the power amplifier. However, Park (figure 1) discloses a transmitter (100) comprising a power amplifier (160) and an output-level-sensing circuit (124) coupled to an output of the power amplifier, wherein the output-level-sensing circuit is configured to dynamically adjust a gain of the power amplifier (column 3, line 60 – column 4, line 28). Therefore it would have been obvious for one having ordinary skill in the art at the time the invention was made to adapt the teaching of Park to the combination of Clark and Okanobu in order to control the transmission power.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Snider et al. (US 5,867,063) disclose a gain distribution circuit.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quochien B Vuong whose telephone number is (703) 306-4530. The examiner can normally be reached on M-F 9:30-18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Urban can be reached on (703) 305-4385. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Quochien B Vuong

QUOCHIEN B. VUONG
PRIMARY EXAMINER

Quochien B. Vuong
Dec. 23, 2004.

OIPE JC56
JUL 02 2004
PATENT & TRADEMARK OFFICE

PTO/SB/08A (08-03)

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 2

Complete if Known	
Application Number	10/784,613
Filing Date	02/23/2004
First Named Inventor	Tsividis, Yannis
Art Unit	2685
Examiner Name	QUOCHIEN VUONG
Attorney Docket Number	021673-000210US

U.S. PATENT DOCUMENTS+

Examiner Initials*	Cite No.[1]	Document Number Number Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
QV	AA	US-4,270,222	05-26-1981	Menant	
	AB	US-5,001,776	03-19-1991	Clark	
	AC	US-5,390,357	02-14-1995	Nobusawa	
	AD	US-5,392,457	02-21-1995	Davis et al.	
	AE	US-5,406,613	04-11-1995	Peponides et al.	
	AF	US-5,564,094	10-08-1996	Anderson et al.	
	AG	US-5,600,271	02-04-1997	Erickson et al.	
	AH	US-6,026,288	02-15-2000	Bronner	
	AI	US-6,389,445	05-14-2002	Tsividis	
	AJ	US-6,400,177	06-04-2002	Yoshizaki	
	AK	US-6,529,069	03-04-2003	Krishnapura et al.	
	AL	US-20030112060	06-19-2003	Krishnapura et al.	
	AM	US-20030117212	06-26-2003	Krishnapura et al.	
QV	AN	US-6,683,492	01-27-2004	Krishnapura et al.	
	AO	US-			

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]	Number[4]	Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
QV	AP	PCT	WO 02/35756		05-02-2002	Yoshizawa et al.		☐
QV	AQ	PCT	WO 02/056558		07-18-2002	Palaskas et al.		☐
QV	AR	PCT	WO 02/056470		07-18-2002	Palaskas et al.		☐
	AS							☐

Examiner Signature	Quochien Vuong	Date Considered	12/17/04

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] Kind Codes of U.S. Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

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Substitute for form 1449B/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	10/784,613
				Filing Date	02/23/2004
				First Named Inventor	Tsividis, Yannis
				Art Unit	2685
(use as many sheets as necessary)				Examiner Name	QUOCHIEN VUONG
Sheet	2	of	2	Attorney Docket Number	021673-000210US

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
QV	AT	P.R. GRAY et al., "Future Directions in Silicon ICs for RF Personal Communications", IEEE 1995 Custom Integrated Circuits Conference	
	AU	Y. TSIVIDIS, "Minimising power dissipation in analogue signal processors through syllabic companding", Electronic Letters, Vol. 35, No. 21, October 14, 1999	
	AV	AARNO PARSSINEN et al., "A 2-GHz Wide-Band Direct Conversion Receiver for WCDMA Applications", IEEE Journal of Solid-State Circuits, Vol. 34, No. 12, December 1999	
	AW	FARBOD BEHBAHANI et al., "A Broad-Band Tunable CMOS Channel-Select Filter for a Low-IF Wireless Receiver", IEEE Journal of Solid-State Circuits, Vol. 35, No. 4, April 2000	
	AX	TUOMAS HOLLMAN et al., "A 2.7-V CMOS Dual-Mode Baseband Filter for PDC and WCDMA", IEEE Journal of Solid-State Circuits, Vol. 36, No. 7, July 2001	
	AY	FARBOD BEHBAHANI et al., "Adaptive Analog IF Signal Processor for a Wide-Band CMOS Wireless Receiver", IEEE Journal of Solid-State Circuits, Vol. 36, No. 8, August 2001	
	AZ	ATUSHI YOSHIZAWA et al., "An Anti-Blocker Structure MOSFET-C Filter for a Direct Conversion Receiver", IEEE 2001 Custom Integrated Circuits Conference	
	BA	JUSSI RYYNANEN et al., "RF Gain Control in Direct Conversion Receivers", 2002 IEEE	
	BB	ALEKSANDAR TASIC et al., "Concept of Frequency-Transconductance Tuning of Bipolar Voltage-Controlled Oscillators", 2002 IEEE	
	BC	ALEKSANDER TASIC et al., "Concept of Phase-Noise Tuning of Bipolar Voltage-Controlled Oscillators", 2002 IEEE	
	BD	Y. TSIVIDIS et al., "Internally Varying Analog Circuits Minimize Power Dissipation", IEEE Circuits & Devices Magazine, January 2003	
QV	BE	CHRIS VAN DEN BOS et al., "Architecture of a Reconfigurable Radio Receiver Front-End Using Overall Feedback", Electronic Research Laboratory, Delft University of Technology	

Examiner Signature	Quochien Vuong	Date Considered	12/17/04

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.
[1] Applicant's unique citation designation number (optional). [2] Applicant is to place a check mark here if English language Translation is attached.

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PTO/SB/08B (08-03)

Substitute for form 1449B/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	10/784,613
Filing Date	February 23, 2004
First Named Inventor	Tsividis, Yannis
Art Unit	2685
Examiner Name	QUOCHIEN VUONG
Attorney Docket Number	021673-000210US

U.S. PATENT DOCUMENTS+

Examiner Initials*	Cite No.[1]	Document Number: Number Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
QV	AA	US-2002/0036519	03-28-2002	Krishnapura et al.	
	AB	US-2003/0112059	06-19-2003	Krishnapura et al.	
	AC	US-2004/0042572	03-04-2004	Palaskas et al.	
QV	AD	US-2004/0091035	05-13-2004	Palaskas et al.	
	AE	US-			

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document: Country Code[3] Number[4] Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
	AF					☐
	AG					☐

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
QV	AH	ARYA R. BEHZAD et al., "A 5-GHz Direct-Conversion CMOS Transceiver Utilizing Automatic Frequency Control for the IEEE 802.11a Wireless LAN Standard", IEEE Journal of Solid-State Circuits, Vol. 38, No. 12, December 2003	
QV	AI	VINCENT LEUNG et al., "Digital-IF WCDMA Handset Transmitter IC in 0.25um SiGe BiCMOS", 2004 IEEE International Solid-State Circuits Conference	
QV	AJ	MASOUD ZARGARI et al., "A Single-Chip Dual-Band Tri-Mode CMOS Transceiver for IEEE 802.11a/b/g WLAN", 2004 IEEE International Solid-State Circuits Conference	
	AK		
	AL		

Examiner Signature	Quochien Ba Vuong	Date Considered	12/17/04

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.
[1] Applicant's unique citation designation number (optional). [2] Applicant is to place a check mark here if English language Translation is attached.

60235517 v1

Notice of References Cited	Application/Control No. 10/784,613	Applicant(s)/Patent Under Reexamination TSIVIDIS, YANNIS	
	Examiner Quochien B Vuong	Art Unit 2685	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-5,020,147	05-1991	Okanobu, Taiwa	455/234.1
	B	US-5,867,063	02-1999	Snider et al.	455/234.2
	C	US-5,995,853	11-1999	Park, Hyung-Weon	455/574
	D	US-6,714,557	03-2004	Smith et al.	370/442
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
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	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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BIBDATASHEET

CONFIRMATION NO. 8357

Bib Data Sheet

SERIAL NUMBER	FILING DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
10/784,613	02/23/2004 RULE	455	2685	021673-000210US

APPLICANTS

Yannis Tsividis, New York, NY;

** CONTINUING DATA **********

This appln claims benefit of 60/451,229 03/01/2003 a
and claims benefit of 60/451,230 03/01/2003 a

** FOREIGN APPLICATIONS **********

NONE a

IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** SMALL ENTITY **
** 05/18/2004

Foreign Priority claimed	STATE OR	SHEETS	TOTAL	INDEPENDENT
35 USC 119 (a-d) conditions met	COUNTRY	DRAWING	CLAIMS	CLAIMS
Verified and Acknowledged	NY	15	30	6

☐ yes ☑ no

☐ yes ☑ no ☐ Met after Allowance

Examiner's Signature _____ Initials _____

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TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO , CA
94111-3834

TITLE

Power dissipation reduction in wireless transceivers

FILING FEE	FEES: Authority has been given in Paper	
RECEIVED	No. _____ to charge/credit DEPOSIT ACCOUNT	☐ All Fees
604	No. _____ for following:	☐ 1.16 Fees (Filing)
		☐ 1.17 Fees (Processing Ext. of time)
		☐ 1.18 Fees (Issue)
		☐ Other _____
		☐ Credit

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Index of Claims

Application No.	Applicant(s)	
10/784,613	TSIVIDIS, YANNIS	
Examiner	**Art Unit**	
Quochien B Vuong	2685	

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

Claim		Date	Claim		Date	Claim		Date
Final	Original	12/23/04	Final	Original		Final	Original	
	1	√		51			101	
	2	|		52			102	
	3	|		53			103	
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	6	|		56			106	
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	49			99			149	
	50			100			150	

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Search Notes

Application No.	Applicant(s)	
10/784,613	TSIVIDIS, YANNIS	
Examiner	**Art Unit**	
Quochien B Vuong	2685	

SEARCHED			
Class	Subclass	Date	Examiner
455	63.1, 67.13, 226.1, 226.2	12/17/04	QV
	232.1, 234.1		
	250.1, 295		
	296, 311		
	333, 343.1		
	127.1, 127.2		
	127.5, 574		
370	442		

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR

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Theta EX2019

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TOWNSEND and TOWNSEND and CREW LLP

By: _____

J. Matthew Zigmant

PATENT
Attorney Docket No.: 021673-000210US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Yannis Tsividis

Application No.: 10/784,613

Filed: February 23, 2004

For: POWER DISSIPATION REDUCTION IN WIRELESS TRANSCEIVERS

Customer No.: 20350

Confirmation No. 8357

Examiner: Vuong, Quochien B.

Technology Center/Art Unit: 2685

AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the office action mailed January 4, 2005, please enter the following amendments and remarks:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 8 of this paper.

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Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claim 1. (Currently amended) A method of receiving a signal using an integrated circuit, the integrated circuit comprising a signal path including a low-noise amplifier configured to receive the signal, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer, the method comprising:

determining a first signal strength at a first node in the signal path in the integrated circuit; and

reducing a switching current in the signal path by dynamically changing an impedance of a component in the signal path based on the first signal strength.

Claim 2. (Original) The method of claim 1 wherein the signal comprises a preamble portion and a data portion, the impedance of a component is changed while receiving the preamble portion, and the method further comprises receiving the data portion of the signal.

Claim 3. (Original) The method of claim 2 further comprising:

determining a second signal strength at a second node in the signal path, wherein the second node in the signal path is after the first node in the signal path.

Claim 4. (Original) The method of claim 3 wherein the impedance of the component in the signal path is also changed based on the second signal strength.

Claim 5. (Original) The method of claim 2 wherein the component in the signal path comprises a MOS transistor.

Claim 6. (Original) The method of claim 2 wherein the component in the signal path comprises a resistor.

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Claim 7. (Original) The method of claim 2 wherein the component in the signal path comprises a capacitor.

Claim 8. (Original) The method of claim 4 wherein the component in the signal path is included in the mixer.

Claim 9. (Original) The method of claim 4 wherein the component in the signal path is included in the low-pass filter.

Claim 10. (Currently amended) A method of receiving a signal comprising a preamble portion and a data portion using an integrated circuit, the integrated circuit comprising a signal path including a low-noise amplifier configured to receive the signal, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer, the method comprising:

determining a first signal strength at a first node in the signal path in the integrated circuit; and

while receiving the preamble portion of the signal, dynamically changing a bias current in the signal path based on the first signal strength, and while receiving the data portion of the signal, maintaining the bias current in the signal path.

Claim 11. (Original) The method of claim 10 wherein the method further comprises receiving the data portion of the signal.

Claim 12. (Original) The method of claim 11 further comprising:

determining a second signal strength at a second node in the signal path, wherein the second node in the signal path is after the first node in the signal path.

Claim 13. (Original) The method of claim 12 wherein the bias current in the signal path is also changed based on the second signal strength.

Claim 14. (Original) The method of claim 11 wherein the bias current is a bias current for the low-noise amplifier.

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Claim 15. (Original) The method of claim 11 wherein the bias current is a bias current for the mixer.

Claim 16. (Original) The method of claim 11 wherein the bias current is a bias current for the low-pass filter.

Claim 17. (Original) A method of receiving a signal using an integrated circuit, the integrated circuit comprising a signal path including a first circuit and a second circuit having an input coupled to an output of the first circuit, the method comprising:

determining a first signal strength at a first node in the signal path in the integrated circuit, wherein the first node is before the first circuit in the signal path;

dynamically changing a gain of the first circuit based on the first signal strength; and

dynamically changing an impedance of a component in the second circuit based on the first signal strength.

Claim 18. (Original) The method of claim 17 wherein the signal comprises a preamble portion and a data portion, the gain and impedance are changed while receiving the preamble portion, and the method further comprises receiving the data portion of the signal.

Claim 19. (Original) The method of claim 18 further comprising:

determining a second signal strength at a second node in the signal path, wherein the second node in the signal path is after the second circuit in the signal path.

Claim 20. (Original) The method of claim 19 wherein the gain of the first circuit and impedance of the component in the second circuit is also changed based on the second signal strength.

Claim 21. (Original) The method of claim 18 wherein the first circuit is a low-noise amplifier.

Claim 22. (Original) The method of claim 18 wherein the first circuit is a mixer.

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Claim 23. (Currently amended) A wireless transceiver integrated circuit comprising:

a receiver comprising a signal path, the signal path comprising:

a low-noise amplifier;

a mixer having an input coupled to an output of the low-noise amplifier; and

a low-pass filter having an input coupled to an output of the mixer; and

a first signal strength indicator circuit coupled to the signal path, and configured to determine a first signal strength;

wherein an impedance in the signal path is configured to be dynamically adjusted to reduce a switching current in response to the first signal strength.

Claim 24. (Original) The wireless transceiver of claim 23 further comprising:

a second signal strength indicator circuit coupled to the output of the mixer, and configured to determine a second signal strength,

wherein the first signal strength indicator is coupled to the output of the low-noise amplifier, and

wherein the impedance in the signal path is configured to be adjusted in response to the first and second signal strengths.

Claim 25. (Original) The wireless transceiver of claim 23 further comprising:

a second signal strength indicator circuit coupled to the output of the low-pass filter, and configured to determine a second signal strength,

wherein the first signal strength indicator is coupled to the output of the mixer, and

wherein the impedance in the signal path is configured to be adjusted in response to the first and second signal strengths.

Claim 26. (Currently amended) A wireless transceiver integrated circuit comprising:

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a receiver comprising a signal path, the signal path comprising:

a low-noise amplifier;

a mixer having an input coupled to an output of the low-noise amplifier; and

a low-pass filter having an input coupled to an output of the mixer; and

a first signal strength indicator circuit coupled to the signal path, and configured to determine a first signal strength, the first signal strength the strength of a signal comprising a preamble portion and a data portion;

wherein a bias current in the signal path is configured to be dynamically adjusted during the preamble portion of the signal in response to the first signal strength, and further configured to be maintained during the data portion of the signal.

Claim 27. (Original) The wireless transceiver of claim 26 further comprising:

a second signal strength indicator circuit coupled to the output of the mixer, and configured to determine a second signal strength,

wherein the first signal strength indicator is coupled to the output of the low-noise amplifier, and

wherein the bias current in the signal path is configured to be adjusted in response to the first and second signal strengths.

Claim 28. (Original) The wireless transceiver of claim 26 further comprising:

a second signal strength indicator circuit coupled to the output of the low-pass filter, and configured to determine a second signal strength,

wherein the first signal strength indicator is coupled to the output of the mixer, and

wherein the bias current in the signal path is configured to be adjusted in response to the first and second signal strengths.

Claim 29. (Original) A wireless transceiver integrated circuit comprising:

a receiver comprising a signal path, the signal path comprising:

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a first circuit; and

a second circuit having an input coupled to an output of the first circuit; and

a first signal strength indicator circuit coupled to the signal path, and configured to determine a first signal strength;

wherein a gain of the first circuit is configured to be dynamically adjusted in response to the first signal strength, and

wherein an impedance in the second circuit is configured to be dynamically adjusted in response to the first signal strength.

Claim 30. (Original) The wireless transceiver of claim 29 further comprising:

a transmitter comprising:

a power amplifier; and

an output-level-sensing circuit coupled to an output of the power amplifier,

wherein the output-level-sensing circuit is configured to dynamically adjust a gain of the power amplifier.

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REMARKS/ARGUMENTS

After entry of this amendment, claims 1-30 will remain pending in this application. Claims 1, 10, 23, and 26 have been amended. Support for the amended claims can be found in the specification. No new matter has been added.

Claims 1, 17, 23-25 and 29 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Clark, United States patent number 5,001,776, in view of Okanobu, United States patent number 5,020,147. Claims 2-16, 18-22, and 26-28 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Clark in view of Okanobu and further in view of Smith, United States patent number 6,714,557. Reconsideration of these rejections and allowance of all the pending claims is respectfully requested.

Claim 1

Claim 1 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Clark in view of Okanobu. But these references do not show or suggest each and every limitation of this claim. For example, Claim 1 recites "reducing a switching current in the signal path by dynamically changing an impedance of a component in the signal path based on the first signal strength." The cited references do not provide this feature.

The pending office action cites Clark as showing "dynamically changing an impedance of a component in the signal path based on the first signal strength." (See pending office action, page 2, section 3.) But Clark shows changing a bias current based on various signal strengths.

A bias current is not the same as a switching current. One skilled the art understands that a bias current is a DC or quiescent current, while a switching current is a dynamic or transient current that occurs during voltage transitions. (See for example, the pending application, Figure 6 and related discussion.) Accordingly, the cited references do not show or suggest reducing a switching current in the signal path by dynamically changing an impedance of a component in the signal path as required by the claim.

For at least this reason, claim 1 should be allowed.

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Claim 10

Claim 10 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Clark in view of Okanobu and further in view of Smith. But these references do not teach each and every limitation of this claim. For example, claim 10 recites "while receiving the preamble portion of the signal, dynamically changing a bias current in the signal path based on the first signal strength, and while receiving the data portion of the signal, maintaining the bias current in the signal path." The cited references do not provide this feature.

There is no motivation in Clark to limit changes to a bias current while receiving a preamble, as is required by the claim. Rather, Clark does not appear to discuss changing a bias current during specific signal events, such as a preamble, an not changing the bias current during others, such as during data transmission. The claim in particular only mention making this current modification during reception of a signal. (See for example, claim 1 in Clark.)

For at least this reason, claim 10 should be allowed.

Claim 17

Claim 17 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Clark in view of Okanobu. But these references do not show or suggest each and every limitation of this claim. For example, Claim 17 recites "dynamically changing a gain of the first circuit based on the first signal strength; and dynamically changing an impedance of a component in the second circuit based on the first signal strength."

The pending office action cites Clark as showing changing an impedance, though appears to be silent regarding a gain change. (See pending office action, page 4, first paragraph.) The cited references do not show or suggest the combination of changing a gain and changing an impedance as required by the claim.

For at least this reason, claim 17 should be allowed.

Other claims

Claim 23 should be allowed for similar reasons as claim 1. Claim 26 should be allowed for similar reasons as claim 10. Claim 29 should be allowed for similar reasons as claim

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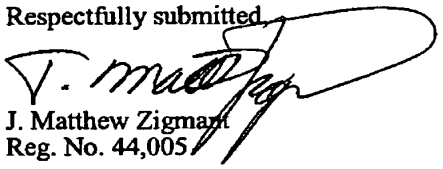
17. The other claims depend on these claims and should be allowed for similar reasons, and for the additional limitations they recite.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this application are in condition for allowance. The issuance of a formal notice of allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,



J. Matthew Zigmant
Reg. No. 44,005

TOWNSEND and TOWNSEND and CREW LLP
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San Francisco, California 94111-3834
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Attachments
JMZ:jmz
60530755 v1

PAGE 14/14 * RCVD AT 7/6/2005 12:46:04 AM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/0 * DNIS:8729306 * CSID:415 576 0300 * DURATION (mm-ss):05-14

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on July 5, 2005
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Signature

J. Matthew Zigmant
Typed or printed name of person signing Certificate

In re: application of: Yannis Tsivdis
Application Number: 10/784,613
Filed: 02/23/2004
Title: Power Dissipation Reduction in Wireless Transceivers
Atty Docket Number: **021673-000210US** JMZ

Being faxed to Examiner Vuong, Quochien B., at facsimile number **1-703-872-9306** are the following documents:

1. This PTO/SB/97 Certificate of Transmission (1 page);
2. PTO/SB/21 - Transmittal Form (1 page);
3. PTO/SB/22 Petition for Extension of Time (1 page submitted in duplicate); and
4. Amendment (10 pages).

Number of pages being transmitted: 14

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PTO/SB/21 (09-04)

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission	14

Application Number	10/784,613
Filing Date	February 23, 2004
First Named Inventor	Tsividis, Yannis
Art Unit	2685
Examiner Name	Vuong, Quochien B.
Attorney Docket Number	021673-000210US

ENCLOSURES *(Check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☒ **Amendment/Reply (10 pages)**
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☒ **Extension of Time Request (1 page in duplicate)**
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Reply to Missing Parts/ Incomplete Application
  - ☐ Reply to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
- ☐ Request for Refund
- ☐ CD, Number of CD(s) _____
  - ☐ Landscape Table on CD
- ☐ After Allowance Communication to TC
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☐ Appeal Communication to TC (Appeal Notice, Brief, Reply Brief)
- ☐ Proprietary Information
- ☐ Status Letter
- ☒ **Other Enclosure(s) (please identify below):**

Fax coversheet (1 page); and
This transmittal (1 page).

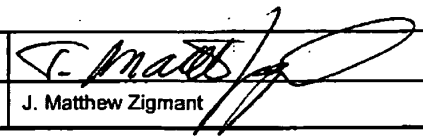
Remarks The Commissioner is authorized to charge any additional fees to Deposit Account 20-1430.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	Townsend and Townsend and Crew LLP		
Signature			
Printed name	J. Matthew Zigmant		
Date	July 5, 2005	Reg. No.	44,005

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PTO/SB/22 (12-04)

PETITION FOR EXTENSION OF TIME UNDER 37 CFR 1.136(a) FY 2005 *(Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).)*	Docket Number (Optional) 021673-000210US
Application Number 10/784,613	Filed February 23, 2004
For POWER DISSIPATION REDUCTION IN WIRELESS TRANSCEIVERS	
Art Unit 2685	Examiner Vuong, Quochien B.

This is a request under the provisions of 37 CFR 1.136(a) to extend the period for filing a reply in the above identified application.

The requested extension and fee are as follows (check time period desired and enter the appropriate fee below):

	Fee	Small Entity Fee	
☐ One month (37 CFR 1.17(a)(1))	$120	$60	$
☐ Two months (37 CFR 1.17(a)(2))	$450	$225	$
☒ Three months (37 CFR 1.17(a)(3))	$1020	$510	$ 510
☐ Four months (37 CFR 1.17(a)(4))	$1590	$795	$
☐ Five months (37 CFR 1.17(a)(5))	$2160	$1080	$

☒ Applicant claims small entity status. See 37 CFR 1.27.

☐ A check in the amount of the fee is enclosed.

07/07/2005 MBINAS 00000014 201430 10784613
01 FC:2253 510.00 DA

☐ Payment by credit card. Form PTO-2038 is attached.

☐ The Director has already been authorized to charge fees in this application to a Deposit Account.

☒ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number 20-1430. I have enclosed a duplicate copy of this sheet.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

I am the

☐ applicant/inventor.

☐ assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed (Form PTO/SB/96).

☒ attorney or agent of record. Registration Number 44,005

☐ attorney or agent under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 _____

Signature	July 5, 2005 Date
J. Matthew Zigmant, Reg. No. 44,005 Typed or printed name	408-273-4782 Telephone Number

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.

☐ Total of 2 forms are submitted.

60530918 v1

PATENT APPLICATION FEE DETERMINATION RECORD
Effective October 1, 2003

Application or Docket Number: 10784613

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	30	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	30 minus 20=	* 10
INDEPENDENT CLAIMS	6 minus 3 =	* 3
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐			OR	OTHER THAN SMALL ENTITY	
RATE	FEE			RATE	FEE
BASIC FEE	385.00		OR	BASIC FEE	770.00
X$ 9=	90		OR	X$18=	
X43=	129		OR	X86=	
+145=			OR	+290=	
TOTAL	604		OR	TOTAL	

CLAIMS AS AMENDED - PART II

AMENDMENT A	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	* 30	Minus	** 30	=
Independent	* 0	Minus	*** 6	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY			OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE			RATE	ADDITIONAL FEE
X$ 9=			OR	X$18=	
X43=			OR	X86=	
+145=			OR	+290=	
TOTAL ADDIT. FEE			OR	TOTAL ADDIT. FEE	

AMENDMENT B	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

			OR		
RATE	ADDITIONAL FEE			RATE	ADDITIONAL FEE
X$ 9=			OR	X$18=	
X43=			OR	X86=	
+145=			OR	+290=	
TOTAL ADDIT. FEE			OR	TOTAL ADDIT. FEE	

AMENDMENT C	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

			OR		
RATE	ADDITIONAL FEE			RATE	ADDITIONAL FEE
X$ 9=			OR	X$18=	
X43=			OR	X86=	
+145=			OR	+290=	
TOTAL ADDIT. FEE			OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

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Mark T. Davis
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In re: application of: Yannis Tsivdis
Application Number: 10/784,613
Filed: 02/23/2004
Title: Power Dissipation Reduction in Wireless Transceivers
Atty Docket Number: **021673-000210US** JMZ

Being faxed to Examiner Vuong, Quochien B., at facsimile number **1-703-872-9306** are the following documents:

1. This PTO/SB/83; Request for Withdrawl as Attorney or Agent

Number of pages being transmitted: 2

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PTO/SB/83 (01-03)
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REQUEST FOR WITHDRAWAL AS ATTORNEY OR AGENT

Application Number	10/784,613
Filing Date	February 23, 2004
First Named Inventor	Yannis Tsividis
Art Unit	2681
Examiner Name	Quochien B. Vuong
Attorney Docket Number	021673-000210US

To: Commissioner for Patents
Washington, DC 20231

I hereby apply to withdraw as attorney or agent for the above identified patent application.

The reasons for this request are: Per request of the client

1. ☐ The correspondence address is NOT affected by this withdrawal.
2. ☐ Change the correspondence address and direct all future correspondence to:

CORRESPONDENCE ADDRESS

☐ Customer Number

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☒ Firm or Individual Name	Blakely, Sokoloff, Taylor & Zafman LLP				
Address	3200 Park Center Drive, Suite 700				
Address	Suite 700				
City	Costa Mesa	State	CA	ZIP	92626
Country	U.S.A.				
Telephone	(714) 557-3800	Fax	(714) 557-3347		

☒ This request is made on behalf of myself and
- ☐ all the attorneys/agents of record.
- ☐ the attorneys/agents (with registration numbers) listed on the attached paper(s), or
- ☒ the attorneys/agents associated with Customer Number 20-1430

This request is enclosed in **triplicate** (including any attachments).

Name	J. Matthew Zigmant
Signature	
Date	August (23), 2005

NOTE: Withdrawal is effective when approved rather than when received. Unless there are at least 30 days between approval of withdrawal and the expiration date of a time period for response or possible extension period, the request to withdraw is normally disapproved.

This collection of information is required by 37 CFR 1.36. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, Washington, DC 20231.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

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Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	121124	gain near2 (control$3 adjust$3 chang$3 varie$1 varying)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/19 07:53
L5	44993	impedance near2 (control$3 adjust$3 chang$3 varie$1 varying)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/19 07:24
L6	1122	2 same 5	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/19 07:24
L7	171	6 same (receiver receiving received)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/19 07:54
L8	89977	"455"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/19 07:25
L9	28	7 and 8	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/19 07:52
L11	23543	switching adj2 current	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/19 07:38
L15	2977	bias same gain same impedance	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/19 07:53
L16	48054	bias near2 (control$3 adjust$3 chang$3 varie$1 varying)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/19 07:53

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L17	41	6 same 16	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/19 07:54
L18	31	17 and (receiver receiving received)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/19 08:05
L22	67	5 same 11	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/19 08:26
L33	1799	330/127,129,134,136,144.ccls.	US-PGPUB; USPAT	OR	ON	2005/09/19 09:54
L34	23	33 and 6	US-PGPUB; USPAT	OR	ON	2005/09/19 09:54
L35	10	((impedance near2 (control$3 adjust$3 chang$3 varie$1 varying)) with (switching adj2 current)).clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/19 09:55
L36	171	((impedance near2 (control$3 adjust$3 chang$3 varie$1 varying)) with (gain near2 (control$3 adjust$3 chang$3 varie$1 varying))).clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/19 09:58

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FEE TRANSMITTAL for FY 2005

Patent fees are subject to annual revision.

☒ Applicant claims small entity status. See 37 CFR 1.27.

TOTAL AMOUNT OF PAYMENT	($)	750.00

Complete if Known	
Application Number	10/784,613
Filing Date	February 23, 2004
First Named Inventor	Yannis Tsividis
Examiner Name	Vuong, Quochien B.
Art Unit	2685
Attorney Docket No.	7084P007

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METHOD OF PAYMENT *(check all that apply)*

☐ Check ☐ Credit card ☐ Money Order ☐ None ☐ Other (please identify): _____

☒ Deposit Account Deposit Account Number: 02-2666 Deposit Account Name: Blakely, Sokoloff, Taylor & Zafman LLP

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☒ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, except for the filing fee

☒ Charge any additional fee(s) or underpayment of fee(s) under 37 CFR §§ 1.16, 1.17, 1.18 and 1.20. ☐ Credit any overpayments

FEE CALCULATION

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet.	
2053	130	2053	130	Non-English specification	
1251	120	2251	60	Extension for reply within first month	
1252	450	2252	225	Extension for reply within second month	
1253	1,020	2253	510	Extension for reply within third month	
1254	1,590	2254	795	Extension for reply within fourth month	
1255	2,160	2255	1,080	Extension for reply within fifth month	
1401	500	2401	250	Notice of Appeal	
1402	500	2402	250	Filing a brief in support of an appeal	
1403	1,000	2403	500	Request for oral hearing	
1451	1,510	2451	1,510	Petition to institute a public use proceeding	
1460	130	2460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
1809	790	1809	395	Filing a submission after final rejection (37 CFR § 1.129(a))	
1810	790	2810	395	For each additional invention to be examined (37 CFR § 1.129(b))	
Other fee (specify) Petition for Revival (Failure to Notify re Foreign Filing)					750.00
SUBTOTAL (2)					($) 750.00

SUBMITTED BY					Complete (if applicable)
Name (Print/Type)	Roger W. Blakely, Jr.	Registration No. (Attorney/Agent)	25,831	Telephone	(714) 557-3800
Signature	Roger W. Blakely			Date	09/21/05

Based on PTO/SB/17 (12-04) as modified by Blakely, Sokoloff, Taylor & Zafman (wir) 12/15/2004.
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FEE TRANSMITTAL for FY 2005

Patent fees are subject to annual revision.

☒ Applicant claims small entity status. See 37 CFR 1.27.

TOTAL AMOUNT OF PAYMENT	($)	750.00

Complete If Known	
Application Number	10/784,613
Filing Date	February 23, 2004
First Named Inventor	Yannis Tsividis
Examiner Name	Vuong, Quochien B
Art Unit	2685
Attorney Docket No.	7084P007

METHOD OF PAYMENT *(check all that apply)*

☐ Check ☐ Credit card ☐ Money Order ☐ None ☐ Other (please identify): _____

☒ Deposit Account Deposit Account Number: 02-2666 Deposit Account Name: Blakely, Sokoloff, Taylor & Zafman LLP

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☒ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, except for the filing fee

☒ Charge any additional fee(s) or underpayment of fee(s) under 37 CFR §§ 1.16, 1.17, 1.18 and 1.20. ☐ Credit any overpayments

FEE CALCULATION

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
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1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet.	
2053	130	2053	130	Non-English specification	
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1255	2,160	2255	1,080	Extension for reply within fifth month	
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1403	1,000	2403	500	Request for oral hearing	
1451	1,510	2451	1,510	Petition to institute a public use proceeding	
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1806	180	1806	180	Submission of Information Disclosure Stmt	
1809	790	1809	395	Filing a submission after final rejection (37 CFR § 1.129(a))	
1810	790	2810	395	For each additional invention to be examined (37 CFR § 1.129(b))	
				Other fee (specify) Petition for Revival (Failure to Notify re Foreign Filing)	750.00
				SUBTOTAL (2)	($) 750.00

SUBMITTED BY Complete (if applicable)

Name (Print/Type)	Roger W. Blakely, Jr.	Registration No. (Attorney/Agent)	25,831	Telephone	(714) 557-3800
Signature	Roger W Blakely			Date	09/21/05

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PETITION FOR REVIVAL OF AN APPLICATION FOR PATENT ABANDONED FOR FAILURE TO NOTIFY THE OFFICE OF A FOREIGN OR INTERNATIONAL FILING (37 CFR 1.137(f))	Docket Number (Optional) 7084P004

First named inventor: Yannis Tsividis

Application No.: 10/784,613 Art Unit: 2685

Filed: 02/23/2004 Examiner: Vuong, Quochien B

Title: POWER DISSIPATION REDUCTION IN WIRELESS TRANSCEIVERS

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Attention: Office of Petitions
Mail Stop Petition
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
FAX (571) 273-8300

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NOTE: If information or assistance is needed in completing this form, please contact Petitions Information at (571) 272-3282.

The above-identified application became abandoned pursuant to 35 U.S.C. 122(b)(2)(B)(iii) for failure to timely notify the Office of the filing of an application in a foreign country or under a multinational international treaty that requires publication of applications eighteen months after filing. The date of abandonment is the day after the expiration date of the forty-five (45) day period set in 35 U.S.C. 122(b)(2)(B)(iii).

PURSUANT TO 37 CFR 1.137(f), APPLICANT HEREYBY PETITIONS FOR REVIVAL OF THIS APPLICATION UNDER 37 CFR 1.137(b)

1. Petition fee

☑ Small entity-fee $ 750.00 (37 CFR 1.17(m)). Applicant claims small entity status. See 37 CFR 1.27.

☐ Other than small entity – fee $ _____ (37 CFR 1.17(m))

2. Notice of Foreign or International Filing (35 U.S.C. 122(b)(2)(B)(iii) and 37 CFR 1.213(c))

Subsequent to the filing of the above-identified application, an application was filed in another country, or under a multinational international treaty (e.g., filed under the Patent Cooperation Treaty), that requires publication of applications eighteen months after the filing. The filing date of the subsequently filed foreign or international application is February 27, 2004.

This collection of information is required by 37 CFR 1.137. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Mail Stop Petition, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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PTO/SB/84a (07-05)
Approved for use through 07/31/2006. OMB 0651-0031
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STATEMENT: The entire delay in filing the required notice of a foreign or international filing from the due date for the required notice until the filing of a grantable petition under 37 CFR 1.137(b) was unintentional. [NOTE: The United States Patent and Trademark Office may require additional information there is a question as to whether either the abandonment or the delay in filing a petition under 37 CFR 1.137(b) was unintentional (MPEP 711.03(c), subsections (III)(C) and (D)).]

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

Roger W Blakely
Signature

September 21, 2005
Date

Roger W. Blakely, Jr.
Typed or printed name

25,831
Registration Number, if applicable

12400 Wilshire Boulevard, Seventh Floor
Address

(714) 557-3800
Telephone Number

Los Angeles, CA 90025
Address

Enclosures: ☑ Fee Payment

☐ Additional sheets containing statements establishing unintentional delay

☑ Other: Revocation of Power of Attorney with New Power of Attorney and Change of Correspondence Address; Statement Under 37 CFR 3.73(b)

CERTIFICATE OF MAILING OR TRANSMISSION [37 CFR 1.8(a)]

I hereby certify that this correspondence is being:

☐ Deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop Petition, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450.

☑ Transmitted by facsimile on the date shown below to the United States Patent and Trademark Office at (571) 273-8300.

September 21, 2005
Date

Jessica A Clark
Signature

Jessica A. Clark
Typed or printed name of person signing certificate

PAGE 6/8 * RCVD AT 9/21/2005 5:08:53 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/33 * DNIS:2738300 * CSID:7145573347 * DURATION (mm-ss):03-50

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REVOCATION OF POWER OF ATTORNEY WITH NEW POWER OF ATTORNEY AND CHANGE OF CORRESPONDENCE ADDRESS		
	Application No.	10/784,613
	Filing Date	February 23, 2004
	First Named Inventor	Yannis Tsividis
	Group Art Unit	2685
	Examiner Name	Vuong, Quochien B.
	Attorney Docket Number	7084P007

I hereby revoke all previous powers of attorney given in the above-identified application:

☐ A Power of Attorney is submitted herewith.

OR

☒ I hereby appoint the practitioners at Customer Number: 08791

☒ Please change the correspondence address for the above-identified application to:

☒ The address associated with Customer Number: 08791

OR

☐ Firm or Individual Name	BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP				
Address	12400 Wilshire Boulevard, 7th Floor				
Address					
City	Los Angeles	State	California	Zip Code	90025
Country	U.S.A.	Telephone	(714) 557-3800	Fax	(714) 557-3347

I am the:

☐ Applicant.

☒ Assignee of record of the entire interest. See 37 CFR 3.71.
Statement under of 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)

SIGNATURE of Applicant or Assignee of Record

Name	Bruce R. Bowbon Chairman & CEO, Theta Microelectronics, Inc.
Signature	Bruce R. Bowbon
Date	9-20-2005

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of _____ forms are submitted.

Based on PTO/SB/32 (09-04) as modified by BSTZ (01/19/05 - VTCR).
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Docket No. 7084P007

STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: Theta Microelectronics, Inc.

Application No./Patent No.: 10/784,613 Filing/issue Date: 2/23/2004

Entitled: POWER DISSIPATION REDUCTION IN WIRELESS TRANSCEIVERS

Theta Microelectronics, Inc., a Corporation
(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

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states that it is:

1. ☒ the assignee of the entire right, title and interest; or
2. ☐ an assignee of less than the entire right, title and interest.
The extent (by percentage) of its ownership interest is _____%

in the patent application/patent identified above by virtue of either:

A. ☒ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the Patent and Trademark Office at Reel 15218, Frame 139, or for which a copy thereof is attached.

OR

B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as shown below:

1. From: _____ To: _____
The document was recorded in the Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.
2. From: _____ To: _____
The document was recorded in the Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.
3. From: _____ To: _____
The document was recorded in the Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.
4. From: _____ To: _____
The document was recorded in the Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet.

☐ Copies of assignments or other documents in the chain of title are attached.
[NOTE: A separate copy (*i.e.*, the original assignment document or a true copy of the original document) must be submitted to Assignment Division in accordance with 37 CFR Part 3, if the assignment is to be recorded in the records of the PTO. See MPEP 302-302.8]

The undersigned (whose title is supplied below) is empowered to sign this statement on behalf of assignee.

September 21, 2005
Date

Roger W. Blakely
Signature

Roger W. Blakely, Jr., Reg. No. 25,831
Typed or printed name

Attorney
Title

Based on PTO/SB/96 (08-03) as modified by Blakely, Sokoloff, Taylor & Zafman (wir) 05/05/2004.
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TELEPHONE: (714) 557-3800
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LOS ANGELES, CA 90025
FACSIMILE: (714) 557-3347

FACSIMILE COVER SHEET

Deliver to: Vuong, Quochien B, USPTO
Art Group: 2685
Facsimile No.: (571) 273-8300
Date: September 21, 2005
From: Roger W. Blakely, Jr., Reg. No. 25,831
Our Docket No.: 7084P007
Number of pages 8 including this sheet.
Application No.: 10/784,613
Filing Date: 2/23/2004
Docket Due Date(s): ____

Enclosed are the following documents:

☐ Amendment: _____ (___pgs)	☐ Issue Fee Transmittal
☐ Appeal Brief (___pgs)	☐ Notice of Appeal
☐ Application: _____	☒ Petition for: Revival
(___pgs) w/cover & abstract)	☐ Request for Continued Examination (RCE)
☐ Assignment & Cover Sheet (___pgs)	☐ Reply Brief (___pgs)
☒ Certificate of Facsimile	☐ Request & Certification Under 35 USC 122(b)(2)(B)(i)
☐ Continued Prosecution Application (CPA)	☐ Request to Rescind Previous Nonpublication Request
☐ Declaration & POA (___pgs)	☐ Response to Notice of Missing Parts & Formalities Letter
☐ Drawings: ___sheets, ___ figures	☐ Response to Written Opinion (___pgs)
☐ Extension of Time: _____	☐ Terminal Disclaimer
☒ Fee Transmittal (in duplicate)	☐ Transmittal of Publication Fee Due
☐ IDS & PTO/SB/08 (pgs)	☒ Transmittal Letter

☒ Other Revocation of Power of Attorney with New Power of Attorney and Change of Correspondence Address (1 pg); Statement Under 3.73(b) (1 pg)

CERTIFICATE OF MAILING/TRANSMISSION (37 CFR 1.8A)

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Jessica A. Clark 9/21/2005

Jessica A. Clark *Date*

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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application No.	10/784,613
Filing Date	February 23, 2004
First Named Inventor	Yannis Tsividis
Art Unit	2685
Examiner Name	Vuong, Quochien B
Total Number of Pages in This Submission	8
Attorney Docket Number	7084P007

ENCLOSURES *(check all that apply)*

- [x] Fee Transmittal Form
  - [x] Fee Attached
- [ ] Amendment / Response
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
  - [ ] PTO/SB/08
- [ ] Certified Copy of Priority Document(s)
- [ ] Response to Missing Parts/ Incomplete Application
  - [ ] Basic Filing Fee
  - [ ] Declaration/POA
  - [ ] Response to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [x] Petition
- [ ] Petition to Convert a Provisional Application
- [x] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s)
- [ ] After Allowance Communication to Group
- [ ] Appeal Communication to Board of Appeals and Interferences
- [ ] Appeal Communication to Group (Appeal Notice, Brief, Reply Brief)
- [ ] Proprietary Information
- [ ] Status Letter
- [x] Other Enclosure(s) *(please identify below):*

Statement Under 37 3.73(b); Facsimile Cover Sheet

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Roger W. Blakely, Jr., Reg. No. 25,831 BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Signature	Roger W. Blakely
Date	September 21, 2005

CERTIFICATE OF MAILING/TRANSMISSION

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Typed or printed name	Jessica A. Clark		
Signature	Jessica A. Clark	Date	September 21, 2005

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SAN FRANCISCO, CA 94111-3834

EXAMINER
VUONG, QUOCHIEN B

ART UNIT	PAPER NUMBER
2685	

DATE MAILED: 09/26/2005

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/784,613	02/23/2004	Yannis Tsividis	021673-000210US	8357

TITLE OF INVENTION: POWER DISSIPATION REDUCTION IN WIRELESS TRANSCEIVERS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	$700	$0	$700	12/27/2005

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE REFLECTS A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE APPLIED IN THIS APPLICATION. THE PTOL-85B (OR AN EQUIVALENT) MUST BE RETURNED WITHIN THIS PERIOD EVEN IF NO FEE IS DUE OR THE APPLICATION WILL BE REGARDED AS ABANDONED.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL should be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). Even if the fee(s) have already been paid, Part B - Fee(s) Transmittal should be completed and returned. If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 07/05) Approved for use through 04/30/2007.

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IPR2023-00819
Theta EX2019

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571) 273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

20350 7590 09/26/2005

TOWNSEND AND TOWNSEND AND CREW, LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO, CA 94111-3834

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)

(Signature)

(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/784,613	02/23/2004	Yannis Tsividis	021673-000210US	8357

TITLE OF INVENTION: POWER DISSIPATION REDUCTION IN WIRELESS TRANSCEIVERS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	$700	$0	$700	12/27/2005

EXAMINER	ART UNIT	CLASS-SUBCLASS
VUONG, QUOCHIEN B	2685	455-574000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are enclosed:

☐ Issue Fee

☐ Publication Fee (No small entity discount permitted)

☐ Advance Order - # of Copies _____

4b. Payment of Fee(s):

☐ A check in the amount of the fee(s) is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☐ The Director is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

The Director of the USPTO is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above.
NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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Apple EX1002 Page 328
IPR2023-00819
Theta EX2019

UNITED STATES PATENT AND TRADEMARK OFFICE

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United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/784,613	02/23/2004	Yannis Tsividis	021673-000210US	8357

20350 7590 09/26/2005

TOWNSEND AND TOWNSEND AND CREW, LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO, CA 94111-3834

EXAMINER	
VUONG, QUOCHIEN B	
ART UNIT	**PAPER NUMBER**
2685	

DATE MAILED: 09/26/2005

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571) 272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (703) 305-8283.

PTOL-85 (Rev. 07/05) Approved for use through 04/30/2007.

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IPR2023-00819
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Notice of Allowability	Application No.	Applicant(s)	
	10/784,613	TSIVIDIS, YANNIS	
	Examiner	Art Unit	
	Quochien B. Vuong	2685	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *07/06/2005*.

2. ☒ The allowed claim(s) is/are *1-30*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 07/02/04
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

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Apple EX1002 Page 330
IPR2023-00819
Theta EX2019

Reasons for Allowance

1. Claims 1-30 are allowed over the cited prior art.

2. The following is an examiner's statement of reasons for allowance:

Regarding independent claims 1 and 23, the claims have been amended to include "...reducing a switching current by dynamically changing an impedance...", wherein the switching current is defined in the Applicant's remark filed 07/06/2005, page 8.

Regarding independent claims 10 and 23, the cited prior art fail to teach or fairly suggest the claimed invention with the reasons set forth in the Applicant's remark filed 07/06/2005, page 9.

Regarding independent claims 17 and 29, the cited prior art fail to teach or fairly suggest the claimed invention with the reasons set forth in the Applicant's remark filed 07/06/2005, page 9.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Nguyen (US 6,298,221) discloses adaptive receiver linearity techniques for a radio transceiver.

Tripathi et al. (Us 6,621,339) disclose method and apparatus facilitating negative feedback providing loop stability, and improving amplifier efficiency.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quochien B. Vuong whose telephone number is (571) 272-7902. The examiner can normally be reached on M-F 9:30-18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Urban can be reached on (571) 272-7899. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Quochien B. Vuong
Sep. 19, 2005.

QUOCHIEN B. VUONG
PRIMARY EXAMINER

OIPE JC34
JUL 02 2004
PATENT & TRADEMARK OFFICE

PTO/SB/08B (08-03)

Substitute for form 1449B/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	10/784,613
Filing Date	February 23, 2004
First Named Inventor	Tsividis, Yannis
Art Unit	2685
Examiner Name	R. Vuong
Attorney Docket Number	021673-000210US

U.S. PATENT DOCUMENTS+

Examiner Initials*	Cite No.[1]	Document Number Number Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
RV	AA	US-2002/0036519	03-28-2002	Krishnapura et al.	
RV	AB	US-2003/0112059	06-19-2003	Krishnapura et al.	
RV	AC	US-2004/0042572	03-04-2004	Palaskas et al.	
RV	AD	US-2004/0091035	05-13-2004	Palaskas et al.	
	AE	US-			

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
	AF					☐
	AG					☐

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
RV	AH	ARYA R. BEHZAD et al., "A 5-GHz Direct-Conversion CMOS Transceiver Utilizing Automatic Frequency Control for the IEEE 802.11a Wireless LAN Standard", IEEE Journal of Solid-State Circuits, Vol. 38, No. 12, December 2003	
RV	AI	VINCENT LEUNG et al., "Digital-IF WCDMA Handset Transmitter IC in 0.25um SiGe BiCMOS", 2004 IEEE International Solid-State Circuits Conference	
RV	AJ	MASOUD ZARGARI et al., "A Single-Chip Dual-Band Tri-Mode CMOS Transceiver for IEEE 802.11a/b/g WLAN", 2004 IEEE International Solid-State Circuits Conference	
	AK		
	AL		

Examiner Signature	Richard Le Vuong	Date Considered	12/17/04

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.
[1] Applicant's unique citation designation number (optional). [2] Applicant is to place a check mark here if English language Translation is attached.

60235517 v1

OIPE JC56 JUL 02 2004 PATENT & TRADEMARK OFFICE

PTO/SB/08A (08-03)

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 2

Complete if Known	
Application Number	10/784,613
Filing Date	02/23/2004
First Named Inventor	Tsividis, Yannis
Art Unit	2685
Examiner Name	Q. Vuong
Attorney Docket Number	021673-000210US

U.S. PATENT DOCUMENTS+

Examiner Initials*	Cite No.[1]	Document Number: Number Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
QV	AA	US-4,270,222	05-26-1981	Menant	
	AB	US-5,001,776	03-19-1991	Clark	
	AC	US-5,390,357	02-14-1995	Nobusawa	
	AD	US-5,392,457	02-21-1995	Davis et al.	
	AE	US-5,406,613	04-11-1995	Peponides et al.	
	AF	US-5,564,094	10-08-1996	Anderson et al.	
	AG	US-5,600,271	02-04-1997	Erickson et al.	
	AH	US-6,026,286	02-15-2000	Bronner	
	AI	US-6,389,445	05-14-2002	Tsividis	
	AJ	US-6,400,177	06-04-2002	Yoshizaki	
	AK	US-6,529,069	03-04-2003	Krishnapura et al.	
	AL	US-20030112060	06-19-2003	Krishnapura et al.	
	AM	US-20030117212	06-26-2003	Krishnapura et al.	
QV	AN	US-6,683,492	01-27-2004	Krishnapura et al.	
	AO	US-			

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document: Country Code[3]	Number[4]	Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
QV	AP	PCT	WO 02/35756		05-02-2002	Yoshizawa et al.		☐
QV	AQ	PCT	WO 02/056558		07-18-2002	Palaskas et al.		☐
QV	AR	PCT	WO 02/056470		07-18-2002	Palaskas et al.		☐
	AS							☐

Examiner Signature	Q. Vuong	Date Considered	12/17/04

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] Kind Codes of U.S. Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

60139978 v1

Substitute for form 1449B/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	10/784,613
				Filing Date	
				First Named Inventor	Tsividis, Yannis
				Art Unit	2685
(use as many sheets as necessary)				Examiner Name	R. Chung
Sheet	2	of	2	Attorney Docket Number	021673-000210US

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
RC	AT	P.R. GRAY et al., "Future Directions in Silicon ICs for RF Personal Communications", IEEE 1995 Custom Integrated Circuits Conference	
	AU	Y. TSIVIDIS, "Minimising power dissipation in analogue signal processors through syllabic companding", Electronic Letters, Vol. 35, No. 21, October 14, 1999	
	AV	AARNO PARSSINEN et al., "A 2-GHz Wide-Band Direct Conversion Receiver for WCDMA Applications", IEEE Journal of Solid-State Circuits, Vol. 34, No. 12, December 1999	
	AW	FARBOD BEHBAHANI et al., "A Broad-Band Tunable CMOS Channel-Select Filter for a Low-IF Wireless Receiver", IEEE Journal of Solid-State Circuits, Vol. 35, No. 4, April 2000	
	AX	TUOMAS HOLLMAN et al., "A 2.7-V CMOS Dual-Mode Baseband Filter for PDC and WCDMA", IEEE Journal of Solid-State Circuits, Vol. 36, No. 7, July 2001	
	AY	FARBOD BEHBAHANI et al., "Adaptive Analog IF Signal Processor for a Wide-Band CMOS Wireless Receiver", IEEE Journal of Solid-State Circuits, Vol. 36, No. 8, August 2001	
	AZ	ATUSHI YOSHIZAWA et al., "An Anti-Blocker Structure MOSFET-C Filter for a Direct Conversion Receiver", IEEE 2001 Custom Integrated Circuits Conference	
	BA	JUSSI RYYNANEN et al., "RF Gain Control in Direct Conversion Receivers", 2002 IEEE	
	BB	ALEKSANDAR TASIC et al., "Concept of Frequency-Transconductance Tuning of Bipolar Voltage-Controlled Oscillators", 2002 IEEE	
	BC	ALEKSANDER TASIC et al., "Concept of Phase-Noise Tuning of Bipolar Voltage-Controlled Oscillators", 2002 IEEE	
	BD	Y. TSIVIDIS et al., "Internally Varying Analog Circuits Minimize Power Dissipation", IEEE Circuits & Devices Magazine, January 2003	
RC	BE	CHRIS VAN DEN BOS et al., "Architecture of a Reconfigurable Radio Receiver Front-End Using Overall Feedback", Electronic Research Laboratory, Delft University of Technology	

Examiner Signature	R. Chung	Date Considered	12/17/04

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.
[1] Applicant's unique citation designation number (optional). [2] Applicant is to place a check mark here if English language Translation is attached.

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Apple EX1002 Page 335
IPR2023-00819
Theta EX2019

Notice of References Cited	Application/Control No. 10/784,613	Applicant(s)/Patent Under Reexamination TSIVIDIS, YANNIS	
	Examiner Quochien B. Vuong	Art Unit 2685	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,298,221	10-2001	Nguyen, Dien M.	455/234.1
	B	US-6,621,339	09-2003	Tripathi et al.	330/136
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Issue Classification	Application/Control No.	Applicant(s)/Patent under Reexamination	
	10/784,613	TSIVIDIS, YANNIS	
	Examiner	Art Unit	
	Quochien B. Vuong	2685	

ISSUE CLASSIFICATION

ORIGINAL		CROSS REFERENCE(S)							
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)						
455	574	455	234.1	251.1	343.1				
INTERNATIONAL CLASSIFICATION									
H 04 B	1/38								
H 04 M	1/00								
/									
/									
/									

(Assistant Examiner) (Date)

Denise Hodkins 9/19/05
(Legal Instruments Examiner) (Date)

QUOCHIEN B. VUONG
PRIMARY EXAMINER

Quochien B. Vuong 9/19/05
(Primary Examiner) (Date)

Total Claims Allowed: 30

O.G. Print Claim(s)	O.G. Print Fig.
1	1

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1		31		61		91		121		151		181
2	2		32		62		92		122		152		182
3	3		33		63		93		123		153		183
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30	30		60		90		120		150		180		210

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Search Notes	Application/Control No.	Applicant(s)/Patent under Reexamination	
	10/784,613	TSIVIDIS, YANNIS	
	Examiner	Art Unit	
	Quochien B. Vuong	2685	

SEARCHED			
Class	Subclass	Date	Examiner
455	63.1, 67.13, 226.1, 226.2, 232.1, 234.1,	9/19/2005	QV
	250.1, 251.1,		
	295, 296,		
	311, 333		
	343.1, 127.1,		
	127.2, 127.5,		
	572, 574		
330	127, 129,		
	134, 136,		
	144		
370	442		

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner
455	574,234.1,	9/19/2005	QV
1	251.1,343.1	1	1
PGPUB text search		9/19/2005	QV

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
EAST search	9/19/2005	QV

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Index of Claims

Application/Control No.	Applicant(s)/Patent under Reexamination
10/784,613	TSIVIDIS, YANNIS
Examiner	**Art Unit**
Quochien B. Vuong	2685

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

Claim		Date
Final	Original	9/19/05
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Claim		Date
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PETITION FOR REVIVAL OF AN APPLICATION FOR PATENT ABANDONED UNINTENTIONALLY UNDER 37 CFR 1.137(b)	Docket Number (Optional) 7084P007

First named inventor: Yannis Tsividis

Application No.: 10/784,613 Art Unit: 2685

Filed: 02/23/2004 Examiner: Vuong, Quochlen B

Title: POWER DISSIPATION REDUCTION IN WIRELESS TRANSCEIVERS

Attention: Office of Petitions
Mail Stop Petition
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
FAX (571) 273-8300

NOTE: If information or assistance is needed in completing this form, please contact Petitions Information at (571) 272-3282.

The above-identified application became abandoned for failure to file a timely and proper reply to a notice or action by the United States Patent and Trademark Office. The date of abandonment is the day after the expiration date of the period set for reply in the office notice or action plus an extensions of time actually obtained.

APPLICANT HEREBY PETITIONS FOR REVIVAL OF THIS APPLICATION

NOTE: A grantable petition requires the following items:
(1) Petition fee;
(2) Reply and/or issue fee;
(3) Terminal disclaimer with disclaimer fee - required for all utility and plant applications filed before June 8, 1995; and for all design applications; and
(4) Statement that the entire delay was unintentional.

1. Petition fee
☑ Small entity-fee $ 750.00 (37 CFR 1.17(m)). Applicant claims small entity status. See 37 CFR 1.27.

☐ Other than small entity – fee $ _____ (37 CFR 1.17(m))

2. Reply and/or fee
A. The reply and/or fee to the above-noted Office action in the form of Amendment (identify type of reply):

☑ has been filed previously on July 6, 2005.
☐ is enclosed herewith.

B. The issue fee and publication fee (if applicable) of $ _____.
☐ has been paid previously on _____.
☐ is enclosed herewith.

This collection of information is required by 37 CFR 1.137(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Mail Stop Petition, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

10/12/2005 EFLORES 00000091 022666 10784613
01 FC:2453 750.00 DA

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3. Terminal disclaimer with disclaimer fee

☑ Since this utility/plant application was filed on or after June 8, 1995, no terminal disclaimer is required.

☐ A terminal disclaimer (and disclaimer fee (37 CFR 1.20(d)) of $ _____ for a small entity or $ _____ for other than a small entity) disclaiming the required period of time is enclosed herewith (see PTO/SB/63).

4. STATEMENT: The entire delay in filing the required reply from the due date for the required reply until the filing of a grantable petition under 37 CFR 1.137(b) was unintentional. [NOTE: The United States Patent and Trademark Office may require additional information if there is a question as to whether either the abandonment or the delay in filing a petition under 37 CFR 1.137(b) was unintentional (MPEP 711.03(c), subsections (III)(C) and (D)).]

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

Roger W Blakely

Signature — October 7, 2005 — Date

Roger W. Blakely, Jr. — Typed or printed name

25,831 — Registration Number, if applicable

12400 Wilshire Boulevard, Seventh Floor — Address

(714) 557-3800 — Telephone Number

Los Angeles, CA 90025 — Address

Enclosures: ☑ Fee Payment

☐ Reply

☐ Terminal Disclaimer Form

☐ Additional sheets containing statements establishing unintentional delay

☑ Other: Copies of Revocation & Power of Attorney and 3.73(b) Statement as previously submitted with Applicant's Communication Dated September 21, 2005

CERTIFICATE OF MAILING OR TRANSMISSION [37 CFR 1.8(a)]

I hereby certify that this correspondence is being:

☐ Deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop Petition, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450.

☑ Transmitted by facsimile on the date shown below to the United States Patent and Trademark Office as (571) 273-8300.

October 3, 2005 — Date

Jessica A Clark

Signature

Jessica A. Clark — Typed or printed name of person signing certificate

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BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP

TELEPHONE: (714) 557-3800
INTELLECTUAL PROPERTY LAW
12400 WILSHIRE BOULEVARD, 7TH FLOOR
LOS ANGELES, CA 90025
FACSIMILE: (714) 557-3347

FACSIMILE COVER SHEET

Deliver to: Vuong, Quochien B, USPTO
Art Group: 2685
Facsimile No.: (571) 273-8300
Date: October 7, 2005
From: Roger W. Blakely, Jr., Reg. No. 25,831
Our Docket No.: 7084P007
Number of pages 8 including this sheet.
Application No.: 10/784,613
Filing Date: 2/23/2004
Docket Due Date(s):

Enclosed are the following documents:

☐ Amendment: (pgs)	☐ Issue Fee Transmittal
☐ Appeal Brief (pgs)	☐ Notice of Appeal
☐ Application:	☒ Petition for: Revival
(pgs) w/cover & abstract)	☐ Request for Continued Examination (RCE)
☐ Assignment & Cover Sheet (pgs)	☐ Reply Brief (pgs)
☒ Certificate of Facsimile	☐ Request & Certification Under 35 USC 122(b)(2)(B)(i)
☐ Continued Prosecution Application (CPA)	☐ Request to Rescind Previous Nonpublication Request
☐ Declaration & POA (pgs)	☐ Response to Notice of Missing Parts & Formalities Letter
☐ Drawings: sheets, figures	☐ Response to Written Opinion (pgs)
☐ Extension of Time:	☐ Terminal Disclaimer
☒ Fee Transmittal (In duplicate)	☐ Transmittal of Publication Fee Due
☐ IDS & PTO/SB/08 (pgs)	☒ Transmittal Letter

☒ Other Copies of Previously Submitted Revocation of Power of Attorney with New Power of Attorney and Change of Correspondence Address and Statement Under 3.73(b)

CERTIFICATE OF MAILING/TRANSMISSION (37 CFR 1.8A)

I hereby certify that this correspondence is being transmitted by facsimile on the date shown below to the United States Patent and Trademark Office.

Jessica A. Clark — 10/7/2005
Jessica A. Clark — *Date*

Confidentiality Note: The documents accompanying this facsimile transmission contain information from the law firm of Blakely, Sokoloff, Taylor & Zafman which is confidential or privileged. The information is intended to be for the use of the individual or entity named on this transmission sheet. If you are not the intended recipient, be aware that any disclosure, copying, distribution or use of the contents of this faxed information is prohibited. If you have received this facsimile in error, please notify us by telephone immediately so that we can arrange for the retrieval of the original documents at no cost to you.

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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Total Number of Pages In This Submission	8

Application No.	10/784,613
Filing Date	February 23, 2004
First Named Inventor	Yannis Tsividis
Art Unit	2685
Examiner Name	Vuong, Quochien B
Attorney Docket Number	7084P007

ENCLOSURES ***(check all that apply)***

- ☒ Fee Transmittal Form
  - ☒ Fee Attached
- ☐ Amendment / Response
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
  - ☐ PTO/SB/08
- ☐ Certified Copy of Priority Document(s)
- ☐ Response to Missing Parts/ Incomplete Application
  - ☐ Basic Filing Fee
  - ☐ Declaration/POA
  - ☐ Response to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☒ Petition
- ☐ Petition to Convert a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
- ☐ Request for Refund
- ☐ CD, Number of CD(s)
- ☐ After Allowance Communication to Group
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☐ Appeal Communication to Group (Appeal Notice, Brief, Reply Brief)
- ☐ Proprietary Information
- ☐ Status Letter
- ☒ Other Enclosure(s) *(please identify below):*

Copies of Previously Submitted Revocation & Power of Attorney and 3.73(b) Statement; Facsimile Cover Sheet

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Roger W. Blakely, Jr., Reg. No. 25,831 BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Signature	Roger W Blakely
Date	October 7, 2005

CERTIFICATE OF MAILING/TRANSMISSION

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Typed or printed name	Jessica A. Clark		
Signature	Jessica A Clark	Date	October 7, 2005

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FEE TRANSMITTAL for FY 2005

Patent fees are subject to annual revision.

☒ Applicant claims small entity status. See 37 CFR 1.27.

TOTAL AMOUNT OF PAYMENT ($) 750.00

Complete If Known	
Application Number	10/784,613
Filing Date	February 23, 2004
First Named Inventor	Yannis Tsividis
Examiner Name	Vuong, Quochien B
Art Unit	2685
Attorney Docket No.	7084P007

METHOD OF PAYMENT *(check all that apply)*

☐ Check ☐ Credit card ☐ Money Order ☐ None ☐ Other (please identify): _____

☒ Deposit Account Deposit Account Number: 02-2666 Deposit Account Name: Blakely, Sokoloff, Taylor & Zafman LLP

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☒ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, except for the filing fee

☒ Charge any additional fee(s) or underpayment of fee(s) under 37 CFR §§ 1.16, 1.17, 1.18 and 1.20. ☐ Credit any overpayments

FEE CALCULATION

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet.	
2053	130	2053	130	Non-English specification	
1251	120	2251	60	Extension for reply within first month	
1252	450	2252	225	Extension for reply within second month	
1253	1,020	2253	510	Extension for reply within third month	
1254	1,590	2254	795	Extension for reply within fourth month	
1255	2,160	2255	1,080	Extension for reply within fifth month	
1401	500	2401	250	Notice of Appeal	
1402	500	2402	250	Filing a brief in support of an appeal	
1403	1,000	2403	500	Request for oral hearing	
1451	1,510	2451	1,510	Petition to institute a public use proceeding	
1460	130	2460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
1809	790	1809	395	Filing a submission after final rejection (37 CFR § 1.129(a))	
1810	790	2810	395	For each additional invention to be examined (37 CFR § 1.129(b))	
Other fee (specify) Petition for Revival Under 37 CFR 1.137(b)					750.00
				SUBTOTAL (2)	($) 750.00

SUBMITTED BY Complete (if applicable)

Name (Print/Type)	Roger W. Blakely, Jr.	Registration No. (Attorney/Agent)	25,831	Telephone	(714) 557-3800
Signature	Roger W. Blakely			Date	10/07/05

Based on PTO/SB/17 (12-04) as modified by Blakely, Sokoloff, Taylor & Zafman (wlr) 12/15/2004.
SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

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Apple EX1002 Page 344
IPR2023-00819
Theta EX2019

REVOCATION OF POWER OF ATTORNEY WITH NEW POWER OF ATTORNEY AND CHANGE OF CORRESPONDENCE ADDRESS		
	Application No.	10/784,613
	Filing Date	February 23, 2004
	First Named Inventor	Yannis Tsividis
	Group Art Unit	2685
	Examiner Name	Vuong, Quochien B.
	Attorney Docket Number	7084P007

I hereby revoke all previous powers of attorney given in the above-identified application:

☐ A Power of Attorney is submitted herewith.

OR

☒ I hereby appoint the practitioners at Customer Number: **08791**

☒ Please change the correspondence address for the above-identified application to:

☒ The address associated with Customer Number: **08791**

OR

☐ Firm or Individual Name	BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP				
Address	12400 Wilshire Boulevard, 7th Floor				
Address					
City	Los Angeles	*State*	California	*Zip Code*	90025
Country	U.S.A.	*Telephone*	(714) 557-3800	*Fax*	(714) 557-3347

I am the:

☐ Applicant.

☒ Assignee of record of the entire interest. See 37 CFR 3.71.
Statement under of 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)

SIGNATURE of Applicant or Assignee of Record

Name	Bruce R. Bowman Chairman & CEO, Theta Microelectronics, Inc.
Signature	Bruce R. Bowman
Date	9-20-2005

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of _____ forms are submitted.

Based on PTO/SB/32 (09-04) as modified by BSTZ (01/19/05 - WCA).
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Docket No. 7084P007

STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: Theta Microelectronics, Inc.

Application No./Patent No.: 10/784,613 Filing/Issue Date: 2/23/2004

Entitled: POWER DISSIPATION REDUCTION IN WIRELESS TRANSCEIVERS

Theta Microelectronics, Inc., a Corporation
(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that it is:

1. ☒ the assignee of the entire right, title and interest; or
2. ☐ an assignee of less than the entire right, title and interest.
The extent (by percentage) of its ownership interest is _____%

in the patent application/patent identified above by virtue of either:

A. ☒ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the Patent and Trademark Office at Reel 15218, Frame 139, or for which a copy thereof is attached.

OR

B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as shown below:

1. From: _____ To: _____
The document was recorded in the Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.
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☐ Additional documents in the chain of title are listed on a supplemental sheet.

☐ Copies of assignments or other documents in the chain of title are attached.
[NOTE: A separate copy (*i.e.*, the original assignment document or a true copy of the original document) must be submitted to Assignment Division in accordance with 37 CFR Part 3, if the assignment is to be recorded in the records of the PTO. See MPEP 302-302.8]

The undersigned (whose title is supplied below) is empowered to sign this statement on behalf of assignee.

September 21, 2005
Date

Roger W. Blakely
Signature

Roger W. Blakely, Jr., Reg. No. 25,831
Typed or printed name

Attorney
Title

Based on PTO/SB/96 (08-03) as modified by Blakely, Sokoloff, Taylor & Zafman (wlr) 05/05/2004.
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UNITED STATES PATENT & TRADEMARK OFFICE
Washington, D.C. 20231

REQUEST FOR **PATENT** FEE REFUND

1 Date of Request: 10/21/05	2 Serial/Patent # 10784613

	3 Please refund the following fee(s):	4 PAPER NUMBER	5 DATE FILED	6 AMOUNT
	Filing			$
	Amendment			$
	Extension of Time			$
	Notice of Appeal/Appeal			$
2453	Petition		10/7/05	$ 750.00
	Issue			$
	Cert of Correction/Terminal Disc.			$
	Maintenance			$
	Assignment			$
	Other			$

7 TOTAL AMOUNT OF REFUND	$ 750.00

8 TO BE REFUNDED BY:

	Treasury Check
X	Credit Deposit A/C #:

9 02--2666

10 REASON:

	Overpayment
	Duplicate Payment
X	No Fee Due (Explanation):

DISMISSED AS MOOT

11 REFUND REQUESTED BY:

TYPED/PRINTED NAME: DOUGLAS WOOD TITLE: SR ATTY

SIGNATURE: [signature] PHONE: 272 3231

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(01/90)

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PETITION FOR REVIVAL OF AN APPLICATION FOR PATENT ABANDONED UNINTENTIONALLY UNDER 37 CFR 1.137(b)	Docket Number (Optional) 7084P007

First named Inventor: Yannis Tsividis

Application No.: 10/784,613 Art Unit: 2685

Filed: 02/23/2004 Examiner: Vuong, Quochien B

Title: POWER DISSIPATION REDUCTION IN WIRELESS TRANSCEIVERS

Attention: Office of Petitions
Mail Stop Petition
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
FAX (571) 273-8300

NOTE: If information or assistance is needed in completing this form, please contact Petitions Information at (571) 272-3282.

The above-identified application became abandoned for failure to file a timely and proper reply to a notice or action by the United States Patent and Trademark Office. The date of abandonment is the day after the expiration date of the period set for reply in the office notice or action plus an extensions of time actually obtained.

APPLICANT HEREBY PETITIONS FOR REVIVAL OF THIS APPLICATION

NOTE: A grantable petition requires the following items:
(1) Petition fee;
(2) Reply and/or issue fee;
(3) Terminal disclaimer with disclaimer fee - required for all utility and plant applications filed before June 8, 1995; and for all design applications; and
(4) Statement that the entire delay was unintentional.

1. Petition fee

☑ Small entity-fee $ 750.00 (37 CFR 1.17(m)). Applicant claims small entity status. See 37 CFR 1.27.

☐ Other than small entity – fee $ _____ (37 CFR 1.17(m))

2. Reply and/or fee

A. The reply and/or fee to the above-noted Office action in the form of Amendment (identify type of reply):

☑ has been filed previously on July 6, 2005.
☐ is enclosed herewith.

B. The issue fee and publication fee (if applicable) of $ _____.

☐ has been paid previously on _____.
☐ is enclosed herewith.

This collection of information is required by 37 CFR 1.137(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: **Mail Stop Petition, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

10/12/2005 EFLORES 00000091 022666 10784613
01 FC:2453 750.00 DA
Adjustment date: 10/24/2005 AKELLEY
10/12/2005 EFLORES 00000091 022666 10784613
01 FC:2453 750.00 CR

IPR2024-00819
Apple EX1002 Page 348
IPR2023-00819
Theta EX2019

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371 (c) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
10/784,613	02/23/2004	Yannis Tsividis	021673-000210US

CONFIRMATION NO. 8357

OC000000017309253

08791
BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

Date Mailed: 10/24/2005

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 10/07/2005.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

DOUGLAS I WOOD
OP (571) 272-3231

OFFICE COPY

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371 (c) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
10/784,613	02/23/2004	Yannis Tsividis	021673-000210US

CONFIRMATION NO. 8357

OC000000017309240

20350
TOWNSEND AND TOWNSEND AND CREW, LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO, CA 94111-3834

Date Mailed: 10/24/2005

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 10/07/2005.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

DOUGLAS I WOOD
OP (571) 272-3231

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UNITED STATES PATENT AND TRADEMARK OFFICE

COMMISSIONER FOR PATENTS
UNITED STATES PATENT AND TRADEMARK OFFICE
P.O. BOX 1450
ALEXANDRIA, VA 22313-1450
www.uspto.gov
DW oct-05

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES CA 90025-1030

COPY MAILED

OCT 24 2005

OFFICE OF PETITIONS

In re Application of :
Yannis Tsividis :
Application No. 10/784,613 : DECISION ON PETITION
Filed: 23 February, 2004 :
Atty Docket No. 021673-000210US :

This is a decision on the petition filed on 7 October, 2005, under 37 CFR 1.137(b), to revive the above-identified application.

The petition is **DISMISSED AS MOOT**.

A review of the record reveals that on 5 January, 2005, a non-final Office action was mailed, setting a three (3) month shortened statutory period for reply.

On 6 July, 2005 (certificate of facsimile transmission date 5 July, 2005), a three (3) month extension of time and amendment in reply to the non-final Office action were filed.

On 26 September, 2005, a Notice of Allowance and Fee(s) Due and Notice of Allowability were mailed, setting a three month period for reply.

As such, the application was never abandoned, and no petition to revive is necessary.

The petition fee will be credited to counsel's deposit account, No. 02-2266.

Receipt of the power of attorney filed on 7 October, 2005, is acknowledged.

The application will be referred to the Office of Publications to await receipt of the issue fee.

Telephone inquiries concerning this matter may be directed to the undersigned at (571) 272-3231.

D Wood

Douglas I. Wood
Senior Petitions Attorney
Office of Petitions

Encl: Notice Regarding Change of Power of Attorney
Notice of Acceptance of Power of Attorney

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov
DRW Dec-05

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES CA 90025-1030

COPY MAILED

DEC 0 8 2005

OFFICE OF PETITIONS

In re Application of	:	
Yannis Tsivdis	:	DECISION ON PETITION
Application No. 10/784,613	:	
Filed: 23 February, 2004	:	
Atty Docket No. 7084P004	:	

This is a decision on the petition, filed on 21 September, 2005, under 37 CFR 1.137(f) which is treated as a petition to revive the above-identified nonprovisional application under the unintentional provisions of 37 CFR 1.137(b).

The petition is **GRANTED**.

Petitioner states that the present nonprovisional application is the subject of a foreign or international application filed on 27 February, 2004. However, the U.S. Patent and Trademark Office was unintentionally not notified of this filing within 45 days subsequent to the filing of the subject application in a foreign country.

In view of the above, this application became abandoned pursuant to 35 U.S.C. § 122(b)(2)(B)(iii) and 37 CFR 1.213(c) for failure to timely notify the Office of the filing of an application in a foreign country, or under a multilateral international agreement, that requires publication of applications 18 months after filing.

A petition under 37 CFR 1.137(f) must be accompanied by:

(1) the reply which is met by the notification of such filing in a foreign country or under a multinational treaty;

(2) the petition fee as set forth in 37 CFR 1.17(m); and

(3) a statement that the entire delay in filing the required reply from the due date of the reply until the filing of a grantable petition was unintentional.

The present petition has been found to be in compliance with 37 CFR 1.137(f). Accordingly, the failure to timely notify the Office of a foreign or international filing within 45 days after the date of filing of such foreign or international application as provided by 35 U.S.C. § 122(b)(2)(B)(i) has been rescinded.

A Notice of Allowability and a Notice of Allowance and Fee(s) Due were mailed in this case on 26 September, 2005. However, in view of the nonpublication request filed with the application, the Notice of Allowance mailed in this case did not require the submission of a publication fee. Therefore, in view of the rescinding of the nonpublication request, a Notice of Publication Fee Due is being mailed under separate cover. Petitioner should note that payment of the publication fee is required to be filed within the period set forth in the Notice to avoid abandonment of the application.

A projected publication date will be assigned in due course. Petitioner will be notified of this date in a separate correspondence.

The application is being referred to the Office of Publication to await receipt of the issue fee.

Any inquiries concerning this decision may be directed to the undersigned at 571.272.3231.

D Wood

Douglas I. Wood
Senior Petitions Attorney
Office of Petitions

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING/RECEIPT DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO.
10/784,613	02/23/2004	Yannis Tsividis	021673-000210US

CONFIRMATION NO. 8357

08791
BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

Date Mailed: 12/09/2005

Communication Regarding Rescission Of Nonpublication Request and/or Notice of Foreign Filing

Applicant's rescission of the previously-filed nonpublication request and/or notice of foreign filing is acknowledged. The paper has been reflected in the Patent and Trademark Office's (USPTO's) computer records so that the earliest possible projected publication date can be assigned.

The projected publication date is 03/16/2006.

If applicant rescinded the nonpublication request before or on the date of "foreign filing,"[1] then no notice of foreign filing is required.

If applicant foreign filed the application after filing the above application and before filing the rescission, and the rescission did not also include a notice of foreign filing, then a notice of foreign filing (not merely a rescission) is required to be filed within 45 days of the date of foreign filing. See 35 U.S.C. § 122(b)(2)(B)(iii), and Clarification of the United States Patent and Trademark Office's Interpretation of the Provisions of 35 U.S.C. § 122(b)(2)(B)(ii)-(iv), 1272 Off. Gaz. Pat. Office 22 (July 1, 2003).

If a notice of foreign filing is required and is not filed within 45 days of the date of foreign filing, then the application becomes abandoned pursuant to 35 U.S.C. § 122(b)(2)(B)(iii). In this situation, applicant should either file a petition to revive or notify the Office that the application is abandoned. See 37 CFR 1.137(f). Any such petition to revive will be forwarded to the Office of Petitions for a decision. Note that the filing of the petition will not operate to stay any period of reply that may be running against the application.

Questions regarding petitions to revive should be directed to the Office of Petitions at (571) 272-3282. Questions regarding publications of patent applications should be directed to the patent application publication hotline at (703) 605-4283 or by e-mail pgpub@uspto.gov.

[1] Note, for purpose of this notice, that "foreign filing" means "filing an application directed to the same invention in another country, or under a multilateral international agreement, that requires publication of applications 18 months after filing".

PART B - FEE(S) TRANSMITTAL

OIPE JAP100 DEC 29 2005 PATENT & TRADEMARK OFFICE

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571) 273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

20350 7590 09/26/2005

~~TOWNSEND AND TOWNSEND AND CREW, LLP~~
~~--TWO EMBARCADERO CENTER~~
~~EIGHTH FLOOR~~
~~SAN FRANCISCO, CA 94111-3834~~
Blakely, Sokoloff, Taylor & Zafman LLP
12400 Wilshire Boulevard, Seventh Floor
Los Angeles, CA 90025

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

Jessica A. Clark	(Depositor's name)
Jessica A. Clark	(Signature)
December 27, 2005	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/784,613	02/23/2004	Yannis Tsividis	021673-000210US	8357

TITLE OF INVENTION: POWER DISSIPATION REDUCTION IN WIRELESS TRANSCEIVERS

12/30/2005 SFELEKE2 00000074 10784613
01 FC:2501 700.00 OP
02 FC:1504 300.00 OP
~~04 FC:1806~~ ~~30.00 OP~~

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	$700	~~$0~~ $300	~~$700~~ $1000	12/27/2005

EXAMINER	ART UNIT	CLASS-SUBCLASS
VUONG, QUOCHIEN B	2685	455-574000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 Blakely, Sokoloff, Taylor & Zafman LLP
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Theta Microelectronics, Inc.
(B) RESIDENCE: (CITY and STATE OR COUNTRY): San Jose, California

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are enclosed:
☒ Issue Fee
☒ Publication Fee (No small entity discount permitted)
☒ Advance Order - # of Copies 10

4b. Payment of Fee(s):
☒ A check in the amount of the fee(s) is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☒ The Director is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number 02-2666 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

The Director of the USPTO is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above.
NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature Roger W. Blakely Date December 27, 2005
Typed or printed name Roger W. Blakely, Jr. Registration No. 25,831

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

IPR2024-00816
Apple EX1002 Page 356
IPR2023-00819
Theta EX2019

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

BIBDATASHEET

Bib Data Sheet

CONFIRMATION NO. 8357

SERIAL NUMBER	FILING OR 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
10/784,613	02/23/2004 RULE	455	2685	021673-000210US

APPLICANTS

Yannis Tsividis, New York, NY;

**** CONTINUING DATA ***************************

This appln claims benefit of 60/451,229 03/01/2003
and claims benefit of 60/451,230 03/01/2003

**** FOREIGN APPLICATIONS ********************

IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** SMALL ENTITY **
** 05/18/2004

Foreign Priority claimed	STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
☐ yes ☐ no	NY	15	30	6
35 USC 119 (a-d) conditions met ☐ yes ☐ no ☐ Met after Allowance				
Verified and Acknowledged Examiner's Signature Initials				

ADDRESS

08791

TITLE

POWER DISSIPATION REDUCTION IN WIRELESS TRANSCEIVERS

FILING FEE RECEIVED		
904	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court for the Eastern District of Texas, Marshall Division on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
2:16-CV-527	5/18/2016	for the Eastern District of Texas, Marshall Division

PLAINTIFF	DEFENDANT
THETA IP, LLC	SAMSUNG ELECTRONICS CO., LTD., and SAMSUNG ELECTRONICS AMERICA, INC.

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	7,010,330	3/7/2006	THETA IP, LLC
2	9,331,728	5/3/2016	THETA IP, LLC
3			
4			
5			

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT		
CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director **Copy 3—Upon termination of action, mail this copy to Director**
Copy 2—Upon filing document adding patent(s), mail this copy to Director **Copy 4—Case file copy**

AO 120 (Rev. 08/10)

TO:	**Mail Stop 8** **Director of the U.S. Patent and Trademark Office** **P.O. Box 1450** **Alexandria, VA 22313-1450**	**REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK**

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court for the Eastern District of Texas, Marshall Division on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
2:16-cv-527	5/18/2016	for the Eastern District of Texas, Marshall Division

PLAINTIFF	DEFENDANT
Theta IP, LLC	Samsung Electronics Co., Ltd.; Samsung Electronics America, Inc.; Samsung Telecommunications America, LLC

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	7010330	3/7/2006	Theta IP, LLC
2	9331728	5/3/2016	Theta IP, LLC
3			
4			
5			

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Northern District of Illinois/Eastern Division on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
22cv3441	06/30/2022	Northern District of Illinois/Eastern Division

PLAINTIFF	DEFENDANT
Theta IP, LLC	Motorola Mobility LLC, Lenovo (United States) Inc., Lenovo Group Limited

PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 See Attached		
2		
3		
4		
5		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE
Thomas G. Bruton	David Jozwiak	07/05/2022

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

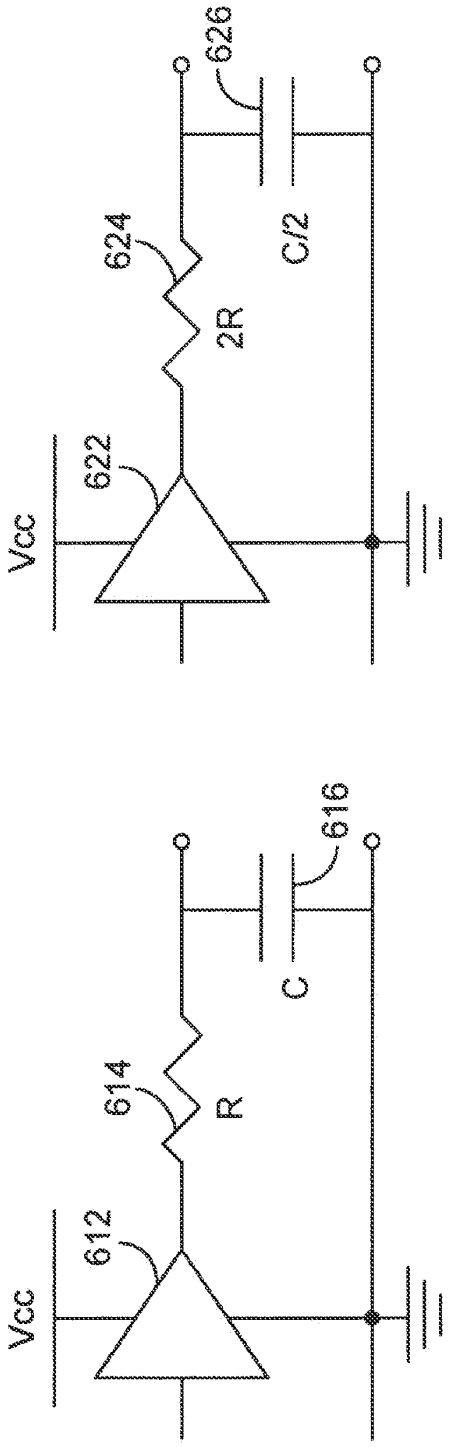


FIG. 6

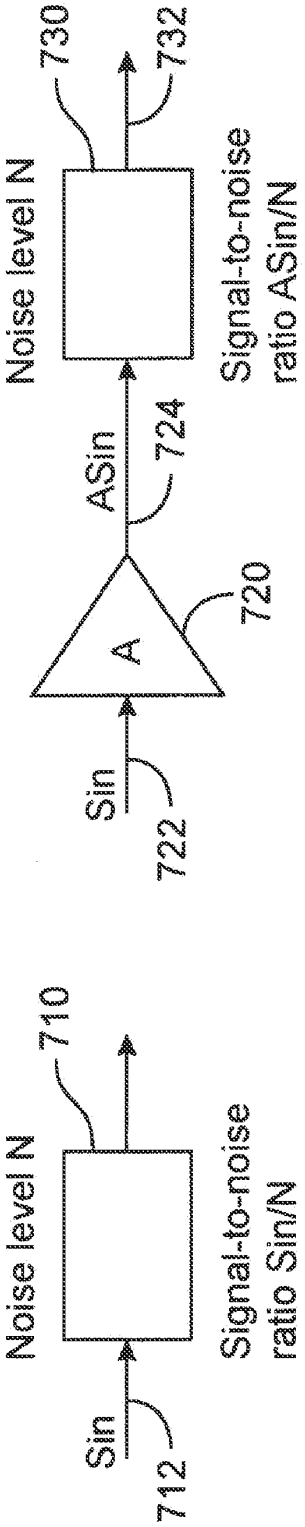

730
732
Noise level N
Signal-to-noise ratio ASin/N
ASin
724
720
A
Sin
722
710
Noise level N
Signal-to-noise ratio Sin/N
Sin
712

FIG. 7

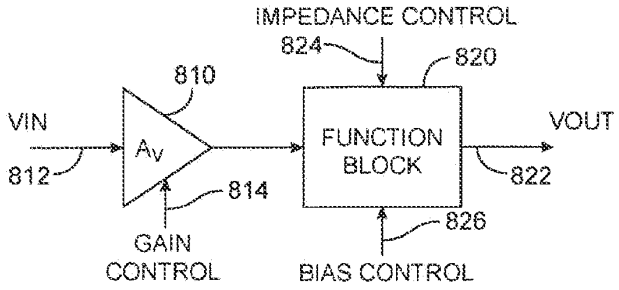


FIG. 8A

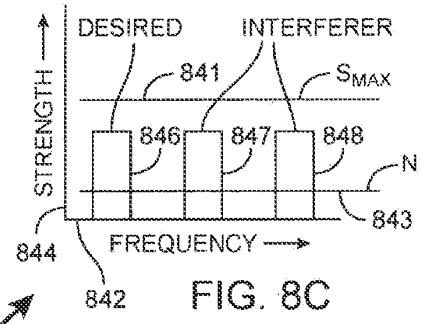


FIG. 8C

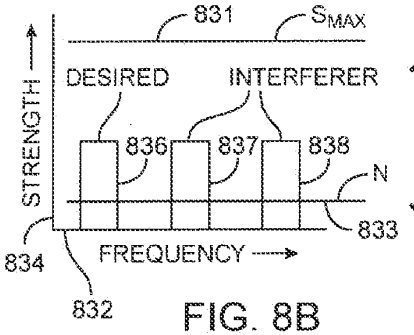


FIG. 8B

DECREASE BIASING

– AND/OR –

INCREASE GAIN AND IMPEDANCES

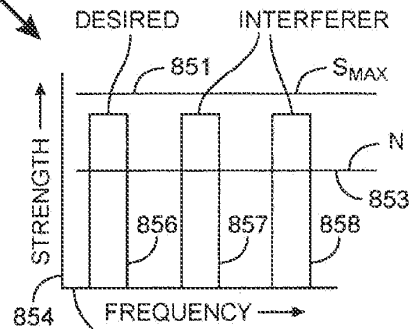


FIG. 8D

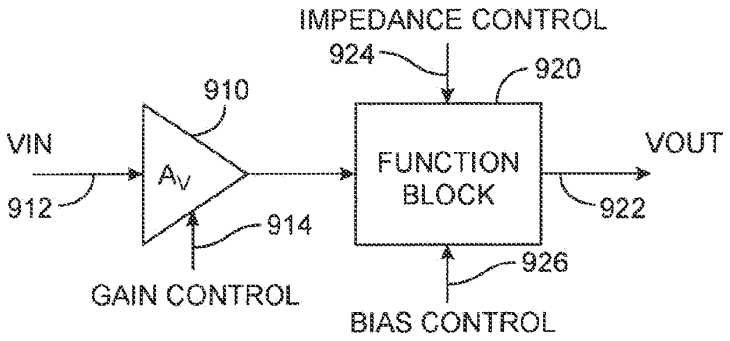


FIG. 9A

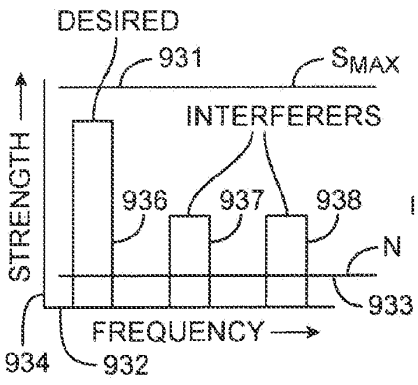


FIG. 9B

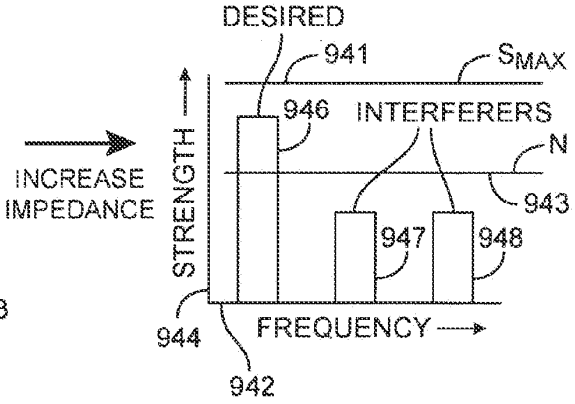


FIG. 9C

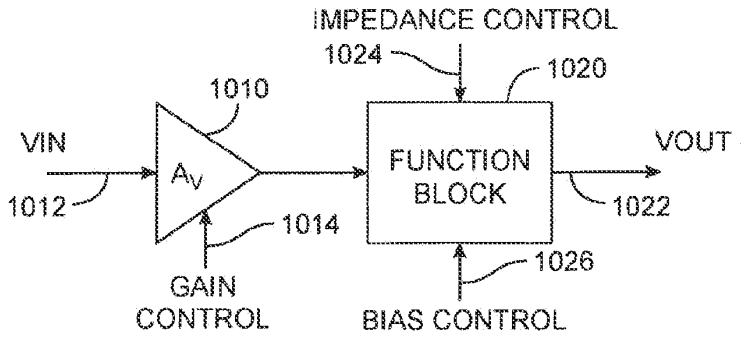


FIG. 10A

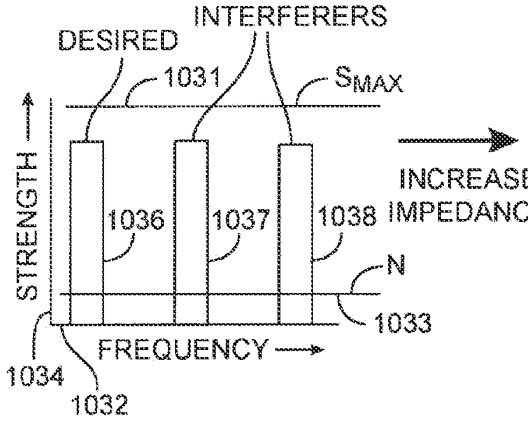


FIG. 10B

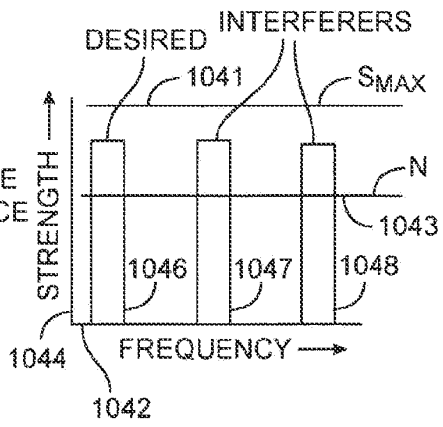


FIG. 10C

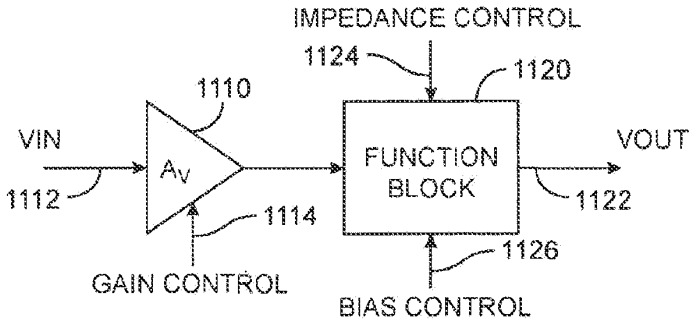


FIG. 11A

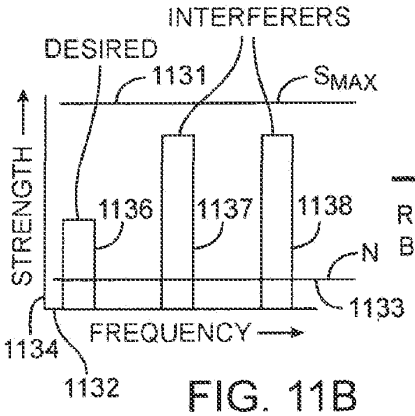


FIG. 11B

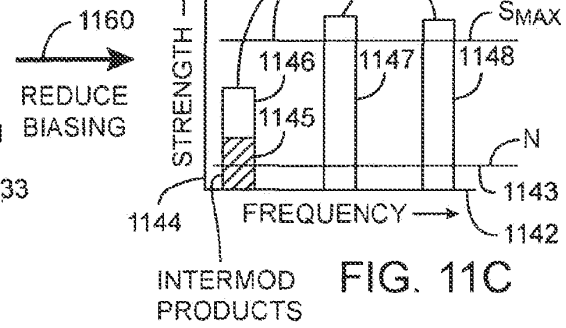
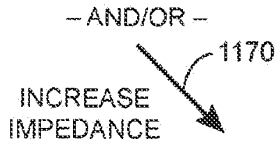


FIG. 11C



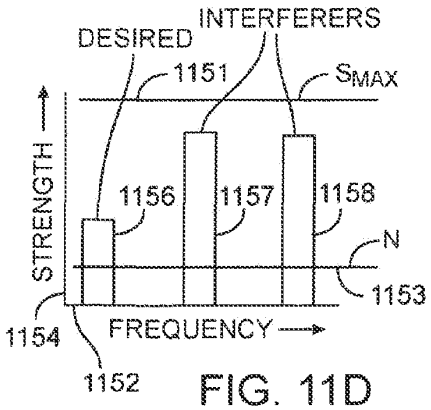


FIG. 11D

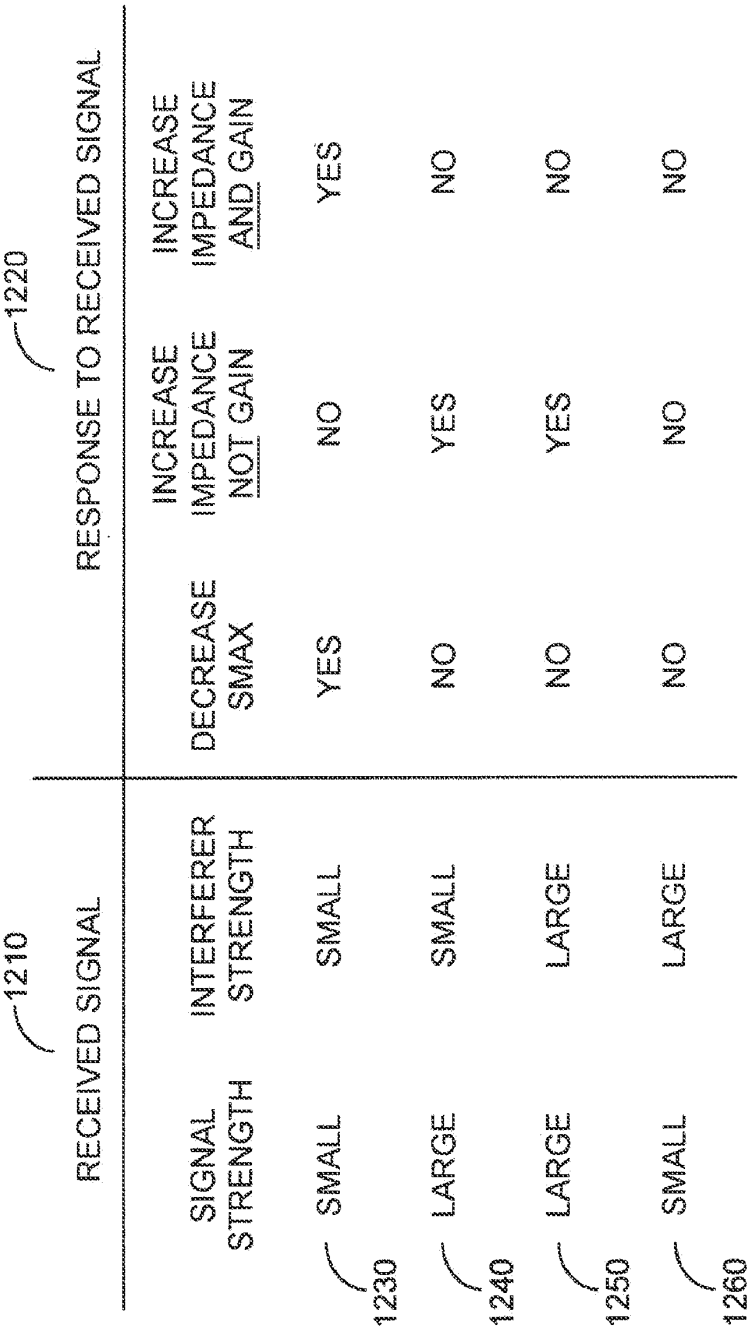

1210
RECEIVED SIGNAL
1220
RESPONSE TO RECEIVED SIGNAL
SIGNAL STRENGTH
INTERFERER STRENGTH
DECREASE SMAX
INCREASE IMPEDANCE NOT GAIN
INCREASE IMPEDANCE AND GAIN
SMALL
SMALL
YES
NO
YES
1230
LARGE
SMALL
NO
YES
NO
1240
LARGE
LARGE
NO
YES
NO
1250
SMALL
LARGE
NO
NO
NO
1260

FIG. 12

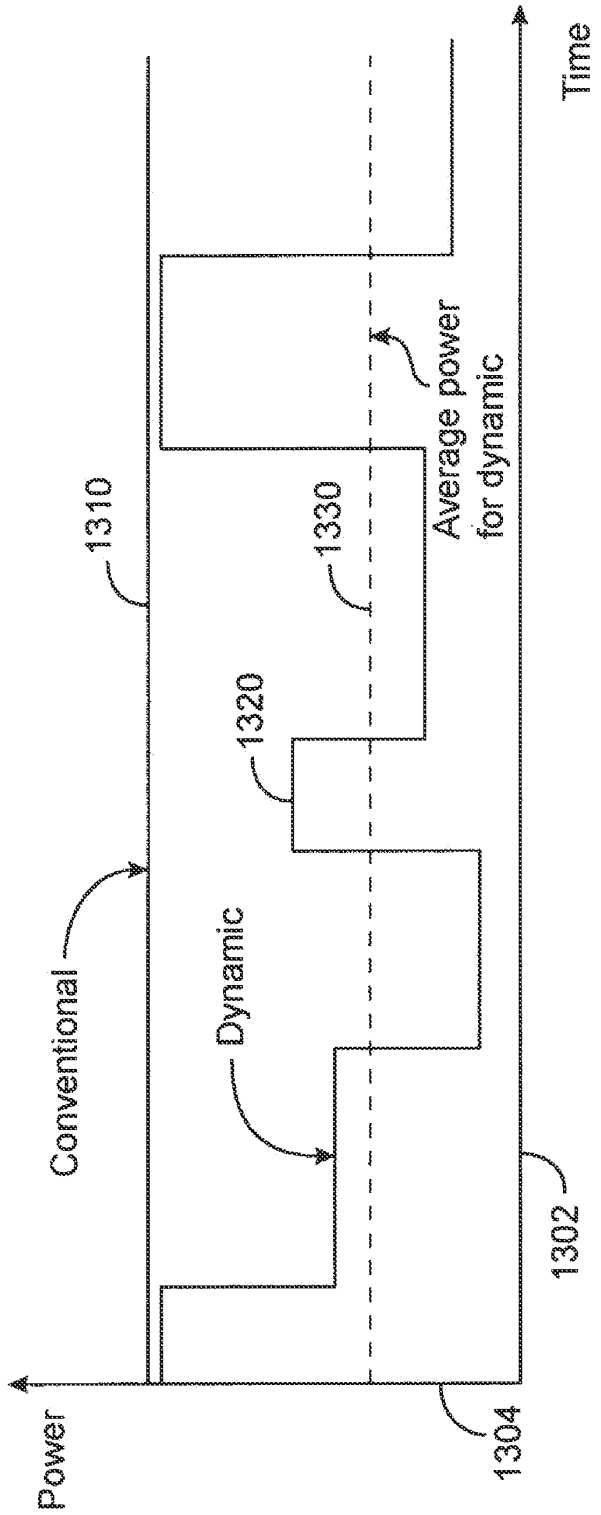

Power
Time
Conventional
Dynamic
1310
1320
1330
1302
1304
Average power
for dynamic

FIG. 13

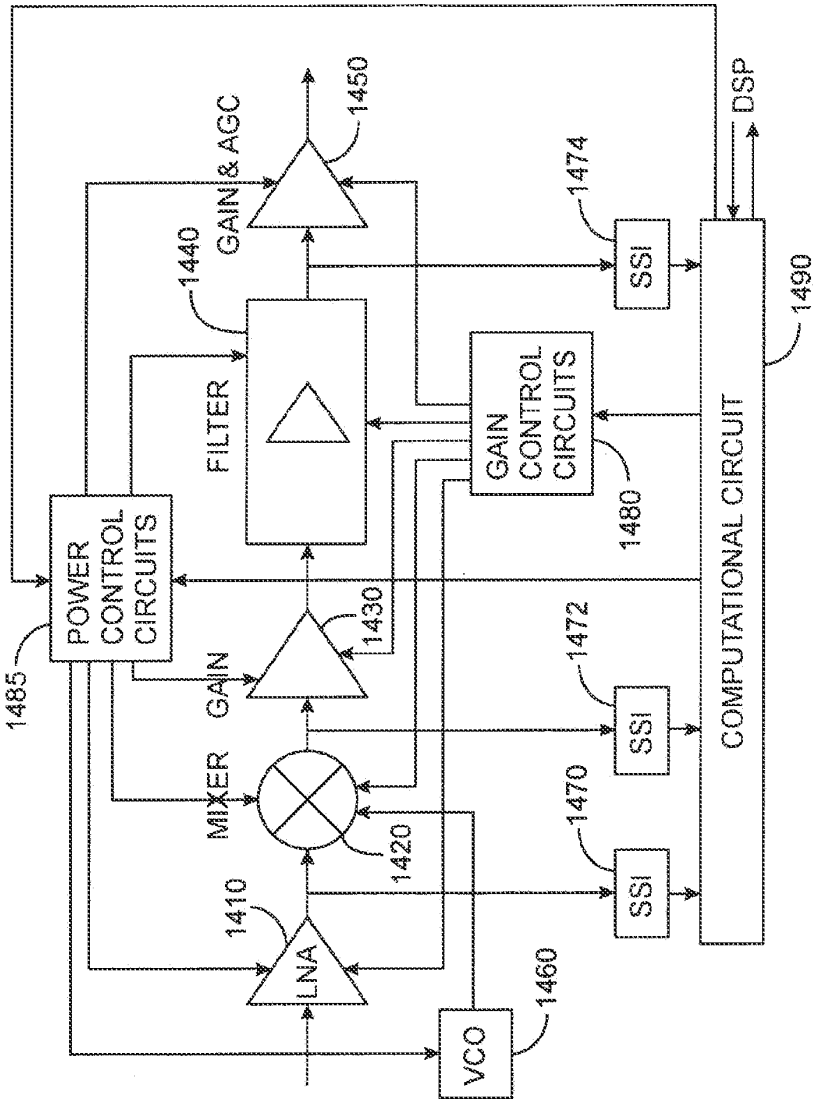

1450
GAIN & AGC
1440
FILTER
1430
GAIN
1410
LNA
1420
MIXER
1460
VCO
1485
POWER CONTROL CIRCUITS
1480
GAIN CONTROL CIRCUITS
1470
1472
1474
SSI
SSI
SSI
1490
COMPUTATIONAL CIRCUIT
DSP

FIG. 14

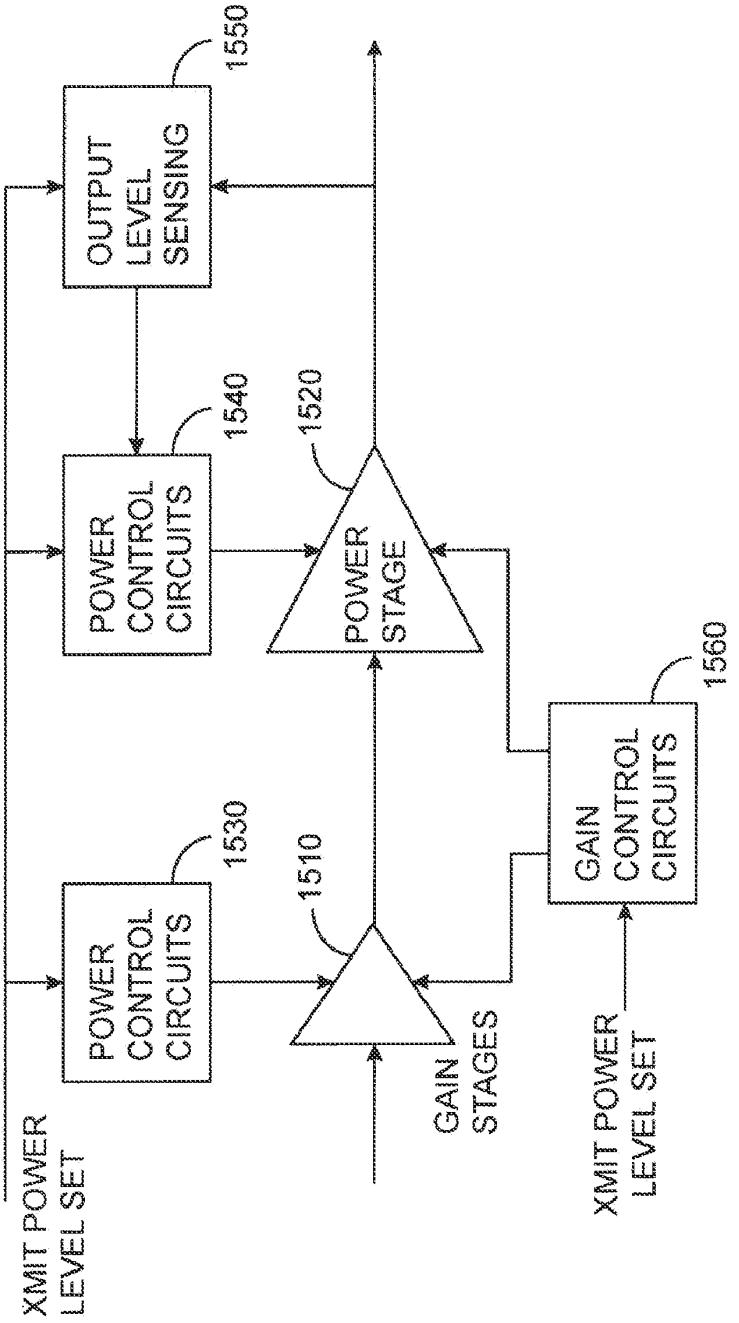

XMIT POWER LEVEL SET
POWER CONTROL CIRCUITS
1530
1510
GAIN STAGES
POWER CONTROL CIRCUITS
1540
1520
POWER STAGE
OUTPUT LEVEL SENSING
1550
GAIN CONTROL CIRCUITS
1560
XMIT POWER LEVEL SET

FIG. 15

Exhibit A

POWER DISSIPATION REDUCTION IN WIRELESS TRANSCEIVERS

CROSS-REFERENCES TO RELATED APPLICATIONS

This application claims the benefit of U.S. provisional application No. 60/451,229, filed Mar. 1, 2003, which is incorporated by reference.

This application is related to U.S. provisional application No. 60/451,230, filed Mar. 1, 2003, which is incorporated by reference.

BACKGROUND

The present invention relates to power dissipation reduction techniques for electronic circuits, for example wireless transceiver integrated circuits.

Wireless networking is quickly becoming ubiquitous, as desktop, notebook, and handheld computers are connected to share Internet access and files. Wireless networking cards compatible with PCMCIA and compact flash form factors are popular for laptops and handhelds respectively, particularly as mobile users connect to the Internet on the road at coffee shops, hotels, and airports.

A downside of this connectivity is a corresponding drain on battery life, especially for these portable devices. The power consumed by a wireless transmitter and receiver reduces the usefulness of a device and sends a user on a hunt for an electrical outlet for recharging.

One reason why this power drain is high is that electronic circuits are typically designed to function properly under worst-case operating conditions. For a wireless transceiver, the worst case condition is when a desired signal reception strength is low, while other transceivers or nearby electronic equipment generate interfering signals and other spurious noise.

But a wireless transceiver does not always operate in these worst-case conditions. For example, a base station, router or access point may be nearby such that the received signal is strong. Also, there may be no interfering signals, or they may be relatively weak. In these situations, receiver circuit currents can be reduced below what is necessary for the worst case condition. If this is done, power dissipation is reduced, and battery life is increased.

Thus, what is needed are circuits and methods that can adapt to a better-than-worst-case condition and reduce circuit currents and therefore power dissipation accordingly.

SUMMARY

Accordingly, embodiments of the present invention provide methods and circuits for reducing power dissipation in wireless transceivers and other electronic circuits and systems. Embodiments of the present invention use bias current reduction, impedance scaling, gain, and other dynamic changes either separately or in combination to reduce power dissipation in response to better-than-worst case conditions. For example, bias currents are reduced in response to a need for reduced signal handling capability, impedances are scaled thus reducing required drive and other bias currents in response to a strong received signal, or gain is varied and impedances are scaled in response to a low received signal in the presence of no or weak interfering signals. Alternately, currents may start low and be increased in response to worse-than-best-case conditions, or they may start at a point in between and vary up or down. These variations may be made to electronic systems generally, and are particularly suited and discussed below in the context of a wireless transceiver that may be used in networking devices, cellular telephones, and other wireless systems.

An exemplary embodiment of the present invention provides a method of receiving a signal using an integrated circuit. The integrated circuit includes a signal path having a low-noise amplifier configured to receive the signal, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer. The method itself includes determining a first signal strength at a first node in the signal path in the integrated circuit and dynamically changing an impedance of a component in the signal path based on the first signal strength.

A further exemplary embodiment of the present invention provides a method of receiving a signal using an integrated circuit. The integrated circuit includes a signal path having a low-noise amplifier configured to receive the signal, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer. The method itself includes determining a first signal strength at a first node in the signal path in the integrated circuit and dynamically changing a bias current in the signal path based on the first signal strength.

Another exemplary embodiment of the present invention provides a method of receiving a signal using an integrated circuit. The integrated circuit includes a signal path having a first circuit and a second circuit having an input coupled to an output of the first circuit. The method itself includes determining a first signal strength at a first node in the signal path in the integrated circuit. The first node is before the first circuit in the signal path. The method further includes dynamically changing a gain of the first circuit based on the first signal strength and dynamically changing an impedance of a component in the second circuit based on the first signal strength.

Still a further exemplary embodiment of the present invention provides a wireless transceiver integrated circuit including a receiver having a signal path, the signal path including a low-noise amplifier, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer, as well as a first signal strength indicator circuit coupled to the signal path and configured to determine a first signal strength. An impedance in the signal path is configured to be dynamically adjusted in response to the first signal strength.

Yet a further exemplary embodiment of the present invention provides a wireless transceiver integrated circuit. This integrated circuit includes a receiver comprising a signal path, the signal path having a low-noise amplifier, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer, as well as a first signal strength indicator circuit coupled to the signal path, and configured to determine a first signal strength. A bias current in the signal path is configured to be dynamically adjusted in response to the first signal strength.

Another exemplary embodiment of the present invention provides a wireless transceiver integrated circuit. This circuit includes a receiver comprising a signal path, the signal path having a first circuit; and a second circuit having an input coupled to an output of the first circuit; as well as a first signal strength indicator circuit coupled to the signal path, and configured to determine a first signal strength. A gain of the first circuit is configured to be dynamically adjusted in

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response to the first signal strength, and an impedance in the second circuit is configured to be dynamically adjusted in response to the first signal strength.

A better understanding of the nature and advantages of the present invention may be gained with reference to the following detailed description and the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram of a wireless transceiver that may benefit by incorporation of embodiments of the present invention;

FIGS. **2**A and **2**B illustrate examples of desired and interfering signals and noise that may be received by a circuit in a wireless receiver;

FIG. **3** illustrates what can occur as a maximum signal handling capability is reduced in the worst-case signal condition;

FIG. **4** illustrates a portion of a receiver consistent with an embodiment of the present invention;

FIG. **5** illustrates the relationship between a required bias current and a given output signal for a representative circuit;

FIG. **6** is an example of how a circuit's impedances may be scaled to reduce drive currents, and depending on the circuit configuration used, to reduce associated bias currents as well;

FIG. **7** illustrates how gain may be inserted in a signal path to improve a circuit's signal to noise ratio;

FIGS. **8**A–**8**D illustrate some of the possible power saving techniques that may be used when received desired and interferer signals are all at a low power level;

FIGS. **9**A–**9**C illustrate one of the possible power saving techniques that may be used when a received desired signal is strong while all interfering signals are at a low power level;

FIGS. **10**A–**10**C illustrate one of the possible power saving techniques that may be used when received desired and interferer signals are all at a high power level;

FIGS. **11**A–**11**D illustrate one of the possible power saving techniques that may be used when a received desired signal is weak while one or more interfering signals are strong;

FIG. **12** is a summary illustrating four different input conditions and some of the appropriate power-saving changes that may be made in response to those conditions;

FIG. **13** shows how power may be saved as a function of time by employing one or more of the power saving methods consistent with embodiments of the present invention;

FIG. **14** is a block diagram of a portion of a receiver consistent with an embodiment of the present invention; and

FIG. **15** is a block diagram of a portion of a transmitter consistent with an embodiment of the present invention.

DESCRIPTION OF EXEMPLARY EMBODIMENTS

FIG. **1** is a block diagram of a wireless transceiver that may benefit by incorporation of embodiments of the present invention. This wireless transceiver may be designed to send and receive signals consistent with the IEEE 802.11a, 802.11b, 802.11 g, or other signaling standard or combination of standards. This figure, as with all the included figures, is shown for illustrative purposes only and does not to limit either the possible embodiments of the present invention or the claims.

There are three main portions of this transceiver circuit, a receiver, transmitter, and synthesizer. This transceiver may be completely or partially integrated on a semiconductor chip, or it may be integrated onto multiple integrated circuits. In a specific embodiment, the circuitry bounded by dashed line **100** is integrated on a single chip coupled to one or more external components or circuits. The integrated circuit or circuits forming this wireless transceiver may incorporate various integrated circuit devices such as a bipolar, CMOS, or BiCMOS devices made using a silicon, silicon-germanium (SiGe), gallium arsenide or other III-V process, or other manufacturing process. Embodiments of the present invention may also be applicable to circuits manufactured using nanotechnology processing.

The receiver includes a signal path formed by low-noise amplifier **102**, I and Q mixers **104** and **106**, low pass filters **108** and **110**, and baseband amplifiers **114** and **116**. Other circuitry in the receiver includes received strength indicator **122**, automatic gain control circuit **166**, baseband gain control circuit **120**, tuning circuit **112**, and offset cancellation circuit **118**.

The transmitter includes input up-converter mixers **124** and **126**, summing node **176**, which may be conceptual rather than an actual circuit, transmit variable gain amplifier **128**, and power amplifier **130**.

The synthesizer includes a voltage-controlled oscillator **148**, which drives I and Q buffers **154** and **152**, prescaler **156**, reference clock buffer **142** and divider **158**, phase-frequency detector **160**, charge pump **162**, and loop filter **146**, which in a specific embodiment is formed by external components.

Signals are received on an antenna, not shown, and typically pass through an RF switch and bandpass filter before being received by the low-noise amplifier **102** on line **101**. The low noise amplifier gains the received signal and provides it to quadrature mixers **104** and **106**. I and Q mixers **104** and **106** down-convert the received signal to baseband by multiplying them with quadrature versions of the oscillator signal provided by buffers **152** and **154**. This down conversion also produces a high frequency component at a frequency that is equal to the sum of the frequencies of the received signal and the VCO. This unwanted signal is filtered by low pass filters **108** and **110**, which in turn drive baseband amplifiers **114** and **116**. The outputs of baseband amplifiers **114** and **116** are typically converted to digital signals by analog-to-digital converters at the front end of a digital signal processing block.

In the transmit mode, I and Q versions of the signal to be transmitted are provided on lines **121** and **123** to up-convert mixers **124** and **126**. These up-convert mixers multiply the I and Q portions of the transmit signal by quadrature versions of the VCO signal provided by buffers **152** and **154**. The outputs of the up-convert mixers **124** and **126** are summed, and amplified by transmit VGA **128**, which in turn drives power amplifier **130**. The output of power amplifier **130** is typically filtered, and passes through the RF switch to the antenna for transmission.

A reference clock is received and buffered by the reference buffer **142**. The VCO generates quadrature oscillatory signals that are divided by prescaler **156**. The reference clock is typically generated by a crystal or other stable periodic clock source. The phase-frequency detector **116** compares the phase or frequency (depending on whether the synthesizer is tracking or acquiring the correct frequency) of the divided VCO signal and the reference clock, or a divided version of the reference clock, and generates an error signal, which drives the charge pump **162**. The output signal of the

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charge pump **162** is filtered by the loop filter **146**, which is commonly a lead-lag filter, and which provides a tuning or correction signal to the VCO **148**.

Embodiments of the present invention may be used to reduce the power dissipation of one or more of these included circuits. For example, the power dissipation in the low-noise amplifier **102**, down-convert mixers **104** and **106**, low pass filters **108** and **110**, or baseband amplifiers **114** and **116** may be optimized. Also, power dissipation in up-convert mixers **124** **126**, variable gain amplifier **128**, and power amplifier **130** may also be optimized. Similarly, VCO **148** and prescaler **156** currents may be adjusted. Embodiments of the present invention may also be applied in other circuits which may be included in other integrated circuit receivers, transmitters, transceivers, or other electronic circuits or systems.

When a receiver is actively receiving a desired signal, each block in the signal path has at its input the desired signal as well as noise and possibly interfering signals. The desired signal is the useful, information-carrying portion of a received signal. The noise may be thermal, shot, or other noise generated on the integrated circuit, in addition to received noise generated by sources external to the chip. The noise at the input of a block may be referred to as the equivalent input noise. The interfering signal or signals, or interferers, may be generated by similar transceivers, or other electrical equipment, circuits, or systems.

FIGS. **2**A and **2**B illustrate examples of desired signals, interferers, and noise that may be received by one of the various circuits in a wireless receiver. In each of these figures, the signal strength is plotted along a Y-axis **204** or **254** as a function of frequency along an X-axis **202** or **252**. In the example of FIG. **2**A, a received desired signal **206** is large in comparison to interfering signals **208** and **210**. In these examples, two interfering signals are shown for illustrative purposes, though there may be no such signals, one such signal, or more than two such signals in the frequency range of interest. Also, while for these examples the interferers are shown as being at a higher frequency than the desired signal, there may be one or more interferers at higher or lower frequencies as the desired signal. In this specific example, the acceptable noise floor **214** is relatively high, while maximum signal handling capability Smax **212** (that is the maximum signal power that can be handled with an acceptably low distortion) needs only to be high enough to accommodate the desired signal. For this specific example, the circuit receiving this input spectrum only requires a relatively small dynamic range for proper operation, that is the range between Smax **212** and the noise floor **214** is relatively small.

Conversely, in the example shown in FIG. **2**B, the desired signal **256** is relatively weak compared to the large interferers **258** and **260**. In this example, the noise floor **264** should be relatively low so as to prevent an unacceptable level of error in the recovery the desired signal **256**. The maximum signal handling capability Smax **262** should be relatively high to accommodate the large interferers in order to avoid the creation of intermodulation products as described below. Accordingly, in this specific example, the circuit receiving this input spectrum should have a large dynamic range, particularly in comparison to the example of FIG. **2**A.

It should be noted that the noise level or noise floors shown in these and the other included figures is the noise density integrated over the bandwidth of interest. For simplicity and comparison, this level is shown as a horizontal line, and is not meant to imply noise density.

Often in wireless receivers, a circuit at different times will receive an input spectrum similar to those shown in FIGS. **2**A and **2**B. The input spectrum of FIG. **2**B is generally considered the worst-case input signal, and typical design methodology involves designing a receiver for this condition, specifically the weakest desired signal accompanied by largest interference level. Circuit impedances and currents are set such that the noise floor **264** is sufficiently low for an acceptable bit-error rate, while bias currents are set sufficiently high for the required Smax **262**.

Conversely, the input spectrum in FIG. **2**A is that of the best-case input signal, specifically, a robust desired signal accompanied by no or low-level interferers. In this case, the noise floor **214** may be allowed to rise, while the maximum signal handling capability Smax **212** may be reduced. When this is done, the receiver circuit may save significant power. For example, the circuit's impedances may be increased, thus reducing required drive currents. Similarly, bias currents may be lowered, thus reducing the maximum signal in handling capability.

The minimum power dissipation for a circuit is proportional to the required maximum signal-to-noise ratio, which is the ratio between Smax **212** or **262** and N **214** and **264**. Thus, a circuit receiving an input similar to the one shown in FIG. **2**A can dissipate less power than one receiving the input as shown in FIG. **2**B, while still achieving an acceptable bit-error rate.

FIG. **3** illustrates what can occur when the maximum signal handling capability Smax **314** is reduced in the worst-case condition, that is when a weak desired signal **306** is accompanied by large interferers **310** and **312**. Again, signal strength is plotted along a Y-axis **304** as a function of frequency along X-axis **302**. In this specific example, Smax **314** is reduced below the peak levels of the interferers **310** and **312**. Since Smax is low, the circuit cannot handle the interferers linearly. The resulting nonlinearities lead to a mixing of the interferers and the creation of intermodulation products **308** (for example, a third-order intermodulation distortion, IM3), one of which in this example occurs at the same frequency as the desired signal **306**. As can be seen, if the intermodulation products **308** become excessive, the received signal bit error rate may become excessive, and the desired signal **306** may be lost. Accordingly, while Smax may be lowered even under some unfavorable conditions in order to reduce power, care should be taken to avoid corruption of the received desired signal.

FIG. **4** illustrates a portion of a receiver consistent with an embodiment of the present invention. Included is a filter **430**. An optional gain element **420** is placed in front of the filter **430** in order to increase signal levels. Signal strength indicator circuits **440** and **450** are connected to input line **410** and output line **460**. In this specific example, the input signal spectrum on line **410** is shown as desired signal **412** and interferers **414** and **416**. The signal spectrum at the output line **460** is shown as desired signal **462** and interferers **464** and **466**. The signal strength indicators **440** and **450** do not provide information as to the relative sizes of the desired and interfering signals. Rather, a cumulative signal level is provided at their outputs. For example, the first signal strength indicator **440** outputs a level corresponding to the sum of desired signal **412** and interfering signals **414** and **416**, while the second signal strength indicator **450** provides a signal level corresponding to the sum of desired signal **462** and interfering signals **464** and **466**. In this specific example, the gain of the gain and filter circuit combinations is shown as approximately one, while the interfering signals **414** and **416** signal levels are reduced.

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A comparison of the signal levels provided by the signal strength indicators **440** and **450** indicates that much of the combined received signal on line **410** has been filtered. Accordingly, it may be deduced that large interfering signals present at the input are being filtered by the filter **430**. From this information, as will be shown in greater detail below, the bias, impedance, and gain of the gain stage **420** and filter **430** combination may be optimized to reduce power dissipation.

There are several real world situations where the received signal is better than the worst-case condition such that power can be saved. For example, large interferers may be present only part of the time, that is, on a temporary or transient basis. The interfering equipment may be some distance from the transceiver, or it may be operating in the low power mode. Also, the desired signal may be very strong as compared to the noise and interferers, for example a hub, router, or access point may be nearby.

Some transceivers consistent with embodiments of the present invention are designed to work with more than one data transfer specification or standard. In this case, when a transceiver is operating in a mode having a lower data rate, the power saving techniques described here may be employed.

FIG. **5** illustrates the relationship between a required biased current **516** for a given output signal **514** for a representative circuit **510**. If the output signal current level is relatively low, such as the output current shown as **526**, the corresponding bias current **528** may be low. Conversely, if the output signal current level is larger as with the example **536**, the corresponding bias current level **538** should also be high. Accordingly, if a bias current is initially set high to handle large a large input signal, for example a large interferer, this current may be reduced if the input signal is smaller.

There are many ways by which these bias currents can be reduced. For example, the current may be generated by placing a voltage across a resistor by applying a bias voltage to the base of a device whose emitter is connected to ground through a resistance. In this case, the resistor may be increased by opening switches across portions of the resistance, or lowering the bias voltage applied at the base. Several ways in which this may be done will be readily understood by one skilled in the art.

FIG. **6** is an example of how a circuit's impedances may be scaled to reduce drive currents, and, depending on the circuit configuration used, associated bias currents as well. A driver **612** has a load R **614** and C **616**. The frequency response of this circuit is the same as that seen by driver **622**, which drives an impedance of 2R **624** and C/2 **626**. But the impedance of the load seen by driver **622** is double that seen by **612**, thus the output current required by the driver **622** is reduced by one-half.

As an example, the output stage of each of these drivers may be a Class A emitter follower formed by an emitter follower connected to a current source. When the outputs are driven high, the emitter of driver **622** need supply only one-half the drive current as driver **612**. In this way, an impedance can be scaled in order to decrease a circuit's required drive current.

Also, the discharge current for driver **622** is only one half that of driver **612** for a given negative-going slew rate. Thus, the current source of **622** may be reduced by the same factor of one-half as compared to driver **612**. In this example, the bias current, that is the current in the pull-down current source can be reduced. Many other examples where drive currents and possibly bias currents may be reduced will be appreciated by one skilled in the art.

FIG. **7** illustrates another degree of freedom that made be employed to reduce current levels in a transceiver. Specifically, a gain element **720** may be inserted in front of a circuit block **730** in order to improve the combined circuit's signal-to-noise ratio by a factor equal to the gain of the inserted gain block. This is particularly useful when large interferers are absent and the desired received signal is moderate or low. Specifically, gain is added to the signal while impedances are increased, which raise the noise floor. In this way, a given signal-to-noise ratio may be maintained while the power is decreased.

The gain of such an element may be varied by increasing a current in a differential pair or increasing a load resistance using switches. Many other examples where the gain of this element may be varied will be appreciated by one skilled in the art.

These variables, or degrees of freedom, specifically reducing bias currents, increasing impedances, and increasing gain may be used as in the following examples.

FIG. **8A** is a block diagram of a functional block **820** and optional gain element **810** in accordance with an embodiment of the present invention. Functional block **820**, like the functional blocks in the following diagrams, may be a filter, mixer, amplifier, or other circuit or circuits in a wireless transceiver or other electronic circuits or system. An input signal is received on line **812** by the optional gain element **814**. When the optional gain block **810** is not used, the input signal may be received directly by the function block **820**. The gain of the optional gain element **812** is controlled by a gain control signal on line **814**. The functional block receives an output signal from the optional gain element **810** and provides an output VOUT on line **822**. The lines in this and the other included figures may be one or more lines, depending on whether single-ended, differential, or other type of signaling is employed.

One or more impedances are under control of signals on impedance control lines **824**. Similarly, one or more bias currents in the function block are under control of one or more signals on bias control lines **826**. These various control lines may be logic signals, analog signals, voltage or currents lines, or other signal or bias lines. In other embodiments of the present invention, the gain control element **810** may be included in the function block **820**. Also, various embodiments may not incorporate either or both the impedance control and bias control.

FIG. **8B** is an example input that may be present on line VIN **812**. In this example, a desired signal **836** is relatively weak, as are interfering signals **837** and **838**. The initial bias and circuit configuration is such that the noise floor **833** and maximum signal handling capability Smax **831** are adjusted for worst case conditions. The circuit of FIG. **8A**, as with all the circuits described here, receives noise at its input which may be referred to as input equivalent noise or input referred noise. Additionally, the circuit of FIG. **8A** generates noise which is added to the input referred noise. Depending on the gain characteristics of the circuitry, the output noise at various frequencies may be greater than, equal to, or less than the input referred noise. For simplicity, the noise floor and maximum signal handling capability Smax, in this and the other figures, are shown as straight lines, though the noise and Smax are typically curved as a function of frequency.

That the input spectrum is as shown in FIG. **8B** can be determined, for example, by low signal strength indications on line VIN **812** and VOUT **822**. That is, a low level signal strength indication on line VIN **812** indicates that no portion of the input signal is particularly large.

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For this exemplary input, there are at least two methods by which the power dissipation for this circuitry may be reduced. Depending on the exact circuits and structures used, one of these methods may be preferred.

In FIG. **8**C, the bias current is decreased, thereby lowering the maximum signal handling capability **841** as compared to **831**, closer to the desired and interfering signal levels. Again, the bias currents in the function block **820** may be reduced by switching impedances that appear across a voltage thereby changing a resulting bias current, by reducing a voltage at the gate of a MOS or base of a bipolar transistor, or by other methods.

In FIG. **8**D, a second method of reducing power dissipation in the function block **820** is employed. Specifically, Smax **851** is held constant as compared Smax **831**. The desired and interfering signals are amplified such that they are closer to the available signaling handling capability **851**. Also, the noise floor **853** is raised as compared to noise floor **833** in FIG. **8**B. Specifically, the noise contributed by the function block **820** is increased, such that the noise at its output is increased to noise floor **853**. This is done by increasing one or more impedance in function block **810**, such that drive currents inside that block are reduced. Depending on the exact configuration, this may also allow some biasing currents to be reduced, while maintaining the maximum signal handling capability **851** at a sufficient level. Alternately, these two methods of reducing power dissipation in function block **820** may be done in combination.

The included examples are explained for the exemplary situation where biasing and other parameters are set for worst-case conditions, and then changed to save power when it is discovered that the conditions are better-than-worst case. Alternately, the bias currents and other parameters may be set for maximum power savings, or an intermediate point, and the power can be adjusted from there.

FIG. **9**A illustrates a block diagram including an optional gain element **910** and function block **920**. Again, an input signal is received on line **912** by optional gain element **910** which in turn drives function block **920**. The function block provides an output VOUT on line **922**, and receives impedance and bias control signals on lines **924** and **926**.

FIG. **9**B shows the spectrum for what may be considered a best-case received signal. Specifically, the desired signal **936** is strong, while the interfering signals **937** and **938** are relatively weak. This may be determined, for example, by detecting a large signal level at the input line VIN **812** and a large signal level after a filter, since these readings would indicate that a large signal is received, but that it is at the desired signal frequency.

The maximum signaling capability **931** and noise floor **933** are shown as being set for the worst case conditions. In this case, the noise floor **933** is lower than the maximum allowed for proper signal reception. Accordingly, one or more impedance in the function block **920** may be increased, such that the noise floor **943** rises as shown in FIG. **9**C. In this way one or more the driving currents in the function block **920** may be reduced. Similarly, since the drive current is reduced, one or more bias current may also be reduced, depending on the exact circuit configuration.

FIG. **10**A illustrates a block diagram showing an optional gain element **1010** driving a function block **1020**. An input signal is received by the gain element **1010** on line **1012**, and an output is provided by function block **1020** on line VOUT **1022**. One or more gain control signals present on lines **1014** control the gain of gain control element **1010**, while one or more impedance and bias control signals are received by the function block **1020** on line to **1024** and **1026**.

FIG. **10**B illustrates a received signal that may be received on line VIN **1012**. In this example, the desired signal **1036** and interferers **1037** and **1038** are each relatively large. This may be determined, for example, by detecting a large signal level at the input line VIN **812** and a smaller signal level after a filter, since these readings would indicate that a large signal is received, but that interferers are being reduced.

As before, in this example, the noise floor **1033** and maximum signal handling capability **1031** are initially set for the worst case conditions. Since the desired signal is relatively large in this case, the noise floor may be allowed to rise, a shown by noise floor **1043** in FIG. **10**C. Since the desired signal **1046** and interferers **1047** are large, the maximum signal handling capability Smax **1041** remains constant. Again, the noise floor is increased by increasing impedances in the function block **1020**. This reduces the required drive current, and may also allow for a reduction in bias currents.

FIG. **11**A illustrates a block diagram including an optional gain element **1110** and function block **1120** in accordance with an embodiment of the present convention. An input signal is received on line **1112** by the optional gain control element **1110**, while an output signal is provided by the function block **1120** on line VOUT **1122**. Gain, impedance, and bias control signals are received on lines **1114**, **1124**, and **1126**.

FIG. **11**B is an exemplary input signal that may be received by the gain control element **1110** on line VIN **1112**. In this specific example, the desired signal **1136** is relatively low or weak while the interfering signals **1137** and **1138** are large. This may be determined, for example, by detecting a large signal level at the input line VIN **812** and a much smaller signal level after a filter, since these readings would indicate that a large signal is received and that large interferers are being reduced such that the resulting signal, the desired signal, is relatively weak.

Again, the maximum signal handling capability **1131** and noise floor **1133** are initially set for worst case conditions. If the desired signal is sufficiently low, while the interferers are sufficiently high, power savings may not be achievable over the worst case settings, since this is in fact the worst case condition. But, if the desired signal is somewhat larger than the worst case condition, then power may be saved in at least two different ways.

For example, FIG. **11**C shows the maximum signal handling capability **1141** being lowered. In this case, the interfering signals **1147** in **1148** began to clip and distort, thereby creating intermodulation products **1145**, which distort the desired signal **1146**. So long as care is taken to not corrupt the desired signal **1146** beyond an acceptable limit, typically measured by a bit-error rate, power may be reduced in this way.

Similarly, in FIG. **11**D, the noise floor **1153** is raised somewhat, thereby saving power. Again, this may be done so long as the noise floor is not sufficiently high that the system bit-error rate becomes unacceptable.

FIG. **12** is a summary of the above four examples. The received signal strengths are shown in column **1210**, while appropriate power saving responses are listed in column **1220**. Specifically, in row **1230**, the desired signal and interferer signal strengths are both weak or small. In this case, proper responses include decreasing Smax, or increasing one or more circuit impedances while increasing the circuit gain. Depending on the exact circuit configuration, one of these options may be preferred over the other. Alternately, they may be done in combination, or done in combination with other power saving techniques. Also, in

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some specific embodiments, when both desired signal and interferer signal strengths are small, the gain may need to be increased while the impedance is maintained or not increased in order to keep the noise floor low.

In row **1240**, the desired signal strength is strong or large, while the interfering signals are small. In this case, an appropriate response is to increase one or more of the circuit impedances. Again, depending on the exact circuit in question, one or more of the bias currents may also be reduced.

In row **1250**, both the desired signals and interfering signal strengths are large. Again, in this case an appropriate response is to increase one or more of the circuit impedances.

In row **1260**, the received desired signal strength is weak or small, while the interfering signals are large. Since this is the worst case situation for which the circuit is designed, substantial power savings are difficult to achieve. However, again, if the received signal is above a minimum level necessary for proper operation, some distortion of the interferers or raising of the noise floor may be acceptable.

It should be noted that not all possible signal conditions are listed here. For example, either the signal or interferer may be of a relatively medium strength, or the interferer may be absent. Also, these terms are for exemplary purposes and are not meant to convey specific signal conditions, but rather are only qualitative. The proper response to a specific condition depends on the embodiment of the present invention, the particular circuit topology, the requirements of the signaling standard used, as well as other constraints.

FIG. **13** is an example shown how power may be saved as a function of time by employing one or more of these methods consistent with embodiments of the present invention. Power is plotted along a Y-axis **1304** as a function of time along X-axis **1302**. Conventional worst case design would fix power dissipation at line **1310**. As can be seen, dynamic power dissipation **1320** under the control of variable gains, impedances, biasing, or combination thereof, allows for a lower average power **1330** as compared to the power dissipated **1310** by the conventional design.

FIG. **14** is a block diagram of a portion of a receiver consistent with an embodiment of the present invention. Included are low-noise amplifier **1410**, mixer **1420**, gain stage **1430**, filter **1440**, AGC amplifier **1450**, and VCO **1460**. Signal strength detection is done at the output of the low-noise amplifier by signal strength indicator **1470**, at the output of the mixer by signal strength indicator **1472**, and at the output of the filter by signal strength indicator **1474**. The outputs of the signal strength indicator circuits are received by the computational circuit **1470**, which in turn controls gain and power control circuits **1480** and **1485**. Power and gain control circuits **1480** and **1485** control the gain, biasing, and impedance levels of the circuits in the receiver signal path. Also, the gain and power control circuits may control the same parameters in the VCO **1460**. This figure is greatly simplified for purposes of explanation. For example, the quadrature nature of the mixers and following circuits are not shown. Also, power-down and start-up circuits are not included.

The current level in the low-noise amplifier determines a multitude of parameters including voltage gain, linearity, input impedance matching, and noise figure. When conditions are better than worst-case, some of these parameters may be relaxed while maintaining an acceptable bit-error rate, thus saving power.

The bias current in the mixers effect that block's noise figure and linearity. Care is taken in reducing power in this block so as not to increase nonlinearities, particularly the third-order nonlinearity as measured by IP3, the third-order intercept point, beyond an acceptable limit.

A key parameter of the VCO is phase noise, an increase in which increases the sidebands on either side of the oscillation signal. During transmission, the phase noise should be kept low to avoid interference with adjacent channels and for preserving modulation information.

During reception however, if the conditions are better than worst case, the phase noise requirement for the VCO is relaxed, and power can be saved consistent with embodiments of the present invention. The achievable phase noise power spectral density is approximately inversely proportional to the bias current used. Thus, when low phase noise is not required during reception, bias current in the VCO can be reduced.

Most of the power savings in a transceiver in accordance with embodiments of the present invention is achieved in the receiver portion. Additional power may be saved in the transmitter section.

FIG. **15** is a block diagram of a transmitter portion consistent with an embodiment of the present invention. Included is a signal path formed by gain stage **1510** and power amplifier **1520**. The output power level is sensed by output level sensing circuit **1550**, which in turn adjusts the biasing of the power amplifier **1520** through the power control circuit **1540**. Additionally, a transmitter level control signal is received by power control circuits **1530** and **1540**, which in turn control the biasing of gain stage **1510** and power amplifier **1520**. Gain control circuit **1560** also adjusts the gain of gain stage **1510** and power amplifier **1520**. Additional circuitry that varies impedances in each of these circuits may also be included.

Since the gain, impedance and biasing of these blocks are being dynamically varied, care must be taken to not negatively affect the signal being processed. For example, specific embodiments of the present invention perform some or all of these variations during preamble. Also, as changes occur, the circuits in some embodiments are limited such that they may only adapt to an improvement in conditions after frames are completed. If conditions worsen, the circuits may be allowed to change in order to save the data. Alternately, a system may be manually calibrated, for example at set up, and when the network configuration is changed.

The above description of specific embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form described, and many modifications and variations are possible in light of the teaching above. The embodiments were chosen and described in order to best explain the principles of the invention and its practical applications to thereby enable others skilled in the art to best utilize the invention in various embodiments and with various modifications as are suited to the particular use contemplated.

What is claimed is:

1. A method of receiving a signal using an integrated circuit, the integrated circuit comprising a signal path including a low-noise amplifier configured to receive the signal, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer, the method comprising:

determining a first signal strength at a first node in the signal path in the integrated circuit; and

reducing a switching current in the signal path by dynamically changing an impedance of a component in the signal path based on the first signal strength.

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2. The method of claim 1 wherein the signal comprises a preamble portion and a data portion, the impedance of a component is changed while receiving the preamble portion, and the method further comprises receiving the data portion of the signal.

3. The method of claim 2 further comprising:

determining a second signal strength at a second node in the signal path, wherein the second node in the signal path is after the first node in the signal path.

4. The method of claim 3 wherein the impedance of the component in the signal path is also changed based on the second signal strength.

5. The method of claim 2 wherein the component in the signal path comprises a MOS transistor.

6. The method of claim 2 wherein the component in the signal path comprises a resistor.

7. The method of claim 2 wherein the component in the signal path comprises a capacitor.

8. The method of claim 4 wherein the component in the signal path is included in the mixer.

9. The method of claim 4 wherein the component in the signal path is included in the low-pass filter.

10. A method of receiving a signal comprising a preamble portion and a data portion using an integrated circuit, the integrated circuit comprising a signal path including a low-noise amplifier configured to receive the signal, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer, the method comprising:

determining a first signal strength at a first node in the signal path in the integrated circuit; and

while receiving the preamble portion of the signal, dynamically changing a bias current in the signal path based on the first signal strength, and while receiving the data portion of the signal, maintaining the bias current in the signal path.

11. The method of claim 10 wherein the method further comprises receiving the data portion of the signal.

12. The method of claim 11 further comprising:

determining a second signal strength at a second node in the signal path, wherein the second node in the signal path is after the first node in the signal path.

13. The method of claim 12 wherein the bias current in the signal path is also changed based on the second signal strength.

14. The method of claim 11 wherein the bias current is a bias current for the low-noise amplifier.

15. The method of claim 11 wherein the bias current is a bias current for the mixer.

16. The method of claim 11 wherein the bias current is a bias current for the low-pass filter.

17. A method of receiving a signal using an integrated circuit, the integrated circuit comprising a signal path including a first circuit and a second circuit having an input coupled to an output of the first circuit, the method comprising:

determining a first signal strength at a first node in the signal path in the integrated circuit, wherein the first node is before the first circuit in the signal path;

dynamically changing a gain of the first circuit based on the first signal strength; and

dynamically changing an impedance of a component in the second circuit based on the first signal strength.

18. The method of claim 17 wherein the signal comprises a preamble portion and a data portion, the gain and impedance are changed while receiving the preamble portion, and the method further comprises receiving the data portion of the signal.

19. The method of claim 18 further comprising:

determining a second signal strength at a second node in the signal path, wherein the second node in the signal path is after the second circuit in the signal path.

20. The method of claim 19 wherein the gain of the first circuit and impedance of the component in the second circuit is also changed based on the second signal strength.

21. The method of claim 18 wherein the first circuit is a low-noise amplifier.

22. The method of claim 18 wherein the first circuit is a mixer.

23. A wireless transceiver integrated circuit comprising:

a receiver comprising a signal path, the signal path comprising:

a low-noise amplifier;

a mixer having an input coupled to an output of the low-noise amplifier; and

a low-pass filter having an input coupled to an output of the mixer; and

a first signal strength indicator circuit coupled to the signal path, and configured to determine a first signal strength;

wherein an impedance in the signal path is configured to be dynamically adjusted to reduce a switching current in response to the first signal strength.

24. The wireless transceiver of claim 23 further comprising:

a second signal strength indicator circuit coupled to the output of the mixer, and configured to determine a second signal strength,

wherein the first signal strength indicator is coupled to the output of the low-noise amplifier, and

wherein the impedance in the signal path is configured to be adjusted in response to the first and second signal strengths.

25. The wireless transceiver of claim 23 further comprising:

a second signal strength indicator circuit coupled to the output of the low-pass filter, and configured to determine a second signal strength,

wherein the first signal strength indicator is coupled to the output of the mixer, and

wherein the impedance in the signal path is configured to be adjusted in response to the first and second signal strengths.

26. A wireless transceiver integrated circuit comprising:

a receiver comprising a signal path, the signal path comprising:

a low-noise amplifier;

a mixer having an input coupled to an output of the low-noise amplifier; and

a low-pass filter having an input coupled to an output of the mixer; and

a first signal strength indicator circuit coupled to the signal path, and configured to determine a first signal strength, the first signal strength the strength of a signal comprising a preamble portion and a data portion;

wherein a bias current in the signal path is configured to be dynamically adjusted during the preamble portion of the signal in response to the first signal strength and further configured to be maintained during the data portion of the signal.

27. The wireless transceiver of claim 26 further comprising:

a second signal strength indicator circuit coupled to the output of the mixer, and configured to determine a second signal strength,

wherein the first signal strength indicator is coupled to the output of the low-noise amplifier, and

wherein the bias current in the signal path is configured to be adjusted in response to the first and second signal strengths.

28. The wireless transceiver of claim 26 further comprising:

a second signal strength indicator circuit coupled to the output of the low-pass filter, and configured to determine a second signal strength,

wherein the first signal strength indicator is coupled to the output of the mixer, and

wherein the bias current in the signal path is configured to be adjusted in response to the first and second signal strengths.

29. A wireless transceiver integrated circuit comprising:

a receiver comprising a signal path, the signal path comprising:

a first circuit; and

a second circuit having an input coupled to an output of the first circuit; and

a first signal strength indicator circuit coupled to the signal path, and configured to determine a first signal strength;

wherein a gain of the first circuit is configured to be dynamically adjusted in response to the first signal strength, and

wherein an impedance in the second circuit is configured to be dynamically adjusted in response to the first signal strength.

30. The wireless transceiver of claim 29 further comprising:

a transmitter comprising:

a power amplifier; and

an output-level-sensing circuit coupled to an output of the power amplifier,

wherein the output-level-sensing circuit is configured to dynamically adjust a gain of the power amplifier.

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(54) **POWER DISSIPATION REDUCTION IN WIRELESS TRANSCEIVERS**

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(58) **Field of Classification Search** 455/63.1, 455/67.13, 226.1, 226.2, 232.1, 234.1, 250.1, 455/251.1, 295, 296, 311, 333, 343.1, 127.1, 455/127.2, 127.5, 574, 572; 370/442; 330/127, 330/129, 134, 136, 144
See application file for complete search history.

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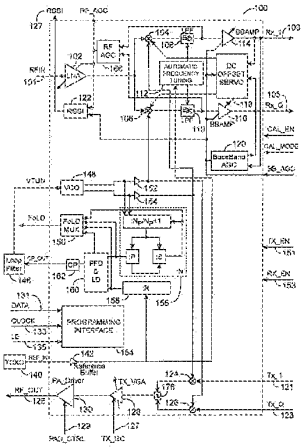
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(57) **ABSTRACT**

Methods and circuits for reducing power dissipation in wireless transceivers and other electronic circuits and systems. Embodiments of the present invention use bias current reduction, impedance scaling, and gain changes either separately or in combination to reduce power dissipation. For example, bias currents are reduced in response to a need for reduced signal handling capability, impedances are scaled thus reducing required drive and other bias currents in response to a strong received signal, or gain is increased and impedances are scaled in response to a low received signal in the presence of no or weak interfering signals.

30 Claims, 15 Drawing Sheets



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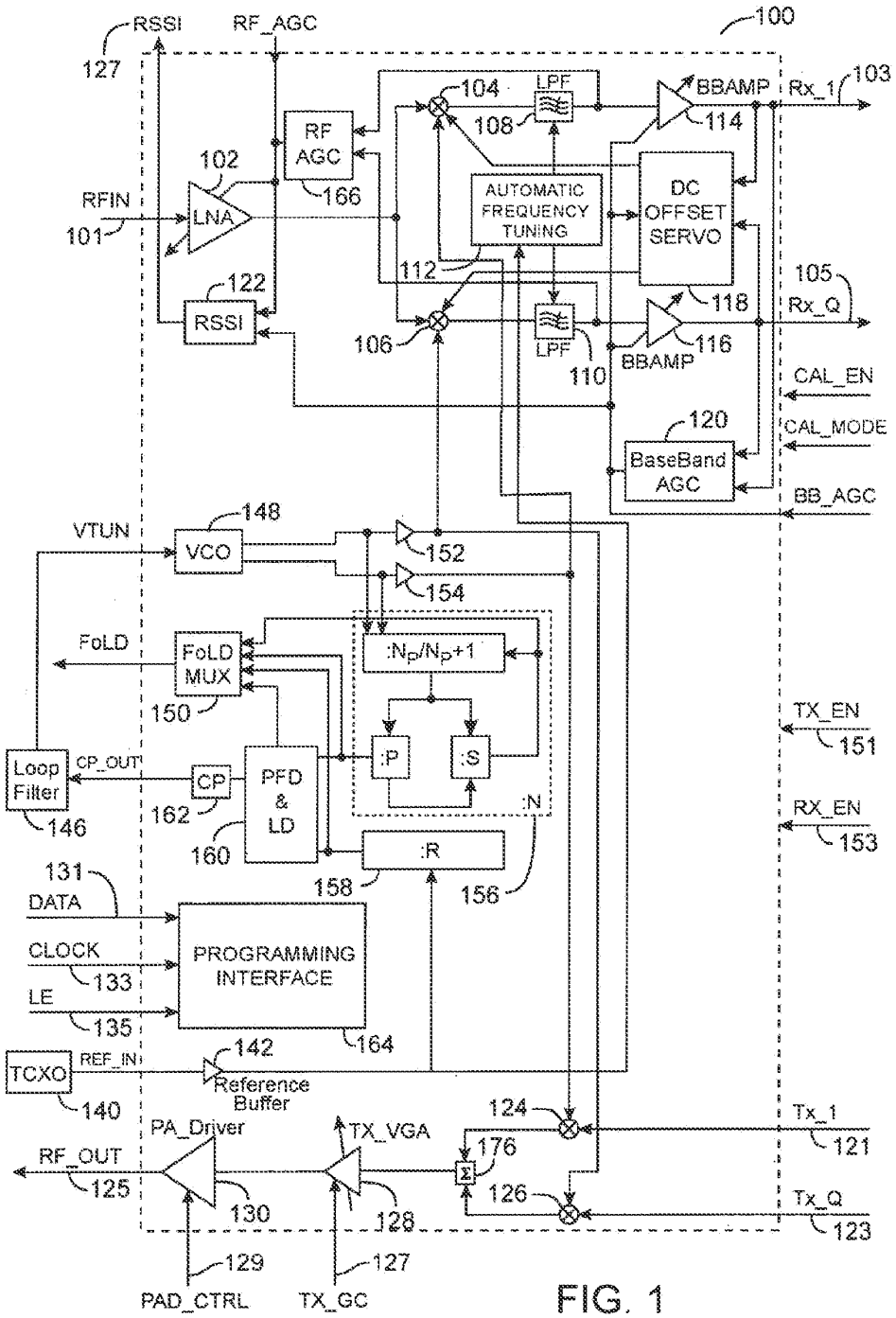

RSSI
127
RF_AGC
100
104
LPF
108
BBAMP
114
Rx_1
103
RF AGC
166
102
RFIN
101
LNA
AUTOMATIC FREQUENCY TUNING
DC OFFSET SERVO
118
112
105
Rx_Q
122
RSSI
106
LPF
110
BBAMP
116
CAL_EN
CAL_MODE
120
BaseBand AGC
BB_AGC
148
VTUN
VCO
152
154
FoLD
FoLD MUX
150
:Np/Np+1
TX_EN
151
Loop Filter
146
CP_OUT
CP
162
PFD & LD
:P
:S
:N
160
:R
158
156
RX_EN
153
131
DATA
CLOCK
133
LE
135
PROGRAMMING INTERFACE
164
TCXO
140
REF_IN
142
Reference Buffer
124
Tx_1
121
PA_Driver
TX_VGA
176
RF_OUT
125
130
128
126
Tx_Q
123
129
PAD_CTRL
127
TX_GC

FIG. 1

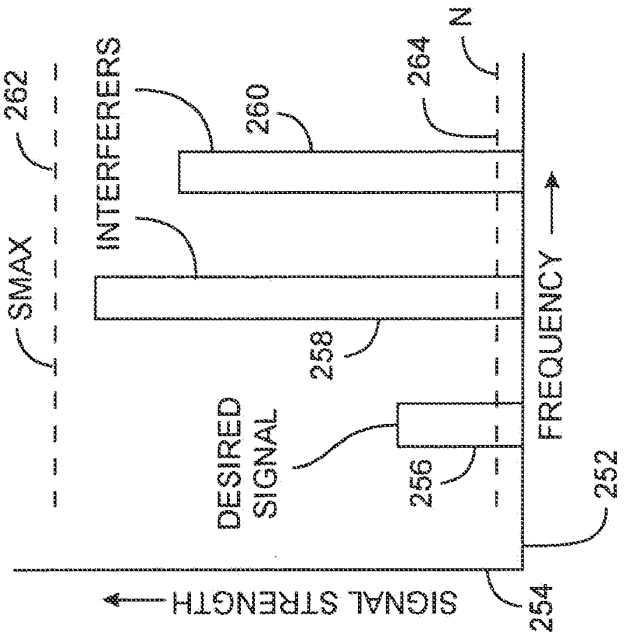

SMAX
262
INTERFERERS
260
264
N
258
DESIRED SIGNAL
256
FREQUENCY
252
SIGNAL STRENGTH
254

FIG. 2B

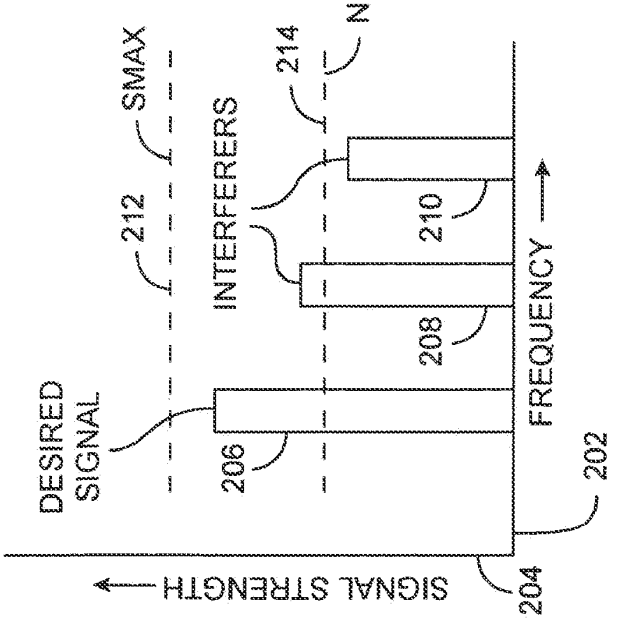

DESIRED SIGNAL
206
SMAX
212
INTERFERERS
214
N
208
210
FREQUENCY
202
SIGNAL STRENGTH
204

FIG. 2A

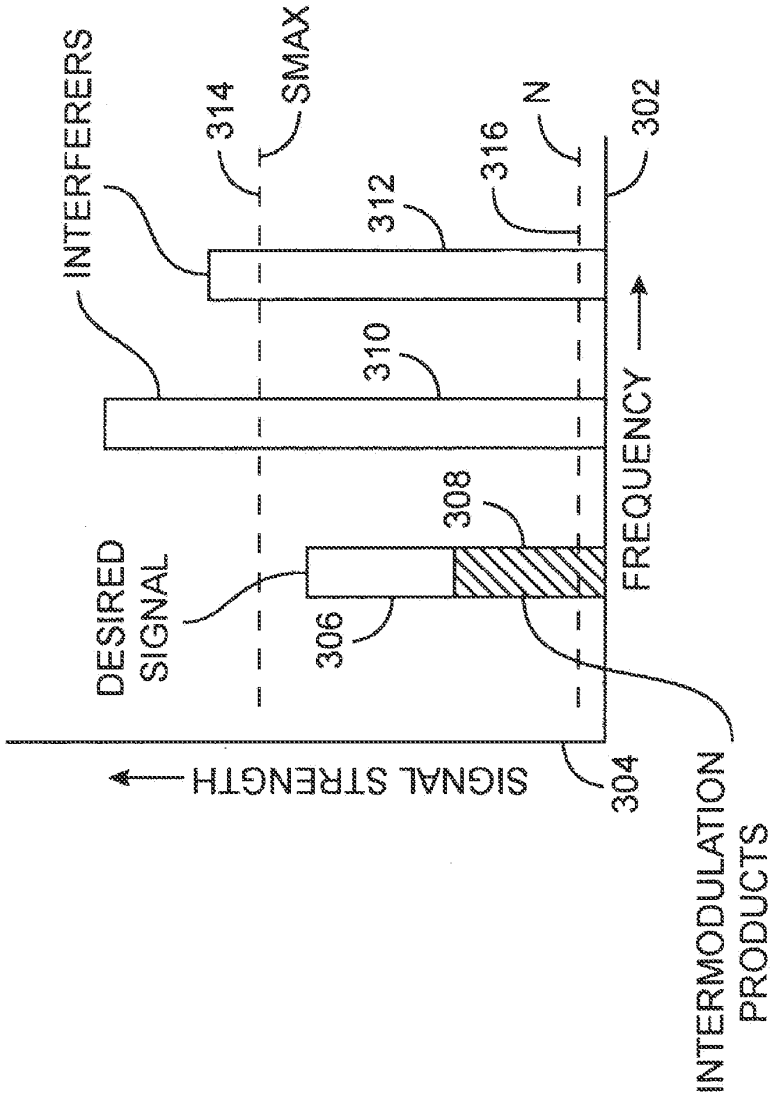

INTERFERERS
314
SMAX
312
316
N
302
310
FREQUENCY
308
DESIRED SIGNAL
306
SIGNAL STRENGTH
304
INTERMODULATION PRODUCTS

FIG. 3

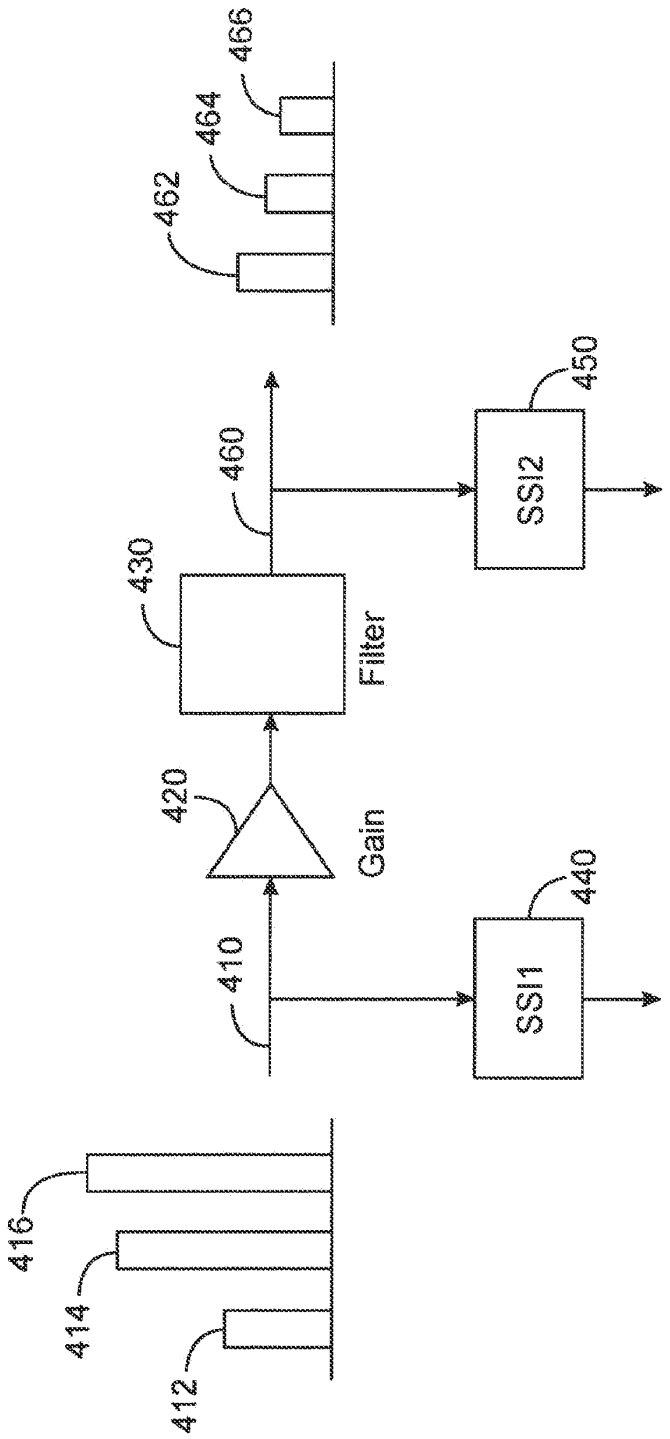

466
464
462
450
SSI2
460
430
Filter
420
Gain
440
SSI1
410
416
414
412

FIG. 4

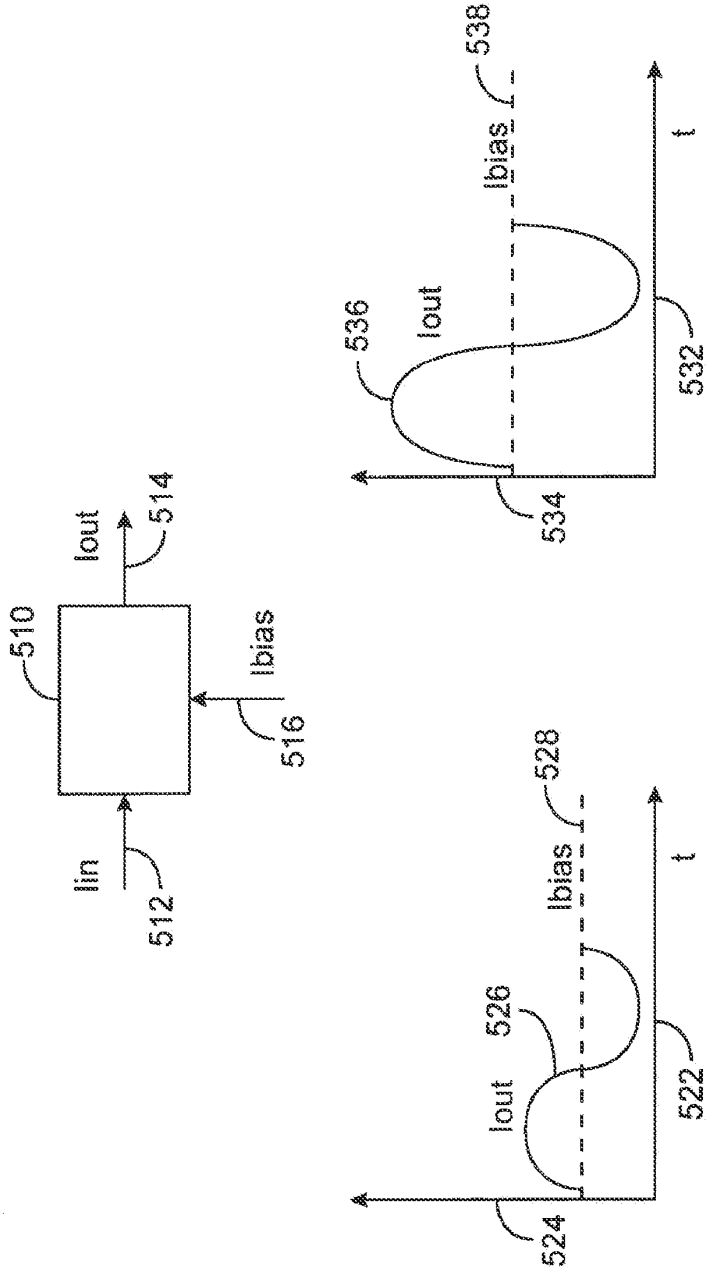

510
Iout
514
Ibias
516
Iin
512
538
Ibias
t
536
Iout
532
534
528
Ibias
t
526
Iout
522
524

FIG. 5

AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Northern District of Illinois/Eastern Division on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
22cv3441	06/30/2022	Northern District of Illinois/Eastern Division

PLAINTIFF	DEFENDANT
Theta IP, LLC	Motorola Mobility LLC, Lenovo (United States) Inc., Lenovo Group Limited

PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 See Attached		
2		
3		
4		
5		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE
Thomas G. Bruton	David Jozwiak	07/05/2022

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

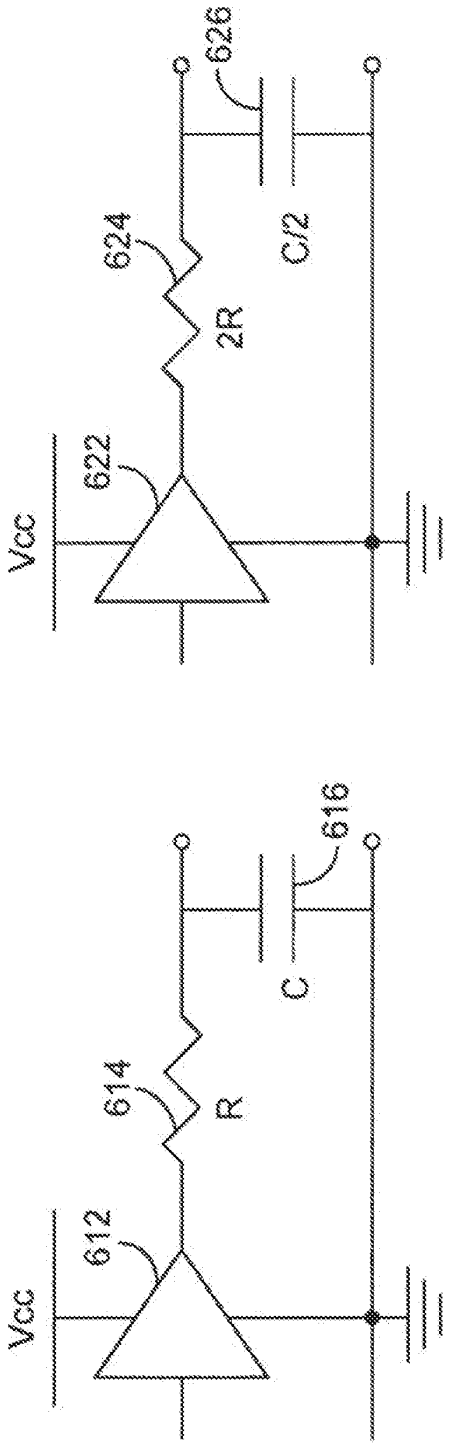
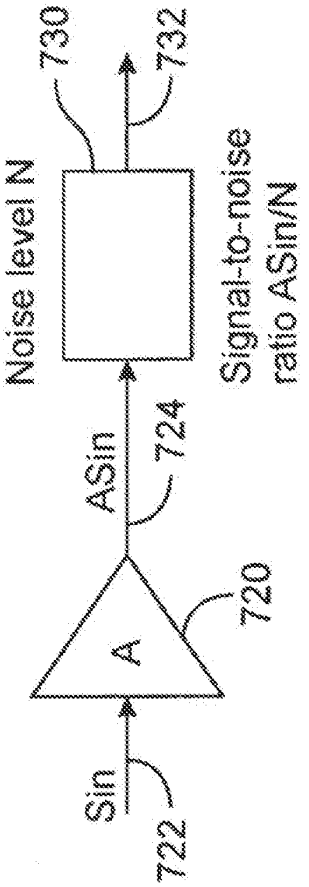


FIG. 6


730
732
Noise level N
Signal-to-noise ratio ASin/N
ASin
724
720
A
Sin
722

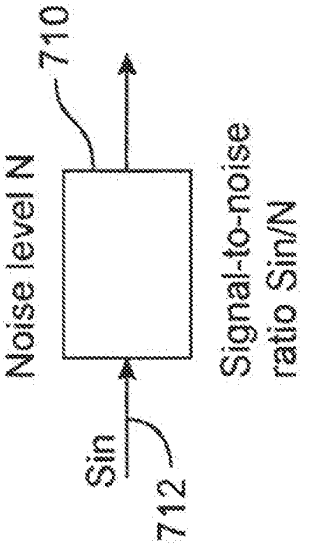

710
Noise level N
Signal-to-noise ratio Sin/N
Sin
712

FIG. 7

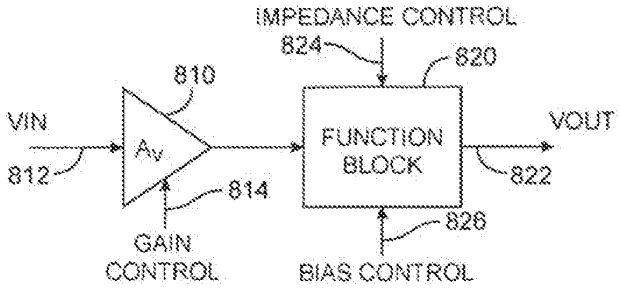


FIG. 8A

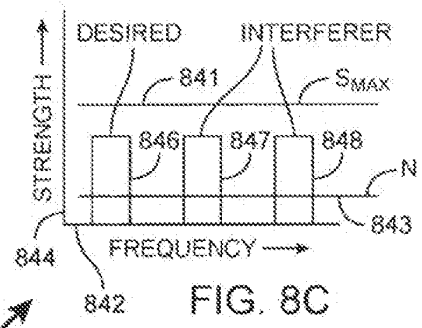


FIG. 8C

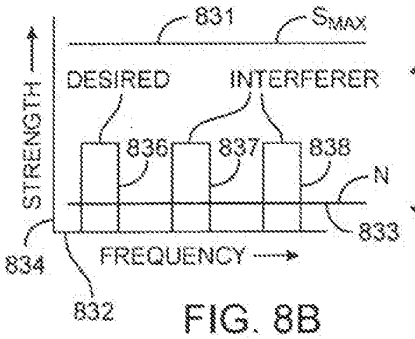


FIG. 8B

DECREASE BIASING

– AND/OR –

INCREASE GAIN AND IMPEDANCES

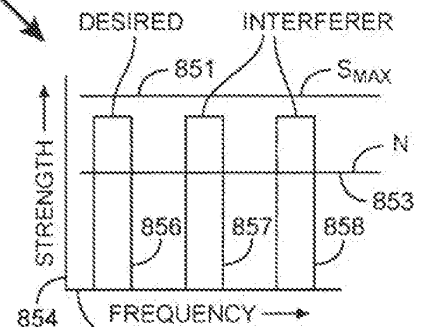


FIG. 8D

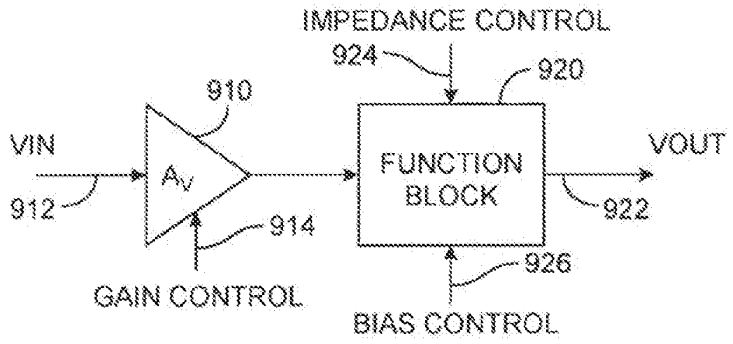


FIG. 9A

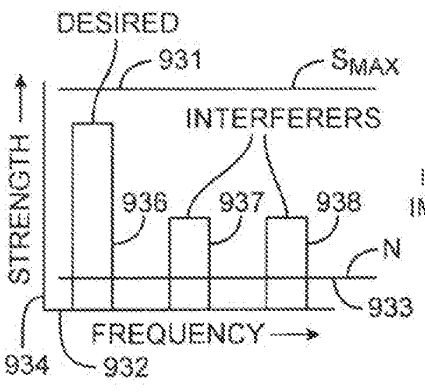


FIG. 9B

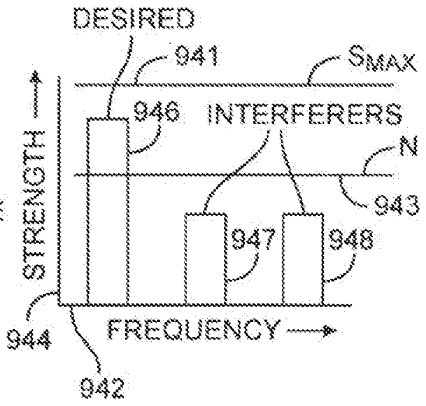


FIG. 9C

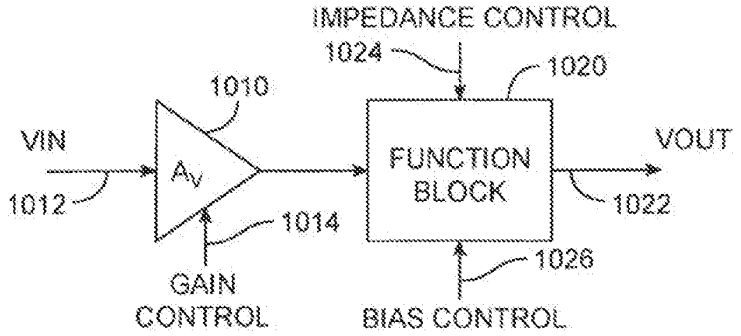


FIG. 10A

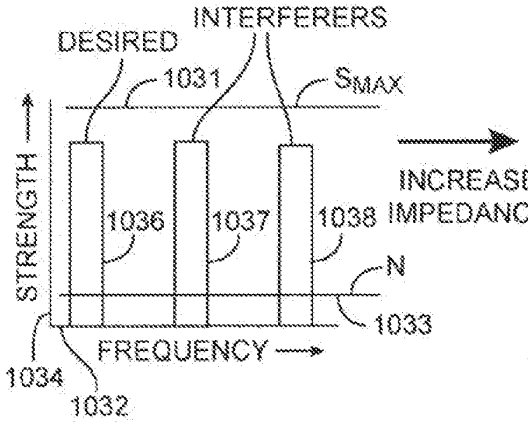


FIG. 10B

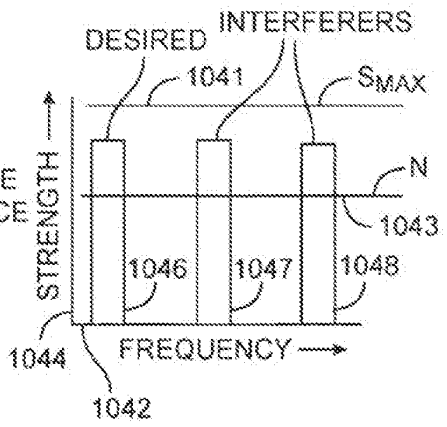


FIG. 10C

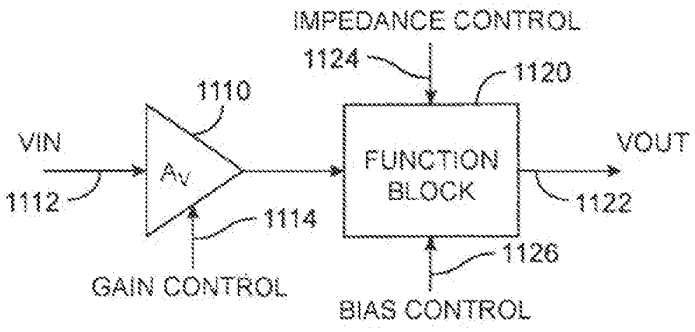


FIG. 11A

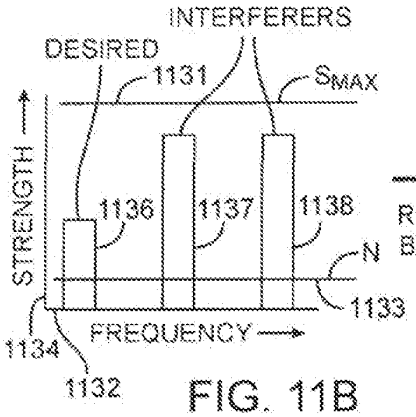


FIG. 11B

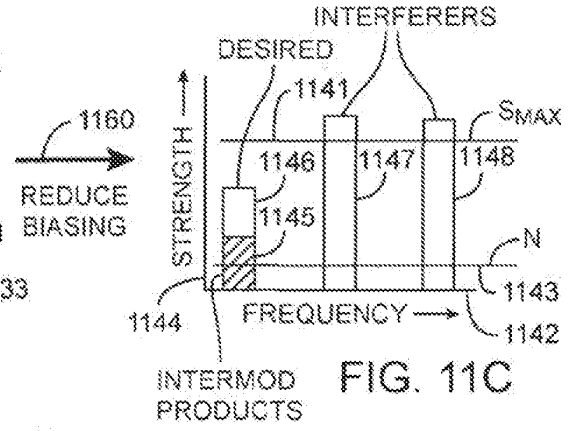


FIG. 11C

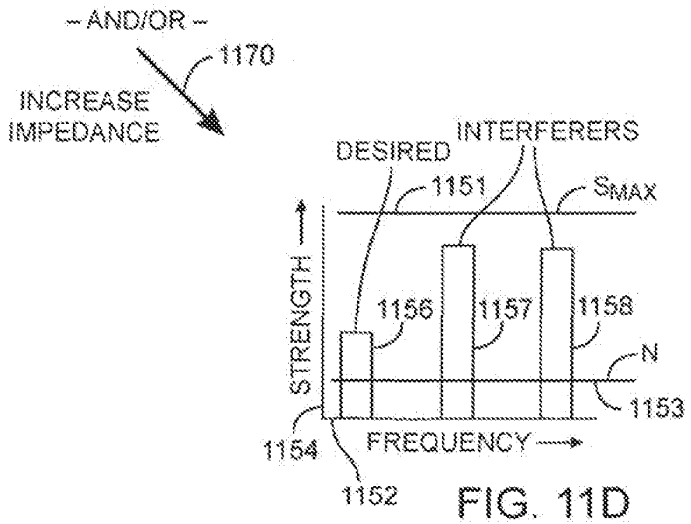


FIG. 11D

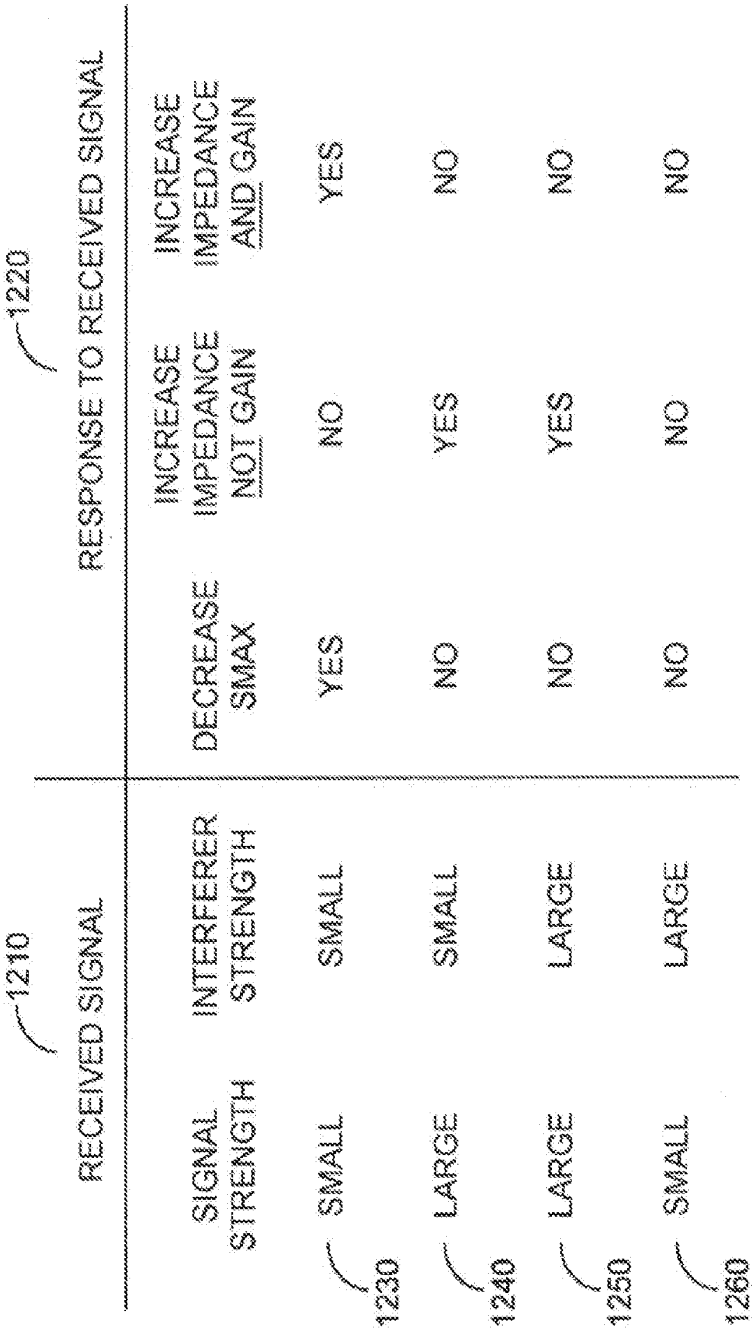

1210
RECEIVED SIGNAL
1220
RESPONSE TO RECEIVED SIGNAL
SIGNAL STRENGTH
INTERFERER STRENGTH
DECREASE SMAX
INCREASE IMPEDANCE NOT GAIN
INCREASE IMPEDANCE AND GAIN
SMALL
SMALL
YES
NO
YES
1230
LARGE
SMALL
NO
YES
NO
1240
LARGE
LARGE
NO
YES
NO
1250
SMALL
LARGE
NO
NO
NO
1260

FIG. 12

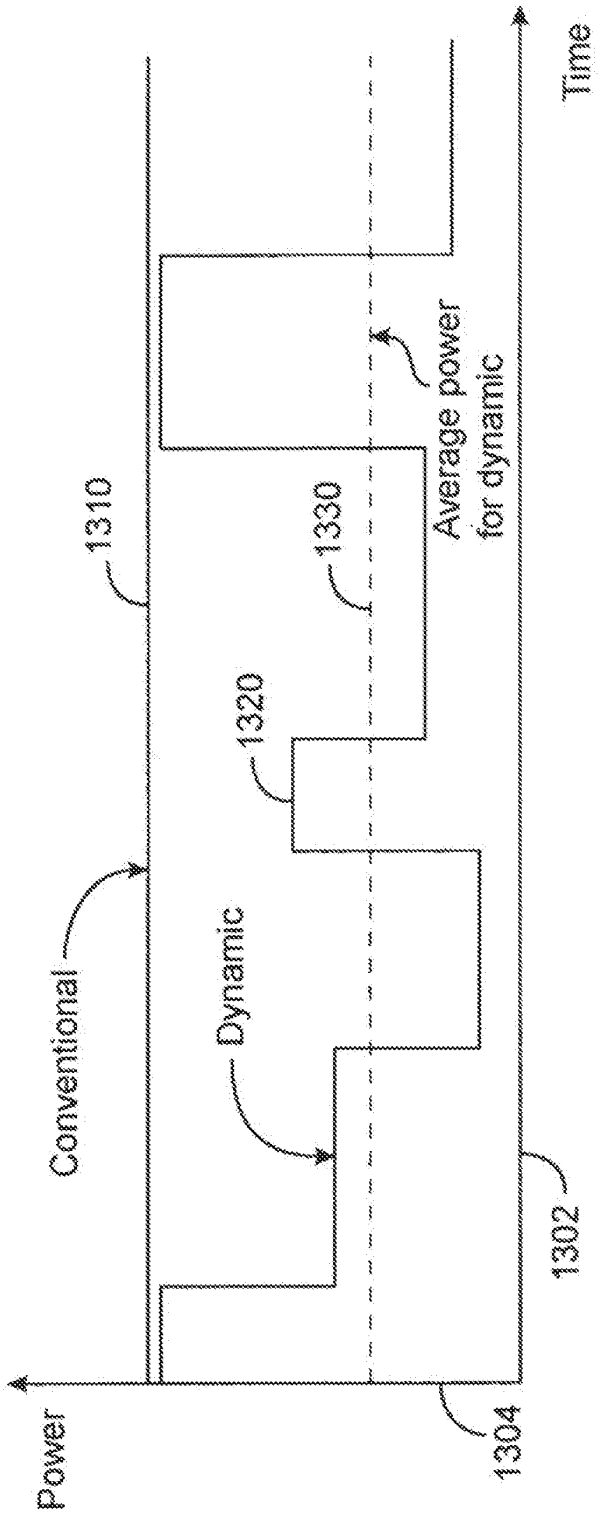

Time
Power
Conventional
Dynamic
1310
1320
1330
1302
1304
Average power
for dynamic

FIG. 13

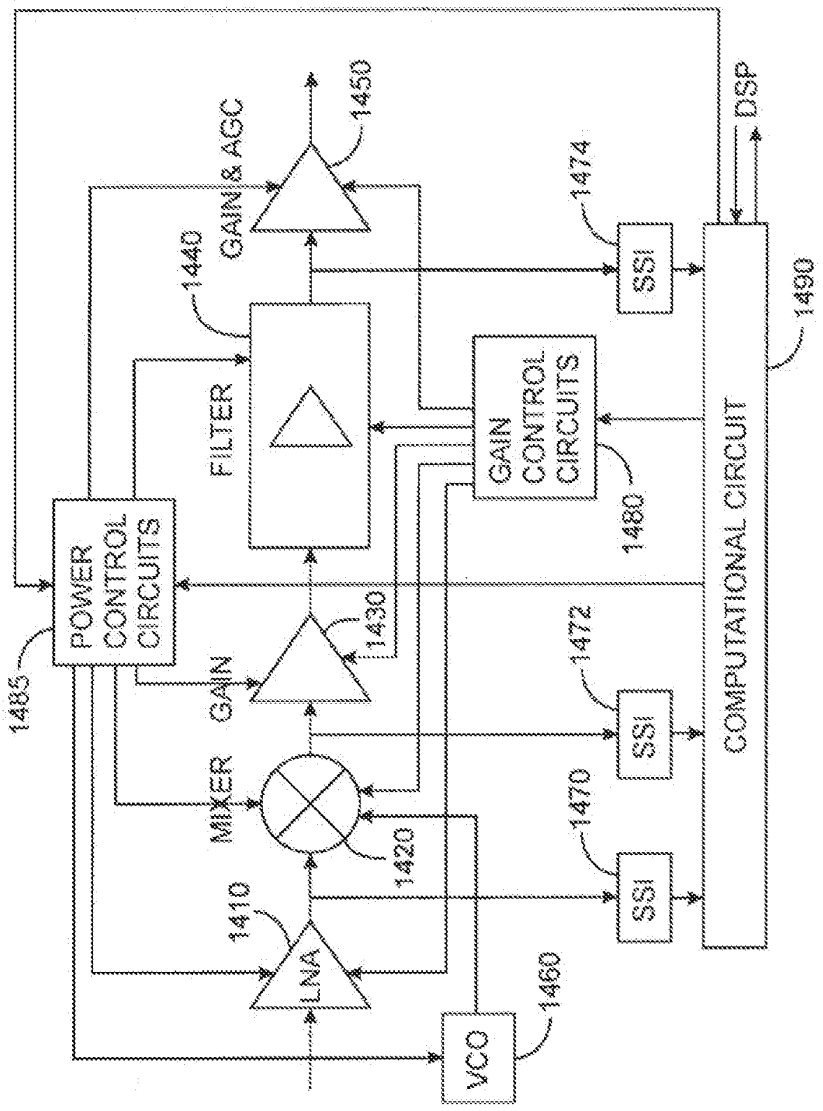

1450
GAIN & AGC
1440
FILTER
1474
SSI
DSP
1490
COMPUTATIONAL CIRCUIT
GAIN CONTROL CIRCUITS
1480
POWER CONTROL CIRCUITS
1485
1430
GAIN
1472
SSI
MIXER
1420
1470
SSI
1410
LNA
VCO
1460

FIG. 14

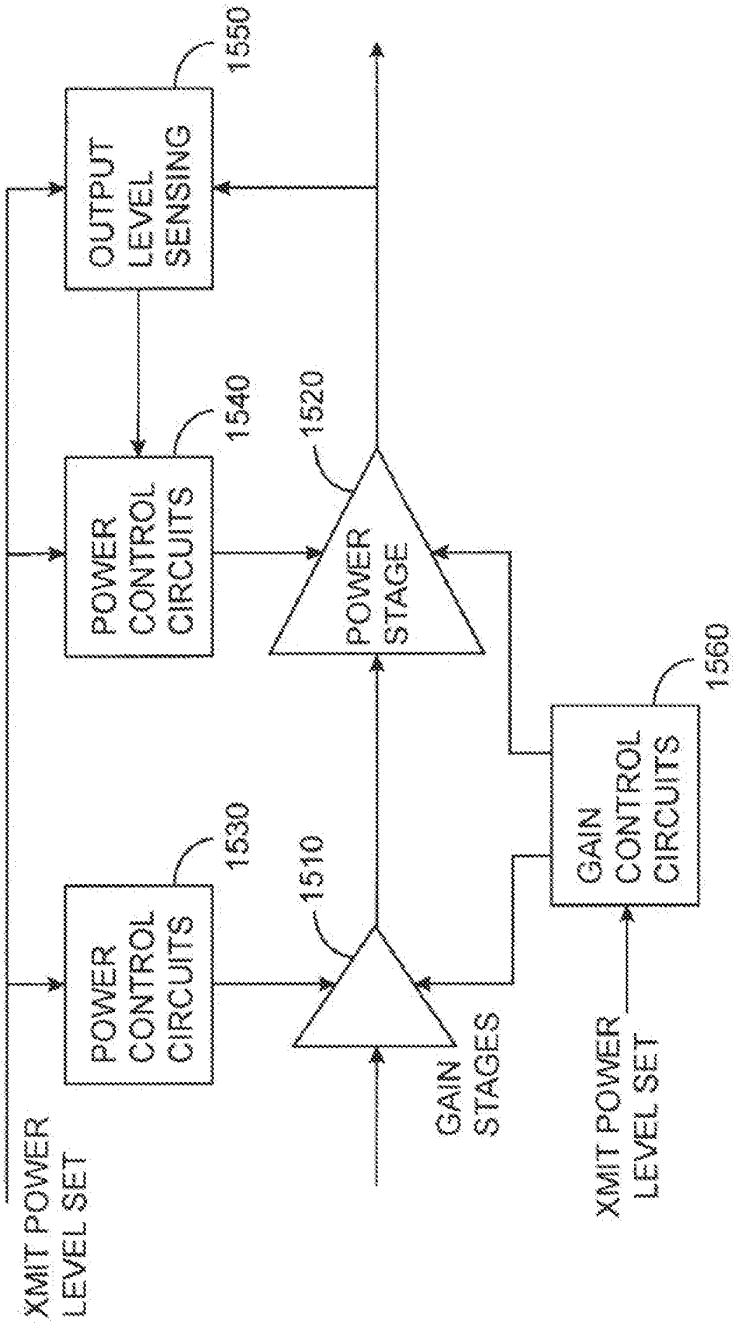

XMIT POWER LEVEL SET
POWER CONTROL CIRCUITS
1530
1510
GAIN STAGES
POWER CONTROL CIRCUITS
1540
1520
POWER STAGE
OUTPUT LEVEL SENSING
1550
GAIN CONTROL CIRCUITS
1560
XMIT POWER LEVEL SET

FIG. 15

Exhibit A

POWER DISSIPATION REDUCTION IN WIRELESS TRANSCEIVERS

CROSS-REFERENCES TO RELATED APPLICATIONS

This application claims the benefit of U.S. provisional application No. 60/451,229, filed Mar. 1, 2003, which is incorporated by reference.

This application is related to U.S. provisional application No. 60/451,230, filed Mar. 1, 2003, which is incorporated by reference.

BACKGROUND

The present invention relates to power dissipation reduction techniques for electronic circuits, for example wireless transceiver integrated circuits.

Wireless networking is quickly becoming ubiquitous, as desktop, notebook, and handheld computers are connected to share Internet access and files. Wireless networking cards compatible with PCMCIA and compact flash form factors are popular for laptops and handhelds respectively, particularly as mobile users connect to the Internet on the road at coffee shops, hotels, and airports.

A downside of this connectivity is a corresponding drain on battery life, especially for these portable devices. The power consumed by a wireless transmitter and receiver reduces the usefulness of a device and sends a user on a hunt for an electrical outlet for recharging.

One reason why this power drain is high is that electronic circuits are typically designed to function properly under worst-case operating conditions. For a wireless transceiver, the worst case condition is when a desired signal reception strength is low, while other transceivers or nearby electronic equipment generate interfering signals and other spurious noise.

But a wireless transceiver does not always operate in these worst-case conditions. For example, a base station, router or access point may be nearby such that the received signal is strong. Also, there may be no interfering signals, or they may be relatively weak. In these situations, receiver circuit currents can be reduced below what is necessary for the worst case condition. If this is done, power dissipation is reduced, and battery life is increased.

Thus, what is needed are circuits and methods that can adapt to a better-than-worst-case condition and reduce circuit currents and therefore power dissipation accordingly.

SUMMARY

Accordingly, embodiments of the present invention provide methods and circuits for reducing power dissipation in wireless transceivers and other electronic circuits and systems. Embodiments of the present invention use bias current reduction, impedance scaling, gain, and other dynamic changes either separately or in combination to reduce power dissipation in response to better-than-worst case conditions. For example, bias currents are reduced in response to a need for reduced signal handling capability, impedances are scaled thus reducing required drive and other bias currents in response to a strong received signal, or gain is varied and impedances are scaled in response to a low received signal in the presence of no or weak interfering signals. Alternately, currents may start low and be increased in response to worse-than-best-case conditions, or they may start at a point in between and vary up or down. These variations may be made to electronic systems generally, and are particularly suited and discussed below in the context of a wireless transceiver that may be used in networking devices, cellular telephones, and other wireless systems.

An exemplary embodiment of the present invention provides a method of receiving a signal using an integrated circuit. The integrated circuit includes a signal path having a low-noise amplifier configured to receive the signal, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer. The method itself includes determining a first signal strength at a first node in the signal path in the integrated circuit and dynamically changing an impedance of a component in the signal path based on the first signal strength.

A further exemplary embodiment of the present invention provides a method of receiving a signal using an integrated circuit. The integrated circuit includes a signal path having a low-noise amplifier configured to receive the signal, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer. The method itself includes determining a first signal strength at a first node in the signal path in the integrated circuit and dynamically changing a bias current in the signal path based on the first signal strength.

Another exemplary embodiment of the present invention provides a method of receiving a signal using an integrated circuit. The integrated circuit includes a signal path having a first circuit and a second circuit having an input coupled to an output of the first circuit. The method itself includes determining a first signal strength at a first node in the signal path in the integrated circuit. The first node is before the first circuit in the signal path. The method further includes dynamically changing a gain of the first circuit based on the first signal strength and dynamically changing an impedance of a component in the second circuit based on the first signal strength.

Still a further exemplary embodiment of the present invention provides a wireless transceiver integrated circuit including a receiver having a signal path, the signal path including a low-noise amplifier, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer, as well as a first signal strength indicator circuit coupled to the signal path and configured to determine a first signal strength. An impedance in the signal path is configured to be dynamically adjusted in response to the first signal strength.

Yet a further exemplary embodiment of the present invention provides a wireless transceiver integrated circuit. This integrated circuit includes a receiver comprising a signal path, the signal path having a low-noise amplifier, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer, as well as a first signal strength indicator circuit coupled to the signal path, and configured to determine a first signal strength. A bias current in the signal path is configured to be dynamically adjusted in response to the first signal strength.

Another exemplary embodiment of the present invention provides a wireless transceiver integrated circuit. This circuit includes a receiver comprising a signal path, the signal path having a first circuit; and a second circuit having an input coupled to an output of the first circuit; as well as a first signal strength indicator circuit coupled to the signal path, and configured to determine a first signal strength. A gain of the first circuit is configured to be dynamically adjusted in

response to the first signal strength, and an impedance in the second circuit is configured to be dynamically adjusted in response to the first signal strength.

A better understanding of the nature and advantages of the present invention may be gained with reference to the following detailed description and the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram of a wireless transceiver that may benefit by incorporation of embodiments of the present invention;

FIGS. **2A** and **2B** illustrate examples of desired and interfering signals and noise that may be received by a circuit in a wireless receiver;

FIG. **3** illustrates what can occur as a maximum signal handling capability is reduced in the worst-case signal condition;

FIG. **4** illustrates a portion of a receiver consistent with an embodiment of the present invention;

FIG. **5** illustrates the relationship between a required bias current and a given output signal for a representative circuit;

FIG. **6** is an example of how a circuit's impedances may be scaled to reduce drive currents, and depending on the circuit configuration used, to reduce associated bias currents as well;

FIG. **7** illustrates how gain may be inserted in a signal path to improve a circuit's signal to noise ratio;

FIGS. **8A–8D** illustrate some of the possible power saving techniques that may be used when received desired and interferer signals are all at a low power level;

FIGS. **9A–9C** illustrate one of the possible power saving techniques that may be used when a received desired signal is strong while all interfering signals are at a low power level;

FIGS. **10A–10C** illustrate one of the possible power saving techniques that may be used when received desired and interferer signals are all at a high power level;

FIGS. **11A–11D** illustrate one of the possible power saving techniques that may be used when a received desired signal is weak while one or more interfering signals are strong;

FIG. **12** is a summary illustrating four different input conditions and some of the appropriate power-saving changes that may be made in response to those conditions;

FIG. **13** shows how power may be saved as a function of time by employing one or more of the power saving methods consistent with embodiments of the present invention;

FIG. **14** is a block diagram of a portion of a receiver consistent with an embodiment of the present invention; and

FIG. **15** is a block diagram of a portion of a transmitter consistent with an embodiment of the present invention.

DESCRIPTION OF EXEMPLARY EMBODIMENTS

FIG. **1** is a block diagram of a wireless transceiver that may benefit by incorporation of embodiments of the present invention. This wireless transceiver may be designed to send and receive signals consistent with the IEEE 802.11a, 802.11b, 802.11 g, or other signaling standard or combination of standards. This figure, as with all the included figures, is shown for illustrative purposes only and does not to limit either the possible embodiments of the present invention or the claims.

There are three main portions of this transceiver circuit, a receiver, transmitter, and synthesizer. This transceiver may be completely or partially integrated on a semiconductor chip, or it may be integrated onto multiple integrated circuits. In a specific embodiment, the circuitry bounded by dashed line **100** is integrated on a single chip coupled to one or more external components or circuits. The integrated circuit or circuits forming this wireless transceiver may incorporate various integrated circuit devices such as a bipolar, CMOS, or BiCMOS devices made using a silicon, silicon-germanium (SiGe), gallium arsenide or other III-V process, or other manufacturing process. Embodiments of the present invention may also be applicable to circuits manufactured using nanotechnology processing.

The receiver includes a signal path formed by low-noise amplifier **102**, I and Q mixers **104** and **106**, low pass filters **108** and **110**, and baseband amplifiers **114** and **116**. Other circuitry in the receiver includes received strength indicator **122**, automatic gain control circuit **166**, baseband gain control circuit **120**, tuning circuit **112**, and offset cancellation circuit **118**.

The transmitter includes input up-converter mixers **124** and **126**, summing node **176**, which may be conceptual rather than an actual circuit, transmit variable gain amplifier **128**, and power amplifier **130**.

The synthesizer includes a voltage-controlled oscillator **148**, which drives I and Q buffers **154** and **152**, prescaler **156**, reference clock buffer **142** and divider **158**, phase-frequency detector **160**, charge pump **162**, and loop filter **146**, which in a specific embodiment is formed by external components.

Signals are received on an antenna, not shown, and typically pass through an RF switch and bandpass filter before being received by the low-noise amplifier **102** on line **101**. The low noise amplifier gains the received signal and provides it to quadrature mixers **104** and **106**. I and Q mixers **104** and **106** down-convert the received signal to baseband by multiplying them with quadrature versions of the oscillator signal provided by buffers **152** and **154**. This down conversion also produces a high frequency component at a frequency that is equal to the sum of the frequencies of the received signal and the VCO. This unwanted signal is filtered by low pass filters **108** and **110**, which in turn drive baseband amplifiers **114** and **116**. The outputs of baseband amplifiers **114** and **116** are typically converted to digital signals by analog-to-digital converters at the front end of a digital signal processing block.

In the transmit mode, I and Q versions of the signal to be transmitted are provided on lines **121** and **123** to up-convert mixers **124** and **126**. These up-convert mixers multiply the I and Q portions of the transmit signal by quadrature versions of the VCO signal provided by buffers **152** and **154**. The outputs of the up-convert mixers **124** and **126** are summed, and amplified by transmit VGA **128**, which in turn drives power amplifier **130**. The output of power amplifier **130** is typically filtered, and passes through the RF switch to the antenna for transmission.

A reference clock is received and buffered by the reference buffer **142**. The VCO generates quadrature oscillatory signals that are divided by prescaler **156**. The reference clock is typically generated by a crystal or other stable periodic clock source. The phase-frequency detector **116** compares the phase or frequency (depending on whether the synthesizer is tracking or acquiring the correct frequency) of the divided VCO signal and the reference clock, or a divided version of the reference clock, and generates an error signal, which drives the charge pump **162**. The output signal of the

charge pump **162** is filtered by the loop filter **146**, which is commonly a lead-lag filter, and which provides a tuning or correction signal to the VCO **148**.

Embodiments of the present invention may be used to reduce the power dissipation of one or more of these included circuits. For example, the power dissipation in the low-noise amplifier **102**, down-convert mixers **104** and **106**, low pass filters **108** and **110**, or baseband amplifiers **114** and **116** may be optimized. Also, power dissipation in up-convert mixers **124** **126**, variable gain amplifier **128**, and power amplifier **130** may also be optimized. Similarly, VCO **148** and prescaler **156** currents may be adjusted. Embodiments of the present invention may also be applied in other circuits which may be included in other integrated circuit receivers, transmitters, transceivers, or other electronic circuits or systems.

When a receiver is actively receiving a desired signal, each block in the signal path has at its input the desired signal as well as noise and possibly interfering signals. The desired signal is the useful, information-carrying portion of a received signal. The noise may be thermal, shot, or other noise generated on the integrated circuit, in addition to received noise generated by sources external to the chip. The noise at the input of a block may be referred to as the equivalent input noise. The interfering signal or signals, or interferers, may be generated by similar transceivers, or other electrical equipment, circuits, or systems.

FIGS. **2**A and **2**B illustrate examples of desired signals, interferers, and noise that may be received by one of the various circuits in a wireless receiver. In each of these figures, the signal strength is plotted along a Y-axis **204** or **254** as a function of frequency along an X-axis **202** or **252**. In the example of FIG. **2**A, a received desired signal **206** is large in comparison to interfering signals **208** and **210**. In these examples, two interfering signals are shown for illustrative purposes, though there may be no such signals, one such signal, or more than two such signals in the frequency range of interest. Also, while for these examples the interferers are shown as being at a higher frequency than the desired signal, there may be one or more interferers at higher or lower frequencies as the desired signal. In this specific example, the acceptable noise floor **214** is relatively high, while maximum signal handling capability Smax **212** (that is the maximum signal power that can be handled with an acceptably low distortion) needs only to be high enough to accommodate the desired signal. For this specific example, the circuit receiving this input spectrum only requires a relatively small dynamic range for proper operation, that is the range between Smax **212** and the noise floor **214** is relatively small.

Conversely, in the example shown in FIG. **2**B, the desired signal **256** is relatively weak compared to the large interferers **258** and **260**. In this example, the noise floor **264** should be relatively low so as to prevent an unacceptable level of error in the recovery the desired signal **256**. The maximum signal handling capability Smax **262** should be relatively high to accommodate the large interferers in order to avoid the creation of intermodulation products as described below. Accordingly, in this specific example, the circuit receiving this input spectrum should have a large dynamic range, particularly in comparison to the example of FIG. **2**A.

It should be noted that the noise level or noise floors shown in these and the other included figures is the noise density integrated over the bandwidth of interest. For simplicity and comparison, this level is shown as a horizontal line, and is not meant to imply noise density.

Often in wireless receivers, a circuit at different times will receive an input spectrum similar to those shown in FIGS. **2**A and **2**B. The input spectrum of FIG. **2**B is generally considered the worst-case input signal, and typical design methodology involves designing a receiver for this condition, specifically the weakest desired signal accompanied by largest interference level. Circuit impedances and currents are set such that the noise floor **264** is sufficiently low for an acceptable bit-error rate, while bias currents are set sufficiently high for the required Smax **262**.

Conversely, the input spectrum in FIG. **2**A is that of the best-case input signal, specifically, a robust desired signal accompanied by no or low-level interferers. In this case, the noise floor **214** may be allowed to rise, while the maximum signal handling capability Smax **212** may be reduced. When this is done, the receiver circuit may save significant power. For example, the circuit's impedances may be increased, thus reducing required drive currents. Similarly, bias currents may be lowered, thus reducing the maximum signal in handling capability.

The minimum power dissipation for a circuit is proportional to the required maximum signal-to-noise ratio, which is the ratio between Smax **212** or **262** and N **214** and **264**. Thus, a circuit receiving an input similar to the one shown in FIG. **2**A can dissipate less power than one receiving the input as shown in FIG. **2**B, while still achieving an acceptable bit-error rate.

FIG. **3** illustrates what can occur when the maximum signal handling capability Smax **314** is reduced in the worst-case condition, that is when a weak desired signal **306** is accompanied by large interferers **310** and **312**. Again, signal strength is plotted along a Y-axis **304** as a function of frequency along X-axis **302**. In this specific example, Smax **314** is reduced below the peak levels of the interferers **310** and **312**. Since Smax is low, the circuit cannot handle the interferers linearly. The resulting nonlinearities lead to a mixing of the interferers and the creation of intermodulation products **308** (for example, a third-order intermodulation distortion, IM3), one of which in this example occurs at the same frequency as the desired signal **306**. As can be seen, if the intermodulation products **308** become excessive, the received signal bit error rate may become excessive, and the desired signal **306** may be lost. Accordingly, while Smax may be lowered even under some unfavorable conditions in order to reduce power, care should be taken to avoid corruption of the received desired signal.

FIG. **4** illustrates a portion of a receiver consistent with an embodiment of the present invention. Included is a filter **430**. An optional gain element **420** is placed in front of the filter **430** in order to increase signal levels. Signal strength indicator circuits **440** and **450** are connected to input line **410** and output line **460**. In this specific example, the input signal spectrum on line **410** is shown as desired signal **412** and interferers **414** and **416**. The signal spectrum at the output line **460** is shown as desired signal **462** and interferers **464** and **466**. The signal strength indicators **440** and **450** do not provide information as to the relative sizes of the desired and interfering signals. Rather, a cumulative signal level is provided at their outputs. For example, the first signal strength indicator **440** outputs a level corresponding to the sum of desired signal **412** and interfering signals **414** and **416**, while the second signal strength indicator **450** provides a signal level corresponding to the sum of desired signal **462** and interfering signals **464** and **466**. In this specific example, the gain of the gain and filter circuit combinations is shown as approximately one, while the interfering signals **414** and **416** signal levels are reduced.

A comparison of the signal levels provided by the signal strength indicators **440** and **450** indicates that much of the combined received signal on line **410** has been filtered. Accordingly, it may be deduced that large interfering signals present at the input are being filtered by the filter **430**. From this information, as will be shown in greater detail below, the bias, impedance, and gain of the gain stage **420** and filter **430** combination may be optimized to reduce power dissipation.

There are several real world situations where the received signal is better than the worst-case condition such that power can be saved. For example, large interferers may be present only part of the time, that is, on a temporary or transient basis. The interfering equipment may be some distance from the transceiver, or it may be operating in the low power mode. Also, the desired signal may be very strong as compared to the noise and interferers, for example a hub, router, or access point may be nearby.

Some transceivers consistent with embodiments of the present invention are designed to work with more than one data transfer specification or standard. In this case, when a transceiver is operating in a mode having a lower data rate, the power saving techniques described here may be employed.

FIG. **5** illustrates the relationship between a required biased current **516** for a given output signal **514** for a representative circuit **510**. If the output signal current level is relatively low, such as the output current shown as **526**, the corresponding bias current **528** may be low. Conversely, if the output signal current level is larger as with the example **536**, the corresponding bias current level **538** should also be high. Accordingly, if a bias current is initially set high to handle large a large input signal, for example a large interferer, this current may be reduced if the input signal is smaller.

There are many ways by which these bias currents can be reduced. For example, the current may be generated by placing a voltage across a resistor by applying a bias voltage to the base of a device whose emitter is connected to ground through a resistance. In this case, the resistor may be increased by opening switches across portions of the resistance, or lowering the bias voltage applied at the base. Several ways in which this may be done will be readily understood by one skilled in the art.

FIG. **6** is an example of how a circuit's impedances may be scaled to reduce drive currents, and, depending on the circuit configuration used, associated bias currents as well. A driver **612** has a load R **614** and C **616**. The frequency response of this circuit is the same as that seen by driver **622**, which drives an impedance of 2R **624** and C/2 **626**. But the impedance of the load seen by driver **622** is double that seen by **612**, thus the output current required by the driver **622** is reduced by one-half.

As an example, the output stage of each of these drivers may be a Class A emitter follower formed by an emitter follower connected to a current source. When the outputs are driven high, the emitter of driver **622** need supply only one-half the drive current as driver **612**. In this way, an impedance can be scaled in order to decrease a circuit's required drive current.

Also, the discharge current for driver **622** is only one half that of driver **612** for a given negative-going slew rate. Thus, the current source of **622** may be reduced by the same factor of one-half as compared to driver **612**. In this example, the bias current, that is the current in the pull-down current source can be reduced. Many other examples where drive currents and possibly bias currents may be reduced will be appreciated by one skilled in the art.

FIG. **7** illustrates another degree of freedom that made be employed to reduce current levels in a transceiver. Specifically, a gain element **720** may be inserted in front of a circuit block **730** in order to improve the combined circuit's signal-to-noise ratio by a factor equal to the gain of the inserted gain block. This is particularly useful when large interferers are absent and the desired received signal is moderate or low. Specifically, gain is added to the signal while impedances are increased, which raise the noise floor. In this way, a given signal-to-noise ratio may be maintained while the power is decreased.

The gain of such an element may be varied by increasing a current in a differential pair or increasing a load resistance using switches. Many other examples where the gain of this element may be varied will be appreciated by one skilled in the art.

These variables, or degrees of freedom, specifically reducing bias currents, increasing impedances, and increasing gain may be used as in the following examples.

FIG. **8A** is a block diagram of a functional block **820** and optional gain element **810** in accordance with an embodiment of the present invention. Functional block **820**, like the functional blocks in the following diagrams, may be a filter, mixer, amplifier, or other circuit or circuits in a wireless transceiver or other electronic circuits or system. An input signal is received on line **812** by the optional gain element **814**. When the optional gain block **810** is not used, the input signal may be received directly by the function block **820**. The gain of the optional gain element **812** is controlled by a gain control signal on line **814**. The functional block receives an output signal from the optional gain element **810** and provides an output VOUT on line **822**. The lines in this and the other included figures may be one or more lines, depending on whether single-ended, differential, or other type of signaling is employed.

One or more impedances are under control of signals on impedance control lines **824**. Similarly, one or more bias currents in the function block are under control of one or more signals on bias control lines **826**. These various control lines may be logic signals, analog signals, voltage or currents lines, or other signal or bias lines. In other embodiments of the present invention, the gain control element **810** may be included in the function block **820**. Also, various embodiments may not incorporate either or both the impedance control and bias control.

FIG. **8B** is an example input that may be present on line VIN **812**. In this example, a desired signal **836** is relatively weak, as are interfering signals **837** and **838**. The initial bias and circuit configuration is such that the noise floor **833** and maximum signal handling capability Smax **831** are adjusted for worst case conditions. The circuit of FIG. **8A**, as with all the circuits described here, receives noise at its input which may be referred to as input equivalent noise or input referred noise. Additionally, the circuit of FIG. **8A** generates noise which is added to the input referred noise. Depending on the gain characteristics of the circuitry, the output noise at various frequencies may be greater than, equal to, or less than the input referred noise. For simplicity, the noise floor and maximum signal handling capability Smax, in this and the other figures, are shown as straight lines, though the noise and Smax are typically curved as a function of frequency.

That the input spectrum is as shown in FIG. **8B** can be determined, for example, by low signal strength indications on line VIN **812** and VOUT **822**. That is, a low level signal strength indication on line VIN **812** indicates that no portion of the input signal is particularly large.

For this exemplary input, there are at least two methods by which the power dissipation for this circuitry may be reduced. Depending on the exact circuits and structures used, one of these methods may be preferred.

In FIG. **8**C, the bias current is decreased, thereby lowering the maximum signal handling capability **841** as compared to **831**, closer to the desired and interfering signal levels. Again, the bias currents in the function block **820** may be reduced by switching impedances that appear across a voltage thereby changing a resulting bias current, by reducing a voltage at the gate of a MOS or base of a bipolar transistor, or by other methods.

In FIG. **8**D, a second method of reducing power dissipation in the function block **820** is employed. Specifically, Smax **851** is held constant as compared Smax **831**. The desired and interfering signals are amplified such that they are closer to the available signaling handling capability **851**. Also, the noise floor **853** is raised as compared to noise floor **833** in FIG. **8**B. Specifically, the noise contributed by the function block **820** is increased, such that the noise at its output is increased to noise floor **853**. This is done by increasing one or more impedance in function block **810**, such that drive currents inside that block are reduced. Depending on the exact configuration, this may also allow some biasing currents to be reduced, while maintaining the maximum signal handling capability **851** at a sufficient level. Alternately, these two methods of reducing power dissipation in function block **820** may be done in combination.

The included examples are explained for the exemplary situation where biasing and other parameters are set for worst-case conditions, and then changed to save power when it is discovered that the conditions are better-than-worst case. Alternately, the bias currents and other parameters may be set for maximum power savings, or an intermediate point, and the power can be adjusted from there.

FIG. **9**A illustrates a block diagram including an optional gain element **910** and function block **920**. Again, an input signal is received on line **912** by optional gain element **910** which in turn drives function block **920**. The function block provides an output VOUT on line **922**, and receives impedance and bias control signals on lines **924** and **926**.

FIG. **9**B shows the spectrum for what may be considered a best-case received signal. Specifically, the desired signal **936** is strong, while the interfering signals **937** and **938** are relatively weak. This may be determined, for example, by detecting a large signal level at the input line VIN **812** and a large signal level after a filter, since these readings would indicate that a large signal is received, but that it is at the desired signal frequency.

The maximum signaling capability **931** and noise floor **933** are shown as being set for the worst case conditions. In this case, the noise floor **933** is lower than the maximum allowed for proper signal reception. Accordingly, one or more impedance in the function block **920** may be increased, such that the noise floor **943** rises as shown in FIG. **9**C. In this way one or more the driving currents in the function block **920** may be reduced. Similarly, since the drive current is reduced, one or more bias current may also be reduced, depending on the exact circuit configuration.

FIG. **10**A illustrates a block diagram showing an optional gain element **1010** driving a function block **1020**. An input signal is received by the gain element **1010** on line **1012**, and an output is provided by function block **1020** on line VOUT **1022**. One or more gain control signals present on lines **1014** control the gain of gain control element **1010**, while one or more impedance and bias control signals are received by the function block **1020** on line to **1024** and **1026**.

FIG. **10**B illustrates a received signal that may be received on line VIN **1012**. In this example, the desired signal **1036** and interferers **1037** and **1038** are each relatively large. This may be determined, for example, by detecting a large signal level at the input line VIN **812** and a smaller signal level after a filter, since these readings would indicate that a large signal is received, but that interferers are being reduced.

As before, in this example, the noise floor **1033** and maximum signal handling capability **1031** are initially set for the worst case conditions. Since the desired signal is relatively large in this case, the noise floor may be allowed to rise, a shown by noise floor **1043** in FIG. **10**C. Since the desired signal **1046** and interferers **1047** are large, the maximum signal handling capability Smax **1041** remains constant. Again, the noise floor is increased by increasing impedances in the function block **1020**. This reduces the required drive current, and may also allow for a reduction in bias currents.

FIG. **11**A illustrates a block diagram including an optional gain element **1110** and function block **1120** in accordance with an embodiment of the present convention. An input signal is received on line **1112** by the optional gain control element **1110**, while an output signal is provided by the function block **1120** on line VOUT **1122**. Gain, impedance, and bias control signals are received on lines **1114**, **1124**, and **1126**.

FIG. **11**B is an exemplary input signal that may be received by the gain control element **1110** on line VIN **1112**. In this specific example, the desired signal **1136** is relatively low or weak while the interfering signals **1137** and **1138** are large. This may be determined, for example, by detecting a large signal level at the input line VIN **812** and a much smaller signal level after a filter, since these readings would indicate that a large signal is received and that large interferers are being reduced such that the resulting signal, the desired signal, is relatively weak.

Again, the maximum signal handling capability **1131** and noise floor **1133** are initially set for worst case conditions. If the desired signal is sufficiently low, while the interferers are sufficiently high, power savings may not be achievable over the worst case settings, since this is in fact the worst case condition. But, if the desired signal is somewhat larger than the worst case condition, then power may be saved in at least two different ways.

For example, FIG. **11**C shows the maximum signal handling capability **1141** being lowered. In this case, the interfering signals **1147** in **1148** began to clip and distort, thereby creating intermodulation products **1145**, which distort the desired signal **1146**. So long as care is taken to not corrupt the desired signal **1146** beyond an acceptable limit, typically measured by a bit-error rate, power may be reduced in this way.

Similarly, in FIG. **11**D, the noise floor **1153** is raised somewhat, thereby saving power. Again, this may be done so long as the noise floor is not sufficiently high that the system bit-error rate becomes unacceptable.

FIG. **12** is a summary of the above four examples. The received signal strengths are shown in column **1210**, while appropriate power saving responses are listed in column **1220**. Specifically, in row **1230**, the desired signal and interferer signal strengths are both weak or small. In this case, proper responses include decreasing Smax, or increasing one or more circuit impedances while increasing the circuit gain. Depending on the exact circuit configuration, one of these options may be preferred over the other. Alternately, they may be done in combination, or done in combination with other power saving techniques. Also, in

some specific embodiments, when both desired signal and interferer signal strengths are small, the gain may need to be increased while the impedance is maintained or not increased in order to keep the noise floor low.

In row **1240**, the desired signal strength is strong or large, while the interfering signals are small. In this case, an appropriate response is to increase one or more of the circuit impedances. Again, depending on the exact circuit in question, one or more of the bias currents may also be reduced.

In row **1250**, both the desired signals and interfering signal strengths are large. Again, in this case an appropriate response is to increase one or more of the circuit impedances.

In row **1260**, the received desired signal strength is weak or small, while the interfering signals are large. Since this is the worst case situation for which the circuit is designed, substantial power savings are difficult to achieve. However, again, if the received signal is above a minimum level necessary for proper operation, some distortion of the interferers or raising of the noise floor may be acceptable.

It should be noted that not all possible signal conditions are listed here. For example, either the signal or interferer may be of a relatively medium strength, or the interferer may be absent. Also, these terms are for exemplary purposes and are not meant to convey specific signal conditions, but rather are only qualitative. The proper response to a specific condition depends on the embodiment of the present invention, the particular circuit topology, the requirements of the signaling standard used, as well as other constraints.

FIG. **13** is an example shown how power may be saved as a function of time by employing one or more of these methods consistent with embodiments of the present invention. Power is plotted along a Y-axis **1304** as a function of time along X-axis **1302**. Conventional worst case design would fix power dissipation at line **1310**. As can be seen, dynamic power dissipation **1320** under the control of variable gains, impedances, biasing, or combination thereof, allows for a lower average power **1330** as compared to the power dissipated **1310** by the conventional design.

FIG. **14** is a block diagram of a portion of a receiver consistent with an embodiment of the present invention. Included are low-noise amplifier **1410**, mixer **1420**, gain stage **1430**, filter **1440**, AGC amplifier **1450**, and VCO **1460**. Signal strength detection is done at the output of the low-noise amplifier by signal strength indicator **1470**, at the output of the mixer by signal strength indicator **1472**, and at the output of the filter by signal strength indicator **1474**. The outputs of the signal strength indicator circuits are received by the computational circuit **1470**, which in turn controls gain and power control circuits **1480** and **1485**. Power and gain control circuits **1480** and **1485** control the gain, biasing, and impedance levels of the circuits in the receiver signal path. Also, the gain and power control circuits may control the same parameters in the VCO **1460**. This figure is greatly simplified for purposes of explanation. For example, the quadrature nature of the mixers and following circuits are not shown. Also, power-down and start-up circuits are not included.

The current level in the low-noise amplifier determines a multitude of parameters including voltage gain, linearity, input impedance matching, and noise figure. When conditions are better than worst-case, some of these parameters may be relaxed while maintaining an acceptable bit-error rate, thus saving power.

The bias current in the mixers effect that block's noise figure and linearity. Care is taken in reducing power in this block so as not to increase nonlinearities, particularly the third-order nonlinearity as measured by IP3, the third-order intercept point, beyond an acceptable limit.

A key parameter of the VCO is phase noise, an increase in which increases the sidebands on either side of the oscillation signal. During transmission, the phase noise should be kept low to avoid interference with adjacent channels and for preserving modulation information.

During reception however, if the conditions are better than worst case, the phase noise requirement for the VCO is relaxed, and power can be saved consistent with embodiments of the present invention. The achievable phase noise power spectral density is approximately inversely proportional to the bias current used. Thus, when low phase noise is not required during reception, bias current in the VCO can be reduced.

Most of the power savings in a transceiver in accordance with embodiments of the present invention is achieved in the receiver portion. Additional power may be saved in the transmitter section.

FIG. **15** is a block diagram of a transmitter portion consistent with an embodiment of the present invention. Included is a signal path formed by gain stage **1510** and power amplifier **1520**. The output power level is sensed by output level sensing circuit **1550**, which in turn adjusts the biasing of the power amplifier **1520** through the power control circuit **1540**. Additionally, a transmitter level control signal is received by power control circuits **1530** and **1540**, which in turn control the biasing of gain stage **1510** and power amplifier **1520**. Gain control circuit **1560** also adjusts the gain of gain stage **1510** and power amplifier **1520**. Additional circuitry that varies impedances in each of these circuits may also be included.

Since the gain, impedance and biasing of these blocks are being dynamically varied, care must be taken to not negatively affect the signal being processed. For example, specific embodiments of the present invention perform some or all of these variations during preamble. Also, as changes occur, the circuits in some embodiments are limited such that they may only adapt to an improvement in conditions after frames are completed. If conditions worsen, the circuits may be allowed to change in order to save the data. Alternately, a system may be manually calibrated, for example at set up, and when the network configuration is changed.

The above description of specific embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form described, and many modifications and variations are possible in light of the teaching above. The embodiments were chosen and described in order to best explain the principles of the invention and its practical applications to thereby enable others skilled in the art to best utilize the invention in various embodiments and with various modifications as are suited to the particular use contemplated.

What is claimed is:

1. A method of receiving a signal using an integrated circuit, the integrated circuit comprising a signal path including a low-noise amplifier configured to receive the signal, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer, the method comprising:

determining a first signal strength at a first node in the signal path in the integrated circuit; and

reducing a switching current in the signal path by dynamically changing an impedance of a component in the signal path based on the first signal strength.

2. The method of claim 1 wherein the signal comprises a preamble portion and a data portion, the impedance of a component is changed while receiving the preamble portion, and the method further comprises receiving the data portion of the signal.

3. The method of claim 2 further comprising:

determining a second signal strength at a second node in the signal path, wherein the second node in the signal path is after the first node in the signal path.

4. The method of claim 3 wherein the impedance of the component in the signal path is also changed based on the second signal strength.

5. The method of claim 2 wherein the component in the signal path comprises a MOS transistor.

6. The method of claim 2 wherein the component in the signal path comprises a resistor.

7. The method of claim 2 wherein the component in the signal path comprises a capacitor.

8. The method of claim 4 wherein the component in the signal path is included in the mixer.

9. The method of claim 4 wherein the component in the signal path is included in the low-pass filter.

10. A method of receiving a signal comprising a preamble portion and a data portion using an integrated circuit, the integrated circuit comprising a signal path including a low-noise amplifier configured to receive the signal, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer, the method comprising:

determining a first signal strength at a first node in the signal path in the integrated circuit; and

while receiving the preamble portion of the signal, dynamically changing a bias current in the signal path based on the first signal strength, and while receiving the data portion of the signal, maintaining the bias current in the signal path.

11. The method of claim 10 wherein the method further comprises receiving the data portion of the signal.

12. The method of claim 11 further comprising:

determining a second signal strength at a second node in the signal path, wherein the second node in the signal path is after the first node in the signal path.

13. The method of claim 12 wherein the bias current in the signal path is also changed based on the second signal strength.

14. The method of claim 11 wherein the bias current is a bias current for the low-noise amplifier.

15. The method of claim 11 wherein the bias current is a bias current for the mixer.

16. The method of claim 11 wherein the bias current is a bias current for the low-pass filter.

17. A method of receiving a signal using an integrated circuit, the integrated circuit comprising a signal path including a first circuit and a second circuit having an input coupled to an output of the first circuit, the method comprising:

determining a first signal strength at a first node in the signal path in the integrated circuit, wherein the first node is before the first circuit in the signal path;

dynamically changing a gain of the first circuit based on the first signal strength; and

dynamically changing an impedance of a component in the second circuit based on the first signal strength.

18. The method of claim 17 wherein the signal comprises a preamble portion and a data portion, the gain and impedance are changed while receiving the preamble portion, and the method further comprises receiving the data portion of the signal.

19. The method of claim 18 further comprising:

determining a second signal strength at a second node in the signal path, wherein the second node in the signal path is after the second circuit in the signal path.

20. The method of claim 19 wherein the gain of the first circuit and impedance of the component in the second circuit is also changed based on the second signal strength.

21. The method of claim 18 wherein the first circuit is a low-noise amplifier.

22. The method of claim 18 wherein the first circuit is a mixer.

23. A wireless transceiver integrated circuit comprising:

a receiver comprising a signal path, the signal path comprising:

a low-noise amplifier;

a mixer having an input coupled to an output of the low-noise amplifier; and

a low-pass filter having an input coupled to an output of the mixer; and

a first signal strength indicator circuit coupled to the signal path, and configured to determine a first signal strength;

wherein an impedance in the signal path is configured to be dynamically adjusted to reduce a switching current in response to the first signal strength.

24. The wireless transceiver of claim 23 further comprising:

a second signal strength indicator circuit coupled to the output of the mixer, and configured to determine a second signal strength,

wherein the first signal strength indicator is coupled to the output of the low-noise amplifier, and

wherein the impedance in the signal path is configured to be adjusted in response to the first and second signal strengths.

25. The wireless transceiver of claim 23 further comprising:

a second signal strength indicator circuit coupled to the output of the low-pass filter, and configured to determine a second signal strength,

wherein the first signal strength indicator is coupled to the output of the mixer, and

wherein the impedance in the signal path is configured to be adjusted in response to the first and second signal strengths.

26. A wireless transceiver integrated circuit comprising:

a receiver comprising a signal path, the signal path comprising:

a low-noise amplifier;

a mixer having an input coupled to an output of the low-noise amplifier; and

a low-pass filter having an input coupled to an output of the mixer; and

a first signal strength indicator circuit coupled to the signal path, and configured to determine a first signal strength, the first signal strength the strength of a signal comprising a preamble portion and a data portion;

wherein a bias current in the signal path is configured to be dynamically adjusted during the preamble portion of the signal in response to the first signal strength and further configured to be maintained during the data portion of the signal.

27. The wireless transceiver of claim 26 further comprising:

a second signal strength indicator circuit coupled to the output of the mixer, and configured to determine a second signal strength,

wherein the first signal strength indicator is coupled to the output of the low-noise amplifier, and

wherein the bias current in the signal path is configured to be adjusted in response to the first and second signal strengths.

28. The wireless transceiver of claim 26 further comprising:

a second signal strength indicator circuit coupled to the output of the low-pass filter, and configured to determine a second signal strength,

wherein the first signal strength indicator is coupled to the output of the mixer, and

wherein the bias current in the signal path is configured to be adjusted in response to the first and second signal strengths.

29. A wireless transceiver integrated circuit comprising:

a receiver comprising a signal path, the signal path comprising:

a first circuit; and

a second circuit having an input coupled to an output of the first circuit; and

a first signal strength indicator circuit coupled to the signal path, and configured to determine a first signal strength,

wherein a gain of the first circuit is configured to be dynamically adjusted in response to the first signal strength, and

wherein an impedance in the second circuit is configured to be dynamically adjusted in response to the first signal strength.

30. The wireless transceiver of claim 29 further comprising:

a transmitter comprising:

a power amplifier; and

an output-level-sensing circuit coupled to an output of the power amplifier,

wherein the output-level-sensing circuit is configured to dynamically adjust a gain of the power amplifier.

* * * * *

Exhibit B

US010129825B2

(12) **United States Patent**
Tsividis

(10) **Patent No.: US 10,129,825 B2**
(45) **Date of Patent: *Nov. 13, 2018**

(54) **POWER DISSIPATION REDUCTION IN WIRELESS TRANSCEIVERS**

(71) Applicant: **Theta IP, LLC**, Coppell, TX (US)

(72) Inventor: **Yannis Tsividis**, New York, NY (US)

(73) Assignee: **Theta IP, LLC**, Coppell, TX (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **15/080,432**

(22) Filed: **Mar. 24, 2016**

(65) **Prior Publication Data**

US 2016/0212701 A1 Jul. 21, 2016

Related U.S. Application Data

(63) Continuation of application No. 11/318,646, filed on Dec. 27, 2005, now Pat. No. 9,331,728, which is a (Continued)

(51) **Int. Cl.**
H04B 1/38 (2015.01)
H04M 1/00 (2006.01)
(Continued)

(52) **U.S. Cl.**
CPC ***H04W 52/0209*** (2013.01); ***H04B 1/109*** (2013.01); ***Y02D 70/00*** (2018.01); ***Y02D 70/142*** (2018.01); ***Y02D 70/40*** (2018.01)

(58) **Field of Classification Search**
CPC ... H04B 1/04; H04B 1/16; H04B 1/40; H04B 1/109; H04B 1/0457; H04B 1/1607;
(Continued)

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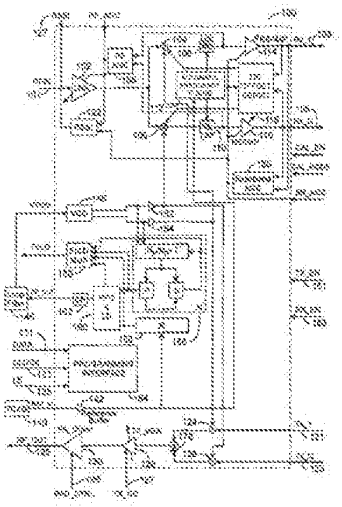
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Primary Examiner — Quochien B Vuong
(74) *Attorney, Agent, or Firm* — Womble Bond Dickinson (US) LLP

(57) **ABSTRACT**

Processes, methods and circuits for improving battery life by reducing the battery power-drain of battery-powered devices using wireless transceivers is disclosed. Embodiments of the present invention provide for dynamically changing the bias current, impedance, and gain, either separately or in combination, during circuit operation to optimize or to reduce power dissipation. The dynamic variations may be implemented by varying the value of a resistance and/or a capacitance by opening switches across one or more portions of the resistance. Also, the dynamic variations may include setting any of the gain, bias current, or impedance parameters of the receiver circuit in between a high and low level, followed by adjusting the parameter up or down in response to a desired signal and an interferer signal.

8 Claims, 15 Drawing Sheets



US007010330B1

(12) **United States Patent**
Tsividis

(10) **Patent No.: US 7,010,330 B1**
(45) **Date of Patent: Mar. 7, 2006**

(54) **POWER DISSIPATION REDUCTION IN WIRELESS TRANSCEIVERS**

(75) Inventor: **Yannis Tsividis**, New York, NY (US)

(73) Assignee: **Theta Microelectronics, Inc.**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/784,613**

(22) Filed: **Feb. 23, 2004**

Related U.S. Application Data

(60) Provisional application No. 60/451,229, filed on Mar. 1, 2003, provisional application No. 60/451,230, filed on Mar. 1, 2003.

(51) **Int. Cl.**
H04B 1/38 (2006.01)
H04M 1/00 (2006.01)

(52) **U.S. Cl.** **455/574**; 455/234.1; 455/251.1; 455/343.1

(58) **Field of Classification Search** 455/63.1, 455/67.13, 226.1, 226.2, 232.1, 234.1, 250.1, 455/251.1, 295, 296, 311, 333, 343.1, 127.1, 455/127.2, 127.5, 574, 572; 370/442; 330/127, 330/129, 134, 136, 144
See application file for complete search history.

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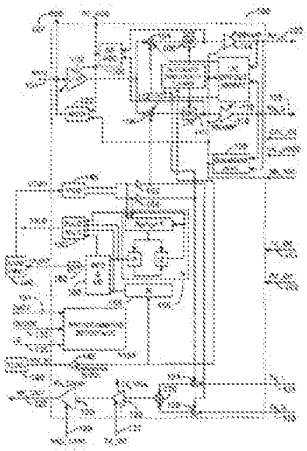
(Continued)

Primary Examiner—Quochien B. Vuong
(74) *Attorney, Agent, or Firm*—Blakely, Sokoloff, Taylor & Zafman LLP

(57) **ABSTRACT**

Methods and circuits for reducing power dissipation in wireless transceivers and other electronic circuits and systems. Embodiments of the present invention use bias current reduction, impedance scaling, and gain changes either separately or in combination to reduce power dissipation. For example, bias currents are reduced in response to a need for reduced signal handling capability, impedances are scaled thus reducing required drive and other bias currents in response to a strong received signal, or gain is increased and impedances are scaled in response to a low received signal in the presence of no or weak interfering signals.

30 Claims, 15 Drawing Sheets



Related U.S. Application Data

continuation of application No. 10/784,613, filed on Feb. 23, 2004, now Pat. No. 7,010,330.

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(51) **Int. Cl.**
H04W 52/02 (2009.01)
H04B 1/10 (2006.01)

(58) **Field of Classification Search**
CPC .. H04B 17/309; H04B 17/318; H04B 17/336; H04B 17/345; H04B 2001/045; H04B 2001/0416; H04W 52/52; H04W 52/0261; H04W 88/02; H03G 3/004; H03G 3/20
USPC 455/63.1, 67.13, 127.1, 127.2, 127.5, 455/226.1, 226.2, 232.1, 234.1, 250.1, 455/251.1, 295, 296, 343.1, 572, 574; 370/442; 330/127, 134, 144
See application file for complete search history.

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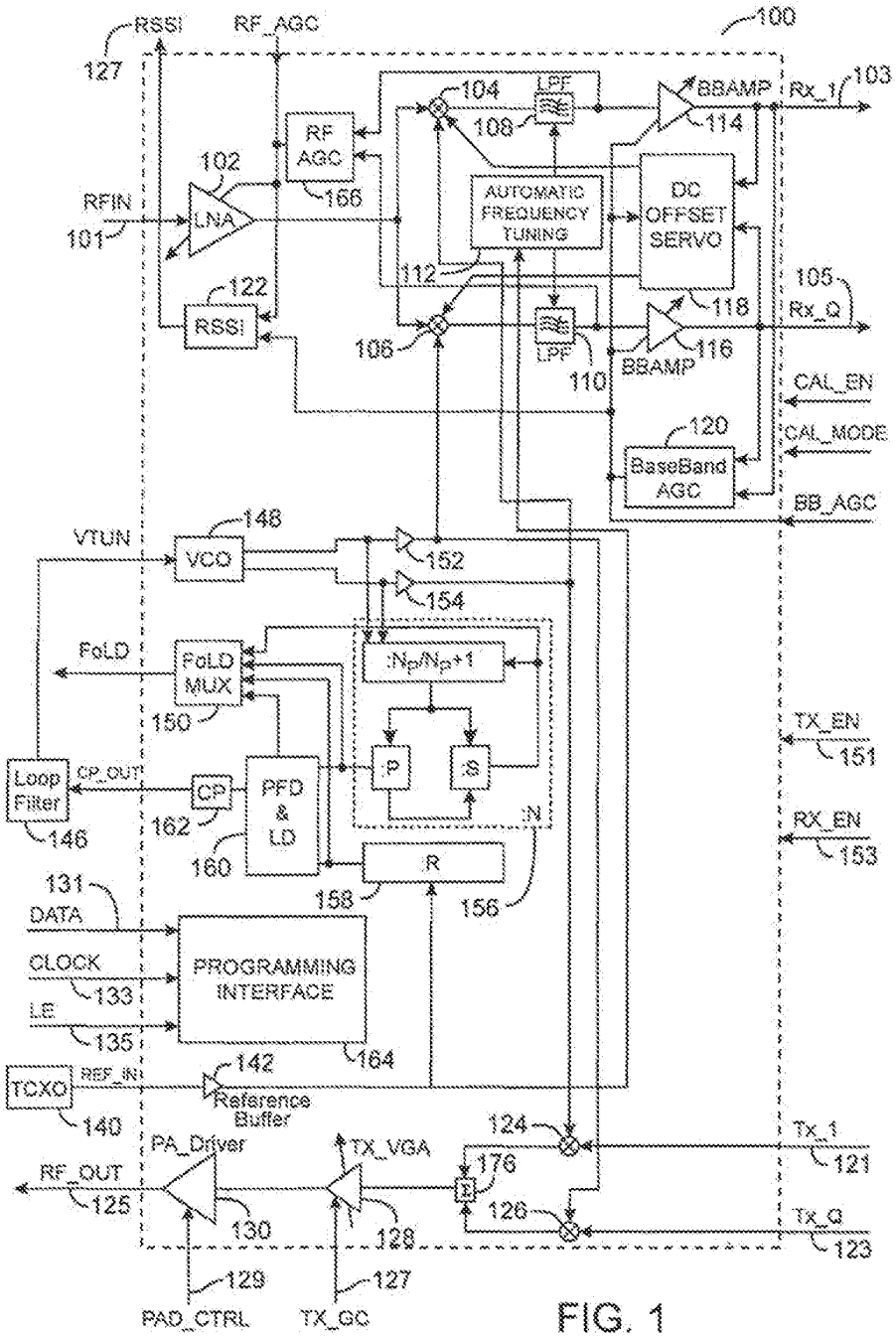

RSSI
127
RF_AGC
100
104
LPF
108
BBAMP
114
Rx_I
103
RF AGC
166
102
RFIN
101
LNA
AUTOMATIC FREQUENCY TUNING
DC OFFSET SERVO
112
122
RSSI
105
Rx_Q
118
106
LPF
110
BBAMP
116
CAL_EN
CAL_MODE
120
BaseBand AGC
BB_AGC
148
VTUN
VCO
152
154
FoLD
FoLD MUX
150
:Np/Np+1
:P
:S
:N
TX_EN
151
Loop Filter
146
CP_OUT
CP
162
PFD & LD
160
R
158
156
RX_EN
153
131
DATA
CLOCK
133
LE
135
PROGRAMMING INTERFACE
164
TCXO
140
REF_IN
142
Reference Buffer
124
Tx_I
121
PA_Driver
TX_VGA
176
RF_OUT
125
130
128
126
Tx_Q
123
129
PAD_CTRL
127
TX_GC

FIG. 1

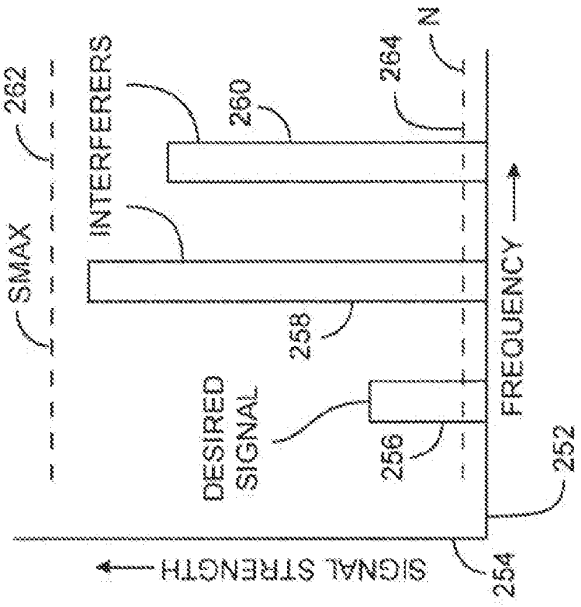

SIGNAL STRENGTH
FREQUENCY
SMAX
262
INTERFERERS
260
264
N
DESIRED SIGNAL
258
256
252
254

FIG. 2B

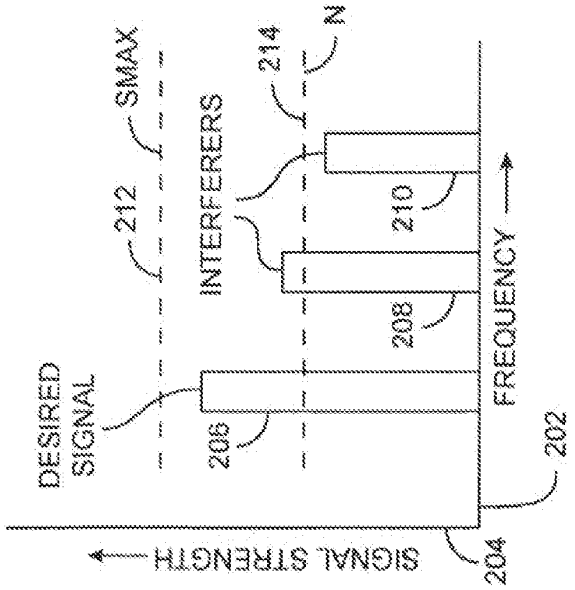

SIGNAL STRENGTH
FREQUENCY
SMAX
212
INTERFERERS
214
N
DESIRED SIGNAL
206
208
210
202
204

FIG. 2A

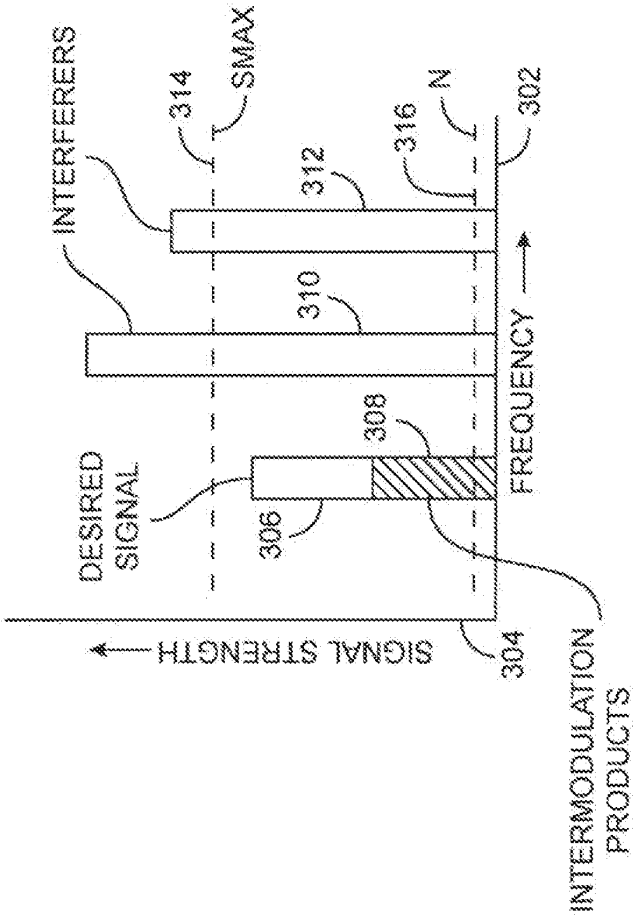

INTERFERERS
314
SMAX
312
316
N
302
310
308
DESIRED SIGNAL
306
FREQUENCY
SIGNAL STRENGTH
304
INTERMODULATION PRODUCTS

FIG. 3

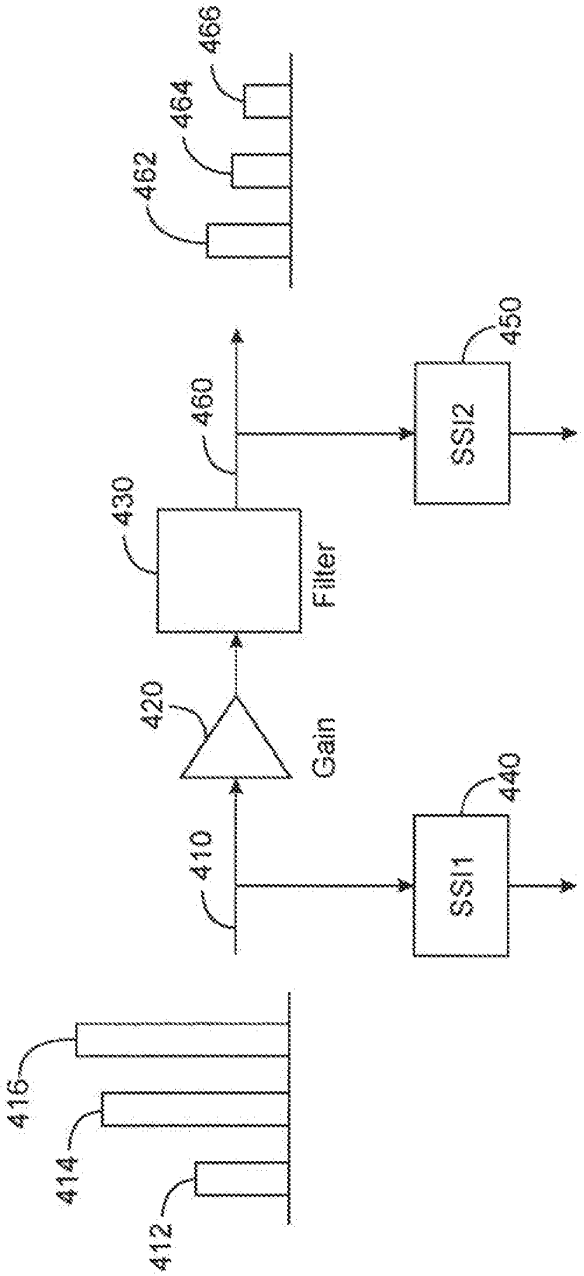

466
464
462
460
450
SSI2
430
Filter
420
Gain
410
440
SSI1
416
414
412

FIG. 4

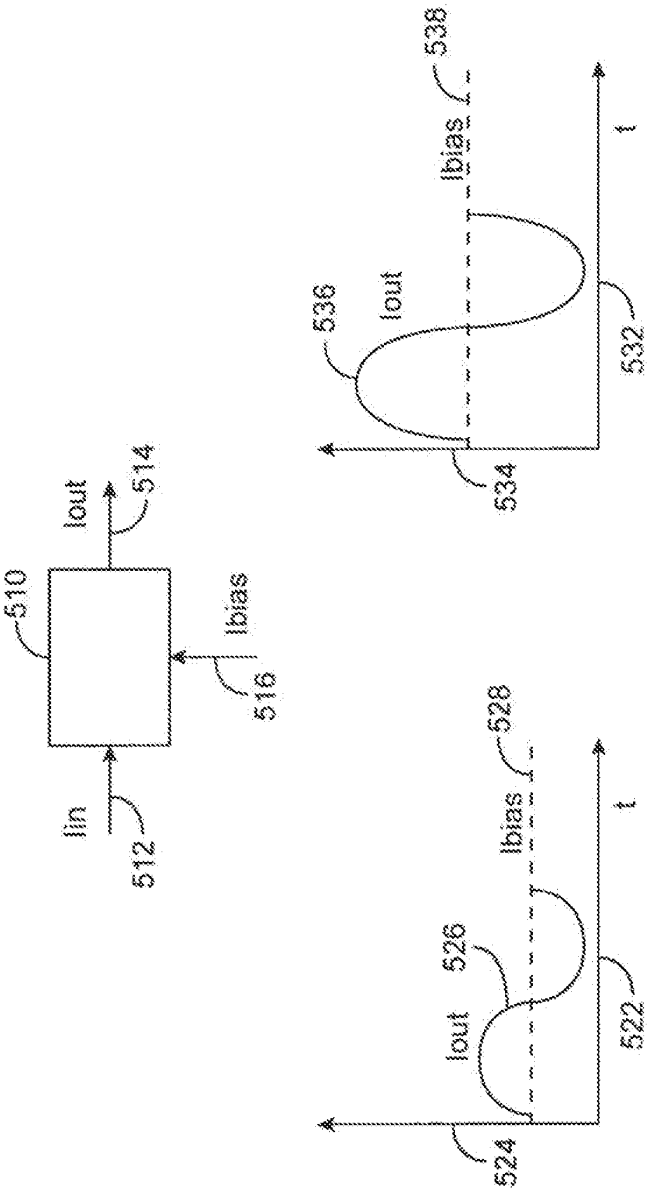

510
Iin
512
Iout
514
Ibias
516
Iout
536
Ibias
538
534
532
t
Iout
526
Ibias
528
524
522
t

FIG. 5

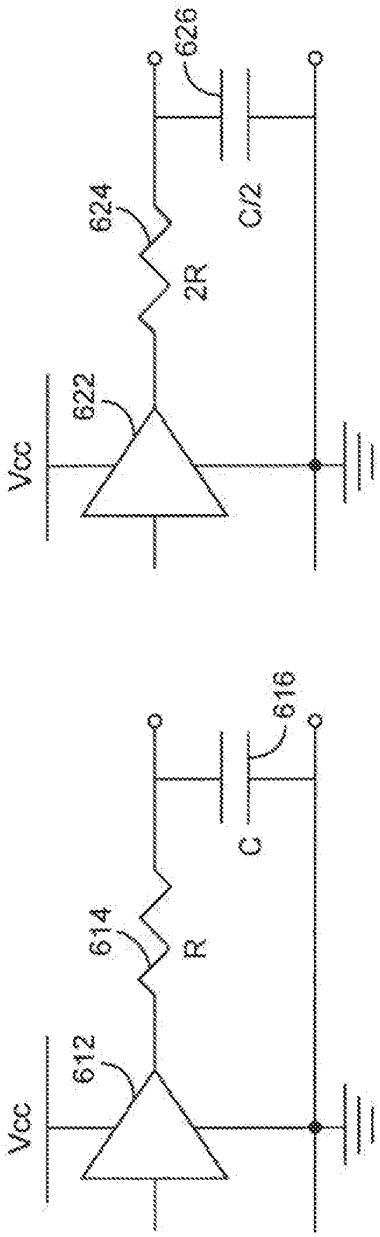


FIG. 6

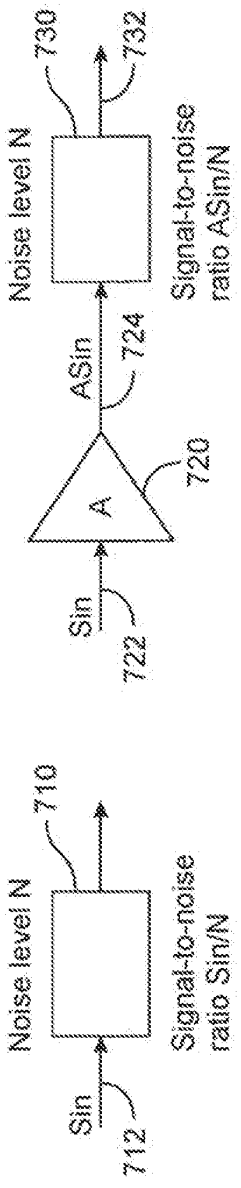

730
732
Noise level N
Signal-to-noise ratio ASin/N
ASin
724
720
A
Sin
722
710
Noise level N
Signal-to-noise ratio Sin/N
Sin
712

FIG. 7

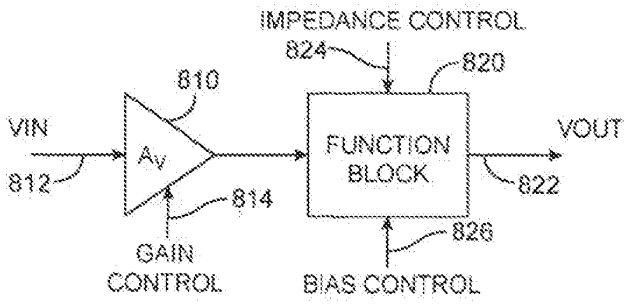


FIG. 8A

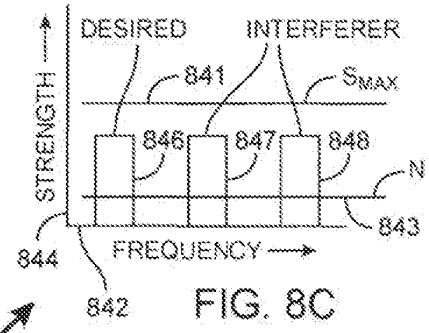


FIG. 8C

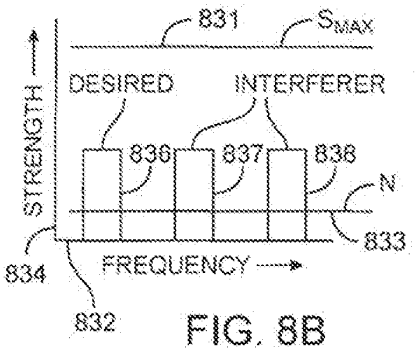


FIG. 8B

DECREASE BIASING

– AND/OR –

INCREASE GAIN AND IMPEDANCES

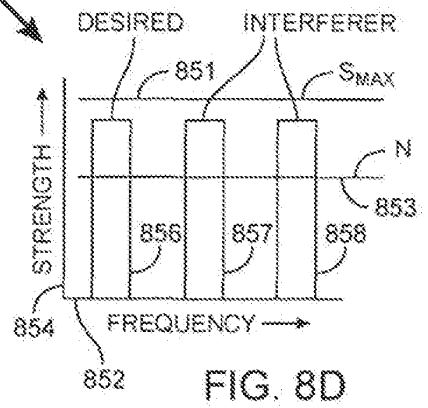


FIG. 8D

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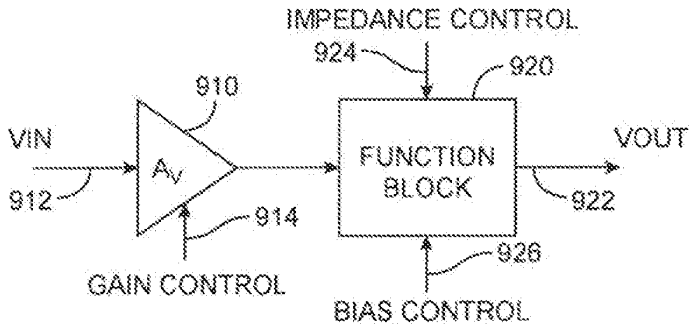


FIG. 9A

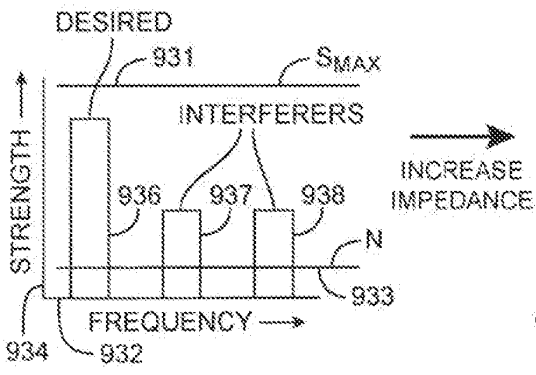


FIG. 9B

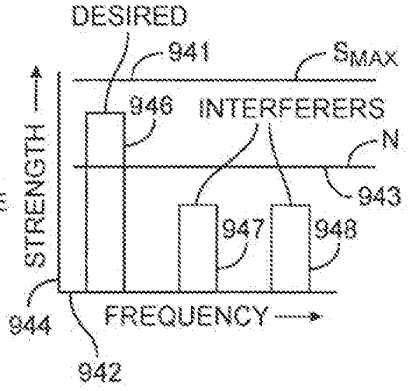


FIG. 9C

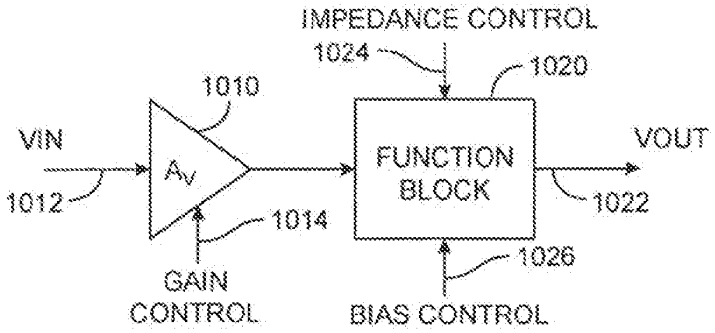


FIG. 10A

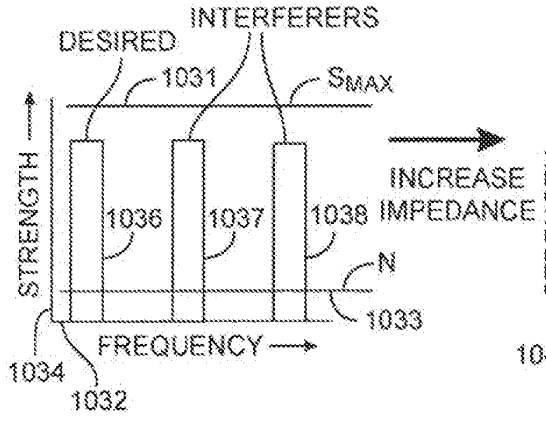


FIG. 10B

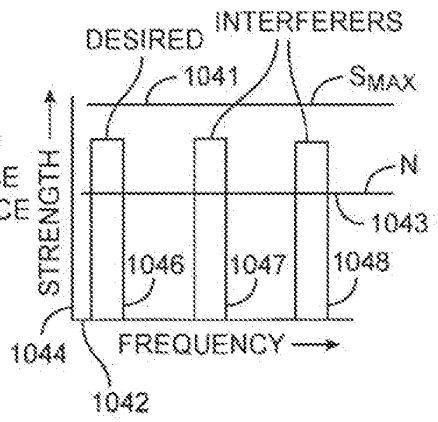


FIG. 10C

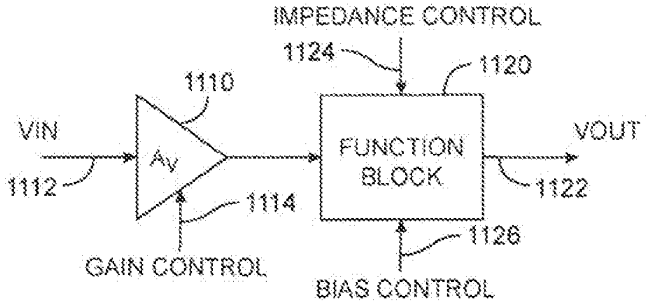


FIG. 11A

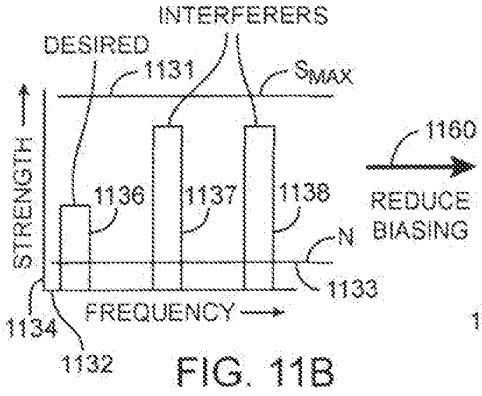


FIG. 11B

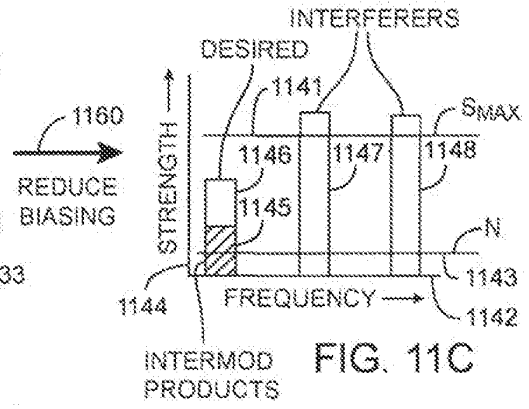


FIG. 11C

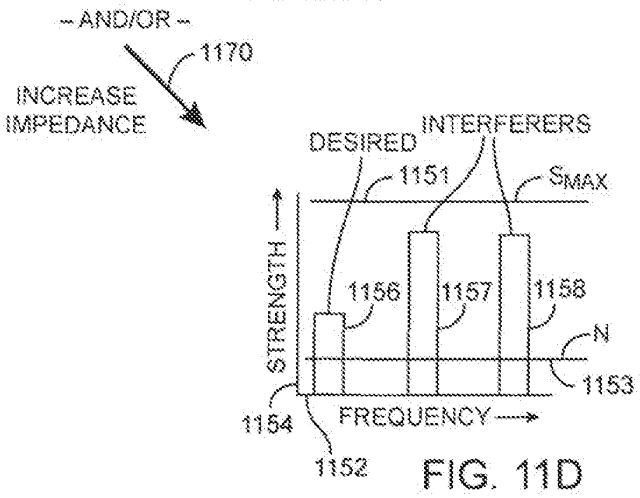


FIG. 11D

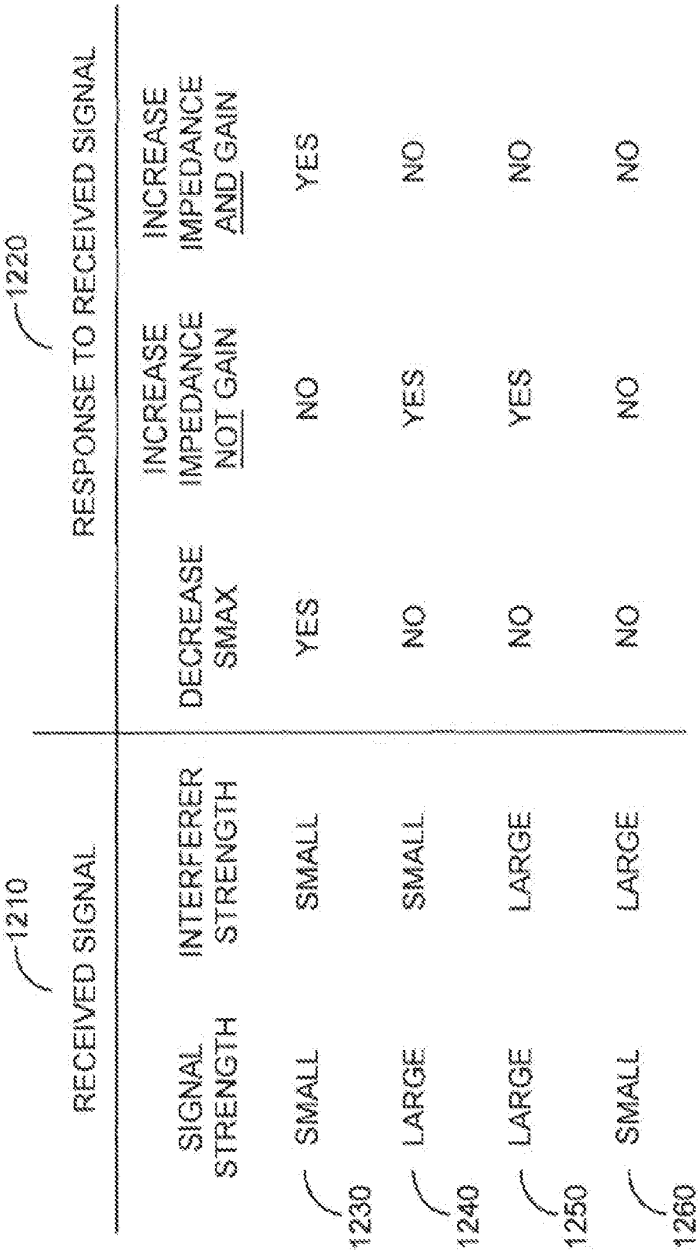

1210
RECEIVED SIGNAL
1220
RESPONSE TO RECEIVED SIGNAL
SIGNAL STRENGTH
INTERFERER STRENGTH
DECREASE SMAX
INCREASE IMPEDANCE NOT GAIN
INCREASE IMPEDANCE AND GAIN
SMALL
SMALL
YES
NO
YES
1230
LARGE
SMALL
NO
YES
NO
1240
LARGE
LARGE
NO
YES
NO
1250
SMALL
LARGE
NO
NO
NO
1260

FIG. 12

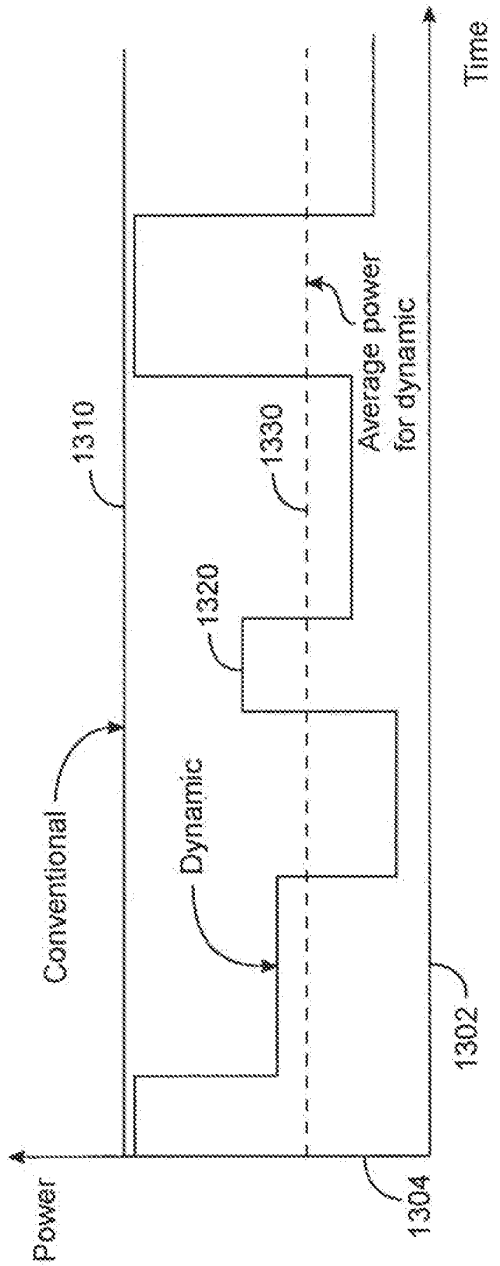

Power
Time
Conventional
Dynamic
1310
1320
1330
1302
1304
Average power
for dynamic

FIG. 13

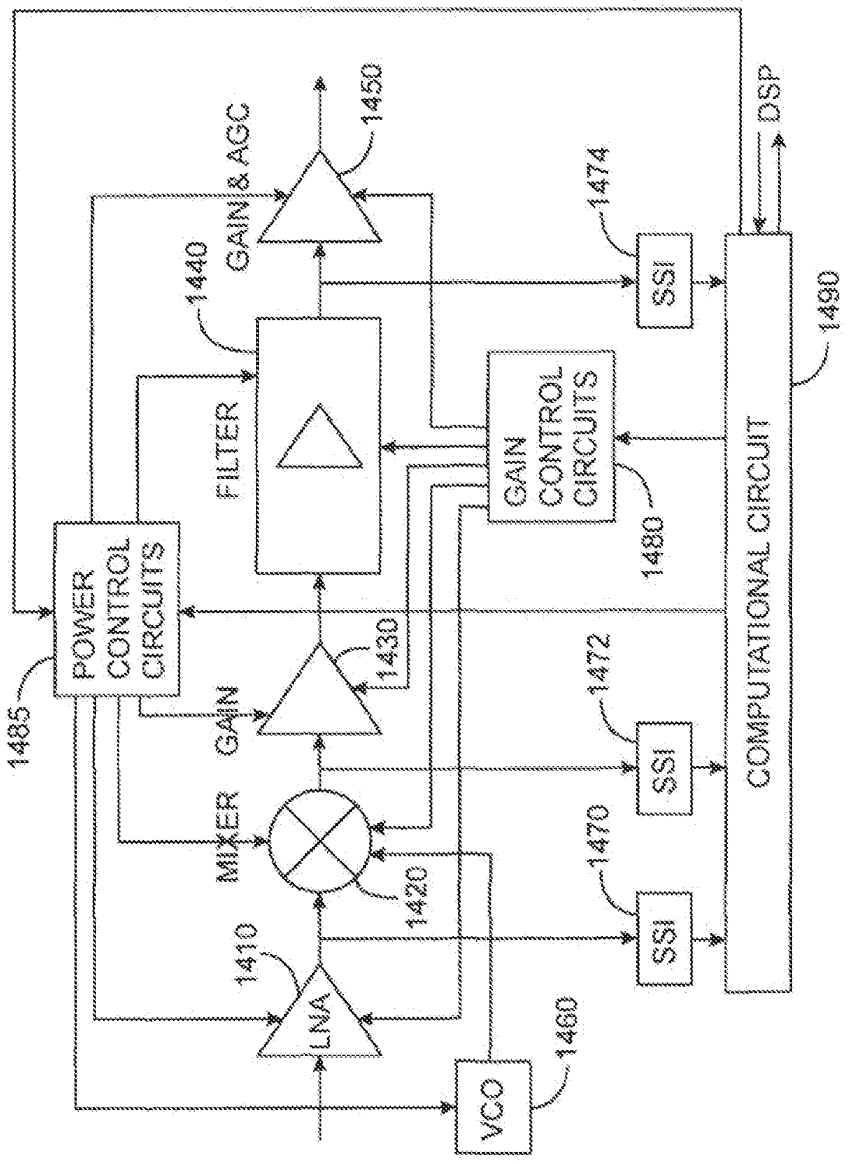

DSP
1450
GAIN & AGC
1474
SSI
1440
FILTER
GAIN CONTROL CIRCUITS
1490
COMPUTATIONAL CIRCUIT
1480
POWER CONTROL CIRCUITS
1485
1430
GAIN
1472
SSI
MIXER
1420
1470
SSI
1410
LNA
VCO
1460

FIG. 14

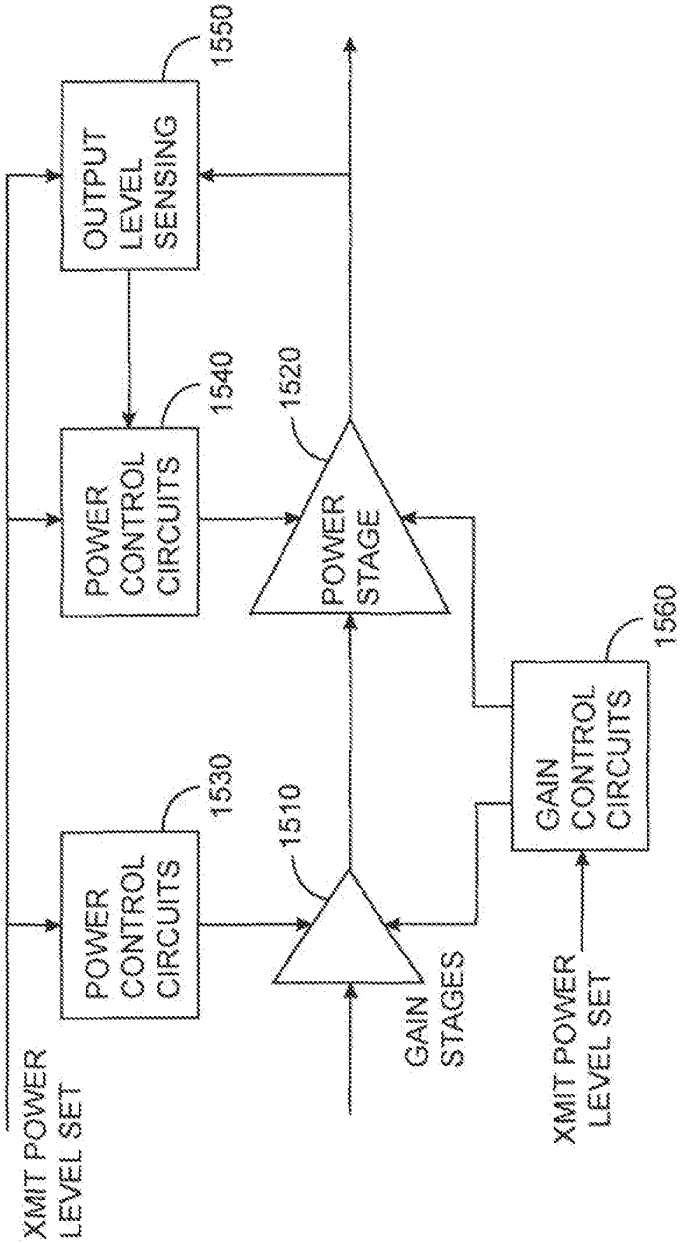

XMIT POWER LEVEL SET
POWER CONTROL CIRCUITS
1530
1510
GAIN STAGES
POWER CONTROL CIRCUITS
1540
1520
POWER STAGE
OUTPUT LEVEL SENSING
1550
GAIN CONTROL CIRCUITS
1560
XMIT POWER LEVEL SET

FIG. 15

POWER DISSIPATION REDUCTION IN WIRELESS TRANSCEIVERS

CROSS-REFERENCES TO RELATED APPLICATIONS

This application is a continuation of U.S. patent application Ser. No. 11/318,646, filed Dec. 27, 2005, which is a continuation of U.S. patent application Ser. No. 10/784,613, filed Feb. 23, 2004, which claims the benefit of U.S. provisional application No. 60/451,229, filed Mar. 1, 2003, which is incorporated by reference.

This application claims the benefit of U.S. provisional application No. 60/451,230, filed Mar. 1, 2003, which is incorporated by reference.

BACKGROUND

The present invention relates to power dissipation reduction techniques for electronic circuits, for example wireless transceiver integrated circuits.

Wireless networking is quickly becoming ubiquitous, as desktop, notebook, and handheld computers are connected to share Internet access and files. Wireless networking cards compatible with PCMCIA and compact flash form factors are popular for laptops and handhelds respectively, particularly as mobile users connect to the Internet on the road at coffee shops, hotels, and airports.

A downside of this connectivity is a corresponding drain on battery life, especially for these portable devices. The power consumed by a wireless transmitter and receiver reduces the usefulness of a device and sends a user on a hunt for an electrical outlet for recharging.

One reason why this power drain is high is that electronic circuits are typically designed to function properly under worst-case operating conditions. For a wireless transceiver, the worst case condition is when a desired signal reception strength is low, while other transceivers or nearby electronic equipment generate interfering signals and other spurious noise.

But a wireless transceiver does not always operate in these worst-case conditions. For example, a base station, router or access point may be nearby such that the received signal is strong. Also, there may be no interfering signals, or they may be relatively weak. In these situations, receiver circuit currents can be reduced below what is necessary for the worst case condition. If this is done, power dissipation is reduced, and battery life is increased.

Thus, what is needed are circuits and methods that can adapt to a better-than-worst-case condition and reduce circuit currents and therefore power dissipation accordingly.

SUMMARY

Accordingly, embodiments of the present invention provide methods and circuits for reducing power dissipation in wireless transceivers and other electronic circuits and systems. Embodiments of the present invention use bias current reduction, impedance scaling, gain, and other dynamic changes either separately or in combination to reduce power dissipation in response to better-than-worst case conditions. For example, bias currents are reduced in response to a need for reduced signal handling capability, impedances are scaled thus reducing required drive and other bias currents in response to a strong received signal, or gain is varied and impedances are scaled in response to a low received signal in the presence of no or weak interfering signals. Alternately, currents may start low and be increased in response to worse-than-best-case conditions, or they may start at a point in between and vary up or down. These variations may be made to electronic systems generally, and are particularly suited and discussed below in the context of a wireless transceiver that may be used in networking devices, cellular telephones, and other wireless systems.

An exemplary embodiment of the present invention provides a method of receiving a signal using an integrated circuit. The integrated circuit includes a signal path having a low-noise amplifier configured to receive the signal, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer. The method itself includes determining a first signal strength at a first node in the signal path in the integrated circuit and dynamically changing an impedance of a component in the signal path based on the first signal strength.

A further exemplary embodiment of the present invention provides a method of receiving a signal using an integrated circuit. The integrated circuit includes a signal path having a low-noise amplifier configured to receive the signal, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer. The method itself includes determining a first signal strength at a first node in the signal path in the integrated circuit and dynamically changing a bias current in the signal path based on the first signal strength.

Another exemplary embodiment of the present invention provides a method of receiving a signal using an integrated circuit. The integrated circuit includes a signal path having a first circuit and a second circuit having an input coupled to an output of the first circuit. The method itself includes determining a first signal strength at a first node in the signal path in the integrated circuit. The first node is before the first circuit in the signal path. The method further includes dynamically changing a gain of the first circuit based on the first signal strength and dynamically changing an impedance of a component in the second circuit based on the first signal strength.

Still a further exemplary embodiment of the present invention provides a wireless transceiver integrated circuit including a receiver having a signal path, the signal path including a low-noise amplifier, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer, as well as a first signal strength indicator circuit coupled to the signal path and configured to determine a first signal strength. An impedance in the signal path is configured to be dynamically adjusted in response to the first signal strength.

Yet a further exemplary embodiment of the present invention provides a wireless transceiver integrated circuit. This integrated circuit includes a receiver comprising a signal path, the signal path having a low-noise amplifier, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer, as well as a first signal strength indicator circuit coupled to the signal path, and configured to determine a first signal strength. A bias current in the signal path is configured to be dynamically adjusted in response to the first signal strength.

Another exemplary embodiment of the present invention provides a wireless transceiver integrated circuit. This circuit includes a receiver comprising a signal path, the signal path having a first circuit; and a second circuit having an input coupled to an output of the first circuit; as well as a first

signal strength indicator circuit coupled to the signal path, and configured to determine a first signal strength. A gain of the first circuit is configured to be dynamically adjusted in response to the first signal strength, and an impedance in the second circuit is configured to be dynamically adjusted in response to the first signal strength.

A better understanding of the nature and advantages of the present invention may be gained with reference to the following detailed description and the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram of a wireless transceiver that may benefit by incorporation of embodiments of the present invention;

FIGS. **2**A and **2**B illustrate examples of desired and interfering signals and noise that may be received by a circuit in a wireless receiver;

FIG. **3** illustrates what can occur as a maximum signal handling capability is reduced in the worst-case signal condition;

FIG. **4** illustrates a portion of a receiver consistent with an embodiment of the present invention;

FIG. **5** illustrates the relationship between a required bias current and a given output signal for a representative circuit;

FIG. **6** is an example of how a circuit's impedances may be scaled to reduce drive currents, and depending on the circuit configuration used, to reduce associated bias currents as well;

FIG. **7** illustrates how gain may be inserted in a signal path to improve a circuit's signal to noise ratio;

FIGS. **8**A-**8**D illustrate some of the possible power saving techniques that may be used when received desired and interferer signals are all at a low power level;

FIGS. **9**A-**9**C illustrate one of the possible power saving techniques that may be used when a received desired signal is strong while all interfering signals are at a low power level;

FIGS. **10**A-**10**C illustrate one of the possible power saving techniques that may be used when received desired and interferer signals are all at a high power level;

FIGS. **11**A-**11**D illustrate one of the possible power saving techniques that may be used when a received desired signal is weak while one or more interfering signals are strong;

FIG. **12** is a summary illustrating four different input conditions and some of the appropriate power-saving changes that may be made in response to those conditions;

FIG. **13** shows how power may be saved as a function of time by employing one or more of the power saving methods consistent with embodiments of the present invention;

FIG. **14** is a block diagram of a portion of a receiver consistent with an embodiment of the present invention; and

FIG. **15** is a block diagram of a portion of a transmitter consistent with an embodiment of the present invention.

DESCRIPTION OF EXEMPLARY EMBODIMENTS

FIG. **1** is a block diagram of a wireless transceiver that may benefit by incorporation of embodiments of the present invention. This wireless transceiver may be designed to send and receive signals consistent with the IEEE 802.11a, 802.11b, 802.11g, or other signaling standard or combination of standards. This figure, as with all the included figures, is shown for illustrative purposes only and does not to limit either the possible embodiments of the present invention or the claims.

There are three main portions of this transceiver circuit, a receiver, transmitter, and synthesizer. This transceiver may be completely or partially integrated on a semiconductor chip, or it may be integrated onto multiple integrated circuits. In a specific embodiment, the circuitry bounded by dashed line **100** is integrated on a single chip coupled to one or more external components or circuits. The integrated circuit or circuits forming this wireless transceiver may incorporate various integrated circuit devices such as a bipolar, CMOS, or BiCMOS devices made using a silicon, silicon-germanium (SiGe), gallium arsenide or other III-V process, or other manufacturing process. Embodiments of the present invention may also be applicable to circuits manufactured using nanotechnology processing.

The receiver includes a signal path formed by low-noise amplifier **102**, I and Q mixers **104** and **106**, low pass filters **108** and **110**, and baseband amplifiers **114** and **116**. Other circuitry in the receiver includes received strength indicator **122**, automatic gain control circuit **166**, baseband gain control circuit **120**, tuning circuit **112**, and offset cancellation circuit **118**.

The transmitter includes input up-converter mixers **124** and **126**, summing node **176**, which may be conceptual rather than an actual circuit, transmit variable gain amplifier **128**, and power amplifier **130**.

The synthesizer includes a voltage-controlled oscillator **148**, which drives I and Q buffers **154** and **152**, prescaler **156**, reference clock buffer **142** and divider **158**, phase-frequency detector **160**, charge pump **162**, and loop filter **146**, which in a specific embodiment is formed by external components.

Signals are received on an antenna, not shown, and typically pass through an RF switch and bandpass filter before being received by the low-noise amplifier **102** on line **101**. The low noise amplifier gains the received signal and provides it to quadrature mixers **104** and **106**. I and Q mixers **104** and **106** down-convert the received signal to baseband by multiplying them with quadrature versions of the oscillator signal provided by buffers **152** and **154**. This down conversion also produces a high frequency component at a frequency that is equal to the sum of the frequencies of the received signal and the VCO. This unwanted signal is filtered by low pass filters **108** and **110**, which in turn drive baseband amplifiers **114** and **116**. The outputs of baseband amplifiers **114** and **116** are typically converted to digital signals by analog-to-digital converters at the front end of a digital signal processing block.

In the transmit mode, I and Q versions of the signal to be transmitted are provided on lines **121** and **123** to up-convert mixers **124** and **126**. These up-convert mixers multiply the I and Q portions of the transmit signal by quadrature versions of the VCO signal provided by buffers **152** and **154**. The outputs of the up-convert mixers **124** and **126** are summed, and amplified by transmit VGA **128**, which in turn drives power amplifier **130**. The output of power amplifier **130** is typically filtered, and passes through the RF switch to the antenna for transmission.

A reference clock is received and buffered by the reference buffer **142**. The VCO generates quadrature oscillatory signals that are divided by prescaler **156**. The reference clock is typically generated by a crystal or other stable periodic clock source. The phase-frequency detector **116** compares the phase or frequency (depending on whether the synthesizer is tracking or acquiring the correct frequency) of

the divided VCO signal and the reference clock, or a divided version of the reference clock, and generates an error signal, which drives the charge pump **162**. The output signal of the charge pump **162** is filtered by the loop filter **146**, which is commonly a lead-lag filter, and which provides a tuning or correction signal to the VCO **148**.

Embodiments of the present invention may be used to reduce the power dissipation of one or more of these included circuits. For example, the power dissipation in the low-noise amplifier **102**, down-convert mixers **104** and **106**, low pass filters **108** and **110**, or baseband amplifiers **114** and **116** may be optimized. Also, power dissipation in up-convert mixers **124** **126**, variable gain amplifier **128**, and power amplifier **130** may also be optimized. Similarly, VCO **148** and prescaler **156** currents may be adjusted. Embodiments of the present invention may also be applied in other circuits which may be included in other integrated circuit receivers, transmitters, transceivers, or other electronic circuits or systems.

When a receiver is actively receiving a desired signal, each block in the signal path has at its input the desired signal as well as noise and possibly interfering signals. The desired signal is the useful, information-carrying portion of a received signal. The noise may be thermal, shot, or other noise generated on the integrated circuit, in addition to received noise generated by sources external to the chip. The noise at the input of a block may be referred to as the equivalent input noise. The interfering signal or signals, or interferers, may be generated by similar transceivers, or other electrical equipment, circuits, or systems.

FIGS. **2**A and **2**B illustrate examples of desired signals, interferers, and noise that may be received by one of the various circuits in a wireless receiver. In each of these figures, the signal strength is plotted along a Y-axis **204** or **254** as a function of frequency along an X-axis **202** or **252**. In the example of FIG. **2**A, a received desired signal **206** is large in comparison to interfering signals **208** and **210**. In these examples, two interfering signals are shown for illustrative purposes, though there may be no such signals, one such signal, or more than two such signals in the frequency range of interest. Also, while for these examples the interferers are shown as being at a higher frequency than the desired signal, there may be one or more interferers at higher or lower frequencies as the desired signal. In this specific example, the acceptable noise floor **214** is relatively high, while maximum signal handling capability Smax **212** (that is the maximum signal power that can be handled with an acceptably low distortion) needs only to be high enough to accommodate the desired signal. For this specific example, the circuit receiving this input spectrum only requires a relatively small dynamic range for proper operation, that is the range between Smax **212** and the noise floor **214** is relatively small.

Conversely, in the example shown in FIG. **2**B, the desired signal **256** is relatively weak compared to the large interferers **258** and **260**. In this example, the noise floor **264** should be relatively low so as to prevent an unacceptable level of error in the recovery the desired signal **256**. The maximum signal handling capability Smax **262** should be relatively high to accommodate the large interferers in order to avoid the creation of intermodulation products as described below. Accordingly, in this specific example, the circuit receiving this input spectrum should have a large dynamic range, particularly in comparison to the example of FIG. **2**A.

It should be noted that the noise level or noise floors shown in these and the other included figures is the noise density integrated over the bandwidth of interest. For simplicity and comparison, this level is shown as a horizontal line, and is not meant to imply noise density.

Often in wireless receivers, a circuit at different times will receive an input spectrum similar to those shown in FIGS. **2**A and **2**B. The input spectrum of FIG. **2**B is generally considered the worst-case input signal, and typical design methodology involves designing a receiver for this condition, specifically the weakest desired signal accompanied by largest interference level. Circuit impedances and currents are set such that the noise floor **264** is sufficiently low for an acceptable bit-error rate, while bias currents are set sufficiently high for the required Smax **262**.

Conversely, the input spectrum in FIG. **2**A is that of the best-case input signal, specifically, a robust desired signal accompanied by no or low-level interferers. In this case, the noise floor **214** may be allowed to rise, while the maximum signal handling capability Smax **212** may be reduced. When this is done, the receiver circuit may save significant power. For example, the circuit's impedances may be increased, thus reducing required drive currents. Similarly, bias currents may be lowered, thus reducing the maximum signal in handling capability.

The minimum power dissipation for a circuit is proportional to the required maximum signal-to-noise ratio, which is the ratio between Smax **212** or **262** and N **214** or **264**. Thus, a circuit receiving an input similar to the one shown in FIG. **2**A can dissipate less power than one receiving the input as shown in FIG. **2**B, while still achieving an acceptable bit-error rate.

FIG. **3** illustrates what can occur when the maximum signal handling capability Smax **314** is reduced in the worst-case condition, that is when a weak desired signal **306** is accompanied by large interferers **310** and **312**. Again, signal strength is plotted along a Y-axis **304** as a function of frequency along X-axis **302**. In this specific example, Smax **314** is reduced below the peak levels of the interferers **310** and **312**. Since Smax is low, the circuit cannot handle the interferers linearly. The resulting nonlinearities lead to a mixing of the interferers and the creation of intermodulation products **308** (for example, a third-order intermodulation distortion, IM3), one of which in this example occurs at the same frequency as the desired signal **306**. As can be seen, if the intermodulation products **308** become excessive, the received signal bit error rate may become excessive, and the desired signal **306** may be lost. Accordingly, while Smax may be lowered even under some unfavorable conditions in order to reduce power, care should be taken to avoid corruption of the received desired signal.

FIG. **4** illustrates a portion of a receiver consistent with an embodiment of the present invention. Included is a filter **430**. An optional gain element **420** is placed in front of the filter **430** in order to increase signal levels. Signal strength indicator circuits **440** and **450** are connected to input line **410** and output line **460**. In this specific example, the input signal spectrum on line **410** is shown as desired signal **412** and interferers **414** and **416**. The signal spectrum at the output line **460** is shown as desired signal **462** and interferers **464** and **466**. The signal strength indicators **440** and **450** do not provide information as to the relative sizes of the desired and interfering signals. Rather, a cumulative signal level is provided at their outputs. For example, the first signal strength indicator **440** outputs a level corresponding to the sum of desired signal **412** and interfering signals **414** and **416**, while the second signal strength indicator **450** provides a signal level corresponding to the sum of desired signal **462** and interfering signals **464** and **466**. In this specific example,

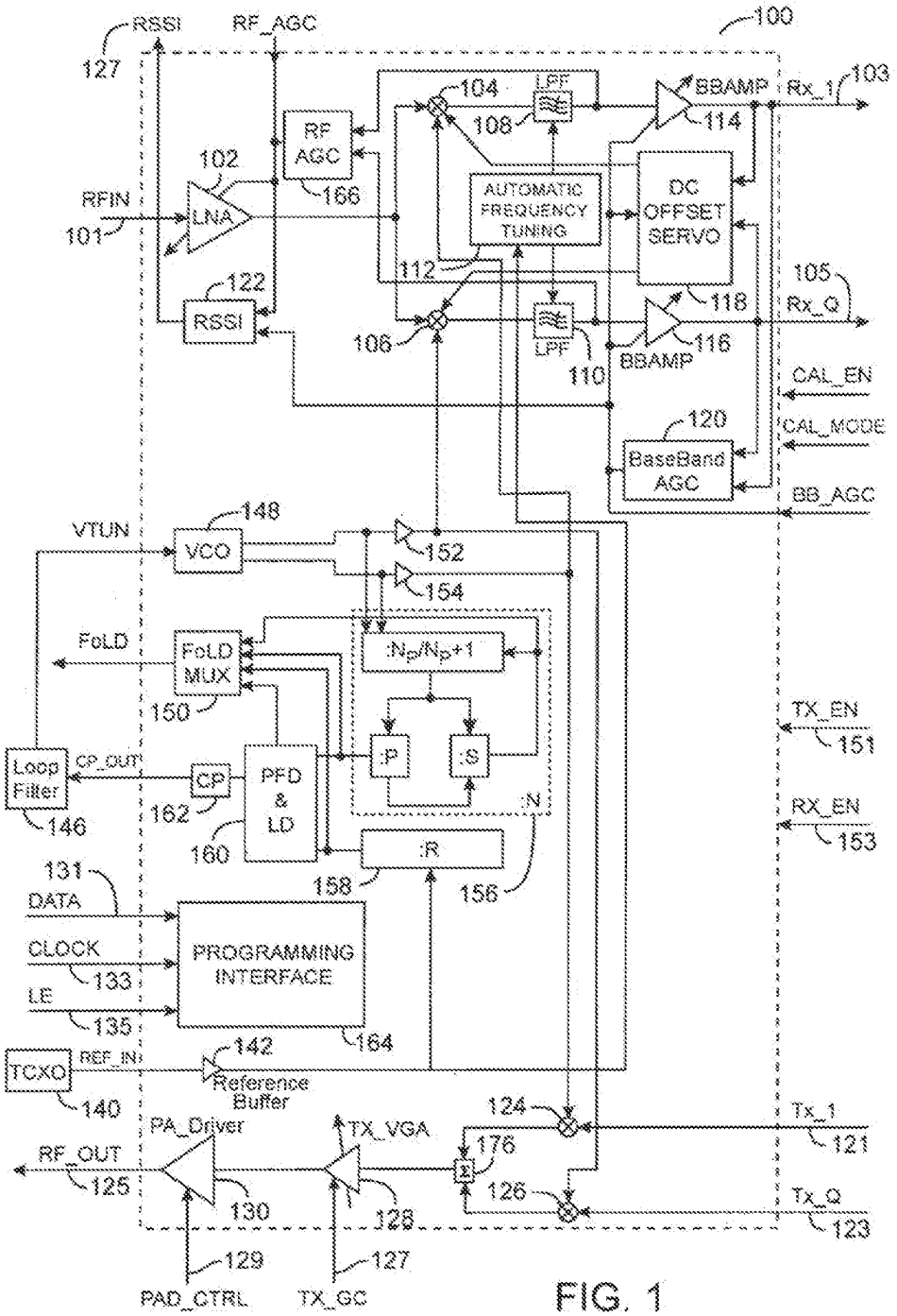

RSSI
127
RF_AGC
100
104
LPF
108
BBAMP
114
Rx_I
103
RF AGC
166
102
RFIN
101
LNA
AUTOMATIC FREQUENCY TUNING
DC OFFSET SERVO
112
118
105
Rx_Q
122
RSSI
106
LPF
110
BBAMP
116
CAL_EN
CAL_MODE
120
BaseBand AGC
BB_AGC
VTUN
148
VCO
152
154
FoLD
FoLD MUX
150
:Np/Np+1
:P
:S
:N
:R
158
156
Loop Filter
146
CP_OUT
CP
162
PFD & LD
160
131
DATA
CLOCK
133
LE
135
PROGRAMMING INTERFACE
164
TCXO
140
REF_IN
142
Reference Buffer
PA_Driver
TX_VGA
124
176
126
Tx_I
121
Tx_Q
123
RF_OUT
125
130
128
129
PAD_CTRL
127
TX_GC
TX_EN
151
RX_EN
153

FIG. 1

the gain of the gain and filter circuit combinations is shown as approximately one, while the interfering signals **414** and **416** signal levels are reduced.

A comparison of the signal levels provided by the signal strength indicators **440** and **450** indicates that much of the combined received signal on line **410** has been filtered. Accordingly, it may be deduced that large interfering signals present at the input are being filtered by the filter **430**. From this information, as will be shown in greater detail below, the bias, impedance, and gain of the gain stage **420** and filter **430** combination may be optimized to reduce power dissipation.

There are several real world situations where the received signal is better than the worst-case condition such that power can be saved. For example, large interferers may be present only part of the time, that is, on a temporary or transient basis. The interfering equipment may be some distance from the transceiver, or it may be operating in the low power mode. Also, the desired signal may be very strong as compared to the noise and interferers, for example a hub, router, or access point may be nearby.

Some transceivers consistent with embodiments of the present invention are designed to work with more than one data transfer specification or standard. In this case, when a transceiver is operating in a mode having a lower data rate, the power saving techniques described here may be employed.

FIG. **5** illustrates the relationship between a required biased current **516** for a given output signal **514** for a representative circuit **510**. If the output signal current level is relatively low, such as the output current shown as **526**, the corresponding bias current **528** may be low. Conversely, if the output signal current level is larger as with the example **536**, the corresponding bias current level **538** should also be high. Accordingly, if a bias current is initially set high to handle large a large input signal, for example a large interferer, this current may be reduced if the input signal is smaller.

There are many ways by which these bias currents can be reduced. For example, the current may be generated by placing a voltage across a resistor by applying a bias voltage to the base of a device whose emitter is connected to ground through a resistance. In this case, the resistor may be increased by opening switches across portions of the resistance, or lowering the bias voltage applied at the base. Several ways in which this may be done will be readily understood by one skilled in the art.

FIG. **6** is an example of how a circuit's impedances may be scaled to reduce drive currents, and, depending on the circuit configuration used, associated bias currents as well. A driver **612** has a load R **614** and C **616**. The frequency response of this circuit is the same as that seen by driver **622**, which drives an impedance of 2R **624** and C/2 **626**. But the impedance of the load seen by driver **622** is double that seen by **612**, thus the output current required by the driver **622** is reduced by one-half.

As an example, the output stage of each of these drivers may be a Class A emitter follower formed by an emitter follower connected to a current source. When the outputs are driven high, the emitter of driver **622** need supply only one-half the drive current as driver **612**. In this way, an impedance can be scaled in order to decrease a circuit's required drive current.

Also, the discharge current for driver **622** is only one half that of driver **612** for a given negative-going slew rate. Thus, the current source of **622** may be reduced by the same factor of one-half as compared to driver **612**. In this example, the bias current, that is the current in the pull-down current source can be reduced. Many other examples where drive currents and possibly bias currents may be reduced will be appreciated by one skilled in the art.

FIG. **7** illustrates another degree of freedom that made be employed to reduce current levels in a transceiver. Specifically, a gain element **720** may be inserted in front of a circuit block **730** in order to improve the combined circuit's signal-to-noise ratio by a factor equal to the gain of the inserted gain block. This is particularly useful when large interferers are absent and the desired received signal is moderate or low. Specifically, gain is added to the signal while impedances are increased, which raise the noise floor. In this way, a given signal-to-noise ratio may be maintained while the power is decreased.

The gain of such an element may be varied by increasing a current in a differential pair or increasing a load resistance using switches. Many other examples where the gain of this element may be varied will be appreciated by one skilled in the art.

These variables, or degrees of freedom, specifically reducing bias currents, increasing impedances, and increasing gain may be used as in the following examples.

FIG. **8**A is a block diagram of a functional block **820** and optional gain element **810** in accordance with an embodiment of the present invention. Functional block **820**, like the functional blocks in the following diagrams, may be a filter, mixer, amplifier, or other circuit or circuits in a wireless transceiver or other electronic circuits or system. An input signal is received on line **812** by the optional gain element **814**. When the optional gain block **810** is not used, the input signal may be received directly by the function block **820**. The gain of the optional gain element **812** is controlled by a gain control signal on line **814**. The functional block receives an output signal from the optional gain element **810** and provides an output VOUT on line **822**. The lines in this and the other included figures may be one or more lines, depending on whether single-ended, differential, or other type of signaling is employed.

One or more impedances are under control of signals on impedance control lines **824**. Similarly, one or more bias currents in the function block are under control of one or more signals on bias control lines **826**. These various control lines may be logic signals, analog signals, voltage or currents lines, or other signal or bias lines. In other embodiments of the present invention, the gain control element **810** may be included in the function block **820**. Also, various embodiments may not incorporate either or both the impedance control and bias control.

FIG. **8**B is an example input that may be present on line VIN **812**. In this example, a desired signal **836** is relatively weak, as are interfering signals **837** and **838**. The initial bias and circuit configuration is such that the noise floor **833** and maximum signal handling capability Smax **831** are adjusted for worst case conditions. The circuit of FIG. **8**A, as with all the circuits described here, receives noise at its input which may be referred to as input equivalent noise or input referred noise. Additionally, the circuit of FIG. **8**A generates noise which is added to the input referred noise. Depending on the gain characteristics of the circuitry, the output noise at various frequencies may be greater than, equal to, or less than the input referred noise. For simplicity, the noise floor and maximum signal handling capability Smax, in this and the other figures, are shown as straight lines, though the noise and Smax are typically curved as a function of frequency.

That the input spectrum is as shown in FIG. **8**B can be determined, for example, by low signal strength indications

on line VIN **812** and VOUT **822**. That is, a low level signal strength indication on line VIN **812** indicates that no portion of the input signal is particularly large.

For this exemplary input, there are at least two methods by which the power dissipation for this circuitry may be reduced. Depending on the exact circuits and structures used, one of these methods may be preferred.

In FIG. **8**C, the bias current is decreased, thereby lowering the maximum signal handling capability **841** as compared to **831**, closer to the desired and interfering signal levels. Again, the bias currents in the function block **820** may be reduced by switching impedances that appear across a voltage thereby changing a resulting bias current, by reducing a voltage at the gate of a MOS or base of a bipolar transistor, or by other methods.

In FIG. **8**D, a second method of reducing power dissipation in the function block **820** is employed. Specifically, Smax **851** is held constant as compared Smax **831**. The desired and interfering signals are amplified such that they are closer to the available signaling handling capability **851**. Also, the noise floor **853** is raised as compared to noise floor **833** in FIG. **8**B. Specifically, the noise contributed by the function block **820** is increased, such that the noise at its output is increased to noise floor **853**. This is done by increasing one or more impedance in function block **810**, such that drive currents inside that block are reduced. Depending on the exact configuration, this may also allow some biasing currents to be reduced, while maintaining the maximum signal handling capability **851** at a sufficient level. Alternately, these two methods of reducing power dissipation in function block **820** may be done in combination.

The included examples are explained for the exemplary situation where biasing and other parameters are set for worst-case conditions, and then changed to save power when it is discovered that the conditions are better-than-worst case. Alternately, the bias currents and other parameters may be set for maximum power savings, or an intermediate point, and the power can be adjusted from there.

FIG. **9**A illustrates a block diagram including an optional gain element **910** and function block **920**. Again, an input signal is received on line **912** by optional gain element **910** which in turn drives function block **920**. The function block provides an output VOUT on line **922**, and receives impedance and bias control signals on lines **924** and **926**.

FIG. **9**B shows the spectrum for what may be considered a best-case received signal. Specifically, the desired signal **936** is strong, while the interfering signals **937** and **938** are relatively weak. This may be determined, for example, by detecting a large signal level at the input line VIN **812** and a large signal level after a filter, since these readings would indicate that a large signal is received, but that it is at the desired signal frequency.

The maximum signaling capability **931** and noise floor **933** are shown as being set for the worst case conditions. In this case, the noise floor **933** is lower than the maximum allowed for proper signal reception. Accordingly, one or more impedance in the function block **920** may be increased, such that the noise floor **943** rises as shown in FIG. **9**C. In this way one or more of the driving currents in the function block **920** may be reduced. Similarly, since the drive current is reduced, one or more bias current may also be reduced, depending on the exact circuit configuration.

FIG. **10**A illustrates a block diagram showing an optional gain element **1010** driving a function block **1020**. An input signal is received by the gain element **1010** on line **1012**, and an output is provided by function block **1020** on line VOUT **1022**. One or more gain control signals present on lines **1014** control the gain of gain control element **1010**, while one or more impedance and bias control signals are received by the function block **1020** on line to **1024** and **1026**.

FIG. **10**B illustrates a received signal that may be received on line VIN **1012**. In this example, the desired signal **1036** and interferers **1037** and **1038** are each relatively large. This may be determined, for example, by detecting a large signal level at the input line VIN **812** and a smaller signal level after a filter, since these readings would indicate that a large signal is received, but that interferers are being reduced.

As before, in this example, the noise floor **1033** and maximum signal handling capability **1031** are initially set for the worst case conditions. Since the desired signal is relatively large in this case, the noise floor may be allowed to rise, a shown by noise floor **1043** in FIG. **10**C. Since the desired signal **1046** and interferers **1047** are large, the maximum signal handling capability Smax **1041** remains constant. Again, the noise floor is increased by increasing impedances in the function block **1020**. This reduces the required drive current, and may also allow for a reduction in bias currents.

FIG. **11**A illustrates a block diagram including an optional gain element **1110** and function block **1120** in accordance with an embodiment of the present convention. An input signal is received on line **1112** by the optional gain control element **1110**, while an output signal is provided by the function block **1120** on line VOUT **1122**. Gain, impedance, and bias control signals are received on lines **1114**, **1124**, and **1126**.

FIG. **11**B is an exemplary input signal that may be received by the gain control element **1110** on line VIN **1112**. In this specific example, the desired signal **1136** is relatively low or weak while the interfering signals **1137** and **1138** are large. This may be determined, for example, by detecting a large signal level at the input line VIN **812** and a much smaller signal level after a filter, since these readings would indicate that a large signal is received and that large interferers are being reduced such that the resulting signal, the desired signal, is relatively weak.

Again, the maximum signal handling capability **1131** and noise floor **1133** are initially set for worst case conditions. If the desired signal is sufficiently low, while the interferers are sufficiently high, power savings may not be achievable over the worst case settings, since this is in fact the worst case condition. But, if the desired signal is somewhat larger than the worst case condition, then power may be saved in at least two different ways.

For example, FIG. **11**C shows the maximum signal handling capability **1141** being lowered. In this case, the interfering signals **1147** in **1148** began to clip and distort, thereby creating intermodulation products **1145**, which distort the desired signal **1146**. So long as care is taken to not corrupt the desired signal **1146** beyond an acceptable limit, typically measured by a bit-error rate, power may be reduced in this way.

Similarly, in FIG. **11**D, the noise floor **1153** is raised somewhat, thereby saving power. Again, this may be done so long as the noise floor is not sufficiently high that the system bit-error rate becomes unacceptable.

FIG. **12** is a summary of the above four examples. The received signal strengths are shown in column **1210**, while appropriate power saving responses are listed in column **1220**. Specifically, in row **1230**, the desired signal and interferer signal strengths are both weak or small. In this case, proper responses include decreasing Smax, or increasing one or more circuit impedances while increasing the circuit gain. Depending on the exact circuit configuration,

one of these options may be preferred over the other. Alternately, they may be done in combination, or done in combination with other power saving techniques. Also, in some specific embodiments, when both desired signal and interferer signal strengths are small, the gain may need to be increased while the impedance is maintained or not increased in order to keep the noise floor low.

In row **1240**, the desired signal strength is strong or large, while the interfering signals are small. In this case, an appropriate response is to increase one or more of the circuit impedances. Again, depending on the exact circuit in question, one or more of the bias currents may also be reduced.

In row **1250**, both the desired signals and interfering signal strengths are large. Again, in this case an appropriate response is to increase one or more of the circuit impedances.

In row **1260**, the received desired signal strength is weak or small, while the interfering signals are large. Since this is the worst case situation for which the circuit is designed, substantial power savings are difficult to achieve. However, again, if the received signal is above a minimum level necessary for proper operation, some distortion of the interferers or raising of the noise floor may be acceptable.

It should be noted that not all possible signal conditions are listed here. For example, either the signal or interferer may be of a relatively medium strength, or the interferer may be absent. Also, these terms are for exemplary purposes and are not meant to convey specific signal conditions, but rather are only qualitative. The proper response to a specific condition depends on the embodiment of the present invention, the particular circuit topology, the requirements of the signaling standard used, as well as other constraints.

FIG. **13** is an example shown how power may be saved as a function of time by employing one or more of these methods consistent with embodiments of the present invention. Power is plotted along a Y-axis **1304** as a function of time along X-axis **1302**. Conventional worst case design would fix power dissipation at line **1310**. As can be seen, dynamic power dissipation **1320** under the control of variable gains, impedances, biasing, or combination thereof, allows for a lower average power **1330** as compared to the power dissipated **1310** by the conventional design.

FIG. **14** is a block diagram of a portion of a receiver consistent with an embodiment of the present invention. Included are low-noise amplifier **1410**, mixer **1420**, gain stage **1430**, filter **1440**, AGC amplifier **1450**, and VCO **1460**. Signal strength detection is done at the output of the low-noise amplifier by signal strength indicator **1470**, at the output of the mixer by signal strength indicator **1472**, and at the output of the filter by signal strength indicator **1474**. The outputs of the signal strength indicator circuits are received by the computational circuit **1470**, which in turn controls gain and power control circuits **1480** and **1485**. Power and gain control circuits **1480** and **1485** control the gain, biasing, and impedance levels of the circuits in the receiver signal path. Also, the gain and power control circuits may control the same parameters in the VCO **1460**. This figure is greatly simplified for purposes of explanation. For example, the quadrature nature of the mixers and following circuits are not shown. Also, power-down and start-up circuits are not included.

The current level in the low-noise amplifier determines a multitude of parameters including voltage gain, linearity, input impedance matching, and noise figure. When conditions are better than worst-case, some of these parameters may be relaxed while maintaining an acceptable bit-error rate, thus saving power.

The bias current in the mixers effect that block's noise figure and linearity. Care is taken in reducing power in this block so as not to increase nonlinearities, particularly the third-order nonlinearity as measured by IP3, the third-order intercept point, beyond an acceptable limit.

A key parameter of the VCO is phase noise, an increase in which increases the sidebands on either side of the oscillation signal. During transmission, the phase noise should be kept low to avoid interference with adjacent channels and for preserving modulation information.

During reception however, if the conditions are better than worst case, the phase noise requirement for the VCO is relaxed, and power can be saved consistent with embodiments of the present invention. The achievable phase noise power spectral density is approximately inversely proportional to the bias current used. Thus, when low phase noise is not required during reception, bias current in the VCO can be reduced.

Most of the power savings in a transceiver in accordance with embodiments of the present invention is achieved in the receiver portion. Additional power may be saved in the transmitter section.

FIG. **15** is a block diagram of a transmitter portion consistent with an embodiment of the present invention. Included is a signal path formed by gain stage **1510** and power amplifier **1520**. The output power level is sensed by output level sensing circuit **1550**, which in turn adjusts the biasing of the power amplifier **1520** through the power control circuit **1540**. Additionally, a transmitter level control signal is received by power control circuits **1530** and **1540**, which in turn control the biasing of gain stage **1510** and power amplifier **1520**. Gain control circuit **1560** also adjusts the gain of gain stage **1510** and power amplifier **1520**. Additional circuitry that varies impedances in each of these circuits may also be included.

Since the gain, impedance and biasing of these blocks are being dynamically varied, care must be taken to not negatively affect the signal being processed. For example, specific embodiments of the present invention perform some or all of these variations during preamble. Also, as changes occur, the circuits in some embodiments are limited such that they may only adapt to an improvement in conditions after frames are completed. If conditions worsen, the circuits may be allowed to change in order to save the data. Alternately, a system may be manually calibrated, for example at set up, and when the network configuration is changed.

The above description of specific embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form described, and many modifications and variations are possible in light of the teaching above. The embodiments were chosen and described in order to best explain the principles of the invention and its practical applications to thereby enable others skilled in the art to best utilize the invention in various embodiments and with various modifications as are suited to the particular use contemplated.

What is claimed is:

1. A method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, and a corresponding increase in battery life of the battery powered portable wireless device, the method comprising:

receiving a wireless signal having a desired signal and an interferer signal, by the wireless transceiver of the battery powered portable wireless device, the wireless

transceiver having a receiver signal path comprising a plurality of circuits, wherein the plurality of circuits includes an amplifier, a filter, and a mixer, and wherein the wireless transceiver comprises a circuit for determining a signal strength of the interferer signal and a circuit for determining a signal strength of the desired signal;

wherein a worst-case power dissipation condition results when the signal strength of the desired signal is low and the signal strength of the interferer signal is high; and

wherein the power dissipation reduction in the receiver is achieved by causing a bias current to vary in one or more of the plurality of circuits in the receiver signal path of the wireless transceiver as the signal strength of the interferer signal and the signal strength of the desired signal vary according to the following:

(i) when the signal strength of the interferer signal is high and the signal strength of the desired signal is low, and the desired signal is larger than in the worst-case power dissipation condition, causing the bias current of the one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be reduced compared to the worst-case power dissipation condition, thereby saving power; and

(ii) when the signal strength of the interferer signal is weak and the signal strength of the desired signal is weak, causing the bias current of the one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be decreased compared to the worst-case power dissipation condition, thereby saving power.

2. The method of claim 1, wherein the change in the bias current of the one or more of the plurality of circuits in the receiver signal path is related to a change in an impedance in the one or more of the plurality of circuits in the receiver signal path and wherein the impedance comprises at least a resistor and a capacitor.

3. A method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, and a corresponding increase in battery life of the battery powered portable wireless device, the method comprising:

receiving a wireless signal having a desired signal and an interferer signal, by the wireless transceiver of the battery powered portable wireless device, the wireless transceiver having a receiver signal path comprising a plurality of circuits, wherein the plurality of circuits includes an amplifier, a filter, and a mixer, and wherein the wireless transceiver comprises a circuit for determining a signal strength of the interferer signal and a circuit for determining a signal strength of the desired signal;

wherein a worst-case power dissipation condition from the battery results when the signal strength of the desired signal is low and the signal strength of the interferer signal is high; and

wherein the power dissipation reduction in the receiver is achieved by causing a bias current to vary in one or more of the plurality of circuits in the receiver signal path of the wireless transceiver as the signal strength of the interferer signal and the signal strength of the desired signal vary, according to the following:

when the signal strength of the interferer signal is high and the signal strength of the desired signal is low, and the desired signal has a signal strength that is larger than in the worst-case power dissipation conditions, causing the bias current of the one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be decreased compared to the worst-case power dissipation condition, causing a reduction in power dissipation.

4. The method of claim 3, wherein the change in the bias current of the one or more of the plurality of circuits in the receiver signal path is related to a change in an impedance in the one or more of the plurality of circuits in the receiver signal path;

and wherein the impedance comprises at least a resistor and a capacitor.

5. A method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, and a corresponding reduction in a drain on battery life of the battery powered portable wireless device, the method comprising:

receiving a wireless signal having a desired signal and an interferer signal, by the wireless transceiver of the battery powered portable wireless device, the wireless transceiver having a receiver signal path comprising a plurality of circuits, wherein the plurality of circuits includes an amplifier, a filter, and a mixer, and wherein the wireless transceiver comprises a circuit for determining a signal strength of the interferer signal and a circuit for determining a signal strength of the desired signal;

wherein a worst-case power dissipation condition results when the signal strength of the desired signal is low and the signal strength of the interferer signal is high; and

wherein the power dissipation reduction in the receiver is achieved by causing a bias current to vary in one or more of the plurality of circuits in the receiver signal path of the wireless transceiver as the signal strength of the interferer signal and the signal strength of the desired signal vary, according to the following:

(i) when the signal strength of the interferer signal is high and the signal strength of the desired signal is weak, and the desired signal is larger than in the worst-case power dissipation condition, causing the bias current of the one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be reduced compared to the worst-case power dissipation condition, thereby saving power;

(ii) when the signal strength of the interferer signal is high and the signal strength of the desired signal is high, causing the bias current of the one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be decreased compared to the worst-case power dissipation condition, thereby saving power;

(iii) when the signal strength of the interferer signal is weak and the signal strength of the desired signal is weak, causing the bias current of the one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be decreased compared to the worst-case power dissipation condition, thereby saving power; and

(iv) when the signal strength of the interferer signal is weak and the signal strength of the desired signal is high, causing the bias current of the one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be decreased compared to the worst-case power dissipation condition, thereby saving power.

6. The method of claim 5, wherein the change in the bias current of the one or more of the plurality of circuits in the

receiver signal path is related to a change in an impedance in the one or more of the plurality of circuits in the receiver signal path;

and wherein the impedance comprises at least a resistor and a capacitor.

7. A method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, and a corresponding reduction in a drain on battery life of the battery powered portable wireless device, the method comprising:

receiving a wireless signal having a desired signal and an interferer signal, by the wireless transceiver of the battery powered portable wireless device, the wireless transceiver having a receiver signal path comprising a plurality of circuits, wherein the plurality of circuits includes an amplifier, a filter, and a mixer, and wherein the wireless transceiver comprises a circuit for determining a signal strength of the interferer signal and a signal strength of the desired signal in the receiver signal path;

wherein a worst-case power dissipation condition in the receiver results when the signal strength of the desired signal is low and the signal strength of the interferer signal is high; and

wherein the power dissipation reduction is achieved by causing an impedance and a bias current of one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to vary as the signal strength of the interferer signal and the signal strength of the desired signal to vary according to the following:

(i) when the signal strength of the interferer signal is high and the signal strength of the desired signal is low and the desired signal is larger than in the worst-case power dissipation conditions, causing the bias current of the circuit in the receiver signal path of the wireless transceiver to be reduced compared to the worst-case power dissipation condition, causing a reduction in power dissipation;

(ii) when the signal strength of the interferer signal is high and the signal strength of the desired signal is high, causing the impedance of the circuit in the receiver signal path of the wireless transceiver to be increased compared to the worst-case power dissipation condition, causing a reduction in power dissipation;

(iii) when the signal strength of the interferer signal is low and the signal strength of the desired signal is low, causing the bias current of the circuit in the receiver signal path of the wireless transceiver to be reduced compared to the worst-case power dissipation condition, causing a reduction in power dissipation;

(iv) when the signal strength of the interferer signal is low and the signal strength of the desired signal is high, causing the impedance of the circuit in the receiver signal path of the wireless transceiver to be increased compared to the worst-case power dissipation condition, causing a reduction in power dissipation; and

wherein increasing the impedance of the circuit reduces a drive current of the circuit and reduces the associated bias current of the circuit.

8. A method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, and a corresponding reduction in power dissipation and an increase in battery life of the battery powered portable wireless device, the method comprising:

receiving a wireless signal having a desired signal and an interferer signal, by the wireless transceiver of the battery powered portable wireless device, the wireless transceiver having a receiver signal path comprising a plurality of circuits, wherein the plurality of circuits includes an amplifier, a filter, and a mixer, and wherein the wireless transceiver comprises a circuit for determining a signal strength of the interferer signal and a circuit for determining a signal strength of the desired signal;

wherein a worst-case power dissipation condition from the battery results when the signal strength of the desired signal is low and the signal strength of the interferer signal is high; and

wherein the power dissipation reduction in the receiver is achieved by causing a bias current and an impedance to vary in one or more of the plurality of circuits in the receiver signal path of the wireless transceiver as the signal strength of the interferer signal and the signal strength of the desired signal vary, according to the following:

when the signal strength of the interferer signal is high and the signal strength of the desired signal is low, and the desired signal has a signal strength that is larger than in the worst-case power dissipation condition, causing:

(i) the bias current of the one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be decreased; and

(ii) an impedance of the one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be increased, thereby causing a drive current of the one or more of the plurality of circuits to be decreased.

* * * * *

Exhibit C

US010524202B2

(12) **United States Patent**
Tsividis

(10) **Patent No.: US 10,524,202 B2**
(45) **Date of Patent: *Dec. 31, 2019**

(54) **POWER DISSIPATION REDUCTION IN WIRELESS TRANSCEIVERS**

(71) Applicant: **Theta IP, LLC**, Coppell, TX (US)

(72) Inventor: **Yannis Tsividis**, New York, NY (US)

(73) Assignee: **THETA IP, LLC**, Coppell, TX (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **15/824,841**

(22) Filed: **Nov. 28, 2017**

(65) **Prior Publication Data**

US 2018/0084492 A1 Mar. 22, 2018

Related U.S. Application Data

(63) Continuation of application No. 15/080,421, filed on Mar. 24, 2016, now Pat. No. 9,838,962, which is a (Continued)

(51) **Int. Cl.**
H04B 1/38 (2015.01)
H04M 1/00 (2006.01)
(Continued)

(52) **U.S. Cl.**
CPC ***H04W 52/0209*** (2013.01); ***H04B 1/109*** (2013.01); *Y02D 70/00* (2018.01); *Y02D 70/142* (2018.01); *Y02D 70/40* (2018.01)

(58) **Field of Classification Search**
CPC H04B 1/16; H04B 1/1607; H04B 1/40; H04B 17/318; H04W 52/52; H03F 1/56;
(Continued)

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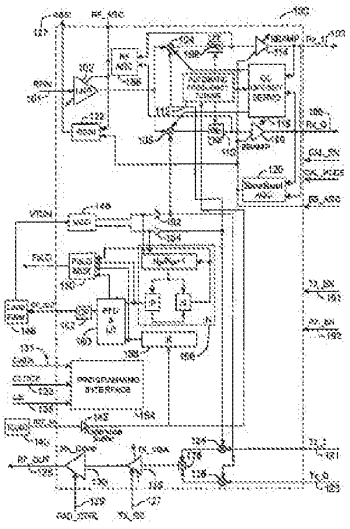
US 6,529,069 B2, 03/2003, Krishnapura et al. (withdrawn)
(Continued)

Primary Examiner — Quochien B Vuong
(74) *Attorney, Agent, or Firm* — Jennifer Hayes; Nixon Peabody LLP

(57) **ABSTRACT**

Methods and circuits for reducing power dissipation in wireless transceivers and other electronic circuits and systems. Embodiments of the present invention use bias current reduction, impedance scaling, and gain changes either separately or in combination to reduce power dissipation. For example, bias currents are reduced in response to a need for reduced signal handling capability, impedances are scaled thus reducing required drive and other bias currents in response to a strong received signal, or gain is increased and impedances are scaled in response to a low received signal in the presence of no or weak interfering signals.

23 Claims, 15 Drawing Sheets



Related U.S. Application Data

continuation of application No. 11/318,646, filed on Dec. 27, 2005, now Pat. No. 9,331,728, which is a continuation of application No. 10/784,613, filed on Feb. 23, 2004, now Pat. No. 7,010,330.

(60) Provisional application No. 60/451,229, filed on Mar. 1, 2003, provisional application No. 60/451,230, filed on Mar. 1, 2003.

(51) **Int. Cl.**
H04W 52/02 (2009.01)
H04B 1/10 (2006.01)

(58) **Field of Classification Search**
CPC ... H03F 3/20; H03F 2200/27; H03F 2200/78; H03F 2200/387; H03F 2200/451
USPC 455/63.1, 67.13, 127.1, 127.2, 127.5, 455/226.1, 226.2, 232.1, 234.1, 250.1, 455/251.1, 295, 296, 311, 343.1, 572, 455/574; 370/442; 330/127, 134, 144
See application file for complete search history.

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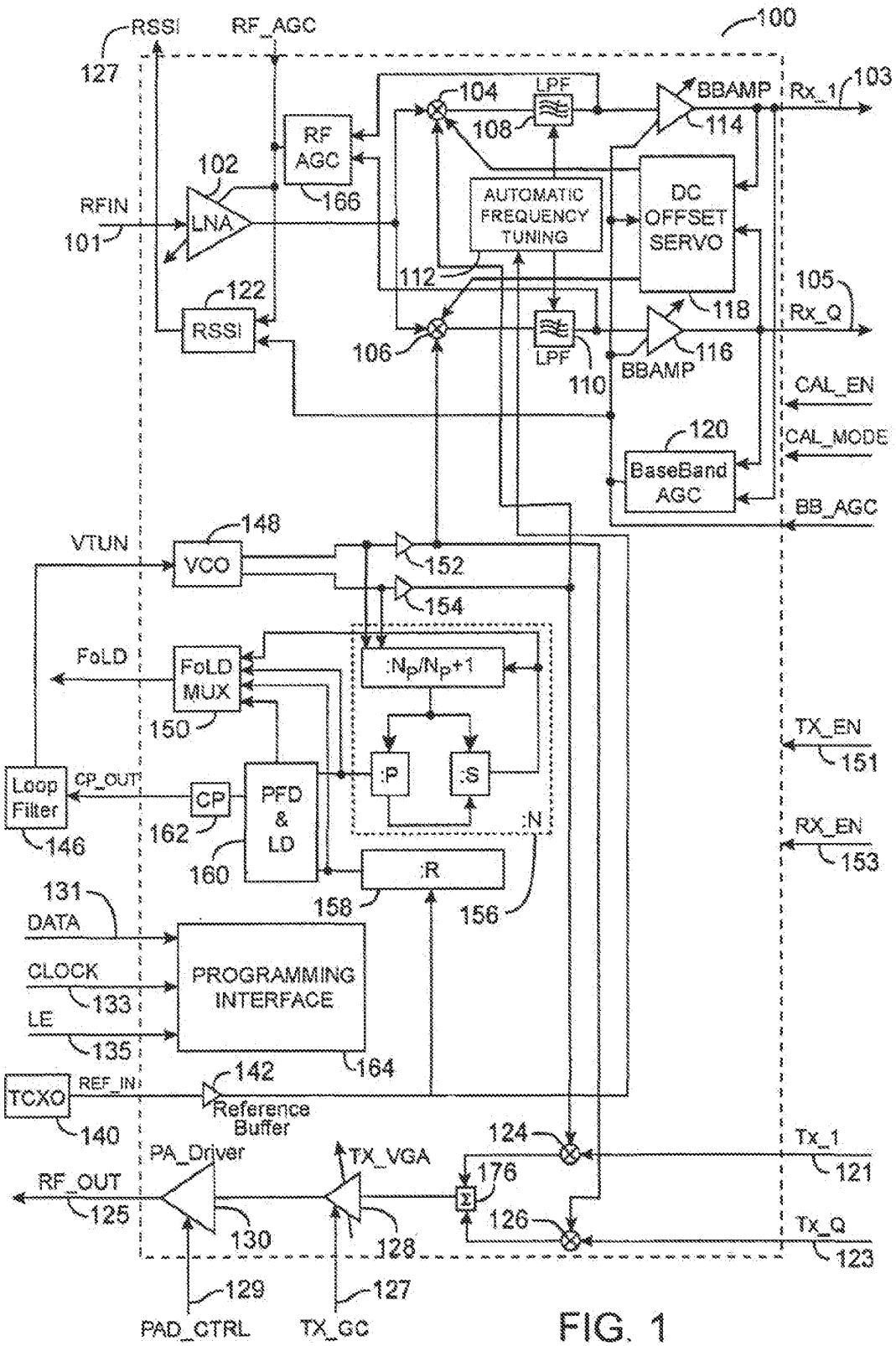

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104
LPF
BBAMP
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108
114
RF AGC
166
102
AUTOMATIC FREQUENCY TUNING
DC OFFSET SERVO
RFIN
101
LNA
112
118
105
Rx_Q
122
RSSI
106
LPF
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BBAMP
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CAL_EN
CAL_MODE
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BaseBand AGC
BB_AGC
VTUN
148
VCO
152
154
FoLD
FoLD MUX
150
:Np/Np+1
TX_EN
151
Loop Filter
146
CP_OUT
CP
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PFD & LD
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:P
:S
:N
RX_EN
153
:R
158
156
131
DATA
CLOCK
133
LE
135
PROGRAMMING INTERFACE
164
TCXO
140
REF_IN
142
Reference Buffer
124
Tx_1
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PA_Driver
TX_VGA
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PAD_CTRL
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TX_GC

FIG. 1

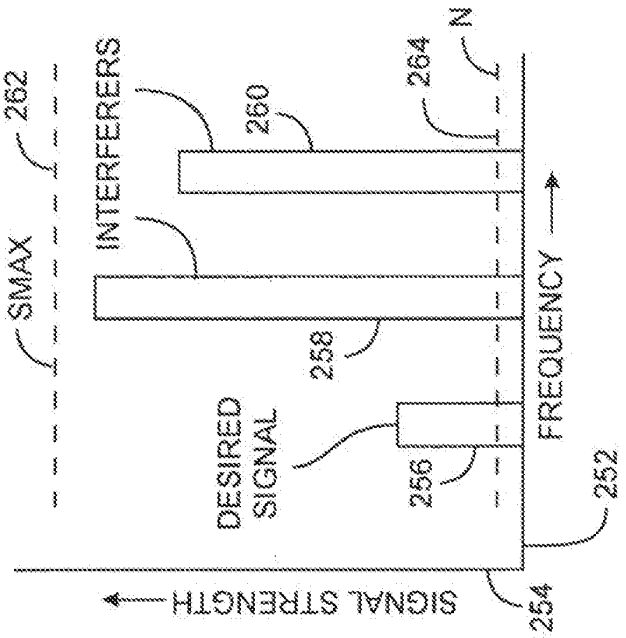

SMAX
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264
N
258
DESIRED SIGNAL
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FREQUENCY
252
SIGNAL STRENGTH
254

FIG. 2B

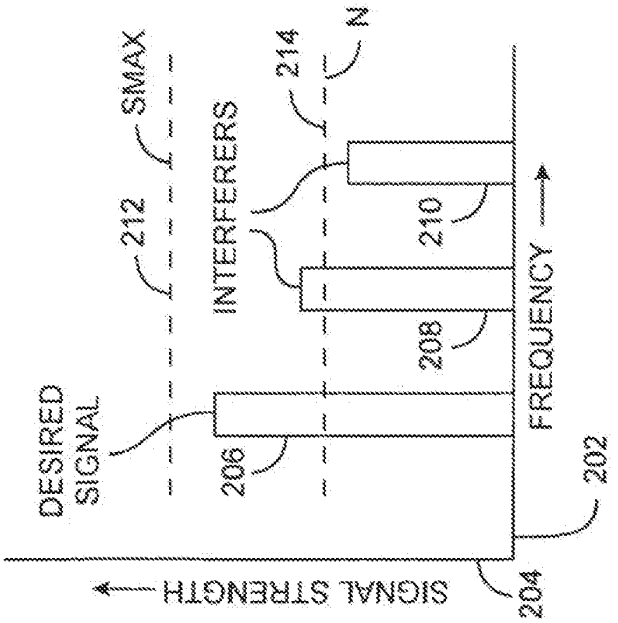

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INTERFERERS
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DESIRED SIGNAL
206
FREQUENCY
202
SIGNAL STRENGTH
204

FIG. 2A

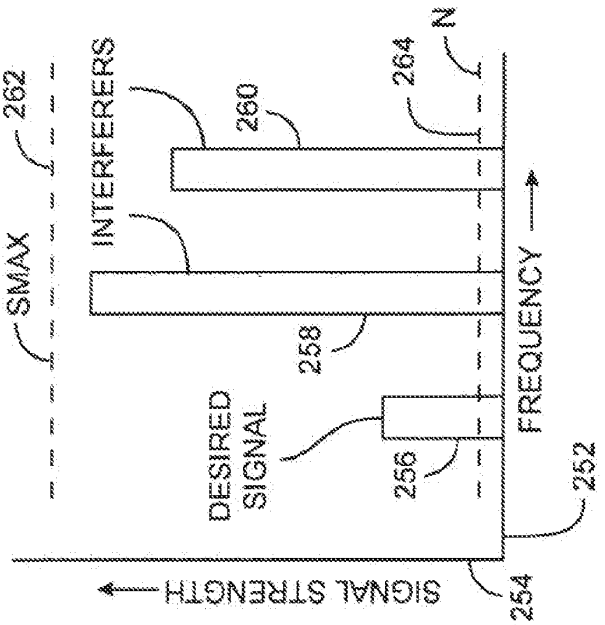

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DESIRED SIGNAL
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254
SIGNAL STRENGTH
FREQUENCY

FIG. 2B

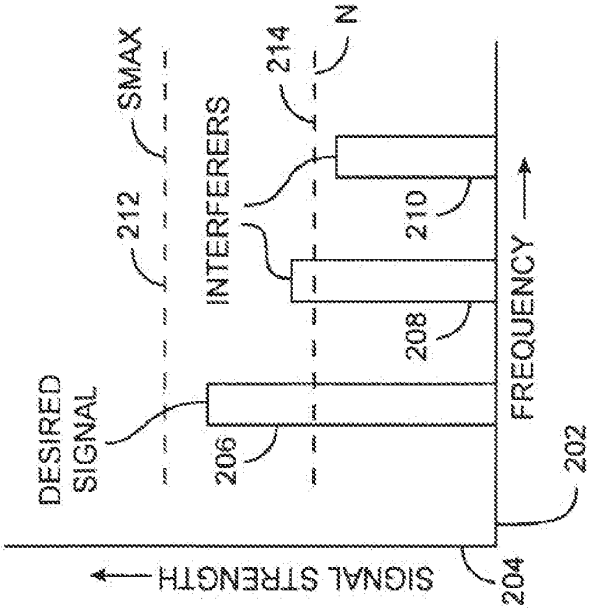

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SIGNAL STRENGTH
FREQUENCY

FIG 2A

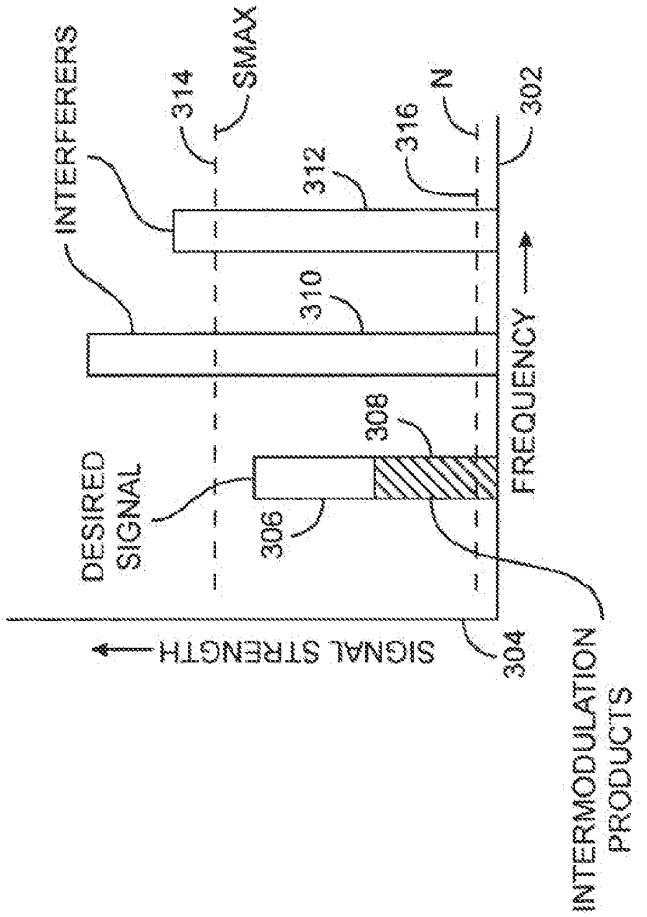

INTERFERERS
314
SMAX
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N
302
310
FREQUENCY
308
DESIRED SIGNAL
306
SIGNAL STRENGTH
304
INTERMODULATION PRODUCTS

FIG. 3

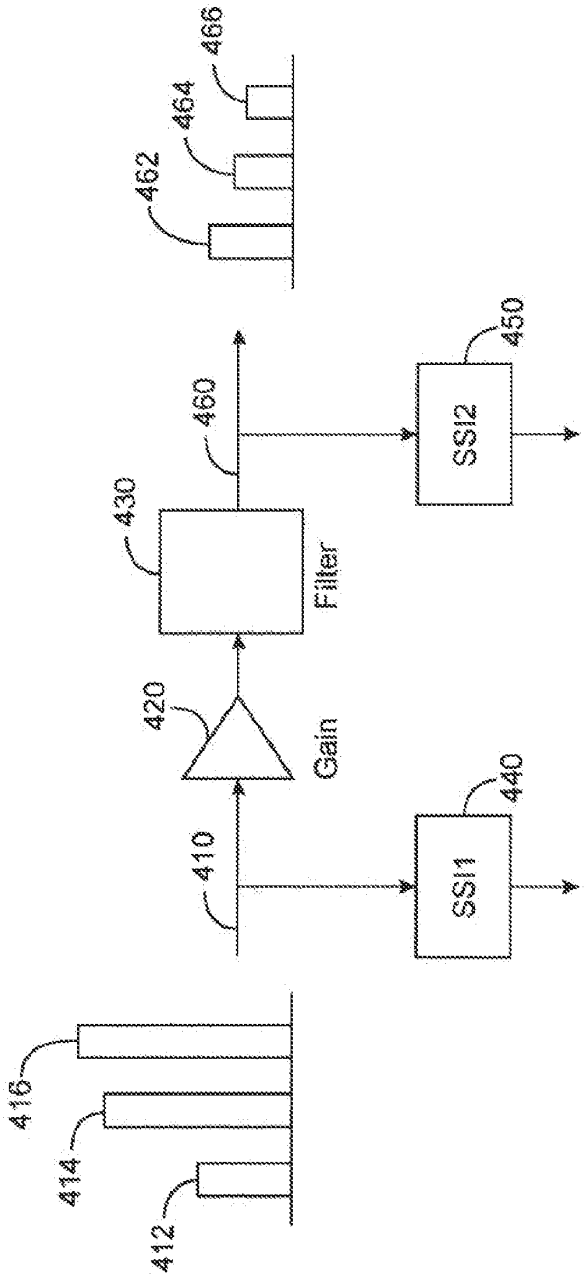

466
464
462
460
450
SSI2
430
Filter
420
Gain
410
440
SSI1
416
414
412

FIG. 4

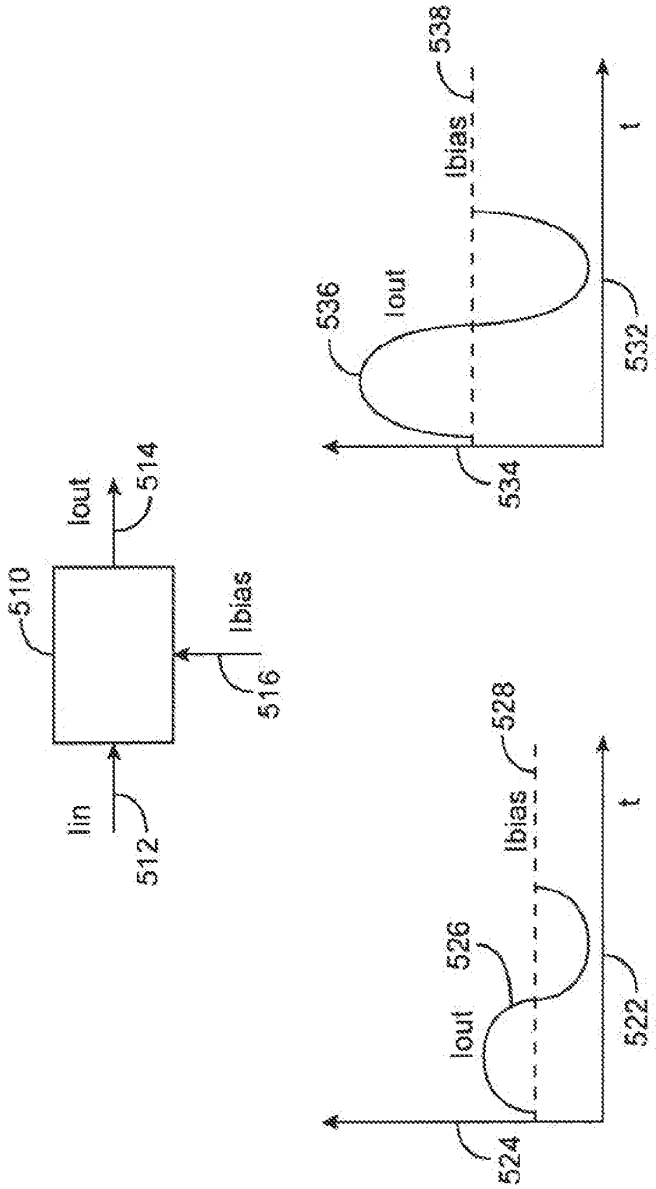

510
Iin
512
Iout
514
Ibias
516
524
Iout
526
Ibias
528
522
t
534
Iout
536
Ibias
538
532
t

FIG 5

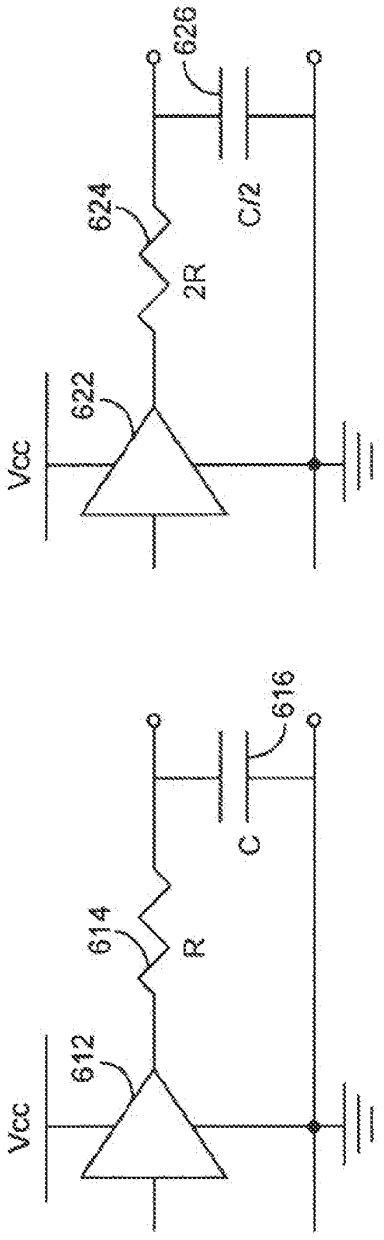


FIG 6

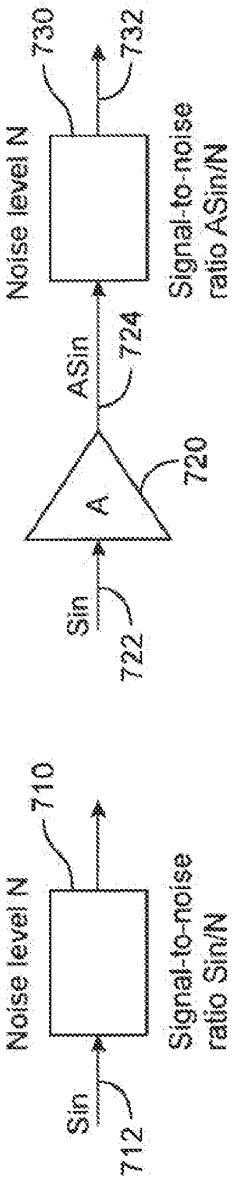

730
732
Noise level N
Signal-to-noise ratio ASin/N
ASin
724
720
A
Sin
722
710
Noise level N
Signal-to-noise ratio Sin/N
Sin
712

FIG. 7

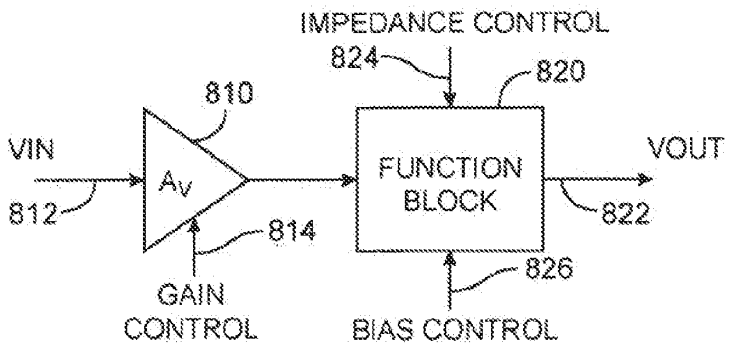


FIG. 8A

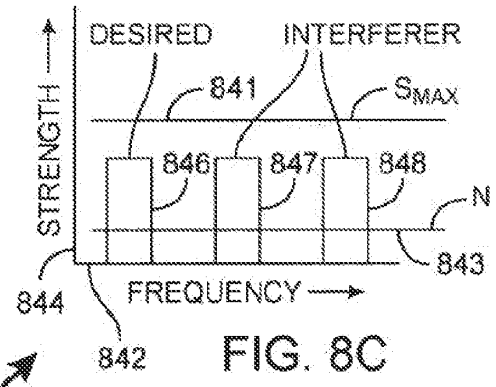


FIG. 8C

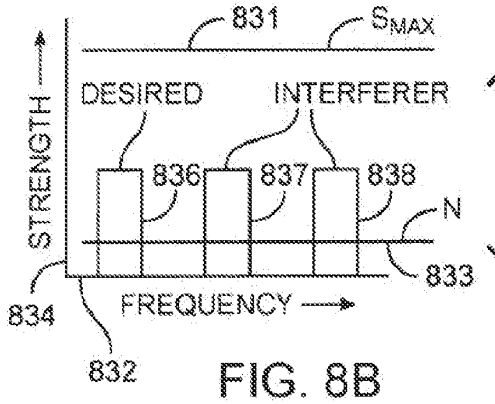


FIG. 8B

DECREASE BIASING

– AND/OR –

INCREASE GAIN AND IMPEDANCES

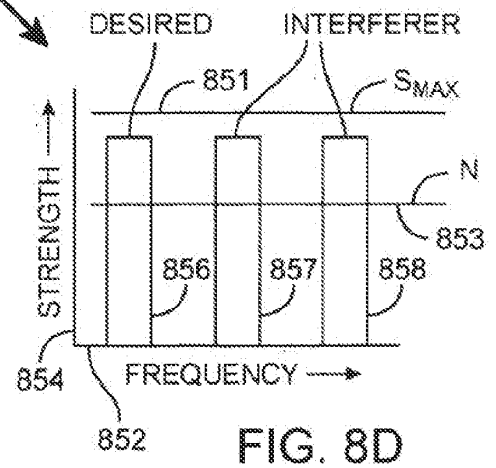


FIG. 8D

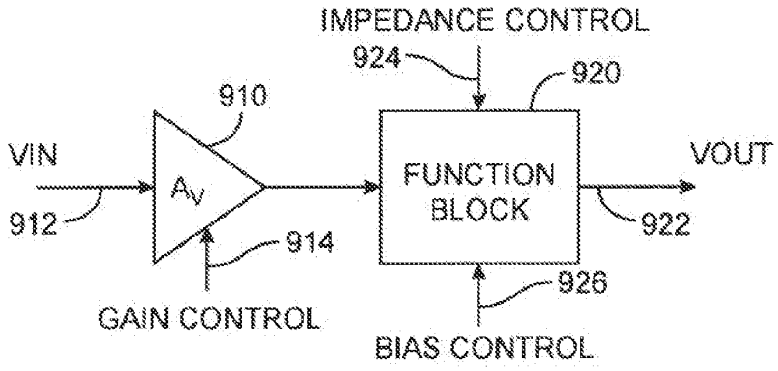


FIG. 9A

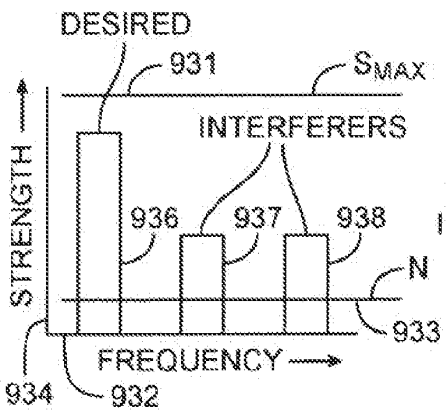


FIG. 9B

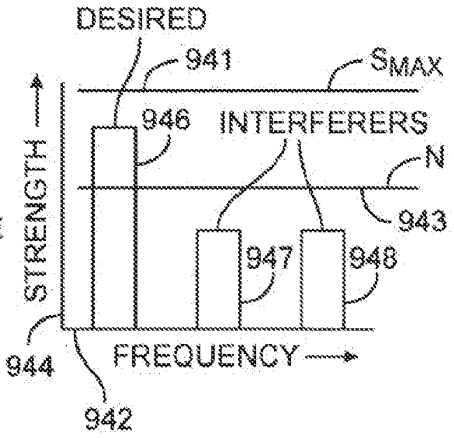


FIG. 9C

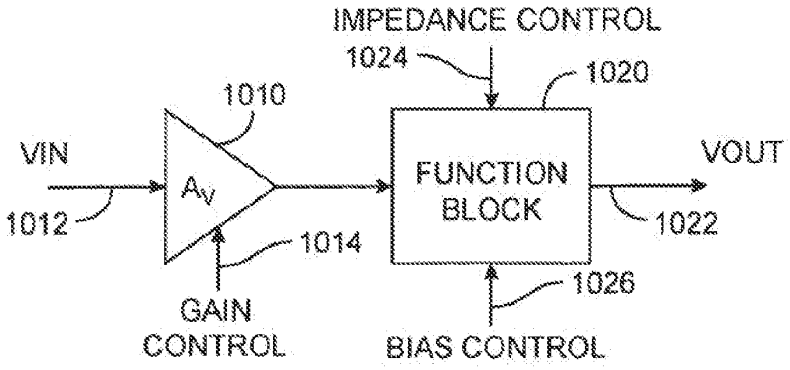


FIG. 10A

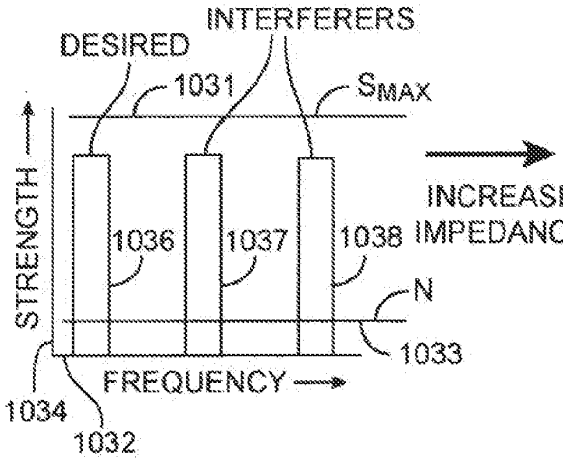


FIG. 10B

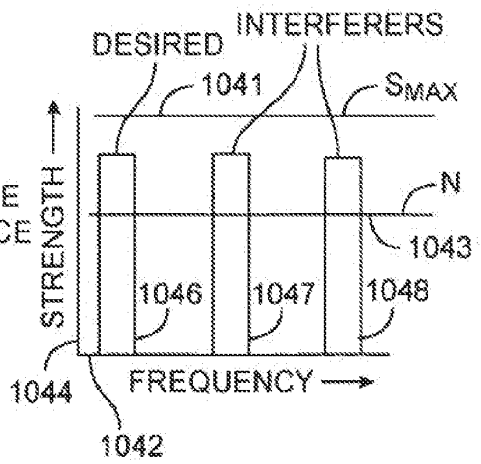


FIG. 10C

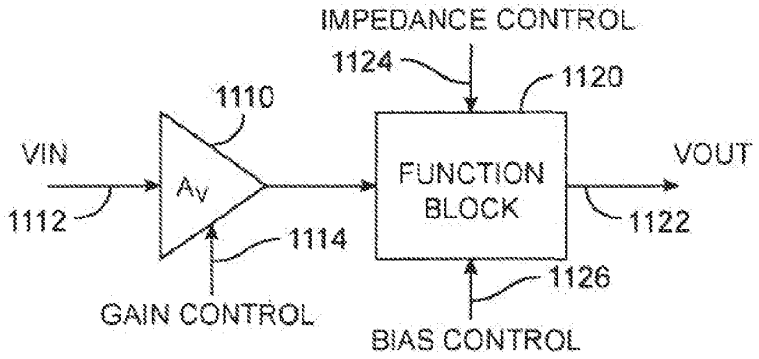


FIG. 11A

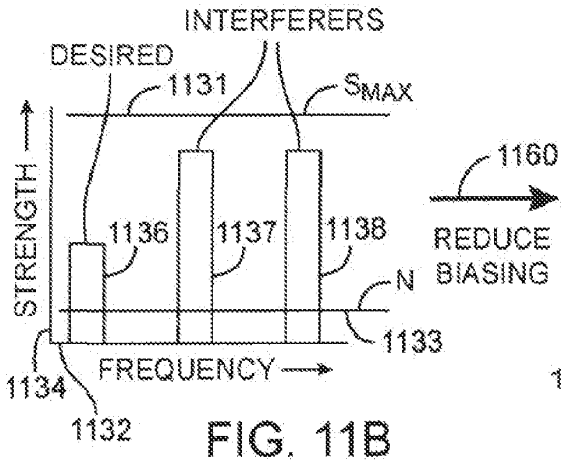


FIG. 11B

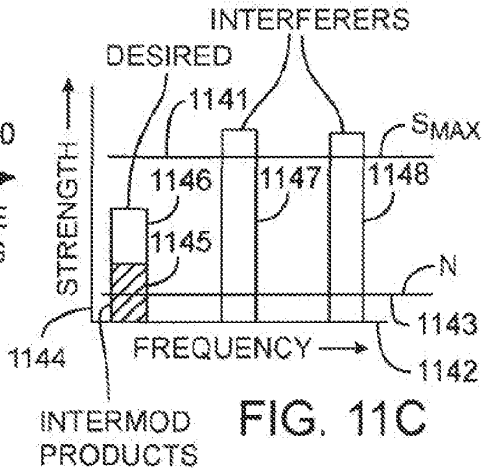


FIG. 11C



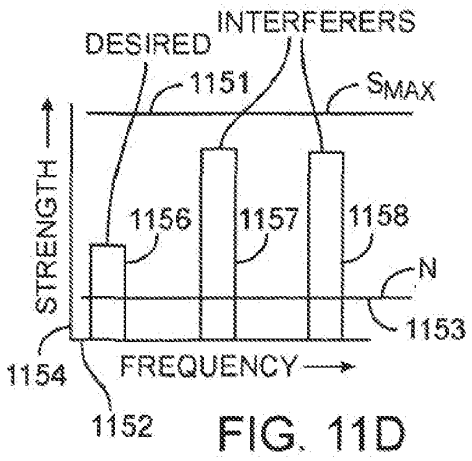


FIG. 11D

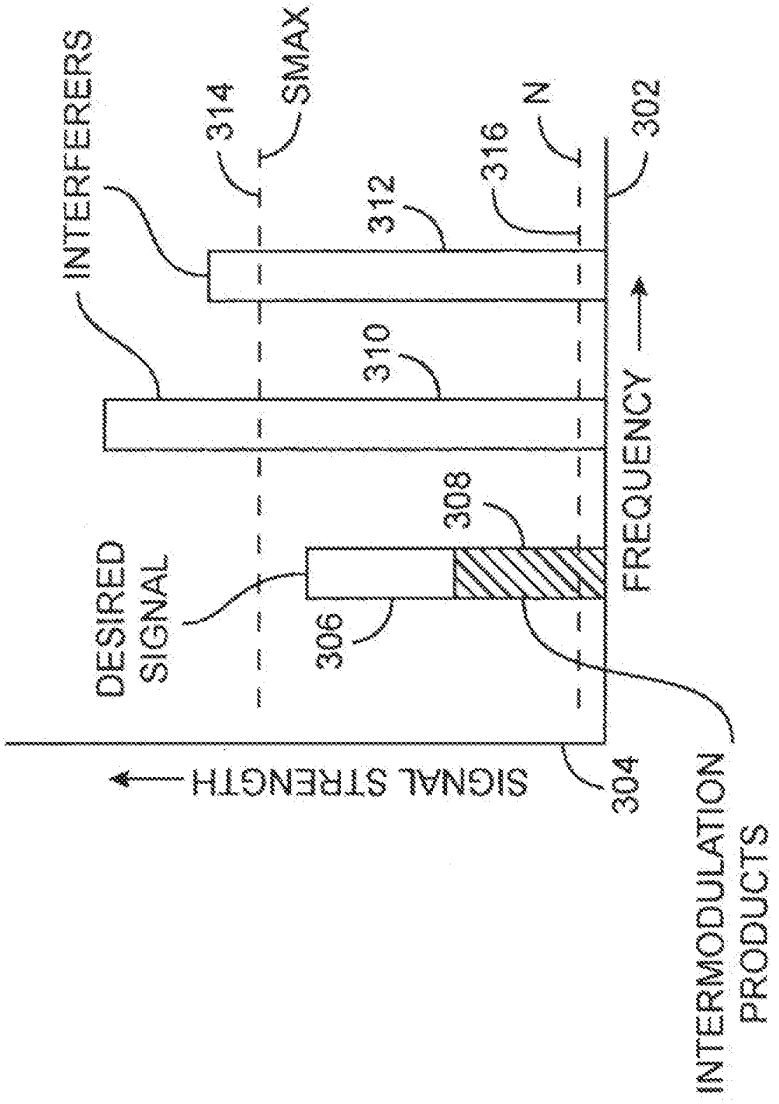

INTERFERERS
314
SMAX
312
316
N
302
310
308
DESIRED SIGNAL
306
FREQUENCY
SIGNAL STRENGTH
304
INTERMODULATION PRODUCTS

FIG. 3

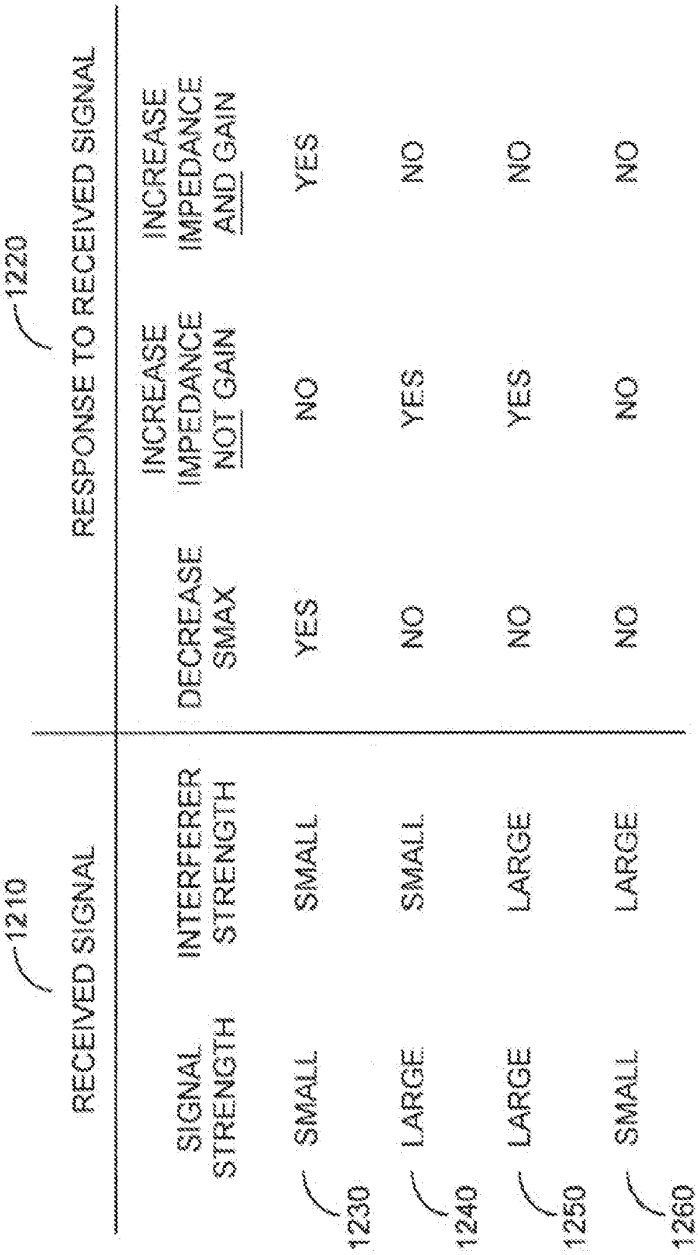

1210
RECEIVED SIGNAL
1220
RESPONSE TO RECEIVED SIGNAL
SIGNAL STRENGTH
INTERFERER STRENGTH
DECREASE SMAX
INCREASE IMPEDANCE NOT GAIN
INCREASE IMPEDANCE AND GAIN
SMALL
SMALL
YES
NO
YES
1230
LARGE
SMALL
NO
YES
NO
1240
LARGE
LARGE
NO
YES
NO
1250
SMALL
LARGE
NO
NO
NO
1260

FIG. 12

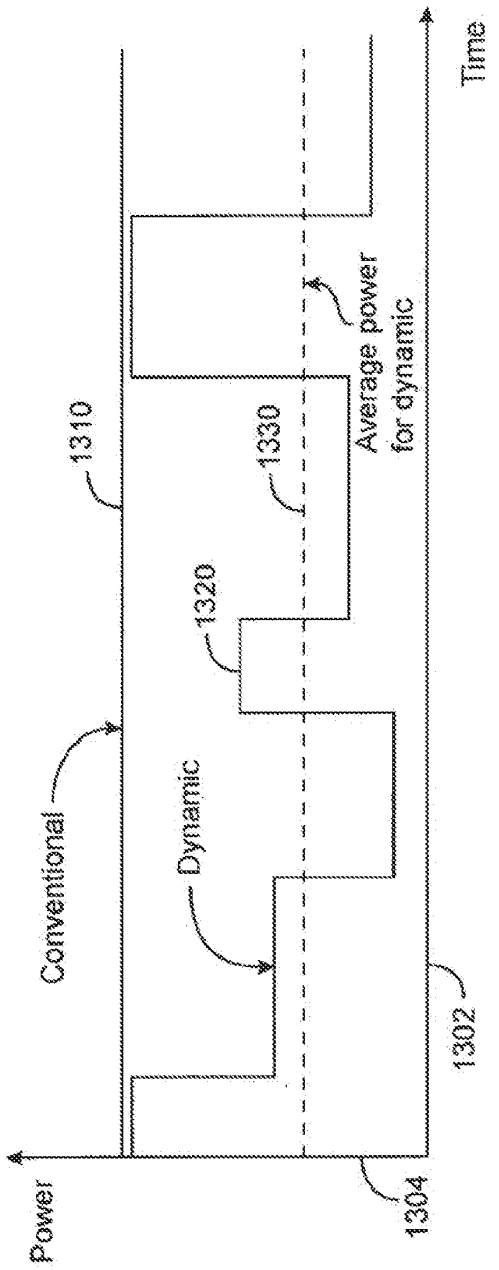

Power
Time
Conventional
Dynamic
1310
1320
1330
1302
1304
Average power for dynamic

FIG 13

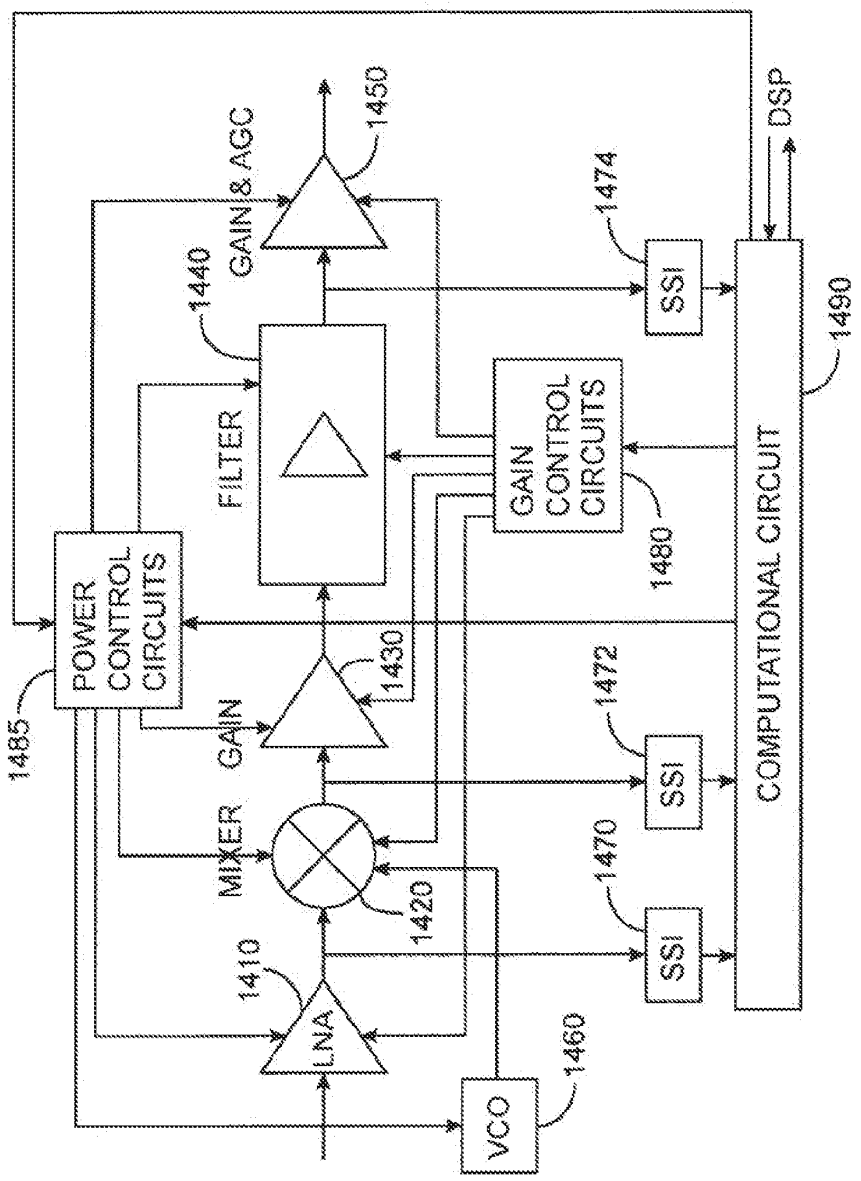

1450
GAIN & AGC
1440
FILTER
1474
SSI
DSP
1490
COMPUTATIONAL CIRCUIT
GAIN CONTROL CIRCUITS
1480
POWER CONTROL CIRCUITS
1485
1430
GAIN
1472
SSI
MIXER
1420
1470
SSI
1410
LNA
VCO
1460

FIG. 14

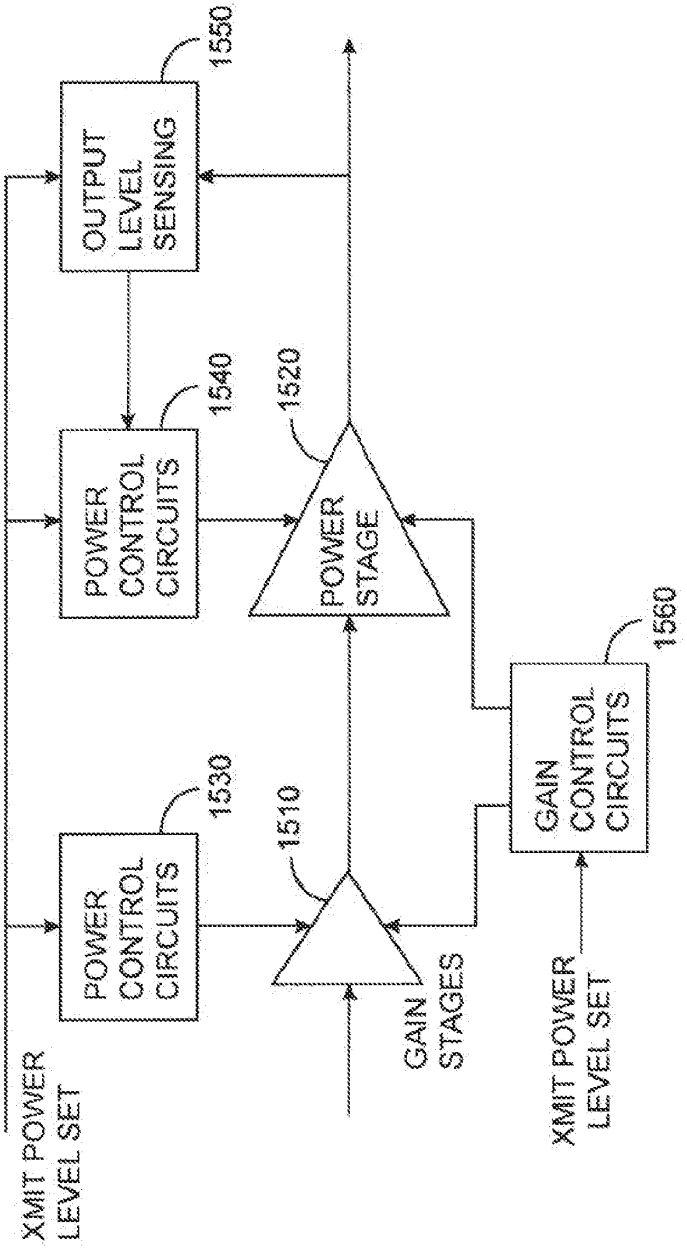

XMIT POWER LEVEL SET
POWER CONTROL CIRCUITS
1530
1510
GAIN STAGES
POWER CONTROL CIRCUITS
1540
1520
POWER STAGE
OUTPUT LEVEL SENSING
1550
GAIN CONTROL CIRCUITS
1560
XMIT POWER LEVEL SET

FIG. 15

POWER DISSIPATION REDUCTION IN WIRELESS TRANSCEIVERS

CROSS-REFERENCES TO RELATED APPLICATIONS

This application is a continuation of U.S. patent application Ser. No. 15/080,421, filed Mar. 24, 2016, which is a continuation of U.S. patent application Ser. No. 11/318,646, filed Dec. 27, 2005, which is a continuation of U.S. patent application Ser. No. 10/784,613, filed Feb. 23, 2004, which claims the benefit of U.S. provisional application No. 60/451,229, filed Mar. 1, 2003, which is incorporated by reference.

This application claims the benefit of U.S. provisional application No. 60/451,230, filed Mar. 1, 2003, which is incorporated by reference.

BACKGROUND

The present invention relates to power dissipation reduction techniques for electronic circuits, for example wireless transceiver integrated circuits.

Wireless networking is quickly becoming ubiquitous, as desktop, notebook, and handheld computers are connected to share Internet access and files. Wireless networking cards compatible with PCMCIA and compact flash form factors are popular for laptops and handhelds respectively, particularly as mobile users connect to the Internet on the road at coffee shops, hotels, and airports.

A downside of this connectivity is a corresponding drain on battery life, especially for these portable devices. The power consumed by a wireless transmitter and receiver reduces the usefulness of a device and sends a user on a hunt for an electrical outlet for recharging.

One reason why this power drain is high is that electronic circuits are typically designed to function properly under worst-case operating conditions. For a wireless transceiver, the worst case condition is when a desired signal reception strength is low, while other transceivers or nearby electronic equipment generate interfering signals and other spurious noise.

But a wireless transceiver does not always operate in these worst-case conditions. For example, a base station, router or access point may be nearby such that the received signal is strong. Also, there may be no interfering signals, or they may be relatively weak. In these situations, receiver circuit currents can be reduced below what is necessary for the worst case condition. If this is done, power dissipation is reduced, and battery life is increased.

Thus, what is needed are circuits and methods that can adapt to a better-than-worst-case condition and reduce circuit currents and therefore power dissipation accordingly.

SUMMARY

Accordingly, embodiments of the present invention provide methods and circuits for reducing power dissipation in wireless transceivers and other electronic circuits and systems. Embodiments of the present invention use bias current reduction, impedance scaling, gain, and other dynamic changes either separately or in combination to reduce power dissipation in response to better-than-worst case conditions. For example, bias currents are reduced in response to a need for reduced signal handling capability, impedances are scaled thus reducing required drive and other bias currents in response to a strong received signal, or gain is varied and

impedances are scaled in response to a low received signal in the presence of no or weak interfering signals. Alternately, currents may start low and be increased in response to worse-than-best-case conditions, or they may start at a point in between and vary up or down. These variations may be made to electronic systems generally, and are particularly suited and discussed below in the context of a wireless transceiver that may be used in networking devices, cellular telephones, and other wireless systems.

An exemplary embodiment of the present invention provides a method of receiving a signal using an integrated circuit. The integrated circuit includes a signal path having a low-noise amplifier configured to receive the signal, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer. The method itself includes determining a first signal strength at a first node in the signal path in the integrated circuit and dynamically changing an impedance of a component in the signal path based on the first signal strength.

A further exemplary embodiment of the present invention provides a method of receiving a signal using an integrated circuit. The integrated circuit includes a signal path having a low-noise amplifier configured to receive the signal, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer. The method itself includes determining a first signal strength at a first node in the signal path in the integrated circuit and dynamically changing a bias current in the signal path based on the first signal strength.

Another exemplary embodiment of the present invention provides a method of receiving a signal using an integrated circuit. The integrated circuit includes a signal path having a first circuit and a second circuit having an input coupled to an output of the first circuit. The method itself includes determining a first signal strength at a first node in the signal path in the integrated circuit. The first node is before the first circuit in the signal path. The method further includes dynamically changing a gain of the first circuit based on the first signal strength and dynamically changing an impedance of a component in the second circuit based on the first signal strength.

Still a further exemplary embodiment of the present invention provides a wireless transceiver integrated circuit including a receiver having a signal path, the signal path including a low-noise amplifier, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer, as well as a first signal strength indicator circuit coupled to the signal path and configured to determine a first signal strength. An impedance in the signal path is configured to be dynamically adjusted in response to the first signal strength.

Yet a further exemplary embodiment of the present invention provides a wireless transceiver integrated circuit. This integrated circuit includes a receiver comprising a signal path, the signal path having a low-noise amplifier, a mixer having an input coupled to an output of the low-noise amplifier, and a low-pass filter having an input coupled to an output of the mixer, as well as a first signal strength indicator circuit coupled to the signal path, and configured to determine a first signal strength. A bias current in the signal path is configured to be dynamically adjusted in response to the first signal strength.

Another exemplary embodiment of the present invention provides a wireless transceiver integrated circuit. This circuit includes a receiver comprising a signal path, the signal

path having a first circuit; and a second circuit having an input coupled to an output of the first circuit, as well as a first signal strength indicator circuit coupled to the signal path, and configured to determine a first signal strength. A gain of the first circuit is configured to be dynamically adjusted in response to the first signal strength, and an impedance in the second circuit is configured to be dynamically adjusted in response to the first signal strength.

A better understanding of the nature and advantages of the present invention may be gained with reference to the following detailed description and the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram of a wireless transceiver that may benefit by incorporation of embodiments of the present invention;

FIGS. **2**A and **2**B illustrate examples of desired and interfering signals and noise that may be received by a circuit in a wireless receiver;

FIG. **3** illustrates what can occur as a maximum signal handling capability is reduced in the worst-case signal condition;

FIG. **4** illustrates a portion of a receiver consistent with an embodiment of the present invention;

FIG. **5** illustrates the relationship between a required bias current and a given output signal for a representative circuit;

FIG. **6** is an example of how a circuit's impedances may be scaled to reduce drive currents, and depending on the circuit configuration used, to reduce associated bias currents as well;

FIG. **7** illustrates how gain may be inserted in a signal path to improve a circuit's signal to noise ratio;

FIGS. **8**A-**8**D illustrate some of the possible power saving techniques that may be used when received desired and interferer signals are all at a low power level;

FIGS. **9**A-**9**C illustrate one of the possible power saving techniques that may be used when a received desired signal is strong while all interfering signals are at a low power level;

FIGS. **10**A-**10**C illustrate one of the possible power saving techniques that may be used when received desired and interferer signals are all at a high power level;

FIGS. **11**A-**11**D illustrate one of the possible power saving techniques that may be used when a received desired signal is weak while one or more interfering signals are strong;

FIG. **12** is a summary illustrating four different input conditions and some of the appropriate power-saving changes that may be made in response to those conditions;

FIG. **13** shows how power may be saved as a function of time by employing one or more of the power saving methods consistent with embodiments of the present invention;

FIG. **14** is a block diagram of a portion of a receiver consistent with an embodiment of the present invention; and

FIG. **15** is a block diagram of a portion of a transmitter consistent with an embodiment of the present invention.

DESCRIPTION OF EXEMPLARY EMBODIMENTS

FIG. **1** is a block diagram of a wireless transceiver that may benefit by incorporation of embodiments of the present invention. This wireless transceiver may be designed to send and receive signals consistent with the IEEE 802.11a, 802.11b, 802.11g, or other signaling standard or combination of standards. This figure, as with all the included figures, is shown for illustrative purposes only and does not to limit either the possible embodiments of the present invention or the claims.

There are three main portions of this transceiver circuit, a receiver, transmitter, and synthesizer. This transceiver may be completely or partially integrated on a semiconductor chip, or it may be integrated onto multiple integrated circuits. In a specific embodiment, the circuitry bounded by dashed line **100** is integrated on a single chip coupled to one or more external components or circuits. The integrated circuit or circuits forming this wireless transceiver may incorporate various integrated circuit devices such as a bipolar, CMOS, or BiCMOS devices made using a silicon, silicon-germanium (SiGe), gallium arsenide or other III-V process, or other manufacturing process. Embodiments of the present invention may also be applicable to circuits manufactured using nanotechnology processing.

The receiver includes a signal path formed by low-noise amplifier **102**, I and Q mixers **104** and **106**, low pass filters **108** and **110**, and baseband amplifiers **114** and **116**. Other circuitry in the receiver includes received strength indicator **122**, automatic gain control circuit **166**, baseband gain control circuit **120**, tuning circuit **112**, and offset cancellation circuit **118**.

The transmitter includes input up-converter mixers **124** and **126**, summing node **176**, which may be conceptual rather than an actual circuit, transmit variable gain amplifier **128**, and power amplifier **130**.

The synthesizer includes a voltage-controlled oscillator **148**, which drives I and Q buffers **154** and **152**, prescaler **156**, reference clock buffer **142** and divider **158**, phase-frequency detector **160**, charge pump **162**, and loop filter **146**, which in a specific embodiment is formed by external components.

Signals are received on an antenna, not shown, and typically pass through an RF switch and bandpass filter before being received by the low-noise amplifier **102** on line **101**. The low noise amplifier gains the received signal and provides it to quadrature mixers **104** and **106**. I and Q mixers **104** and **106** down-convert the received signal to baseband by multiplying them with quadrature versions of the oscillator signal provided by buffers **152** and **154**. This down conversion also produces a high frequency component at a frequency that is equal to the sum of the frequencies of the received signal and the VCO. This unwanted signal is filtered by low pass filters **108** and **110**, which in turn drive baseband amplifiers **114** and **116**. The outputs of baseband amplifiers **114** and **116** are typically converted to digital signals by analog-to-digital converters at the front end of a digital signal processing block.

In the transmit mode, I and Q versions of the signal to be transmitted are provided on lines **121** and **123** to up-convert mixers **124** and **126**. These up-convert mixers multiply the I and Q portions of the transmit signal by quadrature versions of the VCO signal provided by buffers **152** and **154**. The outputs of the up-convert mixers **124** and **126** are summed, and amplified by transmit VGA **128**, which in turn drives power amplifier **130**. The output of power amplifier **130** is typically filtered, and passes through the RF switch to the antenna for transmission.

A reference clock is received and buffered by the reference buffer **142**. The VCO generates quadrature oscillatory signals that are divided by prescaler **156**. The reference clock is typically generated by a crystal or other stable periodic clock source. The phase-frequency detector **116** compares the phase or frequency (depending on whether the

synthesizer is tracking or acquiring the correct frequency) of the divided VCO signal and the reference clock, or a divided version of the reference clock, and generates an error signal, which drives the charge pump **162**. The output signal of the charge pump **162** is filtered by the loop filter **146**, which is commonly a lead-lag filter, and which provides a tuning or correction signal to the VCO **148**.

Embodiments of the present invention may be used to reduce the power dissipation of one or more of these included circuits. For example, the power dissipation in the low-noise amplifier **102**, down-convert mixers **104** and **106**, low pass filters **108** and **110**, or baseband amplifiers **114** and **116** may be optimized. Also, power dissipation in up-convert mixers **124** **126**, variable gain amplifier **128**, and power amplifier **130** may also be optimized. Similarly, VCO **148** and prescaler **156** currents may be adjusted. Embodiments of the present invention may also be applied in other circuits which may be included in other integrated circuit receivers, transmitters, transceivers, or other electronic circuits or systems.

When a receiver is actively receiving a desired signal, each block in the signal path has at its input the desired signal as well as noise and possibly interfering signals. The desired signal is the useful, information-carrying portion of a received signal. The noise may be thermal, shot, or other noise generated on the integrated circuit, in addition to received noise generated by sources external to the chip. The noise at the input of a block may be referred to as the equivalent input noise. The interfering signal or signals, or interferers, may be generated by similar transceivers, or other electrical equipment, circuits, or systems.

FIGS. **2**A and **2**B illustrate examples of desired signals, interferers, and noise that may be received by one of the various circuits in a wireless receiver. In each of these figures, the signal strength is plotted along a Y-axis **204** or **254** as a function of frequency along an X-axis **202** or **252**. In the example of FIG. **2**A, a received desired signal **206** is large in comparison to interfering signals **208** and **210**. In these examples, two interfering signals are shown for illustrative purposes, though there may be no such signals, one such signal, or more than two such signals in the frequency range of interest. Also, while for these examples the interferers are shown as being at a higher frequency than the desired signal, there may be one or more interferers at higher or lower frequencies as the desired signal. In this specific example, the acceptable noise floor **214** is relatively high, while maximum signal handling capability Smax **212** (that is the maximum signal power that can be handled with an acceptably low distortion) needs only to be high enough to accommodate the desired signal. For this specific example, the circuit receiving this input spectrum only requires a relatively small dynamic range for proper operation, that is the range between Smax **212** and the noise floor **214** is relatively small.

Conversely, in the example shown in FIG. **2**B, the desired signal **256** is relatively weak compared to the large interferers **258** and **260**. In this example, the noise floor **264** should be relatively low so as to prevent an unacceptable level of error in the recovery the desired signal **256**. The maximum signal handling capability Smax **262** should be relatively high to accommodate the large interferers in order to avoid the creation of intermodulation products as described below. Accordingly, in this specific example, the circuit receiving this input spectrum should have a large dynamic range, particularly in comparison to the example of FIG. **2**A.

It should be noted that the noise level or noise floors shown in these and the other included figures is the noise density integrated over the bandwidth of interest. For simplicity and comparison, this level is shown as a horizontal line, and is not meant to imply noise density.

Often in wireless receivers, a circuit at different times will receive an input spectrum similar to those shown in FIGS. **2**A and **2**B. The input spectrum of FIG. **2**B is generally considered the worst-case input signal, and typical design methodology involves designing a receiver for this condition, specifically the weakest desired signal accompanied by largest interference level. Circuit impedances and currents are set such that the noise floor **264** is sufficiently low for an acceptable bit-error rate, while bias currents are set sufficiently high for the required Smax **262**.

Conversely, the input spectrum in FIG. **2**A is that of the best-case input signal, specifically, a robust desired signal accompanied by no or low-level interferers. In this case, the noise floor **214** may be allowed to rise, while the maximum signal handling capability Smax **212** may be reduced. When this is done, the receiver circuit may save significant power. For example, the circuit's impedances may be increased, thus reducing required drive currents. Similarly, bias currents may be lowered, thus reducing the maximum signal in handling capability.

The minimum power dissipation for a circuit is proportional to the required maximum signal-to-noise ratio, which is the ratio between Smax **212** or **262** and N **214** and **264**. Thus, a circuit receiving an input similar to the one shown in FIG. **2**A can dissipate less power than one receiving the input as shown in FIG. **2**B, while still achieving an acceptable bit-error rate.

FIG. **3** illustrates what can occur when the maximum signal handling capability Smax **314** is reduced in the worst-case condition, that is when a weak desired signal **306** is accompanied by large interferers **310** and **312**. Again, signal strength is plotted along a Y-axis **304** as a function of frequency along X-axis **302**. In this specific example, Smax **314** is reduced below the peak levels of the interferers **310** and **312**. Since Smax is low, the circuit cannot handle the interferers linearly. The resulting nonlinearities lead to a mixing of the interferers and the creation of intermodulation products **308** (for example, a third-order intermodulation distortion, IM3), one of which in this example occurs at the same frequency as the desired signal **306**. As can be seen, if the intermodulation products **308** become excessive, the received signal bit error rate may become excessive, and the desired signal **306** may be lost. Accordingly, while Smax may be lowered even under some unfavorable conditions in order to reduce power, care should be taken to avoid corruption of the received desired signal.

FIG. **4** illustrates a portion of a receiver consistent with an embodiment of the present invention. Included is a filter **430**. An optional gain element **420** is placed in front of the filter **430** in order to increase signal levels. Signal strength indicator circuits **440** and **450** are connected to input line **410** and output line **460**. In this specific example, the input signal spectrum on line **410** is shown as desired signal **412** and interferers **414** and **416**. The signal spectrum at the output line **460** is shown as desired signal **462** and interferers **464** and **466**. The signal strength indicators **440** and **450** do not provide information as to the relative sizes of the desired and interfering signals. Rather, a cumulative signal level is provided at their outputs. For example, the first signal strength indicator **440** outputs a level corresponding to the sum of desired signal **412** and interfering signals **414** and **416**, while the second signal strength indicator **450** provides

a signal level corresponding to the sum of desired signal **462** and interfering signals **464** and **466**. In this specific example, the gain of the gain and filter circuit combinations is shown as approximately one, while the interfering signals **414** and **416** signal levels are reduced.

A comparison of the signal levels provided by the signal strength indicators **440** and **450** indicates that much of the combined received signal on line **410** has been filtered. Accordingly, it may be deduced that large interfering signals present at the input are being filtered by the filter **430**. From this information, as will be shown in greater detail below, the bias, impedance, and gain of the gain stage **420** and filter **430** combination may be optimized to reduce power dissipation.

There are several real world situations where the received signal is better than the worst-case condition such that power can be saved. For example, large interferers may be present only part of the time, that is, on a temporary or transient basis. The interfering equipment may be some distance from the transceiver, or it may be operating in the low power mode. Also, the desired signal may be very strong as compared to the noise and interferers, for example a hub, router, or access point may be nearby.

Some transceivers consistent with embodiments of the present invention are designed to work with more than one data transfer specification or standard. In this case, when a transceiver is operating in a mode having a lower data rate, the power saving techniques described here may be employed.

FIG. **5** illustrates the relationship between a required biased current **516** for a given output signal **514** for a representative circuit **510**. If the output signal current level is relatively low, such as the output current shown as **526**, the corresponding bias current **528** may be low. Conversely, if the output signal current level is larger as with the example **536**, the corresponding bias current level **538** should also be high. Accordingly, if a bias current is initially set high to handle large a large input signal, for example a large interferer, this current may be reduced if the input signal is smaller.

There are many ways by which these bias currents can be reduced. For example, the current may be generated by placing a voltage across a resistor by applying a bias voltage to the base of a device whose emitter is connected to ground through a resistance. In this case, the resistor may be increased by opening switches across portions of the resistance, or lowering the bias voltage applied at the base. Several ways in which this may be done will be readily understood by one skilled in the art.

FIG. **6** is an example of how a circuit's impedances may be scaled to reduce drive currents, and, depending on the circuit configuration used, associated bias currents as well. A driver **612** has a load R **614** and C **616**. The frequency response of this circuit is the same as that seen by driver **622**, which drives an impedance of 2R **624** and C/2 **626**. But the impedance of the load seen by driver **622** is double that seen by **612**, thus the output current required by the driver **622** is reduced by one-half.

As an example, the output stage of each of these drivers may be a Class A emitter follower formed by an emitter follower connected to a current source. When the outputs are driven high, the emitter of driver **622** need supply only one-half the drive current as driver **612**. In this way, an impedance can be scaled in order to decrease a circuit's required drive current.

Also, the discharge current for driver **622** is only one half that of driver **612** for a given negative-going slew rate. Thus, the current source of **622** may be reduced by the same factor of one-half as compared to driver **612**. In this example, the bias current, that is the current in the pull-down current source can be reduced. Many other examples where drive currents and possibly bias currents may be reduced will be appreciated by one skilled in the art.

FIG. **7** illustrates another degree of freedom that made be employed to reduce current levels in a transceiver. Specifically, a gain element **720** may be inserted in front of a circuit block **730** in order to improve the combined circuit's signal-to-noise ratio by a factor equal to the gain of the inserted gain block. This is particularly useful when large interferers are absent and the desired received signal is moderate or low. Specifically, gain is added to the signal while impedances are increased, which raise the noise floor. In this way, a given signal-to-noise ratio may be maintained while the power is decreased.

The gain of such an element may be varied by increasing a current in a differential pair or increasing a load resistance using switches. Many other examples where the gain of this element may be varied will be appreciated by one skilled in the art.

These variables, or degrees of freedom, specifically reducing bias currents, increasing impedances, and increasing gain may be used as in the following examples.

FIG. **8A** is a block diagram of a functional block **820** and optional gain element **810** in accordance with an embodiment of the present invention. Functional block **820**, like the functional blocks in the following diagrams, may be a filter, mixer, amplifier, or other circuit or circuits in a wireless transceiver or other electronic circuits or system. An input signal is received on line **812** by the optional gain element **814**. When the optional gain block **810** is not used, the input signal may be received directly by the function block **820**. The gain of the optional gain element **812** is controlled by a gain control signal on line **814**. The functional block receives an output signal from the optional gain element **810** and provides an output VOUT on line **822**. The lines in this and the other included figures may be one or more lines, depending on whether single-ended, differential, or other type of signaling is employed.

One or more impedances are under control of signals on impedance control lines **824**. Similarly, one or more bias currents in the function block are under control of one or more signals on bias control lines **826**. These various control lines may be logic signals, analog signals, voltage or currents lines, or other signal or bias lines. In other embodiments of the present invention, the gain control element **810** may be included in the function block **820**. Also, various embodiments may not incorporate either or both the impedance control and bias control.

FIG. **8B** is an example input that may be present on line VIN **812**. In this example, a desired signal **836** is relatively weak, as are interfering signals **837** and **838**. The initial bias and circuit configuration is such that the noise floor **833** and maximum signal handling capability Smax **831** are adjusted for worst case conditions. The circuit of FIG. **8A**, as with all the circuits described here, receives noise at its input which may be referred to as input equivalent noise or input referred noise. Additionally, the circuit of FIG. **8A** generates noise which is added to the input referred noise. Depending on the gain characteristics of the circuitry, the output noise at various frequencies may be greater than, equal to, or less than the input referred noise. For simplicity, the noise floor and maximum signal handling capability Smax, in this and the other figures, are shown as straight lines, though the noise and Smax are typically curved as a function of frequency.

That the input spectrum is as shown in FIG. **8**B can be determined, for example, by low signal strength indications on line VIN **812** and VOUT **822**. That is, a low level signal strength indication on line VIN **812** indicates that no portion of the input signal is particularly large.

For this exemplary input, there are at least two methods by which the power dissipation for this circuitry may be reduced. Depending on the exact circuits and structures used, one of these methods may be preferred.

In FIG. **8**C, the bias current is decreased, thereby lowering the maximum signal handling capability **841** as compared to **831**, closer to the desired and interfering signal levels. Again, the bias currents in the function block **820** may be reduced by switching impedances that appear across a voltage thereby changing a resulting bias current, by reducing a voltage at the gate of a MOS or base of a bipolar transistor, or by other methods.

In FIG. **8**D, a second method of reducing power dissipation in the function block **820** is employed. Specifically, Smax **851** is held constant as compared Smax **831**. The desired and interfering signals are amplified such that they are closer to the available signaling handling capability **851**. Also, the noise floor **853** is raised as compared to noise floor **833** in FIG. **8**B. Specifically, the noise contributed by the function block **820** is increased, such that the noise at its output is increased to noise floor **853**. This is done by increasing one or more impedance in function block **810**, such that drive currents inside that block are reduced. Depending on the exact configuration, this may also allow some biasing currents to be reduced, while maintaining the maximum signal handling capability **851** at a sufficient level. Alternately, these two methods of reducing power dissipation in function block **820** may be done in combination.

The included examples are explained for the exemplary situation where biasing and other parameters are set for worst-case conditions, and then changed to save power when it is discovered that the conditions are better-than-worst case. Alternately, the bias currents and other parameters may be set for maximum power savings, or an intermediate point, and the power can be adjusted from there.

FIG. **9**A illustrates a block diagram including an optional gain element **910** and function block **920**. Again, an input signal is received on line **912** by optional gain element **910** which in turn drives function block **920**. The function block provides an output VOUT on line **922**, and receives impedance and bias control signals on lines **924** and **926**.

FIG. **9**B shows the spectrum for what may be considered a best-case received signal. Specifically, the desired signal **936** is strong, while the interfering signals **937** and **938** are relatively weak. This may be determined, for example, by detecting a large signal level at the input line VIN **812** and a large signal level after a filter, since these readings would indicate that a large signal is received, but that it is at the desired signal frequency.

The maximum signaling capability **931** and noise floor **933** are shown as being set for the worst case conditions. In this case, the noise floor **933** is lower than the maximum allowed for proper signal reception. Accordingly, one or more impedance in the function block **920** may be increased, such that the noise floor **943** rises as shown in FIG. **9**C. In this way one or more the driving currents in the function block **920** may be reduced. Similarly, since the drive current is reduced, one or more bias current may also be reduced, depending on the exact circuit configuration.

FIG. **10**A illustrates a block diagram showing an optional gain element **1010** driving a function block **1020**. An input signal is received by the gain element **1010** on line **1012**, and an output is provided by function block **1020** on line VOUT **1022**. One or more gain control signals present on lines **1014** control the gain of gain control element **1010**, while one or more impedance and bias control signals are received by the function block **1020** on line to **1024** and **1026**.

FIG. **10**B illustrates a received signal that may be received on line VIN **1012**. In this example, the desired signal **1036** and interferers **1037** and **1038** are each relatively large. This may be determined, for example, by detecting a large signal level at the input line VIN **812** and a smaller signal level after a filter, since these readings would indicate that a large signal is received, but that interferers are being reduced.

As before, in this example, the noise floor **1033** and maximum signal handling capability **1031** are initially set for the worst case conditions. Since the desired signal is relatively large in this case, the noise floor may be allowed to rise, a shown by noise floor **1043** in FIG. **10**C. Since the desired signal **1046** and interferers **1047** are large, the maximum signal handling capability Smax **1041** remains constant. Again, the noise floor is increased by increasing impedances in the function block **1020**. This reduces the required drive current, and may also allow for a reduction in bias currents.

FIG. **11**A illustrates a block diagram including an optional gain element **1110** and function block **1120** in accordance with an embodiment of the present convention. An input signal is received on line **1112** by the optional gain control element **1110**, while an output signal is provided by the function block **1120** on line VOUT **1122**. Gain, impedance, and bias control signals are received on lines **1114**, **1124**, and **1126**.

FIG. **11**B is an exemplary input signal that may be received by the gain control element **1110** on line VIN **1112**. In this specific example, the desired signal **1136** is relatively low or weak while the interfering signals **1137** and **1138** are large. This may be determined, for example, by detecting a large signal level at the input line VIN **812** and a much smaller signal level after a filter, since these readings would indicate that a large signal is received and that large interferers are being reduced such that the resulting signal, the desired signal, is relatively weak.

Again, the maximum signal handling capability **1131** and noise floor **1133** are initially set for worst case conditions. If the desired signal is sufficiently low, while the interferers are sufficiently high, power savings may not be achievable over the worst case settings, since this is in fact the worst case condition. But, if the desired signal is somewhat larger than the worst case condition, then power may be saved in at least two different ways.

For example, FIG. **11**C shows the maximum signal handling capability **1141** being lowered. In this case, the interfering signals **1147** in **1148** began to clip and distort, thereby creating intermodulation products **1145**, which distort the desired signal **1146**. So long as care is taken to not corrupt the desired signal **1146** beyond an acceptable limit, typically measured by a bit-error rate, power may be reduced in this way.

Similarly, in FIG. **11**D, the noise floor **1153** is raised somewhat, thereby saving power. Again, this may be done so long as the noise floor is not sufficiently high that the system bit-error rate becomes unacceptable.

FIG. **12** is a summary of the above four examples. The received signal strengths are shown in column **1210**, while appropriate power saving responses are listed in column **1220**. Specifically, in row **1230**, the desired signal and interferer signal strengths are both weak or small. In this case, proper responses include decreasing Smax, or increas-

ing one or more circuit impedances while increasing the circuit gain. Depending on the exact circuit configuration, one of these options may be preferred over the other. Alternately, they may be done in combination, or done in combination with other power saving techniques. Also, in some specific embodiments, when both desired signal and interferer signal strengths are small, the gain may need to be increased while the impedance is maintained or not increased in order to keep the noise floor low.

In row **1240**, the desired signal strength is strong or large, while the interfering signals are small. In this case, an appropriate response is to increase one or more of the circuit impedances. Again, depending on the exact circuit in question, one or more of the bias currents may also be reduced.

In row **1250**, both the desired signals and interfering signal strengths are large. Again, in this case an appropriate response is to increase one or more of the circuit impedances.

In row **1260**, the received desired signal strength is weak or small, while the interfering signals are large. Since this is the worst case situation for which the circuit is designed, substantial power savings are difficult to achieve. However, again, if the received signal is above a minimum level necessary for proper operation, some distortion of the interferers or raising of the noise floor may be acceptable.

It should be noted that not all possible signal conditions are listed here. For example, either the signal or interferer may be of a relatively medium strength, or the interferer may be absent. Also, these terms are for exemplary purposes and are not meant to convey specific signal conditions, but rather are only qualitative. The proper response to a specific condition depends on the embodiment of the present invention, the particular circuit topology, the requirements of the signaling standard used, as well as other constraints.

FIG. **13** is an example shown how power may be saved as a function of time by employing one or more of these methods consistent with embodiments of the present invention. Power is plotted along a Y-axis **1304** as a function of time along X-axis **1302**. Conventional worst case design would fix power dissipation at line **1310**. As can be seen, dynamic power dissipation **1320** under the control of variable gains, impedances, biasing, or combination thereof, allows for a lower average power **1330** as compared to the power dissipated **1310** by the conventional design.

FIG. **14** is a block diagram of a portion of a receiver consistent with an embodiment of the present invention. Included are low-noise amplifier **1410**, mixer **1420**, gain stage **1430**, filter **1440**, AGC amplifier **1450**, and VCO **1460**. Signal strength detection is done at the output of the low-noise amplifier by signal strength indicator **1470**, at the output of the mixer by signal strength indicator **1472**, and at the output of the filter by signal strength indicator **1474**. The outputs of the signal strength indicator circuits are received by the computational circuit **1470**, which in turn controls gain and power control circuits **1480** and **1485**. Power and gain control circuits **1480** and **1485** control the gain, biasing, and impedance levels of the circuits in the receiver signal path. Also, the gain and power control circuits may control the same parameters in the VCO **1460**. This figure is greatly simplified for purposes of explanation. For example, the quadrature nature of the mixers and following circuits are not shown. Also, power-down and start-up circuits are not included.

The current level in the low-noise amplifier determines a multitude of parameters including voltage gain, linearity, input impedance matching, and noise figure. When conditions are better than worst-case, some of these parameters may be relaxed while maintaining an acceptable bit-error rate, thus saving power.

The bias current in the mixers effect that block's noise figure and linearity. Care is taken in reducing power in this block so as not to increase nonlinearities, particularly the third-order nonlinearity as measured by IP3, the third-order intercept point, beyond an acceptable limit.

A key parameter of the VCO is phase noise, an increase in which increases the sidebands on either side of the oscillation signal. During transmission, the phase noise should be kept low to avoid interference with adjacent channels and for preserving modulation information.

During reception however, if the conditions are better than worst case, the phase noise requirement for the VCO is relaxed, and power can be saved consistent with embodiments of the present invention. The achievable phase noise power spectral density is approximately inversely proportional to the bias current used. Thus, when low phase noise is not required during reception, bias current in the VCO can be reduced.

Most of the power savings in a transceiver in accordance with embodiments of the present invention is achieved in the receiver portion. Additional power may be saved in the transmitter section.

FIG. **15** is a block diagram of a transmitter portion consistent with an embodiment of the present invention. Included is a signal path formed by gain stage **1510** and power amplifier **1520**. The output power level is sensed by output level sensing circuit **1550**, which in turn adjusts the biasing of the power amplifier **1520** through the power control circuit **1540**. Additionally, a transmitter level control signal is received by power control circuits **1530** and **1540**, which in turn control the biasing of gain stage **1510** and power amplifier **1520**. Gain control circuit **1560** also adjusts the gain of gain stage **1510** and power amplifier **1520**. Additional circuitry that varies impedances in each of these circuits may also be included.

Since the gain, impedance and biasing of these blocks are being dynamically varied, care must be taken to not negatively affect the signal being processed. For example, specific embodiments of the present invention perform some or all of these variations during preamble. Also, as changes occur, the circuits in some embodiments are limited such that they may only adapt to an improvement in conditions after frames are completed. If conditions worsen, the circuits may be allowed to change in order to save the data. Alternately, a system may be manually calibrated, for example at set up, and when the network configuration is changed.

The above description of specific embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form described, and many modifications and variations are possible in light of the teaching above. The embodiments were chosen and described in order to best explain the principles of the invention and its practical applications to thereby enable others skilled in the art to best utilize the invention in various embodiments and with various modifications as are suited to the particular use contemplated.

What is claimed is:

1. A method of reducing the power consumption of a receiver of a battery operated transceiver having a plurality of circuits, wherein the plurality of circuits comprise a receiver signal path comprising at least an amplifier, a mixer and a filter, wherein the plurality of circuits are designed to

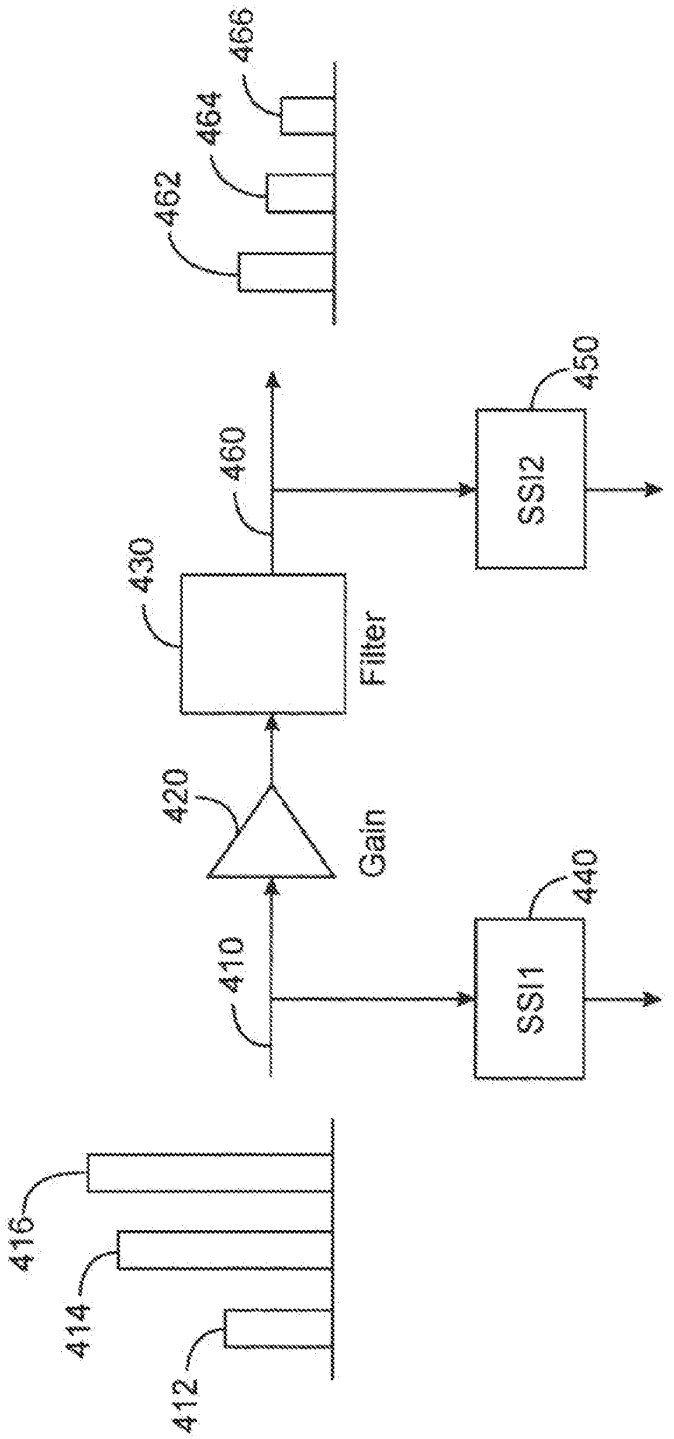

466
464
462
450
460
SSI2
430
Filter
420
Gain
440
410
SSI1
416
414
412

FIG. 4

function between a worst-case operating condition and a best case operating condition, wherein the worst-case operating condition is when a desired signal strength is low and an interferer signal strength is high and the receiver operates with a maximum power dissipation and the best-case operating condition is when the desired signal strength is high and the interferer signal strength is low and the receiver operates with a minimum power dissipation, the method comprising:

receiving a signal comprising a desired signal and an interferer signal;

determining a strength of the desired signal;

determining a strength of the interferer signal;

comparing the strength of the desired signal to the strength of the interfere signal; and

dynamically adjusting at least one of an impedance, a bias or a gain of at least one of the amplifier, filter or mixer in the receiver signal path, responsive to the comparing.

2. The method of claim 1, wherein when the strength of the interferer signal decreases over time, and the strength of the desired signal is low, dynamically decreasing the bias of at least one of the plurality of circuits in the receiver signal path.

3. The method of claim 1, wherein when the strength of the interferer signal is low, and the strength of the desired signal decreases over time, dynamically increasing a gain of at least one of a plurality of circuits in the receiver signal path and dynamically increasing the impedance of at least one of the plurality of circuits in the receiver signal path.

4. The method of claim 1 wherein when the strength of the interferer signal is low and the strength of the desired signal increases over time, dynamically increasing the impedance of one or more of the plurality of circuits in the receiver signal path.

5. The method of claim 1, wherein when the interferer signal is weak and the desired signal is low and the strength of the desired signal increases over time, dynamically decreasing the bias of one or more of the plurality of circuits in the receiver signal path.

6. A method for reducing power consumption in a receiver in a battery operated mobile device, wherein the receiver comprises a plurality of circuits, and wherein the plurality of circuits comprise a signal path including at least an amplifier, a mixer and a filter, the method comprising:

receiving a wireless signal comprising a desired signal and an interferer signal at the receiver;

determining a strength of the desired signal;

determining a strength of the interferer signal;

comparing the strength of the desired signal to the strength of the interferer signal; and

when the strength of the interferer signal is low and the relative strength of the desired signal is greater than the strength of the interferer signal, dynamically increasing an impedance of at least one of the amplifier, filter or mixer in the signal path of the receiver, thereby reducing power dissipation in the receiver.

7. A method for power dissipation control in a receiver of a wireless transceiver of a battery-powered portable wireless device, the receiver having a signal path comprising a plurality of circuits including at least an amplifier, a filter, and a mixer, wherein the receiver is configured to receive a wireless signal having a desired signal and an interferer signal, wherein the plurality of circuits are designed to function between a worst-case condition when a strength of the desired signal is low and a strength of the interferer signal is high, and a best-case condition when the strength of the desired signal is high and the strength of the interferer signal is low, the method comprising:

receiving the wireless signal having the desired signal and the interferer signal by the receiver;

determining the strength of the desired signal;

determining the strength of the interferer signal;

comparing the strength of the desired signal relative to the strength of the interferer signal; and

based on the comparison, when the plurality of circuits are functioning at better than the worst-case condition, dynamically adjusting one or more of an impedance, a bias or a gain of one or more of the plurality of circuits in the signal path, thereby controlling power dissipation.

8. The method of claim 7, wherein when the strength of the interferer signal is low and the relative strength of the desired signal with respect to the interferer signal increases, dynamically increasing the impedance of one or more of the plurality of circuits in the signal path to reduce the power dissipation and thereby save power.

9. The method of claim 7, wherein when the strength of the desired signal is low but the relative strength of the desired signal with respect to the interferer signal is better than the worst-case condition and the interferer signal reduces in strength, dynamically reducing the bias of one or more of the plurality of circuits in the signal path, thereby reducing power dissipation and saving power.

10. The method of claim 9, wherein reducing power dissipation reduces a power drain from a battery in the battery-powered portable wireless device.

11. A method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, the receiver having a signal path comprising a plurality of circuits including at least an amplifier, a filter, and a mixer, the plurality of circuits designed to function under at least a worst case condition when a strength of a received desired signal is low and a strength of a received interferer signal is high, the method comprising:

receiving a wireless signal having a desired signal and an interferer signal by the receiver;

determining a strength of the desired signal;

determining a strength of the interferer signal;

comparing the strength of the desired signal relative to the strength of the interferer signal;

based on the comparing, determining a functioning condition of the plurality of circuits; and

when the plurality of circuits are determined to function at a better than the worst case condition in which the strength of the interferer signal is low and the strength of the desired signal is low, causing a bias current of one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be dynamically decreased relative to the worst-case condition, thereby saving power.

12. A method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device, the receiver configured to function under at least a worst case condition when a received desired signal strength is low and a received interferer signal strength is high, the receiver having a signal path comprising at least an amplifier, a filter, and a mixer, the method comprising:

receiving a wireless signal having a desired signal and an interferer signal by the receiver;

determining a strength of the desired signal;

determining a strength of the interferer signal;

comparing the strength of the desired signal relative to the strength of the interferer signal;

based on the comparing, determining a functioning condition of the plurality of circuits; and

when the plurality of circuits are determined to function at a better than the worst case condition in which the strength of the interferer signal is low and the strength of the desired signal is high, causing an impedance of one or more of amplifier, filter or the mixer in the receiver signal path of the wireless transceiver to be increased relative to the worst-case condition, thereby saving power.

13. A method for power dissipation control in a receiver of a wireless transceiver of a battery powered portable wireless device, the receiver having a signal path comprising a plurality of circuits including at least an amplifier, a filter, and a mixer, the method comprising:

receiving a wireless signal having a desired signal and an interferer signal by the receiver;

determining the strength of the desired signal;

determining the strength of the interferer signal;

comparing the strength of the desired signal relative to the strength of the interferer signal; and

when the interferer signal is high and the desired signal is low, causing a bias current of one or more of the plurality of circuits in the receiver signal path of the wireless transceiver to be dynamically increased, controlling the power dissipation of the receiver.

14. A method for power dissipation reduction in a receiver of a wireless transceiver of a battery powered portable wireless device based on its operating signal conditions, wherein the receiver has a signal path comprising a plurality of circuits including at least an amplifier, a filter, and a mixer, the plurality of circuits designed to function under operating signal conditions that vary based on relative signal strengths of an interferer signal and a desired signal, wherein the operating signal conditions vary between a worst-case operating condition and a best-case operating condition, wherein the worst-case operating condition occurs when a desired signal strength is low and an interferer signal is high and the receiver operates with a maximum power dissipation, wherein the best-case operating condition occurs when the desired signal is high and the interferer signal strength is low and the receiver operates with a minimum power dissipation, the method comprising:

receiving a wireless signal having a desired signal and an interferer signal by the receiver;

determining the strength of the desired signal;

determining the strength of the interferer signal;

comparing the strength of the desired signal relative to the strength of the interferer signal strength;

based on the comparing, when the plurality of circuits are determined to be functioning at better than the worst-case operating signal condition, dynamically adjusting at least one of an impedance, a bias current or a gain of one or more of the amplifier, filter or mixer in the signal path of the receiver, thereby reducing power consumption to save power.

15. The method of claim 14, wherein when the desired signal strength is low and the receiver is operating at better than the worst-case operating signal condition by having the interferer strength lower than that in the worst case operating signal condition, dynamically reducing the bias of one or more of the plurality of circuits in the signal path of the receiver, thereby reducing power dissipation and saving power; and

wherein when the interferer signal strength is high and the receiver is operating at better than the worst-case operating signal condition by having the desired signal higher than that in the worst case operating signal condition, dynamically increasing the impedance of one or more of the plurality of circuits in the signal path of the receiver, thereby reducing power dissipation and saving power.

16. A method for power dissipation optimization in a receiver of a wireless transceiver of a battery powered portable wireless device, the receiver having a signal path comprising a plurality of circuits including at least an amplifier, a filter, and a mixer, wherein the plurality of circuits are designed to function between a worst-case operating condition and a best case operating condition, wherein the worst-case operating condition is when a desired signal strength is low and an interferer signal strength is high and the receiver operates with a maximum power dissipation and the best-case operating condition is when the desired signal strength is high and the interferer signal strength is low and the receiver operates with a minimum power dissipation, the method comprising:

receiving a wireless signal having a desired signal and an interferer signal by the receiver;

determining a strength of the desired signal;

determining a strength of the interferer signal;

comparing the strength of the desired signal relative to the strength of the interferer signal; and

based on the comparing, when the plurality of circuits are determined to be functioning at better than the worst-case operating condition, dynamically adjusting at least one of an impedance, a bias current or a gain of one or more of the amplifier, filter or mixer in the signal path of the receiver to optimize power dissipation and save power.

17. The method of claim 16, wherein when the desired signal strength is low and the operating signal condition of the receiver is better than the worst-case operating signal condition and the interferer signal strength is increasing, dynamically increasing a bias current of at least one of the plurality of circuits in the receiver signal path of the wireless transceiver, optimizing the power dissipation;

wherein when the desired signal strength is low and the operating signal condition of the receiver is better than the worst-case operating condition and the interferer signal strength reduces over time, dynamically decreasing a bias current of at least one of the plurality of circuits in the receiver signal path of the wireless transceiver, optimizing the power dissipation, and

wherein optimizing the power dissipation under better than the worst-case operating signal condition saves power with respect to the maximum power dissipation of the worst-case operating signal condition.

18. A method for controlling power dissipation in a receiver of a wireless transceiver of a battery powered portable wireless device, the receiver having a signal path comprising a plurality of circuits including at least an amplifier, a filter, and a mixer, wherein the plurality of circuits are designed to function between a worst-case operating condition and a best case operating condition, wherein the worst-case operating condition is when a desired signal strength is low and an interferer signal strength is high and the receiver operates with a maximum power dissipation and the best-case operating condition is when the desired signal strength is high and the interferer signal strength is low and the receiver operates with a minimum power dissipation, the method comprising:

receiving a wireless signal having a desired signal strength and an interferer signal by the receiver;

determining a strength of the desired signal;

determining a strength of the interferer signal;

comparing the strength of the desired signal relative to the strength of the interferer signal; and

wherein when the strength of the interferer signal is low and when the strength of the received desired signal is higher than the desired signal of the worst-case operating signal condition, dynamically adjusting an impedance of at least one of the plurality of circuits in the signal path to reduce power dissipation.

19. A method of power dissipation optimization in a receiver of a wireless transceiver of a wireless communication device based on its operating signal conditions, wherein the transceiver has a signal path comprising a plurality of circuits designed to function under operating signal conditions that vary based on relative signal strengths of an interferer signal and a desired signal in a received wireless signal, wherein operating conditions vary between a worst-case operating signal condition, wherein the receiver operates with a maximum power dissipation when a desired signal strength is low and an interferer signal strength is high and a best-case operating signal condition, wherein the receiver operates with minimum power dissipation when the desired signal strength is high and the interferer signal strength is low, the method comprising:

receiving the wireless signal having the desired signal and the interferer signal by the receiver;

determining the desired signal strength;

determining the interferer signal strength;

comparing the desired signal strength to the interferer signal strength to determine an operating signal condition of the receiver;

based on the comparing, when the receiver operating signal condition is better than the worst case operating signal condition, dynamically adjusting one or more of an impedance, a bias, or a gain of one or more of the plurality of circuits in the receiver signal path, thereby optimizing power consumption to save power.

20. The method of claim 19, wherein power saving occurs when the desired signal strength is low and the operating signal condition is better than the worst-case operating signal condition, by dynamically reducing the bias current of one or more of the plurality of circuits in the signal path of the receiver, thereby reducing power dissipation.

21. The method of claim 20, wherein power saving occurs when the operating signal condition improves when the strength of the interferer signal decreases over time, and the bias current is reduced by dynamically adjusting the bias current of one or more of the plurality of circuits in the signal path of the receiver.

22. A method of power dissipation optimization in a receiver of a wireless transceiver of a wireless communication device based on its operating signal conditions, wherein the transceiver has a signal path comprising a plurality of circuits designed to function under operating signal conditions that vary based on relative signal strengths of an interferer signal and a desired signal in a received wireless signal received, wherein the operating signal conditions vary between a worst-case operating signal condition and a best-case operating signal condition, wherein in the worst-case operating signal condition the receiver operates with a maximum power dissipation when a desired signal strength is low and an interferer signal strength is high, and wherein in the best-case operating signal condition the receiver operates with minimum power dissipation when the desired signal strength is high and the interferer signal strength is low, the method comprising:

receiving the wireless signal having the desired signal and the interferer signal by the receiver;

determining the desired signal strength;

determining the interferer signal strength;

comparing the desired signal strength to the interferer signal strength;

determining an operating signal condition of the receiver between the best and worst-case operating signal conditions based on the comparing;

when the interferer signal strength is high and the operating signal condition is better than the worst-case operating signal condition, dynamically increasing an impedance of one or more of the plurality of circuits in the signal path of the receiver, thereby reducing power dissipation.

23. The method of claim 22, wherein when the desired signal strength increases over time resulting in an improvement in the operating condition, dynamically adjusting the impedance of one or more of the plurality of circuits in the signal path of the receiver results in power saving.

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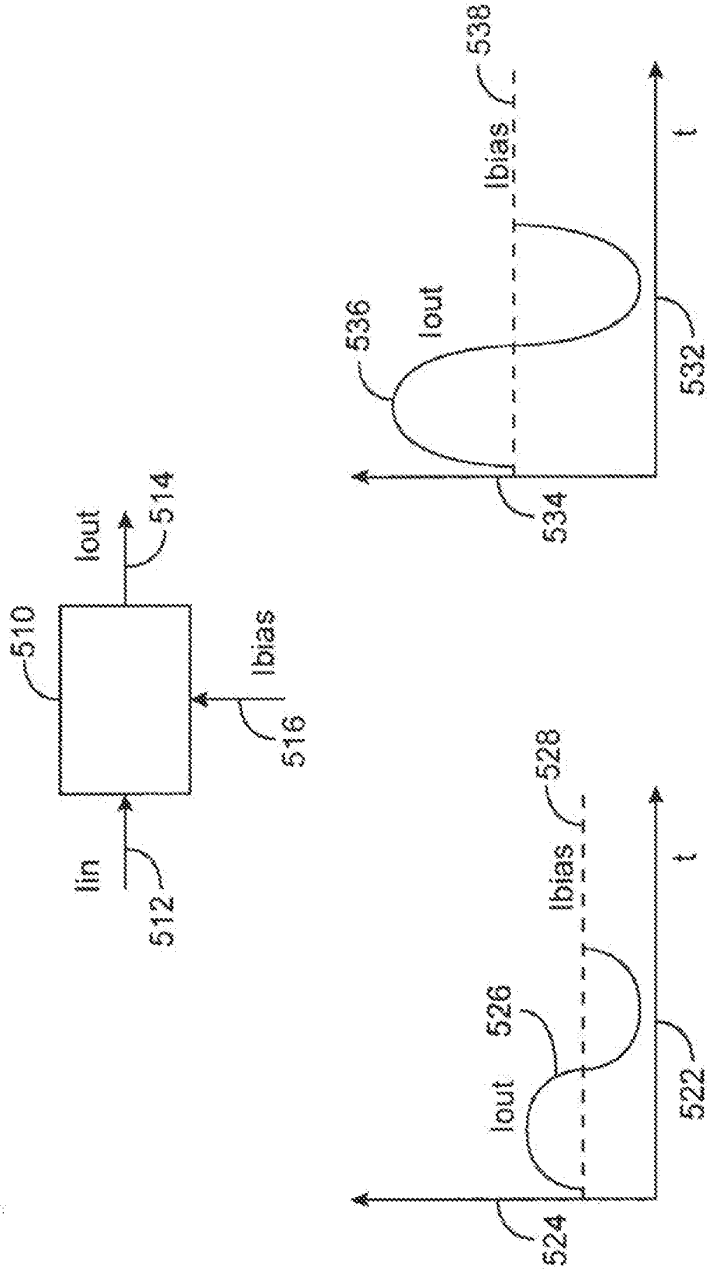

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FIG. 5