TA 8.5 An Adaptive 2.4GHz Low-IF Receiver in 0.6μm CMOS for Wideband Wireless LAN

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High bit-rate communications require wideband channels and complex modulation schemes, such as QAM, to convey multiple bits per symbol. Available bandwidth (BW) and desired user density per cell together determine the BW allocated per channel. In short-range applications like indoor wireless LAN where transmitted power is limited to 1mW, FCC rules allow channel BW higher than 1MHz. This system adapts to channel bandwidths ranging from 0.625MHz to 10MHz, and modulations spanning 4-QAM to 64-QAM. The carrier frequency is slowly hopped across the 2.4GHz ISM band.

Figure 8.5.1 shows the block diagram of the integrated CMOS dual downconversion receiver. With 64-QAM and 625kHz channel BW, 1/f noise and DC offset in the receiver IF circuits may significantly degrade error rate. A non-zero IF positions the downconverted channel beyond the 1/f noise corner. The RF input is applied to differential common-source LNA degenerated by wirebond inductors (Figure 8.5.2a). To lower junction capacitance, M1 and M2 are laid out as a dual-gate MOSFET, with no contacts on the common junction. Biased at 8mA from 3.3V, its measured noise figure (NF) at 2.4GHz is 2.4dB, gain is 19dB, input-referred 3rd-order intercept (IIP3) is +1.5dBm, and input return loss is 13dB. Each Gilbert-cell type mixer after the LNA biases at 3mA, and gives 15dB NF and +17dB IIP3 (Figure 8.5.2b). An amplifier with 8dB gain and low output impedance drives the IF1 signals into a two-stage polyphase filter. Mixer gain matching and LO quadrature accuracy limit on-chip image rejection in this single-quadrature downconverter to 35dB, but at IF1 of 190MHz the RF preselect filter attenuates image frequencies by an additional 40dB (Figure 8.5.3a). A two-stage RC polyphase filter tuned to 2GHz creates balanced quadrature outputs for LO1. The gains of the RF mixer and IF1 amplifier are switch selectable.

Unaided by an external filter, on-chip analog circuits cancel the image after downconversion to IF2. Only the channel of interest now appears at the receiver output, and this is digitized for demodulation by one A/D converter with relaxed dynamic range. A double-quadrature mixer downconverts the quadrature signals at IF1 with quadrature phases of LO2. Image rejection in this mixer is insensitive to imbalance in the IF1 inputs or LO2 phase inaccuracy [1], but is limited by gain mismatch between the four mixers and component spreads in the subsequent polyphase filter. IF2 spans 5 to 15MHz. The gains of four-FET passive commutating mixers deviate by less than 0.1% when well-matched polysilicon resistors are inserted in series, and the mixer gates are switched rail-to-rail by square waves at LO2. Five stages of passive RC polyphase filters reject the image by about 60dB over 3.5MHz to 19MHz, thereby covering the required 10MHz BW with ±25% margin for process variations. Well-matched interstage amplifiers with low output impedance partly compensate the cascade loss of the polyphase filter and passive mixers. Figure 8.5.3b shows the image rejection of the 2nd-downconversion in the complete RX for three measured chips. This is comparable to results reported without interstage amplifiers [1].

The IF strip consists of a pre-filter programmable gain amplifier (PGA), a variable BW channel select bandpass filter (BPF), a post-filter PGA and continuously variable gain amplifier (VGA). Nominally the IF strip takes 15mA from 3.3V. The pre-filter PGA slides the dynamic range of the BPF to best fit the needs of the received signal. For a weak received signal, the PGA gain is increased to a maximum of 30dB to lower the noise contributed by the IF strip, mainly arising in the active filter. When the desired channel is strong, pre-filter gain is lowered to improve the IP3 of the BPF referred to the receiver input. However, when strong in-band interferers accompany a weak desired signal, the dynamic range and power consumption are stepped up. The PGA gain is lowered to suppress intermodulation, and an auxiliary BPF is substituted with 10dB lower NF but 10× higher current to maintain high SNR in the desired channel. This infrequent condition only slightly raises average power consumption in long-term use.

Demodulation of 64-QAM is sensitive to jumps in signal amplitude during a data packet. After a frequency hop, the post-filter PGA with 60dB range but 3dB resolution coarsely sets the receiver gain during the preamble. Then over the data sector, a continuous VGA tracks the channel path loss, estimated to vary by no more than ±10dB over a frame. This coarse-fine scheme best combines the power-efficient PGA with a VGA. The digital demodulator supplies AGC feedback after detecting the signal level relative to the A/D full-scale [3]. Figure 8.5.4a shows the circuit of a VGA stage. As described in Reference [2], the wideband BPF with variable BW is realized with a LPF in series with a HPF. All the blocks of the IF strip are in common-centroid layout to reject stray feedback through the substrate. No instability is observed during measurements on the packaged chip at post-filter gains as large as 85dB (Figure 8.5.4b).

This receiver IC occupies 20mm² implemented in 0.6μm 3M1P CMOS. Nominal current consumption is 50mA from 3.3V, rising to 100mA when the auxiliary filter is enabled. The measured minimum cascade NF is 8.9dB, and cascade IIP3 is higher than −10dBm.

The IF2 output of this receiver is digitized by a 10b ADC, and applied to an adaptive digital QAM demodulator [3]. The digital circuit operates at a maximum of 5Mbaud. For 10^{-6} BER, 16-QAM must be received with 21.5dB SNR, and 64-QAM with 27dB SNR. With -71.5dBmRF input level, the demodulator reconstructs a 64-QAM, 5 Mbaud (30Mb/s) constellation with 27dB SNR. This corresponds to receiver NF of 8.9dB. Figure 8.5.5 shows the levels of blockers within the ISM band, such as microwave oven emissions, and two-tone interferers, which desensitize the receiver by 3dB at fixed gain.

The receiver sliding dynamic range for 16-QAM, 5Mbaud is measured by adjusting the gains in the RF mixer, IF1 amplifier, and pre-filter PGA for best sensitivity, as a function of rising interferer levels (Figure 8.5.6a,b). The interferers lie in the ISM band, but after downconversion fall in the stopband of the on-chip BPF. NF and IIP3 deduced from the sensitivity and two-tone test are shown in Figure 8.5.6b.

References:
[1] F. Behbahani, Y. Kishigami, J. Leete, and A. A. Abidi, "CMOS 10MHz-IF Downconverter with On-Chip Broadband Circuit for Large Image-Suppression," in *Symp. on VLSI Circuits*, Kyoto, Japan, pp. 83-86, 1999.
[2] F. Behbahani, W. Tan, A.Karimi, A. Reithmeier, and A. A. Abidi, "A Wideband Tunable CMOS Channel-Select Filter for a Low-IF Wireless Receiver," in *Custom IC Conf.*, San Diego, CA, pp. 501-504, 1999.
[3] J. S. Putnam and H. Samueli, "A 4 Channel Diversity QAM Receiver for Broadband Wireless Communications," in *Intl. Solid-State Circuits Conf.*, San Francisco, pp. 338-339,476, 1999.

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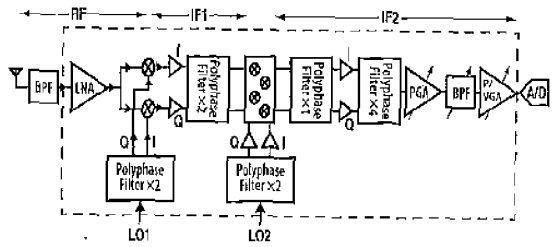

Figure 8.5.1: Block diagram of integrated dual-conversion receiver.

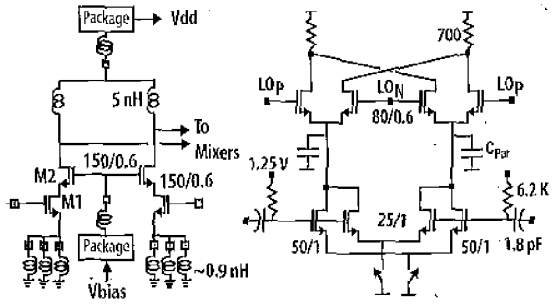

Figure 8.5.2: (a) Low noise amplifier, (b) First mixer circuits.

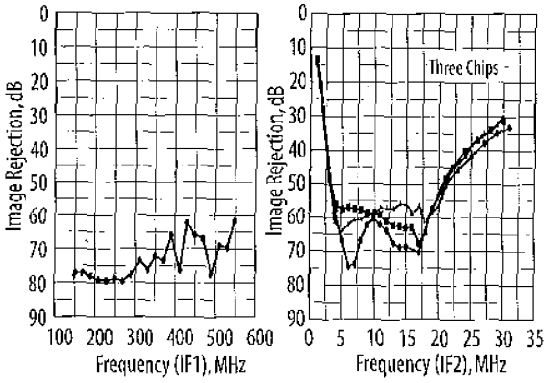

Figure 8.5.3: Measured image rejection at (a) first IF, (b) second IF.

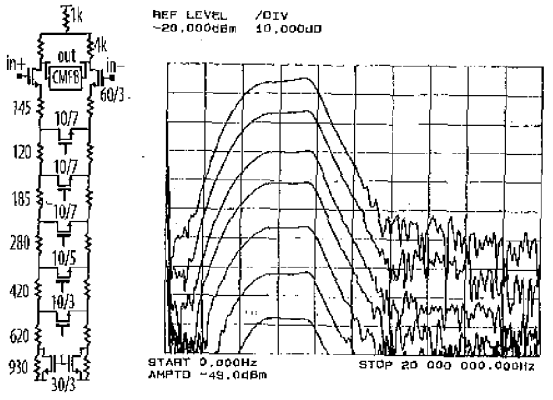

Figure 8.5.4: (a) One stage of VGA, (b) Measured frequency response of IF strip.

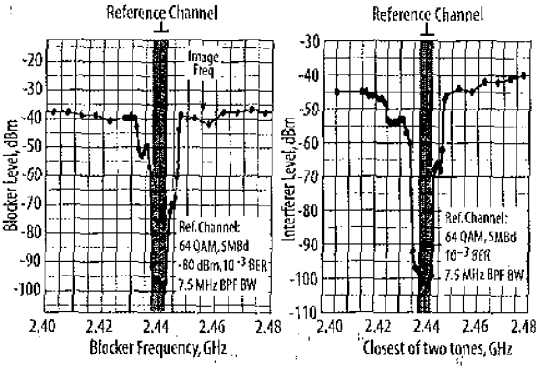

Figure 8.5.5: Measured tolerance to (a) single-tone, (b) two-tone interferers, at fixed gain.

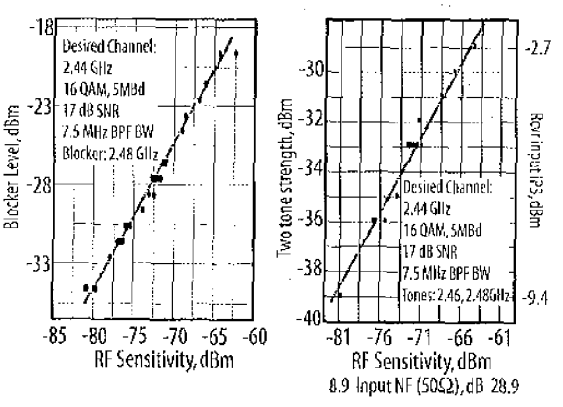

Figure 8.5.6: Measured sliding dynamic range for (a) single-tone, (b) two-tone interferers.

Figure 8.5.7: See page 452.

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