UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

VALEO SE and VALEO SCHALTER UND SENSOREN GMBH,

Petitioner,

v.

Foras Technologies Ltd.,

Patent Owner.

Case IPR2024-00823
Patent 7,502,958

PATENT OWNER'S PRELIMINARY RESPONSE TO THE PETITION

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Exhibit No.	Description
2001	Declaration of Nigel Jones (previously filed as EX2007 in IPR2023-01373)
2002	Nigel Jones CV (previously filed as EX2008 in IPR2023-01373)
2003	Deposition Transcript of Michael C. Brogioli (previously filed as EX2009 in IPR2023-10373)

I. INTRODUCTION

Petitioner has failed to show reasonable likelihood of success in demonstrating any of the challenged claims of U.S. Patent Number 7,502,958 is obvious. Its single ground is premised on a fatally flawed obvious combination that would not achieve the results it contends would motivate a POSITA to create it.

II. OVERVIEW

A. The '958 Patent

The '958 patent describes a method for providing firmware recoverable lockstep protection. The method comprises, for example, detecting loss of lockstep for a pair of processors; triggering, by firmware, an operating system to idle the processors; and recovering, by firmware, lockstep between the pair of processors. EX1001, 4:14-55. The '958 patent further discloses determining whether lockstep is recoverable based on a determination, by firmware, of a mismatch error in a pair of processors. EX1001, 5:49-62.

B. Claim Construction

For purposes of *inter partes* review, disputed claim terms are construed to give them "the meaning that the term would have to a person of ordinary skill in the art in question at the time of the

invention." *See* 83 Fed. Reg. 51341 (Oct. 11, 2018) (adopting the standard of *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312-13 (Fed. Cir. 2005)). The proper construction is considered in the context of, and must be consistent with, the specification—and the claim language should be read in light of the specification as it would be interpreted by one of ordinary skill in the art. *See, e.g.*, *Phillips*, 415 F.3d at 1313.

Petitioner has proposed that the terms "detection of loss of lockstep" and "detecting loss of lockstep" should be construed to include both mismatch errors and errors that may eventually result in mismatch errors constituting a "precursor to lockstep mismatch" – including at least one of (1) detecting a lockstep mismatch error; and (2) detecting an error that may eventually cause a lockstep mismatch error. Pet. at 17.

Petitioner has also proposed that the terms "lockstep is recoverable" and "loss of lockstep is recoverable" should be construed as "lockstep is recoverable from the detected loss of lockstep." Pet. at 19.

Patent Owner does not believe either term requires construction, because, as shown below, Petitioner fails to demonstrate obviousness regardless of how these terms are construed.

C. Person of Ordinary Skill in the Art

A person of ordinary skill in the art of the subject matter of the '958 patent would have the equivalent of a bachelor's degree in Computer Science, Computer Engineering (or a related field) and approximately two years of work experience with computer architecture design. Additional education in the field could be substituted for industry experience, and vice versa.

D. Obviousness

Whether a patent claiming a combination of prior art elements would have been obvious is determined by whether the improvement is more than the predictable use of prior art elements according to their established functions. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007). To reach this conclusion, however, requires more than a mere showing that the prior art includes separate references covering each separate limitation in a claim under examination. *Unigene Labs., Inc. v. Apotex, Inc.*, 655 F.3d 1352, 1360 (Fed. Cir. 2011). Rather, obviousness requires the additional showing that a person of ordinary skill at the time of the invention would have selected and combined those prior art elements in the normal course of research and development to yield the

claimed invention. *Id.* "To satisfy its burden of proving obviousness, a petitioner cannot employ mere conclusory statements. The petitioner must instead articulate specific reasoning, based on evidence of record, to support the legal conclusion of obviousness." *In re Magnum Oil Tools Int'l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016); *see In re NuVasive, Inc.*, 842 F.3d at 1383 (stating that "conclusory statements" amount to an "insufficient articulation[ ] of motivation to combine"; "instead, the finding must be supported by a 'reasoned explanation'").

The absence of evidence of any benefit of an asserted combination of references is strong evidence against obviousness. As the Court explained in *KSR*:

> Although common sense directs one to look with care at a patent application that claims as innovation the combination of two known devices according to their established functions, *it can be important to identify a* ***reason*** *that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does*. This is so because inventions in most, if not all, instances rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known.

KSR Int'l Co. v. Teleflex Inc., 550 U.S. 398, 418–19 (2007) ; *see also id.* at 424 ("The proper question to have asked was whether a [POSITA] . . . would have seen a ***benefit*** to upgrading Asano with a sensor."); *Ex Parte Debates*, Appeal No. 2020-006536, 2022 WL 263587, at *4 (PTAB Jan. 27, 2022) (reversing examiner's obviousness rejection because it was "too general and [was] not tailored to explaining why one skilled in the art would have seen the ***benefit*** of modifying Lerner's electronic device and tag reading method to include the specific overlay features of Detlefsen"); *Duo Sec. Inc. v. Strikeforce Techs., Inc.*, IPR2017-01041, 2017 WL 4677235, at *9 (PTAB Oct. 16, 2017) (finding no motivation to combine where "Petitioner never identifies or explains adequately any ***benefit or improvement*** gained by adding Falk, and specifically, Falk's relevant message, to the proposed combination of Feigen and Bulfer"); *Ex Parte Brillowska-Dabrowska*, Appeal No. 2016-006485, 2016 WL 4525004, at *4 (PTAB Aug. 24, 2016) (reversing rejection based on a combination of references where it was "unclear why" the combination "would be particularly useful").

As the Federal Circuit has recognized, it is not sufficient to show that two references could be combined. *See Personal Web Techs., LLC v.*

Apple, Inc., 848 F.3d 987, 993 (Fed. Cir. 2017) (it is not enough to show that "a skilled artisan, once presented with the two references, would have understood that they ***could*** be combined"); *Apple, Inc. v. Realtime Data LLC*, IPR2016-01737, 2018 WL 1326656, at *25 (PTAB Mar. 13, 2018) (granting motion to amend because petitioner did not adequately "articulate a *reason why* a person of ordinary skill in the art would combine the prior art references") (citing and quoting *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015) ("obviousness concerns whether a skilled artisan not only *could have made* but *would have been motivated to make* the combination or modifications of prior art to arrive at the claimed invention")) (emphases in original).

E. Bigbee (EX1005)

Petitioner sets forth only one ground of unpatentability relying primarily on a reference presented as Exhibit 1005 ("Bigbee"), which describes "[a] method and apparatus for functional redundancy check mode recovery." EX1005 at Abstract. Bigbee describes a scheme in which the hardware includes FRC logic that detects an error in an individual processor core:

> In one embodiment, hardware **102** includes two or more processor packages, where each physical processor package

> includes two or more physical processor cores operating in lock step in FRC mode as a single logical processor from the point of view of operating system **106**. Hardware **102** of the disclosed embodiment further includes FRC logic. FRC logic detects errors within individual processor cores of the described embodiment which causes hardware **102** to break lock step between at least two processor cores within a processor package, disabling FRC mode operation. Hardware **102** then disables any of the package's error containing cores, placing them into a "zombie" state, and generates a recoverable machine check exception. The generated machine check exception in turn triggers the execution of a processor error handler within a PAL of one of the package's error-free cores.

EX1005 at ¶19. Bigbee describes a scheme in which a system can detect an error in one of the individual processor cores, disable that processor core, and ultimately eject the processor. *See id.* at ¶¶35-36; *id.* at Fig. 4A.

F. Nguyen (EX1006)

Petitioner relies on a second reference presented as Exhibit 1006 ("Nguyen"), which describes a scheme for processing lockstep errors. Nguyen determines an error is non-recoverable <u>only</u> when (1) a mismatch error is detected and (2) a soft error (e.g., individual processor error) is <u>not</u> detected either before, or within a timeout interval after, a mismatch error is detected. EX1006 [0005], [0007], [0023]-[0024], [0030], [0046] ; Pet. 40-41; EX1002 ¶ 106. Outside of these conditions (e.g., whenever an

individual error is detected prior to detection of a mismatch error), Nguyen will not determine that the error is non-recoverable. *Id.* When Nguyen detects an error from an individual processor, it disables error detector 140 (used to detect mismatch errors) and directly activates recovery module 150 to implement a recovery routine. EX1006 at [0022]-[0023].

III. THE CHALLENGED CLAIMS ARE NOT OBVIOUS OVER BIGBEE IN VIEW OF NGUYEN

A. A POSITA would not have been motivated to combine Bigbee and Nguyen

Petitioner presents only a single ground based on a proposed combination of two references, Bigbee (EX1005) and Nguyen (EX1006). Petitioner admits that Bigbee does not disclose "those elements that require determining if the lockstep of a lockstep processor pair is recoverable." Pet. 18. In claim 1, for example, these include "determining if lockstep is recoverable" and "wherein said firmware code for determining if the lockstep is recoverable further comprises firmware code for determining if a lockstep mismatch has occurred between the pair of lockstep processors." Independent claim 19 similarly recites "firmware code … for determining if the lockstep is recoverable" and

"wherein said firmware code … further comprises firmware code for determining if a lockstep mismatch has occurred." Thus, to fill the admitted gap in Bigbee's disclosures, Petitioner argues that a POSITA would have been motivated to add certain features from Nguyen to Bigbee and create a "combined system." Pet. 26-27.

Petitioner's obviousness theory is based on its contention that a POSITA would have recognized that "[b]ecause different responsive actions should be taken to handle each of nonrecoverable and recoverable errors, determining whether the error is recoverable or non-recoverable is critical to reduce the impact of the errors on the system" and that "it is critical to handle recoverable errors differently from non-recoverable errors." Pet. 27-28. Thus, Petitioner contends that by adding Nguyen to Bigbee, a POSITA would recognize that the combined system would be able to "handle both recoverable and non-recoverable lockstep errors." Pet. 27.

Petitioner's proposed Nguyen-Bigbee "combined system" is shown through annotated figures from Bigbee that include additions from Nguyen. Pet. 26-27 ("The combined system … would be as follows:").

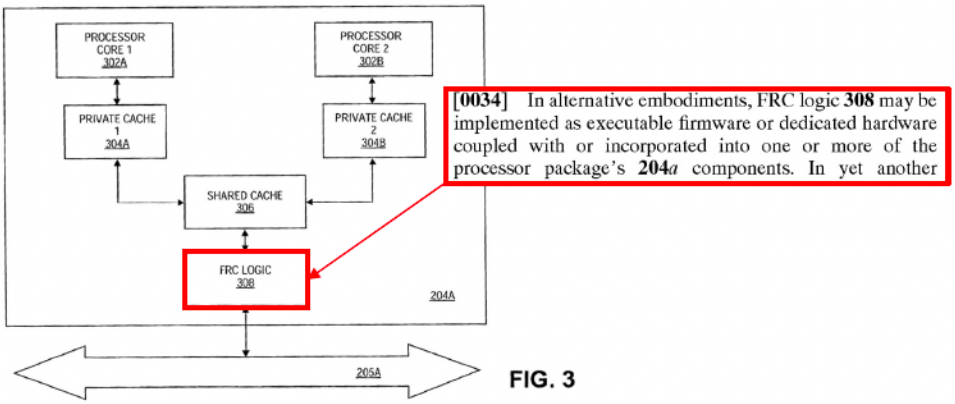
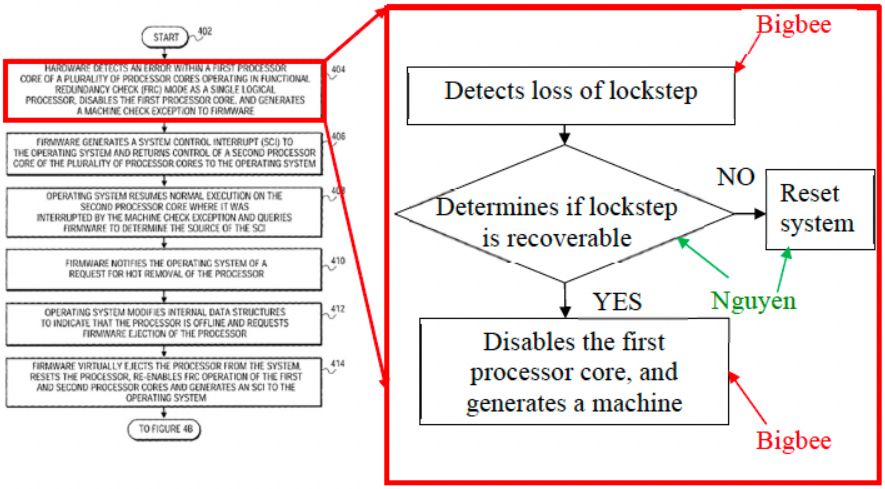


FIG. 3

Pet. 26 (annotations in Petition).



Pet. 27 (annotations in Petition); *see also* EX1002 ¶¶84-86 (describing the "Bigbee-Nguyen system" as "[t]aking step 404 of Bigbee's Figure 2 (sic),[1]

[1] Dr. Brogioli confirmed during deposition in IPR2023-01373 that "Figure 2" was a typographical error and that he meant to reference Figure 4A of Bigbee. EX2003 (Brogioli Dep.) at 74:14-75:9.

and adding Nguyen's step of determining whether lockstep is recoverable after Bigbee detects loss of lockstep"); EX2003 (Brogioli Dep.) at 74:14-76:8 ("So here in block 404 of Figure 4a of Bigbee is where Bigbee's hardware detects an error within the first processor core…And this is the step in which I incorporate the – determining if that lockstep is recoverable using the portion from the Nguyen reference.") *see also id.* at 78:11-21.

These descriptions in the Petition, Dr. Brogioli's declaration, and Dr. Brogioli's testimony show that Petitioner's "combined system" allegedly follows the following process. It begins with step 404 in Bigbee's Figure 4A, which says "HARDWARE DETECTS AN ERROR WITHIN A FIRST PROCESSOR CORE OF A PLURALITY OF PROCESSOR CORES." Following this detection, which Petitioner annotates as "Detects loss of lockstep," the combined system performs a step from Nguyen that Petitioner labels "Determines if lockstep is recoverable." Pet. 27; EX1002 ¶ 85; EX2001 ¶ 29. If the system determines that lockstep is recoverable (i.e., the "YES" determination in Petitioner's annotations to Figure 4A of Bigbee), the combined system proceeds with the remainder of step 404 from Bigbee, beginning with "disables the first

processor core, and generates a machine check exception to firmware." *Id.*; *see also* EX2003 (Brogioli Dep.) at 76:10-77:11. If Nguyen's determination is that lockstep is not recoverable (i.e., the "NO" determination in Petitioner's annotations to Figure 4A of Bigbee), the "combined system" follows Nguyen's process to "reset system." *Id.*

A critical flaw in Petitioner's combination is that—as Bigbee expressly discloses, and Petitioner's expert acknowledged—the recovery process begins after Bigbee has detected an "error within a first processor." EX1005 Fig. 4A (block 404); EX2003 (Brogioli Dep.) 74:14-76:8; EX2001 ¶ 27. As explained below, this means that Nguyen will never determine that lockstep is non-recoverable. Every error processed by Nguyen's "determines if lockstep is recoverable" routine will be handled the same way, i.e., it will follow the "YES" path shown in Petitioner's annotations to Figure 4A and proceed through the remainder of Bigbee's routing for attempting to recover from recoverable individual processor errors. EX2001 ¶ 29-30.

This outcome is the result of how Nguyen's "determination" process works. As Petitioner and its expert readily acknowledge, Nguyen determines a lockstep error is non-recoverable only when (1) a mismatch

error is detected and (2) a soft error (e.g., individual processor error) is not detected before, or within a timeout interval after, a mismatch error is detected. EX1006 [0005], [0007], [0023]-[0024], [0030], [0046] ; Pet. 37; EX1002 ¶ 106. Outside of these conditions—e.g., whenever an individual error is detected prior to detection of a mismatch error—Nguyen will not determine that lockstep is non-recoverable. *Id.* Indeed, when Nguyen detects an error from an individual processor, it disables error detector 140 (used to detect mismatch errors) and directly activates recovery module 150 to implement a recovery routine. EX1006 at [0022]-[0023].

In Nguyen, Error Detector 140 receives signals from error pipeline 128, which represents the logic that detects errors in the data. EX1006 at [0021]; EX2001 ¶ 32. As Nguyen describes, "soft errors in these arrays may appear as parity or ECC error flags when the corrupted data is accessed." *Id.* Bigbee similarly describes that errors in an individual processor can be "error correcting code (ECC) errors…or parity errors." EX1005 [0018]. And Dr. Brogioli similarly explained that "a digital bit within a processor that has – is the wrong value, but that can be corrected, perhaps internally, using parity bits or things like that" is an example of a "soft error." EX2003 (Brogioli Dep.) at 14:18-15:10; *see also*

EX1002 ¶ 81. As Dr. Brogioli also recognized, Bigbee's individual processor errors are recoverable. *Id.*; EX2001 ¶ 29.

As a result, the Nguyen-Bigbee "combined system" that Petitioner says would be obvious, is a system without any mechanism for handling recoverable errors differently from non-recoverable errors. Nguyen's alleged "determination" technique would not, as combined with Bigbee, have any capability to distinguish recoverable from non-recoverable errors. It would provide none of the "critical" benefits of handling recoverable and non-recoverable errors differently that Petitioner says a POSITA would recognize. Accordingly, a POSITA would readily recognize that the Nguyen-Bigbee "combined system" provides <u>no benefit</u> in terms of distinguishing recoverable from non-recoverable errors, does not allow non-recoverable errors to be treated differently from recoverable errors.

In addition, Petitioner's contention that it would have been obvious to "implement Nguyen's determination of whether the detected error causing the loss of lockstep is recoverable by Bigbee's firmware FRC logic" is flawed because Petitioner has not shown that implementing, in ***firmware***, the portions of Nguyen on which it relies would have been obvious. Pet. 27; EX1002 ¶86 (arguing it would be obvious to "modify

Bigbee's firmware FRC logic to perform Nguyen's disclosed determination of whether lockstep is recoverable"). As Mr. Jones explains, "[a] person of skill in the art would recognize that implementing Nguyen's 'FRC checker's compare unit' in firmware code would be impractical for several reasons. First, detecting errors by comparing data from both cores using firmware would require a separate processor running approximately twenty times faster than the processor cores being monitored. This adds complexity and expense. Second, proving by formal methods that firmware configured to perform bit-by-bit error checking is operating correctly is much more difficult than proving the same for a hardware implementation. This means that it is more difficult to assure reliable performance in a firmware implementation compared to a hardware implementation. Third, firmware is more vulnerable than hardware to malicious attacks, which a person of skill in the art would consider as highly relevant in a system designed for reliability." EX2001 ¶32.

Petitioner's additional contention that firmware would be desirable for implementing the relevant features of Nguyen due to its flexibility and ease of modification is also unsupported. Those qualities would not

be viewed as desirable in the context of Nguyen's error detection hardware. In fact, as Mr. Jones explains, "a person of skill in the art would recognize that when reliability, speed, stability, and accuracy are import—which they would be in this context—the flexibility and ease of modification of firmware serve to introduce more opportunities for error, which is undesirable. A person of skill in the art would recognize that in a system designed to provide "high levels of reliability and availability," (Ex. 1006 at [0004]) an implementation that can be easily modified is undesirable because it introduces more opportunities for intentional or unintentional errors." EX2001 ¶33. Similarly, Petitioner's contention that a firmware implementation of Nguyen would have been "obvious to try" fails because it does not recognize the above-mentioned disadvantages of using firmware in this context, which would have "affirmatively dissuaded [a POSITA] from using it." *Id.*

Petitioner has fallen far short of its burden to prove obviousness. The Nguyen-Bigbee "combined system" fails to achieve the benefits Petitioner contends would motivate a POSITA and instead introduces more vulnerabilities to the system. A POSITA would have no motivation to implement this "combined system" and would instead recognize that it

would hurt Bigbee's reliability and availability without any benefit. Absent any evidence of motivation to combine Bigbee and Nguyen, Petitioner can only arrive at its conclusion of obviousness using improper hindsight reconstruction of the challenged claims. *See In re NTP, Inc.*, 654 F.3d 1279, 1299 (Fed. Cir. 2011) ("Care must be taken to avoid hindsight reconstruction by using 'the patent in suit as a guide through the maze of prior art references, combining the right references in the right way so as to achieve the result of the claims in suit.'") (quoting *Grain Processing Corp. v. American–Maize Prods. Co.*, 840 F.2d 902, 907 (Fed. Cir. 1988)).

Because Petitioner has not shown that a POSITA would have been motivated to combine Nguyen and Bigbee into the "combined system" Petitioner proposes, and because Petitioner relies on this combination for every challenged claim, Petitioner has not shown reasonable likelihood that any challenged claims would have been obvious.

B. The Bigbee-Nguyen combination does not render obvious "if determined that a lockstep mismatch has occurred between the lockstep pair of processors, then determining that the loss of lockstep is not recoverable."

In addition to the reasons provided above in §III.A, Petitioner has also failed to show that claim 8 is obvious in view of Bigbee and Nguyen. In particular, Petitioner has not shown that the Nguyen-Bigbee "combined system" ever makes a determination that "loss of lockstep is not recoverable." As previously described, the Nguyen-Bigbee "combined system" handles each error the same way and, because it begins with Bigbee's detection of a recoverable error in an individual processor, it never determines that any loss of lockstep is not recoverable. EX1006 [0005], [0007], [0023]-[0024], [0030], [0046]; Pet. 36-37; EX1002 ¶ 106.

Date: July 29, 2024

Respectfully submitted,

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CERTIFICATION REGARDING WORD COUNT

Pursuant to 37 C.F.R. § 42.24(d), Patent Owner certifies that there are no more than 3630 words in the paper excluding the portions exempted under 37 C.F.R. § 42.24(a)(1).

Dated: July 29, 2024

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CERTIFICATE OF SERVICE (37 C.F.R. § 42.6(e))

The undersigned hereby certifies that the above document was served on July 29, 2024, by filing this document through the Patent Trial and Appeal Case Tracking System as well as delivering a copy via electronic mail upon the following attorneys of record for the Petitioner:

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