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A low power 2.4 GHz transceiver for ZigBee applications*

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Abstract: This paper presents a low power 2.4 GHz transceiver for ZigBee applications. This transceiver adopts low power system architecture with a low-IF receiver and a direct-conversion transmitter. The receiver consists of a new low noise amplifier (LNA) with a noise cancellation function, a new inverter-based variable gain complex filter (VGCF) for image rejection, a passive quadrature mixer, and a decibel linear programmable gain amplifier (PGA). The transmitter adopts a quadrature mixer and a class-B mode variable gain power amplifier (PA) to reduce power consumption. This transceiver is implemented in 0.18 μm CMOS technology. The receiver achieves -95 dBm of sensitivity, 28 dBc of image rejection, and -8 dBm of third-order input intercept point (IIP3). The transmitter can deliver a maximum of $+3$ dBm output power with PA efficiency of 30%. The whole chip area is less than 4.32 mm². It only consumes 12.63 mW in receiving mode and 14.22 mW in transmitting mode, respectively.

Key words: low power; noise cancellation; quadrature mixer; transceiver; variable gain complex filter

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1. Introduction

In recent years, low power has become one of main challenges for wireless short-range communication devices. The low power wireless transceiver is a significant feature to prolong device service life. The IEEE 802.15.4 (ZigBee) standard is one of the low cost and low power short-range wireless communication standards^[1]. It supports three operation frequency bands (868 MHz/915 MHz/2.4 GHz). The maximum chip and data rates are 2 Mchip/s and 250 kbps, respectively. Recently, some CMOS transceivers based on the standard have been reported^[2–9]. The zero-IF receiver architecture was used to reduce the power consumption of the receiver circuit^[2]. However, it requires extra complexity circuits and much power to overcome its drawbacks, such as DC offset, flicker noise and high LO leakage. Another receiver adopted a current-reused low noise amplifier (LNA), a mixer and a VCO to reduce power^[5]. Nevertheless, the noise and linearity are limited due to the stack of transistors. The VCO-based two-point modulation transmitter can be used in constant envelope modulation to avoid using an up-conversion mixer^[7]. However, inherent gain and phase mismatches always exist in two modulation points, which may lead to serious EVM loss^[8]. Although the transceiver achieves ultra-low power in sleep mode using an optimal operation process^[9]. Unfortunately, it still dissipates much power in active mode.

In this paper, a low power 2.4 GHz transceiver is presented for ZigBee applications. This transceiver adopts low power system architecture with a low-IF receiver and a direct-conversion transmitter. Some novel circuits are proposed to reduce the power consumption and chip area of the transceiver.

An LNA with a noise cancellation function and a passive quadrature mixer are combined to constitute a novel receiver front-end circuit block. It can reduce the noise figure (NF) and the power consumption of the front-end block efficiently. To improve image rejection performance and receiver sensitivity, a new variable gain complex filter (VGCF) circuit with an automatic frequency tuning function is proposed. The decibel linear programmable gain amplifier (PGA) adopts resistor-feedback to achieve high linearity and constant bandwidth. It can provide a wide gain range with a 3 dB gain step. The transmitter consists of a quadrature mixer and a variable gain power amplifier (PA) for minimum shift keying (MSK) modulation. The mismatch calibration circuit is applied in this mixer to reduce amplitude and phase errors. The PA adopts a cascode amplifier at the driver stage and a class-B mode push-pull amplifier at the output stage to improve PA efficiency and reduce power consumption.

2. Transceiver architecture

The key specifications of the transceiver are sensitivity, linearity, image rejection, transmit power, and transmitter spectral density mask. The proposed low power transceiver is shown in Fig. 1. It mainly includes: the receiver, the transmitter, the frequency synthesizer, and nonvolatile memory (NVM). Some novel key circuit blocks are proposed to reduce power consumption and chip area.

The zero-IF receiver and low-IF receiver are suitable for low power signal-chip transceiver design. As is well known, the zero-IF receiver requires extra auxiliary circuits and consumption power to relieve those drawbacks^[10]. Moreover,

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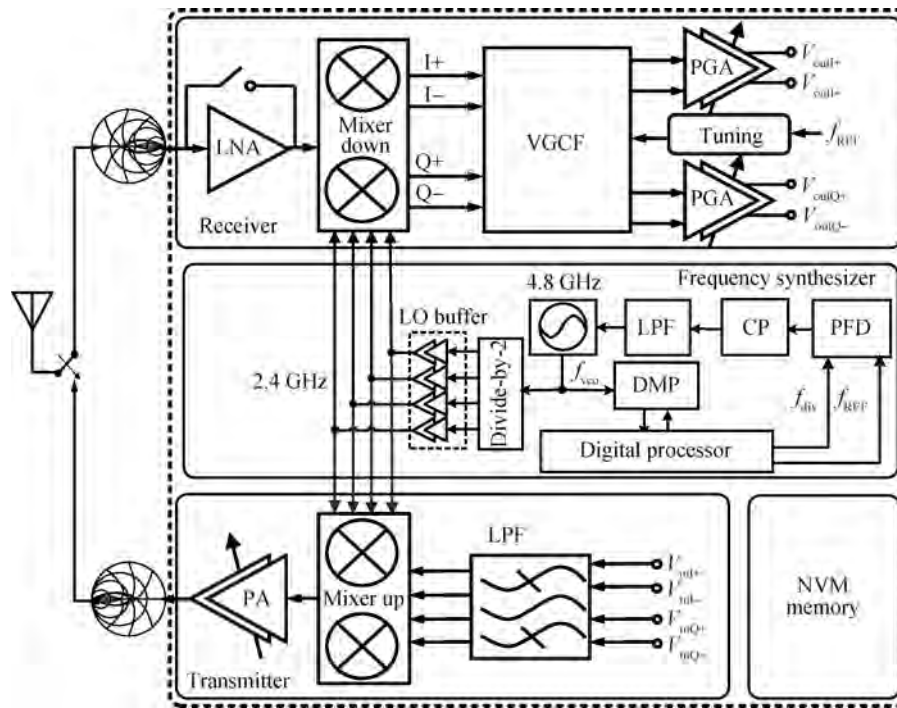


Fig. 1. System architecture of the proposed transceiver.

MOSFET devices inherently have a large $1/f$ noise which deteriorates the receiver noise performance. For a wireless communication system with a narrower bandwidth, the low-IF receiver can better solve the above problems. This proposed low-IF receiver mainly includes: a novel low noise, low power RF front-end block, a novel variable gain complex filter (VGCF), a passive quadrature mixer, and PGAs. The receiver front-end circuit block consists of an LNA with a noise cancellation function and a passive quadrature mixer. The proposed LNA with a noise cancellation function can improve the noise performance and conversion gain, and can operate in high and low gain modes. In low gain mode, the LNA is shut down to consume no dc power. The passive quadrature mixer also consumes no dc power. To improve the image rejection performance and sensitivity of this architecture, the inverter-based VGCF with automatic frequency tuning function is proposed. The linearity of the PGA is critical for the receiver. This decibel linear PGA is based on a resistor-feedback loop to improve high linearity. To achieve constant bandwidth, a digital-controlled Miller capacitor array is used in the PGA. Both PGAs can provide a wide gain range with 3 dB gain step. The linear-in-dB gain is controlled by a digital control word from the digital processor.

The direct-conversion transmitter can be integrated in a signal-chip without extra components. It consists of a passive low-pass filter (LPF), an up-conversion mixer, and a variable gain PA. Though the passive mixer draws no power from the supply voltage, it usually requires relatively large LO signals to the mixer's switching pair. The LO buffer will consume much more power. So this transmitter adopts an active mixer with resistive load to reduce consumption power and chip area. The mixer is based on quadrature double-balanced topology, which reduces LO leakage and suppresses the common mode interference. The PA is the power hungry part in the transmitter. The MSK modulation is considered as a constant envelope charac-

teristic, and the specification of error vector magnitude (EVM) is less than 35%. This PA adopts class-B push-pull amplifier as an output stage to improve PA efficiency. The RF signal outputs to a $50\ \Omega$ antenna through a matching network.

A frequency synthesizer is used to provide the 2.4 GHz quadrature LO quadrature signals for the transceiver. It consists of a phase frequency detector (PFD), a charge pump (CP), a third-order LPF, a stacked LC-VCO, a dual mode prescaler (DMP), a divide-by-2 circuit, and the digital processor. The VCO operates at 4.8 GHz. The LO signals can be achieved by using a divide-by-2 circuit. In order to reduce power consumption, the tail current of the LC-VCO is shared by the DMP and the divide-by-2 circuit. The ultra-low power NVM is based on the FN tunneling phenomenon and is compatible with standard CMOS processes. It is embedded to store the configuration and calibration data of the transceiver to save power in practical applications. The techniques were proposed by our research group and are very effective^[11, 12].

3. Low power circuit design

3.1. Receiver front-end

This proposed receiver front-end circuit is shown in Fig. 2. It consists of an LNA with a noise cancellation function and a passive quadrature mixer. The transistors M1 and M2 form a cascode amplifier. The transistor M3 is an auxiliary common-source amplifier. The transistor M4 is a switch for the selection of high and low gain mode. The L_S is a source degeneration inductor to reduce NF. The L_d and C_O are the output load inductor and capacitor, respectively. The resistor R_{B1} is used for biasing. The C_{in} and C_P are coupling capacitors. The output of the LNA is connected to one terminal of the differential input of the mixer via coupling capacitor C_d , and the other terminal

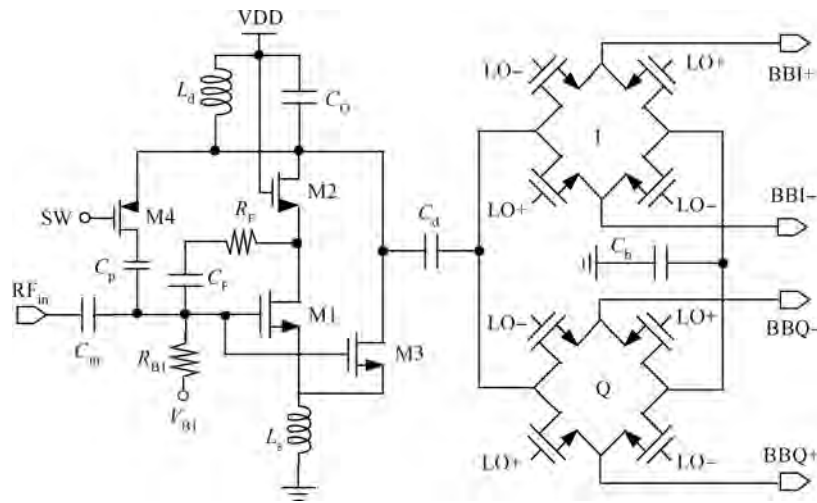


Fig. 2. The receiver front-end circuit.

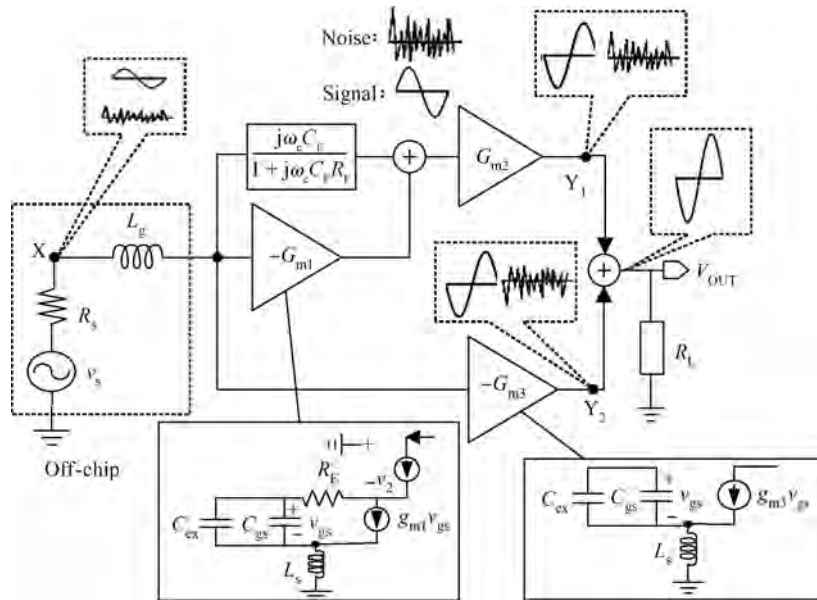


Fig. 3. Simplified small-signal model of the proposed LNA.

of the mixer is connected to ground through the bypass capacitor C_b .

The noise cancellation technique^[13] is applied in this LNA to reduce noise. In this paper, the noise cancelling circuit consists of the capacitor C_F , resistor R_F and transistors M1, M2 and M3. The C_F and R_F form the shunt negative feedback. The small signal circuit model of LNA is shown in Fig. 3. The input matching is implemented by inductor L_g . The input RF signal is amplified by G_{m1} , G_{m2} and G_{m3} . The noise cancellation is implemented by using a main amplifier M1 and M2, and auxiliary amplifier M3. The noise current $I_{n,M1}$ generates the noise voltages $V_{n,X}$, $V_{n,Y1}$, and $V_{n,Y2}$ at nodes X, Y1 and Y2. $V_{n,X}$ and $V_{n,Y1}$ have the same phase polarity. $V_{n,X}$ and $V_{n,Y2}$ have the opposite phase polarity. So the output noise voltage is given as:

$$V_{n,out} = I_{n,M1}(R_S + R_F - G_{m3}R_LR_S). \quad (1)$$

To cancel the output noise voltage introduced by M1, the

G_{m3} should be

$$G_{m3} = \frac{R_S + R_F}{R_LR_S}. \quad (2)$$

The M2 is a cascode transistor whose noise contribution can be neglected. So the noise factor F of the LNA can be written as

$$F = 1 + F_{M1} + F_{M3} + F_{RF}, \quad (3)$$

where F_{M1} , F_{M3} and F_{RF} refer to the noise factors of M1, M3 and R_F . The excess noise factors F_{M1} , F_{M3} and F_{RF} are mainly to quantify the noise contribution to F . When the noise of the input transistor M1 is canceled at the output, the noise factor is mainly determined by the resistor R_F and the transistor M3. The minimum NF of the transistor M3 can be achieved for inductively degenerated LNA^[14]. Under these conditions, the minimum noise factor of the LNA is determined as follows:

$$F_{min} = 1 + \frac{R_S}{R_F} + \frac{2}{\sqrt{5}} \frac{\omega}{\omega_T} \sqrt{\frac{\delta}{5\gamma}} (1 - |c|^2), \quad (4)$$

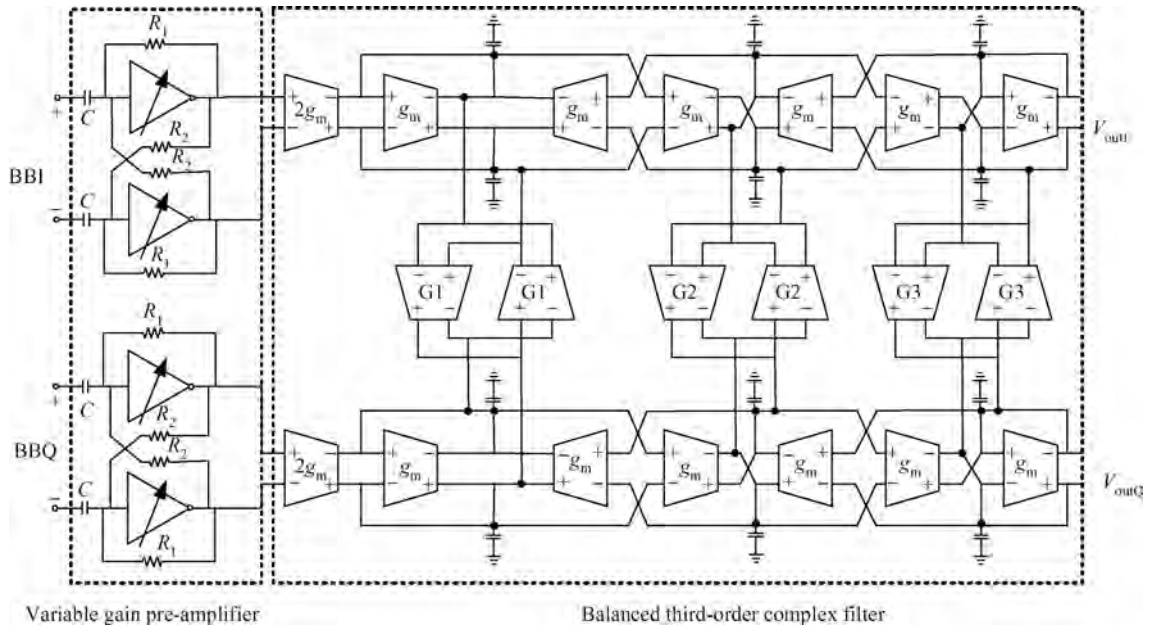


Fig. 4. Schematic of the VFCE.

where ω is equal to $1/\sqrt{L_g(C_{gs3} + C_F)}$; ω_T is equal to g_m/C_{gs3} ; δ, γ are constant; c is correlation coefficient between gate induced noise and channel noise.

The input impedance of the LNA is:

$$Z_{in} \approx j\omega(L_g + L_s) + \frac{1}{j\omega(C_{gs1} + C_{gs3} + C_F)} + \frac{g_{m1} + g_{m3}}{C_{gs} + C_{gs3}} L_s. \quad (5)$$

The input signal voltage V_X , V_{Y1} and V_{Y2} have the same phase polarity. The output signal voltage V_{OUT} is equal to $V_{Y1} + V_{Y2}$. Therefore, the overall voltage gain of the LNA can be derived as

$$A_v = \frac{V_{OUT}}{V_X} = -\left(G_{m1} + G_{m3} - \frac{1}{R_F}\right) R_L, \quad (6)$$

where R_L is the effective load impedance, which can be expressed as $R_L = \omega L_d Q_{Ld}$. Q_{Ld} is the Q -factor of L_d . $G_{m1} = g_{m1}g_{m2}r_o/(1 + g_{m2}r_o)$, $G_{m2} = 1$ and $G_{m3} = g_{m3}$. r_o is the output resistance of M1.

This passive quadrature mixer has high linearity, and dissipates no dc current. It uses a double-balanced topology to suppress the common mode interference and the LO leakage. The voltage conversion gain is equal to $2/\pi$. In order to achieve low NF, the switch capacitor should be large enough to provide a low switch resistance and reduce $1/f$ noise. However, it is a trade-off between the mixer noise performance and the gain of the LNA. If the switch capacitor is increased, the inductor must be decreased to keep the same resonant frequency of the load impedance. The gain of the LNA will decrease due to the lower inductor load. In this design, the optimum width of the switch transistor is set to be $10 \mu\text{m}$.

3.2. Variable gain complex filter

For ZigBee application, it requires 0 dB rejection at the adjacent channel (± 5 MHz) and 30 dB rejection at the alternate channel (± 10 MHz) for the receiver, respectively. The high

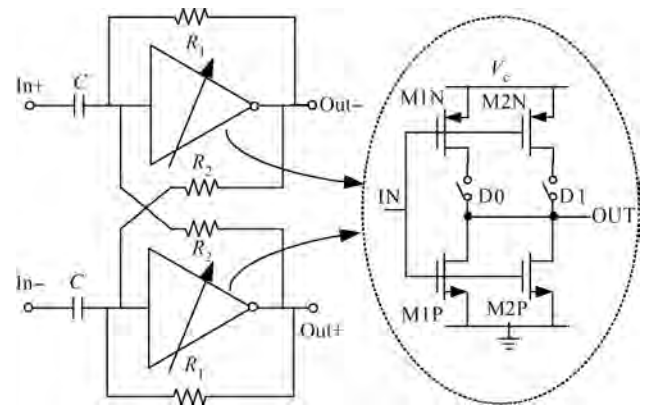


Fig. 5. Variable gain pre-amplifier.

performance of image rejection will improve the receiver robustness. This inverter-based VGCF can achieve a high image rejection value and consume low power. As shown in Fig. 4, it consists of a variable gain pre-amplifier and a balanced third-order complex filter.

The current signal from the down-mixer is converted to the voltage signal by the variable gain pre-amplifier. The pre-amplifier is based on a transimpedance amplifier (TIA) which consists of parallel inverters and resistive feedback loops, as shown in Fig. 5. The resistors R_1 and R_2 are used to maintain common-mode voltage stability and produce an effective resistance $R_1 R_2 / (R_2 - R_1)$. The effective resistance and the capacitor C form a high pass filter (HPF) to eliminate the DC-offset. This effective resistance allows a smaller capacitor C , thus both of the noise and area can be reduced^[15]. The voltage gain of the pre-amplifier can be derived as

$$A_v = \frac{V_{OUT}}{V_{in}} = 1 - (g_{MN} + g_{MP}) \frac{R_1 R_2}{R_2 - R_1}. \quad (7)$$

Its voltage gain can be controlled by adjusting the g_m of the

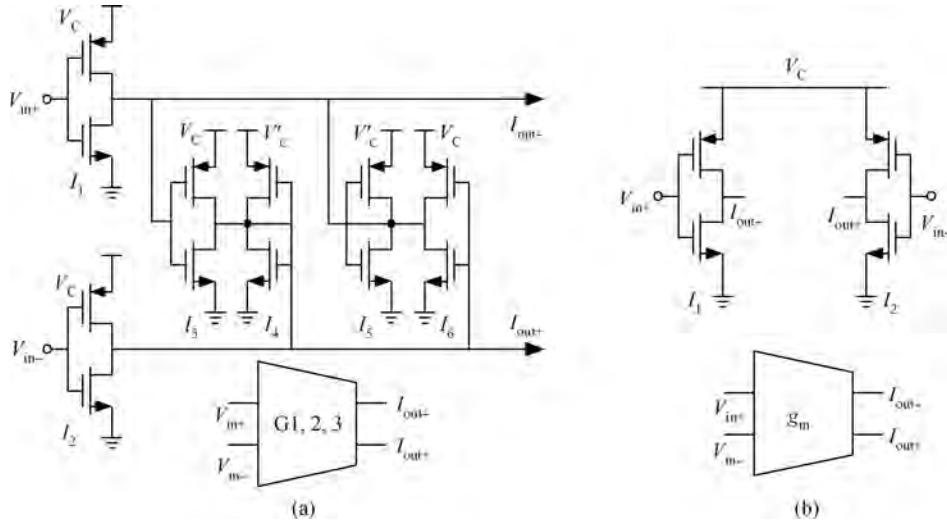


Fig. 6. (a) Nauta's transconductor. (b) Class-AB transconductor.

inverters. The switches D0 and D1 are used to control the amplifier operate at high and low gain modes. This pre-amplifier also can provide common-mode bias voltage for the complex filter.

The balanced third-order complex filter is used for image rejection and channel selection. The G_m - C filter topology was chosen to realize this complex filter, because it can not only filter image signal effectively, but also compensate filter insertion loss. In Fig. 6(a), the Nauta's transconductor is used in G1, G2 and G3 to achieve a third-order Butterworth complex filter^[16]. Inverters I3, I4, I5 and I6 are used to maintain output common-mode voltage stability and enhance the DC-gain. The class-AB transconductor is used in gm cells to reduce power consumption in Fig. 6(b). To compensate the inherent 6 dB insertion loss of the filter, the transconductance of the first input stage is set to $2g_m$. The VGCF is based on inverters which can consume very small current at low voltage supply. The whole VGCF can operate at 1.4 V supply.

The PLL-based automatic frequency tuning circuit is used to tune the cutoff frequency accurately and to improve the frequency response of the VGCF effectively. Since the frequency characteristic of the VGCF is determined by the C_m - C , the cutoff frequency can be tuned though locking $g_m/2\pi C$ to the reference frequency f_{REF} as follows:

$$f_{REF} = \frac{G_m}{2\pi C} = \frac{(V_c - V_{thn} - V_{thp})\sqrt{k_n k_p}}{2\pi C}, \quad (8)$$

where $k_n = \mu_n C_{ox} W_n/L_n$, $k_p = \mu_p C_{ox} W_p/L_p$.

To guarantee an accurate frequency response of the filter, the automatic PLL-based master-slave frequency tuning circuit is implemented, as shown in Fig. 7. It consists of a PFD, a CP, an LPF, a VCO, a V - I converter, and buffers. The VCO includes two stage G_m - C integrators which are same as the G_m - C integrators in the master block. The complex filter is used as a slave block. To correct the frequency response deviation caused by process, voltage and temperature (PVT) variations, automatic frequency tuning (F-tuning) is applied. Tuning of the quality factor (Q-tuning) is used to keep the VCO oscillating with constant amplitude to achieve a more exact filter response.

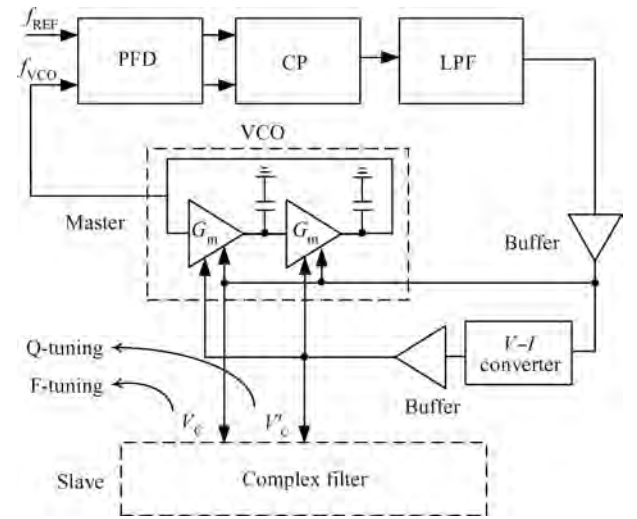


Fig. 7. Schematic of the PLL-based tuning circuit.

The voltage V_c and V'_c are used for F-tuning and Q-tuning, respectively. Built with Nauta's transconductor, the oscillating frequency and the quality factor of the VCO are controlled by V_c and V'_c , respectively^[16]. The combination of F-tuning and Q-tuning loops can also reduce power consumption and area. The G_m from the master VCO and slave complex filter has the same value of k_n and k_p . Since $g_m \propto V_c$ and $G_1 = \frac{1}{2}G_2 = G_3 \propto V_c$, the Nauta's transconductor and Class-AB transconductor can be tuned by a same control voltage V_c . Figure 8(a) shows the simulated frequency response variation without tuning at FF, SS and TT corner. The bandwidth and frequency of the complex filter are tuned simultaneously with tuning circuits in Fig. 8(b). The tuning accuracy of the complex filter can achieve less than 1%. It has good performance in terms of immunity to process variations.

3.3. Decibel linear PGA

The block diagram of a decibel linear PGA is shown in Fig. 9. The PGA consists of two cascaded amplifiers and an

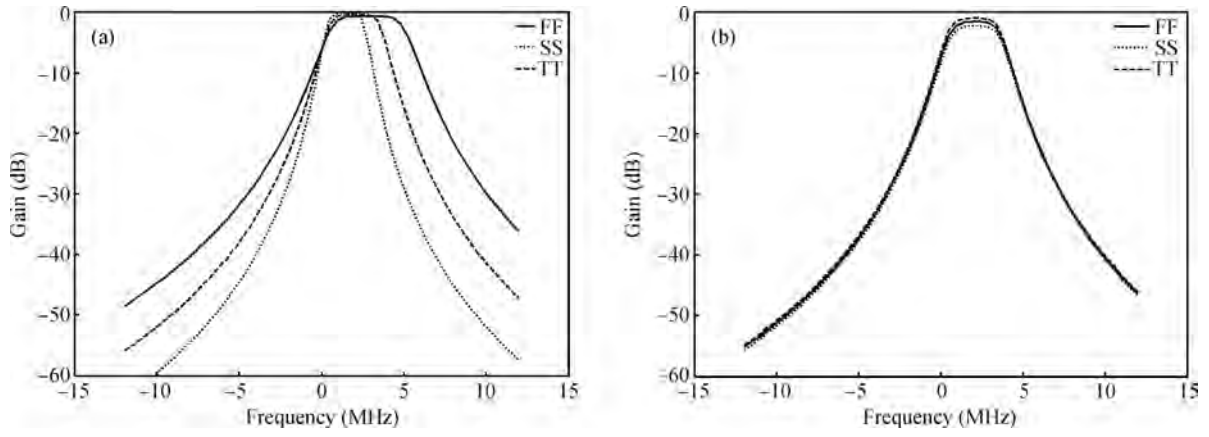


Fig. 8. (a) Frequency response without tuning. (b) Frequency response with tuning.

HPF at I/Q path. The passive HPF is used to cancel the DC offset and provide common-mode bias for the next stage. It consumes no dc power. Each amplifier is based on a high gain operational amplifier (OPAMP). It adopts switched-resistor feedback to achieve high linearity and wide dynamic range. The voltage gain A_{VP} and the bandwidth f_{BW} of the cascaded amplifier can be expressed as

$$A_{VP} = V_{out}/V_{in} = -R_{f-array}/R_{in}, \quad (9)$$

$$f_{BW} = g_{in}/2\pi C_C, \quad (10)$$

where g_{in} is the input transconductor of the OPAMP.

The linear-in-dB gain can be achieved by changing the feedback $R_{f-array}$. Each amplifier has 0–21 dB voltage gain range. The whole gain of the PGA can achieve maximum 42 dB voltage gain at I/Q path. The PGA gain is controlled in decibels linearly by 16 steps with a 3 dB step. To achieve constant bandwidth, the digital-controlled Miller capacitor array $C_{c-array}$ is used to keep a fixed bandwidth under different gain. It has a 16-step digital controller to compensate the deviations of the center frequency and the bandwidth due to PVT variations.

3.4. RF transmitter

The transmitter adopts a direct-conversion scheme. The baseband analog signal is filtered by an LPF, and then up-converted to the PA by a quadrature mixer. The up-conversion mixer of the I path is shown in Fig. 10. The first-order passive LPF is used to eliminate harmonic components from the digital-to-analog converter (DAC). It adopts a quadrature double-balanced topology to reduce the LO leakage and suppress the common mode interference. The mixer uses resistors as load to reduce area. Since the MOSFET devices inherently have mismatching characteristics, the mismatch calibration circuit is applied in this mixer. It has 5 bits switch bias current for each branch to compensate output amplitude and phase errors at the I/Q path.

For the MSK having the constant envelope characteristic, the nonlinear PA can be applied to reduce power and enhance PA efficiency. This variable gain PA is shown in Fig. 11. The inductance L_0 is used for input impedance matching for enhancing output voltage gain. The driver stage is a cascode amplifier which consists of transistors M1 and M2. The M2 is

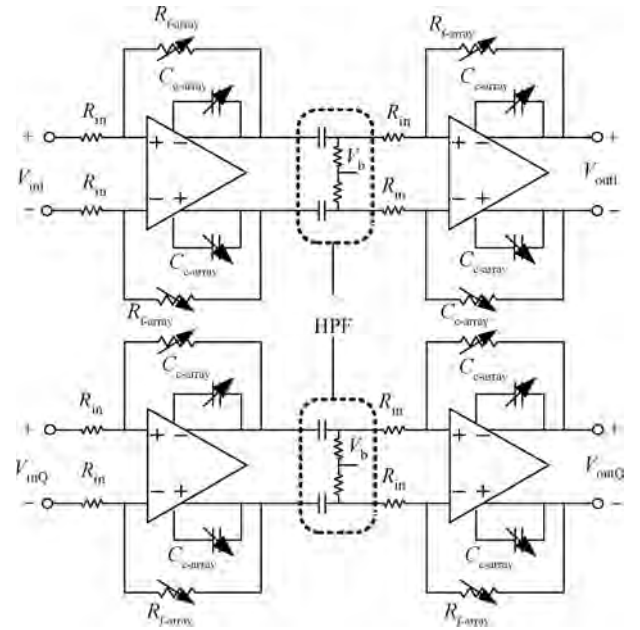


Fig. 9. Block diagram of the decibel linear PGA.

a thick gate-oxide transistor to increase its breakdown voltage^[17]. The variable bias current is used to adjust the gain of the PA. The gain range is from 0 to 20 dB. The output stage is a push-pull class B mode that mainly consists of transistors M5 and M6. Components R_B , R_{BP} and R_{BN} are bias resistors. Transistors M5 and M6 are biased in the sub-threshold to achieve low dc power and high PA efficiency. This PA can provide maximum 3 dBm output power at 1.8-V supply.

4. Measurement results

The proposed transceiver is implemented in 0.18 μm CMOS technology. The chip area is $1.8 \times 2.4 \text{ mm}^2$, as shown in Fig. 12. The total power consumption of the transceiver consumes only 12.63 mW in the receiving mode and 14.22 mW in the transmitting mode at 1.8-V supply, respectively.

At the receiver chain, the measured NF of the receiver is less than 8.5 dB within the baseband channel (from 1 to 3 MHz), as shown in Fig. 13. The measured frequency re-

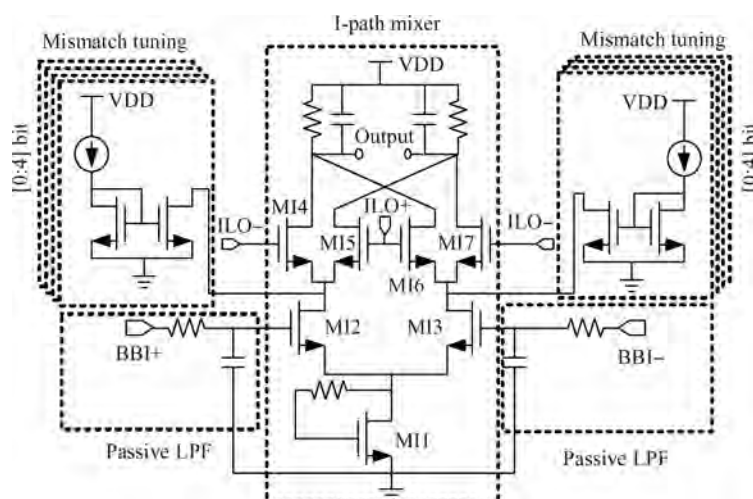


Fig. 10. Schematic of the up-conversion mixer of the I path.

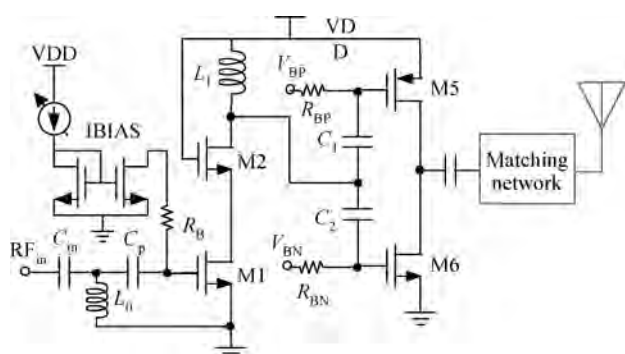


Fig. 11. Schematic of the power amplifier.

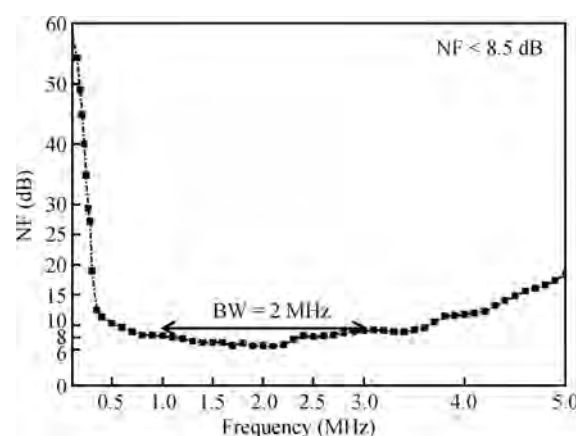


Fig. 13. Measured NF of the receiver.

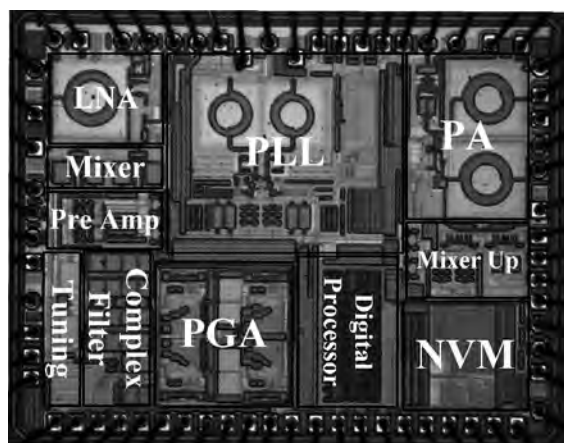


Fig. 12. The chip micrograph.

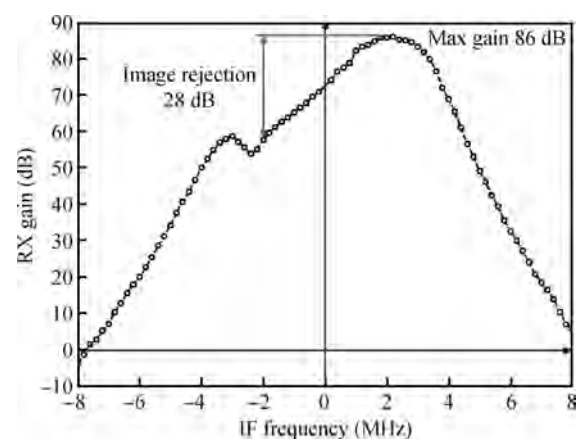


Fig. 14. Measured frequency response of the receiver.

sponse of the receiver from RF to the output of PGA is shown in Fig. 14. The maximum gain exceeds 86 dB, while the image rejection is approximately 28 dB. In the receiver path, the required sensitivity is defined in the IEEE 802.15.4 standard. The standard defines -85 dBm of minimum input signal and -20 dBm of maximum input signal that yields less than 1% packet error rate (PER). Good sensitivity and high image rejection can increase the communication range and reliability. The measured sensitivity is -95 dBm of minimum input sig-

nal and -9 dBm of maximum input signal through conjunction with ADC and digital demodulator from PCB test-board. The input signal dynamic range is from -95 to -9 dBm. The measurement results show that it is good enough to meet the specifications of the standard. The RF front-end circuit has a high gain mode with 21 dB and a low gain mode with -4 dB. The

Table 1. Measurement results.

Receiver/Transmitter		Current consumption (mA)		
IF frequency	2 MHz	Power supply	1.4–1.8 V	
Receiver AC gain	86 dB	Sub block	RX	TX
Receiver NF	< 8.5 dB	Synthesizer & buffer	3.5	3.5
Receiver sensitivity	−95 dBm	LNA & mixer down	1.25	—
Input P_{1dB}	0	Complex filter & tuning	0.83	—
Receiver IIP3	−8 dBm	PGA	1.42	—
Image rejection	28 dBc	Bias	0.2	0.1
Transmitter output power	+3 dBm	Mixer up	—	0.6
EVM	< 23%	PA	—	3.4
Phase noise @ 1 MHz	−108 dBc/Hz	Digital & NVM	0.3	0.3
PLL lock time	75 μ s	Total	7.5	7.9

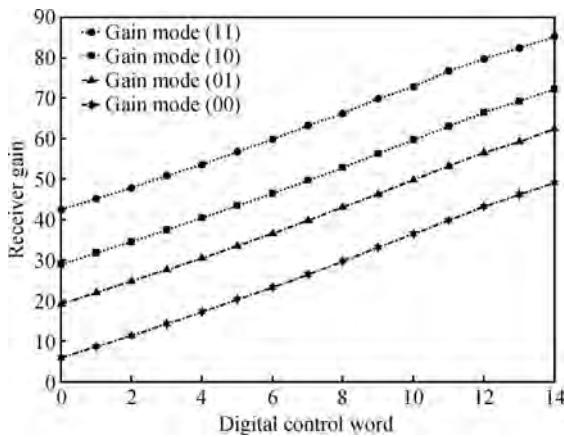


Fig. 15. Measured receiver chain gain with the digital control word.

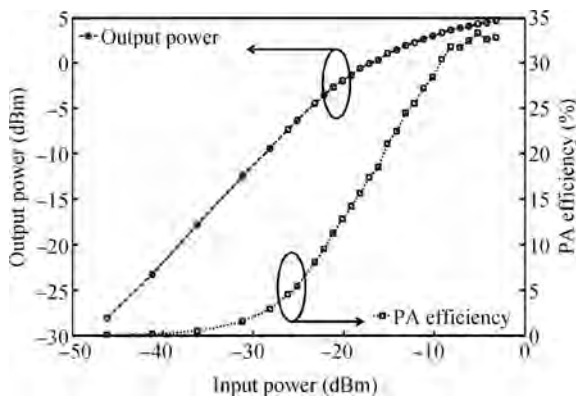
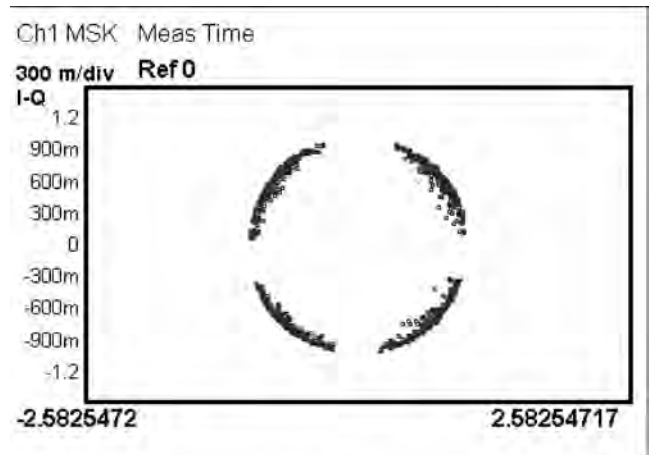


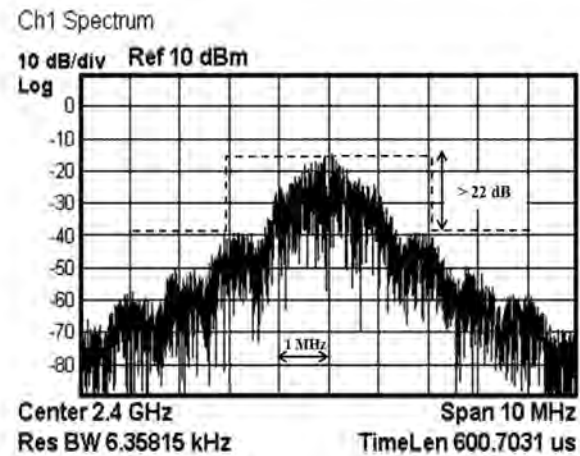
Fig. 16. Measured output power and PA efficiency.

pre-amplifier of the VGCF has a high gain mode with 23 dB and a low gain mode with 9 dB. The decibel linear PGA has 0–42 dB gain range. The measured receiver gain with the digital control word is shown in Fig. 15. The gain of the PGA linearly in decibels is controlled by a 6 bit digital word with 16 steps. Each OPAMP amplifier has a 3 bit digital word with 8 steps. The gain step of the PGA is 3 dB with 0.9 dB gain error.

At the transmitter chain, Figure 16 shows that the measured maximum output power of the transmitter is +3 dBm. The PA efficiency is above 30% at 1.8-V supply. The measured constellation of MSK modulation is shown in Fig. 17(a). The EVM of transmitted signal is less than 23% without using



(a)



(b)

Fig. 17. (a) Measured constellation for EVM and (b) transmitter output spectrum.

any calibration. It is well within the specified requirements of 35%. From constellation, it has a slightly large spread along the circumference. This is mainly due to the power efficient class B PA with nonlinear distortion deteriorated EVM deteriorated EVM, and the phase noise of PLL also has an effect on EVM. The output spectrum of the transmitter is shown in Fig. 17(b). The side lobes are above 22 dB which meet the requirement of 20 dB.

Table 1 concludes the measured performance of the pro-

Table 2. Transceiver performance comparison.

Reference	Ref. [4]	Ref. [6]	Ref. [7]	Ref. [18]	This work
Technology CMOS (μm)	0.18	0.18	0.18	0.09	0.18
Power supply (V)	1.8–3.6	1.8	1.8	0.6	1.4–1.8
Frequency (GHz)	2.4	2.4	2.4	2.4	2.4
NF (dB)	9.5	—	6.2	16	8.5
Sensitivity (dBm)	−96	−94	−101	—	−95
Image rejection (dBc)	> 54	40	22.4	—	28
IIP3 (dBm)	−18	—	−11	—	−8
Max. gain (dB)	85	89	102.5	—	86
Po (dBm)	3	0	0	—	0
P_{dc} (RX) (mW)	30.24	22	25.74	32.5	12.63
P_{dc} (TX) (mW)	32.4	18	23.58	NC	14.22
Die size (mm^2)	5.9*	5.125	7.84*	2.9	4.32

* Die size includes MCU and memory block.

posed transceiver. In the receiver chain, the input P_{1dB} is 0 dBm and the third-order input intercept point (IIP3) is −8 dBm, when two-tone signal as spaced by 1 MHz. The receiver sensitivity is −95 dBm for 1% packet error rate (PER). The total measured current consumption is 7.5 mA in receiving mode. The current consumption of the LNA & Mixer, VGCF, PAG and bias blocks are 1.25 mA, 0.83 mA, 1.42 mA, and 0.2 mA, respectively. In the transmitter chain, it has maximum 3 dBm output power and EVM less than 23% for MSK modulation. The total measured current consumption is 7.9 mA in transmitting mode. The current consumption of the up-conversion mixer, PA and bias blocks are 0.6 mA, 3.4 mA, and 0.1 mA, respectively. The measured typical PLL phase noise at 1 MHz offset is −108 dBc/Hz at 2.45 GHz carrier frequency. The measured current consumption of the frequency synthesizer is less than 3.5 mA. The digital and NVM current consumption is less than 0.3 mA. This ultra-low power 192 bit NVM consumes only 4 $\mu\text{A}/10 \mu\text{A}$ at the reading/writing mode with 1 MHz clock frequency. Table 2 compares performance of the transceiver with the other published works. The measurement results show that this work has lower power consumption in receiving/transmitting mode than the same CMOS technology.

5. Conclusion

A low power 2.4 GHz transceiver for ZigBee applications is implemented in 0.18- μm CMOS technology at 1.8-V supply. This transceiver adopts a low-IF receiver and a direct-conversion transmitter. The system structure and some key circuit blocks are optimized to reduce power consumption and area. The measurement results show that the transceiver only consumes 12.63 mW in receiving mode and 14.22 mW in transmitting mode, respectively. The whole chip area is less than 4.32 mm^2 . The receiver consists of the LNA with noise cancellation, a passive quadrature mixer, an inverter-based VGCF, and a decibel linear PGA to achieve good performance and low power consumption. The transmitter adopts a quadrature mixer and a class-B mode variable gain PA to improve power efficiency and reduce power. The receiver achieves −95 dBm sensitivity, 28 dBc image rejection, and −8 dBm IIP3. The transmitter can deliver maximum +3 dBm output power with EVM < 23% for MSK modulation.

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