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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number			
	Filing Date		2015-08-11	
	First Named Inventor	Li Xu		
	Art Unit	N/A		
	Examiner Name	Not Yet Assigned		
	Attorney Docket Number	0386168386US		

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		
	Filing Date		2015-08-11
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	Attorney Docket Number	0386168386US	

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Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

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☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Rodney Tullett/	Date (YYYY-MM-DD)	2015-08-11
Name/Print	Rodney C. Tullett	Registration Number	34034

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Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		BOOTSTRAP REFRESH CONTROL CIRCUIT, VOLTAGE CONVERTER AND ASSOCIATED METHOD		
First Named Inventor/Applicant Name:		Li XU		
Filer:		Rodney C. Tullett/Jordan Huntley		
Attorney Docket Number:		38616-8386.US00		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility application filing	1011	1	280	280
Utility Search Fee	1111	1	600	600
Utility Examination Fee	1311	1	720	720
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1600

Electronic Acknowledgement Receipt	
EFS ID:	23182029
Application Number:	14823900
International Application Number:	
Confirmation Number:	6869
Title of Invention:	BOOTSTRAP REFRESH CONTROL CIRCUIT, VOLTAGE CONVERTER AND ASSOCIATED METHOD
First Named Inventor/Applicant Name:	Li XU
Customer Number:	67394
Filer:	Rodney C. Tullett/Jordan Huntley
Filer Authorized By:	Rodney C. Tullett
Attorney Docket Number:	38616-8386.US00
Receipt Date:	11-AUG-2015
Filing Date:	
Time Stamp:	19:03:14
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$1600
RAM confirmation Number	5244
Deposit Account	500665
Authorized User	TULLETT, RODNEY C.
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		2015-08-11_38616-8386US_AP P.PDF	1235856 a10144426cdd9f73121ee533136650f5b8f1dcb	yes	51
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Transmittal of New Application		1	1	
	Authorization for Extension of Time all replies		2	3	
	Specification		4	31	
	Claims		32	43	
	Abstract		44	44	
	Drawings-only black and white line drawings		45	50	
	Oath or Declaration filed		51	51	
Warnings:					
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2	Application Data Sheet	2015-08-11_38616-8386US_AD S.PDF	1561234 b64f21bbd9ca5e85abdffa644a8f9eaa07bafe5b	no	7
Warnings:					
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3	Transmittal Letter	2015-08-11_38616-8386US_IDS _LTR.PDF	65414 9446526025c778f7b0a042f9f481e65175c4ebda	no	2
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4	Information Disclosure Statement (IDS) Form (SB08)	2015-08-11_38616-8386US_IDS _SB08.PDF	612145 fe67dcea796822d6b92a1d36b436b5dfd1820631	no	4
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5	Fee Worksheet (SB06)	fee-info.pdf	35213 31cd53f22262f8e855e384f1791eed3a0c0e7c84	no	2
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UTILITY PATENT APPLICATION TRANSMITTAL (ONLY FOR NEW NONPROVISIONAL APPLICATIONS UNDER 37 CFR 1.53(B))		Attorney Docket No. 0386168386US	
		First Named Inventor Li Xu	
		Title	BOOTSTRAP REFRESH CONTROL CIRCUIT, VOLTAGE CONVERTER AND ASSOCIATED METHOD
		Express Mail Label No.	via EFS-Web
APPLICATION ELEMENTS See MPEP chapter 600 concerning utility patent application contents.		Commissioner for Patents ADDRESS TO: P.O. Box 1450 Alexandria, VA 22313-1450	
1. ☐ Fee Transmittal Form (PTO/SB/17 or equivalent) 2. ☐ Applicant asserts small entity status. See 37 CFR 1.27 3. ☐ Applicant certifies micro entity status. See 37 CFR 1.29. Applicant must attach form PTO/SB/15A or B or equivalent. 4. ☒ Specification [Total Pages <u>41</u>] Both the claims and abstract must start on a new page. (See MPEP § 608.01(a) for information on the preferred arrangement) 5. ☒ Drawing(s) (35 U.S.C. 113) [Total Sheets <u>6</u>] 6. Inventor's Oath or Declaration [Total Pages <u>1</u>] (including substitute statements under 37 CFR 1.64 and assignments serving as an oath or declaration under 37 CFR 1.63(e)) a. ☒ Newly executed (original or copy) b. ☐ A copy from a prior application (37 CFR 1.63(d)) 7. ☒ Application Data Sheet *See note below. See 37 CFR 1.76 (PTO/AIA/14 or equivalent) 8. ☐ CD-ROM or CD-R In duplicate, large table, or Computer Program (Appendix) ☐ Landscape Table on CD 9. Nucleotide and/or Amino Acid Sequence Submission (if applicable, items a. – c. are required) a. ☐ Computer Readable Form (CRF) b. Specification Sequence Listing on: i. ☐ CD-ROM or CD-R (2 copies); or ii. ☐ Paper c. ☐ Statements verifying identity of above copies		ACCOMPANYING APPLICATION PARTS 10. ☐ Assignment Papers (cover sheet & document(s)) Name of Assignee 11. ☐ 37 CFR 3.73(c) Statement ☐ Power of Attorney (when there is an assignee) 12. ☐ English Translation Document (if applicable) 13. ☒ Information Disclosure Statement (PTO/SB/08 or PTO-1449) ☐ Copies of citations attached 14. ☐ Preliminary Amendment 15. ☐ Return Receipt Postcard (MPEP § 503) (Should be specifically itemized) 16. ☐ Certified Copy of Priority Document(s) (if foreign priority is claimed) 17. ☐ Nonpublication Request Under 35 U.S.C.122 (b)(2)(B)(i). Applicant must attach form PTO/SB/35 or equivalent. 18. ☒ Other: Authorization for Extension of Time - All Replies	
*Note: (1) Benefit claims under 37 CFR 1.78 and foreign priority claims under 1.55 must be included in an Application Data Sheet (ADS). (2) For applications filed under 35 U.S.C. 111, the application must contain an ADS specifying the applicant if the applicant is an assignee, person to whom the inventor is under an obligation to assign, or person who otherwise shows sufficient proprietary interest in the matter. See 37 CFR 1.46(b).			
18. CORRESPONDENCE ADDRESS			
☒ The address associated with Customer Number: 67394 OR ☐ Correspondence address below			
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City		State	Zip Code
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Signature /Rodney Tullett /		Date August 11, 2015	
Name (Print/Type) Rodney C. Tullett		Registration No. (Attorney/Agent) 34,034	

38616-8386.US00/LEGAL127297356.1

Docket No.: 0386168386US
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

Li XU

Confirmation No.: N/A

Application No.: Not Yet Assigned

Art Unit: N/A

Filed: Concurrently Herewith

Examiner: Not Yet Assigned

For: BOOTSTRAP REFRESH CONTROL
CIRCUIT, VOLTAGE CONVERTER AND
ASSOCIATED METHOD

AUTHORIZATION FOR: EXTENSIONS OF TIME UNDER 37 C.F.R. § 1.136(A)(3)
AND FEES UNDER 37 C.F.R. § 1.17

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Madam:

With respect to the above-identified application, the Commissioner is authorized to treat any concurrent or future reply requiring a petition for an extension of time under 37 C.F.R. § 1.136(a)(3) for its timely submission as incorporating a petition therefor for the appropriate length of time.

Application No.: Not Yet Assigned

Docket No.: 0386168386US

The Commissioner is also authorized to charge any extension of time fees or other fees that may be required under 37 C.F.R. § 1.17 for any paper filed concurrently herewith or in the future, or credit any overpayment, to Deposit Account No. 50-0665.

Dated: August 11, 2015

Respectfully submitted,

By / Rodney Tullett/
Rodney C. Tullett
Registration No.: 34,034
PERKINS COIE LLP
P.O. Box 1247
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(206) 359-8000
(206) 359-9000 (Fax)
Attorney for Applicant

BOOTSTRAP REFRESH CONTROL CIRCUIT, VOLTAGE CONVERTER AND ASSOCIATED METHOD

CROSS-REFERENCE TO RELATED APPLICATION(S)

[0001] This application claims the benefit of CN application No. **201410390708.2** filed on Aug.11, 2014 and incorporated herein by reference.

TECHNICAL FIELD

[0002] This disclosure relates generally to electronic circuits, and more particularly but not exclusively relates to voltage converters and bootstrap refresh control circuit and associated method.

BACKGROUND

[0003] Power converters such as switch-mode voltage regulators are widely used in various electronic devices. In the presently existing switch-mode voltage regulators, a high voltage signal may be needed to drive the switches. So a bootstrap circuit will be applied to provide the high voltage signal.

[0004] Fig. 1 illustrates schematically a voltage converter 50. As shown in Fig. 1, the voltage converter 50 comprises a switching circuit 51 and a control circuit 52.

[0005] The switching circuit 51 may comprise a high side switch 11, a low side switch 12, an inductor (L), a capacitor (C) and a load (R). The high side switch 11 and the low side switch 12 have a source, a drain and a gate respectively. The high side switch 11 and the low side switch 12 may comprise a power switching device, such as a Metal Oxide Semiconductor Field Effect Transistor (MOSFET), a Junction Field Effect Transistor (JFET) etc. The drain of the high side switch 11 is coupled to an input terminal (IN) of the voltage converter 50 for receiving an input voltage (VIN). The source of the high side switch 11 is coupled to the drain of the low side switch 12 so as to constitute a common connection node (SW). The source of the low side switch 12 is connected to a logic ground. The inductor (L) is coupled between the common

connection node (SW) and an output terminal (OUT) of the voltage converter 50. The capacitor (C) and the load (R) are connected in parallel between the output terminal (OUT) of the voltage converter 50 and the logic ground.

[0006] The control circuit 52 is coupled to the output terminal (OUT) of the voltage converter 50 for receiving a feedback signal FB representing an output voltage signal (VOUT) of the voltage converter 50, and configured to generate a first control signal (SH) and a second control signal (SL) to switch the high side switch 11 and the low side switch 12 on and off in a complementary manner. In one embodiment, the control circuit 52 may comprise a Pulse-Width Modulation (PWM) control circuit, wherein the PWM control circuit is configured to regulate the output voltage signal (VOUT) by providing a plurality of square pulse signals with different duty cycle.

[0007] In the embodiment as shown in Fig.1, the control circuit 52 may further comprise a driver configured to drive the high side switch 11 and the low side switch 12. During positive energy storage on the inductor (L), the driver may pull up the voltage of the gate of the high side switch 11. In such application, in order to make the high side switch 11 to be fully turned on (i.e. to make the high side switch 11 to operate in saturation region in which the switch 11 has a quite small on resistance), a voltage applied between the gate of the high side switch 11 and a terminal connected to the common connection node SW of the high side switch 11 must be large enough, at least larger than a conduction threshold voltage of the switch 11. However, when the high side switch 11 is on, the voltage at the common connection node (SW) can reach the input voltage (VIN), and thus a voltage higher than the input voltage (VIN) must be provided to the gate of the high side switch 11 so as to turn it on completely.

[0008] Therefore, in order to generate a voltage higher than the input voltage (VIN), the voltage converter 50 generally further comprises a bootstrap circuit 53. The bootstrap circuit 53 is configured to provide a bootstrap voltage (VBST) referenced to the common connection node (SW). The bootstrap voltage (VBST) can be used to enhance the driving capability of the first control signal (SH) provided to the gate of the high side switch 11, so that the first control signal (SH) can drive the high side switch 11 to turn on and off in good condition.

[0009] In the example of Fig. 1, the bootstrap circuit 53 is illustrated to comprise a diode (DB) and a bootstrap capacitor (CB) connected in series between a bootstrap supply terminal and the common connection node (SW), wherein a cathode of the diode (DB) is connected to the bootstrap supply terminal to receive a bootstrap supply voltage (VB), an anode of the diode (DB) is connected to a first terminal of the bootstrap capacitor (CB) to constitute a common connection node (BST), and a second terminal of the bootstrap capacitor (CB) is connected to the common connection node (SW). The operating principles of the bootstrap circuit 53 can be easily understood by one of ordinary skilled in the art. When the high side switch 11 is turned off and the low side switch 12 is turned on, the voltage of the common connection node (SW) is equal to the ground potential and the bootstrap capacitor (CB) is charged by the bootstrap supply voltage (VB) till the voltage across the bootstrap capacitor (CB) reaches the bootstrap voltage (VBST). When the high side switch 12 is turned on and the low side switch 11 is turned off, the input voltage (VIN) of the voltage converter 50 is transmitted to the common connection node (SW), i.e. the voltage at the second terminal of the bootstrap capacitor (CB) is pulled up to the input voltage (VIN). Thus, the voltage at the common connection node (BST) is raised to a voltage higher than the input voltage (VIN), substantially equal to the input voltage (VIN) plus the bootstrap voltage (VBST). Thus, a voltage higher than the input voltage (VIN) can be obtained in the step-down voltage converter 50. Meanwhile, the diode (DB) is reversely biased and is thus turned off so as to protect the bootstrap supply voltage source (VB) from being damaged by the relatively higher input voltage (VIN).

[0010] In view of the above, it can be understood that the bootstrap capacitor (CB) can be charged to refresh the bootstrap voltage (VBST) by pulling down the second terminal of the bootstrap capacitor (CB) to ground potential when the low side switch 12 is turned on. However, in certain circumstances, the bootstrap capacitor (CB) may not have enough charge stored and may not be charged/recharged in time, resulting in the bootstrap voltage (VBST) to be decreased, which may cause the first control signal (SH) unable to drive the high side switch 11 on and off properly. Consequently, the voltage converter 50 can not be operated properly. Or in another situation, the bootstrap voltage

(VBST) may drop to a default lock-out threshold value resulting in a lock of the voltage converter 50, which may also cause the voltage converter 50 operating improperly.

[0011] For example, when the output voltage signal (VOUT) is approximately close to the input voltage signal (VIN), the high side switch 11 has to operate with a quite high duty cycle, even in a 100% duty cycle. Therefore, the low side switch 12 may have a very short conduction time or hardly have chance to turn on resulting in the bootstrap capacitor (CB) unable to be charged to a desired value.

[0012] In another condition, for example, when the voltage converter 50 operates in light load or no load condition, the control circuit 52 is configured to reduce the conduction time and/or the switching frequency of the high side switch 11 and the low side switch 12 to improve the conversion efficiency of the voltage converter 50, which may lead to the bootstrap capacitor (CB) not being able to be charged/recharged in time since the on time of the low side switch 12 is too short or there is no switching in a relatively long time.

[0013] Therefore, all the conditions mentioned above can result in drops of the bootstrap voltage (VBST), which in turn causes failure in driving the high side switch 11 on and off properly. Thus, the voltage converter 50 operates in an abnormal condition. In such circumstances, only when the output voltage signal (VOUT) drops low enough after several operation cycles, can the bootstrap capacitor (CB) have the opportunity to be charged to refresh the bootstrap voltage (VBST). However, during such processes, a plurality of large spikes may occur in the output voltage signal (VOUT), which may damage the voltage converter 50 and the load (R). Thus, it is undesirable.

[0014] A need therefore exists for solving the problem of refreshing the bootstrap voltage (VBST) timely in voltage converters.

SUMMARY

[0015] In one embodiment, the present invention discloses a bootstrap refresh control circuit for a voltage converter, wherein the voltage converter comprises a high side switch, a low side switch and a bootstrap capacitor for providing a bootstrap voltage signal to supply a high side driver of the high side switch, and wherein the

voltage converter is configured to receive an input voltage at an input terminal and to provide an output voltage at an output terminal based on driving the high side switch and the low side switch to switch on and off, and wherein the bootstrap refresh control circuit comprising: a bootstrap refresh module, wherein the bootstrap refresh module comprises a first comparing module having a first input terminal, a second input terminal and an output terminal, and wherein the first input terminal of the first comparing module is configured to receive the bootstrap voltage signal, the second input terminal of the first comparing module is configured to receive a bootstrap refresh threshold, and the first comparing module is configured to compare the bootstrap voltage signal with the bootstrap refresh threshold to provide a first comparing signal having a first logic state and a second logic state at the output terminal, and wherein the first comparing signal has the first logic state when the bootstrap voltage signal is lower than the bootstrap refresh threshold, and wherein the first comparing signal has the second logic state when the bootstrap voltage signal is larger than the bootstrap refresh threshold; a voltage difference module having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal of the voltage difference module is configured to receive a feedback signal representing the output voltage of the voltage converter, the second input terminal of the voltage difference module is configured to receive a reference voltage signal representing a desired value of the output voltage of the voltage converter, the voltage difference module is configured to compare the feedback signal with the reference voltage signal so as to provide a difference signal at the output terminal; and wherein when the first comparing signal has the first logic state, the bootstrap refresh module is configured to decrease the output voltage of the voltage converter; and wherein when the feedback signal is smaller than the reference voltage signal, the bootstrap refresh control circuit is configured to control the high side switch and the low side switch to switch on and off based on the difference signal so as to charge the bootstrap capacitor for refreshing the bootstrap voltage signal.

[0016] In one embodiment, the present invention discloses a voltage converter, comprising: a switching circuit having a high side switch and a low side switch, wherein the switching circuit is configured to receive an input voltage, and further configured to provide an output voltage based on switching the high side switch and the low side

switch on and off; a bootstrap circuit comprising a bootstrap capacitor, wherein the bootstrap capacitor is charged for providing a bootstrap voltage signal for the high side switch; and a bootstrap refresh control circuit comprising a bootstrap refresh module, wherein the bootstrap refresh module comprises a first comparing module having a first input terminal, a second input terminal and an output terminal, and wherein the first input terminal of the first comparing module is configured to receive the bootstrap voltage signal, the second input terminal of the first comparing module is configured to receive a bootstrap refresh threshold, and the first comparing module is configured to compare the bootstrap voltage signal with the bootstrap refresh threshold to provide a first comparing signal having a first logic state and a second logic state at the output terminal, and wherein the first comparing signal has the first logic state when the bootstrap voltage signal is lower than the bootstrap refresh threshold, and the first comparing signal has the second logic state when the bootstrap voltage signal is larger than the bootstrap refresh threshold; and a voltage difference module having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal of the voltage difference module is configured to receive a feedback signal representing the output voltage of the voltage converter, the second input terminal of the voltage difference module is configured to receive a reference voltage signal representing a desired value of the output voltage of the voltage converter, the voltage difference module is configured to compare the feedback signal with the reference voltage signal so as to provide a difference signal at the output terminal; and wherein when the first comparing signal has the first logic state, the bootstrap refresh module is configured to decrease the output voltage of the voltage converter; and wherein when the feedback signal is smaller than the reference voltage signal, the bootstrap refresh control circuit is configured to control the high side switch and the low side switch to switch on and off based on the difference signal so as to charge the bootstrap capacitor for refreshing the bootstrap voltage signal.

[0017] In one embodiment, the present invention discloses a bootstrap refresh control method for a voltage converter, wherein the voltage converter comprises a high side switch, a low side switch and a bootstrap capacitor for providing a bootstrap voltage signal to supply a high side driver of the high side switch, and wherein the

voltage converter is configured to receive an input voltage and to provide an output voltage based on driving the high side switch and the low side switch to switch on and off, and wherein the bootstrap refresh control method comprising: sensing the bootstrap voltage signal of the voltage converter; comparing the bootstrap voltage with a bootstrap refresh threshold to provide a first comparing signal, wherein the first comparing signal has a first logic state and a second logic state, and wherein the first comparing signal has the first logic state when the bootstrap voltage is lower than the bootstrap refresh threshold, and wherein the first comparing signal has the second logic state when the bootstrap voltage signal is larger than the bootstrap refresh threshold; determining whether the bootstrap voltage signal is smaller than the bootstrap refresh threshold or not; and decreasing the output voltage of the voltage converter by a bootstrap refresh circuit once the bootstrap voltage signal is determined to have dropped to be smaller than the bootstrap refresh threshold; and wherein when the output voltage of the voltage converter is decreased, switching the high side switch and the low side switch on and off so as to refresh the bootstrap voltage signal.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] The following detailed description of various embodiments of the present invention can best be understood when read in conjunction with the following drawings, in which the features are not necessarily drawn to scale but rather are drawn as to best illustrate the pertinent features.

[0019] Fig. 1 illustrates a schematic diagram of a typical voltage converter 50.

[0020] Fig. 2 illustrates a schematic diagram of a voltage converter 100 in accordance with an exemplary embodiment of the present invention.

[0021] Fig. 3 illustrates a schematic diagram of a voltage converter 200 in accordance with an alternative exemplary embodiment of the present invention.

[0022] Fig. 4 illustrates a schematic diagram of a voltage converter 300 in accordance with an alternative exemplary embodiment of the present invention.

[0023] Fig. 5 illustrates an operation waveform diagram of the voltage converter in accordance with an exemplary embodiment of the present invention.

[0024] Fig. 6 illustrates a flow diagram of a method for controlling a voltage converter in accordance with an exemplary embodiment of the present invention.

[0025] The use of the same reference label in different drawings indicates the same or like components or structures with substantially the same functions for the sake of simplicity.

DETAILED DESCRIPTION

[0026] Various embodiments of the present invention will now be described. In the following description, some specific details, such as example circuits and example values for these circuit components, are included to provide a thorough understanding of embodiments. One skilled in the relevant art will recognize, however, that the present invention can be practiced without one or more specific details, or with other methods, components, materials, etc. In other instances, well-known structures, materials, processes or operations are not shown or described in detail to avoid obscuring aspects of the present invention.

[0027] Throughout the specification and claims, the term "coupled," as used herein, is defined as directly or indirectly connected in an electrical or non-electrical manner. The terms "a," "an," and "the" include plural reference, and the term "in" includes "in" and "on". The phrase "in one embodiment," as used herein does not necessarily refer to the same embodiment, although it may. The term "or" is an inclusive "or" operator, and is equivalent to the term "and/or" herein, unless the context clearly dictates otherwise. The term "based on" is not exclusive and allows for being based on additional factors not described, unless the context clearly dictates otherwise. The term "circuit" means at least either a single component or a multiplicity of components, either active and/or passive, that are coupled together to provide a desired function. The term "signal" means at least one current, voltage, charge, temperature, data, or other signal. Where either a field effect transistor ("FET") or a bipolar junction transistor ("BJT") may be employed as an embodiment of a transistor, the scope of the words "gate", "drain",

and “source” includes “base”, “collector”, and “emitter”, respectively, and vice versa. Those skilled in the art should understand that the meanings of the terms identified above do not necessarily limit the terms, but merely provide illustrative examples for the terms.

[0028] Fig. 2 illustrates a schematic diagram of a voltage converter 100 in accordance with an exemplary embodiment of the present invention. In one embodiment, the voltage converter 100 may comprise a switching circuit 110, a bootstrap circuit 120 and a bootstrap refresh control circuit.

[0029] The switching circuit 110 may comprise a high side switch 11, a low side switch 12, an inductor (L), a capacitor (C) and a load (R). The high side switch 11 and the low side switch 12 may have a source, a drain and a gate respectively. The drain of the high side switch 11 is coupled to an input terminal (IN) of the voltage converter 100 for receiving an input voltage (V_{IN}). The source of the high side switch 11 is coupled to the drain of the low side switch 12 so as to constitute a common connection node (SW). The source of the low side switch 12 is connected to a logic ground. The inductor (L) is coupled between the common connection node (SW) and an output terminal (OUT) of the voltage converter 100. The capacitor (C) and the load (R) are connected in parallel between the output terminal (OUT) of the voltage converter 100 and the logic ground. As shown in Fig.2, the switching circuit 110 is illustrated as a step down BUCK topology. It should be known that in other embodiment the switching circuit 110 may comprise other suitable topologies, such as a BOOST, a FORWARD or a FLYBACK converter etc. Likewise, in Fig.2, the high side switch 11 and the low side switch 12 are illustrated as MOSFETs. In other embodiment, the high side switch 11 and the low side switch 12 may comprise other suitable semiconductor devices such as JFETs, Insulated Gate Bipolar Translators (IGBTs) or Double Diffusion Metal Oxide Semiconductor (DMOS) etc.

[0030] The bootstrap circuit 120 may comprise a diode (D_B) and a bootstrap capacitor (C_B) connected in series between a bootstrap supply terminal and the common connection node (SW), wherein a cathode of the diode (D_B) is connected to the bootstrap supply terminal to receive the bootstrap supply voltage (V_B), an anode of

the diode (D_B) is connected to a first terminal of the bootstrap capacitor (C_B) to constitute a common connection node (BST), and a second terminal of the bootstrap capacitor (C_B) is connected to the common connection node (SW). When the high side switch 11 is turned off and the low side switch 12 is turned on, the voltage of the common connection node (SW) is equal to the ground potential and the bootstrap capacitor (C_B) is charged by a bootstrap supply voltage (V_B) till the voltage across the bootstrap capacitor (C_B) reaches the bootstrap voltage (V_{BST}). When the high side switch 12 is turned on and the low side switch 11 is turned off, the input voltage (V_{IN}) of the voltage converter 100 is transmitted to the common connection node (SW), i.e. the voltage at the second terminal of the bootstrap capacitor (C_B) is pulled up to the input voltage (V_{IN}). Thus, the voltage at the common connection node (BST) is raised to the input voltage (V_{IN}) plus the bootstrap voltage (V_{BST}). Thus, a voltage higher than the input voltage (V_{IN}) can be realized in the step-down voltage converter 100. Meanwhile, the diode (D_B) is reversely biased and is thus turned off so as to protect the bootstrap supply voltage source (V_B) from being damaged by the relatively higher input voltage (V_{IN}).

[0031] In one embodiment, the bootstrap refresh control circuit may comprise a voltage difference module 137 having a first input terminal, a second input terminal and an output terminal. The first input terminal of the voltage difference module 137 may be coupled to the output terminal (OUT) of the voltage converter 100, and configured to receive a feedback signal (FB) representing the output voltage signal (V_{OUT}). The second input terminal of the voltage difference module 137 may be configured to receive a reference voltage signal (V_{REF}) representing a desired value of the output voltage signal (V_{OUT}). The voltage difference module 137 is configured to compare the feedback signal (FB) with the reference voltage signal (V_{REF}) so as to provide a difference signal (EA) at the output terminal of the voltage difference module 137. In one embodiment, e.g. for voltage converters using current/ voltage controlled methods, the voltage difference module 137 may comprise an error amplifier which is configured to amplify a difference of the feedback signal (FB) versus the reference voltage signal (V_{REF}) so as to provide an error amplified signal (e.g. labeled with EA in Fig. 2). The error amplified signal (EA) is configured to compare with a ramp signal to generate a

Pulse Width Modulation (PWM) signal for switching the high side switch 11 and the low side switch 12 on and off. In another embodiment, e.g. in examples where the voltage converters using COT control methods or other associated methods, the voltage difference module 137 may comprise a voltage comparator which is configured to compare the feedback signal (FB) and the reference voltage signal (V_{REF}) so as to provide a high-low voltage signal (e.g. also labeled with EA) for switching the high side switch 11 and the low side switch 12 on and off. For example, when the feedback signal (FB) is lower than the reference voltage signal (V_{REF}), the high side switch 11 is turned on while the low side switch 12 is turned off; and when the feedback signal (FB) is larger than the reference voltage signal (V_{REF}), the high side switch 11 is turned off while the low side switch 12 is turned on.

[0032] In one embodiment of Fig.2, the bootstrap refresh control circuit further comprises a control module 131. The control module 131 is coupled to the voltage difference module 137 to receive the difference signal (EA), and configured to estimate the load condition so as to provide a first control signal (S_H) and a second control signal (S_L) for respectively switching the high side switch 11 and the low side switch 12 on and off.

[0033] In one embodiment of Fig.2, the bootstrap refresh control circuit further comprises a driver module 132. The driver module 132 comprises a first driver 31 and a second driver 32. The first driver 31 may comprise an input terminal configured to receive the first control signal (S_H), and an output terminal configured to provide a first drive signal (D_H) to the gate of the high side switch 11 for switching the high side switch 11 on and off. The first driver 31 further comprises a first supply terminal configured to receive the bootstrap voltage signal (V_{BST}), and a second supply terminal connected to the common connection node (SW). The first supply terminal and the second supply terminal are configured to be used to enhance the driving capability of the first drive signal (D_H) so as to better switch the high side switch 11 on and off. The second driver 32 may comprise an input terminal configured to receive the second control signal (S_L), and an output terminal configured to provide a second drive signal (D_L) to the gate of the low side switch 12 for switching the low side switch 12 on and off. In one

embodiment of the present invention, the first driver 31 may comprise one or more inverters, and the bootstrap voltage signal (V_{BST}) is configured to operate as supply sources of the one or more inverters. Besides, the second driver 32 may also comprise one or more inverters.

[0034] In one embodiment, the bootstrap refresh control circuit may further comprise a bootstrap refresh module 133. The bootstrap refresh module 133 is configured to receive a bootstrap voltage signal (V_{BST}), and is further configured to compare the bootstrap voltage signal (V_{BST}) with a bootstrap refresh threshold (V_{TH1}).

[0035] In one embodiment, when the voltage converter 100 operates in light load or no load condition, both the high side switch 11 and the low side switch 12 are turned off so that no current flows through the inductor (L), resulting in drop of the bootstrap voltage signal (V_{BST}). If the bootstrap voltage signal (V_{BST}) drops lower than the bootstrap refresh threshold (V_{TH1}), the bootstrap refresh module 133 starts to operate to reduce the output voltage (V_{OUT}) of the voltage converter 100. Meanwhile, the feedback signal (FB) is decreased with the drops of the output voltage (V_{OUT}). The comparing module 137 may compare the feedback signal (FB) with the reference voltage signal (V_{REF}). When the feedback signal (FB) is smaller than the reference voltage signal (V_{REF}), the control module 131 may control the high side switch 11 and the low side switch 12 to switch normally based on the difference signal (EA) so as to maintain the output voltage signal (V_{OUT}) at a desired value, i.e. the high side switch 11 and the low side switch 12 are recovered from the off states into a complementary conduction states. The conduction time of the low side switch 12 can be increased accompanying the increasing of the switching frequency of the high side switch 11 and the low side switch 12. Thus, the bootstrap capacitor (C_B) can be charged in time to refresh the bootstrap voltage signal (V_{BST}) to the default value. Decreasing the output voltage (V_{OUT}) so as to increase the switching frequency of the high side switch 11 and the low side switch 12 by employing a bootstrap refresh module 133 can avoid using a blanking circuit to blank the high side switch 11. Besides, the control method and the switches sequence will not be affected, i.e. the bootstrap voltage (V_{BST}) can be refreshed by a normal switching of the high side switch 11 and low side switch 12.

[0036] In one exemplary embodiment of Fig.2, the bootstrap refresh module 133 may comprise an input terminal and an output terminal (B_{OUT}). The input terminal of the bootstrap refresh module 133 is configured to receive the bootstrap voltage signal (V_{BST}). The output terminal (B_{OUT}) of the bootstrap refresh module 133 is connected to the common connection node (SW) of the switching circuit 110 to decrease the output voltage (V_{OUT}). In another embodiment, the output terminal (B_{OUT}) of the bootstrap refresh module 133 is connected to the output terminal (OUT) of the voltage converter 100 to decrease the output voltage (V_{OUT}). In another embodiment, the output terminal (B_{OUT}) of the bootstrap refresh module 133 can be connected to both of the common connection node (SW) and the output terminal (OUT) of the voltage converter 100 simultaneously to decrease the output voltage (V_{OUT}) fast.

[0037] In one exemplary embodiment of Fig.2, the bootstrap refresh module 133 may comprise a comparing circuit 33 having a first input terminal, a second input terminal and an output terminal. The first input terminal of the comparing circuit 33 is configured to receive the bootstrap voltage signal (V_{BST}). The second input terminal of the comparing circuit 33 is configured to receive the bootstrap refresh threshold (V_{TH1}). The comparing circuit 33 is configured to compare the bootstrap voltage signal (V_{BST}) with the bootstrap refresh threshold (V_{TH1}) so as to provide a first comparing signal (A_S) having a first logic state and a second logic state at the output terminal. In one embodiment, when the bootstrap voltage signal (V_{BST}) is smaller than the bootstrap refresh threshold (V_{TH1}), the first comparing signal (A_S) may have a first logic state (e.g. logic high state). When the bootstrap voltage signal (V_{BST}) is larger than the bootstrap refresh threshold (V_{TH1}), the first comparing signal (A_S) may have a second logic state (e.g. logic low state). In one embodiment, the comparing circuit 33 may comprise a hysteresis comparator, wherein the bootstrap refresh threshold (V_{TH1}) comprises a first threshold (V_{TH1_L}) and a second threshold (V_{TH1_H}), and wherein the first threshold (V_{TH1_L}) is higher than a ground potential and lower than the second threshold (V_{TH1_H}), and wherein the first comparing signal (A_S) has the first logic state when the bootstrap voltage signal is lower than the first threshold (V_{TH1_L}), and wherein the first comparing signal (A_S) has the second logic state when the bootstrap voltage signal is larger than the second threshold (V_{TH1_H}).

[0038] In one exemplary embodiment of Fig.2, the bootstrap refresh module 133 may further comprise a switch (S1) and a resistor (R1). The switch (S1) has a first terminal, a second terminal and a control terminal. The first terminal of the switch (S1) is connected to one terminal of the resistor (R1). The second terminal of the switch (S1) is operated as the output terminal (B_{OUT}) of the bootstrap refresh module 133. The control terminal of the switch (S1) is coupled to the output terminal of the comparing circuit 33 to receive the first comparing signal (A_S). The other terminal of the resistor (R1) is connected to the logic ground. In one embodiment, when the first comparing signal (A_S) has the first logic state, the switch (S1) is turned on so as to connect the resistor (R1) to the common connection node (SW) and/or the output terminal (OUT) of the voltage converter 100 for decreasing the output voltage (V_{OUT}) of the voltage converter 100, i.e. the output voltage (V_{OUT}) can be decreased due to output capacitor (C) is discharged via the switch (S1) and the resistor (R1). When the first comparing signal (A_S) has the second logic state, the switch (S1) is turned off for separating the resistor (R1) from the common connection node (SW) and/or the output terminal (OUT) of the voltage converter 100. In other embodiment, the resistor (R1) can be replaced with a current sink.

[0039] In one exemplary embodiment of Fig.2, the bootstrap refresh control circuit may further comprise an under voltage lock out module 135 having a first input terminal, a second input terminal and an output terminal. The first input terminal of the under voltage lock out module 135 is configured to receive the bootstrap voltage signal (V_{BST}). The second input terminal of the under voltage lock out module 135 is configured to receive an under voltage lock out threshold (V_{UVLO}). The under voltage lock out module 135 is configured to compare the bootstrap voltage signal (V_{BST}) with the under voltage lock out threshold (V_{UVLO}) so as to provide a bootstrap under voltage signal (LOCK) with a first logic state and a second logic state at the output terminal to the control module 131. When the bootstrap voltage signal (V_{BST}) is smaller than the under voltage lock out threshold (V_{UVLO}), the bootstrap under voltage signal (LOCK) may have a first logic state (e.g. logic high state) so as to protect the high side switch 11 and the low side switch 12 from switching on and off (e.g., turn both of the high side switch 11 and the low side switch 12 off). When the bootstrap voltage signal (V_{BST}) is larger than the under voltage

lock out threshold (V_{UVLO}), the bootstrap under voltage signal (LOCK) may have a second logic state (e.g. logic low state) resulting that the high side switch 11 and the low side switch 12 can be switched on and off based on the difference signal (EA). In one embodiment of the present invention, the under voltage lock out threshold (V_{UVLO}) is lower than the bootstrap refresh threshold (V_{TH1}). The under voltage lock in module 135 is configured to improve the safety performance of the voltage converter 100 by turning the high side switch 11 and the low side switch 12 off once the bootstrap voltage signal (V_{BST}) drops lower than the under voltage lock out threshold (V_{UVLO}) and/or the bootstrap voltage signal (V_{BST}) can not be refreshed in time. In one embodiment, the under voltage lock out module 135 may comprise a hysteresis comparator, wherein the under voltage lock out threshold (V_{UVLO}) comprises a third threshold (V_{UVLO_L}) and a fourth threshold (V_{UVLO_H}), and wherein the third threshold (V_{UVLO_L}) is higher than a ground potential and lower than fourth threshold (V_{UVLO_H}), and wherein the bootstrap under voltage signal (LOCK) has the first logic state when the bootstrap voltage signal is lower than the third threshold (V_{UVLO_L}), and wherein the bootstrap under voltage signal (LOCK) has the second logic state when the bootstrap voltage signal is larger than the fourth threshold (V_{UVLO_H}).

[0040] Fig. 3 illustrates a schematic diagram of a voltage converter 200 in accordance with an exemplary embodiment of the present invention. In one embodiment, the voltage converter 200 also comprises a switching circuit 110, a bootstrap circuit 120 and a bootstrap refresh control circuit. To simple and easy to understand, the components or structures in the voltage converter 200 shown in Fig.3 with substantially same or similar functions as those of the voltage converter 100 shown in Fig. 2 are identified by the same reference labels. Meanwhile, in the exemplary embodiment of the present invention in Fig.3, both the high side witch 11 and the low side switch 12 are illustrated with a body diode. Specifically, a body diode D1 is illustrated between the source and drain of the high side switch 11, and a body diode D2 is illustrated between the source and drain of the high side witch 12. In Fig.3, the high side switch 11 and the low side switch 12 are illustrated as a MOSFET, it should be understood that, the high side switch 11 and the low side switch 12 may comprise other suitable semiconductor devices such as a JFET, IGBT or DMOS etc.

[0041] In the exemplary embodiment of the present invention in Fig.3, the bootstrap refresh control circuit of the voltage converter 200 may comprise a control module 131, a drive module 132, a voltage difference module 137, a bootstrap refresh module 134 and an under voltage lock out module 135. The control module 131, the drive module 132, the voltage difference module 137 and the under voltage lock out 135 of the voltage converter 200 are same as those of the voltage converter 100 in Fig.2. Therefore, same components or structures will no longer be described again for the sake of simplicity.

[0042] In one embodiment of Fig.3, the bootstrap refresh module 134 may comprise a first input terminal and an output terminal. The first input terminal of the bootstrap refresh module 134 is coupled to the bootstrap circuit 120 to receive a bootstrap voltage signal (V_{BST}). The bootstrap refresh module 134 is configured to compare the bootstrap voltage signal (V_{BST}) with a bootstrap refresh threshold (V_{TH1}) for providing an bootstrap refresh signal (RFS). In one embodiment, when the voltage converter 200 operates in light load or no load condition, both the high side switch 11 and the low side switch 12 are turned off so that no current flows through the inductor (L) and the bootstrap voltage signal (V_{BST}) drops. If the bootstrap voltage signal (V_{BST}) drops lower than the bootstrap refresh threshold (V_{TH1}), the bootstrap refresh module 133 start to operate to reduce the output voltage (V_{OUT}) of the voltage converter 200. Meanwhile, the feedback signal (FB) drops with the decreasing of the output voltage (V_{OUT}). The comparing module 137 may compare the feedback signal (FB) with the reference voltage signal (V_{REF}). When the feedback signal (FB) is smaller than the reference voltage signal (V_{REF}), the control module 131 may control the high side switch 11 and the low side switch 12 to switch normally based on the difference signal (EA) so as to maintain the output voltage signal (V_{OUT}) at a desired value, i.e. the high side switch 11 and the low side switch 12 are recovered from the off states into a complementary conduction states. The conduction time of the low side switch 12 can be increased accompanying the increasing of the switching frequency of the high side switch 11 and the low side switch 12. Thus, the bootstrap capacitor (C_B) can be charged in time so as to refresh the bootstrap voltage signal (V_{BST}) to the default value. Decreasing the output voltage (V_{OUT}) for increasing the switching frequency of the high

side switch 11 and the low side switch 12 by employing a bootstrap refresh module 133 can avoid using a blanking circuit to blank the high side switch 11. Besides, the control method and the switches sequence will not be affected, i.e. the bootstrap voltage (V_{BST}) can be refreshed by a normal switching of the high side switch 11 and low side switch 12.

[0043] In one embodiment, the bootstrap refresh module 134 may further comprise a second input terminal coupled to the drain of the low side switch 12 for receiving a sensing signal (V_{CS}) indicating the reversal current flowing through the low side switch 12.

[0044] In one embodiment, still referring to Fig. 3, if the bootstrap voltage (V_{BST}) is lower than the bootstrap refresh threshold (V_{TH1}), the bootstrap refresh signal (RFS) has a first logic state (e.g. logic high state). The low side switch 12 is turned on in response to the logic high state of the bootstrap refresh signal (RFS) to discharge the capacitor (C) via the inductor (L) and the low side switch 12. Meanwhile, an inverse current flowing through the low side switch 12 increases in accordance with the drops of the output voltage (V_{OUT}), while the bootstrap capacitor (C_B) is charged via the low side switch 12. When the sensing signal (V_{CS}) increases in a default current threshold (V_P), the bootstrap refresh signal (RFS) has a second logic state (e.g. logic low state). The low side switch 12 is turned off in response to the logic low state of the bootstrap refresh signal (RFS) to keep the bootstrap capacitor (C_B) from charging. The switching circuit 110 is changed from the BUCK topology to a BOOST topology so as to store the energy discharged by the capacitor (C) in the input terminal (IN) of the voltage converter 200 since the current flow through the inductor (L) freewheels via the body diode D1 of the high side switch 11. In one embodiment, the recover value of the bootstrap voltage (V_{BST}) is relative to the default current threshold (V_P). That is to say, the larger value of the default current threshold (V_P), the recovering ability of the bootstrap voltage (V_{BST}) is stronger, i.e. the bootstrap voltage (V_{BST}) can be refreshed quickly. As a whole, the bootstrap voltage (V_{BST}) recovered in this period is limited since conduction time of the low side switch 12 is short. Thus, generally, the value of the default current threshold (V_P) will be not set too high. The bootstrap refresh module 134 is configured to

decrease the value of the output voltage (V_{OUT}). Once the output voltage (V_{OUT}) drops lower than the desired value, the control model 131 is configured to start to switch the high side switch 11 and the low side switch 12 on and off until the output voltage (V_{OUT}) recovers to the desired value. During this operation, the bootstrap voltage (V_{BST}) can also be refreshed to the default value.

[0045] In the exemplary embodiment of Fig.3, the bootstrap refresh module 134 may comprise a first voltage comparator 34 having a first input terminal configured to receive the bootstrap refresh threshold (V_{TH1}); a second input terminal configured to receive the bootstrap voltage (V_{BST}); and an output terminal. The first voltage comparator 34 is configured to compare the bootstrap voltage (V_{BST}) with bootstrap refresh threshold (V_{TH1}) for providing a first comparing signal (A_S) at the output terminal. In one embodiment, when the bootstrap voltage (V_{BST}) is lower than the bootstrap refresh threshold (V_{TH1}), the first comparing signal (A_S) has a first logic state (e.g. logic high state). When the bootstrap voltage (V_{BST}) is larger than the bootstrap refresh threshold (V_{TH1}), the first comparing signal (A_S) has a second logic state (e.g. logic low state).

[0046] In the exemplary embodiment of the present invention, still referring to Fig.3, the bootstrap refresh module 134 may further comprise a second voltage comparator 35 having a first input terminal configured to receive the default current threshold (V_P); a second input terminal configured to receive the sensing signal (V_{CS}); and an output terminal. The second voltage comparator 35 is configured to compare the sensing signal (V_{CS}) with the default current threshold (V_P) for providing a second comparing signal (A_R) at the output terminal. In one embodiment, when the sensing signal (V_{CS}) is lower than the default current threshold (V_P), the second comparing signal (A_R) has a first logic state (e.g. logic high state); when the sensing signal (V_{CS}) is larger than the default current threshold (V_P), the second comparing signal (A_R) has a second logic state (e.g. logic low state). In one embodiment, setting the default current threshold (V_P) can be based on the desired recovering value of the bootstrap voltage (V_{BST}), for example, the larger default current threshold (V_P), the larger value of the bootstrap voltage (V_{BST}) can be reached.

[0047] In the exemplary embodiment of the present invention, still referring to Fig.3, the bootstrap refresh module 134 may further comprise a logic circuit 36 having a first input terminal configured to receive the first comparing signal (A_S); a second input terminal configured to receive the second comparing signal (A_R); and an output terminal. Logic circuit 36 is configured to conduct a logic operation to the first comparing signal (A_S) and the second comparing signal (A_R) for providing the bootstrap refresh signal (RFS) at the output terminal. In one embodiment, the bootstrap refresh signal (RFS) has a first logic state (e.g. logic high state) when the first comparing signal (A_S) has a first logic state (e.g. logic high state); the bootstrap refresh signal (RFS) has a second logic state (e.g. logic low state) when the second comparing signal (A_R) has a first logic state (e.g. logic high state). In one embodiment, the low side switch 12 is turned on in response to the first logic state of the bootstrap refresh signal (RFS). The capacitor (C) of the switching circuit 110 is discharged via the inductor (L) and the low side switch 12 while the bootstrap capacitor (C_B) is charged. The low side switch 12 is turned off in response to the second logic state of the bootstrap refresh signal (RFS) so that the bootstrap capacitor (C_B) of the switching circuit 110 stop to discharge while the current flowing through the inductor (L) freewheels via the body diode (D1) of the high side switch 11.

[0048] In the exemplary embodiment of Fig.3, the control module 131 is configured to coupled to the voltage comparing circuit 137 for receiving the difference signal (EA), and configured to provide a first control signal (S_H) and a third control signal (S_{L1}) to switch the high side switch 11 and the low side switch 12 on and off based on the change of the difference signal (EA). The first control signal (S_H) and the third control signal (S_{L1}) may have a logic high state and a logic low state respectively. In one embodiment, when the third control signal (S_{L1}) is a first logic state (e.g. logic high state), the low side switch 12 is turned on; when the third control signal (S_{L1}) is a second logic state (e.g. logic low state), the low side switch 12 is turned off. In one embodiment, the control module 131 may further comprise a logic module 30 having a first input terminal configured to receive the third control signal (S_{L1}); a second input terminal configured to receive the bootstrap refresh signal (RFS); and an output terminal. The Logic module 30 is configured to conduct a logic operation to the third

control signal (S_{L1}) and the bootstrap refresh signal (RFS) for providing a second control signal (S_L) at the output terminal. As long as one of the third control signal (S_{L1}) and the bootstrap refresh signal (RFS) has a first logic state (e.g. logic high state), the second control signal (S_L) has a first logic state (e.g. logic high state) so as to turn the low side switch 12 on. In one exemplary embodiment, the logic module 30 is an OR logic gate.

[0049] Fig.4 illustrates a schematic diagram of a voltage converter 300 in accordance with an exemplary embodiment of the present invention. In the exemplary embodiment of Fig.4, the voltage converter 300 also comprises a bootstrap refresh control circuit, wherein the bootstrap refresh control circuit may comprise a control module 131, a driving module 132, a comparing module 137, a bootstrap refresh module 136 and a under voltage lock out module 135. To simple and easy to understand, the components or structures in the voltage converter 300 shown in Fig.4 with substantially same or similar functions as those of the voltage converter 200 shown in Fig.3 and/or the voltage converter 100 shown in Fig.2 are identified by the same reference labels.

[0050] In one embodiment of the present invention in Fig. 4, the bootstrap refresh module 136 may comprise a first voltage comparator 34 having a first input terminal configured to receive the bootstrap refresh threshold (V_{TH1}); a second input terminal configured to receive the bootstrap voltage (V_{BST}); and an output terminal. The first voltage comparator 34 is configured to compare the bootstrap voltage (V_{BST}) with bootstrap refresh threshold (V_{TH1}) for providing a first comparing signal (A_S) at the output terminal. In one embodiment, when the bootstrap voltage (V_{BST}) is lower than the bootstrap refresh threshold (V_{TH1}), the first comparing signal (A_S) has a first logic state (e.g. logic high state); when the bootstrap voltage (V_{BST}) is larger than the bootstrap refresh threshold (V_{TH1}), the first comparing signal (A_S) has a second logic state (e.g. logic low state).

[0051] In the exemplary embodiment of the present invention, still referring to Fig.4, the bootstrap refresh module 134 may further comprise a Constant On Time (COT) circuit 37, wherein the COT circuit 37 is configured to provide a COT control signal (C_R) having a first logic state (e.g. logic high state) and a second logic state (e.g.

logic low state) so as to set a constant on time for the low side switch 12. In one embodiment, the COT control signal (C_R) has the first logic state (e.g. logic low state) during the constant on time and has the second logic state (e.g. logic high state) beyond the constant on time.

[0052] In the exemplary embodiment of the present invention, still referring to Fig.3, the bootstrap refresh module 134 may further comprise logic circuit 36 having a first input terminal configured to receive the first comparing signal (A_S); a second input terminal configured to receive the COT control signal (C_R); and an output terminal. Logic circuit 36 is configured to conduct a logic operation to the first comparing signal (A_S) and the COT control signal (C_R) for providing the bootstrap refresh signal (RFS) at the output terminal. In one embodiment, the bootstrap refresh signal (RFS) has a first logic state (e.g. logic high state) when the first comparing signal (A_S) has a first logic state (e.g. logic high state); and the bootstrap refresh signal (RFS) has a second logic state (e.g. logic low state) when the COT control signal (C_R) has a second logic state (e.g. logic high state).

[0053] In one embodiment, the low side switch 12 is turned on in response to the first logic state of the bootstrap refresh signal (RFS). The capacitor (C) of the switching circuit 110 is discharged via the inductor (L) and the low side switch 12 while the bootstrap capacitor (C_B) is charged. The low side switch 12 is turned off in response to the second logic state of the bootstrap refresh signal (RFS) so that the bootstrap capacitor (C_B) stops to be discharged while the current flowing through the inductor (L) freewheels via the body diode D1 of the high side switch 11. The switching circuit 110 is changed from the BUCK topology to a BOOST topology so as to store the energy discharged by the capacitor (C) in the input terminal (IN) of the voltage converter 300 since the current flow through the inductor (L) freewheels via the body diode D1 of the high side switch 11. In one embodiment, the recover value of the bootstrap voltage (V_{BST}) is relative to the conduction time set by the COT circuit 37. That is to say, the longer on time set by the COT circuit 37, the recovering ability of the bootstrap voltage (V_{BST}) is stronger, i.e. the bootstrap voltage (V_{BST}) can be refreshed quickly. As a whole, the bootstrap voltage (V_{BST}) recovered in this period is limited since conduction time of

the low side switch 12 is short. Thus, generally, the on time will be not set too long by the COT circuit 37. The bootstrap refresh module 136 is configured to decrease the value of the output voltage (V_{OUT}). Once the output voltage (V_{OUT}) drops lower than the desired value, the control model 131 is configured to start to switch the high side switch 11 and the low side switch 12 on and off until the output voltage (V_{OUT}) recovers to the desired value. During this operation, the bootstrap voltage (V_{BST}) can be refreshed to the default value.

[0054] Fig. 5 illustrates an operation waveform diagram of the voltage converter 200 in accordance with an exemplary embodiment of the present invention. In the following, the power converter 200 will be explained in more detail referring to Fig. 3 and Fig. 5. At the time t_0 , both the first control signal (S_H) and the second control signal (S_L) are logic low state so that the high side switch 11 and the low side switch 12 are turned off. Thus, the current (I_L) flowing through the inductor (L) of the switching circuit 110 is zero.

[0055] In the duration of time t_0 to t_1 , both of the first control signal (S_H) and the second control signal (S_L) keep the logic low state so that the high side switch 11 and the low side switch 12 are still turned off. Thus, the current (I_L) flowing through the inductor (L) of the switching circuit 110 is zero. Due to the voltage converter 200 is operated at a light load, the output voltage (V_{OUT}) of the voltage converter 200 almost has no change during this period. At the same time, the bootstrap capacitor (C_B) of the bootstrap circuit 120 can not be charged due to the off state of the low side switch so that the bootstrap voltage (V_{BST}) is dropped.

[0056] At the t_1 time, the first comparing signal (A_S) of the bootstrap refresh circuit is logic high in response to the bootstrap voltage (V_{BST}) drops to the bootstrap refresh threshold (V_{TH1}) resulting the bootstrap refresh signal (RFS) is logic high. Accordingly, the second control signal (S_L) is changed to logic high state so as to turn the low side switch 12 on.

[0057] Form time t_1 to t_2 , the second control signal (S_L) remains a logic high state so as to keep the low side switch 12 on. The capacitor (C) of the switching circuit 110 is discharged via the inductor (L) and the low side switch 12. The current (I_L) flowing

through the inductor (L) increases inversely in accordance with the decreasing of the output voltage (V_{OUT}). Meanwhile, the bootstrap capacitor (C_B) can be charged for refreshing the bootstrap voltage (V_{BST}) by connecting to logic ground through the low side switch 12.

[0058] At the t_2 time, The current (I_L) flowing through the inductor (L) increases to a first current threshold (I_{P1}), i.e. the current sensing signal (V_{CS}) of the second comparator 35 is equal to the default current threshold (V_P) in the bootstrap refresh circuit 134, that is to day, the first current threshold signal (I_{P1}) is indicative of the default current threshold (V_P). At this time, the second comparing signal (A_R) changes to a logic high state so as to turn the low side switch 12 off. Accordingly, the bootstrap voltage signal (V_{BST}) can be refreshed to a first value (V_{BST1}). In other embodiments, different value of the default current threshold (V_P) can be chosen for a purpose of getting different refreshed value of the bootstrap voltage signal (V_{BST}). Without doubt that in the exemplary embodiment of the voltage converter 300 in Fig.4, different refreshed value of the bootstrap voltage signal (V_{BST}) can be abstained by setting different on time of the COT circuit 37.

[0059] Continue to Fig.5, Form time t_2 to t_3 , the second control signal (S_L) backs to the logic low state so that the output voltage signal (V_{OUT}) of voltage converter 200 continues to drop. Accordingly, the current (I_L) flow through the inductor (L) freewheels via the body diode D1 of the high side switch 11.

[0060] At the time t_3 , the current (I_L) flowing through the inductor (L) decreases to zero.

[0061] The durations of time t_1' to t_3' and the time t_1'' to t_3'' are repeated of the above process of time t_1 to t_3 . The output voltage signal (V_{OUT}) of voltage converter 200 continues to drop. In one embodiment, for example, in time T_3'' , the output voltage signal (V_{OUT}) drops to a reference value, the voltage converter 200 jumps out of a light load condition so that the high side switch 11 and the low side switch 12 start to switch on and off normally. At this moment, the first control signal (S_H) changes to a logic high state so as to turn the high side switch 11 on. It should be understood that, in the exemplary embodiment of Fig.5, the low side switch 12 has been switched on and off

three times (i.e. t_1 - t_3 , t_1' - t_3' , and t_1'' - t_3'') for the purpose of decreasing the output voltage (V_{OUT}). In other embodiment, any switching times can be chosen for a different reference value.

[0062] From time t_3'' to t_4 , the high side switch 11 keeps on state in response to the logic high state of the first control signal (S_H). The output voltage (V_{OUT}) increases in accordance with the inductor (L) store energies forward. At the same time, the bootstrap voltage (V_{BST}) continues to drop down.

[0063] At the time t_4 , the high side switch 11 is turned off in response to the logic low state of the first control signal (S_H). Inversely, the low side switch 12 is turned on in response to the logic high state of the second control signal (S_L). Meanwhile, the inductive current (I_L) gets to a peak value.

[0064] From time t_4 to t_5 , the high side switch 11 keeps off state and the low side switch 12 keeps on state. The current (I_L) flowing through the inductor (L) freewheels via the low side switch 12. The bootstrap capacitor (C_B) can be charged for refreshing the bootstrap voltage (V_{BST}) by connecting to logic ground through the low side switch 12.

[0065] At the time t_5 , the high side switch 11 is turned off in response to the logic low state of the second control signal (S_L). The current (I_L) flowing through the inductor (L) is dropped to zero while the bootstrap voltage (V_{BST}) is refreshed.

[0066] Fig. 6 illustrates a flow diagram of a method for controlling a voltage converter in accordance with an exemplary embodiment of the present invention.

[0067] The voltage converter (such as the voltage converters 100, 200, and 300) may comprise a high side switch (e.g. 11 in Figs. 2, 3 and 4), a low side switch (e.g. 12 in Figs. 2, 3 and 4) and a bootstrap capacitor (e.g. C_B in Figs. 2 and 3) for providing a bootstrap voltage (e.g. V_{BST}) to supply a high side driver of the high side switch. The power converter is configured to receive an input voltage (V_{IN}) and to provide an output voltage (V_{OUT}) based on driving the high side switch and the low side switch to switch on and off according to the output voltage and the output current. The method for controlling the power converter may comprise step 601 to step 607.

[0068] In step 601, sensing the bootstrap voltage of a voltage converter (such as the voltage converters 100, 200, and 300) across the bootstrap capacitor (C_B) so as to generate a bootstrap voltage signal (V_{BST}).

[0069] In step 602, comparing the bootstrap voltage signal (V_{BST}) with a bootstrap refresh threshold (V_{TH1}) to provide a first comparing signal (A_S) based on the comparison results of the bootstrap voltage signal (V_{BST}) and the bootstrap refresh threshold (V_{TH1}), wherein the first comparing signal (A_S) has a first logic state and a second logic state, and wherein the first comparing signal (A_S) has the first logic state when the bootstrap voltage signal (V_{BST}) is lower than the bootstrap refresh threshold (V_{TH1}), and wherein the first comparing signal (A_S) has the second logic state when the bootstrap voltage signal (V_{BST}) is larger than the bootstrap refresh threshold (V_{TH1}).

[0070] In step 603, Determining whether the bootstrap voltage signal (V_{BST}) is smaller than the bootstrap refresh threshold (V_{TH1}) or not. If the bootstrap voltage signal (V_{BST}) drops to the bootstrap refresh threshold (V_{TH1}), thus the control method turns to step 604. Otherwise, the control method returns to the step 602 to continue to compare the bootstrap voltage signal (V_{BST}) with a bootstrap refresh threshold (V_{TH1}).

[0071] Continue with Fig. 6, in step 604, decreasing the output voltage signal (V_{OUT}) of the voltage converter once the bootstrap voltage signal (V_{BST}) drops to the bootstrap refresh threshold (V_{TH1}).

[0072] In step 605, the high side switch 11 and the low side switch 12 are switched on and off in response to the decreasing of output voltage signal (V_{OUT}) so as to maintain the output voltage signal (V_{OUT}) at a desirable value. The bootstrap voltage signal (V_{BST}) can be refreshed once the switching frequency of the low side switch 12 gets faster.

[0073] In accordance with an exemplary embodiment of the present invention, the method for controlling the power converter may further comprise step 606 and step 607.

[0074] In step 606, comparing the bootstrap voltage signal (V_{BST}) with an under voltage lock out threshold (V_{UVLO}) so as to provide a bootstrap under voltage signal (LOCK) based on the comparison of the bootstrap voltage signal (V_{BST}) and the under

voltage lock out threshold (V_{UVLO}), wherein the under voltage lock out threshold (V_{UVLO}) is smaller than the bootstrap refresh threshold (V_{TH1}). When the bootstrap voltage signal (V_{BST}) is smaller than the under voltage lock out threshold (V_{UVLO}), the bootstrap under voltage signal (LOCK) may have a first logic state (e.g. logic high state). When the bootstrap voltage signal (V_{BST}) is larger than the under voltage lock out threshold (V_{UVLO}), the bootstrap under-voltage signal (LOCK) may have a second logic state (e.g. logic low state).

[0075] Continue with Fig. 6, in step 607, switching the high side switch 11 and the low side switch 12 on and off based on the logic state of the bootstrap under-voltage signal (LOCK). When the bootstrap under-voltage signal (LOCK) has a first logic state (e.g. logic high state), both of the high side switch 11 and the low side switch 12 stop switching on and off (e.g., turn the high side switch 11 and the low side switch 12 off). When the bootstrap voltage signal (V_{BST}) is larger than the under-voltage lock- out threshold (V_{UVLO}), the bootstrap under-voltage signal (LOCK) has a second logic state (e.g. logic low state), and the high side switch 11 and the low side switch 12 can be switched on and off based on the difference signal (EA) .

[0076] In accordance with an exemplary embodiment of the present invention, in step 604, the high side switch and the low side switch have a common connection node, and decreasing the output voltage signal (V_{OUT}) of the voltage converter may comprise using a resistor or a current sink connected between the output terminal (OUT) of the voltage converter and the logic ground GND to discharge the capacitor (C). In other embodiment, the voltage converter may comprise a common connection node (SW) of the high side switch 11 and the low side switch 12. Decreasing the output voltage signal (V_{OUT}) of the voltage converter may comprise using a resistor or a current sink connected between common connection node (SW) and the logic ground GND to discharge the output capacitor (C).

[0077] In accordance with an exemplary embodiment of the present invention, in step 604, decreasing the output voltage signal (V_{OUT}) of the voltage converter may comprise: sensing the current flowing through the low side switch 12 so as to provide a sensing signal (V_{CS}); comparing the sensing signal (V_{CS}) with a default current threshold

(V_P) so as to provide a second comparing signal (A_R), wherein the second comparing signal (A_R) has a first logic state and a second logic state, wherein the second comparing signal (A_R) has the first logic state when the sensing signal (V_{CS}) is larger than the default current threshold, and wherein the second comparing signal (A_R) has the second logic state when the sensing signal (V_{CS}) is lower than the default current threshold; providing a bootstrap refresh signal (RFS) based on the first comparing signal (A_S) and the second comparing signal (A_R), wherein the a bootstrap refresh signal (RFS) has a first logic state and a second logic state, wherein the bootstrap refresh signal (RFS) has the first logic state when the first comparing signal (A_S) has a first logic state, and wherein the bootstrap refresh signal (RFS) has the second logic state when the second comparing signal (A_R) has the first logic state; switching the low side switch 12 on and off based on the bootstrap refresh signal (RFS) so as to decrease the output voltage (V_{OUT}). In one embodiment, the low side switch 12 is turned on in response to the first logic state of the bootstrap refresh signal (RFS) when the first comparing signal (A_S) has a first logic state (e.g. logic high state); the low side switch 12 is turned off in response to the second logic state of the bootstrap refresh signal (RFS) when the second comparing signal (A_R) has a first logic state (e.g. logic high state).

[0078] In accordance with an exemplary embodiment of the present invention, in step 604, decreasing the output voltage signal (V_{OUT}) of the voltage converter may comprise: providing a Constant On Time control signal (C_R) configured to set a constant on time for the low side switch 12, wherein the Constant On Time control signal (C_R) has a first logic state and a second logic state, wherein the Constant On Time control signal (C_R) has the first logic state during the constant on time, and wherein the Constant On Time control signal (C_R) has the second logic state beyond the constant on time; providing a bootstrap refresh signal (RFS) based on the first comparing signal (A_S) and the Constant On Time control signal (C_R), wherein the a bootstrap refresh signal (RFS) has a first logic state and a second logic state, wherein the bootstrap refresh signal (RFS) has the first logic state when the first comparing signal (A_S) has a first logic state, and wherein the bootstrap refresh signal (A_S) has the second logic state when the Constant On Time control signal (C_R) has a second logic state; switching the low side switch 12 on and off based on the bootstrap refresh signal (RFS) so as to decrease the

output voltage (V_{OUT}). In one embodiment, the low side switch 12 is turned on in response to the first logic state of the bootstrap refresh signal (RFS) when the first comparing signal (A_S) has a first logic state (e.g. logic high state); the low side switch 12 is turned off in response to the second logic state of the bootstrap refresh signal (RFS) when COT control signal (C_R) has a second logic state (e.g. logic high state).

[0079] Methods and steps of controlling the power converter described above in the various embodiments of the present invention are illustrative and not intended to be limiting. Well known controlling steps, operating processes, and parameters etc. are not described in detail to avoid obscuring aspects of the invention. Those skilled in the art should understand that the steps described in the embodiments with reference to Fig. 6 may be implemented in different orders and are not limited to the embodiments described.

[0080] Although a bootstrap refresh control circuit, a power converter comprising the bootstrap refresh control circuit and associated control methods are illustrated and explained based on a buck type power converter according to various embodiments of the present invention, this is not intended to be limiting. Persons of ordinary skill in the art will understand that the circuits, methods and principles taught herein may apply to any other suitable types of power converters, such as boost type power converters, buck-boost type power converters or flyback type power converters etc.

[0081] From the foregoing, it will be appreciated that specific embodiments of the present invention have been described herein for purposes of illustration, but that various modifications may be made without deviating from the spirit and scope of various embodiments of the present invention. Many of the elements of one embodiment may be combined with other embodiments in addition to or in lieu of the elements of the other embodiments. Accordingly, the present invention is not limited except as by the appended claims.

CLAIMS

What is claimed is:

1. A bootstrap refresh control circuit for a voltage converter, wherein the voltage converter comprises a high side switch, a low side switch and a bootstrap capacitor for providing a bootstrap voltage signal to supply a high side driver of the high side switch, and wherein the voltage converter is configured to receive an input voltage at an input terminal and to provide an output voltage at an output terminal based on driving the high side switch and the low side switch to switch on and off, and wherein the bootstrap refresh control circuit comprising:

- a bootstrap refresh module, wherein the bootstrap refresh module comprises a first comparing module having a first input terminal, a second input terminal and an output terminal, and wherein the first input terminal of the first comparing module is configured to receive the bootstrap voltage signal, the second input terminal of the first comparing module is configured to receive a bootstrap refresh threshold, and the first comparing module is configured to compare the bootstrap voltage signal with the bootstrap refresh threshold to provide a first comparing signal having a first logic state and a second logic state at the output terminal, and wherein the first comparing signal has the first logic state when the bootstrap voltage signal is lower than the bootstrap refresh threshold, and wherein the first comparing signal has the second logic state when the bootstrap voltage signal is larger than the bootstrap refresh threshold; and
- a voltage difference module having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal of the voltage difference module is configured to receive a feedback signal representing the output voltage of the voltage converter, the second input terminal of the voltage difference module is configured to receive a reference voltage signal representing a desired value of the output voltage of the voltage

converter, the voltage difference module is configured to compare the feedback signal with the reference voltage signal so as to provide a difference signal at the output terminal; and wherein
when the first comparing signal has the first logic state, the bootstrap refresh module is configured to decrease the output voltage of the voltage converter; and wherein when the feedback signal is smaller than the reference voltage signal, the bootstrap refresh control circuit is configured to control the high side switch and the low side switch to switch on and off based on the difference signal so as to charge the bootstrap capacitor for refreshing the bootstrap voltage signal.

2. The bootstrap refresh control circuit of claim 1, wherein
the bootstrap refresh threshold comprises a first threshold and a second threshold, wherein the first threshold is higher than a ground potential and lower than the second threshold; and wherein
the first comparing signal has the first logic state when the bootstrap voltage signal is lower than the first threshold, and wherein the first comparing signal has the second logic state when the bootstrap voltage signal is larger than the second threshold.
3. The bootstrap refresh control circuit of claim 1, wherein the high side switch and the low side switch have a common connection node, and wherein the bootstrap refresh module further comprises a discharging switch and a resistor, and wherein
the discharging switch has a first terminal, a second terminal and a control terminal, wherein the first terminal of the discharging switch is connected to the common connection node and/or the output terminal of the voltage converter so as to provide a bootstrap refresh signal, the second terminal of the discharging switch is coupled to one terminal of the resistor, the control terminal of the discharging switch is configured to receive the first

comparing signal, and the another terminal of the resistor is connected to the logic ground; and wherein

when the first comparing signal has the first logic state, the discharging switch is turned on so as to connect the resistor to the common connection node and/or the output terminal of the voltage converter for decreasing the output voltage of the voltage converter; and when the first comparing signal has the second logic state, the discharging switch is turned off for disconnecting the resistor from the common connection node and/or the output terminal of the voltage converter.

4. The bootstrap refresh control circuit of claim 3, wherein the bootstrap refresh module further comprises:

a control module comprising an input terminal, a first output terminal and a second output terminal, wherein the input terminal of the control module is coupled to the output terminal of the voltage difference module for receiving the difference signal, the control module is configured to provide a first control signal and a second control signal based on the difference signal for switching the high side switch and the low side switch on and off at the first output terminal and the second output terminal respectively; and wherein when the feedback signal is smaller than the reference voltage signal, the control module is configured to control the high side switch and the low side switch to switch on and off based on the difference signal so as to charge the bootstrap capacitor for refreshing the bootstrap voltage signal.

5. The bootstrap refresh control circuit of claim 1, wherein the bootstrap refresh module further comprises:

a second comparing module having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal of the second comparing module is configured to receive a default current threshold, the

second input terminal of the second comparing module is configured to receive a sensing signal representing the current flowing through the low side switch, and the second comparing module is configured to compare the sensing signal with the default current threshold for providing a second comparing signal having a first logic state and a second logic state at the output terminal, and wherein the second comparing signal has the first logic state when the sensing signal is larger than the default current threshold, and wherein the second comparing signal has the second logic state when the sensing signal is lower than the default current threshold; and

- a first logic module having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal of the first logic module is configured to receive the first comparing signal, the second input terminal of the first logic module is configured to receive the second comparing signal, and the first logic module is configured to conduct a logic operation to the first comparing signal and the second comparing signal for providing a bootstrap refresh signal having a first logic state and a second logic state at the output terminal; and wherein the bootstrap refresh signal has the first logic state when the first comparing signal has a first logic state so as to turn the low side switch on, and the bootstrap refresh signal has the second logic state when the second comparing signal has a first logic state so as to turn the low side switch off.

6. The bootstrap refresh control circuit of claim 1, wherein the bootstrap refresh module further comprises:

- a Constant On Time circuit configured to provide a COT control signal having a first logic state and a second logic state so as to set a constant on time for the low side switch, wherein the COT control signal has the first logic state during the constant on time, and wherein the COT control signal has the second logic state beyond the constant on time; and

a first logic module having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal of the first logic module is configured to receive the first comparing signal, the second input terminal of the first logic module is configured to receive the COT control signal, and the first logic module is configured to conduct a logic operation to the first comparing signal and the COT control signal for providing a bootstrap refresh signal having a first logic state and a second logic state at the output terminal; and wherein the bootstrap refresh signal has the first logic state when the first comparing signal has a first logic state so as to turn the low side switch on, and the bootstrap refresh signal has a second logic state when the COT control signal has a second logic state so as to turn the low side switch off.

7. The bootstrap refresh control circuit of claim 1 further comprising:
an under voltage lock out module having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal of the under voltage lock out module is configured to receive the bootstrap voltage signal, the second input terminal of the under voltage lock out module is configured to receive an under voltage lock out threshold, and the under voltage lock out module is configured to compare the bootstrap voltage signal with the under voltage lock out threshold so as to provide a bootstrap under voltage signal having a first logic state and a second logic state at the output terminal, and wherein the bootstrap refresh signal has the first logic state when the bootstrap voltage signal is lower than the under voltage lock out threshold so as to stop switching the high side switch and the low side switch, and wherein the bootstrap refresh signal has the second logic state when the bootstrap voltage signal is larger than the under voltage lock out threshold so as to permit switching the high side switch and the low side switch.

8. The bootstrap refresh control circuit of claim 5 further comprising:
- a control module having a first input terminal, a second input terminal, a first output terminal and a second output terminal, wherein the first input terminal of the control module is coupled to the output terminal of the voltage difference module for receiving the difference signal, the second input terminal of the control module is configured to receive the bootstrap refresh signal, the control module is configured to conduct a logic operation of difference signal and the bootstrap refresh signal for providing a first control signal and a second control signal to switch the high side switch and the low side switch on and off at the first output terminal and the second output terminal respectively, and wherein the first control signal and the second control signal both have a first logic state and a second logic state; and wherein
 - when the feedback signal is smaller than the reference voltage signal, the high side switch is turned on in response to the first logic state of the first control signal, and the low side switch is turned off in response to the second logic state of the second control signal; and wherein
 - when the feedback signal is larger than the reference voltage signal, the high side switch is turned off in response to the second logic state of the first control signal, and the low side switch is turned on in response to the first logic state of the second control signal; and wherein
 - when the bootstrap refresh signal has the first logic state, the second control signal has the first logic state so as to turn the low side switch on for decreasing the output voltage of the voltage converter; when the bootstrap refresh signal has the second logic state, the second control signal has the second logic state so as to turn the low side switch off.

9. The bootstrap refresh control circuit of claim 6 further comprising:
- a control module having a first input terminal, a second input terminal, a first output terminal and a second output terminal, wherein the first input terminal of the control module is coupled to the output terminal of the voltage difference module for receiving the difference signal, the second input terminal of the control module is configured to receive the bootstrap refresh signal, the control module is configured to conduct a logic operation of difference signal and the bootstrap refresh signal for providing a first control signal and a second control signal to switch the high side switch and the low side switch on and off at the first output terminal and the second output terminal respectively, and wherein the first control signal and the second control signal both have a first logic state and a second logic state; and wherein
- when the feedback signal is smaller than the reference voltage signal, the high side switch is turned on in response to the first logic state of the first control signal, and the low side switch is turned off in response to the second logic state of the second control signal; and wherein
- when the feedback signal is larger than the reference voltage signal, the high side switch is turned off in response to the second logic state of the first control signal, and the low side switch is turned on in response to the first logic state of the second control signal; and wherein
- when the bootstrap refresh signal has the first logic state, the second control signal has the first logic state so as to turn the low side switch on for decreasing the output voltage of the voltage converter; when the bootstrap refresh signal has the second logic state, the second control signal has the second logic state so as to turn the low side switch off.

10. The bootstrap refresh control circuit of claim 8, wherein the bootstrap refresh control circuit further comprising:

- a driver module comprising a first driver and a second driver, wherein the first driver has an input terminal configured to receive the first control signal, a first supply terminal configured to receive the bootstrap voltage signal, a second supply terminal connected to the common connection node, and an output terminal configured to provide a first drive signal to drive the high side switch on and off; and wherein the second driver has an input terminal configured to receive the second control signal, and an output terminal configured to provide a second drive signal to drive the low side switch on and off.

11. A voltage converter, comprising:

- a switching circuit having a high side switch and a low side switch, wherein the switching circuit is configured to receive an input voltage, and further configured to provide an output voltage based on switching the high side switch and the low side switch on and off;

- a bootstrap circuit comprising a bootstrap capacitor, wherein the bootstrap capacitor is charged for providing a bootstrap voltage signal for the high side switch; and

- a bootstrap refresh control circuit comprising:

- a bootstrap refresh module, wherein the bootstrap refresh module comprises a first comparing module having a first input terminal, a second input terminal and an output terminal, and wherein the first input terminal of the first comparing module is configured to receive the bootstrap voltage signal, the second input terminal of the first comparing module is configured to receive a bootstrap refresh threshold, and the first comparing module is configured to compare the bootstrap voltage signal with the bootstrap refresh threshold to provide a first comparing signal having a first logic state and a second logic state at the output terminal, and wherein the first

comparing signal has the first logic state when the bootstrap voltage signal is lower than the bootstrap refresh threshold, and the first comparing signal has the second logic state when the bootstrap voltage signal is larger than the bootstrap refresh threshold; and

a voltage difference module having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal of the voltage difference module is configured to receive a feedback signal representing the output voltage of the voltage converter, the second input terminal of the voltage difference module is configured to receive a reference voltage signal representing a desired value of the output voltage of the voltage converter, the voltage difference module is configured to compare the feedback signal with the reference voltage signal so as to provide a difference signal at the output terminal; and wherein

when the first comparing signal has the first logic state, the bootstrap refresh module is configured to decrease the output voltage of the voltage converter; and wherein when the feedback signal is smaller than the reference voltage signal, the bootstrap refresh control circuit is configured to control the high side switch and the low side switch to switch on and off based on the difference signal so as to charge the bootstrap capacitor for refreshing the bootstrap voltage signal.

12. A bootstrap refresh control method for a voltage converter, wherein the voltage converter comprises a high side switch, a low side switch and a bootstrap capacitor for providing a bootstrap voltage signal to supply a high side driver of the high side switch, and wherein the voltage converter is configured to receive an input voltage and to provide an output voltage based on driving the high side switch and the low side

switch to switch on and off, and wherein the bootstrap refresh control method comprising:

- sensing the bootstrap voltage signal of the voltage converter;
- comparing the bootstrap voltage with a bootstrap refresh threshold to provide a first comparing signal, wherein the first comparing signal has a first logic state and a second logic state, and wherein the first comparing signal has the first logic state when the bootstrap voltage is lower than the bootstrap refresh threshold, and wherein the first comparing signal has the second logic state when the bootstrap voltage signal is larger than the bootstrap refresh threshold;
- determining whether the bootstrap voltage signal is smaller than the bootstrap refresh threshold or not; and
- decreasing the output voltage of the voltage converter by a bootstrap refresh circuit once the bootstrap voltage signal is determined to have dropped to be smaller than the bootstrap refresh threshold; and wherein when the output voltage of the voltage converter is decreased, switching the high side switch and the low side switch on and off so as to refresh the bootstrap voltage signal.

13. The bootstrap refresh control method of claim 12, wherein the high side switch and the low side switch have a common connection node, and wherein decreasing the output voltage of the voltage converter by a bootstrap refresh circuit comprises:

- when the bootstrap voltage signal is smaller than the bootstrap refresh threshold, a resistor and/or a current sink is connected between the common connection node and a logic ground and/or between an output terminal of the voltage converter and the logic ground.

14. The bootstrap refresh control method of claim 12, wherein decreasing the output voltage of the voltage converter by a bootstrap refresh circuit comprises:

sensing a current flowing through the low side switch so as to provide a sensing signal;

comparing the sensing signal with a default current threshold so as to provide a second comparing signal, wherein the second comparing signal has a first logic state and a second logic state, and wherein the second comparing signal has the first logic state when the sensing signal is larger than the default current threshold, and wherein the second comparing signal has the second logic state when the sensing signal is lower than the default current threshold;

providing a bootstrap refresh signal based on the first comparing signal and the second comparing signal, wherein the bootstrap refresh signal has a first logic state and a second logic state, and wherein the bootstrap refresh signal has the first logic state when the first comparing signal has the first logic state, and wherein the bootstrap refresh signal has the second logic state when the second comparing signal has the first logic state; and

switching the low side switch on and off based on the bootstrap refresh signal so as to decrease the output voltage; and wherein

the low side switch is switched on in response to the first logic state of the bootstrap refresh signal; and wherein

the low side switch is switched off in response to the second logic state of the bootstrap refresh signal.

15. The bootstrap refresh control method of claim 12, wherein decreasing the output voltage of the voltage converter by a bootstrap refresh circuit comprising:

providing a Constant On Time control signal to set a constant on time for the low side switch, wherein the Constant On Time control signal has a first logic state and a second logic state, and wherein the Constant On Time control signal has the first logic state during the constant on time, and wherein the

Constant On Time control signal has the second logic state beyond the constant on time;
providing a bootstrap refresh signal based on the first comparing signal and the constant on time control signal, wherein the bootstrap refresh signal has a first logic state and a second logic state, and wherein the bootstrap refresh signal has the first logic state when the first comparing signal has the first logic state, and wherein the bootstrap refresh signal has the second logic state when the Constant On Time control signal has the second logic state; and
switching the low side switch on and off based on the bootstrap refresh signal so as to decrease the output voltage; and wherein
the low side switch is switched on in response to the first logic state of the bootstrap refresh signal; and wherein
the low side switch is switched off in response to the second logic state of the bootstrap refresh signal.

16. The bootstrap refresh control circuit of claim 12, wherein
the bootstrap refresh threshold comprises a first threshold and a second threshold, and wherein the first threshold is higher than a ground potential and lower than the second threshold; and wherein
the first comparing signal has the first logic state when the bootstrap voltage signal is lower than the first threshold, and wherein the first comparing signal has the second logic state when the bootstrap voltage signal is higher than the second threshold.

ABSTRACT OF THE DISCLOSURE

A voltage converter having a bootstrap refresh control circuit and a method for controlling the voltage converter. The bootstrap refresh control circuit monitors a bootstrap voltage across a bootstrap capacitor and provides a high side driving signal to a high side switch of the voltage converter. The bootstrap refresh control circuit also controls the charging of the bootstrap capacitor through decreasing the output voltage of the voltage converter once the bootstrap voltage is dropped to be smaller than a bootstrap refresh threshold. When the output voltage of the voltage converter is decreased enough, the bootstrap refresh control circuit switches the high side switch and the low side switch on and off to refresh the bootstrap voltage.

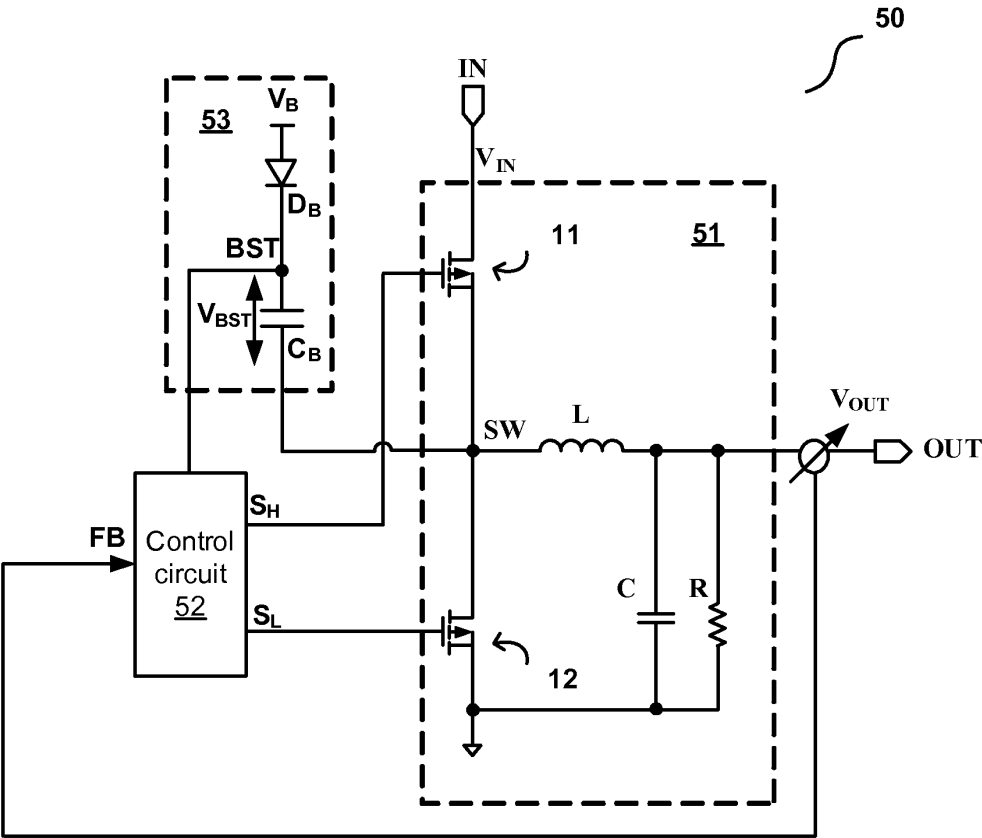


FIG. 1 (Prior Art)

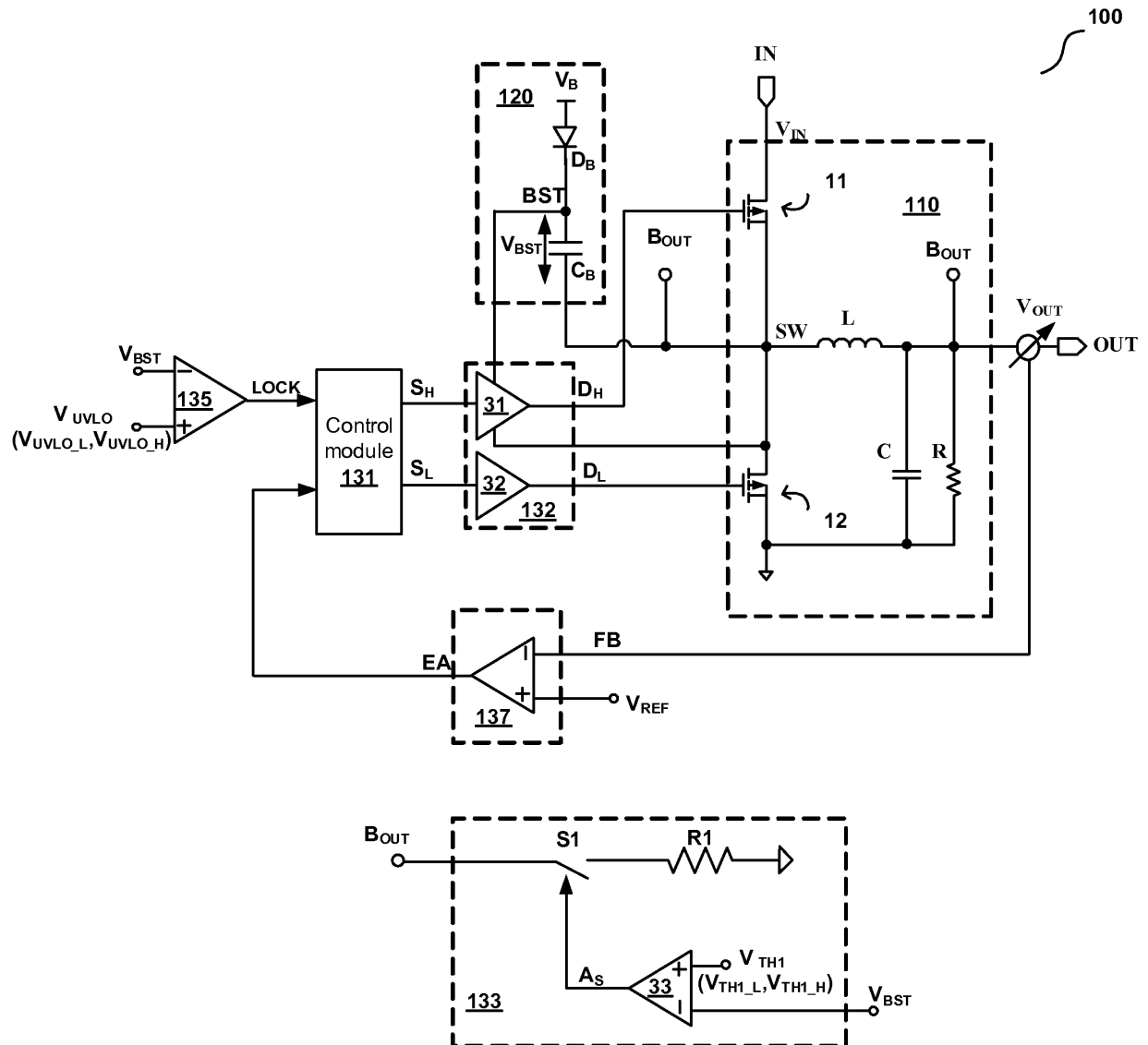
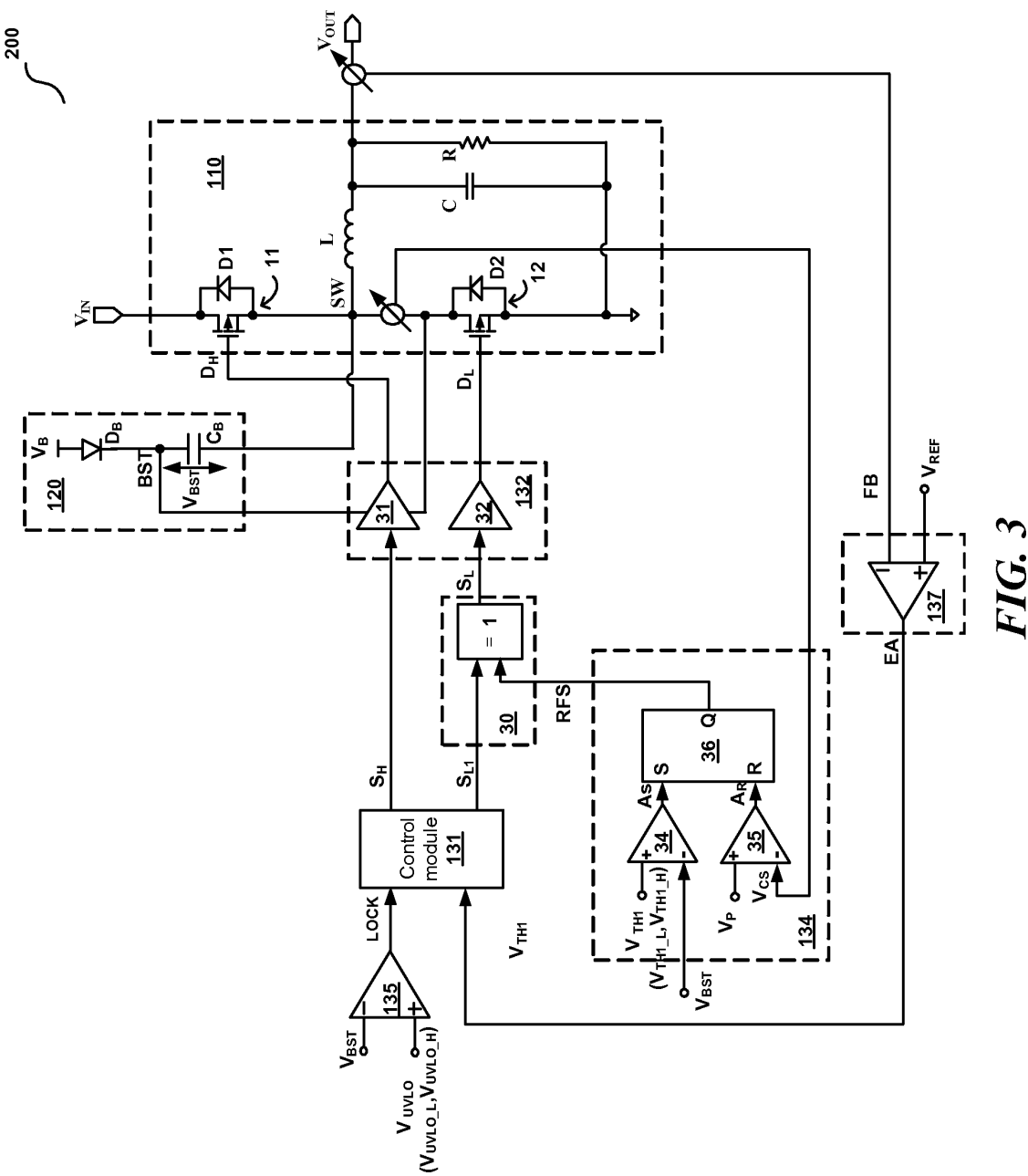
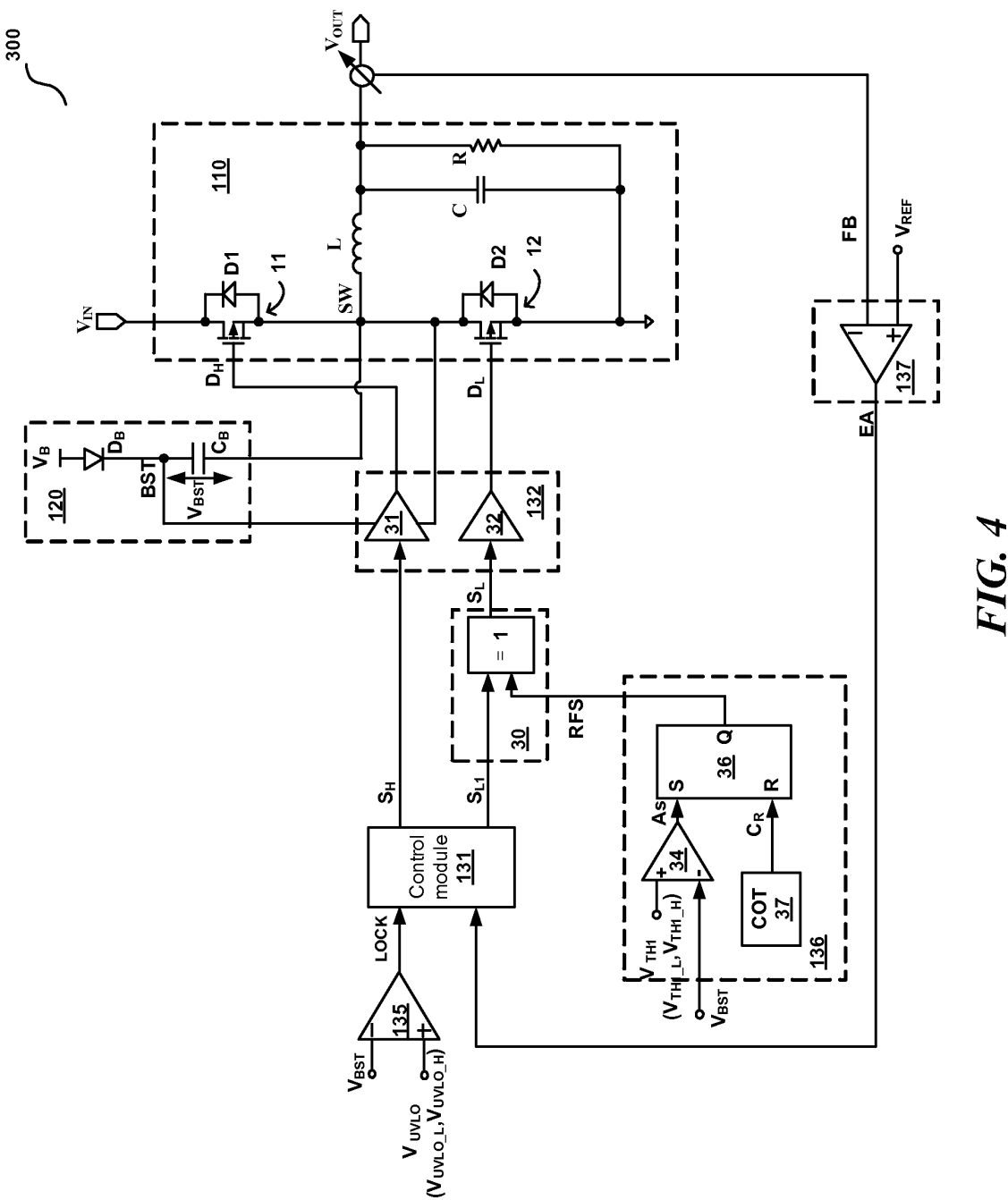


FIG. 2





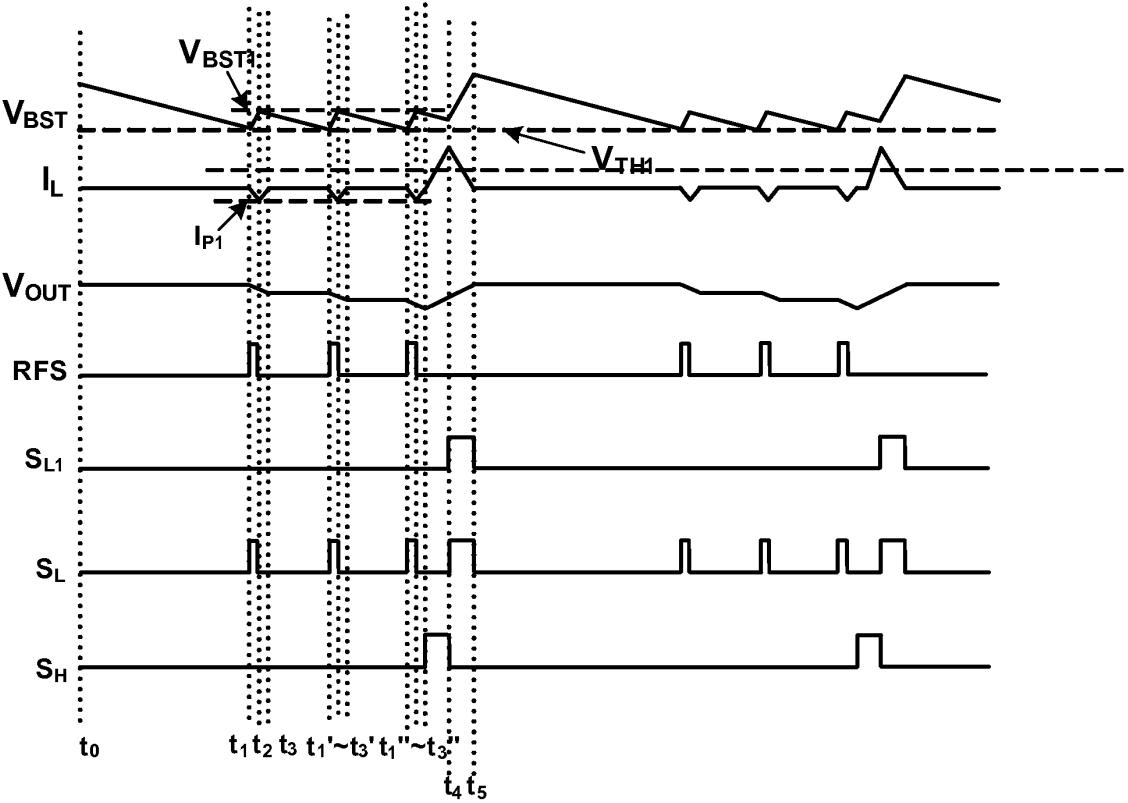


FIG. 5

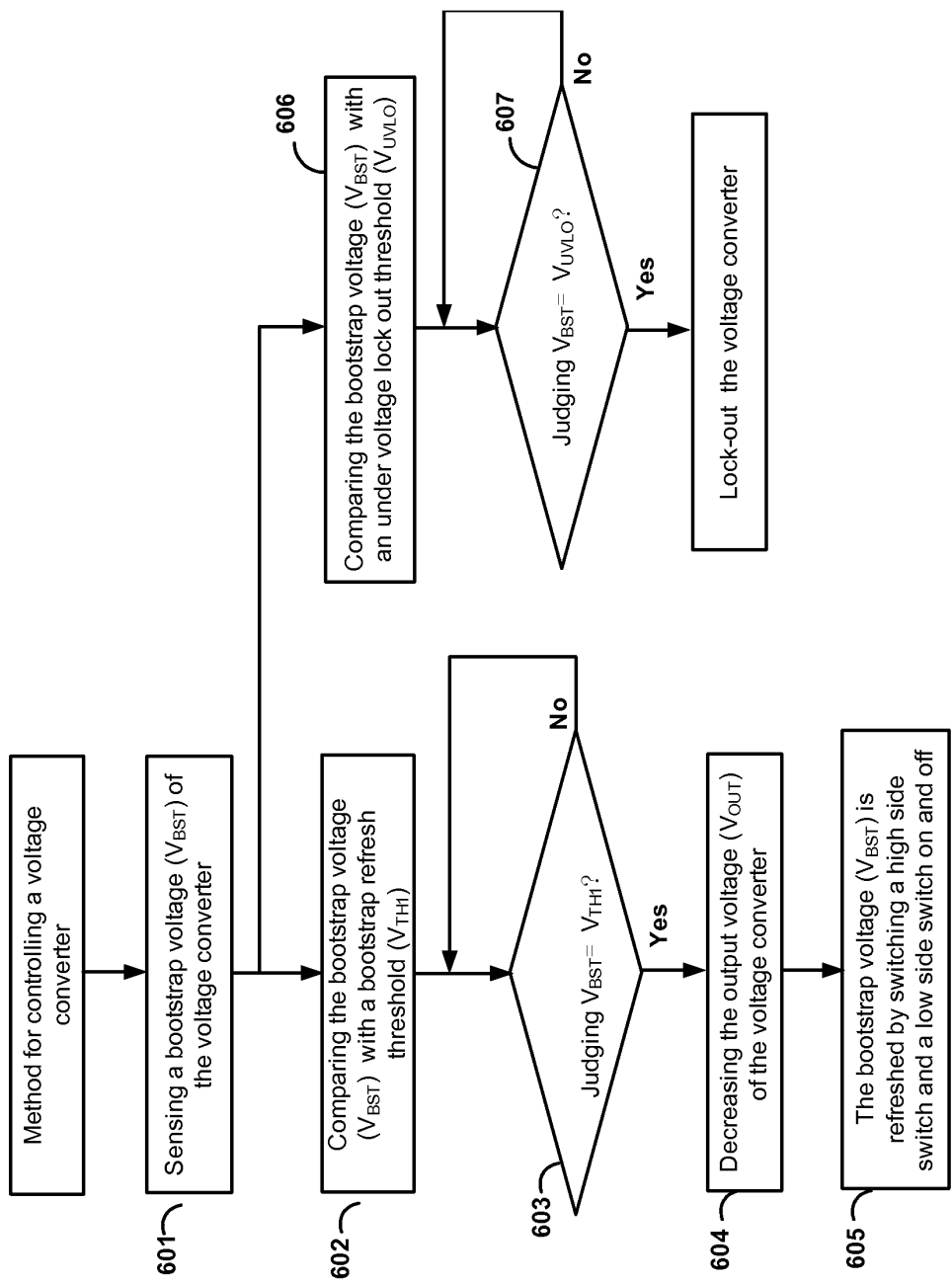


FIG. 6

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)	
Title of Invention	BOOTSTRAP REFRESH CONTROL CIRCUIT, VOLTAGE CONVERTER AND ASSOCIATED METHOD
As the below named inventor, I hereby declare that: This declaration ☒ The attached application, or is directed to: ☐ United States application or PCT international application number _____ filed on _____ The above-identified application was made or authorized to be made by me. I believe that I am the original inventor or an original joint inventor of a claimed invention in the application. I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both. I hereby state that I have reviewed and understand the contents of the above identified application, including the claims, as amended by any amendment specifically referred to above. I acknowledge the duty to disclose information material to patentability as defined in 37 C.F.R. 1.56 including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application. WARNING: Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.	
LEGAL NAME OF INVENTOR Inventor: _____ Li Xu _____ Date (Optional): <u>7.31.2015</u> Signature: <u>Li Xu</u> Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.	

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	38616-8386.US00
		Application Number	
Title of Invention	BOOTSTRAP REFRESH CONTROL CIRCUIT, VOLTAGE CONVERTER AND ASSOCIATED METHOD		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1					Remove
Legal Name					
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Li		Xu		
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
City	Chengdu	Country of Residence i	CN		
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City	Chengdu	State/Province			
Postal Code	611731	Country i	CN		
All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the Add button.					Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).			
☐ An Address is being provided for the correspondence Information of this application.			
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Application Information:

Title of the Invention	BOOTSTRAP REFRESH CONTROL CIRCUIT, VOLTAGE CONVERTER AND ASSOCIATED METHOD		
Attorney Docket Number	38616-8386.US00	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	6	Suggested Figure for Publication (if any)	

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	38616-8386.US00
		Application Number	
Title of Invention	BOOTSTRAP REFRESH CONTROL CIRCUIT, VOLTAGE CONVERTER AND ASSOCIATED METHOD		

Filing By Reference :

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	☒ Customer Number	☐ US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)
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Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.

When referring to the current application, please leave the application number blank.

Prior Application Status		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the Add button.			

Foreign Priority Information:

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	38616-8386.US00
		Application Number	
Title of Invention	BOOTSTRAP REFRESH CONTROL CIRCUIT, VOLTAGE CONVERTER AND ASSOCIATED METHOD		

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(d). When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX) the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(h)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove			
Application Number	Country ⁱ	Filing Date (YYYY-MM-DD)	Access Code ^j (if applicable)
201410390708.2	CN	2014-08-11	

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Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.

NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Authorization to Permit Access:

☐ Authorization to Permit Access to the Instant Application by the Participating Offices

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	38616-8386.US00
		Application Number	
Title of Invention	BOOTSTRAP REFRESH CONTROL CIRCUIT, VOLTAGE CONVERTER AND ASSOCIATED METHOD		

If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application.

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date of filing this Authorization.

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If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.			
Clear			
☒ Assignee	☐ Legal Representative under 35 U.S.C. 117	☐ Joint Inventor	
☐ Person to whom the inventor is obligated to assign.		☐ Person who shows sufficient proprietary interest	
If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:			
Name of the Deceased or Legally Incapacitated Inventor :			
If the Applicant is an Organization check here. ☒			
Organization Name	Chengdu Monolithic Power Systems Co., Ltd.		
Mailing Address Information:			
Address 1	No. 8 Kexin Road		
Address 2	West Zone of Hi-tech Zone		
City	Chengdu	State/Province	
Country ⁱ	CN	Postal Code	
Phone Number		Fax Number	

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	38616-8386.US00
		Application Number	
Title of Invention	BOOTSTRAP REFRESH CONTROL CIRCUIT, VOLTAGE CONVERTER AND ASSOCIATED METHOD		
Email Address			
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Assignee Information including Non-Applicant Assignee Information:

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Assignee 1				
Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.				
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Signature:

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Signature	/Rodney Tullett/		Date (YYYY-MM-DD)	2015-08-11	
First Name	Rodney	Last Name	Tullett	Registration Number	34034
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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	38616-8386.US00
		Application Number	
Title of Invention	BOOTSTRAP REFRESH CONTROL CIRCUIT, VOLTAGE CONVERTER AND ASSOCIATED METHOD		

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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Docket No.: 0386168386US
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

Li XU

Confirmation No.: N/A

Application No.: Not Yet Assigned

Art Unit: N/A

Filed: Concurrently Herewith

Examiner: Not Yet Assigned

For: BOOTSTRAP REFRESH CONTROL
CIRCUIT, VOLTAGE CONVERTER AND
ASSOCIATED METHOD

TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT (IDS)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Madam:

Pursuant to 37 CFR 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached PTO/SB/08. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement accompanies the new patent application submitted herewith.

In accordance with 37 C.F.R. § 1.98(a)(2)(ii), Applicant has not submitted copies of U.S. patents and U.S. patent applications. Applicant submits herewith copies of foreign patents and non-patent literature in accordance with 37 C.F.R. § 1.98(a)(2).

This Information Disclosure Statement is not to be construed as a representation that: (i) a search has been made; (ii) additional information that may be material to the examination of this application does not exist; (iii) the information, protocols, results and the like reported by third parties are accurate or enabling; or (iv) the cited information is, or is considered to be, material to patentability. In addition, applicant does not admit that any enclosed item of information constitutes prior art to the subject invention and specifically reserves the right to demonstrate that any such reference is not prior art.

It is submitted that the Information Disclosure Statement is in compliance with 37 CFR 1.98 and the Examiner is respectfully requested to consider the listed references.

The Director is hereby authorized to charge any deficiency in the fees filed, asserted to be filed or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to our Deposit Account No. 50-0665, under Order No. 0386168386US.

Dated: August 11, 2015

Respectfully submitted,

Electronic signature: / Rodney Tullett /
Rodney C. Tullett

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POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(b).

I hereby appoint:

☒ Practitioners associated with the Customer Number: 67394

AND

☒ Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number
Roland Tso	39,043		

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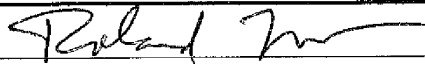
Assignee Name and Address:

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West Hi-tech Zone
Chengdu, China 611731

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SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature		Date	December 9, 2014
Name	Roland Tso	Telephone	408 826 0726
Title	Director of Patents		

Electronic Acknowledgement Receipt	
EFS ID:	23254407
Application Number:	14823900
International Application Number:	
Confirmation Number:	6869
Title of Invention:	BOOTSTRAP REFRESH CONTROL CIRCUIT, VOLTAGE CONVERTER AND ASSOCIATED METHOD
First Named Inventor/Applicant Name:	Li Xu
Customer Number:	67394
Filer:	Chun Ng/Christina Kim
Filer Authorized By:	Chun Ng
Attorney Docket Number:	38616-8386.US00
Receipt Date:	19-AUG-2015
Filing Date:	
Time Stamp:	16:25:35
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
------------------------	----

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		2015-08-19_38616-8386US_PO A.pdf	109076 e0ea3f9b1bfec3fb55d9632855738089c8786601	yes	4

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Assignee showing of ownership per 37 CFR 3.73	1	3
	Power of Attorney	4	4
Warnings:			
Information:			
Total Files Size (in bytes):		109076	
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.			

STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: CHENGDU MONOLITHIC POWER SYSTEMS CO., LTD.

Application No./Patent No.: 14/823,900 Filed/Issue Date: 08/11/2015

Titled: BOOTSTRAP REFRESH CONTROL CIRCUIT, VOLTAGE CONVERTER AND ASSOCIATED METHOD

CHENGDU MONOLITHIC POWER SYSTEMS CO., LTD., a CORPORATION

(Name of Assignee)

(Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☒ The assignee of the entire right, title, and interest.
2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):
- ☐ The extent (by percentage) of its ownership interest is ____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.
- ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (e.g., bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

- A. ☒ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 036302, Frame 0287, or for which a copy thereof is attached.

- B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

2. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

[Page 1 of 2]

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☐ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Chun M. Ng/

Signature

Chun Ng

Printed or Typed Name

August 19, 2015

Date

36,878

Title or Registration Number

[Page 2 of 2]

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 14/823,900	
APPLICATION AS FILED - PART I							
(Column 1)		(Column 2)		SMALL ENTITY		OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	600
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720
TOTAL CLAIMS (37 CFR 1.16(j))	16	minus 20 = *			OR	x 80 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3	minus 3 = *			OR	x 420 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL		TOTAL	1600
APPLICATION AS AMENDED - PART II							
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY	
AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=
	Application Size Fee (37 CFR 1.16(s))						
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	
(Column 1)		(Column 2)		(Column 3)		OTHER THAN SMALL ENTITY	
AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=
	Application Size Fee (37 CFR 1.16(s))						
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.							



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United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO.	TOT CLAIMS	IND CLAIMS
14/823,900	08/11/2015	2842	1600	38616-8386.US00	16	3

CONFIRMATION NO. 6869

FILING RECEIPT



0000000077077469

67394

Perkins Coie LLP - Monolithic Power Systems

P.O. BOX 1247

SEATTLE, WA 98111-1247

Date Mailed: 08/26/2015

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Li Xu, Chengdu, CHINA;

Applicant(s)

Chengdu Monolithic Power Systems Co., Ltd., Chengdu, CHINA;

Power of Attorney: The patent practitioners associated with Customer Number 67394

Domestic Applications for which benefit is claimed - None.

A proper domestic benefit claim must be provided in an Application Data Sheet in order to constitute a claim for domestic benefit. See 37 CFR 1.76 and 1.78.

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.)

CHINA 201410390708.2 08/11/2014

Request to Retrieve - This application either claims priority to one or more applications filed in an intellectual property Office that participates in the Priority Document Exchange (PDX) program or contains a proper **Request to Retrieve Electronic Priority Application(s)** (PTO/SB/38 or its equivalent). Consequently, the USPTO will attempt to electronically retrieve these priority documents.

If Required, Foreign Filing License Granted: 08/25/2015

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 14/823,900**

Projected Publication Date: 02/11/2016

Non-Publication Request: No

Early Publication Request: No

page 1 of 3

Title

BOOTSTRAP REFRESH CONTROL CIRCUIT, VOLTAGE CONVERTER AND ASSOCIATED METHOD

Preliminary Class

327

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER
Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

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0512-CHN-I

中华人民共和国国家知识产权局
STATE INTELLECTUAL PROPERTY OFFICE
OF THE PEOPLE'S REPUBLIC OF CHINA



证 明

本证明之附件是向本局提交的下列专利申请文件副本。

请 号: 201410390708.2

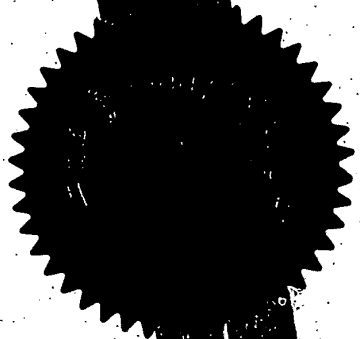
类 型: 发明专利

发明名称: 一种自举电压刷新控制电路、电压转换电路及其控制方法

申 日: 2014年08月11日

申 人: 成都芯源系统有限公司

发明设计人: 许力



局长
申长雨

申长雨

2014 年 09 月 10 日



权利要求书

1、一种自举电压刷新控制电路，用于电压转换电路，其中所述电压转换电路包括高侧开关和低侧开关以及用于为所述高侧开关提供自举电压信号的自举电容，所述电压转换电路基于所述高侧开关和低侧开关的导通和关断切换将其输入端的输入电压转换为其输出端的输出电压，所述自举电压刷新控制电路包括：

自举电压刷新模块，所述自举电压刷新模块包括第一比较模块，所述第一比较模块具有第一输入端、第二输入端和输出端，其中第一比较模块的第一输入端用于接收所述自举电压信号；第一比较模块的第二输入端用于接收一自举电压刷新阈值；第一比较模块用于将所述自举电压信号与所述自举电压刷新阈值进行比较并在第一比较模块的输出端提供第一比较信号；其中，若所述自举电压信号低于所述自举电压刷新阈值，所述第一比较信号具有第一逻辑状态；若所述自举电压信号高于所述自举电压刷新阈值，所述第一比较信号具有第二逻辑状态；以及

电压差值模块，具有第一输入端、第二输入端和输出端，所述电压差值模块的第一输入端接收代表所述输出电压的反馈信号；所述电压差值模块的第二输入端接收参考信号；所述电压差值模块对所述反馈信号和所述参考信号进行比较，并在其输出端输出差值信号；

其中，当所述第一比较信号具有第一逻辑状态时，所述自举电压刷新模块用于降低所述输出电压，当所述反馈信号小于所述参考信号时，所述自举电压刷新控制电路根据所述差值信号控制所述高侧开关和所述低侧开关开始导通和关断切换，所述自举电容被充电，所述自举电压被刷新。

2、根据权利要求1所述的自举电压刷新控制电路，其特征在于：

所述自举电压刷新阈值包括第一刷新阈值和第二刷新阈值，其中所述第一刷新阈值小于所述第二刷新阈值；

若所述自举电压信号低于所述第一刷新阈值，所述第一比较信号具有第一逻辑状态；



...

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1

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•

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Age Group	Percentage
18-29	85%
30-49	80%
50-69	75%
70+	65%



以及

新信号:

低侧开关关断。

自举电压刷新控制电路进一步包括:

号:

举电压欠压阈值信号，所述自举欠压信号具有第二逻辑状态；以及

制电路基于该自举欠压信号将所述高侧开关和所述低侧开关关断, 停





控制模块，具有第一输入端、第二输入端、第三输入端、第一输出端以及第二输出端；控制模块的第一输入端耦接至所述电压误差放大模块的输出端接收所述误差放大信号；控制模块的第二输入端耦接至自举电压刷新模块接收自举电压刷新信号；控制模块的第三输入端耦接至自举欠压闭锁模块接收自举欠压闭锁信号；控制模块的第一输出端输出高侧开关控制信号控制高侧开关的导通和关断切换；控制模块的第二输出端输出低侧开关控制信号控制低侧开关的导通和关断切换；以及

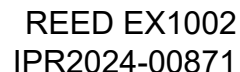
8、一种电压转换电路，包括：

自举电路，包括自举电容，用于为所述高侧开关提供自举电压信号；以及

9、一种自举电压刷新控制方法，用于电压转换电路，其中所述电压转换电路包括高侧开关和低侧开关以及用于为所述高侧开关提供自举电压的自举电容，所述电压转换电路基于所述高侧开关和低侧



根据第一比较信号和恒定导通时间控制信号提供自举电压刷新





信号；以及

基于所述自举电压刷新信号控制所述低侧开关的导通与关断切换以降低输出电压；

其中，若所述自举电压低于所述自举电压刷新阈值，所述自举电压刷新信号具有第一逻辑状态，导通所述低侧开关；

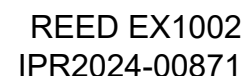
当低侧开关导通所述恒定导通时间之后，所述自举电压刷新信号具有第二逻辑状态，关断低侧开关。







在图 1 所示实施例中，自举电路 53 包括二极管 D_B 和自举电容 C_B ，串联耦接于自举供电输入端和节点 SW 之间，其中二极管 D_B 的阳极耦接自举供电输入端接收自举供电电压 V_B ，二极管 D_B 的阴极耦接自举电容 C_B 的第一端，自举电容 C_B 的第二端耦接节点 SW。自举

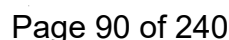






发明内容

本发明一方面提供了一种自举电压刷新控制电路，用于电压转换电路，其中所述电压转换电路包括高侧开关和低侧开关以及用于为所述高侧开关提供自举电压信号的自举电容，所述电压转换电路基于所述高侧开关和低侧开关的导通和关断切换将其输入端的输入电压转换为其输出端的输出电压。所述自举电压刷新控制电路包括：自举电压刷新模块，所述自举电压刷新模块包括第一比较模块，所述第一比较模块具有第一输入端、第二输入端和输出端，其中第一比较模块的第一输入端用于接收所述自举电压信号；第一比较模块的第二输入端用于接收一自举电压刷新阈值；第一比较模块用于将所述自举电压信号与所述自举电压刷新阈值进行比较并在第一比较模块的输出端提

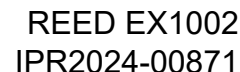








在一个实施例中，控制电路包括电压差值模块 137。电压差值模块 137 具有第一输入端、第二输入端和输出端。电压差值模块 137 的第一输入端耦接至电压转换电路 100 的输出端 OUT 接收输出电压 V_{OUT} 的反馈信号 FB；电压差值模块 137 的第二输入端接收参考电压信号 V_{REF} ；电压差值模块 137 将输出电压反馈信号 FB 和参考电压信号 V_{REF} 进行比较，并在其输出端输出差值信号 EA。在一个实施例中，例如电压控制、电流控制等 PWM 控制方法实施例中，电压差值模块 137 包括一个误差放大器，用于将输出电压反馈信号 FB 和参考电压





信号 V_{REF} 比较后的差值放大，再将该差值放大信号和一个斜坡信号进行比较，进而控制高侧开关 11 和低侧开关 12 的导通和关断切换。在另一个实施例中，例如恒定导通时间控制等 PFM 控制方法实施例中，电压差值模块 137 包括一个电压比较器，用于将输出电压反馈信号 FB 和参考电压信号 V_{REF} 比较，根据比较结果控制高侧开关 11 和低侧开关 12 的导通和关断切换。比如，当输出电压反馈信号 FB 小于参考电压信号 V_{REF} 时高侧开关 11 导通，低侧开关 12 关断；当输出电压反馈信号 FB 大于参考电压信号 V_{REF} 时高侧开关 11 关断，低侧开关 12 导通。

在一个实施例中，控制电路进一步包括控制模块 131。控制模块 131 耦接至电压差值模块 137 的输出端接收差值信号 EA，并根据差值信号 EA 判定输出端的负载情况进而输出高侧开关控制信号 S_H 和低侧开关控制信号 S_L 用于控制高侧开关 11 和低侧开关 12 的导通和关断切换。

在一个实施例中，控制电路进一步包括驱动模块 132。驱动模块 132 包括第一驱动器 31 和第二驱动器 32。第一驱动器 31 具有输入端和输出端，第一驱动器 31 的输入端接收高侧开关控制信号 S_H ，并在其输出端输出高侧开关驱动信号 D_H 至高侧开关 11 的栅极，以驱动高侧开关 11 的导通和关断。第一驱动器 31 包括接收自举电压 V_{BST} ，用于提升/增强第一驱动器 31 提供的高侧开关驱动信号 D_H 的驱动能力，从而更好地控制高侧开关 11 的导通和关断。第二驱动器 32 具有输入端和输出端，第二驱动器 32 的输入端接收低侧开关控制信号 S_L ，并



在其输出端输出低侧开关驱动信号 D_L 至低侧开关的栅极，以驱动低侧开关 12 的导通和关断。根据本发明的一个实施例，所述第一驱动器 31 包括一个或多个反相器，所述自举电压信号 V_{BST} 用作所述一个或多个反相器的供电电源。类似地，所述第二驱动器 32 也可以包括一个或多个反相器。

在一个实施例中，控制电路进一步包括自举电压刷新模块 133。自举电压刷新模块 133 接收自举电压信号 V_{BST} ，并将自举电压信号 V_{BST} 与一个自举电压刷新阈值进行比较。在轻载或空载模式下，高侧开关 11 和低侧开关 12 均关断，流过电感 L 的电感电流为零。与此同时，自举电压 V_{BST} 逐渐降低，当自举电压信号 V_{BST} 小于自举电压刷新阈值时，自举电压刷新模块 133 启用，用于降低输出电压 V_{OUT} 。电压差值模块 137 将代表输出电压 V_{OUT} 的反馈电压 FB 和参考电压信号 V_{REF} 比较，当反馈信号 FB 小于所述参考电压信号 V_{REF} 时，控制模块 131 根据差值信号 EA 控制高侧开关 11 和低侧开关 12 开始导通和关断切换，以使输出电压 V_{OUT} 维持在预设值。即高侧开关 11 和低侧开关 12 从均关断的轻载或空载状态转换为导通和关断切换的正常状态。当高侧开关 11 和低侧开关 12 的切换频率变高，则低侧开关 12 的导通时间增加，自举电容 C_B 可及时被充电，自举电压 V_{BST} 被刷新恢复至期望值。采用自举电压刷新模块 133 降低输出电压 V_{OUT} ，进而增大高侧开关 11 和低侧开关 12 的切换频率以刷新自举电压 V_{BST} ，可以避免使用消隐电路消隐高侧开关 11，同时不影响电压转换电路的控制方式和开关时序，即该实施例通过高侧开关 11 和低侧开关 12





的正常切换就能刷新自举电压 V_{BST} 。

在一个实施例中，自举电压刷新模块 133 包括输入端和输出端，自举电压刷新模块 133 的输入端接收自举电压信号 V_{BST} ，自举电压刷新模块 133 的输出端耦接至开关电路 110 的节点 SW，用于降低输出电压 V_{OUT} 。在另一个实施例中，自举电压刷新模块 133 的输出端耦接至电压变换电路 100 的输出端 OUT，用于降低输出电压 V_{OUT} 。在又一个实施例中，自举电压刷新模块 133 的输出端可以同时耦接至开关电路 110 的节点 SW 处和电压转换电路 100 的输出端 OUT，以加快降低输出电压 V_{OUT} 。

在一个实施例中，自举电压刷新模块 133 包括比较电路 33，比较电路 33 具有第一输入端、第二输入端和输出端。比较电路 33 的第一输入端用于接收自举电压信号 V_{BST} ，比较电路 33 的第二输入端用于接收自举电压刷新阈值 V_{TH1} 。比较电路 33 用于将自举电压信号 V_{BST} 与自举电压刷新阈值 V_{TH1} 相比较，并在所述比较电路 33 的输出端提供第一比较信号 A_S 。若自举电压信号 V_{BST} 低于自举电压刷新阈值信号 V_{TH1} ，则第一比较信号 A_S 具有第一逻辑状态（比如高电平逻辑状态）；若自举电压信号 V_{BST} 高于自举电压刷新阈值信号 V_{TH1} ，则第一比较信号 A_S 具有第二逻辑状态（比如低电平逻辑状态）。

在一个实施例中，自举电压刷新模块 133 还包括开关 S1 和电阻 R1。开关 S1 具有第一端、第二端和控制端。开关 S1 的第一端耦接于电阻 R1 的一端，开关 S1 的第二端作为自举电压刷新模块 133 的输出端提供自举电压刷新信号 RFS，开关 S1 的控制端耦接比较电路





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图3所示为根据本发明一个实施例的电压转换电路200的示意图。

如图3所示，电压转换电路200包括开关电路110、驱动电路120以及控制电路。为了简便且便于理解，电压转换电路200中那些功能上和电压转换电路100中相同的、同样的或类似的组件或结构沿用了相同的附图标记。同时，在图3所示实施例中，对于开关电路110中的高侧开关11和低侧开关12，示出了其体二极管。具体的来说，示出了高侧开关11的体二极管D1和低侧开关12的体二极管D2。此外，在图3所示实施例中，高侧开关11和低侧开关12被示意为金属氧化物半导体场效应晶体管（MOSFET），但应该理解，高侧开关11和低侧开关12不局限于MOSFET，在其他实施例中，高侧开关11和低侧开关12还可以是其他任何可控的半导体开关器件，如结型场效应晶体管（JFET）或绝缘栅双极晶体管（IGBT）。

在一个实施例中，电压转换电路200中控制电路包括：控制模块131、驱动模块132、电压差值模块137、自举电压刷新模块134以及自举欠压闭锁模块135。为了简便且便于理解，电压转换电路200的控制电路中那些功能上和电压转换电路100的控制电路中相同的、同样的或类似的组件或结构沿用了相同的附图标记的模块的功能不再累述。

自举电压刷新模块134包括第一输入端和输出端。自举电压刷新模块134的第一输入端耦接至自举电路120接收自举电压信号 V_{BST} ，并将自举电压信号 V_{BST} 与一个自举电压刷新阈值进行比较。在轻载或空载模式下，高侧开关11和低侧开关12均关断，流过电感L的电





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电容器 C 通过电感器 L 和低侧开关 12 放电，电感器 L 反向储能，自举电容 C_B 被充电；当自举电压刷新信号 RFS 为第二逻辑状态时，低侧开关 12 关断，自举电容 C_B 停止被充电；流过电感器 L 的电流通过高侧开关 11 的体二极管 $D1$ 续流。

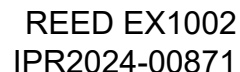
在一个实施例中，控制模块 131 耦接至电压差值模块 137 的输出端，接收差值信号 EA ，并根据差值信号 EA 的变化提供高侧开关控制信号 S_H 和第一低侧开关控制信号 S_{L1} 。高侧开关控制信号 S_H 和第一低侧开关控制信号 S_{L1} 用于控制高侧开关 11 和低侧开关 12 的导通和关断切换。在一个实施例中，当第一低侧开关控制信号 S_{L1} 具有第一逻辑状态（例如逻辑高状态），低侧开关 12 导通；当第一低侧开关控制信号 S_{L1} 具有第二逻辑状态（例如逻辑低状态），低侧开关 12 关断。在一个实施例中，控制模块 131 还包括一个逻辑模块 30。逻辑模块 30 具有第一输入端、第二输入端和输出端。逻辑模块 30 的第一输入端接收第一低侧开关控制信号 S_{L1} ；逻辑模块 30 的第二输入端接收自举电压刷新信号 RFS ；逻辑模块 30 对第一低侧开关控制信号 S_{L1} 和自举电压刷新信号 RFS 做逻辑运算，并在其输出端输出低侧开关控制信号 S_L 。当第一低侧开关控制信号 S_{L1} 和自举电压刷新信号 RFS 任意一个具有第一逻辑状态（例如逻辑高状态），则低侧开关控制信号 S_L 具有第一逻辑状态（例如逻辑高状态），低侧开关 12 导通。在一个实施例中，逻辑模块 30 为一个逻辑或门。

图 4 所示为根据本发明一个实施例的电压转换电路 300 的示意图。
在图 4 所示一个实施例中，电压转换电路 300 中控制电路包括：控制



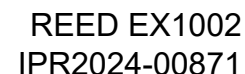


在一个实施例中，自举电压刷新模块 136 进一步包括逻辑电路





在一个实施例中,当自举电压刷新信号 RFS 为第一逻辑状态时,低侧开关管 12 导通,开关电路 110 中的电容器 C 通过电感器 L 和低侧开关 12 放电,电感器 L 反向储能,流过低侧开关 12 的反向电流增大,输出电压 V_{OUT} 降低,与此同时,自举电容 C_B 也将被充电。当自举电压刷新信号 RFS 为第二逻辑状态时,低侧开关 12 关断,自举电容 C_B 停止被充电。此时,流过电感器 L 的电流通过高侧开关 11 的体二极管 D1 续流,开关电路 110 变为一个 BOOST 升压变换器,电容器 C 释放的能量将被存储在电压变换电路 200 的输入端 IN。在一个实施例中,恒定导通时间电路 37 设定的导通时间越长,自举电压信号 V_{BST} 恢复的值越大。但是从总体上来说,自举电压刷新电路 136 主要用于降低输出电压 V_{OUT} ,因此恒定导通时间电路 37 设定的导通时间不会太长,低侧开关 12 导通的时间较短,因此自举电压 V_{BST} 恢复的值有限。一旦输出电压 V_{OUT} 降低,控制模块 131 将根据差值信号 EA 控制高侧开关 11 和低侧开关 12 开始导通和关断切换,自举电





压 V_{BST} 将被刷新恢复至期望值。

图 5 所示为根据本发明一个实施例的电压转换电路 200 的工作波形示意图。在 t_0 时刻，高侧开关控制信号 S_H 和低侧开关控制信号 S_L 为低电平，高侧开关 11 和低侧开关 12 均关断。此时，电压转换电路 300 的输出电压 V_{OUT} 保持不变，流过开关电路 110 中的电感器 L 的电流 I_L 为零。

在 t_0 至 t_1 时刻，高侧开关控制信号 S_H 和低侧开关控制信号 S_L 保持为低电平，因此高侧开关 11 和低侧开关 12 保持关断状态，流过电感器 L 的电流 I_L 依然为零。由于电压转换电路 300 工作在轻载模式下，因此输出电压 V_{OUT} 基本保持不变。同时，由于低侧开关 12 一直保持关断状态，自举电路 120 中的自举电容 C_B 不能及时被充电，自举电压 V_{BST} 下降。

在 t_1 时刻，当自举电压 V_{BST} 下降至自举电压刷新阈值 V_{TH1} 时，自举电压刷新电路 134 中的第一比较信号 A_S 为高电平信号，自举刷新信号 RFS 为高电平，因此，控制模块 131 控制低侧开关控制信号 S_L 变为高电平，低侧开关 12 导通。

在 t_1 至 t_2 时刻，低侧开关控制信号 S_L 维持在高电平，低侧开关 12 保持导通状态。开关电路 110 中的电容器 C 通过电感器 L 和低侧开关 12 放电，流过电感器 L 的电流 I_L 为一反向升高的电流信号；输出电压 V_{OUT} 随着电容器 C 的放电而降低。与此同时，自举电路 120 中的自举电容 C_B 通过低侧开关 12 电连接至逻辑地，因此自举电容 C_B 被充电，自举电压 V_{BST} 升高。











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因此,上述本发明的说明书和实施方式仅仅以示例性的方式对本发明实施例的自举电压刷新控制电路、包含该自举电压刷新控制电路的电压转换电路及其控制方法进行了说明,并不用于限定本发明的范围。对于公开的实施例进行变化和修改都是可能的,其他可行的选择性实施例和对实施例中元件的等同变化可以被本技术领域的普通技术人员所了解。本发明所公开的实施例的其他变化和修改并不超出本发明的精神和保护范围。



说明书附图

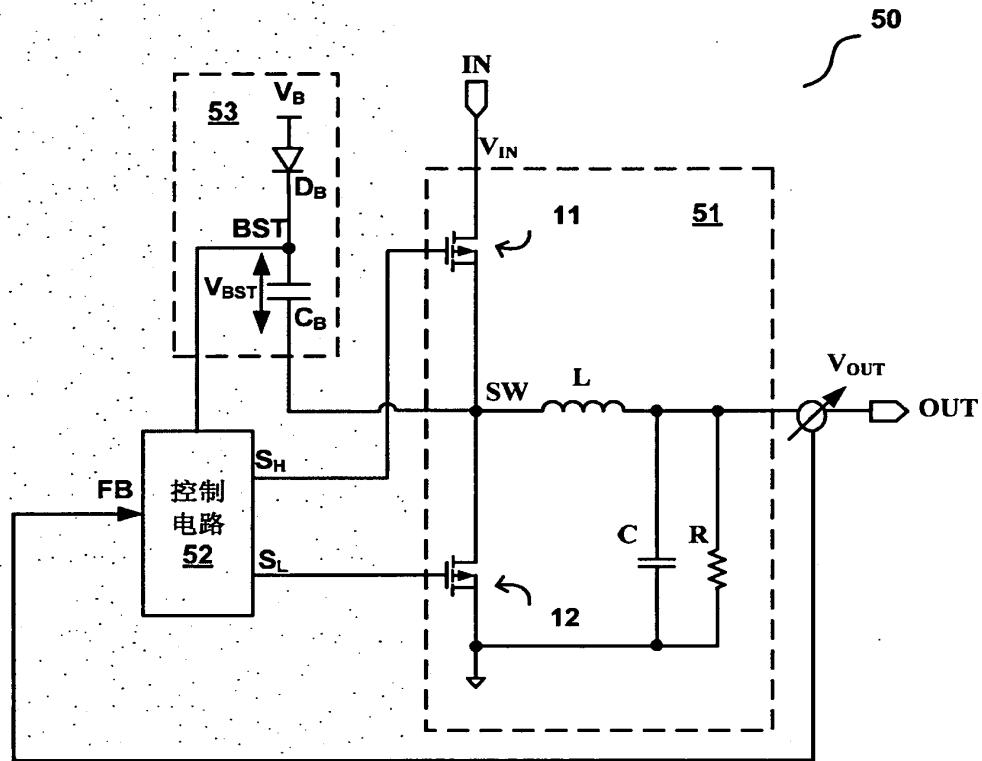
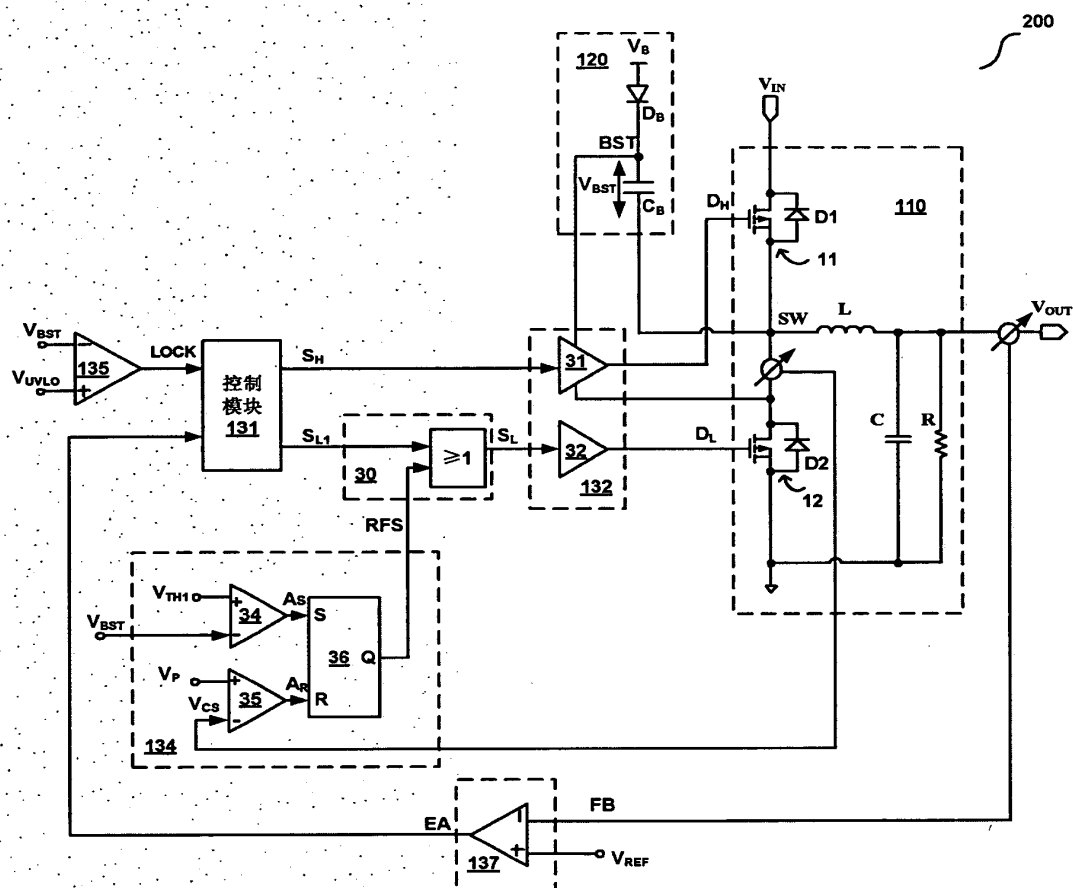


图 1





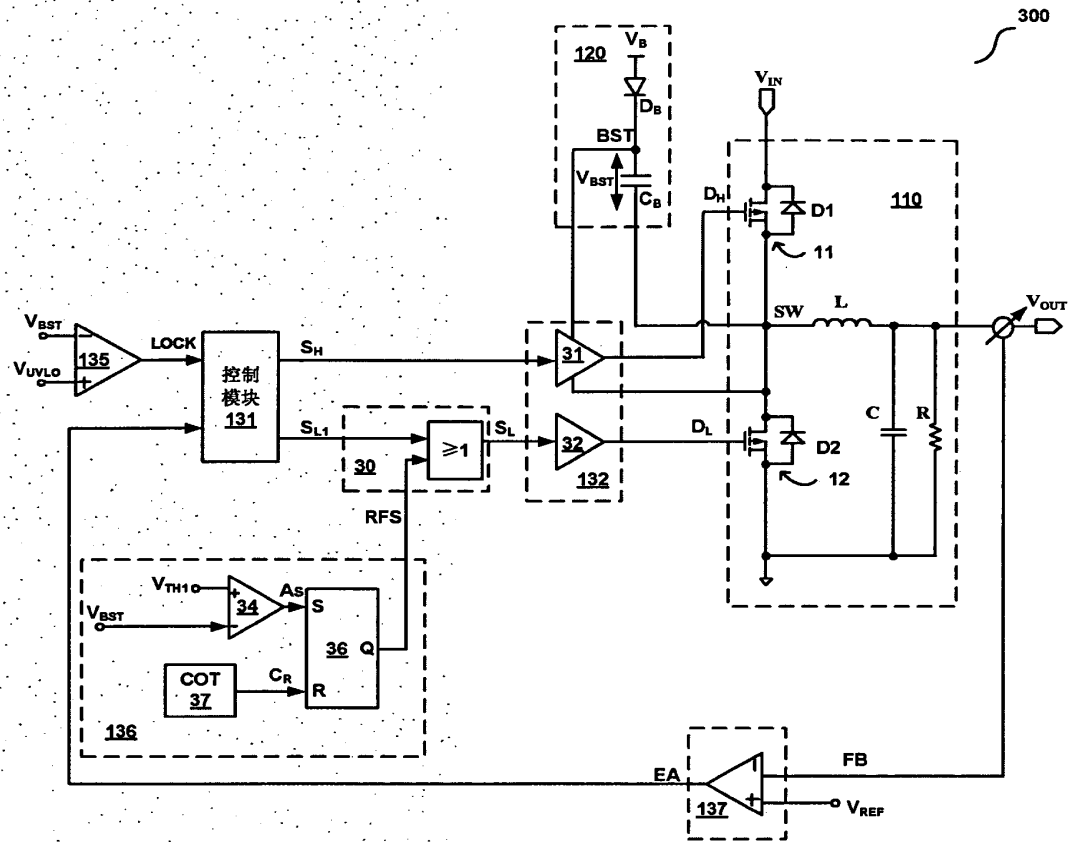


图 4

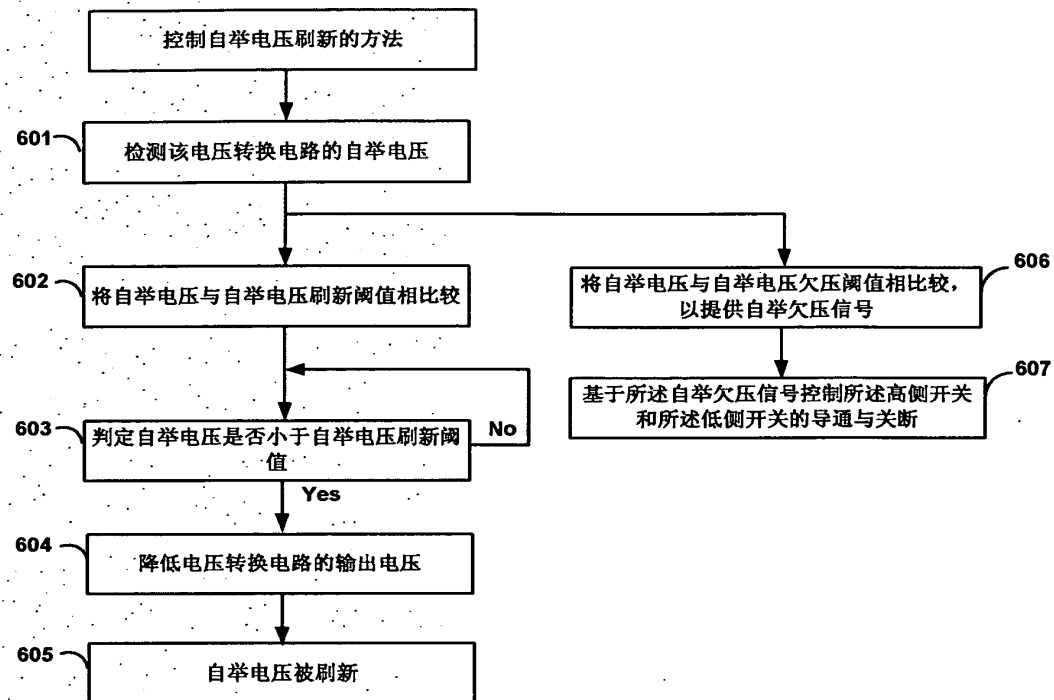


图 6

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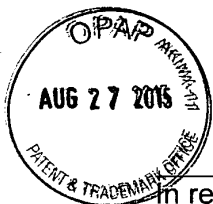
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I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the U.S. Postal Service on the date shown below with sufficient postage as First Class Mail, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Dated: August 24, 2015 Signature: 

Christina J. Kim

Docket No.: 038616-8386.US00
(PATENT)



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

LI et al.

Confirmation No.: 6869

Application No.: 14/823,900

Art Unit: Not Yet Assigned

Filed: August 11, 2015

Examiner: Not Yet Assigned

For: BOOTSTRAP REFRESH CONTROL
CIRCUIT, VOLTAGE CONVERTER
AND ASSOCIATED METHOD

SUBMISSION OF PRIORITY DOCUMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Madam:

Applicants hereby claim priority under 35 U.S.C. § 119 based on the following prior foreign application filed in the following foreign country on the date indicated:

Country	Application No.	Date
China	201410390708.2	August 11, 2014

In support of this claim, a certified copy of the said original foreign application is filed herewith.

38616-8386.US00/LEGAL127414757.1

No fee is believed due; however, the Director is hereby authorized to charge any underpayment or credit any overpayment to Deposit Account No. 50-0665, under Order No. 038616-8386.US00 from which the undersigned is authorized to draw.

Dated: August 20, 2015

Respectfully submitted,

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证 明

本证明之附件是向本局提交的下列专利申请文件副本。

申 请 号：201410390708.2

申 请 类 型：发明专利

发 明 创 造 名 称：一种自举电压刷新控制电路、电压转换电路及其控制方法

申 请 日：2014 年 08 月 11 日

申 请 人：成都芯源系统有限公司

发明人或设计人：许力

局长

申长雨

2015 年 11 月 30 日



权利要求书

1、一种自举电压刷新控制电路，用于电压转换电路，其中所述电压转换电路包括高侧开关和低侧开关以及用于为所述高侧开关提供自举电压信号的自举电容，所述电压转换电路基于所述高侧开关和低侧开关的导通和关断切换将其输入端的输入电压转换为其输出端的输出电压，所述自举电压刷新控制电路包括：

自举电压刷新模块，所述自举电压刷新模块包括第一比较模块，所述第一比较模块具有第一输入端、第二输入端和输出端，其中第一比较模块的第一输入端用于接收所述自举电压信号；第一比较模块的第二输入端用于接收一自举电压刷新阈值；第一比较模块用于将所述自举电压信号与所述自举电压刷新阈值进行比较并在第一比较模块的输出端提供第一比较信号；其中，若所述自举电压信号低于所述自举电压刷新阈值，所述第一比较信号具有第一逻辑状态；若所述自举电压信号高于所述自举电压刷新阈值，所述第一比较信号具有第二逻辑状态；以及

电压差值模块，具有第一输入端、第二输入端和输出端，所述电压差值模块的第一输入端接收代表所述输出电压的反馈信号；所述电压差值模块的第二输入端接收参考信号；所述电压差值模块对所述反馈信号和所述参考信号进行比较，并在其输出端输出差值信号；

其中，当所述第一比较信号具有第一逻辑状态时，所述自举电压刷新模块用于降低所述输出电压，当所述反馈信号小于所述参考信号时，所述自举电压刷新控制电路根据所述差值信号控制所述高侧开关和所述低侧开关开始导通和关断切换，所述自举电容被充电，所述自举电压被刷新。

2、根据权利要求1所述的自举电压刷新控制电路，其特征在于：

所述自举电压刷新阈值包括第一刷新阈值和第二刷新阈值，其中所述第一刷新阈值小于所述第二刷新阈值；

若所述自举电压信号低于所述第一刷新阈值，所述第一比较信号具有第一逻辑状态；



若所述自举电压信号高于所述第二刷新阈值，所述第一比较信号具有第二逻辑状态。

3. 根据权利要求 1 所述的自举电压刷新控制电路，其中，所述高侧开关和所述低侧开关具有公共节点，所述自举电压刷新模块还包括开关管和电阻，其中，

所述开关管具有第一端、第二端和控制端，其中所述开关管的第一端耦接至所述电压转换电路的输出端和/或所述公共节点；所述开关管的第二端耦接电阻的一端；所述开关管的控制端接收所述第一比较信号；所述电阻的第二端电连接至逻辑地；

若所述第一比较信号具有第一逻辑状态，所述开关管导通；若所述第一比较信号具有第二逻辑状态，所述开关管关断。

4. 根据权利要求 1 所述的自举电压刷新控制电路，其中，所述自举电压刷新模块进一步包括：

第二比较模块，具有第一输入端、第二输入端和输出端，其中第二比较模块的第一输入端用于接收所述低侧开关的电流采样信号；第二比较模块的第二输入端用于接收一电流阈值信号；第二比较模块用于将所述电流采样信号与所述电流阈值信号进行比较并在第二比较模块的输出端提供第二比较信号；其中，若所述电流采样信号高于所述电流阈值信号，所述第二比较信号具有第一逻辑状态；若所述电流采样信号低于所述电流阈值信号，所述第二比较信号具有第二逻辑状态；以及

第一逻辑模块，具有第一输入端、第二输入端以及输出端，其中第一逻辑模块的第一输入端耦接至第一比较模块的输出端，接收第一比较信号；第一逻辑模块的第二输入端耦接至第二比较模块的输出端，接收第二比较信号；第一逻辑模块用于将第一比较信号和第二比较信号做逻辑运算并在输出端提供自举电压刷新信号；

其中，若所述第一比较信号具有第一逻辑状态，所述自举电压刷新信号具有第一逻辑状态，所述低侧开关导通；若所述第二比较信号具有第一逻辑状态，所述自举电压刷新信号具有第二逻辑状态，所述低侧开关关断。



5. 根据权利要求 1 所述的自举电压刷新控制电路, 其中, 所述自举电压刷新模块进一步包括:

恒定导通时间电路, 用于设定一个恒定导通时间并提供一个恒定导通时间控制信号, 其中, 所述恒定导通时间控制信号在恒定导通时间以内具有第一逻辑状态, 在恒定导通时间以外具有第二逻辑状态; 以及

第一逻辑模块, 具有第一输入端、第二输入端以及输出端, 其中第一逻辑模块的第一输入端耦接至第一比较模块的输出端, 接收第一比较信号; 第一逻辑模块的第二输入端耦接至恒定导通时间电路的输出端, 接收恒定导通时间控制信号; 第一逻辑模块用于将第一比较信号和恒定导通时间控制信号做逻辑运算并在输出端提供自举电压刷新信号;

其中, 若所述第一比较信号具有第一逻辑状态, 所述自举电压刷新信号具有第一逻辑状态, 低侧开关导通; 若所述恒定导通时间控制信号具有第二逻辑状态, 所述自举电压刷新信号具有第二逻辑状态, 低侧开关关断。

6、根据权利要求 1 所述的自举电压刷新控制电路, 其中, 所述自举电压刷新控制电路进一步包括:

自举欠压闭锁模块, 具有第一输入端、第二输入端和输出端, 其中所述自举欠压闭锁模块的第一输入端用于接收所述自举电压信号; 所述自举欠压闭锁模块的第二输入端用于接收自举电压欠压阈值信号, 且所述自举电压欠压阈值信号小于所述自举电压刷新阈值; 所述自举欠压闭锁模块用于将所述自举电压信号与所述自举电压欠压阈值信号相比较, 并在所述自举欠压闭锁模块的输出端提供自举欠压信号;

其中, 若所述自举电压信号低于所述自举电压欠压阈值信号, 所述自举欠压信号具有第一逻辑状态; 若所述自举电压信号高于所述自举电压欠压阈值信号, 所述自举欠压信号具有第二逻辑状态; 以及

当所述自举欠压信号具有第一逻辑状态时, 所述自举电压刷新控制电路基于该自举欠压信号将所述高侧开关和所述低侧开关关断, 停



止导通与关断切换；当所述自举欠压信号具有第二逻辑状态时，所述自举电压刷新控制电路基于该自举欠压信号允许所述高侧开关和所述低侧开关进行导通和关断切换。

7、根据权利要求 6 所述的自举电压刷新控制电路，其中，所述自举电压刷新控制电路进一步包括：

控制模块，具有第一输入端、第二输入端、第三输入端、第一输出端以及第二输出端；控制模块的第一输入端耦接至所述电压误差放大模块的输出端接收所述误差放大信号；控制模块的第二输入端耦接至自举电压刷新模块接收自举电压刷新信号；控制模块的第三输入端耦接至自举欠压闭锁模块接收自举欠压闭锁信号；控制模块的第一输出端输出高侧开关控制信号控制高侧开关的导通和关断切换；控制模块的第二输出端输出低侧开关控制信号控制低侧开关的导通和关断切换；以及

驱动模块，具有第一输入端、第二输入端、第三输入端、第一输出端以及第二输出端；驱动模块的第一输入端耦接至控制模块的第一输出端接收高侧开关控制信号；驱动模块的第二输入端耦接至控制模块的第二输出端接收低侧开关控制信号；驱动模块的第三输入端耦接至自举电压模块接收自举电压信号；驱动模块的第一输出端输出高侧开关驱动信号驱动高侧开关的导通和关断；驱动模块的第二输出端输出低侧开关驱动信号驱动低侧开关的导通和关断；

8、一种电压转换电路，包括：

开关电路，具有高侧开关和低侧开关，通过高侧开关和低侧开关的导通和关断切换将电压转换电路输入端的输入电压信号转换为其输出端的输出电压信号；

自举电路，包括自举电容，用于为所述高侧开关提供自举电压信号；以及

如权利要求 1~7 所述的自举电压刷新控制电路。

9、一种自举电压刷新控制方法，用于电压转换电路，其中所述电压转换电路包括高侧开关和低侧开关以及用于为所述高侧开关提供自举电压的自举电容，所述电压转换电路基于所述高侧开关和低侧



开关的导通和关断切换将其输入端的输入电压转换为其输出端的输出电压，所述控制电压转换电路的方法包括：

检测所述自举电压；

将所述自举电压与一自举电压刷新阈值相比较，提供第一比较信号；

判定所述自举电压是否小于所述自举电压刷新阈值；

当所述自举电压小于所述自举电压刷新阈值时，采用一个自举电压刷新电路降低所述输出电压；以及

当输出电压降低，所述高侧开关和所述低侧开关开始导通和关断切换，自举电容被充电，自举电压被刷新。

10、根据权利要求 9 所述的自举电压刷新的方法，其中，高侧开关和低侧开关具有公共节点，其中，采用一个自举电压刷新电路降低所述输出电压包括：

当所述自举电压低于所述自举电压刷新阈值，在所述电压转换电路的输出端和/或所述公共节点与地之间连接一个电阻或电流沉。

11、根据权利要求 9 所述的自举电压刷新的方法，其中，采用一个自举电压刷新电路降低所述输出电压包括：

检测流过低侧开关的电流，产生一个电流采样信号；

将所述电流采样信号与一电流阈值信号比较，提供第二比较信号；

根据第一比较信号和第二比较信号提供自举电压刷新信号；以及

基于所述自举电压刷新信号控制所述低侧开关的导通与关断切换以降低输出电压；

其中，若所述自举电压低于所述自举电压刷新阈值，所述自举电压刷新信号具有第一逻辑状态，所述低侧开关导通；

若所述电流采样信号大于所述电流刷新阈值，所述自举电压刷新信号具有第二逻辑状态，所述低侧开关关断。

12、根据权利要求 9 所述的自举电压刷新的方法，其中，采用一个自举电压刷新电路降低所述输出电压包括：

产生一个恒定导通时间控制信号，用于设定一个恒定导通时间；

根据第一比较信号和恒定导通时间控制信号提供自举电压刷新



信号；以及

基于所述自举电压刷新信号控制所述低侧开关的导通与关断切换以降低输出电压；

其中，若所述自举电压低于所述自举电压刷新阈值，所述自举电压刷新信号具有第一逻辑状态，导通所述低侧开关；

当低侧开关导通所述恒定导通时间之后，所述自举电压刷新信号具有第二逻辑状态，关断低侧开关。



说明书

一种自举电压刷新控制电路、电压转换电路及其控制方法

技术领域

本发明的实施例涉及电子电路，尤其涉及电压转换电路、自举电压刷新控制电路及其控制方法。

背景技术

在目前的开关型直流变换电路中，需要高压驱动开关管，因此常用到自举电路以提供所需的驱动电压。

图 1 所示为一电压转换电路 50。如图 1 所示，电压转换电路 50 包括开关电路 51，控制电路 52。开关电路 51 包括高侧开关 11、低侧开关 12，电感器 L、电容器 C 以及负载 R。高侧开关 11 的漏极电连接至电压转换电路 50 的输入端 IN 接收输入电压信号 V_{IN} ；低侧开关 12 的源极电连接至地；高侧开关 11 的源极和低侧开关 12 的漏极耦接形成公共节点 SW；电感 L 电连接于节点 SW 和电压转换电路 50 的输出端 OUT 之间；电容器 C 和负载 R 并联连接于电压转换电路 50 的输出端 OUT 和地之间。

控制电路 52 耦接至电压转换电路 50 的输出端 OUT 接收代表输出电压 V_{OUT} 的反馈信号 FB，控制电路 52 根据输出电压 V_{OUT} 的变化，产生用于导通和关断高侧开关 11 和低侧开关 12 的控制信号 S_H 和 S_L 。在一个实施例中，控制电路 52 包括脉冲宽度调制 (PWM) 电路，PWM



控制电路通过提供不同占空比的方形脉冲信号，进而调节输出电压 V_{OUT} 的大小。在另一个实施例中，控制电路 52 包括脉冲频率调制（PFM）电路，PFM 控制电路通过提供不同频率的方形脉冲信号，进而调节输出电压 V_{OUT} 的大小。

在图 1 所示实施例中，控制电路 52 中还包括驱动电路用于驱动高侧开关 11 和低侧开关 12。在电感器正向储能期间，驱动电路将拉高高侧开关管 11 的栅极电压，在这种情况下，为了使高侧开关 11 能够充分导通（即：高侧开关 11 工作在饱和区，这样高侧开关 11 的导通电阻很小），高侧开关 11 的栅极与其耦接至节点 SW 的一端之间的电压差应该足够大，至少需要大于高侧开关 11 的导通阈值电压。然而，若高侧开关 11 导通，节点 SW 的电压可以是输入电压 V_{IN} ，这时，需要为高侧开关 11 的栅极提供高于节点 SW 的电压（即高于输入电压 V_{IN} ）的电压才能使高侧开关 11 充分导通。

为了在电压转换电路 50 中获得高于输入电压 V_{IN} 的电压，因此，通常电压转换电路 50 中还包括自举电路 53，用于以节点 SW 的电压为参考电势产生自举电压 V_{BST} ，该自举电压 V_{BST} 可以用于提升/增强驱动电路驱动的驱动能力，从而更好地控制高侧开关 11 的导通和关断。

在图 1 所示实施例中，自举电路 53 包括二极管 D_B 和自举电容 C_B ，串联耦接于自举供电输入端和节点 SW 之间，其中二极管 D_B 的阳极耦接自举供电输入端接收自举供电电压 V_B ，二极管 D_B 的阴极耦接自举电容 C_B 的第一端，自举电容 C_B 的第二端耦接节点 SW。自举



电路 53 的工作原理是本领域的普通技术人员所熟知的，即，当高侧开关 11 关断时，低侧开关 12 导通，节点 SW 的电压为零，自举供电电压 V_B 通过二极管 D_B 为自举电容 C_B 充电，使得自举电容 C_B 第一端和第二端之间具有自举电压 V_{BST} ；当高侧开关 11 导通时，低侧开关 12 关断，节点 SW 处的电压为 V_{IN} ，此时节点 BST 的电压被抬升为输入电压 V_{IN} 叠加上自举电压 V_{BST} ，从而实现了在降压型直流电压转换电路 50 中获得高于输入电压 V_{IN} 的电压的目的。同时，二极管 D_B 反向偏置而被关断，从而可以保护提供自举供电电压的电源不受相对较高的输入电压 V_{IN} 的损坏。

可见，自举电路 53 通过在低侧开关 12 导通时将自举电容 C_B 第二端的电压拉低至参考地，而获得为自举电容 C_B 充电的机会，以提供自举电压 V_{BST} 。然而在某些工作状态下，由于自举电容 C_B 上的电荷不足而又不能及时被充电到足够的水平，而导致自举电路 53 提供的自举电压 V_{BST} 下降，不足以使高侧开关 11 正常导通和关断，因此电压转换电路 50 不能正常工作；又或自举电压 V_{BST} 下降到电路预设的低压闭锁值，使得整个变换器被锁定，电路也因此不能正常工作。

例如，当输出电压 V_{OUT} 接近输入电压 V_{IN} ，此时需要高侧开关 11 以很高、甚至 100% 的占空比工作（导通时间延长或切换频率增大），低侧开关 12 导通时间非常短、甚至没有导通机会，因此自举电容 C_B 不能及时充电到相关水平。

又如，在轻载或空载条件下，控制电路 52 会降低高侧开关 11 和低侧开关 12 的导通时间和/或者切换频率，甚至同时关断高侧开关 11



和低侧开关 12 以提高转换效率,这样可能由于低侧开关 12 在较长时间内没有进行导通或导通时间很短而无法使自举电容 C_B 被及时充电,以使自举电压 V_{BST} 被刷新恢复至期望值。

这些均会导致自举电路 53 提供的自举电压 V_{BST} 下降,不足以使高侧开关 11 正常导通和关断,那么电压转换电路 50 也因此不能正常工作。这样要等到多个周期之后输出电压 V_{OUT} 自然掉落,自举电容 C_B 才有机会被充电以使自举电压 V_{BST} 恢复。在此过程中,输出电压 V_{OUT} 会出现较大的波动尖峰,这不仅对电压转换电路 50 不利,更有可能损害负载,因而不希望出现的。

发明内容

针对现有技术中的一个或多个问题,提出了一种自举电压刷新控制电路、电压转换电路及其控制方法。

本发明一方面提供了一种自举电压刷新控制电路,用于电压转换电路,其中所述电压转换电路包括高侧开关和低侧开关以及用于为所述高侧开关提供自举电压信号的自举电容,所述电压转换电路基于所述高侧开关和低侧开关的导通和关断切换将其输入端的输入电压转换为其输出端的输出电压。所述自举电压刷新控制电路包括:自举电压刷新模块,所述自举电压刷新模块包括第一比较模块,所述第一比较模块具有第一输入端、第二输入端和输出端,其中第一比较模块的第一输入端用于接收所述自举电压信号;第一比较模块的第二输入端用于接收一自举电压刷新阈值;第一比较模块用于将所述自举电压信号与所述自举电压刷新阈值进行比较并在第一比较模块的输出端提



供第一比较信号；其中，若所述自举电压信号低于所述自举电压刷新阈值，所述第一比较信号具有第一逻辑状态；若所述自举电压信号高于所述自举电压刷新阈值，所述第一比较信号具有第二逻辑状态。所述自举电压刷新控制电路进一步包括电压差值模块，具有第一输入端、第二输入端和输出端，所述电压差值模块的第一输入端接收代表所述输出电压的反馈信号；所述电压差值模块的第二输入端接收参考信号；所述电压差值模块对所述反馈信号和所述参考信号进行比较，并在其输出端输出差值信号。其中，当所述第一比较信号具有第一逻辑状态时，所述自举电压刷新模块用于降低所述输出电压，当所述反馈信号小于所述参考信号时，所述自举电压刷新控制电路根据所述差值信号控制所述高侧开关和所述低侧开关开始导通和关断切换，所述自举电容被充电，所述自举电压被刷新。

本发明另一方面提供了一种电压转换电路，包括：开关电路，具有高侧开关和低侧开关，通过高侧开关和低侧开关的导通和关断切换将电压转换电路输入端的输入电压信号转换为其输出端的输出电压信号；自举电路，包括自举电容，用于为所述高侧开关提供自举电压信号；以及自举电压刷新控制电路。

本发明进一步提供了一种自举电压刷新控制方法，该方法用于电压转换电路，其中所述电压转换电路包括高侧开关和低侧开关以及用于为所述高侧开关提供自举电压的自举电容，所述电压转换电路基于所述高侧开关和低侧开关的导通和关断切换将其输入端的输入电压转换为其输出端的输出电压。所述控制电压转换电路的方法包括：检



测所述自举电压；将所述自举电压与一自举电压刷新阈值相比较，提供第一比较信号；判定所述自举电压是否小于所述自举电压刷新阈值；当所述自举电压小于所述自举电压刷新阈值时，采用一个自举电压刷新电路降低所述输出电压；以及当输出电压降低，所述高侧开关和所述低侧开关开始导通和关断切换，自举电容被充电，自举电压被刷新。根据上述方面的实施例，本申请提出的自举电压刷新控制电路在不影响电路正常的控制方式和开关时序的情况下刷新自举电压，简化了电路逻辑的设计。

附图说明

在所有附图中，相同的标号表示具有相同、相似或相应的特征或功能。

图 1 示出了一种典型的电压转换电路 50 的简化示意图。

图 2 示出了根据本发明一实施例的电压转换电路 100 的示意图。

图 3 示出了根据本发明另一实施例的电压转换电路 200 的示意图。

图 4 示出了根据本发明又一实施例的电压转换电路 300 的示意图。

图 5 示出了根据本发明一个实施例的电压转换电路的工作波形示意图。

图 6 示出了根据本发明一个实施例的控制电压转换电路的方法的流程示意图。

具体实施方式

下面将详细描述本公开的具体实施例，应当注意，这里描述的实



施例只用于举例说明，并不用于限制本公开。相反，本公开意在涵盖由所附权利要求所界定的本公开精神和范围内所定义的各种备选方案、修改方案和等同方案。在以下描述中，为了提供对本公开的透彻理解，阐述了大量特定细节。然而，对于本领域普通技术人员应当理解，没有这些具体细节，本公开同样可以实施。在其他一些实施例中，为了便于凸显本公开的主旨，对于众所周知的方案、流程、元器件以及电路或方法未作详细的描述。

图 2 所示为根据本发明一个实施例的电压转换电路 100 的示意图。如图 2 所示，电压转换电路 100 包括开关电路 110、自举电路 120 以及控制电路。

开关电路 110 包括高侧开关 11、低侧开关 12，电感器 L 、电容器 C 以及负载 R 。高侧开关 11 的漏极电连接至电压转换电路 100 的输入端 IN 接收输入电压 V_{IN} ；低侧开关 12 的源极电连接至地；高侧开关 11 的源极和低侧开关 12 的漏极耦接形成公共节点 SW ；电感 L 电连接于节点 SW 和电压转换电路 100 的输出端 OUT 之间；电容器 C 和负载 R 并联连接于电压转换电路 100 的输出端 OUT 和地之间。在图 2 所示实施例中，开关电路 110 包括一个降压型 **BUCK** 拓扑结构。在其他实施例中，开关电路 110 可以采用升压电路拓扑、升降压电路拓扑、反激电路拓扑等其他直流/直流拓扑结构。在图 2 示实施例中，高侧开关 11 和低侧开关 12 示意为金属氧化物半导体场效应晶体管（**MOSFET**），但应该理解，高侧开关 11 和低侧开关 12 不局限于 **MOSFET**，在其他实施例中，高侧开关 11 和低侧开关 12 还可以是



其他任何可控的半导体开关器件，如结型场效应晶体管（JFET）或绝缘栅双极晶体管（IGBT）。

自举电路 120 包括二极管 D_B 和自举电容 C_B ，串联耦接于自举供电输入端和节点 SW 之间，其中二极管 D_B 的阳极耦接自举供电输入端接收自举供电电压 V_B ，二极管 D_B 的阴极耦接自举电容 C_B 的第一端，自举电容 C_B 的第二端耦接节点 SW。当高侧开关 11 关断时，低侧开关 12 导通，节点 SW 的电压为零，自举供电电压 V_B 通过二极管 D_B 为自举电容 C_B 充电，使得自举电容 C_B 第一端和第二端之间具有自举电压 V_{BST} ；当高侧开关 11 导通时，低侧开关 12 关断，节点 SW 处的电压为 V_{IN} ，此时节点 BST 的电压被抬升为输入电压 V_{IN} 叠加上自举电压 V_{BST} ，从而实现了在降压型直流电压转换电路 100 中获得高于输入电压 V_{IN} 的电压的目的。同时，二极管 D_B 反向偏置而被关断，从而可以保护提供自举供电电压的电源不受相对较高的输入电压 V_{IN} 的损坏。

在一个实施例中，控制电路包括电压差值模块 137。电压差值模块 137 具有第一输入端、第二输入端和输出端。电压差值模块 137 的第一输入端耦接至电压转换电路 100 的输出端 OUT 接收输出电压 V_{OUT} 的反馈信号 FB；电压差值模块 137 的第二输入端接收参考电压信号 V_{REF} ；电压差值模块 137 将输出电压反馈信号 FB 和参考电压信号 V_{REF} 进行比较，并在其输出端输出差值信号 EA。在一个实施例中，例如电压控制、电流控制等 PWM 控制方法实施例中，电压差值模块 137 包括一个误差放大器，用于将输出电压反馈信号 FB 和参考电压



信号 V_{REF} 比较后的差值放大，再将该差值放大信号和一个斜坡信号进行比较，进而控制高侧开关 11 和低侧开关 12 的导通和关断切换。在另一个实施例中，例如恒定导通时间控制等 PFM 控制方法实施例中，电压差值模块 137 包括一个电压比较器，用于将输出电压反馈信号 FB 和参考电压信号 V_{REF} 比较，根据比较结果控制高侧开关 11 和低侧开关 12 的导通和关断切换。比如，当输出电压反馈信号 FB 小于参考电压信号 V_{REF} 时高侧开关 11 导通，低侧开关 12 关断；当输出电压反馈信号 FB 大于参考电压信号 V_{REF} 时高侧开关 11 关断，低侧开关 12 导通。

在一个实施例中，控制电路进一步包括控制模块 131。控制模块 131 耦接至电压差值模块 137 的输出端接收差值信号 EA，并根据差值信号 EA 判定输出端的负载情况进而输出高侧开关控制信号 S_H 和低侧开关控制信号 S_L 用于控制高侧开关 11 和低侧开关 12 的导通和关断切换。

在一个实施例中，控制电路进一步包括驱动模块 132。驱动模块 132 包括第一驱动器 31 和第二驱动器 32。第一驱动器 31 具有输入端和输出端，第一驱动器 31 的输入端接收高侧开关控制信号 S_H ，并在其输出端输出高侧开关驱动信号 D_H 至高侧开关 11 的栅极，以驱动高侧开关 11 的导通和关断。第一驱动器 31 包括接收自举电压 V_{BST} ，用于提升/增强第一驱动器 31 提供的高侧开关驱动信号 D_H 的驱动能力，从而更好地控制高侧开关 11 的导通和关断。第二驱动器 32 具有输入端和输出端，第二驱动器 32 的输入端接收低侧开关控制信号 S_L ，并



在其输出端输出低侧开关驱动信号 D_L 至低侧开关的栅极，以驱动低侧开关 12 的导通和关断。根据本发明的一个实施例，所述第一驱动器 31 包括一个或多个反相器，所述自举电压信号 V_{BST} 用作所述一个或多个反相器的供电电源。类似地，所述第二驱动器 32 也可以包括一个或多个反相器。

在一个实施例中，控制电路进一步包括自举电压刷新模块 133。自举电压刷新模块 133 接收自举电压信号 V_{BST} ，并将自举电压信号 V_{BST} 与一个自举电压刷新阈值进行比较。在轻载或空载模式下，高侧开关 11 和低侧开关 12 均关断，流过电感 L 的电感电流为零。与此同时，自举电压 V_{BST} 逐渐降低，当自举电压信号 V_{BST} 小于自举电压刷新阈值时，自举电压刷新模块 133 启用，用于降低输出电压 V_{OUT} 。电压差值模块 137 将代表输出电压 V_{OUT} 的反馈电压 FB 和参考电压信号 V_{REF} 比较，当反馈信号 FB 小于所述参考电压信号 V_{REF} 时，控制模块 131 根据差值信号 EA 控制高侧开关 11 和低侧开关 12 开始导通和关断切换，以使输出电压 V_{OUT} 维持在预设值。即高侧开关 11 和低侧开关 12 从均关断的轻载或空载状态转换为导通和关断切换的正常状态。当高侧开关 11 和低侧开关 12 的切换频率变高，则低侧开关 12 的导通时间增加，自举电容 C_B 可及时被充电，自举电压 V_{BST} 被刷新恢复至期望值。采用自举电压刷新模块 133 降低输出电压 V_{OUT} ，进而增大高侧开关 11 和低侧开关 12 的切换频率以刷新自举电压 V_{BST} ，可以避免使用消隐电路消隐高侧开关 11，同时不影响电压转换电路的控制方式和开关时序，即该实施例通过高侧开关 11 和低侧开关 12



的正常切换就能刷新自举电压 V_{BST} 。

在一个实施例中，自举电压刷新模块 133 包括输入端和输出端，自举电压刷新模块 133 的输入端接收自举电压信号 V_{BST} ，自举电压刷新模块 133 的输出端耦接至开关电路 110 的节点 SW，用于降低输出电压 V_{OUT} 。在另一个实施例中，自举电压刷新模块 133 的输出端耦接至电压变换电路 100 的输出端 OUT，用于降低输出电压 V_{OUT} 。在又一个实施例中，自举电压刷新模块 133 的输出端可以同时耦接至开关电路 110 的节点 SW 处和电压转换电路 100 的输出端 OUT，以加快降低输出电压 V_{OUT} 。

在一个实施例中，自举电压刷新模块 133 包括比较电路 33，比较电路 33 具有第一输入端、第二输入端和输出端。比较电路 33 的第一输入端用于接收自举电压信号 V_{BST} ，比较电路 33 的第二输入端用于接收自举电压刷新阈值 V_{TH1} 。比较电路 33 用于将自举电压信号 V_{BST} 与自举电压刷新阈值 V_{TH1} 相比较，并在所述比较电路 33 的输出端提供第一比较信号 A_S 。若自举电压信号 V_{BST} 低于自举电压刷新阈值信号 V_{TH1} ，则第一比较信号 A_S 具有第一逻辑状态（比如高电平逻辑状态）；若自举电压信号 V_{BST} 高于自举电压刷新阈值信号 V_{TH1} ，则第一比较信号 A_S 具有第二逻辑状态（比如低电平逻辑状态）。

在一个实施例中，自举电压刷新模块 133 还包括开关 S1 和电阻 R1。开关 S1 具有第一端、第二端和控制端。开关 S1 的第一端耦接于电阻 R1 的一端，开关 S1 的第二端作为自举电压刷新模块 133 的输出端提供自举电压刷新信号 RFS，开关 S1 的控制端耦接比较电路



33 的输出端接收第一比较信号 A_S 。电阻 R_1 的另一端电连接至逻辑地。若第一比较信号 A_S 具有第一逻辑状态，开关 S_1 导通，电容器 C 通过开关 S_1 和电阻 R_1 放电，输出电压 V_{OUT} 降低。在另一个实施例中，电阻 R_1 也可以用一个电流沉代替。

在一个实施例中，控制电路包括自举欠压闭锁模块 135。自举欠压闭锁电路 135 具有第一闭锁输入端、第二闭锁输入端和闭锁输出端。该第一闭锁输入端用于接收自举电压信号 V_{BST} ，该第二闭锁输入端用于接收自举电压欠压阈值信号 V_{UVLO} 。自举欠压闭锁电路 135 用于将自举电压信号 V_{BST} 与自举电压欠压阈值信号 V_{UVLO} 相比较，并在所述闭锁电路 135 的输出端提供自举欠压信号 $LOCK$ 至控制模块 131。若自举电压信号 V_{BST} 低于自举电压欠压阈值信号 V_{UVLO} ，则自举欠压信号 $LOCK$ 具有第一逻辑状态（比如高电平逻辑状态）。这时控制模块 131 控制高侧开关 11 和低侧开关 12 同时关断，停止导通与关断切换。若自举电压信号 V_{BST} 高于自举电压欠压阈值信号 V_{UVLO} ，则自举欠压信号 $LOCK$ 具有第二逻辑状态（比如低电平逻辑状态），这时控制模块 131 控制高侧开关 11 和低侧开关 12 进行导通和关断切换。根据本发明的一个实施例，所述自举电压欠压阈值信号 V_{UVLO} 小于所述自举电压刷新阈值 V_{TH1} 。自举欠压闭锁电路 135 有助于在自举电压信号 V_{BST} 已经低于自举电压欠压阈值信号 V_{UVLO} ，而且未能及时被刷新（即，自举电容 C_B 未能被及时充电使该自举电压信号 V_{BST} 恢复至高于该自举电压欠压阈值信号 V_{UVLO} ）时，将高侧开关 11 和低侧开关 12 均关断，以改善电压转换电路 100 的工作安全性能。



图 3 所示为根据本发明一个实施例的电压转换电路 200 的示意图。如图 3 所示，电压转换电路 200 包括开关电路 110、驱动电路 120 以及控制电路。为了简便且便于理解，电压转换电路 200 中那些功能上和电压转换电路 100 中相同的、同样的或类似的组件或结构沿用了相同的附图标记。同时，在图 3 所示实施例中，对于开关电路 110 中的高侧开关 11 和低侧开关 12，示出了其体二极管。具体的来说，示出了高侧开关 11 的体二极管 D1 和低侧开关 12 的体二极管 D2。此外，在图 3 所示实施例中，高侧开关 11 和低侧开关 12 被示意为金属氧化物半导体场效应晶体管（MOSFET），但应该理解，高侧开关 11 和低侧开关 12 不局限于 MOSFET，在其他实施例中，高侧开关 11 和低侧开关 12 还可以是其他任何可控的半导体开关器件，如结型场效应晶体管（JFET）或绝缘栅双极晶体管（IGBT）。

在一个实施例中，电压转换电路 200 中控制电路包括：控制模块 131、驱动模块 132、电压差值模块 137、自举电压刷新模块 134 以及自举欠压闭锁模块 135。为了简便且便于理解，电压转换电路 200 的控制电路中那些功能上和电压转换电路 100 的控制电路中相同的、同样的或类似的组件或结构沿用了相同的附图标记的模块的功能不再累述。

自举电压刷新模块 134 包括第一输入端和输出端。自举电压刷新模块 134 的第一输入端耦接至自举电路 120 接收自举电压信号 V_{BST} ，并将自举电压信号 V_{BST} 与一个自举电压刷新阈值进行比较。在轻载或空载模式下，高侧开关 11 和低侧开关 12 均关断，流过电感 L 的电



感电流为零。与此同时，自举电压 V_{BST} 逐渐降低，当自举电压信号 V_{BST} 小于自举电压刷新阈值时，自举电压刷新模块 134 启动用于降低输出电压 V_{OUT} 。电压差值模块 137 将代表输出电压 V_{OUT} 的反馈电压 FB 和参考电压信号 V_{REF} 比较，当反馈信号 FB 小于所述参考电压信号 V_{REF} 时，控制模块 131 根据差值信号 EA 控制高侧开关 11 和低侧开关 12 开始导通和关断切换，以使输出电压 V_{OUT} 维持在预设值。当高侧开关 11 和低侧开关 12 的切换频率变高，则低侧开关 12 的导通时间增加，自举电容 C_B 可及时被充电，自举电压 V_{BST} 被刷新恢复至期望值。采用自举电压刷新模块 134 降低输出电压 V_{OUT} ，进而增大高侧开关 11 和低侧开关 12 的切换频率以刷新自举电压 V_{BST} ，可以避免使用消隐电路消隐高侧开关 11，同时不影响电压转换电路的控制方式和开关时序，即该实施例通过高侧开关 11 和低侧开关 12 的正常切换就能刷新自举电压 V_{BST} 。

在一个实施例中，自举电压刷新模块 134 还包括第二输入端耦接至低侧开关 12 的漏极，接收一个表征流过低侧开关 12 的反向电流的采样信号 V_{CS} ；自举电压刷新模块 134 的输出端提供一自举电压刷新信号 RFS 。

在一个实施例中，若自举电压信号 V_{BST} 低于自举电压刷新阈值 V_{TH1} ，自举电压刷新信号 RFS 具有第一逻辑状态(比如逻辑高状态)，控制电路 131 控制低侧开关管 12 导通，电容器 C 通过电感器 L 和低侧开关 12 放电，流过低侧开关 12 的反向电流增大，输出电压 V_{OUT} 降低，与此同时，自举电容 C_B 也通过低侧开关 12 被充电。当电流采



样信号 V_{CS} 增大到一个预设电流阈值 V_P 后, 自举电压刷新信号 RFS 具有第二逻辑状态 (比如逻辑低状态), 控制电路 131 控制低侧开关管 12 关断, 自举电容 C_B 停止充电。此时, 流过电感器 L 的电流通过高侧开关 11 的体二极管 $D1$ 续流, 此时开关电路 110 变为一个 BOOST 升压变换器, 电容器 C 释放的能量将被存储在电压变换电路 200 的输入端 IN 。在一个实施例中, 电流阈值信号 V_P 越大, 自举电压信号 V_{BST} 恢复的值越大。但是从总体上来说, 自举电压刷新模块 134 主要用于降低输出电压 V_{OUT} , 因此电流阈值信号 V_P 的值不会太大, 低侧开关 12 导通的时间较短, 因此自举电压 V_{BST} 恢复的值有限。一旦输出电压 V_{OUT} 降低, 控制模块 131 将根据差值信号 EA 控制高侧开关 11 和低侧开关 12 开始导通和关断切换, 自举电压 V_{BST} 将被刷新恢复至期望值。

在一个实施例中, 自举电压刷新模块 134 包括第一比较器 34。第一比较器 34 具有第一输入端、第二输入端和输出端。第一比较器 34 的第一输入端用于接收自举电压刷新阈值 V_{TH1} , 第一比较器 34 的第二输入端用于接收自举电压信号 V_{BST} 。第一比较器 34 用于将自举电压信号 V_{BST} 与自举电压刷新阈值 V_{TH1} 相比较, 并在第一比较器 34 的输出端提供第一比较信号 A_S 。在一个实施例中, 若自举电压信号 V_{BST} 低于自举电压刷新阈值 V_{TH1} , 则第一比较信号 A_S 具有第一逻辑状态 (比如高电平逻辑状态); 若自举电压信号 V_{BST} 高于自举电压刷新阈值 V_{TH1} , 则第一比较信号 A_S 具有第二逻辑状态 (比如低电平逻辑状态)。



在一个实施例中，自举电压刷新模块 134 进一步包括第二比较器 35。第二比较器 35 具有第一输入端、第二输入端和输出端。第二比较器 35 的第一输入端用于接收电流阈值信号 V_P ，第二比较器 35 的第二输入端用于接收采样电压信号 V_{CS} 。第二比较器 35 用于将采样电压信号 V_{CS} 与电流阈值信号 V_P 相比较，并在第二比较器 35 的输出端提供自第二比较信号 A_R 。在一个实施例中，若采样电压信号 V_{CS} 高于电流阈值信号 V_P ，则第二比较信号 A_R 具有第一逻辑状态（比如高电平逻辑状态）；若采样电压信号 V_{CS} 低于电流阈值信号 V_P ，则第二比较信号 A_R 具有第二逻辑状态（比如低电平逻辑状态）。在一个实施例中，电流阈值信号 V_P 的选择可根据所需恢复的自举电压信号 V_{BST} 的值选择，电流阈值信号 V_P 越大，所提供的自举电压信号 V_{BST} 的值越大。

在一个实施例中，自举电压刷新模块 134 进一步包括逻辑电路 36。逻辑电路 36 具有第一输入端、第二输入端和输出端。逻辑电路 36 的第一输入端耦接至第一比较器 34 的输出端接收第一比较信号 A_S ，逻辑电路 36 的第二输入端耦接至第二比较器的输出端接收第二比较信号 A_R 。逻辑电路 36 对第一比较信号 A_S 和第二比较信号 A_R 进行逻辑运算，并在其输出端提供一个自举电压刷新信号 RFS 。当第一比较信号 A_S 具有第一逻辑状态时，自举电压刷新信号 RFS 具有第一逻辑状态；当第二比较信号 A_R 具有第一逻辑状态时，自举电压刷新信号 RFS 具有第二逻辑状态。在一个实施例中，当自举电压刷新信号 RFS 为第一逻辑状态时，低侧开关管 12 导通，开关电路 110 中的



电容器 C 通过电感器 L 和低侧开关 12 放电，电感器 L 反向储能，自举电容 C_B 被充电；当自举电压刷新信号 RFS 为第二逻辑状态时，低侧开关 12 关断，自举电容 C_B 停止被充电；流过电感器 L 的电流通过高侧开关 11 的体二极管 $D1$ 续流。

在一个实施例中，控制模块 131 耦接至电压差值模块 137 的输出端，接收差值信号 EA ，并根据差值信号 EA 的变化提供高侧开关控制信号 S_H 和第一低侧开关控制信号 S_{L1} 。高侧开关控制信号 S_H 和第一低侧开关控制信号 S_{L1} 用于控制高侧开关 11 和低侧开关 12 的导通和关断切换。在一个实施例中，当第一低侧开关控制信号 S_{L1} 具有第一逻辑状态（例如逻辑高状态），低侧开关 12 导通；当第一低侧开关控制信号 S_{L1} 具有第二逻辑状态（例如逻辑低状态），低侧开关 12 关断。在一个实施例中，控制模块 131 还包括一个逻辑模块 30。逻辑模块 30 具有第一输入端、第二输入端和输出端。逻辑模块 30 的第一输入端接收第一低侧开关控制信号 S_{L1} ；逻辑模块 30 的第二输入端接收自举电压刷新信号 RFS ；逻辑模块 30 对第一低侧开关控制信号 S_{L1} 和自举电压刷新信号 RFS 做逻辑运算，并在其输出端输出低侧开关控制信号 S_L 。当第一低侧开关控制信号 S_{L1} 和自举电压刷新信号 RFS 任意一个具有第一逻辑状态（例如逻辑高状态），则低侧开关控制信号 S_L 具有第一逻辑状态（例如逻辑高状态），低侧开关 12 导通。在一个实施例中，逻辑模块 30 为一个逻辑或门。

图 4 所示为根据本发明一个实施例的电压转换电路 300 的示意图。在图 4 所示一个实施例中，电压转换电路 300 中控制电路包括：控制



模块 131、驱动模块 132、电压差值模块 137、自举电压刷新模块 136 以及自举欠压闭锁模块 135。为了简便且便于理解，电压转换电路 300 中那些功能上和电压转换电路 200、100 中相同的、同样的或类似的组件或结构沿用了相同的附图标记，同时，不再累述与电压转换电路 200、100 中相同的功能模块。

在一个实施例中，自举电压刷新模块 136 包括第一比较器 34。第一比较器 34 具有第一输入端、第二输入端和输出端。第一比较器 34 的第一输入端用于接收自举电压刷新阈值 V_{TH1} ，第一比较器 34 的第二输入端用于接收自举电压信号 V_{BST} 。第一比较器 34 用于将自举电压信号 V_{BST} 与自举电压刷新阈值 V_{TH1} 相比较，并在第一比较器 34 的输出端提供第一比较信号 A_S 。在一个实施例中，若自举电压信号 V_{BST} 低于自举电压刷新阈值 V_{TH1} ，则第一比较信号 A_S 具有第一逻辑状态（比如高电平逻辑状态）；若自举电压信号 V_{BST} 高于自举电压刷新阈值 V_{TH1} ，则第一比较信号 A_S 具有第二逻辑状态（比如低电平逻辑状态）。

在一个实施例中，自举电压刷新模块 136 进一步包括一个恒定时间导通电路 37。恒定导通时间电路 37 用于设定一个低侧开关的导通时间，并输出一个恒定时间控制信号 C_R 。在一个实施例中，恒定时间控制信号 C_R 包括高低电平信号，具有第一逻辑状态和第二逻辑状态。其中，恒定导通时间控制信号 C_R 在恒定导通时间以内具有第一逻辑状态，在恒定导通时间以外具有第二逻辑状态。

在一个实施例中，自举电压刷新模块 136 进一步包括逻辑电路



36。逻辑电路 36 具有第一输入端、第二输入端和输出端。逻辑电路 36 的第一输入端耦接至第一比较器 34 的输出端接收第一比较信号 A_S ，逻辑电路 36 的第二输入端耦接至第二比较器的输出端接收恒定时间控制信号 C_R 。逻辑电路 36 对第一比较信号 A_S 和恒定时间控制信号 C_R 进行逻辑运算，并在其输出端提供一个自举电压刷新信号 RFS 。当第一比较信号 A_S 具有第一逻辑状态时，自举电压刷新信号 RFS 具有第一逻辑状态；当恒定时间控制信号 C_R 具有第二逻辑状态时，自举电压刷新信号 RFS 具有第二逻辑状态。

在一个实施例中，当自举电压刷新信号 RFS 为第一逻辑状态时，低侧开关管 12 导通，开关电路 110 中的电容器 C 通过电感器 L 和低侧开关 12 放电，电感器 L 反向储能，流过低侧开关 12 的反向电流增大，输出电压 V_{OUT} 降低，与此同时，自举电容 C_B 也将被充电。当自举电压刷新信号 RFS 为第二逻辑状态时，低侧开关 12 关断，自举电容 C_B 停止被充电。此时，流过电感器 L 的电流通过高侧开关 11 的体二极管 $D1$ 续流，开关电路 110 变为一个 **BOOST** 升压变换器，电容器 C 释放的能量将被存储在电压变换电路 200 的输入端 IN 。在一个实施例中，恒定导通时间电路 37 设定的导通时间越长，自举电压信号 V_{BST} 恢复的值越大。但是从总体上来说，自举电压刷新电路 136 主要用于降低输出电压 V_{OUT} ，因此恒定导通时间电路 37 设定的导通时间不会太长，低侧开关 12 导通的时间较短，因此自举电压 V_{BST} 恢复的值有限。一旦输出电压 V_{OUT} 降低，控制模块 131 将根据差值信号 EA 控制高侧开关 11 和低侧开关 12 开始导通和关断切换，自举电



压 V_{BST} 将被刷新恢复至期望值。

图 5 所示为根据本发明一个实施例的电压转换电路 200 的工作波形示意图。在 t_0 时刻，高侧开关控制信号 S_H 和低侧开关控制信号 S_L 为低电平，高侧开关 11 和低侧开关 12 均关断。此时，电压转换电路 300 的输出电压 V_{OUT} 保持不变，流过开关电路 110 中的电感器 L 的电流 I_L 为零。

在 t_0 至 t_1 时刻，高侧开关控制信号 S_H 和低侧开关控制信号 S_L 保持为低电平，因此高侧开关 11 和低侧开关 12 保持关断状态，流过电感器 L 的电流 I_L 依然为零。由于电压转换电路 300 工作在轻载模式下，因此输出电压 V_{OUT} 基本保持不变。同时，由于低侧开关 12 一直保持关断状态，自举电路 120 中的自举电容 C_B 不能及时被充电，自举电压 V_{BST} 下降。

在 t_1 时刻，当自举电压 V_{BST} 下降至自举电压刷新阈值 V_{TH1} 时，自举电压刷新电路 134 中的第一比较信号 A_S 为高电平信号，自举刷新信号 RFS 为高电平，因此，控制模块 131 控制低侧开关控制信号 S_L 变为高电平，低侧开关 12 导通。

在 t_1 至 t_2 时刻，低侧开关控制信号 S_L 维持在高电平，低侧开关 12 保持导通状态。开关电路 110 中的电容器 C 通过电感器 L 和低侧开关 12 放电，流过电感器 L 的电流 I_L 为一反向升高的电流信号；输出电压 V_{OUT} 随着电容器 C 的放电而降低。与此同时，自举电路 120 中的自举电容 C_B 通过低侧开关 12 电连接至逻辑地，因此自举电容 C_B 被充电，自举电压 V_{BST} 升高。



在 t_2 时刻, 电感电流 I_L 反向增大到第一电流阈值 I_{p1} , 也即是, 在一个实施例中, 自举电压刷新电路 134 中的第二比较器 35 中的电流采样信号 V_{CS} 等于电流阈值信号 V_P (电流阈值信号 V_P 代表第一电流阈值信号 I_{p1}); 第二比较信号 A_R 为高电平, 自举刷新信号 RFS 变为低电平。由于此时第一低侧开关信号 S_{L1} 依然为低电平信号, 因此低侧开关控制信号 S_L 为低电平, 低侧开关 12 关断。此刻, 自举电压 V_{BST} 被充电恢复至第一自举电压值 V_{BST1} 。在其他实施例中, 也可以设定不同的电流阈值信号, 对应地自举电压 V_{BST} 被充电恢复至不同的值。当然, 在图 4 所示的实施例电压转换电路 300 中, 通过设定低侧开关 12 不同的导通时间也可以达到相同的效果。

在 t_2 至 t_3 时刻, 高侧开关 11 和低侧开关 12 均保持关断状态; 电感电流 I_L 通过高侧开关 11 的体二极管 $D1$ 续流, 反向减小; 输出电压 V_{OUT} 继续降低。

在 t_3 时刻, 电感电流 I_L 减小到零, 输出电压 V_{OUT} 基本保持不变。

t_1' 至 t_3' 时刻以及 t_1'' 至 t_3'' 时刻重复 t_1 至 t_3 时刻, 输出电压 V_{OUT} 持续下降。在 t_3'' 时刻, 由于输出电压 V_{OUT} 下降到一定的限值, 开关变换器进入正常工作模式, 高侧开关 11 和低侧开关 12 开始正常的导通和关断切换。此刻, 高侧开关控制信号 S_H 变为高电平, 高侧开关 11 导通。需要说明的是, 在图示实施例中, 为了降低输出电压 V_{OUT} , 低侧开关 12 被导通和关断了三次, 即 t_1 至 t_3 、 t_1' 至 t_3' 、 t_1'' 至 t_3'' 。然而本领域技术人员应该理解, 三次只是示意性地, 在其他实施例中, 可以根据输出电压 V_{OUT} 下降限值的不同, 选择任意导通和关断的次



数。

在 t_3 至 t_4 时刻, 高侧开关控制信号 S_H 保持高电平, 高侧开关 11 保持导通状态, 电感器 L 正向储能, 电感电流 I_L 正向增大, 输出电压 V_{OUT} 升高。与此同时, 自举电压 V_{BST} 继续下降。

在 t_4 时刻, 高侧开关控制信号 S_H 变为低电平, 高侧开关 11 关断; 低侧开关控制信号 S_L 变为高电平, 低侧开关 12 导通。电感电流 I_L 增大到其峰值。

在 t_4 至 t_5 时刻, 高侧开关控制信号 S_H 保持低电平, 高侧开关 11 保持关断状态; 低侧开关控制信号 S_L 保持高电平, 低侧开关 12 保持导通状态; 电感电流 I_L 通过低侧开关 12 续流, 线性下降。自举电容 C_B 通过低侧开关 12 电连接至逻辑地, 因此自举电容 C_B 被充电, 自举电压 V_{BST} 升高。

在 t_5 时刻, 低侧开关控制信号 S_L 变为低电平, 低侧开关 12 关断, 电感电流 I_L 线性下降至 0。自举电压 V_{BST} 恢复至预定值。

图 6 示出了根据本发明一个实施例的控制电压转换电路的方法的流程示意图。如图 6 所示, 控制电压转换电路的方法包括步骤 601-步骤 607。

步骤 601, 检测电压转换电路 (例如 100、200 或 300) 的自举电压, 产生一个自举电压信号 V_{BST} ;

步骤 602, 将自举电压信号 V_{BST} 与一自举电压刷新阈值 V_{TH1} 相比较, 并提供第一比较信号 A_S ;

步骤 603, 判定自举电压 V_{BST} 是否小于自举电压刷新阈值 V_{TH1} ,



如果自举电压 V_{BST} 大于自举电压刷新阈值 V_{TH1} ，则返回步骤 602，

如果自举电压 V_{BST} 小于自举电压刷新阈值 V_{TH1} ，则转至步骤 604；

步骤 604，如果自举电压 V_{BST} 小于自举电压刷新阈值 V_{TH1} ，降低电压转换电路的输出电压 V_{OUT} ；

步骤 605，当输出电压 V_{OUT} 降低，高侧开关 11 和低侧开关 12 开始导通和关断切换以维持输出电压 V_{OUT} 保持不变，一旦低侧开关 12 的导通频率增大，自举电压 V_{BST} 被及时刷新恢复至预定值。

根据本发明一个实施例的控制电压转换电路的方法还可以包括：

步骤 606，检测自举电压，并将自举电压信号 V_{BST} 与自举电压欠压阈值 V_{UVLO} 相比较，以提供自举欠压信号 **LOCK**。其中，自举电压欠压阈值 V_{UVLO} 小于自举电压刷新阈值 V_{TH1} 。若自举电压信号 V_{BST} 低于自举电压欠压阈值 V_{UVLO} ，自举欠压信号 **LOCK** 具有第一逻辑状态；若自举电压信号 V_{BST} 高于自举电压欠压阈值信号 V_{UVLO} ，自举欠压信号 **LOCK** 具有第二逻辑状态。

步骤 607，基于自举欠压信号 **LOCK** 控制高侧开关 11 和低侧开关 12 的导通与关断。当自举欠压信号 **LOCK** 具有第一逻辑状态时，将高侧开关 11 和低侧开关 12 关断，使其停止导通与关断切换；当自举欠压信号 **LOCK** 具有第二逻辑状态时，允许高侧开关 11 和低侧开关 12 进行导通和关断切换。

在一个实施例中，高侧开关 11 和低侧开关 12 具有公共节点 **SW**，步骤 604 中降低电压转换电路的输出电压 V_{OUT} 包括：在电压转换电路的输出端 **OUT** 和/或所述公共节点 **SW** 与地 **GND** 之间连接一个电



阻 R_1 或电流沉对输出电压 V_{OUT} 放电。

在一个实施例中,步骤 604 中降低电压转换电路的输出电压 V_{OUT} 包括:检测流过低侧开关 12 的电流,产生一个电流采样信号 V_{CS} ;将电流采样信号 V_{CS} 与一电流阈值信号 V_P 比较,提供第二比较信号 A_R ;根据第一比较信号 A_S 和第二比较信号 A_R 提供自举电压刷新信号 RFS ;基于自举电压刷新信号 RFS 控制低侧开关 12 的导通与关断切换以降低输出电压 V_{OUT} ;其中,若自举电压 V_{BST} 低于自举电压刷新阈值 V_{TH1} ,自举电压刷新信号 RFS 具有第一逻辑状态,低侧开关 12 管导通;若电流采样信号 V_{CS} 高于电流刷新阈值 V_{TH1} ,自举电压刷新信号 RFS 具有第二逻辑状态,低侧开 12 关断。

在一个实施例中,步骤 604 中降低电压转换电路的输出电压 V_{OUT} 包括:产生一个恒定导通时间控制信号 C_R ,用于设定一个恒定导通时间;根据第一比较信号 A_S 和恒定导通时间控制信号 C_R 提供自举电压刷新信号 RFS ;基于自举电压刷新信号 RFS 控制低侧开关 12 的导通与关断切换以降低输出电压 V_{OUT} 。其中,当若自举电压 V_{BST} 低于自举电压刷新阈值 V_{TH1} ,自举电压刷新信号 RFS 具有第一逻辑状态,导通低侧开关管 12;当低侧开关导通恒定导通时间之后,自举电压刷新信号 RFS 具有第二逻辑状态,关断低侧开关管 12。

以上对根据本发明各实施例及其变形实施方式的控制电压转换电路的方法及步骤的描述仅为示例性的,并不用于对本发明进行限定。另外,一些公知的控制步骤及所用控制参数等并未给出或者并未详细描述,以使本发明清楚、简明且便于理解。发明所属技术领域的技术



人员应该理解，以上对根据本发明各实施例的控制电压转换电路的方法及步骤的描述中所述使用的步骤编号并不用于表示各步骤的绝对先后顺序，这些步骤并不按照步骤编号顺序实现，而可能采用不同的顺序实现，也可能同时并列地实现，并不仅仅局限于所描述的实施例。

虽然本说明书中以降压型电压转换电路为例对根据本发明各实施例的自举电压刷新控制电路、包含该自举电压刷新控制电路的电压转换电路及其控制方法进行了示意与描述，但这并不意味着对本发明的限定，本领域的技术人员应该理解这里给出的结构及原理也可以适用于具有其它拓扑结构的电压转换电路，例如：升压型电压转换电路、降压-升压型电压转换电路等等。

因此，上述本发明的说明书和实施方式仅仅以示例性的方式对本发明实施例的自举电压刷新控制电路、包含该自举电压刷新控制电路的电压转换电路及其控制方法进行了说明，并不用于限定本发明的范围。对于公开的实施例进行变化和修改都是可能的，其他可行的选择性实施例和对实施例中元件的等同变化可以被本技术领域的普通技术人员所了解。本发明所公开的实施例的其他变化和修改并不超出本发明的精神和保护范围

说明书附图

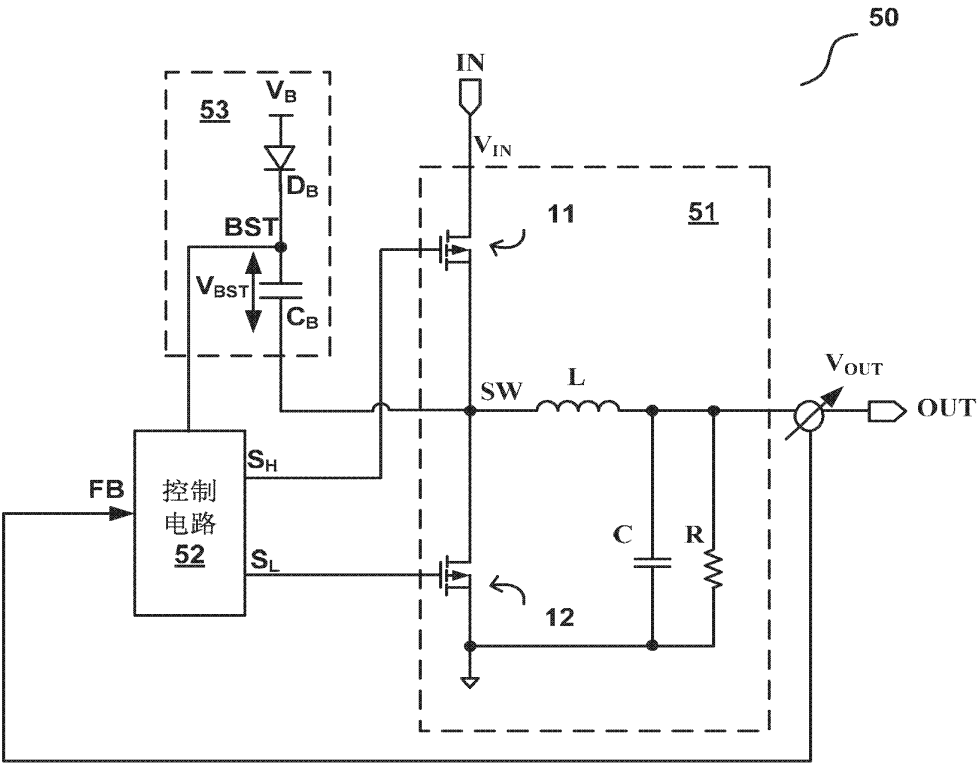


图 1

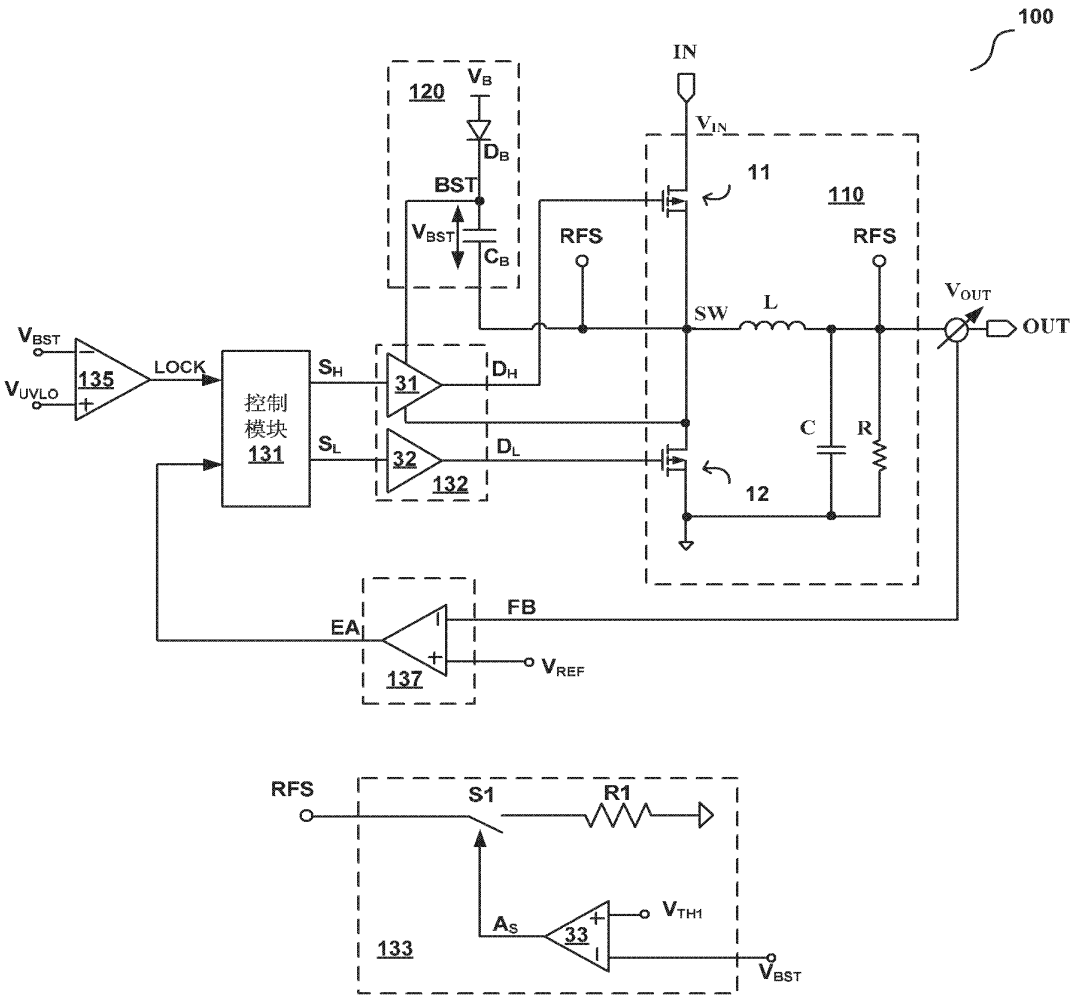


图 2

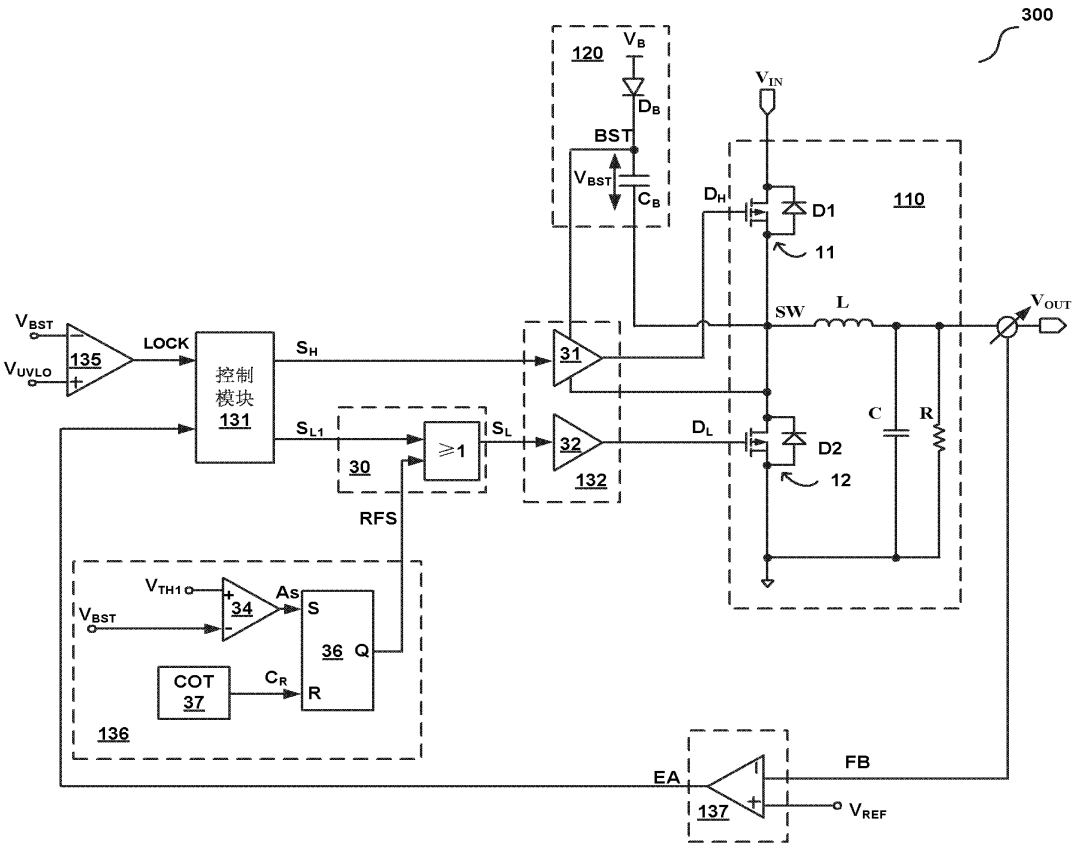


图 4

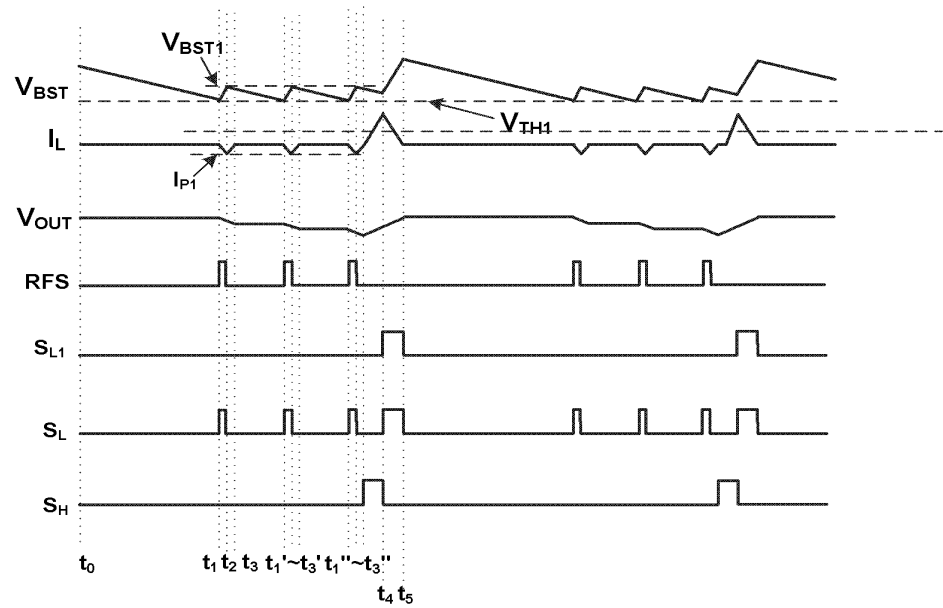


图 5

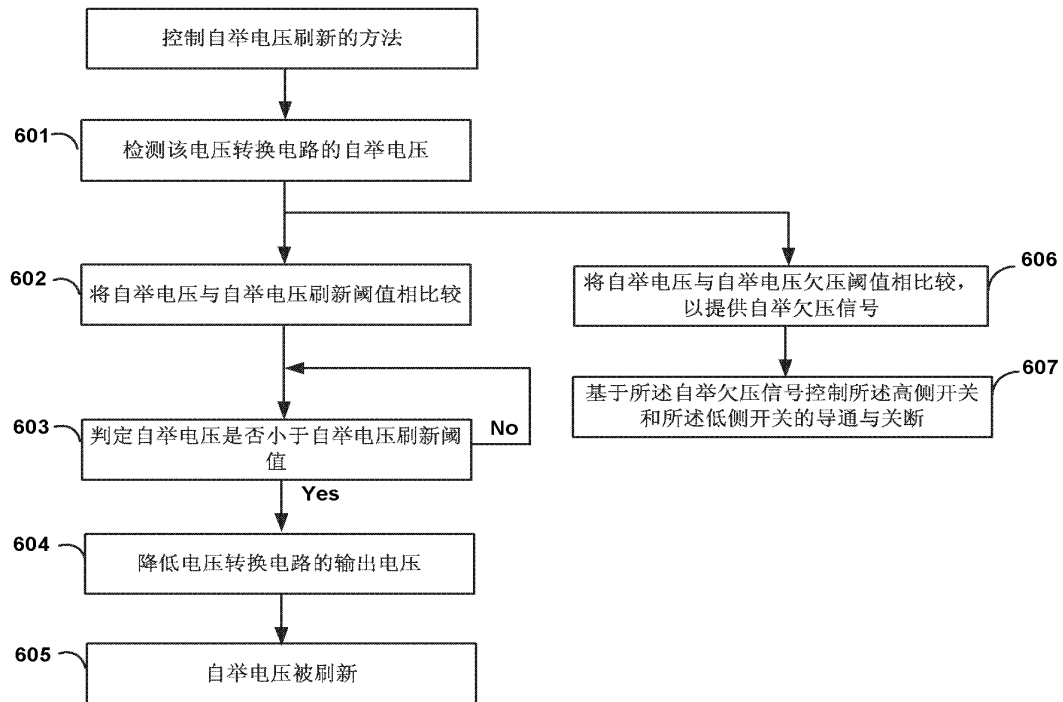


图 6



UNITED STATES PATENT AND TRADEMARK OFFICE

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Alexandria, Virginia 22313-1450
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/823,900	08/11/2015	Li Xu	38616-8386.US00

CONFIRMATION NO. 6869

67394
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PUBLICATION NOTICE



OC000000080541375

Title:BOOTSTRAP REFRESH CONTROL CIRCUIT, VOLTAGE CONVERTER AND ASSOCIATED METHOD

Publication No.US-2016-0043642-A1

Publication Date:02/11/2016

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

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Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

Docket No.: 038616-8386.US00
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
Li Xu

Application No.: 14/823,900

Confirmation No.: 6869

Filed: August 11, 2015

Art Unit: 2838

For: BOOTSTRAP REFRESH CONTROL
CIRCUIT, VOLTAGE CONVERTER AND
ASSOCIATED METHOD

Examiner: Adolf D. Berhane

REQUEST TO CORRECT APPLICATION DATA

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Commissioner:

Applicant hereby requests that the application number indicated below be added to the previously listed foreign priority claim on the Application Data Sheet filed on August 11, 2015 in the above-identified U.S. patent application. Submitted herewith is an annotated updated Application Data Sheet.

<u>Country</u>	<u>Application No.</u>	<u>Date</u>
China	201410658580.3	November 18, 2014

A certified copy of the priority application has been submitted to the United States Patent and Trademark Office.

Applicant additionally requests that all pertinent U.S. Patent and Trademark Office records relating to the subject application be changed to reflect this correction.

-1-

131643837.1

Applicant believes no fee is due with this request. However, if a fee is due, please charge our Deposit Account No. 50-0665, under Order No. 038616-8386.US00 from which the undersigned is authorized to draw.

Dated: July 8, 2016

Respectfully submitted,

By /Chun M. Ng/
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Attorneys for Applicant

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	38616-8386.US00
		Application Number	
Title of Invention	BOOTSTRAP REFRESH CONTROL CIRCUIT, VOLTAGE CONVERTER AND ASSOCIATED METHOD		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

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Legal Name				
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Residence Information (Select One) ☐ US Residence ☒ Non US Residence ☐ Active US Military Service				
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City	Chengdu	State/Province		
Postal Code	611731	Country ⁱ	CN	
All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the Add button. Add				

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).			
☐ An Address is being provided for the correspondence information of this application.			
Customer Number	67394		
Email Address	patentprocurement@perkinscoie.com	Add Email	Remove Email

Application Information:

Title of the Invention	BOOTSTRAP REFRESH CONTROL CIRCUIT, VOLTAGE CONVERTER AND ASSOCIATED METHOD		
Attorney Docket Number	38616-8386.US00	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	6	Suggested Figure for Publication (if any)	

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	38616-8386.US00
		Application Number	
Title of Invention	BOOTSTRAP REFRESH CONTROL CIRCUIT, VOLTAGE CONVERTER AND ASSOCIATED METHOD		

Filing By Reference :

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

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☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

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Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

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This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.

When referring to the current application, please leave the application number blank.

Prior Application Status		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	38616-8386.US00
		Application Number	
Title of Invention	BOOTSTRAP REFRESH CONTROL CIRCUIT, VOLTAGE CONVERTER AND ASSOCIATED METHOD		

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(d). When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)¹ the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(h)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove			
Application Number	Country ¹	Filing Date (YYYY-MM-DD)	Access Code ¹ (if applicable)
201410390708.2	CN	2014-08-11	
Remove			
Application Number	Country ¹	Filing Date (YYYY-MM-DD)	Access Code ¹ (if applicable)
201410658580.3	CN	2014-11-18	
Additional Foreign Priority Data may be generated within this form by selecting the Add button.			

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013. ☐ NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.
--

Authorization to Permit Access:

☐ Authorization to Permit Access to the Instant Application by the Participating Offices

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	38616-8386.US00
		Application Number	
Title of Invention	BOOTSTRAP REFRESH CONTROL CIRCUIT, VOLTAGE CONVERTER AND ASSOCIATED METHOD		

If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application.

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date of filing this Authorization.

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

☒ Assignee
 ☐ Legal Representative under 35 U.S.C. 117
 ☐ Joint Inventor

☐ Person to whom the inventor is obligated to assign.
 ☐ Person who shows sufficient proprietary interest

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor :

If the Applicant is an Organization check here. ☒

Organization Name Chengdu Monolithic Power Systems Co., Ltd.

Mailing Address Information For Applicant:

Address 1		No. 8 Kexin Road	
Address 2		West Zone of Hi-tech Zone	
City	Chengdu	State/Province	
Country	CN	Postal Code	
Phone Number		Fax Number	

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	38616-8386.US00
		Application Number	
Title of Invention	BOOTSTRAP REFRESH CONTROL CIRCUIT, VOLTAGE CONVERTER AND ASSOCIATED METHOD		
Email Address			
Additional Applicant Data may be generated within this form by selecting the Add button.			

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.				
Assignee 1				
Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.				
If the Assignee or Non-Applicant Assignee is an Organization check here. ☐				
Prefix	Given Name	Middle Name	Family Name	Suffix
Mailing Address Information For Assignee including Non-Applicant Assignee:				
Address 1				
Address 2				
City		State/Province		
Country		Postal Code		
Phone Number		Fax Number		
Email Address				
Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button.				

Signature:

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications.					
Signature	/Rodney-Fullett-/Chun M. Ng/		Date (YYYY-MM-DD)	2015-08-14	2016-07-08
First Name	Chun	Last Name	Fullett Ng	Registration Number	34934 36878
Additional Signature may be generated within this form by selecting the Add button.					

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	38616-8386.US00
		Application Number	
Title of Invention	BOOTSTRAP REFRESH CONTROL CIRCUIT, VOLTAGE CONVERTER AND ASSOCIATED METHOD		

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt	
EFS ID:	26301780
Application Number:	14823900
International Application Number:	
Confirmation Number:	6869
Title of Invention:	BOOTSTRAP REFRESH CONTROL CIRCUIT, VOLTAGE CONVERTER AND ASSOCIATED METHOD
First Named Inventor/Applicant Name:	Li Xu
Customer Number:	67394
Filer:	Chun Ng/Pamela Stenslie
Filer Authorized By:	Chun Ng
Attorney Docket Number:	38616-8386.US00
Receipt Date:	08-JUL-2016
Filing Date:	11-AUG-2015
Time Stamp:	18:28:18
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment		no			
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Corrected Filing Receipt	2016_07_08_RequesttoCorrect ApplicationData.PDF	64108	no	2
			4359e581bfd797525b0753fc5b7d83847df d5b3		
Warnings:					

Information:					
2	Application Data Sheet	Annotated_Updated_ADS_386168386US.PDF	186833	no	7
			f0565aaacaa9c7c90726b98d730a9d1bad7f0be7		
Warnings:					
Information:					
This is not an USPTO supplied ADS fillable form					
Total Files Size (in bytes):			250941		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

MPS 0512-CHN-IZ

14/823,900

8/11/2015



中华人民共和国国家知识产权局
STATE INTELLECTUAL PROPERTY OFFICE
OF THE PEOPLE'S REPUBLIC OF CHINA

证 明

本证明之附件是向本局提交的下列专利申请文件副本。

申 请 号： 201410658580.3

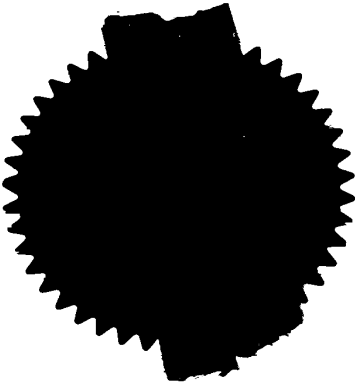
申 请 类 型： 发明专利

发 明 创 造 名 称： 一种自举电压刷新控制电路、电压转换电路及其控制方法

申 请 日： 2014年11月18日

申 请 人： 成都芯源系统有限公司

发明人或设计人： 许力



局长

申长雨

申长雨

2015 年 03 月 23 日



权利要求书

1、一种自举电压刷新控制电路，用于电压转换电路，其中所述电压转换电路包括高侧开关和低侧开关以及用于为所述高侧开关提供自举电压信号的自举电容，所述电压转换电路基于所述高侧开关和低侧开关的导通和关断切换将其输入端的输入电压转换为其输出端的输出电压，所述自举电压刷新控制电路包括：

自举电压刷新模块，所述自举电压刷新模块包括第一比较模块，所述第一比较模块具有第一输入端、第二输入端和输出端，其中第一比较模块的第一输入端用于接收所述自举电压信号；第一比较模块的第二输入端用于接收一自举电压刷新阈值；第一比较模块用于将所述自举电压信号与所述自举电压刷新阈值进行比较并在第一比较模块的输出端提供第一比较信号；其中，若所述自举电压信号低于所述自举电压刷新阈值，所述第一比较信号具有第一逻辑状态；若所述自举电压信号高于所述自举电压刷新阈值，所述第一比较信号具有第二逻辑状态；以及

电压差值模块，具有第一输入端、第二输入端和输出端，所述电压差值模块的第一输入端接收代表所述输出电压的反馈信号；所述电压差值模块的第二输入端接收参考信号；所述电压差值模块对所述反馈信号和所述参考信号进行比较，并在其输出端输出差值信号；

其中，当所述第一比较信号具有第一逻辑状态时，所述自举电压刷新模块用于降低所述输出电压，当所述反馈信号小于所述参考信号时，所述自举电压刷新控制电路根据所述差值信号控制所述高侧开关和所述低侧开关开始导通和关断切换，所述自举电容被充电，所述自举电压被刷新。

2、根据权利要求1所述的自举电压刷新控制电路，其特征在于：

所述自举电压刷新阈值包括第一刷新阈值和第二刷新阈值，其中所述第一刷新阈值小于所述第二刷新阈值；

若所述自举电压信号低于所述第一刷新阈值，所述第一比较信号具有第一逻辑状态；





若所述自举电压信号高于所述第二刷新阈值，所述第一比较信号具有第二逻辑状态。

3. 根据权利要求 1 所述的自举电压刷新控制电路，其中，所述高侧开关和所述低侧开关具有公共节点，所述自举电压刷新模块还包括开关管和电阻，其中，

所述开关管具有第一端、第二端和控制端，其中所述开关管的第一端耦接至所述电压转换电路的输出端和/或所述公共节点；所述开关管的第二端耦接电阻的一端；所述开关管的控制端接收所述第一比较信号；所述电阻的第二端电连接至逻辑地；

若所述第一比较信号具有第一逻辑状态，所述开关管导通；若所述第一比较信号具有第二逻辑状态，所述开关管关断。

4. 根据权利要求 1 所述的自举电压刷新控制电路，其中，所述自举电压刷新模块进一步包括：

第二比较模块，具有第一输入端、第二输入端和输出端，其中第二比较模块的第一输入端用于接收所述低侧开关的电流采样信号；第二比较模块的第二输入端用于接收一电流阈值信号；第二比较模块用于将所述电流采样信号与所述电流阈值信号进行比较并在第二比较模块的输出端提供第二比较信号；其中，若所述电流采样信号高于所述电流阈值信号，所述第二比较信号具有第一逻辑状态；若所述电流采样信号低于所述电流阈值信号，所述第二比较信号具有第二逻辑状态；以及

第一逻辑模块，具有第一输入端、第二输入端以及输出端，其中第一逻辑模块的第一输入端耦接至第一比较模块的输出端，接收第一比较信号；第一逻辑模块的第二输入端耦接至第二比较模块的输出端，接收第二比较信号；第一逻辑模块用于将第一比较信号和第二比较信号做逻辑运算并在输出端提供自举电压刷新信号；

其中，若所述第一比较信号具有第一逻辑状态，所述自举电压刷新信号具有第一逻辑状态，所述低侧开关导通；若所述第二比较信号具有第一逻辑状态，所述自举电压刷新信号具有第二逻辑状态，所述低侧开关关断。





5. 根据权利要求 1 所述的自举电压刷新控制电路, 其中, 所述自举电压刷新模块进一步包括:

恒定导通时间电路, 用于设定一个恒定导通时间并提供一个恒定导通时间控制信号, 其中, 所述恒定导通时间控制信号在恒定导通时间以内具有第一逻辑状态, 在恒定导通时间以外具有第二逻辑状态; 以及

第一逻辑模块, 具有第一输入端、第二输入端以及输出端, 其中第一逻辑模块的第一输入端耦接至第一比较模块的输出端, 接收第一比较信号; 第一逻辑模块的第二输入端耦接至恒定导通时间电路的输出端, 接收恒定导通时间控制信号; 第一逻辑模块用于将第一比较信号和恒定导通时间控制信号做逻辑运算并在输出端提供自举电压刷新信号;

其中, 若所述第一比较信号具有第一逻辑状态, 所述自举电压刷新信号具有第一逻辑状态, 低侧开关导通; 若所述恒定导通时间控制信号具有第二逻辑状态, 所述自举电压刷新信号具有第二逻辑状态, 低侧开关关断。

6、根据权利要求 1 所述的自举电压刷新控制电路, 其中, 所述自举电压刷新控制电路进一步包括:

自举欠压闭锁模块, 具有第一输入端、第二输入端和输出端, 其中所述自举欠压闭锁模块的第一输入端用于接收所述自举电压信号; 所述自举欠压闭锁模块的第二输入端用于接收自举电压欠压阈值信号, 且所述自举电压欠压阈值信号小于所述自举电压刷新阈值; 所述自举欠压闭锁模块用于将所述自举电压信号与所述自举电压欠压阈值信号相比较, 并在所述自举欠压闭锁模块的输出端提供自举欠压信号;

其中, 若所述自举电压信号低于所述自举电压欠压阈值信号, 所述自举欠压信号具有第一逻辑状态; 若所述自举电压信号高于所述自举电压欠压阈值信号, 所述自举欠压信号具有第二逻辑状态; 以及

当所述自举欠压信号具有第一逻辑状态时, 所述自举电压刷新控制电路基于该自举欠压信号将所述高侧开关和所述低侧开关关断, 停







开关的导通和关断切换将其输入端的输入电压转换为其输出端的输出电压，所述控制电压转换电路的方法包括：

检测所述自举电压；

将所述自举电压与一自举电压刷新阈值相比较，提供第一比较信号；

判定所述自举电压是否小于所述自举电压刷新阈值；

当所述自举电压小于所述自举电压刷新阈值时，采用一个自举电压刷新电路降低所述输出电压；以及

当输出电压降低，所述高侧开关和所述低侧开关开始导通和关断切换，自举电容被充电，自举电压被刷新。

10、根据权利要求 9 所述的自举电压刷新的方法，其中，高侧开关和低侧开关具有公共节点，其中，采用一个自举电压刷新电路降低所述输出电压包括：

当所述自举电压低于所述自举电压刷新阈值，在所述电压转换电路的输出端和/或所述公共节点与地之间连接一个电阻或电流沉。

11、根据权利要求 9 所述的自举电压刷新的方法，其中，采用一个自举电压刷新电路降低所述输出电压包括：

检测流过低侧开关的电流，产生一个电流采样信号；

将所述电流采样信号与一电流阈值信号比较，提供第二比较信号；

根据第一比较信号和第二比较信号提供自举电压刷新信号；以及

基于所述自举电压刷新信号控制所述低侧开关的导通与关断切换以降低输出电压；

其中，若所述自举电压低于所述自举电压刷新阈值，所述自举电压刷新信号具有第一逻辑状态，所述低侧开关导通；

若所述电流采样信号大于所述电流刷新阈值，所述自举电压刷新信号具有第二逻辑状态，所述低侧开关关断。

12、根据权利要求 9 所述的自举电压刷新的方法，其中，采用一个自举电压刷新电路降低所述输出电压包括：

产生一个恒定导通时间控制信号，用于设定一个恒定导通时间；

根据第一比较信号和恒定导通时间控制信号提供自举电压刷新





信号；以及

基于所述自举电压刷新信号控制所述低侧开关的导通与关断切换以降低输出电压；

其中，若所述自举电压低于所述自举电压刷新阈值，所述自举电压刷新信号具有第一逻辑状态，导通所述低侧开关；

当低侧开关导通所述恒定导通时间之后，所述自举电压刷新信号具有第二逻辑状态，关断低侧开关。





说明书

一种自举电压刷新控制电路、电压转换电路及其控制方法

技术领域

本发明的实施例涉及电子电路，尤其涉及电压转换电路、自举电压刷新控制电路及其控制方法。

背景技术

在目前的开关型直流变换电路中，需要高压驱动开关管，因此常用到自举电路以提供所需的驱动电压。

图 1 所示为一电压转换电路 50。如图 1 所示，电压转换电路 50 包括开关电路 51，控制电路 52。开关电路 51 包括高侧开关 11、低侧开关 12，电感器 L、电容器 C 以及负载 R。高侧开关 11 的漏极电连接至电压转换电路 50 的输入端 IN 接收输入电压信号 V_{IN} ；低侧开关 12 的源极电连接至地；高侧开关 11 的源极和低侧开关 12 的漏极耦接形成公共节点 SW；电感 L 电连接于节点 SW 和电压转换电路 50 的输出端 OUT 之间；电容器 C 和负载 R 并联连接于电压转换电路 50 的输出端 OUT 和地之间。

控制电路 52 耦接至电压转换电路 50 的输出端 OUT 接收代表输出电压 V_{OUT} 的反馈信号 FB，控制电路 52 根据输出电压 V_{OUT} 的变化，产生用于导通和关断高侧开关 11 和低侧开关 12 的控制信号 S_H 和 S_L 。在一个实施例中，控制电路 52 包括脉冲宽度调制(PWM)电路，PWM



控制电路通过提供不同占空比的方形脉冲信号，进而调节输出电压 V_{OUT} 的大小。在另一个实施例中，控制电路 52 包括脉冲频率调制（PFM）电路，PFM 控制电路通过提供不同频率的方形脉冲信号，进而调节输出电压 V_{OUT} 的大小。

在图 1 所示实施例中，控制电路 52 中还包括驱动电路用于驱动高侧开关 11 和低侧开关 12。在电感器正向储能期间，驱动电路将拉高高侧开关管 11 的栅极电压，在这种情况下，为了使高侧开关 11 能够充分导通（即：高侧开关 11 工作在饱和区，这样高侧开关 11 的导通电阻很小），高侧开关 11 的栅极与其耦接至节点 SW 的一端之间的电压差应该足够大，至少需要大于高侧开关 11 的导通阈值电压。然而，若高侧开关 11 导通，节点 SW 的电压可以是输入电压 V_{IN} ，这时，需要为高侧开关 11 的栅极提供高于节点 SW 的电压（即高于输入电压 V_{IN} ）的电压才能使高侧开关 11 充分导通。

为了在电压转换电路 50 中获得高于输入电压 V_{IN} 的电压，因此，通常电压转换电路 50 中还包括自举电路 53，用于以节点 SW 的电压为参考电势产生自举电压 V_{BST} ，该自举电压 V_{BST} 可以用于提升/增强驱动电路驱动的驱动能力，从而更好地控制高侧开关 11 的导通和关断。

在图 1 所示实施例中，自举电路 53 包括二极管 D_B 和自举电容 C_B ，串联耦接于自举供电输入端和节点 SW 之间，其中二极管 D_B 的阳极耦接自举供电输入端接收自举供电电压 V_B ，二极管 D_B 的阴极耦接自举电容 C_B 的第一端，自举电容 C_B 的第二端耦接节点 SW。自举





电路 53 的工作原理是本领域的普通技术人员所熟知的，即，当高侧开关 11 关断时，低侧开关 12 导通，节点 SW 的电压为零，自举供电电压 V_B 通过二极管 D_B 为自举电容 C_B 充电，使得自举电容 C_B 第一端和第二端之间具有自举电压 V_{BST} ；当高侧开关 11 导通时，低侧开关 12 关断，节点 SW 处的电压为 V_{IN} ，此时节点 BST 的电压被抬升为输入电压 V_{IN} 叠加上自举电压 V_{BST} ，从而实现了在降压型直流电压转换电路 50 中获得高于输入电压 V_{IN} 的电压的目的。同时，二极管 D_B 反向偏置而被关断，从而可以保护提供自举供电电压的电源不受相对较高的输入电压 V_{IN} 的损坏。

可见，自举电路 53 通过在低侧开关 12 导通时将自举电容 C_B 第二端的电压拉低至参考地，而获得为自举电容 C_B 充电的机会，以提供自举电压 V_{BST} 。然而在某些工作状态下，由于自举电容 C_B 上的电荷不足而又不能及时被充电到足够的水平，而导致自举电路 53 提供的自举电压 V_{BST} 下降，不足以使高侧开关 11 正常导通和关断，因此电压转换电路 50 不能正常工作；又或自举电压 V_{BST} 下降到电路预设的低压闭锁值，使得整个变换器被锁定，电路也因此不能正常工作。

例如，当输出电压 V_{OUT} 接近输入电压 V_{IN} ，此时需要高侧开关 11 以很高、甚至 100% 的占空比工作（导通时间延长或切换频率增大），低侧开关 12 导通时间非常短、甚至没有导通机会，因此自举电容 C_B 不能及时充电到相关水平。

又如，在轻载或空载条件下，控制电路 52 会降低高侧开关 11 和低侧开关 12 的导通时间和/或者切换频率，甚至同时关断高侧开关 11





和低侧开关 12 以提高转换效率, 这样可能由于低侧开关 12 在较长时间内没有进行导通或导通时间很短而无法使自举电容 C_B 被及时充电, 以使自举电压 V_{BST} 被刷新恢复至期望值。

这些均会导致自举电路 53 提供的自举电压 V_{BST} 下降, 不足以使高侧开关 11 正常导通和关断, 那么电压转换电路 50 也因此不能正常工作。这样要等到多个周期之后输出电压 V_{OUT} 自然掉落, 自举电容 C_B 才有机会被充电以使自举电压 V_{BST} 恢复。在此过程中, 输出电压 V_{OUT} 会出现较大的波动尖峰, 这不仅对电压转换电路 50 不利, 更有可能损害负载, 因而不希望出现的。

发明内容

针对现有技术中的一个或多个问题, 提出了一种自举电压刷新控制电路、电压转换电路及其控制方法。

本发明一方面提供了一种自举电压刷新控制电路, 用于电压转换电路, 其中所述电压转换电路包括高侧开关和低侧开关以及用于为所述高侧开关提供自举电压信号的自举电容, 所述电压转换电路基于所述高侧开关和低侧开关的导通和关断切换将其输入端的输入电压转换为其输出端的输出电压。所述自举电压刷新控制电路包括: 自举电压刷新模块, 所述自举电压刷新模块包括第一比较模块, 所述第一比较模块具有第一输入端、第二输入端和输出端, 其中第一比较模块的第一输入端用于接收所述自举电压信号; 第一比较模块的第二输入端用于接收一自举电压刷新阈值; 第一比较模块用于将所述自举电压信号与所述自举电压刷新阈值进行比较并在第一比较模块的输出端提





供第一比较信号；其中，若所述自举电压信号低于所述自举电压刷新阈值，所述第一比较信号具有第一逻辑状态；若所述自举电压信号高于所述自举电压刷新阈值，所述第一比较信号具有第二逻辑状态。所述自举电压刷新控制电路进一步包括电压差值模块，具有第一输入端、第二输入端和输出端，所述电压差值模块的第一输入端接收代表所述输出电压的反馈信号；所述电压差值模块的第二输入端接收参考信号；所述电压差值模块对所述反馈信号和所述参考信号进行比较，并在其输出端输出差值信号。其中，当所述第一比较信号具有第一逻辑状态时，所述自举电压刷新模块用于降低所述输出电压，当所述反馈信号小于所述参考信号时，所述自举电压刷新控制电路根据所述差值信号控制所述高侧开关和所述低侧开关开始导通和关断切换，所述自举电容被充电，所述自举电压被刷新。

本发明另一方面提供了一种电压转换电路，包括：开关电路，具有高侧开关和低侧开关，通过高侧开关和低侧开关的导通和关断切换将电压转换电路输入端的输入电压信号转换为其输出端的输出电压信号；自举电路，包括自举电容，用于为所述高侧开关提供自举电压信号；以及自举电压刷新控制电路。

本发明进一步提供了一种自举电压刷新控制方法，该方法用于电压转换电路，其中所述电压转换电路包括高侧开关和低侧开关以及用于为所述高侧开关提供自举电压的自举电容，所述电压转换电路基于所述高侧开关和低侧开关的导通和关断切换将其输入端的输入电压转换为其输出端的输出电压。所述控制电压转换电路的方法包括：检





测所述自举电压；将所述自举电压与一自举电压刷新阈值相比较，提供第一比较信号；判定所述自举电压是否小于所述自举电压刷新阈值；当所述自举电压小于所述自举电压刷新阈值时，采用一个自举电压刷新电路降低所述输出电压；以及当输出电压降低，所述高侧开关和所述低侧开关开始导通和关断切换，自举电容被充电，自举电压被刷新。根据上述方面的实施例，本申请提出的自举电压刷新控制电路在不影响电路正常的控制方式和开关时序的情况下刷新自举电压，简化了电路逻辑的设计。

附图说明

在所有附图中，相同的标号表示具有相同、相似或相应的特征或功能。

图 1 示出了一种典型的电压转换电路 50 的简化示意图。

图 2 示出了根据本发明一实施例的电压转换电路 100 的示意图。

图 3 示出了根据本发明另一实施例的电压转换电路 200 的示意图。

图 4 示出了根据本发明又一实施例的电压转换电路 300 的示意图。

图 5 示出了根据本发明一个实施例的电压转换电路的工作波形示意图。

图 6 示出了根据本发明一个实施例的控制电压转换电路的方法的流程示意图。

具体实施方式

下面将详细描述本公开的具体实施例，应当注意，这里描述的实



施例只用于举例说明，并不用于限制本公开。相反，本公开意在涵盖由所附权利要求所界定的本公开精神和范围内所定义的各种备选方案、修改方案和等同方案。在以下描述中，为了提供对本公开的透彻理解，阐述了大量特定细节。然而，对于本领域普通技术人员应当理解，没有这些具体细节，本公开同样可以实施。在其他一些实施例中，为了便于凸显本公开的主旨，对于众所周知的方案、流程、元器件以及电路或方法未作详细的描述。

图2所示为根据本发明一个实施例的电压转换电路100的示意图。如图2所示，电压转换电路100包括开关电路110、自举电路120以及控制电路。

开关电路110包括高侧开关11、低侧开关12，电感器L、电容器C以及负载R。高侧开关11的漏极电连接至电压转换电路100的输入端IN接收输入电压 V_{IN} ；低侧开关12的源极电连接至地；高侧开关11的源极和低侧开关12的漏极耦接形成公共节点SW；电感L电连接于节点SW和电压转换电路100的输出端OUT之间；电容器C和负载R并联连接于电压转换电路100的输出端OUT和地之间。在图2所示实施例中，开关电路110包括一个降压型BUCK拓扑结构。在其他实施例中，开关电路110可以采用升压电路拓扑、升降压电路拓扑、反激电路拓扑等其他直流/直流拓扑结构。在图2所示实施例中，高侧开关11和低侧开关12示意为金属氧化物半导体场效应晶体管（MOSFET），但应该理解，高侧开关11和低侧开关12不局限于MOSFET，在其他实施例中，高侧开关11和低侧开关12还可以是





其他任何可控的半导体开关器件，如结型场效应晶体管（JFET）或绝缘栅双极晶体管（IGBT）。

自举电路 120 包括二极管 D_B 和自举电容 C_B ，串联耦接于自举供电输入端和节点 SW 之间，其中二极管 D_B 的阳极耦接自举供电输入端接收自举供电电压 V_B ，二极管 D_B 的阴极耦接自举电容 C_B 的第一端，自举电容 C_B 的第二端耦接节点 SW。当高侧开关 11 关断时，低侧开关 12 导通，节点 SW 的电压为零，自举供电电压 V_B 通过二极管 D_B 为自举电容 C_B 充电，使得自举电容 C_B 第一端和第二端之间具有自举电压 V_{BST} ；当高侧开关 11 导通时，低侧开关 12 关断，节点 SW 处的电压为 V_{IN} ，此时节点 BST 的电压被抬升为输入电压 V_{IN} 叠加上自举电压 V_{BST} ，从而实现了在降压型直流电压转换电路 100 中获得高于输入电压 V_{IN} 的电压的目的。同时，二极管 D_B 反向偏置而被关断，从而可以保护提供自举供电电压的电源不受相对较高的输入电压 V_{IN} 的损坏。

在一个实施例中，控制电路包括电压差值模块 137。电压差值模块 137 具有第一输入端、第二输入端和输出端。电压差值模块 137 的第一输入端耦接至电压转换电路 100 的输出端 OUT 接收输出电压 V_{OUT} 的反馈信号 FB；电压差值模块 137 的第二输入端接收参考电压信号 V_{REF} ；电压差值模块 137 将输出电压反馈信号 FB 和参考电压信号 V_{REF} 进行比较，并在其输出端输出差值信号 EA。在一个实施例中，例如电压控制、电流控制等 PWM 控制方法实施例中，电压差值模块 137 包括一个误差放大器，用于将输出电压反馈信号 FB 和参考电压





信号 V_{REF} 比较后的差值放大，再将该差值放大信号和一个斜坡信号进行比较，进而控制高侧开关 11 和低侧开关 12 的导通和关断切换。在另一个实施例中，例如恒定导通时间控制等 PFM 控制方法实施例中，电压差值模块 137 包括一个电压比较器，用于将输出电压反馈信号 FB 和参考电压信号 V_{REF} 比较，根据比较结果控制高侧开关 11 和低侧开关 12 的导通和关断切换。比如，当输出电压反馈信号 FB 小于参考电压信号 V_{REF} 时高侧开关 11 导通，低侧开关 12 关断；当输出电压反馈信号 FB 大于参考电压信号 V_{REF} 时高侧开关 11 关断，低侧开关 12 导通。

在一个实施例中，控制电路进一步包括控制模块 131。控制模块 131 耦接至电压差值模块 137 的输出端接收差值信号 EA，并根据差值信号 EA 判定输出端的负载情况进而输出高侧开关控制信号 S_H 和低侧开关控制信号 S_L 用于控制高侧开关 11 和低侧开关 12 的导通和关断切换。

在一个实施例中，控制电路进一步包括驱动模块 132。驱动模块 132 包括第一驱动器 31 和第二驱动器 32。第一驱动器 31 具有输入端和输出端，第一驱动器 31 的输入端接收高侧开关控制信号 S_H ，并在其输出端输出高侧开关驱动信号 D_H 至高侧开关 11 的栅极，以驱动高侧开关 11 的导通和关断。第一驱动器 31 包括接收自举电压 V_{BST} ，用于提升/增强第一驱动器 31 提供的高侧开关驱动信号 D_H 的驱动能力，从而更好地控制高侧开关 11 的导通和关断。第二驱动器 32 具有输入端和输出端，第二驱动器 32 的输入端接收低侧开关控制信号 S_L ，并





在其输出端输出低侧开关驱动信号 D_L 至低侧开关的栅极，以驱动低侧开关 12 的导通和关断。根据本发明的一个实施例，所述第一驱动器 31 包括一个或多个反相器，所述自举电压信号 V_{BST} 用作所述一个或多个反相器的供电电源。类似地，所述第二驱动器 32 也可以包括一个或多个反相器。

在一个实施例中，控制电路进一步包括自举电压刷新模块 133。自举电压刷新模块 133 接收自举电压信号 V_{BST} ，并将自举电压信号 V_{BST} 与一个自举电压刷新阈值进行比较。在轻载或空载模式下，高侧开关 11 和低侧开关 12 均关断，流过电感 L 的电感电流为零。与此同时，自举电压 V_{BST} 逐渐降低，当自举电压信号 V_{BST} 小于自举电压刷新阈值时，自举电压刷新模块 133 启用，用于降低输出电压 V_{OUT} 。电压差值模块 137 将代表输出电压 V_{OUT} 的反馈电压 FB 和参考电压信号 V_{REF} 比较，当反馈信号 FB 小于所述参考电压信号 V_{REF} 时，控制模块 131 根据差值信号 EA 控制高侧开关 11 和低侧开关 12 开始导通和关断切换，以使输出电压 V_{OUT} 维持在预设值。即高侧开关 11 和低侧开关 12 从均关断的轻载或空载状态转换为导通和关断切换的正常状态。当高侧开关 11 和低侧开关 12 的切换频率变高，则低侧开关 12 的导通时间增加，自举电容 C_B 可及时被充电，自举电压 V_{BST} 被刷新恢复至期望值。采用自举电压刷新模块 133 降低输出电压 V_{OUT} ，进而增大高侧开关 11 和低侧开关 12 的切换频率以刷新自举电压 V_{BST} ，可以避免使用消隐电路消隐高侧开关 11，同时不影响电压转换电路的控制方式和开关时序，即该实施例通过高侧开关 11 和低侧开关 12







33 的输出端接收第一比较信号 A_S 。电阻 $R1$ 的另一端电连接至逻辑地。若第一比较信号 A_S 具有第一逻辑状态，开关 $S1$ 导通，电容器 C 通过开关 $S1$ 和电阻 $R1$ 放电，输出电压 V_{OUT} 降低。在另一个实施例中，电阻 $R1$ 也可以用一个电流沉代替。

在一个实施例中，控制电路包括自举欠压闭锁模块 135。自举欠压闭锁电路 135 具有第一闭锁输入端、第二闭锁输入端和闭锁输出端。该第一闭锁输入端用于接收自举电压信号 V_{BST} ，该第二闭锁输入端用于接收自举电压欠压阈值信号 V_{UVLO} 。自举欠压闭锁电路 135 用于将自举电压信号 V_{BST} 与自举电压欠压阈值信号 V_{UVLO} 相比较，并在所述闭锁电路 135 的输出端提供自举欠压信号 $LOCK$ 至控制模块 131。若自举电压信号 V_{BST} 低于自举电压欠压阈值信号 V_{UVLO} ，则自举欠压信号 $LOCK$ 具有第一逻辑状态（比如高电平逻辑状态）。这时控制模块 131 控制高侧开关 11 和低侧开关 12 同时关断，停止导通与关断切换。若自举电压信号 V_{BST} 高于自举电压欠压阈值信号 V_{UVLO} ，则自举欠压信号 $LOCK$ 具有第二逻辑状态（比如低电平逻辑状态），这时控制模块 131 控制高侧开关 11 和低侧开关 12 进行导通和关断切换。根据本发明的一个实施例，所述自举电压欠压阈值信号 V_{UVLO} 小于所述自举电压刷新阈值 V_{TH1} 。自举欠压闭锁电路 135 有助于在自举电压信号 V_{BST} 已经低于自举电压欠压阈值信号 V_{UVLO} ，而且未能及时被刷新（即，自举电容 C_B 未能被及时充电使该自举电压信号 V_{BST} 恢复至高于该自举电压欠压阈值信号 V_{UVLO} ）时，将高侧开关 11 和低侧开关 12 均关断，以改善电压转换电路 100 的工作安全性能。





图3所示为根据本发明一个实施例的电压转换电路200的示意图。如图3所示，电压转换电路200包括开关电路110、驱动电路120以及控制电路。为了简便且便于理解，电压转换电路200中那些功能上和电压转换电路100中相同的、同样的或类似的组件或结构沿用了相同的附图标记。同时，在图3所示实施例中，对于开关电路110中的高侧开关11和低侧开关12，示出了其体二极管。具体的来说，示出了高侧开关11的体二极管D1和低侧开关12的体二极管D2。此外，在图3所示实施例中，高侧开关11和低侧开关12被示意为金属氧化物半导体场效应晶体管（MOSFET），但应该理解，高侧开关11和低侧开关12不局限于MOSFET，在其他实施例中，高侧开关11和低侧开关12还可以是其他任何可控的半导体开关器件，如结型场效应晶体管（JFET）或绝缘栅双极晶体管（IGBT）。

在一个实施例中，电压转换电路200中控制电路包括：控制模块131、驱动模块132、电压差值模块137、自举电压刷新模块134以及自举欠压闭锁模块135。为了简便且便于理解，电压转换电路200的控制电路中那些功能上和电压转换电路100的控制电路中相同的、同样的或类似的组件或结构沿用了相同的附图标记的模块的功能不再累述。

自举电压刷新模块134包括第一输入端和输出端。自举电压刷新模块134的第一输入端耦接至自举电路120接收自举电压信号 V_{BST} ，并将自举电压信号 V_{BST} 与一个自举电压刷新阈值进行比较。在轻载或空载模式下，高侧开关11和低侧开关12均关断，流过电感L的电





感电流为零。与此同时，自举电压 V_{BST} 逐渐降低，当自举电压信号 V_{BST} 小于自举电压刷新阈值时，自举电压刷新模块 134 启动用于降低输出电压 V_{OUT} 。电压差值模块 137 将代表输出电压 V_{OUT} 的反馈电压 FB 和参考电压信号 V_{REF} 比较，当反馈信号 FB 小于所述参考电压信号 V_{REF} 时，控制模块 131 根据差值信号 EA 控制高侧开关 11 和低侧开关 12 开始导通和关断切换，以使输出电压 V_{OUT} 维持在预设值。当高侧开关 11 和低侧开关 12 的切换频率变高，则低侧开关 12 的导通时间增加，自举电容 C_B 可及时被充电，自举电压 V_{BST} 被刷新恢复至期望值。采用自举电压刷新模块 134 降低输出电压 V_{OUT} ，进而增大高侧开关 11 和低侧开关 12 的切换频率以刷新自举电压 V_{BST} ，可以避免使用消隐电路消隐高侧开关 11，同时不影响电压转换电路的控制方式和开关时序，即该实施例通过高侧开关 11 和低侧开关 12 的正常切换就能刷新自举电压 V_{BST} 。

在一个实施例中，自举电压刷新模块 134 还包括第二输入端耦接至低侧开关 12 的漏极，接收一个表征流过低侧开关 12 的反向电流的采样信号 V_{CS} ；自举电压刷新模块 134 的输出端提供一自举电压刷新信号 RFS 。

在一个实施例中，若自举电压信号 V_{BST} 低于自举电压刷新阈值 V_{TH1} ，自举电压刷新信号 RFS 具有第一逻辑状态(比如逻辑高状态)，控制电路 131 控制低侧开关管 12 导通，电容器 C 通过电感器 L 和低侧开关 12 放电，流过低侧开关 12 的反向电流增大，输出电压 V_{OUT} 降低，与此同时，自举电容 C_B 也通过低侧开关 12 被充电。当电流采





样信号 V_{CS} 增大到一个预设电流阈值 V_P 后, 自举电压刷新信号 RFS 具有第二逻辑状态 (比如逻辑低状态), 控制电路 131 控制低侧开关管 12 关断, 自举电容 C_B 停止充电。此时, 流过电感器 L 的电流通过高侧开关 11 的体二极管 $D1$ 续流, 此时开关电路 110 变为一个 BOOST 升压变换器, 电容器 C 释放的能量将被存储在电压变换电路 200 的输入端 IN 。在一个实施例中, 电流阈值信号 V_P 越大, 自举电压信号 V_{BST} 恢复的值越大。但是从总体上来说, 自举电压刷新模块 134 主要用于降低输出电压 V_{OUT} , 因此电流阈值信号 V_P 的值不会太大, 低侧开关 12 导通的时间较短, 因此自举电压 V_{BST} 恢复的值有限。一旦输出电压 V_{OUT} 降低, 控制模块 131 将根据差值信号 EA 控制高侧开关 11 和低侧开关 12 开始导通和关断切换, 自举电压 V_{BST} 将被刷新恢复至期望值。

在一个实施例中, 自举电压刷新模块 134 包括第一比较器 34。第一比较器 34 具有第一输入端、第二输入端和输出端。第一比较器 34 的第一输入端用于接收自举电压刷新阈值 V_{TH1} , 第一比较器 34 的第二输入端用于接收自举电压信号 V_{BST} 。第一比较器 34 用于将自举电压信号 V_{BST} 与自举电压刷新阈值 V_{TH1} 相比较, 并在第一比较器 34 的输出端提供第一比较信号 A_S 。在一个实施例中, 若自举电压信号 V_{BST} 低于自举电压刷新阈值 V_{TH1} , 则第一比较信号 A_S 具有第一逻辑状态 (比如高电平逻辑状态); 若自举电压信号 V_{BST} 高于自举电压刷新阈值 V_{TH1} , 则第一比较信号 A_S 具有第二逻辑状态 (比如低电平逻辑状态)。





在一个实施例中，自举电压刷新模块 134 进一步包括第二比较器 35。第二比较器 35 具有第一输入端、第二输入端和输出端。第二比较器 35 的第一输入端用于接收电流阈值信号 V_P ，第二比较器 35 的第二输入端用于接收采样电压信号 V_{CS} 。第二比较器 35 用于将采样电压信号 V_{CS} 与电流阈值信号 V_P 相比较，并在第二比较器 35 的输出端提供自第二比较信号 A_R 。在一个实施例中，若采样电压信号 V_{CS} 高于电流阈值信号 V_P ，则第二比较信号 A_R 具有第一逻辑状态（比如高电平逻辑状态）；若采样电压信号 V_{CS} 低于电流阈值信号 V_P ，则第二比较信号 A_R 具有第二逻辑状态（比如低电平逻辑状态）。在一个实施例中，电流阈值信号 V_P 的选择可根据所需恢复的自举电压信号 V_{BST} 的值选择，电流阈值信号 V_P 越大，所提供的自举电压信号 V_{BST} 的值越大。

在一个实施例中，自举电压刷新模块 134 进一步包括逻辑电路 36。逻辑电路 36 具有第一输入端、第二输入端和输出端。逻辑电路 36 的第一输入端耦接至第一比较器 34 的输出端接收第一比较信号 A_S ，逻辑电路 36 的第二输入端耦接至第二比较器的输出端接收第二比较信号 A_R 。逻辑电路 36 对第一比较信号 A_S 和第二比较信号 A_R 进行逻辑运算，并在其输出端提供一个自举电压刷新信号 RFS 。当第一比较信号 A_S 具有第一逻辑状态时，自举电压刷新信号 RFS 具有第一逻辑状态；当第二比较信号 A_R 具有第一逻辑状态时，自举电压刷新信号 RFS 具有第二逻辑状态。在一个实施例中，当自举电压刷新信号 RFS 为第一逻辑状态时，低侧开关管 12 导通，开关电路 110 中的





电容器 C 通过电感器 L 和低侧开关 12 放电，电感器 L 反向储能，自举电容 C_B 被充电；当自举电压刷新信号 RFS 为第二逻辑状态时，低侧开关 12 关断，自举电容 C_B 停止被充电；流过电感器 L 的电流通过高侧开关 11 的体二极管 $D1$ 续流。

在一个实施例中，控制模块 131 耦接至电压差值模块 137 的输出端，接收差值信号 EA ，并根据差值信号 EA 的变化提供高侧开关控制信号 S_H 和第一低侧开关控制信号 S_{L1} 。高侧开关控制信号 S_H 和第一低侧开关控制信号 S_{L1} 用于控制高侧开关 11 和低侧开关 12 的导通和关断切换。在一个实施例中，当第一低侧开关控制信号 S_{L1} 具有第一逻辑状态（例如逻辑高状态），低侧开关 12 导通；当第一低侧开关控制信号 S_{L1} 具有第二逻辑状态（例如逻辑低状态），低侧开关 12 关断。在一个实施例中，控制模块 131 还包括一个逻辑模块 30。逻辑模块 30 具有第一输入端、第二输入端和输出端。逻辑模块 30 的第一输入端接收第一低侧开关控制信号 S_{L1} ；逻辑模块 30 的第二输入端接收自举电压刷新信号 RFS ；逻辑模块 30 对第一低侧开关控制信号 S_{L1} 和自举电压刷新信号 RFS 做逻辑运算，并在其输出端输出低侧开关控制信号 S_L 。当第一低侧开关控制信号 S_{L1} 和自举电压刷新信号 RFS 任意一个具有第一逻辑状态（例如逻辑高状态），则低侧开关控制信号 S_L 具有第一逻辑状态（例如逻辑高状态），低侧开关 12 导通。在一个实施例中，逻辑模块 30 为一个逻辑或门。

图 4 所示为根据本发明一个实施例的电压转换电路 300 的示意图。在图 4 所示一个实施例中，电压转换电路 300 中控制电路包括：控制





模块 131、驱动模块 132、电压差值模块 137、自举电压刷新模块 136 以及自举欠压闭锁模块 135。为了简便且便于理解，电压转换电路 300 中那些功能上和电压转换电路 200、100 中相同的、同样的或类似的组件或结构沿用了相同的附图标记，同时，不再累述与电压转换电路 200、100 中相同的功能模块。

在一个实施例中，自举电压刷新模块 136 包括第一比较器 34。第一比较器 34 具有第一输入端、第二输入端和输出端。第一比较器 34 的第一输入端用于接收自举电压刷新阈值 V_{TH1} ，第一比较器 34 的第二输入端用于接收自举电压信号 V_{BST} 。第一比较器 34 用于将自举电压信号 V_{BST} 与自举电压刷新阈值 V_{TH1} 相比较，并在第一比较器 34 的输出端提供第一比较信号 A_S 。在一个实施例中，若自举电压信号 V_{BST} 低于自举电压刷新阈值 V_{TH1} ，则第一比较信号 A_S 具有第一逻辑状态（比如高电平逻辑状态）；若自举电压信号 V_{BST} 高于自举电压刷新阈值 V_{TH1} ，则第一比较信号 A_S 具有第二逻辑状态（比如低电平逻辑状态）。

在一个实施例中，自举电压刷新模块 136 进一步包括一个恒定时间导通电路 37。恒定导通时间电路 37 用于设定一个低侧开关的导通时间，并输出一个恒定时间控制信号 C_R 。在一个实施例中，恒定时间控制信号 C_R 包括高低电平信号，具有第一逻辑状态和第二逻辑状态。其中，恒定导通时间控制信号 C_R 在恒定导通时间以内具有第一逻辑状态，在恒定导通时间以外具有第二逻辑状态。

在一个实施例中，自举电压刷新模块 136 进一步包括逻辑电路





36。逻辑电路 36 具有第一输入端、第二输入端和输出端。逻辑电路 36 的第一输入端耦接至第一比较器 34 的输出端接收第一比较信号 A_S ，逻辑电路 36 的第二输入端耦接至第二比较器的输出端接收恒定时间控制信号 C_R 。逻辑电路 36 对第一比较信号 A_S 和恒定时间控制信号 C_R 进行逻辑运算，并在其输出端提供一个自举电压刷新信号 RFS。当第一比较信号 A_S 具有第一逻辑状态时，自举电压刷新信号 RFS 具有第一逻辑状态；当恒定时间控制信号 C_R 具有第二逻辑状态时，自举电压刷新信号 RFS 具有第二逻辑状态。

在一个实施例中，当自举电压刷新信号 RFS 为第一逻辑状态时，低侧开关管 12 导通，开关电路 110 中的电容器 C 通过电感器 L 和低侧开关 12 放电，电感器 L 反向储能，流过低侧开关 12 的反向电流增大，输出电压 V_{OUT} 降低，与此同时，自举电容 C_B 也将被充电。当自举电压刷新信号 RFS 为第二逻辑状态时，低侧开关 12 关断，自举电容 C_B 停止被充电。此时，流过电感器 L 的电流通过高侧开关 11 的体二极管 D1 续流，开关电路 110 变为一个 BOOST 升压变换器，电容器 C 释放的能量将被存储在电压变换电路 200 的输入端 IN。在一个实施例中，恒定导通时间电路 37 设定的导通时间越长，自举电压信号 V_{BST} 恢复的值越大。但是从总体上来说，自举电压刷新电路 136 主要用于降低输出电压 V_{OUT} ，因此恒定导通时间电路 37 设定的导通时间不会太长，低侧开关 12 导通的时间较短，因此自举电压 V_{BST} 恢复的值有限。一旦输出电压 V_{OUT} 降低，控制模块 131 将根据差值信号 EA 控制高侧开关 11 和低侧开关 12 开始导通和关断切换，自举电





压 V_{BST} 将被刷新恢复至期望值。

图 5 所示为根据本发明一个实施例的电压转换电路 200 的工作波形示意图。在 t_0 时刻，高侧开关控制信号 S_H 和低侧开关控制信号 S_L 为低电平，高侧开关 11 和低侧开关 12 均关断。此时，电压转换电路 300 的输出电压 V_{OUT} 保持不变，流过开关电路 110 中的电感器 L 的电流 I_L 为零。

在 t_0 至 t_1 时刻，高侧开关控制信号 S_H 和低侧开关控制信号 S_L 保持为低电平，因此高侧开关 11 和低侧开关 12 保持关断状态，流过电感器 L 的电流 I_L 依然为零。由于电压转换电路 300 工作在轻载模式下，因此输出电压 V_{OUT} 基本保持不变。同时，由于低侧开关 12 一直保持关断状态，自举电路 120 中的自举电容 C_B 不能及时被充电，自举电压 V_{BST} 下降。

在 t_1 时刻，当自举电压 V_{BST} 下降至自举电压刷新阈值 V_{TH1} 时，自举电压刷新电路 134 中的第一比较信号 A_S 为高电平信号，自举刷新信号 RFS 为高电平，因此，控制模块 131 控制低侧开关控制信号 S_L 变为高电平，低侧开关 12 导通。

在 t_1 至 t_2 时刻，低侧开关控制信号 S_L 维持在高电平，低侧开关 12 保持导通状态。开关电路 110 中的电容器 C 通过电感器 L 和低侧开关 12 放电，流过电感器 L 的电流 I_L 为一反向升高的电流信号；输出电压 V_{OUT} 随着电容器 C 的放电而降低。与此同时，自举电路 120 中的自举电容 C_B 通过低侧开关 12 电连接至逻辑地，因此自举电容 C_B 被充电，自举电压 V_{BST} 升高。





在 t_2 时刻, 电感电流 I_L 反向增大到第一电流阈值 I_{P1} , 也即是, 在一个实施例中, 自举电压刷新电路 134 中的第二比较器 35 中的电流采样信号 V_{CS} 等于电流阈值信号 V_P (电流阈值信号 V_P 代表第一电流阈值信号 I_{P1}); 第二比较信号 A_R 为高电平, 自举刷新信号 RFS 变为低电平。由于此时第一低侧开关信号 S_{L1} 依然为低电平信号, 因此低侧开关控制信号 S_L 为低电平, 低侧开关 12 关断。此刻, 自举电压 V_{BST} 被充电恢复至第一自举电压值 V_{BST1} 。在其他实施例中, 也可以设定不同的电流阈值信号, 对应地自举电压 V_{BST} 被充电恢复至不同的值。当然, 在图 4 所示的实施例电压转换电路 300 中, 通过设定低侧开关 12 不同的导通时间也可以达到相同的效果。

在 t_2 至 t_3 时刻, 高侧开关 11 和低侧开关 12 均保持关断状态; 电感电流 I_L 通过高侧开关 11 的体二极管 $D1$ 续流, 反向减小; 输出电压 V_{OUT} 继续降低。

在 t_3 时刻, 电感电流 I_L 减小到零, 输出电压 V_{OUT} 基本保持不变。

t_1' 至 t_3' 时刻以及 t_1'' 至 t_3'' 时刻重复 t_1 至 t_3 时刻, 输出电压 V_{OUT} 持续下降。在 t_3'' 时刻, 由于输出电压 V_{OUT} 下降到一定的限值, 开关变换器进入正常工作模式, 高侧开关 11 和低侧开关 12 开始正常的导通和关断切换。此刻, 高侧开关控制信号 S_H 变为高电平, 高侧开关 11 导通。需要说明的是, 在图示实施例中, 为了降低输出电压 V_{OUT} , 低侧开关 12 被导通和关断了三次, 即 t_1 至 t_3 、 t_1' 至 t_3' 、 t_1'' 至 t_3'' 。然而本领域技术人员应该理解, 三次只是示意性地, 在其他实施例中, 可以根据输出电压 V_{OUT} 下降限值的不同, 选择任意导通和关断的次





数。

在 t_3 至 t_4 时刻, 高侧开关控制信号 S_H 保持高电平, 高侧开关 11 保持导通状态, 电感器 L 正向储能, 电感电流 I_L 正向增大, 输出电压 V_{OUT} 升高。与此同时, 自举电压 V_{BST} 继续下降。

在 t_4 时刻, 高侧开关控制信号 S_H 变为低电平, 高侧开关 11 关断; 低侧开关控制信号 S_L 变为高电平, 低侧开关 12 导通。电感电流 I_L 增大到其峰值。

在 t_4 至 t_5 时刻, 高侧开关控制信号 S_H 保持低电平, 高侧开关 11 保持关断状态; 低侧开关控制信号 S_L 保持高电平, 低侧开关 12 保持导通状态; 电感电流 I_L 通过低侧开关 12 续流, 线性下降。自举电容 C_B 通过低侧开关 12 电连接至逻辑地, 因此自举电容 C_B 被充电, 自举电压 V_{BST} 升高。

在 t_5 时刻, 低侧开关控制信号 S_L 变为低电平, 低侧开关 12 关断, 电感电流 I_L 线性下降至 0。自举电压 V_{BST} 恢复至预定值。

图 6 示出了根据本发明一个实施例的控制电压转换电路的方法的流程示意图。如图 6 所示, 控制电压转换电路的方法包括步骤 601-步骤 607。

步骤 601, 检测电压转换电路 (例如 100、200 或 300) 的自举电压, 产生一个自举电压信号 V_{BST} ;

步骤 602, 将自举电压信号 V_{BST} 与一自举电压刷新阈值 V_{TH1} 相比较, 并提供第一比较信号 A_S ;

步骤 603, 判定自举电压 V_{BST} 是否小于自举电压刷新阈值 V_{TH1} ,





如果自举电压 V_{BST} 大于自举电压刷新阈值 V_{TH1} ，则返回步骤 602，

如果自举电压 V_{BST} 小于自举电压刷新阈值 V_{TH1} ，则转至步骤 604；

步骤 604，如果自举电压 V_{BST} 小于自举电压刷新阈值 V_{TH1} ，降低电压转换电路的输出电压 V_{OUT} ；

步骤 605，当输出电压 V_{OUT} 降低，高侧开关 11 和低侧开关 12 开始导通和关断切换以维持输出电压 V_{OUT} 保持不变，一旦低侧开关 12 的导通频率增大，自举电压 V_{BST} 被及时刷新恢复至预定值。

根据本发明一个实施例的控制电压转换电路的方法还可以包括：

步骤 606，检测自举电压，并将自举电压信号 V_{BST} 与自举电压欠压阈值 V_{UVLO} 相比较，以提供自举欠压信号 LOCK。其中，自举电压欠压阈值 V_{UVLO} 小于自举电压刷新阈值 V_{TH1} 。若自举电压信号 V_{BST} 低于自举电压欠压阈值 V_{UVLO} ，自举欠压信号 LOCK 具有第一逻辑状态；若自举电压信号 V_{BST} 高于自举电压欠压阈值信号 V_{UVLO} ，自举欠压信号 LOCK 具有第二逻辑状态。

步骤 607，基于自举欠压信号 LOCK 控制高侧开关 11 和低侧开关 12 的导通与关断。当自举欠压信号 LOCK 具有第一逻辑状态时，将高侧开关 11 和低侧开关 12 关断，使其停止导通与关断切换；当自举欠压信号 LOCK 具有第二逻辑状态时，允许高侧开关 11 和低侧开关 12 进行导通和关断切换。

在一个实施例中，高侧开关 11 和低侧开关 12 具有公共节点 SW，步骤 604 中降低电压转换电路的输出电压 V_{OUT} 包括：在电压转换电路的输出端 OUT 和/或所述公共节点 SW 与地 GND 之间连接一个电





阻 R_1 或电流沉对输出电压 V_{OUT} 放电。

在一个实施例中,步骤 604 中降低电压转换电路的输出电压 V_{OUT} 包括:检测流过低侧开关 12 的电流,产生一个电流采样信号 V_{CS} ;将电流采样信号 V_{CS} 与一电流阈值信号 V_P 比较,提供第二比较信号 A_R ;根据第一比较信号 A_S 和第二比较信号 A_R 提供自举电压刷新信号 RFS ;基于自举电压刷新信号 RFS 控制低侧开关 12 的导通与关断切换以降低输出电压 V_{OUT} ;其中,若自举电压 V_{BST} 低于自举电压刷新阈值 V_{TH1} ,自举电压刷新信号 RFS 具有第一逻辑状态,低侧开关 12 管导通;若电流采样信号 V_{CS} 高于电流刷新阈值 V_{TH1} ,自举电压刷新信号 RFS 具有第二逻辑状态,低侧开 12 关断。

在一个实施例中,步骤 604 中降低电压转换电路的输出电压 V_{OUT} 包括:产生一个恒定导通时间控制信号 C_R ,用于设定一个恒定导通时间;根据第一比较信号 A_S 和恒定导通时间控制信号 C_R 提供自举电压刷新信号 RFS ;基于自举电压刷新信号 RFS 控制低侧开关 12 的导通与关断切换以降低输出电压 V_{OUT} 。其中,当若自举电压 V_{BST} 低于自举电压刷新阈值 V_{TH1} ,自举电压刷新信号 RFS 具有第一逻辑状态,导通低侧开关管 12;当低侧开关导通恒定导通时间之后,自举电压刷新信号 RFS 具有第二逻辑状态,关断低侧开关管 12。

以上对根据本发明各实施例及其变形实施方式的控制电压转换电路的方法及步骤的描述仅为示例性的,并不用于对本发明进行限定。另外,一些公知的控制步骤及所用控制参数等并未给出或者并未详细描述,以使本发明清楚、简明且便于理解。发明所属技术领域的技术





人员应该理解，以上对根据本发明各实施例的控制电压转换电路的方法及步骤的描述中所述使用的步骤编号并不用于表示各步骤的绝对先后顺序，这些步骤并不按照步骤编号顺序实现，而可能采用不同的顺序实现，也可能同时并列地实现，并不仅仅局限于所描述的实施例。

虽然本说明书中以降压型电压转换电路为例对根据本发明各实施例的自举电压刷新控制电路、包含该自举电压刷新控制电路的电压转换电路及其控制方法进行了示意与描述，但这并不意味着对本发明的限定，本领域的技术人员应该理解这里给出的结构及原理也可以适用于具有其它拓扑结构的电压转换电路，例如：升压型电压转换电路、降压-升压型电压转换电路等等。

因此，上述本发明的说明书和实施方式仅仅以示例性的方式对本发明实施例的自举电压刷新控制电路、包含该自举电压刷新控制电路的电压转换电路及其控制方法进行了说明，并不用于限定本发明的范围。对于公开的实施例进行变化和修改都是可能的，其他可行的选择性实施例和对实施例中元件的等同变化可以被本技术领域的普通技术人员所了解。本发明所公开的实施例的其他变化和修改并不超出本发明的精神和保护范围





说明书附图

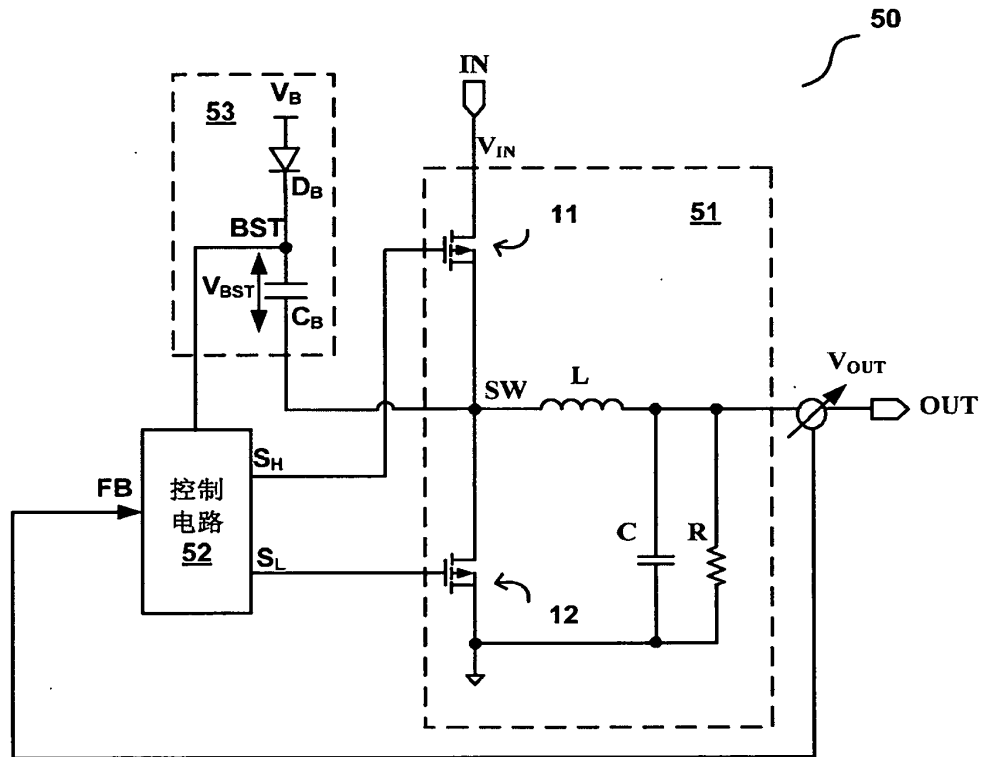


图 1



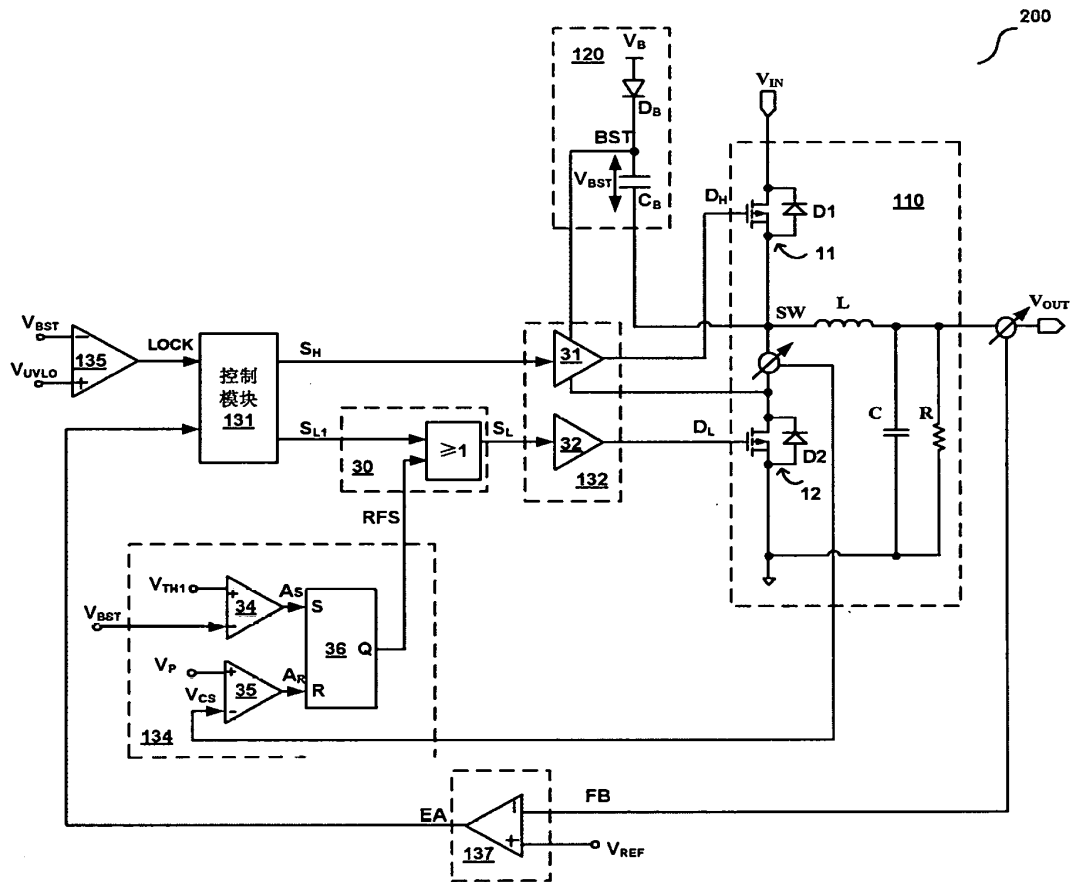


图 3



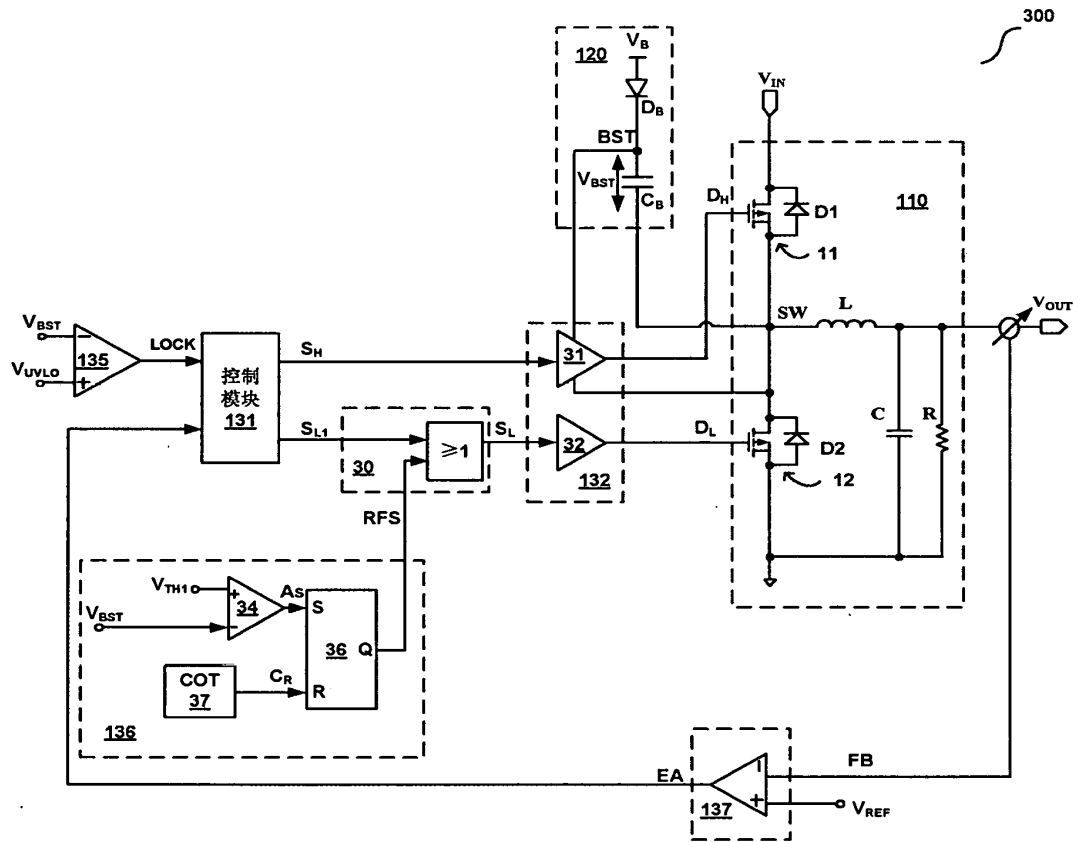


图 4

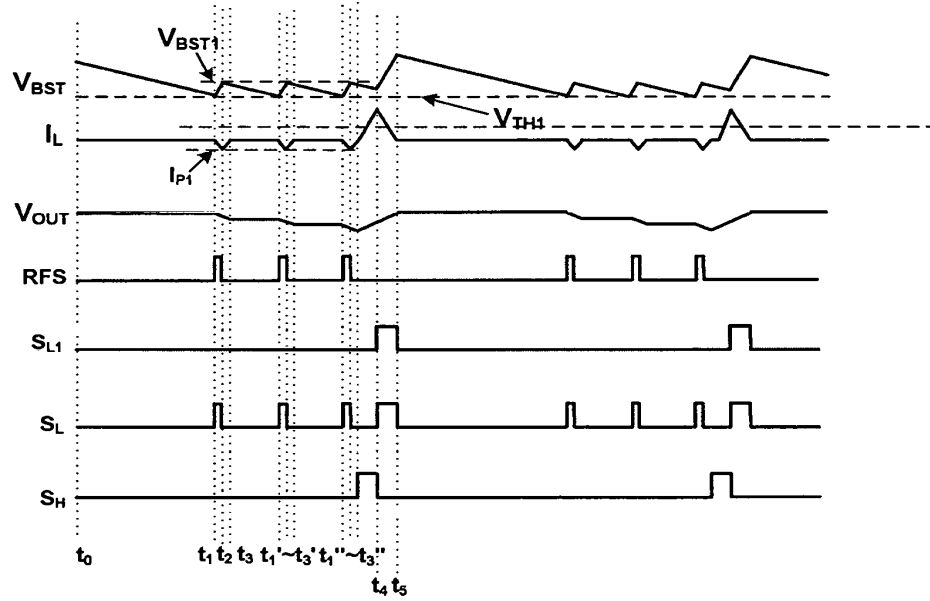


图 5

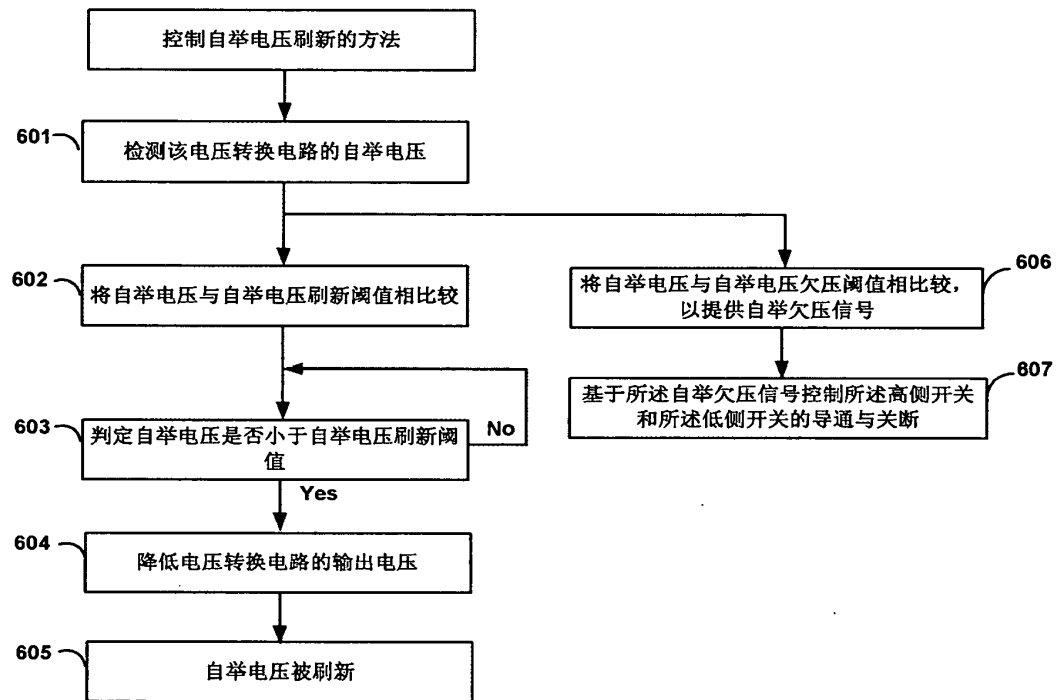
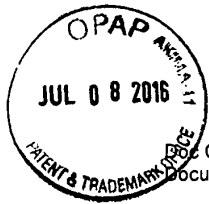


图 6





07-11-16

ITJ

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USED IN LIEU OF PTO/SB/21 (07-09)

TRANSMITTAL FORM (to be used for all correspondence after initial filing)	Application Number	14/823,900	
	Filing Date	August 11, 2015	
	First Named Inventor	Li Xu	
	Art Unit	2838	
	Examiner Name	Adolf D. Berhane	
Total Number of Pages in This Submission	41	Attorney Docket Number	038616-8386.US00

ENCLOSURES (Check all that apply)		
☐ Fee Transmittal Form ☐ Fee Attached ☐ Amendment/Reply ☐ After Final ☐ Affidavits/declaration(s) ☐ Extension of Time Request ☐ Express Abandonment Request ☐ Information Disclosure Statement ☒ Certified Copy of Priority Document(s) ☐ Reply to Missing Parts/Incomplete Application ☐ Reply to Missing Parts under 37 CFR 1.52 or 1.53	☐ Drawing(s) ☐ Licensing-related Papers ☐ Petition ☐ Petition to Convert to a Provisional Application ☐ Power of Attorney, Revocation Change of Correspondence Address ☐ Terminal Disclaimer ☐ Request for Refund ☐ CD, Number of CD(s) _____ ☐ Landscape Table on CD	☐ After Allowance Communication to TC ☐ Appeal Communication to Board of Appeals and Interferences ☐ Appeal Communication to TC (Appeal Notice, Brief, Reply Brief) ☐ Proprietary Information ☐ Status Letter ☒ Other Enclosure(s) (please identify below): Return Receipt Postcard
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SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT			
Firm Name	PERKINS COIE LLP		
Signature	/Chun M. Ng/		
Printed name	Chun M. Ng		
Date	July 8, 2016	Reg. No.	36,878

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the U.S. Postal Service as Priority Mail Express, Airbill No. EM 724269723 US, on the date shown below in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.	
Dated: 7-8-2016	Signature: <u>Pamela Stenslie</u> (Pamela Stenslie)

38616-8386.US00/131860186.1



Docket No.: 038616-8386.US00
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Li Xu

Application No.: 14/823,900

Confirmation No.: 6869

Filed: August 11, 2015

Art Unit: 2838

For: BOOTSTRAP REFRESH CONTROL
CIRCUIT, VOLTAGE CONVERTER AND
ASSOCIATED METHOD

Examiner: Adolf D. Berhane

CLAIM FOR PRIORITY AND SUBMISSION OF DOCUMENTS

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Commissioner:

Applicant hereby claims priority under 35 U.S.C. § 119 based on the following
prior foreign application filed in the following foreign country on the date indicated:

<u>Country</u>	<u>Application No.</u>	<u>Date</u>
China	201410658580.3	November 18, 2014

In support of this claim, a certified copy of said original foreign application is filed
herewith.

Applicant believes no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 50-0665, under Order No. 038616-8386.US00 from which the undersigned is authorized to draw.

Dated: July 8, 2016

Respectfully submitted,

By /Chun M. Ng/
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/823,900	08/11/2015	Li Xu	38616-8386.US00

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IMPROPER CFR REQUEST



OC000000084376542

67394
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SEATTLE, WA 98111-1247

Date Mailed: 07/15/2016

RESPONSE TO REQUEST FOR CORRECTED FILING RECEIPT

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In response to your request for a corrected Filing Receipt, the Office is unable to comply with your request because:

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Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

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67394 7590 10/24/2016
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BERHANE, ADOLF D

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/823,900	08/11/2015	Li Xu	38616-8386.US00	6869

TITLE OF INVENTION: BOOTSTRAP REFRESH CONTROL CIRCUIT, VOLTAGE CONVERTER AND ASSOCIATED METHOD

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	01/24/2017

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or **Fax** **(571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

67394 7590 10/24/2016
Perkins Coie LLP - Monolithic Power Systems
P.O. BOX 1247
SEATTLE, WA 98111-1247

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

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14/823,900	08/11/2015	Li Xu	38616-8386.US00	6869

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APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	01/24/2017

EXAMINER	ART UNIT	CLASS-SUBCLASS
BERHANE, ADOLF D	2838	323-271000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
- 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____



UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/823,900	08/11/2015	Li Xu	38616-8386.US00	6869
67394	7590	10/24/2016	EXAMINER	
Perkins Coie LLP - Monolithic Power Systems P.O. BOX 1247 SEATTLE, WA 98111-1247			BERHANE, ADOLF D	
			ART UNIT	PAPER NUMBER
			2838	

DATE MAILED: 10/24/2016

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 14/823,900	Applicant(s) XU, LI	
	Examiner ADOLF BERHANE	Art Unit 2838	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to papers filed on 8/11/1.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are 1-16. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☒ All b) ☐ Some *c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|--|--|
| 1. ☒ Notice of References Cited (PTO-892) | 5. ☐ Examiner's Amendment/Comment |
| 2. ☒ Information Disclosure Statements (PTO/SB/08),
Paper No./Mail Date _____ | 6. ☒ Examiner's Statement of Reasons for Allowance |
| 3. ☐ Examiner's Comment Regarding Requirement for Deposit
of Biological Material | 7. ☐ Other _____. |
| 4. ☐ Interview Summary (PTO-413),
Paper No./Mail Date _____. | |

/ADOLF BERHANE/
Primary Examiner, Art Unit 2838

DETAILED ACTION

Notice of Pre-AIA or AIA Status

1. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Priority

2. Receipt is acknowledged of certified copies of papers required by 37 CFR 1.55.

Information Disclosure Statement

3. The information disclosure statement (IDS) submitted on 8/11/15 has been considered by the examiner.

Drawings

4. The drawings received on 8/11/15 are acceptable.

Allowable Subject Matter

5. Claims 1-16 are allowed over the cited prior art of record.
6. The following is an examiner's statement of reasons for allowance:

Claim 1 is allowed because the prior art of record fails to disclose or suggest a bootstrap refresh control circuit including the limitation " a voltage difference module having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal of the voltage difference module is configured to receive a feedback signal representing the output voltage of the voltage converter, the second input terminal of the voltage difference module is configured to receive a reference voltage signal representing a desired value of the output voltage of the voltage converter, the voltage difference module is configured to compare the feedback signal with the

reference voltage signal so as to provide a difference signal at the output terminal; and wherein when the first comparing signal has the first logic state, the bootstrap refresh module is configured to decrease the output voltage of the voltage converter; and wherein when the feedback signal is smaller than the reference voltage signal, the bootstrap refresh control circuit is configured to control the high side switch and the low side switch to switch on and off based on the difference signal so as to charge the bootstrap capacitor for refreshing the bootstrap voltage signal" in addition to other limitations recited therein.

Claim 11 is allowed because the prior art of record fails to disclose or suggest a bootstrap refresh control circuit including the limitation" a voltage difference module having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal of the voltage difference module is configured to receive a feedback signal representing the output voltage of the voltage converter, the second input terminal of the voltage difference module is configured to receive a reference voltage signal representing a desired value of the output voltage of the voltage converter, the voltage difference module is configured to compare the feedback signal with the reference voltage signal so as to provide a difference signal at the output terminal; and wherein when the first comparing signal has the first logic state, the bootstrap refresh module is configured to decrease the output voltage of the voltage converter; and wherein when the feedback signal is smaller than the reference voltage signal, the bootstrap refresh control circuit is configured to control the high side switch and the low side switch to switch on and off based on the difference signal so as to charge the

bootstrap capacitor for refreshing the bootstrap voltage signal" in addition to other limitations recited therein.

Claim 12 is allowed because the prior art of record fails to disclose or suggest a bootstrap refresh control circuit including the limitation "comparing the bootstrap voltage with a bootstrap refresh threshold to provide a first comparing signal, wherein the first comparing signal has a first logic state and a second logic state, and wherein the first comparing signal has the first logic state when the bootstrap voltage is lower than the bootstrap refresh threshold, and wherein the first comparing signal has the second logic state when the bootstrap voltage signal is larger than the bootstrap refresh threshold; determining whether the bootstrap voltage signal is smaller than the bootstrap refresh threshold or not; and decreasing the output voltage of the voltage converter by a bootstrap refresh circuit once the bootstrap voltage signal is determined to have dropped to be smaller than the bootstrap refresh threshold; and wherein when the output voltage of the voltage converter is decreased, switching the high side switch and the low side switch on and off so as to refresh the bootstrap voltage signal" in addition to other limitations recited therein.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ADOLF BERHANE whose telephone number is (571)272-2077. The examiner can normally be reached on Monday- Friday 8 AM to 6 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Monica Lewis can be reached on 571-272-1838. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Adolf Berhane/
Adolf Berhane
Primary Examiner
Art Unit 2838

Notice of References Cited	Application/Control No. 14/823,900		Applicant(s)/Patent Under Reexamination XU, LI	
	Examiner ADOLF BERHANE		Art Unit 2838	Page 1 of 2

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-5,365,118 A	11-1994	Wilcox; Milton E.	H02M1/38	327/109
*	B	US-5,705,919 A	01-1998	Wilcox; Milton E.	G05F1/618	323/268
*	C	US-6,396,251 B2	05-2002	Corva; Giulio	H02M3/1588	323/283
*	D	US-6,456,050 B1	09-2002	Agiman; Dan	H02M3/1563	323/282
*	E	US-2005/0231177 A1	10-2005	Tateno, Koji	H02M3/1588	323/225
*	F	US-2010/0001704 A1	01-2010	Williams; Richard K.	H02M3/158	323/283
*	G	US-2010/0315055 A1	12-2010	Miyazaki; Takahiro	H02M1/12	323/283
*	H	US-2011/0127975 A1	06-2011	HOSOKAWA; KYOICHI	H02M3/1588	323/271
*	I	US-2012/0049829 A1	03-2012	Murakami; Kazuhiro	H02M1/32	323/288
*	J	US-2013/0328540 A1	12-2013	Kung; Nien-Hui	H02M3/158	323/311
*	K	US-2015/0008890 A1	01-2015	Sasao; Kazuki	H02M1/08	323/271
*	L	US-2015/0042298 A1	02-2015	Kung; Nien-Hui	H02M3/1588	323/271
*	M	US-2016/0065072 A1	03-2016	Xiu; Liping	H02M1/08	323/271

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Notice of References Cited	Application/Control No. 14/823,900		Applicant(s)/Patent Under Reexamination XU, LI	
	Examiner ADOLF BERHANE		Art Unit 2838	Page 2 of 2

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-2016/0105175 A1	04-2016	ISHIMATSU; Yuji	H03K17/162	327/109
*	B	US-9,312,773 B2	04-2016	Li; Yike	H02M3/1588	1/1
*	C	US-2016/0221332 A1	08-2016	SANO; Takafumi	B41J2/04541	1/1
	D	US-				
	E	US-				
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
 Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Issue Classification 	Application/Control No. 14823900	Applicant(s)/Patent Under Reexamination XU, LI
	Examiner ADOLF BERHANE	Art Unit 2838

CPC					
Symbol				Type	Version
H03K	17	063		F	2013-01-01
H02M	1	08		I	2013-01-01
H02M	3	1588		I	2013-01-01
H03K	2217	0081		A	2013-01-01

CPC Combination Sets				
Symbol	Type	Set	Ranking	Version

NONE		Total Claims Allowed: 16	
(Assistant Examiner)	(Date)		
/ADOLF BERHANE/ Primary Examiner.Art Unit 2838	10/14/2016	O.G. Print Claim(s) 1	O.G. Print Figure 3
(Primary Examiner)	(Date)		

Doc code: IDS

Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)

Approved for use through 07/31/2012. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number			
	Filing Date		2015-08-11	
	First Named Inventor	Li Xu		
	Art Unit		N/A	
	Examiner Name	Not Yet Assigned		
	Attorney Docket Number	0386168386US		

U.S. PATENTS							Remove	
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear		
	1							
If you wish to add additional U.S. Patent citation information please click the Add button.							Add	
U.S. PATENT APPLICATION PUBLICATIONS							Remove	
Examiner Initial*	Cite No	Publication Number	Kind Code ¹	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear		
	1	20150061611	A1	2015-03-05	Li			
If you wish to add additional U.S. Published Application citation information please click the Add button.							Add	
FOREIGN PATENT DOCUMENTS							Remove	
Examiner Initial*	Cite No	Foreign Document Number ³	Country Code ² j	Kind Code ⁴	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear	T ⁵
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If you wish to add additional Foreign Patent Document citation information please click the Add button								Add
NON-PATENT LITERATURE DOCUMENTS							Remove	
Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.						T ⁵

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /A.B./

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number		
Filing Date		2015-08-11
First Named Inventor	Li Xu	
Art Unit	N/A	
Examiner Name	Not Yet Assigned	
Attorney Docket Number	0386168386US	

	1		☐
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If you wish to add additional non-patent literature document citation information please click the Add button **Add**

EXAMINER SIGNATURE

Examiner Signature	/Adolf Berhane/	Date Considered	10/14/2016
--------------------	-----------------	-----------------	------------

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /A.B./

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number		
Filing Date		2015-08-11
First Named Inventor	Li Xu	
Art Unit	N/A	
Examiner Name	Not Yet Assigned	
Attorney Docket Number	0386168386US	

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

- ☐ See attached certification statement.
- ☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.
- ☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Rodney Tullett/	Date (YYYY-MM-DD)	2015-08-11
Name/Print	Rodney C. Tullett	Registration Number	34034

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /A.B./

EAST Search History**EAST Search History (Interference)**

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	0	("bootstrap refresh" AND converter AND comparing AND threshold AND "voltage difference" AND feedback AND "reference voltage" AND "bootstrap capacitor").CLM.	US-PGPUB; USPAT	OR	OFF	2016/10/14 22:00
L2	1	("bootstrap refresh" AND converter AND comparing AND threshold AND "voltage difference" AND feedback AND "reference voltage" AND "bootstrap capacitor").CLM.	US-PGPUB; USPAT	OR	OFF	2016/10/14 22:02
L3	1	("bootstrap refresh" AND "switching circuit" AND comparing AND threshold AND "voltage difference" AND feedback AND "reference voltage" AND "bootstrap capacitor").CLM.	US-PGPUB; USPAT	OR	OFF	2016/10/14 22:02
L4	1	("bootstrap refresh" AND sensing AND comparing AND threshold AND "voltage difference" AND feedback AND "reference voltage" AND "bootstrap capacitor").CLM.	US-PGPUB; USPAT	OR	OFF	2016/10/14 22:03
L5	1	("bootstrap refresh" AND threshold AND "voltage difference" AND feedback AND "reference voltage" AND "bootstrap capacitor").CLM.	US-PGPUB; USPAT	OR	OFF	2016/10/14 22:03
L6	1	("bootstrap refresh" AND threshold AND feedback AND "reference voltage" AND "bootstrap capacitor").CLM.	US-PGPUB; USPAT	OR	OFF	2016/10/14 22:03
L7	1	("bootstrap refresh" AND "reference voltage" AND "bootstrap capacitor").CLM.	US-PGPUB; USPAT	OR	OFF	2016/10/14 22:04

10/ 14/ 2016 10:04:29 PM**C:\ Users\ aberhane\ Documents\ EAST\ Workspaces\ 14725060.wsp**

Search Notes 	Application/Control No. 14823900	Applicant(s)/Patent Under Reexamination XU, LI
	Examiner ADOLF BERHANE	Art Unit 2838

CPC- SEARCHED		
Symbol	Date	Examiner
H02M 3/156, 3/155, 3/1582, 3/1588, 3/157, 3/158	10/14/16	AB
H02M 1/08	10/14/16	AB
H03K 17/063	10/14/16	AB
H03K 2217/0081	10/14/16	AB

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
323	222, 282-285, 351	10/14/16	AB

SEARCH NOTES		
Search Notes	Date	Examiner

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
323	282	10/14/16	AB
H02M	3/156	10/14/16	AB

	/ADOLF BERHANE/ Primary Examiner.Art Unit 2838
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UNITED STATES DEPARTMENT OF COMMERCE
 United States Patent and Trademark Office
 Address: COMMISSIONER FOR PATENTS
 P.O. Box 1450
 Alexandria, Virginia 22313-1450
 www.uspto.gov

BIB DATA SHEET

CONFIRMATION NO. 6869

SERIAL NUMBER 14/823,900	FILING or 371(c) DATE 08/11/2015 RULE	CLASS 323	GROUP ART UNIT 2838	ATTORNEY DOCKET NO. 38616-8386.US00		
APPLICANTS Chengdu Monolithic Power Systems Co., Ltd., Chengdu, CHINA; INVENTORS Li Xu, Chengdu, CHINA; ** CONTINUING DATA ***** ** FOREIGN APPLICATIONS ***** CHINA 201410390708.2 08/11/2014 ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 08/25/2015						
Foreign Priority claimed ☒ Yes ☐ No 35 USC 119(a-d) conditions met ☒ Yes ☐ No Verified and Acknowledged <u>/ADOLF D BERHANE/</u> Examiner's Signature		☐ Met after Allowance Initials	STATE OR COUNTRY CHINA	SHEETS DRAWINGS 6	TOTAL CLAIMS 16	INDEPENDENT CLAIMS 3
ADDRESS Perkins Coie LLP - Monolithic Power Systems P.O. BOX 1247 SEATTLE, WA 98111-1247 UNITED STATES						
TITLE BOOTSTRAP REFRESH CONTROL CIRCUIT, VOLTAGE CONVERTER AND ASSOCIATED METHOD						
FILING FEE RECEIVED 1600	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		☐ All Fees			
			☐ 1.16 Fees (Filing)			
			☐ 1.17 Fees (Processing Ext. of time)			
			☐ 1.18 Fees (Issue)			
			☐ Other _____			
			☐ Credit			

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail

Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

PERKINS COIE LLP
P.O. Box 1247
Seattle, Washington 98111-1247

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being transmitted to the USPTO on the date indicated below.

Tracy Meeker	(Depositor's name)
/Tracy Meeker/	(Signature)
January 20, 2017	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/823,900	08/11/2015	Li Xu	038616-8386.US00	6869

TITLE OF INVENTION: BOOTSTRAP REFRESH CONTROL CIRCUIT, VOLTAGE CONVERTER AND ASSOCIATED METHOD

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960.00	\$0	\$0	\$960.00	01/24/2017

EXAMINER	ART UNIT	CLASS-SUBCLASS
BERHAVE, ADOLF D.	2838	323-271000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1	_____
2	_____
3	_____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY AND STATE OR COUNTRY)

CHENGDU MONOLITHIC POWER SYSTEMS CO., LTD.

CHENGDU, CHINA

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☒ Payment by credit card.
- ☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 50-0665 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ /Chun M. Ng/

Date January 20, 2017

Typed or printed name _____ Chun M. Ng

Registration No. 36,878

Docket No.: 038616-8386.US00
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Li Xu

Application No.: 14/823,900

Confirmation No.: 6869

Filed: August 11, 2015

Art Unit: 2838

For: BOOTSTRAP REFRESH CONTROL
CIRCUIT, VOLTAGE CONVERTER AND
ASSOCIATED METHOD

Examiner: Adolf D. Berhane

COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Commissioner:

In the Notice of Allowability mailed October 24, 2016, the Examiner allowed claims 1-16. Applicant acknowledges Examiner's statements of Reasons for Allowance of the above-referenced patent application and agrees that the claimed subject matter is patentable. However, Applicant takes no position regarding the Reasons for Allowance presented by the Examiner other than the positions Applicant may have previously taken during prosecution. Therefore, the Examiner's Reasons for Allowance should not be attributed to Applicant as an indication of the basis for Applicant's belief that the claims are patentable. Furthermore, Applicant respectfully asserts that there may also be additional reasons for patentability of the claimed subject matter not explicitly stated in this record and Applicant does not waive its rights to such arguments by not further addressing such reasons herein.

134217704.1

Application No.: 14/823,900

Docket No.: 038616-8386.US00

If additional fees are due, please charge our Deposit Account No. 50-0665, under Order No. 0386168386US from which the undersigned is authorized to draw.

Dated: January 20, 2017

Respectfully submitted,

By___/Chun M. Ng/_____
Chun M. Ng
Registration No.: 36,878
PERKINS COIE LLP
P.O. Box 1247
Seattle, Washington 98111-1247
(206) 359-8000
(206) 359-9000 (Fax)
Attorney for Applicant

Electronic Patent Application Fee Transmittal				
Application Number:		14823900		
Filing Date:		11-Aug-2015		
Title of Invention:		BOOTSTRAP REFRESH CONTROL CIRCUIT, VOLTAGE CONVERTER AND ASSOCIATED METHOD		
First Named Inventor/Applicant Name:		Li Xu		
Filer:		Chun Ng/Tracy Meeker		
Attorney Docket Number:		38616-8386.US00		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	960	960

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				960

Electronic Acknowledgement Receipt	
EFS ID:	28126894
Application Number:	14823900
International Application Number:	
Confirmation Number:	6869
Title of Invention:	BOOTSTRAP REFRESH CONTROL CIRCUIT, VOLTAGE CONVERTER AND ASSOCIATED METHOD
First Named Inventor/Applicant Name:	Li Xu
Customer Number:	67394
Filer:	Chun Ng/Tracy Meeker
Filer Authorized By:	Chun Ng
Attorney Docket Number:	38616-8386.US00
Receipt Date:	20-JAN-2017
Filing Date:	11-AUG-2015
Time Stamp:	19:59:41
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	\$960
RAM confirmation Number	012317INTEFSW20003400
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	2017_1_20_Issue_Fee_0386168386US.PDF	108079	no	1
			8dca64f10ba0d65c5ad8a62100d3b1882c6bc4bd		
Warnings:					
Information:					
2	Post Allowance Communication - Incoming	2017_1_20_Comments_on_Reasons_for_Allowance_0386168386US.PDF	69811	no	2
			e07e9ef8bc0c6a41d06d760331d8138037f1d51e		
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	30667	no	2
			e0e14c372332fda81a09024a370efef6aecca b1c4		
Warnings:					
Information:					
Total Files Size (in bytes):			208557		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/823,900	03/07/2017	9590608	38616-8386.US00	6869

67394 7590 02/15/2017
Perkins Coie LLP - Monolithic Power Systems
P.O. BOX 1247
SEATTLE, WA 98111-1247

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 13 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Li Xu, Chengdu, CHINA;
Chengdu Monolithic Power Systems Co., Ltd., Chengdu, CHINA;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.