



1. A bootstrap voltage refresh control circuit, which is used for a voltage conversion circuit, wherein the voltage conversion circuit comprises a high-side switch, a low-side switch, and a bootstrap capacitor for providing a bootstrap voltage for the high-side switch, and the voltage conversion circuit provides an output voltage and an output current on the basis of on and off switching of the high-side switch and the low-side switch, the bootstrap voltage refresh control circuit comprising:

a first comparison module having a first comparison input terminal, a second comparison input terminal, and a first comparison output terminal, wherein the first comparison input terminal is configured to receive the bootstrap voltage, the second comparison input terminal is configured to receive a bootstrap voltage refresh threshold, and the first comparison module is configured to compare the bootstrap voltage with the bootstrap voltage refresh threshold and provide a bootstrap voltage refresh signal at the first comparison output terminal; and

a control module having a first control input terminal configured to receive the bootstrap voltage refresh signal and controlling the on and off switching of the high-side switch and the low-side switch on the basis of the bootstrap voltage refresh signal to control charging of the bootstrap capacitor.

2. The bootstrap voltage refresh control circuit according to claim 1, characterized in that:

the control module further has a second control input terminal and a third control input terminal, wherein the second control input terminal is configured to detect an output voltage of the voltage conversion circuit, and the third control input terminal is configured to detect an output current of the voltage conversion circuit;

if the bootstrap voltage is lower than the bootstrap voltage refresh threshold, the bootstrap voltage refresh signal has a first logic state, and if the bootstrap voltage is higher than the bootstrap voltage refresh threshold, the bootstrap voltage refresh signal has a second logic state; and

if the bootstrap voltage refresh signal has the first logic state, the control module controls, on the basis of the bootstrap voltage refresh signal, the high-side switch and the low-side switch to perform on and off switching in a complementary manner at a substantially constant frequency, so as to charge the bootstrap capacitor; and if the bootstrap voltage refresh signal has the second logic state, the control module controls, on the basis of the bootstrap voltage refresh signal, the high-side switch and the low-side switch to perform on and off switching according to the output voltage and the output current.

3. The bootstrap voltage refresh control circuit according to claim 2, characterized in that:

the bootstrap voltage refresh threshold comprises a first refresh threshold and a second refresh threshold, wherein the first refresh threshold is smaller than the second refresh threshold;

if the bootstrap voltage is lower than the first refresh threshold, the bootstrap voltage refresh signal has the first logic state; and

if the bootstrap voltage is higher than the second refresh threshold, the bootstrap voltage refresh signal has the second logic state.

4. The bootstrap voltage refresh control circuit according to one of claims 1 to 3, characterized in that the control module comprises:

a second comparison module having an enable input terminal, a third comparison input terminal, a fourth comparison input terminal, and a second comparison output terminal, wherein the enable input terminal is configured to receive the bootstrap voltage refresh signal, the third comparison input terminal is configured to receive a load signal representing the output current of the voltage conversion circuit, the fourth comparison input terminal is configured to receive a light load threshold, and the second comparison module is configured to compare the load signal with the light load threshold and provide a load comparison signal at the second comparison output terminal;

if the bootstrap voltage is lower than the bootstrap voltage refresh threshold, the bootstrap voltage refresh signal controls the second comparison module to be disabled; and if the bootstrap voltage is higher than the bootstrap voltage refresh threshold, the bootstrap voltage refresh signal controls the second comparison module to be enabled;

if the second comparison module is enabled, when the load signal is higher than the light load threshold, the load comparison signal has a first logic state, and when the load signal is lower than the light load threshold, the load comparison signal has a second logic state;

if the second comparison module is disabled, the load comparison signal has the first logic state substantially constantly;

if the load comparison signal has the first logic state, the control module controls, on the basis of the load comparison signal, the high-side switch and the low-side switch to perform constant-frequency on and off switching of pulse width modulation; and

if the load comparison signal has the second logic state, the control module controls, on the basis of the load comparison signal, the high-side switch and the low-side switch to perform variable-frequency on and off switching of pulse frequency modulation.

5. The bootstrap voltage refresh control circuit according to claim 4, characterized in that when the load comparison signal has the first logic state, the frequency of the on and off switching of the high-side switch and the low-side switch is a substantially constant first switching frequency; and when the load comparison signal has the second logic state, the frequency of the on and off switching of the high-side switch and the low-side switch is a changing second switching

frequency; wherein the second switching frequency changes according to changes in the load signal.

6. The bootstrap voltage refresh control circuit according to claim 4, characterized in that the control module further comprises:

a pulse width modulation module having a first modulation input terminal, a second modulation input terminal, a third modulation input terminal, and a modulation output terminal, wherein the first modulation input terminal is configured to receive the load comparison signal, the second modulation input terminal is configured to detect the output voltage, the third modulation input terminal is configured to detect the output current, and the modulation output terminal provides a high-side switch control signal and a low-side switch control signal on the basis of the output voltage and the output current; and

the pulse width modulation module adjusts the high-side switch control signal and the low-side switch control signal according to the load comparison signal; when the load comparison signal has the first logic state, the high-side switch control signal and the low-side switch control signal maintain being pulse width modulated or are converted from being pulse frequency modulated to being pulse width modulated, so that the high-side switch and the low-side switch perform constant-frequency on and off switching of pulse width modulation; and when the load comparison signal has the second logic state, the high-side switch control signal and the low-side switch control signal are converted from pulse width modulated to pulse frequency modulated, so that the high-side switch and the low-side switch perform variable-frequency on and off switching of pulse frequency modulation.

7. The bootstrap voltage refresh control circuit according to claim 6, characterized in that:

when the load comparison signal has the first logic state, the pulse width modulation module controls the high-side switch and the low-side switch to perform constant-frequency on and off switching of pulse width modulation; and

when the load comparison signal has the second logic state, the pulse width modulation module controls the high-side switch and the low-side switch to be switched off and stop switching on and off.

8. The bootstrap voltage refresh control circuit according to claim 6, characterized in that the pulse width modulation module comprises:

a pulse width modulated signal generation circuit that receives a first feedback signal representing the output voltage and a second feedback signal representing the output current, and provides a pulse width modulated signal on the basis of the first feedback signal and the second feedback signal;

a switching frequency control circuit that receives the load comparison signal and provides a switching frequency modulated signal on the basis of the load comparison signal, wherein when the load comparison signal has the first logic state, the switching frequency modulated signal has a substantially constant first switching frequency, and when the load comparison signal has the second logic state, the switching frequency modulated signal has a second switching frequency that changes with the load signal; and

a logic control circuit that receives the pulse width modulated signal and the switching frequency modulated signal, and provides the high-side switch control signal and the low-side switch control signal on the basis of the pulse width modulated signal and the switching frequency modulated signal, wherein when the load comparison signal has the first logic state, the high-side switch control signal and the low-side switch control signal are pulse width modulated signals with the first switching frequency and are used to control the high-side switch and the low-side switch to perform constant-frequency on and off switching of pulse width modulation, and when the load comparison signal has the second logic state, the high-side switch control signal and the low-side switch control signal are pulse frequency modulated signals with the second switching frequency, and used to control the high-side switch and the low-side switch to perform variable-frequency on and off switching of pulse frequency modulation.

9. The bootstrap voltage refresh control circuit according to claim 1, characterized in that the bootstrap voltage refresh control circuit further comprises:

a zero-crossing detection module having a first detection input terminal, a second detection input terminal, and a detection output terminal, wherein the first detection input terminal is configured to receive a third feedback signal representing a current flowing through the low-side switch, the second detection input terminal is configured to receive a low-side switch current limiting threshold, and the detection output terminal is configured to provide a zero-crossing comparison signal according to a comparison result between the third feedback signal and the low-side switch current limiting threshold;

when the third feedback signal is higher than the low-side switch current limiting threshold, the zero-crossing comparison signal has a first logic state, and when the third feedback signal is lower than the low-side switch current limiting threshold, the zero-crossing comparison signal has a second logic state; and

when the zero-crossing comparison signal has the first logic state, the bootstrap voltage refresh control circuit allows the low-side switch to perform on and off switching on the basis of the zero-crossing comparison signal, and when the zero-crossing comparison signal has the second logic state, on the basis of the zero-crossing comparison signal, the bootstrap voltage refresh control circuit switches off the low-side switch and causes the low-side switch to stop switching on and off.

10. The bootstrap voltage refresh control circuit according to claim 9, characterized in that the low-side switch current limiting threshold has a set compensation value that is lower than zero and close to zero.

11. The bootstrap voltage refresh control circuit according to claim 1, characterized in that the bootstrap voltage refresh control circuit further comprises:

a bootstrap under-voltage lockout circuit having a first lockout input terminal, a second lockout input terminal, and a lockout output terminal, wherein the first lockout input terminal is configured to receive the bootstrap voltage, the second lockout input terminal is configured to receive a bootstrap voltage under-voltage threshold, the bootstrap voltage under-voltage threshold being less than the bootstrap voltage refresh threshold, and the bootstrap under-voltage lockout circuit is configured to compare the bootstrap voltage with the bootstrap voltage under-voltage threshold and provide a bootstrap under-voltage signal at the lockout output terminal;

if the bootstrap voltage is lower than the bootstrap voltage under-voltage threshold, the bootstrap under-voltage signal has a first logic state, and if the bootstrap voltage is higher than the bootstrap voltage under-voltage threshold, the bootstrap under-voltage signal has a second logic state; and

when the bootstrap under-voltage signal has the first logic state, on the basis of the bootstrap under-voltage signal, the bootstrap voltage refresh control circuit switches off the high-side switch and the low-side switch and stops switching on and off, and when the bootstrap under-voltage signal has the second logic state, on the basis of the bootstrap under-voltage signal, the bootstrap voltage refresh control circuit allows the high-side switch and the low-side switch to perform on and off switching.

12. A voltage conversion circuit, comprising:

an input terminal configured to receive an input voltage;

an output terminal configured to provide an output voltage and an output current;

a high-side switch and a low-side switch coupled in series between the input terminal and a reference ground, a coupling point of the high-side switch and the low-side switch forming a switching voltage output terminal;

an output filter circuit coupled between the switching voltage output terminal and the output terminal and configured to convert a switching voltage at the switching voltage output terminal into the output voltage;

a bootstrap circuit comprising a bootstrap capacitor and coupled to the input terminal and the low-side switch, so that the bootstrap capacitor is charged to generate a bootstrap voltage when the low-side switch is switched on; and

a control circuit that receives the bootstrap voltage, provides enhanced on and off driving signals for the high-side switch on the basis of the bootstrap voltage, and controls charging of the bootstrap capacitor by controlling the on and off switching of the high-side switch and a low-side switch on the basis of the bootstrap voltage.

13. The voltage conversion circuit according to claim 12, characterized in that the control module comprises:

a first comparison module having a first comparison input terminal, a second comparison input terminal, and a first comparison output terminal, wherein the first comparison input terminal is configured to receive the bootstrap voltage, the second comparison input terminal is configured to receive a bootstrap voltage refresh threshold, and the first comparison module is configured to compare the bootstrap voltage with the bootstrap voltage refresh threshold and provide a bootstrap voltage refresh signal at the first comparison output terminal; and

a control module having a first control input terminal configured to receive the bootstrap voltage refresh signal and controlling the on and off switching of the high-side switch and the low-side switch on the basis of the bootstrap voltage refresh signal to control the charging of the bootstrap capacitor.

14. The voltage conversion circuit according to claim 13, characterized in that:

the control module further has a second control input terminal and a third control input terminal, wherein the second control input terminal is configured to detect the output voltage of the voltage conversion circuit, and the third control input terminal is configured to detect the output current of the voltage conversion circuit;

if the bootstrap voltage is lower than the bootstrap voltage refresh threshold, the bootstrap voltage refresh signal has a first logic state, and if the bootstrap voltage is higher than the bootstrap voltage refresh threshold, the bootstrap voltage refresh signal has a second logic state; and

if the bootstrap voltage refresh signal has the first logic state, the control module controls, on the basis of the bootstrap voltage refresh signal, the high-side switch and the low-side switch to perform on and off switching in a complementary manner at a substantially constant frequency, so as to charge the bootstrap capacitor; and if the bootstrap voltage refresh signal has the second logic state, the control module controls, on the basis of the bootstrap voltage refresh signal, the high-side switch and the low-side switch to perform on and off switching according to the output voltage and the output current.

15. The voltage conversion circuit according to claim 13, characterized in that:

the bootstrap voltage refresh threshold comprises a first refresh threshold and a second refresh threshold, wherein the first refresh threshold is smaller than the second refresh threshold;

if the bootstrap voltage is lower than the first refresh threshold, the bootstrap voltage refresh signal has the first logic state; and

if the bootstrap voltage is higher than the second refresh threshold, the bootstrap voltage refresh signal has the second logic state.

16. The bootstrap voltage refresh control circuit according to one of claims 13 to 15, characterized in that the control module comprises:

a second comparison module having an enable input terminal, a third comparison input terminal, a fourth comparison input terminal, and a second comparison output terminal, wherein the enable input terminal is configured to receive the bootstrap voltage refresh signal, the third comparison input terminal is configured to receive a load signal representing the output current of the voltage conversion circuit, the fourth comparison input terminal is configured to receive a light load threshold, and the second comparison module is configured to compare the load signal with the light load threshold and provide a load comparison signal at the second comparison output terminal; further characterized in that:

if the bootstrap voltage is lower than the bootstrap voltage refresh threshold, the bootstrap voltage refresh signal controls the second comparison module to be disabled; and if the bootstrap voltage is higher than the bootstrap voltage refresh threshold, the bootstrap voltage refresh signal controls the second comparison module to be enabled; further characterized in that:

if the second comparison module is enabled, when the load signal is higher than the light load threshold, the load comparison signal has a first logic state, and when the load signal is lower than the light load threshold, the load comparison signal has a second logic state;

if the second comparison module is disabled, the load comparison signal has the first logic state substantially constantly; and further characterized in that:

if the load comparison signal has the first logic state, the control module controls, on the basis of the load comparison signal, the high-side switch and the low-side switch to perform constant-frequency on and off switching of pulse width modulation; and

if the load comparison signal has the second logic state, the control module controls, on the basis of the load comparison signal, the high-side switch and the low-side switch to perform variable-frequency on and off switching of pulse frequency modulation.

17. The voltage conversion circuit according to claim 12, characterized in that the voltage conversion circuit further comprises:

a zero-crossing detection module having a first detection input terminal, a second detection input terminal, and a detection output terminal, wherein the first detection input terminal is configured to receive a third feedback signal representing a current flowing through the low-side

switch, the second detection input terminal is configured to receive a low-side switch current limiting threshold, and the detection output terminal is configured to provide a zero-crossing comparison signal according to a comparison result between the third feedback signal and the low-side switch current limiting threshold; further characterized in that:

when the third feedback signal is higher than the low-side switch current limiting threshold, the zero-crossing comparison signal has a first logic state, and when the third feedback signal is lower than the low-side switch current limiting threshold, the zero-crossing comparison signal has a second logic state; and further characterized in that:

when the zero-crossing comparison signal has the first logic state, the control circuit allows the low-side switch to perform on and off switching on the basis of the zero-crossing comparison signal, and when the zero-crossing comparison signal has the second logic state, on the basis of the zero-crossing comparison signal, the bootstrap voltage refresh control circuit switches off the low-side switch and causes the low-side switch to stop switching on and off.

18. The voltage conversion circuit according to claim 17, characterized in that: the low-side switch current limiting threshold has a set compensation value that is lower than zero and close to zero.

19. A method for controlling a voltage conversion circuit, wherein the voltage conversion circuit has a high-side switch, a low-side switch and a bootstrap capacitor for providing a bootstrap voltage for the high-side switch, and the voltage conversion circuit provides an output voltage and an output current on the basis of on and off switching of the high-side switch and the low-side switch, the method for controlling the voltage conversion circuit comprising:

detecting the bootstrap voltage;

comparing the bootstrap voltage with a bootstrap voltage refresh threshold to provide a bootstrap voltage refresh signal; and

controlling the on and off switching of the high-side switch and the low-side switch on the basis of the bootstrap voltage refresh signal to control charging of the bootstrap capacitor.

20. The method according to claim 19, characterized in that:

if the bootstrap voltage is lower than the bootstrap voltage refresh threshold, the bootstrap voltage refresh signal has a first logic state, and if the bootstrap voltage is higher than the bootstrap voltage refresh threshold, the bootstrap voltage refresh signal has a second logic state; and

if the bootstrap voltage refresh signal has the first logic state, the high-side switch and the low-side switch are caused to perform on and off switching in a complementary manner at a substantially constant frequency, so as to charge the bootstrap capacitor; and if the bootstrap

voltage refresh signal has the second logic state, the high-side switch and the low-side switch are caused to perform on and off switching according to the output voltage and the output current.

BOOTSTRAP VOLTAGE REFRESH CONTROL CIRCUIT, VOLTAGE CONVERSION CIRCUIT AND RELATED CONTROL METHOD

Technical Field

[0001] Embodiments of the present invention relate to power converters, and in particular to refreshing of bootstrap voltages in the power converters.

Background Art

[0002] Power converters such as switch-type voltage converters have been widely used in various industrial electronic equipment and consumer electronic equipment. By taking a buck-type DC voltage converter for example, the buck-type DC voltage converter has relatively high conversion efficiency, wide bandwidth, and easy stability compensation, and is thus often used in applications where a relatively high DC input voltage needs to be converted to a relatively low DC output voltage. Fig. 1 is a simplified schematic diagram showing a typical buck-type DC voltage conversion circuit 50. In brief, the buck-type DC voltage conversion circuit 50 receives an input voltage V_{in} through an input terminal IN and converts the input voltage V_{in} into an appropriate output voltage V_o for outputting at its output terminal OUT through controlling on and off switching of a high-side switch M_{HS} (illustrated as MOSFET in Fig. 1) and a low-side switch M_{LS} (illustrated as MOSFET in Fig. 1) by a control circuit 51. The high-side switch M_{HS} (illustrated as MOSFET in Fig. 1) and the low-side switch M_{LS} are coupled in series between the input terminal IN and a reference ground GND, and a coupling point SW (i.e., a switching voltage output terminal SW) is coupled to the output terminal OUT through an inductive energy storage element L_o . A capacitive energy storage element C_o is coupled between the output terminal OUT and the reference ground GND to smooth the output voltage V_o .

[0003] The high-side switch M_{HS} may include an N-channel power switching device, such as an N-channel FET, an N-channel DMOS or the like, so as to save chip area, reduce the size of the voltage conversion circuit 50, and improve the operation performance of the voltage conversion circuit 50. In this case, in order to enable the high-side switch M_{HS} to be fully switched on (which means causing the M_{HS} to operate in a saturation region in which the M_{HS} has a quite small on-resistance), a voltage difference between a control terminal and a terminal connected to the node SW of the high-side switch M_{HS} must be large enough and is larger than at least an on-threshold voltage of the high-side switch M_{HS} . However, if the high-side switch M_{HS} is switched on, the voltage at the node SW may be an input voltage V_{in} . At this time, it is necessary to provide a voltage higher than that of the SW node for the control terminal of the high-side switch M_{HS} , that is, a voltage higher than the input voltage V_{in} can cause the high-side switch M_{HS} to be fully switched on.

[0004] In order to obtain a voltage higher than the input voltage V_{in} in the buck-type DC voltage conversion circuit 50, the buck-type DC voltage conversion circuit 50 generally further includes a bootstrap circuit 52 configured to provide a bootstrap voltage V_{BST} with the voltage at the node SW as a reference potential. The bootstrap voltage V_{BST} may be used to improve/enhance the

driving capability of a control signal DR_H provided by the control circuit 51 for the control terminal of the high-side switch M_{HS} , thereby controlling on and off of the high-side switch M_{HS} well. In Fig. 1, the bootstrap circuit 52 is illustrated to include a diode DB and a bootstrap capacitor CB and is coupled in series between a bootstrap power supply input terminal VB and a switching voltage output terminal SW, wherein a cathode of the diode DB is coupled to the bootstrap power supply input terminal VB, an anode of the diode DB is coupled to a first terminal of the bootstrap capacitor CB, a second terminal of the bootstrap capacitor CB is coupled to the switching voltage output terminal SW, the bootstrap power supply input terminal VB receives a bootstrap power supply voltage, and the voltage between the first terminal and the second terminal of the bootstrap capacitor CB is the bootstrap voltage V_{BST} . The operating principles of the bootstrap circuit 52 are well known by those of ordinary skill in the art. That is, when the high-side switch M_{HS} is switched off, the low-side switch M_{LS} is switched on, and the bootstrap power supply voltage charges the bootstrap capacitor CB through the diode DB so that there is the bootstrap voltage V_{BST} between the first terminal and the second terminal of the bootstrap capacitor CB. When the high-side switch M_{HS} is switched on, the low-side switch M_{LS} is switched off, and the input voltage V_{in} of the voltage conversion circuit 50 is transmitted to the switching voltage output terminal SW, that is, the voltage at the second terminal of the bootstrap capacitor CB becomes V_{in} . Therefore, at this time, the voltage at the first terminal of the bootstrap capacitor CB is raised to the input voltage V_{in} plus the bootstrap voltage V_{BST} , thereby obtaining a voltage higher than the input voltage V_{in} in the buck-type DC voltage conversion circuit 50. After the voltage at the first terminal of the bootstrap capacitor CB is raised to the input voltage V_{in} plus the bootstrap voltage V_{BST} , the diode DB is reversely biased and is thus switched off so that the power supply providing the bootstrap power supply voltage can be protected from being damaged by the relatively high input voltage V_{in} .

[0005] It can be seen that the bootstrap circuit 52 obtains a chance to charge the bootstrap capacitor CB by pulling down the voltage at the second terminal of the bootstrap capacitor CB to the reference ground when the low-side switch M_{LS} is switched on, so as to provide the bootstrap voltage V_{BST} . However, in certain operating states, the bootstrap capacitor CB may not have sufficient charge and cannot be charged to a sufficient level in time, resulting in a decrease of the bootstrap voltage V_{BST} provided by the bootstrap circuit 52, which is not enough to cause the high-side switch M_{HS} to be normally switched on and off. Therefore, the voltage conversion circuit 50 is also unable to operate normally. For example, if the voltage conversion circuit 50 operates in the case of light load or no load, the control circuit 51 will reduce the on-time and/or the switching frequency of the high-side switch M_{HS} and the low-side switch M_{LS} to improve the conversion efficiency. This may lead to the bootstrap capacitor CB not being able to be charged in time because the on-time of the low-side switch M_{LS} is too short or the high-side switch M_{HS} and the low-side switch M_{LS} do not perform on and off switching in a relatively long time. In addition, if the output voltage V_o of the voltage conversion circuit 50 is close to the input voltage V_{in} , the high-side switch M_{HS} may be required to operate in a quite high duty cycle, even 100% (that is, the on-time of the high-side switch M_{HS} may account for a considerable proportion of the entire

switching cycle, or even the full cycle). Therefore, the on-time of the low-side switch M_{LS} is very short, or the low-side switch M_{LS} does not even have a chance to switch on, so that the bootstrap capacitor CB is unable to be charged in time. In this way, only after the output voltage V_o decreases, the bootstrap capacitor CB has a chance to be charged to recover the bootstrap voltage V_{BST} , which may result in fluctuation spikes in the output voltage V_o . For example, if the input voltage V_{in} is 6 V and the output voltage V_o is 3.3 V, the bootstrap voltage V_{BST} of at least 3 V is enough to allow the high-side switch M_{HS} to be normally switched on and off. In this case, if the output current of the voltage conversion circuit 50 is relatively small or zero (that is, the voltage conversion circuit 50 operates in the case of light load or no load), the bootstrap voltage V_{BST} will inevitably decrease to be lower than 2.7 V, so that the high-side switch M_{HS} is unable to be normally switched on. Therefore, the voltage conversion circuit 50 needs to wait until the output voltage V_o decreases to be lower than 3 V, so that the bootstrap capacitor CB has a chance to be charged, so as to recover the bootstrap voltage V_{BST} to 3 V. Then, the voltage conversion circuit 50 operates normally so that the output voltage V_o returns to a desired value of 3.3 V. Each time the output voltage V_o is recovered from lower than 3 V to 3.3 V, a large fluctuation spike occurs, which is not only detrimental to the voltage conversion circuit 50 but also may damage the load, and is thus undesirable.

Summary of the Invention

[0006] In view of one or more problems in the prior art, embodiments of the present invention provide a bootstrap voltage refresh control circuit, a voltage conversion circuit, and a control method therefor.

[0007] In one aspect of the present invention, a bootstrap voltage refresh control circuit is provided, which is used for a voltage conversion circuit, wherein the voltage conversion circuit may comprise a high-side switch, a low-side switch, and a bootstrap capacitor for providing a bootstrap voltage for the high-side switch, and the voltage conversion circuit provides an output voltage and an output current on the basis of on and off switching of the high-side switch and the low-side switch. According to the embodiments of the present invention, the bootstrap voltage refresh control circuit may comprise: a first comparison module having a first comparison input terminal, a second comparison input terminal, and a first comparison output terminal, wherein the first comparison module receives the bootstrap voltage at the first comparison input terminal thereof, receives a bootstrap voltage refresh threshold at the second comparison input terminal thereof, compares the bootstrap voltage with the bootstrap voltage refresh threshold, and provides a bootstrap voltage refresh signal at the first comparison output terminal thereof; and a control module having a first control input terminal configured to receive the bootstrap voltage refresh signal and controlling the on and off switching of the high-side switch and the low-side switch on the basis of the bootstrap voltage refresh signal to control charging of the bootstrap capacitor.

[0008] In another aspect of the present invention, a voltage conversion circuit is provided. The voltage conversion circuit comprises: an input terminal configured to receive an input voltage; an output terminal configured to provide an output voltage and an output current; a high-side switch

and a low-side switch coupled in series between the input terminal and a reference ground, a coupling point of the high-side switch and the low-side switch forming a switching voltage output terminal; an output filter circuit coupled between the switching voltage output terminal and the output terminal and configured to convert a switching voltage at the switching voltage output terminal into the output voltage; a bootstrap circuit comprising a bootstrap capacitor and coupled to the input terminal and the low-side switch, so that the bootstrap capacitor is charged to generate a bootstrap voltage when the low-side switch is switched on; and a control circuit that receives the bootstrap voltage, provides enhanced on and off driving signals for the high-side switch on the basis of the bootstrap voltage, and controls charging of the bootstrap capacitor by controlling the on and off switching of the high-side switch and a low-side switch on the basis of the bootstrap voltage.

[0009] In still another aspect of the present invention, a method for controlling a voltage conversion circuit is provided, wherein the voltage conversion circuit has a high-side switch, a low-side switch, and a bootstrap capacitor for providing a bootstrap voltage for the high-side switch, and the voltage conversion circuit provides an output voltage and an output current on the basis of on and off switching of the high-side switch and the low-side switch. The method for controlling the voltage conversion circuit may comprises: detecting the bootstrap voltage; comparing the bootstrap voltage with a bootstrap voltage refresh threshold to provide a bootstrap voltage refresh signal; and controlling the on and off switching of the high-side switch and the low-side switch on the basis of the bootstrap voltage refresh signal to control charging of the bootstrap capacitor.

[0010] By using the above solutions, the bootstrap voltage refresh control circuit according to the embodiments of the present invention recovers the bootstrap voltage in time by adjusting the on and off switching of the high-side switch and the low-side switch when the bootstrap voltage is insufficient, without adding more switching devices. The voltage conversion circuit comprising the bootstrap voltage refresh control circuit has good working stability and can still operate normally when its input voltage and output voltage are relatively close, with less power consumption.

Brief Description of the Drawings

[0011] The following accompanying drawings are helpful for a better understanding of the following description of different embodiments of the present invention. The accompanying drawings are not drawn according to actual features, dimensions, and proportions, but schematically show the main features of some implementations of the present invention. The accompanying drawings and implementations provide some embodiments of the present invention in a non-limiting, non-exhaustive manner. For the sake of simplicity, the same or similar components or structures having the same function in different drawings are provided with the same reference numerals.

[0012] Fig. 1 is a simplified schematic diagram showing a typical buck-type DC voltage conversion circuit 50;

[0013] Fig. 2 is a schematic circuit architecture diagram showing a voltage conversion circuit 100 according to an embodiment of the present invention;

[0014] Fig. 3 is a schematic circuit architecture diagram showing a voltage conversion circuit 200 according to an embodiment of the present invention;

[0015] Fig. 4 is a schematic architecture diagram showing a switching frequency control circuit according to an embodiment of the present invention;

[0016] Fig. 5 is a schematic diagram showing main operating waveforms of the voltage conversion circuit 200 shown in Fig. 3 according to an embodiment of the present invention; and

[0017] Fig. 6 is a schematic diagram showing a method for controlling a voltage conversion circuit according to an embodiment of the present invention.

Detailed Description of the Preferred Embodiments

[0018] Some embodiments of the present invention will be described in detail below. In the following description, some specific details, such as specific circuit structures and specific parameters of these circuit elements in the embodiments, are all used to provide a better understanding of the embodiments of the present invention. It will be understood by those skilled in the art that the embodiments of the present invention may be implemented even in the absence of some details or combinations of other methods, elements, materials, etc.

[0019] In the description of the present invention, any reference to "an embodiment" means that the specific features, structures or parameters, steps, etc. described in the embodiment are included in at least one embodiment according to the present invention. Therefore, in the description of the present invention, if the terms such as "according to an embodiment of the present invention" and "in an embodiment" are used, they are not used to specifically refer to the same embodiment. If the terms such as "in other embodiments," "according to different embodiments of the present invention," and "according to other embodiments of the present invention" are used, they are not used to specifically indicate that the mentioned features can only be included in specific different embodiments. It will be understood by those skilled in the art that each specific feature, structure or parameter, step, etc. disclosed in one or more embodiments of the present invention may be combined in any suitable manner. In addition, in the description and claims of the present invention, the word "coupling" means a direct or indirect connection in an electrical or non-electrical manner. "A" is not used to refer specifically to a single form, but may include the plural form. "In" may include the meanings of "in" and "on." Unless specifically stated otherwise, "or" may include the meanings of "or," "and," and "or/and." It does not mean that only one of several parallel features can be selected, but it means that one or several of the features can be selected or a combination of several of the features. Unless otherwise expressly stated, the phrase "on the basis of" is not exclusive, but means that in addition to the explicitly described features, it may also be on the basis of other non-explicitly described features. "Circuit" means a structure in which at least one or more active or passive elements are coupled together to provide a specified function. "Signal" may mean at least a current, a voltage, charge, temperature, data, or other signals. If an embodiment of a "transistor" may include a "field-effect transistor" or a "bipolar junction transistor," then a

"gate/gate region," a "source/source region," and a "drain/drain region" may include a "base/base region," an "emitter/emitter region," and a "collector/collector region," respectively, and vice versa. It will be understood by those skilled in the art that the above-listed explanations of the terms used to describe the present invention are only exemplary and are not intended to be an absolute limitation on the terms.

[0020] Fig. 2 is a schematic circuit architecture diagram showing a voltage conversion circuit 100 according to an embodiment of the present invention. The voltage conversion circuit 100 includes: an input terminal IN configured to receive an input voltage V_{in} ; an output terminal OUT configured to provide an output voltage V_o and an output current I_o ; a high-side switch M_{HS} and a low-side switch M_{LS} coupled in series between the input terminal IN and a reference ground GND, a coupling point of the high-side switch M_{HS} and the low-side switch M_{LS} forming a switching voltage output terminal SW; an output filter circuit 101 coupled between the switching voltage output terminal SW and the output terminal OUT and configured to convert a switching voltage V_{SW} at the switching voltage output terminal SW into the output voltage V_o ; a bootstrap circuit 102 including a bootstrap capacitor CB and coupled to the input terminal IN and the low-side switch M_{LS} , so that the bootstrap capacitor CB is charged to generate a bootstrap voltage V_{BST} when the low-side switch M_{LS} is switched on; and a control circuit 103 that receives the bootstrap voltage V_{BST} , provides enhanced on and off driving signals DR_H for the high-side switch M_{HS} on the basis of the bootstrap voltage V_{BST} , and controls charging of the bootstrap capacitor CB by controlling on and off switching of the high-side switch M_{HS} and the low-side switch M_{LS} on the basis of the bootstrap voltage V_{BST} .

[0021] According to an embodiment of the present invention, the control circuit 103 compares the bootstrap voltage V_{BST} with a bootstrap voltage refresh threshold V_{th1} (a first threshold voltage V_{th1}) and outputs a bootstrap voltage refresh signal RFS. If the bootstrap voltage V_{BST} is lower than the bootstrap voltage refresh threshold V_{th1} , it indicates that the bootstrap voltage V_{BST} is too low, so that the driving capability of the on and off driving signals DR_H provided by the control circuit 103 on the basis of the bootstrap voltage V_{BST} is reduced, and the signals are unable to drive the high-side switch M_{HS} to be normally switched on. At this time, the control circuit 103 controls the high-side switch M_{HS} and the low-side switch M_{LS} to perform on and off switching in a complementary manner at a substantially constant frequency on the basis of the bootstrap voltage refresh signal RFS, which allows the low-side switch M_{LS} to have an appropriate on-time in each switching cycle to charge the bootstrap capacitor CB. In this way, after a certain number of switching cycles, the bootstrap voltage V_{BST} gradually increases until the bootstrap voltage V_{BST} is higher than the bootstrap voltage refresh threshold V_{th1} . If the bootstrap voltage V_{BST} is higher than the bootstrap voltage refresh threshold V_{th1} , it indicates that the bootstrap voltage V_{BST} is large enough and the control circuit 103 is able to provide enhanced on and off driving signals DR_H on the basis of the bootstrap voltage V_{BST} , so as to drive the high-side switch M_{HS} to be fully switched on. At this time, the control circuit 103 controls the high-side switch M_{HS} and the low-side switch M_{LS} on the basis of the bootstrap voltage refresh signal RFS to perform on and off

switching according to the output voltage V_o and the load state (such as heavy load, light load, no load, etc.) of the output terminal OUT.

[0022] According to an embodiment of the present invention, if the bootstrap voltage V_{BST} is higher than the bootstrap voltage refresh threshold V_{th1} , the control circuit 103 controls the high-side switch M_{HS} and the low-side switch M_{LS} on the basis of the bootstrap voltage refresh signal RFS to perform on and off switching according to the output voltage V_o and the output current I_o . This is because the output current I_o can actually represent the load state of the output terminal OUT. The larger the output current I_o is, the heavier the load of the output terminal OUT is. The smaller the output current I_o is, the lighter the load of the output terminal OUT is. For example, if the output current I_o is larger, it indicates that the load of the output terminal OUT is heavier. If the output current I_o is smaller, it indicates that the load of the output terminal OUT is lighter. If the output current I_o is zero, it indicates that the load of the output terminal OUT is no-load.

[0023] Therefore, according to the various exemplary embodiments and variant implementations thereof described on the basis of Fig. 2 of the present invention, the control circuit 103 controls the on and off switching of the high-side switch M_{HS} and the low-side switch M_{LS} on the basis of the bootstrap voltage V_{BST} to control the charging of the bootstrap capacitor CB, thereby ensuring that the bootstrap voltage V_{BST} is large enough, so that the control circuit 103 is able to provide enhanced on and off driving signals DR_H on the basis of the bootstrap voltage V_{BST} to drive the high-side switch M_{HS} to be fully switched on. Since the control circuit 103 controls the on and off switching of the high-side switch M_{HS} and the low-side switch M_{LS} on the basis of the bootstrap voltage V_{BST} , the on and off switching of the high-side switch M_{HS} and the low-side switch M_{LS} can be adjusted in time according to the state of the bootstrap voltage V_{BST} (for example, adjusting the on-time and the frequency of on and off switching of the high-side switch M_{HS} and low-side switch M_{LS}), thereby charging the bootstrap capacitor CB in time when the bootstrap voltage V_{BST} is too low, so that the bootstrap voltage V_{BST} is able to be recovered in time. Moreover, according to various embodiments of the present invention, the bootstrap capacitor CB can be charged in time by adjusting the on and off switching of the high-side switch M_{HS} and the low-side switch M_{LS} on the basis of the bootstrap voltage V_{BST} , without adding more switching devices and corresponding control circuits, so as to ensure that the bootstrap voltage V_{BST} is able to be used to enhance on and off driving of the high-side switch M_{HS} .

[0024] According to various exemplary embodiments and variant implementations thereof described on the basis of Fig. 2 of the present invention, the control circuit 103 detects the bootstrap voltage V_{BST} and determines whether the bootstrap voltage V_{BST} is too low or not by comparing the bootstrap voltage V_{BST} with the bootstrap voltage refresh threshold V_{th1} . If the bootstrap voltage V_{BST} is too low (that is, it is lower than the bootstrap voltage refresh threshold V_{th1}), regardless of the load state of the voltage conversion circuit 100, such as heavy load, light load, or no load, the control circuit 103 controls the high-side switch M_{HS} and the low-side switch M_{LS} to perform on and off switching in a complementary manner at a substantially constant frequency, so that the low-side switch M_{LS} has an appropriate on-time in each switching cycle, thereby charging the bootstrap capacitor CB. If the bootstrap voltage V_{BST} is normal (that is, it is higher than the

bootstrap voltage refresh threshold V_{th1}), the control circuit 103 controls the high-side switch M_{HS} and the low-side switch M_{LS} to perform on and off switching according to the output voltage V_o and the load of the output terminal OUT. For example, according to an embodiment of the present invention, if the bootstrap voltage V_{BST} is higher than the bootstrap voltage refresh threshold V_{th1} , when the load of the output terminal OUT is relatively heavy or normal, the control circuit 103 controls the high-side switch M_{HS} and the low-side switch M_{LS} to perform substantially-constant-frequency on and off switching of pulse width modulation according to the output voltage V_o and the load of the output terminal OUT. When the load of the output terminal OUT is relatively light or no-load, the control circuit 103 controls the high-side switch M_{HS} and the low-side switch M_{LS} to perform variable-frequency on and off switching of pulse frequency modulation according to the output voltage V_o and the load state of the output terminal OUT, so as to reduce the switching frequency of the high-side switch M_{HS} and the low-side switch M_{LS} , thereby reducing the power consumption of the voltage conversion circuit 100.

[0025] According to an embodiment of the present invention, the bootstrap voltage refresh threshold V_{th1} (a first threshold V_{th1}) may include a first refresh threshold V_{th1L} and a second refresh threshold V_{th1H} , wherein the first refresh threshold V_{th1L} is smaller than the second refresh threshold V_{th1H} . If the bootstrap voltage V_{BST} is lower than the first refresh threshold V_{th1L} , the control circuit 103 controls, on the basis of the bootstrap voltage refresh signal RFS, the high-side switch M_{HS} and the low-side switch M_{LS} to perform on and off switching in a complementary manner at a substantially constant frequency. If the bootstrap voltage V_{BST} is higher than the second refresh threshold V_{th1H} , the control circuit 103 controls, on the basis of the bootstrap voltage refresh signal RFS, the high-side switch M_{HS} and the low-side switch M_{LS} to perform on and off switching according to the output voltage V_o and the load state of the output terminal OUT. In this way, there is a certain hysteresis between the first refresh threshold V_{th1L} and the second refresh threshold V_{th1H} , which can avoid false triggering caused by small fluctuations in the bootstrap voltage V_{BST} , thereby improving the operating stability of the voltage conversion circuit 100.

[0026] According to an embodiment of the present invention, the bootstrap capacitor CB is coupled between the input terminal IN and the switching voltage output terminal SW and is configured to generate the bootstrap voltage V_{BST} with the switching voltage V_{SW} at the switching voltage output terminal SW as a reference potential. When the low-side switch M_{LS} is switched on, the bootstrap capacitor CB is charged to refresh the bootstrap voltage V_{BST} .

[0027] According to an embodiment of the present invention, the bootstrap circuit 102 may further include a bootstrap switch DB coupled between the input terminal IN and the bootstrap capacitor CB. The bootstrap switch DB and the low-side switch M_{LS} are switched on and off synchronously. When the low-side switch M_{LS} is switched on, the bootstrap switch DB is switched on, providing a charging path from the input terminal IN to the reference ground GND for the bootstrap capacitor CB. When the low-side switch M_{LS} is switched off, the bootstrap switch DB is switched off to ensure the safety of the charging path of the bootstrap capacitor CB. In the illustrative embodiment of Fig. 2, the bootstrap switch DB is illustrated as including a diode DB.

However, it should be understood by those of ordinary skill in the art that the implementation of the bootstrap switch DB is not limited to the diode, and the bootstrap switch DB may also include MOSFET, JFET, BJT or other controllable switching devices. In this case, the control circuit 103 may provide a switch control signal for the bootstrap switch DB to drive it to switch on and off synchronously with the low-side switch M_{LS} .

[0028] According to an embodiment of the present invention, the bootstrap circuit 102 may further include a bootstrap power supply regulating module BSTREG coupled to the input terminal IN and the bootstrap capacitor CB and configured to regulate the input voltage V_{in} to an appropriate bootstrap charging power supply voltage VB, so as to charge the bootstrap capacitor CB. In this way, the maximum value of the bootstrap voltage V_{BST} obtained by charging the bootstrap capacitor CB may be limited to the bootstrap charging power supply voltage VB. For example, if the input voltage V_{in} is 12 V and it is desirable to obtain a bootstrap voltage V_{BST} of 5 V, the input voltage V_{in} of 12 V may be regulated to a bootstrap charging power supply voltage of 5 V by the bootstrap power supply regulating module BSTREG to charge the bootstrap capacitor CB. According to an embodiment of the present invention, the bootstrap power supply regulating module BSTREG includes a low dropout voltage regulator.

[0029] According to an embodiment of the present invention, the control circuit 103 may include a first comparison module 104. The first comparison module 104 has a first comparison input terminal, a second comparison input terminal, and a first comparison output terminal, receives the bootstrap voltage V_{BST} at the first comparison input terminal, receives the bootstrap voltage refresh threshold V_{th1} at the second comparison input terminal, and compares the bootstrap voltage V_{BST} with the bootstrap voltage refresh threshold V_{th1} (the first threshold voltage V_{th1}) so that the bootstrap voltage refresh signal RFS is provided at the first comparison output terminal. If the bootstrap voltage V_{BST} is lower than the bootstrap voltage refresh threshold V_{th1} , the bootstrap voltage refresh signal RFS has a first logic state (such as a high-level logic state). If the bootstrap voltage V_{BST} is higher than the bootstrap voltage refresh threshold V_{th1} , the bootstrap voltage refresh signal RFS has a second logic state (such as a low-level logic state).

[0030] According to an embodiment of the present invention, the bootstrap voltage refresh threshold V_{th1} (the first threshold V_{th1}) may include a first refresh threshold V_{th1L} and a second refresh threshold V_{th1H} , wherein the first refresh threshold V_{th1L} is smaller than the second refresh threshold V_{th1H} . If the bootstrap voltage V_{BST} is lower than the first refresh threshold V_{th1L} , the bootstrap voltage refresh signal RFS has the first logic state (such as the high-level logic state). If the bootstrap voltage V_{BST} is higher than the second refresh threshold V_{th1H} , the bootstrap voltage refresh signal RFS has the second logic state (such as the low-level logic state). In this way, there is a certain hysteresis between the first refresh threshold V_{th1L} and the second refresh threshold V_{th1H} , which can avoid false triggering caused by small fluctuations in the bootstrap voltage V_{BST} .

[0031] According to an embodiment of the present invention, the control circuit 103 may further include a control module 105 having a first control input terminal configured to receive the bootstrap voltage refresh signal RFS. The control module 105 controls on and off switching of the

high-side switch M_{HS} and the low-side switch M_{LS} on the basis of the bootstrap voltage refresh signal RFS to control the charging of the bootstrap capacitor CB.

[0032] According to an embodiment of the present invention, the control module 105 further has a second control input terminal and a third control input terminal, wherein the second control input terminal is configured to detect the output voltage V_o , and the third control input terminal is configured to detect the output current I_o representing the load state of the output terminal OUT. The control module 105 provides a high-side switch control signal SH and a low-side switch control signal SL on the basis of the bootstrap voltage refresh signal RFS, the output voltage V_o , and the output current I_o . When the bootstrap voltage refresh signal RFS has the first logic state, the high-side switch control signal SH and the low-side switch control signal SL provided by the control module 105 are used to control the high-side switch M_{HS} and the low-side switch M_{LS} to perform on and off switching in a complementary manner at a substantially constant frequency, so that the low-side switch M_{LS} has an appropriate on-time in each switching cycle to charge the bootstrap capacitor CB. When the bootstrap voltage refresh signal RFS has the second logic state, the high-side switch control signal SH and the low-side switch control signal SL provided by the control module 105 are used to control the high-side switch M_{HS} and the low-side switch M_{LS} to perform on and off switching according to the output voltage V_o and the output current I_o .

[0033] According to an embodiment of the present invention, the control module 105 may detect the output current I_o by detecting a current I_{LO} flowing through an output inductor L_o or a current I_H flowing through the high-side switch M_{HS} to provide a signal representing the load state of the output terminal OUT, i.e., a load signal V_{load} .

[0034] According to an embodiment of the present invention, the control circuit 103 may further include a driving module 106 that receives the bootstrap voltage V_{BST} , the high-side switch control signal SH and the low-side switch control signal SL, and on the basis of the bootstrap voltage V_{BST} and the high-side switch control signal SH, provides an enhanced high-side switch driving signal DR_H for driving the high-side switch M_{HS} to switch on and off, and at the same time, on the basis of the low-side switch control signal SL, provides an enhanced low-side switch driving signal DR_L for driving the low-side switch M_{LS} to switch on and off.

[0035] According to an embodiment of the present invention, the driving module 106 may include a high-side switch driver 106_H and a low-side switch driver 106_L. The high-side switch driver 106_H receives the bootstrap voltage V_{BST} and the high-side switch control signal SH, and on the basis of the bootstrap voltage V_{BST} and the high-side switch control signal SH, provides an enhanced high-side switch driving signal DR_H for driving the high-side switch M_{HS} to switch on and off. The low-side switch driver 106_L receives the low-side switch control signal SL, and on the basis of the low-side switch control signal SL, provides an enhanced low-side switch driving signal DR_L for driving the low-side switch M_{LS} to switch on and off. According to an embodiment of the present invention, the high-side switch driver 106_H may include one or more inverters, and the bootstrap voltage V_{BST} is used as a power supply for the one or more inverters. Similarly, the low-side switch driver 106_L may also include one or more inverters.

[0036] According to an embodiment of the present invention, the control circuit 103 may further include a bootstrap under-voltage lockout circuit 107 having a first lockout input terminal, a second lockout input terminal, and a lockout output terminal. The first lockout input terminal is used to receive the bootstrap voltage V_{BST} , and the second lockout input terminal is used to receive a bootstrap voltage under-voltage threshold V_{th2} (a second threshold voltage V_{th2}). The bootstrap under-voltage lockout circuit is configured to compare the bootstrap voltage V_{BST} with the bootstrap voltage under-voltage threshold V_{th2} and provide a bootstrap under-voltage signal LOCK at the lockout output terminal. If the bootstrap voltage V_{BST} is lower than the bootstrap voltage under-voltage threshold V_{th2} , the bootstrap under-voltage signal LOCK has a first logic state (such as a high-level logic state). At this time, the control circuit 103 controls the high-side switch M_{HS} and the low-side switch M_{LS} to be switched off and stop switching on and off. If the bootstrap voltage V_{BST} is higher than the bootstrap voltage under-voltage threshold V_{th2} , the bootstrap under-voltage signal LOCK has a second logic state (such as a low-level logic state). At this time, the control circuit 103 is allowed to control the high-side switch M_{HS} and the low-side switch M_{LS} to perform on and off switching. According to an embodiment of the present invention, the bootstrap voltage under-voltage threshold V_{th2} is smaller than the bootstrap voltage refresh threshold V_{th1} . The bootstrap under-voltage lockout circuit 107 is helpful to switch off both the high-side switch M_{HS} and the low-side switch M_{LS} when the bootstrap voltage V_{BST} has been lower than the bootstrap voltage under-voltage threshold V_{th2} and failed to be refreshed in time (that is, the bootstrap capacitor CB failed to be charged in time, so that the bootstrap voltage V_{BST} is recovered to be higher than the bootstrap voltage under-voltage threshold V_{th2}), so as to improve the operating safety performance of the voltage conversion circuit 100.

[0037] Fig. 3 is a schematic circuit architecture diagram showing a voltage conversion circuit 200 according to an embodiment of the present invention. For the sake of simplicity and ease of understanding, the same or similar components or structures in the voltage conversion circuit 200 that are functionally the same as in the voltage conversion circuit 100 are also provided with the same reference numerals.

[0038] As shown in Fig. 3, according to an embodiment of the present invention, the control module 105 may include a second comparison module 201 having a third comparison input terminal, a fourth comparison input terminal, and a second comparison output terminal. The third comparison input terminal is configured to receive the load signal V_{load} representing the output current I_o (i.e., representing the load state of the output terminal OUT), and the fourth comparison input terminal is configured to receive a light load threshold V_{th3} (a third threshold voltage V_{th3}). The second comparison module is configured to compare the load signal V_{load} with the light load threshold V_{th3} and provide a load comparison signal CMP at the second comparison output terminal. If the load signal V_{load} is higher than the light load threshold V_{th3} , it indicates that the voltage conversion circuit 200 is operating in a non-light load and non-no-load state. At this time, the load comparison signal CMP has a first logic state (such as a high-level logic state). If the load signal V_{load} is lower than the light load threshold V_{th3} , it indicates that the voltage conversion

circuit 200 is operating in a light load or no-load state. At this time, the load comparison signal CMP has a second logic state (such as a low-level logic state).

[0039] According to an embodiment of the present invention, if the load comparison signal CMP has the first logic state (that is, the load signal V_{load} is higher than the light load threshold V_{th3} , and the load state of the output terminal OUT is not light-load and no-load), then the control circuit 103 controls, on the basis of the load comparison signal CMP, the high-side switch M_{HS} and the low-side switch M_{LS} to operate in a constant-frequency on and off switching mode of pulse width modulation (PWM). If the load comparison signal CMP has the second logic state (that is, the load signal V_{load} is lower than the light load threshold V_{th3} , and the load state of the output terminal OUT is light-load or no-load), the control circuit 103 controls, on the basis of the load comparison signal CMP, the high-side switch M_{HS} and the low-side switch M_{LS} to operate in a variable-frequency on and off switching mode of pulse frequency modulation (PFM). According to an embodiment of the present invention, if the load comparison signal CMP has the first logic state, when the high-side switch M_{HS} and the low-side switch M_{LS} operate in the constant-frequency switching mode of pulse width modulation (PWM), the on and off switching frequency of the high-side switch M_{HS} and the low-side switch M_{LS} is substantially a constant first switching frequency F_c . If the load comparison signal CMP has the first logic state, when the high-side switch M_{HS} and the low-side switch M_{LS} operate in the variable frequency switching mode of pulse frequency modulation (PFM), the on and off switching frequency of the high-side switch M_{HS} and the low-side switch M_{LS} is a changing second switching frequency F_s , which changes according to the load state of the output terminal OUT, that is, according to the change of the load signal V_{load} . The smaller the load of the output terminal OUT (for example, the smaller the load signal V_{load}), the smaller the second switching frequency F_s , so as to reduce the power consumption of the voltage conversion circuit 200 in the case of light load or no load (that is, when the load signal V_{load} is lower than the light load threshold V_{th3}).

[0040] According to an embodiment of the present invention, the second comparison module 201 further has an enable input terminal configured to receive the bootstrap voltage refresh signal RFS, and the bootstrap voltage refresh signal RFS is used to control the second comparison module 201 to be enabled or disabled. When the bootstrap voltage refresh signal RFS has the first logic state (that is, the bootstrap voltage V_{BST} is lower than the bootstrap voltage refresh threshold V_{th1}), the second comparison module 201 is not enabled, and the load comparison signal CMP output thereby has the first logical state substantially constantly. When the bootstrap voltage refresh signal RFS has the second logic state (that is, the bootstrap voltage V_{BST} is higher than the bootstrap voltage refresh threshold V_{th1}), the second comparison module 201 is enabled, and the load comparison signal CMP output thereby has the first logic state or the second logic state according to a comparison result between the load signal V_{load} representing the load state of the output terminal OUT and the light load threshold V_{th3} . In this way, if the bootstrap voltage V_{BST} is lower than the bootstrap voltage refresh threshold V_{th1} , the bootstrap voltage refresh signal RFS will disable the second comparison module 201. Even if the load signal V_{load} has been lower than the light load threshold V_{th3} (that is, the load state of the output terminal OUT is light-load or no-

load), the load comparison signal CMP output by the second comparison module 201 still has the first logic state. The control circuit 103 will control the high-side switch M_{HS} and the low-side switch M_{LS} to operate in a constant-frequency on and off switching mode of pulse width modulation (PWM), and the high-side switch M_{HS} and the low-side switch M_{LS} will perform on and off switching periodically in a complementary manner at a substantially constant frequency (such as the first frequency F_C), so that the low-side switch M_{HS} has an appropriate on-time in each switching cycle to charge the bootstrap capacitor CB. Until the amount of charge on the bootstrap capacitor CB is charged enough so that the bootstrap voltage V_{BST} is refreshed higher than the bootstrap voltage refresh threshold V_{th1} , the bootstrap voltage refresh signal RFS enables the second comparison module 201, and the control circuit 103 controls, according to the comparison result (i.e., the load comparison signal CMP) of the load signal V_{load} and the light load threshold V_{th3} , the high-side switch M_{HS} and the low-side switch M_{LS} to operate in the variable-frequency switching mode of pulse frequency modulation (PFM) or the constant-frequency switching mode of pulse width modulation (PWM).

[0041] According to an exemplary embodiment of the present invention, when the bootstrap voltage refresh signal RFS has the first logic state, it controls the light load threshold V_{th3} to decrease (for example, the light load threshold V_{th3} is controlled to be coupled to the reference ground GND), so that the second comparison module 201 is disabled, and the load comparison signal CMP output by the second comparison module 201 has the first logic state substantially constantly. When the bootstrap voltage refresh signal RFS has the second logic state, it controls the light load threshold V_{th3} to recover so that the second comparison module 201 is enabled, and the load comparison signal CMP output by the second comparison module 201 has the first logic state or the second logic state according to the comparison result between the load signal V_{load} and the light load threshold V_{th3} .

[0042] According to an embodiment of the present invention, the control module 105 may further include a pulse width modulation module 202 having a first modulation input terminal, a second modulation input terminal, a third modulation input terminal, and a modulation output terminal, wherein the first modulation input terminal is configured to receive the load comparison signal CMP, the second modulation input terminal is configured to detect the output voltage V_o , the third modulation input terminal is configured to detect the output current I_o , and the modulation output terminal provides, on the basis of the output voltage V_o and the output current I_o , a high-side switch control signal SH and a low-side switch control signal SL which are pulse width modulated.

[0043] According to an embodiment of the present invention, the pulse width modulation module 202 also adjusts, according to the load comparison signal CMP, the high-side switch control signal SH and the low-side switch control signal SL which are pulse width modulated. When the load comparison signal CMP has the first logic state (that is, the load signal V_{load} is higher than the light load threshold V_{th3}), the high-side switch control signal SH and the low-side switch control signal SL maintain being pulse width modulated or are converted from being pulse frequency modulated to being pulse width modulated, so that the high-side switch M_{HS} and low-

side switch M_{LS} perform constant-frequency on and off switching of pulse width modulation. When the load comparison signal CMP has the second logic state (that is, the load signal V_{load} is lower than the light load threshold V_{th3}), the high-side switch control signal SH and the low-side switch control signal SL are converted from being pulse width modulated to being pulse frequency modulated, so that the high-side switch M_{HS} and the low-side switch M_{LS} perform variable-frequency on and off switching of pulse frequency modulation.

[0044] According to an embodiment of the present invention, when the load comparison signal CMP has the first logic state (that is, the load signal V_{load} is higher than the light load threshold V_{th3}), the pulse width modulation module 202 causes the high-side switch control signal SH and the low-side switch control signal SL to control the high-side switch M_{HS} and the low-side switch M_{LS} to maintain/recover constant-frequency on and off switching of pulse width modulation. When the load comparison signal CMP has the second logic state (that is, the load signal V_{load} is lower than the light load threshold V_{th3}), the pulse width modulation module 202 causes the high-side switch control signal SH and the low-side switch control signal SL to control the high-side switch M_{HS} and the low-side switch M_{LS} to switch off and stop switching on and off. In this way, the pulse width modulation module 202 realizes the conversion of the high-side switch control signal SH and the low-side switch control signal SL between being pulse width modulated and being pulse frequency modulated according to the load comparison signal CMP, thereby realizing the control of the conversion of the high-side switch M_{HS} and the low-side switch M_{LS} between constant-frequency on and off switching of pulse width modulation and variable-frequency on and off switching of pulse frequency modulation.

[0045] According to an embodiment of the present invention, the pulse width modulation module 202 may include a pulse width modulated signal generation circuit 203, a switching frequency control circuit 204, and a logic control circuit 205. The pulse width modulated signal generation circuit 203 receives a first feedback signal V_{FB} representing the output voltage V_o and a second feedback signal V_{cs1} representing the load current of the output terminal OUT and provides a pulse width modulated signal C_{PWM} on the basis of the first feedback signal V_{FB} and the second feedback signal V_{cs1} . The switching frequency control circuit 204 receives the load comparison signal CMP output by the second comparison module 201 and provides a switching frequency modulated signal Clk on the basis of the load comparison signal CMP. When the load comparison signal CMP has the first logic state, the switching frequency modulated signal Clk has a substantially constant first switching frequency F_C . When the load comparison signal CMP has the second logic state, the switching frequency modulated signal Clk has a second switching frequency F_s that changes with the load signal V_{load} representing the load state of the output terminal OUT. The logic control circuit 205 receives the pulse width modulated signal C_{PWM} and the switching frequency modulated signal Clk and provides the high-side switch control signal SH and the low-side switch control signal SL on the basis of the pulse width modulated signal C_{PWM} and the switching frequency modulated signal Clk. When the load comparison signal CMP has the first logic state, the high-side switch control signal SH and the low-side switch control signal SL are pulse width modulated signals with a substantially constant first switching frequency F_C for

controlling the high-side switch M_{HS} and the low-side switch M_{LS} to perform constant-frequency on and off switching of pulse width modulation. When the load comparison signal CMP has the second logic state, the high-side switch control signal SH and the low-side switch control signal SL are pulse frequency modulated signals with a second switching frequency F_s that changes with the load state of the output terminal OUT (i.e., with the load signal V_{load}), which are used to control the high-side switch M_{HS} and the low-side switch M_{LS} to perform variable-frequency on and off switching of pulse frequency modulation.

[0046] According to an exemplary embodiment of the present invention, the pulse width modulated signal generation circuit 203 may include an error amplifier 206 and a pulse width modulation comparator 207. A first input terminal of the error amplifier 206 (for example, terminal "-" illustrated in Fig. 3) receives a first feedback signal V_{FB} representing the output voltage V_o , a second input terminal (for example, terminal "+" illustrated in Fig. 3) of the error amplifier receives a reference voltage V_{ref} representing a desired value of the output voltage V_o , and an output terminal of the error amplifier is configured to provide a difference amplified signal V_e representing the difference between the output voltage V_o and the desired value thereof. A first input terminal (for example, terminal "-" illustrated in Fig. 3) of the pulse width modulation comparator 207 receives the difference amplified signal V_e , a second input terminal (for example, terminal "+" illustrated in Fig. 3) of the pulse width modulation comparator receives a second feedback signal V_{cs1} representing the load current I_o of the output terminal OUT , and an output terminal of the pulse width modulation comparator is configured to provide the pulse width modulated signal C_{PWM} .

[0047] According to an exemplary embodiment of the present invention, the control circuit 103 obtains the second feedback signal V_{cs1} representing the load current I_o of the output terminal OUT by detecting the current I_H flowing through the high-side switch M_{HS} . According to an exemplary embodiment of the present invention, the control circuit 103 may further include a high-side switch current detection circuit 208 configured to detect the current I_H flowing through the high-side switch M_{HS} and provide the second feedback signal V_{cs1} .

[0048] According to an exemplary embodiment of the present invention, the load signal V_{load} representing the load state of the output terminal OUT may include the difference amplified signal V_e .

[0049] According to an exemplary embodiment of the present invention, the switching frequency control circuit 204 may include an oscillator OSC and a logic circuit $LOGIC$, as shown in Fig. 4. The oscillator OSC is configured to generate a clock signal $CLOCK$ with a substantially constant frequency. According to an embodiment of the present invention, the frequency of the clock signal $CLOCK$ is the second frequency F_c . The logic circuit $LOGIC$ has a first logic input terminal, a second logic input terminal, and a logic output terminal. The first logic input terminal is configured to receive the clock signal $CLOCK$. The second logic input terminal is configured to receive the load comparison signal CMP . The logic circuit provides the switching frequency modulated signal Clk on the basis of the clock signal $CLOCK$ and the load comparison signal CMP . When the load comparison signal has a first logic state (for example, a high-level logic state),

the logic circuit LOGIC outputs the clock signal CLOCK as the switching frequency modulated signal Clk. When the load comparison signal has a second logic state (for example, a low-level logic state), the switching frequency modulated signal Clk output by the logic circuit LOGIC is in a low-level logic state, that is to say, the clock signal CLOCK is masked at this time (the logic circuit LOGIC skips a part of the pulses of the clock signal CLOCK). In the exemplary embodiment illustrated in Fig. 4, the logic circuit LOGIC includes an AND circuit.

[0050] Still referring to Fig. 3 below, according to an embodiment of the present invention, the control circuit 103 may further include a zero-crossing detection module 209. A first input terminal of the zero-crossing detection module receives a third feedback signal Vcs2 representing a current I_L flowing through the low-side switch M_{LS} , a second input terminal (for example, terminal "-" illustrated in Fig. 3) of the zero-crossing detection module receives a low-side switch current limiting threshold Vth4 (a fourth threshold voltage Vth4), and an output terminal of the zero-crossing detection module provides a zero-crossing comparison signal CZCD according to a comparison result between the third feedback signal Vcs2 and the low-side switch current limiting threshold Vth4. When the third feedback signal Vcs2 is higher than the low-side switch current limiting threshold Vth4, the zero-crossing comparison signal CZCD has a first logic state (for example, a high-level logic state), and the control circuit 103 allows the low-side switch M_{LS} to perform on and off switching on the basis of the zero-crossing comparison signal CZCD. When the third feedback signal Vcs2 is lower than the low-side switch current limiting threshold Vth4, the zero-crossing comparison signal CZCD has a second logic state (for example, a low-level logic state), and on the basis of the zero-crossing comparison signal CZCD, the control circuit 103 switches off the low-side switch M_{LS} and causes it to stop switching on and off.

[0051] According to an embodiment of the present invention, the control circuit 103 realizes the control of the low-side switch M_{LS} according to the zero-crossing comparison signal CZCD by coupling the zero-crossing comparison signal CZCD to the low-side switch driver 106L. For example, according to an embodiment of the present invention, the low-side switch driver 106L has an enable input terminal for receiving the zero-crossing comparison signal CZCD. When the zero-crossing comparison signal CZCD has a first logic state, the low-side switch driver 106L enables and drives the low-side switch M_{LS} to perform on and off switching. When the zero-crossing comparison signal CZCD has the second logic state, the low-side switch driver 106L is disabled, and the low-side switch M_{LS} is switched off and caused to stop switching on and off.

[0052] According to an embodiment of the present invention, the low-side switch current limiting threshold Vth4 is zero, so that when the third feedback signal Vcs2 is lower than zero (that is, when the current I_L flowing through the low-side switch M_{LS} is lower than zero), the low-side switch M_{LS} is switched off, thereby reducing the conduction loss and switching loss of the low-side switch M_{LS} and improving the conversion efficiency of the voltage conversion circuit 200.

[0053] According to an embodiment of the present invention, the low-side switch current limiting threshold Vth4 may have a set compensation value Vos that is lower than zero and close to zero. The amplitude of the compensation value Vos is relatively small, and an appropriate value may be selected according to actual design and application requirements. For example, the

compensation value V_{OS} may be selected with reference to the minimum peak value of the current I_H flowing through the high-side switch that needs to be maintained when the voltage conversion circuit 200 operates in an ultra-light load or no-load state. Setting the low-side switch current limiting threshold V_{th4} to the compensation value V_{OS} that is lower than zero and close to zero, means that the current I_L flowing through the low-side switch M_{LS} is allowed to be less than zero but close to zero. This is helpful to ensure that when the voltage conversion circuit 200 operates in an ultra-light load or no-load state, the current I_H flowing through the high-side switch M_{HS} can be greater than zero, which is used to compensate a part of the current I_L flowing through the low-side switch M_{LS} that is less than zero. In this case, when the bootstrap voltage refresh signal RFS has the first logic state (that is, the bootstrap voltage V_{BST} is lower than the bootstrap voltage refresh threshold V_{th1}), if the voltage conversion circuit 200 operates in the light load or no-load state (that is, the load comparison signal CMP has the first logic state), then both the high-side switch M_{HS} and the low-side switch M_{LS} that perform on and off complementary switching of pulse width modulation at the first frequency F_C can have a relatively large on-time. Therefore, the bootstrap capacitor CB has an appropriate charging time within a switching cycle so as to refresh the bootstrap voltage V_{BST} to at least higher than the bootstrap voltage refresh threshold V_{th1} as soon as possible, so as to ensure the normal on and off switching of the high-side switch M_{HS} , thereby enhancing the operating stability of the voltage conversion circuit 200. At the same time, since the compensation value V_{OS} is lower than zero and close to zero, its amplitude is relatively small. Therefore, the part of the current I_L flowing through the low-side switch M_{LS} that is lower than zero is allowed to be very small, which will not significantly increase the conduction loss and switching loss of the low-side switch M_{LS} and will not have a negative impact on the conversion efficiency of the voltage conversion circuit 200.

[0054] Fig. 5 is a schematic diagram showing main operating waveforms of the voltage conversion circuit 200 shown in Fig. 3 according to an embodiment of the present invention. Next, the voltage conversion circuit 200 will be further explained with reference to Figs. 3 and 5. In the exemplary illustration of Fig. 5, the control circuit 103 obtains the second feedback signal V_{cs1} representing the load current I_o by detecting the current I_H flowing through the high-side switch M_{HS} , and the load signal V_{load} representing the load state of the output terminal OUT includes the difference amplified signal V_e . Since the difference amplified signal V_e defines the peak value of the current I_H flowing through the high-side switch M_{HS} , the difference amplified signal V_e can be used as the load signal V_{load} representing the load state of the output terminal. Of course, selecting the difference amplified signal V_e as the load signal V_{load} is only an exemplary implementation of the present invention. It should be understood by those of ordinary skill in the art that according to different embodiments of the present invention, other suitable signals may also be selected as the load signal V_{load} , such as the load current I_o , the output inductor current I_L , the current I_H of the high-side switch M_{HS} , or their peak values and average values, and their sampling signals, etc. As shown in Fig. 5, the load current I_o is relatively low within the time from t_0 to t_3 , and it can be considered that the load on the output terminal OUT is relatively light. After time t_3 , the load

current I_o suddenly increases, and it can be considered that the load of the output terminal OUT becomes heavier.

[0055] From time t_0 to t_1 , the bootstrap voltage V_{BST} is higher than the first refresh threshold V_{th1L} , and then the bootstrap voltage refresh signal RFS output by the first comparison module 104 has the second logic state (illustrated as a low-level logic state in Fig. 5). At this time, the second comparison module 201 is enabled, and the logic state of the load comparison signal CMP output thereby depends on the comparison result between the load signal V_e and the light load threshold V_{th3} . The control circuit 103 controls the high-side switch M_{HS} and the low-side switch M_{LS} to operate in the variable frequency switching mode of pulse frequency modulation according to the load comparison signal CMP. Specifically, in conjunction with the exemplary embodiments of the present invention as shown in Figs. 3 and 4, when the load signal V_e is higher than the light load threshold V_{th3} , the load comparison signal CMP has the first logic state (illustrated as the high-level logic state in Fig. 5), and the clock signal CLOCK generated by the oscillator OSC is used as the frequency switching control signal Clk (it can be considered that at this time, the frequency switching control signal Clk replicates a part of the pulses of the clock signal CLOCK and has a substantially constant first switching frequency F_C). When the load signal V_e is lower than the light load threshold V_{th3} , the load comparison signal CMP has the second logic state (illustrated as the low-level logic state in Fig. 5), and the frequency switching control signal Clk is at the low level (it can be considered that at this time, the frequency switching control signal Clk skips a part of the pulses of the clock signal CLOCK). Therefore, the switching frequency modulated signal Clk has a second switching frequency F_S that changes with the load signal V_e so that the control module 105 controls, on the basis of the switching frequency control signal Clk, the high-side switch M_{HS} and the low-side switch M_{LS} to operate in the variable-frequency switching mode of pulse frequency modulation. At time t_1 , the bootstrap voltage V_{BST} decreases to be lower than the first refresh threshold V_{th1L} , and the bootstrap voltage refresh signal RFS output by the first comparison module 104 jumps to have the first logic state (the high-level logic state in Fig. 5). At this time, the bootstrap voltage refresh signal RFS controls the second comparison module 201 to be disabled (illustrated in Fig. 5 by reducing the light load threshold V_{th3} to be coupled to the reference ground GND), and then the load comparison signal CMP has the first logic state (illustrated as the high-level logic state in Fig. 5) substantially constantly. At this time, it can be considered that the frequency switching control signal Clk has replicated a part of the pulses of the clock signal CLOCK and has the first switching frequency F_C . Therefore, the control module 105 controls the high-side switch M_{HS} and the low-side switch M_{LS} to perform on and off switching in a complementary manner at the first switching frequency F_C , so that the bootstrap capacitor CB is charged during the on time of the low-side switch M_{LS} in each switching cycle. After several switching cycles, until time t_2 , the bootstrap voltage V_{BST} is charged to be higher than the second refresh threshold V_{th1H} , and the bootstrap voltage refresh signal RFS is recovered to have the second logic state (illustrated as the low-level logic state in Fig. 5) so that the second comparison module 201 is recovered to be enabled. From time t_2 to t_3 , the bootstrap voltage V_{BST} continues to be higher than the first refresh threshold V_{th1L} . The operating process

of the voltage conversion circuit 200 is the same as that from time t_0 to t_1 . The control circuit 103 controls, according to the load comparison signal CMP, the high-side switch M_{HS} and the low-side switch M_{LS} to operate in the variable-frequency switching mode of pulse frequency modulation. At time t_3 , the output current I_o suddenly increases (the load of the output terminal OUT increases), and the load signal V_e representing the output current I_o continues to be higher than the light load threshold V_{th3} so that the load comparison signal CMP has the first logic state (illustrated as the high-level logic state in Fig. 5), and the frequency switching control signal Clk replicates a part of the pulses of the clock signal CLOCK and has a substantially constant first switching frequency F_C . Therefore, the control module 105 controls the high-side switch M_{HS} and the low-side switch M_{LS} to perform constant-frequency on and off switching of pulse width modulation at the first switching frequency F_C so that the bootstrap capacitor CB is charged during the on-time of the low-side switch M_{LS} in each switching cycle, and the bootstrap voltage V_{BST} gradually increases until it stabilizes at the bootstrap charging power supply voltage VB (which is implemented through the adjustment of the bootstrap power supply regulating module BSTREG).

[0056] According to the exemplary embodiments and variant implementations thereof described on the basis of Figs. 3 to 5 of the present invention, the control circuit 103 controls the charging of the bootstrap capacitor CB by controlling the on and off switching of the high-side switch M_{HS} and the low-side switch M_{LS} on the basis of the bootstrap voltage V_{BST} so that when the bootstrap voltage V_{BST} is insufficient (that is, when the bootstrap voltage V_{BST} is lower than the bootstrap voltage refresh threshold V_{th1}), the bootstrap voltage V_{BST} is refreshed to a sufficient level in time (that is, the bootstrap voltage V_{BST} is refreshed to a value higher than the bootstrap voltage refresh threshold V_{th1}), thereby ensuring normal on and off driving of the high-side switch M_{HS} and allowing the voltage conversion circuit 200 to operate normally.

[0057] According to the exemplary embodiments and variant implementations thereof described on the basis of Figs. 3 to 5 of the present invention, the first comparison module 104 compares the bootstrap voltage V_{BST} with the bootstrap voltage refresh threshold V_{th1} to provide a bootstrap voltage refresh signal RFS so as to control whether the second comparison module 201 is enabled or disabled. If the second comparison module 201 is enabled, when the load current I_o is small (that is, when the load signal V_{load} representing the output current I_o is lower than the light load threshold V_{th3} , the load of the output terminal OUT is relatively light), the control circuit 103 will control the high-side switch M_{HS} and the low-side switch M_{LS} to operate in the variable-frequency switching mode of pulse frequency modulation. When the load current I_o is relatively large (that is, when the load signal V_{load} representing the output current I_o is higher than the light load threshold V_{th3} , the load of the output terminal OUT is relatively large), the control circuit 103 will control the high-side switch M_{HS} and the low-side switch M_{LS} to operate in the constant-frequency switching mode of pulse width modulation. If the second comparison module 201 is disabled, regardless of the state of the load current I_o (the load state of the output terminal OUT), the control circuit 103 causes the high-side switch M_{HS} and the low-side switch M_{LS} to operate in the constant-frequency switching mode of pulse width modulation so as to charge the bootstrap capacitor CB. Therefore, when the bootstrap voltage V_{BST} is lower than the bootstrap voltage refresh threshold

Vth1 (that is, when the bootstrap voltage V_{BST} is insufficient), the control circuit 103 disables the second comparison module through the bootstrap voltage refresh signal RFS so that the high-side switch M_{HS} and the low-side switch M_{LS} perform constant-frequency on and off switching of pulse width modulation, thereby charging the bootstrap capacitor CB during the on-time of the low-side switch M_{LS} in each switching cycle to refresh the bootstrap voltage V_{BST} .

[0058] According to the exemplary embodiments and variant implementations thereof described on the basis of Figs. 3 to 5 of the present invention, even if the load of the output terminal OUT is relatively light (that is, the load current I_o is relatively small, and the load signal V_{load} representing the output current I_o has been lower than the light load threshold V_{th3}), and the high-side switch M_{HS} and the low-side switch M_{LS} should operate in the variable-frequency switching mode of pulse frequency modulation (for example, within the time from t_0 to t_3 as shown in Fig. 5), once the bootstrap voltage V_{BST} is lower than the bootstrap voltage refresh threshold V_{th1} (for example, at time t_1 shown in Fig. 5), the control circuit 103 causes the high-side switch M_{HS} and the low-side switch M_{LS} to recover the constant-frequency on and off switching of pulse width modulation so that the bootstrap capacitor CB is charged (for example, within the time from t_1 to t_2 as shown in Fig. 5), and the bootstrap voltage V_{BST} begins to recover. Within the time from t_1 to t_2 , since the peak current of the high-side switch current I_H is relatively small, the voltage ripple of the output voltage V_o is also relatively small, and the conversion efficiency of the voltage conversion circuit is still relatively high. The high-side switch M_{HS} and the low-side switch M_{LS} undergo constant-frequency on and off switching of small peak current pulse width modulation for a certain number of cycles until the bootstrap voltage V_{BST} is recovered to be higher than the bootstrap voltage refresh threshold V_{th1} (for example, at time t_2 as shown in Fig. 5), and the control circuit 103 causes the high-side switch M_{HS} and the low-side switch M_{LS} to continue the variable-frequency on and off switching of the pulse frequency modulation that should be performed. In this way, the voltage conversion circuit according to various exemplary embodiments of the present invention and variant implementations thereof can operate when the output voltage V_o is close to the output voltage V_{in} . The control circuit 103 can not only recover the bootstrap voltage V_{BST} to a level sufficient to drive the high-side switch M_{HS} in time without causing large fluctuations in the output voltage V_o , but also ensure that the voltage conversion circuit has relatively high conversion efficiency.

[0059] For the bootstrap voltage refresh control circuit 103 according to various embodiments of the present invention and variant implementations thereof, the beneficial effects thereof including the voltage conversion circuit of the bootstrap voltage refresh control circuit 103 should not be considered to be limited only to the above. These and other beneficial effects according to various embodiments of the present invention may be better understood by reading the detailed description of the present invention and studying the accompanying drawings of the various embodiments.

[0060] Fig. 6 is a schematic diagram showing a method for controlling a voltage conversion circuit according to an embodiment of the present invention. The voltage conversion circuit may comprise a high-side switch, a low-side switch, and a bootstrap capacitor for providing a bootstrap

voltage for the high-side switch, and the voltage conversion circuit provides an output voltage and an output current on the basis of on and off switching of the high-side switch and the low-side switch. The method of controlling the voltage conversion circuit includes: step 601, detecting the bootstrap voltage; step 602, comparing the bootstrap voltage with a bootstrap voltage refresh threshold to provide a bootstrap voltage refresh signal; and step 603, controlling the on and off switching of the high-side switch and the low-side switch on the basis of the bootstrap voltage refresh signal to control charging of the bootstrap capacitor.

[0061] According to an embodiment of the present invention, in step 602, if the bootstrap voltage is lower than the bootstrap voltage refresh threshold, the bootstrap voltage refresh signal has a first logic state. If the bootstrap voltage is higher than the bootstrap voltage refresh threshold, the bootstrap voltage refresh signal has a second logic state. In step 603, if the bootstrap voltage refresh signal has the first logic state, the high-side switch and the low-side switch are switched on and off in a complementary manner at a substantially constant frequency, so as to charge the bootstrap capacitor. If the bootstrap voltage refresh signal has the second logic state, the high-side switch and the low-side switch are switched on and off according to the output voltage and the output current.

[0062] According to an embodiment of the present invention, in step 602, the bootstrap voltage refresh threshold may include a first refresh threshold and a second refresh threshold, wherein the first refresh threshold is smaller than the second refresh threshold. If the bootstrap voltage is lower than the first refresh threshold, the bootstrap voltage refresh signal has a first logic state. If the bootstrap voltage is higher than the second refresh threshold, the bootstrap voltage refresh signal has a second logic state.

[0063] According to an embodiment of the present invention, step 603 may include: step 604, detecting the output current of the voltage conversion circuit and providing a load signal representing the output current; step 605, comparing the load signal with a light load threshold to provide a load comparison signal, wherein the load signal has a first logic state and a second logic state; step 606, adjusting the load comparison signal on the basis of the bootstrap voltage refresh signal, wherein if the bootstrap voltage is lower than the bootstrap voltage refresh threshold, the load comparison signal has a first logic state, and if the bootstrap voltage is higher than the bootstrap voltage refresh threshold, the load comparison signal has a first logic state when the load signal is higher than the light load threshold and a second logic state when the load signal is lower than the light load threshold; and step 607, controlling the on and off switching of the high-side switch and the low-side switch on the basis of the load comparison signal, wherein if the load comparison signal has the first logic state, the high-side switch and the low-side switch are caused to perform constant-frequency on and off switching of pulse width modulation, and if the load comparison signal has the second logic state, the high-side switch and the low-side switch are caused to perform variable-frequency on and off switching of pulse frequency modulation.

[0064] According to an embodiment of the present invention, in step 607, when the load comparison signal has the first logic state, the frequency of the on and off switching of the high-side switch and the low-side switch is a substantially constant first switching frequency, and when

the load comparison signal has the second logic state, the frequency of the on and off switching of the high-side switch and the low-side switch is a changing second switching frequency, wherein the second switching frequency changes according to changes in the load signal. According to an embodiment of the present invention, the smaller the load signal is, the smaller the second switching frequency is.

[0065] According to an embodiment of the present invention, in step 607, if the load comparison signal has the first logic state, the high-side switch and the low-side switch are caused to perform constant-frequency on and off switching of pulse width modulation, and if the load comparison signal has the second logic state, the high-side switch and the low-side switch are caused to switch off and stop switching on and off.

[0066] According to an embodiment of the present invention, step 607 may include: step 608, detecting the output voltage and providing a first feedback signal representing the output voltage, and detecting the output current and providing a second feedback signal representing the output current; step 609, providing a pulse width modulated signal on the basis of the first feedback signal and the second feedback signal; step 610, generating a switching frequency modulated signal on the basis of the load comparison signal, wherein if the load comparison signal has a first logic state, the switching frequency modulated signal has a substantially constant first switching frequency, and if the load comparison signal has a second logic state, the switching frequency modulated signal has a second switching frequency that changes with the load signal; and step 611, providing a high-side switch control signal and a low-side switch control signal on the basis of the pulse width modulated signal and the switching frequency modulated signal, wherein when the load comparison signal has a first logic state, the high-side switch control signal and the low-side switch control signal are pulse width modulated signals with the first switching frequency and are used to control the high-side switch and the low-side switch to perform constant-frequency on and off switching of pulse width modulation, and when the load comparison signal has a second logic state, the high-side switch control signal and the low-side switch control signal are pulse frequency modulated signals with the second switching frequency, and are used to control the high-side switch and the low-side switch to perform variable-frequency on and off switching of pulse frequency modulation.

[0067] The method for controlling the voltage conversion circuit according to an embodiment of the present invention may further include: step 612, detecting a current flowing through the low-side switch and generating a third feedback signal representing the current flowing through the low-side switch; step 613, comparing the third feedback signal with a low-side switch current limiting threshold to generate a zero-crossing comparison signal, wherein when the third feedback signal is higher than the low-side switch current limiting threshold, the zero-crossing comparison signal has a first logic state, and when the third feedback signal is lower than the low-side switch current limiting threshold, the zero-crossing comparison signal has a second logic state; and step 614, controlling the on and off of the low-side switch on the basis of the zero-crossing comparison signal, wherein when the zero-crossing comparison signal has a first logic state, the low-side switch is allowed to perform on and off switching, and when the zero-crossing comparison signal

has a second logic state, the low-side switch is caused to be switched off to stop switching on and off.

[0068] According to an embodiment of the present invention, the low-side switch current limiting threshold has a set compensation value that is lower than zero and close to zero.

[0069] The method for controlling the voltage conversion circuit according to an embodiment of the present invention may further include: step 615, detecting the bootstrap voltage, and comparing the bootstrap voltage with a bootstrap voltage under-voltage threshold to provide a bootstrap under-voltage signal, wherein the bootstrap voltage under-voltage threshold is smaller than the bootstrap voltage refresh threshold, if the bootstrap voltage is lower than the bootstrap voltage under-voltage threshold, the bootstrap under-voltage signal has a first logic state, and if the bootstrap voltage is higher than the bootstrap voltage under-voltage threshold, the bootstrap under-voltage signal has a second logic state; and step 616, controlling on and off of the high-side switch and the low-side switch on the basis of the bootstrap under-voltage signal, wherein when the bootstrap under-voltage signal has a first logic state, the high-side switch and the low-side switch are switched off and caused to stop switching on and off, and when the bootstrap under-voltage signal has a second logic state, the high-side switch and the low-side switch are allowed to perform on and off switching.

[0070] The above descriptions of the methods and steps for controlling the voltage conversion circuit according to various embodiments of the present invention and variant implementations thereof are only exemplary and are not intended to limit the present invention. In addition, some well-known control steps and used control parameters are not given or described in detail to make the present invention clear, concise, and easy to understand. It should be understood by those skilled in the technical field to which the present invention pertains that the step numbers used in the above descriptions of the methods and steps for controlling the voltage conversion circuit according to various embodiments of the present invention are not used to indicate the absolute order of the steps, and these steps are not implemented in the order of step numbers, but rather may be implemented in different orders, or may be implemented simultaneously and in parallel, which is not limited to the described embodiments.

[0071] Although the bootstrap voltage refresh control circuit according to various embodiments of the present invention, the voltage conversion circuit including the bootstrap voltage refresh control circuit, and the control method therefor are described in the description with the buck-type voltage conversion circuit as an example, this does not mean that the present invention is limited thereto. It should be understood by those skilled in the art that the structure and principles given here may also be applied to voltage conversion circuits with other topologies, such as boost type voltage conversion circuits, buck-boost type voltage conversion circuits, etc.

[0072] Therefore, the above description and embodiments of the present invention only describe the bootstrap voltage refresh control circuit, the voltage conversion circuit including the bootstrap voltage refresh control circuit, and the control method therefor in an exemplary manner, and are not intended to limit the scope of the present invention. It is possible to make variations and modifications to the disclosed embodiments, and other feasible alternative embodiments and

equivalent changes to elements in the embodiments can be understood by those of ordinary skill in the art. Other variations and modifications to the disclosed embodiments of the present invention do not exceed the spirit and scope of protection of the present invention.

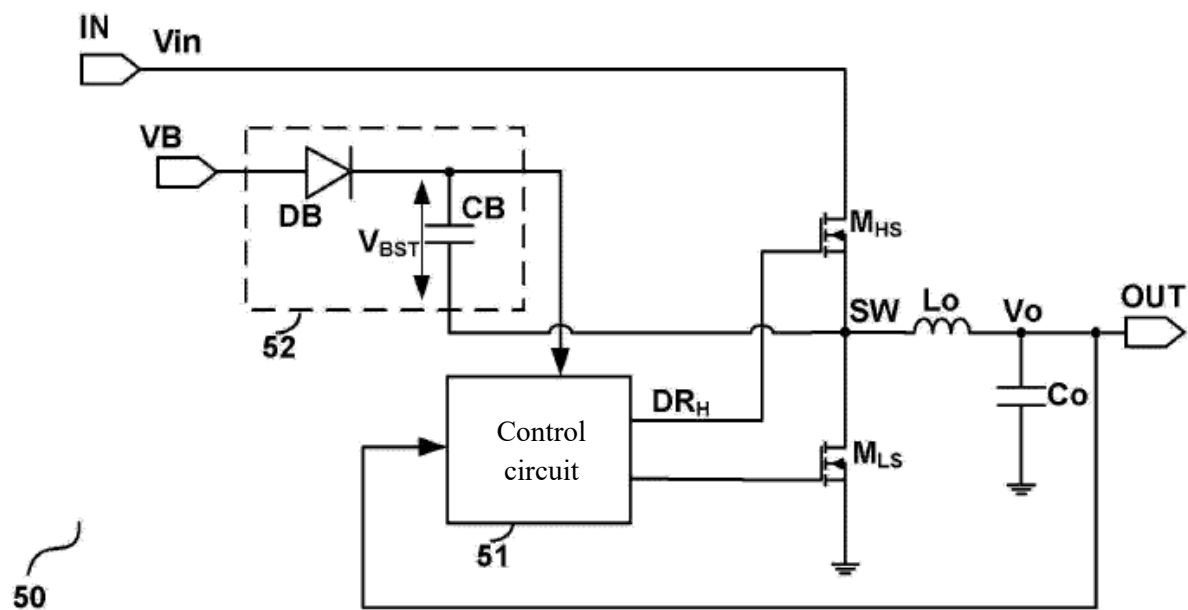


Fig. 1

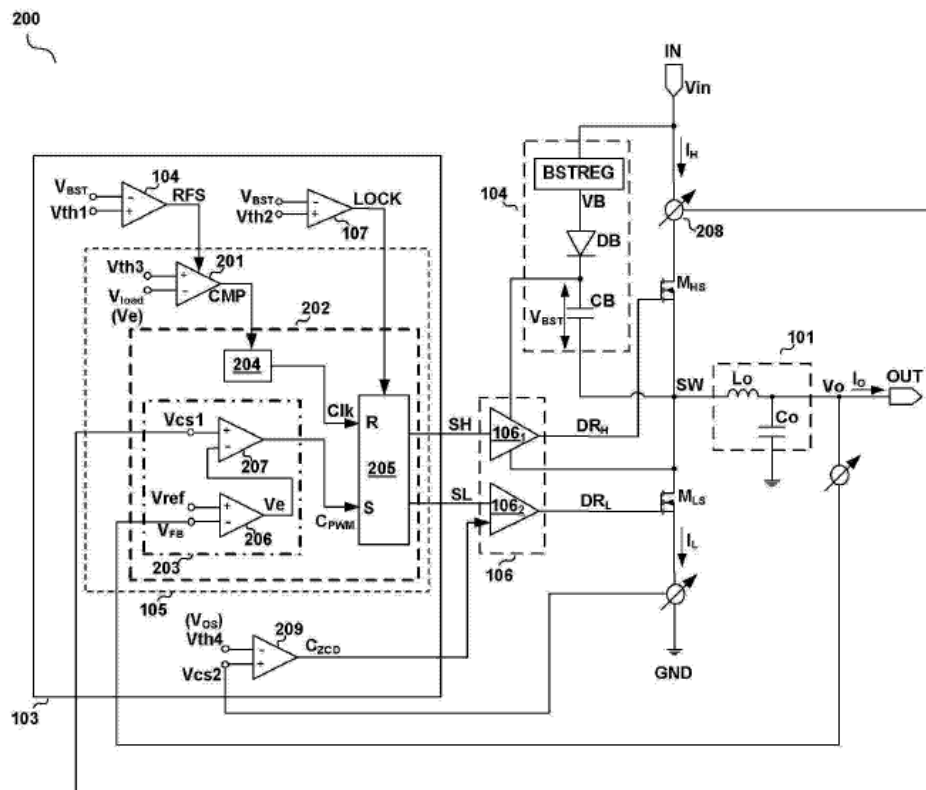


Fig. 3

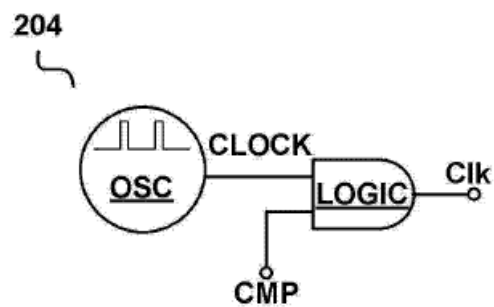


Fig. 4

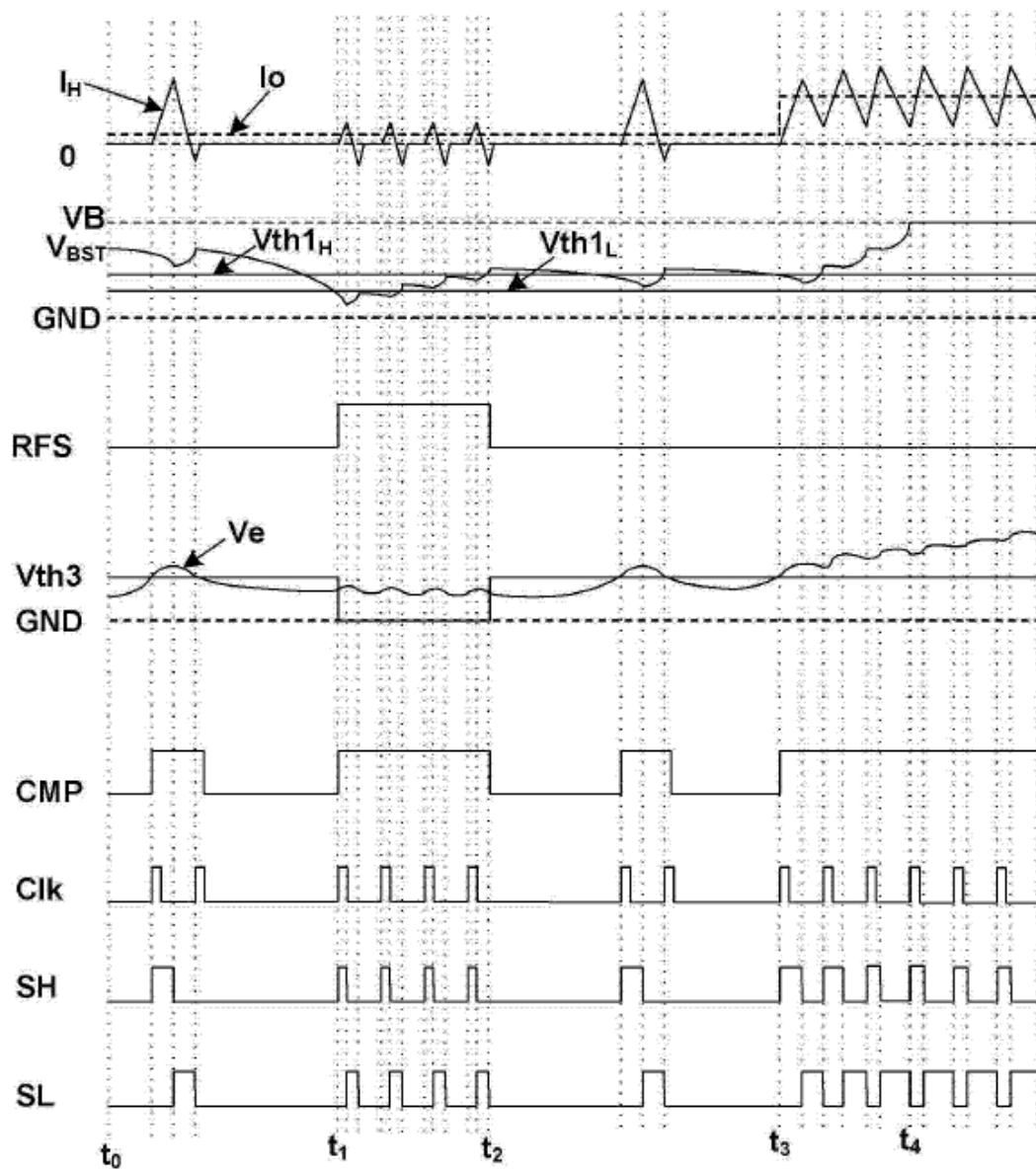


Fig. 5

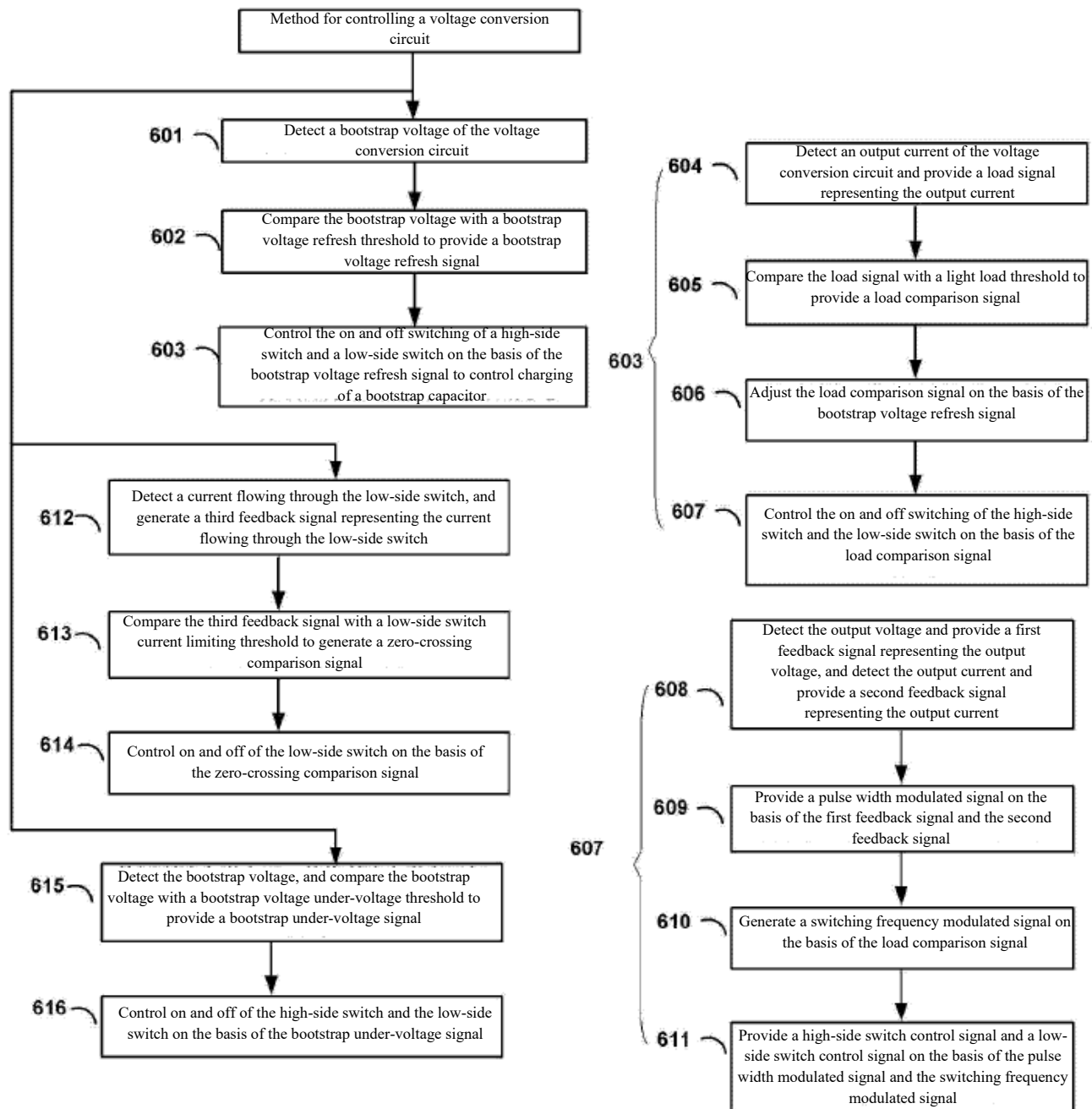


Fig. 6