

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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REED SEMICONDUCTOR CORP.,

*Petitioner*

v.

MONOLITHIC POWER SYSTEMS, INC.

*Patent Owner*

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IPR2024-00871

Patent No. 9,590,608

Filing Date: August 11, 2015

Issue Date: March 7, 2017

Title: Bootstrap refresh control circuit, voltage converter and associated method

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*Inter Partes* Review No.: IPR2024-00871

Exhibit 1003

**Declaration of Douglas Holberg**

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## **I. INTRODUCTION**

1. I have been engaged by REED SEMICONDUCTOR CORP to opine on the patentability or otherwise of U.S. Patent No. 9,590,608 (—the '608 Patent), entitled — BOOTSTRAP REFRESH CONTROL CIRCUIT, VOLTAGE CONVERTER AND ASSOCIATED METHOD. My opinions are set forth herein. I submit this Declaration on behalf of REED SEMICONDUCTOR CORP in connection with its request for *inter partes* review of the '608 Patent.

### **A. Education and Relevant Experience**

2. My education includes a B.S. in Electrical Engineering from Texas A&M University in 1977, followed by a M.S. in Electrical Engineering from the University of Texas at Austin in 1989. I earned a Ph.D. in Electrical Engineering from the University of Texas at Austin in 1992.

3. I have over 40 years of experience in the electronics field. During that time, I have worked for several different electronics companies including: Mostek, Texas Micro Engineering (acquired by Crystal Semiconductor), Crystal Semiconductor, Cirrus Logic, Cygnal Integrated Products, and Silicon Laboratories. I joined Silicon Laboratories when they acquired Cygnal, which I co-founded in 1999.

4. I am a named inventor on 43 U.S. granted patents. I have held a variety of engineering positions throughout my career, from circuit designer,

design manager, Director of Engineering, Chief Technology Officer (CTO), Vice President (V.P.) of Engineering, and V.P. of Technology. In addition to my engineering experience, I also have served as an adjunct faculty member at the University of Texas, where I taught CMOS analog and mixed-signal design for six years.

5. I am the co-author of the textbook —CMOS Analog Circuit Design, the first edition of which published 1987. As explained in the Preface of the second edition, published in 2002, the objective of the textbook is to teach the fundamentals and background that are necessary to understand how a —circuit works. It is now available in third edition and published in English and Chinese (first and second edition). This textbook is widely used throughout the world by new and experienced engineers in industry and by students in the classroom.

6. Upon graduating from Texas A&M University, I went to work for Mostek Corporation designing integrated circuits for telecommunications applications. I designed an integrated dual tone multi frequency (DTMF) generator. I received my first patent for this integrated DTMF generator. After leaving Mostek, I joined a startup company, Texas Micro Engineering, as the second employee. At Texas Micro Engineering, I designed, among other things, a dual-channel (atrium-ventricle) pacemaker sense amplifier/filter using discrete-time switched-capacitor technology.

7. While enrolled in the Masters/Ph.D. program at the University of Texas at Austin, I worked on the application of bipolar technology to dynamic random access memory (DRAM) sense-amplifier architectures and circuit-simulation algorithms. While at The University of Texas at Austin, I also designed and laid out the mask set (The Holberg Mask Set) still in use by the fabrication class/lab.

8. Upon graduating with a Ph.D. in Electrical Engineering, I went to work for Crystal Semiconductor/Cirrus Logic, where I designed high frequency synthesizers for hard-disk read-channel applications. I managed a group designing charge-coupled device (CCD) interface circuits for digital camera applications, as well as television encoder chips and CMOS imagers.

9. Upon leaving Cirrus, I started a company called Cygnal Integrated Products that developed mixed-signal microcontrollers. At Cygnal, I was the founder, CTO, V.P. of Engineering, and an individual contributor. While at Cygnal, I designed analog-to-digital converters (ADCs), Vbe temperature sensors, input/output (I/O) cells/pads (both design and layout), as well as many additional miscellaneous circuits. My company was later purchased by Silicon Labs, where I remained employed as a manager of the microcontroller group, followed by the position of V.P. of Technology.

10. I have significant experience with the technology described in the '608 patent, including resistors, capacitors, diodes, inductors, transistors, transformers, oscillators, operational amplifiers, comparators, general integrated-circuit technology, analog/digital mixed-signal circuits, DC-DC converters, device analysis and modeling, floor-planning, and layout of integrated circuits, and the tools used to design, and verify integrated circuits (CAD tools). In addition, I have experience with device modeling and characterization, which has been applied throughout my career.

11. My analyses set forth in this declaration are informed by my experience in the field of electrical engineering, including analog circuitry, ADCs, power circuits, and digital circuits. Based on my above-described experience, I believe that I am considered to be an expert in the field.

12. The '608 Patent is entitled — BOOTSTRAP REFRESH CONTROL CIRCUIT, VOLTAGE CONVERTER AND ASSOCIATED METHOD. Prior to reviewing the '608 Patent, I was well familiar with the subject matter described and claimed therein. I am well familiar with circuits generally, such as disclosed in the '608 Patent.

**B. Materials Considered**

13. The analysis that I provide in this Declaration is based on my education and experience as an engineer, and upon my knowledge of general

circuit analysis and design, as well as the documents I have considered, including the '608 Patent (Ex.1001). I have reviewed the prosecution history for the '608 Patent (Ex.1002).

14. I have reviewed various publications from the prior art at the time of the alleged invention of the '608 Patent. These publications, along with other materials I have reviewed, include those listed in the table below:

| <b>Exhibit No.</b> | <b>Description</b>                                                                                                    |
|--------------------|-----------------------------------------------------------------------------------------------------------------------|
| 1001               | U.S. Patent No. 9,590,608 B2 to Xu                                                                                    |
| 1002               | Prosecution History of U.S. 9,590,608                                                                                 |
| 1005               | U.S. Patent No. 7,145,316 B1 to Galinski                                                                              |
| 1006               | Texas Instruments TPS54620 4.5V to 17V Input, 6A Synchronous Step Down SWIFT™ Converter Data Sheet (Revised May 2011) |
| 1007               | U.S. Patent No. 7,321,258 B2 to Wong                                                                                  |
| 1008               | Chinese Patent Application Publication No. CN 102832810 A to Li                                                       |
| 1009               | U.S. Patent No. 7,026,801 B2 to Fowler                                                                                |
| 1010               | U.S. Patent Application Publication No. 2015/0214839 A1 to Shiu                                                       |
| 1011               | Certified English Translation of Exhibit 1008 - Chinese Patent Application Publication No. CN 102832810 A to Li       |
| 1012               | Translator Certification Regarding Exhibit 1011                                                                       |
| 1013               | U.S. Patent Application Publication 2007/0024261 A1 to Wong                                                           |

| <b>Exhibit No.</b> | <b>Description</b>                                                                                                           |
|--------------------|------------------------------------------------------------------------------------------------------------------------------|
| 1017               | U.S. Patent Application Publication No. 2015/0061611 A1 to Li                                                                |
| 1018               | Declaration of Maureen M. Honeycutt                                                                                          |
| 1019               | Texas Instruments TPS54620 4.5V to 17V Input, 6A Synchronous Step Down SWIFT™ Converter Data Sheet (Revised May 2009)        |
| 1020               | Texas Instruments TPS54620 4.5V to 17V Input, 6A Synchronous Step Down SWIFT™ Converter Data Sheet (Revised January 2010)    |
| 1021               | Texas Instruments TPS54620 4.5V to 17V Input, 6A Synchronous Step Down SWIFT™ Converter Data Sheet (Revised October 2010)    |
| 1022               | Texas Instruments TPS54560 4.5V to 60 V input, 5 A step-down converter with Eco-Mode™ Data Sheet (Revised March 2013)        |
| 1023               | Texas Instruments TPS54560 4.5V to 60 V input, 5 A step-down converter with Eco-Mode™ Data Sheet (Revised March 2014)        |
| 1024               | Allen, Philip E., and Douglas R. Holberg. “CMOS Analog Circuit Design” (Third Edition) (“CMOS”)                              |
| 1025               | US Patent Application Publication No. 2003/0155894A1 to Dubhashi and Vaysse (“Dubhashi”)                                     |
| 1026               | U.S. Patent No. 5,097,196A to Schoneman (“Schoneman”)                                                                        |
| 1027               | U.S. Patent No. 5,770,940 to Goder (“Goder”)                                                                                 |
| 1028               | Wait, John V, Huelsman, Lawrence P, Korn, Granino. “Introduction to Operational Amplifiers Theory and Applications” (“Wait”) |
| 1029               | Assignment of U.S. Patent No. 9,590,608 from Chengdu Monolithic Power Systems Co., Ltd. to Monolithic Power Systems, Inc.    |

| <b>Exhibit No.</b> | <b>Description</b>                                                                        |
|--------------------|-------------------------------------------------------------------------------------------|
| 1030               | Redacted Exhibit A from Monolithic Power Systems, Inc.'s Initial Infringement Contentions |
| 1033               | Texas Instruments TLC551, TLC551Y LinCMOSE™ TIMERS Data Sheet (Revised September 1997)    |

## **II. LEGAL PRINCIPLES USED IN MY ANALYSIS**

15. I understand that in writing this Declaration I am obliged to follow existing applicable law. I have therefore been asked to apply the following legal principles to my analysis, and I have done so.

### **A. Person Having Ordinary Skill in the Art**

16. I understand that my assessment of the claims of the '608 Patent must be undertaken from the perspective of what would have been known or understood by a person having ordinary skill in the art, reading the '608 Patent on its relevant filing date and in light of the specification and file history of that patent. I often refer to such a person as a —POSITA in this Declaration.

17. I am informed and understand that various factors can be considered in determining a person having ordinary skill in the art (POSITA). I am informed and understand that those factors include: (1) the educational level of the inventor(s); (2) the type of problems encountered in the art; (3) prior art solutions to those problems; (4) the rapidity with which innovations are made; (5)

sophistication of the technology; and (6) education level of active workers in the field.

18. I understand that REED SEMICONDUCTOR CORP proposed in the Petition that a person having ordinary skill in the art (POSITA) in the field of the '608 Patent in 2015 would have been someone knowledgeable about and familiar with the DC-DC switch-mode power converter technology that is pertinent to the '608 Patent. A POSITA would have had a bachelor's degree in Electrical Engineering or equivalent training, and approximately two years of experience working in the field of power converters, feedback systems, or related technologies. Lack of work experience can be remedied by additional education, and vice versa.

19. I agree with this level of ordinary skill for the '608 Patent. Based on my experience, I understand and know of the capabilities of a person of this skill level as of the time the '608 Patent was filed. I am familiar with how a POSITA would have understood and used the terminology found in the '608 Patent at the time of its filing, and with the state of the art at that time.

20. My analysis and opinions presented herein regarding the claims of the '608 Patent have been and are based on the perspective of a POSITA as defined above as of August 11, 2014, the priority date for the '608 patent. As described

above and as shown in my CV, I have extensive experience in the field of electronics in the relevant timeframe.

**B. The Prior Art**

21. I understand that applicable patent law provides categories of information that constitute prior art that may be used to anticipate patent claims or to render them obvious. I understand that for a reference to qualify as prior art to a particular patent claim under the relevant law, that reference must have been made, known, used, published, or patented, or must have been the subject of a patent application by another person, before the priority date of the patent, and in this matter, must satisfy one of the standards of pre-AIA 35 U.S.C. §102.

**C. Claim Construction Standard**

22. In making this Declaration, I have been asked to review the terms in the '608 Patent claims to determine what a POSITA would have understood those terms to have meant at the time of the alleged invention. In addition, I have been informed that, in an *inter partes* review proceeding, the claim terms under consideration are to be construed using the same claim construction standard used in a civil action under 35 U.S.C. § 282(b), which is articulated in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc), and its progeny. I further understand that under the *Phillips* standard, the claim terms are given their ordinary and customary meaning, as would be understood by a POSITA at the time

of the invention, consistent with the specification and the prosecution history. My opinions regarding the meaning of claim terms of the '608 Patent are based on the construction of the claim terms using the *Phillips* standard in view of the specification and the prosecution history of the '608 Patent.

**D. Anticipation**

23. I understand that to be valid, a patent claim must be —novel, and that a claim is invalid if it is —anticipated by a single prior art reference. I further understand that a reference anticipates if it discloses each and every element of the claim and enables a POSITA to make and use the claimed invention without undue experimentation.

**E. Obviousness**

24. I also understand that even if a claim of a patent is not anticipated, that claim is still invalid if the differences between the claimed subject matter and the prior art are such that the subject matter as a whole would have been obvious to a POSITA at the time the invention was made.

25. I understand further that the condition “at the time the invention was made” in an obviousness determination is imposed to rule out impermissible hindsight. Accordingly, permissible reasoning takes into account only knowledge which was within the level of ordinary skill in the art at the time the claimed invention was made and does not include knowledge gleaned from the applicant’s

disclosure in the patent under analysis. I also understand that an opining expert is required to analyze prior art from the perspective of a POSITA and may not simply provide his or her own personal conclusions.

26. I also understand that an obviousness determination includes several factual inquiries, including: (1) determining the scope and content of the prior art; (2) ascertaining the differences between the claimed invention and the prior art; (3) resolving the level of ordinary skill in the pertinent art; and (4) taking into consideration any secondary indicia (objective evidence) of non-obviousness.

27. I also understand that such objective evidence of non-obviousness may include: (1) a long felt but unsolved need that was satisfied by the claimed invention; (2) commercial success attributable to the claimed invention; (3) unexpected results achieved by the claimed invention; (4) praise by experts of the claimed invention with factual support; (5) taking of licenses under the patent by others for reasons related to the alleged non-obviousness of the claimed invention; (6) the failure of others; (7) the teaching away of others; (8) skepticism by experts; and (9) evidence that competitors in the marketplace have copied the invention instead of using the prior art. I also understand that, in order to establish non-obviousness, there must be a demonstrated relationship, or nexus, between any such secondary indicia and the claimed invention, i.e., there must be objective evidence of non-obviousness attributable to the claimed invention.

28. I further understand that near simultaneous invention by two or more equally talented inventors working independently may or may not be an indication of obviousness when considered in light of all the circumstances.

29. I understand that a conclusion of obviousness can be based on a combination of multiple prior art references. I understand that rationales that may support a conclusion of obviousness include:

(A) Combining prior art elements according to known methods to yield predictable results;

(B) Simply substituting one known element for another to obtain predictable results;

(C) Using known techniques to improve similar devices (methods, or products) in the same way;

(D) Applying a known technique to a known device (method, or product) ready for improvement to yield predictable results;

(E) Using an obvious to try solution, i.e., choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;

(F) Applying known work in one field of endeavor to yield variations of it for use in either the same field or a different one based on design

incentives or other market forces if the variations are predictable to one of ordinary skill in the art;

(G) Applying some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference disclosures to arrive at the claimed invention.

30. I further understand that an analysis of obviousness should recognize that market demand, rather than scientific literature, often drives design trends.

31. I also understand that if a technique has been used to improve one device, and if a POSITA would recognize the technique would improve similar devices in the same way, then using that technique would be obvious to a POSITA unless actual application of that technique is beyond his or her skill.

32. I also understand that practical and common-sense considerations should guide an analysis of obviousness, because familiar items may have obvious uses beyond their primary purposes. I further understand that applying common sense does not require a specific hint or suggestion in a particular reference. Rather, applying common sense requires a reasoned explanation that avoids conclusory generalizations and false deductions.

33. I also understand that, when addressing a problem, a POSITA will often be able to fit together the disclosures of multiple publications. In this regard,

I understand that an analysis of obviousness may consider inferences and creative steps that a POSITA would normally employ.

34. I also understand that a particular combination of prior art may be proven obvious merely by showing that it was obvious for a POSITA to try that combination. For example, when there is a design need or a market pressure to solve a problem, and/or there exists a finite number of identified, predictable solutions with a reasonable expectation of success, a POSITA has good reason to pursue the known options within his or her technical grasp. I understand that if this leads to anticipated success, it is likely that the result is not of innovation but of ordinary skill and common sense.

35. I also understand that a combination of familiar elements according to known methods is presumed to be obvious when that combination does no more than yield predictable results. Work known in one field of endeavor may prompt variations of that work for use in either the same field or a different field, based on design incentives and other market forces. If a technique has been used to improve some device, and a POSITA can implement a predictable variation of that technique, then that variation is likely unpatentable.

36. I further understand that to be proper for use in an analysis of obviousness, a reference must teach art that is analogous to the claimed invention. I also understand that under a correct analysis, any need or problem known in the

field of endeavor at the time of the invention and addressed by the claimed invention can provide a reason for combining the elements in the manner claimed.

37. I understand that a claim can be obvious in light of a single reference, without the need to combine references, if the elements of the claim that are not found explicitly or inherently in that single reference can be supplied by the common sense or technical knowledge of a POSITA. For example, combining two embodiments disclosed adjacent to each other in a prior art patent likely does not require a leap of inventiveness.

38. I also understand that a claimed invention may be obvious if it merely involves simple substitution of one known element for another to obtain predictable results.

39. I understand further that, in an analysis of obviousness, two items of prior art need not be like two puzzle pieces that must fit together perfectly. For example, a claimed invention may be found obvious if a POSITA would view rearrangement as an obvious matter of design choice.

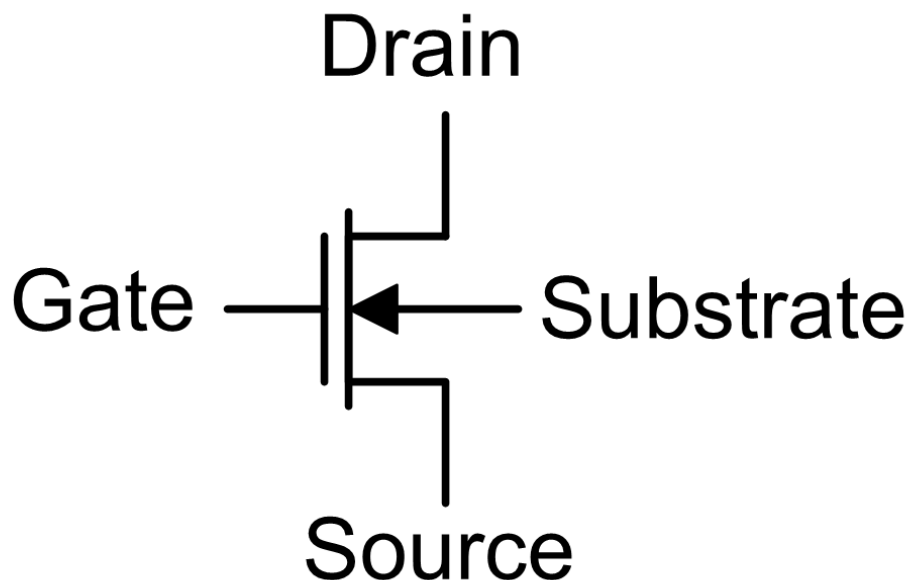
40. I also understand that an analysis of obviousness requires a comparison between the properly construed claim language and the prior art on a limitation-by-limitation basis.

### III. BACKGROUND OF THE TECHNOLOGY

#### A. MOSFET

41. MOSFETS encompass a broad field well beyond the scope of the background necessary to understand the patents in this proceeding. Thus, only information germane to this declaration will be provided.

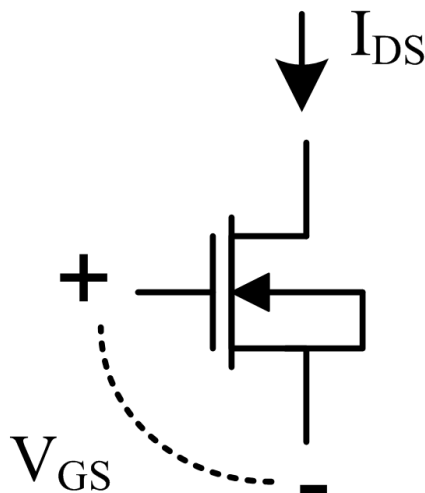
42. A MOSFET transistor is a four-terminal electrical device that is used as an amplifier or a switch. They are manufactured in fundamentally two varieties: P-channel and N-channel. Each can be implemented as enhancement-mode or depletion-mode. Only N-channel enhancement mode MOSFETs are of interest here. The symbol for a four-terminal N-channel transistor is shown below. The terminals are identified as Drain (drain), Gate (gate), Source (source), and Substrate (substrate).



43. A general MOSFET is a bi-directional device and as such, the drain and source can often be interchanged. This is particularly the case when implemented on an integrated circuit. When manufactured as a discrete component, the manufacturer determines which terminal is the drain and source.

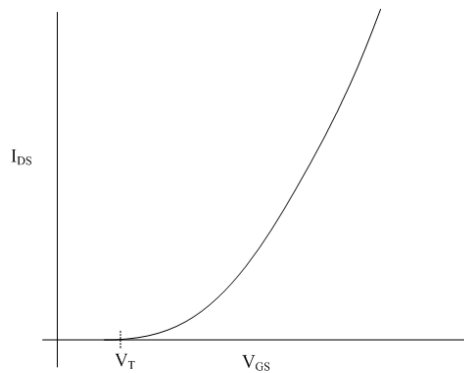
44. All of the MOSFETs considered in this declaration tie the substrate terminal to the source terminal. When configured this way, the terminal where the substrate is connected is considered the source.

45. N-channel MOSFETS conduct current from the drain to the source (conventional current flows into the drain and out the source). The amount of current that flows in a MOSFET is determined by the voltages on all four terminals. When configured with the substrate connected to the source terminal, the amount of current is determined by the potential across the gate,  $V_{GS}$ , and source as illustrated below.



46. The voltage from gate to source,  $V_{GS}$ , must be greater than the threshold voltage of the transistor,  $V_T$ . The manufacturer of the MOSFET establishes the value of the threshold voltage and it will vary from device to device and over temperature. Typical values range from 1 to 3 volts.

47. A MOSFET relationship between the  $V_{GS}$  and  $I_{DS}$  is illustrated in the figure below, where the voltage from gate to drain,  $V_{GD}$  is less than  $V_T$ . The transistor operating in this way is referred to the “saturation” region of operation. In this mode, the relationship between the current and the voltage follows a more or less square law (meaning that the current increases as the square of the gate-source voltage).



48. Once the voltage  $V_{GD}$  is greater than  $V_T$ , the transistor begins to operate in what is called the “linear” region (some prefer to call this the “non-saturation” region, *See CMOS: Chapters 2,3*). When used as switches (e.g., in a

DC-DC converter), it is important to operate them in the linear region to get maximum performance. Therefore, it is important to drive the gate voltage of the MOSFET above the drain voltage by at least the threshold voltage,  $V_T$ .

Understanding this makes it clear why bootstrap circuits are important elements of DC-DC converters such as those discussed in this declaration.

## **B. Comparator**

49. Comparators are a widely used component that detects and indicates the relationship between its two inputs. A symbol for a comparator is shown in Fig. 1 below, but can be illustrated in other ways as well.

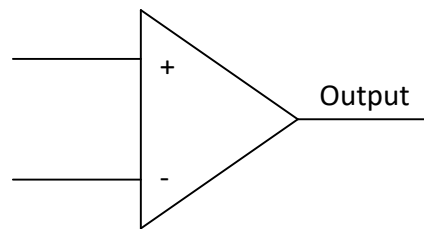


Fig. 1

50. The inputs are characterized as the positive input and the negative input. Sometimes also referred to as the non-inverting and inverting inputs, respectively. A comparator generally has, but is not limited to, a single output that indicates the relationship between the input signals at the positive and negative inputs. If the positive input is greater than the negative input, then the output of the comparator will be high. Alternatively, if the positive input is less than the negative

input, then the output of the comparator is low. Theoretically for an ideal comparator, if the inputs are equal, the output is indeterminate. The ideal transfer curve for a comparator is shown in Fig. 2 below. (CMOS: Fig 8.1-2).

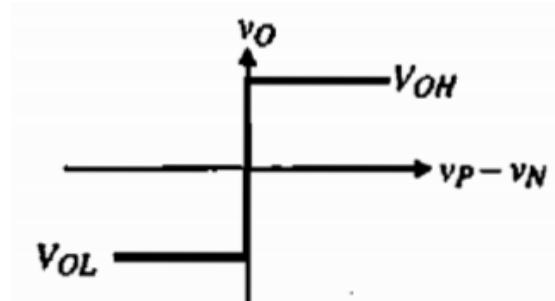


Fig. 2

51. Comparators, like all electronic devices, are subject to noise—both internal and external noise. When comparators are intrinsically noisy, or are placed in a noisy environment they can “chatter” when the input is close to the switching threshold (comparator threshold). This is illustrated in Fig. 3 below. (CMOS: Fig 8.4-6a).

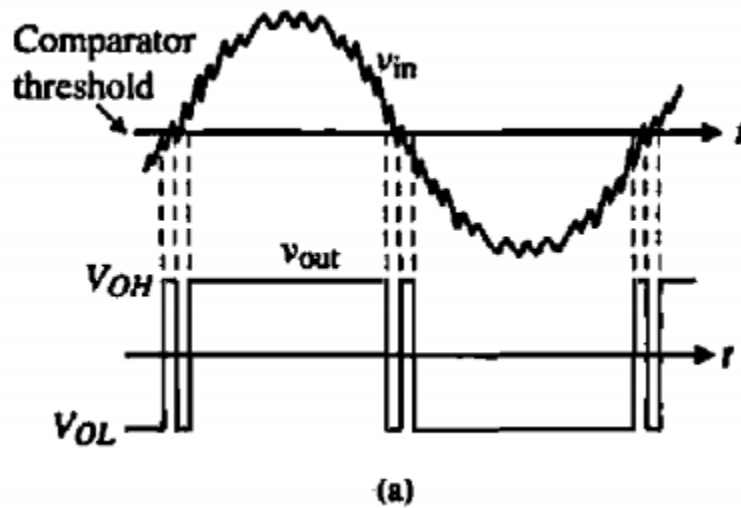


Fig. 3

52. As seen in Fig. 3, due to the noise on  $v_{in}$  (the positive input terminal of the comparator), at the comparator threshold, the noise of the signal bounces above and below the threshold, causing the signal at the output ( $v_{out}$ ) to switch quickly or “chatter” between  $V_{OH}$  and  $V_{OL}$ , in some instances, multiple times depending upon the frequency of the noise on the input signal. One of the methods to avoid this “chatter” on a comparator output is to add hysteresis to the transfer function curve of the comparator. To add hysteresis, the trip threshold of the comparator is varied based on the state of the comparator. This can be understood as follows.

When the input signal to the comparator is rising, the state of the comparator does not change until the input signal reaches a positive trip point threshold ( $V_{TRP}^+$  as shown in Fig. 4 below). Once the state has changed due to the input signal exceeding the threshold, the trip-point threshold is reduced to a negative trip point

so that the state of the comparator output does not change until the input signal falls below the negative trip point ( $V_{TRP}^-$ , as shown in Fig. 4 below). This is illustrated in Fig. 4 below (CMOS:, Fig. 8.4-5).

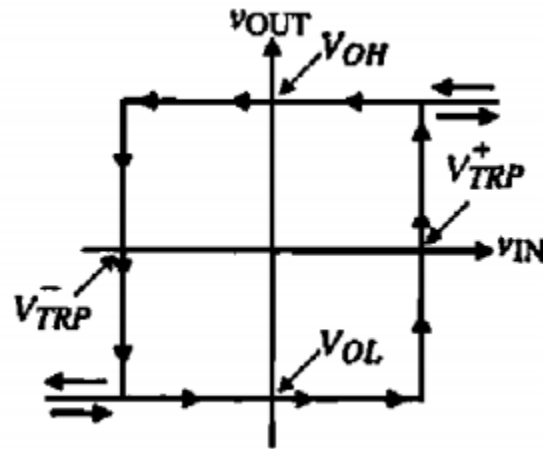


Fig. 4

53. As shown, the input signal,  $v_{IN}$ , starting from the left is low causing  $v_{OUT}$  to be low ( $V_{OL}$  or the “first state”). As  $v_{IN}$  increases to the right, a positive trip point is reached,  $V_{TRP}^+$ . At that point  $v_{OUT}$  goes high ( $V_{OH}$  or the “second state”).  $v_{IN}$  can continue increasing with no change in state. As  $v_{IN}$  starts decreasing, the output,  $v_{OUT}$ , remains high (second state) until it reaches a negative trip point threshold  $V_{TRP}^-$  (which is lower than the initial positive trip point  $V_{TRP}^+$ ) causing the comparator output,  $v_{OUT}$ , to go low (first state).

54. Once hysteresis is introduced to the comparator, the “chatter” effect is removed as long as the noise amplitude on the signal is less than the difference of

the positive and negative trip voltages (i.e., keeping the noise less than the hysteresis “window”). This is illustrated in Fig. 5 below (CMOS:, Fig. 8.4-6b) where the “chatter” on the output signal of the comparator no longer exists.

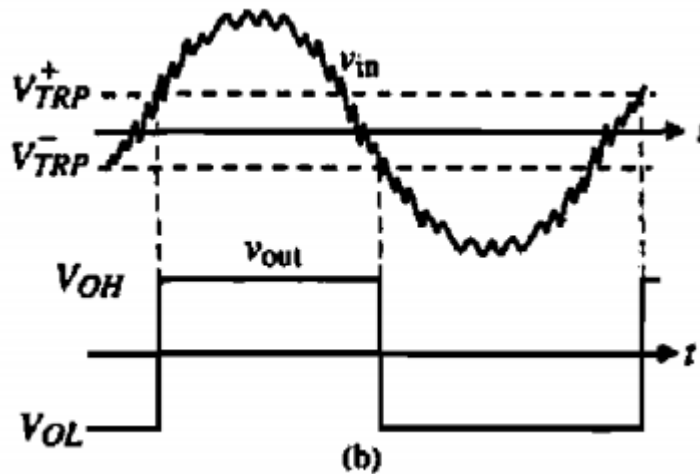


Fig. 5

55. When the signals at the positive and negative inputs cross (e.g., when the positive input becomes greater than the negative input), the state of the comparator output changes (e.g., goes from a low state to a high state in this case). This transition does not happen instantaneously—there is some intrinsic delay. This delay is generally referred to as propagation delay as illustrated in Fig. 6 below (CMOS:, Fig. 8.1-9). In fact, nothing in real-world circuitry happens instantaneously, i.e., without delay.

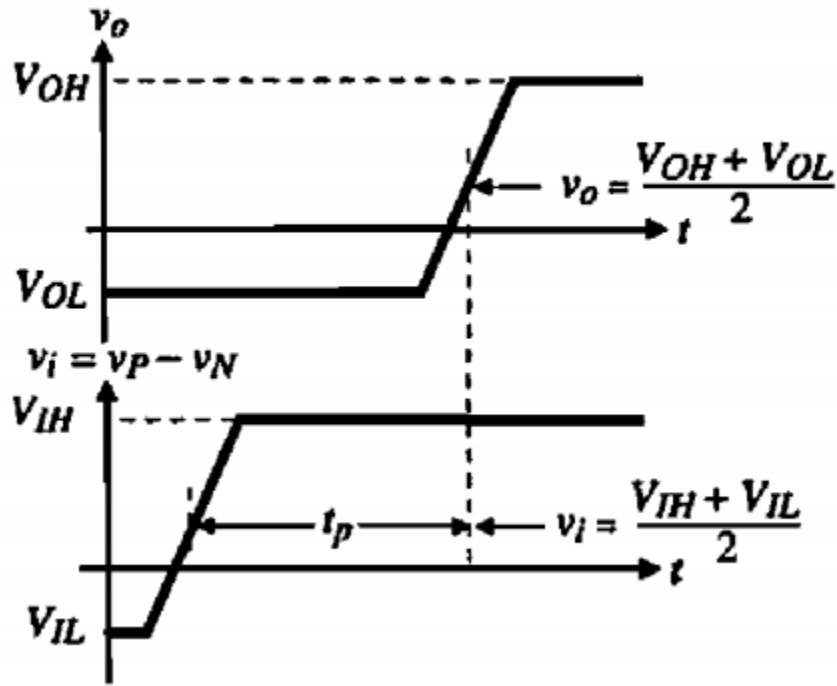
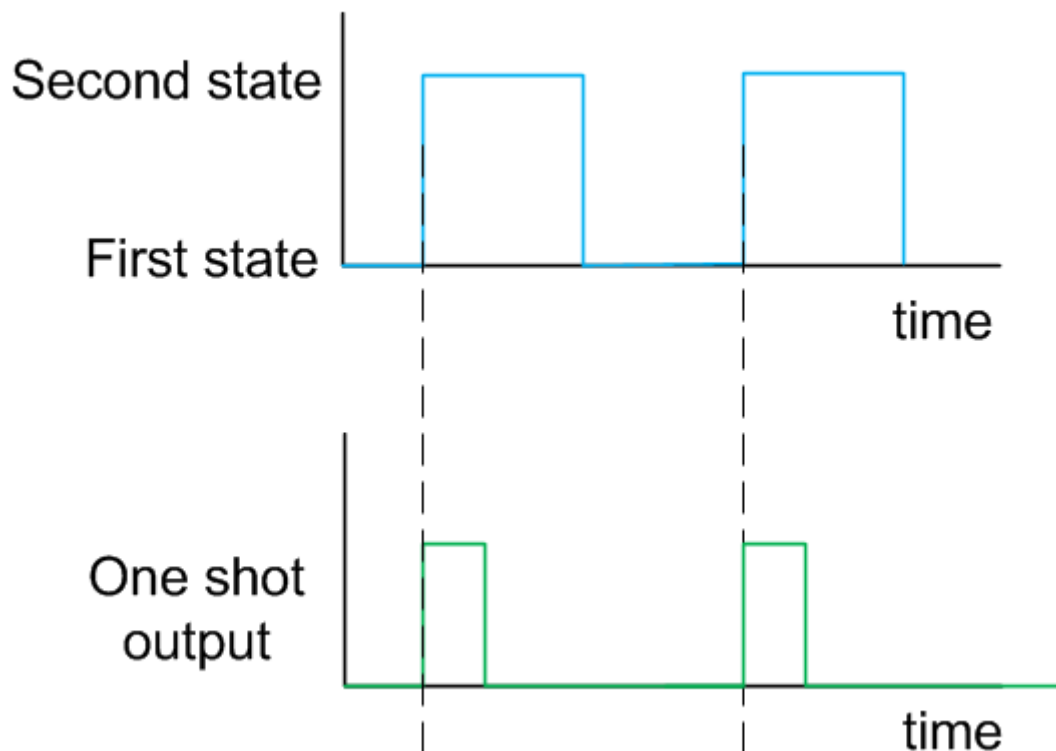


Fig. 6

56. As can be seen in the figure, if the midpoint of the transition is taken as the reference point between the low state and high state of both the input signal and the output signal, respectively, it is clear that a delay of  $t_p$  represents the time delay between the transition at the comparator input and the corresponding signal transition at the comparator output. This delay,  $t_p$ , represents a delay associated with the various internal circuitry of the comparator to effectuate the corresponding signal transition at the output in response to the transition at the comparator input. Comparators are ubiquitous circuits used to compare one signal with another and provide an output based on the comparison.

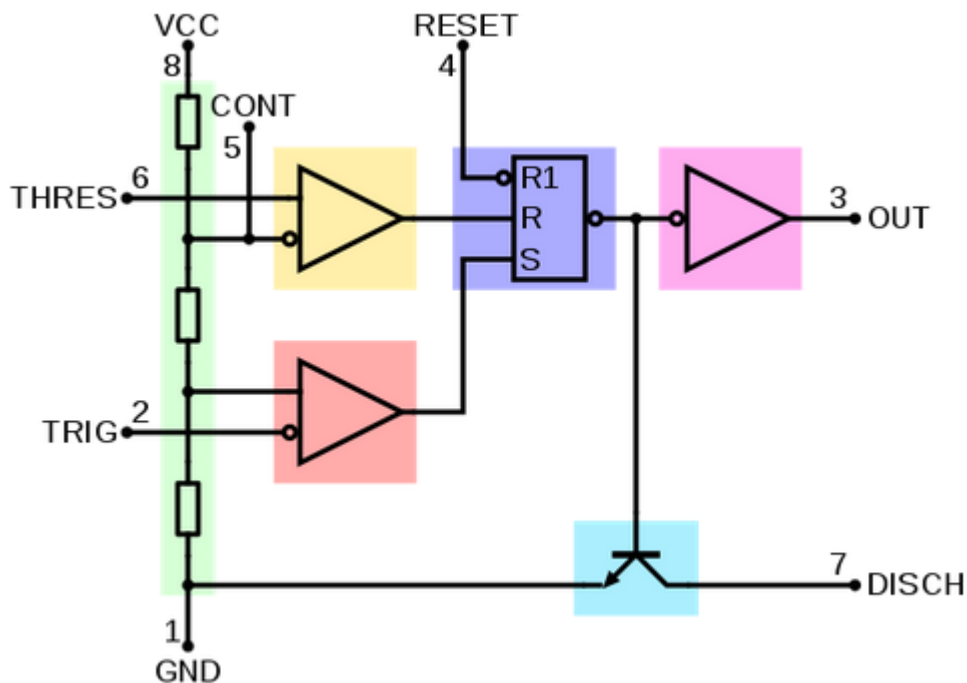
### C. One Shot

57. A one shot is a well-known circuit that is designed to generate a controlled pulse when its input transitions from a first state to a second state. Generally, the one shot will only generate a pulse for one polarity of state change, i.e., a pulse will be generated when the input changes from a first state to a second state but not generate a pulse when the input changes from a second state to a first state as illustrated in the figure below.



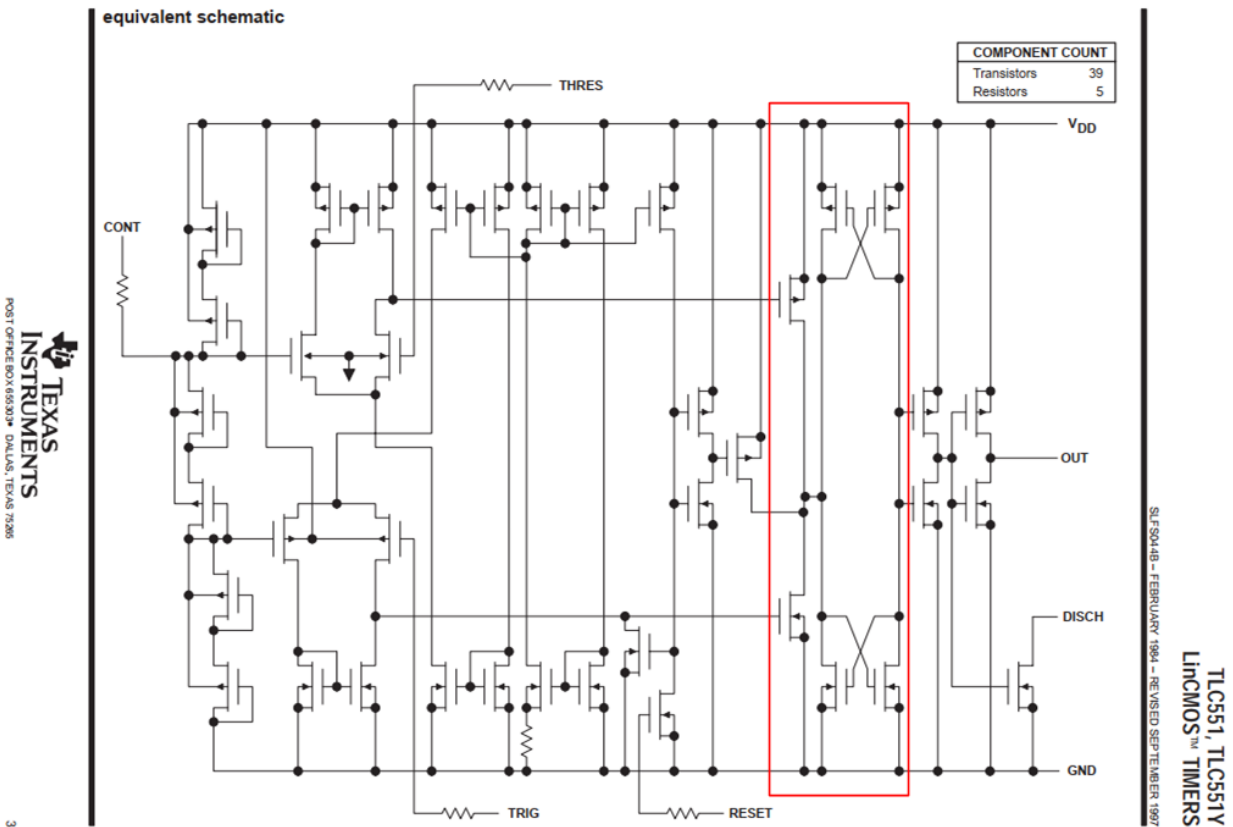
58. When confronted with a need to implement a one-shot, one of the first circuits a POSITA would investigate would be the ubiquitous 555 timer which was

invented in 1971 and is still being manufactured today. The 555 timer would have been well known to a POSITA at the time of filing of the '608 patent application. The 555 timer IC is described in a data sheet from my personal library, which is included as EX1033 in the associated Petition. I have been familiar with the 555 timer IC and the contents of the data sheet since at least 1997. On May 5, 2024, I retrieved the block diagram of the 555 timer shown below from [https://en.wikipedia.org/wiki/555\\_timer\\_IC](https://en.wikipedia.org/wiki/555_timer_IC). Based on my personal knowledge, the diagram provided below properly illustrates the 555 timer.

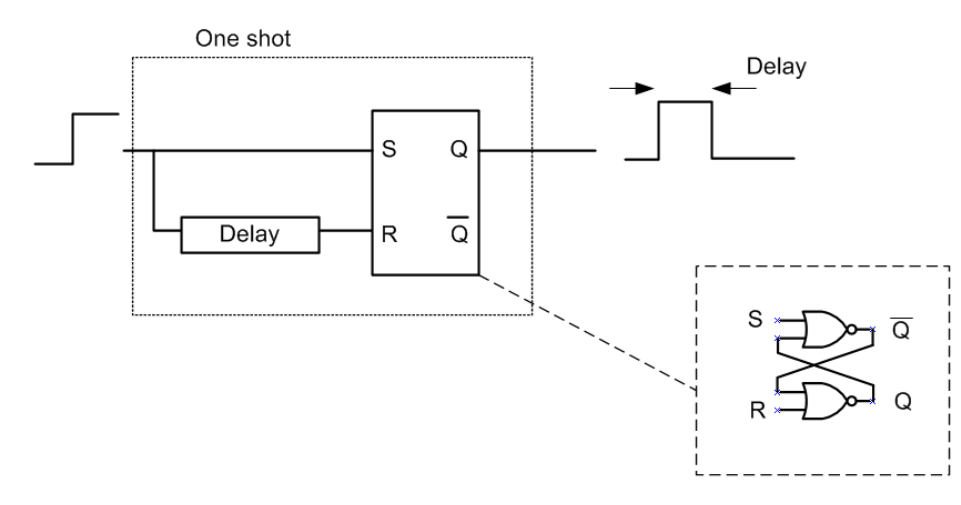


59. A POSITA would recognize that there is more circuitry in the 555 timer than necessary to implement a one-shot but the concepts underlying the 555

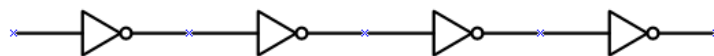
one-shot could be used to implement a simpler circuit. For example, internal circuitry of the 555 (*see* equivalent schematic below from page 3 of EX1033) includes a CMOS cross-coupled latch (highlighted in RED), which is functionally equivalent to an SRFF (cross-coupled NOR gates) in this application.



60. It would be obvious for a POSITA to use this SRFF concept and a delay block to implement the circuit as shown below.



61. The delay element can be implemented in a variety of ways. For example, a series of inverters can be used to implement a delay of an amount equal to the sum of their propagation delays as illustrated in the figure below. Alternatively, a timer/delay chip may provide for a fixed or configurable delay.



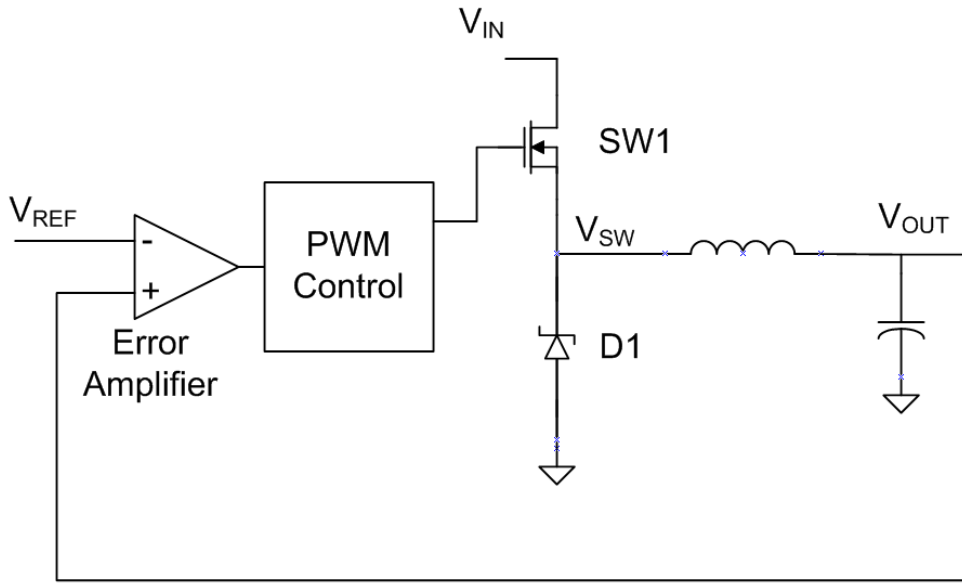
62. When the input to the one-shot circuit goes high, the non-inverting output of the SRFF (Q) is set high, causing the output of the circuit to remain high until the SRFF is reset after the delay period.

#### **D. DC-DC Converters**

63. DC-DC converters are also known by other names: Switch Mode Power Supply, (SMPS), switching regulator, switching power supply, switch-mode converter, DC/DC converter, and perhaps other names as well. These devices

improve on the efficiency of linear converters (also called linear regulators) in that switch-mode converters consume less power than linear regulators in most conditions. A DC-DC converter takes an input and supplies an output. If the output is greater than the input, it is a step-up converter generally called a Boost converter whereas, if the output is less than the input, it is a step-down converter generally called a Buck converter.

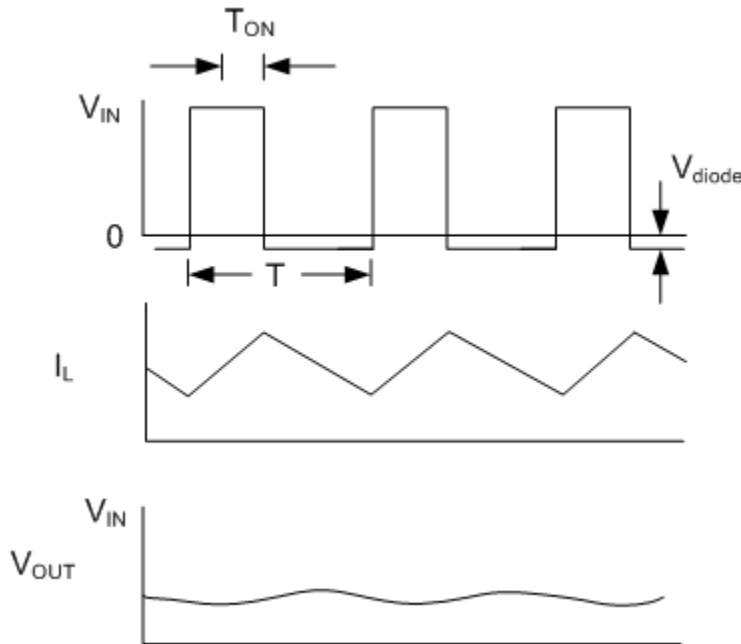
64. A simplified model of a step-down SMPS (Buck converter) is shown in the figure below. (*See* Dubhashi: Fig. 1, Goder: Fig. 1, and Schoneman: Fig. 1.) At a high level, it operates as follows. A Pulse-Width-Modulated (PWM) signal turns switch SW1 on and off, generating a PWM voltage at the output of the switch. This switch-node voltage is filtered by the LC circuit to yield an output voltage that is an average of that PWM voltage. An error amplifier compares a signal representing this output voltage to a reference voltage ( $V_{REF}$ ) representing a desired output voltage. The error amplifier produces a difference signal representing the difference between the output voltage and the desired output voltage, and the difference signal is fed back to the PWM generator. Based on the difference signal, the PWM generator continually adjusts its duty cycle (*infra* ¶67), to maintain the output voltage at the desired value. Details of this operation are as follows.



65. When the switch, SW1, is closed, a voltage,  $V_{IN}-V_{OUT}$ , is imposed across the inductor and a linearly increasing current flows in the inductor toward the load (at  $V_{OUT}$ ). When SW1 is opened, current continues to flow in the inductor (in the same direction, but decreasing over time) causing the voltage at node  $V_{SW}$  to go negative, turning on the diode, which is functioning as a switch (*see* Wait pp 332,333, and Schoneman: 1:26). Current continues to flow while decreasing in magnitude. On a subsequent command of the PWM controller, switch SW1 is turned on again cause  $V_{SW}$  to increase. This cycle repeats at the duty cycle established by the PWM controller. The LC circuit averages the voltage variations at  $V_{SW}$  to produce  $V_{OUT}$ , which is fed to the error amplifier for comparison with  $V_{REF}$ . The output of the error amplifier tells the PWM controller to adjust the duty

cycle accordingly. If  $V_{OUT}$  is lower than  $V_{REF}$ , the duty cycle is increased while if  $V_{OUT}$  is greater than  $V_{REF}$ , the duty cycle is decreased.

66. The figure below illustrates the waveforms of the Buck converter described above.



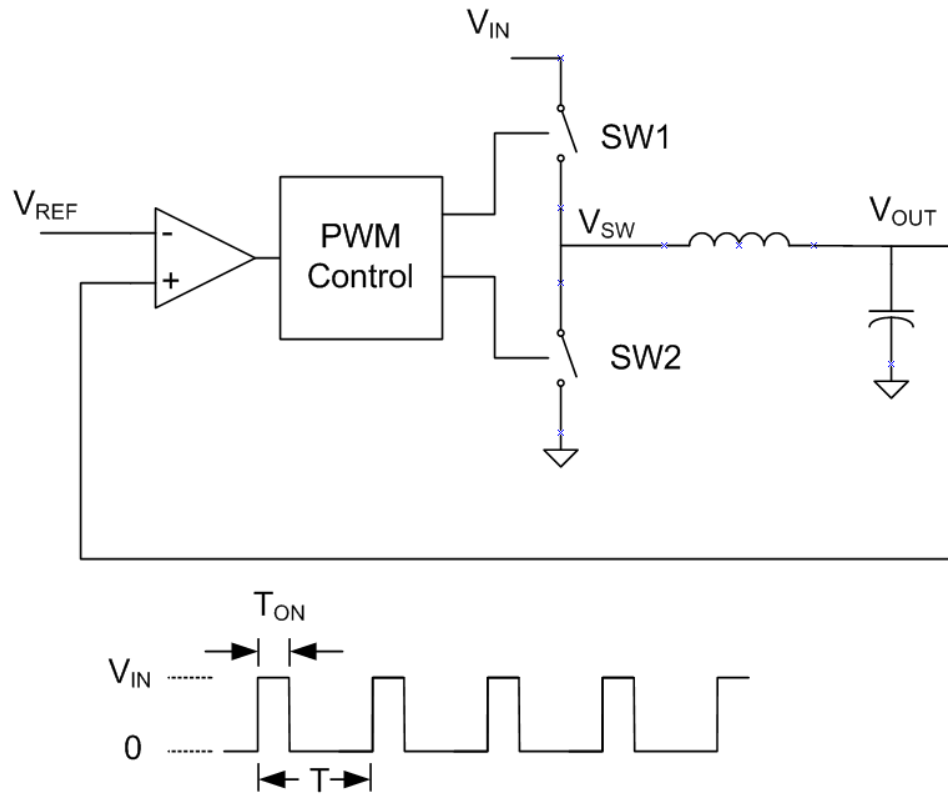
67. The average output voltage,  $V_{OUT}$ , is a function of the duty cycle,  $D = t_{ON} / (t_{ON} + t_{OFF})$ . In particular,  $V_{OUT} / V_{IN} = D$ . The diode in this buck converter acts as a voltage-controlled switch. *See Schoneman: 1:26.* When the voltage at node  $V_{SW}$  goes below ground, the diode switches on, holding the voltage at  $V_{SW}$  to be a diode drop below ground.

68. While this architecture is very simple, one down side is that the diode dissipates power when it is on. An improved solution with better efficiency,

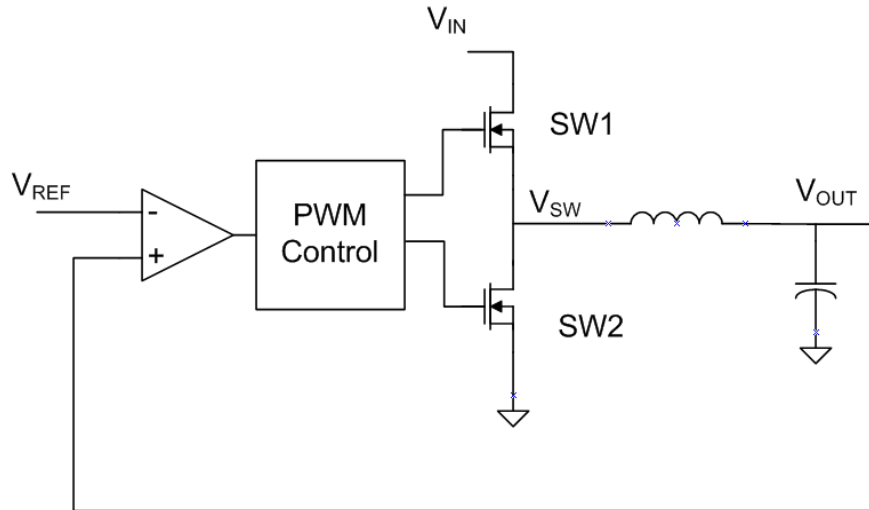
though more complex, is to use a synchronous rectifier. *See* Dubhashi: ¶0021 and Schoneman: 1:49-59. A synchronous rectifier is merely a switch driven in the opposite phase as the high-side switch.

69. A buck SMPS using a synchronous rectifier is shown below. It works as follows. An output voltage is compared to a reference voltage,  $V_{REF}$ , and a PWM (Pulse Width Modulator) controller alternately turns on switches SW1 and SW2 (SW1 switches  $V_{SW}$  to  $V_{IN}$  and SW2 switches  $V_{SW}$  to ground) at an appropriate duty cycle such that the average value of  $V_{SW}$  is equal to  $V_{REF}$ . The average value is determined by the ratio of the on time of SW1 ( $T_{ON}$ ) to the period of the waveform ( $T$ ). If the output voltage,  $V_{OUT}$ , is decreased from its normal (desired) output, the feedback voltage will necessarily fall below  $V_{REF}$ , and the PWM controller will increase the duty cycle accordingly to increase  $V_{OUT}$ . Similarly, if the output voltage increases such that the feedback voltage increases above  $V_{REF}$ , the PWM controller will decrease the duty cycle in order to decrease  $V_{OUT}$ . The averaging is accomplished by the low-pass filter comprising the inductor and capacitor. The output voltage is, thus,  $V_{IN} * T_{ON} / T$ . In addition to the above described “normal operation” of the voltage converter, certain other modes of operation for DC-DC converters were well known prior to the effective filing date of the '608 Patent. For example, to reduce inrush current and protect the internal circuitry during startup, a “soft start” or “slow start” sequence is often

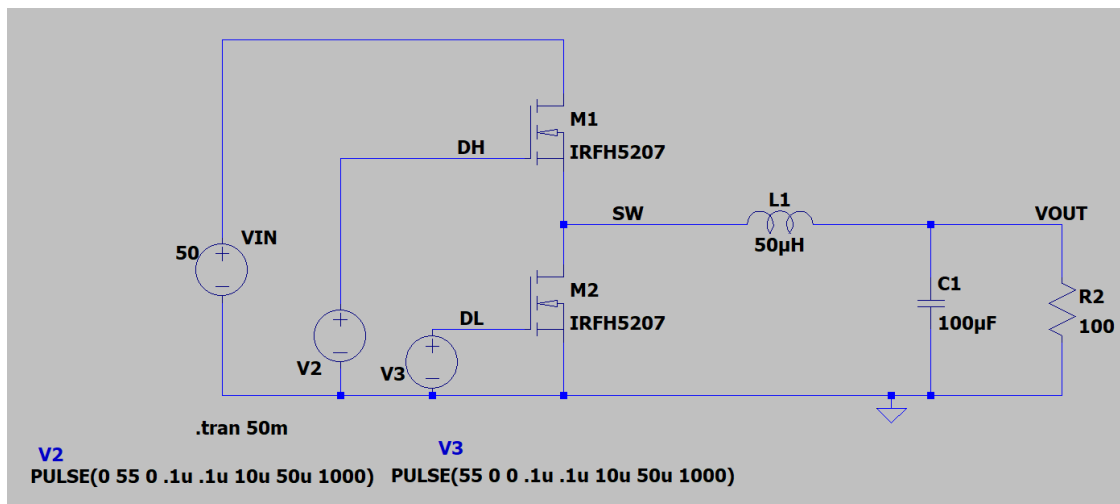
used. This soft-start sequence performs a controlled ramp of the reference voltage (over a period of time) up to the final  $V_{REF}$ , causing  $V_{OUT}$  to similarly ramp up to the desired target value. That is, the ramping threshold voltage causes the threshold to be greater than the feedback signal (representing  $V_{OUT}$ ). In response, the error amplifier and PWM controller will alternately turn on and off the high-side and low-side switches based on the difference between  $V_{OUT}$  and the ramping threshold, causing  $V_{OUT}$  to follow the ramping threshold to the desired value. This switching naturally refreshes and recharges the bootstrap capacitor. EX1006, 10, 14; EX1022, 10, 12-13. In another example operating mode, DC-DC converters may inhibit or “skip” one or more PWM cycles to achieve higher efficiency. For example, during light current loads, a converter may completely turn off or inhibit the high-side and low-side switches to reduce switching and gate-drive losses. While in this pulse-skipping mode, the output voltage will begin to decay at a rate that depends on the load. After the output voltage falls below the desired output, the converter will resume normal operation. That is, the converter will exit the pulse-skipping mode. At that point, the feedback signal (representing the output voltage) will necessarily be less than the threshold (representing the desired output voltage). In response, the converter will resume operating the high-side and low-side switches to recover  $V_{OUT}$ . This operation of the switches naturally refreshes and recharges the bootstrap capacitor. EX1022, 10-11.



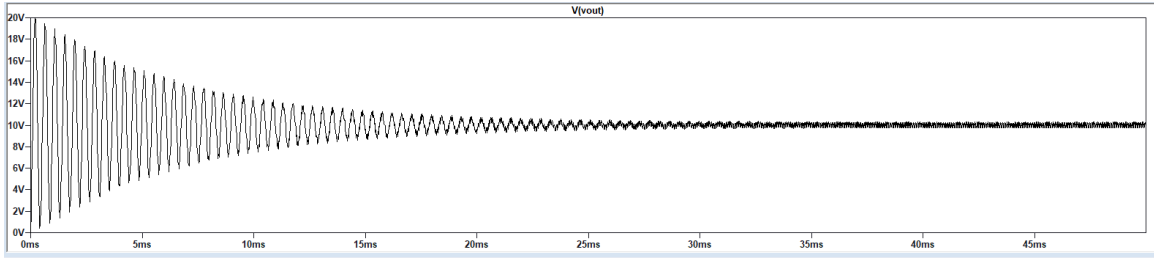
70. In actual SMPS circuits, the switches, SW1 and SW2, are implemented with transistors. Typically, these transistors are N-channel MOSFET transistors as illustrated in the figure below.



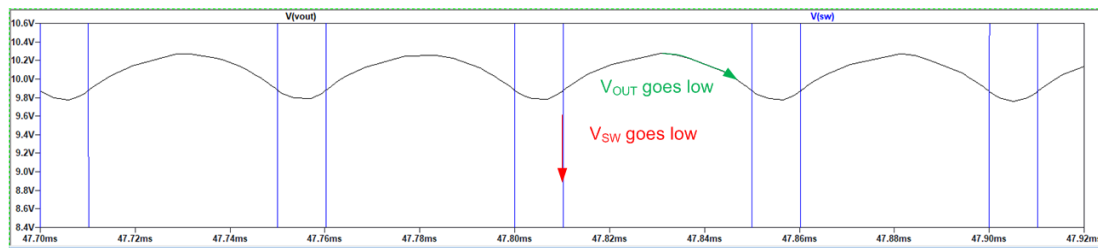
71. In order to illustrate the operation, I have simulated a simplified model of a SMPS below using LTSPICE [appendix A]. A fixed duty cycle  $T_{ON}/T = 1/5$  was applied with an input voltage of 50 volts, giving an average output voltage of  $50 \times 1/5 = 10$  volts.



72. Simulation results plotting the node  $V_{OUT}$  are shown below. The output converges to 10 volts as expected for the given duty cycle.



73. An additional plot from the same simulation is shown below. Both nodes SW and  $V_{OUT}$  are plotted at a point in time where the output is converged around 10 volts.



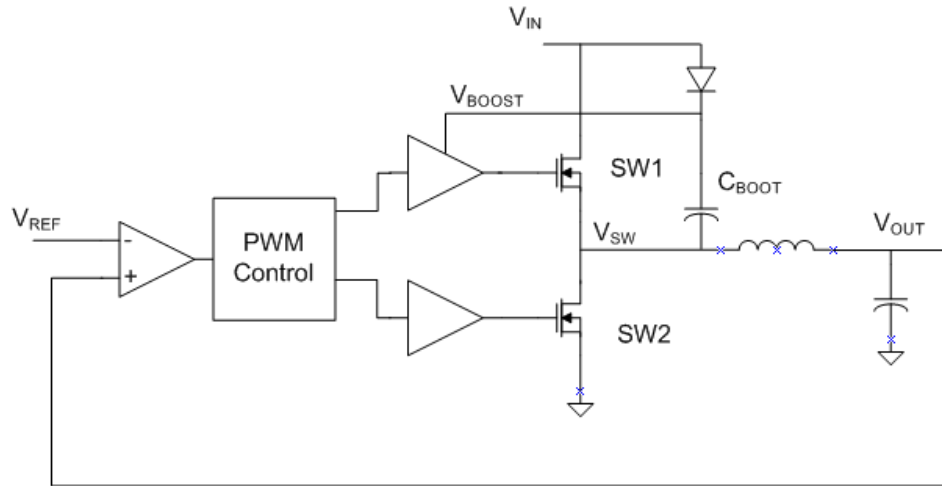
74. It is observed, as expected, that when  $V_{SW}$  goes low, it necessarily causes the output ( $V_{OUT}$ ) to go low as well, though delayed by the LC filter.

75. For a MOSFET to operate as a switch, a sufficient voltage must be available at the gate relative to the channel of the transistor in order for it to turn on and provide a short circuit between the drain and source. In order to turn on an N-channel MOSFET (in the linear region of operation), it is necessary that the gate voltage be greater than the drain/source voltage by some amount. That amount is the threshold voltage of the transistor,  $V_T$ . Because  $V_{IN}$  will be greater than  $V_{OUT}$  in this application, the gate voltage must be greater than  $V_{IN} + V_T$  in order to turn the

transistor on in the linear region. If the highest voltage available to the SMPS is  $V_{IN}$ , then there is insufficient voltage available to drive the MOSFET into the linear region and operate as a switch. *supra* §III.A.

76. In order to address the need for a higher gate drive voltage, the concept of a bootstrapped driver was developed. The concept was not new to SMPS applications as it was a common technique used in N-channel integrated circuits in the 1970's. The idea is to charge a bootstrap capacitor with a sufficient voltage and then boost that voltage to achieve enough gate drive for the N-channel switch.

77. An example of an SMPS using a bootstrap capacitor is shown below. The gate driver of SW1 is powered by a bootstrap capacitor,  $C_{BOOT}$ . Each time, once the SW2 is turned on (and SW1 is turned off),  $C_{BOOT}$  is charged to  $V_{IN}$  (ignoring the forward voltage of the diode). Then, when SW1 is turned on (and SW2 is turned off),  $V_{BOOST}$  increases to  $2*V_{IN}$ , thus providing ample amount of gate voltage to drive SW1 into the linear region of operation. As long as, during each PWM period, the low-side switch (SW2) turns on for sufficient enough time, the bootstrap capacitor will be refreshed (recharged).



78. The breadth of switch-mode power supply technology is huge, but this brief overview of a particular style of converter is sufficient to understand the '608 patent and the prior art presented. Furthermore, I have reviewed exhibits EX1005, EX1006, EX1007, EX1009, EX1010, EX1011, EX10017, EX1019, EX1020, EX1021, EX1022, and EX1023. It is my opinion that these references all describe examples of switch-mode power supplies that would have been well known in the art before the effective filing date of the '608 patent. EX1005, 1:8-10, Figs. 1-2; EX1006 at 1, 6; EX1007, 1:9-15, Figs. 1, 3, 6; EX1009, 1:5-10, Fig. 1; EX1010, ¶¶[0002]-[0003], Figs. 1, 2A, 2B; EX1011, ¶[0001], Figs. 1-3; EX1017, ¶[0002], Figs. 1-3; EX1019 at 1, 6; EX1020 at 1, 6; EX1021 at 1, 6; EX1022 at 1, 3; EX1023 at 1, 11.

#### IV. OVERVIEW OF THE '608 PATENT

##### A. Brief Description

79. The '608 patent (EX. 1001) is directed to switch-mode power supplies (DC-DC converters). In particular, the '608 patent is directed toward maintaining the voltage across the bootstrap capacitor that provides gate drive to the high-side switch (in a high-side/low-side driver switching arrangement).

80. Admitted prior art of the '608 patent is shown in Fig. 1 of the specification and shown below.

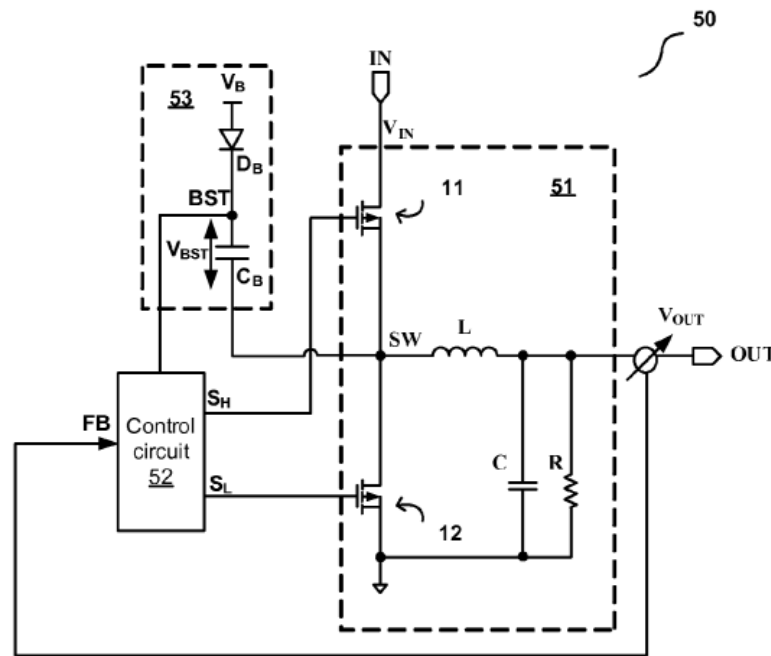


**FIG. 1 (Prior Art)**

81. As shown, high-side and low-side switches 11 and 12, respectively drive inductor L, capacitor C, and resistor R. The output voltage ( $V_{OUT}$ ) is fed back to a control circuit 52 where it is compared to a reference voltage (not

shown), and, based on the comparison, control circuit 52 drives the high-side and low-side switches so as to drive the output voltage to equal the reference voltage. A bootstrap capacitor,  $C_B$ , is included that provides a boosted voltage to the control circuit which the control circuit uses for the gate drive of high-side switch 11. The control circuit drives (in one embodiment) the high-side and low-side switches in a PWM manner.

82. The high-side and low-side driver switches are, N-channel MOSFET switches (the type of switches is obvious from the description even though the symbols are drawn incorrectly in the figures—they are drawn as P-channel MOSFETs).

83. During proper operation of the DC-DC converter, the high-side switch must drive  $V_{IN}$  to the node SW. In order to do this, the gate of the high-side driver must be driven above  $V_{IN}$  by at least a threshold voltage (the threshold voltage of the N-channel transistor). When there is no drive voltage above  $V_{IN}$  available, one must be generated in some fashion. *supra* §III.D.

84. The need for a gate drive greater than  $V_{IN}$  is met by using a bootstrap capacitor. In order for the bootstrap capacitor to be charged (refreshed) fully (enough for the circuit to operate properly), the low-side switch must be on for enough time during each PWM cycle. The '608 patent describes a situation where the input voltage is close to the desired output voltage causing the PWM to operate

at near 100%. In such a situation, the low-side switch is never on long enough to properly charge the bootstrap capacitor sufficiently. Another situation may arise where the DC-DC converter drives a very light load, thus reducing the switching frequency of the high-side and low-side transistors. As in the case of a near 100% duty cycle, the bootstrap capacitor does not have the chance to be fully charged.

85. The '608 recognizes the need to insure that the bootstrap capacitor is fully refreshed so as always able to provide the maximum gate drive to the high-side transistor. The '608 proposes several embodiments to do this. In each embodiment, a bootstrap refresh module is configured to compare the bootstrap voltage signal ( $V_{BST}$ ) with a bootstrap refresh threshold ( $V_{TH1}$ ). *Id.* at 11:3-6 See Fig. 3 below. When the bootstrap voltage signal becomes too low, the bootstrap refresh module decreases the output voltage ( $V_{OUT}$ ) of the voltage converter. *Id.* at 11:11-15. As a result of  $V_{OUT}$  decreasing, the feedback signal (FB) also decreases below  $V_{REF}$  (desired value of the output signal). Therefore, the error amplifier generates a difference signal (EA) which causes the high side and low-side switches to switch normally in order to maintain the output voltage at the desired value. *Id.* at 11:15-25. During this process, the bootstrap voltage is refreshed *Id.* at 11:36-38.

86. In the embodiment of Fig. 3 shown below, the bootstrap refresh module 134 reduces the output voltage ( $V_{OUT}$ ) by operating the low-side switch to

charged for refreshing the bootstrap voltage  $V_{\text{BST}}$ . *Id.* at 15:22-24.



**B. Earliest Priority Date for the Claims**

87. The '608 patent was filed as Application 14/823,900 on Aug 11, 2015. The '608 Patent claims priority to Chinese Patent Application No 201410390708, filed on August 11, 2014. For purposes of my analysis, all Challenged Claims of the '608 Patent have a priority date of August 11, 2014, and that they were effectively filed as of that date.

**V. OVERVIEW OF PRIOR ART**

**A. U.S. Patent No. 7,145,316 to Galinski**

88. Galinski is directed to DC-DC switching voltage converters having a high-side switch and a low-side switch and that require a “bootstrap” voltage to drive the high-side switch. EX1005 at 2:12. In particular, the Galinski is directed to using bootstrap-voltage monitoring to allow the voltage converter to operate at or near 100% duty cycle. *Id.* at 2:44-48. As explained in the description of the related art, a buck voltage converter alternately operates a pair of power switches (a high-side switch and a low-side switch) to produce a switching voltage ( $V_{sw}$ ) at a common node which is coupled to a LC network to generate a relatively constant output voltage  $V_{OUT}$ . *Id.* at 1:20-36.

89. Such voltage converters typically include a feedback control loop formed by dividing down the output voltage  $V_{OUT}$  to provide a feedback voltage ( $V_{FB}$ ) and feeding back the feedback voltage ( $V_{FB}$ ) to an error amplifier where the

feedback voltage ( $V_{FB}$ ) is compared to a reference voltage. *Id.* at 5:56-61. The feedback control loop regulates the output voltage  $V_{OUT}$  at a constant level over changing load conditions by varying the duty cycle of the power switches. *Id.* at 6:2-5. That is, the high-side switch and the low-side switch are turned on alternately to increase or decrease the current through the output inductor. *Id.* at 2:5-8.

90. The power switches may be controlled by driver circuitry. Both the high-side and low-side drivers (Q1 and Q2 respectively) are N-Channel transistors. The high-side driver, Q1, is configured in a source-follower configuration. The source voltage will follow the gate voltage minus a threshold ( $V_{TH}$ ) as long as the transistor is operating in the saturation region. Once the gate voltage rises above the drain voltage by a threshold ( $V_G - V_D > V_{TH}$ ), the transistor will enter the “linear” region of operation. *See* §III.A Once the transistor enters the linear region, the source and drain will be at approximately the same voltage (depending on factors such as transistor size, geometry, and parasitic resistance). For converters such as shown in Galinski Fig. 1 (below), it is most desirable for the high-side transistor be driven into the linear region during operation. This is only possible if the gate can be driven above  $V_{IN}$ . To accomplish this, the high-side driver is supplied by the “bootstrap” voltage to drive the high-side switch. *Id.* at 6:50-6:52. The low-side driver may be supplied by a voltage between  $V_{IN}$  and ground. *Id.* at

6:52-6:54. The bootstrap voltage may be generated during the switching of the high-side and low-side switches, avoiding the need for a separate higher supply voltage. *Id.* at 2:8-13. An exemplary circuit is shown in Fig. 1, reproduced below.

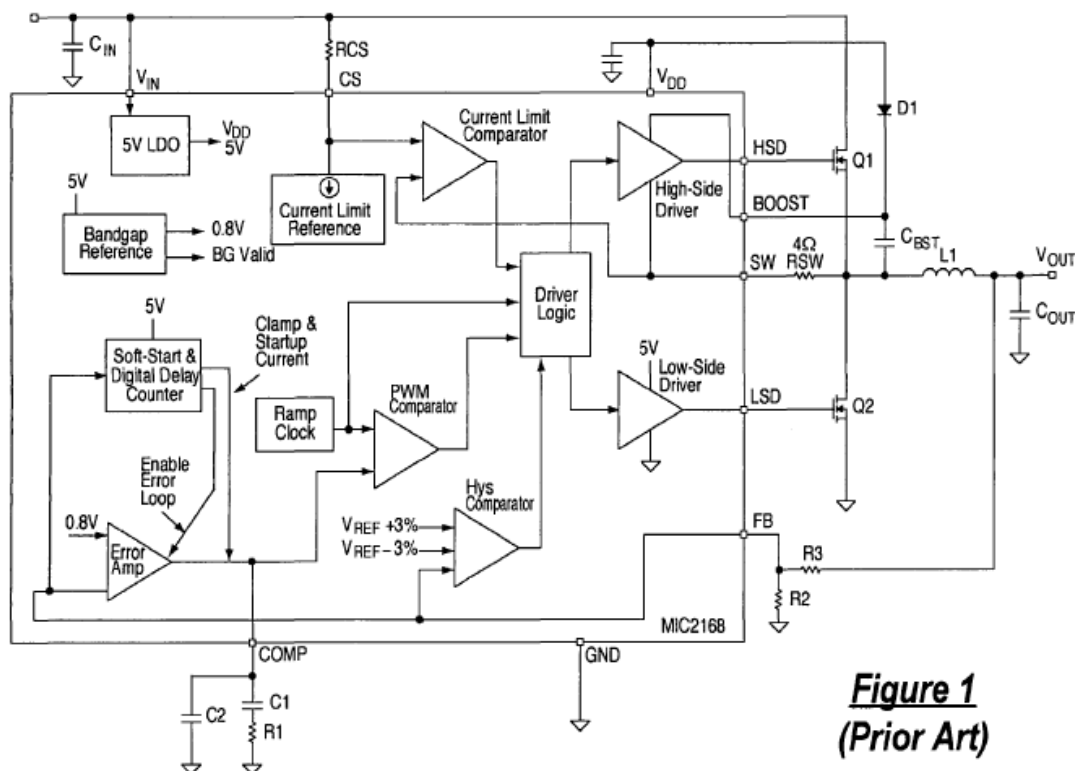


**Figure 1**  
(Prior Art)

91. Fig. 1 shows an example integrated circuit coupled to discrete high-side and low-side power switches (Q1, Q2) which are external to the controller integrated circuit. *Id.* at 4:57-59. As shown, the controller includes the driver circuitry associated with each switch. Each driver circuit receives a logic signal from the driver logic block, and the high-side driver also receives the bootstrap voltage (BOOST). *Id.* at 2:7-13. The driver logic block, in turn, receives a control

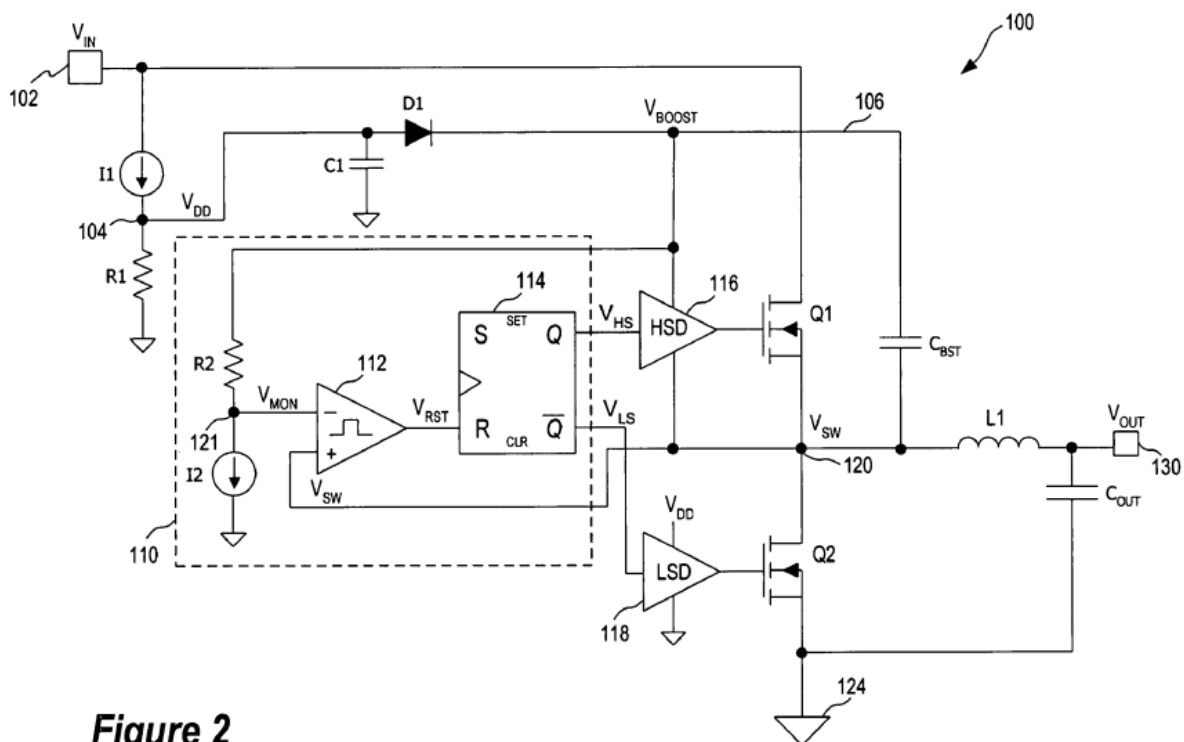
signal from a comparator circuit which receives the feedback signal ( $V_{FB}$ ) and one or more reference voltages. The comparator circuit compares the feedback voltage ( $V_{FB}$ ) to one or more reference voltages to produce a control signal, which is received by the driver logic block. *Id.* 5:56-6:2. Based on the control signal, the driver logic block alternately operates the power switches to regulate the output voltage ( $V_{OUT}$ ). *Id.* at 11:1-9.

92. The power switches are alternately turned on and off at a given duty cycle to achieve the desired  $V_{OUT}$ . This on/off duty cycle is commonly referred to as Pulse Width Modulated (PWM) control. *supra* ¶64.

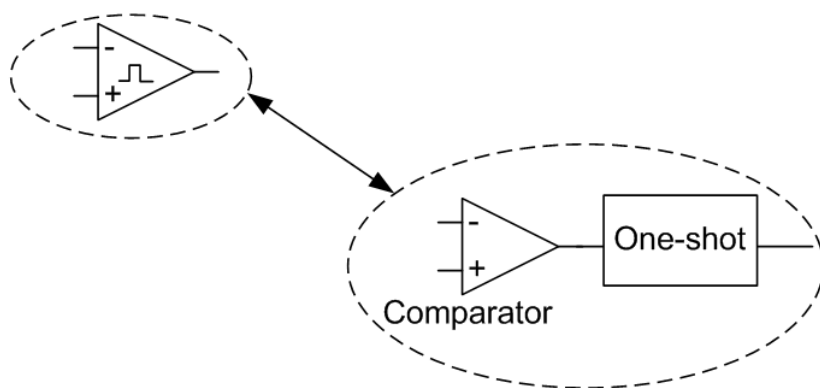
93. When the low-side driver is on (and the high-side driver is off), the bootstrap capacitor  $C_{BST}$  is charged through a diode (D1) and  $V_{DD}$ . EX1005 at 7:42-65. Making the approximation that the voltage drop across the diode is zero (normally around 0.7 volts),  $C_{BST}$  is charged to  $V_{DD}$ . When the low-side driver is turned off and the high side-driver is turned on, the high-side driver is driven into the linear region as the voltage at the BOOST node is driven to  $V_{DD} + V_{IN}$ . The bootstrap capacitor and associated circuitry play a critical role ensuring that the high-side driver is driven into the linear region and, thus, driving the common node of the two driver switches to  $V_{IN}$  when the high-side driver is on. In order for this bootstrap circuit to work properly, however, the low-side driver must be turned on

regularly and for a sufficient period of time because the charge on  $C_{BST}$  will leak (decay, or decrease) away unless it is regularly refreshed.

94. In some operating conditions, the output voltage ( $V_{OUT}$ ) may be set very close to the input voltage ( $V_{IN}$ ). *Id.* at 1:56-58. Under these conditions, the converter may not naturally cause the switches to alternate often enough (near 100% duty cycle) to maintain the bootstrap voltage. Thus, the bootstrap voltage may decay or decrease over time until it is no longer able to drive the high-side switch into the linear region. *Id.* at 2:15-24. This issue is addressed by incorporating a bootstrap voltage control circuit in the voltage converter for monitoring and periodically refreshing the bootstrap voltage. *Id.* at 2:44-49. In particular, when the monitored bootstrap voltage decays below a predetermined level, the control circuit causes the converter to operate the switches for a short time to refresh the bootstrap voltage. *Id.* at 4:4-11. Control signals from the feedback loop described above are logically combined with output signals from the bootstrap voltage control circuit to provide the final control signals for the high-side and low-side driver circuits. *Id.* at 6:8-13. Therefore, the output signals of the bootstrap voltage control circuit serve to modify or override the nominal feedback-control signals. FIG. 2 (below) is a circuit diagram of a control circuit for monitoring and maintaining the bootstrap voltage incorporated in an N-channel buck switching voltage regulator. *Id.* at 5:3-8.

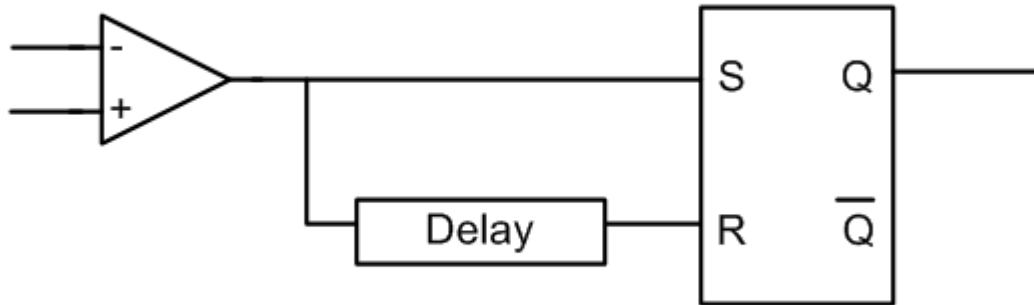


95. As shown, the bootstrap voltage control circuit includes a one-shot comparator and associated elements that act collectively to compare the bootstrap voltage ( $V_{\text{BOOST}}$ ) to a threshold voltage. *Id.* at 8:30-67. A POSITA would understand the one-shot comparator comprises a comparator element (*supra* §III.B) followed by a one-shot circuit *supra* §III.C as shown below.



96. Based on the inputs to the comparator, the output of the comparator element would be one of two states. *supra* §III.B. A one-shot circuit element is well known in the art and operates to provide an output pulse when the input changes state (either low to high, or high to low). *supra* §III.C. Galinski teaches that, when the non-inverting input ( $V_{SW}$ ) goes above the inverting input ( $V_{MON}$ ), the comparator generates a pulse. EX1005 at 9:3-7.

97. Furthermore, it would be obvious to a POSITA how to implement a one-shot from other logic devices, such as timer/delay chips, latches, flip-flops, and so on. That is, a POSITA would understand that one obvious implementation of Galinski's one-shot comparator is the circuit shown below. *supra* ¶95, §III.C.



98. As shown, comparator circuit 112 receives the switching output voltage  $V_{SW}$  (node 120) on its non-inverting input terminal and  $V_{MON}$  a scaled down voltage of bootstrap voltage  $V_{BOOST}$  on its inverting terminal. The voltage,  $V_{MON}$ , is derived from current source  $I2$  and resistor,  $R2$  such that  $V_{MON} = V_{BOOST} - I2 \cdot R2$ . *Id.* at 8:35-42. The voltage  $V_{MON}$  is selected to establish a minimum bootstrap voltage  $V_{BOOST-MIN}$  greater than a voltage  $V_{IN} + V_{TH\_HS}$ , where  $V_{TH\_HS}$  is the threshold voltage of high-side switch  $Q1$ , so that high-side driver circuit 116 can drive high-side switch  $Q1$  properly (i.e., drive the high-side transistor into the linear region of operation). *Id.* at 8:64-52. In the embodiment shown in FIG. 2, the scaling of the bootstrap voltage  $V_{BOOST}$  is accomplished by resistor  $R2$  biased by current source  $I2$ , although it is possible to use other circuit configuration to realize the voltage feedback and divide function. *Id.* at 8:54-67.

99. The one-shot comparator, 112, compares  $V_{MON}$  to  $V_{SW}$ . The point at which the comparator switches is when  $V_{MON} = V_{SW}$ , substituting yields  $V_{BOOST} - I_2 \cdot R_2 = V_{SW}$ . In order for transistor Q1 to operate in the linear region, the gate voltage must be driven above  $V_{IN}$  by a voltage equal or greater than the threshold voltage of the high-side transistor ( $V_{TH\_HS}$ ):  $V_{IN} + V_{TH\_HS}$ . Since the drive of the high-side transistor is  $V_{BOOST}$ , then  $V_{BOOST}$  must be equal or greater than  $V_{IN} + V_{TH\_HS}$ , in order to function properly.

$$V_{BOOST} = V_{IN} + V_{TH\_HS} \Rightarrow V_{SW} = V_{IN}.$$

A POSITA would understand that the voltage drop across R2 would be designed to be slightly greater than  $V_{TH\_HS}$  ( $V_{TH\_HS}^+$ ). Substituting:

$$I_2 \cdot R_2 = V_{TH\_HS}^+,$$

gives:

$$V_{MON} = V_{BOOST} - V_{TH\_HS}^+.$$

When  $V_{BOOST}$  drops to  $V_{IN} + V_{TH\_HS}$ , then

$$V_{SW} = V_{IN}$$

$$V_{MON} = V_{IN} + V_{TH\_HS} - V_{TH\_HS}^+$$

Thus:

$$V_{MON} < V_{IN} \Rightarrow V_{MON} < V_{SW}$$

Once  $V_{MON}$  is less than  $V_{SW}$ ,  $V_{RST}$  is triggered to refresh the bootstrap capacitor.

100. Therefore, when the bootstrap voltage ( $V_{\text{BOOST}}$ ) is equal to or less than  $V_{\text{IN}} + V_{\text{TH\_HS}}$ , the comparator generates an output pulse ( $V_{\text{RST}}$ ). *Id.* at 9:3-5. In this embodiment, the comparator output ( $V_{\text{RST}}$ ) has a duration sufficient to allow  $C_{\text{BST}}$  to be recharged. *Id.* at 9:5-7. As in the case of the comparator circuit, the specific logic circuitry for generating the drive control signals for the driver circuits is not critical to the practice of the present invention. *Id.* at 9:41-47. Regardless of the specific logic circuitry, power switches Q1 and Q2 are caused to switch, and the bootstrap voltage  $V_{\text{BOOST}}$  is thereby refreshed. *Id.* at 9:17-21. During this recharge phase, the switching output voltage  $V_{\text{SW}}$  switches from input voltage  $V_{\text{IN}}$  to 0 volt temporarily. *Id.* at 10:19-23. As shown in the timing diagram of FIG. 3 (below), the switching output voltage  $V_{\text{SW}}$  dips below the ground voltage. *Id.* at 10:23-24.

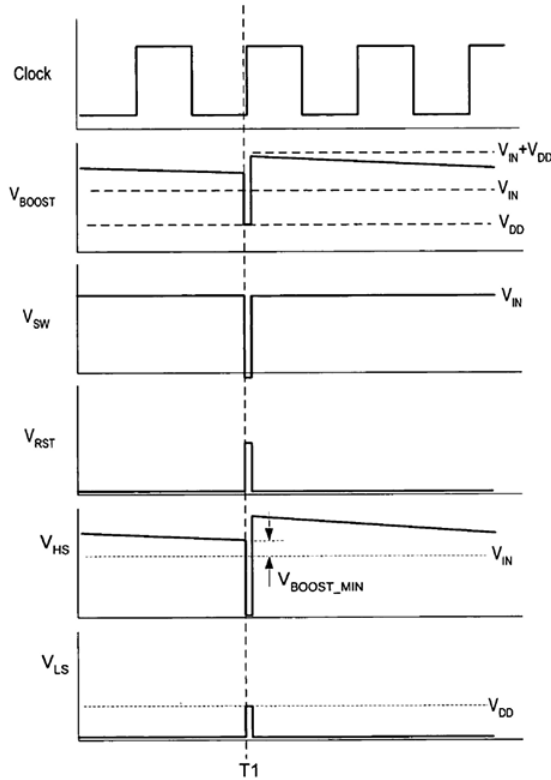


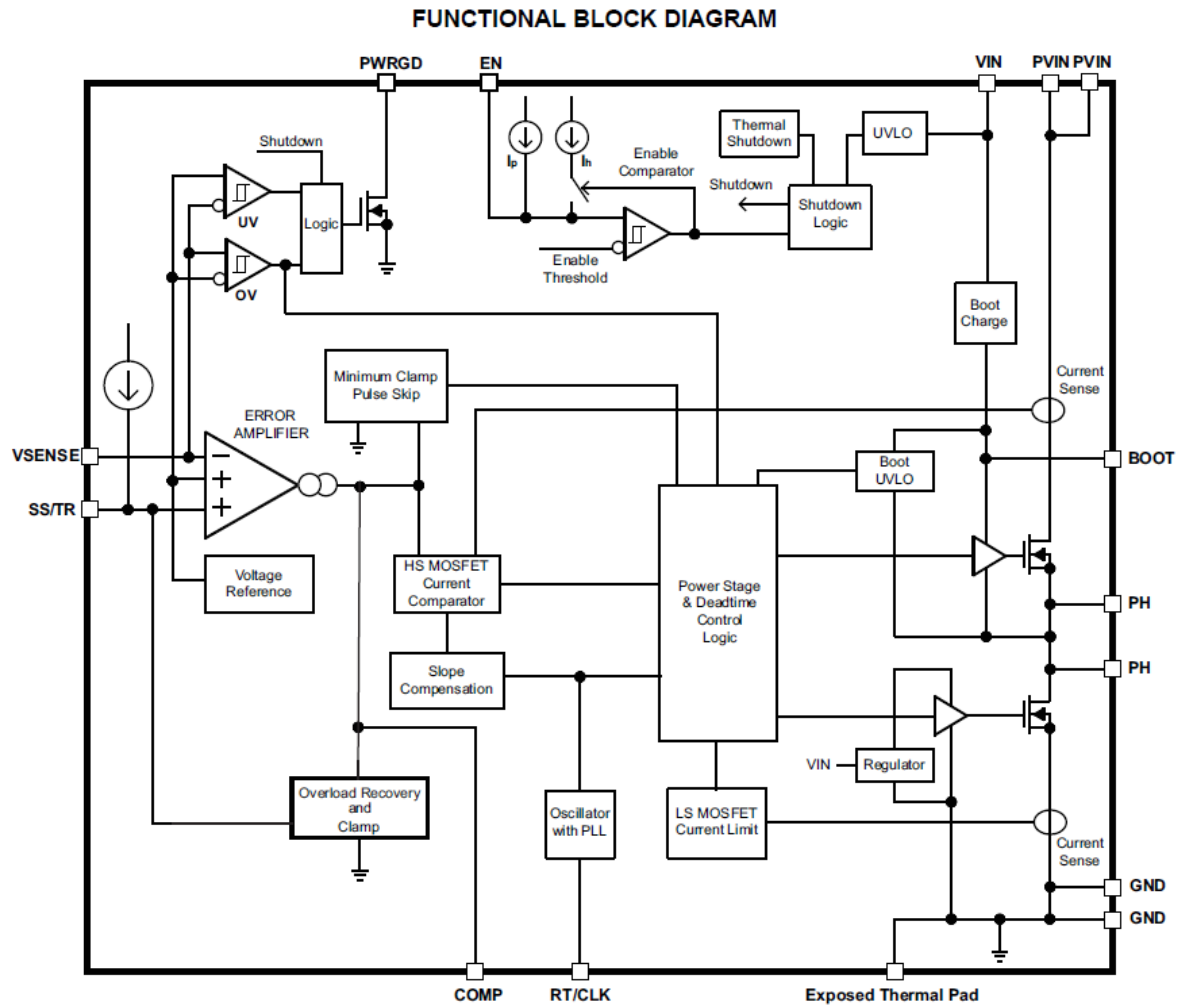
**Figure 3**

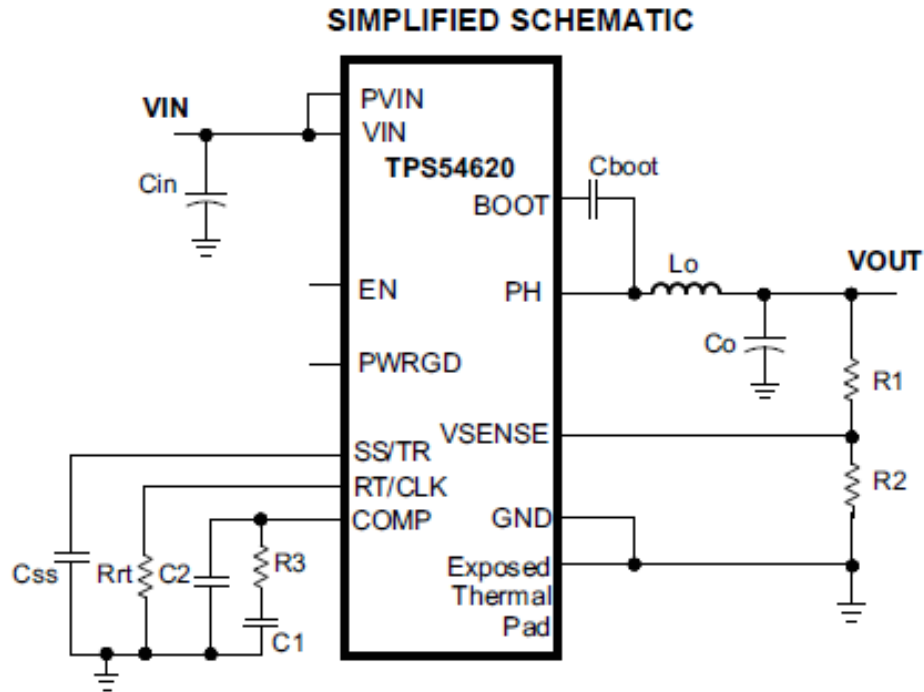
## **B. Texas Instruments TPS54620 Datasheet**

101. The TPS54620 data sheet was created by Texas Instruments to allow users to understand how to use component TPS54620 in a larger system. The data sheet summarizes the performance and other characteristics of that component.

102. In particular, the data sheet discloses that the TPS54620 is a 4.5-17V input, step down DC/DC voltage converter having integrated high-side and low-side MOSFETs, for use, e.g., in a point-of-load voltage regulator. EX1006 at 1. The data sheet includes a step-by-step design process for a high frequency switching regulator based on the TPS54620. *Id.* at 21. A simplified schematic

circuit including the TPS54620 is included on page 1 of the data sheet, and a functional block diagram Functional Block Diagram is included on page 6 of the data sheet, both of which are reproduced below.





103. As shown in the Functional Block Diagram, the high-side and low-side MOSFETS are controlled by the Power Stage Control Logic. The Power Stage Control Logic receives control signals from several sources, including the Boot UVLO monitoring circuit.

104. According to the data sheet, a bootstrap capacitor is required between the boot pin (BOOT) and the switch node pin (phase node, PH). *Id.* at 5. The voltage on the bootstrap capacitor carries the gate drive voltage for the high-side MOSFET. *Id.* The gate drive voltage for the high-side and low-side MOSFETS are applied by corresponding driver circuits.

105. The bootstrap capacitor voltage is monitored by a BOOT-PH UVLO circuit allowing PH pin to be pulled low to recharge the boot capacitor. *Id.* at 10. That is, when the bootstrap voltage drops below a threshold (about 2.1V, depending on temperature), the high-side MOSFET is turned off and the low-side MOSFET is turned on, allowing the boot capacitor to be recharged. *Id.* at 14. A POSITA would understand that the BOOT-PH UVLO circuit necessarily includes an input for the threshold voltage. Alternatively, it would be straightforward and obvious to include this input.

106. As shown in the Functional Block Diagram, the BOOT-PH UVLO circuit produces an output which is connected to the Power Stage Logic. The output indicates whether the bootstrap voltage is above or below the bootstrap voltage threshold.

107. As shown in the simplified schematic, the voltage converter receives an input voltage (on the VIN pin). A switch node (PH) is connected to the high-side and low-side MOSFETS which alternately switch the switch node (PH) between VIN and ground. The switch node (PH) is connected through an output inductor to produce a filtered output voltage (VOUT). The converter output voltage (VOUT) level is set by providing a feedback signal based on VOUT (scaled down through a resistor divider) to the VSENSE pin. *Id.* at 11. As shown in the functional block diagram, the VSENSE feedback signal is connected to an error

amplifier, which compares VSENSE to a voltage threshold (the lower of the SS/TR pin voltage or the internal 0.8V voltage reference) and which produces an output which drives the COMP pin. *Id.* at 10-11. The error amplifier output is also connected to the Power Stage Control Logic which operates the high-side and low-side switches to produce the output voltage (VOUT). *Id.* at 10, 14, 30. The SS/TR pin is externally connected to a capacitor to provide a “slow start” (commonly known as “soft start”) of the converter upon power up to reduce inrush current. *Id.* at 10. Soft start was well known to a POSITA and was understood as required for any voltage converter to properly function. *Supra* ¶69. During soft start, the error amplifier compares the feedback signal to the rising reference voltage signal (on the SS/TR pin) until it reaches the internal voltage reference value, and the PWM controller operates the high-side and low-side switches based on the difference between the output voltage and the rising reference voltage signal. EX1006 at 10. This slowly ramps up the output voltage to the desired final value. Thus, during soft start, the feedback signal is below the reference voltage until the soft start sequence completes and VSENSE equals the internal reference voltage.

108. Also, the TPS54620 data sheet discloses that the TPS54620 is protected from overcurrent conditions by cycle-by-cycle current limiting on both the high-side MOSFET and the low-side MOSFET. *Id.* at 17. At the end of every clock cycle, a low-side overprotection circuit (LS MOSFET Limit) compares the

low-side MOSFET sinking current to a predetermined low-side sinking current limit. *Id.* at 18. As shown, the output of the overprotection circuit is received by the Power Stage Logic. If the low-side sinking current limit is exceeded, the low-side MOSFET is turned off immediately. *Id.*

109. Furthermore, the TPS54620 data sheet discloses that the TPS54620 implements internal under-voltage lockout (UVLO) circuitry on the VIN pin. *Id.* at 18. That is, the device is disabled when the VIN pin voltage falls below the internal VIN UVLO threshold. *Id.* The internal VIN UVLO threshold has a hysteresis of 150mV. *Id.*

110. The TPS54620 data sheet also discloses comparing VIN to a first threshold when VIN is rising and comparing VIN to a second threshold when VIN is falling. *Id.* at 3, 11. The TPS54620 data sheet does not expressly disclose such hysteresis monitoring of the bootstrap voltage, but that feature was known in the art and included in similar DC/DC voltage converters that were available prior to the filing date of the '608 patent, such as the TPS54560 4.5V to 60V Input, 5A Step Down DC-DC Converter. For example, Figure 19 of the TPS54560 data sheet show a plot of the high and low (rising and falling) UVLO thresholds as a function of temperature. EX1023 at 9.

**C. Chinese Patent Application Publication No. CN 102832810 A to Li**

111. Li is directed to DC-DC switch-mode voltage regulators having a high side switch  $M_{HS}$  and a low side switch  $M_{LS}$  and configured to provide a bootstrap voltage  $V_{BST}$  to the control terminal of the high side switch. EX1008, EX1011 at ¶¶[0002]-[0005]. An example circuit is shown in Fig. 2, reproduced below from EX1011. As shown in Fig. 2, the example circuit includes control logic which outputs high-side and low-side control signals to operate the high-side and low-side switches, respectively, via high-side and low-side drivers of a driver module. The inputs to the control logic also include the output voltage ( $V_o$ ), a bootstrap refresh signal (RFS) and an undervoltage lockout signal (LOCK). *Id.* at ¶¶[0032], [0036], [0040]. A POSITA would understand that the purpose of providing the output voltage to the control logic is to allow the control logic to regulate the output voltage to a desired level. That is, the control logic must compare the output voltage to a desired voltage level and operate the high-side and low-side switches accordingly to achieve the desired level. As described in more detail below, the bootstrap refresh signal, the undervoltage lockout signal, and the associated components provide for refreshing the bootstrap capacitor.

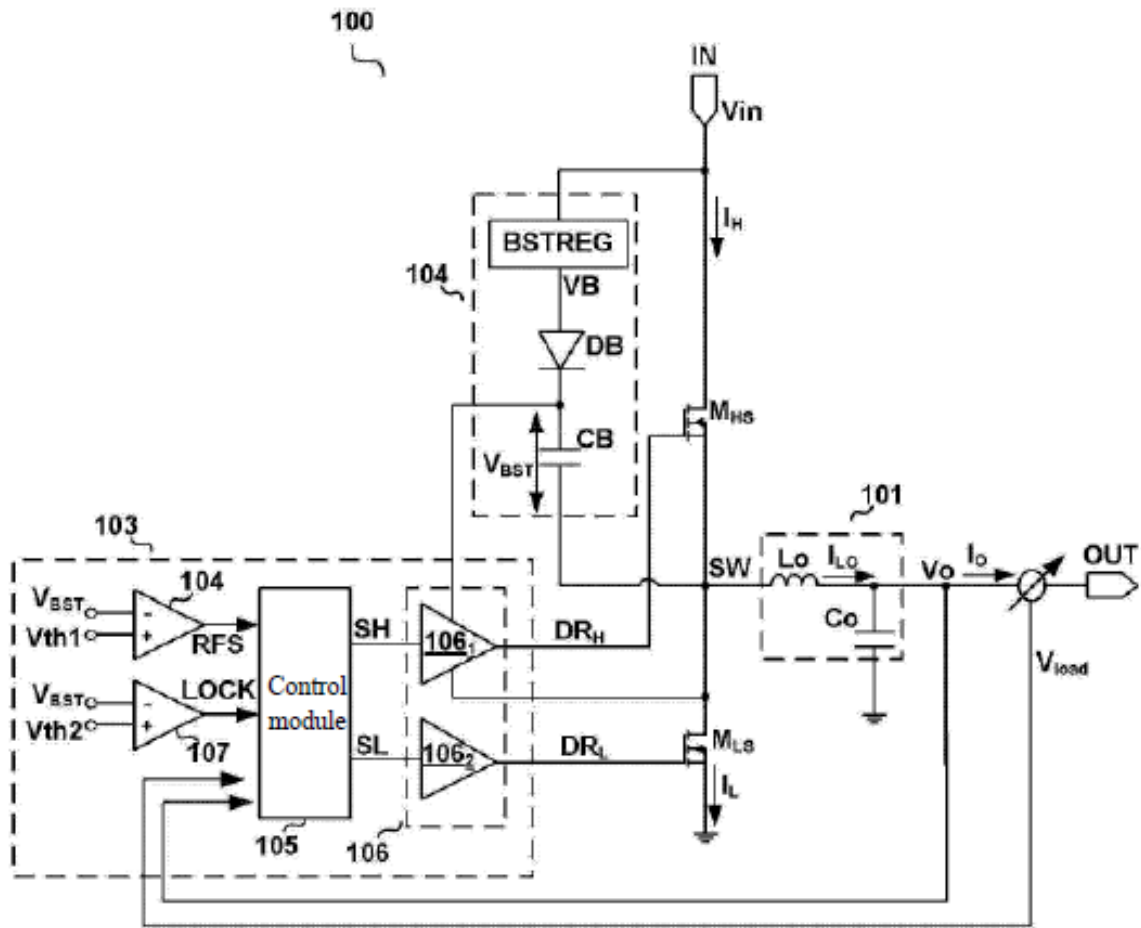


Fig. 2

112. A first comparison module compares the bootstrap voltage  $V_{BST}$  and a first threshold signal  $V_{th1}$  to produce the bootstrap refresh signal (RFS)  $I_d$  at ¶[0030]. According to this exemplary embodiment, the first threshold signal  $V_{th1}$  has a hysteresis between the first low threshold  $V_{L1}$  and the first high threshold  $V_{H1}$ , so as to reduce the possibility of false triggering due to small fluctuations of

the bootstrap voltage  $V_{BST}$ . *Id.* That is, the voltage threshold received by the first comparison module includes a low threshold and a high threshold, such that the bootstrap refresh signal has a first logic state when the bootstrap voltage drops lower than the low threshold and has a second logic state when the bootstrap voltage becomes higher than the high threshold. When the bootstrap refresh signal has the first logic state, the control logic causes the high side switch  $M_{HS}$  and the low side switch  $M_{LS}$  to switch on and off in a complementary fashion so as to enable the bootstrap capacitor CB to be recharged. *Id.* at ¶[0023].

113. The example circuit also includes an under-voltage lock out (UVLO) circuit configured to compare the bootstrap voltage  $V_{BST}$  with a second threshold signal  $V_{th2}$  (lower than  $V_{th1}$ ) to keep the high side switch  $M_{HS}$  and the low side switch  $M_{LS}$  from switching when the bootstrap voltage  $V_{BST}$  is lower than the second threshold signal and has not yet refreshed to the level of the first threshold signal. *Id.* at ¶[0036].

114. Thus, a POSITA would understand that, as a whole, the control logic refreshes the bootstrap capacitor when the bootstrap voltage is less than the first threshold (and greater than the second threshold), by controlling the logic switches to switch on and off complementarily to recharge the bootstrap capacitor. A POSITA would further understand that if the bootstrap voltage is less than the second threshold, the control logic causes the switches to stop switching.

115. In a second embodiment, Li discloses a zero-crossing detection (ZCD) module configured to provide a zero-crossing indicating signal  $C_{ZCD}$  based on comparing the current flowing through the low side switch ( $I_L$ ) to a threshold signal  $V_{th4}$  to turn the low side switch  $M_{LS}$  off when the current  $I_L$  flowing through the low-side switch  $M_{LS}$  is lower than zero. *Id.* at ¶¶ [0050]-[0053], Fig. 3, reproduced below. Thus, when the reverse current flowing through the low-side switch is greater than the threshold, the control module shuts off the low-side switch.

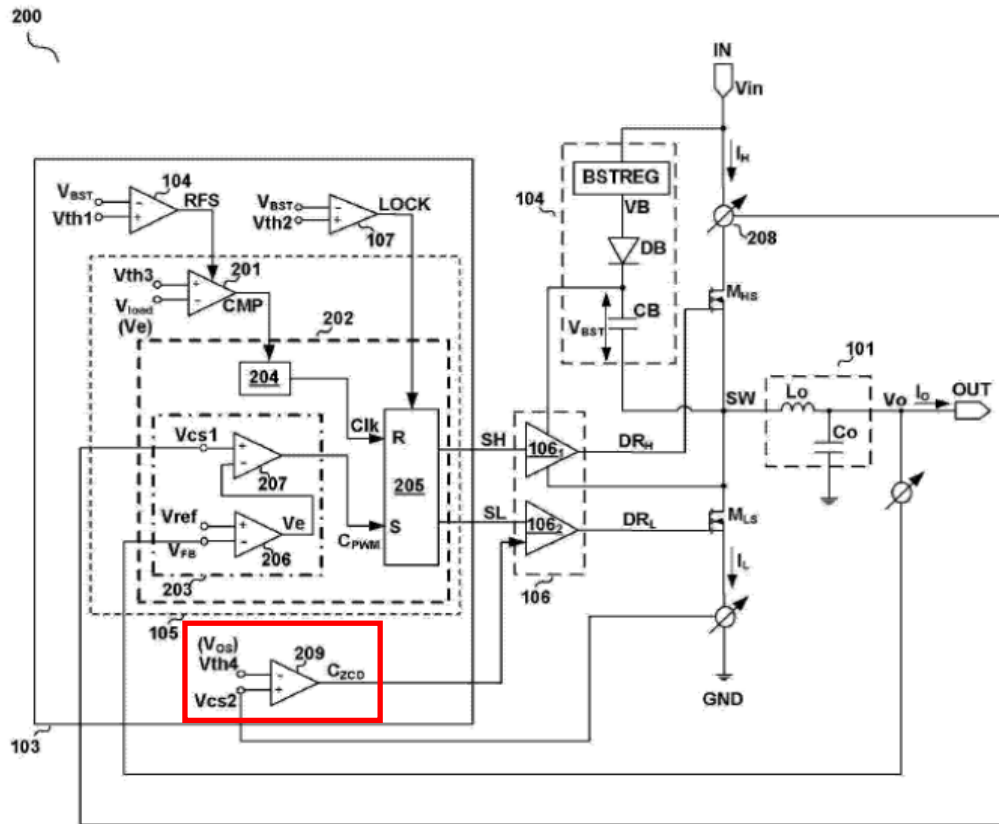


Fig. 3

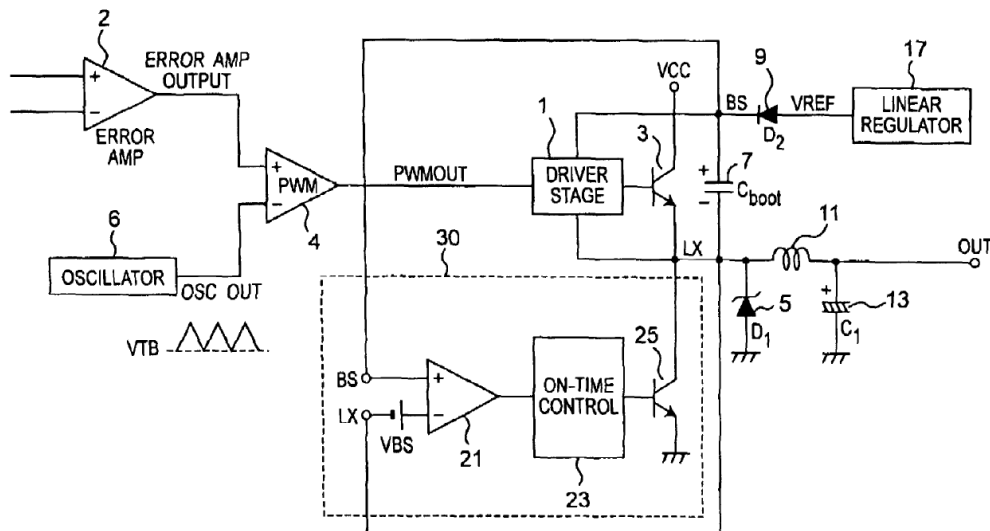
**D. U.S. Patent No. 7,321,258 to Wong**

116. Wong is directed to DC-DC switching power converters having a bootstrap capacitor and particularly to methods for controlling the charge of the bootstrap capacitor so that the voltage is enough to turn on the driver for the power transistor. EX1007 at 1:9-13, 38-42. Wong describes the known solution of connecting a dummy load at the output of the voltage converter, which would keep

the output transistor switching (thus recharging the bootstrap capacitor), but at the expense of reduced efficiency. *Id.* at 1:43-54.

117. As an alternative, Wong discloses monitoring the bootstrap voltage and connecting the switching node (LX) to ground when the bootstrap voltage becomes less than a predetermined threshold (VBS). *Id.* at 5:3-13; 5:64-66. An example circuit is shown in Fig. 6 (reproduced below).

**Fig.6**

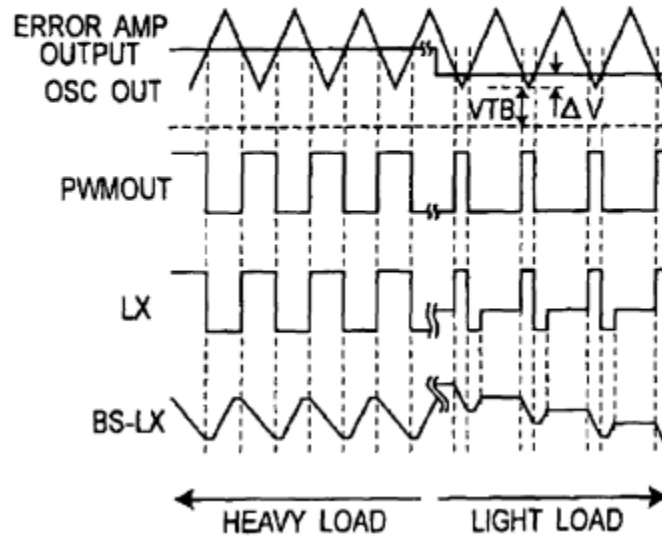


118. As shown in Fig. 6, Wong discloses a DC-DC converter having a power transistor (high-side switch) configured to connect the input voltage (VCC) to a switching node (LX). Fig. 6 also shows LX connected to ground through a free-wheeling diode 5 acting as a low-side switch. *supra* §III.D. That is, a POSITA would understand that Wong's diode could be replaced with an actively controlled switch to improve efficiency of Wong's converter. *Id.* Fig. 6 also shows a

secondary (low-side) switch configured to connect the switching node to ground. The voltage across the bootstrap capacitor ( $C_{boot}$ ) is applied to the high-side switch driver stage to operate the high-side switch. A load control circuit includes a BS voltage detector which compares the bootstrap voltage to a threshold voltage (VBS) to provide a control signal for switching on the secondary switch (during the off-time of the main power transistor) when the bootstrap voltage is less than the threshold. *Id.* at 4:66-5:9; 5:64-66. When the secondary switch/transistor is turned on as a result of the bootstrap voltage being low, the switching node voltage is pulled near to the ground voltage, thus recharging the bootstrap capacitor. *Id.* at 5:10-12; 5:64-66.

119. As shown in Fig. 6, in a PWM DC-DC converter, the duty cycle is determined by a comparator 4 which compares the output of the error amplifier 2 with a triangular signal produced from oscillator 6 and outputs a signal with a high state when the error signal is greater than the triangular signal, so as to switch on the power transistor, and a low state when the error signal is less than the triangular signal so as to turn off the power transistor. *Id.* at 5:23-23; 5:64-66. A POSITA would understand that the duty cycle is the amount of time that the power transistor is switched on (and providing power to the switch node) during one switching period relative to the period of the PWM signal, as illustrated in Fig. 4B below.

*Fig.4B*

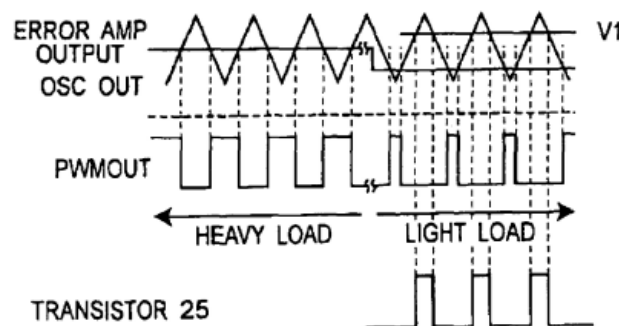


120. Furthermore, a POSITA would understand that the purpose of adjusting the duty cycle is for the voltage converter to provide a regulated voltage output. To achieve that aim, the output of the error amplifier must represent the difference between the desired output voltage of the DC-DC converter and a measured (feedback) output voltage. That is, in the disclosed PWM DC-DC converter, the output of the error amplifier represents the output voltage error that is corrected by adjusting the duty cycle. Thus, the inputs to the error amplifier include the desired output voltage of the DC-DC converter and the measured (feedback) output voltage.

121. Wong further discloses the PWM DC-DC converter including an on-time control configured to only switch on the secondary switch when the bootstrap

voltage is less than a threshold and when the power switch is off. In one embodiment, the on time for the secondary switch is determined by comparing the triangular oscillator signal discussed above to another threshold voltage which is higher than the maximum output of the error amplifier. *Id.* at 5:42-55. As shown in Fig. 5B, shown below, a POSITA would understand that by setting the threshold to a value greater than the maximum error-amplifier output, the secondary switch will only be turned on when the power transistor is turned off. A POSITA would also understand that the on-time for the secondary switch is based only on the triangular signal and the constant voltage threshold. Thus, the secondary-switch on-time is constant.

**Fig.5B**



## **VI. SPECIFIC GROUNDS FOR UNPATENTABILITY**

### **A. Ground 1: Claims 1, 11, and 12 are anticipated by or obvious over TI**

#### **1. Claim 1**

- a. **Limitation 1[PRE]: A bootstrap refresh control circuit for a voltage converter, wherein the voltage converter comprises a high side switch, a low side switch and a bootstrap capacitor for providing a bootstrap voltage signal to supply a high side driver of the high side switch, and wherein the voltage converter is configured to receive an input voltage at an input terminal and to provide an output voltage at an output terminal based on driving the high side switch and the low side switch to switch on and off, and**

122. Limitation 1[PRE] limits the scope of claim 1 to circuits for use in voltage converters having high side and low side switches and a bootstrap capacitor to supply a bootstrap voltage to a driver of the high side switch, where the input voltage is converted to the output voltage based on switching the high side and low side switches on and off.

123. TI discloses a voltage converter. See cropped image below from the TPS54620 datasheet. EX1006 at 1.



[www.ti.com](http://www.ti.com)

**TPS54620**

SLVS949C – MAY 2009 – REVISED MAY 2011

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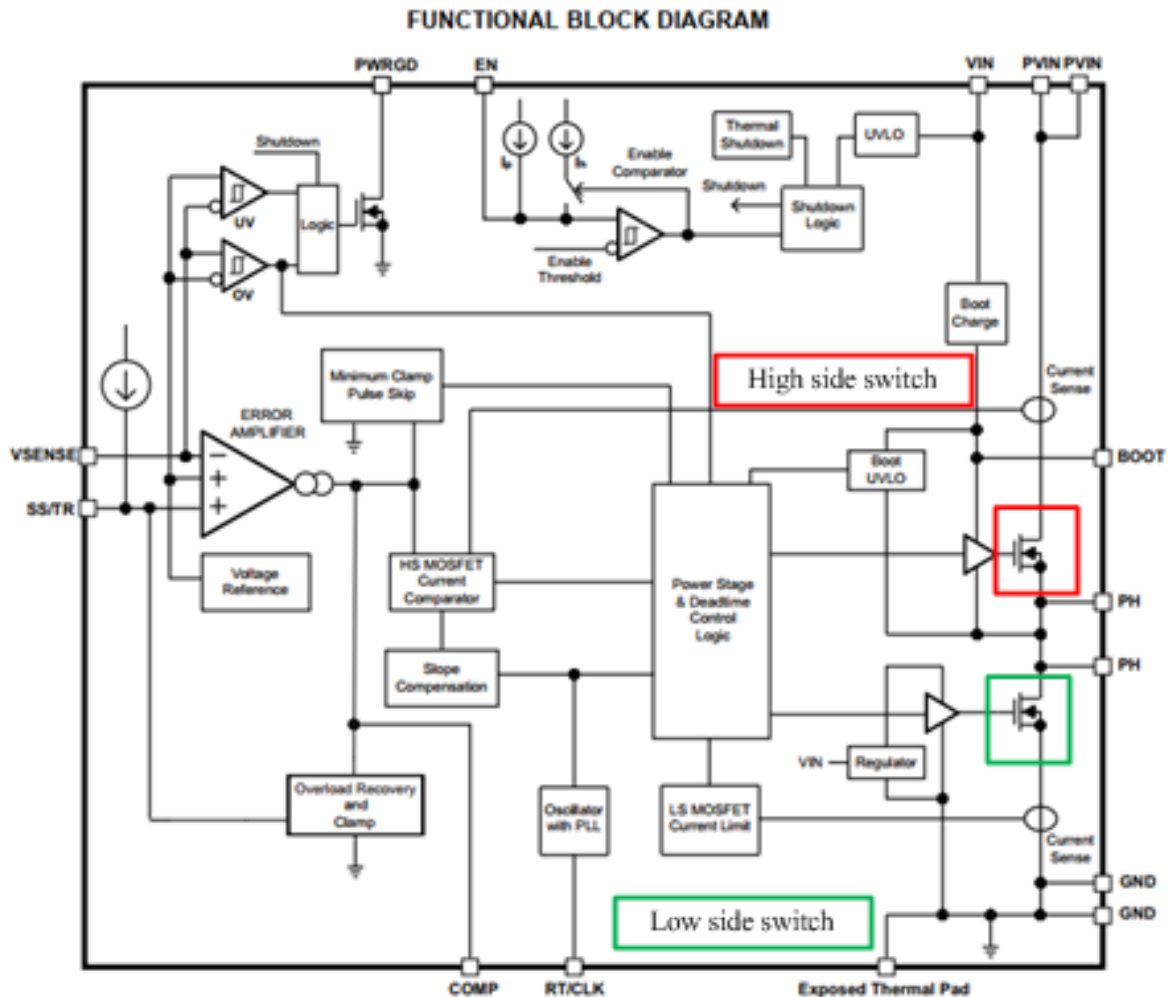
**4.5V to 17V Input, 6A Synchronous Step Down SWIFT™ Converter**

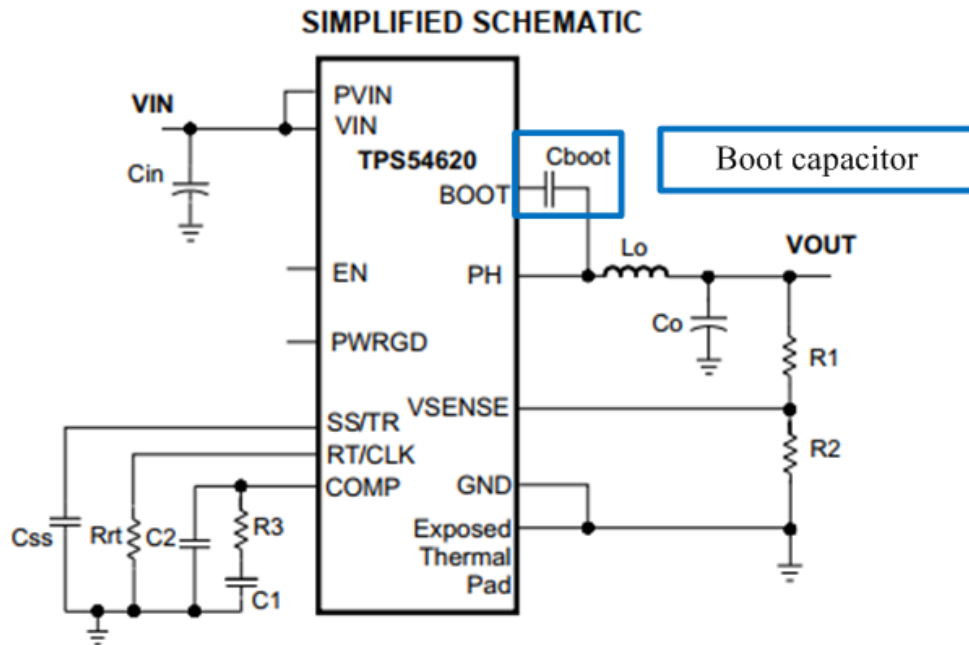
Check for Samples: [TPS54620](#)

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124. TI further discloses the voltage converter having integrated high-side and low-side MOSFETs and requiring a bootstrap capacitor between boot and switch-node pins to carry the drive voltage for the high-side MOSFET. *Id.* at 1,6,

See also **FUNCTIONAL BLOCK DIAGRAM AND SIMPLIFIED**





125. Thus, the TPS54620 data sheet discloses a voltage converter having a high side switch, a low side switch, a bootstrap capacitor providing the drive voltage for the high-side switch, and a bootstrap refresh control circuit for recharging the bootstrap capacitor when the bootstrap voltage drops below a threshold. Therefore, TI anticipates limitation 1[PRE].

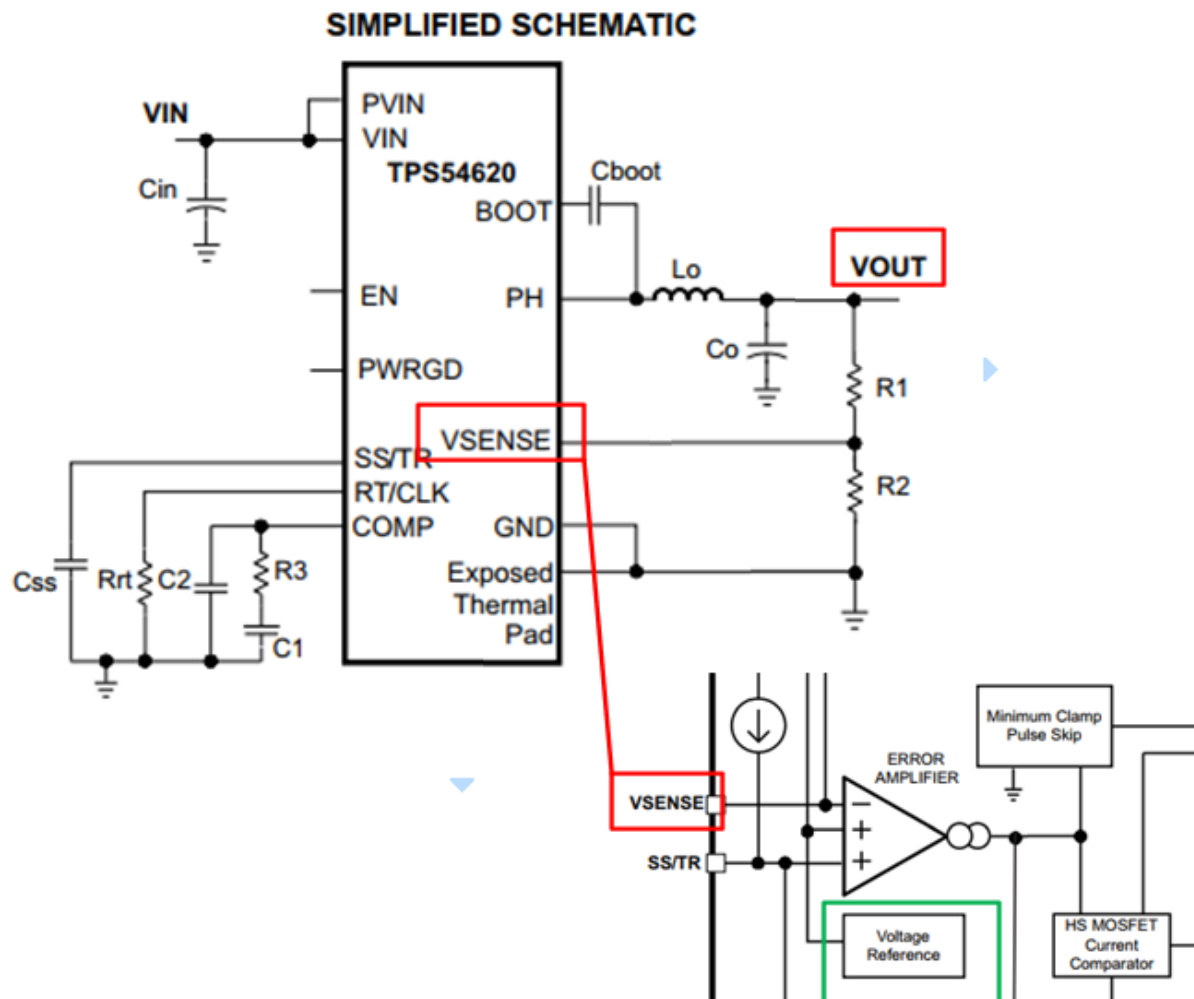
- b. Limitation 1[A]: wherein the bootstrap refresh control circuit comprising: a bootstrap refresh module, wherein the bootstrap refresh module comprises a first comparing module having a first input terminal, a second input terminal and an output terminal, and wherein the first input terminal of the first comparing module is configured to receive the bootstrap voltage signal, the second input terminal of the first comparing module is configured to receive a bootstrap refresh threshold, and the first comparing module is configured to compare the bootstrap voltage signal with the bootstrap refresh threshold to provide a first comparing signal having a first logic state and a second logic state at the output terminal, and wherein the first comparing signal has the first logic state when the bootstrap voltage signal is lower than the bootstrap refresh threshold, and wherein the first comparing signal has the second logic state when the bootstrap voltage signal is larger than the bootstrap refresh threshold; and

126. Limitation 1[A] recites the structure of a bootstrap refresh module that comprises a first comparing module having two inputs and an output that outputs a first comparing signal by comparing the bootstrap voltage signal and the bootstrap refresh threshold and defines the first comparing signal as having one of two logic states depending on which input signal is larger. As discussed above, TI discloses the TPS54620 including a monitor circuit (Boot UVLO) which compares the bootstrap voltage to a threshold (about 2.1 volts). *Id.* at 14. The output of the monitor circuit is received by the Power Stage & Deadtime Control Logic. Depending on the state of the monitor-circuit output (i.e., when the bootstrap

voltage drops below a threshold), the Power Stage & Deadtime Control Logic will turn on the low-side MOSFET, allowing the boot capacitor to be recharged. *Id.* at 14. It is my opinion that a POSITA would understand a threshold input into the comparator of the monitor circuit would necessarily be present based on the disclosures in TI. Thus, the TPS54620 data sheet discloses a bootstrap refresh module, comprising the Boot UVLO and at least a portion of the Power Stage & Deadtime Control Logic, that compares the bootstrap voltage signal to a bootstrap refresh threshold to produce an output having one of two states. Therefore, it is my opinion that TI expressly or inherently anticipates limitation 1[A]. Alternatively, it is my opinion that a POSITA would find limitation 1[A] obvious over TI and other background knowledge in the art because it would be straightforward and obvious to do so. *Supra* ¶105, §III.B.

- c. **Limitation 1[B]: a voltage difference module having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal of the voltage difference module is configured to receive a feedback signal representing the output voltage of the voltage converter, the second input terminal of the voltage difference module is configured to receive a reference voltage signal representing a desired value of the output voltage of the voltage converter, the voltage difference module is configured to compare the feedback signal with the reference voltage signal so as to provide a difference signal at the output terminal; and**

127. Limitation 1[B] recites a voltage difference module that has two input terminals and an output terminal, and compares an output voltage feedback signal to a reference voltage to provide a difference signal at the output terminal. As shown below in the combined figures from the TI datasheet, *Id.* 1,6, TI discloses an error amplifier which receives a feedback signal based on VOUT (scaled down through a resistor divider), via the VSENSE pin.



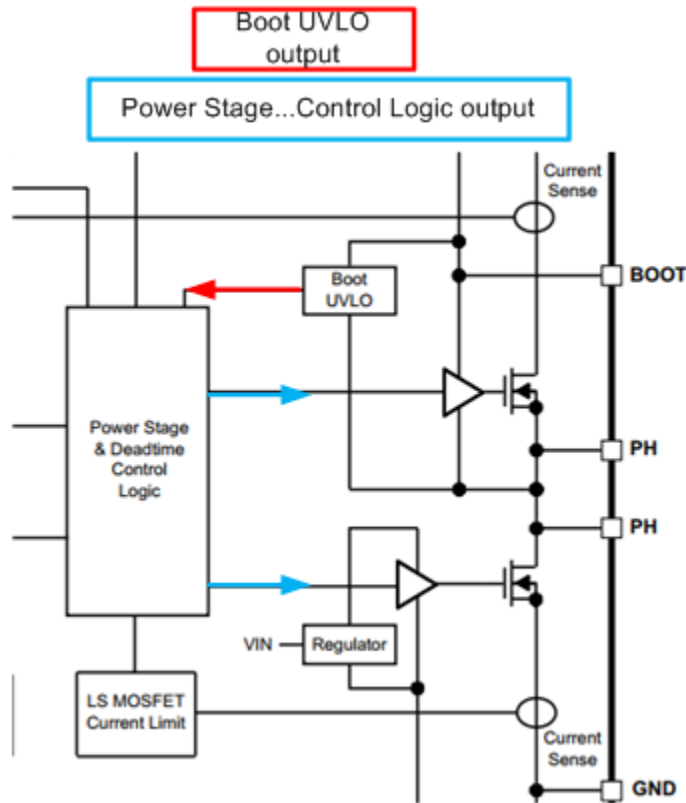
128. The error amplifier also receives a voltage reference, either from an internal source or the SS/TR pin. The output of the error amplifier is based on the error, i.e., the difference, between the feedback signal and the voltage reference. Thus, the TPS54620 data sheet discloses a voltage difference module that receives a feedback signal representing the output voltage of the voltage converter, and a reference voltage signal representing a desired output voltage and compares the feedback signal and the reference voltage to produce a difference signal at the output. Therefore, TI anticipates limitation 1[B].

- d. **Limitation 1[C]: wherein when the first comparing signal has the first logic state, the bootstrap refresh module is configured to decrease the output voltage of the voltage converter; and**

129. Limitation 1[C] recites that the bootstrap refresh module is configured to decrease the output voltage of the voltage converter when the bootstrap voltage signal is lower than the bootstrap refresh threshold (first comparing signal has the first logic state).

130. TI discloses when the voltage between BOOT and PH pins drops below a threshold (about 2.1V, depending on temperature), the high-side MOSFET is turned off and the low-side MOSFET is turned on to recharge the boot capacitor. During the operation of recharging the boot capacitors, the switch node (PH) is pulled low (connected to ground), thus necessarily causing VOUT (which is

connected to the switch node through the output inductor) to decrease. *See* ¶¶73, 74. As shown below, the Functional Block Diagram (cropped and annotated) from the TI datasheet at 6, the output of TI's bootstrap monitor-circuit (first comparing signal) is connected to the Power Stage & Deadtime Control Logic, which is configured to provide control signals for driving the high-side and low-side switches. A POSITA would understand that the switch node is pulled low by a control signal from the Power Stage & Deadtime Control Logic which is based on the output of TI's bootstrap monitor-circuit (when the bootstrap voltage drops below a threshold). Thus, TI discloses a bootstrap refresh module configured to decrease the output voltage of the voltage converter when the bootstrap voltage signal is lower than the bootstrap refresh threshold. Therefore, TI anticipates limitation 1[C]. Alternatively, it would be obvious to a POSITA that when the switch node is pulled low, VOUT would decrease. *See* ¶¶73, 74.



- e. Limitation 1[D]: wherein when the feedback signal is smaller than the reference voltage signal, the bootstrap refresh control circuit is configured to control the high side switch and the low side switch to switch on and off based on the difference signal so as to charge the bootstrap capacitor for refreshing the bootstrap voltage signal.

131. Limitation 1[D] recites circuitry switching on and off the high-side and low-side switches based on the difference signal (recited in limitation 1[B]) when the feedback signal is less than the reference voltage, so as to charge the bootstrap capacitor. As explained in the overview of the '608 patent, the normal

switching of the high-side and low-side switches to maintain the output voltage also refreshes the bootstrap voltage. *See* ¶85.

132. TI discloses the TPS54620 synchronous buck converter. *Id.* at 9. Providing point of load regulation. *Id.* at 1. A POSITA would understand that a voltage regulator with integrated MOSFETs would include circuitry that switches the MOSFETS on and off to regulate the output voltage, and that the regulation is based on a difference between a feedback signal and the reference voltage. Furthermore, a POSITA would understand that switching the MOSFETS on and off would charge the bootstrap capacitor at least during the time when the high-side switch is off and the low-side switch is on.

133. Furthermore, TI discloses the output of the TPS54620 error amplifier connected to Power Stage & Deadtime Control Logic (indirectly, through the HS MOSFET Current Comparator), and that the Power Stage & Deadtime Control Logic provides control signals for controlling the high-side and low-side switches. Additionally, a POSITA would understand that the purpose of adjusting the timing and duration that the power switching period is for the voltage converter to provide a regulated voltage output. Thus, when the output of the error amplifier indicates that the output voltage is different (either less than or greater than) than the reference signal, TI's Power Stage & Deadtime Control Logic is configured to control the high side switch to switch on and off based on the difference signal.

Further, a POSITA would understand that, during normal operation, when VOUT of TI is decreased from its normal (desired) level, for example, when the low-side switch is turned on, the feedback signal will necessarily also decrease and fall below the reference voltage (which establishes the desired output voltage). Further, during “soft start”, the feedback signal is below the reference voltage. *See* ¶69.

Therefore, a POSITA would understand that the TPS54620’s Power Stage & Deadtime Control Logic switches on and off the high-side and low-side switches based on the output of the error amplifier, so as to charge the bootstrap capacitor, including when the feedback signal is less than the reference voltage. Finally, when exiting “pulse skipping” mode, the feedback signal is also below the reference voltage. *See* ¶69. Thus, in any of these operational modes, the TPS54620’s Power Stage & Deadtime Control Logic switches on and off the high-side and low-side switches based on the output of the error amplifier, so as to charge the bootstrap capacitor, including when the feedback signal is less than the reference voltage. Therefore, TI expressly or inherently anticipates limitation 1[D].

Alternatively, it would be obvious to a POSITA that when VOUT is decreased, the feedback signal falls below the reference voltage and that the Power Stage & Deadtime Control Logic controls the high side switch to switch on and off based on the difference signal. *See* ¶68.

## 2. Claim 11

134. Claim 11 is directed to a voltage converter comprising a switching circuit and a bootstrap circuit substantially identical to the recitations in claim 1. Thus, claim 11, for at least the same reasons as claim 1, is unpatentable over TI. See §VI.A.1.

### a. Limitation 11[PRE]: A voltage converter, comprising:

135. TI discloses a voltage converter. *supra* ¶¶122-123.

### b. Limitation 11[A]: a switching circuit having a high side switch and a low side switch, wherein the switching circuit is configured to receive an input voltage, and further configured to provide an output voltage based on switching the high side switch and the low side switch on and off;

136. Limitation 11[A] is disclosed by TI. *supra* ¶¶124-125.

### c. Limitation 11[B]: a bootstrap circuit comprising a bootstrap capacitor, wherein the bootstrap capacitor is charged for providing a bootstrap voltage signal for the high side switch; and

137. Limitation 11[B] is disclosed by TI. *supra* ¶¶131-133.

- d. Limitation 11[C]: a bootstrap refresh control circuit comprising: a bootstrap refresh module, wherein the bootstrap refresh module comprises a first comparing module having a first input terminal, a second input terminal and an output terminal, and wherein the first input terminal of the first comparing module is configured to receive the bootstrap voltage signal, the second input terminal of the first comparing module is configured to receive a bootstrap refresh threshold, and the first comparing module is configured to compare the bootstrap voltage signal with the bootstrap refresh threshold to provide a first comparing signal having a first logic state and a second logic state at the output terminal, and wherein the first comparing signal has the first logic state when the bootstrap voltage signal is lower than the bootstrap refresh threshold, and the first comparing signal has the second logic state when the bootstrap voltage signal is larger than the bootstrap refresh threshold; and

138. Limitation 11[C] is disclosed by TI. *supra* ¶126. Alternatively, a POSITA would find this limitation obvious. *Id.*

- e. Limitation 11[D]: a voltage difference module having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal of the voltage difference module is configured to receive a feedback signal representing the output voltage of the voltage converter, the second input terminal of the voltage difference module is configured to receive a reference voltage signal representing a desired value of the output voltage of the voltage converter, the voltage difference module is configured to compare the feedback signal with the reference voltage signal so as to provide a difference signal at the output terminal; and wherein

139. Limitation 11[D] is disclosed by TI. *supra* ¶¶127,128.

- f. **Limitation 11[E]: when the first comparing signal has the first logic state, the bootstrap refresh module is configured to decrease the output voltage of the voltage converter; and**

140. Limitation 11[E] is disclosed by TI. *supra* ¶¶129, 130. Alternatively, it would be obvious to a POSITA that when the switch node is pulled low, VOUT would decrease. See ¶¶72, 73.

- g. **Limitation 11[F]: wherein when the feedback signal is smaller than the reference voltage signal, the bootstrap refresh control circuit is configured to control the high side switch and the low side switch to switch on and off based on the difference signal so as to charge the bootstrap capacitor for refreshing the bootstrap voltage signal.**

141. Limitation 11[F] is disclosed by TI. *supra* ¶¶131-133.

### 3. **Claim 12**

142. Claim 12 is a method claim reciting a method of use for a voltage converter. TI anticipates each step of claim 12.

- a. **Limitation 12[PRE]: A bootstrap refresh control method for a voltage converter, wherein the voltage converter comprises a high side switch, a low side switch and a bootstrap capacitor for providing a bootstrap voltage signal to supply a high side driver of the high side switch, and wherein the voltage converter is configured to receive an input voltage and to provide an output voltage based on driving the high side switch and the low side switch to switch on and off, and wherein the bootstrap refresh control method comprising:**

143. Limitation 12[PRE] recites the structural requirements of a voltage converter for use in the recited method in claim 12. TI discloses a voltage converter as recited in limitation 12[PRE]. *supra* ¶¶122-123.

- b. **Limitation 12[A]: sensing the bootstrap voltage signal of the voltage converter;**

144. Limitation 12[A] recites sensing a bootstrap voltage signal. TI discloses this method step. *supra* ¶126.

- c. **Limitation 12[B]: comparing the bootstrap voltage with a bootstrap refresh threshold to provide a first comparing signal, wherein the first comparing signal has a first logic state and a second logic state, and wherein the first comparing signal has the first logic state when the bootstrap voltage is lower than the bootstrap refresh threshold, and wherein the first comparing signal has the second logic state when the bootstrap voltage signal is larger than the bootstrap refresh threshold;**

145. Limitation 12[B] recites comparing the bootstrap voltage with a bootstrap refresh threshold to provide a first comparing signal having one of two

logic states. TI discloses this method step, including the recited logic states. *supra* ¶126.

- d. **Limitation 12[C]: determining whether the bootstrap voltage signal is smaller than the bootstrap refresh threshold or not; and**

146. Limitation 12[C] recites determining whether the voltage signal is smaller than the bootstrap refresh threshold. TI discloses this method step. *supra* ¶126.

- e. **Limitation 12[D]: decreasing the output voltage of the voltage converter by a bootstrap refresh circuit once the bootstrap voltage signal is determined to have dropped to be smaller than the bootstrap refresh threshold; and**

147. Limitation 12[D] recites decreasing the output voltage when the bootstrap voltage signal is determined to be lower than the bootstrap refresh threshold. TI discloses this limitation. *supra* ¶¶129,130.

- f. **Limitation 12[E]: wherein when the output voltage of the voltage converter is decreased, switching the high side switch and the low side switch on and off so as to refresh the bootstrap voltage signal.**

148. Limitation 12[E] recites switching the high side and low side switches to increase the bootstrap voltage (i.e., to charge the bootstrap capacitor). TI discloses this limitation. *supra* ¶¶131-133.

**B. Ground 2: Claims 1, 11, and 12 are anticipated by Galinski**

1. Claim 1

- a. Limitation 1[PRE] : A bootstrap refresh control circuit for a voltage converter, wherein the voltage converter comprises a high side switch, a low side switch and a bootstrap capacitor for providing a bootstrap voltage signal to supply a high side driver of the high side switch, and wherein the voltage converter is configured to receive an input voltage at an input terminal and to provide an output voltage at an output terminal based on driving the high side switch and the low side switch to switch on and off, and

149. The preamble of Claim 1 limits the scope of the claim to circuits for use in a voltage converter receiving an input voltage and generating an output voltage by driving a high-side switch and a low-side switch on and off. The scope of the claim is further limited to a voltage converter comprising a bootstrap capacitor to supply a bootstrap voltage to the driver of the high-side switch.

150. Galinski discloses the elements of the Claim 1 preamble. As shown in the Fig. 2 of Galinski (annotated) below, Galinski discloses a voltage converter with an input terminal and an output terminal.

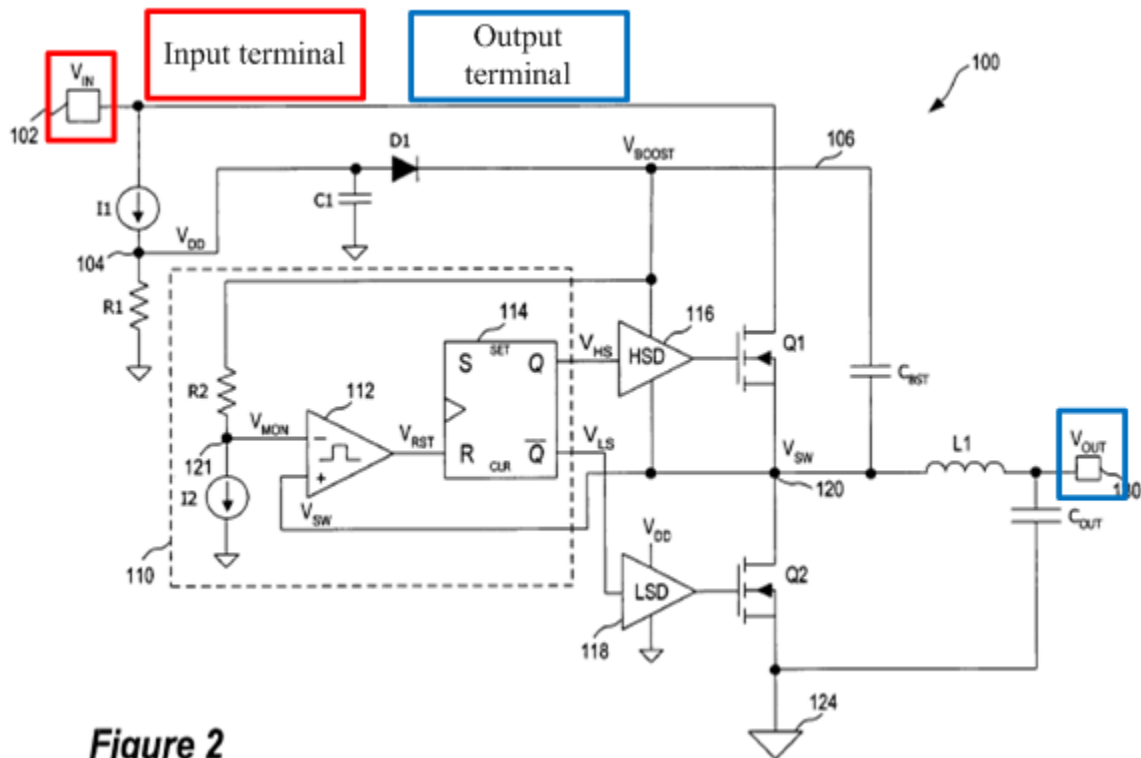
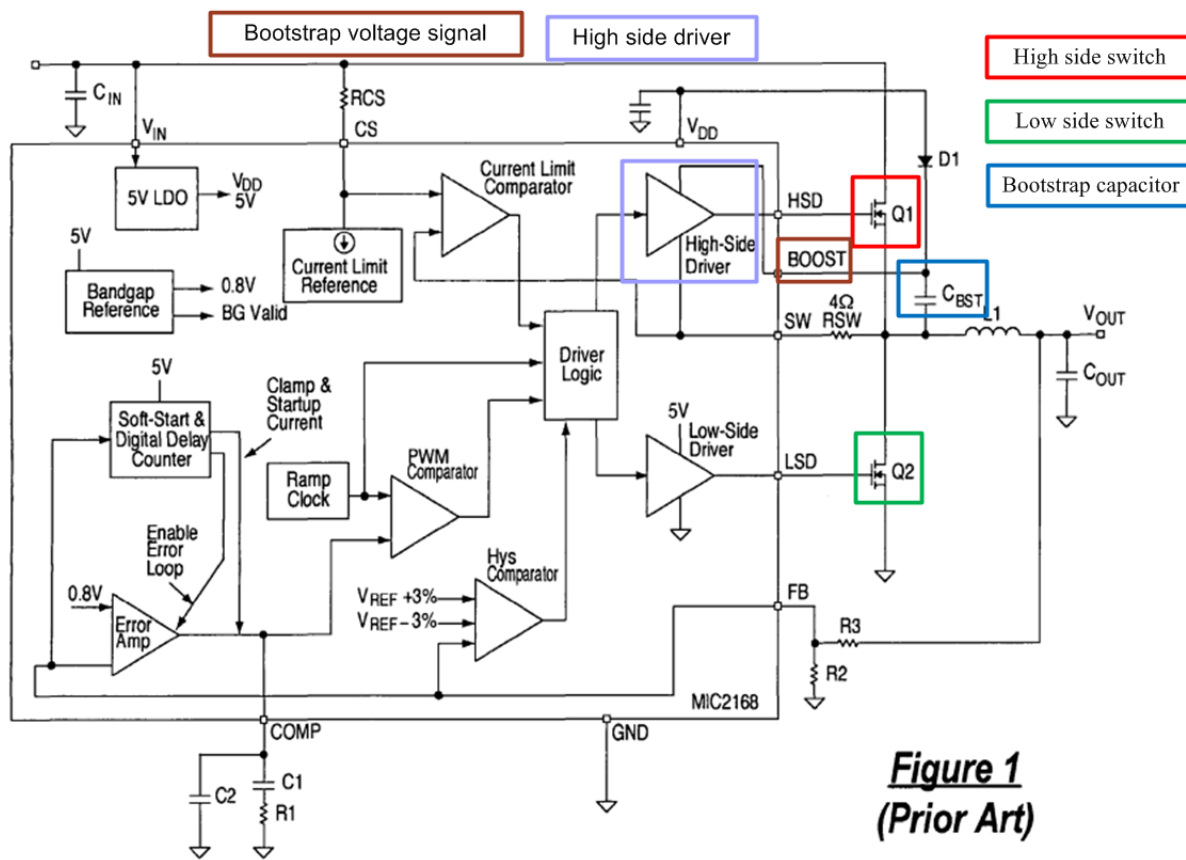


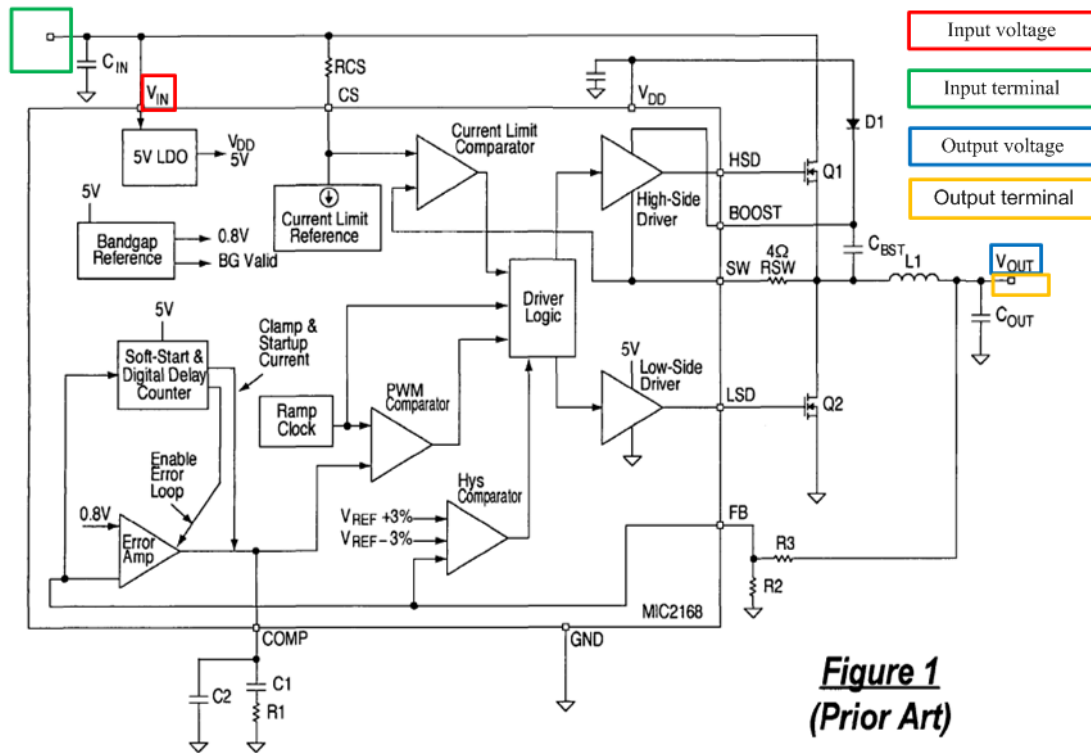
**Figure 2**

151. As illustrated, Galinski Fig. 1 below, Galinski further discloses a voltage converter that comprises a high-side switch, a low-side switch and a bootstrap capacitor for providing a bootstrap voltage signal to supply a high side driver of the high side switch.



152. As show in the figure below, Galinski further discloses a voltage converter configured to receive an input voltage at an input terminal and to provide an output voltage at an output terminal. As Galinski explains, a switching voltage regulator provides power supply function through power switches that are turned on and off to transfer energy from the input to the output in discrete packets. A feedback control circuit is used to regulate the energy transfer to maintain a constant output voltage within certain load limits of the circuit. *Id.* at 1:14-26. The power switches, switching on and off, generate a switching output voltage ( $V_{sw}$ )

which is coupled to an inductor-capacitor (LC) network for filtering the switching voltage to provide an output voltage at an output terminal.



153. Galinski discloses Limitation 1[PRE].

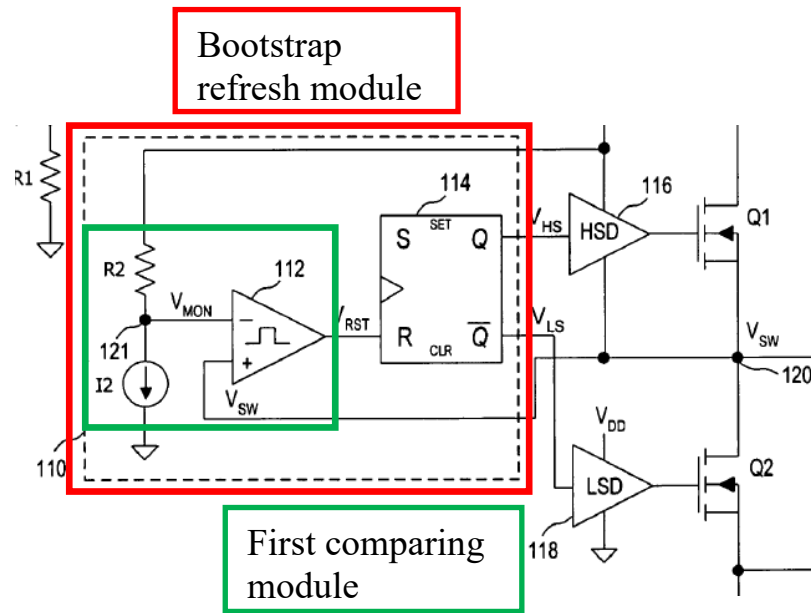
- b. Limitation 1[A]: wherein the bootstrap refresh control circuit comprising: a bootstrap refresh module, wherein the bootstrap refresh module comprises a first comparing module having a first input terminal, a second input terminal and an output terminal, and wherein the first input terminal of the first comparing module is configured to receive the bootstrap voltage signal, the second input terminal of the first comparing module is configured to receive a bootstrap refresh threshold, and the first comparing module is configured to compare the bootstrap voltage signal with the bootstrap refresh threshold to provide a first comparing signal having a first logic state and a second logic state at the output terminal, and wherein the first comparing signal has the first logic state when the bootstrap voltage signal is lower than the bootstrap refresh threshold, and wherein the first comparing signal has the second logic state when the bootstrap voltage signal is larger than the bootstrap refresh threshold; and

154. Limitation 1[A] recites the structure of a bootstrap refresh module that comprises a first comparing module having two inputs and an output that outputs a first comparing signal by comparing the bootstrap voltage signal and the bootstrap refresh threshold and defines the first comparing signal as having one of two logic states, a first logic state and a second logic state, depending on which input signal is larger. Galinski discloses a control circuit for monitoring and maintaining the bootstrap voltage incorporated in [a] switching regulator. *See Id.*, 5:4-24, Fig. 2. The complete voltage regulator includes other circuit elements as shown in FIG. 1. *Id.*

155. Referring to FIG. 2 of Galinski shown below (cropped and annotated), bootstrap voltage control circuit 110 includes a comparator circuit 112 that receives a monitor voltage  $V_{\text{MON}}$  at a first input and a switching output voltage  $V_{\text{SW}}$  at a second input. *Id.* at 8:30-53. A POSITA would understand Galinski's bootstrap voltage control circuit is a bootstrap refresh control circuit. Galinski teaches that comparator circuit 112 is a one-shot comparator that generates a reset pulse based on a comparison at the inputs. *Id.* 9:1-6. A POSITA would understand that a one-shot comparator would comprise a comparator followed by a one-shot circuit. *supra* ¶95, §III.B, §III.C. The comparator element of a one-shot comparator would output one of two states depending on the state of the inputs. *supra* §III.B. It is my opinion that a POSITA would understand Galinski's one-shot comparator necessarily contains a first comparing module with a first input terminal, a second input terminal, and an output terminal. Alternatively, it is my opinion that a POSITA would find it obvious to include such a comparing module.

156. Galinski discloses that  $V_{\text{MON}}$  is scaled from  $V_{\text{BOOST}}$  ( $V_{\text{MON}} = V_{\text{BOOST}} - I_2 R_2$ ) such that a minimum bootstrap voltage  $V_{\text{BOOST\_MIN}}$  is always greater than  $V_{\text{IN}} + V_{\text{TH\_HS}}$ , where  $V_{\text{TH\_HS}}$  is the threshold voltage of the MOSFET (*see* III.A) required to turn on the high side switch. *Id.*, 8:54-61. A POSITA would recognize that  $V_{\text{MON}}$  is derived from bootstrap voltage  $V_{\text{BOOST}}$  and, thus, represents a bootstrap voltage signal. It is my opinion that a POSITA would understand the

bootstrap voltage signal to be necessarily present in Galinski. Alternatively, it is my opinion that a POSITA would find it obvious to calculate a bootstrap voltage signal based on the disclosures of Galinski.



157. Galinski further discloses that [w]hen the monitor voltage  $V_{MON}$  is equal to or less than voltage  $V_{SW}$ , comparator circuit 112 generates a reset pulse as the output voltage signal  $V_{RST}$ . *Id.*, 9:1-5. A POSITA would understand that the one-shot comparator circuit 112 would internally change states based on the voltages,  $V_{MON}$  and  $V_{SW}$  and that when  $V_{MON}$  transitions to be less than  $V_{SW}$ , the comparator element of the one-shot comparator would change state thereby initiating the one-shot element to generate a pulse. *Supra* ¶¶95,96. Moreover, a POSITA would understand that when  $V_{SW}$  transitions to be less than  $V_{MON}$ , the comparator element of the one shot would change state and not initiate the one-

shot element to generate a pulse. A POSITA would further understand that, as used by the bootstrap voltage control circuit 110 and comparator circuit 112, the switching output voltage  $V_{SW}$  is a threshold against which the bootstrap voltage signal is compared to determine whether to recharge the bootstrap capacitor, i.e. a bootstrap refresh threshold. *Id.*, 9:1-28, Fig. 3 (shown below). A POSITA reading Galinski would understand that  $V_{MON}$  is designed such that it falls below  $V_{SW}$  at the same time that  $V_{HS}$  falls below  $V_{BOOST\_MIN} = V_{IN} + V_{TH\_HS}$  indicating that the bootstrap capacitor needs to be refreshed to enable  $V_{HS}$  to drive the high side switch. Therefore, Galinski anticipates limitation 1[A].

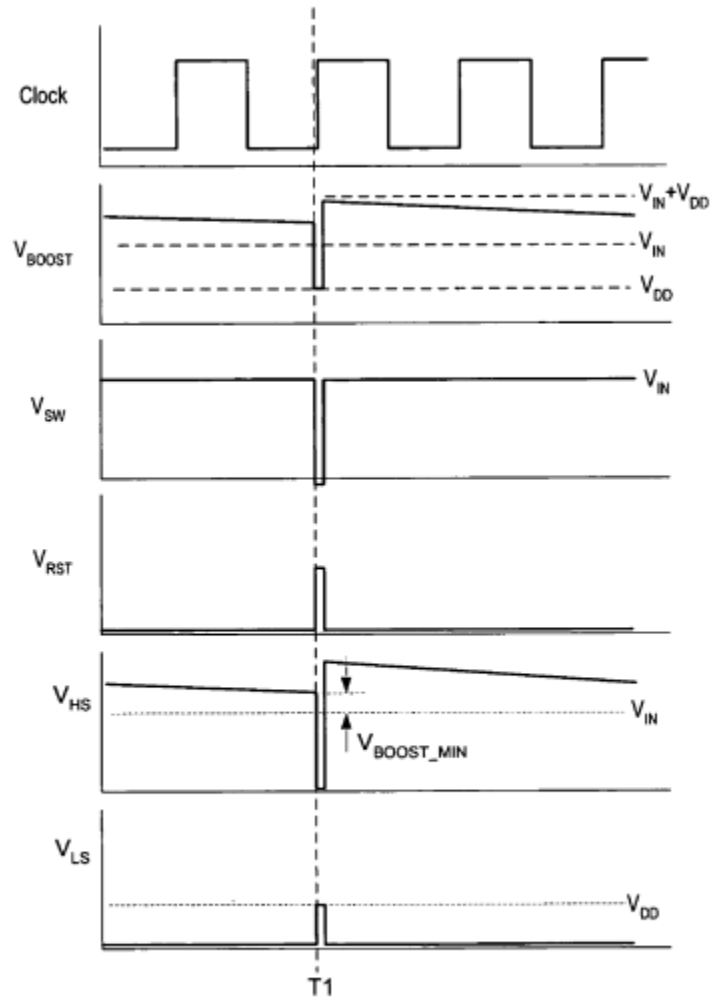
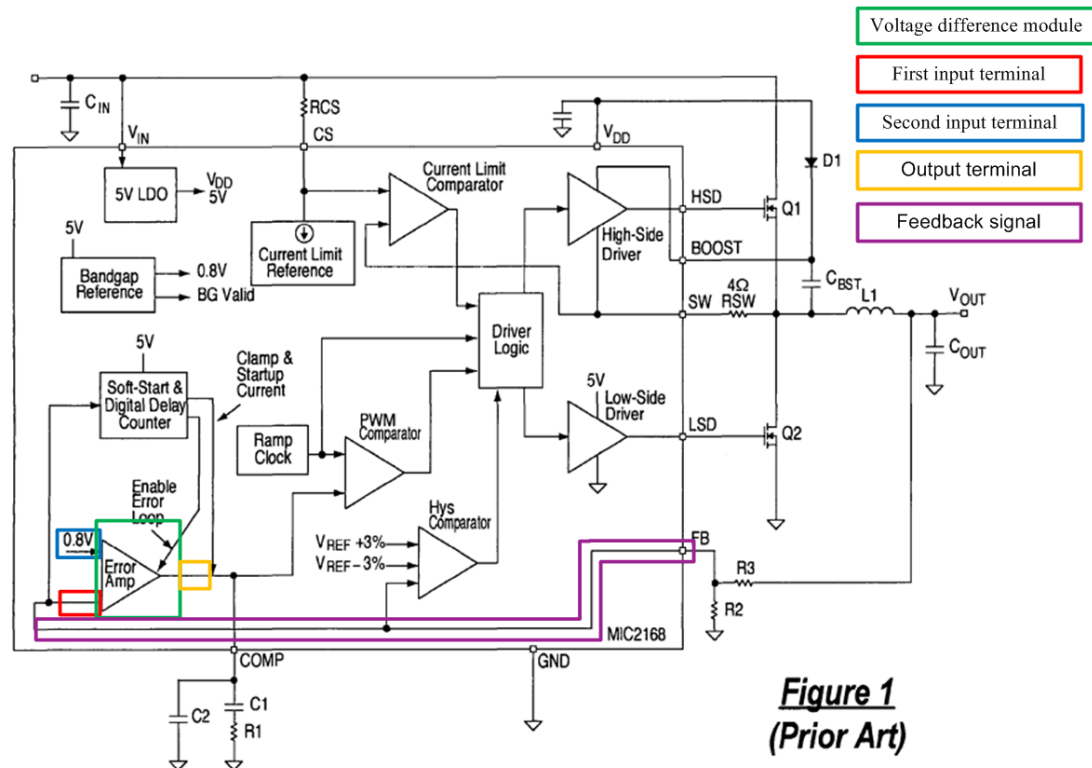


**Figure 3**

- c. Limitation 1[B]: a voltage difference module having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal of the voltage difference module is configured to receive a feedback signal representing the output voltage of the voltage converter, the second input terminal of the voltage difference module is configured to receive a reference voltage signal representing a desired value of the output voltage of the voltage converter, the voltage difference module is configured to compare the feedback signal with the reference voltage signal so as to provide a difference signal at the output terminal; and

158. Limitation 1[B] recites a voltage difference module that has two input terminals and an output terminal, and compares an output voltage feedback signal to a reference voltage to provide a difference signal at the output terminal. A POSITA would recognize that a voltage difference module and an error amplifier are equivalent. Galinski discloses that voltage converters typically include a feedback control loop formed by dividing down the output voltage  $V_{OUT}$  to provide a feedback voltage  $V_{FB}$  and feeding back the feedback voltage  $V_{FB}$  to an error amplifier where the feedback voltage ( $V_{FB}$ ) is compared to a reference voltage. *Id.* at 5:56-61. *Id.* at, 5:65-6:8. Fig. 1 of Galinski (annotated) is shown below. Galinski teaches a voltage difference module having a first input terminal, a second input terminal and an output terminal. The first input terminal is configured to receive a feedback signal representing the output voltage of the voltage converter. Galinski's error amplifier (voltage difference module) receives  $V_{FB}$  (derived from  $V_{OUT}$ ) and a

reference voltage (e.g., 0.8 V) at its input terminals and provides a difference signal at its output terminal. Thus, Galinski anticipates Limitation 1[B].



d. **Limitation 1[C]: wherein when the first comparing signal has the first logic state, the bootstrap refresh module is configured to decrease the output voltage of the voltage converter; and**

159. Limitation 1[C] recites that the bootstrap refresh module is configured to decrease the output voltage of the voltage converter when the bootstrap voltage signal is lower than the bootstrap refresh threshold (first comparing signal has the first logic state).

160. When the  $V_{\text{MON}}$  is equal to or less than the  $V_{\text{SW}}$  (the threshold voltage), the comparator element of one-shot comparator 112 changes state internally and (*supra* ¶¶95,96) generates reset pulse ( $V_{\text{RST}}$ ) of a short duration, causing the power switches Q1 and Q2 to switch in such a way to turn off Q1 and turn on Q2, thereby refreshing the bootstrap voltage  $V_{\text{BOOST}}$ . *Id.* at 9:3-21. During this recharge phase, the switching output voltage  $V_{\text{SW}}$  switches from input voltage  $V_{\text{IN}}$  to 0 volt temporarily. *Id.* at 10:19-23. As shown in the timing diagram of FIG. 3 below, the switching output voltage  $V_{\text{SW}}$  dips below the ground voltage. *Id.* at 10:23-24. A POSITA would understand that driving  $V_{\text{SW}}$  to ground will necessarily cause the output voltage to dip because  $V_{\text{SW}}$  is connected to the output via an LC filter. *Supra* ¶74.

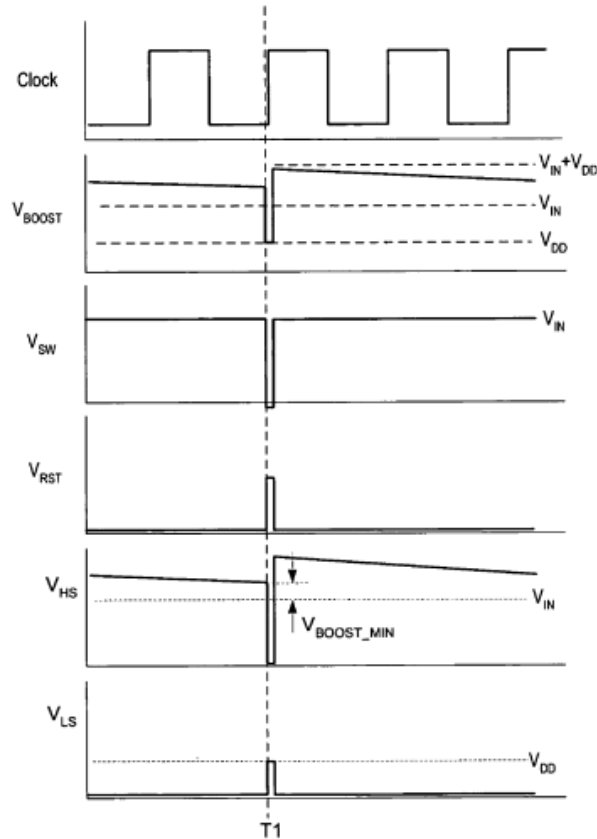


**Figure 3**

161. Thus, Galinski anticipates Limitation 1[C].

- e. **Limitation 1[D]: wherein when the feedback signal is smaller than the reference voltage signal, the bootstrap refresh control circuit is configured to control the high side switch and the low side switch to switch on and off based on the difference signal so as to charge the bootstrap capacitor for refreshing the bootstrap voltage signal.**

162. Limitation 1[D] recites circuitry switching on and off the high-side and low-side switches based on the difference signal (when the feedback signal is less than the reference voltage) so as to charge the bootstrap capacitor. As

explained in the overview of the '608 patent, the normal switching of the high-side and low-side switches to maintain the output voltage, also refreshes the bootstrap voltage. *See* ¶85.

163. Galinski discloses feeding back the voltage  $V_{FB}$  to an error amplifier where the feedback voltage ( $V_{FB}$ ) is compared to a reference voltage. *Id.* at 5:56-61. The feedback control loop regulates the output voltage  $V_{OUT}$  at a constant level over changing load conditions by varying the duty cycle of the power switches. That is, the high-side switch and the low-side switch are turned on alternately to increase or decrease the inductor current through the output inductor. *Id.* at 5:65-6:8. As a result of  $V_{OUT}$  decreasing from its desired level, the feedback signal ( $V_{FB}$ ) also necessarily decreases below a reference voltage. *Id.* 5: 59-61; *see also supra*, ¶¶64-69. In another example, the feedback signal would necessarily be below the reference voltage during a “soft start” of the converter, a well-known technique for slowly ramping up the output voltage so as to reduce inrush current. *Supra* ¶107. In a third example, the feedback signal would necessarily be below the reference voltage when exiting “pulse skipping” mode of the converter, a well-known technique for improving converter efficiency. *Supra* ¶69. In each of these examples, the error amplifier generates a difference signal so as to cause the high side and low-side switches to switch normally in order to maintain the output voltage at the desired value. *Id.* 5:64-6:7. Once the high-side and low-side switches

are switching normally, the bootstrap voltage is refreshed. In the conventional buck regulator such as that shown in Galinski FIG. 1, the bootstrap voltage (“BOOST”) is generated (refreshed) by switching of the switching output voltage  $V_{sw}$  by the driver logic. Thus, Galinski discloses switching on and off the high-side and low-side switches based on the difference signal so as to charge the bootstrap capacitor (including when the feedback signal is less than the reference voltage). Thus, Galinski anticipates Limitation 1[D].

## **2. Claim 11**

164. Claim 11 is directed to a voltage converter comprising a switching circuit and a bootstrap circuit substantially identical to the recitations in claim 1. Thus, claim 11, for at least the same reasons as claim 1, is unpatentable over the Galinski.

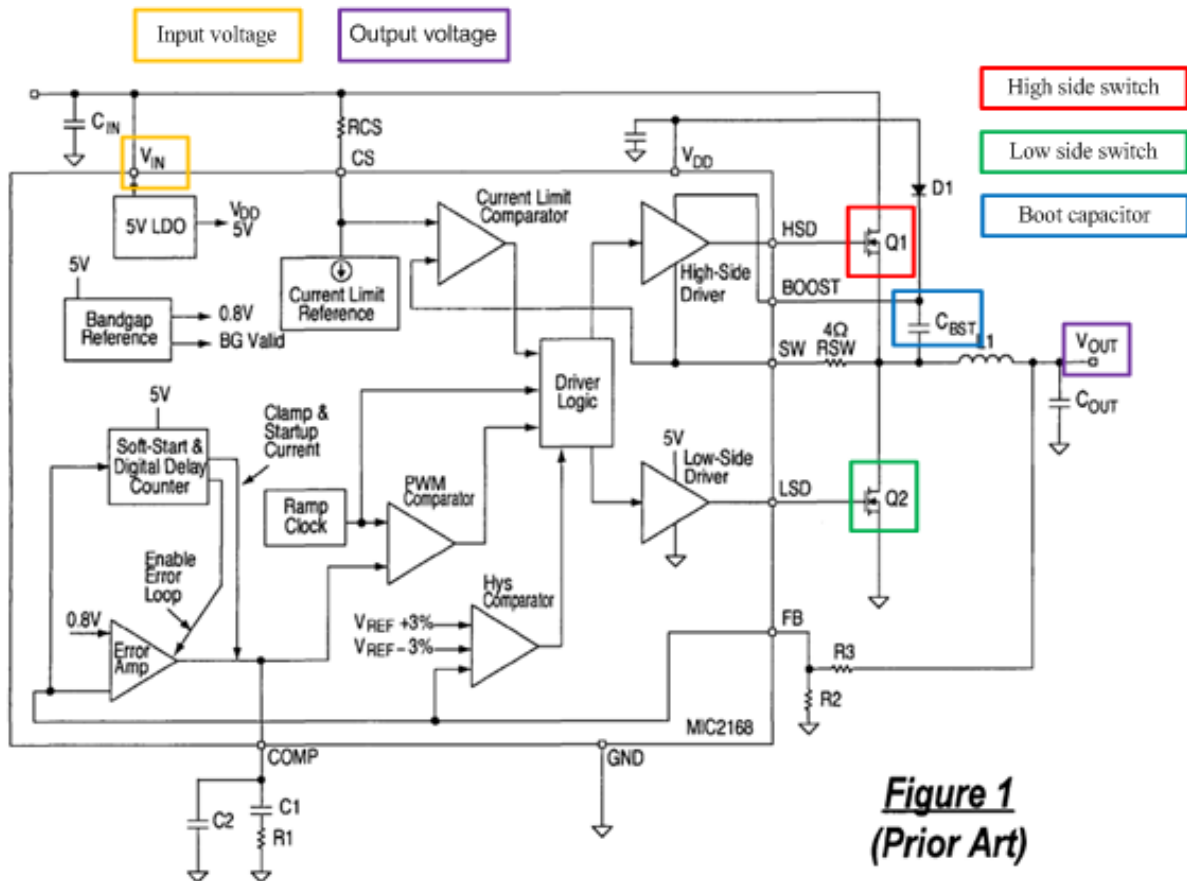
### **a. Limitation 11[PRE]: A voltage converter, comprising:**

165. To the extent that the preamble of claim 11 recites a limitation, Galinski discloses: “In many applications, a buck switching regulator is used to convert a DC input voltage to a regulated DC output voltage being near or lower than the input voltage.” *Id.* 1:27-29. A POSITA would understand that converting a DC input voltage to a regulated DC output voltage is the operation of a voltage converter. Thus, Galinski discloses a voltage converter.

- b. **Limitation 11[A]: a switching circuit having a high side switch and a low side switch, wherein the switching circuit is configured to receive an input voltage, and further configured to provide an output voltage based on switching the high side switch and the low side switch on and off;**

166. Limitation 11[A] recites a switching circuit comprising a high side and a low side switch that receives an input voltage and provides an output voltage based on switching the high switch and low side switch on and off. *Supra*, ¶¶149-152.

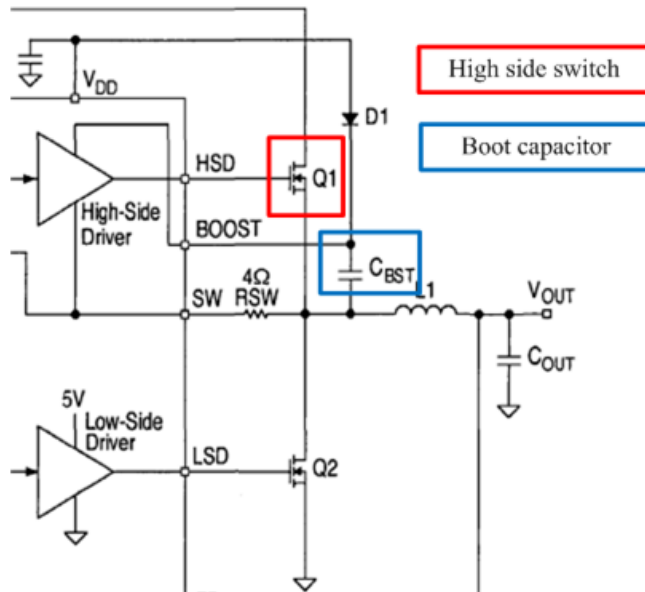
167. As illustrated below, Galinski Fig. 1 below (annotated), Galinski discloses a voltage converter comprising a high-side switch, a low-side switch, configured to receive an input voltage ( $V_{IN}$ ) and an output voltage ( $V_{OUT}$ ). Galinski states at *Id.* 1:36-47. Specifically, the high-side switch and the low-side switch are turned on alternately to increase or decrease the inductor current through the inductor. The capacitor of the LC network filters the output voltage to reduce ripples. The regulated output voltage  $V_{OUT}$  at the LC network is coupled back to the switching regulator for forming a feedback control loop to regulate the output voltage to a desired value. Galinski's Fig. 1 (shown below, annotated) is an exemplary circuit diagram of a buck switching regulator using N-channel transistors as the power switches.



- c. Limitation 11[B]: a bootstrap circuit comprising a bootstrap capacitor, wherein the bootstrap capacitor is charged for providing a bootstrap voltage signal for the high side switch; and

168. Limitation 11[B] recites a bootstrap circuit comprising a bootstrap capacitor that provides a bootstrap voltage signal to the high side switch. Galinski discloses such a bootstrap circuit. *Supra* ¶151.

169. As illustrated below, Galinski Fig. 1 below (cropped and annotated), Galinski discloses a bootstrap circuit comprising voltage signal to supply a high side driver of the high side switch a bootstrap capacitor for providing a bootstrap.



- d. Limitation 11[C]: a bootstrap refresh control circuit comprising: a bootstrap refresh module, wherein the bootstrap refresh module comprises a first comparing module having a first input terminal, a second input terminal and an output terminal, and wherein the first input terminal of the first comparing module is configured to receive the bootstrap voltage signal, the second input terminal of the first comparing module is configured to receive a bootstrap refresh threshold, and the first comparing module is configured to compare the bootstrap voltage signal with the bootstrap refresh threshold to provide a first comparing signal having a first logic state and a second logic state at the output terminal, and wherein the first comparing signal has the first logic state when the bootstrap voltage signal is lower than the bootstrap refresh threshold, and the first comparing signal has the second logic state when the bootstrap voltage signal is larger than the bootstrap refresh threshold; and

170. Limitation 11[C] recites same claim limitations as limitation 1[A], thus the same arguments apply. *Supra* ¶¶154-157.

- e. **Limitation 11[D]: a voltage difference module having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal of the voltage difference module is configured to receive a feedback signal representing the output voltage of the voltage converter, the second input terminal of the voltage difference module is configured to receive a reference voltage signal representing a desired value of the output voltage of the voltage converter, the voltage difference module is configured to compare the feedback signal with the reference voltage signal so as to provide a difference signal at the output terminal; and wherein**

171. Limitation 11[D] recites same claim limitations as limitation 1[B], thus the same arguments apply. *Supra* ¶¶158.

- f. **Limitation 11[E]: when the first comparing signal has the first logic state, the bootstrap refresh module is configured to decrease the output voltage of the voltage converter; and**

172. Limitation 11[E] recites same claim limitations as limitation 1[C], thus the same arguments apply. *Supra* ¶¶159-161.

- g. **Limitation 11[F]: wherein when the feedback signal is smaller than the reference voltage signal, the bootstrap refresh control circuit is configured to control the high side switch and the low side switch to switch on and off based on the difference signal so as to charge the bootstrap capacitor for refreshing the bootstrap voltage signal.**

173. Limitation 11[F] recites same claim limitations as limitation 1[D], thus the same arguments apply. *Supra* ¶¶162-163.

### 3. Claim 12

174. Claim 12 is a method claim reciting a method of use for a voltage converter. Galinski anticipates each step of claim 12.

- a. **Limitation 12[PRE]: A bootstrap refresh control method for a voltage converter, wherein the voltage converter comprises a high side switch, a low side switch and a bootstrap capacitor for providing a bootstrap voltage signal to supply a high side driver of the high side switch, and wherein the voltage converter is configured to receive an input voltage and to provide an output voltage based on driving the high side switch and the low side switch to switch on and off, and wherein the bootstrap refresh control method comprising:**

175. Limitation 12[PRE] recites the same structure as Limitation 1[PRE], thus the same arguments apply. *Supra*, ¶¶149-153.

- b. **Limitation 12[A]: sensing the bootstrap voltage signal of the voltage converter;**

176. Galinski bootstrap control circuit comprises comparator 112 which receives a monitor voltage  $V_{MON}$  as illustrated in Galinski Fig. 2 shown below (cropped and annotated). A POSITA would understand that monitoring a voltage signal is the same as sensing a voltage signal. *See* Galinski 8:30-34. Thus, Galinski teaches Limitation 12[A].

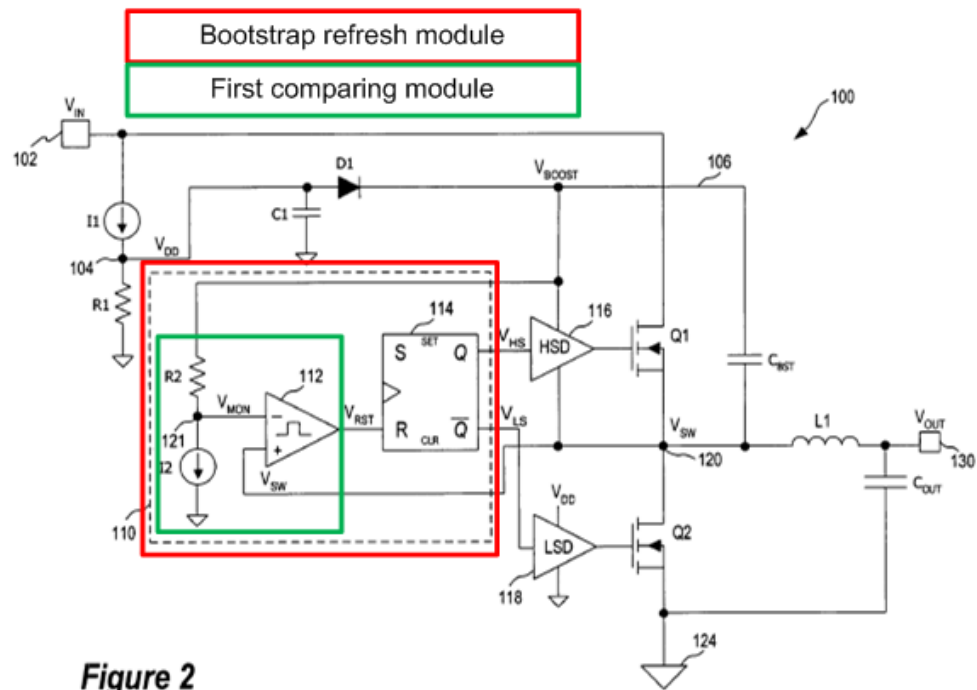


**Figure 2**

- c. **Limitation 12[B]: comparing the bootstrap voltage with a bootstrap refresh threshold to provide a first comparing signal, wherein the first comparing signal has a first logic state and a second logic state, and wherein the first comparing signal has the first logic state when the bootstrap voltage is lower than the bootstrap refresh threshold, and wherein the first comparing signal has the second logic state when the bootstrap voltage signal is larger than the bootstrap refresh threshold;**

177. Galinski shows in Fig. 2 (annotated and cropped) above, a one-shot comparator 112. A POSITA would know that a one-shot comparator circuit 112 comprises a comparator driving a one-shot. *Supra* ¶¶95,96. A POSITA would understand that the comparator element of the one-shot comparator 112 would output a first comparing signal with a first logic state and a second logic state

based on comparing  $V_{\text{MON}}$ , which represents the bootstrap voltage, to the bootstrap refresh threshold,  $V_{\text{IN}} + V_{\text{TH\_HS}}$ . *Supra* ¶99.

178. Galinski teaches that when  $V_{\text{SW}}$  is equal or greater than  $V_{\text{MON}}$  comparator circuit 112 generates a reset pulse  $V_{\text{RST}}$ . A POSITA would understand that the comparison of  $V_{\text{MON}}$  and  $V_{\text{SW}}$  generates an output of the comparator (input to the one-shot) and that output would be one of two logical states depending on the state of the inputs. Thus, Galinski teaches Limitation 12[B].

d. **Limitation 12[C]: determining whether the bootstrap voltage signal is smaller than the bootstrap refresh threshold or not; and**

179. Limitation 12[C] recites determining whether the voltage signal is smaller than the bootstrap refresh threshold.

180. Galinski teaches that comparator circuit 112 generates a reset pulse when  $V_{\text{MON}}$  is equal or less than  $V_{\text{SW}}$  at *Id.* 9:3-5. Thus, Galinski teaches Limitation 12[C].

e. **Limitation 12[D]: decreasing the output voltage of the voltage converter by a bootstrap refresh circuit once the bootstrap voltage signal is determined to have dropped to be smaller than the bootstrap refresh threshold; and**

181. Limitation 12[D] recites decreasing the output voltage when the bootstrap voltage signal is determined to be lower than the bootstrap refresh threshold.

182. Galinski teaches when the  $V_{\text{MON}}$  is equal to or less than the  $V_{\text{SW}}$  (the threshold voltage), the comparator generates reset pulse ( $V_{\text{RST}}$ ) of a short duration, causing the power switches Q1 and Q2 to switch in such a way to turn off Q1 and turn on Q2, thereby refreshing the bootstrap voltage  $V_{\text{BOOST}}$ . *Id.* at 9:3-21. During this recharge phase, the switching output voltage  $V_{\text{SW}}$  switches from input voltage  $V_{\text{IN}}$  to 0 volt temporarily. *Id.* at 10:19-23. As shown in the timing diagram of FIG. 3 of Galinski, the switching output voltage  $V_{\text{SW}}$  dips below the ground voltage. *Id.* at 10:23-24. A POSITA would understand that driving  $V_{\text{SW}}$  to ground, even temporarily, will cause the output voltage to dip because  $V_{\text{SW}}$  is connected to the output via an LC filter. Thus, Galinski anticipates Limitation 12[D].

f. **Limitation 12[E]: wherein when the output voltage of the voltage converter is decreased, switching the high side switch and the low side switch on and off so as to refresh the bootstrap voltage signal.**

183. Limitation 12[E] recites switching on and off the high-side and low-side switches based on the difference signal (when the feedback signal is less than the reference voltage) so as to refresh the bootstrap voltage signal.

184. Galinski discloses feeding back the feedback voltage  $V_{\text{FB}}$  to an error amplifier where the feedback voltage ( $V_{\text{FB}}$ ) is compared to a reference voltage. *Id.* at 5:56-61. The feedback control loop regulates the output voltage  $V_{\text{OUT}}$  at a constant level over changing load conditions by varying the duty cycle of the

power switches. That is, the high-side switch and the low-side switch are turned on alternately to increase or decrease the inductor current through the output inductor. *Id.* at 5:65-6:8. In the conventional buck regulator such as that shown in FIG. 1 of Galinski, the bootstrap voltage (“BOOST”) is generated (refreshed) by switching of the switching output voltage  $V_{sw}$ . Thus, Galinski discloses switching on and off the high-side and low-side switches based on the difference signal so as to charge the bootstrap capacitor (including when the feedback signal is less than the reference voltage). Thus, Galinski anticipates Limitation 12[E].

**C. Ground 3: Claims 1, 2, 11, 12, and 16 are rendered obvious by Galinski in view of Li and/or the knowledge of a POSITA**

**1. Reasons to combine**

185. A POSITA would have been motivated to modify or combine Galinski with Li and/or the knowledge of a POSITA to arrive at the features of claims 1-2, 11, 12, and 16 for the reasons presented below.

**a. Analogous Art**

186. Galinski and Li are each in the same field DC-DC converters and therefore analogous art to the '608 Patent, namely methods of recharging a bootstrap capacitor in power converters. EX1005 at 2:12, 2:44-48; EX1008, EX1011 at [0003]-[0006]. Galinski and Li are also each reasonably pertinent to a problem the inventors of the '608 Patent attempted to solve, namely the problem of

timely recharging a bootstrap capacitor for maintaining high side voltage in buck converters. *Id.*

**b. Motivation to Combine**

187. A POSITA would understand that Galinski could be readily modified to include features taught by Li and/or the knowledge of a POSITA for advantageous reasons. For example, Galinski would be motivated to use the conventional voltage comparator of Li to compare the bootstrap voltage to a bootstrap threshold. Doing so would avoid the leakage on the bootstrap capacitor that results from the  $V_{MON}$  generating circuit of Galinski. In addition, Galinski could be modified to include Li's monitoring of  $V_{BST}$  using hysteresis to avoid "chattering."

**c. Reasonable Expectation of Success**

188. The references include similar arrangements of well-understood components and use predictable technology in routine and conventional ways. Li offers different circuits to achieve the same goal as Galinski, that is, a DC-DC converter using a bootstrap capacitor that is sensed and refreshed as needed. A POSITA would find it straightforward to adapt the ideas presented in Li, or those within the knowledge of a POSITA, to Galinski's DC-DC converter.

**2. Claim 1**

189. Galinski teaches every element of Claim 1. *See* ¶¶149-163. In addition to every element of claim 1 being expressly or inherently anticipated by Galinski, it is my opinion a POSITA would find it obvious, for the reasons stated above. *See* §III.B, §III.C, §V.A.

3. **Claim 2**

190. Claim 2 depends from Claim 1.

- a. **Limitation 2[A]: The bootstrap refresh control circuit of claim 1, wherein the bootstrap refresh threshold comprises a first threshold and a second threshold, wherein the first threshold is higher than a ground potential and lower than the second threshold; and wherein**

191. Li discloses a bootstrap refresh threshold comprising two thresholds for hysteresis, a first high threshold,  $V_{H1}$ , and a first low threshold,  $V_{L1}$ , where the first low threshold is higher than ground and lower than the first high threshold. EX1008, EX1011, ¶109. It is my opinion that a POSITA would find limitation 2[A] to be obvious over the disclosures of Galinski and Li.

- b. **Limitation 2[B]: the first comparing signal has the first logic state when the bootstrap voltage signal is lower than the first threshold, and wherein the first comparing signal has the second logic state when the bootstrap voltage signal is larger than the second threshold.**

192. In Li, if the bootstrap voltage drops lower than the first low threshold the comparing signal (RFS) changes to a first logic state and when the bootstrap

voltage rises above the first high threshold, the comparing signal (RFS) changes to a second logic state. *Id.* It is my opinion that a POSITA would find limitation 2[B] to be obvious over the disclosures of Galinski and Li.

4. **Claim 11**

193. Galinski teaches every element of Claim 11 *See* ¶¶164-173. In addition to every element of claim 11 being expressly or inherently anticipated by Galinski, it is my opinion a POSITA would find it obvious, for the reasons stated above. *See* §III.B, §III.C, §V.A.

5. **Claim 12**

194. Galinski teaches every element of Claim 12. *See* ¶¶174-184. In addition to every element of claim 12 being expressly or inherently anticipated by Galinski, it is my opinion a POSITA would find it obvious, for the reasons stated above. *See* §III.B, §III.C, §V.A.

6. **Claim 16**

- a. **The bootstrap refresh control circuit [sic] of claim 12, wherein the bootstrap refresh threshold comprises a first threshold and a second threshold, and wherein the first threshold is higher than a ground potential and lower than the second threshold; and wherein the first comparing signal has the first logic state when the bootstrap voltage signal is lower than the first threshold, and wherein the first comparing signal has the second logic state when the bootstrap voltage signal is higher than the second threshold.**

195. Claim 16 depends on claim 12 and is essentially identical to Limitations 2[A] and 2[B]. Accordingly, Galinski and Li render Limitation 16 obvious for the same reasons. *See* ¶¶191,192.

**D. Ground 4: Claims 1, 6, 11, 12 and 15 are rendered obvious by Wong**

**1. Claim 1**

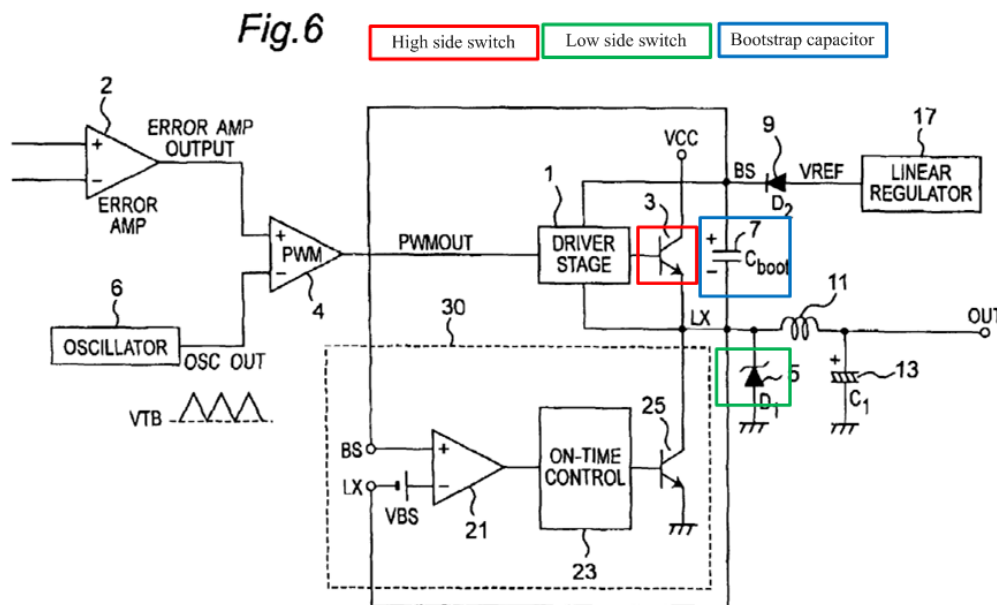
- a. **Limitation 1[PRE]: A bootstrap refresh control circuit for a voltage converter, wherein the voltage converter comprises a high side switch, a low side switch and a bootstrap capacitor for providing a bootstrap voltage signal to supply a high side driver of the high side switch, and wherein the voltage converter is configured to receive an input voltage at an input terminal and to provide an output voltage at an output terminal based on driving the high side switch and the low side switch to switch on and off, and**

196. Limitation 1[PRE] limits the scope of claim 1 to circuits for use in voltage converters having high side and low side switches and a bootstrap capacitor to supply a bootstrap voltage to a driver of the high side switch, where the input voltage is converted to the output voltage based on switching the high side and low side switches on and off.

197. Wong discloses an integrated step-down DC-DC converter system, having an NPN top power transistor and a bootstrap capacitor configured to store a voltage to turn on the power transistor and, more particularly, to a control circuit

and a method for controlling the charge of the bootstrap capacitor. EX1007 at 1:9-42.

198. A switching node (LX) switches between a high voltage (up to VCC) when the power transistor turns on, and  $(-V_d)$  during the off-time of the power transistor, where  $V_d$  is the forward diode voltage drop of a low-side diode connected between the switching node and ground. *Id.*, Fig. 6.



199. A POSITA would understand that a low-side diode functions as a low-side switch, that diodes and switches are interchangeable in Wong's converter system, and that replacing Wong's low-side diode with a low-side switch is an obvious variation of Wong's converter system. *Supra* ¶¶65-68. The motivation for using a low-side switch is for greater conversion efficiency and is well-known in the art. *supra* ¶68.

200. Thus, Wong teaches circuits for use in voltage converters having high side (3) and low side (5) switches and a bootstrap capacitor (7) to supply a bootstrap voltage to a driver (1) of the high side switch.

201. Furthermore, a POSITA looking at Wong's circuit diagram would understand that the converter system receives input voltage VCC and converts the input voltage to an output voltage (OUT) based on operations of the high-side switch and low-side diode (or switch). That is, Wong discloses switching the power transistor on and off to switch the switching node LX between a high voltage (up to VCC) and a low voltage (-VD1) to provide a predictable output voltage based on the voltage at the switching node and associated circuit components. EX1007 at 1:60-67. Thus, it is my opinion that Wong renders obvious limitation 1[PRE] to a POSITA.

- b. Limitation 1[A]: wherein the bootstrap refresh control circuit comprising: a bootstrap refresh module, wherein the bootstrap refresh module comprises a first comparing module having a first input terminal, a second input terminal and an output terminal, and wherein the first input terminal of the first comparing module is configured to receive the bootstrap voltage signal, the second input terminal of the first comparing module is configured to receive a bootstrap refresh threshold, and the first comparing module is configured to compare the bootstrap voltage signal with the bootstrap refresh threshold to provide a first comparing signal having a first logic state and a second logic state at the output terminal, and wherein the first comparing signal has the first logic state when the bootstrap voltage signal is lower than the bootstrap refresh threshold, and wherein the first comparing signal has the second logic state when the bootstrap voltage signal is larger than the bootstrap refresh threshold; and

202. Limitation 1[A] recites the structure of “a bootstrap refresh module” that comprises a “first comparing module” having two inputs and an output that outputs a “first comparing signal” by comparing the bootstrap voltage signal and the bootstrap refresh threshold and defines the first comparing signal as having one of two logic states depending on which input signal is larger.

203. Wong discloses a BS voltage detector 21 that “detects the voltage across the bootstrap capacitor 7, and compares the detected voltage with a predetermined voltage VBS. The voltage VBS is the preset threshold voltage

EX1007 at 4:67-5:3. *See* Fig. 6 annotated below.

205. Thus, a POSITA would understand that Wong's BS voltage detector compares the bootstrap voltage and a predetermined voltage threshold (VBS) to produce an output signal having one of two states, including a high state when the bootstrap voltage is less than a predetermined threshold. Thus, Wong discloses a bootstrap refresh control circuit including a comparing module configured to compare the bootstrap voltage to a threshold and produce an output having one of two states. *Id.*, 4:63-5:7, Fig. 6, element 21. Thus, Wong discloses the recited comparing signal.

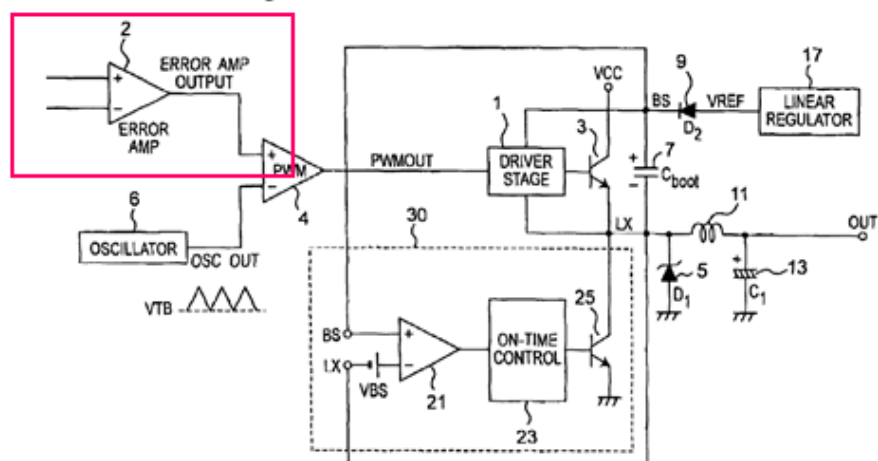
206. Thus, it is my opinion that Wong renders obvious limitation 1[A] to a POSITA.

- c. **Limitation 1[B]: a voltage difference module having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal of the voltage difference module is configured to receive a feedback signal representing the output voltage of the voltage converter, the second input terminal of the voltage difference module is configured to receive a reference voltage signal representing a desired value of the output voltage of the voltage converter, the voltage difference module is configured to compare the feedback signal with the reference voltage signal so as to provide a difference signal at the output terminal; and**

207. Limitation 1[B] recites “a voltage difference module” that has two input terminals and an output terminal, and compares an output voltage feedback signal to a reference voltage to provide a difference signal at the output terminal.

208. Wong discloses, “As shown in FIG. 3, in a PWM DC-DC converter, the duty cycle is determined by a comparator 4 which compares the output of the error amplifier 2 with a triangular signal produced from oscillator 6. As shown in Wong FIG. 4B, when the error amplifier output is higher than the triangular oscillator output, the PWM output is high and the power transistor 3 is turned on.”  
EX1007 at 5:23-23, *See* Fig. 3 annotated below.

Fig.6



209. While Wong does not explicitly state the connection, a POSITA would recognize that Wong is disclosing a DC-DC converter that compares the output (or a divided-down portion of the output) with a reference voltage and adjusts the PWM to cause the voltage being fed back to equal the reference voltage. Most DC-DC converters work in this general fashion.

210. Thus, Wong's error amplifier is configured to receive a reference voltage signal representing a desired value of the output voltage of the voltage converter and is configured to receive a feedback signal representing the output voltage of the voltage converter, and is configured to compare the feedback signal with the reference voltage signal so as to provide a difference signal at the output terminal. Thus, it is my opinion that Wong renders obvious limitation 1[B] to a POSITA.

- d. **Limitation 1[C]: wherein when the first comparing signal has the first logic state, the bootstrap refresh module is configured to decrease the output voltage of the voltage converter; and**

211. Limitation 1[C] recites that the bootstrap refresh module is configured to decrease the output voltage of the voltage converter when the bootstrap voltage signal is lower than the bootstrap refresh threshold (first comparing signal has the first logic state).

212. Wong discloses, “When the voltage across the bootstrap capacitor becomes less than the voltage VBS, the BS voltage detector 21 produces a high level signal. When . . . the BS voltage detector 21 produces high level signals, the on-time control 23 produces a high level signal to turn on the secondary transistor 25. “When the secondary transistor 25 is turned on, LX voltage will be pulled near to the ground voltage.” EX1007 at 5:3-24. That is, Wong discloses pulling the switching node to ground potential when the voltage across the bootstrap capacitor becomes less than a threshold.

213. Furthermore, a POSITA would understand, based on the well-understood behavior of standard circuit components connecting the switching node to the output of the voltage converter, that grounding the switching node in this way necessarily causes a decrease in the output voltage of the voltage converter. That is, when the switching node is pulled to ground, Wong’s output node is

necessarily decreased by way of inductor 11. Thus, Wong inherently discloses this feature.

214. A POSITA would also understand that the principle of pulling the switching-node voltage near to ground to recharge the bootstrap capacitor is applicable to other configurations of voltage converters. For example, if Wong's low-side diode was replaced with a low-side switch, Wong's secondary switch would be unnecessary for pulling the switching-node voltage near to ground, because that function could be performed by the low-side switch. Similarly, although Wong discloses a PWM DC-DC converter, the teaching of grounding the switching node (thus decreasing the output voltage) to recharge the bootstrap capacitor is broadly applicable to DC-DC converters having different timing characteristics. Thus, it is my opinion that Wong renders obvious limitation 1[C] to a POSITA.

- e. **Limitation 1[D]: wherein when the feedback signal is smaller than the reference voltage signal, the bootstrap refresh control circuit is configured to control the high side switch and the low side switch to switch on and off based on the difference signal so as to charge the bootstrap capacitor for refreshing the bootstrap voltage signal.**

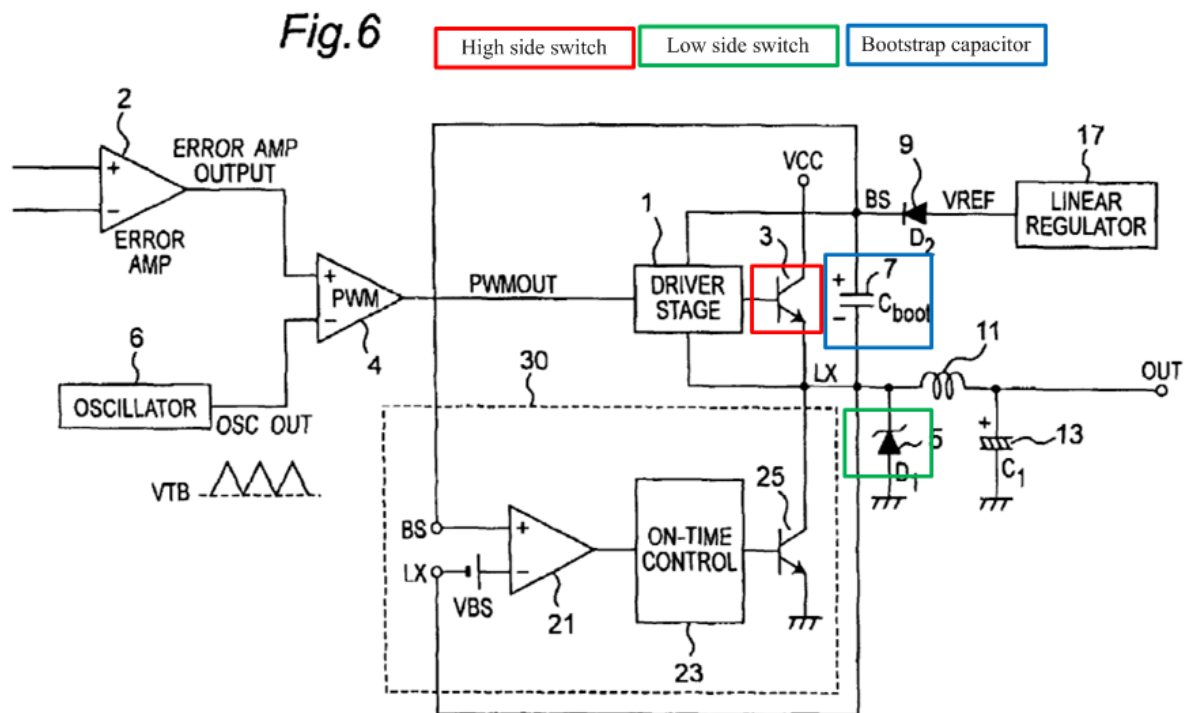
215. Limitation 1[D] recites circuitry switching on and off the high-side and low-side switches based on the difference signal when the feedback signal is less than the reference voltage so as to charge the bootstrap capacitor. As

explained in the overview of the '608 patent, the normal switching of the high-side and low-side switches to maintain the output voltage also refreshes the bootstrap voltage. *See* ¶85.

216. A POSITA would understand that the purpose of adjusting the timing and duration that the power switching period is for the voltage converter to provide a regulated voltage output. Thus, when the output of the error amplifier indicates that the output voltage is different (either less than or greater than) than the reference signal, Wong's control circuit is configured to control the high side switch to switch on and off based on the difference signal. A POSITA would understand that Wong regulates the output voltage as in a conventional DC-DC converter, i.e., as a result of the output voltage decreasing below a reference voltage, the error amp causes the high side switch to switch on and off in order to maintain the output voltage to the desired value. When the high side switch is turned off, node LX goes negative (as a result of decreasing current in the inductor) turning on diode switch  $D_1$  (the low-side switch). Once the high-side and low-side switches are switching normally, the bootstrap voltage is refreshed. Thus, Wong discloses switching on and off the high-side and low-side switches based on the difference signal.

217. Wong also discloses a voltage converter having at a high side switch, a low-side switch, and a bootstrap capacitor to supply a bootstrap voltage to a

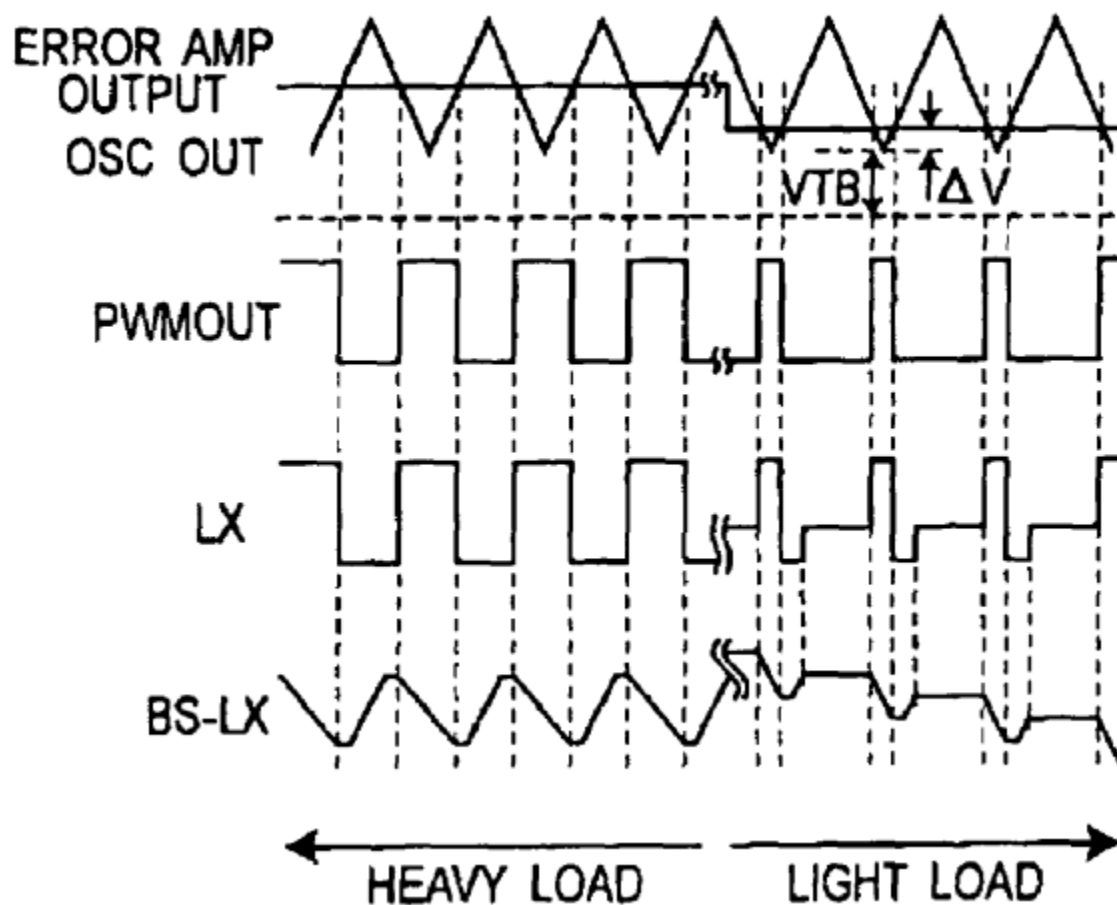
driver of the high side switch, where the input voltage is converted to the output voltage based on switching at least the high side switch on and off. EX1007 at 4:30-52, Fig 6 (reproduced below annotated).



218. Wong's low side switch is a freewheeling diode (D<sub>1</sub>). A POSITA would know that a diode can act as a passive switch, See ¶65. Furthermore, it is well known that replacing the freewheeling diode with a synchronous switch (synchronous rectifier) improves converter efficiency. See ¶68. A POSITA would be motivated to replace Wong's freewheeling diode with a low side switch in order to improve efficiency. Therefore, Wong renders obvious a low side switch.

219. Furthermore, Wong discloses an error amplifier that compares an output voltage feedback signal to a reference voltage to provide a difference signal at the output terminal. EX1007, Fig. 6, element 2.

220. Wong further discloses connecting the switching node (LX) to ground when the bootstrap voltage becomes less than a predetermined threshold (VBS) otherwise switching at least the high-side switch on and off at a duty cycle to regulate the output voltage. *Id.* at 5:6-13, Fig. 4B (shown below). In normal operation, when the feedback signal is equal to the reference voltage signal and then the output voltage is decreased by pulling LX voltage to ground, the feedback signal will necessarily fall below the reference voltage. *Supra* ¶69. During a soft start, the feedback signal will also necessarily be below the reference voltage. *Supra* ¶¶69, 107. And when exiting “pulse skipping” mode, the feedback signal will also necessarily be below the reference voltage. *Supra* ¶69. Thus, it is my opinion that Wong also discloses Limitation 1[D].



2. Claim 6

- a. Limitation 6[A]: The bootstrap refresh control circuit of claim 1, wherein the bootstrap refresh module further comprises: a Constant On Time circuit configured to provide a COT control signal having a first logic state and a second logic state so as to set a constant on time for the low side switch, wherein the COT control signal has the first logic state during the constant on time, and wherein the COT control signal has the second logic state beyond the constant on time; and

221. Limitation 6[A] recites a Constant On Time circuit configured to provide a COT control signal so as to set a constant on time for the low side switch.

222. Wong discloses an on-time control configured to only switch on the secondary (low-side) switch based on a triangular signal and a predetermined voltage. Thus, Wong discloses an on-time control that provides a COT control signal so as to set a constant on time for the secondary switch. It would be obvious for a POSITA to replace diode, D<sub>1</sub> (functioning as a low-side switch), with a synchronous rectifier (switch) to achieve better efficiency. This is well known. Once the diode is replaced by a synchronous rectifier, a POSITA would be further motivated to use the synchronous rectifier as the secondary switch driven by the On-Time Control block, 23.

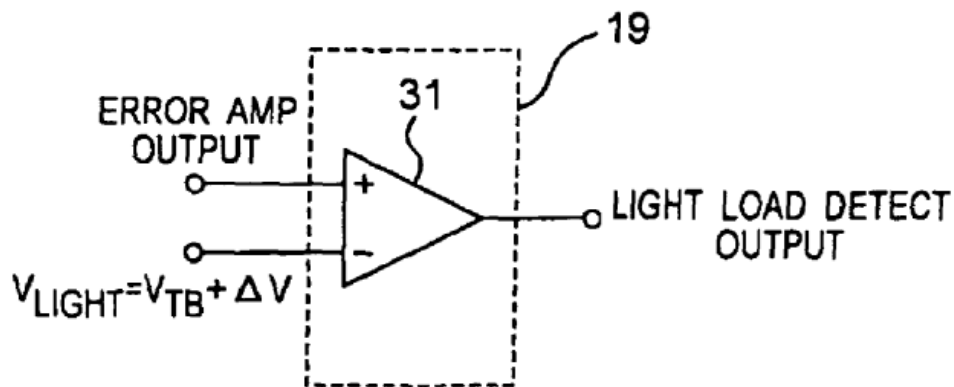
- b. **Limitation 6[B]: a first logic module having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal of the first logic module is configured to receive the first comparing signal, the second input terminal of the first logic module is configured to receive the COT control signal, and the first logic module is configured to conduct a logic operation to the first comparing signal and the COT control signal for providing a bootstrap refresh signal having a first logic state and a second logic state at the output terminal; and**

223. Limitation 6[B] recites a logic module having two inputs and an output, the inputs configured to receive the COT control signal and the comparing

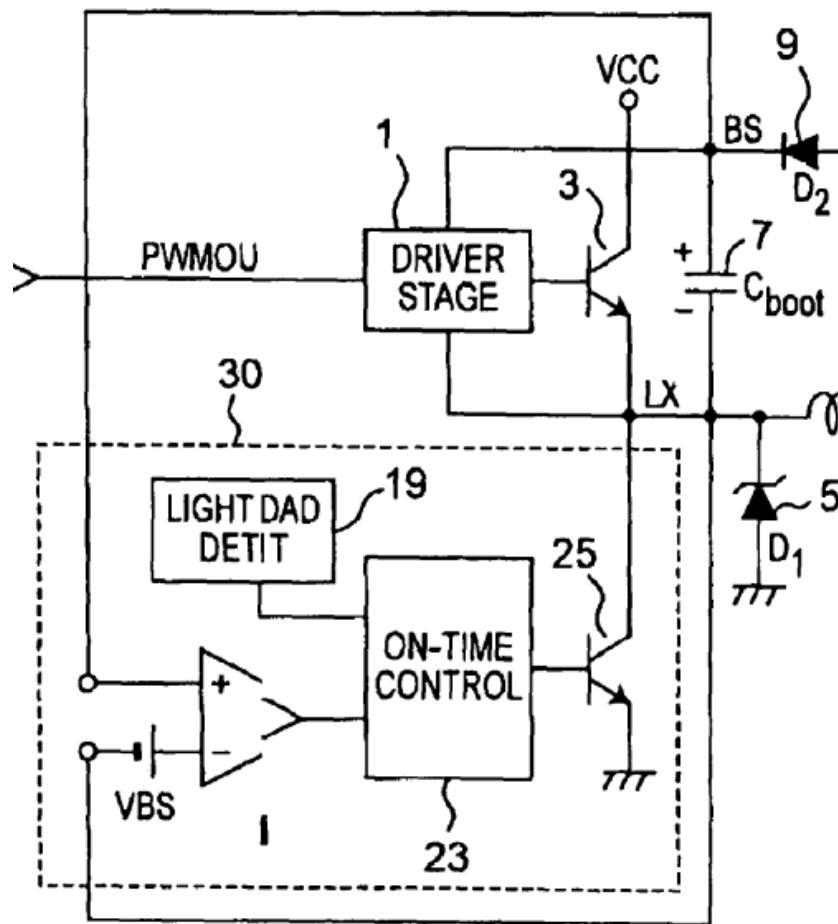
signal of Limitation 1[A], the logic module configured to perform logic on the input signals and provide a bootstrap refresh signal at the output terminal.

224. Wong discloses a light-load detector, show in Fig. 4A below, which compares the output of the error amplifier with a predetermined voltage. *See* Wong 5:14-19. Wong's light-load detector outputs a logical signal indicating whether a light load has been detected.

**Fig. 4A**



225. Wong further discloses a bootstrap voltage detector shown in Fig. 3 below (cropped), that monitors the voltage across the bootstrap capacitor. When the voltage across the bootstrap capacitor is lower than the threshold voltage, the bootstrap voltage detector will output a “bootstrap low” signal. *Id.* 2:51-57.



226. Wong discloses an on-time control circuit, Fig. 5A shown below, that generates a pulse determined by the ramp signal generated by the oscillator and a predetermined voltage higher than the error amplifier output during light load conditions. Wong shows a timing diagram illustrating the operation of Fig. 5A in Fig. 5B below. A POSITA would know that the oscillator output is a fixed and known amplitude in order for the power supply to function properly, and that the

input, V1, to the on time control circuit would be a fixed voltage, thus generating a fixed pulse with a constant pulse width.

**Fig.5A**

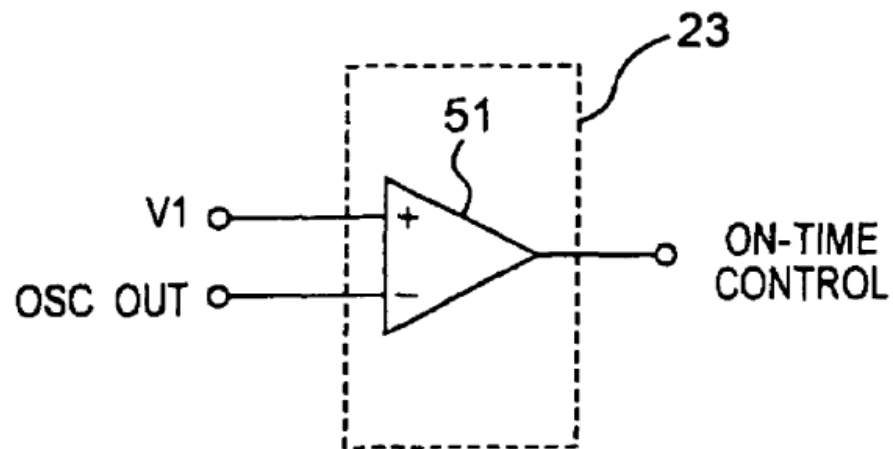
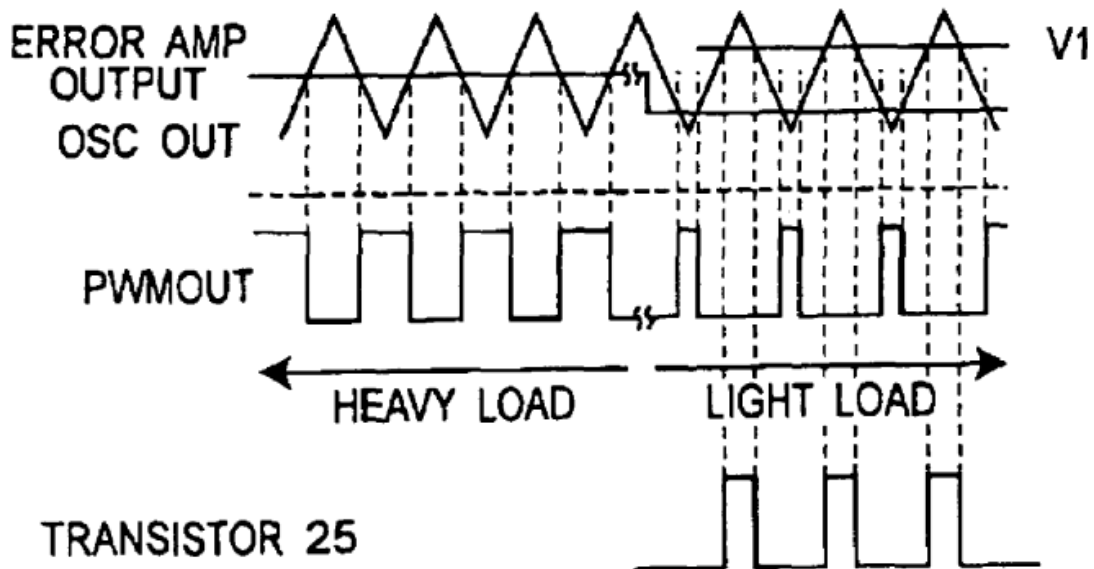


*Fig.5B*



227. Wong states that when the light load signal “and” the bootstrap low signal are received, a secondary switch will turn on during the off time of the power transistor. A POSITA would understand that a logical AND operation of the bootstrap low signal and the light load signal is performed to generate an output that has a first state when the logical operation (AND) is true and a second state when the logical operation (AND) is false. Thus, Wong teaches Limitation 6[B].

- c. **Limitation 6[C]: wherein the bootstrap refresh signal has the first logic state when the first comparing signal has a first logic state so as to turn the low side switch on, and the bootstrap refresh signal has a second logic state when the COT control signal has a second logic state so as to turn the low side switch off.**

228. Limitation 6[C] recites the bootstrap refresh signal having a first logic state when the bootstrap voltage is lower than the threshold so as to turn the low side switch on, and the bootstrap refresh signal has a second logic state beyond the constant on time of the low-side switch, so as to turn the low side switch off.

229. Wong states that when both the light load signal and bootstrap low signal are received, a secondary switch will turn on during the off-time of the power transistor, pulling the switching node voltage to nearly ground, thus charging the bootstrap capacitor. A POSITA would recognize the benefit of replacing diode D<sub>1</sub> with a synchronous rectifier (a switch) to achieve improved efficiency. Moreover, once the synchronous rectifier is installed, a POSITA would use that switch to perform the function of the secondary switch, 25. A POSITA would further understand that Wong teaches the logical AND operation on the light load signal and the bootstrap low signal, so that if either one is false, the output of the AND operation will be false. Therefore, a POSITA would understand that the constant on-time circuit of Fig. 5A will turn off the switch operating as a replacement for diode D<sub>1</sub> once the constant on time is completed.

230. Therefore, Wong teaches Claim 6.

### **3. Claim 11**

231. Claim 11 is directed to a voltage converter comprising a switching circuit and a bootstrap circuit substantially identical to the recitations in claim 1.

Thus, claim 11, for at least the same reasons as claim 1, is unpatentable over Wong.

a. **Limitation 11[PRE]: A voltage converter, comprising:**

232. Limitation 11[PRE], to the extent it is a limitation of claim 11, recites a voltage converter. Wong discloses a voltage converter. *See* ¶¶196-201.

b. **Limitation 11[A]: a switching circuit having a high side switch and a low side switch, wherein the switching circuit is configured to receive an input voltage, and further configured to provide an output voltage based on switching the high side switch and the low side switch on and off;**

233. Limitation 11[A] recites a switching circuit comprising a high side and a low side switch that receives an input voltage and provides an output voltage based on switching the high and low side switches. Wong teaches such a switching circuit. *See* ¶¶196-201.

c. **Limitation 11[B]: a bootstrap circuit comprising a bootstrap capacitor, wherein the bootstrap capacitor is charged for providing a bootstrap voltage signal for the high side switch; and**

234. Limitation 11[B] recites a bootstrap circuit comprising a bootstrap capacitor that provides a bootstrap voltage signal to the high side switch. Wong discloses such a bootstrap circuit for charging the bootstrap capacitor. *See* ¶¶215-220.

- d. Limitation 11[C]: a bootstrap refresh control circuit comprising: a bootstrap refresh module, wherein the bootstrap refresh module comprises a first comparing module having a first input terminal, a second input terminal and an output terminal, and wherein the first input terminal of the first comparing module is configured to receive the bootstrap voltage signal, the second input terminal of the first comparing module is configured to receive a bootstrap refresh threshold, and the first comparing module is configured to compare the bootstrap voltage signal with the bootstrap refresh threshold to provide a first comparing signal having a first logic state and a second logic state at the output terminal, and wherein the first comparing signal has the first logic state when the bootstrap voltage signal is lower than the bootstrap refresh threshold, and the first comparing signal has the second logic state when the bootstrap voltage signal is larger than the bootstrap refresh threshold; and

235. Limitation 11[C] recites a bootstrap refresh control circuit comprising a bootstrap refresh module having inputs and outputs sufficient to compare the bootstrap voltage signal with a bootstrap refresh threshold to generate a first comparing signal having one of two logic states. Wong discloses a bootstrap refresh control circuit as recited in limitation 1[C]. See ¶¶202-206.

- e. **Limitation 11[D]: a voltage difference module having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal of the voltage difference module is configured to receive a feedback signal representing the output voltage of the voltage converter, the second input terminal of the voltage difference module is configured to receive a reference voltage signal representing a desired value of the output voltage of the voltage converter, the voltage difference module is configured to compare the feedback signal with the reference voltage signal so as to provide a difference signal at the output terminal; and wherein**

236. Limitation 11[D] recites a voltage difference module having inputs and outputs sufficient to compare a feedback signal representing the output voltage of the voltage converter with a reference voltage signal representing a desired value of the output voltage to generate a difference signal. Wong discloses a voltage difference module as recited in limitation 1[B]. See ¶¶206-210.

- f. **Limitation 11[E]: when the first comparing signal has the first logic state, the bootstrap refresh module is configured to decrease the output voltage of the voltage converter; and**

237. Limitation 11[E] recites that the bootstrap refresh module is configured to decrease the output voltage of the voltage converter when the first comparing signal has a first logic state (i.e., when the bootstrap voltage signal is lower than the bootstrap refresh threshold). Wong teaches limitation 11[E]. See ¶¶211-214.

- g. Limitation 11[F]: wherein when the feedback signal is smaller than the reference voltage signal, the bootstrap refresh control circuit is configured to control the high side switch and the low side switch to switch on and off based on the difference signal so as to charge the bootstrap capacitor for refreshing the bootstrap voltage signal.

238. Limitation 11[F] recites that the bootstrap refresh control circuit is configured to control the high side and low side switches based on the difference signal generated by the voltage difference module when the feedback signal is smaller than the reference voltage signal. Wong teaches limitation 11[F]. See ¶¶215-220.

#### 4. Claim 12

239. Claim 12 is a method claim reciting a method of use for a voltage converter. Wong renders obvious each step of claim 12.

- a. Limitation 12[PRE]: A bootstrap refresh control method for a voltage converter, wherein the voltage converter comprises a high side switch, a low side switch and a bootstrap capacitor for providing a bootstrap voltage signal to supply a high side driver of the high side switch, and wherein the voltage converter is configured to receive an input voltage and to provide an output voltage based on driving the high side switch and the low side switch to switch on and off, and wherein the bootstrap refresh control method comprising:

240. Limitation 12[PRE] recites the structural requirements of a voltage converter for use in the recited method in claim 12. Wong discloses a voltage converter as recited in limitation 12[PRE]. *See* ¶¶196-201.

b. **Limitation 12[A]: sensing the bootstrap voltage signal of the voltage converter;**

241. Limitation 12[A] recites sensing a bootstrap voltage signal. Wong discloses this method step. *See* EX1007 at 4:67-5:3, Fig. 6. *See* ¶¶202-206.

c. **Limitation 12[B]: comparing the bootstrap voltage with a bootstrap refresh threshold to provide a first comparing signal, wherein the first comparing signal has a first logic state and a second logic state, and wherein the first comparing signal has the first logic state when the bootstrap voltage is lower than the bootstrap refresh threshold, and wherein the first comparing signal has the second logic state when the bootstrap voltage signal is larger than the bootstrap refresh threshold;**

242. Limitation 12[B] recites comparing the bootstrap voltage with a bootstrap refresh threshold to provide a first comparing signal having one of two logic states. Wong discloses this method step, including the recited logic states. *See* ¶¶202-206.

d. **Limitation 12[C]: determining whether the bootstrap voltage signal is smaller than the bootstrap refresh threshold or not; and**

243. Limitation 12[C] recites determining whether the voltage signal is smaller than the bootstrap refresh threshold. Wong discloses this method step. *See*

EX1007 at 5:3-6, Fig. 6; *See* ¶¶211-214. A POSITA would understand that the method disclosed in Wong necessarily requires the determination of whether the bootstrap voltage signal is smaller than the bootstrap refresh threshold.

- e. **Limitation 12[D]: decreasing the output voltage of the voltage converter by a bootstrap refresh circuit once the bootstrap voltage signal is determined to have dropped to be smaller than the bootstrap refresh threshold; and**

244. Limitation 12[D] recites decreasing the output voltage when the bootstrap voltage signal is determined to be lower than the bootstrap refresh threshold. Wong teaches this limitation. *See* EX1007, 4:30-38, 4:66-5:13; *See* ¶¶211-214.

- f. **Limitation 12[E]: wherein when the output voltage of the voltage converter is decreased, switching the high side switch and the low side switch on and off so as to refresh the bootstrap voltage signal.**

245. Limitation 12[E] recites switching the high side and low side switches to increase the bootstrap voltage (i.e., to charge the bootstrap capacitor). Wong teaches this limitation. *See* ¶¶215-220.

## 5. **Claim 15**

246. Claim 15 depends from claim 12. Wong teaches claim 12. *supra* ¶¶240-245.

- a. **Limitation 15[A]: The bootstrap refresh control method of claim 12, wherein decreasing the output voltage of the voltage converter by a bootstrap refresh circuit comprising: providing a Constant On Time control signal to set a constant on time for the low side switch, wherein the Constant On Time control signal has a first logic state and a second logic state, and wherein the Constant On Time control signal has the first logic state during the constant on time, and wherein the Constant On Time control signal has the second logic state beyond the constant on time;**

247. Limitation 15[A] recites providing a Constant On Time (COT) control signal having the features recited in limitation 6[A]. Wong teaches limitation 6[A].  
*See ¶¶222.*

- b. **Limitation 15[B]: providing a bootstrap refresh signal based on the first comparing signal and the constant on time control signal, wherein the bootstrap refresh signal has a first logic state and a second logic state, and wherein the bootstrap refresh signal has the first logic state when the first comparing signal has the first logic state, and wherein the bootstrap refresh signal has the second logic state when the Constant On Time control signal has the second logic state; and**

248. Limitation 15[B] recites providing a bootstrap refresh signal having the features recited in limitations 6[B] and 6[C]. Wong teaches limitations 6[B] and 6[C]. *See ¶¶223-229.*

- c. **Limitation 15[C]: switching the low side switch on and off based on the bootstrap refresh signal so as to decrease the output voltage; and wherein the low side switch is switched on in response to the first logic state of the bootstrap refresh signal; and wherein the low side switch is switched off in response to the second logic state of the bootstrap refresh signal.**

249. Limitation 15[C] recites switching the low side switch on and off based on the bootstrap refresh signal according to the logic recited in limitation 6[C]. Wong teaches limitation 6[C]. *See* ¶¶228-229.

E. **Ground 5: Claims 6 and 15 are rendered obvious by Galinski or, in the alternative, by Galinski in view of Wong**

1. **Reasons to combine**

250. A POSITA would have been motivated to combine Galinski and Wong to arrive at the features of claims 6 and 15 for the reasons presented below.

a. **Analogous Art**

251. Galinski and Wong are each in the same field of endeavor and therefore analogous art to the '608 Patent, namely methods of recharging a bootstrap capacitor in power converters. EX1005 at 2:12, 2:44-48; EX1007 at 1:9-13, 38-42. Galinski and Wong are also each reasonably pertinent to a problem the inventors of the '608 Patent attempted to solve, generating a reset pulse of a short duration, but sufficient to allow capacitor  $C_{BST}$  to be recharged. EX1001, 14:38-48; EX1005, 9:5-14; EX1007 at 5:30-36.

**b. Motivation to Combine**

252. Galinski discloses a bootstrap voltage control circuit 110 that includes a comparator 112 that compares the bootstrap voltage to a threshold. In response to the bootstrap voltage falling below the threshold, the bootstrap voltage control circuit 110 is configured to generate a pulse to switch on the low-side switch for a duration sufficient to allow capacitor  $C_{BST}$  to be recharged. EX1005, 9:32-42.

253. However, Galinski explains that the N-channel buck regulator of Fig. 2 is simplified and only those circuit elements that are relevant and related to the claimed invention are included in Fig. 2. EX1005, 5:7-15. That is, other circuit elements, not disclosed in Fig. 2, are necessary for completing the switching regulator. *Id.* For example, Fig. 2 illustrates a set-reset latch 114, without expressly showing an input to the set terminal of the SR latch. A POSITA would understand that a complete switching regulator circuit according to the teaching of Galinski would have at least an additional signal at the set terminal to terminate the refresh cycle.

254. Wong discloses a load control circuit 30 that includes a BS voltage detector 21 that compares the voltage detected across the bootstrap capacitor 7 with a predetermined voltage  $V_{BS}$  to turn on the secondary transistor 25 during the off-time of the main power transistor 3. EX1007 at 4:66-5:9. The on-time of the

secondary transistor 25 is determined by an on-time control 23 of the load control circuit 30. *Id.* at 5:23-55.

255. Thus, both Wong's load control circuit 30 and Galinski's bootstrap voltage control circuit 110 include logic modules for providing a constant on time signal for turning on the low-side switch. A POSITA seeking to implement the functionality of Galinski's (incomplete) bootstrap voltage control circuit 110 would understand that using Wong's disclosed load control circuit 30 would achieve the desired result.

**c. Reasonable Expectation of Success**

256. The references include similar arrangements of well-understood components, and use predictable technology in routine and conventional ways. Wong offers different circuits to achieve the same goal as Galinski, that is, generating a reset pulse of a short duration, but sufficient to allow capacitor  $C_{BST}$  to be recharged. A POSITA would find it straightforward to adapt the ideas presented in Wong to Galinski's DC-DC converter with predictable results.

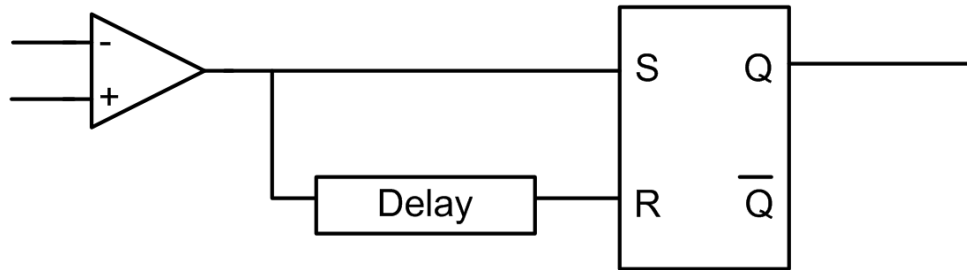
**2. Claim 6**

257. Claim 6 depends from claim 1. Galinski discloses every element of claim 1. *See* ¶¶149-163. As explained in the following subsections, Galinski renders the limitations of claim 6 obvious to a POSITA. To any extent that

Galinski may not fully teach the limitations of claim 6, Wong also teaches these limitations. See ¶¶222-230.

- a. **Limitation 6[A]: The bootstrap refresh control circuit of claim 1, wherein the bootstrap refresh module further comprises: a Constant On Time circuit configured to provide a COT control signal having a first logic state and a second logic state so as to set a constant on time for the low side switch, wherein the COT control signal has the first logic state during the constant on time, and wherein the COT control signal has the second logic state beyond the constant on time; and**

258. Galinski discloses a bootstrap voltage control circuit 110 configured to generate a pulse to switch on the low-side switch for a duration sufficient to allow capacitor  $C_{BST}$  to be recharged. EX1005, 9:32-42, Fig. 2. While Galinski does not disclose the details of the one-shot comparator, 112, a POSITA would understand the one-shot comparator circuit to be a comparator followed by a one-shot circuit. Moreover, a POSITA would understand that one of the most basic circuits for implementing a one shot would comprise an SR flip flop (SRFF) and a delay element as shown below. See ¶¶57-62.

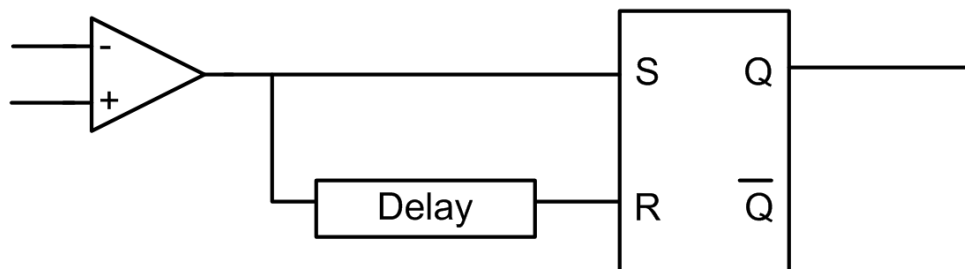


259. When the comparator output is low (for as long as the Delay time), the logic state of the comparator and Delay output are the same. When the comparator logic state goes high, the Delay logic state remains low for the period of the Delay time. A logic high at the S input of the SRFF causes the Q output to go high. After a delay time has passed, the output of the Delay block follows the logic state of its input (the output of the comparator) and goes high which, in turn, drives R high resetting the Q output of the SRFF to a logic low state. The output of the Delay block is the constant on time signal as understood by a POSITA.

260. Thus, Galinski teaches limitation 6[A].

- b. Limitation 6[B]: a first logic module having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal of the first logic module is configured to receive the first comparing signal, the second input terminal of the first logic module is configured to receive the COT control signal, and the first logic module is configured to conduct a logic operation to the first comparing signal and the COT control signal for providing a bootstrap refresh signal having a first logic state and a second logic state at the output terminal; and

261. As noted above, Galinski does not disclose the details of the one-shot comparator, but a POSITA would understand that it could be implemented as shown below. The SRFF is a logic module with two inputs. One of the inputs receives a comparing signal from a comparator. When the comparing signal goes high, the Q output of the logic block (SRFF) goes high and remains high until a signal at the R input goes high, thus resetting the Q output. The second input, to the logic module (R) is the output of the Delay block whose time delay determines how long the Q output remains high before being reset low.



262. A POSITA would understand the comparator generates the comparing signal and the Delay block generates the constant on time signal resulting in the Q output of the SRFF logic block having two states, the first state being established by the comparing signal going high, and the second state being established when the Delay output (constant on time signal) goes high resetting the Q output of the SRFF.

263. Thus, Galinski renders obvious, to a POSITA, the concept of a logic module configured to receive (i) the comparing signal of limitation 1[A] and (ii) a COT control signal and renders obvious the concept of performing logic on these input signals to provide a bootstrap refresh signal at the output terminal. Thus, Galinski teaches limitation 6[B].

- c. **Limitation 6[C]: wherein the bootstrap refresh signal has the first logic state when the first comparing signal has a first logic state so as to turn the low side switch on, and the bootstrap refresh signal has a second logic state when the COT control signal has a second logic state so as to turn the low side switch off.**

264. As explained above [6B], when the comparator output goes high, the Q output of the SRFF goes high and remains high until the comparator output signal propagates through the Delay block resetting the Q output low. A POSITA would understand the Q output is the output of the comparator 12,  $V_{RST}$ .

265. Galinski teaches that the reset pulse,  $V_{RST}$ , causes the high side switch to turn off and the low side switch to turn on, and the bootstrap voltage is refreshed. EX1005, 9:1-21. Furthermore, a POSITA would understand that a drive control signal that causes a driver circuit to turn the low-side power switch on or off has two logic states.

266. Thus, Galinski teaches 6[C].

### 3. Claim 15

267. Claim 15 depends from claim 12. Galinski discloses every limitation of claim 12. *See* ¶¶174-184. Claim 15 recites elements that are substantially similar to claim 6. As discussed with respect to claim 6, either Galinski or Galinski in view of Wong render these limitations obvious to a POSITA. *See* ¶¶221-230, 257-266.

- a. **Limitation 15[A]: The bootstrap refresh control method of claim 12, wherein decreasing the output voltage of the voltage converter by a bootstrap refresh circuit comprising: providing a Constant On Time control signal to set a constant on time for the low side switch, wherein the Constant On Time control signal has a first logic state and a second logic state, and wherein the Constant On Time control signal has the first logic state during the constant on time, and wherein the Constant On Time control signal has the second logic state beyond the constant on time;**

268. Limitation 15[A] recites providing a Constant On Time (COT) control signal having the features recited in limitation 6[A]. Galinski teaches limitation 15[A]. *See* ¶¶258-260.

- b. **Limitation 15[B]: providing a bootstrap refresh signal based on the first comparing signal and the constant on time control signal, wherein the bootstrap refresh signal has a first logic state and a second logic state, and wherein the bootstrap refresh signal has the first logic state when the first comparing signal has the first logic state, and wherein the bootstrap refresh signal has the second logic state when the Constant On Time control signal has the second logic state; and**

269. Limitation 15[B] recites providing a bootstrap refresh signal having the features recited in limitations 6[B] and 6[C]. Galinski teaches limitations 15[B] and 6[C]. See ¶¶261-266.

- c. **Limitation 15[C]: switching the low side switch on and off based on the bootstrap refresh signal so as to decrease the output voltage; and wherein the low side switch is switched on in response to the first logic state of the bootstrap refresh signal; and wherein the low side switch is switched off in response to the second logic state of the bootstrap refresh signal.**

270. Limitation 15[C] recites switching the low side switch on and off based on the bootstrap refresh signal according to the logic recited in limitation 6[C]. Galinski teaches limitation 15[C]. See ¶¶264-266.

## **VII. CONCLUDING STATEMENT**

271. Under penalty of perjury, all statements made herein of my own knowledge are true, and I believe that all statements made herein on information and belief to be true. I have been warned and I am aware that willful false statements are punishable by fine or imprisonment or both under Section 1001 of

Title 18 of the United States Code. In signing this Declaration, I understand that the Declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I acknowledge that I may be subject to cross-examination in the case and that cross-examination will take place in the United States. If cross examination is required of me, I undertake to appear within the United States during the time allotted for cross-examination, and within the limits of my ability so to do. I declare under penalty of perjury that the foregoing is true and correct.

Executed on 16 May 2024

A handwritten signature in cursive script, reading "Douglas Holberg", written over a horizontal line.

Douglas Holberg

## Appendix A

### SPICE Simulation Netlist

```
* C:\Users\doug\Desktop\FoxRothschild-Reed Semiconductor\9,590,608\Petition
and Declaration\pulse test3.asc
L1 SW VOUT 50µH
C1 VOUT 0 100µF
VIN N001 0 50
R2 VOUT 0 100
M1 N001 DH SW SW IRFH5207
V2 DH 0 PULSE(0 55 0 .1u .1u 10u 50u 1000)
V3 DL 0 PULSE(55 0 0 .1u .1u 10u 50u 1000)
M2 SW DL 0 0 IRFH5207
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.model PMOS PMOS
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.tran 50m
* V2
* V3
.backanno
.end
```

