

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

REED SEMICONDUCTOR CORP.,

Petitioner

v.

MONOLITHIC POWER SYSTEMS, INC.

Patent Owner

IPR2024-00871
Patent No. 9,590,608

**PETITION FOR *INTER PARTES* REVIEW
UNDER 35 U.S.C. § 312 AND 37 C.F.R. § 42.104**

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Petitioner's Exhibit List¹

Exhibit No.	Description
1001	U.S. Patent No. 9,590,608 B2 to Xu
1002	Prosecution History of U.S. 9,590,608
1003	Declaration of Doug Holberg
1004	<i>Curriculum Vitae</i> of Doug Holberg
1005	U.S. Patent No. 7,145,316 B1 to Galinski
1006	Texas Instruments TPS54620 4.5V to 17V Input, 6A Synchronous Step Down SWIFT™ Converter Data Sheet (Revised May 2011)
1007	U.S. Patent No. 7,321,258 B2 to Wong
1008	Chinese Patent Application Publication No. CN 102832810 A to Li
1009	U.S. Patent No. 7,026,801 B2 to Fowler
1010	U.S. Patent Application Publication No. 2015/0214839 A1 to Shiu
1011	Certified English Translation of Exhibit 1008 - Chinese Patent Application Publication No. CN 102832810 A to Li
1012	Translator Certification Regarding Exhibit 1011
1013	U.S. Patent Application Publication 2007/0024261 A1 to Wong
1014	U.S. Patent Application Publication 2005/0057239 A1 to Fowler
1015	U.S. Patent No. 7,746,616 B2 to Arndt

¹ Petitioner cites to exhibits' original page numbers. Unless otherwise noted, all emphasis in any quoted material has been added.

Exhibit No.	Description
1016	U.S. Patent Application Publication No. 2007/0076342 A1 to Arndt
1017	U.S. Patent Application Publication No. 2015/0061611 A1 to Li
1018	Declaration of Maureen M. Honeycutt
1019	Texas Instruments TPS54620 4.5V to 17V Input, 6A Synchronous Step Down SWIFT™ Converter Data Sheet (Revised May 2009)
1020	Texas Instruments TPS54620 4.5V to 17V Input, 6A Synchronous Step Down SWIFT™ Converter Data Sheet (Revised January 2010)
1021	Texas Instruments TPS54620 4.5V to 17V Input, 6A Synchronous Step Down SWIFT™ Converter Data Sheet (Revised October 2010)
1022	Texas Instruments TPS54560 4.5V to 60 V input, 5 A step-down converter with Eco-Mode™ Data Sheet (Revised March 2013)
1023	Texas Instruments TPS54560 4.5V to 60 V input, 5 A step-down converter with Eco-Mode™ Data Sheet (Revised March 2014)
1024	CMOS Analog Circuit Design, Third Edition, Allen et al.
1025	U.S. Patent Application Publication No. 2003/0155894 to Dubhashi et al. (“Dubhashi”)
1026	U.S. Patent No. 5,097,196 to Schoneman (“Schoneman”)
1027	U.S. Patent No. 5,770,940 to Goder (“Goder”)
1028	Wait, John V, Huelsman, Lawrence P, Korn, Granino. “Introduction to Operational Amplifiers Theory and Applications” (“Wait”)

Exhibit No.	Description
1029	Assignment of U.S. Patent No. 9,590,608 from Chengdu Monolithic Power Systems Co., Ltd. to Monolithic Power Systems, Inc.
1030	Redacted Exhibit A from Monolithic Power Systems, Inc.'s Initial Infringement Contentions
1031	Reed Stipulation Regarding Invalidity Contentions (<i>Sotera</i> Stipulation)
1032	Nengda Stipulation Regarding Invalidity Contentions (<i>Sotera</i> Stipulation)
1033	Texas Instruments TLC551, TLC551Y LinCMOSE™ TIMERS Data Sheet (Revised September 1997)

Claim Appendix

Claim Limitation	Claim Language
1[PRE]	1. A bootstrap refresh control circuit for a voltage converter, wherein the voltage converter comprises a high side switch, a low side switch and a bootstrap capacitor for providing a bootstrap voltage signal to supply a high side driver of the high side switch, and wherein the voltage converter is configured to receive an input voltage at an input terminal and to provide an output voltage at an output terminal based on driving the high side switch and the low side switch to switch on and off, and
1[A]	wherein the bootstrap refresh control circuit comprising: a bootstrap refresh module, wherein the bootstrap refresh module comprises a first comparing module having a first input terminal, a second input terminal and an output terminal, and wherein the first input terminal of the first comparing module is configured to receive the bootstrap voltage signal, the second input terminal of the first comparing module is configured to receive a bootstrap refresh threshold, and the first comparing module is configured to compare the bootstrap voltage signal with the bootstrap refresh threshold to provide a first comparing signal having a first logic state and a second logic state at the output terminal, and wherein the first comparing signal has the first logic state when the bootstrap voltage signal is lower than the bootstrap refresh threshold, and wherein the first comparing signal has the second logic state when the bootstrap voltage signal is larger than the bootstrap refresh threshold; and
1[B]	a voltage difference module having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal of the voltage difference module is configured to receive a feedback signal representing the output voltage of the voltage converter, the second input terminal of the voltage difference module is configured to receive a reference voltage signal representing a desired value of the output voltage of the voltage converter, the voltage difference module is configured to compare

	the feedback signal with the reference voltage signal so as to provide a difference signal at the output terminal; and
1[C]	wherein when the first comparing signal has the first logic state, the bootstrap refresh module is configured to decrease the output voltage of the voltage converter; and
1[D]	wherein when the feedback signal is smaller than the reference voltage signal, the bootstrap refresh control circuit is configured to control the high side switch and the low side switch to switch on and off based on the difference signal so as to charge the bootstrap capacitor for refreshing the bootstrap voltage signal.
2[A]	2. The bootstrap refresh control circuit of claim 1, wherein the bootstrap refresh threshold comprises a first threshold and a second threshold, wherein the first threshold is higher than a ground potential and lower than the second threshold; and wherein
2[B]	the first comparing signal has the first logic state when the bootstrap voltage signal is lower than the first threshold, and wherein the first comparing signal has the second logic state when the bootstrap voltage signal is larger than the second threshold.
6[A]	6. The bootstrap refresh control circuit of claim 1, wherein the bootstrap refresh module further comprises: a Constant On Time circuit configured to provide a COT control signal having a first logic state and a second logic state so as to set a constant on time for the low side switch, wherein the COT control signal has the first logic state during the constant on time, and wherein the COT control signal has the second logic state beyond the constant on time; and
6[B]	a first logic module having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal of the first logic module is configured to receive the first comparing

	signal, the second input terminal of the first logic module is configured to receive the COT control signal, and the first logic module is configured to conduct a logic operation to the first comparing signal and the COT control signal for providing a bootstrap refresh signal having a first logic state and a second logic state at the output terminal; and
6[C]	wherein the bootstrap refresh signal has the first logic state when the first comparing signal has a first logic state so as to turn the low side switch on, and the bootstrap refresh signal has a second logic state when the COT control signal has a second logic state so as to turn the low side switch off.
11[PRE]	11. A voltage converter, comprising:
11[A]	a switching circuit having a high side switch and a low side switch, wherein the switching circuit is configured to receive an input voltage, and further configured to provide an output voltage based on switching the high side switch and the low side switch on and off;
11[B]	a bootstrap circuit comprising a bootstrap capacitor, wherein the bootstrap capacitor is charged for providing a bootstrap voltage signal for the high side switch; and
11[C]	a bootstrap refresh control circuit comprising: a bootstrap refresh module, wherein the bootstrap refresh module comprises a first comparing module having a first input terminal, a second input terminal and an output terminal, and wherein the first input terminal of the first comparing module is configured to receive the bootstrap voltage signal, the second input terminal of the first comparing module is configured to receive a bootstrap refresh threshold, and the first comparing module is configured to compare the bootstrap voltage signal with the bootstrap refresh threshold to provide a first comparing signal having a first logic state and a second logic state at the output terminal, and wherein the first comparing signal has the first logic state when the bootstrap voltage

	signal is lower than the bootstrap refresh threshold, and the first comparing signal has the second logic state when the bootstrap voltage signal is larger than the bootstrap refresh threshold; and
11[D]	a voltage difference module having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal of the voltage difference module is configured to receive a feedback signal representing the output voltage of the voltage converter, the second input terminal of the voltage difference module is configured to receive a reference voltage signal representing a desired value of the output voltage of the voltage converter, the voltage difference module is configured to compare the feedback signal with the reference voltage signal so as to provide a difference signal at the output terminal; and wherein
11[E]	when the first comparing signal has the first logic state, the bootstrap refresh module is configured to decrease the output voltage of the voltage converter; and
11[F]	wherein when the feedback signal is smaller than the reference voltage signal, the bootstrap refresh control circuit is configured to control the high side switch and the low side switch to switch on and off based on the difference signal so as to charge the bootstrap capacitor for refreshing the bootstrap voltage signal.
12[PRE]	12. A bootstrap refresh control method for a voltage converter, wherein the voltage converter comprises a high side switch, a low side switch and a bootstrap capacitor for providing a bootstrap voltage signal to supply a high side driver of the high side switch, and wherein the voltage converter is configured to receive an input voltage and to provide an output voltage based on driving the high side switch and the low side switch to switch on and off, and wherein the bootstrap refresh control method comprising:
12[A]	sensing the bootstrap voltage signal of the voltage converter;

12[B]	comparing the bootstrap voltage with a bootstrap refresh threshold to provide a first comparing signal, wherein the first comparing signal has a first logic state and a second logic state, and wherein the first comparing signal has the first logic state when the bootstrap voltage is lower than the bootstrap refresh threshold, and wherein the first comparing signal has the second logic state when the bootstrap voltage signal is larger than the bootstrap refresh threshold;
12[C]	determining whether the bootstrap voltage signal is smaller than the bootstrap refresh threshold or not; and
12[D]	decreasing the output voltage of the voltage converter by a bootstrap refresh circuit once the bootstrap voltage signal is determined to have dropped to be smaller than the bootstrap refresh threshold; and
12[E]	wherein when the output voltage of the voltage converter is decreased, switching the high side switch and the low side switch on and off so as to refresh the bootstrap voltage signal.
15[A]	15. The bootstrap refresh control method of claim 12, wherein decreasing the output voltage of the voltage converter by a bootstrap refresh circuit comprising: providing a Constant On Time control signal to set a constant on time for the low side switch, wherein the Constant On Time control signal has a first logic state and a second logic state, and wherein the Constant On Time control signal has the first logic state during the constant on time, and wherein the Constant On Time control signal has the second logic state beyond the constant on time;
15[B]	providing a bootstrap refresh signal based on the first comparing signal and the constant on time control signal, wherein the bootstrap refresh signal has a first logic state and a second logic state, and wherein the bootstrap refresh signal has the first logic state when the first comparing signal has the first logic state, and wherein the

	bootstrap refresh signal has the second logic state when the Constant On Time control signal has the second logic state; and
15[C]	switching the low side switch on and off based on the bootstrap refresh signal so as to decrease the output voltage; and wherein the low side switch is switched on in response to the first logic state of the bootstrap refresh signal; and wherein the low side switch is switched off in response to the second logic state of the bootstrap refresh signal.
16	16. The bootstrap refresh control circuit [sic] of claim 12, wherein the bootstrap refresh threshold comprises a first threshold and a second threshold, and wherein the first threshold is higher than a ground potential and lower than the second threshold; and wherein the first comparing signal has the first logic state when the bootstrap voltage signal is lower than the first threshold, and wherein the first comparing signal has the second logic state when the bootstrap voltage signal is higher than the second threshold.

I. INTRODUCTION

Pursuant to 35 U.S.C. §§311, 314(a), and 37 C.F.R. §42.100, Reed Semiconductor Corp. (“Petitioner”) respectfully requests that the Board review and cancel claims 1, 2, 6, 11, 12, 15, and 16 (the “Challenged Claims”) of U.S. Patent No. 9,590,608 (“the ’608 Patent”) (EX1001) as unpatentable under 35 U.S.C. §§102 and/or 103.

II. PETITION REQUIREMENTS

A. Grounds For Standing and Timeliness

Petitioner certifies that the ’608 Patent is eligible for IPR and that Petitioner is not barred or estopped from requesting IPR. 37 C.F.R. §42.104(a). The ’608 Patent was filed on August 11, 2015, and issued on March 7, 2017. It is subject to the America Invents Act (“AIA”) as a first-to-file patent and this Petition is filed more than 9 months from the issue date. *See* 37 C.F.R. §42.102(a)(1). This Petition is also filed within one year of Petitioner being served an allegation of infringement of the ’608 Patent. *See* Patent Owner Mandatory Notices, *infra*.

B. Payment of Fees

Pursuant to 37 C.F.R. §§42.103(a) and 42.15(a), the required fees are submitted herewith. If additional fees are due during this proceeding, the Office is authorized to charge Deposit Account 50-1943.

C. Identification of Challenge and Relief Requested²

Pursuant to 37 C.F.R. §§ 42.22(a) and 42.104(b), Petitioner requests a final written decision that the Challenged Claims are unpatentable in view of the analysis below. *See* §VII, *infra* (incorporated here). The effective filing date of the '608 Patent is, for purposes of this Petition only, assumed to be August 11, 2014 (the “Effective Filing Date”). *See* §III, *infra* (incorporated here). The following is a list of prior art that anticipate and/or render obvious the Challenged Claims.

Exhibit	Description	Operative Date
1005	U.S. Patent No. 7,145,316 (“Galinski”)	December 5, 2006
1006	Texas Instruments TPS54620 4.5V to 17V Input, 6A Synchronous Step Down SWIFT™ Converter Data Sheet (“TI”)	May 2011 ³
1007	U.S. Patent No. 7,321,258 (“Wong”)	January 22, 2008

² For each combination, Petitioner relies on the teachings, and not on a physical incorporation of elements. *See In re Mouttet*, 686 F.3d 1322, 1332 (Fed. Cir. 2012); *In re Etter*, 756 F.2d 852, 859 (Fed. Cir. 1985).

³ TI is a printed publication. *See* EX1018, ¶¶1-31, in particular ¶¶22-24, referencing EX1006; §VI.B, *infra* (incorporated here)

1008, 1011 ⁴	Chinese Patent Application Publication CN 102832810 (“Li”)	December 19, 2012
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Galinski, TI, Wong, and Li are all prior art under §102(a)(1) because each was published prior to the Effective Filing Date. Furthermore, all references were published more than one year before the effective filing date of the claimed invention. Thus, the exceptions of §102(b)(1) do not apply.

Petitioner requests cancellation of the Challenged Claims on the following grounds:

Ground	Claims	Description
1	1, 11, 12	Anticipated and/or obvious under §102/103 by TI.
2	1, 11, 12	Anticipated under §102 by Galinski.
3	1, 2, 11, 12, 16	Obvious under §103 by Galinski in view of Li.
4	1, 6, 11, 12, 15	Obvious under §103 by Wong.
5	6, 15	Obvious under §103 by Galinski or, in the alternative, Galinski in view of Wong.

⁴ EX1008 is the original Chinese language publication for the Li reference. EX1011 is the certified English translation thereof. *See* EX1012. Petitioner’s citations to this reference herein will be to the English translation.

III. SUMMARY OF THE '608 PATENT

The '608 Patent issued on March 7, 2017 from Patent Application Serial No. 14/823,900 (EX1002 at 13-59) (“the '900 Appl.”), filed on August 11, 2015 by Chengdu Monolithic Power Systems Co., Ltd. The '608 Patent claims priority to Chinese Patent Application No. 201410390708, filed on August 11, 2014. For purposes of this proceeding and without conceding the issue, Petitioner assumes all Challenged Claims of the '608 Patent have a priority date of August 11, 2014, and that they were effectively filed as of that date. The '608 Patent was assigned to Patent Owner on October 13, 2023. *See* EX1029.

A. Overview of the '608 Patent

The '608 Patent is directed to switch-mode DC-DC voltage converters having circuitry for refreshing the voltage maintained across a “bootstrap” capacitor. EX1001, 6:21-67, Figs. 2-4; EX1003, ¶79. The “bootstrap” voltage is used to properly operate the high-side switch of the voltage converter. EX1001, 6:67-7:12; EX1003, ¶79.

The '608 Patent explains that when typical step-down power converters operate either (i) with an output voltage close to the input voltage (so that the high-side switch is generally closed and the low-side switch is generally open), or (ii) with very little load (in which case, both switches may be generally open for high

efficiency), the bootstrap voltage may drop over time, resulting in the inability to operate the high-side switch properly (until the bootstrap voltage can be refreshed). EX1001, 3:3-27; EX1003, ¶84.

To detect this situation, a bootstrap refresh module 134 is configured to compare the bootstrap voltage signal (V_{BST}) with a bootstrap refresh threshold (V_{TH1}). EX1001, 8:40-54; EX1003, ¶85. When the bootstrap voltage signal becomes too low, the bootstrap refresh module 134 reduces the output voltage (V_{OUT}) by operating the low-side switch to connect the common connection node (SW) to ground through the low-side switch. EX1001, 11:11-14, 13:9-34, 15:16-24 Fig. 3; EX1003, ¶86. Logic module 30 performs a logic OR of bootstrap refresh module 134 output signal (RFS) and low-side switch control signal (S_{L1}), so that if either RFS or S_{L1} has a logic high state, the low-side switch is turned on. *Id.* Thus RFS effectively overrides S_{L1} , causing the common connection node (SW) to be connected to ground regardless of the state of S_{L1} . *Id.*

B. Prosecution History

During prosecution of Application No. 14/823,900 (which issued as the '608 Patent), the Applicant only submitted a single Information Disclosure Statement. The IDS, submitted on the same date as the filing of the '900 application, only discloses a single reference: U.S. Publication No. 2015/0061611, the publication of

U.S. Application No. 14/015,964 to Li, filed by Patent Owner on August 30, 2013. The '964 application claims priority to counterpart Chinese application CN201210315162.5, which published on December 19, 2012 as the Li reference, and issued as CN102832810 on April 8, 2015.

IV. LEVEL OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art (“POSITA”) in the field of the '608 Patent, as of its earliest possible filing date of August 11, 2014, would have been someone knowledgeable about and familiar with the DC-DC switch-mode power converter technology that is pertinent to the '608 Patent. A POSITA would have had a bachelor’s degree in Electrical Engineering or equivalent training, and approximately two years of experience working in the field of power converters, feedback systems, or related technologies. Lack of work experience can be remedied by additional education, and vice versa. EX1003, ¶¶17-19.

V. CLAIM CONSTRUCTION

Claim terms in IPR are construed according to their “ordinary and customary meaning” to those of skill in the art. 37 C.F.R. § 42.100(b). *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). Petitioner submits that, for the purposes of this proceeding and the grounds presented herein, no claim term requires express construction. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d

1013, 1017 (Fed. Cir. 2017). Petitioner further notes that some claim terms are provided with explicit definitions in the specification. EX1001 at 5:64-6:20.

VI. SUMMARY OF THE PRIOR ART

A. Galinski

Galinski is directed to DC-DC switching voltage converters having a high-side switch and a low-side switch and that require a “bootstrap” voltage to drive the high-side switch. EX1005, 2:12; EX1003, ¶88. Galinski uses bootstrap-voltage monitoring to allow the voltage converter to operate at or near 100% duty cycle. EX1005, 2:44-48; EX1003, ¶88. The disclosed converter alternately operates a pair of power switches (a high-side switch and a low-side switch) to produce a switching voltage (V_{sw}) at a common node which is coupled to a LC network to generate a relatively constant output voltage V_{out} . EX1005, 1:20-36; EX1003, ¶88.

Such voltage converters typically include a feedback control loop formed by dividing down the output voltage V_{out} to provide a feedback voltage (V_{FB}) and feeding back the feedback voltage (V_{FB}) to an error amplifier where the feedback voltage (V_{FB}) is compared to a reference voltage. EX1005, 5:56-61; EX1003, ¶89. The feedback control loop regulates the output voltage V_{out} at a constant level over changing load conditions by varying the duty cycle of the power switches. EX1005, 6:2-5; EX1003, ¶89. That is, the high-side switch and the low-side switch are turned

on alternately to increase or decrease the current through the output inductor.
EX1005, 2:5-8; EX1003, ¶89.

A high-side driver circuit is supplied by the “bootstrap” voltage to drive the high-side switch. EX1005, 6:50-6:52; EX1003, ¶90. A low-side driver may be supplied by a voltage between V_{IN} and ground. EX1005, 6:52-6:54; EX1003, ¶90. The bootstrap voltage may be generated during the switching of the high-side and low-side switches, avoiding the need for a separate higher supply voltage. EX1005, 2:8-13; EX1003, ¶90. An exemplary circuit is shown in Fig. 1 of Galinski, reproduced below.

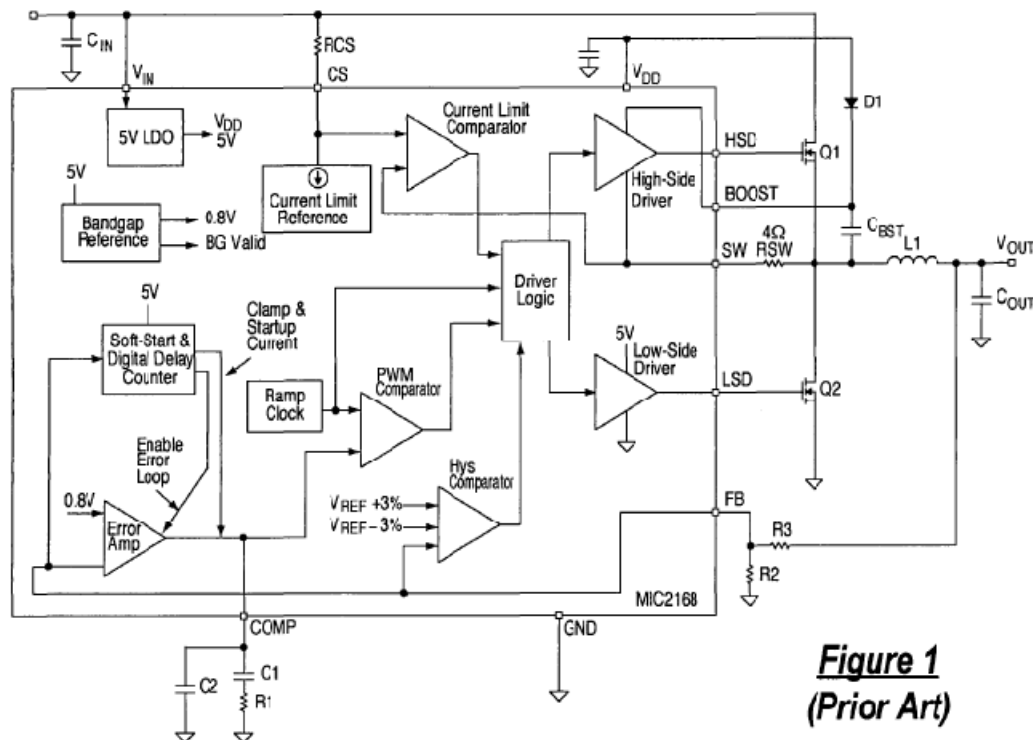
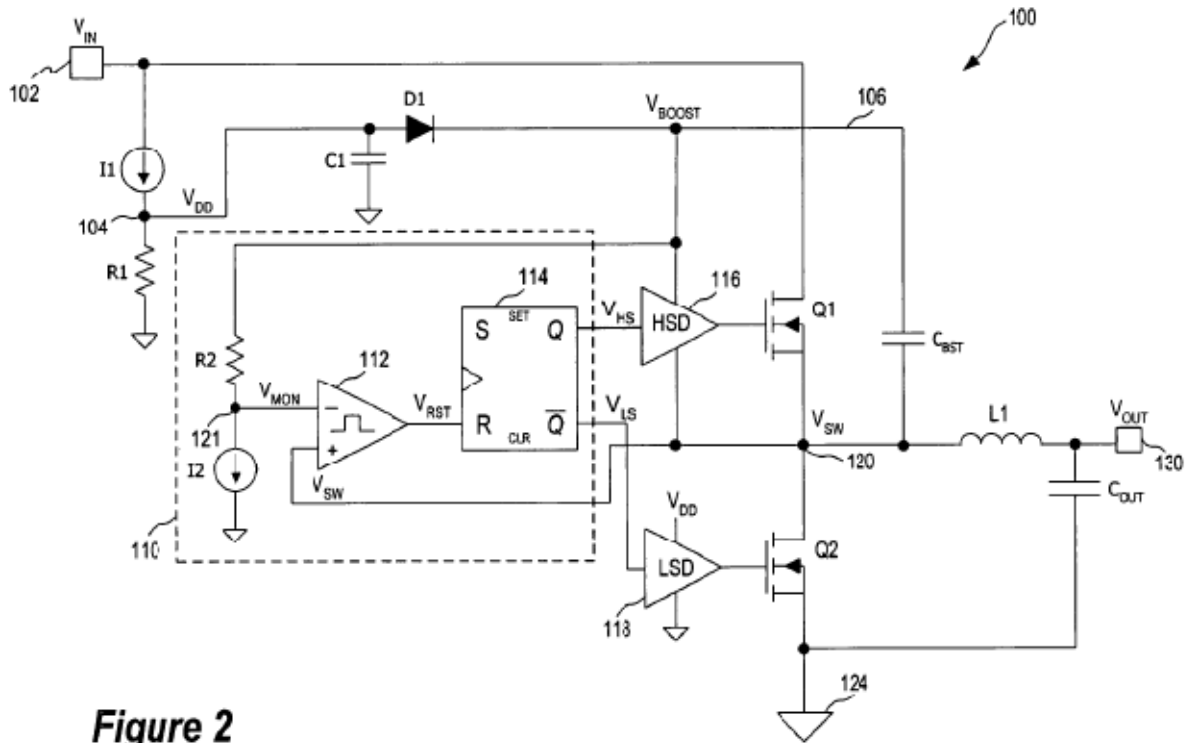


Figure 1
(Prior Art)

The exemplary integrated circuit is coupled to discrete high-side and low-side power switches (Q1, Q2) which are external to the controller circuit. EX1005, 4:57-59; EX1003, ¶91. As shown in Fig. 1, the controller includes the driver circuitry associated with each switch. Each driver circuit receives a logic signal from the driver logic block, and the high-side driver also receives the bootstrap voltage (BOOST). The driver logic block, in turn, receives a control signal from a comparator circuit which receives the feedback signal (V_{FB}) and one or more reference voltages. *Id.* The comparator circuit compares the feedback voltage (V_{FB}) to one or more reference voltages to produce a control signal, which is received by the driver logic block. *Id.* Based on the control signal, the driver logic block alternately operates the power switches to regulate the output voltage (V_{OUT}). *Id.*, ¶91-92.

In some operating conditions, the output voltage (V_{OUT}) may be set very close to the input voltage (V_{IN}). EX1005, 1:56-58; EX1003, ¶94. Under these conditions, the converter may not naturally cause the switches to alternate often enough to maintain the bootstrap voltage. Thus, the bootstrap voltage may decay or decrease over time until it is no longer able to control the high-side switch. EX1005, 2:15-24; EX1003, ¶94. This issue is addressed by incorporating a bootstrap voltage control circuit for monitoring and periodically refreshing the bootstrap voltage. EX1005,

2:44-49; EX1003, ¶94. When the monitored bootstrap voltage decays below a predetermined level, the control circuit causes the converter to operate the switches for a short time to refresh the bootstrap voltage. EX1005, at 4:4-11; EX1003, ¶94. Control signals from the feedback loop described above are logically combined with output signals from the bootstrap voltage control circuit to provide the final control signals for the high-side and low-side driver circuits. EX1005, 6:8-13; EX1003, ¶94. Therefore, the output signals of the bootstrap voltage control circuit serve to modify or override the nominal feedback-control signals. *Id.* FIG. 2 is a circuit diagram of a control circuit for monitoring and maintaining the bootstrap voltage incorporated in an N-channel buck switching voltage regulator and is reproduced below. *Id.*, 5:3-8. As Galinski explains, a POSITA would appreciate that the N-channel buck regulator of Fig. 2 is simplified and only those circuit elements that are relevant and related to the claimed invention are included. EX1005, 5:7-15. Other circuit elements required to complete the switching regulator circuit are shown, e.g., in the exemplary circuit diagram of Fig. 1. *Id.* For example, Fig. 2 illustrates a set-reset latch 114, without expressly showing an input to the set terminal of the SR latch. EX1003, ¶253. A POSITA would understand that a complete switching regulator circuit according to the teaching of Galinski would necessarily have at least an additional signal at the set terminal to terminate the refresh cycle. *Id.*

**Figure 2**

As shown, the bootstrap voltage control circuit includes a comparator and associated elements that act collectively to compare the bootstrap voltage (V_{BOOST}) to a threshold voltage (V_{TH}). EX1005, 8:30-67; EX1003, ¶95. Comparator circuit 112 receives the switching output voltage V_{SW} (node 120) on its non-inverting input terminal and receives a scaled down voltage of bootstrap voltage V_{BOOST} on its inverting terminal. *Id.*, ¶98. The scaling of the bootstrap voltage V_{BOOST} to generate the monitor voltage V_{MON} is selected to establish a minimum bootstrap voltage $V_{\text{BOOST_MIN}}$ greater than a voltage $V_{\text{IN}} + V_{\text{TH_HS}}$, where $V_{\text{TH_HS}}$ is the threshold voltage

of high side switch Q1, so that high-side driver circuit 116 can drive high-side switch Q1 properly. EX1005, 8:64-52; EX1003, ¶98. In the embodiment shown in Fig. 2, the scaling of the bootstrap voltage V_{BOOST} is accomplished by resistor R2 biased by current source I2, although it is possible to use other circuit configurations to realize the voltage feedback and divide function. EX1005, 8:54-67; EX1003, ¶98.

When the bootstrap voltage (V_{BOOST}) is equal to or less than the threshold voltage (V_{TH}), the comparator generates an output pulse (V_{RST}). EX1005, 9:3-5; EX1003, ¶100. In this embodiment, the comparator output (V_{RST}) is a duration sufficient to allow C_{BST} to be recharged. EX1005, 9:5-7; EX1003, ¶100. As in the case of the comparator circuit, the specific logic circuitry for generating the drive control signals for the driver circuits is not critical to the practice of the present invention. EX1005, 9:41-47; EX1003, ¶100. Regardless of the specific logic circuitry, power switches Q1 and Q2 are caused to switch, and the bootstrap voltage V_{BOOST} is thereby refreshed. EX1005, 9:17-21; EX1003, ¶100. During this recharge phase, the switching output voltage V_{SW} switches from input voltage V_{IN} to 0 volt temporarily. EX1005, 10:19-23; EX1003, ¶100. As shown in the timing diagram of FIG. 3 reproduced below, the switching output voltage V_{SW} dips below the ground voltage. EX1005, 10:23-24; EX1003, ¶100.

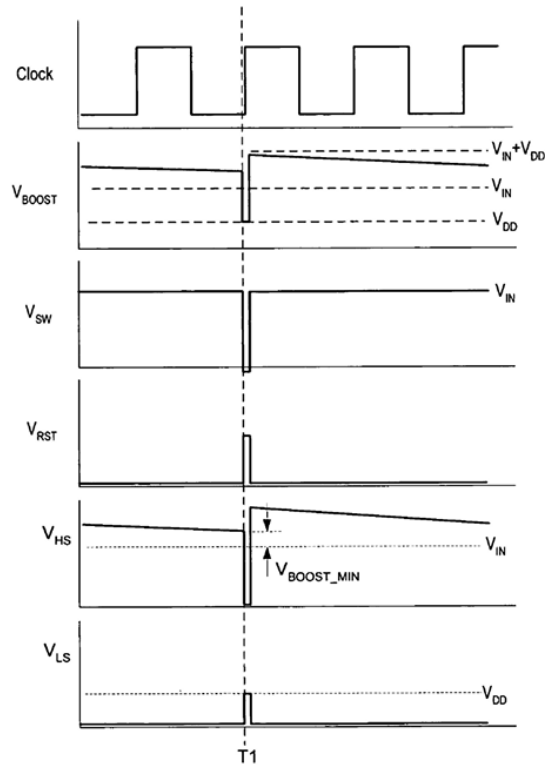


Figure 3

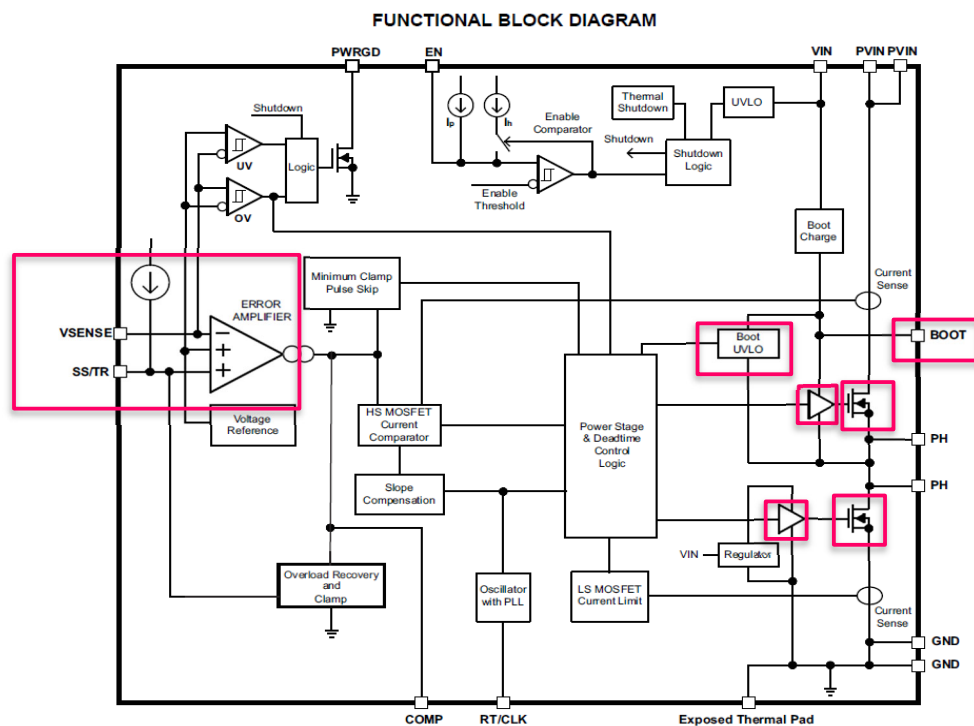
B. TPS54620 Data Sheet (TI)

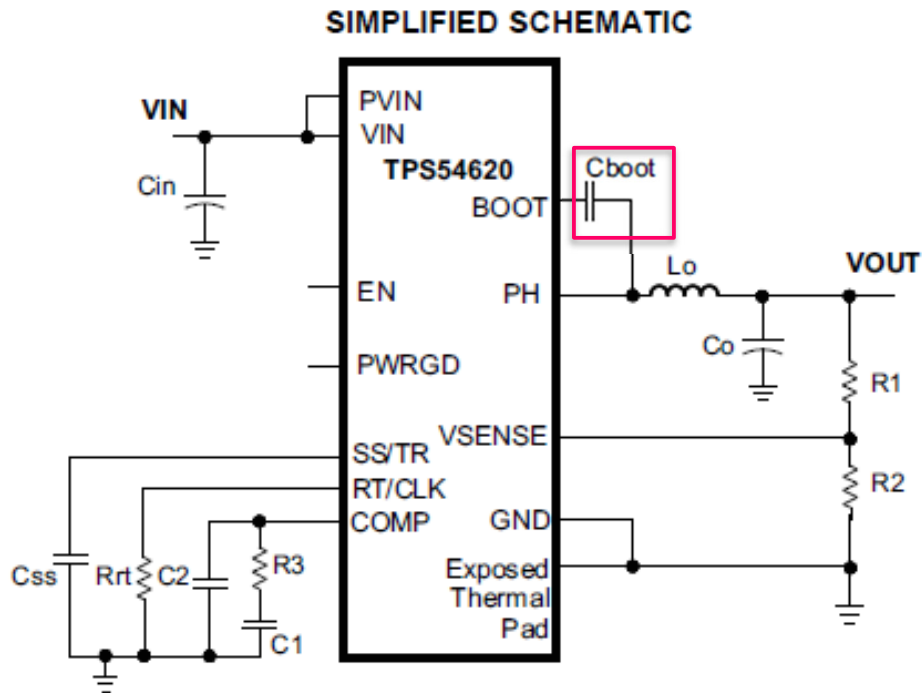
TI was available for free download by any interested POSITA, without restriction, as early as May 4, 2011. *See* EX1018, ¶¶23-24. TI was created by Texas Instruments to allow users to understand how to use component TPS54620 in a larger system. The data sheet summarizes the performance and other characteristics of that component. EX1003, ¶101.

In particular, TI discloses that the TPS54620 is a 4.5-17V input, step-down DC/DC voltage converter having integrated high-side and low-side MOSFETs, for use, e.g., in a point-of-load voltage regulator. EX1006, 1; *see also* EX1003, ¶¶41-

48. The data sheet includes a step-by-step design process for a high frequency switching regulator based on the TPS54620. *Id.*, 21; EX1003, ¶102. A Simplified Schematic circuit including the TPS54620 is included on page 1, and a Functional Block Diagram is included on page 6, both of which are reproduced below. EX1003, ¶102.

As shown in the Functional Block Diagram, the high-side and low-side MOSFETS are controlled by the Power Stage Control Logic (via corresponding driver circuits). The Power Stage Control Logic receives control signals from several sources, including the Boot UVLO monitoring circuit. *Id.*, ¶103.





A bootstrap capacitor is required between the boot pin (BOOT) and the switch node pin (PH). EX1006 at 5. The voltage on the bootstrap capacitor carries the gate drive voltage for the high-side MOSFET. *Id.* The boot capacitor voltage is monitored by a BOOT-PH UVLO circuit allowing PH pin to be pulled low to recharge the boot capacitor. *Id.* at 10; EX1003, ¶102. That is, when the bootstrap voltage drops below a threshold (about 2.1V, depending on temperature), the high-side MOSFET is turned off and the low-side MOSFET is turned on, allowing the boot capacitor to be recharged. EX1006 at 14.

EX1006 further discloses hysteresis monitoring of the input voltage (VIN). EX1006 at 3, 11. That is, EX1006 discloses comparing VIN to a first threshold when

VIN is rising and comparing VIN to a second threshold when VIN is falling. EX1003, ¶110. EX1006 does not expressly disclose hysteresis monitoring of the bootstrap voltage, but that feature was known in the art, e.g., included in similar DC/DC voltage converters that were available prior to the filing date of the '608 patent. *Id.*, see EX1023 at Figure 19.

As shown in the Functional Block Diagram, the BOOT-PH UVLO circuit produces an output which is connected to the Power Stage Logic. The output indicates whether the bootstrap voltage is above or below the bootstrap voltage threshold.

As shown in the simplified schematic, the voltage converter receives an input voltage (on the VIN pin). EX1003, ¶107. A switch node (PH) is connected to the high-side and low-side MOSFETS which alternately switch the switch node (PH) between VIN and ground. *Id.* The switch node (PH) is connected through an output inductor to produce a filtered output voltage (VOUT). *Id.* The converter output voltage (VOUT) level is set by providing a feedback signal based on VOUT (scaled down through a resistor divider) to the VSENSE pin. *Id.* at 11. As shown in the functional block diagram, the VSENSE feedback signal is connected to an error amplifier, which compares VSENSE to a voltage threshold (the lower of the SS/TR pin voltage during a “soft start” or the internal 0.8V voltage reference) and which

produces an output which drives the COMP pin. EX1006 at 10-11. The error amplifier output is also connected to the Power Stage Control Logic which operates the high-side and low-side switches to produce the output voltage (VOUT). EX1003, ¶¶106-107.

Also, TI discloses that the TPS54620 is protected from overcurrent conditions by cycle-by-cycle current limiting both the high-side MOSFET and the low-side MOSFET. EX1006 at 17. A low-side overprotection circuit (LS MOSFET Limit) compares the low-side MOSFET sinking current to a predetermined limit. *Id.* at 18. As shown, the output of the overprotection circuit is received by the Power Stage Logic. If the low-side sinking current limit is exceeded, the low-side MOSFET is turned off immediately. *Id.*

C. Li

Li is directed to DC-DC switch-mode voltage regulators having a high side switch M_{HS} and a low side switch M_{LS} and configured to provide a bootstrap voltage V_{BST} to the control terminal of the high side switch. EX1011, ¶¶2-5. An example circuit (shown in Fig. 2, reproduced below) includes control logic which outputs high-side and low-side control signals to operate the high-side and low-side switches, respectively, via high-side and low-side drivers of a driver module. EX1003, ¶111. The inputs to the control logic also include the output voltage (V_o),

a bootstrap refresh signal (RFS) and an undervoltage lockout signal (LOCK). EX1011, ¶¶32, 36, 40. A POSITA would understand that the purpose of providing the output voltage to the control logic is to allow the control logic to regulate the output voltage to a desired level. EX1003, ¶111. That is, the control logic must compare the output voltage to a desired voltage level and operate the high-side and low-side switches accordingly to achieve the desired level. As described in more

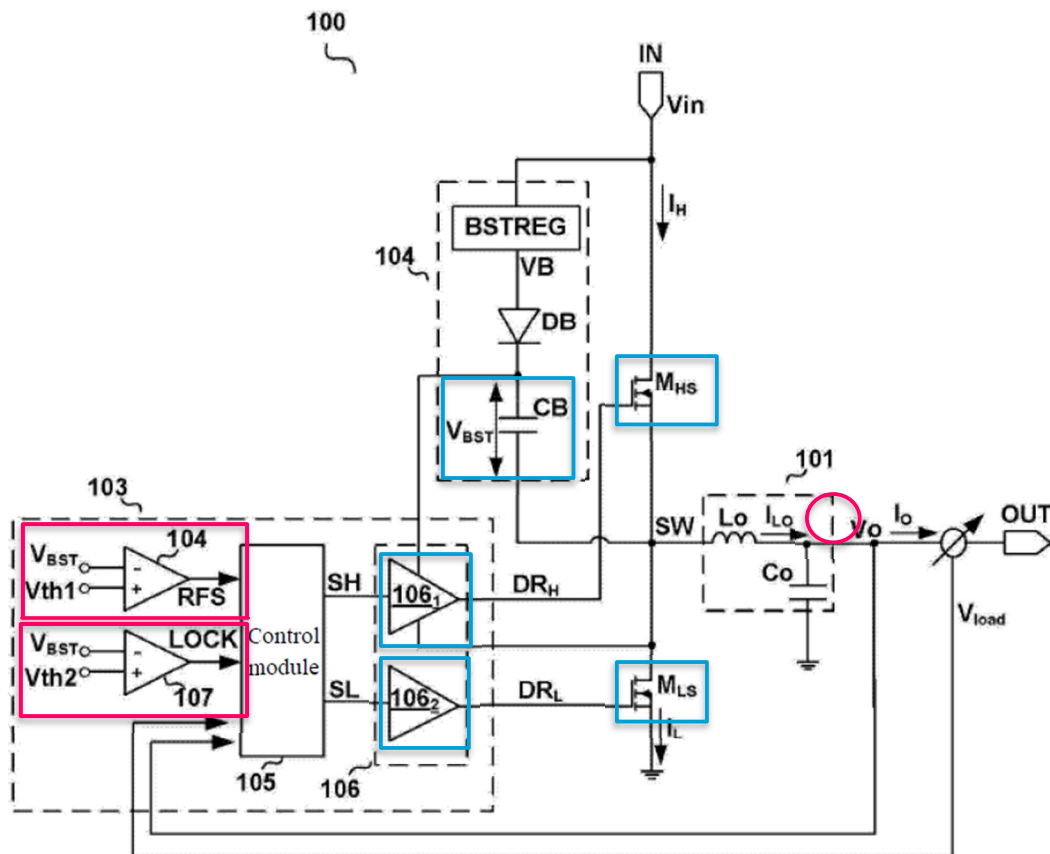


Fig. 2

detail below, the bootstrap refresh signal, the undervoltage lockout signal, and the associated components provide for refreshing the bootstrap capacitor.

A first comparison module compares the bootstrap voltage V_{BST} and a first threshold signal V_{th1} to produce the bootstrap refresh signal (RFS). EX1011 at ¶30. According to this exemplary embodiment, the first threshold signal V_{th1} has a hysteresis between the first low threshold V_{L1} and the first high threshold V_{H1} , so as to reduce the possibility of false triggering due to small fluctuations of the bootstrap voltage V_{BST} . *Id.* That is, the voltage threshold received by the first comparison module includes a low threshold and a high threshold, such that the bootstrap refresh signal has a first logic state when the bootstrap voltage drops lower than the low threshold and has a second logic state when the bootstrap voltage becomes higher than the high threshold. EX1011 at ¶25; EX1003, ¶112. When the bootstrap refresh signal has the first logic state, the control logic causes the high side switch M_{HS} and the low side switch M_{LS} to switch on and off complementarily to enable the bootstrap capacitor CB to be recharged. EX1011 at ¶23.

The example circuit also includes an under-voltage lock out (UVLO) circuit configured to compare the bootstrap voltage V_{BST} with a second threshold signal V_{th2} to keep the high side switch M_{HS} and the low side switch M_{LS} from switching

when the bootstrap voltage V_{BST} is lower than the second threshold signal and has not yet refreshed to the level of the first threshold signal. *Id.* at ¶36.

Thus, a POSITA would understand that, as a whole, the control logic includes two modes of refreshing the bootstrap capacitor; in the first mode, when the bootstrap voltage is less than the first threshold, control logic switches to switch on and off complementarily to recharge the bootstrap capacitor; and in the second mode, bootstrap voltage is also less than the second threshold, control logic causes the switches to stop switching. EX1003, ¶¶113-114.

In a second embodiment, Li discloses a zero-crossing detection (ZCD) module configured to provide a zero-crossing indicating signal C_{ZCD} based on comparing the current flowing through the low side switch (I_L) to a threshold signal V_{th4} to turn the low side switch M_{LS} off when reverse current flowing in the low-side switch is greater than a threshold. EX1011 at ¶¶50-53, Fig. 3, reproduced below. Thus, when the reverse current flowing through the low-side switch is greater than the threshold, the control module shuts off the low-side switch.

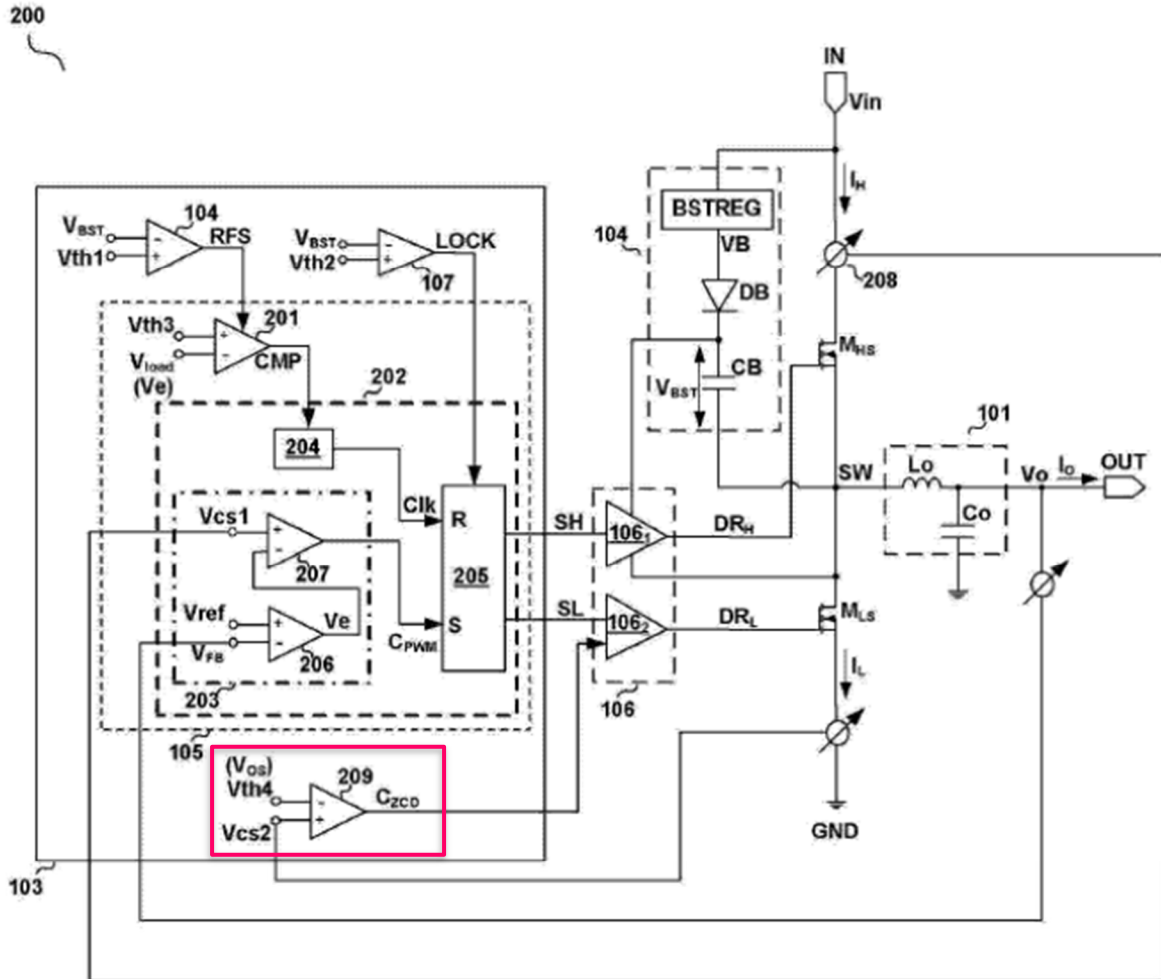


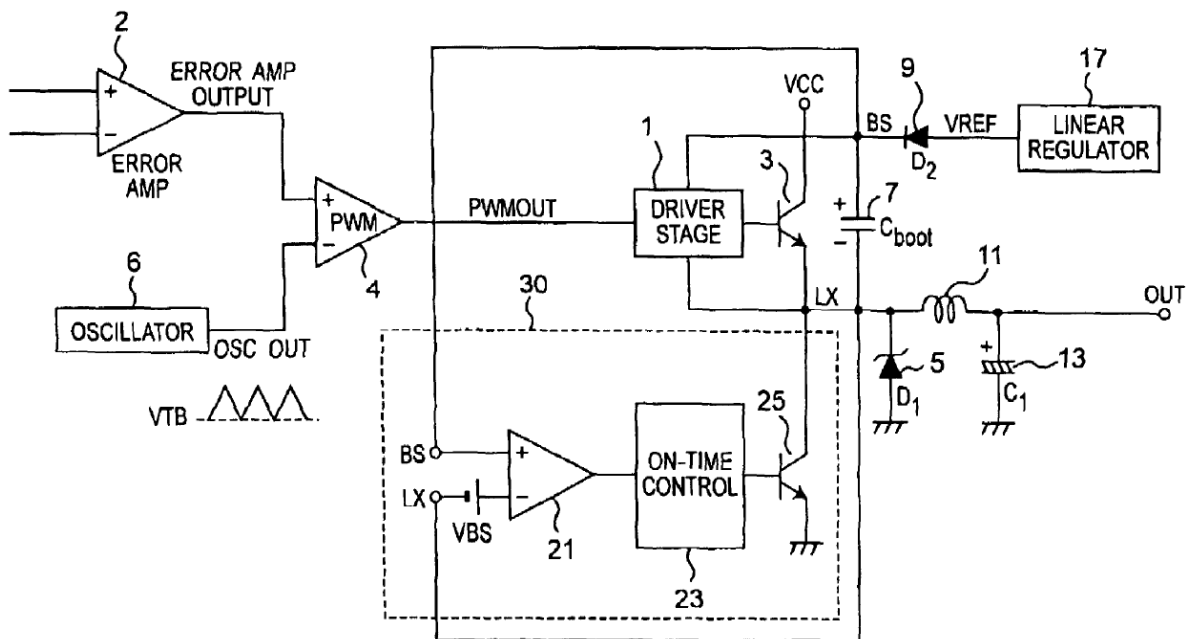
Fig. 3

D. Wong

Wong is directed to DC-DC switching power converters having a bootstrap capacitor and particularly to methods for controlling the charge of the bootstrap capacitor so that the voltage is enough to turn on the driver for the power transistor. EX1007 at 1:9-13, 38-42. Wong discloses monitoring the bootstrap voltage and

connecting the switching node (LX) to ground when the bootstrap voltage becomes less than a predetermined threshold (VBS). *Id.*, 5:3-13. An example circuit is shown in Fig. 6 (reproduced below).

Fig.6

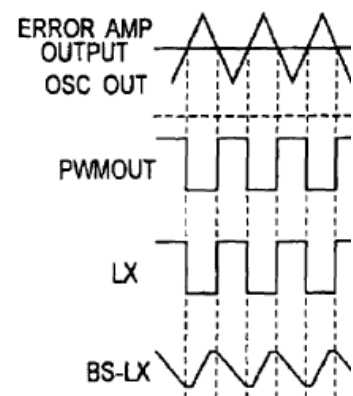


As shown in Fig. 6, Wong discloses a DC-DC converter having a power transistor (high-side switch) configured to connect the input voltage (VCC) to a switching node (LX). Fig. 6 also shows a secondary (low-side) switch 25 configured to connect the switching node to ground. The voltage across the bootstrap capacitor (Cboot) is applied to the high-side switch driver stage to operate the high-side switch. EX1003, ¶116. A load control circuit includes a BS voltage detector which compares the bootstrap voltage (referred to by Wong as VREF) to a threshold

voltage (referred to by Wong as VBS) to provide a control signal for switching on the secondary switch (during the off-time of the main power transistor) when the bootstrap voltage is less than the threshold. EX1007, 4:66-5:9; 5:64-66; EX1003, ¶118. When the secondary switch/transistor is turned on as a result of the bootstrap voltage being low, the switching node voltage is pulled near to the ground voltage, thus recharging the bootstrap capacitor. EX1007, 5:10-12; 5:64-66; EX1003, ¶118.

As shown in Fig. 6, in a PWM DC-DC converter, the duty cycle is determined by a comparator 4 which compares the output of the error amplifier 2 with a triangular signal produced from oscillator 6 and outputs a signal with a first (high) state when the error signal is greater than the triangular signal, so as to switch on the power transistor. EX1007, 5:23-35; 5:64-66. EX1003, ¶119. A POSITA would understand that the duty cycle is the relative amount of time that the power transistor is switched on (and providing power to the switch node) during one switching period. EX1003, ¶119. Thus, as shown in Fig. 4B, reproduced at right, a lower error signal (relative to the average value of the triangular signal), will result in shorter periods of time when the error signal is greater than the triangular signal and, thus, a smaller duty cycle of the power transistor. *Id.*

Fig.4B



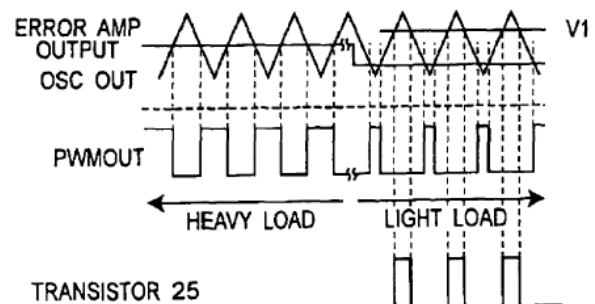
Furthermore, a POSITA would understand that the purpose of adjusting the duty cycle is for the voltage converter to provide a regulated voltage output. EX1003, ¶120. To achieve that aim, the output of the error amplifier must represent the difference between the desired output voltage of the DC-DC converter and a measured (feedback) output voltage. *Id.* That is, in the disclosed PWM DC-DC converter, the output of the error amplifier represents the output-voltage error to be corrected by adjusting the duty cycle. *Id.* Thus, the inputs to the error amplifier include the desired output voltage of the DC-DC converter and the measured (feedback) output voltage. *Id.*

Wong further discloses the PWM DC-DC converter including an on-time control configured to only switch on the secondary switch (Fig. 6, reference numeral 25) when the bootstrap voltage is less than a threshold and when the power switch is off. In one embodiment, the on time

for the secondary switch is determined by comparing the triangular oscillator signal discussed above to another threshold voltage which is higher than the maximum output of the error

amplifier. EX1007, 5:42-55. As shown in Fig. 5B (reproduced above), a POSITA

Fig.5B



would understand that by setting the threshold to a value greater than the maximum error-amplifier output, the secondary switch will only be turned on when the power transistor is turned off. EX1003, ¶121. A POSITA would also understand that the on-time for the secondary switch is based only on the triangular signal and the constant voltage threshold. *Id.* A POSITA would understand that the triangular signal will be greater than the constant voltage threshold for a fixed length each period, as shown in Fig. 5B. *Id.* Thus, the secondary switch is switched on for a constant time each period. *Id.*

VII. IT IS MORE LIKELY THAN NOT THAT AT LEAST ONE OF THE CHALLENGED CLAIMS IS UNPATENTABLE

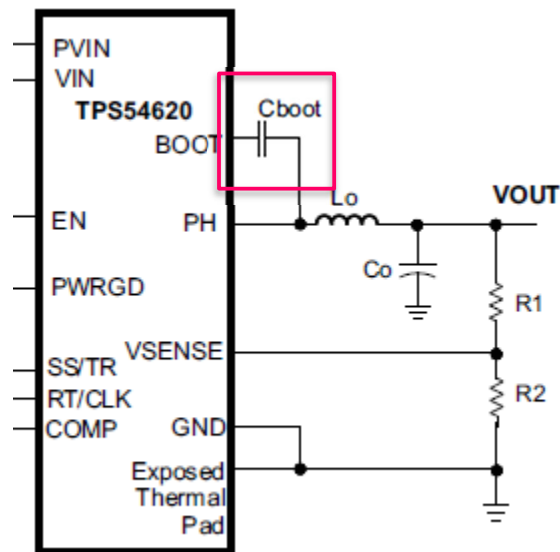
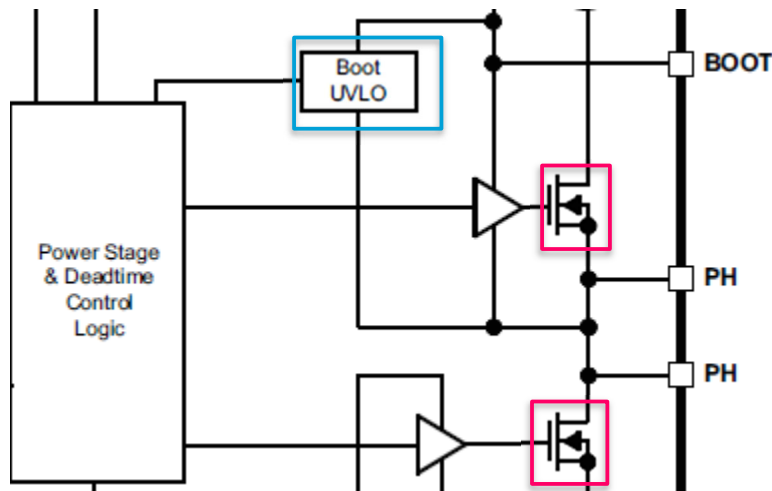
A. Ground 1: Claims 1, 11, and 12 are anticipated by, or obvious over, TI

1. Claim 1

a. Limitation 1[PRE]

To the extent the preamble is limiting, TI discloses a voltage converter having integrated high-side and low-side MOSFETs and requiring a bootstrap capacitor between boot and switch-node pins to carry the drive voltage for the high-side MOSFET. EX1006, 1, 5; EX1003, ¶¶122-23. See also Functional Block Diagram and Simplified Schematic, portions of which are reproduced below. The TPS54620 includes a monitor circuit (Boot ULVO) which pulls the switch node low when the

bootstrap voltage is equal to or less than a threshold voltage, allowing the boot capacitor to be recharged. EX1006 at 14; EX1003, ¶123.



Thus, TI discloses a voltage converter having a high-side switch, a low-side switch, a bootstrap capacitor that provides the drive voltage for the high-side switch, and a bootstrap refresh control circuit for recharging the bootstrap capacitor when

the bootstrap voltage drops below a threshold. *Id.*, ¶125. Therefore, TI anticipates limitation 1[PRE]. *Id.*

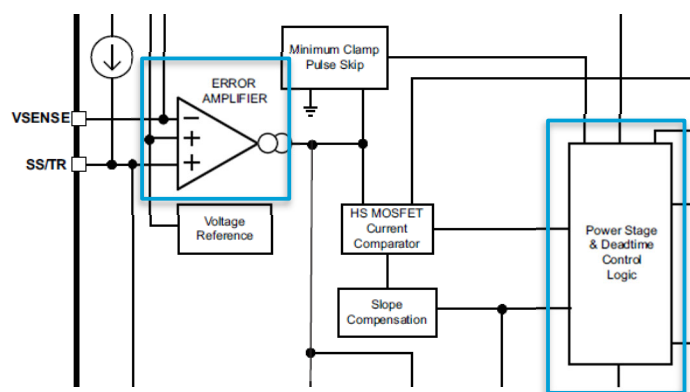
b. Limitation 1[A]

Limitation 1[A] recites the structure of “a bootstrap refresh module” that comprises a “first comparing module” having two inputs and an output that outputs a “first comparing signal” by comparing the bootstrap voltage signal and the bootstrap refresh threshold and defines the first comparing signal as having one of two logic states depending on which input signal is larger. EX1003, ¶126. As discussed, with respect to limitation 1[PRE], TI discloses the TPS54620 including a monitor circuit (Boot ULVO) which compares the bootstrap voltage to a threshold (about 2.1 volts). *See* §VII.A.1.a, *supra* (incorporated here); EX1006, 10. The output of the monitor circuit is received by the Power Stage Logic. EX1003, ¶126. Depending on the state of the monitor-circuit output (i.e., when the bootstrap voltage drops below a threshold), the Power Stage Logic will turn on the low-side MOSFET, allowing the boot capacitor to be recharged. EX1006, 14. A POSITA would understand from this disclosure that a comparator input receiving the threshold voltage is necessarily present, notwithstanding the simplicity of TI’s high level block diagrams. EX1003, ¶¶126, 49-56. Thus, TI discloses a bootstrap refresh module, comprising the Boot ULVO and at least a portion of the Power Stage Logic, that

compares the bootstrap voltage signal to a bootstrap refresh threshold to produce an output having one of two states. EX1003, ¶126. Therefore, TI expressly or inherently anticipates limitation 1[A]. *Id.* Alternatively, limitation 1[A] is obvious over TI in view of the knowledge of a POSITA. *See* EX1003, ¶49-56, 105, 126.

c. Limitation 1[B]

Limitation 1[B] recites “a voltage difference module” that has two input terminals and an output terminal, and compares an output voltage feedback signal to a reference voltage to provide a difference signal at the output terminal. EX1003, ¶127. A POSITA would understand that a voltage difference module and an error amplifier are equivalent. *Id.*, ¶158. TI discloses an error amplifier which receives a feedback signal based on VOUT (scaled down through a resistor divider), via the



VSENSE pin as shown in the Functional Block Diagram, a portion of which is reproduced at left. EX1006, 6, 11; EX1003, ¶127.

The error amplifier also receives a voltage reference, either from an internal source or the SS/TR pin. *Id.*, ¶128. The output of the error amplifier is based on the error, i.e., the difference, between the feedback signal and the voltage reference. *Id.* Thus, TI discloses a voltage difference

module that receives a feedback signal representing the output voltage of the voltage converter, and a reference voltage signal representing a desired output voltage and compares the feedback signal and the reference voltage to produce a difference signal at the output. *Id.* Therefore, TI anticipates limitation 1[B]. *Id.*

d. Limitation 1[C]

Limitation 1[C] recites that the bootstrap refresh module is configured to decrease the output voltage of the voltage converter when the bootstrap voltage signal is lower than the bootstrap refresh threshold (first comparing signal has the first logic state). EX1003, ¶129.

TI discloses that, when the bootstrap voltage drops below a threshold (about 2.1V, depending on temperature), the switch node (PH) is pulled low (connected to ground). EX1006, 10. Pulling the switch node low necessarily causes VOUT (which is connected to the switch node through the output inductor) to decrease. EX1003, ¶131; *see also* ¶70-74. Patent Owner applies this understanding in its allegation of infringement. *See* EX1030, 15.

The output of TI's bootstrap-monitor circuit (i.e., the first comparing signal) is connected to the Power Stage Logic, which is configured to provide control signals for driving the high-side and low-side switches. EX1006, 6; EX1003, ¶130. A POSITA would understand that the switch node is pulled low by a control signal

from the Power Stage Logic which is based on the output of TI's bootstrap monitor-circuit (when the bootstrap voltage drops below a threshold). *Id.* Thus, TI discloses a bootstrap refresh module configured to decrease the output voltage of the voltage converter when the bootstrap voltage signal is lower than the bootstrap refresh threshold. Therefore, TI expressly or inherently anticipates limitation 1[C]. *Id.* Alternatively, it would be obvious to a POSITA. *See* EX1003, ¶¶70-74, 131.

e. Limitation 1[D]

Limitation 1[D] recites circuitry switching on and off the high-side and low-side switches based on the difference signal (recited in limitation 1[B]) when the feedback signal is less than the reference voltage, to charge the bootstrap capacitor. EX1003, ¶131.

TI discloses using the TPS54620 in a point-of-load voltage regulation circuit. EX1006, 1; EX1003, ¶132. A POSITA would understand that a voltage regulator with integrated MOSFETs would include circuitry that switches the MOSFETS on and off to regulate the output voltage, and that the regulation is based on a difference between a feedback signal and the reference voltage. *Id.* Furthermore, a POSITA would understand that switching the MOSFETS on and off would charge the bootstrap capacitor at least during the time when the high-side switch is off and the low-side switch is on. EX1003, ¶132. In normal operation of a DC-DC power

converter, the output voltage is maintained at a desired value such that the feedback signal is equal to the reference voltage. *Id.*, ¶64. Thus, when the output voltage is subsequently decreased from the desired value, the feedback signal necessarily falls below the reference voltage. *Id.*, ¶69. Further, TI discloses that when the TPS54620 begins a “soft start” sequence, the feedback signal will be below the reference voltage. *Id.*, ¶¶69, 107, 133; EX1006 at 10, 14. Additionally, a POSITA would understand that at the time when the TPS54620 exits a “pulse skipping” mode of operation (and resumes switching the MOSFETS on and off to regulate the output voltage), the feedback signal will also be below the reference voltage. EX1003, ¶¶69, 133; EX1022, 10-11; EX1023, 12.

Furthermore, TI discloses the output of the disclosed error amplifier connected to Power Stage Logic (indirectly, through the HS Current Comparator), and that the Power Stage Logic provides control signals for controlling the high-side and low-side switches. EX1006, 6; EX1003, ¶133. Therefore, a POSITA would understand that TI’s disclosed Power Stage Logic switches on and off the high-side and low-side switches based on the output of the error amplifier, thus charging the bootstrap capacitor. EX1003, ¶133. A POSITA would also understand that this would include when the feedback signal is less than the reference voltage, as described above. *Id.* Therefore, TI anticipates limitation 1[D]. *Id.*

2. Claim 11

Claim 11 is directed to a voltage converter comprising a switching circuit and a bootstrap circuit substantially identical to the recitations in claim 1. Thus, claim 11, for at least the same reasons as claim 1, is unpatentable over TI. *See* EX1003, ¶134; *see also* §VII.A.1, *supra* (incorporated here).

a. Limitation 11[PRE]

TI discloses a voltage converter as recited in limitation 11[PRE]. *See* §VII.A.1.a, *supra* (incorporated here); EX1003, ¶¶135, 122-23.

b. Limitation 11[A]

TI discloses such a switching circuit as recited in limitation 11[A]. *See* §VII.A.1.a, *supra* (incorporated here); EX1003, ¶¶136, 124-25.

c. Limitation 11[B]

TI discloses such a bootstrap circuit as recited in limitation 11[B]. *See* §VII.A.1.b, *supra* (incorporated here); EX1003, ¶¶137, 131-33.

d. Limitation 11[C]

TI expressly or inherently discloses a bootstrap refresh control circuit as recited in limitation 11[C]. *See* §VII.A.1.b, *supra* (incorporated here); EX1003, ¶¶138, 126. Alternatively, a POSITA would find this limitation obvious for the same reasons as limitation 1[A]. *Id.*

e. Limitation 11[D]

TI discloses a voltage difference module as recited in limitation 11[D]. *See* §VII.A.1.c, *supra* (incorporated here); EX1003, ¶¶139, 127-28.

f. Limitation 11[E]

TI expressly or inherently discloses limitation 11[E]. *See* §VII.A.1.d, *supra* (incorporated here); EX1003, ¶¶140, 129-30. Alternatively, it would be obvious to a POSITA. *See Id.*, ¶¶71-74, 130.

g. Limitation 11[F]

TI discloses limitation 11[F]. *See* §VII.A.1.e, *supra* (incorporated here); EX1003, ¶¶141, 131-33.

3. Claim 12

Claim 12 is a method claim reciting a method of use for a voltage converter. TI expressly or inherently anticipates each step of claim 12. EX1003, ¶142; see also §VII.A.1, *supra* (incorporated here).

a. Limitation 12[PRE]

TI discloses a voltage converter as recited in limitation 12[PRE]. *See* §VII.A.1.a, *supra* (incorporated here); EX1003, ¶¶143, 122-23.

b. Limitation 12[A]

Limitation 12[A] recites sensing a bootstrap voltage signal. TI discloses this method step. *See* EX1006 at 14; EX1003, ¶¶144, 126; *see also* §VII.A.1.b, *supra*; §VII.A.1.d, *supra* (incorporated here).

c. Limitation 12[B]

Limitation 12[B] recites comparing the bootstrap voltage with a bootstrap refresh threshold to provide a first comparing signal having one of two logic states. TI discloses this method step, including the recited logic states. *See* EX1006 at 14; EX1003, ¶¶145, 126; *see also* §VII.A.1.b, *supra* (incorporated here).

d. Limitation 12[C]

Limitation 12[C] recites determining whether the voltage signal is smaller than the bootstrap refresh threshold. TI discloses this method step. *See* EX1006 at 14; EX1003, ¶¶146, 126; *see also* §VII.A.1.b, *supra* (incorporated here).

e. Limitation 12[D]

Limitation 12[D] recites decreasing the output voltage when the bootstrap voltage signal is determined to be lower than the bootstrap refresh threshold. TI discloses this limitation. *See* §VII.A.1.d, *supra* (incorporated here); *See* EX1006 at 14; EX1003, ¶¶147, 129-30.

f. Limitation 12[E]

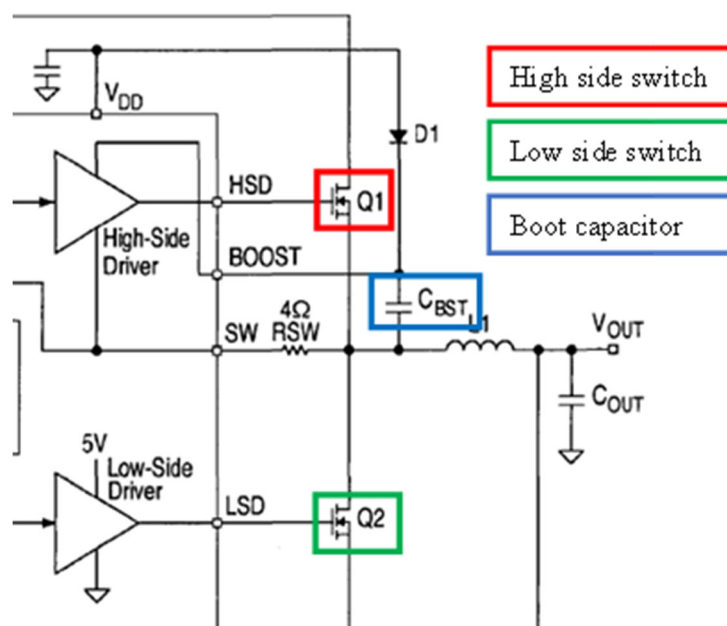
Limitation 12[E] recites switching the high side and low side switches to increase the bootstrap voltage (i.e., to charge the bootstrap capacitor). TI discloses this limitation. See §VII.A.1.e *supra* (incorporated here); EX1006 at 14; EX1003, ¶¶148, 131-33.

B. Ground 2: Claims 1, 11, and 12 are anticipated by Galinski

1. Claim 1

a. Limitation 1[PRE]

To the extent limitation 1[PRE] is limiting, Galinski discloses a voltage converter that comprises a high-side switch, a low-side switch and a bootstrap capacitor for providing a bootstrap voltage signal to supply a high side driver of the high side switch. See EX1005, Fig. 1 (annotated), reproduced below; EX1003, ¶151.

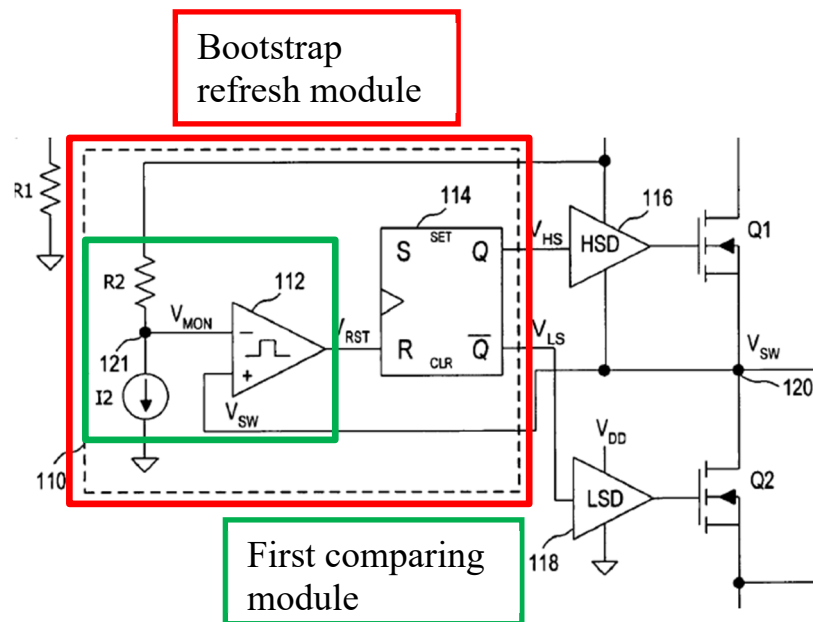


As Galinski explains, a switching voltage regulator provides power supply function through power switches that are turned on and off to transfer energy from the input to the output in discrete packets. EX1005, 1:14-19. The power switches generate a switching output voltage (V_{SW}) which is coupled to an inductor-capacitor (LC) network for filtering the switching output voltage to generate a relatively constant DC output voltage V_{OUT} . *Id.*, 1:32-40. Specifically, the high-side switch and the low-side switch are turned on alternately to increase or decrease the inductor current through the inductor. *Id.* Thus, Galinski discloses converting the input voltage to the output voltage based on switching the high side and low side switches on and off. EX1003, ¶152.

Galinski further discloses that the bootstrap voltage (“BOOST”) is generated by switching of the switching-output voltage V_{SW} . EX1005, 2:8-18. If the duty cycle goes to 100%, there will be no switching at the switching output voltage V_{SW} and the bootstrap voltage cannot be maintained. *Id.* For instance, even though capacitor C_{BST} (FIG. 1) is charged up to the bootstrap voltage BOOST, leakage current will cause the precharged voltage at capacitor C_{BST} to decrease so that periodic refreshing of the bootstrap voltage BOOST is required. *Id.*, 2:19-22. Thus, Galinski discloses a bootstrap capacitor for providing a bootstrap voltage signal to supply a high side driver of the high side switch. EX1003, ¶153.

b. Limitation 1[A]

Limitation 1[A] recites the structure of “a bootstrap refresh module” that comprises a “first comparing module” having two inputs and an output that outputs a “first comparing signal” by comparing the bootstrap voltage signal and the bootstrap refresh threshold and defines the first comparing signal as having one of two logic states depending on which input signal is larger. EX1003, ¶154. Galinski discloses “a control circuit for monitoring and maintaining the bootstrap voltage incorporated in [a] switching regulator.” See EX1005, 5:4-24, Fig. 2. The complete voltage regulator includes other circuit elements as shown in FIG. 1. *Id.*



Referring to FIG. 2, bootstrap voltage control circuit 110 includes a comparator circuit 112 that receives a monitor voltage V_{MON} at a first input and a switching output voltage V_{SW} at a second input. *Id.*, 8:30-53. Galinski discloses that

V_{MON} is scaled from V_{BOOST} such that a minimum bootstrap voltage V_{BOOST_MIN} is always greater than V_{IN} plus V_{TH_HS} , or the threshold voltage required to operate the high side switch. *Id.*, 8:54-61. A POSITA would recognize that V_{MON} is derived from bootstrap voltage V_{BOOST} and thus represents, expressly or inherently, the voltage across the bootstrap capacitor. EX1005, 7:28-41; EX1003, ¶155-56.

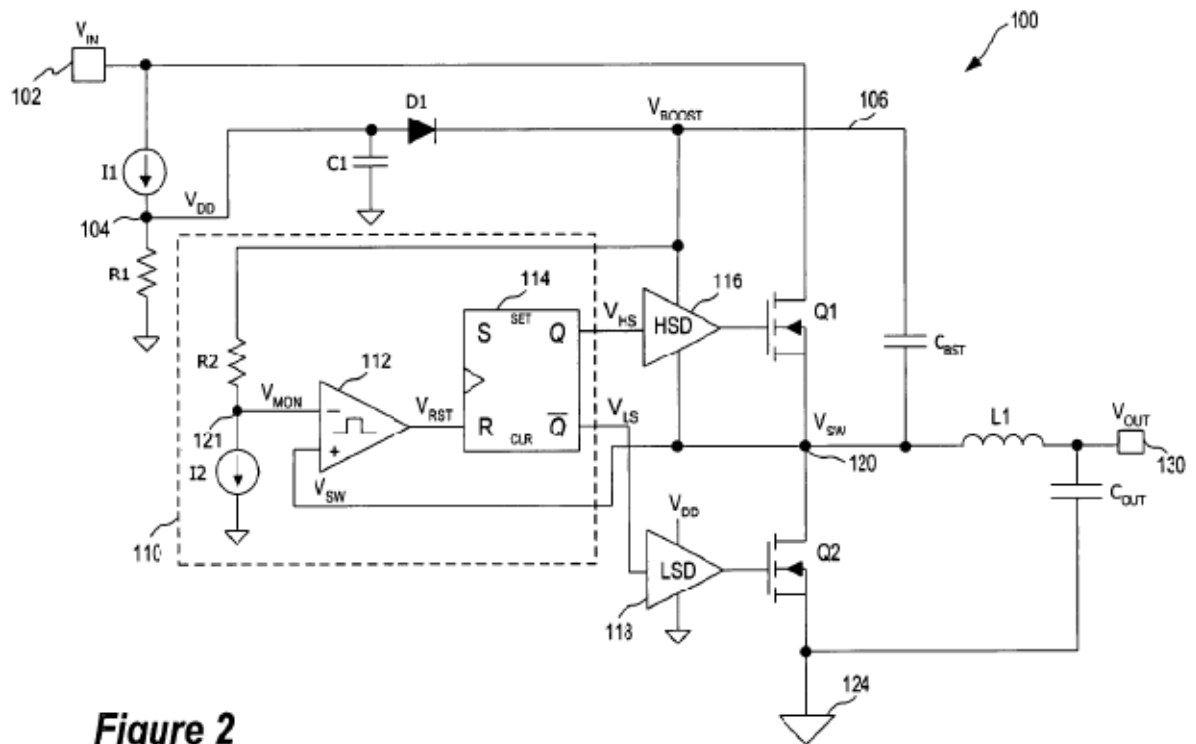


Figure 2

Galinski further discloses that “[w]hen the monitor voltage V_{MON} is equal to or less than voltage V_{SW} , comparator circuit 112 generates a[n]... output voltage signal V_{RST} .” EX1005, 9:1-5. A POSITA would understand that, as used by the bootstrap voltage control circuit 110 and comparator circuit 112, the switching output voltage V_{SW} is a threshold against which the bootstrap voltage is compared to determine

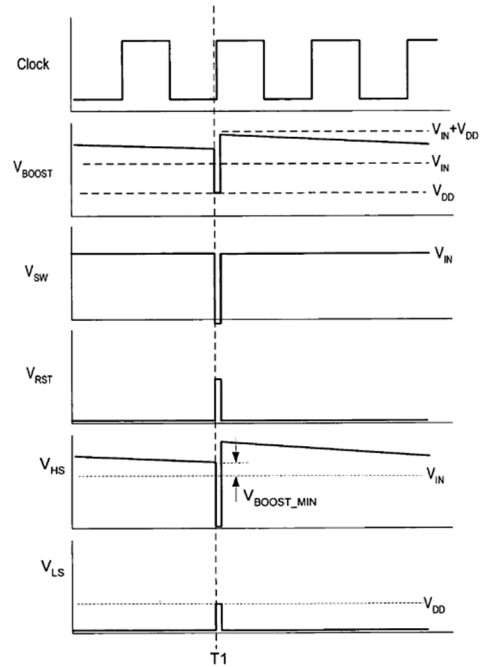


Figure 3

whether to recharge the bootstrap capacitor, i.e. a bootstrap refresh threshold. EX1005, 9:1-28, Fig. 3 (reproduced above); EX1003, ¶157. A POSITA reading Galinski would understand that V_{MON} is selected such that it falls below V_{SW} at the same time that V_{HS} falls below V_{BOOST_MIN} indicating that the bootstrap capacitor needs to be refreshed to enable V_{HS} to drive the high side switch. *Id.* Therefore, Galinski expressly or inherently anticipates limitation 1[A]. *Id.*

c. Limitation 1[B]

Limitation 1[B] recites “a voltage difference module” that has two input terminals and an output terminal, and compares an output voltage feedback signal to a reference voltage to provide a difference signal at the output terminal. EX1003,

¶158. Galinski discloses that voltage converters typically include a feedback control loop formed by dividing down the output voltage V_{OUT} to provide a feedback voltage V_{FB} and feeding back the feedback voltage V_{FB} to an error amplifier where the feedback voltage (V_{FB}) is compared to a reference voltage. EX1005, 5:56-61, 5:65-6:8. In particular, Galinski's error amplifier receives V_{FB} and V_{REF} (in the example of Fig. 1, 0.8 V) at its input terminals and provides a difference signal at its output terminal. A POSITA would recognize the "voltage difference module" is simply an error amplifier comparing a feedback signal indicating the voltage at the output of the voltage converter to a reference voltage indicating the desired output voltage. EX1003, ¶158. The difference between the two is the "error" at the output, or the amount of difference between the actual output voltage and the desired output voltage. *Id.* Thus, Galinski expressly or inherently anticipates limitation 1[B]. *Id.*

d. Limitation 1[C]

Limitation 1[C] recites that the bootstrap refresh module is configured to decrease the output voltage of the voltage converter when the bootstrap voltage signal is lower than the bootstrap refresh threshold (first comparing signal has the first logic state). EX1003, ¶159.

When the bootstrap voltage (V_{BOOST}) is equal to or less than the threshold voltage (V_{th}), the comparator generates an output pulse (V_{RST}), causing the power

switches Q1 and Q2 to switch, thereby refreshing the bootstrap voltage V_{BOOST} . *Id.*, 9:3-5. During this recharge phase, the switching output voltage V_{sw} switches from input voltage V_{in} to 0 volt temporarily. EX1005, 10:19-23. A POSITA would understand that a decrease in V_{sw} would necessarily lead to a decrease in V_{OUT} . EX1003, ¶¶160-61. Thus, Galinski expressly or inherently anticipates limitation 1[C].

e. Limitation 1[D]

Limitation 1[D] recites circuitry switching on and off the high-side and low-side switches based on the difference signal (when the feedback signal is less than the reference voltage) to charge the bootstrap capacitor. EX1003, ¶162.

Galinski discloses feeding back V_{FB} to an error amplifier where V_{FB} is compared to a reference voltage. EX1005, 5:56-61. The feedback control loop regulates the output voltage V_{OUT} at a constant level over changing load conditions by varying the duty cycle of the power switches. EX1003, ¶163. That is, the high-side switch and the low-side switch are turned on alternately to increase or decrease the inductor current through the output inductor. EX1005, 5:65-6:8. A POSITA would understand that, in normal operation of a DC-DC power converter, the output voltage is maintained at a desired value such that the feedback signal is equal to the reference voltage. EX1003, ¶64. Thus, when the output voltage is subsequently

decreased from the desired value, the feedback signal necessarily falls below the reference voltage. *Id.*, ¶69. Further, it was well known that during a “soft start” the feedback signal (V_{FB}) would be below the reference voltage as V_{OUT} ramps up. *Id.*, ¶¶69, 107, 163. And it was also well known that when exiting “pulse skipping” mode, the feedback signal will also be below the reference voltage. *Id.*, ¶¶69, 163. In the conventional buck regulator such as that shown in FIG. 1, the bootstrap voltage (“BOOST”) is generated (refreshed) by switching of the switching output voltage V_{SW} by the driver logic. *Id.*, ¶163. Galinski discloses switching on and off the high-side and low-side switches based on the difference signal to charge the bootstrap capacitor, including when the feedback signal is less than the reference voltage because of the decrease in output voltage from the desired value, when the regulator is in “soft start” mode, or when the regulator exits a “pulse skipping” mode. *Id.* Thus, Galinski expressly or inherently anticipates limitation 1[D]. *Id.*

2. Claim 11

Claim 11 is directed to a voltage converter comprising a switching circuit and a bootstrap circuit substantially identical to the recitations in claim 1. Thus, claim 11, for at least the same reasons as claim 1, is unpatentable over the Galinski. *See* EX1003, ¶164; *see also* §VII.B.1, *supra* (incorporated here).

a. Limitation 11[PRE]

Galinski discloses a voltage converter as recited in limitation 11[PRE], to the extent it is limiting. *See* §VII.B.1.a, *supra* (incorporated here); EX1003, ¶165.

b. Limitation 11[A]

Galinski discloses such a switching circuit as recited in limitation 11[A]. *See* §VII.B.1.a, *supra* (incorporated here); *Id.*, ¶166-67; 149-52.

c. Limitation 11[B]

EX1003, ¶168. Galinski discloses such a bootstrap circuit as recited in limitation 11[B]. *See* §VII.B.1.b, *supra* (incorporated here); *Id.*, ¶168-69, 151.

d. Limitation 11[C]

Galinski discloses a bootstrap refresh control circuit as recited in limitation 11[C]. *See* §VII.B.1.a, *supra*; §VII.B.1.b, *supra* (incorporated here); EX1003, ¶170, 154-57.

e. Limitation 11[D]

Galinski discloses a voltage difference module as recited in limitation 11[D]. *See* §VII.B.1.c, *supra* (incorporated here); EX1003, ¶171, 158.

f. Limitation 11[E]

Galinski discloses limitation 11[E]. *See* §VII.B.1.d *supra* (incorporated here); EX1003, ¶172, 159-61.

g. Limitation 11[F]

Galinski discloses limitation 11[F]. *See* §VII.B.1.e, *supra* (incorporated here); EX1003, ¶173, 162-63.

3. Claim 12

Claim 12 is a method claim reciting a method of use for a voltage converter. Galinski expressly or inherently anticipates each step of claim 12. EX1003, ¶174; *see also* §VII.B.1, *supra* (incorporated here).

a. Limitation 12[PRE]

Limitation 12[PRE] recites the structural requirements of a voltage converter for use in the recited method in claim 12. Galinski discloses a voltage converter as recited in limitation 12[PRE]. *See* §VII.B.1.a, *supra* (incorporated here); EX1003, ¶175.

b. Limitation 12[A]

Limitation 12[A] recites sensing a bootstrap voltage signal. Galinski discloses this method step. *See* EX1005 at 2:44-49, Fig. 2; EX1003, ¶176; *see also* §VII.B.1.b, *supra*.; §VII.B.1.d, *supra* (both incorporated here).

c. Limitation 12[B]

Limitation 12[B] recites comparing the bootstrap voltage with a bootstrap refresh threshold to provide a first comparing signal having one of two logic states. Galinski discloses this method step. *See* EX1005 at 9:1-5. (“When the monitor

voltage V_{MON} is equal to or less than voltage V_{SW} , comparator circuit 112 generates a reset pulse as the output voltage signal V_{RST} .”), EX1003, ¶¶177-178; *see also* §VII.B.1.b, *supra* (incorporated here).

d. Limitation 12[C]

Limitation 12[C] recites determining whether the voltage signal is smaller than the bootstrap refresh threshold. EX1003, ¶179. Galinski discloses this method step. *See* EX1005 at 9:1-5., EX1003, ¶180; *see also* §VII.B.1.b, *supra* (incorporated here).

e. Limitation 12[D]

Limitation 12[D] recites decreasing the output voltage when the bootstrap voltage signal is determined to be lower than the bootstrap refresh threshold. EX1003, ¶181. Galinski discloses this limitation. *See* §VII.B.1.d, *supra* (incorporated here); EX1005 at 10:19-23 (“the switching output voltage V_{sw} switches from input voltage V_{in} to 0 volt temporarily”); EX1003, ¶182.

f. Limitation 12[E]

Limitation 12[E] recites switching the high side and low side switches to increase the bootstrap voltage (i.e., to charge the bootstrap capacitor). EX1003, ¶183. Galinski disclose this limitation. *See* §VII.B.1.e, *supra* (incorporated here); EX1003, ¶184.

C. Ground 3: Claims 1, 2, 11, 12, and 16 are rendered obvious by Galinski in view of Li and/or the knowledge of ordinary skill

1. Reasons to combine

A POSITA would have been motivated to modify Galinski based on the knowledge of ordinary skill or combine Galinski with Li to arrive at the features of claims 1-2, 11-12, and 16 for numerous reasons presented below. EX1003, ¶185.

a. Analogous Art

Galinski and Li are each in the same field of endeavor and therefore analogous art to the '608 Patent, namely methods of recharging a bootstrap capacitor in power converters. EX1005 at 2:12, 2:44-48; EX1008 at ¶[0002]-[0005]; EX1003, ¶186. Galinski and Li are also each reasonably pertinent to a problem the inventors of the '608 Patent attempted to solve, namely the problem of timely recharging a bootstrap capacitor for maintaining high side voltage in buck converters. *Id.*

b. Motivation to Combine

A POSITA would readily modify Galinski to include features taught by Li for advantageous reasons. EX1003, ¶187. For example, a POSITA would combine Galinski with Li's hysteresis monitoring of V_{BST} to avoid "chattering" (false triggering). EX1008, ¶25; EX1003, ¶187.

c. Reasonable Expectation of Success

The references include similar arrangements of well-understood components and use predictable technology in routine and conventional ways. EX1003, ¶188. For example, Li offers different circuits to achieve the same goal as Galinski, that is, a DC-DC converter using a bootstrap capacitor that is sensed and refreshed as needed. EX1005, 3:17-22; EX1008, ¶6-7; EX1003, ¶188. A POSITA would find it straightforward to adapt the ideas presented in Li, or within a POSITA's knowledge, to Galinski's DC-DC converter with predictable results. EX1003, ¶188.

2. Claim 1

Galinski teaches every element of claim 1. *See* §VII.B.1, *supra* (incorporated here); EX1003, ¶189; *see also* §VI.A, *supra* (incorporated here), EX1003, ¶¶49-62, 87-99, 148-62. To the extent that Galinski does not expressly or inherently disclose the one-shot comparator circuit 112 outputting a signal having a first logic state when the bootstrap voltage signal is lower than the bootstrap refresh threshold and a second logic state when the bootstrap voltage signal is larger than the bootstrap refresh threshold, Galinski renders this feature obvious to a POSITA. EX1003, ¶¶57-62, 155. Similarly, to the extent that Galinski does not expressly or inherently disclose the bootstrap voltage control circuit 110 receiving a bootstrap refresh threshold, Galinski renders this feature obvious to a POSITA. EX1003, ¶156.

3. Claim 2

Claim 2 recites hysteresis monitoring of the bootstrap voltage signal. This concept was known in the art at the time the '608 patent was effectively filed. EX1003, ¶110; EX1022, Figure 19; EX1023, Figure 19. Furthermore, Li discloses every element of claim 2. EX1003, ¶¶191-192.

a. Limitation 2[A]

Limitation 2[A] recites the bootstrap refresh threshold comprises two different thresholds. Li discloses the first threshold signal V_{th1} having a hysteresis between the first low threshold V_{L1} and the first high threshold V_{H1} . EX1008 at ¶25. Thus, Galinski and Li render obvious Limitation 2[A]. EX1003, ¶191.

b. Limitation 2[B]

Limitation 2[B] recites the comparing signal having the first logic state when the bootstrap voltage signal is lower than the low threshold and the second logic state when the bootstrap voltage signal is larger than the high threshold. A POSITA would understand that the output of Li's hysteresis comparator would have the first logic state when the bootstrap voltage V_{BST} rises above the high threshold V_{H1} and have the second logic state when the bootstrap voltage V_{BST} falls below the low threshold V_{L1} . EX1003, ¶112. Thus, Galinski and Li render obvious Limitation 2[B]. *Id.*, ¶192.

4. Claim 11

Galinski teaches every element of claim 11. *See* §VII.B.2, *supra*; VII.C.2, *supra* (incorporated here); EX1003, ¶193.

5. Claim 12

Galinski teaches every element of claim 12. *See* §VII.B.3, *supra*; VII.C.2, *supra* (incorporated here); EX1003, ¶194.

6. Claim 16

Galinski and Li render claim 16 obvious for the same reasons as Limitations 2[A] and 2[B]. EX1003, ¶195; *see* §§VII.C.3, *supra* (incorporated here).

D. Ground 4: Claims 1, 6, 11, 12, and 15 are rendered obvious by Wong

1. Claim 1

a. Limitation 1[PRE]

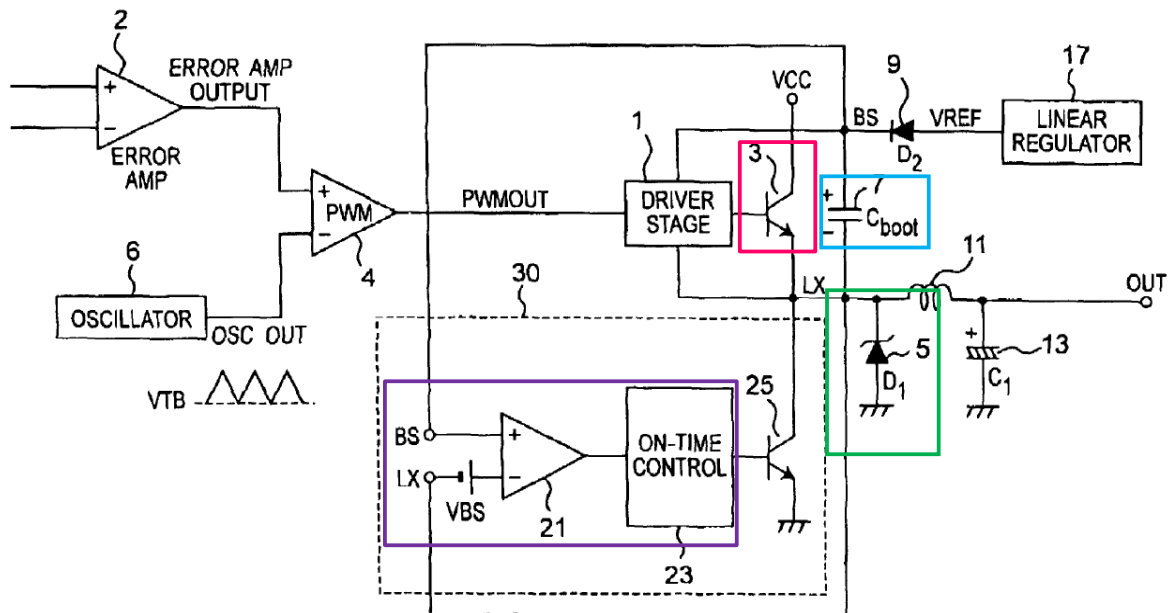
To the extent it is limiting, limitation 1[PRE] recites circuits for use in voltage converters having high side and low side switches and a bootstrap capacitor to supply a bootstrap voltage to a driver of the high side switch, where the input voltage is converted to the output voltage based on switching the high side and low side switches on and off. EX1003, ¶196; *see also* §VI.D, *supra* (incorporated here).

Wong discloses an integrated step-down DC-DC converter system, having an N-type top power transistor and a bootstrap capacitor configured to store a voltage

to turn on the power transistor and, more particularly, to a control circuit and a method for controlling the charge of the bootstrap capacitor. EX1007 at 1:9-42.

A switching node (LX) switches between a high voltage (up to VCC) when the power transistor turns on, and $(-V_d)$ during the off-time of the power transistor, where V_d is the forward diode voltage drop of a low-side diode connected between the switching node and ground. *Id.*, Fig. 6.

Fig.6



A POSITA would understand that a low-side diode is analogous to a low-side switch and that replacing Wong's low-side diode with a low-side switch is an obvious variation of Wong's converter system. EX1003, ¶¶65-68, 199. The motivation for using a low-side switch is for greater conversion efficiency and is

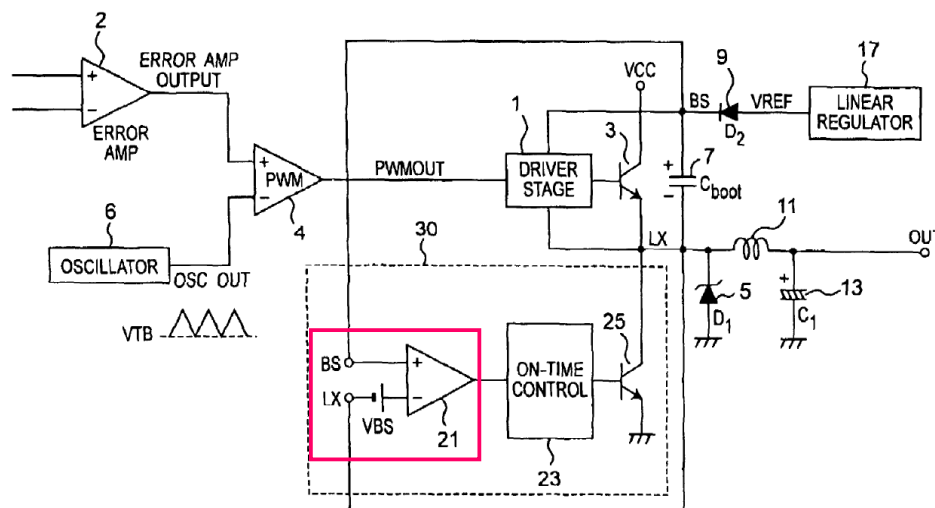
well-known in the art. *Id.* Thus, when combined with the knowledge of a POSITA, Wong teaches circuits for use in voltage converters having high side (3) and low side (5) switches and a bootstrap capacitor (7) to supply a bootstrap voltage to a driver (1) of the high side switch. *Id.*, ¶200. Furthermore, a POSITA looking at Wong's circuit diagram would understand that the converter system receives input voltage VCC and converts the input voltage to an output voltage (OUT) based on operations of the high-side switch and low-side diode (or switch). *Id.*, ¶201. That is, Wong discloses switching the power transistor on and off to switch the switching node LX between a high voltage (up to VCC) and a low voltage (-VD1) to provide a predictable output voltage based on the voltage at the switching node and associated circuit components. EX1007 at 1:60-67, EX1003, ¶201. Thus, Wong renders obvious limitation 1[PRE]. EX1003, ¶201.

b. Limitation 1[A]

Limitation 1[A] recites the structure of “a bootstrap refresh module” that comprises a “first comparing module” having two inputs and an output that outputs a “first comparing signal” by comparing the bootstrap voltage signal and the bootstrap refresh threshold and defines the first comparing signal as having one of two logic states depending on which input signal is larger. EX1003, ¶202.

Wong discloses a BS voltage detector 21 that “detects the voltage across the bootstrap capacitor 7, and compares the detected voltage with a predetermined voltage VBS. The voltage VBS is the preset threshold voltage which is higher than the minimum required voltage for the bootstrap to work.” EX1007 at 4:67-5:3. “When the voltage across the bootstrap capacitor becomes less than the voltage VBS, the BS voltage detector 21 produces a high level signal.” *Id.*, 5:3-6. Thus, a POSITA would understand that Wong’s BS voltage detector compares the bootstrap voltage and a predetermined voltage threshold (which Wong refers to as “VBS”) to produce an output signal having one of two states, including a high state when the bootstrap voltage is less than a predetermined threshold. EX1003, ¶205.

Fig.6

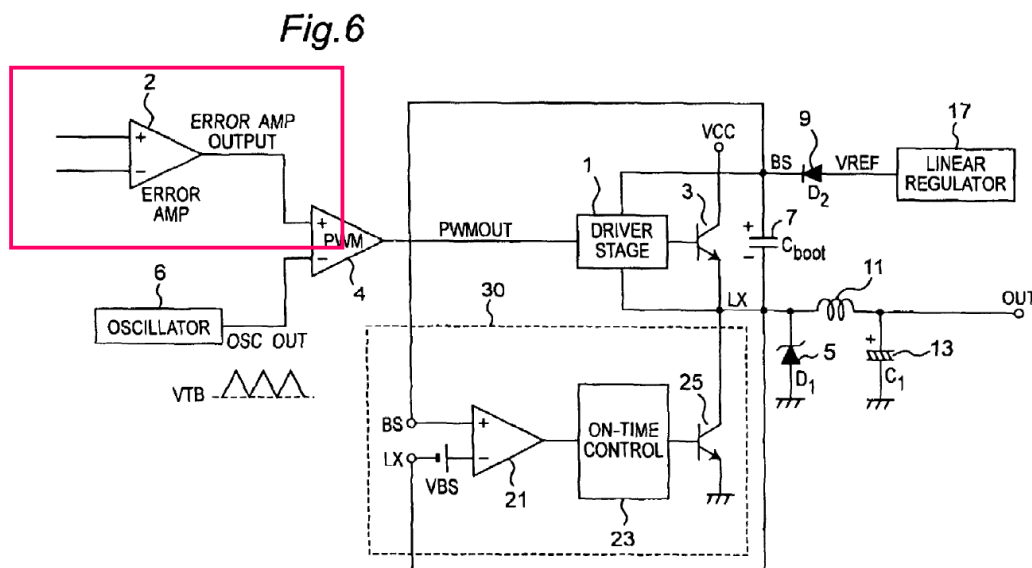


Thus, Wong renders obvious limitation 1[A]. EX1003, ¶206.

c. Limitation 1[B]

Limitation 1[B] recites “a voltage difference module” that has two input terminals and an output terminal, and compares an output voltage feedback signal to a reference voltage to provide a difference signal at the output terminal. EX1003, ¶207.

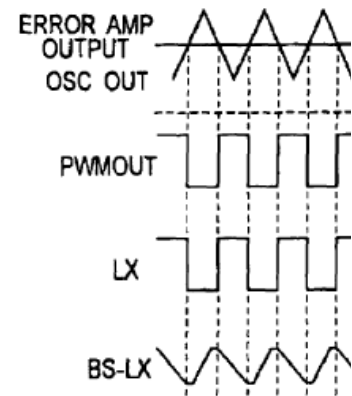
Wong discloses, “As shown in FIG. 3, in a PWM DC-DC converter, the duty cycle is determined by a comparator 4 which compares the output of the error amplifier 2 with a triangular signal produced from oscillator 6. As shown in FIG. 4B, when the error amplifier output is higher than the triangular oscillator output, the PWM output is high and the power transistor 3 is turned on.” EX1007 at 5:23-23, Figs. 3, 6 (reproduced below).



A POSITA would understand that the duty cycle is the relative amount of time that the power transistor is switched on (and providing power to the switch node) during one switching period.

EX1003, ¶119. Thus, as shown in Fig. 4B (reproduced at right), a lower error signal (relative to the average value of the triangular signal), will result in shorter periods of time when the error signal is greater than the triangular signal and, thus, a smaller duty cycle of the power transistor.

Fig.4B



Furthermore, a POSITA would understand that providing a regulated voltage output is the purpose of adjusting the timing and duration of the power switching periods of the voltage converter. EX1003, ¶216. To achieve that aim, the output of the error amplifier must represent the difference between the desired output voltage of the DC-DC converter and a measured (feedback) output voltage. EX1003, ¶120. That is, in Wong's disclosed PWM DC-DC converter, the output of the error amplifier represents the output voltage error to be corrected by adjusting the duty cycle. *Id.*

Thus, Wong's error amplifier is configured to receive a reference voltage signal representing a desired value of the output voltage of the voltage converter and

is configured to receive a feedback signal representing the output voltage of the voltage converter, and is configured to compare the feedback signal with the reference voltage signal so as to provide a difference signal at the output terminal. EX1003, ¶210. Thus, Wong renders obvious limitation 1[B].

d. Limitation 1[C]

Limitation 1[C] recites that the bootstrap refresh module is configured to decrease the output voltage of the voltage converter when the bootstrap voltage signal is lower than the bootstrap refresh threshold (first comparing signal has the first logic state). EX1003, ¶211.

Wong discloses, “When the voltage across the bootstrap capacitor becomes less than the voltage VBS, the BS voltage detector 21 produces a high level signal. When ... the BS voltage detector 21 produces high level signals, the on-time control 23 produces a high level signal to turn on the secondary transistor 25.... When the secondary transistor 25 is turned on, LX voltage will be pulled near to the ground voltage.” EX1007 at 5:3-24. That is, Wong discloses pulling the switching node to ground potential when the voltage across the bootstrap capacitor becomes less than a threshold. EX1003, ¶212. Furthermore, a POSITA would understand, based on the well-understood behavior of standard circuit components connecting the switching node to the output of the voltage converter, that grounding the switching node in this

way necessarily causes a decrease in the output voltage of the voltage converter. EX1003, ¶213; EX1030, 15 (Patent Owner applying this understanding in its allegations of infringement). Thus, Wong inherently discloses this feature. EX1003, ¶213.

A POSITA would also understand that the principle of pulling the switching-node voltage near to ground to recharge the bootstrap capacitor is applicable to other configurations of voltage converters. EX1003, ¶214. For example, if Wong's low-side diode was replaced with a low-side switch, Wong's secondary switch would be unnecessary for pulling the switching-node voltage near to ground, because that function could be performed by the low-side switch. *Id.* Similarly, although Wong discloses a PWM DC-DC converter, the teaching of grounding the switching node (thus decreasing the output voltage) to recharge the bootstrap capacitor is broadly applicable to DC-DC converters having different timing characteristics. *Id.* Thus, Wong renders obvious limitation 1[C]. *Id.*

e. Limitation 1[D]

Limitation 1[D] recites circuitry switching on and off the high-side and low-side switches based on the difference signal when the feedback signal is less than the reference voltage to charge the bootstrap capacitor. EX1003, ¶215.

As described above with respect to limitation 1[B], a POSITA would understand that the purpose of adjusting the timing and duration that the power switch(es) are turned on is for the voltage converter to provide a regulated voltage output. EX1003, ¶216; §VII.D.1.c, *supra* (incorporated here). Thus, when the output of the error amplifier indicates that the output voltage is different (either less than or greater than) than the reference signal, Wong's control circuit is configured to control the high side switch to switch on and off based on the difference signal. EX1003, ¶216. And, as discussed above with respect to limitation 1[PRE], Wong's low-side diode is analogous to a low-side switch. EX1003, ¶¶65-68, 199, 218; §VII.D.1.b, *supra* (incorporated here). Thus, Wong discloses circuitry switching on and off the high-side and low-side switches based on the difference signal. EX1003, ¶217-20.

Furthermore, Wong discloses, "The on-time of the secondary transistor 25 is determined by the on-time control 23. When the secondary transistor 25 is turned on, LX voltage will be pulled near to the ground voltage. Hence, the bootstrap capacitor 7 is charged up to 'VREF-VD'". EX1007 at 5:5-14. Therefore, the switching (on and off) of the switches causes the bootstrap capacitor to recharge. EX1003, ¶118. In normal operation, when the feedback signal is equal to the reference voltage signal and then the output voltage is decreased by pulling LX

voltage to ground, the feedback signal will necessarily fall below the reference voltage. *Id.*, ¶¶69, 220. Additionally, during a soft start, and/or when exiting a “pulse skipping” mode, the feedback signal will necessarily be below the reference voltage. *Id.*, ¶¶69, 107, 220. Thus, Wong renders obvious limitation 1[D]. *Id.*, ¶220.

2. Claim 6

a. Limitation 6[A]

Limitation 6[A] recites a Constant On Time circuit configured to provide a COT control signal so as to set a constant on time for the low side switch. EX1003, ¶221.

Wong discloses an on-time control configured to cause the secondary (low-side) switch to switch on during the period of time when a triangular oscillator signal is greater than a constant voltage threshold. EX1007 at 5:46-54, Figs. 5A, 5B (both reproduced below). It is axiomatic that a triangular signal will be greater than a constant voltage threshold for a constant period of time for each cycle of the

Fig.5B

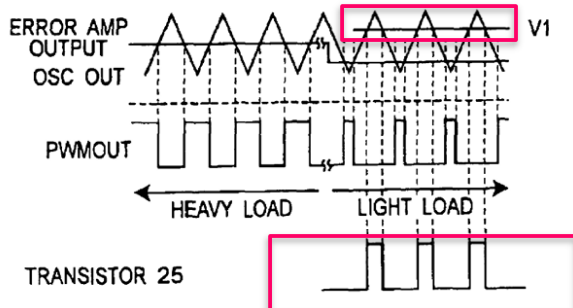
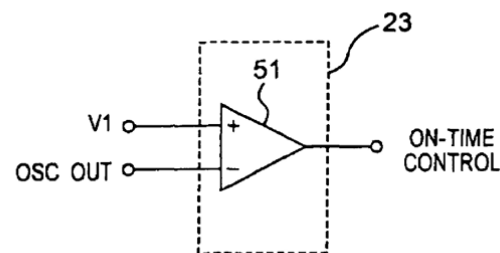


Fig.5A



triangular signal. *See* EX1003, ¶121. Wong discloses a circuit diagram including a comparator 51, where one input of the comparator 51 is applied with a predetermined voltage V1 and the other input of the same is applied with the triangular output of the oscillator 6. EX1007 at 5:43-47.

The predetermined voltage V1 is configured to be higher than the error amplifier output voltage so that the on-time of the secondary transistor 25 is set during power transistor off-time. *Id.*, 5:47-55. Thus, Wong discloses an on-time control that provides a COT control signal to set a constant on time for the low side switch and renders obvious limitation 6[A]. EX1003, ¶222.

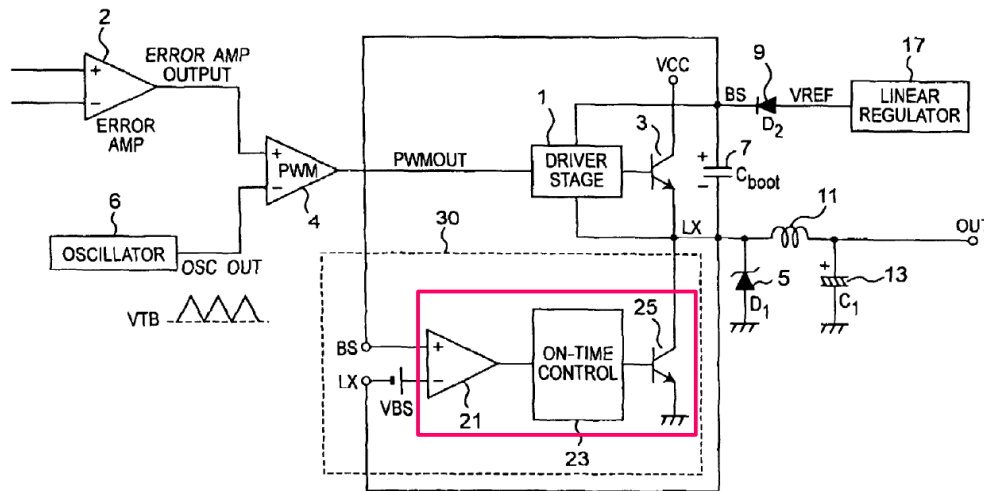
b. Limitation 6[B]

Limitation 6[B] recites a logic module having two inputs and an output, the inputs configured to receive the COT control signal and the comparing signal of limitation 1[A], the logic module configured to perform logic on the input signals and provide a bootstrap refresh signal at the output terminal. EX1003, ¶223. Thus, limitation 6[B] recites using the comparing signal and the COT control signal to produce a bootstrap refresh signal.

As discussed above with respect to limitation 1[A], Wong discloses a BS voltage detector 21 that “detects the voltage across the bootstrap capacitor 7, and compares the detected voltage with a predetermined voltage VBS.” EX1007 at 4:67-

5:3; §VII.D.1.b, *supra* (incorporated here). Wong’s BS voltage detector 21 directly interfaces with Wong’s on-time control. *Id.*, 5:6-9, Fig. 6 (reproduced below).

Fig.6



A POSITA would understand that Wong's on-time control includes modules configured to generate a COT control signal. EX1003, ¶226. In some embodiments, Wong discloses the on-time control also including discrete logic modules (e.g., comparator 51). EX1007 at 5:42-44, Fig. 5A. In some embodiments, Wong discloses the on-time control performing logical operations ("When the light load is detected, *and* the BS voltage detector 21 produces high level signals, the on-time control 23 produces a high level signal to turn on the secondary transistor 25"). EX1007 at 5:6-9 (emphasis added).

Thus, a POSITA would understand that Wong’s on-time control includes modules configured to perform logic operations on input signals, including the

comparing signal from the BS voltage detector 21 and the COT control signal, and to produce the recited bootstrap refresh signal. EX1003, ¶¶226-27; §VII.D.1.b, *supra*. (incorporated here) Because the combination of Wong’s BS voltage detector 21 and on-time control produces the recited bootstrap refresh signal based on the comparing signal of limitation 1[A] and a COT control signal, Wong renders obvious limitation 6[B]. EX1003, ¶¶226-27.

c. Limitation 6[C]

Limitation 6[C] recites the bootstrap refresh signal having a first logic state when the bootstrap voltage is lower than the threshold so as to turn the low side switch on, and the bootstrap refresh signal has a second logic state beyond the constant on time of the low-side switch, so as to turn the low side switch off. EX1003, ¶228.

Wong discloses that “when the amplified error voltage is higher than the triangular signal, the output power transistor will be turned on.” EX1007 at 2:42-45. Wong also discloses that when the bootstrap voltage detector outputs a “bootstrap low” signal, “a secondary switch will turn on during the off-time of the power transistor.” *Id.*, 2:54-60. Thus, when the bootstrap voltage is lower than the threshold, the secondary switch is turned on (for a constant time) during the off-time

of the power transistor. EX1003, ¶229. Beyond that time, the secondary switch is turned off. *Id.* Thus, Wong discloses limitation 6[C]. *Id.*, ¶230.

3. Claim 11

Claim 11 is directed to a voltage converter comprising a switching circuit and a bootstrap circuit substantially identical to the recitations in claim 1. EX1003, ¶231. Thus, for at least the same reasons as claim 1, claim 11 is unpatentable over Wong. *See* EX1003, ¶231; *see also* §VII.D.1, *supra* (incorporated here).

a. Limitation 11[PRE]

Wong discloses a voltage converter as recited in limitation 11[PRE], to the extent it is limiting. *See* §VII.D.1.a, *supra* (incorporated here); EX1003, ¶232.

b. Limitation 11[A]

Wong teaches such a switching circuit as recited in limitation 11[A]. *See* §VII.D.1.a, *supra* (incorporated here); EX1003, ¶233.

c. Limitation 11[B]

Wong discloses such a bootstrap circuit as recited in limitation 11[B]. *See* §VII.D.1.a, *supra* (incorporated here); EX1003, ¶234.

d. Limitation 11[C]

Wong discloses a bootstrap refresh control circuit as recited in limitation 11[C]. *See* §VII.D.1.b, *supra* (incorporated here); EX1003, ¶235.

e. Limitation 11[D]

Wong discloses a voltage difference module as recited in limitation 11[D].
See §VII.D.1.c, *supra* (incorporated here); EX1003, ¶236.

f. Limitation 11[E]

Wong teaches limitation 11[E]. *See* §VII.D.1.d, *supra* (incorporated here); EX1003, ¶237.

g. Limitation 11[F]

Wong teaches limitation 11[F]. *See* §VII.D.1.e, *supra* (incorporated here); EX1003, ¶238.

4. Claim 12

Claim 12 is a method claim reciting a method of use for a voltage converter. Wong renders obvious each step of claim 12. EX1003, ¶239; *see also* §VII.D.1, *supra* (incorporated here).

a. Limitation 12[PRE]

Limitation 12[PRE] recites the structural requirements of a voltage converter for use in the recited method in claim 12. Wong discloses a voltage converter as recited in limitation 12[PRE]. *See* §VII.D.1.a, *supra* (incorporated here); EX1003, ¶240.

b. Limitation 12[A]

Limitation 12[A] recites sensing a bootstrap voltage signal. Wong discloses sensing a bootstrap voltage signal. *See* EX1007 at 4:67-5:3, Fig. 6; EX1003, ¶241; *see also* §VII.D.1.b *supra*.; §VII.D.1.d, *supra* (incorporated here).

c. Limitation 12[B]

Limitation 12[B] recites comparing the bootstrap voltage with a bootstrap refresh threshold to provide a first comparing signal having one of two logic states. Wong discloses comparing the bootstrap voltage with a bootstrap refresh threshold to provide a first comparing signal having one of two logic states. *See* EX1003, ¶242; *see also* §VII.D.1.b, *supra* (incorporated here).

d. Limitation 12[C]

Limitation 12[C] recites determining whether the voltage signal is smaller than the bootstrap refresh threshold. Wong discloses determining whether the voltage signal is smaller than the bootstrap refresh threshold. *See* EX1007 at 5:3-6, Fig. 6; *see also* §VII.D.1.d *supra*.; §VII.D.1.b, *supra* (incorporated here). A POSITA would understand that the method disclosed in Wong necessarily requires the determination of whether the bootstrap voltage signal is smaller than the bootstrap refresh threshold. EX1003, ¶243.

e. Limitation 12[D]

Limitation 12[D] recites decreasing the output voltage when the bootstrap voltage signal is determined to be lower than the bootstrap refresh threshold. Wong teaches decreasing the output voltage when the bootstrap voltage signal is determined to be lower than the bootstrap refresh threshold. *See* §VII.D.1.d, *supra* (incorporated here); EX1007, 4:30-38, 4:66-5:13; EX1003, ¶244.

f. Limitation 12[E]

Limitation 12[E] recites switching the high side and low side switches to increase the bootstrap voltage (i.e., to charge the bootstrap capacitor). Wong teaches switching the high side and low side switches to increase the bootstrap voltage (i.e., to charge the bootstrap capacitor). *See* §VII.D.1.e, *supra* (incorporated here); EX1003, ¶245.

5. Claim 15

a. Limitation 15[A]

Limitation 15[A] recites providing a Constant On Time (COT) control signal having the features recited in limitation 6[A]. Wong discloses limitation 6[A]. *See* §VII.D.2.a, *supra* (incorporated here); EX1003, ¶247.

b. Limitation 15[B]

Limitation 15[B] recites providing a bootstrap refresh signal having the features recited in limitations 6[B] and 6[C]. Wong discloses limitations 6[B] and 6[C]. *See* §VII.D.2.b, §VII.D.2.c, *supra* (incorporated here); EX1003, ¶248.

c. Limitation 15[C]

Limitation 15[C] recites switching the low side switch on and off based on the bootstrap refresh signal according to the logic recited in limitation 6[C]. Wong discloses limitation 6[C]. *See* §VII.D.2.c, *supra* (incorporated here); EX1003, ¶249.

E. Ground 5: Claims 6 and 15 are rendered obvious by Galinski or, in the alternative, by Galinski in view of Wong

1. Reasons to combine

A POSITA would have been motivated to combine Galinski and Wong to arrive at the features of claims 6 and 15 for numerous reasons presented below. EX1003, ¶250.

a. Analogous Art

Galinski and Wong are each in the same field of endeavor and therefore analogous art to the '608 Patent, namely methods of recharging a bootstrap capacitor in power converters. EX1005 at 2:12, 2:44-48; EX1007 at 1:9-13, 38-42; EX1003, ¶251. Galinski and Wong are also each reasonably pertinent to a problem the inventors of the '608 Patent attempted to solve, generating a reset pulse of a short

duration, but sufficient to allow capacitor C_{BST} to be recharged. EX1001, 14:38-48; EX1005, 9:5-14; EX1007 at 5:30-36; EX1003, ¶251.

b. Motivation to Combine

A POSITA would understand that Galinski could be readily modified to include Wong's on-time control. EX1003, ¶252. Galinski discloses a bootstrap voltage control circuit 110 that includes a comparator 112 that compares the bootstrap voltage to a threshold. *Id.* In response to the bootstrap voltage falling below the threshold, the bootstrap voltage control circuit 110 is configured to generate a pulse to switch on the low-side switch for a duration sufficient to allow capacitor C_{BST} to be recharged. EX1005, 9:32-42. The bootstrap voltage control circuit 110 further includes a set-reset latch 114 that provides complementary outputs to drive the high-side and low-side switches so that the high-side switch is off during the constant on-time of the low-side switch. *Id.*, 9:7-2.

However, Galinski explains that the disclosed set-reset latch is “illustrative only and the logic circuitry for generating the drive control signals for the driver circuits is not critical to the practice of the present invention.” EX1005, 9:42-47. Galinski adds that “in other embodiments, other comparator circuits can be used to implement comparator circuit 112.” 11:23-25. Furthermore, Galinski discloses that the N-channel buck regulator of Fig. 2 is simplified and only those circuit elements

that are relevant and related to the claimed invention are included in Fig. 2. EX1005, 5:7-15. That is, other circuit elements, not disclosed in Fig. 2, are necessary for completing the switching regulator. *Id.*; EX1003, ¶253.

Wong discloses a load control circuit 30 that includes a BS voltage detector 21 that compares the voltage detected across the bootstrap capacitor 7 with a predetermined voltage VBS. The load control circuit 30 is configured to produce a signal to turn on the secondary transistor 25 during the off-time of the main power transistor 3. EX1007 at 4:66-5:9. The on-time of the secondary transistor 25 is determined by an on-time control 23 of the load control circuit 30. *Id.* at 5:23-55.

Thus, both Wong's load control circuit 30 and Galinski's bootstrap voltage control circuit 110 include logic modules for providing a constant on time signal for turning on the low-side switch. EX1003, ¶255. A POSITA would understand that Wong's disclosed load control circuit 30 could be substituted for Galinski's bootstrap voltage control circuit 110 to achieve the desired result. EX1003, ¶255. Furthermore, at least because Galinski's disclosed embodiment is "illustrative only," and does not include a complete, working circuit, a POSITA would be motivated to substitute Wong's complete load control circuit 30. EX1003, ¶255.

c. Reasonable Expectation of Success

The references include similar arrangements of well-understood components, and use predictable technology in routine and conventional ways. EX1003, ¶256. Wong offers different circuits to achieve the same goal as Galinski, that is, generating a reset pulse of a short duration, but sufficient to allow capacitor C_{BST} to be recharged. *Id.* A POSITA would find it straightforward to adapt the ideas presented in Wong to Galinski's DC-DC converter with predictable results. *Id.*

2. Claim 6

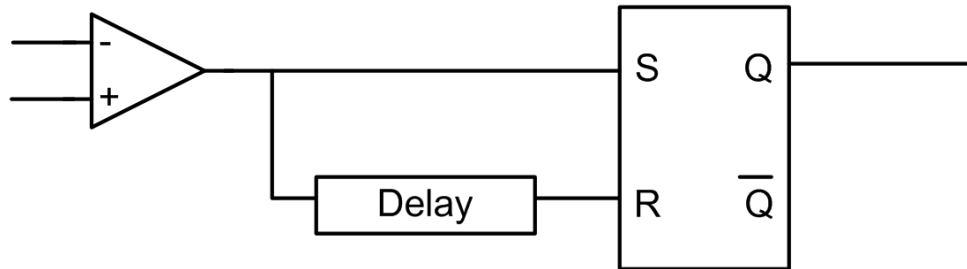
Claim 6 depends from claim 1. Galinski discloses every element of claim 1. *See* §VII.B.1, *supra* (incorporated here); EX1003, ¶257. As explained in the following subsections, Galinski renders the limitations of claim 6 obvious to a POSITA. EX1003, ¶257. In the alternative, i.e., to any extent that Galinski may not fully teach the limitations of claim 6, Wong also teaches these limitations. *See* §VII.D.2 *supra* (incorporated here), EX1003, ¶257.

a. Limitation 6[A]

Limitation 6[A] recites a Constant On Time circuit configured to provide a COT control signal so as to set a constant on time for the low side switch.

Galinski discloses a bootstrap voltage control circuit 110 including a one-shot comparator circuit 112 and configured to generate a pulse to switch on the low-side

switch for a duration sufficient to allow capacitor C_{BST} to be recharged. EX1005, 9:32-42, Fig. 2. A POSITA would understand the circuit to be a comparator followed by a one-shot circuit. EX1003, ¶258. Moreover, a POSITA would understand that one of the most basic circuits for implementing a one shot would comprise an SR flip flop (SRFF) and a delay element as shown below. EX1003, ¶¶58-62, 97, 258; EX1033, 3.



Thus, Galinski teaches limitation 6[A]. EX1003, ¶260. Wong also teaches these limitations. *See* §VII.D.2.a, *supra* (incorporated here).

b. Limitation 6[B]

Limitation 6[B] recites a logic module having two inputs and an output, the inputs configured to receive the COT control signal and the comparing signal of limitation 1[A], the logic module configured to perform logic on the input signals and provide a bootstrap refresh signal at the output terminal. Thus, limitation 6[B]

recites using the comparing signal and the COT control signal to produce a bootstrap refresh signal.

Galinski discloses a circuit generating a pulse of a short duration when the monitor voltage is less than the switching output voltage V_{sw} . EX1005, 11:20-23, Fig. 2. Galinski does not disclose a complete circuit. EX1005, 5:7-15, Fig. 2; EX1003, ¶261. However, a POSITA would understand that one of the most basic circuits for implementing a one-shot comparator would include an SR flip-flop (SRFF) and a delay element as described above. *Id.*, ¶¶58-62, 261; §VII.E.2.a, *supra* (incorporated here).

Thus, Galinski renders obvious, to a POSITA, the concept of a logic module configured to receive the comparing signal of limitation 1[A] and a COT control signal and the concept of performing logic on the input signals to provide a bootstrap refresh signal at the output terminal, generating a pulse of a short duration when the monitor voltage is less than the switching output voltage V_{sw} . *Id.*, ¶263. Thus, Galinski teaches limitation 6[B]. *Id.* Wong also teaches these limitations. *See* §VII.D.2.b, *supra* (incorporated here).

c. Limitation 6[C]

Limitation 6[C] recites the bootstrap refresh signal having a first logic state when the bootstrap voltage is lower than the threshold so as to turn the low side

switch on, and the bootstrap refresh signal has a second logic state beyond the constant on time of the low-side switch, so as to turn the low side switch off.

Galinski discloses the bootstrap voltage control circuit 110 generating drive control signal V_{LS} to cause the low-side driver circuit to turn the low-side power switch on or off. EX1005, 5:37-43. A POSITA would understand that a drive control signal that causes a driver circuit to turn the low-side power switch on or off has two logic states. EX1003, ¶265. Furthermore, Galinski discloses the bootstrap voltage control circuit 110 generating a pulse to temporarily switch on the low-side switch in response to the bootstrap voltage falling below the threshold. *Id.*, ¶100. Thus, Galinski discloses the bootstrap refresh signal having a first logic state so as to turn the low side switch on, and a second logic state beyond the (short duration) constant on time of the low-side switch, so as to turn the low side switch off. EX1003, ¶265. Thus, Galinski teaches limitation 6[C]. *Id.*, ¶266. Wong also teaches these limitations. *See* §VII.D.2.c, *supra* (incorporated here).

3. Claim 15

Claim 15 depends from claim 12. Galinski discloses every limitation of claim 12. *See* §VII.B.3, *supra* (incorporated here); EX1003, ¶267. Claim 15 recites elements that are substantially similar to claim 6. *Id.* As discussed with respect to claim 6, Galinski renders these limitations obvious to a POSITA. *See* §VII.E.2,

supra (incorporated here); EX1003, ¶267. In the alternative, i.e., to any extent that Galinski may not fully teach these limitations, Wong also teaches the limitation of claim 15. *See* §VII.D.5 *supra* (incorporated here).

a. Limitation 15[A]

Limitation 15[A] recites providing a Constant On Time (COT) control signal having the features recited in limitation 6[A]. EX1003, ¶268. Galinski teaches limitation 6[A]. *See* §VII.E.2.a, *supra* (incorporated here). Wong also teaches these limitations. *See* §VII.D.5.a, *supra* (incorporated here).

b. Limitation 15[B]

Limitation 15[B] recites providing a bootstrap refresh signal having the features recited in limitations 6[B] and 6[C]. EX1003, ¶269. Galinski teaches limitations 6[B] and 6[C]. *See* §VII.E.2.b, §VII.E.2.c, *supra* (incorporated here). Wong also teaches these limitations. *See* §VII.D.5.b, *supra* (incorporated here).

c. Limitation 15[C]

Limitation 15[C] recites switching the low side switch on and off based on the bootstrap refresh signal according to the logic recited in limitation 6[C]. EX1003, ¶270. Galinski teaches limitation 6[C]. *See* §VII.E.2.c, *supra* (incorporated here). Wong also teaches these limitations. *See* §VII.D.5.c, *supra* (incorporated here).

VIII. DISCRETIONARY DENIAL WOULD BE INAPPROPRIATE

A. Discretionary denial under the *Fintiv* factors is not appropriate

The *Fintiv* factors favor institution. (1) No motion to stay has been filed. (2) The trial date is irrelevant in light of Petitioner’s stipulation below. (3) The copending litigations are in relatively early stages. (4) Petitioner hereby stipulates that if instituted, Petitioner will not pursue in District Court the specific grounds asserted here, or on any other ground that was raised or could have been reasonably raised in this IPR. *See* EX1031, EX1032. For this reason alone, the Board should not discretionarily deny institution in view of the parallel proceedings. *See* Director Vidal, Memorandum, “Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation,” 3 (June 21, 2022). (5) Petitioner’s involvement in the parallel proceeding should not be a basis for denying institution. (6) The merits of this case are compelling for the reasons described above. Accordingly, discretionary denial is inappropriate here.

Further, “[T]he PTAB will not deny institution [] under *Fintiv*... when a petition presents compelling evidence of unpatentability.” June 21, 2022 Director Memo, p. 9. As an example of compelling evidence, Grounds 1 and 2 present anticipation arguments for all independent claims of the ’608 patent, each based on never-before-examined references, Galinski and TI. Further Ground 4 is a single-

reference obviousness ground explaining how the never-before-examined Wong reference discloses or, at a minimum, renders obvious all but two of the Challenged Claims. Grounds 3 and 5 present Galinski in combination with Li, which is §102(a)(1) art not presented to the USPTO, and Wong respectively. Although Li's U.S. counterpart, prior art under §102(a)(2), was submitted in an IDS, it is a separate reference with a much later publication date than Li, and in any case was never cited in a rejection. The Petition therefore presents very compelling reasons of invalidity and should be instituted. Moreover, none of Petitioner's references (Galinski, TI, Wong, Li) were examined by USPTO during prosecution. And, this evidence, "if unrebutted in trial, would plainly lead to a conclusion that one or more claims are unpatentable" and the Board must decline to exercise its discretion under §314(a) to deny institution. June 21, 2022 Director Memo, p. 4; *PopSockets LLC v. Flygrip, Inc.*, IPR2022- 00938, Paper 8 at 9 (P.T.A.B. Nov. 1, 2022).

B. Discretionary denial under 35 U.S.C. § 325(d) is not appropriate

The Board uses a two-part framework to evaluate arguments under 35 U.S.C. § 325(d): "(1) whether the same or substantially the same art previously was presented to the Office or whether the same or substantially the same arguments previously were presented to the Office; and (2) if either condition of the first part of the framework is satisfied, whether the petitioner has demonstrated that the Office

erred in a manner material to the patentability of challenged claims.” *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 8 (PTAB Feb. 13, 2020) (precedential). This framework is assessed under the *Becton, Dickinson* factors. *Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 (PTAB Dec. 15, 2017) (precedential as to § III.C.5, first paragraph).

1. Petitioner does not rely on the same or substantially the same prior art and arguments

Becton, Dickinson factors (a), (b), and (d) each weigh against discretionary denial under the first part of the *Advanced Bionics* framework. Although the U.S. counterpart publication to Li (EX1017) was submitted to the USPTO in an IDS, the Chinese publication (EX1008) was not. Therefore, none of the references used in the petition Grounds were before the USPTO. To the extent submission of the U.S. publication is sufficient, Li was not used in any rejection. “The Board frequently holds that a reference that ‘was neither applied against the claims nor discussed by the Examiner’ does not weigh in favor of exercising the Board’s discretion under § 325(d) to deny a petition.” *Amazon.com, Inc. v. M2M Sols. LLC*, IPR2019-01204, Paper 14 at 16 (PTAB. Jan. 23, 2020); *see also Apotex Inc. v. UCB Biopharma SPRL*, IPR2019-00400, Paper 17 at 25 (PTAB July 15, 2019). In fact, the Challenged

Claims were not rejected at all during prosecution. The remainder of the references were never disclosed nor considered by the Examiner. *See* EX1002, 221.

2. The patent office materially erred in allowing the claims of the '608 patent

To the extent the first Advanced Bionic prong is not dispositive of §325(d) discretionary denial, allowance of the challenged claims was also material error under the second prong of the *Advanced Bionics* framework which warrants against exercise of discretion under *Becton, Dickinson* factors (c), (e), and (f). Specifically, the first action allowance over EX1017 demonstrates the Examiner did not sufficiently locate, evaluate, or appreciate relevant prior art, e.g., prior art teaching pulling the switch node to ground to facilitate recharging of the bootstrap capacitor. As discussed above, Galinski, Wong, and TI—which were not before the Examiner—disclose this missing element of Li, in addition to each reference anticipating or rendering obvious the independent claims separately. *See Samsung*, IPR2023-01157, slip op. at 6-7 (Paper 9) (granting institution where non-cumulative art, which was not before the examiner, taught a missing limitation).

The Examiner was also not presented with the substantial evidence accompanying this Petition. This evidence demonstrates the known desirability and predictability of pulling the switch node to ground to facilitate recharging of the bootstrap capacitor. Nor did the Examiner substantively address similar evidence

that would render Petitioner's evidence cumulative. For example, evidence of motivation to combine and reasonable expectation of success relied upon herein—specifically Galinski (EX1005), TI (EX1006), Wong (EX1007), and the expert declaration of Dr. Holberg (EX1003)—were not of record during prosecution. EX1001, [56] References Cited.

Finally, with respect to Li, there is no evidence in the prosecution history of the extent to which the Examiner considered either the Chinese or the U.S. publication of Li, that the Examiner applied the references against the claims, or that the Examiner considered the particular disclosures of the references presented in a petition. *See Vizio, Inc. v. Nichia Corp.*, IPR2017-00551, Paper 9 at 7-8 (PTAB July 7, 2017).

Petitioner respectfully submits the Board should decline to exercise discretionary denial under § 325(d).

IX. CONCLUSION

Petitioner has established a reasonable likelihood that the Challenged Claims are unpatentable.

Dated: May 17, 2024

Respectfully submitted
By: /s/ Ryan N. Miller
Ryan North Miller
Reg. No. 68,262

**Counsel for Petitioner
Reed Semiconductor Corp.**

PETITIONER MANDATORY NOTICES

Real Party-in-Interest

Pursuant to 37 C.F.R. § 42.8(b)(1), Petitioner certifies that the real party-in interest is Reed Semiconductor Corp.

Nengda Microelectronics (Shenzen) Co., LTD. (“Nengda Microelectronics”) and Nengda Semiconductor Technology (Shenzen) Co., LTD. (“Nengda Semiconductor”) are also named as real parties-in-interest in this Petition. Nengda are defendants in a separate lawsuit brought by Patent Owner, filed as related to the lawsuit against Reed. *See* Related Matters, below. Petitioner does not believe either Nengda party rises to the level of real parties-in-interest as Nengda Semiconductor is non-operational and Nengda Microelectronics has not exercised any control over this Petition or Reed’s decision to file this Petition. However, because Nengda Microelectronics and Nengda Semiconductor agree to be bound by the estoppel provisions of 35 U.S.C. § 315(e), and to prevent a costly challenge by Patent Owner regarding whether these entities are real parties-in-interest, Nengda Microelectronics and Nengda Semiconductor have been named as real parties-in-interest.

Related Matters

Pursuant to 37 C.F.R. § 42.8(b)(2), to the best knowledge of the Petitioner, the ’608 patent is involved in the following cases:

- *Monolithic Power Systems, Inc. v. Reed Semiconductor Corp.*, No. 1:23-cv-01155-JFM (D. Del. filed October 13, 2023)

- *Monolithic Power Systems, Inc. v. Nengda Microelectronics (Shenzhen) Co. LTD. et al.*, No. 1:24-cv-00166-JFM (D. Del. filed February 8, 2024)

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Please address all correspondence to lead and back-up counsel. Petitioner consents to service in this proceeding by email at the addresses above.

Dated: May 17, 2024 By: Respectfully submitted
 /s/ Ryan N. Miller
 Ryan North Miller
 Reg. No. 68,262

Counsel for Petitioner
Reed Semiconductor Corp.

CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. § 42.24(d), Petitioner hereby certifies, in accordance with and in reliance on the word count provided by the word-processing system used to prepare this Petition, that the number of words in this paper is 13,811. Pursuant to 37 C.F.R. § 42.24(a)(1), this word count excludes the table of contents, table of authorities, mandatory notices under § 42.8, certificate of service, certificate of word count, appendix of exhibits, and any claim listing.

Dated: May 17, 2024

/s/ Ryan N. Miller
Ryan N. Miller
Reg. No. 68,262
Counsel for Petitioner
Reed Semiconductor Corp.

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. §§ 42.6(e) and 42.205(b), the undersigned certifies that on the 17th day of May, 2024 a complete and entire copy of this Petition for Post Grant Review and all supporting exhibits was provided via Federal Express to:

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