

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

REED SEMICONDUCTOR CORP.,

Petitioner

v.

MONOLITHIC POWER SYSTEMS, INC.,

Patent Owner

Case No. IPR2024-00871

Patent No. 9,590,608

PATENT OWNER'S PRELIMINARY RESPONSE

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EXHIBIT LIST

Exhibit No.	Description
2001	Declaration of Joseph C. McAlexander III
2002	Joseph C. McAlexander III Curriculum Vitae
2003	MPS Counsel's Identification of Terms in District Court
2004	Microsemi Technical Note, Voltage-Mode, Current-Mode
2005	Micrel Article, Putting Adaptive Constant-ON-Time Buck ICs and Modules to Work
2006	Texas Instruments, Application Report, Adaptive Constant On-Time (D-CAP) Control Study
2007	Evertiq, Application Notes, Part 3: Design considerations of the switching power components
2008	MPS, Article, Advantages of Constant-On-Time Control
2009	Barr Group, Article, How Programmable Logic Works
2010	Sparkfun, Diodes Tutorial
2011	Sparkfun, Transistor Tutorial
2012	ECSTUDIO, Textbooks, Chapter 4, The Transistor as a Switch
2013	ECSTUDIO, Textbooks, Chapter 2, Junction Field-Effect Transistors
2014	Electronics-Tutorials.ws – The Zener Diode
2015	Electronics-Tutorials.ws – Transistor Biasing
2016	Electronical Engineering – Stack Exchange Online Forum re. Usage of a transistor configured as diode

I. INTRODUCTION

Patent Owner Monolithic Power Systems, Inc. (“MPS”) hereby submits its preliminary response to the petition for *inter partes* review against U.S. Patent No. 9,590,608 (the “’608 Patent”).

The Petition relies on three key references for its five grounds:

Ground(s)	Reference	Description
1	TI Datasheet (Petitioner refers to it as “TI”) (EX1006)	Petitioner offers the TI Datasheet for independent claims 1, 11, and 12 under anticipation and/or obviousness.
2, 3, and 5	Galinski (EX1005)	Petitioner offers Galinski for independent claims 1, 11, and 12 under anticipation (ground 2) and obviousness (ground 3). Dependent claims rely on Galinski combined with another reference for ground 3. Ground 5 only focuses on dependent claims.
4	Wong (EX1007)	Petitioner offers Wong for independent claims 1, 11, and 12 (and other dependent claims) under obviousness.

All of Petitioner’s grounds fail to present a reasonable likelihood of success and institution is not warranted.

Ground 1 relies on the TI Datasheet and it fails for several independent reasons.

First, the TI Datasheet fails to teach, or render obvious, the limitations of

1[D]. The claims require that the high side and low side switches are configured to switch on and off when the feedback signal is smaller than the reference voltage signal. The TI Datasheet is a fixed frequency current mode device whose alleged high-side switch is tied to and turned on via the clock, not the feedback signal.

Second, the TI Datasheet fails to disclose or teach the limitations of 1[A], which require “a first comparing module” that compares inputs (a “bootstrap voltage signal” and a “bootstrap refresh threshold”) and outputs a resulting “first comparing signal.” The identified TI Datasheet circuit element has, at most, a “bootstrap voltage signal” as an input and lacks the other claimed input “bootstrap refresh threshold” and lacks the resulting output of the “first comparing signal.” Petitioner acknowledges these deficiencies and attempts to cure them via inherency arguments. The inherency arguments fail because the required claim limitations do not necessarily flow from the TI Datasheet’s teachings.

Third, because Petitioner failed to identify a “first comparing signal” for 1[A], the functionality performed based on that signal for 1[C] (which requires that the “bootstrap refresh module” “decrease[s] the output voltage of the voltage converter” based on the “first comparing signal”) also fails.

Fourth, the Petition fails to properly present an anticipatory ground. The Petition presents the TI Datasheet as anticipating the independent claims but relies extensively on a POSITA’s supposed understanding to fill-in the non-present claim

limitations but does not explain how or why a POSITA would fill-in the missing limitations.

Ground 1 thusly fails.

Grounds 2, 3, and 5 rely on Galinski, but Galinski does not anticipate or render obvious the independent claims for several reasons. First, the functionality Petitioner identifies for 1[D] is unrelated to the claim requirement of “control the [switches] ... based on the difference signal so as to charge the bootstrap capacitor.” Petitioner identifies circuitry relating to voltage regulation based on feedback to teach 1[D], but this circuitry is effectively disabled during a bootstrap capacitor refresh, *i.e.*, it cannot charge it. Second, Galinski does not teach a “bootstrap refresh threshold” as required by 1[A]. Instead, Petitioner identifies, as the claimed “bootstrap refresh threshold” of 1[A], Galinski’s switching output voltage that drives its output voltage, V_{OUT} . A converter’s output voltage is not a “bootstrap refresh threshold.” Grounds 2, 3, and 5 thusly fail.

Petitioner’s Ground 4 relies on its replacement of a Zener diode of Wong with a switch. This fails for two reasons: (1) Petitioner fails to describe how that switch would be controlled, leaving the limitations relating to its control (1[PRE] and 1[D]) untaught; and (2) a POSITA would not have replaced a Zener diode in Wong’s circuits with a switch because the Zener diode exists in the circuit to provide a functionality that the switch does not provide. Namely, provide a stable

output voltage.

Further, non-institution is warranted because Petitioner and its expert make conclusory statements about the prior art to supply missing limitations, but neither Petitioner nor its expert support those conclusions with evidence.

Finally, non-institution is also warranted due to Petitioner's numerous faulty grounds (described above) that have large gaps in identifying the required claim limitations in the prior art. Petitioner attempts to cure deficiencies based on a conclusory and insufficient analysis relying on impermissible hindsight reconstruction. Due to the large number of gaps in Petitioner's analysis, non-institution is warranted.

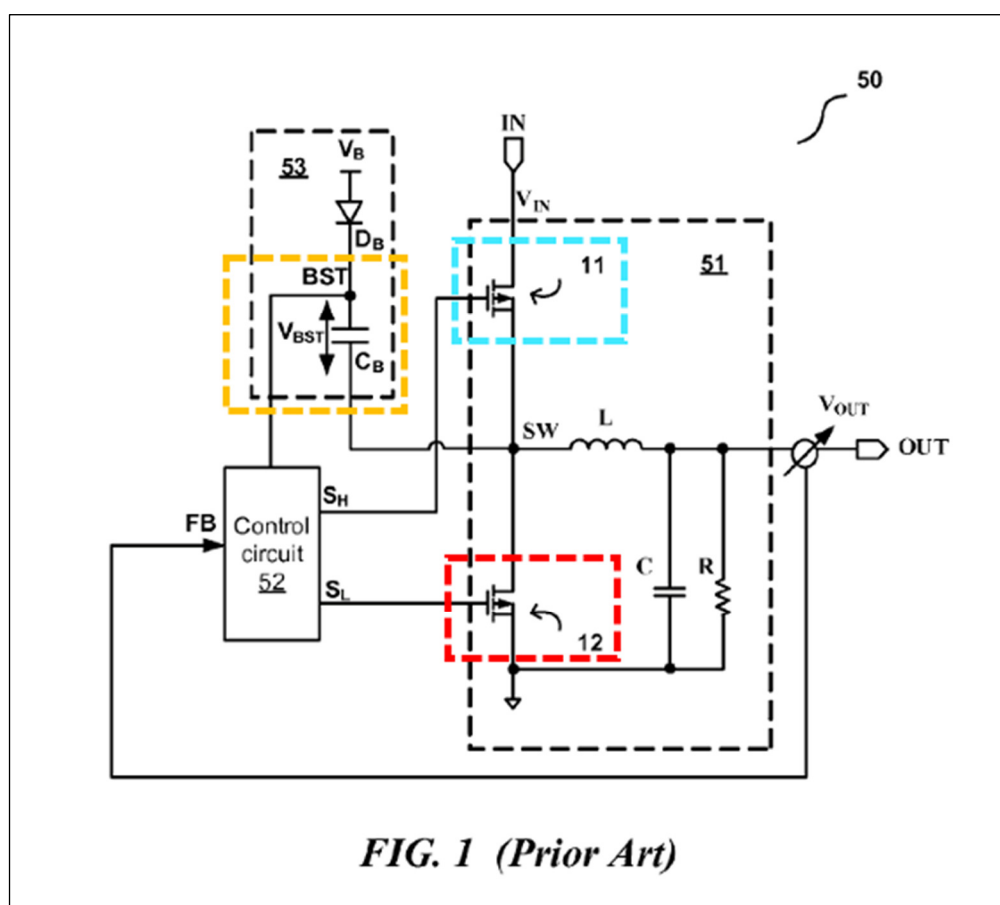
The '608 Patent and Petitioner's failures to present a reasonable likelihood of success are described below.

II. Overview of the '608 Patent and Its Related Technology

The '608 Patent improves upon operational problems in switch-mode voltage converters that rely on a bootstrap capacitor. (EX1001 at 1:14-17, 3:37-42; EX2001 at ¶¶ 34-37.)

The basic structure of a prior art switch-mode voltage converter is illustrated in Figure 1. As shown below, switch-mode converters use a high side switch (blue) and a low side switch (red). (EX1001 at 1:30-31; EX2001 at ¶ 34.) The high side switch is turned on or off to regulate the conversion of voltage from the input

voltage (V_{IN}) to SW and then to the output voltage (V_{OUT}), *e.g.*, down-stepping a V_{IN} of 3.3V to a V_{OUT} of 2.7V. (EX2001 at ¶¶ 34.) The bootstrap capacitor (orange) provides additional voltage at the BST node equal to the initial BST voltage plus V_{IN} . (EX1001 at 2:12-22.) The bootstrap capacitor is refreshed via the low side switch (described in more detail in the following paragraphs). (EX1001 at 2:45-59.)



More specifically, the high side switch needs a “driver” (not shown in Figure 1) to turn the high side switch on. (EX1001, 1:61-63; EX2001 at ¶ 35.) That driver must receive a voltage higher than the input voltage to turn the high side switch on

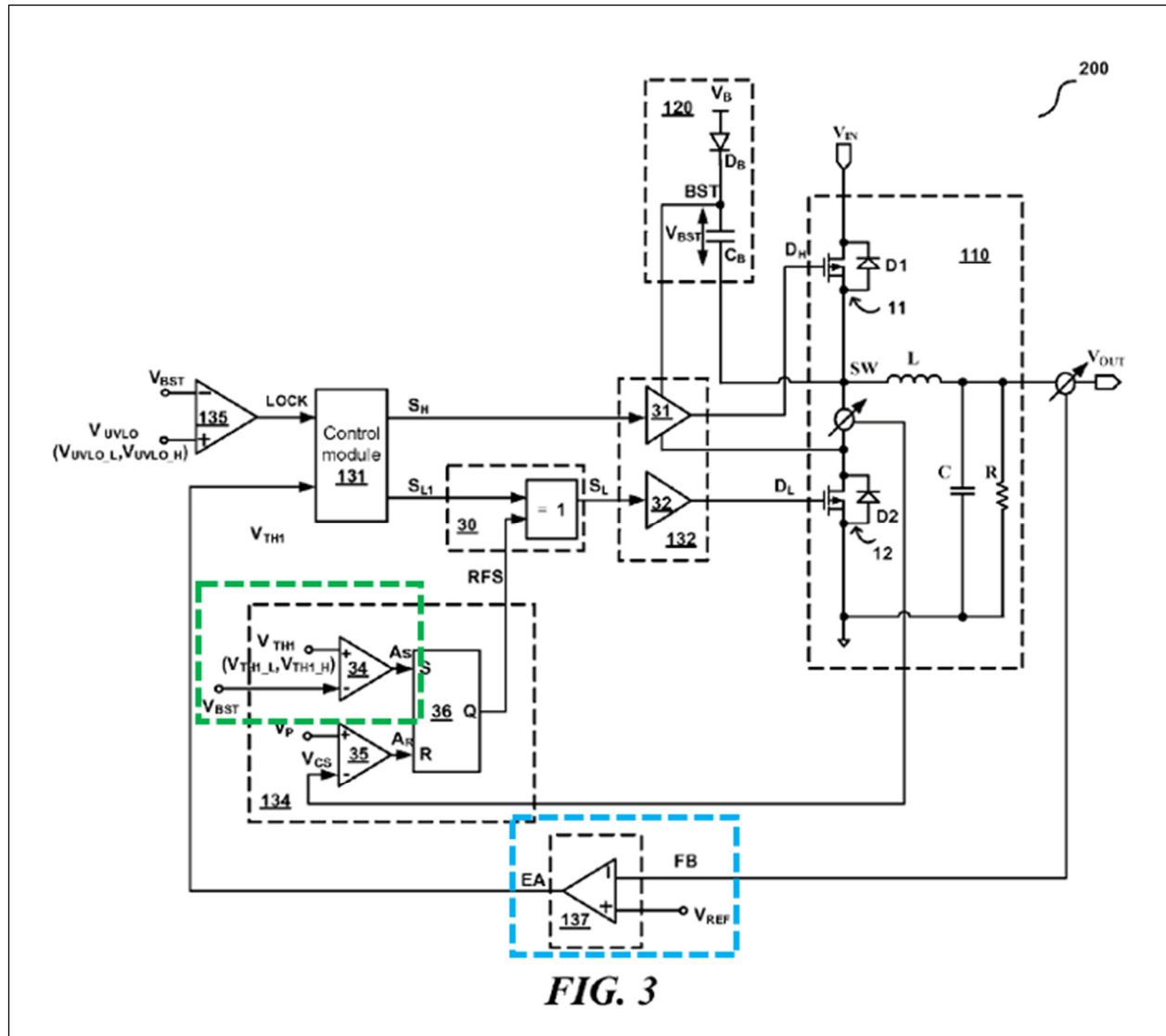
completely. (EX1001 at 1:65–2:22; EX2001 at ¶ 35.) Thus, a “bootstrap capacitor” (C_B) that stores a higher voltage is coupled to the high side switch’s driver so that the driver is able to drive the high side switch on completely. (EX1001 at 2:45-59; EX2001 at ¶¶ 35-36.)

The bootstrap capacitor needs to be refreshed periodically and this is done via the low side switch. When the high side switch is driven (*e.g.*, turned on), the bootstrap voltage is used to enhance “the driving capability of the first control signal (SH) provide to the gate of the high side switch 11, so that the first control signal (SH) can drive the high side switch 11...”. (EX1001 at 2:15-22, 2:45-49; EX2001 at ¶ 36.) The bootstrap capacitor needs to be periodically recharged. (EX1001 at 2:55-59, 2:35-40; EX2001 at ¶ 36.) The bootstrap capacitor is recharged when the high side switch is off and the low side switch is on for a period of time that is long enough to refresh the bootstrap capacitor. (EX1001 at 2:55-59, 2:35-40, 2:55-59; EX2001 at ¶ 36.)

The general switch-mode voltage converter described above has problems, such as an inadequate low side switch on-time which results in an insufficient recharge of the bootstrap capacitor. (EX1001 at 3:3-18; EX2001, ¶ 37.) The ’608 Patent remedies this problem; it controls how its switches are operated via: (1) a first comparing module (Fig. 3 below, green) that compares a *bootstrap voltage signal* (V_{BST}) to a refresh threshold (*bootstrap refresh threshold* (V_{TH1})) (EX1001

at 19:10-20, 9:10-20, 10:60-63, 11:1-6, 12:15-29) and (2) a voltage difference module Fig. 3 below, blue) that compares the output signal V_{out} (*i.e.*, *feedback signal* (FB)) with a *reference voltage* (V_{REF}) that represents the voltage converter's desired output. (EX1001 at 7:16-27, 8:31-33, 10:60-63, 11:16-17, 13:9-11; EX2001 at ¶ 38.)

These two modules work to control, and maintain, the output voltage (V_{OUT}) to ensure proper capacitor recharge. (EX2001 at ¶¶ 39-44.) Via the first comparing module, when V_{BST} is lower than V_{TH1} , V_{out} is decreased. (EX1001 at 19:39-41, 8:26-30, 8:58-9:2, 9:42-49, 12:6-9, 14:47-49; *see also* EX2001 at ¶¶ 40-41 (Mr. McAlexander explaining in further detail).) Via the voltage difference module, when FB is smaller than V_{REF} , the high side switch and low side switch are switched on and off to maintain V_{out} . (EX1001 at 8:34-40, 11:18-23; *see also* EX2001 at 42-44 (Mr. McAlexander explaining in further detail).) As a result, when FB is smaller than V_{REF} (the difference signal indicates that V_{OUT} is too low), the high side switch and low side switch are switched on and off so as to charge the bootstrap capacitor for refreshing the bootstrap voltage signal.

**FIG. 3**

III. Level Of Ordinary Skill in The Art

A person of ordinary skill in the art (“POSITA”) in the field of the ’608 Patent, as of its priority date of August 11, 2014, would have had a bachelor’s degree in Electric Engineering or equivalent, and approximately two years of experience working in the field of power converters, circuit design, device physics, or related technologies. Lack of work experience can be remedied by additional education, and vice versa. (EX2001 at ¶ 32.)

IV. Claim Construction

The Board construes claims in accordance with their ordinary and customary meaning as understood by one of ordinary skill in the art. 37 C.F.R. § 42.100; *see also Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005). At this preliminary stage, and because the deficiencies of the Petition can be addressed absent construction, Patent Owner presents no constructions at this time. Patent Owner reserves the right to present constructions with the Patent Owner Response should the Board institute the Petition.

For the sole purposes of disclosure to the Board, Patent Owner has identified terms for construction in the parties' parallel district court proceeding: *Monolithic Power Systems, Inc. v. Reed Semiconductor Corp.*, Monolithic Power Systems, Inc. v. Reed Semiconductor Corp., C.A. No. 23-1155-JFM (D. Del.). (EX2003.) No constructions were exchanged, and the identification of terms was preliminary. Patent Owner submits that these terms need not be construed for purposes of this Preliminary Response and reserves its right to address these or additional claims terms if needed if the Petition is instituted.

V. The Grounds Do Not Provide a Reasonable Likelihood of Unpatentability for Any Claim

A. Ground 1: the TI Datasheet does not anticipate or render any claim obvious.

Ground 1 fails for several independent reasons.

First, the TI Datasheet fails to teach or render obvious the limitations of

1[D]. The claim requires that the high side and low side switches are configured to switch on and off when the feedback signal is smaller than the reference voltage signal. The TI Datasheet is a fixed frequency current mode device whose alleged high-side switch is tied to, and turned on via, the clock. This is dissimilar to the claim requirements which turn on the high-side switch using feedback.

Second, the TI Datasheet fails to teach—or render obvious—the limitations of 1[A], which require a “a first comparing module” that compares inputs (a “bootstrap voltage signal” and a “bootstrap refresh threshold”) and outputs a resulting “first comparing signal.” The Petition lacks sufficient analysis and support, leaving limitations and obviousness combinations vague and failing to demonstrate the requisite clarity required by 35 U.S.C. § 312(a)(3) and 37 C.F.R. § 42.104(b)(5). Moreover, the Petition fails to demonstrate that these limitations are met, because the identified circuit element has, at most, a “bootstrap voltage signal” as an input and lacks the other claimed input “bootstrap refresh threshold” and lacks the resulting output of the “first comparing signal.” Petitioner acknowledges these deficiencies and attempts to cure them via inherency arguments. The inherency arguments fail because the required claim limitations do not necessarily flow from the TI Datasheet’s teachings.

Third, the TI Datasheet fails to teach—or render obvious—the limitations of 1[C] which requires that the “bootstrap refresh module” “decrease[s] the output

voltage of the voltage converter” based on the “first comparing signal.” Because Petitioner failed to identify a “first comparing signal,” the functionality performed based on that signal fails.

Fourth, the Petition fails to properly present an anticipatory ground. The Petition presents the TI Datasheet as anticipating the independent claims but relies extensively on a POSITA’s supposed understanding to fill-in the non-present claim limitations. And, to support its inherency arguments, Petitioner repeatedly concludes that a “POSITA would understand” that certain limitations are met without offering supporting evidence or reasons why that would be true. Petitioner alternatively presents Ground 1 as obvious but does not describe how those above-described limitations would have been obvious.

Ground 1, which states that claims 1, 11, and 12 are anticipated or rendered obvious by the TI Datasheet, fails. This is described in more detail below.

1. Ground 1: the TI Datasheet does not anticipate/render obvious the limitations of 1[D].

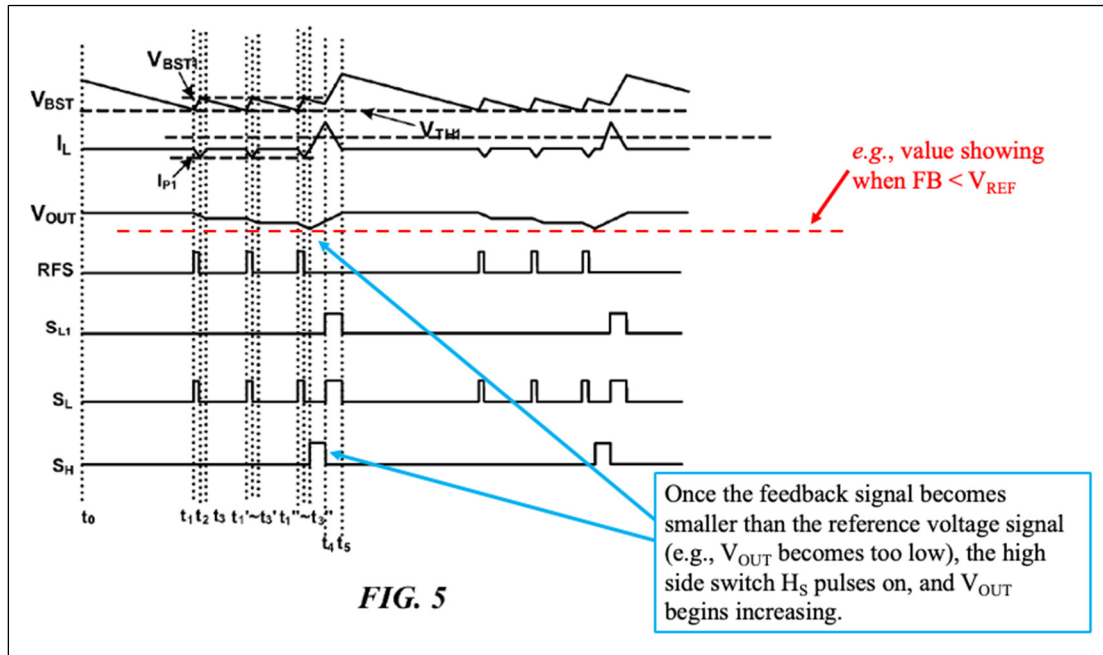
The claims require that the high side and low side switches are configured to switch on and off when the feedback signal is smaller than the reference voltage signal. (Claim limitations 1[D], 11[F], and 12[E]¹ (“when the feedback signal is

¹ Claim limitation 12[E] is worded differently, but Petitioner treats 12[E] as

smaller than the reference voltage signal, the bootstrap refresh control circuit is configured to control the high side switch and the low side switch to switch on and off based on the difference signal.”)

As an example of the high side switch, Figure 5 of the '608 Patent (reproduced and annotated below) illustrates feedback voltage FB (*i.e.*, output voltage V_{OUT}) decreasing less than a reference threshold voltage V_{REF} (EX1001 at 15:52-57) which triggers the high-side switch (S_H) high and the low-side switch (S_L) low. (EX2001 at ¶52-54.)

mirroring the limitations of 1[D] and 11[F]. Instead of reciting that the switching of the high and low switches occurs “when the feedback signal is smaller than the reference voltage signal,” limitation 12[E] recites that the switching occurs “when the output voltage of the voltage converter is decreased.” While Petitioner does not construe what “decreased” means, Petitioner treats all three limitations as the same, meaning that “decreased” means when an output voltage is below a certain threshold. Thus, all three claim limitations occur based on a voltage change, and, for purposes of this response, Patent Owner’s arguments apply to 12[E] like the other limitations because Petitioner treats these limitations as the same. (*See also* EX2001 at ¶51.)



The TI Datasheet does not teach a high side switch that is triggered on via the difference signal. (EX2001 at ¶54.) Instead, the alleged high side switch is controlled to be turned on during a clock cycle (and not controlled via a threshold). Ground 1 accordingly fails to show element 1[D], “when the feedback signal is smaller than the reference voltage signal, the bootstrap refresh control circuit is configured to control the high side switch and the low side switch to switch on and off based on the difference signal.”

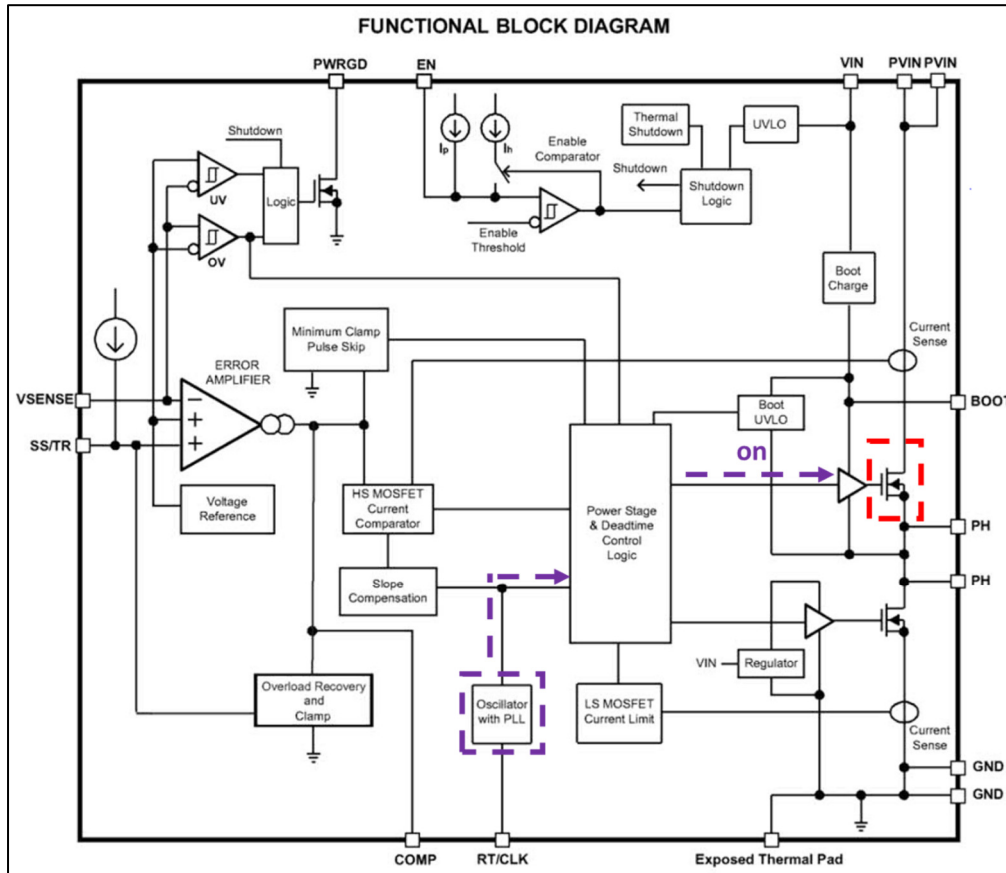
This failure of the TI Datasheet, and the relevant control schemes demonstrating that this failure is significant, are described in more detail below.

a. Ground 1: the TI Datasheet fails to teach 1[D].

The TI Datasheet’s output current control does not meet the claimed turning on and off of the high side switch when the feedback signal is smaller than the

reference voltage, based on the difference signal, as required by 1[D]. (*See* 1[D] (“when the feedback signal is smaller than the reference voltage signal, the bootstrap refresh control circuit is configured to control the high side switch and the low side switch to switch on and off based on the difference signal”).) This is because the high-side switch is turned on by an oscillator in the TI Datasheet (not “when the feedback signal is smaller than the reference voltage signal” and, moreover, there is no “control [of] the high side switch ... to switch on ... based on the difference signal”). (EX2001 at ¶55.) Thus, Ground 1 fails for the below independent reasons.

The TI Datasheet “uses a fixed frequency, peak current mode control” scheme where the alleged **high side switch** (annotated below) is turned **on** via an **oscillator** (*e.g.*, it produces a period signal). (EX1011 at 11 (“An internal oscillator initiates the turn on of the high-side power switch”).) This is a fixed-frequency PWM control scheme (EX1006 at 11; EX2001 at ¶55; *see below* § V.A.1.b) that directly controls turning on the high-side switch via a clock cycle. (EX1006 at 11 (“An internal oscillator initiates the turn on of the high-side power switch”).) As such, because the oscillator directly controls the high-side switch to turn on, limitation 1[D]’s requirements of “control the high side switch ... to switch on ... based on the difference signal” “when the feedback signal is smaller than the reference voltage signal” is not taught. (EX2001, ¶55.)



Furthermore, the Petition’s conclusory analysis is deficient. The TI Datasheet’s teaching of “a fixed frequency, peak current mode control” scheme precludes 1[D] from being taught (described in more detail in § V.A.1.b).

Petitioner and its expert never reconcile how this mode—which ties the high side switch’s on-stage to an oscillator’s on-stage—can meet 1[D]. (EX2001, ¶56.)

Instead, Petitioner and its expert broadly argue that TI’s high side and low side switches are controlled; and because this would include a scenario where the feedback signal is less than the reference voltage, Petitioner and its expert argue that TI anticipates limitation 1[D]:

Furthermore, TI discloses the output of the disclosed error amplifier connected to Power Stage Logic (indirectly, through the HS Current Comparator), and that the Power Stage Logic provides control signals for controlling the high-side and low-side switches. Therefore, a POSITA would understand that TI's disclosed Power Stage Logic switches on and off the high-side and low-side switches based on the output of the error amplifier, thus charging the bootstrap capacitor. A POSITA would also understand that this would include when the feedback signal is less than the reference voltage, as described above. Therefore, TI anticipates limitation 1[D].

(Pet. at 31 (citations omitted).)

Petitioner's expert offers no better detail. (EX2001, ¶57.) Ignoring the TI Datasheet's explicit disclosure that the high side switch is turned on every clock cycle, he argues that the switches are turned on and off in multiple modes "including when the feedback signal is less than the reference voltage." (EX1003 at ¶ 133.) But the claims recite a different trigger—that *when the feedback signal becomes less than the reference voltage*, the high side switch is turned on. (See 1[D]; EX2001 at ¶57.) Petitioner and its expert never grapple with this triggering event for the high side switch, and instead, rearrange the claim limitation as separate unrelated requirements that can be individually taught by the TI Datasheet. Petitioner's (and its expert's) distortion of the claim elements—and conclusory analysis—do not teach the claims.

Ground 1 accordingly fails to present a reasonable likelihood of success for element 1[D] at least for this reason.

Provided below is further detail regarding why the TI Datasheet's "fixed

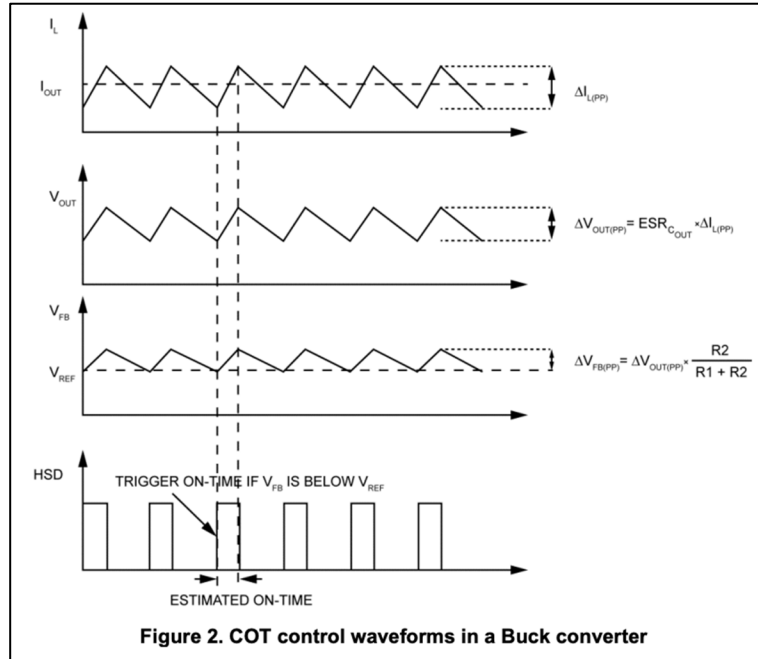
frequency current mode control” is markedly dissimilar from the control methodology described by 1[D].

b. Claim 1[D] describes a distinctly different control scheme than the TI Datasheet.

Claim 1[D] and the TI Datasheet described distinctly different control types. As described above, 1[D] requires that the high side switch is turned on during a triggering event: “when the feedback signal is smaller than the reference voltage signal.” The fact that the high side switch is turned on by this triggering event would inform a POSITA that the ’608 Patent is not a “fixed frequency current mode control” described by the TI Datasheet. (*See, e.g.*, EX2002 at ¶¶60-76; EX1001 at 13:64-14:55). Instead, 1[D] covers a control mode such as a COT control mode or equivalent. (*See, e.g.*, EX1001 at 7:37-44; EX2001 at ¶¶60-76.) These topologies are substantively different and provide further context for why 1[D] is not taught. (*See* § V.A.1.b below.)

The fixed frequency current mode control mode—such as the one described by the TI Datasheet—uses a clock to turn the high side switch ON every clock cycle. (EX1006, 11; EX2001 at ¶¶61-69; *see also* EX2004 at 2 (showing another fixed-frequency mode, voltage mode).) In contrast, Constant On-Time (“COT”) control turns the high side switch ON based on feedback; this responds faster to changes in the converter’s load. (*See* EX2001 at ¶¶70-74.) In COT control, when the voltage feedback V_{FB} falls below a reference voltage V_{REF} , the high side switch

(also referred to as an active switch) is turned ON. (EX2001, ¶ 71; EX2005, 2; EX2006, 2 (Fig. 3) (“Ton is triggered when Vo declines to Vref level).)

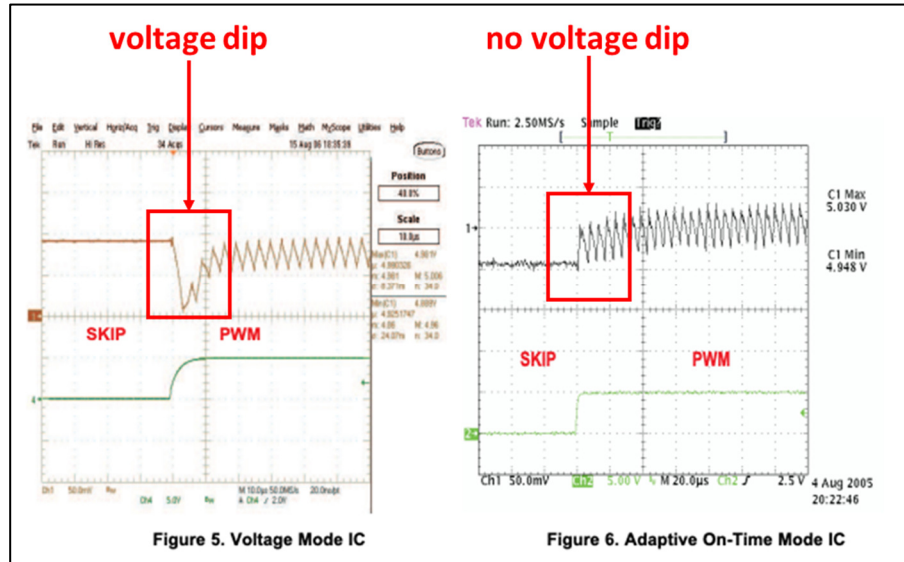


The fixed switching frequency current mode switching the high side switch based on the clock impedes the converter’s response time to load demand.

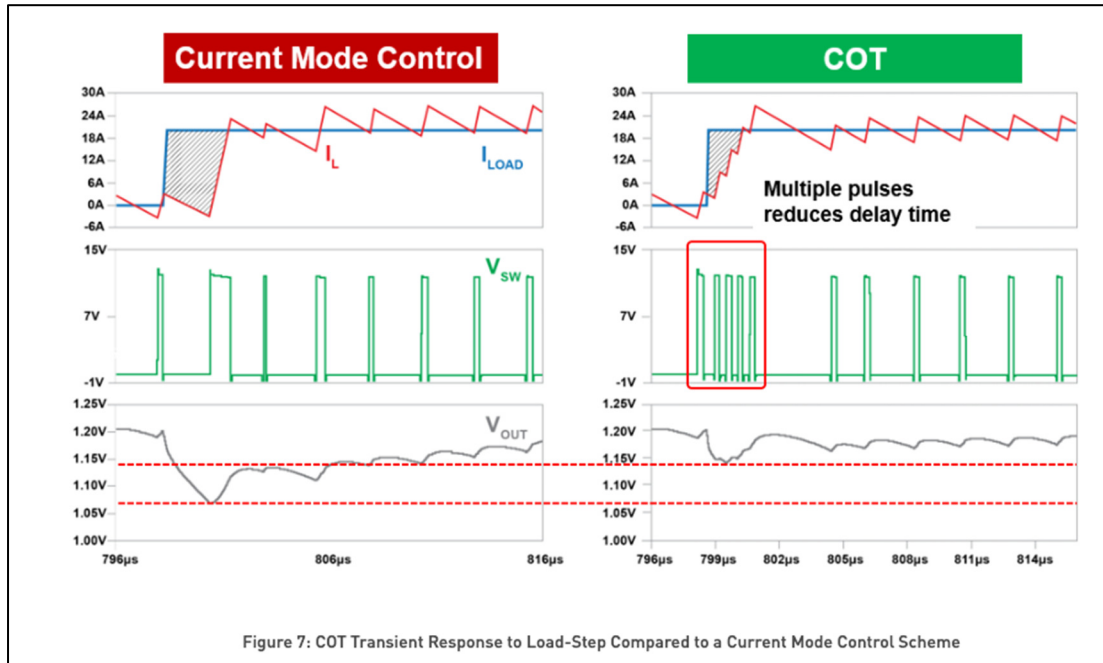
(EX2001 at ¶70.) For example, if the load changes right after the high side switch is turned off, the converter must wait an entire clock cycle to respond to the changed load to turn the switch on. (EX2007 at 5.) The COT control scheme responds directly to load conditions. (EX2001 at ¶71.) As such, these two schemes are dissimilar.

Moreover, COT control provides benefits over fixed frequency current mode control schemes (*i.e.*, 1[D] provides a benefit over the TI Datasheet). For example, COT control can respond faster to transient changes. (EX2001 at ¶72-73.) As

shown in the reproduced Figures 5 and 6 below taken from EX2008 at 3, the voltage mode control scheme of Figure 5 has a large voltage dip when moving from a light load to a heavy load, whereas the COT scheme in Figure 6 responds faster and does not have a voltage dip.



See also EX2008 at 4 (Figure 7 reproduced below illustrating that COT responds faster to load changes than current mode control). (EX2001, ¶ 73.)



As illustrated above, the COT control scheme is dissimilar to the fixed frequency current control mode that is taught by the TI Datasheet because the fixed frequency mode controls on-time via clock and the COT scheme controls on-time via feedback. (EX2001 at ¶75.) As such, the TI Datasheet is a fixed frequency control mode that fails to teach a triggering event to turn on the high side switch as required by 1[D], which would encompass a COT control scheme and equivalents.

2. Ground 1: the TI Datasheet does not anticipate/render obvious the limitations of 1[A].

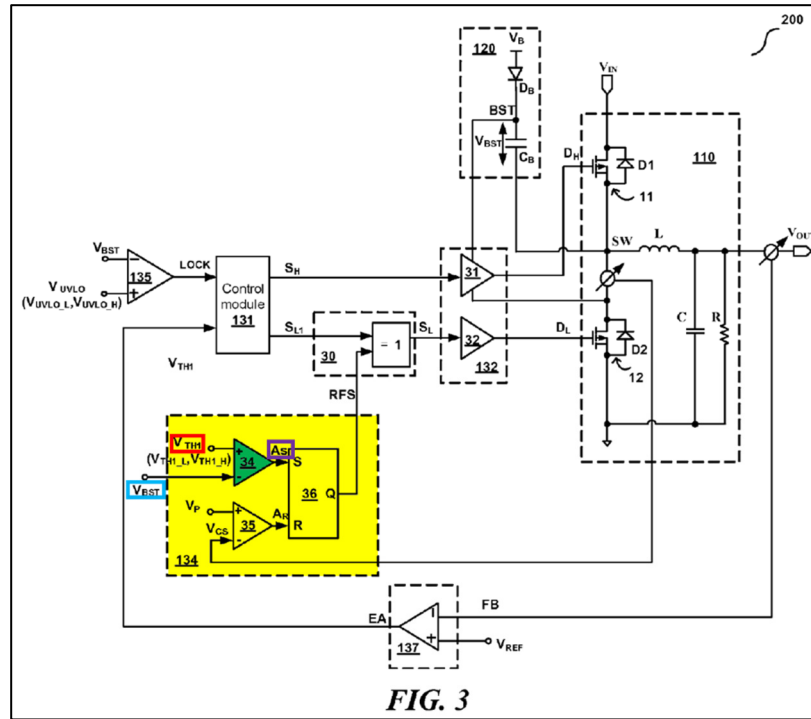
Claim 1[A]² requires a “bootstrap refresh control circuit” that has a

² Claims 11 and 12 have substantively similar limitations. (EX1001, 23:20-39, 24:5-16.)

“bootstrap refresh module” that comprises “a first comparing module” that compares inputs (a “bootstrap voltage signal” and a “bootstrap refresh threshold”) and outputs a resulting “first comparing signal.” (’608 Patent at 19:9-26.) The TI Datasheet does not teach or suggest these claim limitations and, more specifically, lacks the “first comparing module” and its respective signals (“bootstrap voltage signal,” “bootstrap refresh threshold,” and “first comparing signal”). (EX2001 at ¶¶79-81.)

Figure 3 of the ’608 Patent is provided below to provide further context. It illustrates a bootstrap refresh module 134 (yellow)³ that has a first comparing module (comparator 34, green) that receives as its inputs—and compares—a bootstrap voltage signal (V_{BST}) (blue) to a refresh threshold (*bootstrap refresh threshold* (V_{TH1})) (red) and outputs a comparing signal (signal A_S) (purple) based on that comparison. (EX1001 at 19:10-20, 9:10-20, 10:60-63, 11:1-6, 12:15-29; EX2001 at ¶¶79-81.)

³ The “bootstrap refresh control circuit” comprises “a control module 131, a drive module 132, a voltage difference module 137, a bootstrap refresh module 134 and an under voltage lock out module 135.” (’608 Patent at 10:56-60.)



As described below, Petitioner has failed to present a reasonable likelihood of success because the Petition: (i) fails to present the requisite clarity and specificity required by 35 U.S.C. § 312(a)(3) and 37 C.F.R. § 42.104(b)(5) and (ii) fails to demonstrate that the TI Datasheet anticipates—or renders obvious—the claimed “first comparing module” and its respective three signals.

(i) The Petition fails to present the requisite clarity for 1[A] and should be denied.

As a threshold issue, Petitioner’s Ground 1 fails because it fails to address these limitations with the requisite particularity. A Petitioner must identify its grounds with particularity (35 U.S.C. § 312(a)(3)) and “specify where each element of the claim is found in the prior art” (37 C.F.R. § 42.104(b)(5)). Petitioner’s analysis fails as a threshold issue.

The TI Datasheet was presented as the singular reference, but the Petition is vague, and conclusory, regarding exactly where in the TI Datasheet the separate 1[A] limitation of (1) “bootstrap refresh control circuit,” and separate 1[A] limitations of (2) “bootstrap refresh module,” (3) “first comparing module,” and (4) the signals of the “first comparing module” are met, requiring significant effort by Patent Owner, and the Board, to decipher a mapping. (*Compare* 1[PRE] and 1[A] *with* 1[A] analysis at Pet. 27-28. See EX2001 at ¶ 82.) Petitioner is required to make its mapping clear and cannot simply leave it to the Board to decipher. 37 C.F.R. § 42.104(b)((5) (stating that a petition must set forth “[t]he exhibit number of the supporting evidence relied upon to support the challenge and the relevance of the evidence to the challenge raised, *including identifying specific portions of the evidence that support the challenge*” (emphasis added)); *see Netflix, Inc. v. DivX, LLC*, 84 F.4th 1371, 1377 (Fed. Cir. 2023) (“[T]he Board should also not have to decode a petition to locate additional arguments beyond the ones clearly made. A petitioner may not rely on a vague, generic, and/or meandering petition and later fault the Board for failing to understand what the petition really meant. Ultimately, it is the petitioner’s burden to present a clear argument.”) (citations omitted).

After an attempt at deciphering, the Petition does appear to vaguely identify the Boot UVLO and Power Stage logic to meet limitations (1) and (2), Boot UVLO

to meet limitation (3), and limitation (4) appears to be allegedly met via the inputs/outputs of Boot UVLO. (Pet. at 25-28 (analyzing 1[PRE] and 1[A]); EX2001 at ¶ 83.) But this identification is insufficient because Petitioner must be clear in its Petition and the Board and Patent Owner should not have to decipher Petitioner's arguments. As a consequence, the Petition fails at a threshold level and should be denied.

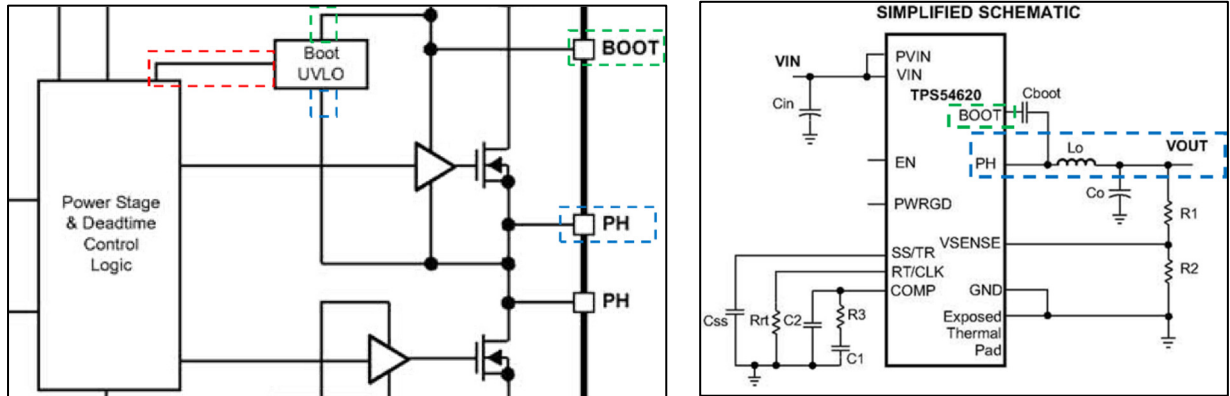
(ii) The Petition fails to demonstrate that the TI Datasheet anticipates/renders obvious 1[A].

Beyond failing at a threshold level, the Petition fails to demonstrate that the TI Datasheet anticipates/renders obvious 1[A].

The limitations of 1[A] (the claimed “first comparing module” and its signal limitations, *e.g.*, “bootstrap voltage signal,” “bootstrap refresh threshold,” and “first comparing signal”) are not shown, not described, and not taught by the TI Datasheet. (EX2001 at ¶¶ 84-92.) While Petitioner appears to identify Boot ULVO as the claimed “first comparing module,” it proclaims (without evidence) that Boot ULVO satisfies the three separate signals. (Pet. at 27-28.) Petitioner's conclusory analysis fails because the TI Datasheet's Boot ULVO does not teach these limitations.

Shown below, Boot ULVO has, as its signals, an undescribed signal (annotated red), BOOT (green), and PH (blue). BOOT is an external capacitor voltage and PH is a switch node (EX1006 at 6) tied to V_{OUT} and is tied to the

capacitor's other terminal (*id.* at 2). (EX2001 at ¶¶86.) Functionally, Boot UVLO monitors the voltage across the boot capacitor to have the device operate at 100% duty cycle. (EX1006 at 11; EX2001 at ¶¶87.)



There is a mismatch between Boot UVLO and 1[A]. Boot UVLO's signals, collectively, do not match the claimed inputs ("bootstrap voltage signal" and "bootstrap refresh threshold") because Boot UVLO's inputs are simply the boot capacitor's terminal (BOOT) and V_{OUT} (*e.g.*, PH). (EX2001 at ¶¶88-92.) While BOOT is akin to the claimed "bootstrap voltage signal," there is no "bootstrap refresh threshold" input to Boot UVLO. Further, the comparison requirement between the two inputs is not met, because the TI Datasheet shows that Boot UVLO uses its inputs to monitor the voltage across the boot capacitor (*i.e.*, the boot capacitor's terminal and V_{OUT} together provide a voltage potential). (EX1006 at 11.) Nor does Boot UVLO's other signal (red) match the claimed output ("first comparing signal") because the red signal is wholly undescribed. (EX2001 at ¶¶88-92.) Indeed, Petitioner does not appear to even make an effort to map Boot UVLO

and its signals to 1[A]. As such, the claimed “first comparing module” and its three signal are not taught by Boot UVLO.

Acknowledging the deficiencies of the TI Datasheet and Boot UVLO’s literal teachings, the Petition provides a single conclusory sentence arguing that the limitations of 1[A] are inherent. (Pet. at 27 (“A POSITA would understand from this disclosure that a comparator input receiving the threshold voltage is necessarily present, notwithstanding the simplicity of TI’s high level block diagrams”).) This conclusory analysis, even if accepted as correct, fails to describe how the claimed signals would necessarily exist and be connected within the Boot UVLO to arrive at limitation 1[A]. (*See also* EX2001 at ¶¶93.) Because the Petition fails to provide the requisite analysis to support institution, it fails to present a reasonable likelihood of success. Ground 1 should be denied for at least this reason.

Moreover, Ground 1 should be denied because the Petition’s inherency arguments fail as a legal matter. To arrive at the “first comparing module” and its three signals, the Petition argues that a comparator is inherent within Boot UVLO, and the comparator must inherently be wired to provide the claimed signals. However, for a limitation to be inherent, it must necessarily exist within the prior art reference and cannot be there as a mere possibility. *PAR Pharm., Inc. v. TWI Pharm., Inc.*, 773 F.3d 1186, 1195 (Fed. Cir. 2014). (“Inherency ... may not be

established by probabilities or possibilities.”) “The mere fact that a certain thing *may* result from a given set of circumstances is not sufficient.” *Id.* (emphasis added). Rather, a party must “show that *the natural result flowing* from the operation as taught would result in the performance of the questioned function.” *Id.* (emphasis in original); *Toshiba Corp. v. Optical Devices, LLC*, IPR2014-01446, Paper 31, 21-23 (March 9, 2016) (finding petitioner failed to prove the prior art inherently disclosed claimed limitations where expert did not provide explanation of why it was true, explained that the prior art “was probably using” a device according to the limitation, and patent owner presented a rebuttal that the prior art could use other implementations for that function).

A comparator—along with the specifically claimed inputs/outputs of 1[A]—is not necessarily present in Boot UVLO. (EX2001 at ¶¶93-94.) The TI Datasheet does not state that it uses Boot UVLO to compare two specific signals (a “bootstrap voltage signal” and a “bootstrap refresh threshold”) to output a result of that comparison.

Petitioner’s citations to the TI Datasheet does not lead to the conclusion that a comparator is necessarily present. The only physical signal provided is the “bootstrap voltage signal,” and any determination that it is higher than a threshold can be done in other ways not involving comparison to a threshold. It can be done programmatically to ensure a 100% duty cycle, *e.g.*, by providing the “bootstrap

voltage signal” into a programmable logic device. (EX2001 at ¶¶94.) Furthermore, Boot UVLO can be designed so that it has a diode biased via the alleged bootstrap voltage signal; this is not the comparator that Petitioner argues is necessarily present. (EX2001 at ¶¶94-95.) These are just two examples, but the fact that circuits other than a comparator exist demonstrates that a comparator with specific wirings does not necessarily flow from the teaching of Boot UVLO. (EX2001 at ¶¶95-96.) *HTC Corp. v. Cellular Commc’ns Equip., LLC*, 877 F.3d 1361, 1369 (Fed. Cir. 2017) (affirming finding of no inherency because, while the prior art *may* have disclosed a frame that was the start of a message transmission, that did not mean the reference *necessarily* disclosed a start of a message transmission); *PersonalWeb Techs., LLC v. Apple, Inc.*, 917 F.3d 1376, 1382-83 (Fed. Cir. 2019) (reversing finding of inherency in IPR because, while the system *may* have used a lookup table, another equally plausible result was that the system used a conventional file system to locate files). Because the comparator (and the claimed inputs/outputs) do not necessarily result from the teachings of Boot UVLO, Petitioner’s inherency arguments fail.

To make matters worse, Petitioner’s expert does not offer supporting rationale. Instead, he describes comparators as a type of device and then states in a conclusory statement that, in his opinion, a comparator would exist. (EX1003 at ¶¶49-56, 126; EX2001 at ¶¶95.) Nothing in the Petition or the expert declaration arrive

at the conclusion that the limitations of 1[A] are necessarily present.

Finally, Ground 1 was presented as anticipation/obviousness. Petitioner does not provide any obviousness rationale to cure the above deficiencies, and instead merely proclaims 1[A] is obvious in view of a POSITA's knowledge. (Pet. at 28; EX2001 at ¶¶97.) Petitioner does not describe why a POSITA would have been motivated to include a comparator, and why a POSITA would have been motivated to provide a comparator with the claimed inputs/outputs. Petitioner's obviousness analysis does not save the TI Datasheet's lack of disclosure of 1[A].

For the above reasons, the Petition fails to demonstrate that the limitations of 1[A] are anticipated or rendered obvious by the TI Datasheet. Ground 1 thusly fails to present a reasonable likelihood of success and denial of the petition is warranted.

3. Ground 1: the TI Datasheet does not anticipate/render obvious the limitations of 1[C].

Limitation 1[C] requires that the “bootstrap refresh module” “decrease[s] the output voltage of the voltage converter” based on the “first comparing signal.” However, as described immediately above, the Petition fails to demonstrate that the TI Datasheet teaches the “first comparing module” and its output, the “first comparing signal.” As such, because the “first comparing signal” is absent, 1[C] is not taught.

The TI Datasheet's failure to teach the “first comparing module” and its

output, the “first comparing signal,” is evident in Petitioner’s analysis of 1[C].

There, Petitioner, in pure conclusory fashion, proclaims that the “first comparing signal” exists. (Pet. at 29 (“The output of TI’s bootstrap-monitor circuit (i.e., the first comparing signal) is connected to the Power Stage Logic, which is configured to provide control signals for driving the high-side and low-side switches”); EX2001 at ¶101.) For 1[C], however, there is no tie between any actual signal described in the TI Datasheet, and the comparator that Petitioner claimed was inherently present in 1[A], to satisfy the claimed “first comparing signal” limitation. Petitioner cannot meet claim limitations by simply proclaiming them met in conclusory statements.

For the above reasons, the Petition fails to demonstrate that the limitations of 1[C] are anticipated or rendered obvious by the TI Datasheet. Ground 1 thusly fails to present a reasonable likelihood of success.

4. Ground 1: the Petition fails to present its grounds with the requisite clarity.

The Petition presents the TI Datasheet but injects substantial analysis to cure claim limitations that are not literally present. This fails to (1) present a proper anticipatory analysis and (2) fails to describe how/why a POSITA would find the limitations obvious. *See, e.g., Motorola, Inc. v. Interdigital Tech. Corp.*, 121 F.3d 1461, 1473 (Fed. Cir. 1997) (expert’s conclusory statement of anticipation unsupported by documentary evidence not a substitute for “anticipatory disclosure

in the prior art reference itself.”); *Initiative for Medicines, Access & Knowledge (I-Mak), Inc. v. Gilead Pharmasset LLC*, Case IPR2018-00390, Paper 7, 14-15 (P.T.A.B. July 19, 2018) (denying institution where petitioner asserted obviousness in a conclusory fashion as part of the anticipation challenge).

a. The Petition fails to present a reasonable basis to assert that the TI Datasheet anticipates.

The Petition fails to properly present an anticipatory ground; it presents the TI Datasheet to anticipate the independent claims but relies extensively on a POSITA’s supposed understanding to fill-in non-present limitations. The TI Datasheet lacks many express limitations required by the claims, and the Petition tries to overcome this by relying on POSITA-plug-in statements (*i.e.*, conclusions that “a POSITA would understand ...”) even though those POSITA-plug-ins are conclusory and not supported with evidence. For instance, the Petition relies on a POSITA-plug-in to teach limitation 1[A]’s “first comparing module” and its inputs/outputs (“bootstrap voltage signal,” “bootstrap refresh threshold,” and “first comparing signal”). (Pet. at 27 (“A POSITA would understand from this disclosure that a comparator input receiving the threshold voltage is necessarily present, notwithstanding the simplicity of TI’s high level block diagrams”); EX2001 at ¶¶104-106.)

Compounding the problem, Petitioner extensively uses a POSITA-plug-in to arrive at the limitations of 1[D] (which describes functionality based on the “first

comparing module”) based on its 1[A] POSITA-plug-in, the extent of which is illustrated by the below excerpt and annotations (yellow indicating each time a POSITA’s supposed understanding was invoked; aqua emphasizing the functionality/circuitry that is conjured):

A POSITA would understand that a voltage regulator with integrated MOSFETs would include circuitry that switches the MOSFETS on and off to regulate the output voltage, and that the regulation is based on a difference between a feedback signal and the reference voltage. *Id.* Furthermore, a POSITA would understand that switching the MOSFETS on and off would charge the bootstrap capacitor at least during the time when the high-side switch is off and the low-side switch is on. EX1003, ¶132.

Additionally, a POSITA would understand that at the time when the TPS54620 exits a “pulse skipping” mode of operation (and resumes switching the MOSFETS on and off to regulate the output voltage), the feedback signal will also be below the reference voltage. EX1003, ¶¶69, 133; EX1022, 10-11; EX1023, 12.

Therefore, a POSITA would understand that TI’s disclosed Power Stage Logic switches on and off the high-side and low-side switches based on the output of the error amplifier, thus charging the bootstrap capacitor. EX1003, ¶133. A POSITA would also understand that this would include when the feedback signal is less than the reference voltage, as described above. *Id.*

And, this extensive POSITA plug-in is done across only 1.5 pages of analysis, *i.e.*, the whole of the analysis is based on functionality not literally present. (Pet. at 30-31; EX2001 at ¶¶107-109.) As such, Ground 1 fails as an anticipatory ground at a threshold level and should be denied.

b. The Petition fails to present a reasonable basis to assert that the TI Datasheet renders the claims obvious.

As described above, Petitioner utilizes a POSITA-plugin for inherency, but does not offer any evidence or reasons to support its inherency arguments—a necessary requirement of inherency. Petitioner alternatively presents Ground 1 as obvious but does not describe how those above-described limitations would have been obvious, *i.e.*, Petitioner does not describe how a POSITA would have been motivated to provide them and would have had a reasonable expectation of success via their inclusion. *See Initiative for Medicines*, Case IPR2018-00390, Paper 7, 14 (“A petitioner in our forum cannot satisfy its burden of proving obviousness by employing ‘mere conclusory statements’ regarding the motivations of an ordinarily skilled artisan.”) (citing *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016)). Instead, Petitioner presents obviousness as an alternative catch-all (without any supporting analysis). (Pet. at 28 (“Alternatively, limitation 1[A] is obvious over TI in view of the knowledge of a POSITA”), 30 (arguing for 1[C] that “[a]lternatively, it would be obvious to a POSITA”); EX2001 at ¶¶110-11.) The Petition further fails to properly provide a rationale for obviousness and fails to describe the scope of the prior art under a proper *Graham* factor inquiry required for obviousness. *See Google Inc. v. EveryMD.com LLC*, IPR2014-00347, Paper 9, 23–25 (May 22, 2014) (denying institution because petitioner did not meaningfully

address the first two *Graham* factors). Ground 1 thusly fails to present the requisite obviousness analysis.

Petitioner's catch-all fails to present proper motivations, expectations of success, and fails to make a proper *Graham* factor inquiry. Ground 1 thusly fails.

B. Grounds 2, 3, and 5: Galinski does not anticipate or render any claim obvious.

Grounds 2, 3, and 5 rely on Galinski, but it does not anticipate or render obvious the independent claims for several reasons.

First, limitation 1[D]'s requirement to “control the [switches] ... based on the difference signal so as to charge the bootstrap capacitor” is not taught.

Petitioner relies on circuitry relating to voltage regulation based on feedback, which would effectively be disabled when the capacitor is being refreshed via circuitry the Petition identified in 1[C].

Second, a “bootstrap refresh threshold” as required by 1[A] is not taught. Petitioner relies on Galinski's output voltage to be the “bootstrap refresh threshold.” These two are dissimilar.

This is described in detail below.

1. Grounds 2, 3, and 5: Galinski does not teach the limitation to “control the [switches] ... based on the difference signal so as to charge the bootstrap capacitor” as required by 1[D].

The Petition has a fatal gap; namely, the functionality Petitioner identifies

for 1[D] is unrelated to the claim requirement that the bootstrap refresh control circuit “control[s] the [switches] ... based on the difference signal so as to charge the bootstrap capacitor.” (EX2001 at ¶ 113.) Limitation 1[D] requires that once the output voltage has decreased too much (*e.g.*, the output voltage has been decreased because the feedback signal is smaller than the reference voltage signal, according to 1[C]), the high side and low side switches are controlled so as to charge the bootstrap capacitor. The circuitry Petitioner relies on for 1[D] is related only to regulating an output voltage, and not for controlling high and low side switches to charge the bootstrap capacitor. (EX2001 at ¶114.)

Galinski operates its switches in two ways, either they are operating normally, or they are responding to a reset pulse to recharge the capacitor. (*See* EX2001, ¶¶115-16 (describing that the switches are controlled during normal operation to achieve a desired output voltage, but that during the reset pulse, the normal operation is disabled and the high side switch is turned off and the low side switch is turned on.) There is normal operation circuitry that regulates the switches to reach a desired output voltage V_{OUT} and reset circuitry that disables the voltage regulation circuitry’s ability to control the switches under normal operation. (EX2001, ¶ 117.) Problematically, Petitioner relies on reset circuitry for 1[A] and 1[C] and normal operational circuitry for 1[B] and 1[D], but the normal operation circuitry is not responsible for charging the bootstrap capacitor. (EX2001 at ¶¶118-

119.) As a consequence, 1[D]—which requires that the bootstrap capacitor be recharged—is not met by the identified circuitry.

Specifically, Petitioner relies on comparator 112 and the reset pulse (V_{RST}) to satisfy 1[A]’s “comparing module” that generates a “comparing signal” and the functionality performed when reset pulse is generated to satisfy 1[C]. (Pet. at 37-39 and 40-41.) This circuitry disables normal switching via a reset pulse to refresh the bootstrap capacitor because the reset pulse (V_{RST}) is a short pulse generated by a comparator 112—that toggles switches Q1 and Q2 for a short duration via set/reset flip-flop 114—to recharge the capacitor. (EX1005 at 9:5-7, 9:21-23, 10:18-23, 10:32-35; EX2001, ¶ 115.) After the reset pulse, the circuit returns to normal operation (*id.* at 9:23-28, 10:32-35) where the voltage is regulated by modulating the duty cycle via a feedback loop. (*Id.* at 6:2-7, 6:25-37; EX2001, ¶ 115.) The reset pulse is the mechanism used to recharge the capacitor, and it disables the voltage regulation circuitry’s ability to control the switches. (EX2001, ¶¶ 115-16).

Petitioner relies upon the circuitry that is disabled during a capacitor recharge (e.g., Petitioner relies on the voltage regulation via feedback loop) to meet the elements of 1[B] and 1[D], but that disabled circuitry is not responsible for charging the capacitor. (Pet. at 39-40 and 41-41; EX2001, ¶¶ 117-19.) 1[D] as previously noted requires that the circuitry be “configure[d] to *control the high side switch and the low side switch* to switch on and off *based on the difference*

signal so as *to charge the bootstrap capacitor.*” (1[D] (emphasis added).)

Galinski’s voltage regulation circuitry does not control the switches to charge the bootstrap capacitor and is, in fact, precluded from controlling the switches when other circuitry (comparator 112) is used to charge the bootstrap capacitor.

(EX2001, ¶ 119.) As a consequence, Petitioner has failed to demonstrate a reasonable likelihood that Galinski teaches 1[D].

Tellingly, Petitioner’s analysis regarding how Galinski’s voltage regulation circuits meet 1[D]’s bootstrap capacitor requirements are conclusory and untied to the specifics of the claim language or Galinski. Petitioner relies upon its expert for the premise that these limitations are met “because of the decrease in output voltage from the desired value, when the regulator is in ‘soft start’ mode, or when the regulator exits a ‘pulse skipping’ mode.” (Pet. at 42 (citing EX1003 at ¶ 163).) This statement fails several reasons.

First, the Petition’s conclusory statement makes no tie between a pulse skipping or soft start mode and the charging of the capacitor based on the difference signal. (See Pet. at 42; EX2001 at ¶120.) The difference signal is based off of feedback from the output voltage and, by its very nature, the feedback signal would only have a value if the output is being driven and operational, *i.e.*, the circuit began generating V_{OUT} . And, once the circuit is operating and driving an output voltage, the only circuit controlling the capacitor recharge is comparator

112 as described above. The capacitor recharge in Galinski is not controlled by the “difference signal” which is based on feedback from the output voltage of the circuit. (EX2001 at ¶¶120-21.)

Second, Galinski does not teach a “soft start” or “pulse skipping” mode. (*See generally* EX1005.) Further, its teachings indicate that such a mode would not exist in relation to capacitor charging via the reset pulse. Galinski immediately returns to normal operating conditions after the very short reset pulse. (EX1005 at 9:5-7, 9:21-23, 10:18-23, FIG. 3.) Galinski states that “the switching of the power switches caused by bootstrap voltage control circuit 110 is of such short duration that the overall duty cycle of buck regulator 100 does not deviate appreciably from the 100% or near 100% level.” (*Id.* at 9:25-28.) Petitioner’s referenced “soft start” and “pulse skipping” modes are not present in Galinski, and Galinski indicates that they would not be present whenever a reset pulse is generated. (EX2001 at ¶122.)

Third, the cited-to portion of Petitioner’s expert (EX1003 at ¶ 163) provides no real support. ¶ 163 repeats the conclusion and back-references ¶ 107 and ¶ 69 for support of soft start and pulse skipping, respectively. ¶ 107 is related to the TI Datasheet’s specific circuitry and ¶ 69 is related to general background stating that pulse skipping reduces voltage. None of this supports the conclusion that Galinski teaches a soft start” or “pulse skipping” mode after a reset pulse, or that the limitations of 1[d] relating to the difference signal would be met in Galinski.

(EX2001 at ¶123.)

Finally, as described above, the alleged “first comparing module” and “voltage difference module” in Galinski are diametrically opposed to each-other because one disables the other. The ’608 Patent’s embodiments, in contrast, work in tandem. This is described in more detail in § V.B.1. (EX2001 at ¶124.)

Thusly, Galinski does not anticipate the ’608 Patent expressly or inherently.

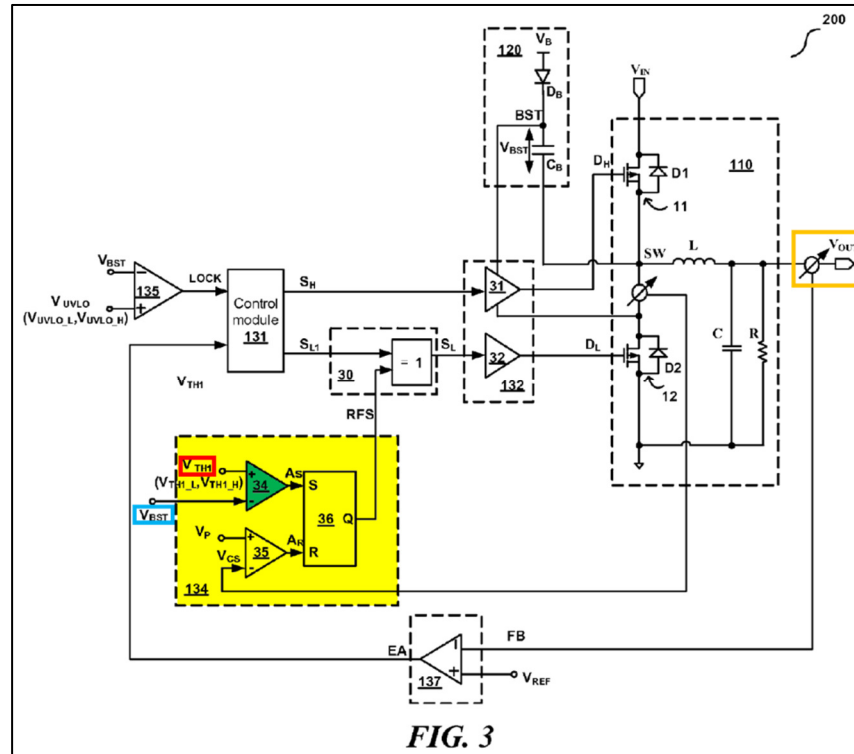
2. Grounds 2, 3, and 5: Galinski does not teach a “bootstrap refresh threshold” as required by 1[A].

Petitioner identifies the claimed “bootstrap refresh threshold” of 1[A]⁴ as Galinski’s switching output voltage V_{SW} (which drives its V_{OUT}). A converter’s output voltage, however, is not a “bootstrap refresh threshold.” Thus, Ground 1 fails.

Figure 3 of the ’608 Patent is excerpted below to provide illustrative context to the claims. (EX2001 at ¶¶126-27.) 1[A] requires a “bootstrap refresh control circuit” that has a “bootstrap refresh module” (*e.g.*, bootstrap refresh module 134 (yellow, below)) which comprises “a first comparing module” (*e.g.*, comparator 34, green) that compares a “bootstrap voltage signal” (*e.g.*, V_{BST} , blue) with a “bootstrap refresh threshold” (V_{TH1} , red). (EX1001, 19:10-20, 9:10-20, 10:60-63,

⁴ Claims 11 and 12 require the same limitations and fail for the same reasons. (*See* EX1001 at 23:24-28, 24,7-8).

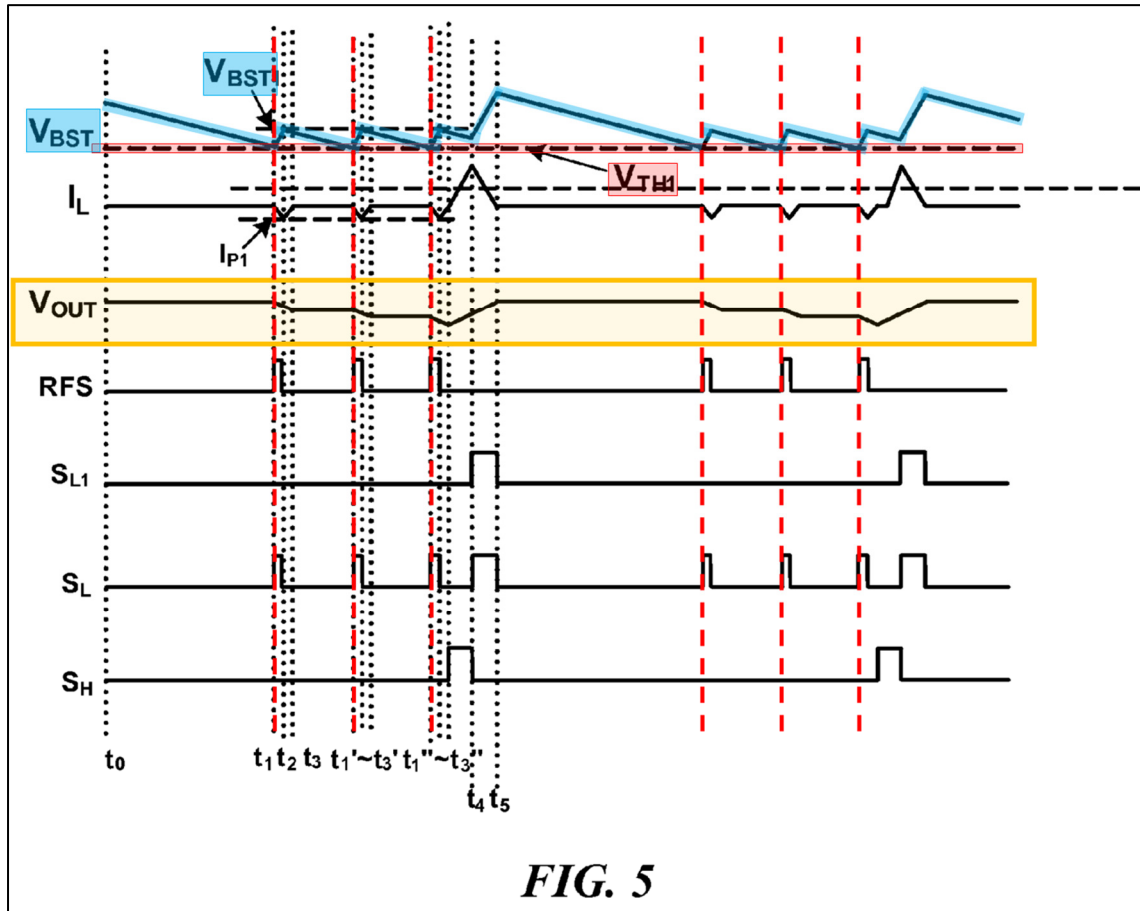
11:1-6, 12:15-29); EX2001 at ¶127.)



The '608 Patent describes the “bootstrap refresh threshold” as a level that indicates when the “bootstrap voltage signal” (*e.g.*, V_{BST}) is too low. (EX1001, 3:19-32; 8:16-21; EX2001 at ¶¶127-128.) And, when “bootstrap voltage signal” (*e.g.*, V_{BST}) falls below the level defined by the “bootstrap refresh threshold” (V_{TH1}), the output voltage V_{OUT} (orange, above) is controlled to decrease. (*See* 1[A] and 1[C] (stating that during the first logic state, *i.e.*, “bootstrap voltage signal” < “bootstrap refresh threshold” to “decrease the output voltage of the voltage converter”); *see also* '608 Patent at 8:26-30 (“If the “bootstrap voltage signal” (V_{BST}) drops lower than the “bootstrap refresh threshold” (V_{TH1}), the bootstrap refresh module 133 starts to operate to reduce the output voltage (V_{OUT}) of the

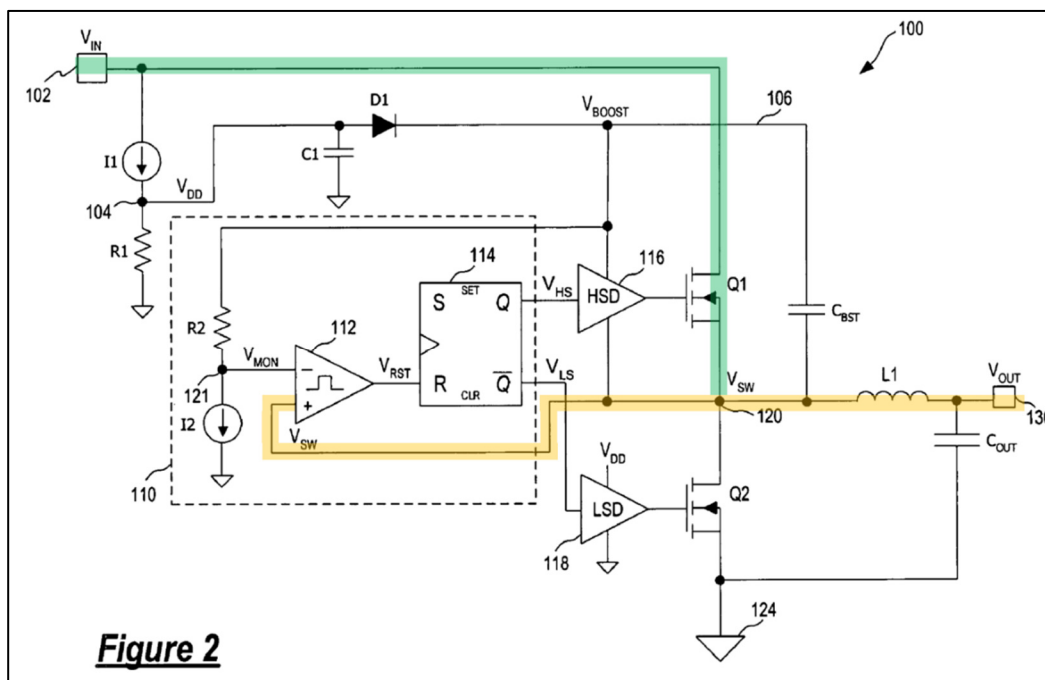
voltage converter 100”).)

The interaction between V_{BST} , V_{TH1} , and V_{OUT} is illustrated in Figure 5 of the '608 Patent. There, “bootstrap voltage” V_{BST} (blue) is shown as decreasing, and when it drops below “bootstrap refresh threshold” V_{TH1} (red), the output voltage V_{OUT} (orange) decreases. (EX1001, 15:16-17, 22-23.) Instances where $V_{BST} < V_{TH1}$, and consequently a decreasing V_{OUT} , are depicted with the vertical dashed-red line. (EX2001 at ¶128.)



As can be seen from the above, “bootstrap refresh threshold” indicates when the “bootstrap voltage” becomes too low; it is distinctly different from V_{OUT}

because the “bootstrap voltage” is compared to the “bootstrap refresh threshold” irrespective of the output voltage V_{OUT} , but when the “bootstrap voltage signal” is less than the “bootstrap refresh threshold,” then there is a “decrease [of] the output voltage of the voltage converter.” (EX2001, ¶¶127-29.) Despite this, Petitioner relies on Galinski’s switching output voltage V_{SW} that drives V_{OUT} to satisfy the “bootstrap refresh threshold.” (Pet. at 39 (“the switching output voltage V_{SW} is a threshold against which the bootstrap voltage is compared”).) As depicted below with respect to Galinski, the switching output voltage V_{SW} is a voltage taken from the voltage node 120 that generates a regulated output voltage V_{OUT} via capacitor C_{OUT} and inductor L_1 . (EX1005 at 5:30-36.) V_{SW} is the pulsed output of Q1 from V_{IN} (path in green). (EX1005, 1:129-30.) As such, the switching output voltage V_{SW} drives the output voltage V_{OUT} and is not the claimed “bootstrap refresh threshold.” (EX2001 at ¶129.) Petitioner’s Galinski-based grounds thusly fail.



Ground 2 accordingly fails to present a reasonable likelihood of success and the Petition should be denied.

3. Grounds 3 and 5 fail for the same reason that Ground 2 fails.

The above was described with respect to Ground 2. Grounds 3 and 5 do not cure the above-described deficiency and, instead, seemingly rely on the same analysis. (Pet. at 47, 67-68.) To the extent any additional analysis is assumed, the obviousness analysis is purely conclusory as it repeats that certain elements are obvious, without any explanation as to why or how. (*Id.*)

a. Ground 3

In Ground 3, Petitioner relies on the exact same arguments as it did in Ground 2 for the independent claims, but instead of arguing an anticipation theory,

Petitioner argues that Galinski renders the claims obvious.⁵ Paper 1, 47, 49.

However, Petitioner offers no additional substance to support *why* Galinski renders the limitations obvious. (EX2001 at ¶131.) Petitioner states, in a conclusory fashion, that it just would be obvious: “To the extent that Galinski does not expressly or inherently disclose the one-shot comparator circuit 112 outputting a signal having a first logic state when the bootstrap voltage signal is lower than the bootstrap refresh threshold and a second logic state when the bootstrap voltage signal is larger than the bootstrap refresh threshold, Galinski renders this feature obvious to a POSITA.” (Pet. at 47.) Petitioner’s expert also offers no obviousness analysis, and the Petitioner just cites to the same paragraphs of the expert’s report as they did in the anticipation theory in Ground 2. (Pet. at 38-39, 47, EX1003, ¶¶ 57-62, 155.)

Such conclusory statements do not meet the Petitioner’s requirement to set forth a reasonable likelihood of success that Galinski renders the independent claims of the ’608 Patent obvious. *Initiative for Medicines, Access & Knowledge (I-Mak), Inc. v. Gilead Pharmasset LLC*, Case IPR2018-00390, Paper 7, 14-15 (P.T.A.B. July 19, 2018) (denying institution where petitioner asserted obviousness

⁵ Petitioner only asserts the alleged combination of Galinski with Li in the dependent claims 2 and 16. (Paper 1, 48, 49.)

in a conclusory fashion as part of the anticipation challenge). Ground 3 accordingly fails for the same reasons as Ground 2.

b. Ground 5

In Ground 5, Petitioner only focuses on dependent claims 6 and 15. (Pet., 66; (EX2001 at ¶131.) Because the independent claims are not rendered obvious by Galinski, then Ground 5 fails for the reasons discussed above.

C. Ground 4: Wong does not render any claim obvious.

Petitioner's Ground 4 relies on its replacement of a Zener diode of Wong with a switch. This fails for two reasons: (1) Petitioner fails to describe how that switch would be controlled, leaving the limitations relating to its control (1[PRE] and 1[D]) untaught; and (2) a POSITA would not have replaced a Zener diode in Wong's circuits with a switch, because the Zener diode exists in the circuit to provide a functionality that the switch does not provide. Namely, the Zener diode provides a stable output voltage.

1. Ground 4: Petitioner's obviousness modification of Wong fails to address 1[PRE]'s "driving the high side and low side switch to switch on and off" and 1[D]'s "control the high side and the low side switch ... to switch on and off."

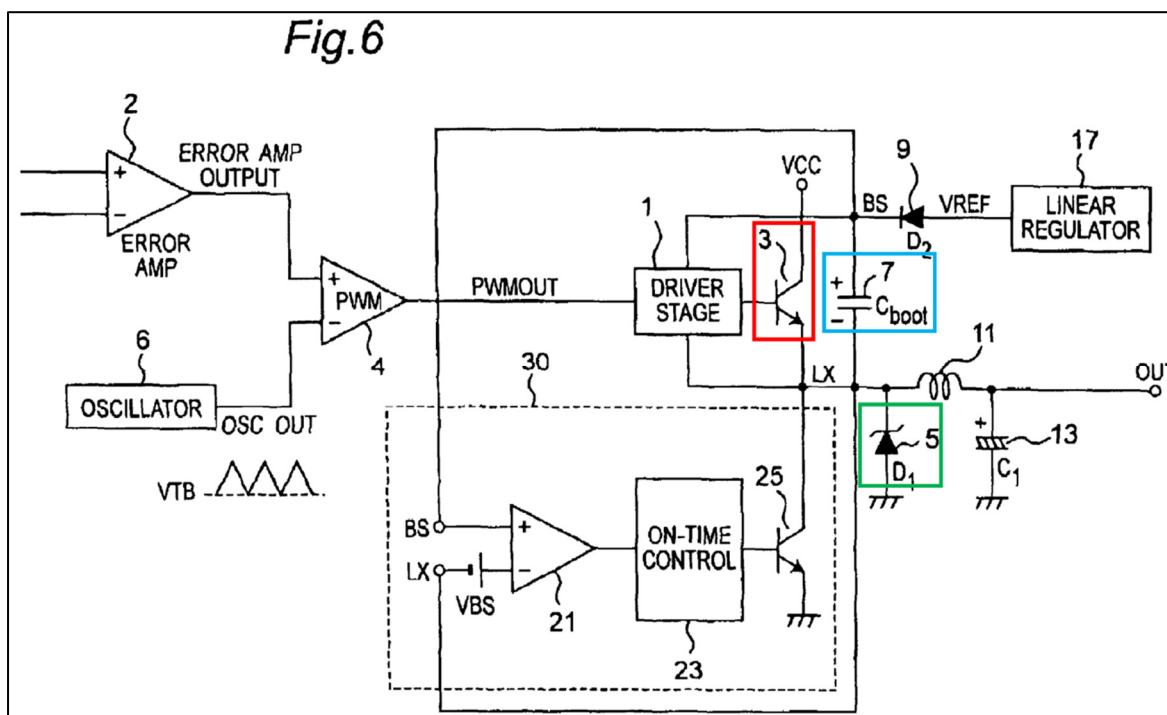
The Petition suffers from a fatal deficiency which demonstrates a failure to present a reasonable likelihood of success for Ground 4.

The Petition fails to address how its purported combination (which replaces a Zener diode with switch) would be driven according to 1[PRE] or controlled to

switch according to 1[D]. (*See* 1[PRE] (“driving the high side switch and the low side switch to switch on and off”) and 1[D] (“the bootstrap refresh control circuit is configured to control the high side switch and the low side switch to switch on and off based on the difference signal”); EX2001 at ¶¶133-37.) The Petition thusly fails even if Petitioner’s rationale for combination were adopted.

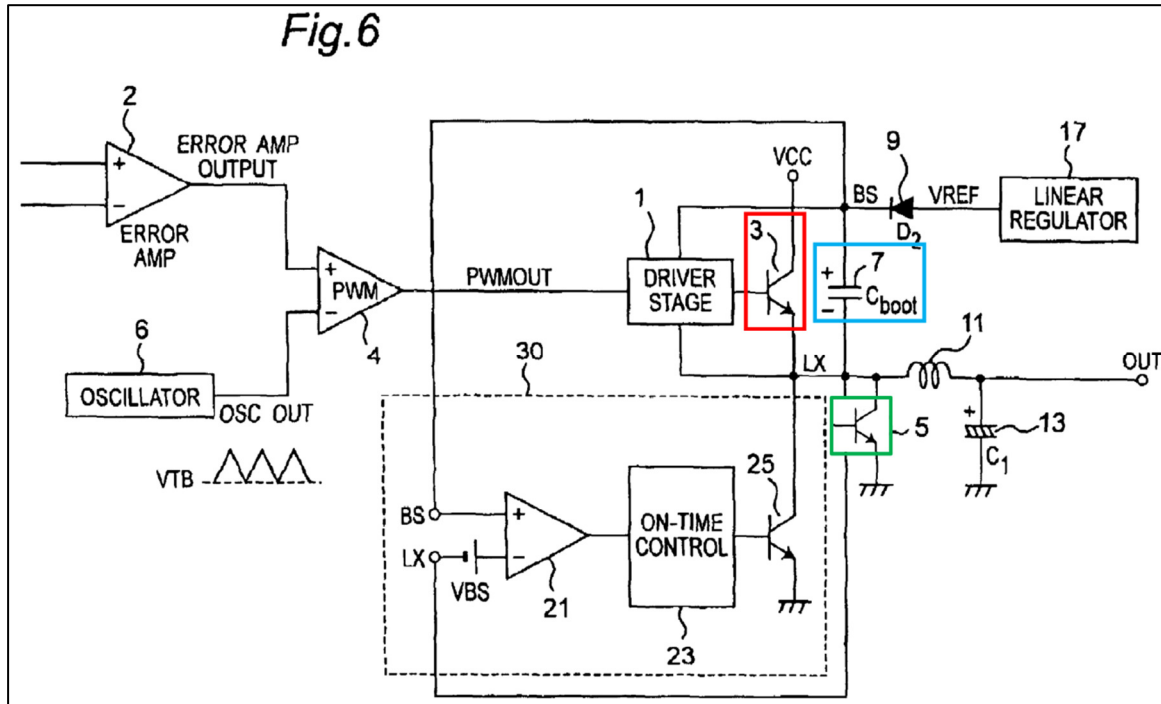
The Petition contains a fatal hole in its analysis for the claimed “low side switch” because it does not describe how the switch’s gate would be controlled.

This deficiency is introduced in the Petition’s analysis of 1[PRE]. There, Petitioner’s combination replaces Wong’s Zener diode 5 (D_1) with a switch to meet the claimed “low side switch.” (Pet. at 50 (“A POSITA would understand that a low-side diode is analogous to a low-side switch and that replacing Wong’s low-side diode with a low-side switch is an obvious variation of Wong’s converter system”); EX2001 at ¶¶134-36.) For further context, Petitioner’s articulation of its combination is graphically illustrated below. Petitioner states that “when combined with the knowledge of a POSITA, Wong teaches circuits for use in voltage converters having high side (3) [(red)] and low side (5) [(green)] switches and a bootstrap capacitor (7) [(blue)] to supply a bootstrap voltage to a driver (1) of the high side switch.” (Pet. at 51 (additions for coloring added by Patent Owner).)



The circuit of Fig. 6 above, with Petitioner's modification, would replace Zener diode 5 (green, above) with a switch (green, below). Petitioner never reconciles how the switch is controlled. (EX2001 at ¶136.) As shown below, the BJT's base is floating (because Petitioner never describes how it would be controlled).⁶

⁶ Although a BJT is described, the discussion applies equally for any other transistor. (EX2001 at ¶136.)

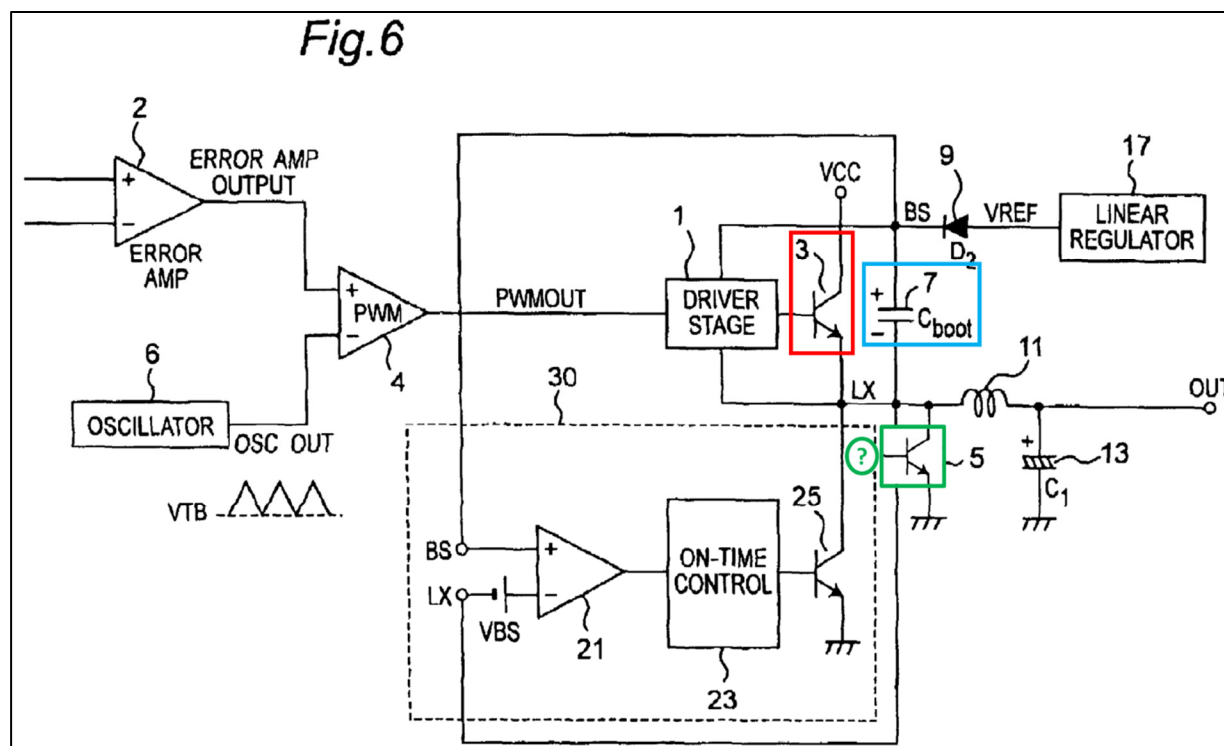


As such, lacking any description regarding how the switch (green, above) is controlled, the purported obviousness modification of Wong fails to teach 1[PRE]. (EX2001 at ¶¶136-37.) Ground 4 thusly fails from this fatal flaw and fails to demonstrate a reasonable likelihood of success.

This fatal flaw continues to 1[D], which further demonstrates Ground 4's deficiencies. 1[D] requires that an action be performed on the low side switch under a certain control condition. Specifically, it requires that *“when the feedback signal is smaller than the reference voltage signal, the bootstrap refresh control circuit is configured to control the high side switch and the low side switch to switch on and off based on the difference signal.”* (1[D] (emphasis added).) In other words, there is a specific control performance required (“switch on and off

based on the difference signal”) under a certain condition (“when the feedback signal is smaller than the reference voltage signal”).

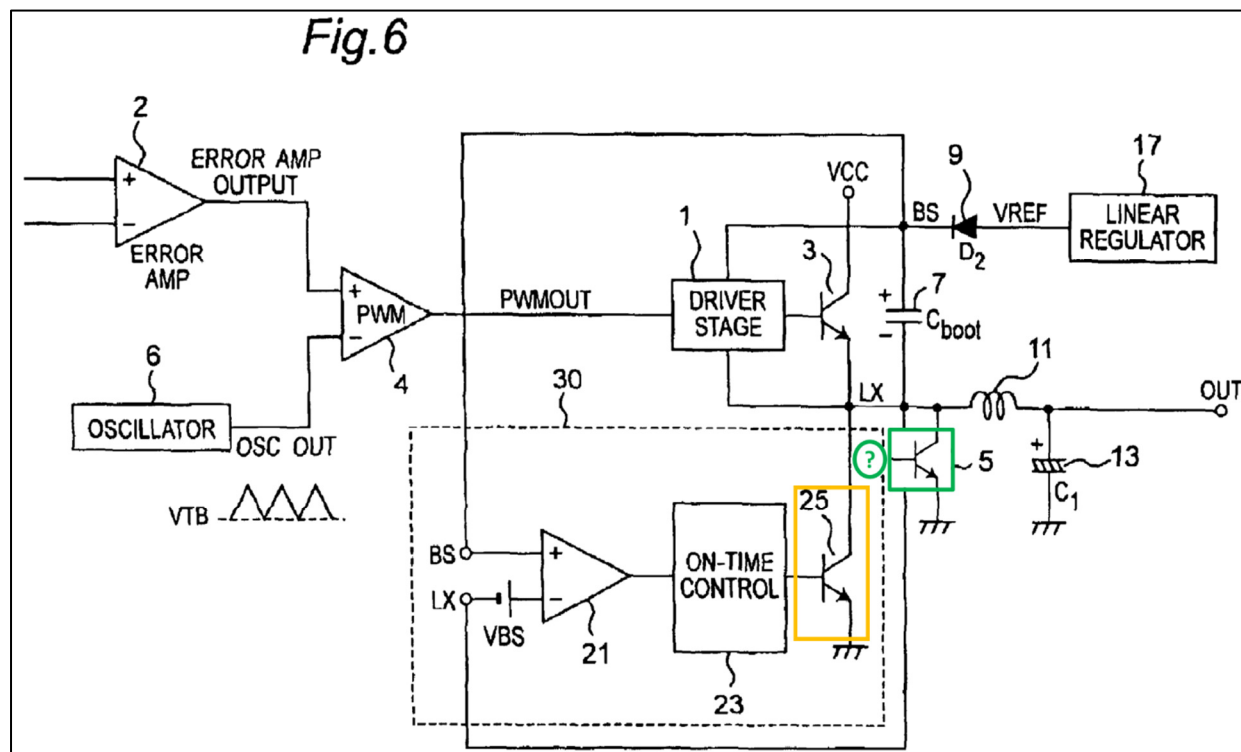
The Petition’s analysis for 1[D] is wholly vacant regarding how its low side switch (*i.e.*, the Zener diode D1 being replaced with a switch) would be controlled. (Pet. at 56-58; EX2001 at ¶138.) Instead, Petitioner merely back-references its 1[PRE] analysis. (Pet. at 57 (“And, as discussed above with respect to limitation 1[PRE], Wong’s low-side diode is analogous to a low-side switch.”).) As such, the Petition is wholly vacant regarding how the alleged “low side switch” (which is a switch replacing Zener diode 5) would be controlled (annotated again below).



Rather than provide a consistent analysis, Petition performs a switcheroo and analyzes switch 25 instead of the alleged “low side switch” (which is a switch

replacing Zener diode 5). (Pet at 57-58.) These two separate switches are annotated below (switch 25 in orange and the alleged low side switch in green). As can be seen below, these two switches are very different and cannot be conflated.

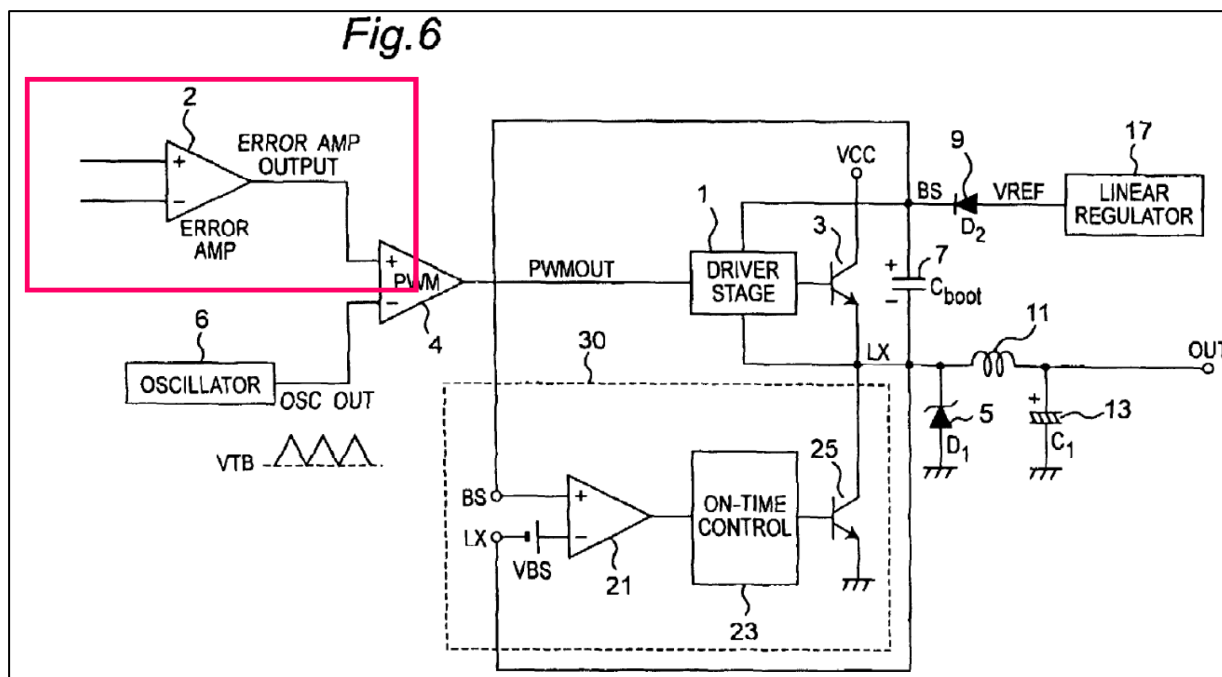
(EX2001 at ¶139.)



Finally, Petitioner’s analysis of switch 25 (orange) and its alleged “low side switch” (which is a switch replacing Zener diode 5) cannot merely be taken to be the same control scheme and be consistent with the claims. (EX2001 at ¶140.) 1[D] is directed to performing control of the high side switch and low side switch based on the feedback signal (e.g., the difference signal) which is from the “voltage difference module” of 1[B]. Petitioner, however, has identified the “voltage difference module” as being the error amp, as illustrated below from the excerpted

image from the Petition. (Pet. at 53.) As can be seen below, the error amp's PWMOUT controls the driver stage of the alleged high side switch 3 and is entirely unrelated to any control of switch 25. Moreover, the on-time control switch 25 has been identified as the "first comparing module" by Petitioner (1[A]), which is separate from the "voltage difference module" of 1[B]. As a consequence, Petitioner's switch 25 analysis is wholly inapplicable to the limitations of 1[D]. (EX2001 at ¶140.)

Fig.6



Petitioner's expert provides no further analysis, and instead repeats
Petitioner's analysis. (EX2001 at ¶¶141-42; EX1003 at ¶¶ 65-69, 107, 199, 215-
220.)

Ground 4 is thusly fatally deficient and fails to present a reasonable likelihood of success.

2. Ground 4: Petitioner fails to present a motivation to replace Wong's Zener diode with a switch.

As described above, Ground 4 fails to present a reasonable likelihood of success because it lacks required claim limitations. It further fails to present a reasonable likelihood of success because there is no motivation to make the alleged combination (replacing Wong's Zener diode D1 with a switch).

a. Petitioner's combination does not comport with Wong's teachings.

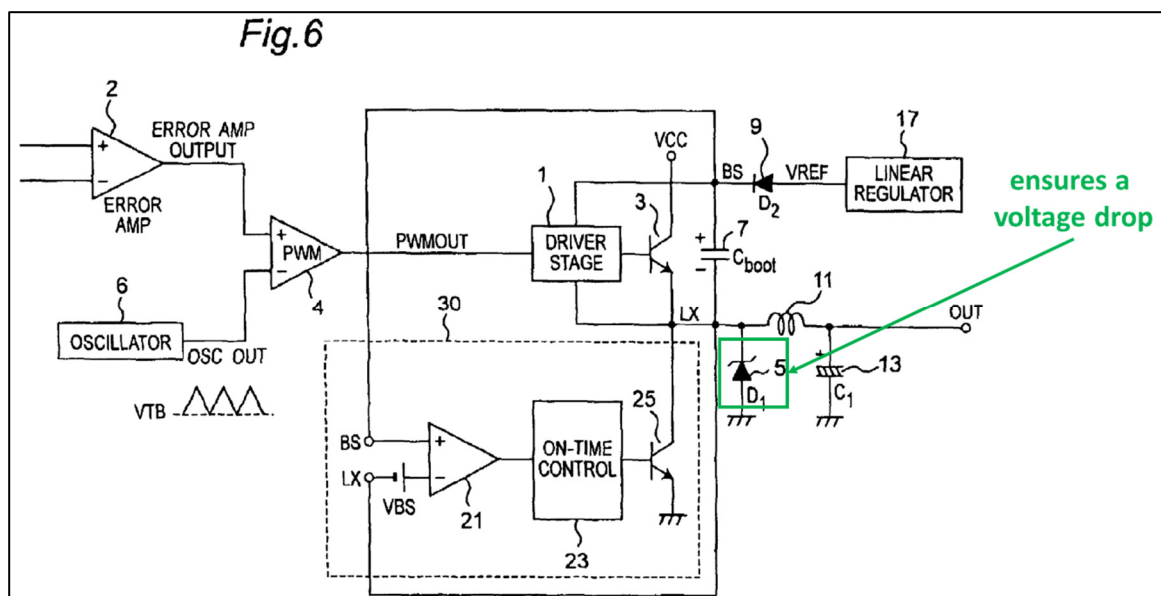
As described above, Petitioner takes Wong's Zener diode D1 and replaces it with a switch. A POSITA would not have done this because doing so would obfuscate the purpose of the Zener diode. *See Intel Corp. v. Koninklijke Philips N.V.*, No. 2022-2034, 2024 WL 725243, at *1 (Fed. Cir. Feb. 22, 2024) (affirming the Board's finding that two references were incompatible and could not be combined with another reference because the two were directed to multi-bit exchanges, but the latter reference was directed to a single bit, and the petitioner did not reconcile this conflict); *Adidas AG v. Nike, Inc.*, 963 F.3d 1355, 1358-60 (Fed. Cir. 2020), cert. denied, 141 S. Ct. 1376 (2021) (affirming finding in an IPR that the patent was not found to be obvious over the prior art because "combining Reed with Nishida would 'require the alteration of the principles of operation of Reed or would render Reed inoperable for its intended purpose.'").

Specifically, and fatally to the Petition, Petitioner does not acknowledge that

Wong's Zener diode 5 (green, below) is in fact a Zener diode, nor does Petitioner appreciate the Zener diode's functionality in the circuit. (EX1005 at Figure 6.)

Replacing the Zener diode with a switch defeats the functionality of the Zener diode, and a POSITA would not have made this change. (EX2001 at ¶144.)

The Zener diode is provided in Wong to provide a stable output voltage. (EX2001 at ¶144.) A Zener diode is a diode that controls current in both directions. (*Id.*) And, in the particular configuration of Wong, the Zener diode is placed in its reverse bias configuration to shunt the output voltage at a higher bias voltage (its breakdown voltage). (*Id.*) The Zener diode is used to help provide a sufficient, stabilized voltage drop for the output voltage. (*Id.*) With the Zener diode, the voltage across any load connected to the circuit will be the same as the Zener diode's breakdown voltage, which is high. (*Id.*) As a consequence, the Zener diode D1 in the below circuit of Wong ensures a stable voltage irrespective of the value of any load. (*Id.*) This output voltage stability, irrespective of the value of any load, is not achieved by a simple switch substitution. (EX2001 at ¶145) And it is not the type of substitution that a POSITA would make for at least the reasons of extensive evaluation requirements and added control circuitry (none of which is even addressed by Wong) to control the on/off conditions of the substituted switch. (EX2001 at ¶144-46.)

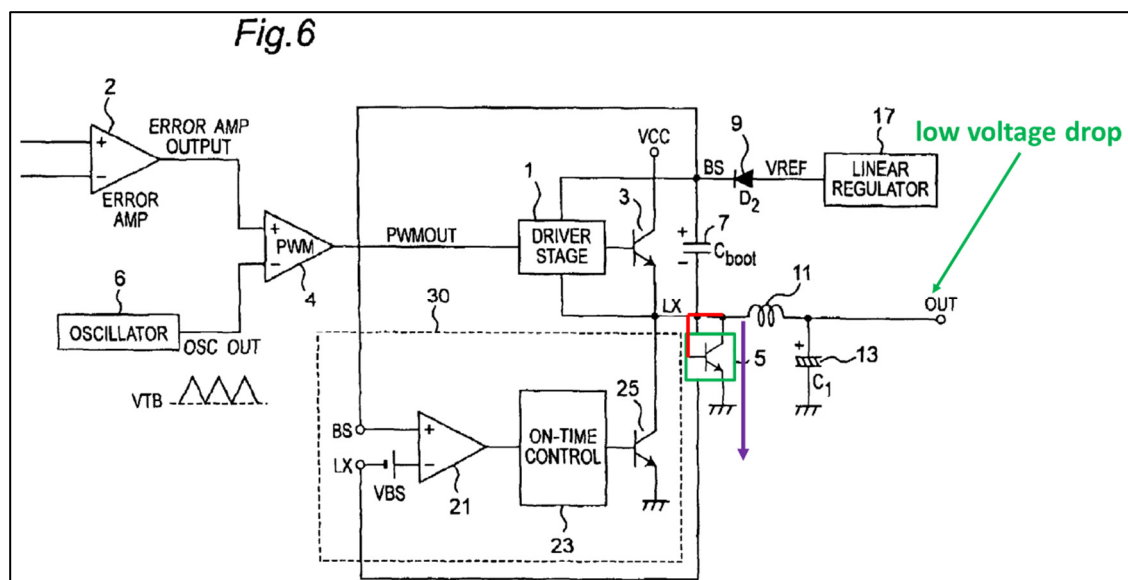


Petitioner's analysis is deficient because it assumes that this Zener diode is simply a normal forward-biased diode whose functionality simply allows current to flow and can as such be replaced with a switch. (Pet. at 50-51.) This cannot be done because, as noted above, the Zener diode's reverse bias voltage stably controls an output voltage. (EX2001 at ¶147.) A switch (like a BJT)⁷ will not do this; it would act as an effective short with a very low voltage drop if on and an open circuit if off. (EX2001 at ¶147.) Moreover, a switch (e.g., BJT's) voltage drop will be significantly lower than a Zener diode's reverse bias voltage, making it ineffective at providing a stable output voltage. (EX2001 at ¶147.) A BJT (or any other switch) cannot act as a stand-in for the Zener diode as Petitioner alleges. (EX2001 at ¶147.)

⁷ A BJT is described because Wong's figures illustrate using BJTs.

Furthermore, as described above in § V.C.1, Petitioner makes zero effort to describe how its switch would be controlled, a fatal flaw in its motivation to replace the Zener diode with a switch. (EX2001 at ¶148.)

Moreover, attempting to resolve Petitioner's lack of discussion of how the transistor switch is controlled demonstrates the impropriety of Petitioner's modifications. A POSITA would understand that a switch (BJT) can function similar to a standard diode by wiring a BJT's base to its collector. (EX2001 at ¶148.) This is shown below (red) for the stand-in BJT of Petitioner's combination. This, however, causes a problem with this circuit because whenever there is a voltage on the collector, the BJT will be biased by the base, and current will flow to ground (purple). This results in a voltage drop across the BJT which is low, resulting in a lower voltage to the load whenever voltage is applied to the circuit. (EX2001 at ¶148.) A POSITA would not have made this circuit substitution because it defeats the functionality of the Zener diode to provide a higher, stabilized output voltage. (EX2001 at ¶148.)



Petitioner's arguments to support this theory are further conclusory.

Petitioner states with two conclusive sentences that replacing a low side switch with a diode would be obvious and that the motivation for using a switch instead of a diode is for greater conversion efficiency. (Pet. at 50-51.) Petitioner's expert repeats these conclusive assumptions, citing EX1028, 332, 333 ("Wait") and EX1026, 1:26 ("Schoneman") for the assumption that a diode can function as a switch (EX1003, ¶¶ 65, 67; *see* EX2001 at ¶¶ 149-50.)

But Wait and Schoneman do not support this assumption. Wait simply offers circuit architectures that use four or more diodes in certain configurations to *act* like a switch, but Wait never stands for the assertion that a single diode—and especially a Zener diode—is interchangeable with a switch, and it certainly does not say a Zener diode is interchangeable with a switch in the context of a voltage converter. (EX10028 at 332, 333; EX2001 at ¶150.) Further, the expert's cite to

Schoneman, a patent from 1992, simply alleges that a diode in *that patent's* converter *acts* as “a passive switch,” but neither Petitioner nor its expert explain how this can mean that the Zener diode can be replaced with a switch. (EX2001 at ¶151.) Not only would a POSITA not be motivated to replace the Zener diode with a switch (because the Zener diode is selected for output stability, and a switch would not do that), but Petitioner and its expert do not explain how the switch would be controlled. (*See supra*, § V.C.1). Unlike a Zener diode, which is selected based on its operating properties for that circuit and operates without a control signal, a switch like a BJT needs a control signal, and Petitioner and its expert fail to explain how that switch would be controlled and turned on and off and what the extra circuitry would be to control that switch and interact with the rest of the circuit—a requirement of 1[PRE] and 1[D]. Petitioner’s extrinsic evidence fails.

Petitioner’s expert also cites Schoneman, 1:49-59 and EX10025, ¶ 0021 (“Dubhashi”) for the wrong assumption that a switch would result in higher efficiency than a diode. (EX1003, ¶ 68.) Schoneman states nothing about efficiency, and Dubhashi explicitly states that a switch is advantageous from an efficiency perspective in systems that specifically need bidirectional current and reversed power flow. (EX1025, ¶ 21; EX2001 at ¶152.) Petitioner’s expert’s blanket assumption that switches are more efficient under all conditions is simply not true. Whether a switch results in higher efficiency depends on the architecture

of the converter, and neither Petitioner nor its expert attempt to explain why a POSITA would find that a switch results in higher efficiencies *for Wong*. (EX1003 at ¶ 68; (EX2001 at ¶152-53.) Moreover, none of Petitioner’s evidence addresses Wong’s usage of the Zener diode.

Petitioner’s motivation and rationale to replace Wong’s Zener diode with a switch accordingly falls short. Wong’s Zener diode is not interchangeable with a switch, such as a transistor. Petitioner’s Ground 4 thusly fails to present a reasonable likelihood of success.

VI. THE PETITION RELIES HEAVILY UPON CONCLUSORY STATEMENTS THAT LACK EVIDENTIARY SUPPORT

A petitioner must support their conclusory assertions with evidence. *See, e.g., Xerox Corp. v. Bytemark, Inc.*, IPR2022-00624, Paper 9, 15-17 (August 24, 2022) (precedential) (denying institution because expert declaration is entitled to little weight when it contains a restatement of the petitioner’s unsupported, conclusory assertions without any additional supporting evidence or reasoning). “This is particularly problematic in cases where, like here, expert testimony is offered not simply to provide a motivation to combine prior-art teachings, but rather to supply a limitation missing from the prior art.” *Id.* at 16 (citations omitted).

Here, the Petition and its expert repeatedly fail to provide evidence or reasoning to back up many of Petitioner’s conclusory statements which are

necessary to support its infringement theories. This is improper, and Petitioner cannot demonstrate a reasonable likelihood of success when it omitted such information.

For example, in its discussion about the TI Datasheet and 1[D], Petitioner repeatedly states in a conclusory fashion that “a POSITA would understand” and then recites a list of general assumptions without support. (*See supra*, § V.A.4.a; Pet., 30-31). As one example, Petitioner states:

A POSITA would understand that a voltage regulator with integrated MOSFETs would include circuitry that switches the MOSFETS on and off to regulate the output voltage, and that the *regulation is based on a difference between a feedback signal and the reference voltage*. (Pet., 30 (emphasis added)).

Petitioner’s expert repeats this statement, never explaining why the switching is done based on the feedback signal and reference voltage:

A POSITA would understand that a voltage regulator with integrated MOSFETS would include circuitry that switches the MOSFETS on and off to regulate the output voltage, and that the regulation is based on a difference between a feedback signal and the reference voltage. (EX1003, ¶ 132).

Petitioner and its expert are required to set forth more, but they repeat this behavior throughout their discussion of limitation 1[D]. (*See supra* § V.A.4.a; Pet., 30-31, EX1003, ¶¶ 132-33).

As another example, Petitioner injects a “soft start” and “pulse skipping”

mode into Galinski without support to arrive at 1[D]. (*See* § V.B.1.) Its expert repeats these conclusions, and no effort is made by Petitioner or its expert to tie these modes to key limitations of 1[D]. (*Id.*)

As another example, Petitioner asserts that Wong’s Zener diode could be replaced with a switch but makes no effort to explain how that switch would be controlled. (*See supra* § V.C.1; Pet., 50-51.) This is important because a Zener diode is passive and acts without a control signal, but a switch would need additional external circuitry added to Wong so that the switch is turned on and off correctly in relation to the high side switch. (EX2002 at ¶¶ 136, 144-145.)

Further, 1[D] is directed to performing control of the high side switch and low side switch based on the feedback signal which is from the “voltage difference module” of 1[B]. But instead of analyzing the “voltage difference module” of 1[B], Petitioner focuses on switch 25, which is not controlled by the voltage difference module. (*E.g.*, EX2001, ¶¶ 139-40.) Petitioner’s expert provides no further analysis, and instead repeats Petitioner’s analysis.

Overall, Petitioner and its expert repeatedly try to fill gaps in the prior art with conclusory statements but never provide supporting evidence for those conclusions. Institution is not warranted.

VII. THE BOARD SHOULD APPLY A DISCRETIONARY DENIAL

The Board should exercise its discretion to deny the Petition under 35 USC

§§ 314(a) and 316(b).

Petitioner has presented an excessive number of faulty grounds, each of which contain superficial analysis on a bevy of claim limitations for the independent claims. This warrants denial. *See, e.g., Adaptics Ltd. v. Perfect Co.*, Case IPR2018-01596, Paper 20 (March 6, 2019) (stating that the Board can deny rather than institute the entire petition under SAS Institute when there are a significant number of excessive grounds that lack merit).

All of Petitioner's grounds have gaps at the threshold level. For instance, Ground 1's analysis lacks discussion regarding how and where certain elements of 1[A] can be found in the TI Datasheet's Boot UVLO. (§ V.A.2.i) Petitioner leaves it up to the Board to decipher. Ground 2, 3, and 5's analysis fails to analyze how bootstrap capacitor refresh could be based on the "difference signal" which the circuitry providing such a signal cannot access the switches because they are disabled. (§ V.B.1.) Moreover, Ground 4 on Wong fails at a threshold level to identify a necessary controller for the low-side switch. (§ V.C.1.) All of Grounds 1-5 lack the appropriate element-level analysis.

If the Board tried to grant institution, the Board would be placed in a position to expend its resources to handle Petitioner filling-in and recreating analysis for the Petition. This analysis should have been in the Petition in the first instance, and the Board should not waste its resources. *See Netflix*, 84 F.4th at

1377 (“Ultimately, it is the petitioner’s burden to present a clear argument.”).

Petitioner’s failure—and presentation of numerous faulty grounds—warrants denial of institution.

VIII. CONCLUSION

For the foregoing reasons, Patent Owner respectfully requests that the Petition be denied.

Dated: September 3, 2024

Respectfully submitted,

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MONOLITHIC POWER SYSTEMS,
INC.,

CERTIFICATE OF WORD COUNT UNDER 37 CFR § 42.24(d)

Under 37 C.F.R. § 42.24(d), the undersigned certifies that the word count for this Patent Owner's Preliminary Response to the Petition for *inter partes* review totals 11,946, excluding the parts exempted by 37 C.F.R. § 42.24(a). The word count was made using the built-in word count function in the Microsoft® Word software used to prepare this document.

Dated: September 3, 2024

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), I certify that I caused to be served a true and correct copy of the foregoing: PATENT OWNER'S PRELIMINARY RESPONSE and accompanying exhibits by email to the electronic service addresses for Petitioner on the date indicated below:

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