

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

REED SEMICONDUCTOR CORP.,

PETITIONER

v.

MONOLITHIC POWER SYSTEMS, INC.,

Patent Owner.

Case No. IPR2024-00871

Patent No. 9,590,608

DECLARATION OF JOSEPH C. MCALEXANDER III, P.E.

TABLE OF CONTENTS

I.	INTRODUCTION AND QUALIFICATIONS	1
A.	Qualifications	2
B.	Materials Reviewed	4
C.	Summary of My Opinions.....	5
II.	UNDERSTANDING OF LEGAL PRINCIPLES AND PERSPECTIVES	6
A.	Types of Claims.....	7
B.	Anticipation	7
C.	Obviousness.....	8
D.	Claim Construction.....	10
E.	Person of Ordinary Skill in the Art	11
III.	BACKGROUND OF THE '608 PATENT	12
IV.	REASONS FOR PATENTABILITY	20
A.	Ground 1 (the “TI Datasheet”).....	20
1.	The TI Datasheet does not meet the requirements of limitation 1[D].....	21
a.	The TI Datasheet does not turn the high side switch on when the feedback signal is smaller than the reference voltage.....	24
b.	The TI Datasheet describes a fixed frequency control type, which is different from the control type of the '608 Patent.	27
(i)	Background of Fixed Frequency Modes vs. Constant On-Time modes.....	28
(a)	 Fixed Frequency Voltage Mode Control vs. Fixed Frequency Current Mode Control	28
(b)	 Constant On-Time (“COT”) Control	32
(ii)	The TI Datasheet uses fixed frequency mode, which is different from 1[D].	36
2.	The TI Datasheet does not anticipate or render obvious 1[A].	36

a.	The Petition is vague and conclusory where the separate limitations of 1[A] are found.....	40
b.	The Petition does not show that the TI Datasheet anticipates or renders obvious 1[A].....	41
3.	The TI Datasheet does not anticipate or render obvious 1[C].	47
4.	The Petition does not provide sufficient evidence to support its anticipation and obviousness arguments.....	48
a.	The Petition does not provide enough evidence to support its anticipation arguments.....	48
b.	The Petition does not provide enough evidence to support its obviousness arguments.	51
B.	Galinski does not anticipate or render obvious any claims.....	52
1.	Galinski does not describe the requirements of 1[D] that the switches are turned on and off “based on the difference signal so as to charge the bootstrap capacitor.”	53
2.	Galinski does not expressly or inherently describe 1[A]’s bootstrap refresh threshold.”	60
3.	Grounds 2, 3 and 5 fail for the same reasons that I described above.	63
C.	Wong does not render any claim obvious.....	64
1.	Petitioner’s modification of Wong, to replace the Zener diode with a switch, does not meet the claim limitations of 1[PRE] and 1[D].	65
2.	Petitioner does not present a motivation or reason to replace Wong’s Zener diode with a switch.	71
V.	CONCLUSION.....	77

LIST OF EXHIBITS

Exhibit	Description
2001	Declaration of Joseph C. McAlexander III
2002	Joseph C. McAlexander III Curriculum Vitae
2003	MPS Counsel's Identification of Terms in District Court
2004	Microsemi Technical Note, Voltage-Mode, Current-Mode
2005	Micrel Article, Putting Adaptive Constant-ON-Time Buck ICs and Modules to Work
2006	Texas Instruments, Application Report, Adaptive Constant On-Time (D-CAP) Control Study
2007	Evertiq, Application Notes, Part 3: Design considerations of the switching power components
2008	MPS, Article, Advantages of Constant-On-Time Control
2009	Barr Group, Article, How Programmable Logic Works
2010	Sparkfun, Diodes Tutorial
2011	Sparkfun, Transistor Tutorial
2012	ECSTUDIO, Textbooks, Chapter 4, The Transistor as a Switch
2013	ECSTUDIO, Textbooks, Chapter 2, Junction Field-Effect Transistors
2014	Electronics-Tutorials.ws – The Zener Diode
2015	Electronics-Tutorials.ws – Transistor Biasing
2016	Electronical Engineering – Stack Exchange Online Forum re. Usage of a transistor configured as diode

I, Joseph C. McAlexander ^{III} declare as follows:

1. I have been retained as an expert consultant by Perkins Coie LLP on behalf of Monolithic Power Systems, Inc. (“Patent Owner”) in this proceeding before the United States Patent and Trademark Office (“PTO”) initiated by Reed Semiconductor Corp. (“Petitioner”) regarding U.S. Patent No. 9,590,608 (“the ’608 Patent”) (Ex 1001). I have been asked to provide my technical review, analysis, insights, and opinions regarding the references that form the basis for the alleged grounds of unpatentability set forth in the Petition. For this service, I am being compensated for my time, and I am reimbursed for actual expenses. I have no interest in the outcome of this proceeding, and my compensation is not dependent on the content of my opinions or the outcome of this proceeding.

I. INTRODUCTION AND QUALIFICATIONS

2. I am an independent consultant. All opinions stated in this Declaration are based on my own personal knowledge and professional judgment. In forming my opinions, I have relied on my knowledge and experience relating to the technology referenced in this Declaration.

3. I am over 18 years of age and, if I am called upon to do so, I would be competent to testify as to the matters set forth herein. A copy of my current curriculum vitae, which includes a more detailed summary of my education and professional and academic experience is provided as Appendix A to this Declaration.

The following provides an overview of some of my experience that is relevant to the matters set forth in this Declaration.

A. Qualifications

4. I am a Registered Professional Engineer (#79454) and the President of M^cAlexander Sound, Inc. I hold a Bachelor of Science degree in Electrical Engineering from North Carolina State University. I have been associated with the integrated circuit and electronics industry as a designer and consultant for the past 52 years and am a named inventor on 31 U.S. patents and a number of foreign patents.

5. I have extensive expertise in the subject matter area relevant to this matter, specifically the design, fabrication, and testing of integrated circuits, including that of power and timing control circuits embedded in integrated circuits. For example, I have over fourteen years of experience at Texas Instruments. There, I designed, developed and implemented circuits, processes, and procedures to assure product and process reliability. More specifically, I designed and managed the processing and productization of many types of integrated circuit devices, including, among others, dynamic and static storage devices, charge coupled devices (CCD) for imaging applications, electrically programmable and erasable non-volatile devices (EPROM / EEPROM) for instruction storage and access, logic devices, and controllers. I also was responsible for the design and use of many performance

boards used in testing and performance characterization of integrated circuits as well as the creation and implementation of the testing programs used to evaluate the performance characteristics of the integrated circuits. These boards required power control and signal stability for accurate assessment of device performance under various timing and power requirement conditions, adjusted according to specific, current circuit operation and load demands.

6. Additionally, while at EPI for 5 years, I managed activities which included board designs that required power and signal control. Specifically, my experience in the industry and with engineers practicing in the industry informs my opinion as to the level of skill of individuals and the general state of the art.

7. Specifically, I have:

designed memories, including Dynamic Random Access Memories (DRAMs), Static Random Access Memories (SRAMs), Charge Coupled Devices (CCDs), Shift Registers (SRs), and functional circuits including I/O buffers for address and data, decoders, clocks, sense amplifiers, fault tolerant (incorporating both nonvolatile EPROM and random access memory components), parallel-to-serial data paths for video applications, level shifters, converters, pumps, and logic, as well as wireless communication systems and MEMs;

managed operations including engineering, training, and quality assurance for device fabrication, assembly, test, analysis, and reliability assessment, as well as manufacturing control, each of which involved both volatile and non-volatile memory; testing, analysis, and control involved use of mechanical calibration and measuring equipment, including optical, scanning e-beam, IR, capacitive, and laser using phase contrast and FFT for HARI applications;

taught courses in solid-state device physics, integrated circuit design, integrated circuit fabrication, and statistical control;

provided expert services, investigating both process and design technologies of various devices (microprocessor and controller, volatile and non-volatile memory, programmable logic, card, tag, module, mixed signal, custom, and other), systems (PC and peripheral, computer, control, laser measurement, switch, architecture, software, and other), consumer products (medical, TV, telephone, VCR, facsimile, copier, lighting, game, and other), and products related to wireless tracking and geofencing; and

designed and managed development, testing, and evaluation of memory devices and systems incorporating such devices, including simulation of operation. I have also had experience in programming, erasing, and wearout of electrically programmable and erasable non-volatile memories.

8. I am qualified to reach the opinions and conclusions stated in this Declaration.

9. In forming my opinions, I rely on my knowledge and experience in the fields relevant to this Declaration. I further rely on documents and information referenced in this Declaration.

10. A more detailed account of my work experience and other qualifications is listed in my Curriculum Vitae attached to this Declaration.

B. Materials Reviewed

11. The opinions contained in this Declaration are based on the documents I have reviewed, my professional judgment, and my education, experience, and knowledge relating to power control and related fields. In forming my opinions, I

have reviewed all materials referenced by the Petition and Dr. Holberg's report and all materials listed in the List of Exhibits provided above (as well as any other materials and information I reference in this Declaration).

12. My opinions contained in this Declaration are based on the documents I have reviewed and considered, as well as my knowledge and professional judgment. My opinions have been guided by my appreciation of how a person of ordinary skill in the art ("POSITA") would have understood the state of the art, the prior art, and the claims and the specification of the '608 Patent at the time of the alleged invention.

13. The time of the alleged invention of the '608 Patent encompasses the time frames near and including August 11, 2014. I understand the application for the '608 Patent claims priority to a Chinese patent application (CN application No. 201410390708/2), which was filed on August 11, 2014. (Ex. 1001, 1:8-10). My opinions reflect how a POSITA (which I describe below) would have understood the '608 Patent, the prior art to the patent, and the state of the art at the time of the alleged invention.

C. Summary of My Opinions

14. The challenged claims of the '608 Patent are not anticipated or rendered obvious under 35 U.S.C. §§ 102 and 103 based on Petitioner's grounds shown in the table below:

Ground	Claims	Description
1	1, 11, 12	Anticipated and/or obvious under §102/103 by TI.
2	1, 11, 12	Anticipated under §102 by Galinski.
3	1, 2, 11, 12, 16	Obvious under §103 by Galinski in view of Li.
4	1, 6, 11, 12, 15	Obvious under §103 by Wong.
5	6, 15	Obvious under §103 by Galinski or, in the alternative, Galinski in view of Wong.

15. Based on my experience and expertise, it is my opinion that the prior art fails to disclose and/or suggest all the limitations recited in challenged claims of the '608 Patent, as I discuss in detail below.

II. UNDERSTANDING OF LEGAL PRINCIPLES AND PERSPECTIVES

16. I am not a lawyer, and I will not provide legal opinions. Although I am not a lawyer, I have been advised that certain legal standards are to be applied by technical experts in forming opinions regarding the meaning and validity of patent claims.

17. I understand that a patent claim is invalid if it is anticipated or rendered obvious over the prior art and that a claim can be unpatentable even if all requirements of the claim cannot be found in a single prior art reference. I further understand that invalidating a claim requires that the claim be anticipated or rendered obvious from the perspective of a POSITA at the time the invention was made.

18. In forming my analysis, opinions, and conclusions expressed in this Declaration, I have applied the legal principles set forth below, which were provided to me by counsel for Patent Owner.

A. Types of Claims

19. I understand that there are two types of U.S. patent claims: 1) independent claims, and 2) dependent claims. I understand that independent claims only include the aspects stated in the independent claim. I further understand that dependent claims include the aspects stated in the independent claim, and any other aspects stated in any claim from which that dependent claim depends, as well as any limitations required by the dependent claim.

B. Anticipation

20. I understand that a claim in an issued patent can be invalid if it is anticipated. In this case, “anticipation” means there is a single prior art reference that discloses every element of the claim, arranged in the way required by the claim, either expressly or inherently.

21. I understand that anticipation of a claim requires that every element of a claim is disclosed expressly or inherently in the single prior art reference. I understand that “inherent” disclosure means that the claim element, although not expressly described by the prior art reference, must necessarily be present based on

the disclosure. I understand that a mere probability that the element is present is not sufficient to qualify as “inherent disclosure.”

C. Obviousness

22. I understand that a claim in an issued patent can be rendered invalid if it is obvious. Unlike anticipation, obviousness does not require that every element of the claim be in a single prior art reference. Instead, it is possible for claim elements to be described in different prior art references, so long as there is motivation or sufficient reasoning to combine the references and a reasonable expectation of success.

23. I understand that a claim is invalid for obviousness if the differences between the claimed subject matter and the prior art are such that the subject matter as a whole would have been obvious from the perspective of a person of ordinary skill in the relevant art at the time the invention was made. I also understand that, when evaluating obviousness, one must consider obviousness of the claim “as a whole.” This must be from the perspective of the person of ordinary skill in the relevant art at the time the invention was made.

24. I further understand that exemplary rationales that may support a conclusion of obviousness include:

- a) combining prior art elements according to known methods to yield predictable results;
- b) simple substitution of one known element for another to obtain

predictable results;

- c) use of known technique(s) to improve similar devices (methods or products) in the same way;
- d) applying a known technique to a known device (method or product) ready for improvement to yield predictable results;
- e) “obvious to try” - choosing from a finite number of identified, predictable solutions with a reasonable expectation of success;
- f) known work in one field of endeavor may prompt variations of the work for use in either the same field or a different field based on design incentives or other market forces if the variations are predictable to a POSITA; and
- g) some teaching, suggestion, or motivation in the prior art that would have led a POSITA to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

25. In analyzing obviousness, I understand that it is important to understand the scope of the claims, the level of skill in the relevant art, the scope and content of the prior art, the differences between the prior art and the claims, and any “secondary considerations” (described below). I also understand that, if a technique has been used to improve one device, and a POSITA would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill. Although I understand that it is not required, there may also be a specific “teaching, suggestion or motivation” to combine any first prior art reference with a second prior art reference. Such a “teaching, suggestion, or motivation” to combine the first prior art reference with the second

prior art reference can be explicit or implicit and may provide further evidence of obviousness.

26. I understand that secondary (or objective) considerations are relevant to the determination of whether a claim is obvious. Such secondary (or objective) considerations can include evidence of commercial success caused by an invention, evidence of a long-felt need that was solved by an invention, evidence that others copied an invention, or evidence that an invention achieved a surprising or unexpected result, among others. I understand that such evidence must have a nexus, or causal relationship to the elements of a claim, to be relevant to a determination of obviousness of the claim.

27. I also understand that, at least in IPR proceedings, admissions in the patent or in the prosecution file history of the patent (Applicant Admitted Prior Art or “AAPA”) can be used to establish background knowledge possessed by a POSITA, to furnish a motivation to combine, to assess whether a patent’s claims would have been obvious, and/or to supply a missing limitation.

D. Claim Construction

28. I understand that, for purposes of my analysis, the terms appearing in the patent claims should be interpreted according to their “ordinary and customary meaning” at the time the alleged invention was made. In determining the ordinary and customary meaning, the words of a claim are given the plain meaning that those

words would have had to a POSITA. I understand that the structure of the claims, the specification, and the file history also may be used to assist in the construction of a claim term. Additionally, treatises and dictionaries may be used, in limited circumstances, to determine the meaning attributed by a POSITA to a claim term at the time of filing as long as such extrinsic input is consistent with the claim term as used in the claim.

29. For all claim terms considered in this Declaration, I have applied the ordinary and customary meaning of those terms as they would have been understood by a POSITA at the time the alleged invention was made. To the extent the Patent Owner proposes any constructions, or the Board construes any claims, I reserve the right to address such proposals or constructions. Under any reasonable construction of the claims, it is my opinion that the prior art does not disclose and/or suggest all the limitations recited in challenged claims of the '608 Patent.

E. Person of Ordinary Skill in the Art

30. I understand that my assessment and determination of invalidity must be undertaken from the perspective of what would have been known or understood by a POSITA at the time of the earliest patent application supporting the '608 Patent.

31. I have been informed and understand that the POSITA is not a real person, but rather a legal construct—a hypothetical person. This person is presumed to have known the relevant art at the time of the invention. I have been informed by

counsel that relevant factors in determining the level of ordinary skill include (1) the educational level of the inventor, (2) the type of problems encountered in the art, (3) prior art solutions to those problems, (4) the rapidity with which innovations are made, (5) sophistication of the technology, and (6) the educational level of active workers in the field. I further understand that the person of “ordinary skill” is not a person of extraordinary skill in the art. In other words, this person of ordinary skill is not necessarily an expert in the field.

32. As of the alleged August 11, 2014 priority date, a POSITA would have had a bachelor’s degree in Electric Engineering or equivalent, and approximately two years of experience working in the field of power converters, circuit design, device physics, or related technologies. Lack of work experience can be remedied by additional education, and vice versa.

33. At the time of the alleged invention, I was a person of at least ordinary skill in the art, and I have applied the perspective of the POSITA in forming and expressing my opinions below.

III. BACKGROUND OF THE ’608 PATENT

34. The ’608 Patent is directed to switch-mode voltage converters that rely on a bootstrap capacitor. (EX1001, 1:14-17, 3:37-42). The basic structure of a prior art switch-mode voltage converter is illustrated in Figure 1 of the ’608 Patent. As shown in annotated Figure 1 below, switch-mode converters can function by using

a **high side switch** and a **low side switch**. (EX1001, 1:30-31). The **high side switch** is turned on or off to regulate how much voltage from the input voltage (V_{IN}) is output from the converter (V_{OUT}). For example, if V_{IN} is 3.3V, the converter could turn on and off in such a way that V_{OUT} is around 2.7V on average.

35. The **high side switch** needs a “driver,” not shown in Figure 1, to turn the **high side switch** on. (EX1001, 1:61-63). That driver must receive a voltage higher than the input voltage in order to function correctly and to turn on completely. (EX1001, 1:65–2:22). Thus, a “**bootstrap capacitor**” (C_B), which stores a voltage charge, is coupled to the **high side switch**’s driver in order for the driver to receive the input voltage plus the **bootstrap capacitor**’s stored voltage so that the **high side switch** can fully turn on. (EX1001, 2:45-59).

36. When the **high side switch** is driven (*e.g.*, turned on), the **bootstrap capacitor** discharges its stored voltage into the **high side switch**’s driver. (EX1001, 2:15-22, 2:45-49). Thus, the bootstrap capacitor needs to be charged at certain times (*e.g.*, “refreshed”) in order to adequately drive the **high side switch**. (EX1001, 2:55-59, 2:35-40). The bootstrap capacitor is recharged (*e.g.*, “refreshed”) when the **high side switch** is off and the **low side switch** is on. (EX1001, 2:55-59, 2:35-40). The **low side switch** must remain on (and consequently the **high side switch** must remain off) for a certain time period long enough to charge the **bootstrap capacitor**. (EX1001, 2:55-59, 2:35-40).

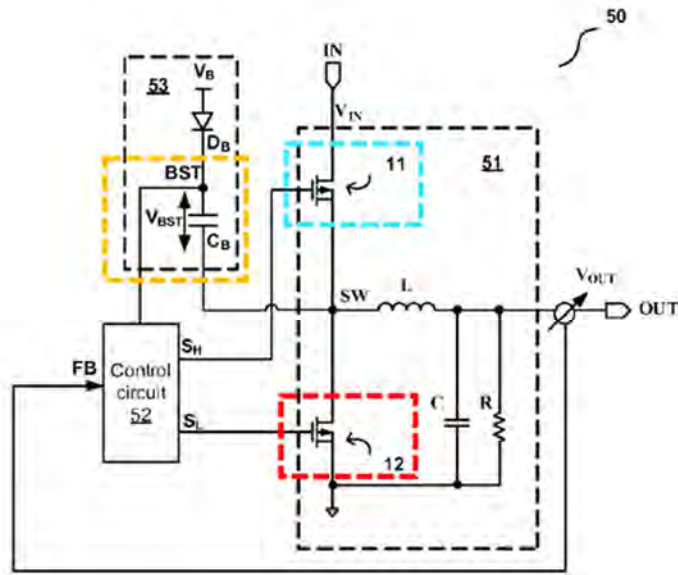


FIG. 1 (Prior Art)

37. The '608 Patent describes that there can be operational problems in the general switch-mode converters described above when they rely on a bootstrap capacitor. For example, when the converter needs to output a voltage that is near or at the same level of the input voltage, the high side switch always is on, and thus, the bootstrap capacitor is not adequately refreshed because the low side switch cannot turn on long enough. (EX1001, 3:3-9). As another example, when the voltage converter operates in light load or no load condition, the conduction time or switching frequency of the switches is reduced, and thus, the bootstrap capacitor might not be fully charged because the low side switch was not turned on long enough or it had not been turned on for a relatively long time. (EX1001, 3:10-18).

38. The '608 Patent solves these issues. First, the '608 Patent describes a bootstrap refresh module comprising a **first comparing module**, illustrated in green in the exemplary annotation of Figure 3 reproduced below. (EX1001, 19:9-10). This module compares the *bootstrap voltage signal* (V_{BST}) with a *bootstrap refresh threshold* (V_{TH1}), and outputs a *first comparing signal* with two logic states. (EX1001, 19:10-20, 9:10-20, 10:60-63, 11:1-6, 12:15-29). The first logic state exists when the bootstrap voltage signal (V_{BST}) is lower than the bootstrap refresh threshold (V_{TH1}). (EX1001, 9:14-16, 10:60-63, 11:1-6, 12:15-29). Second, the '608 Patent describes a **voltage difference module**, illustrated in blue in the exemplary annotation of Figure 3 reproduced below. (EX1001, 7:16-27, 8:31-33, 10:60-63, 11:16-17, 13:9-11). This module compares a *feedback signal* (FB) with a *reference voltage* (V_{REF}) representing a desired value of the output voltage of the voltage converter, and outputs a *difference signal* (EA). (EX1001, 7:16-27, 8:31-33, 10:60-63, 11:16-17, 13:9-11).

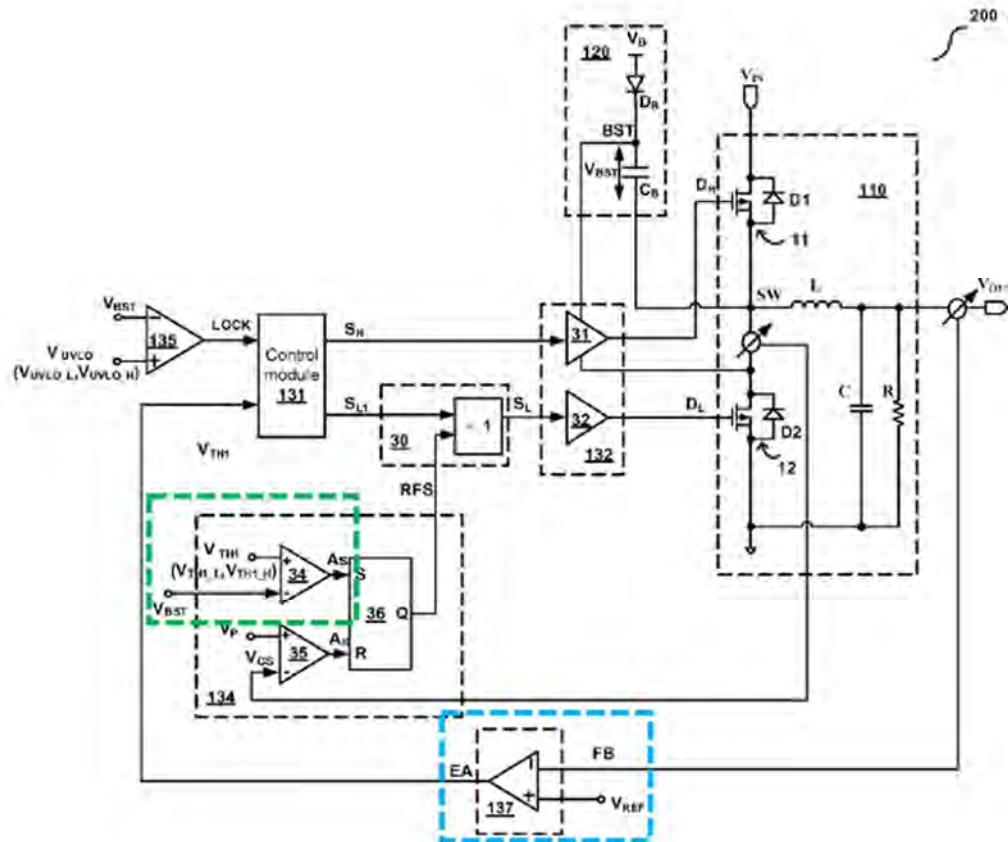


FIG. 3

39. These two modules work to control, and maintain, the output voltage (V_{OUT}) to ensure that the bootstrap capacitor recharges adequately. I discuss these in turn.

40. First, when the *first comparing module* has the first logic state (*e.g.*, when the bootstrap voltage signal is lower than the bootstrap refresh threshold ($V_{BST} < V_{TH1}$)), the bootstrap refresh module is configured to decrease the output voltage of the voltage converter. (EX1001, 19:39-41, 8:26-30, 8:58-9:2, 9:42-49, 12:6-9, 14:47-49).

41. As a non-limiting example, the exemplary annotated Figure 5 below illustrates this behavior in one embodiment. Figure 5 is directed to the voltage converter operating a light load. (EX1001, 15:3-5). Because the converter has a light load, V_{OUT} does not decrease from t_0 to t_1 . (EX1001, 15:3-5). However, as shown by the illustrated green arrows in Figure 5 below, the bootstrap capacitor will naturally dissipate its charge, and thus, V_{BST} decreases over time. (EX1001, 15:8 (“[T]he bootstrap voltage (V_{BST}) is dropped.”). When V_{BST} reaches a threshold V_{TH1} , the low side switch L_S pulses on (from t_1 to t_2), and thus, the bootstrap capacitor is charged (V_{BST} increases). (EX1001, 15:16-17, 22-23). Because the low side switch L_S is pulsed on, the output voltage V_{OUT} decreases because there is no input voltage out of the converter and the switching node is pulled to ground. The output voltage continues to decrease until time t_3 . (EX1001, 15:16-21, 15:42-49, 2:35-37). Thus, when the bootstrap voltage signal is lower than the bootstrap refresh threshold, the output voltage is decreased.

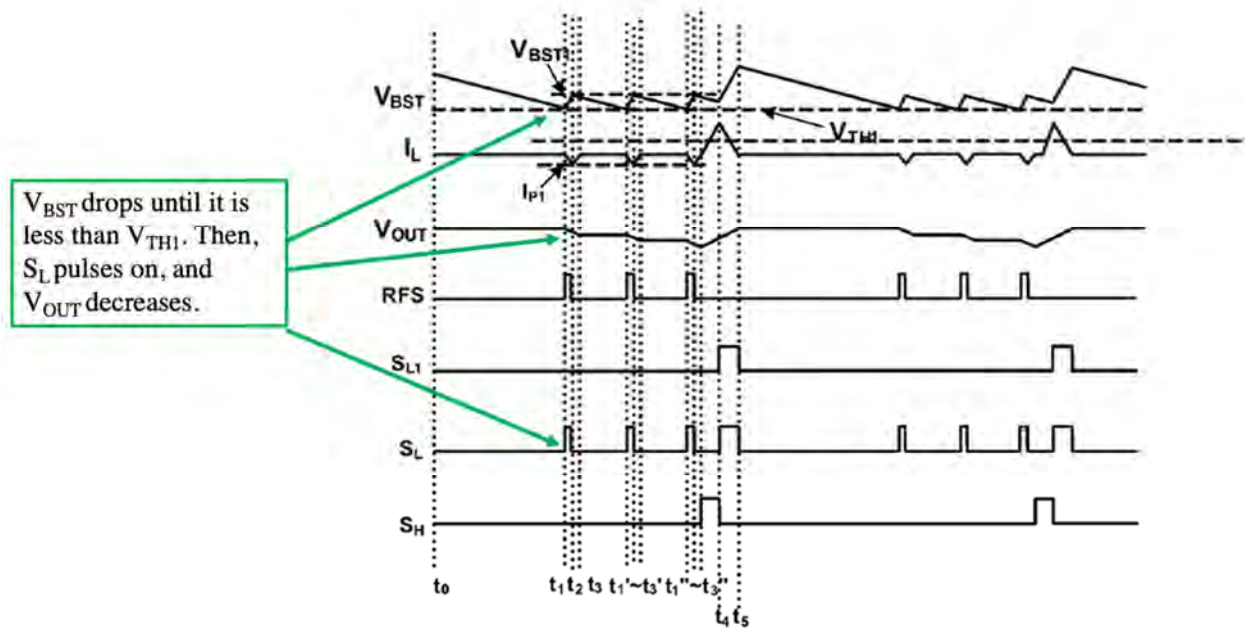
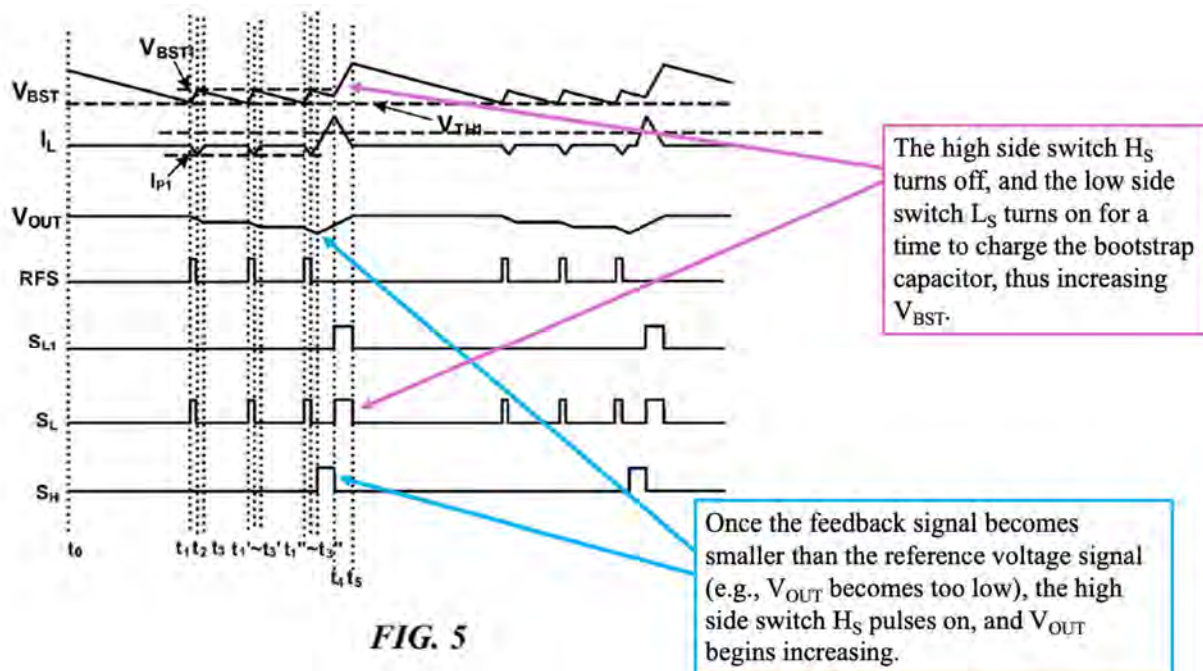


FIG. 5

42. Second, (*e.g.*, because of the voltage difference module), when the feedback signal is smaller than the reference voltage signal, the high side switch and low side switch are switched on and off based on the difference signal so as to charge the bootstrap capacitor for refreshing the bootstrap voltage signal. (*E.g.*, EX1001, 8:34-40, 11:18-23).

43. As a non-limiting example, the exemplary annotated Figure 5 below further illustrates this behavior in one embodiment. As shown in the blue arrows in the exemplary annotation reproduced below, once the feedback signal (FB) becomes smaller than the reference voltage signal (V_{REF}) (*e.g.*, V_{OUT} drops too low), the high side switch (S_H) turns on and the output voltage V_{OUT} increases. (EX1001, 15:53-54 (“[I]n time t_3 ”, the output voltage signal (V_{OUT}) drops to a reference value”), 15:65-

67 (“From time t_3 ” to t_4 , the high side switch 11 keeps on state . . . The output voltage (V_{OUT}) increases”). Then, as shown in the **purple arrows** illustrated in the exemplary annotation of Figure 5 reproduced below, the high side switch (S_H) is turned off and the low side switch (S_L) turns on to refresh the bootstrap capacitor. (EX1001, 16:3 (“At time t_4 , the high side switch 11 is turned off”), 16:11 (“The bootstrap capacitor (CB) can be charged for refreshing the bootstrap voltage (V_{BST})”).).



44. Thus, when the feedback signal is smaller than the reference voltage signal (e.g., the difference signal indicates that V_{OUT} is too low), the high side switch and low side switch are switched on and off based on the difference signal so as to charge the bootstrap capacitor for refreshing the bootstrap voltage signal.

IV. REASONS FOR PATENTABILITY

A. Ground 1 (the “TI Datasheet”)

45. In my opinion, the TI Datasheet does not anticipate or render obvious the claims for a few reasons.

46. First, in my opinion, the TI Datasheet fails to anticipate or render obvious the limitations of 1[D]. As I described earlier, the '608 Patent recites that the high side and low side switches are configured to switch on and off when the feedback signal is smaller than the reference voltage signal. This is reflected in the limitation of 1[D]. The TI Datasheet refers to a device that is a fixed frequency current mode control device. Its high-side switch is turned on via the clock. This is not like the claim requirements of 1[D], which requires that the high-side switch is turned on using feedback. Additionally, the TI Datasheet's high-side switch is turned off via a power switch current.

47. Second, the TI Datasheet fails to teach—or render obvious—the limitations of 1[A], which require a “a first comparing module” that compares inputs (a “bootstrap voltage signal” and a “bootstrap refresh threshold”) and outputs a resulting “first comparing signal.”

48. Third, the TI Datasheet fails to teach or render obvious the limitations of 1[C] which requires that the “bootstrap refresh module” “decrease[s] the output voltage of the voltage converter” based on the “first comparing signal.” Because

Petitioner failed to identify a “first comparing signal,” the functionality performed based on that signal fails.

49. Fourth, in my opinion, the Petition also does not present proper analysis based on anticipation or obviousness. Petitioner and its expert, Dr. Holberg, use repeated conclusory statements of how a “POSITA would understand” to fill gaps in its anticipation arguments for the TI Datasheet. Petitioner and Dr. Holberg also do not describe how those limitations would be obvious to a POSITA.

1. The TI Datasheet does not meet the requirements of limitation 1[D].

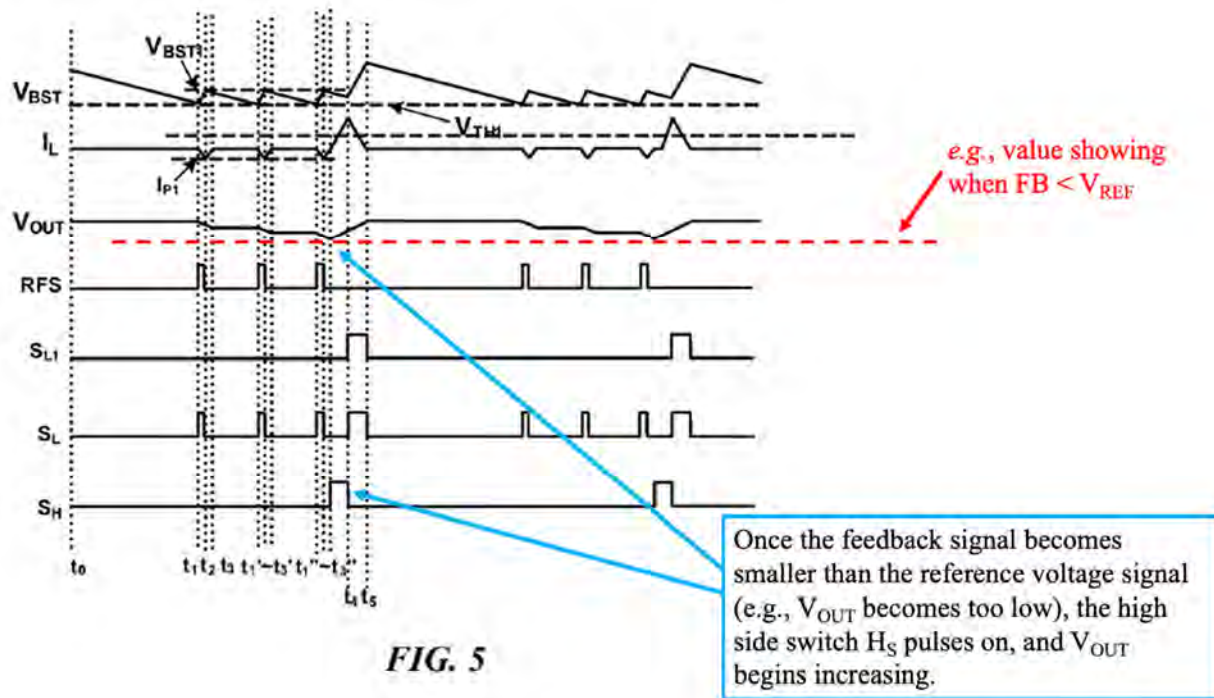
50. In my opinion, the TI Datasheet does not meet the requirements of limitation 1[D]. Limitation 1[D] requires that, “when the feedback signal is smaller than the reference voltage signal, the bootstrap refresh control circuit is configured to control the high side switch and the low side switch to switch on and off based on the different signal so as to charge the bootstrap capacitor for refreshing the bootstrap voltage signal.”

51. The other independent claims 11 and 12 have similar limitations. Limitation 11[F] has a similar requirement to 1[D]. Limitation 12[E] is worded slightly differently. Instead of reciting that the switching of the high and low switches occurs “when the feedback signal is smaller than the reference voltage,” the limitation of 12[E] recites that the switching of the high and low switches occurs

“when the output voltage of the voltage converter is decreased.” Petitioner and its expert appear to treat all three limitations as the same. Thus, when the limitation of 12[E] recites that the switching occurs “when the feedback signal is smaller than the reference voltage,” Petitioner treats this limitation is being met “when the feedback signal is smaller than the reference voltage signal.” Petitioner never defines what “decreased” means, but because Petitioner treats all three limitations as the same, for purposes of my analysis, “decreased” means when an output voltage is below a certain threshold. Thus, all three independent claim limitations occur based on a voltage change. For purposes of my analyses in support of Patent Owner’s Preliminary Response, I adopt this understanding, and my analysis of limitation 1[D] applies equally to limitations 11[F] and 12[E].

52. Figure 5 of the ’608 Patent illustrates limitation 1[D] as a non-limiting example. As I just stated above, the ’608 Patent recites, in part, that when the feedback signal is smaller than the reference voltage signal, the high side switch and low side switch are switched on and off based on the difference signal so as to charge the bootstrap capacitor for refreshing the bootstrap voltage signal. This is important because when the output voltage of the converter (*e.g.*, the feedback signal) drops too low, the high side switch and the low side switch are switched normally to maintain the output voltage V_{OUT} at a desired value. (*E.g.*, EX1001, 8:34-40, 11:18-23).

53. Yet, because the output voltage is sometimes decreasing (*e.g.*, the feedback is decreasing) and sometimes increasing, the feedback signal is not always less than the reference voltage. As a non-limiting example, in Figure 5, annotated and reproduced below, the output voltage V_{OUT} decreases at a time point to a certain reference voltage level. (EX1001, 15:51-52). This reference occurs when the feedback voltage FB (which is representative of the output voltage V_{OUT}) is less than a reference threshold voltage V_{REF} . (EX1001, 15:52-57). When FB is less than V_{REF} (as shown by V_{OUT} reaching the red line), the high side switch S_H turns on (at t_3''), and the output voltage (*e.g.*, the feedback voltage) begins increasing. (EX1001, 15:57-59, 15:65-16:1; see also EX1001, 11:18-23, 12:8-12, 14:49-55).



54. Thus, the triggering event for limitation 1[D] happens “when the

feedback signal is smaller than the reference voltage signal.” In my opinion, this is important for at least two reasons. First, the TI Datasheet describes a different triggering event to turn on the high side switch. Second, this triggering event would inform a POSITA of what type of control architecture the ’608 Patent is describing, and this type of control architecture is very different from the control architecture described by the TI Datasheet. I address each of these in turn.

a. The TI Datasheet does not turn the high side switch on when the feedback signal is smaller than the reference voltage.

55. In my opinion, the TI Datasheet does not meet the claimed turning on of the high side switch when the feedback signal is smaller than the reference voltage based on the difference signal. This is because the TI Datasheet describes that its high side switch is turned on by an oscillator. In other words, the high side switch is turned on every clock cycle. The TI Datasheet describes that it “uses a fixed frequency, peak current mode control” scheme and that the high side switch is *not* turned on *once the feedback signal becomes less than a voltage reference signal*; instead, the high side switch is *always turned on* during a clock cycle, and that switch is turned off when the current across that switch reaches a threshold. (EX1006, 11 (“An internal oscillator initiates the turn on of the high-side power switch. The error amplifier output is converted into a current reference which compares to the high-side power switch current. When the power switch current reaches current reference

generated by the COMP voltage level, the high-side power switch is turned off and the low-side power switch is turned on.”)). Accordingly, in my opinion, limitation 1[D]’s requirement to control the high side switch based on the difference signal “when the feedback signal is smaller than the reference voltage signal” is not anticipated by the TI Datasheet. In fact, the TI Datasheet is different because the internal oscillator initiates the turn on of the high-side power switch.

56. In my opinion, the Petition glosses over this important fact. The Petitioner never grapples with the TI Datasheet’s fixed frequency current control scheme in relation to the requirement that the high side switch turn on when the feedback signal is lower than the voltage threshold. Instead, Petitioner argues that the TI Datasheet anticipates 1[D] because the TI Datasheet’s high side switch and low side switch are controlled, and this control occurs allegedly based on when the feedback signal is less than the reference voltage. (See Petition, 31 (“Furthermore, TI discloses the output of the disclosed error amplifier connected to Power Stage Logic (indirectly, through the HS Current Comparator), and that the Power Stage Logic provides control signals for controlling the high-side and low-side switches. Therefore, a POSITA would understand that TI’s disclosed Power Stage Logic switches on and off the high-side and low-side switches based on the output of the error amplifier, thus charging the bootstrap capacitor. A POSITA would also understand that this would include when the feedback signal is less than the reference

voltage, as described above. Therefore, TI anticipates limitation 1[D].”). But this argument merely states, in a conclusory fashion, that the high and low side switches are controlled during this scenario that includes when the feedback signal is less than the reference voltage. This argument does not support a causal relationship between the feedback signal being less than a reference voltage and the high side switch being turned on as required by the claim which states “when the feedback signal is less than the reference voltage, the bootstrap refresh control circuit is configured to control the high side switch and the low side switch to switch on and off”

57. I reviewed Dr. Holberg’s declaration to see if he addressed this important distinction, but he did not. Dr. Holberg simply states that the switches are turned on and off in multiple modes “including when the feedback signal is less than the reference voltage.” (EX1003, ¶ 133). But this ignores the TI Datasheet’s express description that the high side switch is always turned on by an internal oscillator. Dr. Holberg does not home in on this, and he does not state that a POSITA would deduce a relationship between the high side switch being turned on “when the feedback signal is less than the reference voltage.”

58. Thus, in my opinion, the TI Datasheet does not meet the claimed turning on of the high side switch when the feedback signal is smaller than the reference voltage based on the difference signal.

b. The TI Datasheet describes a fixed frequency control type, which is different from the control type of the '608 Patent.

59. There is also a second reason why the TI Datasheet does not meet the language of limitation 1[D].

60. As I described above, 1[D] requires that the high side switch is turned on during a triggering event—“when the feedback signal is smaller than the reference voltage signal.” This is important because a POSITA would understand that this triggering event covers certain types of “control.” Specifically, as I describe below, a POSITA would understand that such a triggering event to turn on the high side switch would be a control type that would at least encompass a “constant on-time” control type. Conversely, as I also describe below, the TI Datasheet uses a “fixed frequency current mode control” type. These are different types of control; and they initiate the turning on of the high side switch differently.

61. Converters are notoriously “tricky to design,” and slight differences in the architecture of converters present drastically different types of control topologies and resulting behavior in the converters. (EX2004, 1). To understand how a POSITA would view different control topologies, I provide a brief description of them.

62. Converters are generally thought to have three different functional blocks: a power stage, a control stage, and a feedback stage. (See EX2004, 2). The power stage usually consists of the switches, and the input voltage enters this block

and gets converted into the output voltage. (See EX2004, 2). The control stage controls the turning on and off of the switches. (See EX2004, 2). The Feedback stage generally returns a feedback signal to the control stage and helps determine the turning on and off of the switches. (See EX2004, 2).

63. There are numerous types of control modes that can be used in a converter. These control schemes dictate how the converters respond to change (such as when their switches turn on and off in response to behaviors from the converter or the load); and each control mode has its pros and cons and can be more or less desirable depending on the requirements of each application. I discuss below three types of control schemes that are helpful in knowing how a POSITA would understand the '608 Patent. These three control schemes are: 1) fixed frequency voltage mode control; 2) fixed frequency current mode control; and 3) constant on-time control.

(i) Background of Fixed Frequency Modes vs. Constant On-Time modes

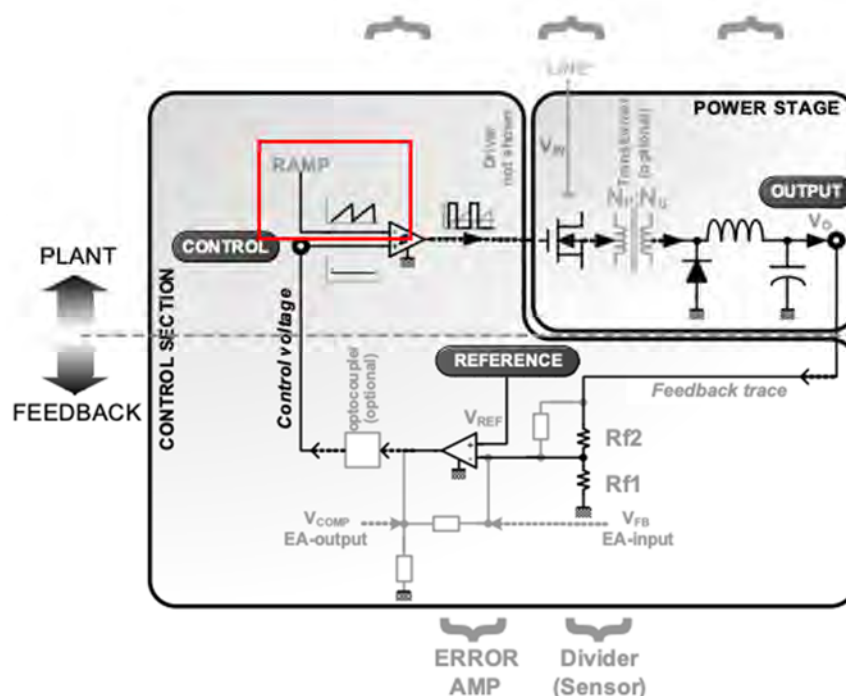
(a) Fixed Frequency Voltage Mode Control vs. Fixed Frequency Current Mode Control

64. Both the fixed frequency voltage mode control and the fixed frequency current mode control types use a clock that determines when the *high side switch turns ON* every clock cycle. (EX2004, 2). They are different in how they determine when the high side switch turns OFF, and this is dictated by their control topology

(e.g., which relates to their feedback architecture). (EX2004, 2).

65. In both the voltage mode control and the current mode control types, the output voltage of the converter is fed back as a control signal. (EX2004, 1-2). This feedback signal enters an error comparator and is compared to a reference voltage. (EX2004, 1-2). An error output signal is then fed into a “PWM comparator,” which compares the error output signal to a **RAMP signal**. (EX2004, 2). The **RAMP signal** is a wave signal generated by the clock. By comparing the feedback signal with the clock signal, the high side switch turns off after a certain duration of a clock cycle. (EX2004, 2).

66. This is shown in the Figure 1 annotated and reproduced below from EX2004, 2.



67. Voltage mode and current mode control types have different **RAMP signals**. (EX2004, 2). In voltage mode, the **RAMP signal** is fixed. (EX2004, 2). Conversely, in current mode, the **RAMP** signal is (1) a sensed switch current (2) mapped into a voltage ramp that is then (3) applied to a PWM comparator. (EX2004, 2). This current mode control is exactly what is described in the TI Datasheet, and I refer to this above when I cite that the TI datasheet uses a “fixed frequency current mode control” type.

68. This can be further seen in the block diagram images reproduced below from EX2006, 1, 2.

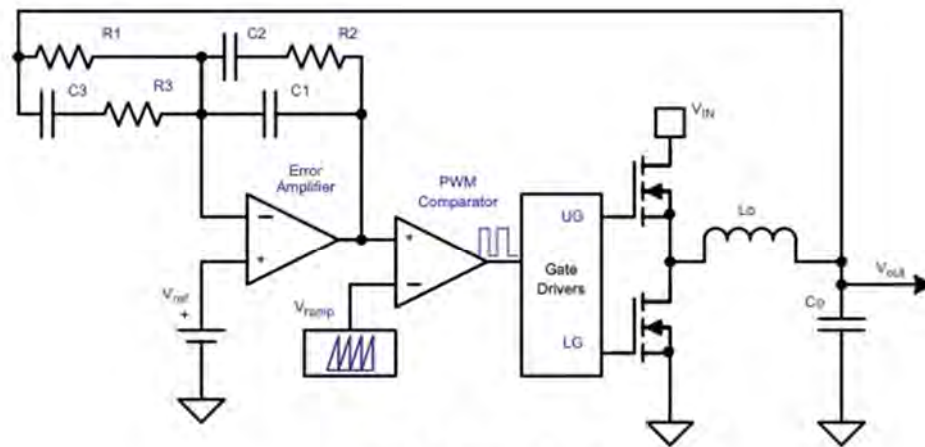


Figure 1. Voltage Mode

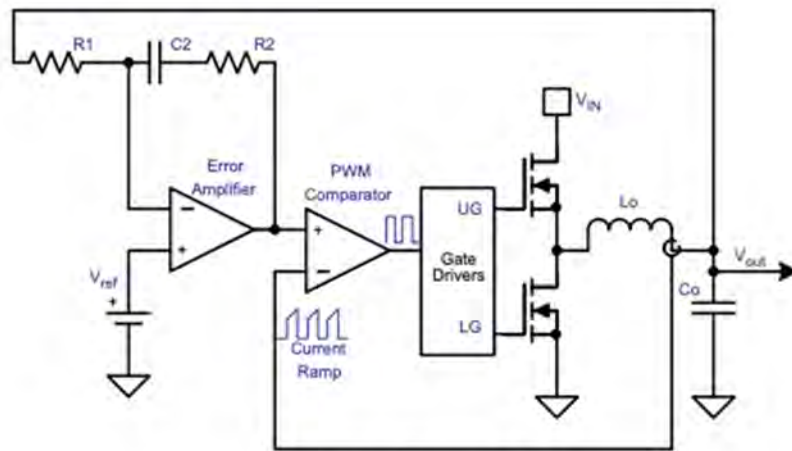


Figure 2. Peak Current Mode

69. Thus, while their architectures seem similar, a POSITA would understand that these small changes have big consequences. For example, current mode control was thought to address many of the issues present in voltage mode control. (EX2004, 1). However, current mode control suffers from what is called “subharmonic instability,” (EX2004, Introduction, 10-11 (form of instability that can be generated when current mode [switching regulators](#) have a continuous inductor current and a duty cycle exceeding 50% and presents a major drawback). With subharmonic instability, the device seems fine under steady state operating conditions, but when there are sudden line or load disturbances, the response of the device is impaired and sluggish. (EX2004, 10, 11). Further, because current mode control depends on sensing the current of the high-side switch and because there is noise generated when the switch turns on, there has to be a minimum on-time of the

high-side switch so that the control scheme does not change based off of noise. (EX2004, 11). This minimum on-time can cause issues in high-voltage to low-voltage down-conversion ratios at high switching frequencies. (EX2004, 11). In these scenarios, voltage mode control is inherently more robust and more noise resistant. (EX2004, 11).

(b) Constant On-Time (“COT”) Control

70. Unlike the voltage and current mode controllers, which rely on a constant switching frequency, Constant On-Time (“COT”) Control turns the high side switch ON based more immediately on the feedback signal (as opposed to having it turn on every clock cycle), and thus responds faster to changes in the converter’s load. (See EX2006, 3). Typical current mode control and voltage mode control topologies have a constant switching frequency generated by the internal clocks. (EX2007, 5). For example, as described above, their high side signals always turn on at the rising edge of a clock cycle. This can impede the converter’s response time to load demand. (See EX2007, 5). For example, if the load changes right after the high side switch is turned off, the converter must wait an entire clock cycle to respond to the changed load. (EX2007, 5).

71. Conversely, in COT control, the COT control mode responds directly to load conditions. When the voltage feedback V_{FB} falls below a reference voltage V_{REF} , the high side switch (also referred to as an active switch) is turned ON.

(EX2005, 2; EX2006, 2 (“Ton is triggered when Vo declines to Vref level)). This is the purpose of COT control and is illustrated in Figure 2 reproduced below taken from EX2005, 2.

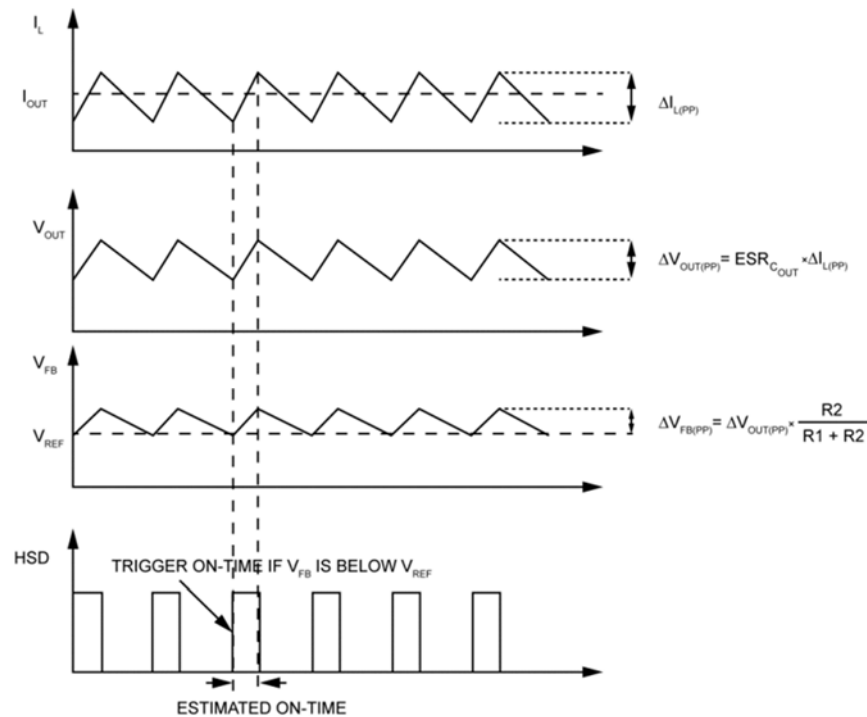


Figure 2. COT control waveforms in a Buck converter

72. COT control provides certain benefits over voltage and current mode control schemes. First, for example, it is easier to design. (EX2006, 3). Second, it can respond faster to transient changes. (EX2006, 3). As shown in the reproduced and annotated Figures 5 and 6 below taken from EX2006, 4, the voltage mode control scheme of Figure 5 has a large voltage dip when moving from a light load to a heavy load, whereas the COT scheme in Figure 6 responds faster and does not have a voltage dip.

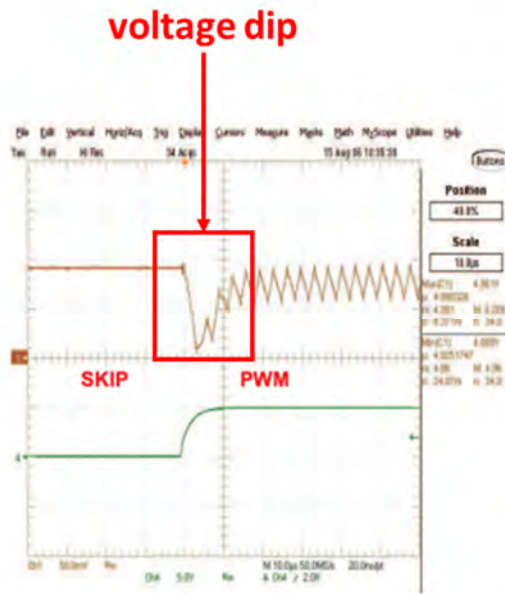


Figure 5. Voltage Mode IC

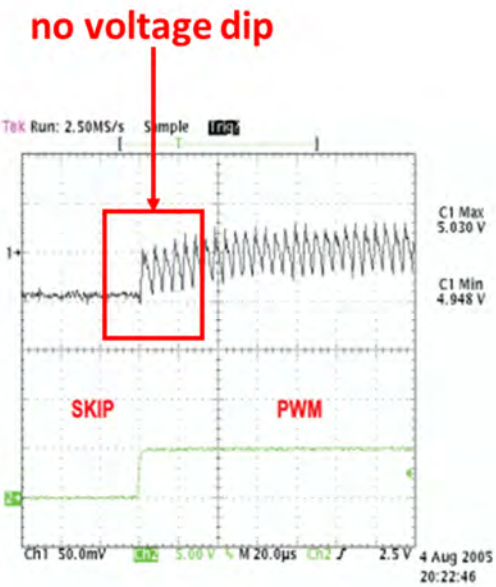


Figure 6. Adaptive On-Time Mode IC

73. And, while EX2008, 4 was published in 2022, Figure 7 (reproduced below) provides another helpful illustration of this concept. It shows that a COT mode responds faster to load changes than current mode control.

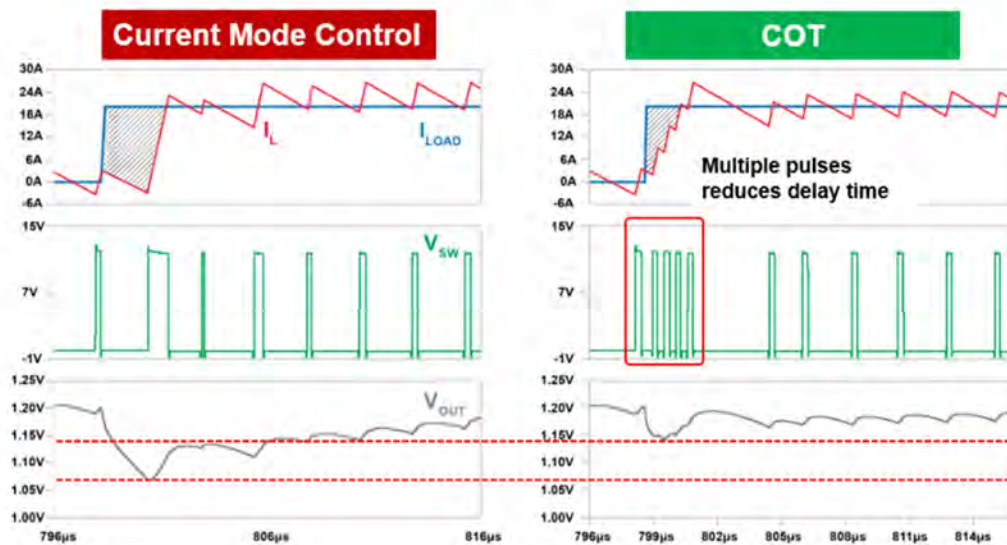


Figure 7: COT Transient Response to Load-Step Compared to a Current Mode Control Scheme

74. While there are multiple ways to implement COT control schemes, they generally rely on using what is called “ripple.” (See EX2006, 3; EX2005, 2). Converters output voltages in a “ripple” format, and the COT topology uses that ripple (*e.g.*, a rippling feedback) to generate a pulse to turn on the high side switch—effectively using the ripple to act as the RAMP signal. (See EX2006, 3 (“This control method uses the output ripple as a PWM ramp signal to compare with the reference voltage to regulate the voltage.”); EX2005, 2 (“In the COT control for buck converter, the threshold crossing of the *falling* output ripple waveform invoked a new active switch ON-time when the V_{FB} waveform crosses the regulation voltage V_{REF} .”)). This is illustrated in a portion of Figure 3 below reproduced from EX2006, 2.

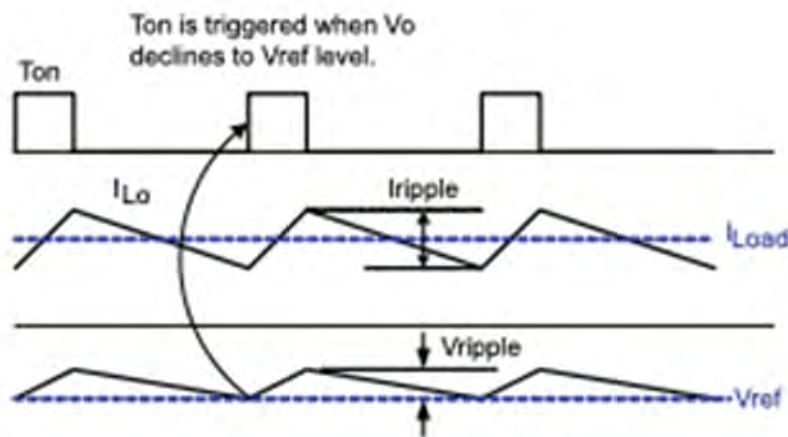


Figure 3. Constant on Time Mode

(ii) The TI Datasheet uses fixed frequency mode, which is different from 1[D].

75. With the above background in mind, it is my opinion that the TI Datasheet is different from the '608 Patent's 1[D] limitation. As I described above, 1[D] requires that the high side switch is turned on during a triggering event—"when the feedback signal is smaller than the reference voltage signal." Accordingly, a POSITA would understand that the triggering event would encompass a control mode such as a COT control mode. This is because the COT control mode turns the high side switch ON based on directly comparing to the feedback signal. (EX2006, 3). Conversely, the TI Datasheet uses a fixed frequency current mode control. (EX1006 at 11). This is different from the triggering event recited in 1[D] in the '608 Patent because a fixed frequency control mode uses a clock to turn the high side switch ON every clock cycle. (EX2004, 2).

76. Accordingly, in my opinion the TI Datasheet does not anticipate or render obvious limitation 1[D].

2. The TI Datasheet does not anticipate or render obvious 1[A].

77. In my opinion, the TI Datasheet does not anticipate or render obvious the limitations of 1[A].

78. The whole context of the claim with Petitioner's lettering identifiers is provided below:

Claim Limitation	Claim Language
1[PRE]	1. A bootstrap refresh control circuit for a voltage converter, wherein the voltage converter comprises a high side switch, a low side switch and a bootstrap capacitor for providing a bootstrap voltage signal to supply a high side driver of the high side switch, and wherein the voltage converter is configured to receive an input voltage at an input terminal and to provide an output voltage at an output terminal based on driving the high side switch and the low side switch to switch on and off, and
1[A]	wherein the bootstrap refresh control circuit comprising: a bootstrap refresh module, wherein the bootstrap refresh module comprises a first comparing module having a first input terminal, a second input terminal and an output terminal, and wherein the first input terminal of the first comparing module is configured to receive the bootstrap voltage signal, the second input terminal of the first comparing module is configured to receive a bootstrap refresh threshold, and the first comparing module is configured to compare the bootstrap voltage signal with the bootstrap refresh threshold to provide a first comparing signal having a first logic state and a second logic state at the output terminal, and wherein the first comparing signal has the first logic state when the bootstrap voltage signal is lower than the bootstrap refresh threshold, and wherein the first comparing signal has the second logic state when the bootstrap voltage signal is larger than the bootstrap refresh threshold; and
1[B]	a voltage difference module having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal of the voltage difference module is configured to receive a feedback signal representing the output voltage of the voltage converter, the second input terminal of the voltage difference module is configured to receive a reference voltage signal representing a desired value of the output voltage of the voltage converter, the voltage difference module is configured to compare the feedback signal with the reference voltage signal so as to provide a difference signal at the output terminal; and
1[C]	wherein when the first comparing signal has the first logic state, the bootstrap refresh module is configured to decrease the output voltage of the voltage converter; and
1[D]	wherein when the feedback signal is smaller than the reference voltage signal, the bootstrap refresh control circuit is configured to control the high side switch and the low side switch to switch on and off based on the difference signal so as to charge the bootstrap capacitor for refreshing the bootstrap voltage signal.

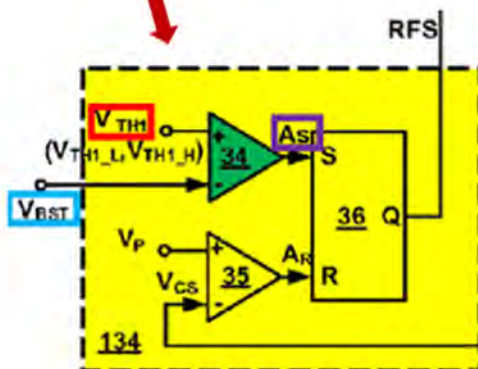
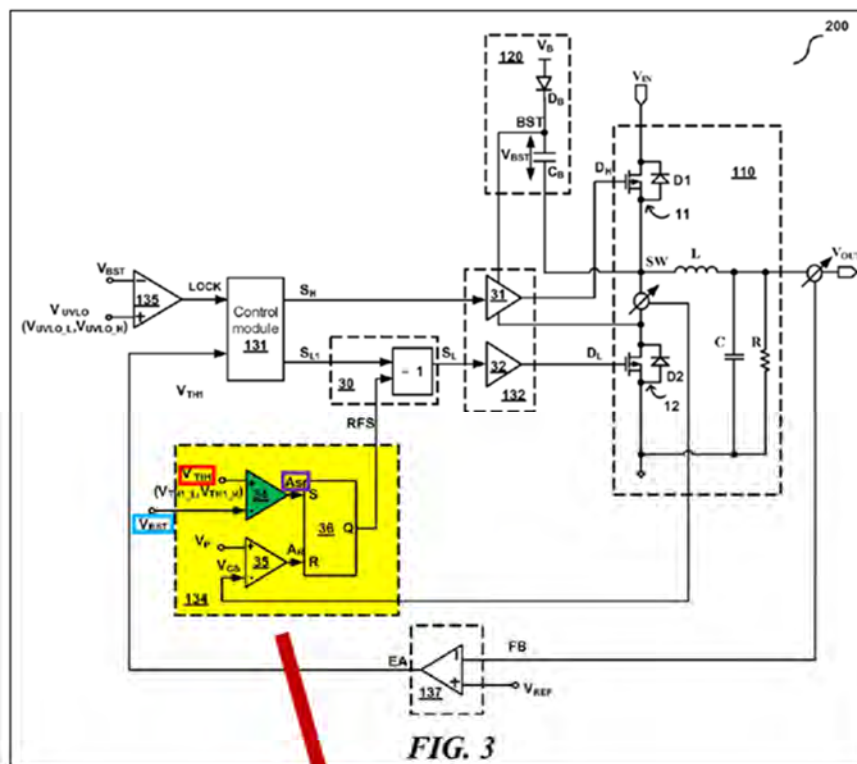
79. Claim 1[A] recites “a bootstrap refresh module, wherein the bootstrap

refresh module comprises a first comparing module having a first input terminal, a second input terminal and an output terminal, and wherein the first input terminal of the first comparing module is configured to receive the bootstrap voltage signal, the second input terminal of the first comparing module is configured to receive a bootstrap refresh threshold, the first comparing module is configured to compare the bootstrap voltage signal with the bootstrap refresh threshold to provide a first comparing signal” (EX1001, 19:9-19). Thus, 1[A] recites a “bootstrap refresh control circuit” that has a “bootstrap refresh module” that comprises “a first comparing module” that compares inputs (a “bootstrap voltage signal” and a “bootstrap refresh threshold”) and outputs a resulting “first comparing signal.” The other independent claims 11 and 12 have similar limitations. (See EX1001, 23:21-32, 24:5-8).

80. Figure 3 of the '608 Patent illustrates the three signals claimed in 1[A]. Figure 3 shows a bootstrap refresh module 134 (yellow)¹ that has a first comparing module (comparator 34, green) that has inputs bootstrap voltage signal (V_{BST}) (blue) and a refresh threshold (*bootstrap refresh threshold* (V_{TH1})) (red), which it compares, and outputs a comparing signal (signal A_S) (purple) based on that comparison.

¹ The “bootstrap refresh control circuit” comprises “a control module 131, a drive module 132, a voltage difference module 137, a bootstrap refresh module 134 and an under voltage lock out module 135.” ('608 Patent at 10:56-60.)

(EX1001 at 19:10-20, 9:10-20, 10:60-63, 11:1-6, 12:15-29.)



81. In my opinion, the TI Datasheet does not expressly or inherently disclose these limitations or even suggest that they exist. In other words, it lacks the “first comparing module” and its two inputs that, respectively, receive signals “bootstrap voltage signal” and “bootstrap refresh threshold,” and one output that

outputs a “first comparing signal”. The Petition does not show that the TI Datasheet anticipates or renders obvious these limitations either. First, the Petition does not specify where the signals and comparator are in the TI Datasheet. Second, the Petition also does not show how the TI Datasheet anticipates or renders obvious the first comparing module and its three signals. I address each in turn.

a. The Petition is vague and conclusory where the separate limitations of 1[A] are found.

82. I understand that a petitioner must specify where each element of the claim is found in the prior art. Here the petition is vague and conclusory when discussing where in the TI data sheet the separate limitations of one 1[A] are found. Specifically, it is not clear where the (1) “bootstrap refresh control circuit,” and separate 1[A] limitations of (2) “bootstrap refresh module,” (3) “first comparing module,” and (4) the signals of the “first comparing module” are found. (See Petition, 25-28).

83. It is hard to figure out what Petitioner’s arguments are, but it appears that Petitioner asserts that the Boot UVLO and Power Stage Logic of the TI Datasheet allegedly meet limitations (1) “bootstrap refresh control circuit” and (2) “bootstrap refresh module,” the Boot UVLO allegedly meets (3) the “first comparing module,” and the inputs/outputs of Boot UVLO allegedly meet (4) the signals of the “first comparing module.” (Petition, 25-28). Thus, in my opinion, the Petition does

not properly show how the TI Datasheet anticipates or renders obvious the limitations of 1[A].

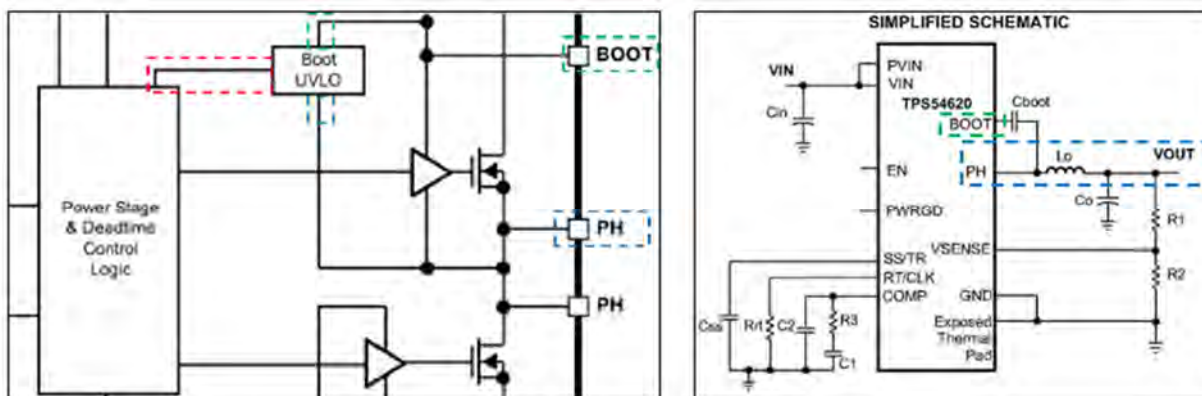
b. The Petition does not show that the TI Datasheet anticipates or renders obvious 1[A].

84. In my opinion, the Petition does not show that the TI Datasheet anticipates or renders obvious 1[A].

85. Petitioner appears to identify Boot ULVO as the claimed “first comparing module. (Petition, 27-28). Petitioner suggests, without offering evidence why, that Boot ULVO satisfies the claimed “first comparing module” that has two inputs and one output that receive/output the claimed signals: “bootstrap voltage signal,” “bootstrap refresh threshold,” and “first comparing signal.” (Petition, 27-28).

86. The TI Datasheet shows a Boot UVLO block in its block diagram. (EX1006, 6). Annotated portions of the TI Datasheet’s block diagram and simplified schematics are shown below and illustrate that the Boot UVLO block has three signal ports for input/output. The TI Datasheet identifies three signals associated, respectively, with these ports: an undescribed signal (annotated red), BOOT (green), and PH (blue). The pin labeled BOOT is a pin that receives an external bootstrap capacitor voltage. (EX1006, 6). The pin labeled PH is the same as the switching node and is inductively coupled to the output voltage (VOUT), and PH is tied to one

terminal of the bootstrap capacitor. (EX1006, 2, 6). This is illustrated below.



87. The purpose of Boot UVLO is to monitor the voltage across the bootstrap capacitor so that the TI device can operate around or near 100% duty cycle. (EX1006, 11).

88. My review of the TI Datasheet indicates that the TI Datasheet, and specifically, the Boot UVLO block, does not anticipate or render obvious the claimed “first comparing module” having two inputs and one output with its respective three separate signals: “bootstrap voltage signal,” “bootstrap refresh threshold,” and “first comparing signal.” These limitations are not expressly or inherently disclosed, and Petitioner does not put forth an obviousness argument.

89. The limitations are not expressly or inherently disclosed for a few reasons. First, the Boot UVLO’s signals do not match the claimed inputs of “bootstrap voltage signal” and “bootstrap refresh threshold.” Boot UVLO’s inputs are from the bootstrap capacitor’s boosted terminal (BOOT) and from the PH pin

which is tied to the other terminal of the capacitor. (EX1006, 2, 6). Thus, the two inputs to Boot UVLO are simply the two sides of the boost capacitor. Even if one were to assume that the BOOT pin could be considered to be the “bootstrap voltage signal,” there is no input into the Boot UVLO block that is the “bootstrap refresh threshold.” Aside from the BOOT pin, the only other input shown is the PH pin. (EX1006, 2, 6).

90. Second, there does not appear to be a comparing of a “bootstrap voltage signal” and “bootstrap refresh threshold.” The TI Datasheet shows that the Boot UVLO block only receives these two inputs from the two terminals of the boot capacitor and uses them to monitor the voltage across the bootstrap capacitor. For example, the voltage across the bootstrap capacitor can be obtained by analyzing the bootstrap capacitor’s BOOT terminal and its other terminal (which is effectively related to PH). (See EX1006, 6, 11).

91. Third, Boot UVLO’s other signal (which is the red signal shown above), does not appear to be the claimed “first comparing signal.” The TI Datasheet is silent on what this signal is for the Boot UVLO block. (EX1006, 6).

92. Accordingly, the signal limitations and the comparison are not expressly or inherently disclosed. Petitioner does not attempt to map these signals for the Boot UVLO block to the signals of 1[A], understandably so since it is clear from the TI datasheet that the required signals are not present and the document is

silent as to what structure and function occurs within the Boot UVLO block.

93. The Petition recognizes this clear lack of evidentiary support and argues that the limitations are inherent. Specifically, the Petition states: “A POSITA would understand from this disclosure that a comparator input receiving the threshold voltage is necessarily present, notwithstanding the simplicity of TI’s high level block diagrams.” (Petition, 27). Even if this analysis were right, which it is not, in my opinion, it still does not describe why the limitations of 1[A] would necessarily exist. I understand that inherency requires that the natural result of the disclosure results in the claimed limitation, and the Petition does not show this. (See Petition, 27). The Petitioner’s proffer is conclusory.

94. Petitioner’s argument that a comparator is inherent within the Boot UVLO block and that the alleged comparator must inherently be wired to provide the claimed signals is also wrong, in my opinion. (Petition, 27-28). The comparator and the inputs and output of limitation 1[A] are not necessarily present in the Boot UVLO block. The TI Datasheet recites that the “The device can operate at 100% duty cycle as long as the boot capacitor voltage is higher than the preset BOOT_PH UVLO threshold which is typically 2.1V.” (EX1006, 11). But this does not mean that a comparator device is necessarily present. The only physical signal provided is the “bootstrap voltage signal,” and any determination that it is higher than a threshold can be done in other ways not involving comparison to a threshold. For

example, there are Programmable Logic Devices (“PDLs”) that can be programmed to execute certain logical functions. EX2009, 3-4). The functionality of the TI Datasheet can be done programmatically to ensure a 100% duty cycle and the “bootstrap voltage signal” can enter as a signal into the PDL. As another example, the Boot UVLO block could be designed in a way such that it uses a diode biased with respect to the bootstrap voltage signal. Diodes, which have been around long before 2014, need a certain amount of “forward voltage,” which is the amount of voltage difference across the diode required for the charge associated with a signal to flow across the diode. (EX2010, 1). Here, the TI Datasheet could just be using a circuit having a diode or network of diodes with a roughly 2.1V trigger level for turn on.

95. This is a different type of circuit element and configuration than the comparator device that Petitioner and Dr. Holberg refer to as the claimed comparator within 1[A]. (See Petition, 27; EX1003, ¶¶ 49-56). Petitioner and Dr. Holberg do not say that a PDL or diode could be the claimed comparator. They refer to a specific comparator device. But the Boot UVLO block does not necessarily have a comparator in order to achieve functions recited in the TI Datasheet. Other devices or circuits could be present instead, and Dr. Holberg does not address this. He simply states, in a conclusory statement that, in his opinion, a comparator would exist. (EX1003, ¶ 126). Nothing in the Petition or the expert declaration arrive at the

conclusion that the limitations of 1[A] are necessarily present.

96. Thus, it is my opinion that the claimed comparator and the two inputs and output recited in 1[A] are not expressly or necessarily present in the Boot UVLO block of the TI Datasheet.

97. Additionally, Petitioner and Dr. Holberg argue that the TI Datasheet would render the limitations of 1[A] obvious, but they do so in a catchall fashion. They just say: “Alternatively, limitation 1[A] is obvious over TI in view of knowledge of a POSITA” (Petition, 28) and “Alternatively, it is my opinion that a POSITA would find limitation 1[A] obvious over TI and other background knowledge in the art because it would be straightforward and obvious to do so” (EX1003, ¶ 126). Petitioner and Dr. Holberg do not describe why a POSITA would have been motivated to or have a reason to include a comparator. Petitioner and Dr. Holberg do not describe why a POSITA would have been motivated to or have a reason to provide a comparator that has the two required, claimed inputs of “bootstrap voltage signal” and “bootstrap refresh threshold” and output of a “first comparing signal.” In my opinion, Petitioner and Dr. Holberg do not provide a sufficient obviousness analysis.

98. Accordingly, it is my opinion that the TI Datasheet does not anticipate or render obvious 1[A].

3. The TI Datasheet does not anticipate or render obvious 1[C].

99. In my opinion, the TI Datasheet does not anticipation or render obvious 1[C].

100. Limitation 1[C] requires that “when the first comparing signal has the first logic state, the bootstrap refresh module is configured to decrease the output voltage of the voltage converter.” (EX1001, Claim 1). The antecedent for the comparing signal is recited in limitation 1[A] and is the output of the “first comparing module.” (See EX1001, Claim 1). Thus, limitation 1[C] requires that the bootstrap refresh module decrease the output voltage of the voltage converter based on the “first comparing signal.” As shown above, the claimed first comparing module is not found in the TI datasheet and thus, the claimed first comparing signal is also not found in the TI datasheet.

101. The Petitioner alleges that the “first comparing signal” is the output of the TI Datasheet’s bootstrap monitor circuit but offers no evidence to support that this signal is responsible for the recited functionality of 1[C]. (Petition, 29 (“The output of TI’s bootstrap-monitor circuit (i.e., the first comparing signal) is connected to the Power Stage Logic, which is configured to provide control signals for driving the high-side and low-side switches”)). In my opinion, there is no tie between any actual signal described in the TI Datasheet and the comparator that Petitioner claimed was inherently present in 1[A], to satisfy the claimed “first comparing

signal” limitation. Accordingly, the Petition does not demonstrate that the TI Datasheet anticipates or renders obvious 1[C].

4. The Petition does not provide sufficient evidence to support its anticipation and obviousness arguments.

102. In my opinion, the Petition does not present a proper analysis based on anticipation or obviousness. First, Petitioner and its expert Dr. Holberg use repeated conclusory statements of how a “POSITA would understand” to fill many gaps in its anticipation arguments for the TI Datasheet. Not only does the TI Datasheet lack express disclosure of many limitations, but Petitioner and Dr. Holberg also do not provide evidence to back up their conclusions, attempting to fill those limitations impermissibly using hindsight reconstruction. Second, Petitioner and Dr. Holberg also do not describe how those limitations would be obvious to a POSITA. I discuss these points in turn.

a. The Petition does not provide enough evidence to support its anticipation arguments.

103. In my opinion, the Petition does not present enough evidence to support its theory that the TI Datasheet anticipates the claims of the ’608 Patent.

104. The TI Datasheet does not expressly or inherently disclose many limitations that are required by the claims. To overcome this, it appears that the Petitioner simply states “a POSITA would understand” followed by language assuming that the limitation recited in the ’608 Patent would be inherently met by

the TI Datasheet. But this, in my opinion, is the Petitioner conducting impermissible hindsight because the Petitioner does not support its conclusions with concrete evidence backing why the TI Datasheet allegedly meets those claims either inherently or expressly.

105. As an example, Petitioner does this improper analysis for 1[A]. Limitation 1[A] recites a “first comparing module” which has two inputs respectively receiving a “bootstrap voltage signal” and a “bootstrap refresh threshold,” and an output that outputs a “first comparing signal.” (See 1[A]). The TI Datasheet does not expressly describe these two inputs and output. Thus, Petitioner fills this gap by stating: “A POSITA would understand from this disclosure that a comparator input receiving the threshold voltage is necessarily present, notwithstanding the simplicity of TI’s high level block diagrams.” (Petition, 27).

106. Petitioner’s assumption is merely that, having no basis in fact and certainly not backed by any support that the claimed structure would be necessarily present. There are many other circuits that could be used to implement some broad functionality described by the TI Datasheet, as I explained above. Because the Petitioner does not show why the comparator with those inputs is the necessary result, it is my opinion that Petitioner failed to present a proper anticipation argument for limitation 1[A]. Further undermining Petitioner’s proffer is that at least one of the required input signals, the “bootstrap refresh threshold,” is clearly not present.

107. As another related example, Petitioner conducts this similar improper analysis for 1[D]. Instead of pointing to an express disclosure for 1[D], Petitioner just recites at length that a “POSITA would understand” that certain limitations are present. This is restated below and taken from Petition, 30-31.

A POSITA would understand that a voltage regulator with integrated MOSFETs would include circuitry that switches the MOSFETs on and off to regulate the output voltage, and that the regulation is based on a difference between a feedback signal and the reference voltage. *Id.* Furthermore, a POSITA would understand that switching the MOSFETs on and off would charge the bootstrap capacitor at least during the time when the high-side switch is off and the low-side switch is on. EX1003, ¶132.

Additionally, a POSITA would understand that at the time when the TPS54620 exits a “pulse skipping” mode of operation (and resumes switching the MOSFETs on and off to regulate the output voltage), the feedback signal will also be below the reference voltage. EX1003, ¶¶69, 133; EX1022, 10-11; EX1023, 12.

Therefore, a POSITA would understand that TI’s disclosed Power Stage Logic switches on and off the high-side and low-side switches based on the output of the error amplifier, thus charging the bootstrap capacitor. EX1003, ¶133. A POSITA would also understand that this would include when the feedback signal is less than the reference voltage, as described above. *Id.*

108. As can be seen from the portion of the Petition repeated above, Petitioner repeatedly states that “a POSITA would understand” recited by functional language in order to allege that the TI Datasheet meets the limitations of 1[D]. I understand that anticipation requires that a reference expressly or inherently disclose

limitations. But because Petitioner does not point to express disclosure in the TI Datasheet, Petitioner attempts to support its anticipation arguments with inherency. Petitioner does that by basing much of 1[D] on a supposed POSITA's understanding, but Petitioner never explains why the limitations of 1[D] are the necessary result of attributes of the TI Datasheet. Instead, Petitioner conducts impermissible hindsight and says that the limitations of 1[D] must be present because a POSITA "would understand" that they are there, a circular argument. Thus, it is my opinion that the Petition has not set forth sufficient evidence to support that the TI Datasheet anticipates 1[D].

109. Accordingly, the Petition does not present enough evidence to support its theory that the TI Datasheet anticipates the claims of the '608 Patent in my opinion.

b. The Petition does not provide enough evidence to support its obviousness arguments.

110. I also understand that, to support an argument of obviousness, the Petitioner must describe how a POSITA would have been motivated to, or have sufficient reason to, combine the references and would have had a reasonable expectation of success. I also understand that the Petitioner must describe the scope of the prior art. Here, however, the Petitioner presents obviousness as an alternative to anticipation, but never offers the additional discussion needed that is required by

an obviousness analysis. (Petition, 28 (“Therefore, TI expressly or inherently anticipates limitation 1[A]. Alternatively, limitation 1[A] is obvious over TI in view of the knowledge of a POSITA.”). Petition cites to Dr. Holberg’s report (EX1003, ¶¶ 49-56, 105, 126), but paragraphs 49-56 just recite general circuit understanding. Paragraph 105 does not have an analysis of why a POSITA would be motivated or have expectation of success, and also ends with obviousness as a catch-all. And paragraph 126 also uses obviousness as a catchall. This is similarly true for limitation 1[C], and Dr. Holberg does not even use obviousness as a catch-all in his support in paragraph 131. (See Petition, 30 (“Therefore, TI expressly or inherently anticipates limitation 1[C]. Alternatively, it would be obvious to a POSITA.”); EX1003, ¶¶ 70-74, 131).

111. Accordingly, the Petition does not provide enough evidence to support its obviousness arguments in my opinion.

B. Galinski does not anticipate or render obvious any claims.

112. It is my opinion that Galinski does not anticipate or render obvious the independent claims of the ’608 Patent for at least two reasons. First, 1[D] requires that the switches are turned on and off “based on the difference signal so as to charge the bootstrap capacitor.” (EX1001, 19:44-47). Petitioner relies on circuitry relating to voltage regulation based on feedback, which would effectively be disabled when the capacitor is being refreshed via circuitry the Petition identified in 1[C]. Second,

Galinski does not anticipate or render obvious a “bootstrap refresh threshold.” I address these in turn.

1. Galinski does not describe the requirements of 1[D] that the switches are turned on and off “based on the difference signal so as to charge the bootstrap capacitor.”

113. It is my opinion that Galinski does not disclose the requirements of 1[D] and that Petitioner has not identified functionality in Galinski to meet 1[D].

114. Limitation 1[D] requires that, once the output voltage has decreased too much (*e.g.*, the feedback signal is smaller than the reference voltage signal), the high side and low side switches are controlled so as to charge the bootstrap capacitor based on the difference signal. (EX1001, 19:42-47). However, the circuitry that the Petitioner relies on to meet 1[D] only relates to regulating an output voltage and does not control the high and low side switches so as to charge the bootstrap capacitor. I describe this below.

115. It is important to understand that Galinski operates its switches in two ways. The switches are operating normally to control the output voltage or they are responding to a reset pulse to recharge the capacitor, and the normal control of the switches is turned off during the reset pulse. Specifically, Petitioner relies on comparator 112 and the reset pulse (V_{RST}) to satisfy 1[A]’s “comparing module” that generates a “comparing signal” and the functionality performed when reset pulse is generated to satisfy 1[C]. (Pet. at 37-39 and 40-41.) Galinsky’s circuit generally

operates in normal switching mode, but when the comparing module generates a short reset pulse to refresh the bootstrap capacitor, this reset pulse toggles the switches (*e.g.*, the low side turns on and the high side turns off), and the normal operation of switching is disabled; once the short reset pulse has happened, the circuit returns to normal operation where the switches are controlled normally, which, in Galinski, is particularly directed towards operating at a 100% duty cycle (meaning the high side switch is always on). (See EX1005, 10:14-23 (“The reset pulse causes the high-side drive control signal to switch to a logical low and the low-side control signal to switch to a logical high for the duration of the reset pulse. The switching of the drive control signals results in switching of the power switches Q1 and Q2. High side power switch Q1 is temporarily turned off while low-side power switch Q2 is temporarily turned on. The switching output voltage V_{SW} therefore switches from input voltage V_{IN} to 0 volt temporarily.”), 9:5-7 (“The reset pulse is of a short duration”), 9:21-23 (“Because the rest pulse is of a short duration, the switching of power switches Q1 and Q2 is only of a short duration.”), 9:23-28 (“When buck regulator is operated at 100% or near 100% duty cycle, the switching of the power switches caused by eh bootstrap voltage control circuit 110 is of such short duration that the overall duty cycle of buck regulator 100 does not deviate appreciably from the 100% or near 100% level), 10:32-35 (“At the end of the recharge phase, buck regulator 100 returns to normal operation where buck regulator

100 is again operated at near 100% duty cycle), 6:25-41 (describing that duty cycle is defined as the percentage of time a power switch is turned on (e.g. the high side power switch is turned on)).

116. Thus, it is my opinion that Galinski operates its switches in two ways—there is a normal operation or there is a reset operation where the switches are briefly forced into a configuration where the high side switch is off and the low side switch is on, and the normal operation does not happen until after the brief reset pulse is finished. The reset pulse is used to recharge the capacitor, and it disables the voltage regulation circuitry’s ability to control the switches.

117. The circuitry for Galinski’s reset pulse and normal operation are different. In its analysis, Petitioner relies on comparator 112 and the reset pulse to satisfy 1[A]’s “comparing module” that generates a “first comparing signal” and 1[C]’s functionality of performing a reset pulse based on the “first comparing signal.” (Petition, 37-39, 40-41). Galinski describes that the normal operation circuitry is a feedback loop that regulates the output voltage by modulating the duty cycle of the device. (EX1005, 5:30-32 (“Power switches Q1 and Q2 are turned on alternately to generate a switching output voltage VSW at the switching output voltage node 120”), 5:56-59 (“For example, buck regulator 100 typically includes a feedback control loop (not shown) formed by driving down the output voltage VOUT (on node 130) to provide a feedback voltage VFB and feeding back the

feedback voltage VFC”), 6:2-7 (“The feedback control loop operates to regulate the output voltage V_{OUT} at a constant level over changing load conditions by varying the duty cycle of power switches Q1 and Q2. That is, the high-side switch Q1 and the low-side switch Q2 are turned on alternately to increase or decrease the inductor current through inductor L1.”), 6:25-41 (describing that the duty cycle is the percent time-on of the high side switch).

118. Galinski never teaches that the normal operation of the high and low side switches charges the bootstrap capacitor. Specifically, Galinski states that the normal operation can turn on both the high and low side switches, but there is no indication that the low side switch is ever turned on long enough to charge the bootstrap capacitor during normal operation because Galinski is directed at achieving a 100% duty cycle, meaning that high side switch is always on, and the low side switch is always off. (EX1005, 4:11-13 (“In this manner, the switching regulator can maintain a duty cycle approaching 100% to avoid voltage dropout...”), 6:16-17 (“the output voltage V_{OUT} of the switching regulator is regulated by controlling the duty cycle”), 6:33-35 (“the duty cycle is also equivalent to the amount of time within a systems clock cycle the high-side switch Q1 is turned on”), 8:12-14 (“conventional N-channel buck regulators limits the duty cycle of the regulators to less than 100%”), 8:16-25 (“In accordance with the present invention ... buck regulator 100 can be operated at near 100% duty cycle when needed to generate the

desired output voltage V_{OUT} . Switching of the power switches Q1 and Q2 occurs only when bootstrap voltage control circuit 110 determines that the bootstrap voltage V_{BOOST} has decayed....”). Thus, Galinski does not describe using the normal mode to charge the capacitor.

119. Petitioner relies upon the circuitry that is disabled during a capacitor recharge (voltage regulation via feedback loop) to meet the elements of 1[B] and 1[D]. Specifically, Petitioner relies on the feedback control loop discussed in Galinski which is used to turn on and off the switches to regulate the output voltage and control the duty cycle. (EX1005, 2:30-36, 6:25-36; Petition, 39-40, 41-41). Limitation 1[D] requires that the circuit “control the high side switch and the low side switch to switch on and off based on the difference signal so as to charge the bootstrap capacitor.” (EX1001, 19:42-48). But this feedback circuitry which regulates the output voltage is not the circuitry that charges the bootstrap capacitor, as I described above. That is done by the pulse reset circuitry which is identified by Petitioner as the circuitry allegedly meeting limitations 1[A] and 1[C] (*e.g.*, comparator 112 and reset pulse (V_{RST})). (See Petition, 37-39, 40-41). As I described above, this pulse reset circuitry disables the normal switching of the high and low switches. As a result, the circuitry of 1[A] and 1[C] precludes the controlling of switches to charge the capacitor because the comparator (112) is used to charge the bootstrap capacitor. Accordingly, it is my opinion that the Petition does not show

how Galinski anticipates or renders obvious 1[D].

120. The Petitioner makes conclusory arguments trying to tie 1[D] to Galinski but does not address this distinction that the reset pulse mode disables the normal control of the high and low side switches. (See Petition, 41-42). To salvage this, Petitioner relies on Dr. Holberg's statements that 1[D] must be met because it was well known that, during a "soft start," the feedback signal would be below the reference voltage and that it was also well known during a "pulse skipping" mode that the feedback signal would be below the reference voltage. (Petition, 42, EX1003, ¶¶ 69, 107 163). These statements do not show that 1[D] is met, in my opinion, for at least four reasons.

121. First, the Petition never explains how a soft start mode or pulse skipping mode would charge the bootstrap capacitor based on a difference signal. (Petition, 42). The capacitor reset pulse in Galinski is not controlled by the "difference signal," which is based on feedback from the output voltage of the circuit. The difference signal is based off of feedback from the output voltage and, by its very nature, the feedback signal would only have a value if the output is being driven and operational, *i.e.*, the circuit began generating V_{OUT} . And, once the circuit is operating and driving an output voltage, the only circuit controlling the capacitor recharge is comparator 112, as described above.

122. Second, Galinski never describes a "soft start" or "pulse skipping"

mode, and these modes would not exist whenever a reset pulse is generated according to Galinski. Galinski immediately returns to normal operating conditions after the very short reset pulse. (EX1005 at 9:5-7, 9:21-23, 10:18-23, FIG. 3.) Also, Galinski states that “the switching of the power switches caused by bootstrap voltage control circuit 110 is of such short duration that the overall duty cycle of buck regulator 100 does not deviate appreciably from the 100% or near 100% level.” (*Id.* at 9:25-28.) Galinski is directed at always maintaining a 100% duty cycle and does not describe the “soft start” or “pulse skipping” modes.

123. Third, Dr. Holberg does not provide a specific analysis of the “soft start” and “pulse skipping” modes in view of Galinski. Instead, Dr. Holberg’s paragraph no. 163 repeats the simple conclusion and references paragraphs 107 and 69. But 107 is related to the TI Datasheet’s specific circuitry, and paragraph 69 is related to the general concept that pulse skipping reduces voltage. (See EX1003, ¶¶ 163, 107, 69).

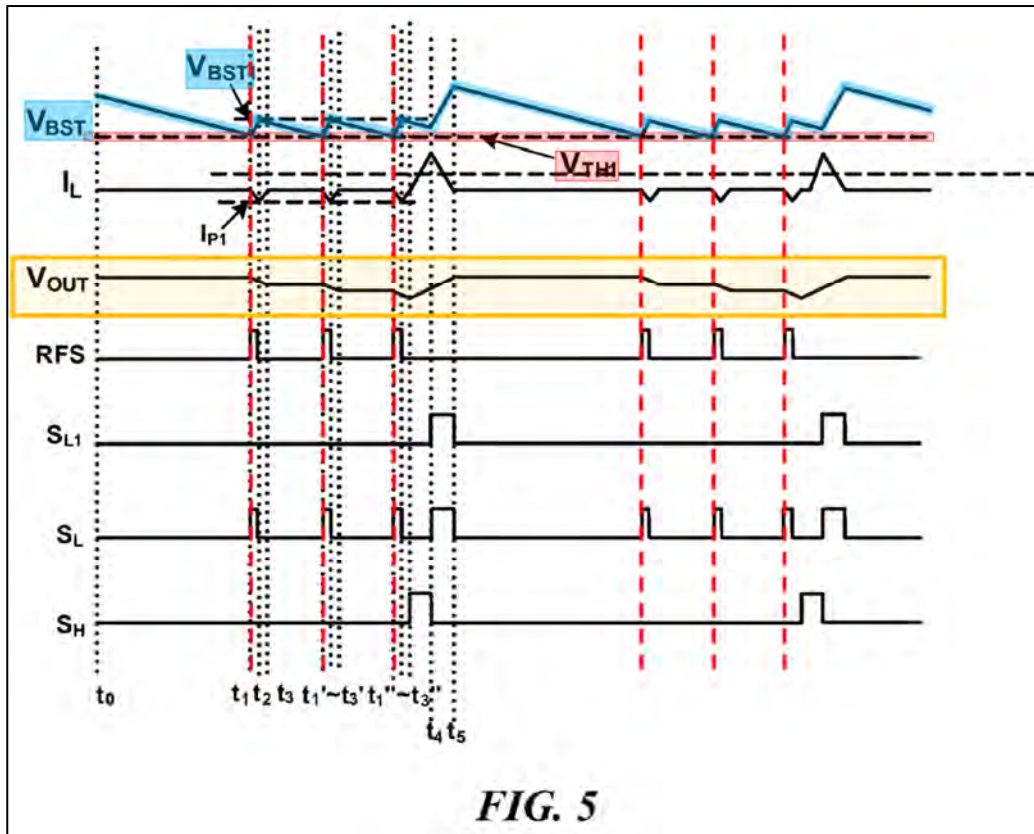
124. Fourth, as I describe above, it is my opinion that what the Petitioner points to in Galinski to be the “first comparing module” and “voltage difference module” are opposed to each other. The first comparing module effectively disables the voltage difference module during a reset pulse.

125. Accordingly, it is my opinion that Galinski does not expressly or inherently anticipate the ’608 Patent.

2. Galinski does not expressly or inherently describe 1[A]’s bootstrap refresh threshold.”

126. Petitioner identifies the claimed “bootstrap refresh threshold” of 1[A] as Galinski’s switching output voltage V_{SW} (which drives its V_{OUT}), but an output voltage is not a “bootstrap refresh threshold” in my opinion. Independent claims 11 and 12 contain similar limitations as 1[A] and Galinski does not anticipate or render obvious those claims for the same reasons. Claim 11 recites a bootstrap refresh threshold (EX1001, 23:28); and Claim 12 recites a bootstrap refresh threshold (EX1001, 24:7-8).

127. Figure 3 of the ’608 Patent is helpful to illustrate the claim limitation 1[A]. Figure 3 is annotated and reproduced below and illustrates how 1[A] requires a “bootstrap refresh control circuit” that has a “bootstrap refresh module” (*e.g.*, bootstrap refresh module 134 (yellow, below)) which comprises “a first comparing module” (*e.g.*, comparator 34, green) that compares a “bootstrap voltage signal” (*e.g.*, V_{BST} , blue) with a “bootstrap refresh threshold” (V_{TH1} , red). (EX1001, 19:10-20, 9:10-20, 10:60-63, 11:1-6, 12:15-29.) The ’608 Patent describes that the “bootstrap refresh threshold” is an indicator that the “bootstrap voltage signal” is too low. (EX1001, 3:19-32; 8:16-21). When the “bootstrap voltage signal” becomes lower than “bootstrap refresh threshold” value, the circuit operates to reduce the output voltage (V_{OUT} is orange, below). (Limitation 1[C], EX1001, 8:26-30).



129. Despite a bootstrap refresh threshold being different from the output voltage, Petitioner points to Galinski's switching node V_{SW} that drives the output voltage V_{OUT} as the alleged bootstrap refresh threshold. (Petition, 39). Galinski's switching output voltage V_{SW} drives the output voltage V_{OUT} . This can be seen in the annotated Figure 2 from Galinski reproduced below. The switching output voltage V_{SW} is from the voltage node at 120, and it generates a regulated output voltage V_{OUT} via an Inductor L_1 and capacitor C_{OUT} (shown in yellow below). (EX1005 at 5:30-36). V_{SW} is the pulsed output from the switch Q1 which either allows the input voltage V_{IN} to transfer to V_{SW} or not (shown in green below).

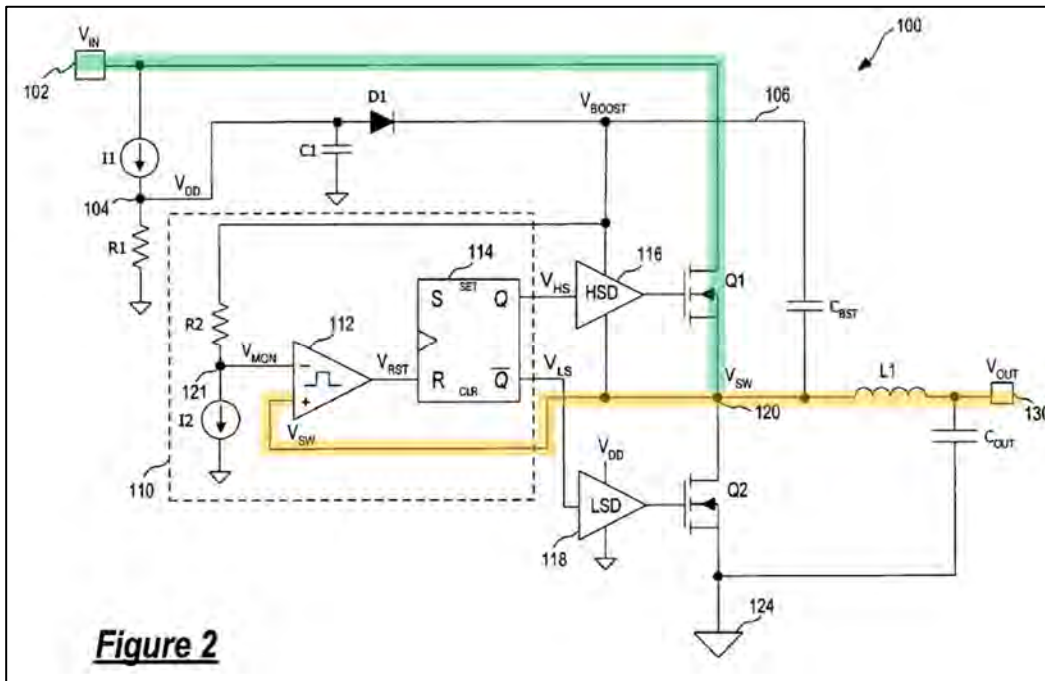


Figure 2

130. Accordingly, it is my opinion that V_{SW} cannot be the claimed “bootstrap refresh threshold” because the switching output voltage V_{SW} drives the output voltage V_{OUT} . Galinski does not anticipate or render obvious the limitations of the claims.

3. Grounds 2, 3 and 5 fail for the same reasons that I described above.

131. As I described above, it is my opinion that Galinski does not anticipate or render obvious the claims of the '608 Patent. The Petition presents its analysis about Galinski in Ground 2 (Petition, 35-42), and thus for the reasons I stated above, it is my opinion that Ground 2 does not demonstrate how Galinski anticipates the claims of the '608 Patent. In Ground 3, Petitioner relies on the exact same arguments as it did in Ground 2 for the independent claims, but instead of arguing an

anticipation theory, Petitioner argues that Galinski renders the claims obvious. (Petition, 47, 49). In Ground 3, Petitioner and Dr. Holberg do not offer any evidence supporting why Galinski renders the limitations obvious. (See Petition, 47, 49; EX1003, ¶¶ 57-62, 155, 156, 193, 194). I understand that Petitioner and Dr. Holberg need to offer evidence to support their obviousness assertions. Accordingly, for the reasons I described above, Ground 3 fails. Ground 5 only focuses on dependent claims 6 and 15. Because the independent claims are not rendered obvious over Galinski, then Ground 5 fails for the reasons discussed above. Thus, it is my opinion that Grounds 2, 3, and 5 fail.

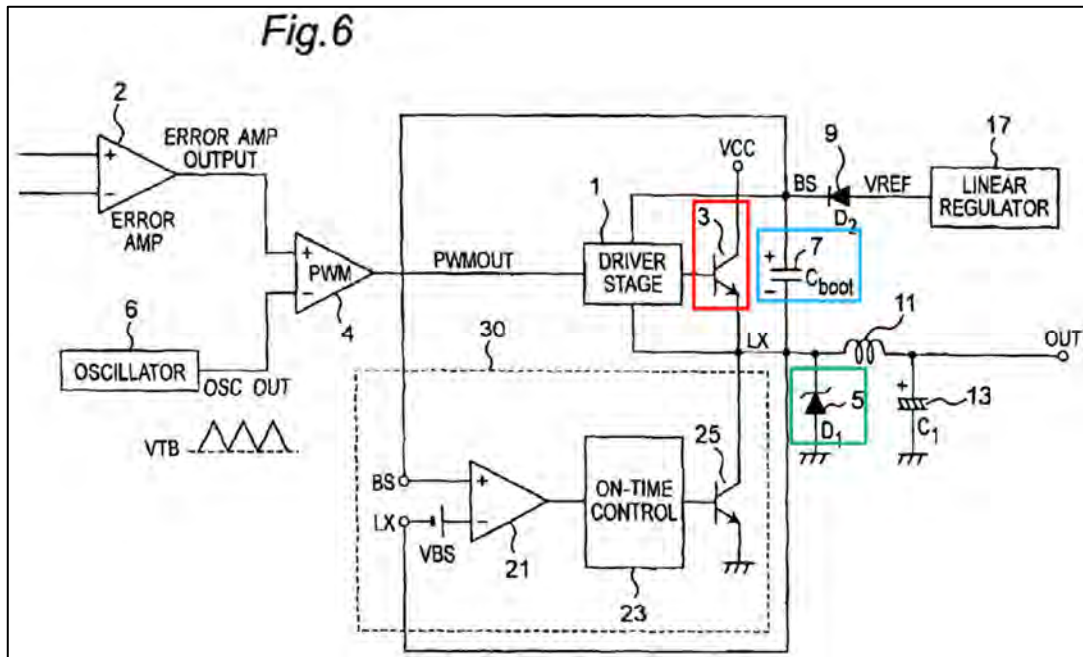
C. Wong does not render any claim obvious.

132. In my opinion, Wong does not render any claim obvious of the '608 Patent. Wong does not have a low side switch, and Petitioner attempted to replace a Zener diode in the circuit with a switch to meet the claimed “low side switch.” But this does not work for two reasons. First, the Petitioner never describes how that switch would be controlled. This is big oversight because a switch requires additional complex circuitry to control. Second, it is my opinion that a POSITA would not have replaced a Zener diode in Wong with a switch. A Zener diode has certain behaviors that a switch does not have. A Zener diode is specifically present in Wong to provide a stable output, and a switch would not provide this function. I address each issue in turn.

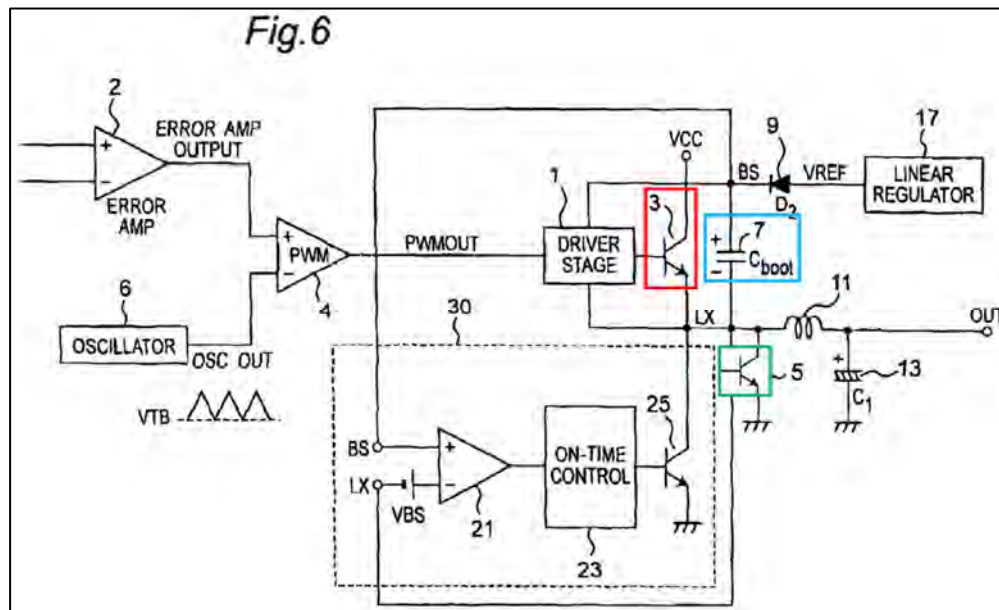
1. Petitioner's modification of Wong, to replace the Zener diode with a switch, does not meet the claim limitations of 1[PRE] and 1[D].

133. It is my opinion that Petitioner's modification of Wong, to replace the Zener diode with a switch does not meet the claim limitations of 1[PRE] and 1[D] because Petitioner never describes how the low side switch would be controlled. Limitation 1[PRE] requires "driving the high side switch and the low side switch to switch on and off." (EX1001, 19:6-7). Limitation 1[D] requires that "the bootstrap refresh control circuit is configured to control the high side switch and the low side switch to switch on and off based on the difference signal." (EX1001, 19:43-45). Claims 11 and 12 have similar limitations. (EX1001, 23:11-15, 23:56-60, 24:1-3, 24:23-25). Accordingly, the low side switch needs to be turned on and off. However, in my opinion, the Petitioner never explains how the low side switch, even if it replaced the Zener diode in Wong, would be controlled.

134. For example, when discussing 1[PRE], the Petitioner attempts to replace Wong's Zener diode 5 (D_1) with a switch to meet the claimed "low side switch," and states that a POSITA would understand that the diode could be replaced with a switch. (Petition, 50). Figure 6 of Wong, which was annotated by Petitioner, is reproduced below and illustrates that the red switch is the claimed high side switch and the green diode D_1 is what could be allegedly replaced with a switch to meet the claimed low side switch requirement. (See Petition, 51).



135. Such a replacement would make Wong's annotated Figure 6 circuit look like the following, where the diode 5 (D_1) is replaced with a switch (*e.g.*, a green switch is replacing the diode 5).



136. Petitioner never explains what the circuitry is to control this new low

side switch. (Petition, 49-51). This is important because switches (which are called transistors in electrical engineering) have three fundamental terminals. (EX2011, 3-4). They have a collector, base, and emitter. (EX2011, 3-4). A transistor allows current from the collector to the emitter or vice versa, and the base pin receives a signal that is used to “switch” the transistor on or off. (EX2011, 6). If the base is not connected to anything (*e.g.*, it is called “floating”), then the base does not have an input voltage so the transistor is basically turned off. (EX2012,² 2 (If there is no base connection, “the base wire of the transistor will be left ‘floating’ (not connected to anything) and there will be no current through it. In this state, the transistor is said to be *cutoff*.”)). This would be true for any type of switch or transistor. There are two types of transistors, BJTs and FETs, and while FETs have terminals that are called a gate, a source, and a drain, these are analogous to the BJT’s emitter, collector, and base. (*E.g.*, EX2013, 1). This is basic knowledge in electrical engineering and there are many website publications and academic papers discussing this, and I have offered just a few more-recent public websites that discuss this since they articulate these points clearly. These points would have been known far before 2014.

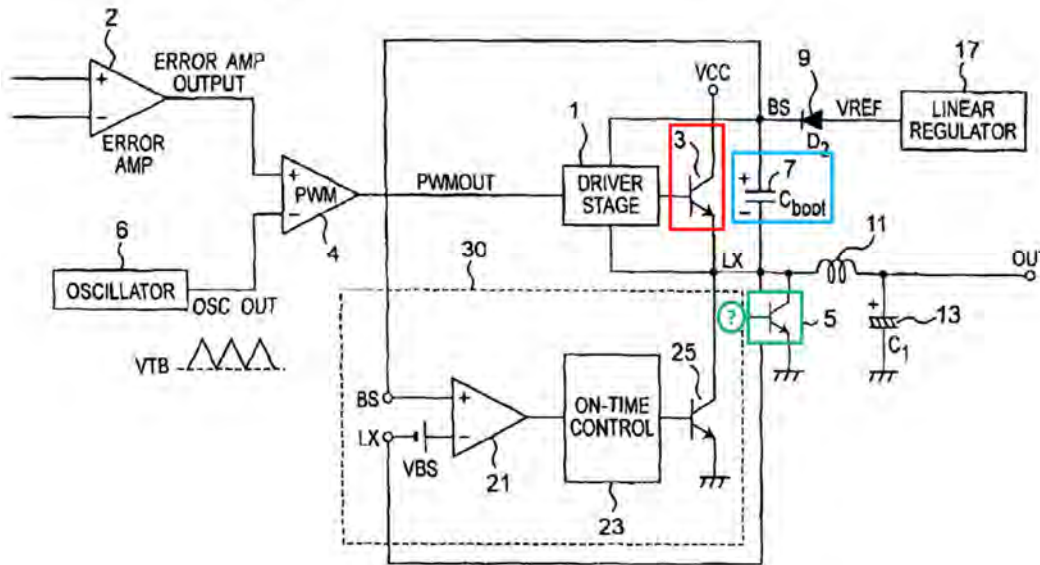
137. Accordingly, in my opinion, because Petitioner never offers any

² Exhibits EX2011 and EX2012 is from a reference that appears to be more recent than 2014 but offers an excellent discussion of these elementary points, which is why I include it here. This information would have been known for far longer than before 2014.

description in 1[PRE] about how the alleged low side switch would be controlled, Petitioner fails to show how it would be obvious to modify Wong to replace the Zener diode with a switch.

138. Petitioner also never heals this issue in 1[D] in my opinion. As I described above, 1[D] requires that “when the feedback signal is smaller than the reference voltage signal, the bootstrap refresh control circuit is configured to control the high side switch and the low side switch to switch on and off based on the difference signal.” Thus, the low side switch needs to be controlled on and off. However, Petitioner’s and Dr. Holberg’s analysis for 1[D] does not describe how this low side switch would be controlled. (Petition, 56-58). The Petitioner just refers to its analysis in 1[PRE] and alleges that Wong’s diode is analogous to a low-side switch. My review of Dr. Holberg’s analysis also indicates that he never describes how this would be controlled. (See EX1003, ¶¶ 199, 218). Figure 6 annotated with a floating diode is repeated below:

Fig.6

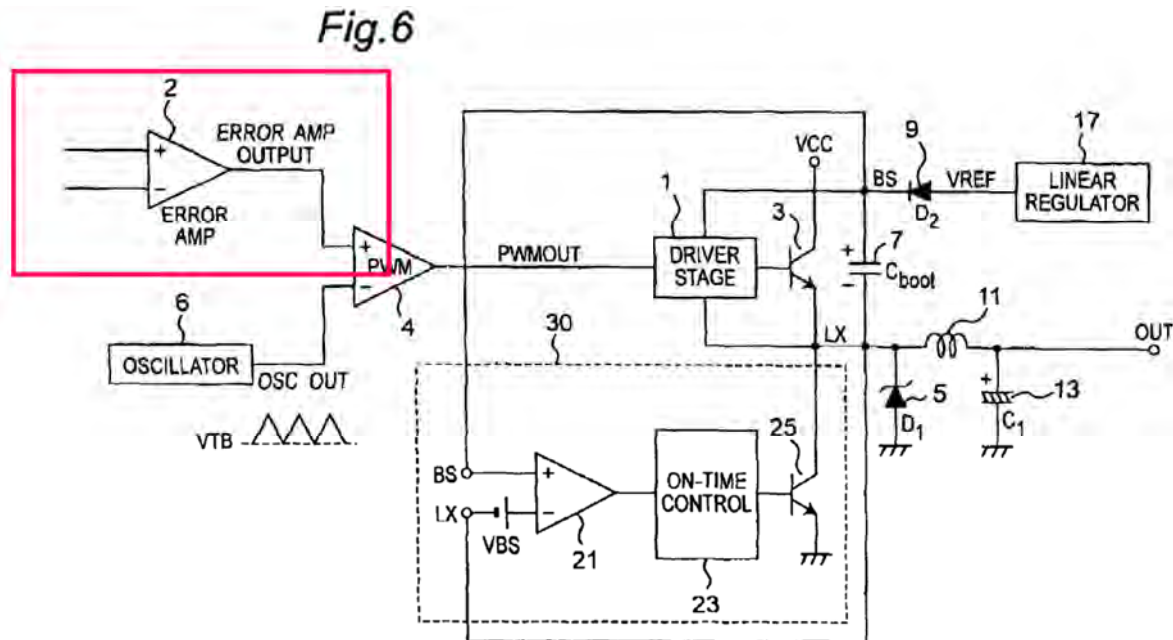


139. Instead of attempting to show how this low side switch would be controlled, the Petition analyzes switch 25. (Petition, 57-58). These two separate switches are annotated below (switch 25 in orange and the alleged low side switch in green). These two switches are different and Petitioner and Dr. Holberg do not explain why a POSITA would be motivated to somehow use the control logic of switch 25 for the new low side switch. In fact, these switches are different. Wong states that this secondary switch 25 “is not the same as the commonly referred “synchronous rectifier” which turn on every cycle where the bootstrap capacitor is charged through the switch under normal operation.” (EX1007, 2:66-3:2). Thus, Wong explains that the switch is different. Switch 25 and some replacement switch for the diode are different and cannot be conflated.

[illegible]

-70-

a “first comparing signal” and 1[D] does not act based on that “first comparing signal.” (See EX1001, 19:9-47).



141. Additionally, my review of Dr. Holberg’s declaration indicates that he did not conduct any additional analysis. He repeats much of Petitioner’s analysis. (See, e.g., EX1003, ¶¶ 65-69, 107, 199, 215-220).

142. Accordingly, in my opinion, Petitioner has not shown why Wong renders limitations 1[PRE] and 1[D] obvious.

2. Petitioner does not present a motivation or reason to replace Wong’s Zener diode with a switch.

143. In my opinion, the Petition fails to present a motivation to replace Wong’s Zener diode with a switch, and thus, Petition does not set forth why Wong renders the ’608 Patent obvious.

144. Fundamentally, Petitioner's proposed combination of replacing the Zener diode with a switch goes against what Wong discloses and a POSITA would not have done this proposed combination, in my opinion. Specifically, Wong's Zener diode 5 is a Zener diode and Zener diodes existed long before Wong. (*Compare* EX2014, 1 (showing the Zener diode schematic symbol *with* EX1007, Fig. 6). Zener diodes are used as voltage regulators in circuits because of their unique properties. (EX2014, 1, 2.) Zener diodes are unique because unlike normal diodes, which only allow current to flow in one direction (*e.g.*, the diodes are forward biased to do so), Zener diodes allow current to flow in both directions at certain thresholds. (EX2014 at 1). Thus, Zener diodes can function like a normal diode in forward bias but can also allow a certain current to pass through when reversed bias (*e.g.*, at a predetermined value, the Zener diode will conduct in this reverse direction). (EX2014 at 1.) Zener diodes take advantage of this reverse bias situation. (EX2014 at 1-2). When Zener diodes are placed in a reverse bias configuration (the anode is connected to a negative side and the cathode is connected to the positive side), the Zener diode has an almost constant voltage at after a certain threshold even though there could be large changes in current. (EX2014 at 1-2). Thus, the Zener diode intrinsically controls itself and is useful in voltage regulators because it provides a constant output voltage to a load despite ripples in the supply voltage or variations in the load current. (EX2014 at 1-2). Additionally, in Wong, it is clear that the Zener

diode 5 is in its reverse bias configuration, where the anode is connected to ground and the cathode is connected to the LX node. (EX2014 at 1-2) describes this configuration. Accordingly, in Wong, the Zener diode helps provide a stabilized voltage for the output voltage and it does this for any varying load.

145. Switches (such as BJT and FET transistors) are unlike a Zener diode in that the switches do not produce a stable output voltage without additional circuitry. As I described above, their outputs are dependent on their control and input signals. Also, transistors can fluctuate based on temperature. (*E.g.*, EX2015, 1-5 (“With this single resistor type of biasing method the biasing voltages and currents do not remain stable during transistor operation and can vary enormously as temperature also adversely effects the operating point.”)). Also, as I reference above, a Zener diode is a passive device that reacts intrinsically, whereas a switch needs external control circuitry to operate.

146. Accordingly, it is my opinion that the Zener diode of Wong is deliberate to ensure a stable voltage irrespective of the value of any load; and this output stability is not achieved when the diode is substituted by a switch. Additionally, as I described above, a switch needs a signal to control it, and a POSITA would not make this substitution because added control circuitry would be needed and there would be extensive evaluation needed to make the switch perform in Wong. Wong does not address this in its disclosure.

147. Petitioner's analysis assumes that this Zener diode is just a normal diode that can be replaced with a switch and only allow current in one direction. (Petition, 50-51). As I described above, this does not make sense because a Zener diode allows current in both directions and is used to maintain a stable output voltage as it is configured in Wong. A transistor (such as BJT) would not provide the same stable output voltage as I describe above. In fact, if a switch were turned on, it would act like an effective, minimally resistive short to ground (since a transistor turned on effectively acts like a wire) and if it were turned off it would act like an open circuit. (See EX2011, 7-8). Thus, a transistor (*e.g.*, a BJT or FET or another switch) cannot replace a Zener diode because they have inherently different characteristics and operate for different purposes.

148. Additionally, as I described above, Petitioner and Dr. Holberg do not describe how the switch would be controlled if the switch were used to replace the Zener diode. However, a POSITA would understand that a switch (BJT) can function similar to a standard diode by wiring a BJT's base to its collector. (*E.g.*, EX2016, 1-3 (an engineering forum discussing this)). But even if a POSITA followed this configuration, it would not make sense in the circuit. This is because whenever the BJT receives a voltage on its collector, it will also receive one on its base, meaning that for any voltage, there will be a voltage drop across the transistor. (See EX2011, 13 (showing that if the control is the same voltage as the input, the switch is on)).

This would effectively short out the circuit every time there is a voltage flowing to the output of the circuit in Wong. Accordingly, this would result in a lower voltage to the load whenever voltage is applied to the circuit. This would defeat the purpose of the Zener diode because the purpose of the Zener diode is to provide a stabilized output voltage that is high. Accordingly, in my opinion, a POSITA would not have made the alleged circuit substitution.

149. Additionally, the Petition does not address this and just states in conclusory fashion that a switch can replace a diode. (Petition, 50-51).

150. Dr. Holberg repeats these conclusory assumptions citing EX1028, 332, 333 (“Wait”) and EX1026, 1:26 (“Schoneman”) for the assumption that a diode can function as a switch (EX1003, ¶¶ 65, 67). Wait and Schoneman do not support this assumption. Wait describes circuit architectures that use four or more diodes in certain configurations to *act* like a switch (these are often called “equivalents” in electrical engineering), but Wait never stands for the assertion that a single diode—and especially a Zener diode—is interchangeable with a switch, and it certainly does not say a Zener diode is interchangeable with a switch in the context of a voltage converter. (EX10028, 332, 333).

151. Further, Dr. Holberg’s cite to Schoneman (EX1003, ¶¶ 65, 67), a patent from 1992, simply alleges that a diode in *that patent’s* converter *acts* as “a passive switch,” but Petitioner and Dr. Holberg do not explain how this can mean that the

Zener diode can be replaced with an active switch such as a transistor. A POSITA would not be motivated, in my opinion, to replace the Zener diode with a switch (as I described above.) Also, Petitioner and Dr. Holberg do not explain how the switch would be controlled (ss I described above). A BJT is different from a Zener diode because a BJT switch needs a control signal (*e.g.*, a base signal) whereas a Zener diode does not need a control signal and is a device that intrinsically controls itself.

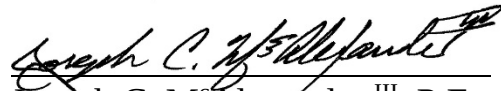
152. Additionally, Dr. Holberg also cites to Schoneman, 1:49-59 and EX10025, ¶ 0021 (“Dubhashi”) for the wrong assumption that a switch would result in higher efficiency than a diode. EX1003, ¶ 68. Schoneman states nothing about efficiency. Dubhashi states that a switch is advantageous in systems that need bidirectional current and reversed power flow for efficiency. (EX1025, ¶ 21). Switches are not always “more efficient.” As I described above, they could actually be less efficient because they can cause wide changes in voltage output. Whether a switch results in higher efficiency depends on the architecture of the converter. Petitioner and Dr. Holberg do not explain why a POSITA would find that a switch results in higher efficiencies *for Wong*. (EX1003 at ¶ 68).

153. Accordingly, it is my opinion that Wong does not render obvious the limitations of the ’608 Patent.

V. CONCLUSION

I hereby declare that all the statements made in this declaration are based on my own true knowledge, that all statements made on information and belief are believed to be true, and that all statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001. I declare under the penalty of perjury under the laws of the United States that all statements made in this declaration are true and correct.

Dated this 3rd day of September, 2024


Joseph C. McAlexander III, P.E.