

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

REED SEMICONDUCTOR CORP.,
Petitioner,

v.

MONOLITHIC POWER SYSTEMS, INC.,
Patent Owner.

IPR2024-00871
Patent 9,590,608 B2

Before KARL D. EASTHOM, KEN B. BARRETT, and
LARRY J. HUME, *Administrative Patent Judges*.

BARRETT, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. *Background and Summary*

Reed Semiconductor Corp. (“Petitioner”)¹ filed a Petition requesting *inter partes* review of U.S. Patent No. 9,590,608 B2 (“the ’608 patent,” Ex. 1001). Paper 1 (“Pet.”). The Petition challenges the patentability of claims 1, 2, 6, 11, 12, 15, and 16 of the ’608 patent. Monolithic Power Systems, Inc. (“Patent Owner”)² filed a Preliminary Response to the Petition. Paper 5 (“Prelim. Resp.”).

An *inter partes* review may not be instituted “unless . . . the information presented in the petition . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a) (2018). Having considered the arguments and evidence presented by Petitioner and Patent Owner, we determine that Petitioner has not demonstrated a reasonable likelihood of prevailing on at least one of the challenged claims of the ’608 patent. Accordingly, we do not institute an *inter partes* review of the challenged claims.

B. *Related Proceedings*

Both parties identify, as matters involving or related to the ’608 patent, *Monolithic Power Systems, Inc. v. Reed Semiconductor Corp.*, No. 1:23-cv-01155-JFM (D. Del.), and *Monolithic Power Systems, Inc. v.*

¹ Petitioner identifies Reed Semiconductor Corp., Nengda Microelectronics (Shenzen) Co., LTD., and Nengda Semiconductor Technology (Shenzen) Co., LTD. as real parties in interest. Pet. 80.

² Patent Owner identifies Monolithic Power Systems, Inc. as the real party in interest. Paper 4, 2.

Nengda Microelectronics (Shenzhen) Co. Ltd. et al., No. 1:24-cv-00166-JFM (D. Del.). Pet. 80–81; Paper 4, 2.

C. The '608 Patent

The '608 patent “relates generally to electronic circuits, and more particularly but not exclusively relates to voltage converters and [a] bootstrap refresh control circuit.” Ex. 1001, 1:14–17. According to the '608 patent, “[i]n the presently existing switch-mode voltage regulators, a high voltage signal may be needed to drive the switches,” and “a bootstrap circuit will be applied to provide the high voltage signal.” *Id.* at 1:22–26.

Figure 3 of the '608 patent is reproduced below.

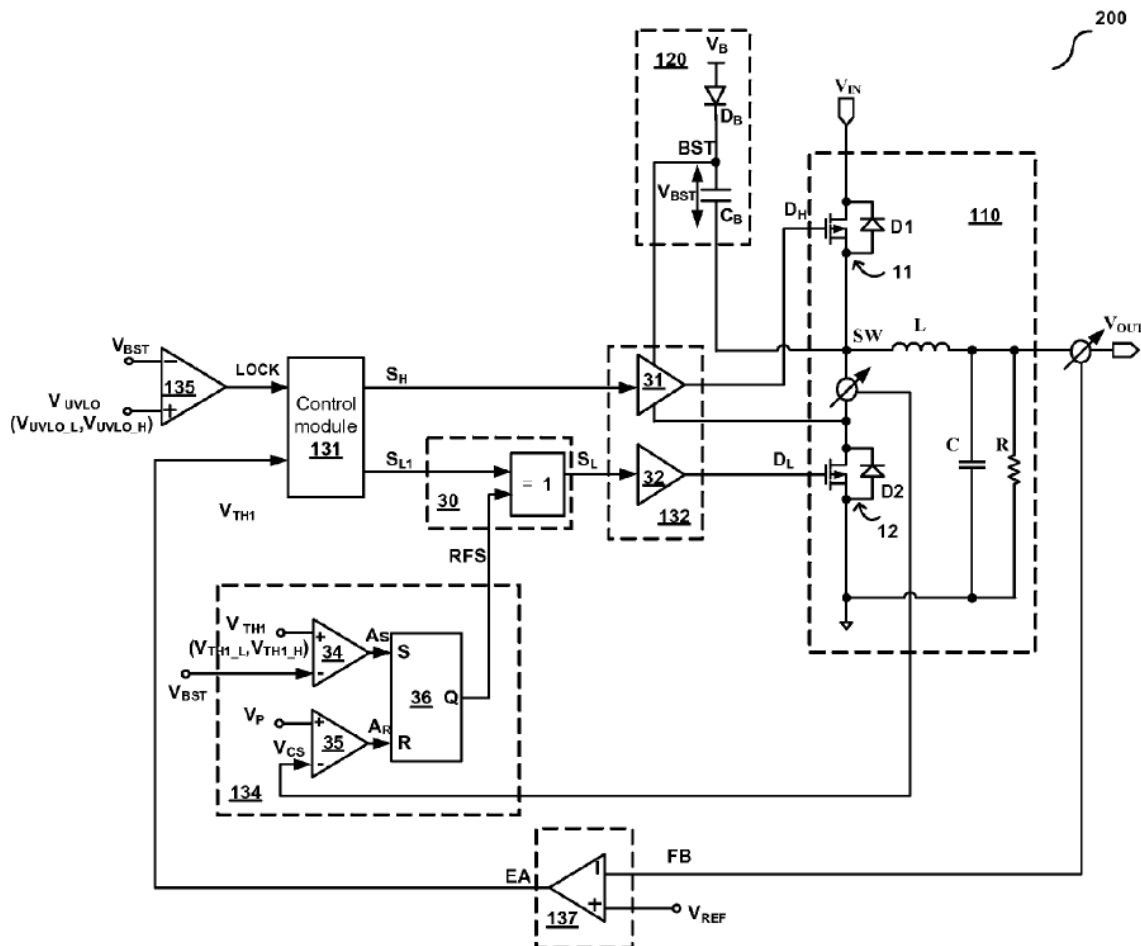


FIG. 3

Figure 3 “illustrates a schematic diagram of a voltage converter 200 in accordance with an exemplary embodiment of the [’608 patent].” *Id.* at 10:35–37. “Voltage converter 200 . . . comprises a switching circuit 110, a bootstrap circuit 120 and a bootstrap refresh control circuit.” *Id.* at 10:35–39. Switching circuit 110 includes a high side switch 11, a low side switch 12, an inductor (L), a capacitor (C) and a load (R). *See id.* at 1:30–32, 10:56–57, Fig. 3. Voltage difference module 137 receives feedback signal (FB) representing the voltage converter’s output voltage signal (V_{OUT}). *See id.* at 7:13–20. The voltage difference module also “receive[s] a reference voltage signal (V_{REF}) representing a desired value of the output voltage signal (V_{OUT}),” and “is configured to compare the feedback signal (FB) with the reference voltage signal (V_{REF}) so as to provide a difference signal (EA).” *Id.* at 7:20–26. The difference signal is used to control the high side switch and the low side switch in a complimentary manner to obtain the desired output terminal voltage. *See id.* at 1:49–55, 7:27–50.

“The high side switch 11 and the low side switch 12 may comprise a power switching device, such as a Metal Oxide Semiconductor Field Effect Transistor (MOSFET), a Junction Field Effect Transistor (JFET)[,] etc.” *Id.* at 1:33–37. “[I]n order to make the high side switch 11 to be fully turned on (i.e. to make the high side switch 11 to operate in saturation region in which the switch 11 has a quite small on resistance), . . . a voltage higher than the input voltage (V_{IN}) must be provided to the gate of the high side switch 11.” *Id.* at 1:65–2:12. Such a voltage is supplied by the bootstrap circuit 120, which has bootstrap capacitor (CB). *See id.* at 2:12–14, Fig. 3.

“When the high side switch 11 is turned off and the low side switch 12 is turned on, the voltage of the common connection node (SW) is equal to the ground potential and the bootstrap capacitor (CB) is charged by the bootstrap supply voltage (VB) till the voltage across the bootstrap capacitor (CB) reaches the bootstrap voltage (VBST).” *Id.* at 2:35–40. In certain circumstances, the bootstrap capacitor is unable to be fully charged, which can result in failure to drive high side switch 11 properly, which causes the voltage converter to operate improperly. *See id.* at 3:3–30. For example, “when the output voltage signal (VOUT) is approximately close to the input voltage signal (VIN), the high side switch 11 has to operate with a quite high duty cycle, even in a 100% duty cycle,” and “[t]herefore, the low side switch 12 may have a very short conduction time or hardly have chance to turn on resulting in the bootstrap capacitor (CB) unable to be charged to a desired value.” *Id.* at 3:3–9. Another example is during a light load or no load condition when the control circuit “reduce[s] the conduction time and/or the switching frequency of the high side switch 11 and the low side switch 12 to improve the conversion efficiency which may lead to the bootstrap capacitor (CB) not being able to be charged/recharged in time since the on time of the low side switch 12 is too short or there is no switching in a relatively long time.” *Id.* at 3:10–18.

As mentioned, the voltage converter includes a bootstrap refresh control circuit. “[T]he bootstrap refresh control circuit of the voltage converter 200 may comprise a control module 131, a drive module 132, a voltage difference module 137, a bootstrap refresh module 134 and an under voltage lock out module 135.” *Id.* at 10:56–60.

The bootstrap refresh module 134 is configured to compare the bootstrap voltage signal (V_{BST}) with a bootstrap refresh

threshold (V_{TH1}) for providing an bootstrap refresh signal (RFS). In one embodiment, when the voltage converter 200 operates in light load or no load condition, both the high side switch 11 and the low side switch 12 are turned off so that no current flows through the inductor (L) and the bootstrap voltage signal (V_{BST}) drops. If the bootstrap voltage signal (V_{BST}) drops lower than the bootstrap refresh threshold (V_{TH1}), the bootstrap refresh module 133 start to operate to reduce the output voltage (V_{OUT}) of the voltage converter 200. Meanwhile, the feedback signal (FB) drops with the decreasing of the output voltage (V_{OUT}). The comparing module 137 may compare the feedback signal (FB) with the reference voltage signal (V_{REF}). When the feedback signal (FB) is smaller than the reference voltage signal (V_{REF}), the control module 131 may control the high side switch 11 and the low side switch 12 to switch normally based on the difference signal (EA) so as to maintain the output voltage signal (V_{OUT}) at a desired value, i.e. the high side switch 11 and the low side switch 12 are recovered from the off states into a complementary conduction states. The conduction time of the low side switch 12 can be increased accompanying the increasing of the switching frequency of the high side switch 11 and the low side switch 12. Thus, the bootstrap capacitor (C_B) can be charged in time so as to refresh the bootstrap voltage signal (V_{BST}) to the default value.

Id. at 11:3–31.

D. Illustrative Claim

Of the challenged claims of the '608 patent, claims 1, 11, and 12 are independent. Claim 1, reproduced below with bracketed annotations³ inserted, is illustrative.

1. [1Pre] A bootstrap refresh control circuit for a voltage converter, wherein the voltage converter comprises a high side switch, a low side switch and a bootstrap capacitor for providing a bootstrap voltage signal to supply a high side

³ We utilize annotations for claim 1 similar to Petitioner's but have retained the paragraph formatting from the issued patent.

driver of the high side switch, and wherein the voltage converter is configured to receive an input voltage at an input terminal and to provide an output voltage at an output terminal based on driving the high side switch and the low side switch to switch on and off, and wherein the bootstrap refresh control circuit comprising:

- [1A] a bootstrap refresh module, wherein the bootstrap refresh module comprises a first comparing module having a first input terminal, a second input terminal and an output terminal, and wherein the first input terminal of the first comparing module is configured to receive the bootstrap voltage signal, the second input terminal of the first comparing module is configured to receive a bootstrap refresh threshold, and the first comparing module is configured to compare the bootstrap voltage signal with the bootstrap refresh threshold to provide a first comparing signal having a first logic state and a second logic state at the output terminal, and wherein the first comparing signal has the first logic state when the bootstrap voltage signal is lower than the bootstrap refresh threshold, and wherein the first comparing signal has the second logic state when the bootstrap voltage signal is larger than the bootstrap refresh threshold; and
- [1B] a voltage difference module having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal of the voltage difference module is configured to receive a feedback signal representing the output voltage of the voltage converter, the second input terminal of the voltage difference module is configured to receive a reference voltage signal representing a desired value of the output voltage of the voltage converter, the voltage difference module is configured to compare the feedback signal with the reference voltage signal so as to provide a difference signal at the output terminal; and wherein
- [1C] when the first comparing signal has the first logic state, the bootstrap refresh module is configured to

decrease the output voltage of the voltage converter;
and [1D] wherein when the feedback signal is smaller
than the reference voltage signal, the bootstrap
refresh control circuit is configured to control the
high side switch and the low side switch to switch on
and off based on the difference signal so as to charge
the bootstrap capacitor for refreshing the bootstrap
voltage signal.

Ex. 1001, 18:66–19:48.

E. Evidence

Petitioner relies on the following references:

Name	Reference	Exhibit No.
Galinski	US 7,145,316 B1, issued Dec. 5, 2006	1005
TI	Texas Instruments, TPS54620, <i>4.5V to 17V Input, 6A Synchronous Step Down SWIFT™ Converter</i> , May 2011	1006
Wong	US 7,321,258 B2, issued Jan. 22, 2008	1007
Li	Chinese Patent Application Publication No. CN 102832810 A, published Dec. 19, 2012	1008, 1011 ⁴

Petitioner also relies on the declaration of Dr. Douglas Holberg (Ex. 1003) in support of its arguments, and Patent Owner relies on the declaration of Joseph C. McAlexander III, P.E. (Ex. 2001) in support of its arguments. The parties also rely on other exhibits as discussed below.

⁴ Petitioner represents that Exhibit 1008 is the original Chinese language publication of the Li reference, and Exhibit 1011 is the certified English translation thereof. Pet. 3 n.4 (citing Ex. 1012).

F. Asserted Grounds of Unpatentability

Petitioner asserts that the challenged claims are unpatentable on the following grounds:

Claim(s) Challenged	35 U.S.C. §⁵	Reference(s)/Basis
1, 11, 12	102/103	TI
1, 11, 12	102	Galinski
1, 2, 11, 12, 16	103	Galinski, Li
1, 6, 11, 12, 15	103	Wong
6, 15	103	Galinski, Wong

II. ANALYSIS

A. Principles of Law

Petitioner bears the burden of persuasion to prove unpatentability of the claims challenged in the Petition, and that burden never shifts to Patent Owner. *Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015).

“A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.” *Verdegaal Bros., Inc. v. Union Oil Co. of Cal.*, 814 F.2d 628, 631 (Fed. Cir. 1987); *see also Finisar Corp. v. DirecTV Group, Inc.*, 523 F.3d 1323, 1334 (Fed. Cir. 2008) (to anticipate a patent claim under 35 U.S.C. § 102, “a single prior art reference must expressly or inherently

⁵ The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), includes revisions to 35 U.S.C. §§ 102 and 103 that became effective on March 16, 2013. Because the earliest filed application identified in the ’608 patent has a filing date of August 11, 2014 (Ex. 1001, code (30), 1:8–10), we apply the AIA-versions of 35 U.S.C. §§ 102 and 103.

disclose each claim limitation”). Moreover, “[b]ecause the hallmark of anticipation is prior invention, the prior art reference—in order to anticipate under 35 U.S.C. § 102—must not only disclose all elements of the claim within the four corners of the document, but must also disclose those elements ‘arranged as in the claim.’” *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1369 (Fed. Cir. 2008) (quoting *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 1548 (Fed. Cir. 1983)). Whether a reference anticipates is assessed from the perspective of one of ordinary skill in the art. *See Dayco Prods., Inc. v. Total Containment, Inc.*, 329 F.3d 1358, 1368–69 (Fed. Cir. 2003) (“‘[T]he dispositive question regarding anticipation [i]s whether *one skilled in the art* would reasonably understand or infer from the [prior art reference’s] teaching’ that every claim element was disclosed in that single reference.” (second and third alterations in original) (quoting *In re Baxter Travenol Labs.*, 952 F.2d 388, 390 (Fed. Cir. 1991))).

Additionally, “[u]nder the principles of inherency, if the prior art necessarily functions in accordance with, or includes, the claimed limitations, it anticipates.” *MEHL/Biophile Int’l Corp. v. Milgraum*, 192 F.3d 1362, 1365 (Fed. Cir. 1999); *see In re Cruciferous Sprout Litig.*, 301 F.3d 1343, 1349–50 (Fed. Cir. 2002).

A patent claim is unpatentable under 35 U.S.C. § 103 “if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains.” 35 U.S.C. § 103; *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the

scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) if present, any objective evidence of obviousness or non-obviousness.

Graham v. John Deere Co., 383 U.S. 1, 17–18 (1966).

B. The Level of Ordinary Skill in the Art

In determining the level of ordinary skill in the art, various factors may be considered, including the “type of problems encountered in the art; prior art solutions to those problems; rapidity with which innovations are made; sophistication of the technology; and educational level of active workers in the field.” *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995) (quoting *Custom Accessories, Inc. v. Jeffrey–Allan Indus., Inc.*, 807 F.2d 955, 962 (Fed. Cir. 1986)).

Petitioner contends:

A person of ordinary skill in the art (“POSITA”) in the field of the ’608 Patent, as of its earliest possible filing date of August 11, 2014, would have been someone knowledgeable about and familiar with the DC-DC switch-mode power converter technology that is pertinent to the ’608 Patent. A POSITA would have had a bachelor’s degree in Electrical Engineering or equivalent training, and approximately two years of experience working in the field of power converters, feedback systems, or related technologies. Lack of work experience can be remedied by additional education, and vice versa.

Pet. 6 (citing Ex. 1003 ¶¶ 17–19).

Patent Owner contends:

A person of ordinary skill in the art . . . would have had a bachelor’s degree in Electric Engineering or equivalent, and approximately two years of experience working in the field of power converters, circuit design, device physics, or related

technologies. Lack of work experience can be remedied by additional education, and vice versa.

Prelim. Resp. 8 (citing Ex. 2001 ¶ 32).

We discern no material difference between the parties' definitions. Petitioner's definition is consistent with the level of ordinary skill reflected in the prior art references of record. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (recognizing that the prior art itself may reflect an appropriate level of skill in the art). For purposes of this decision, we apply Petitioner's definition of the person of ordinary skill in the art. We note, however, that were we to adopt Patent Owner's assessment, the outcome of this Decision would be the same.

C. Claim Construction

We apply the same claim construction standard used in district court actions under 35 U.S.C. § 282(b), namely that articulated in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). *See* 37 C.F.R. § 42.100(b). In applying that standard, claim terms generally are given their ordinary and customary meaning as would have been understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure. *Phillips*, 415 F.3d at 1312–13. “In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence.” *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17). “[W]hile extrinsic evidence can shed useful light on the relevant art, . . . it is less significant than the intrinsic record in determining the legally operative meaning of claim language.” *Phillips*, 415 F.3d at 1317 (internal quotation marks omitted).

Petitioner states that, “for the purposes of this proceeding and the grounds presented herein, no claim term requires express construction,” and that “Petitioner further notes that some claim terms are provided with explicit definitions in the specification.” Pet. 6–7 (citing Ex. 1001, 5:64–6:20). Patent Owner states, “[a]t this preliminary stage, and because the deficiencies of the Petition can be addressed absent construction, Patent Owner presents no constructions at this time.” Prelim. Resp. 9. Patent Owner also states that it identified terms for construction in the parallel district court proceeding. *Id.* (citing Ex. 1009).

On this record and for purposes of this decision, we determine that no claim terms require express construction.

D. The Alleged Unpatentability of Claims 1, 11, and 12 as Anticipated by TI, or, Alternatively, Obvious Over TI (Ground 1)

Petitioner alleges that independent claims 1, 11, and 12 of the ’608 patent are anticipated by or obvious over TI. *See* Pet. 25–31 (addressing claim 1). Patent Owner argues that TI lacks certain aspects of limitations 1A, 1C, and 1D. *See* Prelim. Resp. 9–34.

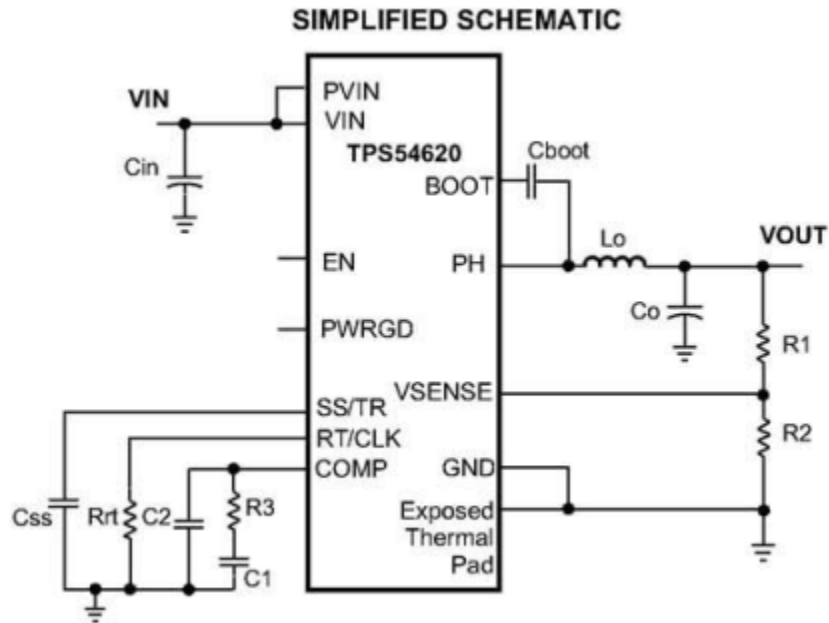
*1. TI (Ex. 1006)*⁶

TI is a Texas Instruments data sheet for TPS54620, “4.5V to 17V Input, 6A Synchronous Step Down SWIFT™ Converter.” Ex. 1006, 1. “The TPS54620 in thermally enhanced 3.5mm x 3.5mm QFN package is a full featured 17V, 6A synchronous step down converter which is optimized for small designs through high efficiency and integrating the high-side and

⁶ We, like Petitioner, cite to the page numbers of the underlying document rather than the exhibit page numbers.

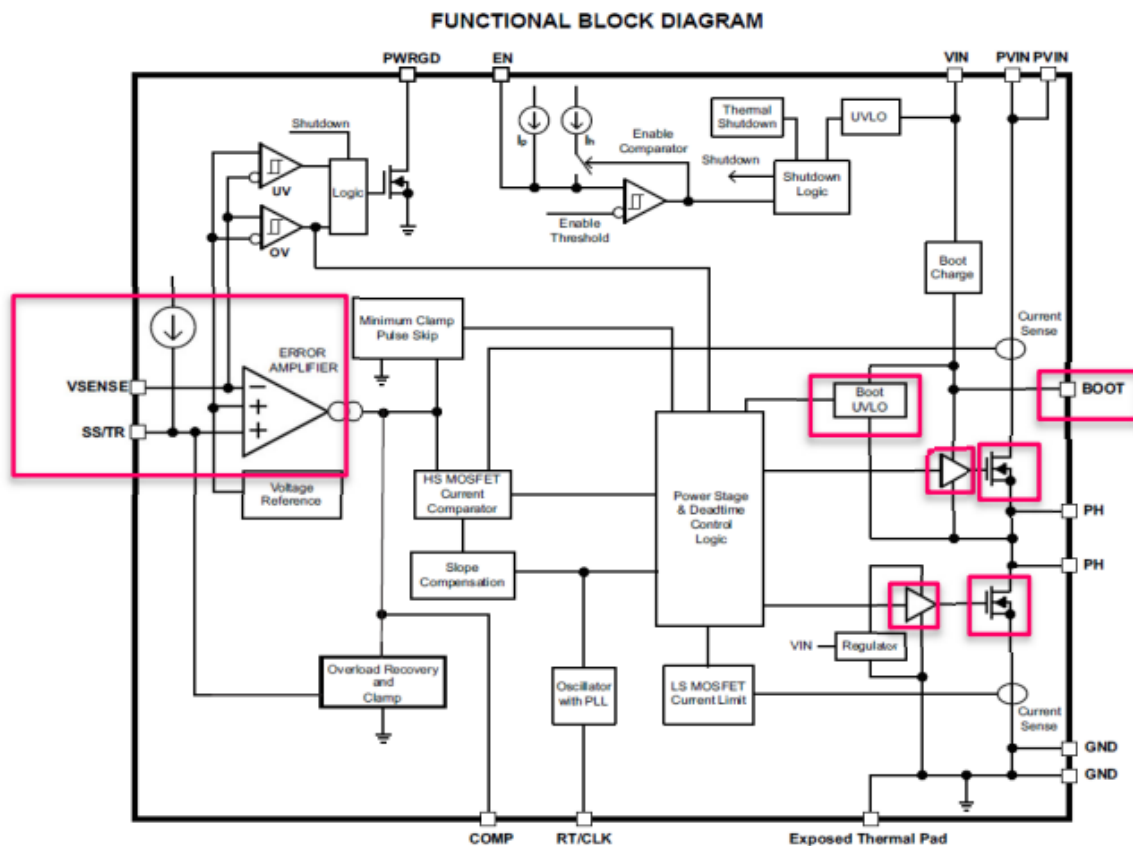
low-side MOSFETs.” *Id.* Applications include high performance point of load regulation. *Id.*

TI includes a Simplified Schematic, which is reproduced below.



Id. The Simplified Schematic depicts TPS54620 along with components attached to the pins thereof, including boot capacitor (Cboot). *See id.*; *see also id.* at 5 (pin assignments). “A bootstrap cap is required between BOOT and [switch node] PH,” and “[t]he voltage on this cap carries the gate drive voltage for the high-side MOSFET.” *Id.* at 5. The GND pins function as the “[r]eturn for control circuitry and low-side power MOSFET.” *Id.*

TI also includes a Functional Block Diagram. *Id.* at 6. We reproduce below Petitioner’s annotated version of that Diagram.



Pet. 14 (citing Ex. 1006, 6). The Functional Block Diagram above depicts the TPS54620 device itself with Petitioner’s annotations in the form of red boxes around, *inter alia*, the error amplifier, the BOOT pin, Boot UVLO (under voltage lockout), and the high-side and low-side MOSFETs along with their respective drivers. *Id.*; *see also* Ex. 1006, 9 (spelling out the UVLO acronym). Also shown in the middle of the diagram is the Power Stage and Deadtime Control Logic.

TI, in the “Overview” portion of the “Typical Characteristics” section, states:

The device reduces the external component count by integrating the boot recharge circuit. The bias voltage for the integrated

high-side MOSFET is supplied by a capacitor between the BOOT and PH pins. The boot capacitor voltage is monitored by a BOOT to PH UVLO (BOOT-PH UVLO) circuit allowing PH pin to be pulled low to recharge the boot capacitor. The device can operate at 100% duty cycle as long as the boot capacitor voltage is higher than the preset BOOT-PH UVLO threshold which is typically 2.1V. The output voltage can be stepped down to as low as the 0.8V voltage reference (Vref).

Ex. 1006, 10.

TI further states, in the “Detailed Description” section, that “[t]he output voltage is set with a resistor divider from the output (VOUT) to the VSENSE pin.” *Id.* at 11 (under the “Adjusting the Output Voltage” heading). “The error amplifier compares the VSENSE pin voltage to the lower of the SS/TR [(slow start and tracking)] pin voltage or the internal 0.8V voltage reference.” *Id.* at 11; *see id.* at 5 (pin functions). TI further explains:

Fixed Frequency PWM Control

The device uses a adjustable fixed frequency, peak current mode control. The output voltage is compared through external resistors on the VSENSE pin to an internal voltage reference by an error amplifier which drives the COMP pin. An internal oscillator initiates the turn on of the high-side power switch. The error amplifier output is converted into a current reference which compares to the high-side power switch current. When the power switch current reaches current reference generated by the COMP voltage level the high-side power switch is turned off and the low-side power switch is turned on.

Id. at 10.

TI also states in the “Detailed Description” section:

Bootstrap Voltage (BOOT) and Low Dropout Operation

The device has an integrated boot regulator, and requires a small ceramic capacitor between the BOOT and PH pins to provide the gate drive voltage for the high-side MOSFET. The

boot capacitor is charged when the BOOT pin voltage is less than VIN and BOOT-PH voltage is below regulation. . . . To improve drop out, the device is designed to operate at 100% duty cycle as long as the BOOT to PH pin voltage is greater than the BOOT-PH UVLO threshold which is typically 2.1V. When the voltage between BOOT and PH drops below the BOOT-PH UVLO threshold the high-side MOSFET is turned off and the low-side MOSFET is turned on allowing the boot capacitor to be recharged. . . .

Id. at 14.

2. The Alleged Unpatentability of Claim 1 As Anticipated by or Obvious Over TI

Patent Owner persuasively argues that Petitioner has failed to satisfy its threshold burden regarding limitation 1D, which pertains to the architecture of the bootstrap refresh control circuit. *See, e.g.*, Prelim. Resp. 11–20.

In the claim, limitation 1D is immediately preceded by the recitation of the requirement that, when the bootstrap voltage is lower than the refresh threshold, “the bootstrap refresh module is configured to decrease the output voltage of the voltage converter.” Ex. 1001, 19:39–41 (limitation 1C); *see also id.* at 19:21–23 (limitation 1A reciting that “the first comparing signal has the first logic state when the bootstrap voltage signal is lower than the bootstrap refresh threshold). Limitation 1D recites:

wherein when the feedback signal [representing the converter output voltage] is smaller than the reference voltage signal, the bootstrap refresh control circuit is configured to control the high side switch and the low side switch to switch on and off based on the difference signal so as to charge the bootstrap capacitor for refreshing the bootstrap voltage signal.

Id. at 19:42–48. Thus, limitation 1D requires an architecture involving a feedback signal indicating that the voltage converter’s output is low and, at

that time, the bootstrap refresh control circuit controls both switches by switching them on and off in a manner to charge *and refresh* the bootstrap voltage. This controlling is performed “based on the difference signal,” which, according to limitation 1B, is the difference between the feedback signal indicating the converter’s output and the reference voltage signal representing a desired value of the converter output voltage. *See id.* at 19:27–39. Petitioner does not adequately explain how all of these aspects are disclosed together by TI such that the reference anticipates claim 1.⁷

As an initial matter, limitation 1D—which is intimately related to the triggering condition of 1C, namely, a below-threshold bootstrap capacitor voltage signal—is directed to more than merely *charging* a bootstrap capacitor at the same time that the output voltage is low, but rather recites a bootstrap refresh control circuit that is configured to control the switches so as to charge the bootstrap capacitor *for refreshing the bootstrap voltage signal*, i.e., from a below-threshold level back to a level above the bootstrap refresh threshold. Much of the discussion of limitation 1D in the Petition appears to describe various parts of what could be considered as the normal operation of a generic voltage regulator. *See* Pet. 30–31; *see, e.g., id.* (“In normal operation of a DC-DC power converter, the output voltage is maintained at a desired value such that the feedback signal is equal to the reference voltage.” (citing Ex. 1003 ¶ 64 (testimony in the Background of the Technology section, rather than a discussion of TI’s disclosure))). For

⁷ Although the challenge of ground 1 is couched as anticipation or, in the alternative, obviousness, Petitioner contends that “TI anticipates limitation 1[D].” Pet. 31 (brackets in original). Petitioner makes obviousness assertions for limitations 1A and 1C. *See id.* at 28, 30.

example, Petitioner contends that a person of ordinary skill in the art would understand that voltage regulators regulate voltage based on feedback by using MOSFETS, and that “a POSITA would understand that switching the MOSFETS on and off would *charge* the bootstrap capacitor at least during the time when the high-side switch is off and the low-side switch is on.” *Id.* at 30 (emphasis added) (citing Ex. 1003 ¶ 132 (stating the same or similar but without citations to evidence)). However, as Petitioner notes, the ’608 patent describes how, in certain situations of normal operation, there may be some charging, but the switching is such that “the bootstrap voltage may drop over time, resulting in the inability to operate the high-side switch properly (until the bootstrap voltage can be refreshed).” *Id.* at 4–5 (citing Ex. 1001, 3:3–27; Ex. 1003 ¶ 84); *see also* Ex. 1003 ¶ 84 (“In such a situation, the low-side switch is never on long enough to properly charge the bootstrap capacitor sufficiently . . . [and, in another situation] the bootstrap capacitor does not have the chance to be fully charged.”). Thus, even if the normal switching identified by Petitioner for limitation 1D results in some charging, Petitioner has not adequately explained how that equates to a disclosure in TI of the recited “bootstrap refresh control circuit [that] is configured to control the [two switches] . . . based on the difference signal so as to charge the bootstrap capacitor for *refreshing* the bootstrap voltage signal.” *See* Pet. 30–31 ((omitting the “for refreshing” phrase from the characterization of the limitation and lacking the “refreshing” term in the contentions)).

Further, as mentioned, limitation 1D requires that the bootstrap refresh control circuit be configured to control both switches “based on the [converter output voltage] difference signal” and that this occurs when the

feedback signal indicates that the converter voltage is low. Patent Owner argues, “[t]he TI Datasheet’s output current control does not meet the claimed turning on and off of the high side switch when the feedback signal is smaller than the reference voltage, based on the difference signal.”

Prelim. Resp. 13–14. Patent Owner, with the support of Mr. McAlexander’s testimony, asserts that the high side switch in TI is turned on by an oscillator, not based on the difference feedback. *See, e.g., id.* at 14 (citing Ex. 2001 ¶ 55).

In that regard, Petitioner contends:

TI discloses the output of the disclosed error amplifier connected to Power Stage Logic (indirectly, through the HS Current Comparator), and that the Power Stage Logic provides control signals for controlling the high-side and low-side switches. EX1006, 6; EX1003, ¶133. Therefore, a POSITA would understand that TI’s disclosed Power Stage Logic switches on and off the high-side and low-side switches based on the output of the error amplifier, thus charging the bootstrap capacitor. EX1003, ¶133. A POSITA would also understand that this would include when the feedback signal is less than the reference voltage, as described above. *Id.* Therefore, TI anticipates limitation 1[D]. *Id.*

Pet. 31. Thus, Petitioner contends that TI discloses that the Power Stage Logic operates both switches based on feedback from the error amplifier. Notably, the block quote above contains only one citation to TI for this purported disclosure of how the circuitry controls the switches. That one citation is TI’s page 6, which merely is the Functional Block Diagram. *See* Ex. 1006, 6. For the critical proposition that TI discloses controlling both the high-side and low-side switches based on the difference signal, Petitioner relies on Dr. Holberg opinions as to what “a POSITA would understand.” *See* Pet. 31 (citing Ex. 1003 ¶ 133).

The cited paragraph of Dr. Holberg’s declaration also lacks any citation to TI for the opinions as to what TI purportedly discloses. *See* Ex. 1003 ¶ 133.⁸ Dr. Holberg’s opinion that, “[t]hus, when the output of the error amplifier indicates that the output voltage is different (either less than or greater than) than the reference signal, TI’s Power Stage & Deadtime Control Logic is configured to control the high side switch to switch on and off based on the difference signal” is conclusory and does not flow logically from the preceding sentences in the paragraph. *See id.* To the extent that Dr. Holberg’s opinion is based on the lines, depicted in the Functional Block Diagram, from the Error Amplifier to the black box labeled “Power Stage & Deadtime Control Logic,” this does not demonstrate adequately, for purposes of institution, the configuration of that Logic that would support an anticipatory challenge to the claim. *See* Ex. 1006, 6.

Patent Owner also argues that “Claim 1[D] and the TI Datasheet described distinctly different control types.” Prelim. Resp. 17 (brackets in original). Patent Owner notes that TI states that the device uses a fixed frequency, peak current mode control and that “[a]n internal oscillator initiates the turn on of the high-side power switch.” *Id.* at 14 (citing, *inter alia*, Ex. 1006, 11⁹). According to Mr. McAlexander, there are different

⁸ Dr. Holberg, in paragraph 133, cites to paragraphs 68 and 69 of his declaration in support of opinions as to what TI discloses. Those paragraphs are under the heading “DC-DC Converters” in the Background of the Technology section (beginning on page 16 of the declaration). *See* Ex. 1003 ¶ 63.

⁹ Patent Owner is citing to exhibit page number 11, which corresponds to page 10 of the underlying document.

types of control schemes for voltage converters. Ex. 2001 ¶ 63. Mr. McAlexander testifies as follows:

[I]t is my opinion that the TI Datasheet is different from the '608 Patent's 1[D] limitation. As I described above, 1[D] requires that the high side switch is turned on during a triggering event—"when the feedback signal is smaller than the reference voltage signal." Accordingly, a POSITA would understand that the triggering event would encompass a control mode such as a COT [(Constant On-Time)] control mode. This is because the COT control mode turns the high side switch ON based on directly comparing to the feedback signal. (EX2006, 3). Conversely, the TI Datasheet uses a fixed frequency current mode control. (EX1006 at 11). This is different from the triggering event recited in 1[D] in the '608 Patent because a fixed frequency control mode uses a clock to turn the high side switch ON every clock cycle. (EX2004, 2).

Ex. 2001 ¶ 75; *see also id.* ¶¶ 55–74 (describing, *inter alia*, different control topographies).

We need not, for purposes of determining whether to institute an *inter partes* review, find that Mr. McAlexander's testimony and Patent Owner's arguments are correct. However, those arguments and evidence, based on a direct quote from TI regarding oscillator control of the high-side switch, highlight the Petition's lack of adequate explanation as to how TI discloses limitation 1D. Petitioner does not contend that limitation 1D would have been obvious. *See* Pet. 30–31. We determine that Petitioner has failed to demonstrate a reasonable likelihood of prevailing in its challenge to claim 1 as anticipated by or as obvious over TI.

3. *The Alleged Unpatentability of Independent Claims 11 and 12*

The remaining claims subject to this ground are independent claims 11 and 12. Claim 11 recites a voltage converter having a bootstrap refresh control circuit and claim 12 recites a bootstrap refresh control

method. *See* Ex. 1001, 23:10–24:26. Petitioner does not draw a pertinent distinction between limitation 1D and the similar limitations in claims 11 and 12, and Petitioner’s arguments against these claims refer to and rely on the same contentions discussed above regarding the claim 1. *See* Pet. 32–35; Prelim. Resp. 11–12 n.1 (“Petitioner treats all three limitations as the same.”). Thus, Petitioner also has not shown a reasonable likelihood of prevailing in showing that claims 11 and 12 are anticipated by or would have been obvious over TI.

4. *Discretionary Denial*

Patent Owner argues that “[t]he Board should exercise its discretion to deny the Petition under 35 USC §§ 314(a) and 316(b).” Prelim. Resp. 60–61. Patent Owner specifically argues that “Petitioner has presented an excessive number of faulty grounds, each of which contain superficial analysis on a bevy of claim limitations for the independent claims,” and that “[t]his warrants denial.” *Id.* at 61 (citing *Adaptics Ltd. v. Perfect Co.*, IPR2018-01596, Paper 20 (PTAB March 6, 2019)).

If the Board institutes an *inter partes* review, it does so on all challenged claims on all asserted grounds. *See SAS Inst. Inc. v. Iancu*, 138 S. Ct. 1348, 1354, 1359–60 (2018); 37 C.F.R. § 42.108(a) (“When instituting *inter partes* review, the Board will authorize the review to proceed on all of the challenged claims and on all grounds of unpatentability asserted for each claim.”). When a petition fails to satisfy the “reasonable likelihood” institution standard as to some challenges, the Board evaluates “all the challenges and determine[s] whether, in the interests of efficient administration of the Office and integrity of the patent system, the entire

petition should be denied.” Patent Trial and Appeal Board Consolidated Trial Practice Guide¹⁰ 64 (Nov. 2019) (citing 37 C.F.R. §§ 316(b), 326(b)).

Here, Petitioner advances five challenges with four directed to the same three independent claims. Pet. 3. We, for the reasons discussed below, determine that Petitioner has failed to show a reasonable likelihood of prevailing on Grounds 2 through 5. We further determine that, based on the particular facts of this proceeding, instituting a trial with respect to all grounds and all the challenged claims based on evidence and arguments directed only to Ground 1 would not be an efficient use of the Board’s time and resources. *Cf. Chevron Oronite Co. LLC v. Infineum USA L.P.*, IPR2018-00923, Paper 9, 10–11 (PTAB Nov. 7, 2018) (informative); *Deeper, UAB v. Vexilar, Inc.*, IPR2018-01310, Paper 7 (PTAB Jan. 24, 2019) (informative). Thus, even if Petitioner met the requisite burden for institution as to Ground 1, we would exercise our discretion and not institute an *inter partes* review.

E. The Alleged Anticipation of Claims 1, 11, and 12 by Galinski (Ground 2)

Petitioner alleges that independent claims 1, 11, and 12 of the ’608 patent are anticipated by Galinski. *See* Pet. 35–45. Patent Owner argues that Galinski lacks certain aspects of limitations 1A, 1C, and 1D. *See* Prelim. Resp. 34–43.

1. Galinski (Ex. 1005)

Galinski pertains to “switching regulators and, in particular, to a buck switching regulator including bootstrap voltage monitoring to achieve very high duty cycles.” Ex. 1005, 1:8–10.

¹⁰ Available at <https://www.uspto.gov/sites/default/files/documents/tpgnov.pdf>.

feedback voltage V_{FB} and feeding back the feedback voltage V_{FB} to an error amplifier where the feedback voltage is compared to a reference voltage.”

Id. at 5:56–61. “The error voltage generated by error amplifier is indicative of the difference between the feedback voltage and the reference voltage.”

Id. at 5:61–63.

In buck regulator 100, high-side driver circuit 116 is supplied by a bootstrap voltage V_{BOOST} and the switching output voltage V_{SW} while low-side driver circuit 118 is supplied by a V_{DD} voltage and the ground voltage. When both power switches Q1 and Q2 are N-channel MOSFET devices, bootstrap voltage V_{BOOST} is used to supply the high-side driver circuit 116 to ensure that the driver circuit can turn on the high-side power switch Q1 completely without using a separate higher supply voltage.

Id. at 6:50–58.

At one-shot comparator circuit 112, the monitor voltage V_{MON} [which is a scaled down voltage of bootstrap voltage V_{BOOST}] is compared to the switching output voltage V_{SW} . When the monitor voltage V_{MON} is equal to or less than voltage V_{SW} , comparator circuit 112 generates a reset pulse as the output voltage signal V_{RST} . The reset pulse is of a short duration where the duration is sufficient to allow capacitor C_{BST} to be recharged.

Id. at 9:1–7; *see id.* at 8:34–35. “Using of the one-shot pulse has the advantage that the power switches are only switched for a minimal time necessary to refresh or recharge the bootstrap voltage V_{BOOST} and bootstrap voltage control circuit 110 returns control of the power switches to buck regulator 100 to regulate the duty cycle of the power switches to provide the desired output voltage V_{OUT} .” *Id.* at 9:35–41; *see also id.* at 10:31–35 (“When voltage V_{SW} switches to 0 volt, capacitor C_{BST} of the bootstrap circuit is recharged up to the V_{DD} voltage. At the end of the recharge phase,

buck regulator 100 returns to normal operation where buck regulator 100 is again operated at near 100% duty cycle.”).

2. Discussion

“In an IPR, the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3)). Here, Petitioner’s contentions are difficult to follow and it is not clear that Petitioner is consistently mapping Galinski’s disclosures to the limitations of claim 1. For at least the following reasons, we determine that Petitioner has not adequately explained how Galinski discloses all of the limitations of claim 1 arranged as in the claim.

Limitation 1A recites a comparing module and involves a comparison of the bootstrap voltage against the bootstrap refresh threshold. *See* Ex. 1001, 19:9–26. For that limitation, Petitioner points to “comparator circuit 112 [of Galinski’s Figure 2] that receives a monitor voltage V_{MON} at a first input and a switching output voltage V_{SW} at a second input.” Pet. 37 (citing Ex. 1005, 8:30–53, Fig. 2). Petitioner contends that “[a] POSITA would recognize that V_{MON} is derived from bootstrap voltage V_{BOOST} and thus represents, expressly or inherently, the voltage across the bootstrap capacitor.” *Id.* at 38 (citing Ex. 1005, 7:28–41; Ex. 1003 ¶¶ 155–156). Although Galinski’s comparison using V_{MON} as the input, we understand Petitioner to map V_{BOOST} to the recited “bootstrap voltage.” *See id.*; *see also id.* at 40 (referring to the “refreshing the bootstrap voltage V_{BOOST} .”). For limitation 1A, Petitioner maps switching output voltage V_{SW} to the recited “bootstrap refresh threshold,” asserting that “the switching output voltage V_{SW} is a threshold against which the bootstrap voltage is compared to determine whether to recharge the bootstrap capacitor, i.e. a bootstrap

refresh threshold.” *Id.* at 39; *but see* Prelim. Resp. 42 (Patent Owner disputing Petitioner’s mapping, arguing that “the switching output voltage V_{SW} drives the output voltage V_{OUT} and is not the claimed ‘bootstrap refresh threshold.’” (citing Ex. 2001 ¶ 129)).

Petitioner, for limitation 1C—which uses the signal from the comparing module of limitation 1A as the trigger to reduce the output voltage of the converter—appears to pivot in its mapping of the recited “bootstrap refresh threshold.” *See* Pet. 40–41; Ex. 1001, 19:39–41 (limitation 1C). Petitioner contends:

When the bootstrap voltage (V_{BOOST}) is equal to or less than the *threshold voltage* (V_{th}), the comparator generates an output pulse (V_{RST}), causing the power switches Q1 and Q2 to switch, thereby refreshing the bootstrap voltage V_{BOOST} . [Ex. 1005], 9:3-5. During this recharge phase, the switching output voltage V_{SW} switches from input voltage V_{in} to 0 volt temporarily. EX1005, 10:19-23. A POSITA would understand that a decrease in V_{SW} would necessarily lead to a decrease in V_{OUT} . EX1003, ¶¶160-61.

Pet. 40–41 (emphasis added). Thus, we understand Petitioner to contend that switching voltage V_{SW} is the “bootstrap refresh threshold” in the comparison of limitation 1A but, for limitation 1C, is a voltage driven to zero as a result of a comparison involving a “threshold voltage (V_{th}).” Due to this apparent inconsistent mapping, Petitioner has not shown with the requisite particularity how Galinski discloses both limitations 1A and 1C.

Further, Patent Owner argues, with the supporting testimony of Mr. McAlexander, that:

Galinski operates its switches in two ways, either they are operating normally, or they are responding to a reset pulse to recharge the capacitor. (See EX2001, ¶¶115-16 (describing that the switches are controlled during normal operation to achieve a desired output voltage, but that during the reset pulse,

the normal operation is disabled and the high side switch is turned off and the low side switch is turned on.) There is normal operation circuitry that regulates the switches to reach a desired output voltage V_{OUT} and reset circuitry that disables the voltage regulation circuitry's ability to control the switches under normal operation. (EX2001, ¶ 117.) Problematically, Petitioner relies on reset circuitry for 1[A] and 1[C] and normal operational circuitry for 1[B] and 1[D], but the normal operation circuitry is not responsible for charging the bootstrap capacitor. (EX2001 at ¶¶118-119.)

Prelim. Resp. 35–36.

We agree with Patent Owner that Petitioner is mapping two different modes of operation to different limitations of claim 1.¹¹ For limitation 1C, Petitioner relies on portions of Galinski's from column 9 and the top of column 10. Pet. 40 (citing Ex. 1005, 9:3–5, 10:19–23). That section discloses, *inter alia*, the one-shot pulse of the one-shot comparator circuit where “power switches Q1 and Q2 are caused to switch in response to the reset pulse and the bootstrap voltage V_{BOOST} is thereby refreshed.” Ex. 1005, 9:19–21. That section also discloses that, after the bootstrap voltage is refreshed or recharged, “bootstrap voltage control circuit 110 returns control of the power switches to buck regulator 100 to regulate the duty cycle of the power switches to provide the desired output voltage V_{OUT} .” *Id.* at 9:35–41;

¹¹ In anticipation, “it is not enough that the prior art reference . . . includes multiple, distinct teachings that [an] artisan might somehow combine to achieve the claimed invention.” *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1371 (Fed. Cir. 2008). Rather, the reference must “clearly and unequivocally disclose the claimed [invention] or direct those skilled in the art to the [invention] without *any* need for picking, choosing, and combining various disclosures not directly related to each other by the teachings of the cited reference.” *Id.* (quoting *In re Arkley*, 455 F.2d 586, 587 (CCPA 1972)).

see also id. at 10:32–35 (“At the end of the recharge phase, buck regulator 100 returns to normal operation where buck regulator 100 is again operated at near 100% duty cycle.”). Consistent with this disclosure, Mr. McAlexander testifies that Galinski generally operates in a normal switching mode, but, upon a reset pulse, disables the normal operation and changes to a mode where the switches are toggled so as to refresh the refresh the bootstrap capacitor, and then, after the reset pulse, returns to normal operation. Ex. 2001 ¶ 115.

For limitation 1D—which requires that, when the feedback signal indicates that output voltage is low, a bootstrap refresh control circuit configured to control both switches “based on the difference signal so as to charge the bootstrap capacitor for refreshing the bootstrap voltage signal”—Petitioner appears to rely on Galinski’s normal operations. *See* Pet. 41–42; *see, e.g., id.* at 41 (“A POSITA would understand that, *in normal operation of a DC-DC power converter*, the output voltage is maintained at a desired value such that the feedback signal is equal to the reference voltage.” (emphasis added)). Petitioner has not explained adequately the apparent inconsistent mapping of modes to the limitations of claim 1 and has not explained adequately how the circuitry of Galinski’s normal mode satisfies all of the aspects of limitation 1D.

Petitioner, for independent claims 11 and 12, relies on the same unpersuasive contentions made for claim 1 and discussed above. *See* Pet. 42–45.

We determine that Petitioner has failed to demonstrate a reasonable likelihood of prevailing in its challenge to independent claims 1, 11, and 12 as anticipated by Galinski.

*F. The Alleged Obviousness of Claims 1, 2, 11, 12, and 16
Over Galinski and Li and/or the Knowledge of Ordinary Skill (Ground 3)*

Petitioner alleges that “[c]laims 1, 2, 11, 12, and 16 are rendered obvious by Galinski in view of Li and/or the knowledge of ordinary skill.” Pet. 46 (section heading); *see id.* at 46–47 (addressing claim 1).

Patent Owner argues that, “[i]n Ground 3, Petitioner relies on the exact same arguments as it did in Ground 2 for the independent claims, but instead of arguing an anticipation theory, Petitioner argues that Galinski renders the claims obvious.” Prelim. Resp. 43–44 (citing Pet. 47, 49). Patent Owner further argues that “Petitioner offers no additional substance to support *why* Galinski renders the limitations obvious,” and that Petitioner offers only conclusory assertions without analysis. *Id.* at 44–45.

Petitioner specific discussion of independent claim 1, in its entirety, follows:

Galinski teaches every element of claim 1. *See* §VII.B.1, *supra* (incorporated here); EX1003, ¶189; *see also* §VI.A, *supra* (incorporated here), EX1003, ¶¶49-62, 87-99, 148-62. To the extent that Galinski does not expressly or inherently disclose the one-shot comparator circuit 112 outputting a signal having a first logic state when the bootstrap voltage signal is lower than the bootstrap refresh threshold and a second logic state when the bootstrap voltage signal is larger than the bootstrap refresh threshold, Galinski renders this feature obvious to a POSITA. EX1003, ¶¶57–62, 155. Similarly, to the extent that Galinski does not expressly or inherently disclose the bootstrap voltage control circuit 110 receiving a bootstrap refresh threshold, Galinski renders this feature obvious to a POSITA. EX1003, ¶156.

Pet. 47. In this discussion above, Petitioner does not mention Li, and, for its obviousness challenge to independent claim 1, Petitioner is relying only on Galinski and possibly the knowledge of a person of ordinary skill in the art.

See id.; *see also id.* at 46 (“A POSITA would have been motivated to modify Galinski *based on the knowledge of ordinary skill* or combine Galinski with Li to arrive at the features of claims 1–2, 11–12, and 16 for numerous reasons presented below.” (emphasis added)); *id.* at 47 (“A POSITA would find it straightforward to adapt the ideas presented in Li, or *within a POSITA’s knowledge*, to Galinski’s DC-DC converter with predictable results.” (emphasis added)). For independent claims 11 and 12, Petitioner relies on the same contentions made for independent claim 1. *Id.* at 49.

As shown in the block quote above, Petitioner’s assertions of obviousness take the following form: “To the extent that Galinski does not expressly or inherently disclose [a recited feature] . . . , Galinski renders this feature obvious to a POSITA.” *Id.* at 47. These assertions are too conclusory to satisfy the threshold burden for institution as the Petition does not explain adequately how or why Galinski would be modified so as to arrive at the claimed invention. *See id.*; *see also id.* at 46 (providing, under the “Motion to Combine” heading, a purported reason why Galinski would be combined with Li’s hysteresis monitoring (apparently for dependent claim 2), but not addressing the single-reference challenge to the independent claims).

The remaining claims challenged in this ground, claims 2 and 16, are dependent claims. Ex. 1001, 19:49–58, 26:9–19. Petitioner contends those claims recite “hysteresis monitoring of the bootstrap voltage signal,” and relies on Li for the recited limitations of these dependent claims. Pet. 48–49. Petitioner does not rely on Li in any persuasive manner that cures the underlying defect in the articulation of the ground of alleged obviousness of the independent claims. *See id.*

We determine that Petitioner has not shown a reasonable likelihood of prevailing in showing that claims 1, 2, 11, 12, and 16 would have been obvious over Galinski and Li and/or the knowledge of ordinary skill.

G. The Alleged Obviousness of Claims 1, 6, 11, 12, and 15 Over Wong (Ground 4)

Petitioner alleges that independent claims 1, 11, and 12 and dependent claims 6 and 15 would have been obvious over Wong. *See* Pet. 49–58 (addressing independent claim 1). Patent Owner argues that “Petitioner fails to describe how that switch [in Petitioner’s proposed modification] would be controlled, leaving the limitations relating to its control (1[PRE] and 1[D]) untaught” and that “POSITA would not have replaced a Zener diode in Wong’s circuits with a switch.” Prelim. Resp. 45. For the reasons discussed below, we determine that Petitioner has not demonstrated a reasonable likelihood of prevailing under this Ground 4 challenge.

1. Wong (Ex. 1007)

Wong pertains to “a non-synchronous dc-dc converter having a bootstrap capacitor and a control circuit and, more particularly, to a method for controlling the charge of a bootstrap capacitor for non-synchronous type DC-DC converter.” Ex. 1007, 1:9–13. Wong explains that “[o]ne problem of the conventional bootstrap method is that the bootstrap capacitor may not be fully charged at light load or no load conditions.” *Id.* at 2:3–5. To address this problem, a dummy load may be added to “maintain a certain amount of current flow in the inductor to keep the switching of the output node.” *Id.* at 2:22–25. However, “this method will reduce the efficiency of the DC-DC converter for all the conditions.” *Id.* at 2:25–27.

Wong states that “[t]he purpose of this invention is to provide a method to control the charge in the bootstrap capacitor for step-down

switch 25 formed by a transistor 25.” *Id.* at 4:34–37. Wong, in describing the embodiment of Figure 3 (not shown here), explains:

The BS voltage detector 21 detects the voltage across the bootstrap capacitor 7, and compares the detected voltage with a predetermined voltage VBS. The voltage VBS is the preset threshold voltage which is higher than the minimum required voltage for the bootstrap to work. When the voltage across the bootstrap capacitor becomes less than the voltage VBS, the BS voltage detector 21 produces a high level signal. When the light load is detected, and the BS voltage detector 21 produces high level signals, the on-time control 23 produces a high level signal to turn on the secondary transistor 25, during the off-time of the main power transistor 3. The on-time of the secondary transistor 25 is determined by the on-time control 23. When the secondary transistor 25 is turned on, LX voltage will be pulled near to the ground voltage. Hence, the bootstrap capacitor 7 is charged up to “VREF-VD”.

Id. at 4:66–5:14; *see also id.* at 5:62–64 (“The second embodiment shown in FIG. 6 differs from the first embodiment of FIG. 3 in that the second embodiment does not have a light load detector 19.”). In the embodiment of Figure 6, “[t]he on-time of the secondary transistor 25 is determined by the duration when the maximum voltage is higher than the ramping signal, or by using the same method as described in FIG. 5.” *Id.* at 5:66–6:3. “During normal operation, when the bootstrap voltage can be maintained above the threshold voltage, the secondary switch is always off and consumes no current.” *Id.* at 2:62–65.

“As shown in FIG. 3, in a PWM DC-DC converter, the duty cycle is determined by a comparator 4 which compares the output of the error amplifier 2 with a triangular signal produced from oscillator 6.” *Id.* at 5:20–23. “As shown in FIG. 4B, when the error amplifier output is higher

than the triangular oscillator output, the PWM output is high and the power transistor 3 is turned on.” *Id.* at 5:23–26.

2. Discussion

Petitioner’s proposed modification of Wong pertains to the low-side switch recited in claim 1, and involves the replacement of Wong’s diode 5 with a low-side switch. *See* Pet. 50, 56. Petitioner contends that “[a] POSITA would understand that a low-side diode is analogous to a low-side switch and that replacing Wong’s low-side diode with a low-side switch is an obvious variation of Wong’s converter system,” and that “[t]he motivation for using a low-side switch is for greater conversion efficiency and is well-known in the art. *Id.* at 50–51 (citing Ex. 1003 ¶¶ 65–68, 199). Petitioner, further describing the proposed modification, contends that, “if Wong’s low-side diode was replaced with a low-side switch, Wong’s secondary switch [transistor 25] would be unnecessary for pulling the switching-node voltage near to ground, because that function could be performed by the low-side switch.” *Id.* at 56 (citing Ex. 1003 ¶ 214).

Patent Owner argues, “[t]he Petition fails to address how its purported combination (which replaces a Zener diode with switch) would be driven according to 1[PRE] or controlled to switch according to 1[D].” Prelim. Resp. 45–46 (citing, *inter alia*, Ex. 2001 ¶¶ 133–137).

For the recited configuration of the control circuitry of the bootstrap refresh module of limitation 1C (which decreases the output voltage when the bootstrap capacitor voltage is low), Petitioner relies on Wong’s disclosure of controlling secondary transistor 25. *See* Pet. 55 (citing Ex. 1007, 5:3–24; Ex. 1003 ¶ 212). Similarly, for the recited configuration of the control circuitry of bootstrap refresh control circuit of limitation 1D (when the output voltage is low, switch on and off both switches for

refreshing the bootstrap voltage), Petitioner relies on Wong’s disclosure of controlling secondary transistor 25. *See id.* at 57. However, in Petitioner’s proposed modification, secondary transistor 25 “would be unnecessary.” *Id.* at 56. The proposed modification replaces diode 5 with a switch, but Petitioner does not explain adequately or persuasively how the configuration of Wong’s control circuitry would be modified to drive a component that previously was a diode¹² to arrive at the recited control circuitry scheme of limitation 1D where two switches are switched on and off based on the output voltage difference for refreshing the bootstrap voltage.

Patent Owner also argues that Petitioner has failed to provide a motivation for replacing the diode with a switch. *See* Prelim. Resp. 52–58. Patent Owner asserts that “Petitioner does not acknowledge that Wong’s Zener diode 5 . . . is in fact a Zener diode, nor does Petitioner appreciate the Zener diode’s functionality in the circuit,” and that “[r]eplacing the Zener diode with a switch defeats the functionality of the Zener diode, and a POSITA would not have made this change.” *Id.* at 52–53 (citing Ex. 1005, Fig. 6; Ex. 2001 ¶ 144). Patent Owner, with the supporting testimony of Mr. McAlexander, discusses at length the purpose and operation of the diode in Wong’s circuit. *See id.* at 53–58.

In order to determine whether Petitioner has met the burden for institution, we need not make findings as to the purpose and operation of the diode. Regardless as to the specific details of diode 5, it cannot be disputed that diode 5, as well as the secondary switch (transistor) 25, are utilized together in Wong’s circuit for some substantive reason. *See, e.g.,* Pet. 22–

¹² Dr. Holberg distinguishes Wong’s “free-wheeling diode 5 acting as a low-side switch” and “an actively controlled switch.” Ex. 1003 ¶ 118.

24, 50 (Petitioner characterizing the purpose of the secondary switch and the diode). Petitioner’s proposed modification of Wong effectively is the deletion of diode 5, the deletion of (or at least rendering “unnecessary”) the existing secondary switch 25, and the addition of a new secondary switch notwithstanding that Wong’s circuit, prior to modification, had a secondary switch. *See* Pet. 56. Petitioner has not explained adequately and persuasively why a person of ordinary skill in the art would have made such a modification.

For independent claims 11 and 12, Petitioner relies on the unpersuasive contentions discussed above. *See* Pet. 62–65. For dependent claims 6 and 15, Petitioner’s contentions do not cure the defects in the challenge to the underlying independent claims. *See id.* at 58–62, 65–66; *see, e.g., id.* at 58–59 (relying on Wong’s pre-modification disclosure of controlling the secondary switch—a switch rendered unnecessary in the proposed combination).

We determine that Petitioner has not shown a reasonable likelihood of prevailing in showing that claims 1, 6, 11, 12, and 15 would have been obvious over Wong.

H. The Alleged Obviousness of Claims 6 and 15 Over Galinski, or, Alternatively, Galinski and Wong (Ground 5)

This Ground 5 challenges dependent claims 6 and 15, and builds on Ground 2, the anticipation challenge to the independent claims. *See* Pet. 66–73. For dependent claims 6 and 15, Petitioner’s contentions do not cure the defects in the challenge to the underlying independent claims. *See id.* Thus, for the same reasons discussed above, Petitioner has not shown a reasonable likelihood of prevailing in showing that claims 5 and 16 would have been obvious over Galinski alone or Galinski in view of Wong.

III. CONCLUSION

Petitioner has not demonstrated that there is a reasonable likelihood of establishing the unpatentability of any of the challenged claims of the '608 patent.

IV. ORDER

For the foregoing reasons, it is

ORDERED that the Petition is *denied* and no trial is instituted.

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Patent 9,590,608 B2

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