

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner
v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner

Case No.: IPR2024-00909
U.S. Patent No. 10,658,378
Issue Date: May 19, 2020
Title: THROUGH ARRAY CONTACT (TAC) FOR
THREE-DIMENSIONAL MEMORY DEVICES

**PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 10,658,378
PURSUANT TO 35 U.S.C. §§311-319 AND 37 C.F.R. §42**

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LISTING OF EXHIBITS

Exhibit	Description
1001	U.S. Patent No. 10,658,378 to Tao et al.
1002	File History of U.S. Patent No. 10,658,378 to Tao et al.
1003	Declaration of Dr. Jack C. Lee (“Lee”)
1004	<i>Curriculum Vitae</i> of Dr. Jack C. Lee
1005	U.S. Patent Publ. No. 2017/0179026 A1 (“Toyama”)
1006	<i>Intentionally Omitted</i>
1007	<i>Intentionally Omitted</i>
1008	Minute Order, Dkt. No. 42, dated February 22, 2024 in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1009	Combined Civil and Criminal Federal Court Management Statistics (December 31, 2023), available at https://www.uscourts.gov/sites/default/files/data_tables/fcms_na_distcomparison1231.2023.pdf
1010	Docket from <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1011	CN109075169A Office Action, dated November 14, 2019
1012	Certified Translation of CN109075169A Office Action, dated November 14, 2019
1013	CN109075169A Reexamination Decision, dated November 25, 2021
1014	Certified Translation of CN109075169A Reexamination Decision, dated November 25, 2021
1015	Michelsoni, “3D Flash Memories” (2016)

Petition for *Inter Partes* Review of U.S. Patent No. 10,658,378

Exhibit	Description
1016	Aritome, “NAND Flash Memory Technologies” (2016)
1017	U.S. Patent No. 9,620,512 to Nishikawa et al.
1018	U.S. Patent Publ. No. 2016/0056188 A1 to Lee et al.
1019	U.S. Patent No. 9,293,348 to Lai et al.
1020	U.S. Patent No. 10,103,169 to Ge et al.
1021	U.S. Patent No. 8,697,519 to Jee et al.
1022	Excerpts from “Merriam-Webster’s Collegiate Dictionary,” Eleventh Edition (2014)
1023	Chang, “ULSI Technology” (1996)
1024	Chen, “CMS Devices & Technology for VLSI” (1988)
1025	Jaeger, “Volume V: Introduction to Microelectronic Fabrication” (1988)
1026	Wagner, “The Use of HBr in Polysilicon Etching,” Gases & Instrumentation International, Vol. 7, Issue 4, July/August (2013) printed from https://www.pall.com/content/dam/pall/microelectronics/literature-library/non-gated/HBr_Polysilicon.pdf
1027	Baker, “CMOS Circuit Design, Layout, and Simulation,” Third Ed. (2010)
1028	U.S. Patent No. 5,776,808 to Muller et al.
1029	U.S. Patent No. 9,236,393 to Cernea
1030	Excerpt from YMTC’s Exemplary Infringement Claim Chart for U.S. Patent No. 10,658,378 – 128L (Ex D-1 to YMTC’s Disclosure of Asserted Claims and Infringement Contentions), dated May 6, 2024 [PROTECTIVE ORDER MATERIAL – FILED UNDER SEAL]

Exhibit	Description
1031	Kim et al., “Three-Dimensional NAND Flash Architecture Design Based on Single-Crystalline Stacked Array,” IEEE Transactions on Electron Devices, Vol. 59, No. 1, Jan. 2012, pp. 35-45
1032	Capogreco et al., “Integration and electrical evaluation of epitaxially grown Si and SiGe channels for vertical NAND Memory applications,” 2015 IEEE International Memory Workshop, 2015
1033	Complaint for Patent Infringement, Dkt. No. 1, filed Nov. 9, 2023, in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1034	First Amended Complaint for Patent Infringement, Dkt. No. 29, filed Feb. 2, 2024, in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1035	Plaintiff and Counterclaim Defendant Yangtze Memory Technologies Company, Ltd.’s Disclosure of Asserted Claims and Infringement Contentions, dated May 6, 2024, in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL

Petitioner Micron Technology, Inc. (“Micron” or “Petitioner”) respectfully requests *Inter Partes* Review (“IPR”) of claims 1-7 and 18 (“the Challenged Claims”) of U.S. Patent Number 10,658,378 (the “378 Patent”). There is more than a reasonable likelihood that Petitioner will prevail with respect to at least one claim.

I. INTRODUCTION

Micron previously filed IPR2024-00788, which challenges a different set of claims from the 378 Patent than this Petition. §II.D. Concurrently filed herewith, Micron’s Explanation for and Ranking of Two Petitions explains the basis for filing this second Petition. Simply put, this Petition challenges claims that Patent Owner only asserted after Micron filed its earlier petition.

The 378 Patent’s title is “Through Array Contact (TAC) for Three-Dimensional Memory Devices.” As its title suggests, the 378 Patent relates to a three-dimensional (3D) NAND memory device with “through array contacts” (“TACs”). TACs are electrical connections that extend through the device’s memory array and may, for example, connect the memory array to a peripheral device located underneath the memory array.

Most elements of the Challenged Claims are conventional for 3D NAND memory devices, which existed long before the 378 Patent’s priority date. And the alleged point of novelty—the TACs—were not, in fact, new. The primary reference

After the Chinese Patent Office rejected all claims of the Chinese counterpart to the 378 Patent as unpatentable in view of Toyama, Patent Owner cited Toyama to the U.S. Examiner. However, despite the Chinese Patent Office rejecting claims materially identical to the claims challenged in this Petition, Patent Owner did **not** provide the U.S. Examiner with the Chinese rejection that specifically mapped Toyama to the claims. Perhaps due to Patent Owner's omission of the bases for the Chinese rejection, the Examiner never discussed or relied on Toyama in any rejection, overlooking that Toyama teaches or renders obvious all elements of the Challenged Claims. Confirming this, after Patent Owner appealed the Chinese rejection, a three-member panel of the Chinese Patent Office affirmed that all claims are unpatentable over Toyama. As this Petition explains, the elements of Toyama that teach the claimed "epitaxial layer" and "etch stop plug"—Toyama's "pedestal channel portions 11" and "drain regions 63," respectively—are the same elements that the Chinese Patent Office found to disclose these limitations. That the U.S. Examiner overlooked material teachings in Toyama provides a further reason for the Board to institute trial here.

In sum, because the Challenged Claims encompass prior art 3D NAND memory devices, and are nothing more than a routine, predictable combination of known elements, Petitioner requests that the Board institute trial and find the Challenged Claims unpatentable as obvious under Section 103.

II. REQUIREMENTS FOR INTER PARTES REVIEW

A. Grounds for Standing (37 C.F.R. §42.104(a))

Petitioner certifies that the 378 Patent is available for IPR and that no law bars Petitioner from requesting IPR of the Challenged Claims of the 378 Patent on the grounds identified herein.

B. Notice of Lead and Backup Counsel and Service Information (37 C.F.R. §§42.8(b)(3-4), 41.10(a))

Pursuant to 37 C.F.R. §§42.8(b)(3-4) and 41.10(a), Petitioner provides the following designation of Lead and Back-Up counsel.

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Petitioner consents to service by electronic mail at the following addresses: PTABDocketJJL2@orrick.com, P52PTABDocket@orrick.com, PTABDocketJ3B3@orrick.com, T61PTABDocket@orrick.com, PTABDocketP2S7@orrick.com, and micron-ymtc_ohs@orrick.com. Pursuant to 37 C.F.R. §42.10(b), Petitioner attaches a Power of Attorney.

C. Notice of Real-Parties-in-Interest (37 C.F.R. §42.8(b)(1))

Petitioner Micron Technology, Inc. and its subsidiaries, including Micron Consumer Products Group LLC, are the real-parties in interest.

D. Notice of Related Matters (37 C.F.R. §42.8(b)(2))

According to USPTO assignment records, the 378 Patent is currently assigned to Yangtze Memory Technologies, Co., Ltd. (“YMTC” or “Patent Owner”). YMTC has asserted the 378 Patent and U.S. Patent Nos. 10,861,872, 10,868,031, 10,937,806, 10,950,623, 11,468,957, 11,501,822, and 11,600,342 in a co-pending litigation, *Yangtze Memory Technologies Co., Ltd. v. Micron Technology, Inc. & Micron Consumer Products Group, LLC*, Case No. 3:23-cv-05792-RFL (N.D. Cal., filed November 9, 2023) (“Co-Pending Litigation”).

In addition to this Petition, Petitioner is filing (or has filed) petitions for *inter partes* review of each asserted patent in the Co-Pending Litigation:

Petition for *Inter Partes* Review of U.S. Patent No. 10,658,378

Patent	PTAB Proceeding	Wave 1/Wave 2
10,658,378 (claims 15-17 and 19-20)	IPR2024-00788	Wave 1 Petitions
10,861,872 (claims 1-6 and 11-13)	IPR2024-00789	
10,868,031	IPR2024-00790	
10,937,806 (claims 8-9 and 11-12)	IPR2024-00791	
10,950,623	IPR2024-00794	
11,468,957	IPR2024-00792	
11,501,822	IPR2024-00795	
11,600,342 (claims 1-6 and 8-20)	IPR2024-00793	
10,658,378 (claims 1-7 & 18)	IPR2024-00909	Wave 2 Petitions
10,861,872 (claims 7-10)	IPR2024-00910	
10,937,806 (claim 10)	IPR2024-00911	
11,600,342 (claim 7)	IPR2024-00912	

The Director and the Board should allow this Petition under 35 U.S.C. §314(a), 35 U.S.C. §325(d), and/or 37 C.F.R. §42.108(a). Concurrently filed herewith, Micron’s Explanation for and Ranking of Two Petitions explains the basis for filing this second Petition challenging a different set of claims of the 378 Patent.

E. Fee for *Inter Partes* Review

The Director is authorized to charge the fee specified by 37 C.F.R. §42.15(a), and any other required fees, to Deposit Account No. 15-0665.

F. Proof of Service

Petitioner has attached proof of service of this Petition on the Patent Owner at the correspondence addresses of record for the 378 Patent.

III. INSTITUTION SHOULD BE GRANTED

Petitioner has established a reasonable likelihood of success on the merits. Petitioner meets all other requirements for IPR. The Board should institute IPR.

A. There Are No Grounds for a § 314 Discretionary Denial

There is a pending district court action involving the 378 Patent. The PTAB has explained that it “will not ... discretionarily deny institution in view of a parallel district court litigation where a petition presents compelling evidence of unpatentability.” 6/21/22 Interim Procedure, 2, 4-5. Petitioner submits that it presents a compelling case here: the claims of the 378 Patent are unambiguously unpatentable.

Petitioner also notes that the factors considered by the Board when assessing whether to institute IPR in light of a parallel proceeding collectively weigh in favor of institution. *See Apple Inc. v. Fintiv, Inc.*, Case No. IPR2020-00019, Paper No. 11 (Mar. 20, 2020) (precedential) (“*Fintiv*”). In particular: the district court may stay the case, any potential trial will occur after the deadline for a final written decision, little district court work has occurred, petitioner diligently prepared this petition, and the petition is substantively strong.

1. Possibility of a Stay

Petitioner intends to seek a stay if the Board institutes IPR. Until this issue is adjudicated, any attempt to predict the outcome would require speculation. This factor is neutral. *See Sand Revolution II, LLC v. Continental Intermodal Group – Trucking LLC*, IPR2019-01393, Paper 24 at 7 (PTAB June 16, 2020) (informative) (“*Sand Revolution*”); *Fintiv* at 12 (similar).

2. Proximity of the Court’s Trial Date

On February 22, 2024, the district court entered a scheduling order which set a trial date of December 1, 2025. *See* Ex. 1008. As a result, if IPR proceedings are instituted, they should be completed well before the scheduled trial date. *See also* Ex. 1009 (statistics indicating that it takes on average 48.9 months to reach trial in district). This weighs strongly in favor of institution.

3. Investment in the Parallel Proceeding

To date, the parties and the district court have invested very little in the parallel proceeding. Indeed, beyond engaging in some motion practice regarding the pleadings, no substantive progress has been made. The parties are over a month away from completing the exchange of contentions and have not taken any depositions. Fact discovery is in its infancy. No claim construction positions have been exchanged, no claim construction order has issued, no infringement or invalidity expert discovery has occurred, and no summary judgment motions have been filed. This weighs in favor of institution. *See Sand Revolution* at 11.

The Board also has explained that institution is appropriate where “the petitioner filed the petition expeditiously....” *Fintiv* at 11. Here, Patent Owner asserted eight different patents against Petitioner. Ex. 1010. Petitioner proceeded with diligence, filing eight petitions approximately six months after being served with the original complaint and approximately three months after the filing of an amended complaint. *Id.*, Exs. 1033-34. After Petitioner filed these eight petitions, Patent Owner asserted new claims against Petitioner in district court on May 6, 2024. Ex. 1035. Petitioner has filed petitions on these new claims—claims that Petitioner could not have foreseen would be asserted—within two weeks. This also weighs strongly in favor of institution.

4. Issue Overlap

The wave 1 and wave 2 Petitions challenge all asserted claims in the Co-Pending Litigation. Should the Board institute, Micron stipulates that it will not advance in District Court any invalidity defense that formed the basis of any of the grounds in this Petition. Micron submits that this eliminates any potential overlap in issues between the proceedings here and in District Court. The Board has found that such stipulations weigh in favor of institution. *Sand Revolution* at 11-12.

5. Party Overlap

Both Petitioner and Patent Owner are parties in the parallel proceeding. This, however, is of little moment as there is often party overlap when there is a parallel proceeding.

6. Other Circumstances

Here, Petitioner submits that its petition has significant substantive merit. It is premised on clear, understandable prior art that the Patent Office did not previously consider. Thus, this factor also weighs in favor of institution.

B. Denial Under Section 325(d) Would Be Inappropriate

The two-part *Advanced Bionics* framework weighs against section 325(d) denial. At Part I, Patent Owner cited Toyama in an IDS after the Examiner indicated two dependent claims to be allowable, but failed to provide the Examiner with the Chinese Patent Office's rejection of claims materially identical to those two dependent claims. Regardless, at §II, the record demonstrates that the Examiner erred by overlooking Toyama's disclosures and failing to reject the claims in light of Toyama.

“[I]f the record of the Office's previous consideration of the art is not well developed or silent, then a petitioner may show the Office erred by overlooking something persuasive.” *Advanced Bionics, LLC v. Med-El Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 (PTAB Feb. 13, 2020), at 10 (precedential).

The record here is silent as to what, if any, substantive consideration the Examiner gave Toyama. As an initial matter, the Examiner never discussed Toyama or its teachings. *Becton, Dickinson, and Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 (Dec. 15, 2017), at 22-23 (factor (c)).

What's more, Patent Owner's conduct during prosecution may have prevented the Examiner from appreciating Toyama's significance. During prosecution, the Examiner issued an Office Action rejecting the then pending independent claims as obvious over two references, U.S. Patent No. 9,620,512 (Ex. 1017, "Nishikawa") and U.S. Pat. Pub. No. 2016/0056188 (Ex. 1018, "188 Publication"). Ex. 1002, 530. However, the Examiner indicated dependent claims 2 and 17 were allowable over these references. *Id.*, 536. Both claims recited structures that, as this Petition explains, were well-known to a POSITA: *an epitaxial layer, an etch stop plug, a staircase structure, slit structures, and contact layers* (claim 2); and *a staircase structure, a word line contact, and local contacts* (claim 17).¹ Ex. 1002, 106, 110. §V.A; *Becton, Dickinson*, at 25-28 (factor (f)). The Examiner only allowed now-challenged claims 1-7 after Patent Owner rewrote independent claim 1 to incorporate

¹ All red italicized text in this Petition is a quotation of the 378 Patent's claim language.

the limitations of original claim 2.² Ex. 1002, 564. And the Examiner only allowed now-challenged claim 18 after Patent Owner rewrote the independent claim upon which it depends (claim 15) to incorporate the limitations of original claim 17. *Id.*, 567.

After the Office Action, but before Patent Owner's response to it, the Chinese Patent Office rejected all claims of the corresponding Chinese patent application as unpatentable over Toyama.³ Ex. 1012 (certified translation of CN109075169A Office Action, dated Nov. 14, 2019), 3-10. The Chinese Patent Office's rejection explained how specific elements of Toyama taught the claim limitations. *Id.* Claim 2 of the Chinese application, which the Chinese Patent Office rejected, is materially

² Patent Owner's amendment included the exact elements of original claim 2 and also addressed an antecedent basis issue by expressly reciting "slit structures," to which original claim 2 referred.

³ Both the Chinese patent application and the application that issued as the 378 Patent claim priority to, and are national stage applications of, PCT App. No. PCT/CN2018/085421.

identical to original U.S. claim 2.⁴ And rejected claim 29 of the Chinese application is materially identical to original U.S. claim 17.⁵

Thus, at the time Patent Owner secured issuance by rewriting original claims 2 and 17 into independent form, it knew the Chinese Patent Office had rejected materially identical claims in view of a reference the U.S. Examiner was not aware of when he indicated the allowability of claims 2 and 17. Despite this, Patent Owner never notified the Examiner of the rejection or provided the Examiner with the Chinese Patent Office's written rejection or its reasoning. Patent Owner's failure to

⁴ Both claims depend on materially identical independent claims (claim 1 of the Chinese application, and original claim 1 of the U.S. application). Ex. 1014, 3. And both claims recite an *epitaxial layer*, an *etch stop plug*, a *staircase structure* ("ladder structure," in the English translation of the Chinese claim), *slit structures* ("crevice structures," in the English translation of the Chinese claim), and *contact layers*. *Id.*

⁵ Both claims depend on materially identical independent claims (claim 28 of the Chinese application, and original claim 16 of the U.S. application). Ex. 1014, 6. And both claims recite a *staircase structure* ("a ladder structure," in the English translation of the Chinese claim), a *word line contact*, and *local contacts disposed on the channel structures and the slit structures* ("crevice structures," in the English translation of the Chinese claim). *Id.*

disclose the Chinese Patent Office's reasoning—including the specific relied-upon elements of Toyama—may have been especially material because of Toyama's length (the reference spans 143 figures and 178 pages). In essence, Patent Owner only gave the Examiner a haystack (i.e., Toyama) despite also knowing the location of the needle (i.e., the specific elements of Toyama identified by the Chinese Patent Office).

The Petition demonstrates that the Examiner erred by overlooking specific teachings in Toyama. *Becton, Dickinson*, at 24-25 (factor (e)). As noted above, the Examiner only allowed the Challenged Claims of the 378 Patent after the applicant rewrote them to incorporate the limitations of original claims 2 and 17. As illustrated below, Toyama teaches each of these claims' limitations:

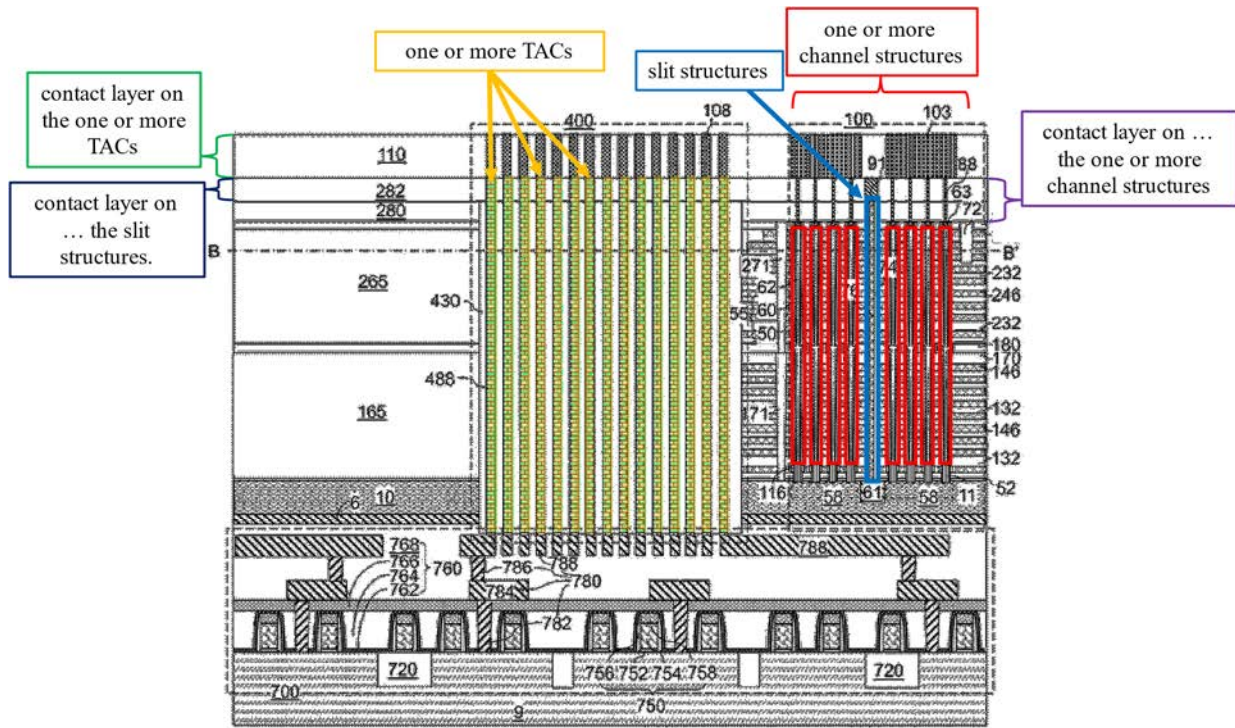


FIG. 17A

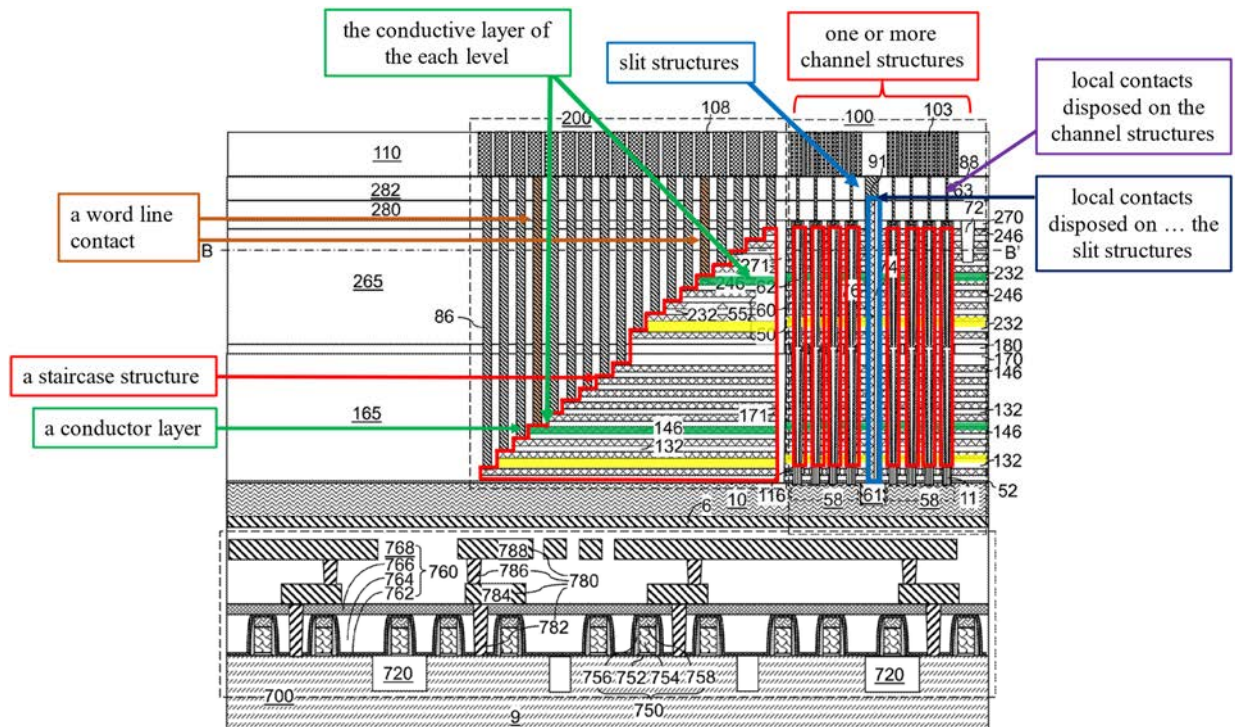


FIG. 17C

See generally Part IX.⁶

The Chinese prosecution history confirms Toyama's merit as an invalidating reference. After the Chinese Examiner maintained the rejection of all claims in view of Toyama, Patent Owner appealed. On appeal, a three-judge panel of the Chinese Patent Office affirmed the Chinese Examiner's rejection of all claims of a related Chinese patent application as unpatentable over Toyama. Ex. 1014 (certified translation of CN109075169A Reexamination Decision, dated Nov. 25, 2021). Notably, the Chinese Patent Office cited to the exact same structures identified in this Petition as disclosing the elements of Chinese claim 2 (i.e., original U.S. claim 2) and Chinese claim 29 (i.e., original U.S. claim 17). *Id.*, 3, 6, 14. To date, Patent Owner has been unable to obtain a patent in its native China corresponding to the 378 Patent. And, to date, Patent Owner has not disclosed this important information to the Patent Office in any continuation of the 378 Patent.

Because the U.S. Examiner overlooked specific teachings in Toyama that disclose what the U.S. Examiner considered as the points of novelty (i.e., the elements of original claims 2 and 17, which were incorporated into the Challenged Claims), the Board should not exercise its discretion under section 325(d) to deny institution.

⁶ Toyama's fourth exemplary structure (also relied upon in this Petition) also discloses the same elements.

IV. IDENTIFICATION OF CLAIMS BEING CHALLENGED (§42.104(B))

This Petition assumes that the 378 Patent’s earliest-listed priority date of May 3, 2018 is the priority date (the “Priority Date”).

Petitioner relies on the following references: (1) U.S. Pat. Pub. No. 2017/0179026 (Ex. 1005, “Toyama”).

Petitioner challenges the claims on the following ground:

Ground 1: Claims 1-7 and 18 would have been obvious over Toyama in view of the knowledge of a person of ordinary skill in the art (“POSITA”).

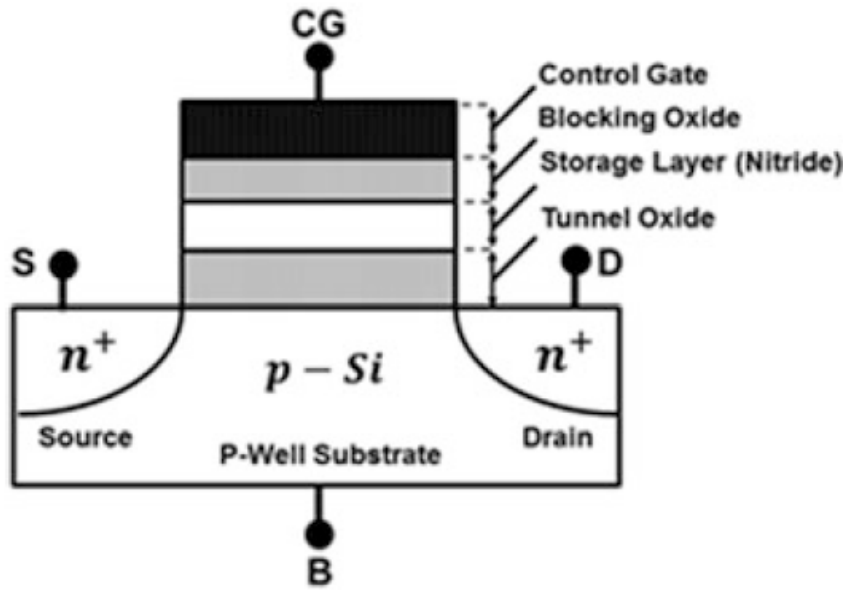
The Declaration of Dr. Jack C. Lee (Ex. 1003, “Lee”) supports this ground.

V. THE 378 PATENT

A. Technology Background

1. 3D NAND Flash Memories

The 378 Patent relates to three-dimensional (3D) NAND flash memory. “NAND” flash memory is a particular type of flash memory where cells form a structure similar to that of a NAND (not-AND) logic gate. Lee ¶ 43; Ex. 1015, 14. At the core of a NAND flash memory is a “memory cell,” which stores information as electrical charge. Lee ¶ 43. One example of a memory cell as shown below:



Ex. 1015, 41. In a memory cell, current flows from the “drain” of the device to the “source” of the device, which is connected to ground (e.g., the negative terminal of a power connection). *Id.*, 150 (“[T]he Source Line ... plays the role of the ‘local ground’ for each memory cell.”); Lee ¶ 42. A flash memory controller reads from or writes to a memory cell by applying a voltage to that cell’s “control gate,” labeled as “CG” in the above figures. *Id.*, ¶ 44.

Initially, a NAND flash memory was “planar,” that is, two-dimensional (2D). Lee ¶ 45. In 2D NAND flash memory, all memory cells lie on a 2D plane (*i.e.*, the x-y plane) on the surface of a memory chip as shown below:

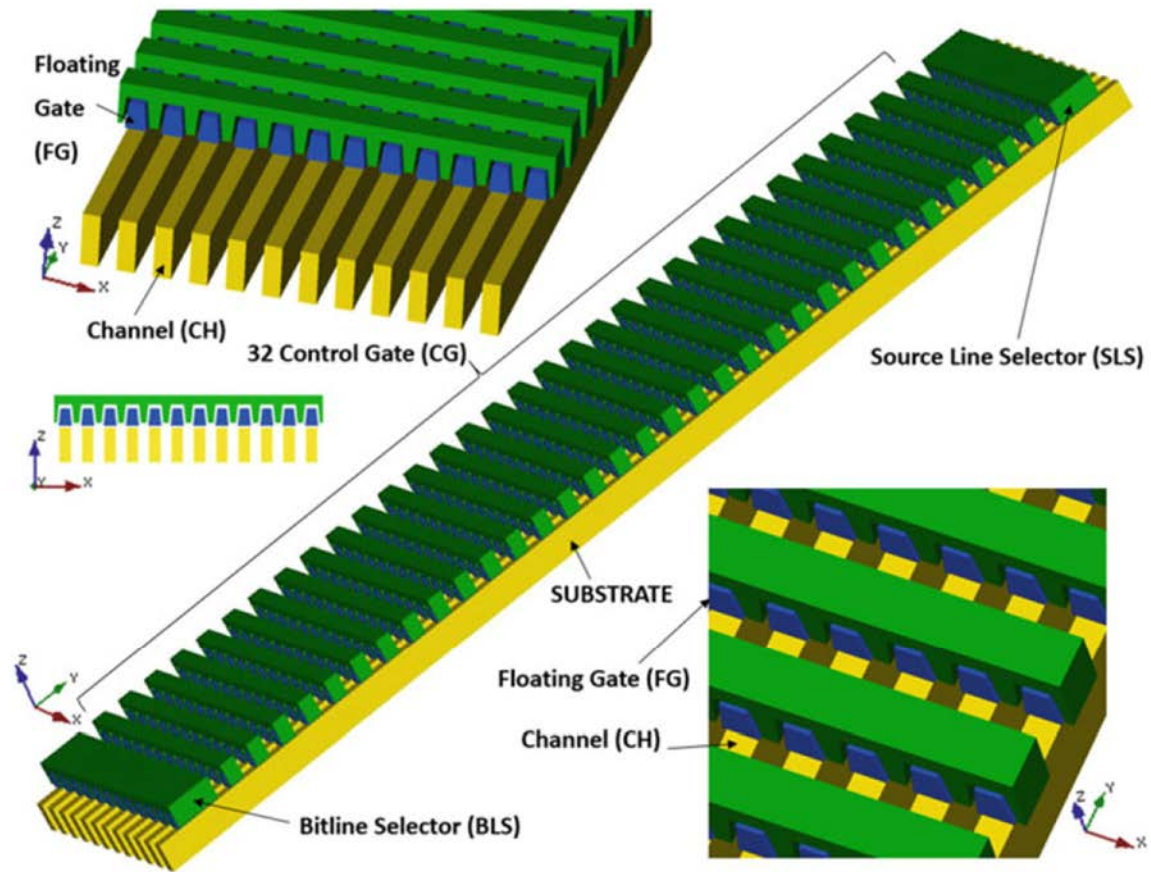


Fig. 3.9 Bird's-eye view of a planar NAND string

Ex. 1015, at 86.

Well before the priority date of the 378 Patent, Petitioner and others had developed techniques for manufacturing 3D NAND flash memory. Lee ¶ 46-55. In a 3D NAND flash memory, memory cells exist in vertical, cylindrical NAND flash “strings”:

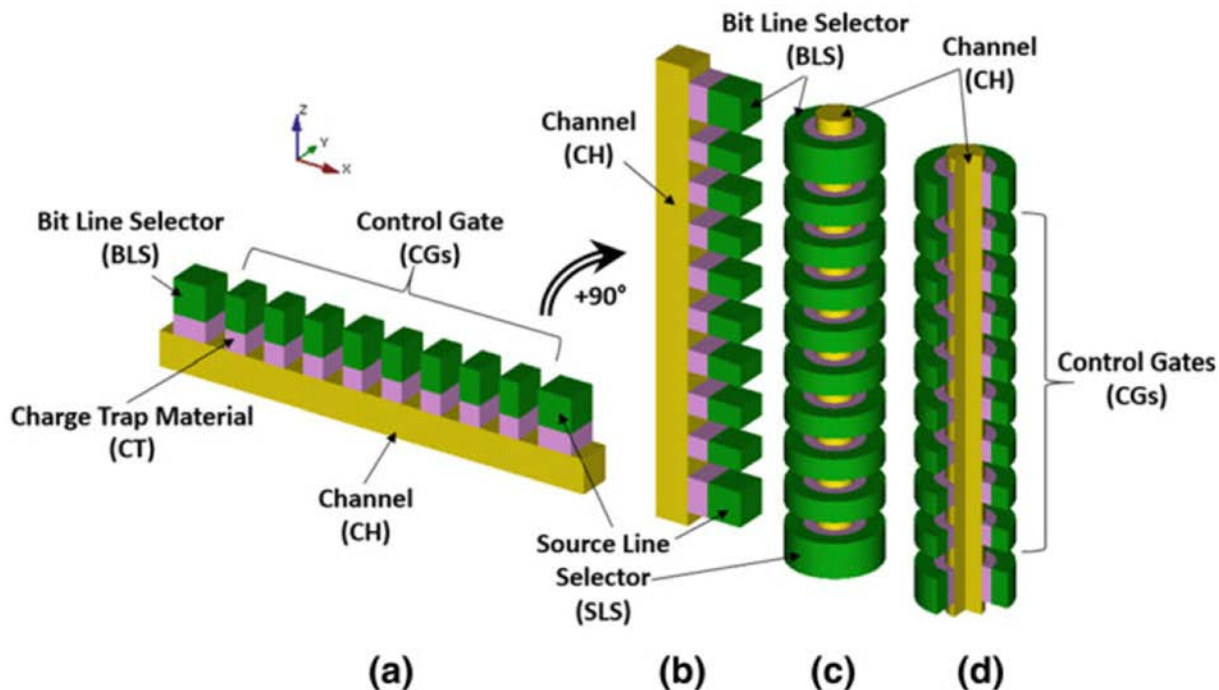


Fig. 4.1 NAND Flash string with horizontal gate and vertical channel: **a** planar, **b** planar rotated by 90°, **c** vertical channel with cylindrical shape and **d** its cross section

Ex. 1015, at 102; Lee ¶ 46. As labeled in Figure 4.1, above, each NAND string includes a “cylindrical channel.” EX1015, 58; Lee ¶ 46.

A number of architectures for constructing a memory device out of NAND strings were known in the art. For example, in the well-known BiCS (Bit Cost Scalable) architecture, various “contacts,” that is, electrical connections, are on top of the memory array. These include source line contacts (for providing a ground connection to the memory cells):

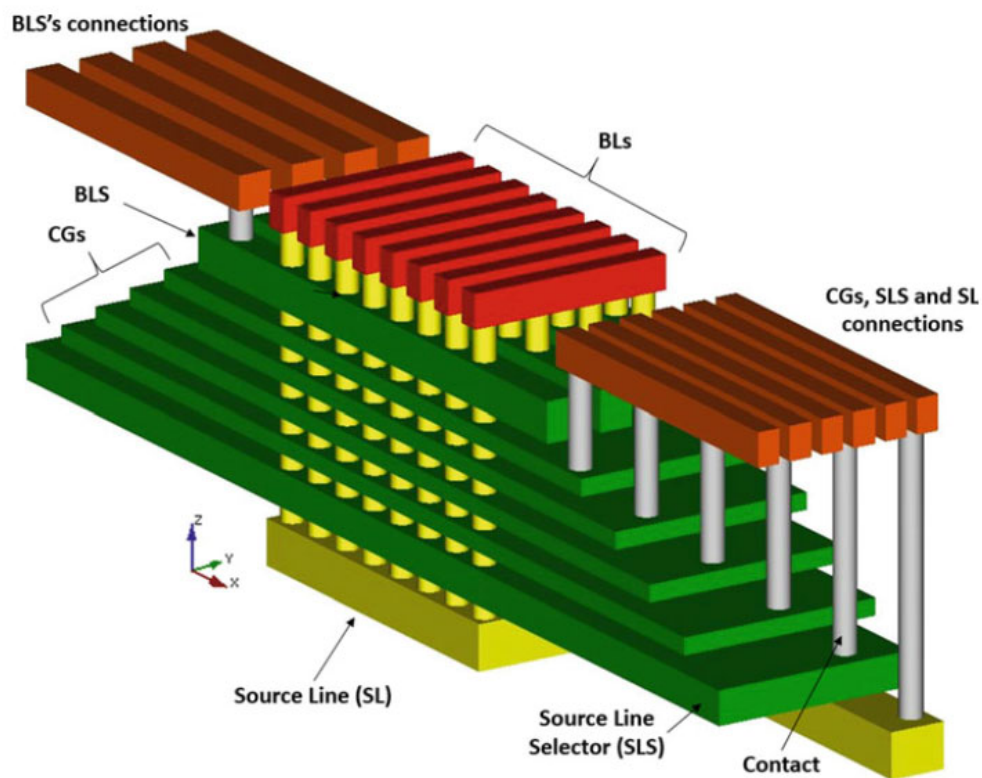


Fig. 4.13 Top bird's eye view of BiCS with gate connections

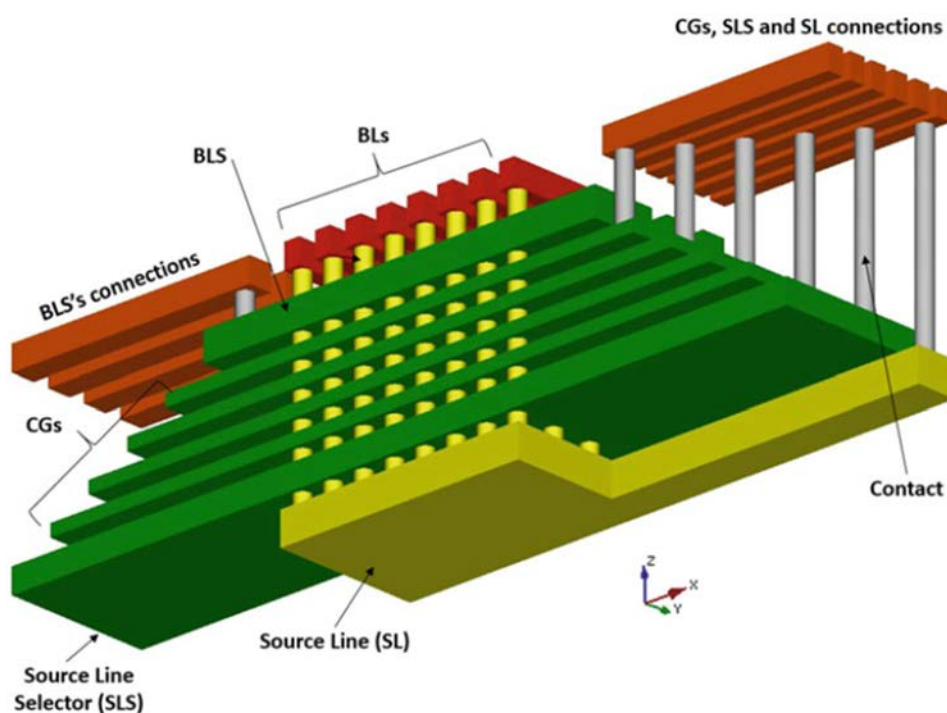


Fig. 4.14 Bottom bird's-eye view of BiCS with gate connections

Ex. 1015, 109-110; Lee ¶ 50. The memory cells' control gates form a staircase structure as shown below:

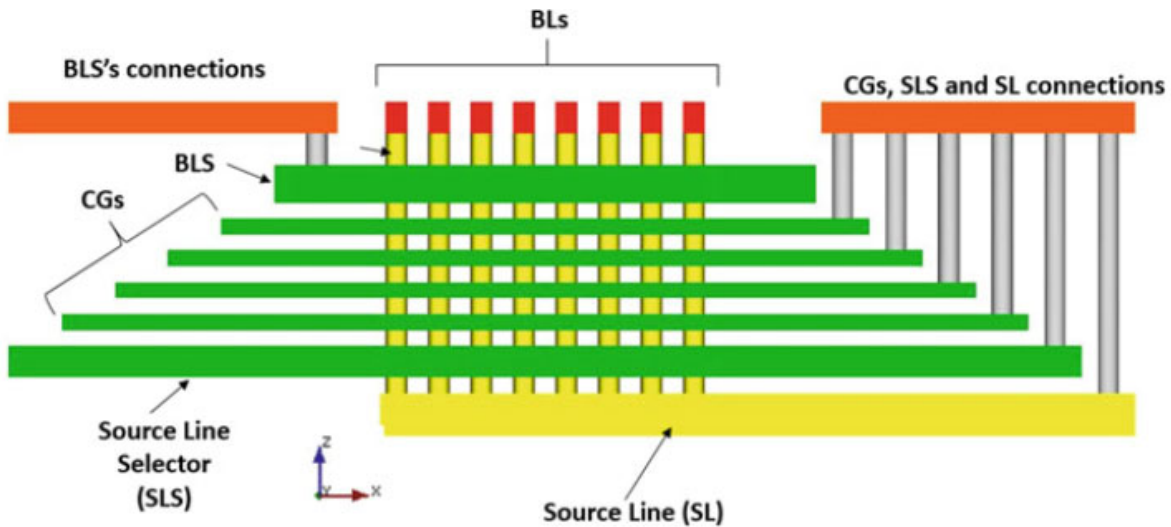


Fig. 4.12 Vertical cross section of BiCS with gate connections

Ex. 1015, 109 (green control gates forming a staircase). Each control gate delivers a control signal to a number of memory cells at the same horizontal level in the 3D NAND memory device. Lee ¶ 51. The memory cells that a single control gate controls are together a “word,” and the control gate is a “word line.” Ex. 1016, 41. Reflecting this, the grey columns contacting the top surface of the control gates (shown above in green) are “word line contacts.” Lee ¶ 52.

Various modifications to the BiCS structure were known, including the use of slit structures to serve as source line contacts for the NAND strings:

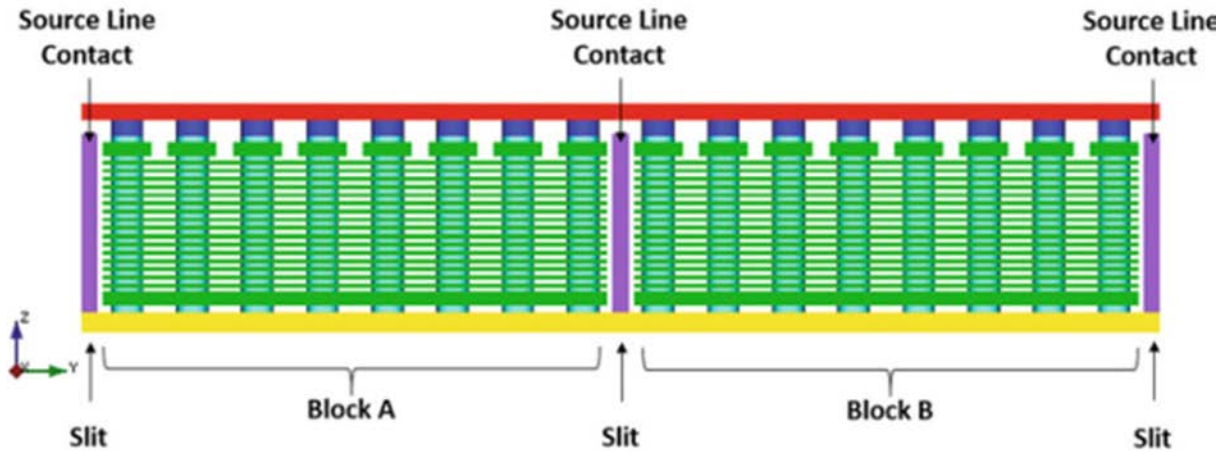


Fig. 6.8 Side view of Fig. 6.7

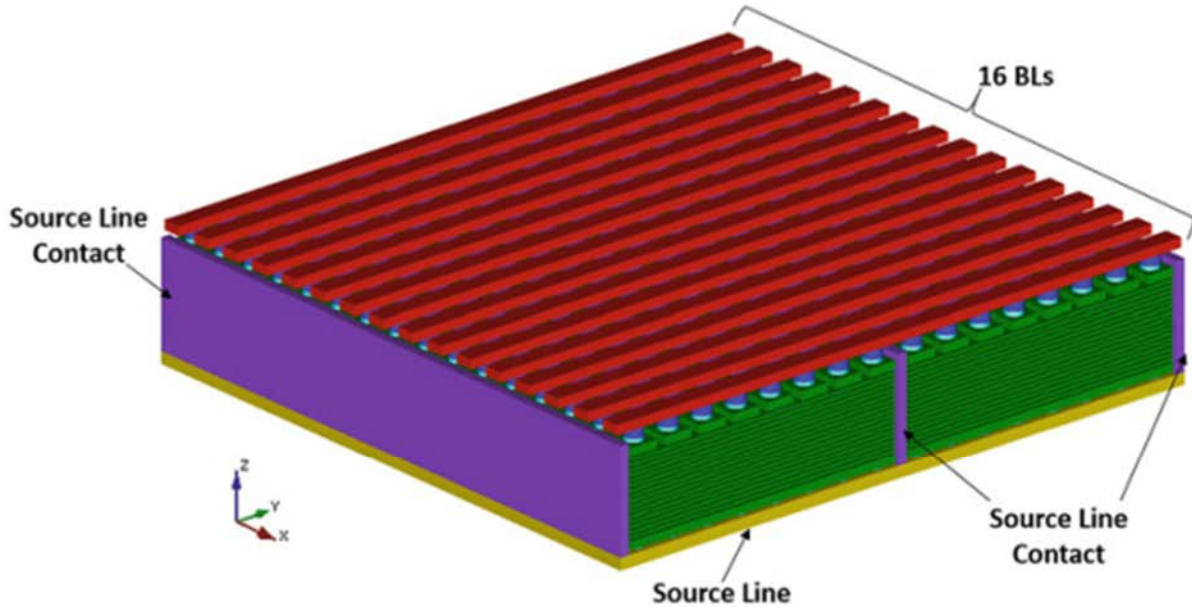


Fig. 6.7 Array slits

Ex. 1015, 185.

In each of the above figures, there are various gaps between the depicted structures. In a real 3D NAND memory device, these gaps are not merely empty space, but instead filled with an insulating material (also known as a “dielectric”).

Lee ¶ 54. One purpose of the dielectric is to prevent electrical signals from one

conductive structure from interfering with the electrical signals in other structures.

Id. Another purpose of the dielectric is as structural support to prevent the conductive structures from collapsing. *Id.*

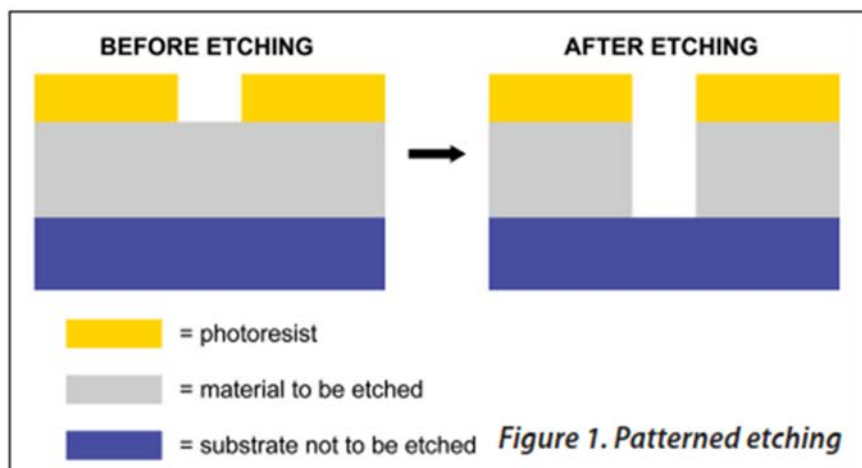
In sum, techniques for manufacturing 3D NAND memory devices were well-known in the art before the 378 Patent's priority date. Lee ¶ 57.

2. Epitaxy

As of the priority date, a POSITA would have well understood the semiconductor manufacturing process of "epitaxy," which involves depositing a crystalline layer of material onto a crystalline substrate in a way that the crystallographic orientation of the deposited material matches that of the substrate. Lee ¶¶ 58-62; Ex. 1023 (Chang, ULSI Technology), 132 (discussing epitaxy); Ex. 1024 (Chen, CMOS Devices & Technology), 65 (same). "The success of an epitaxial growth relies heavily on the chemistry used in the process," which may include "hydrogen and chlorosilanes, such as silicon tetrachloride (SiCl_4), trichlorosilane (SiHCl_3), and dichlorosilane (SiH_2Cl_2). In addition, silane (SiH_4) has also been used when a lower growth temperature is desired. The choice of each source gas is based on the growth conditions and layer requirements." Ex. 1023, 143. Lee ¶ 62.

3. Etching

“Etching” is a well-known semiconductor manufacturing technique for removing material. Lee ¶¶ 63-64; Ex. 1023, 356-357; Ex. 1025 (Jaeger, Introduction to Microelectronic Fabrication), 35-36. A POSITA would have known of chemicals used for etching (etchants) that are “selective,” that is, they will react with some materials preferentially to others. Lee ¶¶ 64-68; Ex. 1025, 35. For example, carbon tetrafluoride (when paired with greater than 40% H₂) can selectively etch silicon dioxide relative to silicon. Ex. 1023, 363-364 (using CF₄ with greater than 40% H₂ etches silicon oxide but not silicon). The following figure illustrates the etching process:



Ex. 1026 (HBr), 1.

A POSITA would have known of the common use of a material to which an etchant is **not** selective to serve as an “etch stop,” that is, to prevent the etch from removing material not intended to be removed. Lee ¶ 69; Ex. 1027 (Baker, CMOS

As reflected in the 378 Patent's title, the alleged point of novelty is a 3D memory device with "vertical interconnects between [a] stacked array device" (e.g., "3D memory device 200") and "a peripheral device," "thereby reducing metal levels and shrinking die size." Ex. 1001, 5:32-59. The 378 Patent refers to these vertical interconnects as "through array contacts" ("TACs"). *Id.*, 1:51-55.

"In some embodiments, TACs 234 can provide electrical connections between 3D memory device 200 and the peripheral device (e.g., on a CMOS chip; not shown in FIG. 2)." *Id.*, 11:3-9. "Each TAC 234 can extend through the entire thickness of dielectric structure 232 and extend through at least a portion of STI structure 233 in a substrate 202." *Id.*, 10:67-11:2.

The 378 Patent's 3D memory device includes an element between each "channel structure" (216) and the substrate (202) known as an "epitaxial plug." *Id.*, Figure 2. The "epitaxial plug" (element 222 in Figure 2) "can include, for example, a semiconductor material (e.g., single crystalline Si) that is epitaxially grown from the substrate 202." *Id.*, 9:37-39.

The 378 Patent's 3D memory device also includes an element between each "channel structure" (216) and "NAND string contact" (236) that it calls an "etch stop plug." *Id.*, Figure 2. The "etch stop plug" (element 224 in the figure above) "is an etch stop layer," made of a material such as polysilicon, "that prevents etching of dielectrics," "such as SiO₂ and SiN," "in channel structure 216." *Id.*, 9:44-46. "In

some embodiments, etch stop plug 224 acts as the drain of NAND string 204.” *Id.*, 9:47-48.

C. Prosecution History

During prosecution of the 378 Patent, the Examiner rejected the then-pending independent claims as obvious in view of Nishikawa and the 188 Publication. Ex. 1002, 530. However, the Examiner indicated that dependent claims 2 and 17 were allowable over these references. *Id.*, 536. The Examiner only allowed now-challenged claims 1-7 and 18 after Patent Owner rewrote the claims to include the limitations of original claims 2 and 17, respectively. *Id.*, 106, 110, 564, 567.

The references on which this Petition relies are not cumulative of those the Examiner discussed. During prosecution, the Examiner found Nishikawa did not disclose the claimed *through array contacts*, instead relying on the 188 Publication. But the 188 Publication does not even relate to memory, let alone a 3D NAND memory device. Ex. 1018, Abstract. Instead, the 188 Publication describes an image sensor. *Id.* By contrast, the primary reference in this Petition (Toyama) discloses or renders obvious *all* claim elements, including the *through array contacts*.

VI. DESCRIPTION OF THE PRIOR ART

Toyama has a filing date of September 19, 2016, a publication date of June 22, 2017, and claims a priority date of December 22, 2015. Toyama is prior art to the 378 Patent under 35 U.S.C. §§ 102(a)(1) and 102(a)(2).

Toyama's title is "Through-Memory-Level Via Structures For A Three-Dimensional Memory Device." Toyama discloses the conventional features of a 3D memory device claimed by the 378 Patent, including an alternating conductor/dielectric layer stack, memory channel structures extending through the alternating stack, word line contacts disposed on the staircase structure, a slit structure, and local contacts. *E.g.*, Toyama, Figure 17A-F (showing these components). And, like the 378 Patent, Toyama discloses 3D NAND memory devices with the electrical connections ("through-memory-level via structures" in Toyama's parlance) that extend through the memory array to provide a connection to "peripheral" devices. *Id.*, [0164] (discussing "peripheral device region 700" located underneath the "memory-level assembly").

Relevant to the present Petition, Toyama discloses a layer between its substrate ("planar semiconductor material layer 10") and its "memory stack structures 55" that it calls "pedestal channel portions 11" or "epitaxial channel portions 11." Toyama, Figures 17A, 49, [0202], [0208]. As the latter name suggests, Toyama forms the "channel portions 11" using an epitaxial process of "selective semiconductor deposition." *Id.*, [0202].

Also relevant to the present Petition, Toyama discloses an element between each "memory stack structures 55" and "drain contact via structures 88" that Toyama calls a "drain regions 63." Toyama, Figures 17A, 49, [0209], [0241]. Toyama's

“drain regions 63” are made of a material such as polysilicon and prevent etching of dielectrics within “memory stack structure 55.” §IX.A.8 (limitation [1.G]). As its name suggests, “drain regions 63” serve as the drain of the “memory stack structures 55.” Toyama, [0209], [0241], [0251].

Toyama discloses four “exemplary structures,” each of which is an embodiment of Toyama’s invention. Each of Toyama’s exemplary structures incorporates the teachings of previously described exemplary structures. Toyama, [0261] (second exemplary structure), [0277] (third exemplary structure), [0310] (fourth exemplary structure). Toyama also discloses a number of “modifications” to its “exemplary structures,” which also incorporate the teachings of previously described embodiments. *Id.*, [0332] (second modification of fourth exemplary structure).

The Petition’s discussion of the Challenged Claims focuses on two of Toyama’s embodiments: (1) the “second modification of the fourth exemplary structure,” illustrated in Figures 44A-B to 49 (hereinafter, “Second Modification”); and (2) the “first exemplary structure,” illustrated in Figures 1A-B to 17A-F. As this Petition explains in further detail below, both of these embodiments independently disclose, or render obvious, all limitations of the Challenged Claims.

VII. CLAIM CONSTRUCTION

A. “a staircase structure in the alternating layer”

Claim 1’s limitation “*a staircase structure in the alternating layer*” has a typographical error; a POSITA would have understood the term to mean “a staircase structure in the alternating layer **stack**.” Lee ¶ 89.

In light of the claim language and specification, this understanding of the claim is the only reasonable one. Lee ¶ 90. The error is evident from the face of the claim, which lacks antecedent basis for *the alternating layer*. Instead, the claim recites *an alternating layer stack disposed on the semiconductor substrate*.

The specification confirms that Patent Owner intended to refer to the *alternating layer stack* recited earlier in the claim. Indeed, the specification never describes an “alternating layer” except in the context of an alternating layer stack. And the specification’s written description support for the limitation at issue is its disclosure that the “alternating conductor/dielectric **stack** ... can include a staircase structure.” Ex. 1001, 8:48-50;⁷ Lee ¶ 91.

The prosecution history, which did not focus on claim 1’s “staircase structure” limitation, does not suggest a different interpretation of the claims. Lee ¶ 92.

⁷ Emphasis in a quotation is added unless otherwise indicated.

Indeed, Patent Owner’s infringement contentions against Micron expressly interpret the claim to require “a staircase structure disposed in the alternating layer *stack*.” Ex. 1030.

For these reasons, the Board should construe *a staircase structure in the alternating layer* as “a staircase structure in the alternating layer *stack*.” *Pavo Sols. LLC v. Kingston Tech. Co.*, 35 F.4th 1367, 1373 (Fed. Cir. 2022) (correcting an error in a claim).

B. Other Terms

For purposes of this petition, Petitioner submits that all other terms of the 378 Patent’s claims do not require further construction and should receive their plain and ordinary meaning. Lee ¶ 93.

VIII. LEVEL OF SKILL IN THE ART

A POSITA in the field of the 378 Patent would have had a bachelor of science degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (e.g., researching, designing, or teaching) NAND flash memory devices, or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may replace some of the professional experience). Lee ¶¶ 37-39. This POSITA would also have been aware of and generally knowledgeable about semiconductor manufacturing and 3D NAND’s structure, its component parts, how it operates, and how it is controlled. *Id.*

IX. GROUND 1: TOYAMA IN VIEW OF THE KNOWLEDGE OF A POSITA

A. Claim 1:

1. [1.PRE] “A three-dimensional (3D) memory device, comprising”

To the extent the preamble is limiting, Toyama discloses *a three-dimensional (3D) memory device*. Indeed, the first sentence of Toyama’s detailed description states that “the present disclosure is directed to three-dimensional non-volatile memory devices, such as vertical NAND strings and other three-dimensional devices, and methods of making the same.” Toyama, [0156]; Lee ¶ 106.

2. [1.A] “a semiconductor substrate”

Toyama discloses, or at least renders obvious, *a semiconductor substrate*.

As an initial matter, the 378 Patent defines a “substrate” as “a material onto which subsequent material layers are added, or otherwise ‘disposed.’” Ex. 1001, 4:41-43. The 378 Patent further notes that “[a] substrate can be a layer, can include one or more layers therein, and/or can have one or more layer thereupon, thereabove, and/or therebelow.” *Id.*, 5:4-6. Reflecting this, the 378 Patent embraces embodiments in which “the array device and a peripheral device are formed on different substrates.” *Id.*, 5:40-45.

Toyama’s “planar semiconductor material layer 10” is *a semiconductor substrate*.

FIG. 17A

⁸ All annotations are added herein unless otherwise noted.

semiconductor material onto which subsequent material layers are added or otherwise disposed, it is *a semiconductor substrate*.

Although the citations above are for Toyama's "first exemplary structure," Toyama's fourth exemplary structure also includes a "planar semiconductor material layer 10," and thus teaches this limitation for the same reason. See, e.g., Toyama, Figure 49 (Second Modification); Lee ¶ 109.

3. [1.B] "an alternating layer stack disposed on the semiconductor substrate;"

Toyama's "alternating stack (132, 146, 232, 246)" (shown below) is *an alternating layer stack disposed on the semiconductor substrate*:

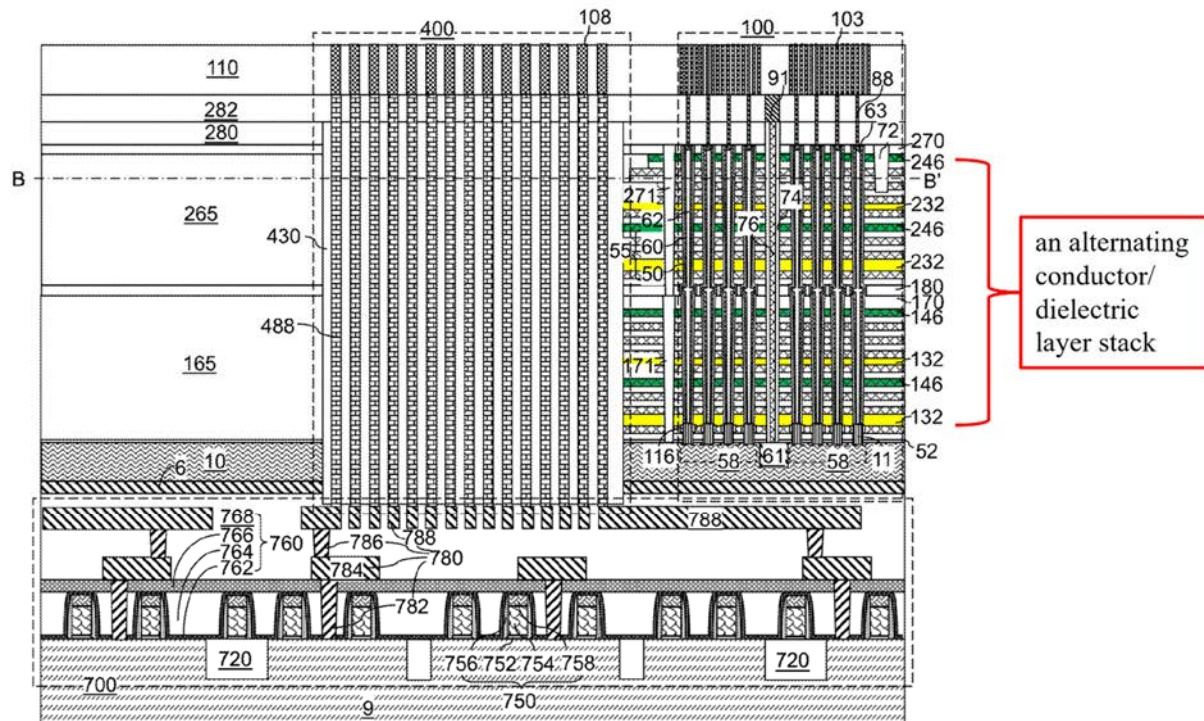


FIG. 17A

Toyama, Figure 17A; Lee ¶ 111. Toyama explains its “alternating stack” comprises “first and second conductive material layers (146, 246)” (representative layers of which Petitioner highlights in green above), “first insulating layers 132,” and “second insulating layers 232” (representative layers of which Petitioner highlights in yellow above). Toyama, [0172], [0190], [0228], [0232].

Toyama’s “alternating stack” is *disposed on the semiconductor substrate*. Lee ¶ 112. As an initial matter, the 378 Patent instructs that the term “on” “should be interpreted in the broadest manner such that ‘on’ not only means ‘directly on’ something but also includes the meaning of ‘on’ something with an intermediate feature or a layer therebetween.” Ex. 1001, 4:20-25. As noted for limitation [1.A],

above, Toyama's "planar semiconductor material layer 10" is a *semiconductor substrate*. Toyama, [0170]-[0171]. Figure 17A, above, shows that Toyama's alternating stack is *disposed on* "planar semiconductor material layer 10."

Although the citations above are for Toyama's "first exemplary structure," Toyama's Second Modification also teaches this limitation for the same reasons. *See, e.g.*, Toyama, Figure 49 (Second Modification), [0337] ("An alternating stack (132, 146, 232, 246) of insulating layers ([1]32, 232) and electrically conductive layers (146, 246) is thus formed."); Lee ¶ 113.

4. **[1.C] "[i] a dielectric structure [ii] on an isolation region of the substrate and [iii] extending vertically through the alternating layer stack, [iv] wherein the alternating layer stack abuts a sidewall surface of the dielectric structure and [v] the dielectric structure is formed of a dielectric material;"**

Toyama's Second Modification and Toyama's first exemplary structure teach this limitation.

a. Second Modification

i. [1.C.i] “a dielectric structure”

In Toyama’s Second Modification, shown below,⁹ “insulating liners 674” are *a dielectric structure*:

⁹ In a clear typographical error, Figure 49 labels its alternating conductor/dielectric layer stack as elements 132, 142, 232, 242. Elements 142, 242 are “sacrificial material layers” which, in a process step prior to Figure 49, were removed and replaced with “electrically conductive layers (146, 246).” Toyama, [0337], [0340]. That is also reflected in the figures, which depict how the sacrificial material layers (shaded in gray, as in Figure 45A) are replaced by electrically conductive layers (cross-hatched, as in Figure 46A).

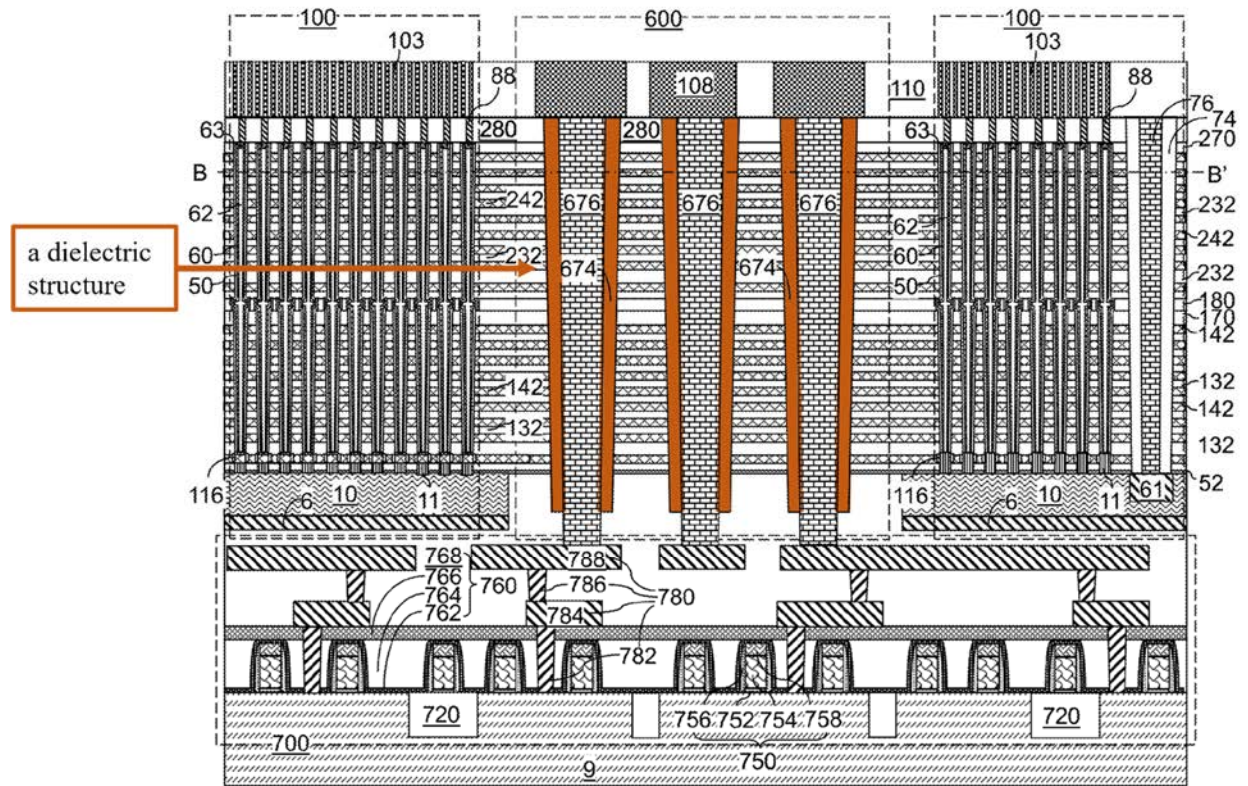


FIG. 49

Toyama, Figure 49; Lee ¶ 115.

As an initial matter, “insulating liners 674” are *dielectric*. Lee ¶¶ 116-117. Toyama forms “insulating liners 674” by depositing “a conformal insulating material layer” in “through-memory-level openings 679.”¹⁰ Toyama, [0338]-[0340]. Insulating liner 674 may be a “dielectric material.” *Id.*, [0233] (“[a]n insulating

¹⁰ Although paragraph 338 of Toyama refers to “through-memory-level openings 689,” that appears to be a typographical error. All of the relevant figures (*e.g.*, Figures 47A-B to 49) and the other textual description refer to the elements as “through-memory-level openings 679.”

spacer 74 including a dielectric material”), [0381] (“insulating liner 674 having a same material composition and a same thickness as the insulating spacer 74”). The claims do not require a “single-material” dielectric structure. Ex. 1001, 5:50-59 (contemplating a “single-material” dielectric structure only “[i]n some embodiments”). Regardless, Toyama contemplates that “insulating liners 674” are made of a single material (e.g., silicon oxide). §IX.E.1 (claim 5).

What’s more, the “insulating liners 674” are collectively a *structure*. Lee ¶ 118. As explained above, they are constructed together. Ex. 1022, 5 (Merriam-Webster’s definition of “structure” as “something (such as a building) that is constructed”). And all of the “liners 674” have the same function of insulating and electrically isolating the *through array contacts* (“through-memory-level via structures 676”) as they pass through the *alternating conductor/dielectric layer stack* (“alternating stack (132, 146, 232, 246).”¹¹

¹¹ If Patent Owner argues “insulating liners 674” are multiple structures and not collectively a single structure, that would be incorrect for the reasons above. And, in any event, it would be irrelevant. The Federal Circuit has “repeatedly emphasized that an indefinite article ‘a’ or ‘an’ in patent parlance carries the meaning of ‘one or more’ in open-ended claims containing the transitional phrase ‘comprising.’” *KCJ Corp. v. Kinetic Concepts, Inc.*, 223 F.3d 1351, 1356 (Fed. Cir. 2000).

Thus, “insulating liners 674” are individually and collectively *a dielectric structure*.

ii. [1.C.ii] “... on an isolation region of the substrate”

Toyama’s description of its Second Modification starts after the alternating stack has already been formed. *See* Toyama, Figure 44A. Toyama explains that the alternating stack can be formed as described for any of the prior structures. Toyama states, for example, “[t]he second modification of the fourth exemplary structure can be formed concurrently with the formation of any of the first, second, and third exemplary structures or modifications thereof.” *Id.*, [0332]. Toyama further states the “alternating stack of insulating layers (132, 232) and dielectric spacer layers (which can be the sacrificial material layers (142, 242)) can be formed over the semiconductor substrate 9 as in previously described embodiments.” *Id.*

A POSITA would have understood Toyama’s Second Modification to contemplate using the process described in the context of the third exemplary structure for creating “opening 151” and filling it with an insulating material. Toyama, [0277] (“The optional planar conductive material layer 6 and the planar semiconductor material layer 10 may be patterned to form an opening 151 extending through these layers to the underlying insulating layer 760. The opening 151 ... may be filled with another insulating material layer (e.g., a silicon oxide or doped silicate glass) 760.”); Lee ¶¶ 119-122. A POSITA would

therefore have understood that, in the context of Toyama's Second Modification, the insulating material layer that fills "opening 151" is *an isolation region*:

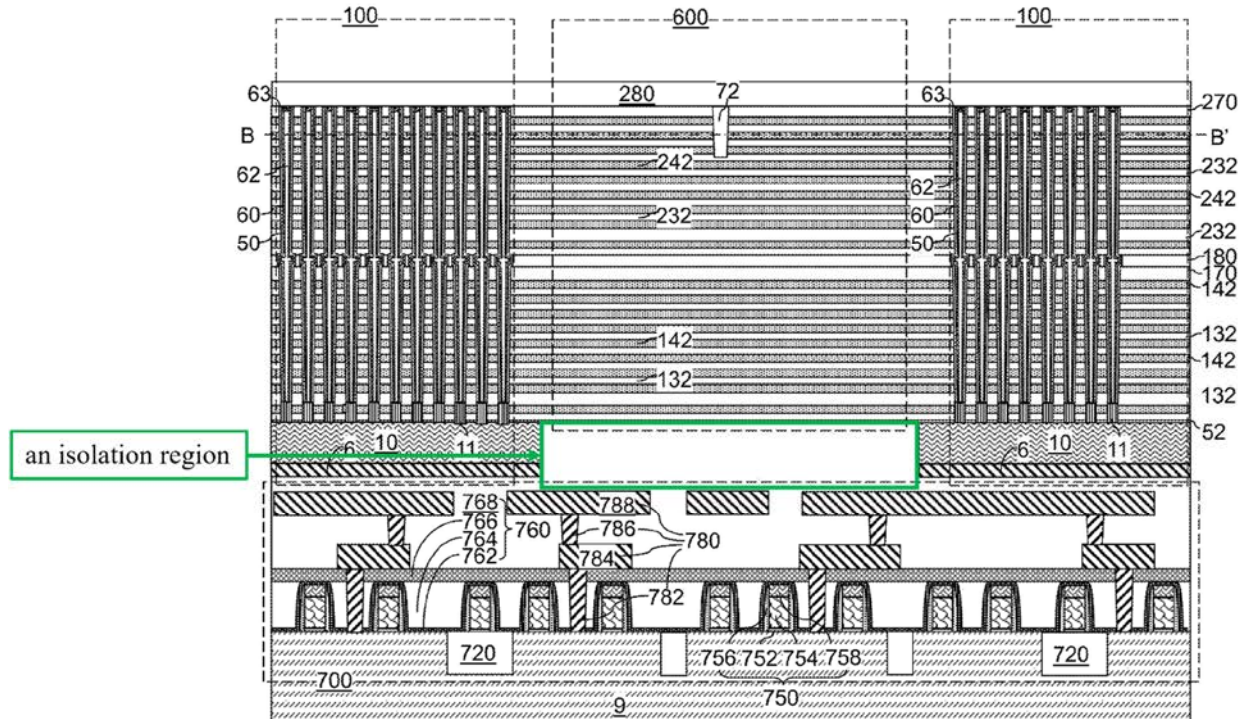


FIG. 44A

Toyama, Figure 44A; Lee ¶ 122. Thus, Toyama's Second Modification teaches *an isolation region* (the insulating material layer that fills "opening 151") *of the substrate* ("planar semiconductor material layer 10").

As illustrated in Figure 49, below, Toyama further teaches the *dielectric structure* ("insulating liners 674") is *on the isolation region* (the insulating material layer filling "opening 151"):

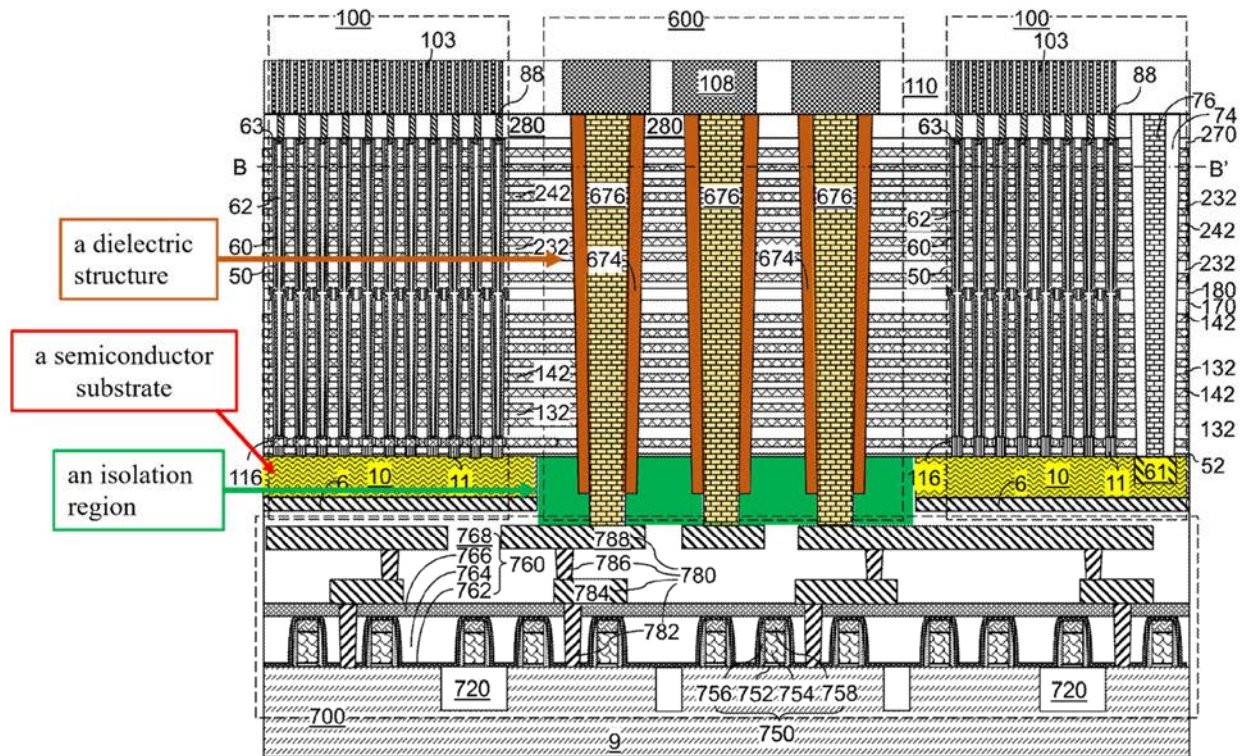


FIG. 49

Toyama, Figure 49; Lee ¶ 123; Ex. 1001, 4:20-29 (defining “on”).

iii. [1.C.iii] “a dielectric structure ... extending vertically through the alternating layer stack”

As noted above, Toyama’s “insulating liners 674” are individually and collectively *a dielectric structure*. §IX.A.4.a.i (limitation [1.C.i]). And, as noted above, Toyama’s “alternating stack (132, 146, 232, 246)” is *the alternating layer stack*. §IX.A.3 (limitation [1.B]). Thus, as Figure 49 shows below, Toyama discloses *a dielectric structure* (“insulating liners 674”) *extending vertically through the alternating layer stack* (“alternating stack 132, 146, 232, 246”):

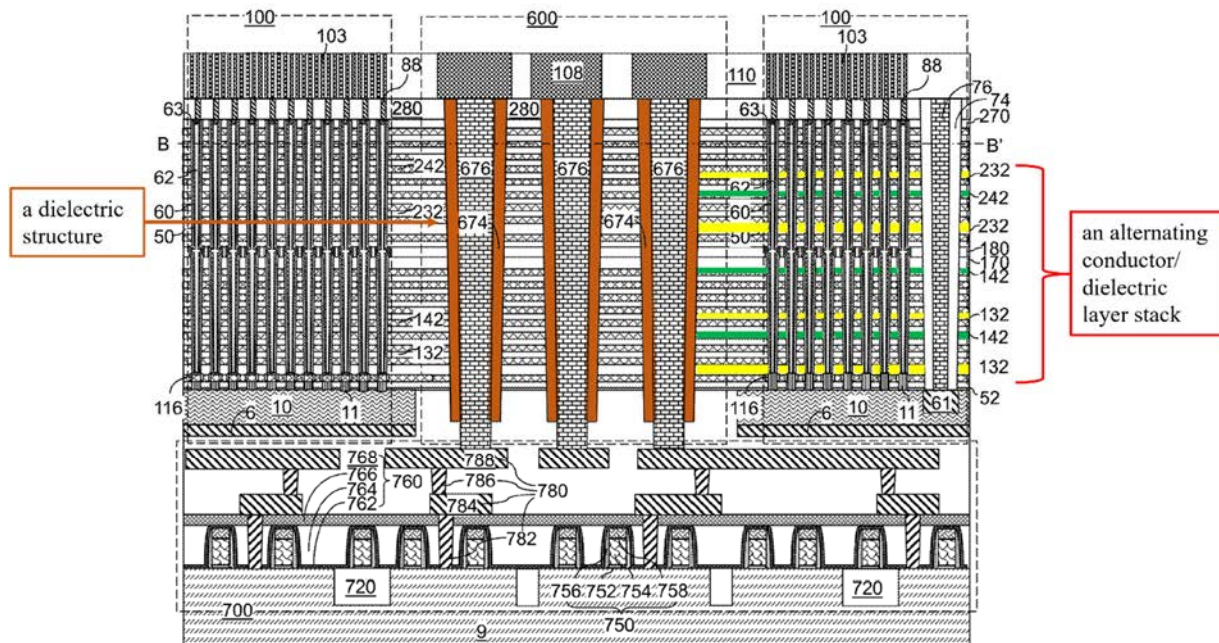


FIG. 49

Toyama, Figure 49;¹² Lee ¶ 124.

- iv. **[1.C.iv] “a dielectric structure ... wherein the alternating layer stack abuts a sidewall surface of the dielectric structure”**

As illustrated below, Toyama discloses *a dielectric structure* (“insulating liners 674”) *wherein the alternating layer stack* (“alternating stack (132, 146, 232, 246)”) *abuts a sidewall surface of the dielectric structure* (a sidewall surface of “insulating liner 674”):

¹² As noted in footnote 9, above, labels 142 and 242 are properly understood to refer to “conductive material layers (146, 246).”

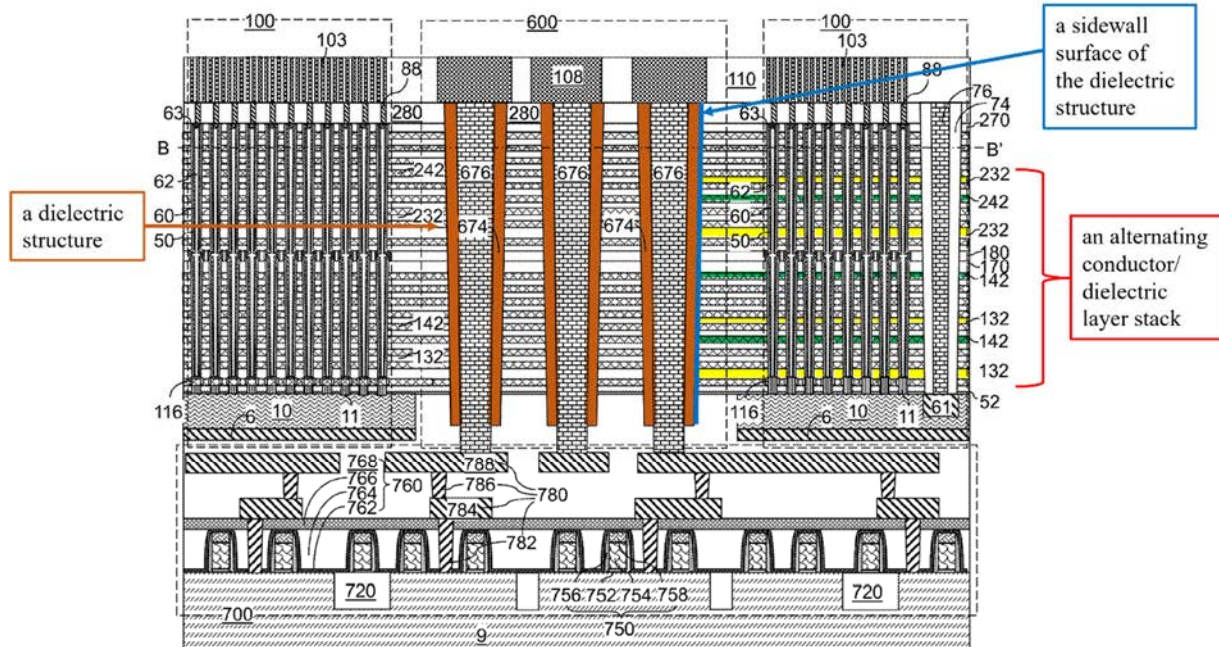


FIG. 49

Toyama, Figure 49;¹³ Lee ¶ 125.

v. [1.C.v] “... wherein ... the dielectric structure is formed of a dielectric material;”

As noted above, Toyama’s “insulating liners 674” are individually and collectively *a dielectric structure*. As noted above, each of these elements comprises a dielectric material. §IX.A.4.a.i (limitation [1.C.i]). Toyama thus discloses *a dielectric structure* (“insulating liners 674”) *wherein the dielectric structure is formed of a dielectric material*. Lee ¶ 126.

¹³ As noted in footnote 9, above, labels 142 and 242 are properly understood to refer to “conductive material layers (146, 246).”

b. First exemplary structure

i. [1.C.i] “a dielectric structure”

Figures 10A-12A show the formation of Toyama’s *dielectric structure* (upper part of “dielectric fill material portion 430”). Initially, “through-memory-level via region 400” comprises a staircase structure of dielectric layers 132, 142, 232, 242:

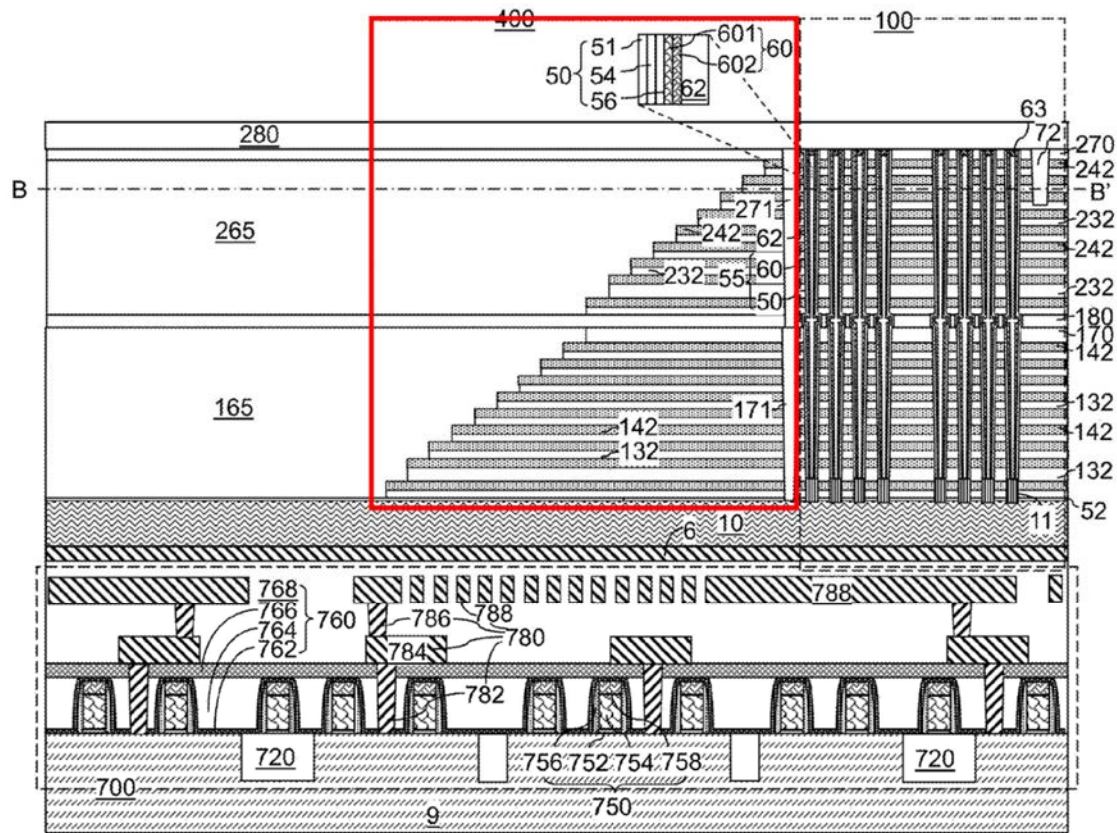


FIG. 10A

Toyama, Figure 10A, [0192]-[0194]. The next step removes these layers, resulting in “through-memory-level opening 769”:

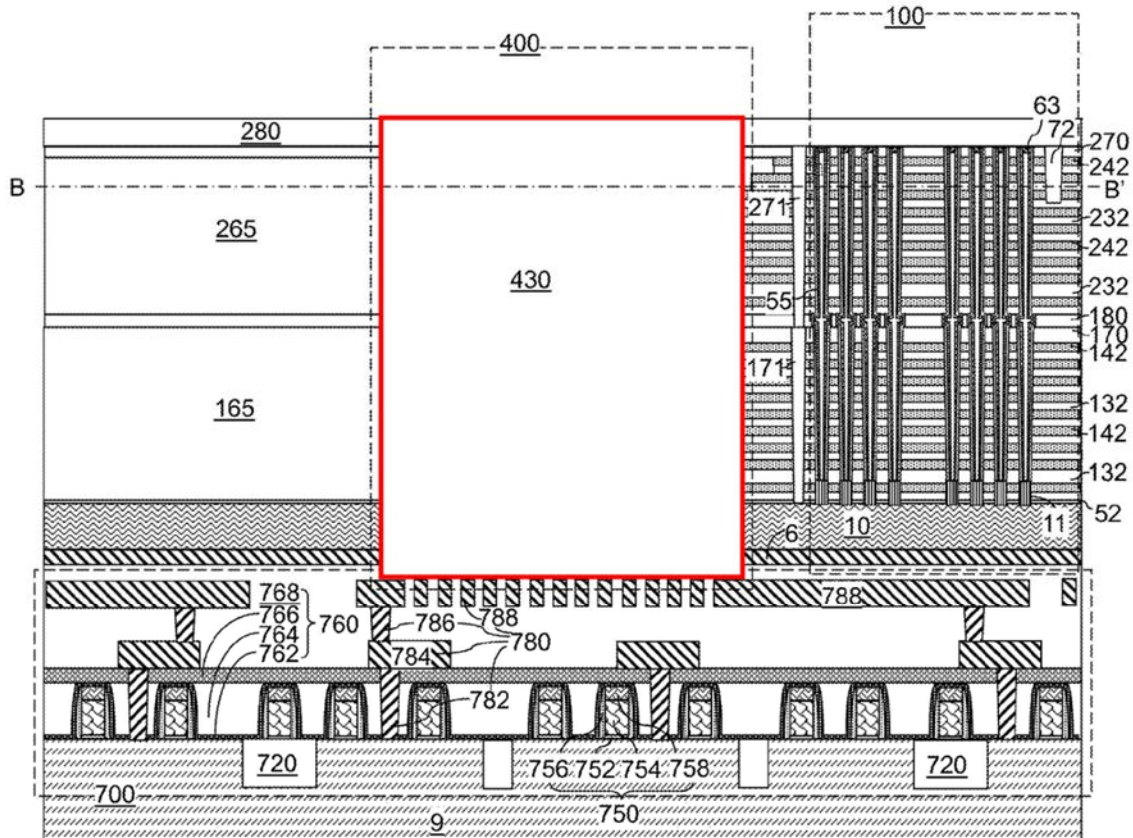


FIG. 12A

Id., Figure 12A; [0216].

In Toyama’s first exemplary structure, shown below, the upper part of “dielectric fill material portion 430” is *a dielectric structure* and, as will be explained below, the lower part of “dielectric fill material portion 430” is *an isolation region*:

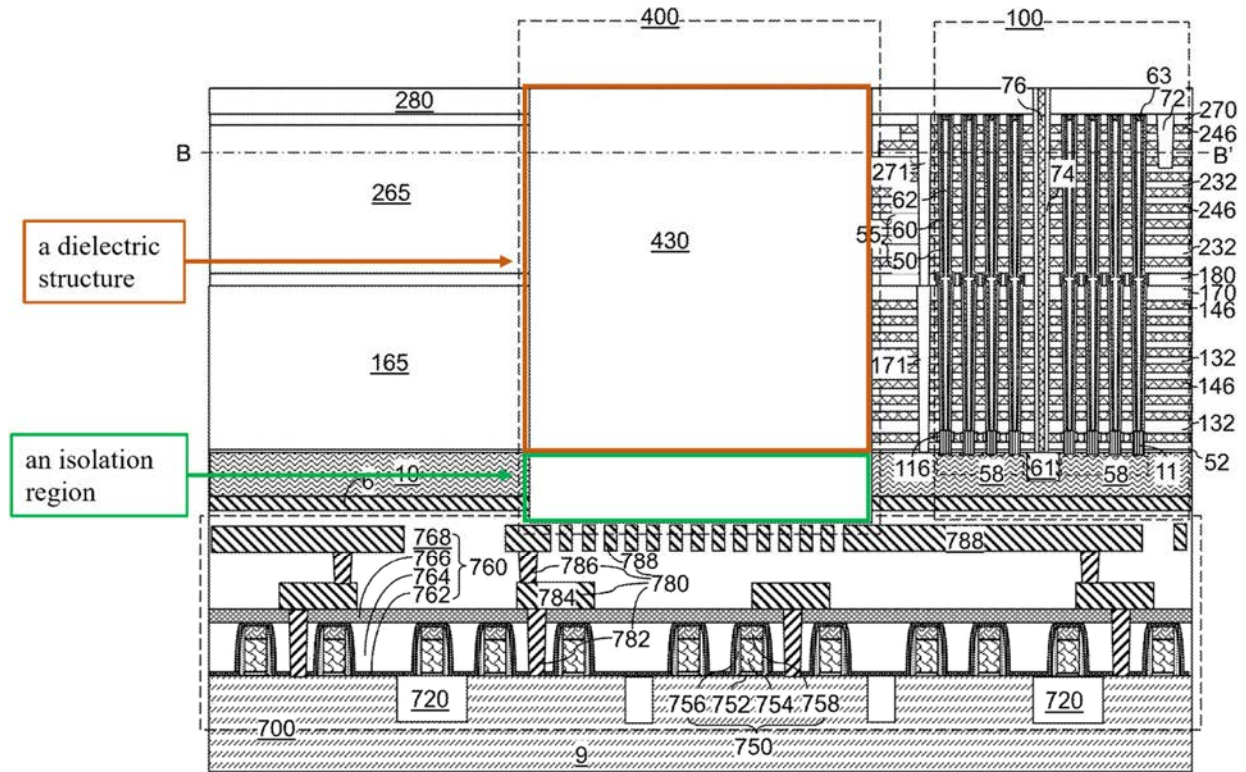


FIG. 15A

Toyama, Figure 15A; §IX.A.4.b.ii (limitation [1.C.ii]); Lee ¶ 127. Toyama explains that “a dielectric fill material portion 430 is formed within each through-memory-level opening 769, for example, by deposition of a dielectric fill material.” Toyama, [0216]. The upper part of “dielectric fill material portion 430” is *a dielectric structure* because it is composed of “a dielectric fill material.” *Id.* What’s more, as will be discussed below, Toyama’s *dielectric structure* (upper part of “dielectric fill material portion 430”) has the function of electrically isolating Toyama’s *through array contacts* (“through-memory-level via structures 488”) from the *alternating layer stack* (“alternating stack (132, 146, 232, 246)”). Lee ¶ 128.

ii. [1.C.ii] “... on an isolation region of the substrate”

In the context of Toyama’s first exemplary structure, the lower part of “dielectric fill material portion 430”—the portion level with and below the top of the “planar semiconductor material layer 10,” shown below—is *an isolation region*:

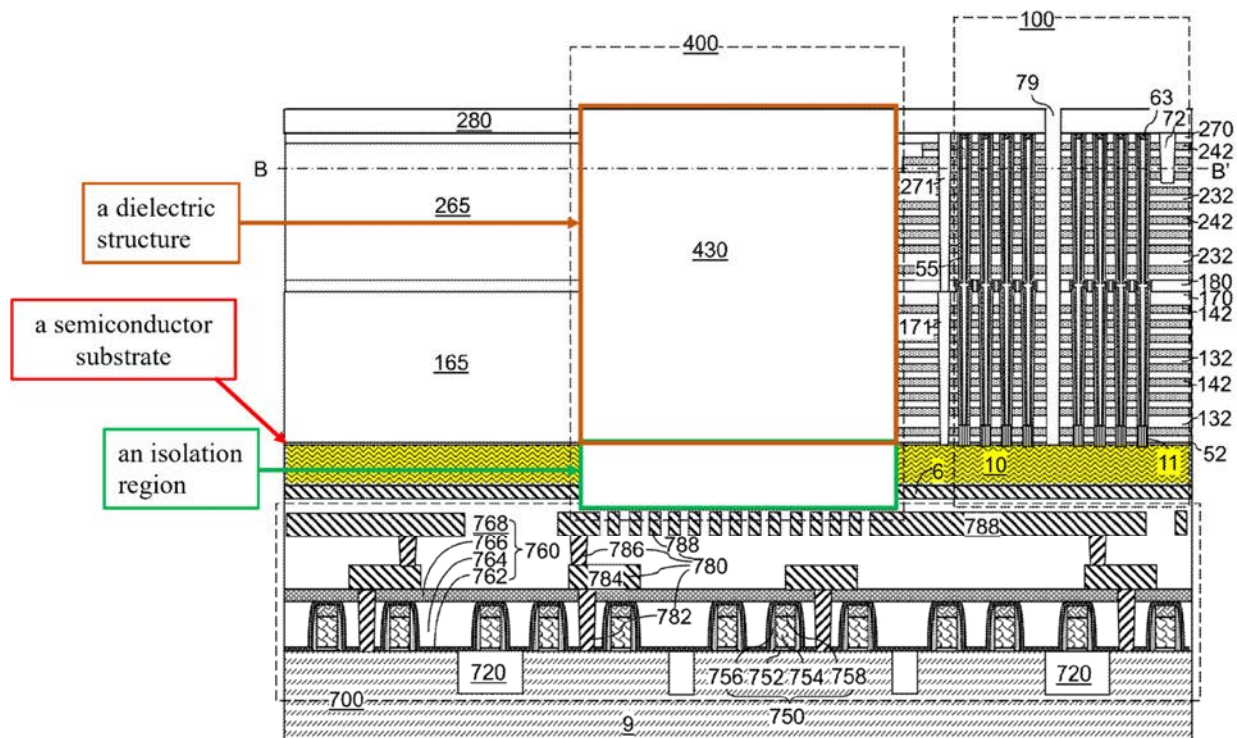


FIG. 13A

Toyama, Figure 13A; Lee ¶ 129. Toyama discloses that “dielectric fill material portion 430 includes a dielectric material such as undoped silicate glass (e.g., silicon oxide).” Toyama, [0216]. A POSITA would have understood that the lower part of “dielectric fill material portion 430” is *an isolation region* because it electrically isolates electrical conductors from each other and from electrical interference from the *substrate* (“planar semiconductor material layer 10”). Lee ¶ 130.

Toyama's *isolation region* (lower part of "dielectric fill material portion 430") is *of* its *substrate* ("planar semiconductor material layer 10"). Indeed, Toyama's *isolation region* (lower part of "dielectric fill material portion 430") **is formed by removing and is surrounded by** the *substrate* ("planar semiconductor material layer 10"). Toyama, Figures 10A-12B (forming "opening 769" in "layer 10," then filling the opening to form "portion 430"); Lee ¶ 131. What's more, Toyama's *isolation region* is within the substrate and isolates portions of the *substrate* from one another. *Id.*

Toyama's first exemplary structure thus discloses *an isolation region* (lower part of "dielectric fill material portion 430") *of the substrate* ("planar semiconductor material layer 10").

As the figure above shows, Toyama teaches that the first exemplary structure's *dielectric structure* (upper part of "dielectric fill material portion 430") is *on* the *isolation region* (lower part of "dielectric fill material portion 430").

If Patent Owner were to contend the claim excludes forming the *isolation region* and the *dielectric structure* during the same process step, that would be incorrect. Nothing in the language of the claim requires forming the structures in different steps or of different materials, nor is there a clear disavowal of such in the specification. On the contrary, the 378 Patent's disclosure expressly broadens "isolation structure" beyond the disclosed embodiment. Ex. 1001, 10:34-35 ("STI

structure 233 is exemplary and not limiting. As such, other isolation structures can be used.”). The purpose of the 378 Patent’s “dielectric structure” is to electrically insulate a “through array contact” as it extends through the “alternating conductor/dielectric layer stack.” *Id.*, 11:12-14; Lee ¶ 133-135. One purpose of the 378 Patent’s “isolation structure” is to electrically insulate a “through array contact” as it extends through the “substrate.” The upper and lower portions, respectively, of Toyama’s “dielectric fill material portion 430” equally serve these purposes. *Id.*

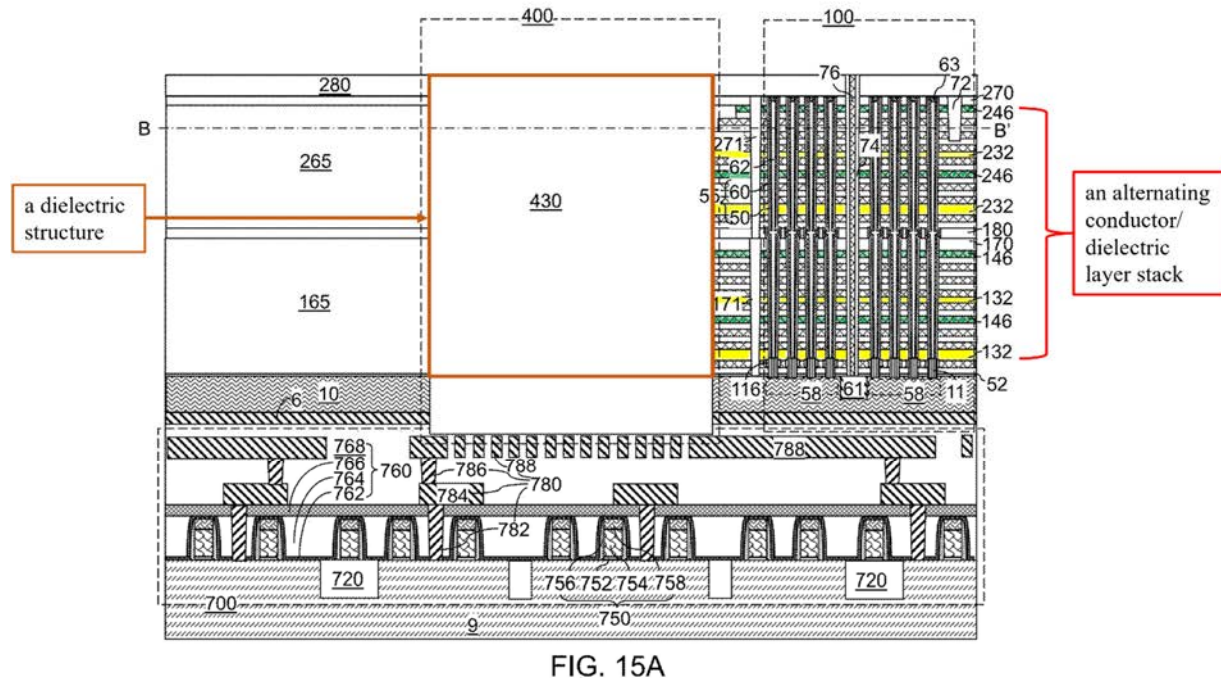
This case is analogous to *Retractable Technologies, Inc. v. Becton, Dickinson & Co.*, 653 F.3d 1296, 1303 (Fed. Cir. 2011), in which the Court held different parts of the same structure can meet distinct claim elements. As in *Retractable*, the intrinsic record here “lacks the clarity required to exclude from the scope of the claims [an isolation structure] and [a dielectric structure] that form distinct portions of a single structure.” *Id.* at 1304. And here, as in *Retractable*, each distinct part of the unitary structure (here, the upper and lower parts of “dielectric fill material portion 430”) fulfills the structural and functional requirements of the respective claim element (here, *dielectric structure* and *isolation region*, respectively).

Even if the claims require forming *the isolation region* separately from *the dielectric structure*, the first exemplary structure’s disclosure nevertheless renders the claims obvious. The use of isolation structures on a substrate to electrically isolate components was well known and commonplace by the priority date. Lee

¶ 135. What’s more, Toyama itself contemplates forming the *isolation region* and *dielectric structure* separately. Indeed, Toyama’s third exemplary structure teaches how to do so. Toyama, [0277], Figure 24A. In the context of Toyama’s first exemplary structure, forming the *isolation region* and the *dielectric structure* separately would be no more than the mere substitution of a known process (forming an isolation structure in “opening 151” before forming the dielectric structure, as in Toyama’s third exemplary structure) for another process (forming the isolation and dielectric structures at the same time, as in Toyama’s first exemplary structure) to obtain predictable results (the insulating material layer filling “opening 151” electrically isolates the conductors embedded within). Lee ¶ 135; *Agrizap, Inc. v. Woodstream Corp.*, 520 F.3d 1337, 1344 (Fed. Cir. 2008).

iii. [1.C.iii] “a dielectric structure ... extending vertically through the alternating layer stack”

As noted above, the upper part of Toyama’s “dielectric fill material portion 430” is *a dielectric structure*. And, as noted above, Toyama’s “alternating stack (132, 146, 232, 246)” is *the alternating layer stack*. §IX.A.3 (limitation [1.B]). Thus, as the figure below shows, Toyama discloses *a dielectric structure* (upper part of “dielectric fill material portion 430”) *extending vertically through the alternating conductor/dielectric layer stack* (“alternating stack 132, 146, 232, 246”):



Toyama, Figure 15A; Lee ¶ 136.

Indeed, Toyama's first exemplary structure discloses this limitation in materially the same way as one of the 378 Patent's embodiments. The 378 Patent discloses an embodiment in which the dielectric structure 124 borders three regions that include an alternating conductor/dielectric layer stack: above and below by staircase (i.e., word line) regions 140, and to the right-hand side by a NAND string region 110:

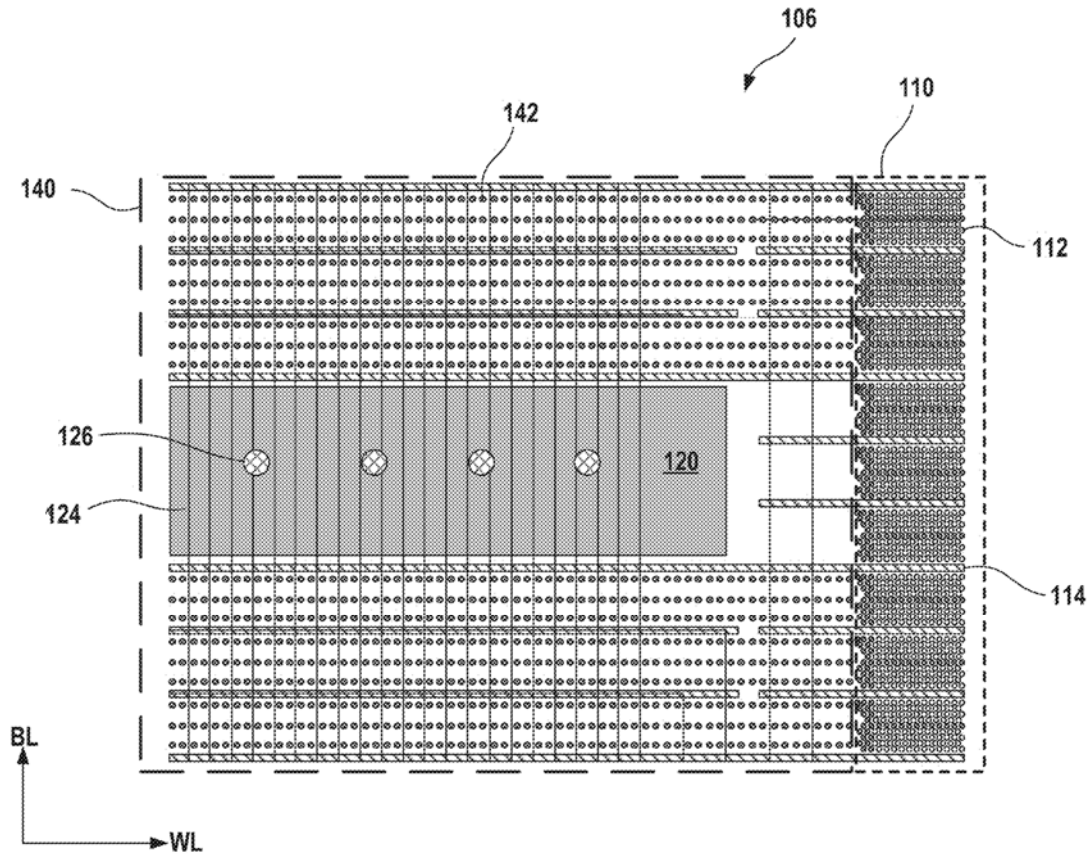


FIG. 1C

Ex. 1001, Figure 1C. Similarly, in Toyama’s first exemplary structure, the *dielectric structure* (“dielectric fill material portion 430”) borders three regions including an alternating conductor/dielectric layer stack: above and below by staircase regions (“word line contact via region 200”) and to the right-hand side by a NAND string region (“memory array region 100”):

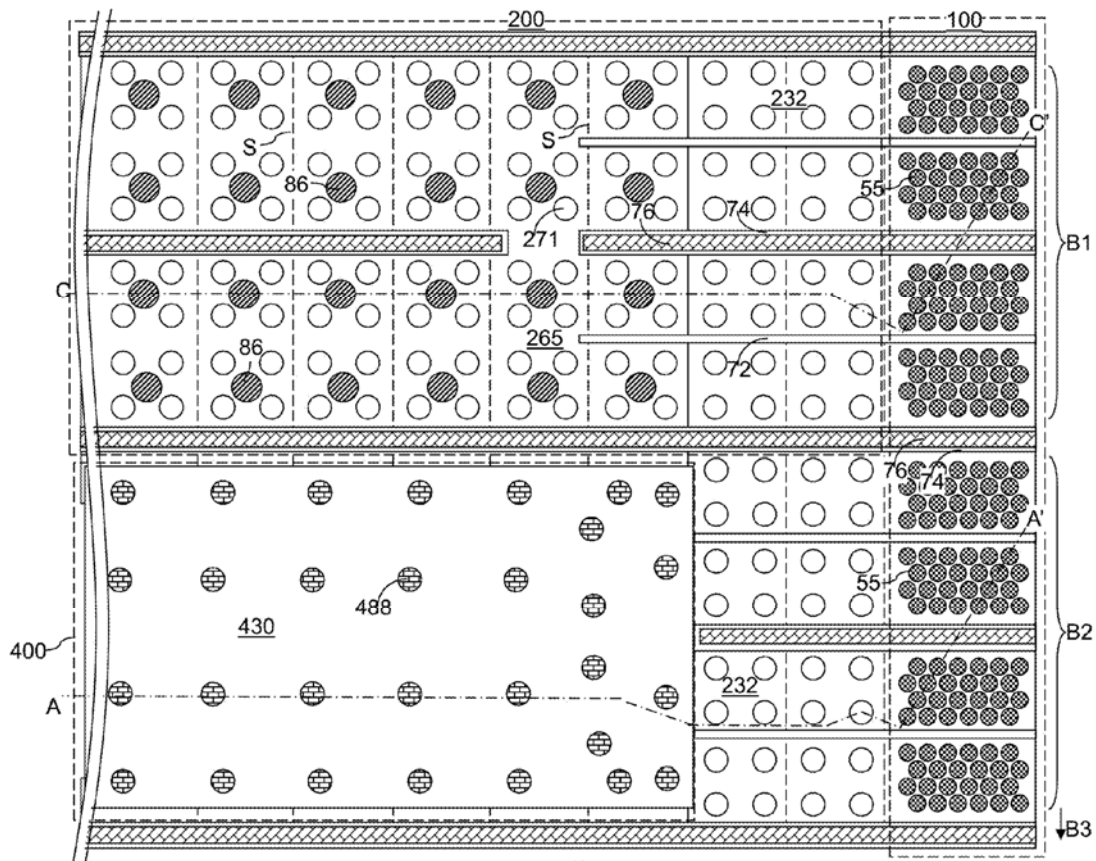


FIG. 16B

Toyama, Figure 16B; Lee ¶ 137.

What's more, Toyama and the 378 Patent form the *dielectric structure* ("dielectric fill material portion 430" and "dielectric layer 702," respectively) in the same way. Toyama forms "dielectric fill material portion 430" like the 378 Patent forms "dielectric layer 702," by removing part of the dielectric stack before replacing the dielectric stack's sacrificial layers with electrically conductive layers. Specifically, the 378 Patent removes part of "dielectric stack 400" to form "opening 600":

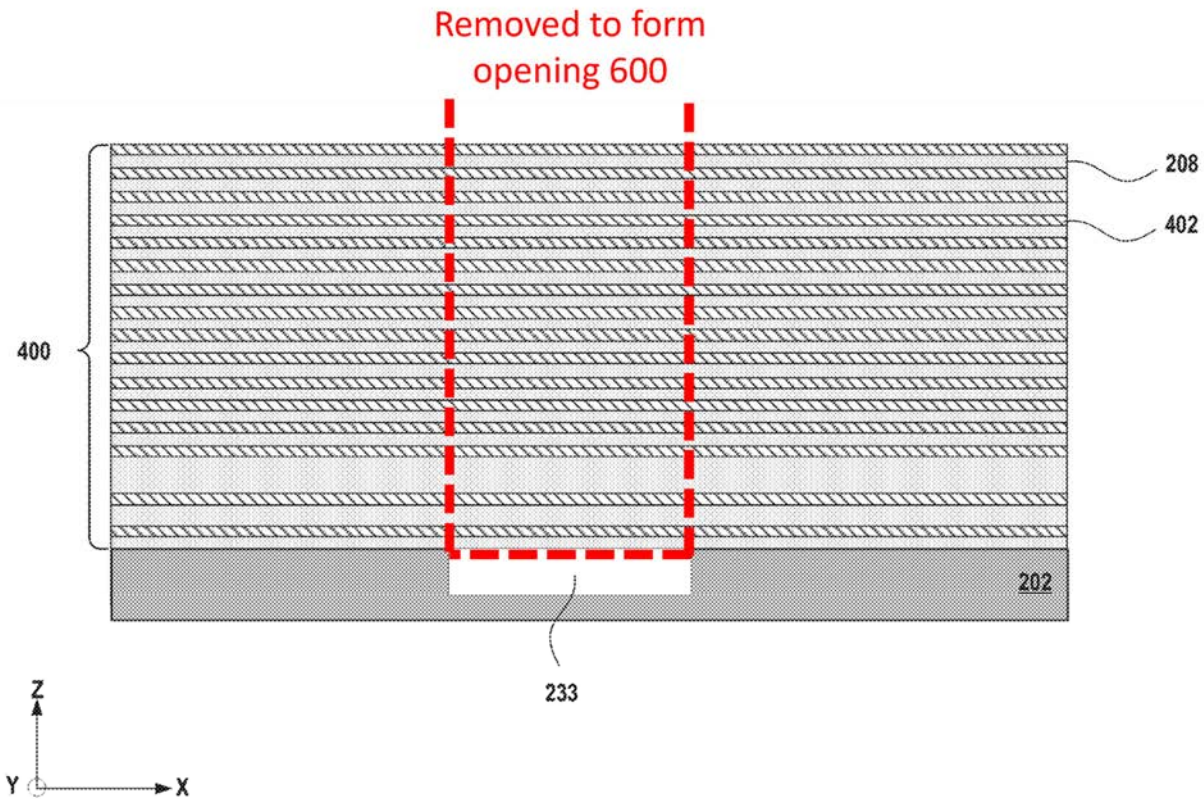


FIG. 4

Ex. 1001, Figure 4, 15:12-14. The 378 Patent then fills “opening 600” with the dielectric structure (“dielectric layer 702”). *Id.*, 15:42-44.

Similarly, Toyama’s first exemplary structure removes “insulating layers” 132, 232 and “sacrificial material layers” 142, 242 to form “opening 769”:

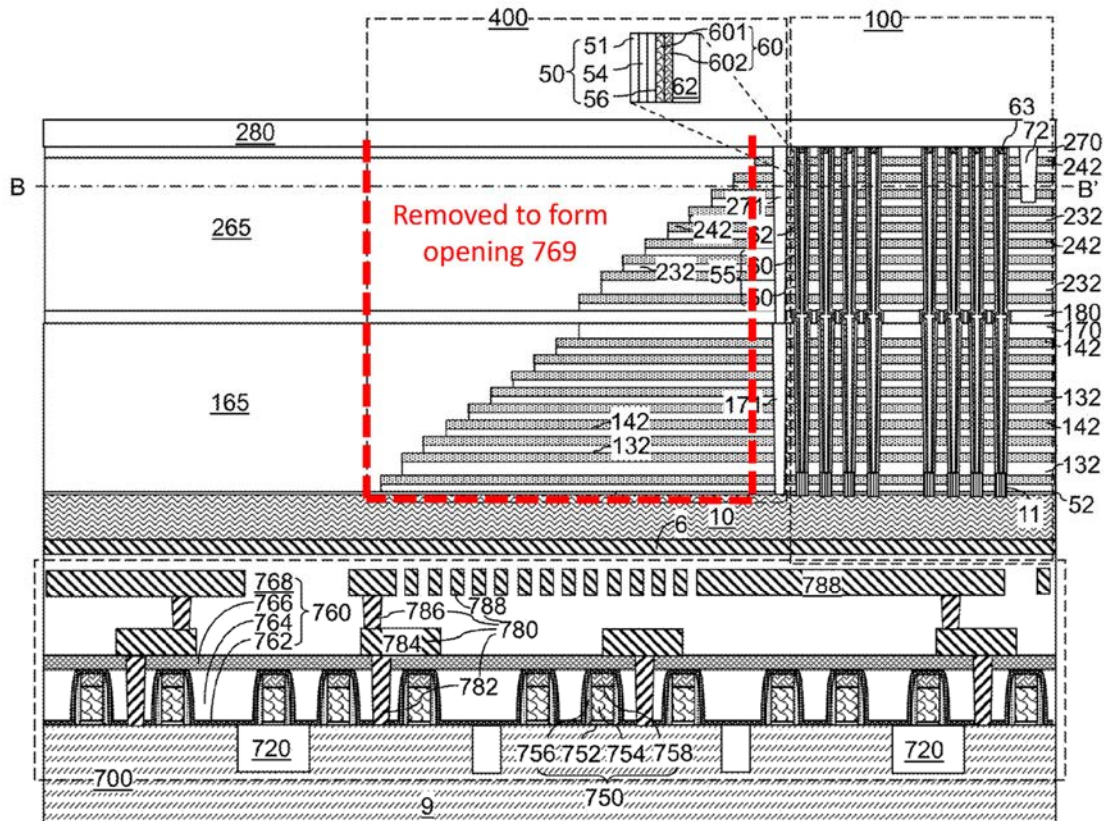


FIG. 10A

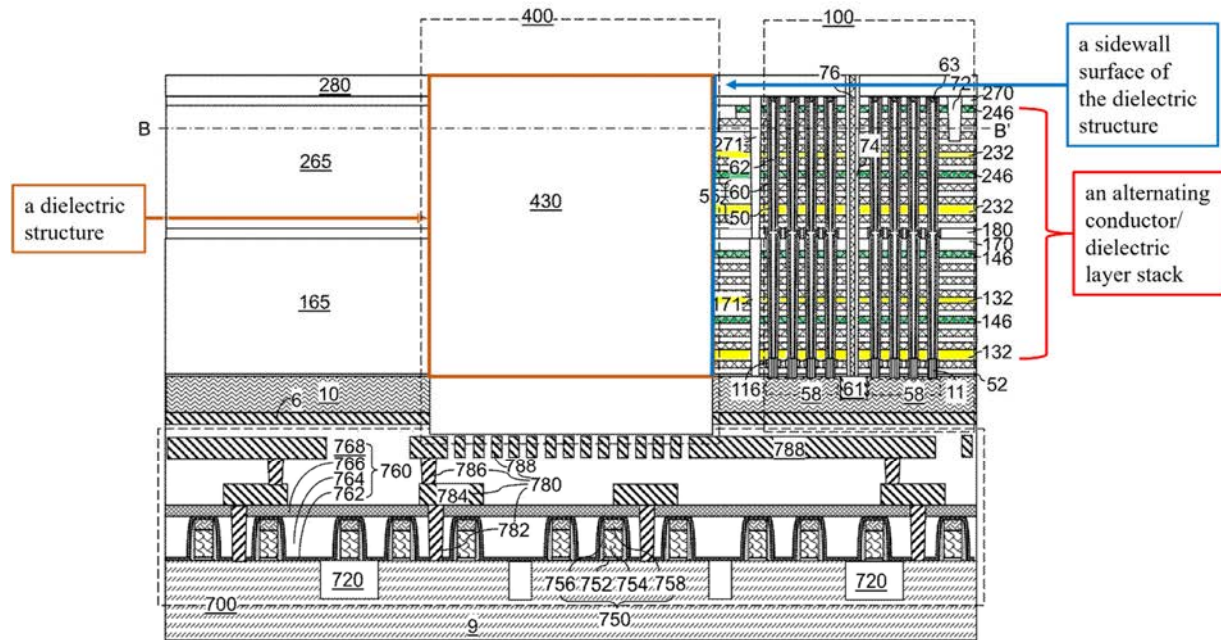
Toyama, Figure 10A, [0173], [0189]. Toyama then fills “opening 769” with the dielectric structure (“dielectric fill material portion 430”).

Toyama’s first exemplary structure thus discloses this limitation. Lee ¶¶ 136-140.

- iv. [1.C.iv] “a dielectric structure ... wherein the alternating layer stack abuts a sidewall surface of the dielectric structure”

As illustrated below, Toyama discloses *a dielectric structure* (upper part of “dielectric fill material portion 430”) *wherein the alternating layer stack*

(“alternating stack (132, 146, 232, 246)”) *abuts* (touches) *a sidewall surface of the dielectric structure* (sidewall of upper part of “dielectric fill material portion 430”):



Toyama, Figure 15A; Lee ¶ 141.

v. [1.C.v] “... wherein ... the dielectric structure is formed of a dielectric material;”

As noted above, the upper part of Toyama’s “dielectric fill material portion 430” is *a dielectric structure*. Toyama discloses “dielectric fill material portion 430 is formed ... for example, by deposition of a dielectric fill material.” Toyama, [0216]. Toyama thus discloses *a dielectric structure* (upper part of “dielectric fill material portion 430”) *wherein the dielectric structure is formed of a dielectric material* (the “dielectric fill material” that forms “dielectric fill material portion 430”). Lee ¶ 142.

5. [1.D] “one or more through array contacts (TACs) extending vertically through the dielectric structure and the isolation region;”

a. Second Modification

In Toyama’s Second Modification, “through-memory-level via structures 676” are *through array contacts*:

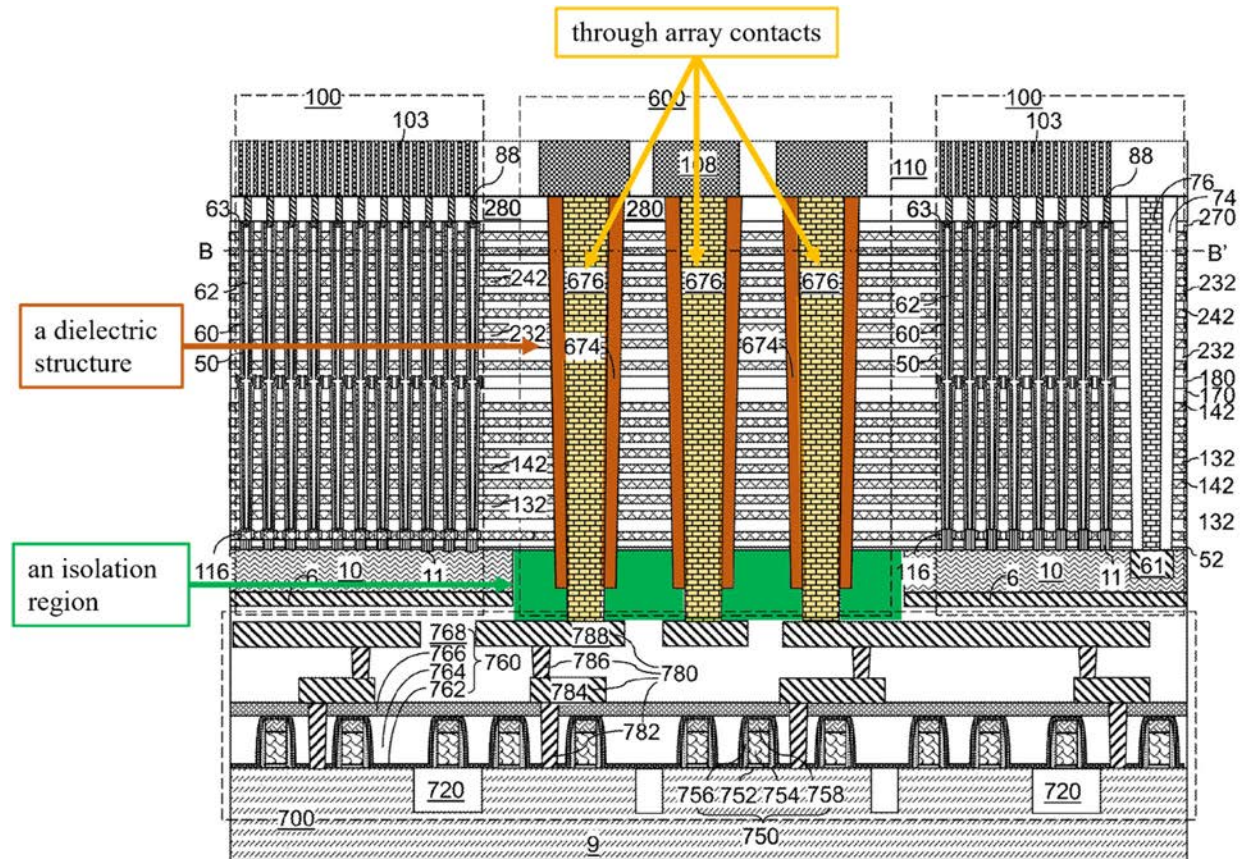


FIG. 49

Toyama, Figure 49; [0341]-[0342]; Lee ¶ 143.

As noted above, in the Second Modification, “insulating liners 674” are individually and collectively *the dielectric structure*, and the insulating material

layer filling “opening 151” is *the isolation region*. §§IX.A.4.a.i (limitation [1.C.i]), IX.A.4.a.ii (limitation [1.C.ii]).

Just as water travels *through* a hose or a pipe extends *through* a wall, Toyama’s “through-memory-level via structures 676” extend *through* “insulating liners 674,” and the insulating material layer filling “opening 151.” Thus, Toyama discloses *through array contacts* (“through-memory-level via structures 676”) *extending vertically through the dielectric structure* (“insulating liners 674”) *and the isolation region* (the insulating material layer filling “opening 151”). Toyama, [0340]-[0342]; Lee ¶¶ 144-145.¹⁴

¹⁴ As explained above, the claim term *a dielectric structure* is properly understood to include one **or more** dielectric structures. §IX.A.4.a.i (limitation [1.C.i]). Accordingly, the claim encompasses embodiments in which each *through array contact* extends vertically through a different *dielectric structure*. *ABS Glob., Inc. v. Cytonome/St, LLC*, 84 F.4th 1034, 1040 (Fed. Cir. 2023) (“The reference-back ‘the’ language takes its meaning from the meaning of the antecedent, so if ‘a sample stream’ has a plural-allowing meaning, so does the reference-back ‘the sample stream’ phrase.”).

Toyama's first exemplary structure thus discloses *through array contacts* ("through-memory-level via structures 488") *extending vertically through the dielectric* (upper part of "dielectric fill material portion 430") *and isolation region* (lower part of "dielectric fill material portion 430"). Toyama, [0239]; Lee ¶¶ 147-148.

6. [1.E] "one or more channel structures extending vertically through the alternating layer stack;"

Toyama teaches *one or more channel structures* ("memory stack structures 55") *extending vertically through the alternating layer stack* ("alternating stack (132, 146, 232, 246)"):

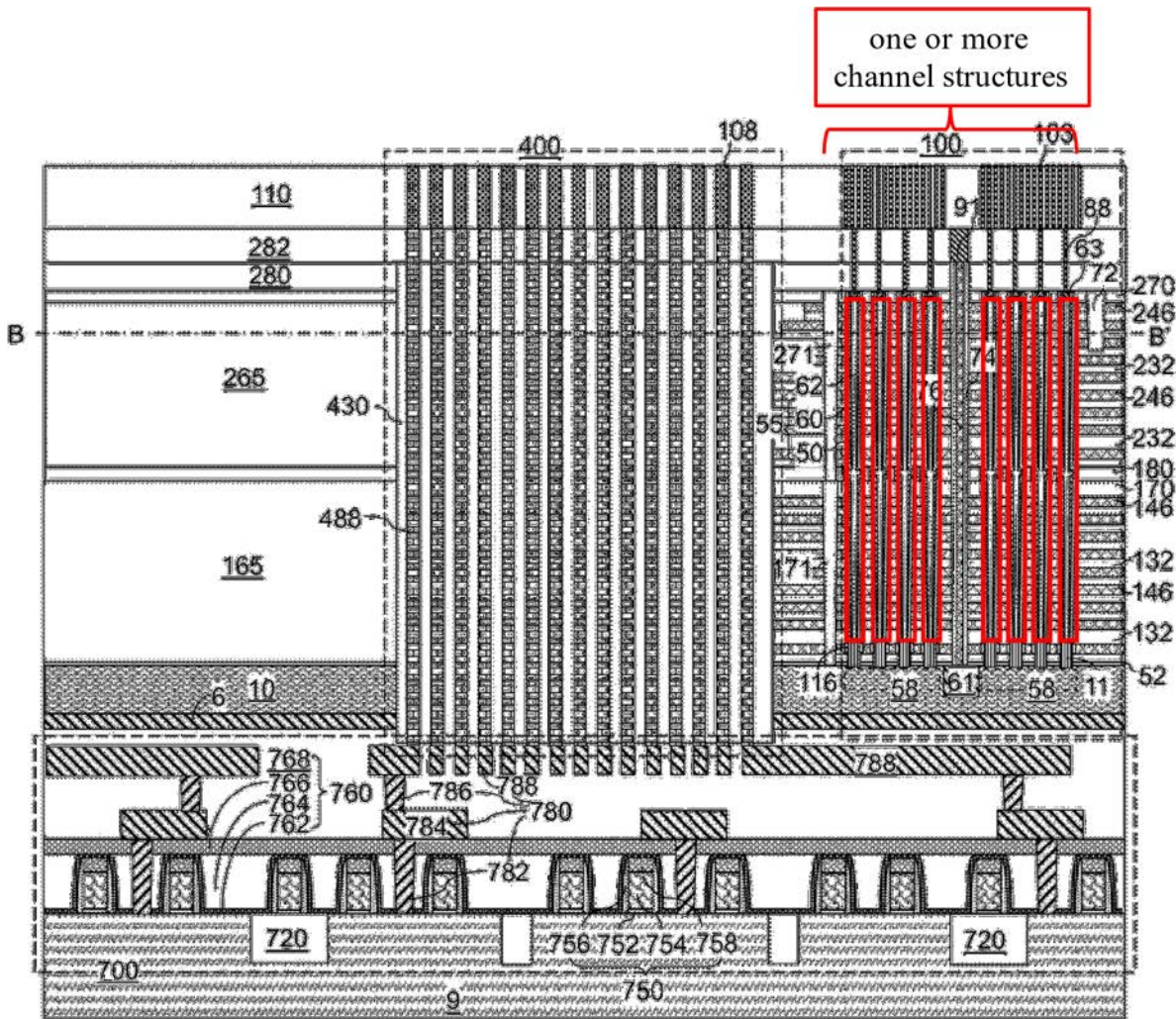


FIG. 17A

Toyama, Figure 17A (channel structures highlighted in red)¹⁵; Lee ¶ 149. Indeed, Toyama explains: “[t]he memory-level assembly includes ... memory stack

¹⁵ Here, as in Petitioner’s prior petition (IPR2024-00788) challenging other claims of the 378 Patent, Petitioner explains that Toyama’s “memory stack structures 55” are the claimed *channel structures*. Petitioner notes, however, that the red boxes

structures 55 vertically extending through the at least one alternating stack (132, 146, 232, 246).” Toyama, [0232].

Although the claim language does not impose any additional functional or structural requirements for the *channel structures*, Toyama’s “memory stack structures 55” perform the same function and are composed of the same components as the 378 Patent’s channel structures. Like the 378 Patent’s channel structures, Toyama’s “memory stack structures 55” serve as the device’s memory elements. Ex. 1001, 14:4-31 (“channel structure” includes a “memory film”); Toyama, [0388] (“The memory stack structures 55 can comprise memory elements of a vertical NAND device.”); Lee ¶ 150. The 378 Patent’s “channel structures” and Toyama’s memory stack structures 55” are also composed of the same components. Ex. 1001,

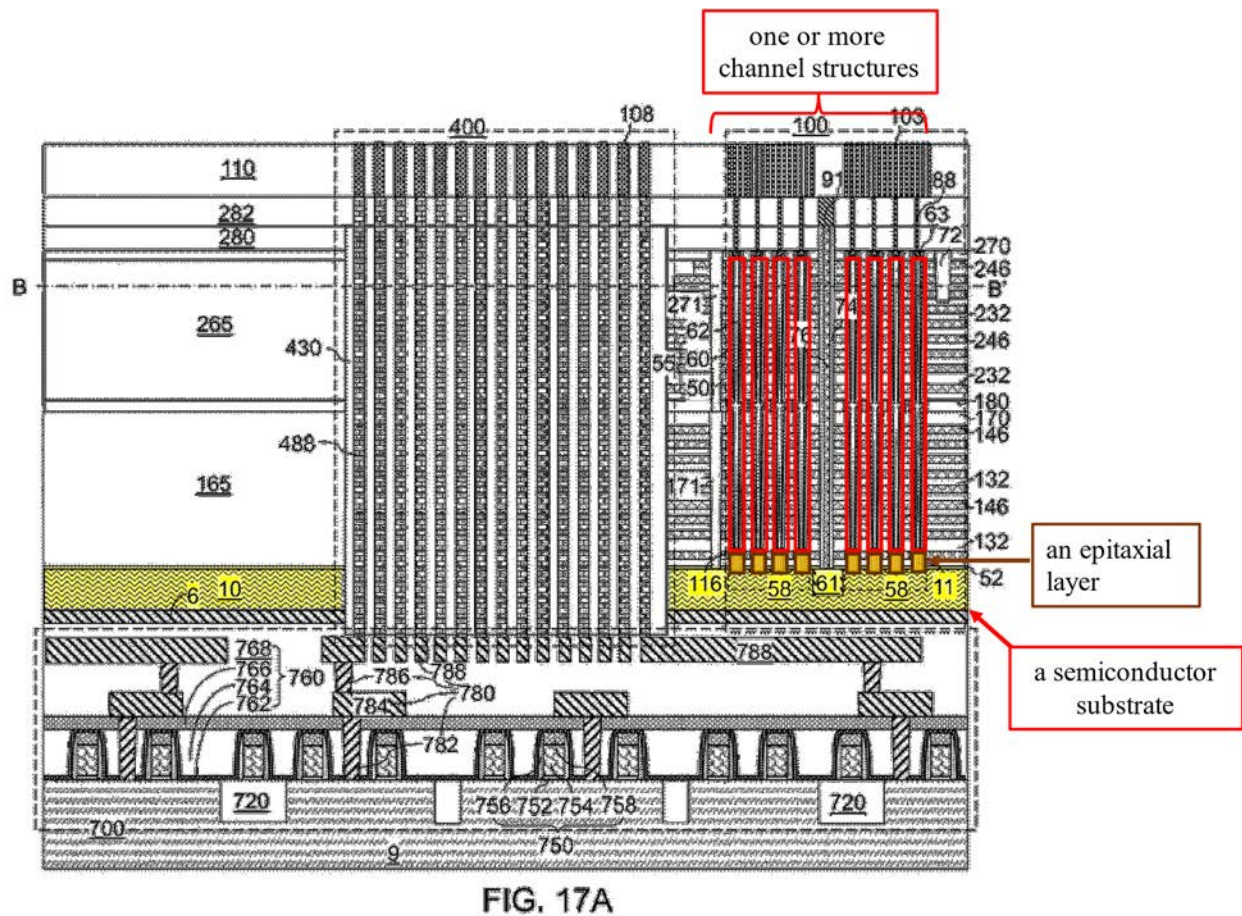
drawn around the *channel structures* in the earlier-filed Petition are larger than they are here, such that in the prior Petition each box encompassed not just a “memory stack structure 55,” but arguably other structures (e.g., “pedestal channel portion 11,” the *epitaxial layer*, and “drain region 63,” the *etch stop plug*). This overinclusive annotation was of no moment in the prior case because the challenged claims there did not recite *an epitaxial layer* or *an etch stop plug*. The boundaries of the box drawn here make clear that the *channel structures* include “memory stack structures 55” but not “pedestal channel portions 11” or “drain regions 63.”

9:1-6 (“[c]hannel structure 216 is filled with semiconductor materials (e.g., as a semiconductor channel 218) and dielectric materials (e.g., as a memory film 220)”); Toyama, [0210] (“[e]ach of the memory stack structures 55 comprises a memory film 50 and a vertical semiconductor channel 60”).

Although the citations above are for Toyama’s “first exemplary structure,” Toyama’s Second Modification also teaches this limitation for the same reason. *See, e.g.,* Toyama, Figure 49 (showing “memory stack structures 55”); Lee ¶ 151.

7. [1.F] “an epitaxial layer between the one or more channel structures and the semiconductor substrate;”

As the below figure shows, Toyama discloses *an epitaxial layer* (“pedestal channel portions 11”) *between the one or more channel structures* (“memory stack structures 55”) *and the semiconductor substrate* (“planar semiconductor material layer 10”):



Toyama, Figure 17A, [0208]; Lee ¶ 153.

Toyama also refers to “pedestal channel portions 11” as “epitaxial channel portions 11,” confirming that these structures constitute *an epitaxial layer*. And a POSITA would have recognized Toyama’s description of how “portions 11” are formed to be consistent with an epitaxial process. Toyama, [0202] (“The selective semiconductor deposition *grows a semiconductor material*. ... During a selective semiconductor deposition process, a reactant (such as silane, dichlorosilane, trichlorosilane, disilane, etc.) can be flowed into a deposition chamber

simultaneously with, or, alternatively with, an etchant (such as hydrogen chloride).”); §V.A.2; Lee ¶ 154.

At the very least, it would have been obvious to form “pedestal channel portions 11” (which a POSITA would have known to have the benefit of improving memory channel performance and reliability) as an epitaxial layer (epitaxy being a known and desirable method of forming crystalline material). Lee ¶ 155.

Although the citations above are for Toyama’s “first exemplary structure,” Toyama’s Second Modification also teaches or renders obvious this limitation for the same reason. See, e.g., Toyama, Figure 49 (showing “pedestal channel portions 11”); §V.A.2; Lee ¶ 156.

8. [1.G] “an etch stop plug on each of the one or more channel structures;”

Toyama teaches, or at least renders obvious, *an etch stop plug* (“drain region 63”) *on each of the one or more channel structures* (“memory stack structures 55”):

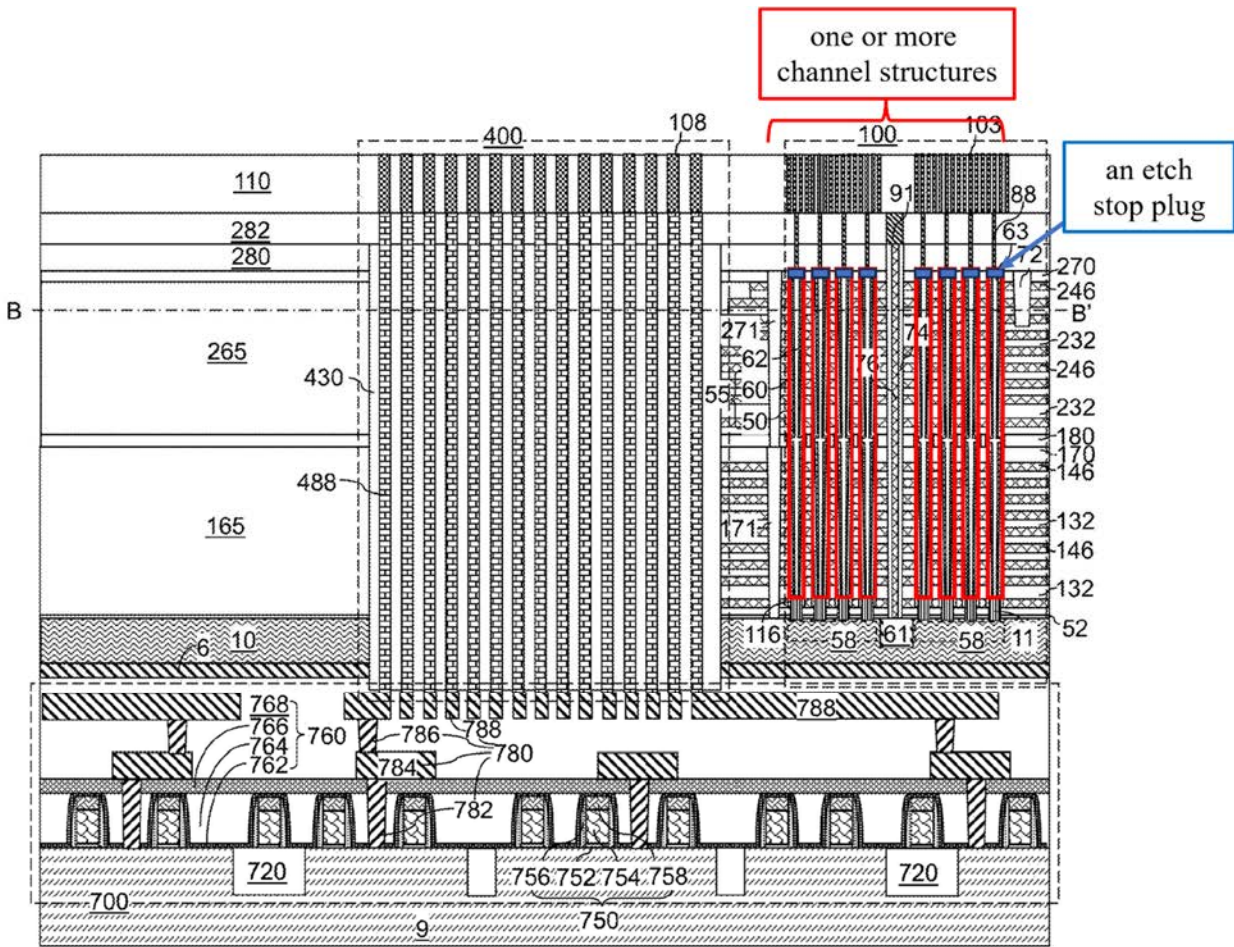


FIG. 17A

Toyama, Figure 17A; Ex. 1001, 4:20-25 (defining “on”); Lee ¶ 157.

Although Toyama does not expressly describe each of “drain regions 63” as being an “etch stop plug,” a POSITA would have understood, or at least found obvious, that “drain regions 63” are plugs that serve the purpose of stopping an etch. §V.A.3 (etching background); Lee ¶ 158.

Each of Toyama’s “drain regions 63” is a *plug*. Lee ¶ 159. As Toyama explains, “[a] doped semiconductor material ... can be deposited over the dielectric cores 62 and within the cavities in the memory openings to form drain regions 63.

The doped semiconductor material can be, for example, doped polysilicon. Excess portions of the deposited semiconductor material can be removed from above the top of the second insulating tier cap layer 270 ... to form the drain regions 63.” Toyama, [0209]. Because Toyama’s “drain regions 63” fill the cavities in the memory openings, they are plugs. Ex. 1022, 3 (Merriam-Webster’s definition of “plug” as “a piece used to fill a hole”).

As Figure 16A shows below, Toyama forms contacts (“drain contact via structures 88”) *on the one or more channel structures* (“memory stack structures 55”) by etching through dielectric layers 280 and 282, and then filling the etched opening with a conductor:

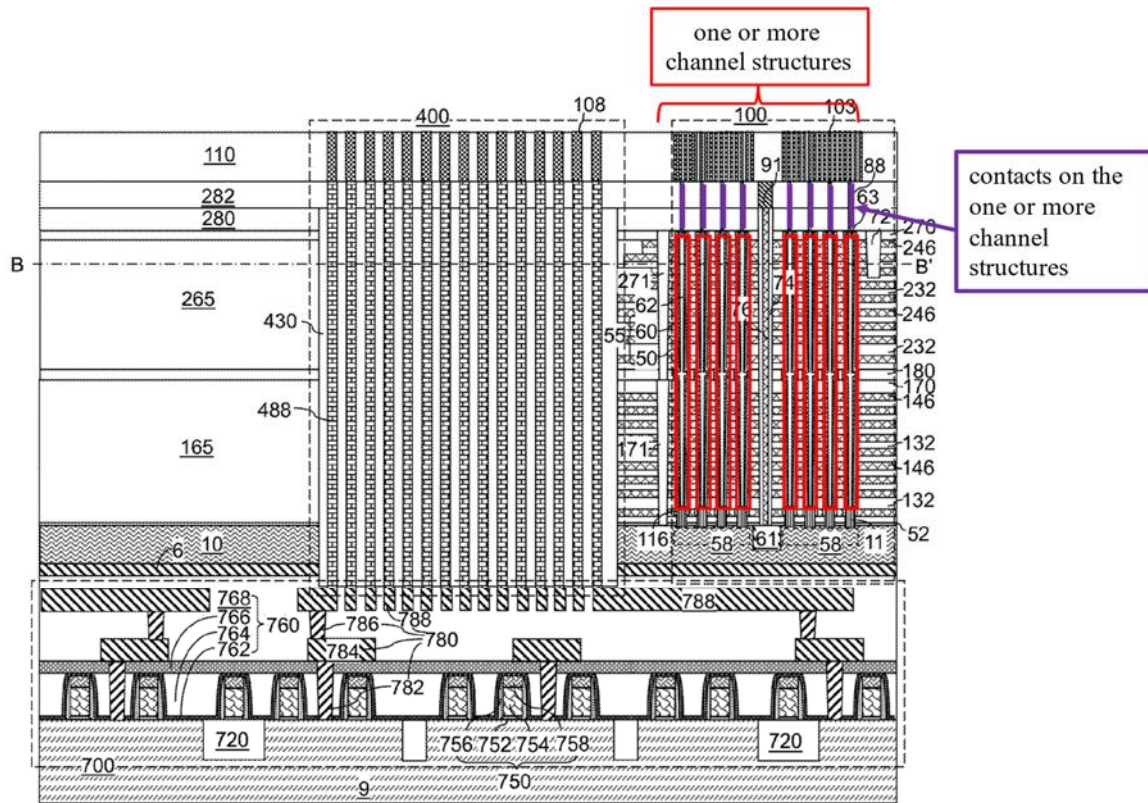


FIG. 17A

Toyama, Figure 16A. “Drain contact via structures 88 contacting the drain regions 63 can extend through the contact level dielectric layers (280, 282).” Toyama, [0241]. Toyama further explains that “drain contact via structures 88” “may be formed employing a respective set of patterning processes and fill processes.” *Id.*, [0241]-[0242].

A POSITA would have understood from Toyama’s disclosure that part of the “patterning” process includes a step of etching an opening in dielectric layers 280 and 282. §V.A.3 (etching background); Lee ¶¶ 160-163. And a POSITA would have understood from Toyama’s disclosure—or at least found obvious—that the dielectric layers 280 and 282 would be formed of a dielectric material such as silicon

oxide. Lee ¶ 163; Toyama, [0212], [0238].¹⁶ Thus, Toyama contemplates—or, at the very least, a POSITA would have found obvious— employing a dielectric-selective etchant (e.g., an etchant selective to silicon oxide) to form the opening that is ultimately filled by “drain contact via structures 88.” §V.A.3; Lee ¶ 163. Such selective etches were textbook material and routine to implement. *Id.*

A POSITA would have understood that without “drain regions 63,” the etch to form “drain contact via structures 88” may risk damaging elements of “memory

¹⁶ Toyama states that “second contact level dielectric layer 282 includes a dielectric material such as silicon oxide.” Toyama, [0238]. Toyama does not expressly state that “dielectric layer 280” is made of silicon oxide, but a POSITA would have understood Toyama to contemplate doing so. At the very least, forming layer 280 of silicon oxide would have been obvious to a POSITA. Lee ¶ 163 n.4. Toyama expressly notes that “dielectric layer 180” could be made of “a dielectric material such as silicon oxide.” Toyama, [0183]. A POSITA would have understood from Toyama’s disclosure that “dielectric layer 280” would similarly be made of silicon oxide, which was a well-known dielectric material. And a POSITA would have found it desirable to form “dielectric layer 280” out of silicon oxide where layer 282 is formed out of silicon dioxide because that would allow a continuous silicon-oxide-selective etch through both layers. Lee ¶ 163 n.4.

stack structures 55.” That is because “memory stack structures 55” may include dielectric elements (e.g., “blocking dielectric layer 51”) that are formed of the same materials (e.g., silicon oxide) as dielectric layers 280 and 282. Toyama, [0204]. Thus, if the etchant that is used to etch through the dielectric layers 280 and 282 were to contact the memory stack structures, it may damage the memory stack structures. §V.A.3; Lee ¶ 164.

That undesirable result is prevented by “drain regions 63,” which are between the opening that is filled to form “drain contact via structures 88” and the “memory stack structures 55.” Toyama, [0209], [0241]. “Drain regions 63” function as an etch stop because they are made of a material like doped polysilicon, which a POSITA would have understood would **not** react significantly with the etchant used to selectively etch the dielectric. §V.A.3 (e.g., CF₄). Even if the etchant were to remove a portion of “drain regions 63,” the thickness of “regions 63” acts as a buffer of sorts, so that the etchant might partially etch and stop before inadvertently etching through to the memory elements. Thus, “drain regions 63” serve to protect the dielectric materials in the memory stack from the etching process used to form “drain contact via structures 88.” In other words, because “drain regions 63” effectively stop the etch that ultimately forms the holes for “drain contact via structures 88,” each of “drain regions 63” is *an etch stop plug* that beneficially protects the channel structure. §V.A.3; Lee ¶¶ 164-165.

Indeed, Toyama’s “drain region 63” and the 378 Patent’s “etch stop plug 224” share similarities even beyond what is required by the claim. The 378 Patent’s “etch stop plug 224,” like Toyama’s “drain region 63,” “acts as the drain of NAND string 204.” Ex. 1001, 9:47-48; Toyama, [0209]. The 378 Patent discloses forming “etch stop plug 224” out of polysilicon, just like Toyama’s “drain region 63.” Ex. 1001, 15:65-16:1; Toyama, [0209]. The 378 Patent deposits “etch stop plug 224” and then levels it using chemical mechanical planarization (CMP) so that it is flush with a dielectric layer, just like Toyama’s “drain regions 63.” Ex. 1001, 15:65-16:1; Toyama, [0209]. Just as the 378 Patent forms contacts (“NAND string contacts 236”) over the “etch stop plug 224,” so too does Toyama form contacts (“drain contact via structures 88”) over “drain regions 63.” Ex. 1001, 17:28-34; Toyama, [0241]. And, as explained above, just as the 378 Patent’s “etch stop plug 224” prevents etching of dielectrics in the channel structure during formation of the contacts, so too do Toyama’s “drain regions 63.” These similarities further confirm that Toyama’s “drain region 63” is an *etch stop plug*.

Although the citations above are for Toyama’s “first exemplary structure,” Toyama’s Second Modification also teaches this limitation for the same reason. See, e.g., Toyama, Figure 49 (showing “drain regions 63”); §V.A.3; Lee ¶ 166.

9. [1.H] “a staircase structure in the alternating layer;”

As this Petition notes in the claim construction section, this limitation has a typographical error, and a POSITA would have interpreted the claim to mean “a staircase structure in the alternating layer **stack**.” §VII.A.

Toyama teaches *a staircase structure* (“staircase regions”) *in the alternating layer stack* (“alternating stack (132, 146, 232, 246)”):

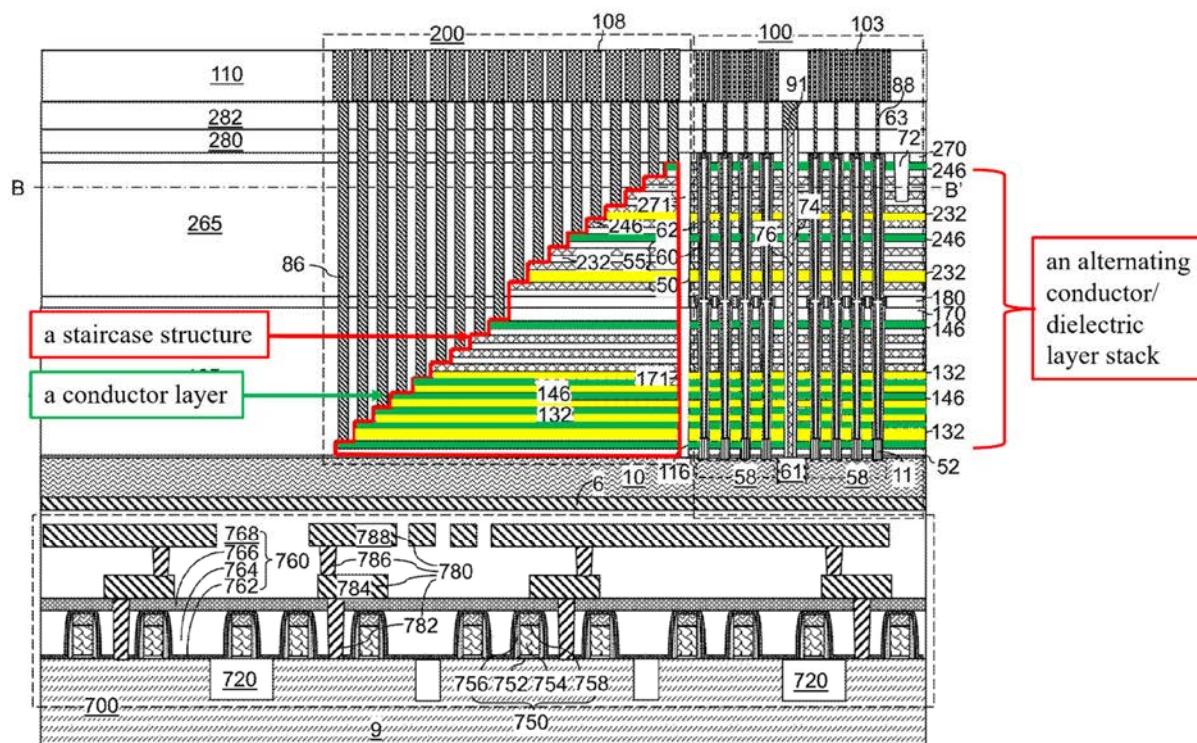


FIG. 17C

Toyama, Figure 17C; Lee ¶ 168. Toyama explains: “[t]he at least one alternating stack (132, 146, 232, 246) comprises staircase regions that include terraces in which each underlying electrically conductive layer (146, 246) extends farther along the

first horizontal direction hd1 than any overlying electrically conductive layer (146, 246).” Toyama, [0232].

Although the citations above are for Toyama’s “first exemplary structure,” a POSITA would have understood that Toyama’s Second Modification also teaches this limitation. In describing the fourth exemplary structure, Toyama notes that “word line contact via structures [86] can be formed as in the first through third embodiments.” Toyama, [0322]. As Toyama shows for the first embodiment, “word line contact via structures 86” are in contact with the electrically conductive layers (146, 246) in the “staircase regions.” *Id.*, Figure 17C, [0243]. A POSITA would therefore have understood Toyama’s fourth exemplary structure (and modifications thereof) to include *a staircase structure* (“staircase regions”). Lee ¶ 169.

At the very least, a POSITA would have found it obvious to implement a *staircase structure* (“staircase regions”) in Toyama’s Second Modification. A POSITA would have known that for the memory device to be functional, there must be some way of conveying signals to the “electrically conductive layers (146, 246)” because these layers serve as the word lines of the memory stack structures. Toyama, [0323]; Lee ¶ 170. A *staircase structure* (such as the first exemplary structure’s “staircase regions”) was a conventional and routine-to-implement structure to enable conveying signals to the electrically conductive layers. *Id.* Therefore, the use of a *staircase structure* in Toyama’s Second Modification is

nothing more than the use of a known technique (the first exemplary structure’s “staircase regions”) to improve a similar device (Toyama’s Second Modification) in the same way (enable the conveying of signals to the electrically conductive layers). *Id.*; *Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1380 (Fed. Cir. 2023).

10. [1.I] “slit structures extending vertically in the alternating layer stack; and”

As shown below, Toyama teaches *slit structures* (“laterally-elongated contact via structures 76”) *extending vertically through the alternating layer stack* (“alternating stack (132, 146, 232, 246)”):

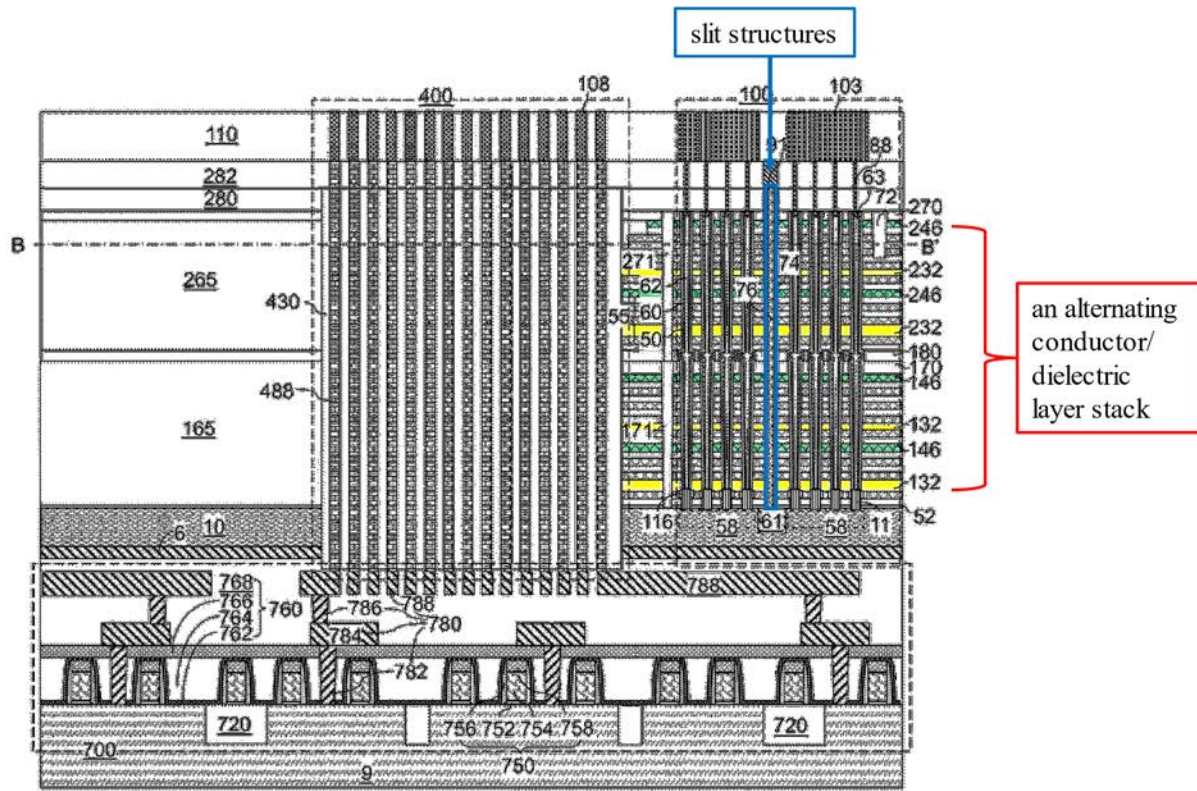
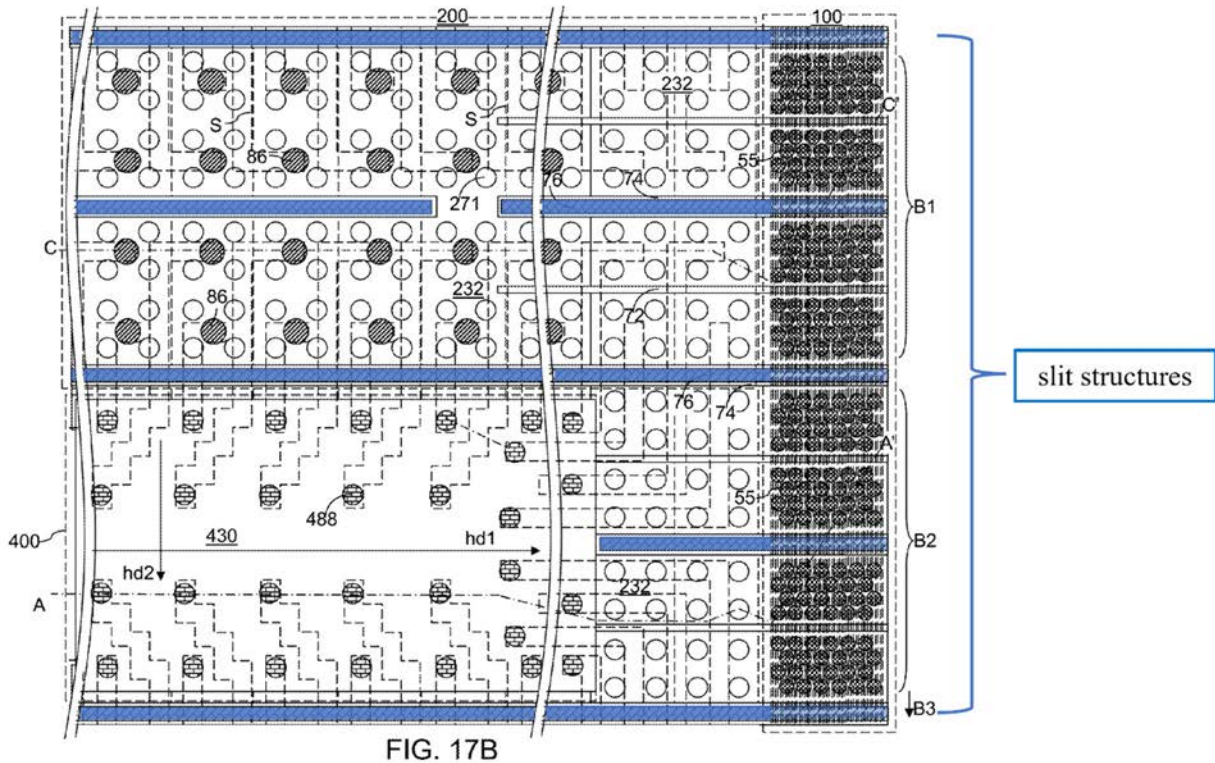


FIG. 17A

Toyama, Figure 17A; Lee ¶ 171. Toyama also depicts its *slit structures* (“laterally-elongated contact via structures 76”) in a top view:



Id., Figure 17B.

Although Toyama and the 378 Patent’s claim use slightly different terminology, each of “laterally-elongated contact via structures 76” is *a slit structure* as claimed. Lee ¶ 172. As an initial matter, the plain meaning of “slit” is of a laterally-elongated structure. *Id.*; Ex. 1022, 4 (Merriam-Webster’s definition of “slit” as “a long narrow cut or opening”). Toyama, Figure 17B (showing structure 76 has a slit shape). And, as shown in Figure 17A, above, Toyama discloses “laterally-elongated contact via structure 76” *extending vertically in the alternating layer stack* (“alternating stack (132, 146, 232, 246)”). Thus, Toyama’s “laterally-elongated contact via structures 76” meets the plain language of the claims.

Although the claims do not place any functional limitation on the “slit structure,” Toyama’s “laterally-elongated contact via structures 76” serves the same function as the 378 Patent’s “slit structures.” Lee ¶ 173. In the 378 Patent, each “slit structure 226 acts as a source contact for NAND strings 204.” Ex. 1001, 9:63-67. Similarly, each of Toyama’s “laterally-elongated contact via structures 76” serves as a “source connection.” Toyama, [0241]. The 378 Patent’s “[s]lit structures 226 ... extend along the y-axis to separate alternating conductor/dielectric stack 210 into multiple blocks.” Ex. 1001, 9:52-54. Similarly, “laterally-elongated contact via structures 76 laterally extend along the first horizontal direction ... and laterally divide the at least one alternating stack ... into a plurality of laterally spaced-apart blocks.” Toyama, [0237].

Although the citations above are for Toyama’s “first exemplary structure,” Toyama’s Second Modification also includes “laterally-elongated contact via structures 76” and teaches this limitation for the same reasons as discussed above. *See, e.g.*, Toyama, Figure 49; Lee ¶ 174.

11. [1.J] “one or more contact layers on the one or more TACs, the one or more channel structures, and the slit structures.”

The 378 Patent teaches that the “3D memory device 200 can further include a contact layer 242.” Ex. 1001, 11:48-49. “Contact layer 242 can include a dielectric layer and a plurality of contacts 246 (e.g., vias) in the dielectric layer.” *Id.*, 11:51-53. As explained below, Toyama discloses *contact layers* on the recited structures.

a. First exemplary structure

In the context of the first exemplary structure, Toyama teaches *TACs* (“through-memory-level via structures 488”), *one or more channel structures* (“memory stack structures 55”), and *slit structures* (“laterally elongated contact via structures 76”). §§IX.A.5.b (limitation [1.D]), IX.A.6 (limitation [1.E]), IX.A.10 (limitation [1.I]).

As the below figure shows, Toyama further discloses a:

- *a contact layer* (including “line level dielectric layer 110” and “upper-level metal interconnect structures 108”) *on* (in contact with or extending above) *the one or more TACs* (“through-memory-level via structures 488”);
- *a contact layer* (including “contact level dielectric layers (280, 282)” and “drain contact via structures 88”) *on the one or more channel structures* (“memory stack structures 55”); and
- *a contact layer* (including “second contact level dielectric layer 282” and “source connection via structures 91”) *on the slit structures* (“laterally-elongated contact via structures 76”):

Toyama, Figure 17A; *id.*, [0238]-[0239], [0250] (“upper level metal interconnect structures 108 ... are electrically coupled to (e.g., formed on or in physical contact with) ... a through-memory-level via structures 488”); *id.*, [0251] (“The bit lines 103 are formed over the memory-level assembly, and are electrically coupled to nodes (e.g., drain regions 63) of the memory stack structures 55 by the drain contact via structures 88.”); *id.*, [0241] (“A source connection via structure 91 can extend through the contact level dielectric layers (280, 282) to provide electrical connection to the laterally-elongated contact via structures 76.”); *id.*, [0250] (“Various metal interconnect structures (108, 103, 101) can be formed in the line level dielectric layer 110. ... [U]pper-level metal interconnect structures 108 ... are electrically coupled

to ... through-memory-level via structure[s] 488”); Ex. 1001, 4:20-25 (defining “on”); Lee ¶ 178.

b. Second Modification

In the context of the Second Modification, Toyama teaches *TACs* (“through-memory-level via structures 676”), *one or more channel structures* (“memory stack structures 55”), and *slit structures* (“laterally elongated contact via structures 76”). §§IX.A.5.a (limitation [1.D]), IX.A.6 (limitation [1.E]), IX.A.10 (limitation [1.I]). For largely the same reasons as described for the first exemplary structure of, Toyama further discloses:

- *a contact layer* (including “line level dielectric layer 110” and “upper-level metal interconnect structures 108”) *on the one or more TACs* (“through-memory-level via structures 676”) *and the slit structures* (“laterally elongated contact via structures 76”)¹⁷; and

¹⁷ The plain language of limitation [1.J] requires *a contact layer* (which may include dielectric material) on *the slit structures*, but not necessarily *contacts* on *the slit structures*. Even if it did, Toyama’s Second Modification discloses or renders obvious contacts on the slit structures. §IX.H.8.b (limitation [15.G]).

- *a contact layer* (including “first contact level dielectric layer 280” and “drain contact via structures 88”) *on the one or more channel structures* (“memory stack structures 55”):

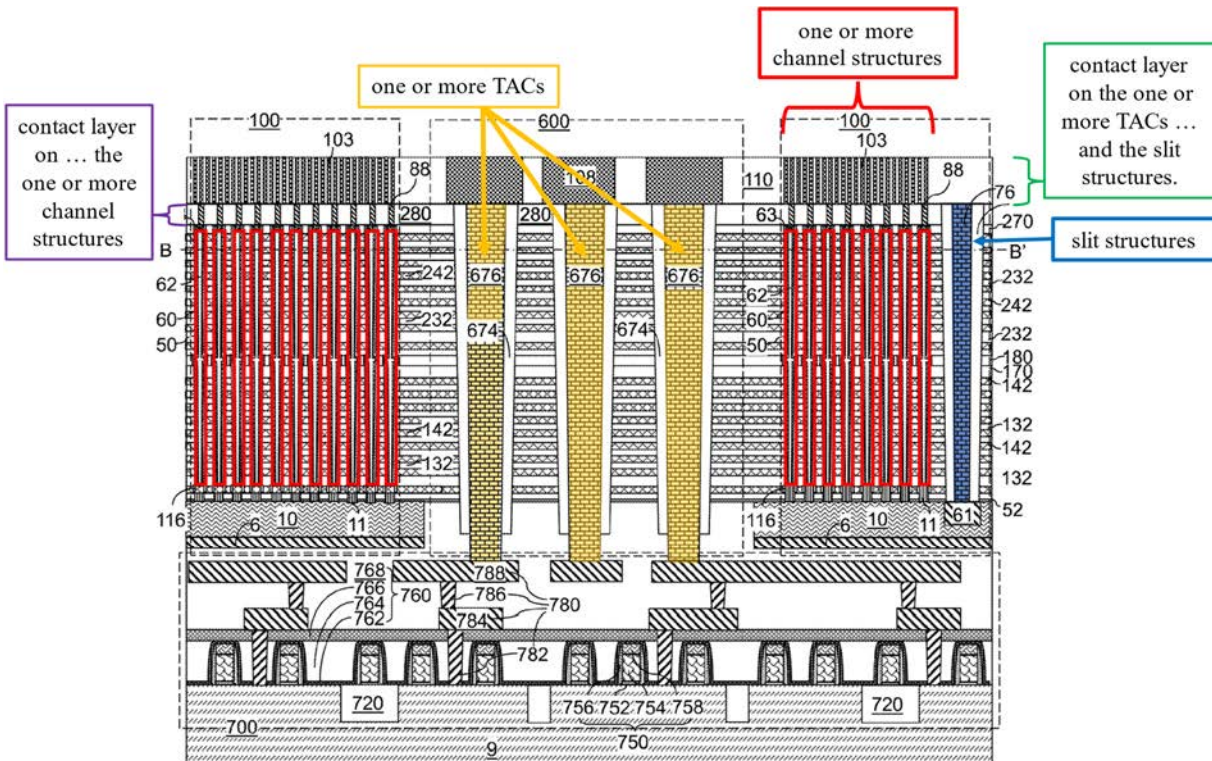


FIG. 49

Toyama, Figure 49, [0342]; Ex. 1001, 4:20-25 (defining “on”); Lee ¶¶ 180-184.

B. Claim 2:

1. [2] “The 3D memory device of claim 1, wherein the dielectric structure abuts a sidewall surface of the TACs.”

a. Second Modification

In the context of its Second Modification, Toyama teaches *the dielectric structure* (“insulating liners 674”) *abuts a sidewall surface of the TACs* (a sidewall of each of the “through-memory-level via structures 676”):

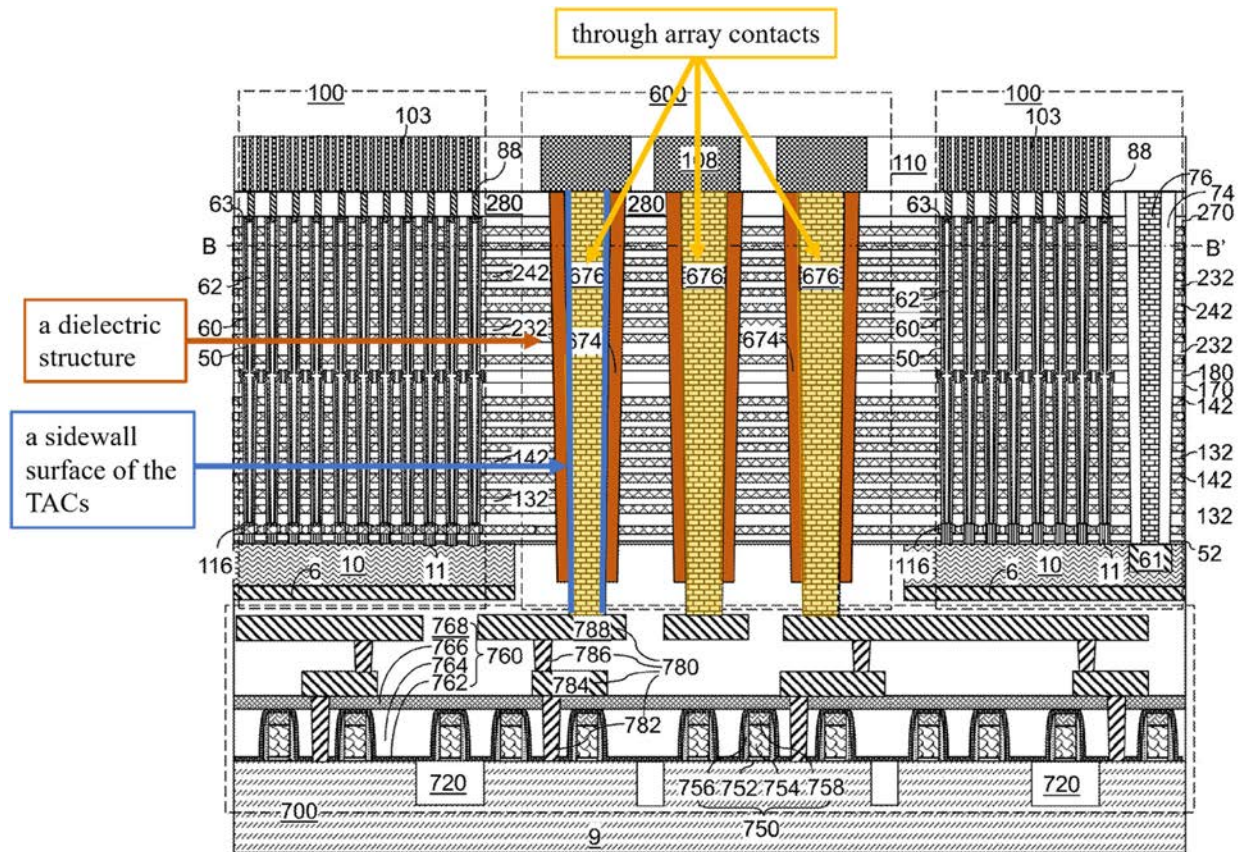
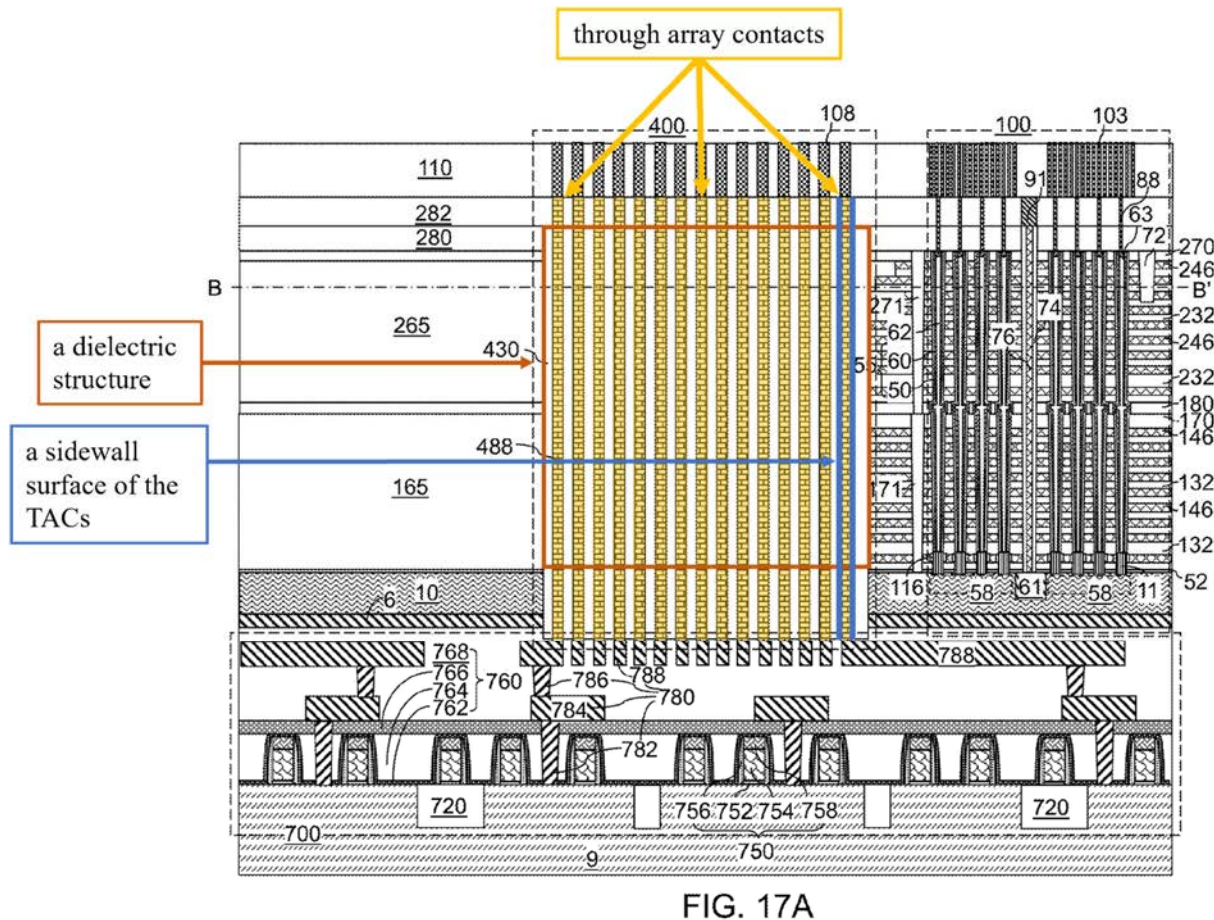


FIG. 49

Toyama, Figure 49; Lee ¶ 186.

b. First exemplary structure

In the context of its first exemplary structure, Toyama teaches *the dielectric structure* (upper part of “dielectric fill material portion 430”) *abuts a sidewall surface of the TACs* (sidewall surface of “through-memory-level via structures 488”):



Toyama, Figure 17A; Lee ¶ 187.

C. Claim 3:

1. [3] “The 3D memory device claim 1, wherein the 3D memory device is a NAND 3D memory device.”

A POSITA would have readily appreciated that Toyama’s exemplary structures are each *a 3D NAND memory device*. Lee ¶ 188; Toyama, Abstract; §IX.A.1 (limitation [1.PRE]).

D. Claim 4:

1. [4] **“The 3D memory device of claim 1, wherein the alternating layer stack comprises alternating pairs of a dielectric and a conductor layer.”**

As explained for limitation [1.B], above, Toyama discloses that its *alternating layer stack* (“alternating stack (132, 146, 232, 246)”) *comprises alternating pairs of a dielectric layer and a conductor layer* (“insulating layers (132, 232)” and “electrically conductive layers (146, 246),” respectively. Toyama, Figures 17A (first exemplary structure), 49 (Second Modification), [0172], [0190], [0228], [0232], [0337]; Lee ¶ 189.

E. Claim 5:

1. [5] **“The 3D memory device of claim 1, wherein the dielectric material is silicon oxide.”**

a. Second Modification

In Toyama’s Second Modification, “insulating liners 674” are *a dielectric structure*, and the material from which “insulating liners 674” are made is *a dielectric material*. §IX.A.4.a (limitation [1.C]).

Toyama contemplates that “insulating liner 674” comprises silicon oxide. Specifically, Toyama notes that “insulating liner 674” may “hav[e] a same material composition ... as the insulating spacer 74.” Toyama, [0381]. Toyama describes “spacer 74,” in turn, as including “an insulating material such as silicon oxide.” *Id.*, [0234].

Thus, Toyama teaches *the dielectric material* (a material out of which “insulating liners 674” are made) *comprises silicon oxide*.

To the extent Toyama does not expressly disclose this limitation, it would have been obvious to a POSITA. By its very terms, “insulating liner 674” is insulating, and a POSITA would have known silicon oxide to be a commonplace and suitable insulating material from which “insulating liner 674” could be made. Ex. 1019 (U.S. Pat. No. 9,293,348), 2:61-65 (“dielectric structure” may comprise an “oxide” such as “silicon oxide”); Ex. 1020 (U.S. Pat. No. 10,103,169), Figs. 11-12, 3:1-8 (discussing “formation of a conformal silicon oxide liner” in 3D-NAND); Ex. 1021 (U.S. Pat. No. 8,697,519), 7:29-40 (“the liner insulating layer may include a silicon oxide layer”); Lee ¶¶ 191-192.

b. First exemplary structure

In Toyama’s first exemplary structure, *the dielectric material* is the “dielectric fill material” that forms “dielectric fill material portion 430.” §IX.A.4.b (limitation [1.C]).

Toyama further notes “dielectric fill material portion 430 includes a dielectric material such as undoped silicate glass (e.g., silicon oxide), doped silicate glass, or a spin-on glass (SOG).” Toyama, [0216].

Toyama thus teaches *the dielectric material* (“dielectric fill material” that forms “dielectric fill material portion 430”) *comprises silicon oxide*. Lee ¶ 193.

F. Claim 6:

1. [6] “The 3D memory device of claim 1, wherein the dielectric structure comprises an oxide.”

For the reasons explained above, Toyama teaches that *the dielectric structure* (“insulating liners 674” in the Second Modification, and the upper part of “dielectric fill material portion 430” in the first example structure) *comprises an oxide* (e.g., silicon oxide). §§IX.A.4.a.v (Second Modification, limitation [1.C.v]), IX.A.4.b.v (first exemplary structure, limitation [1.C.v]), IX.E.1 (claim 5); Lee ¶ 194.

G. Claim 7:

1. [7] “The 3D memory device of claim 1, wherein the dielectric structure defines a through array contact region within the 3D memory device.”

As an initial matter, the 378 Patent broadly defines *through array contact region*, noting that it “can have a rectangle or square shape” but that “these shapes are not limiting and dielectric structure 232 can have any shape according to a design layout,” and that “multiple dielectric structures ... are possible across [the] substrate.” Ex. 1001, 10:49-56. Toyama’s Second Modification, and Toyama’s first exemplary structure, both teach this limitation. Lee ¶ 195.

a. Second Modification

In its Second Modification, Toyama discloses *the dielectric structure* (“insulating liners 674”) *defines a through array contact region within the 3D memory device* (part of “through-memory-level via region 600”):

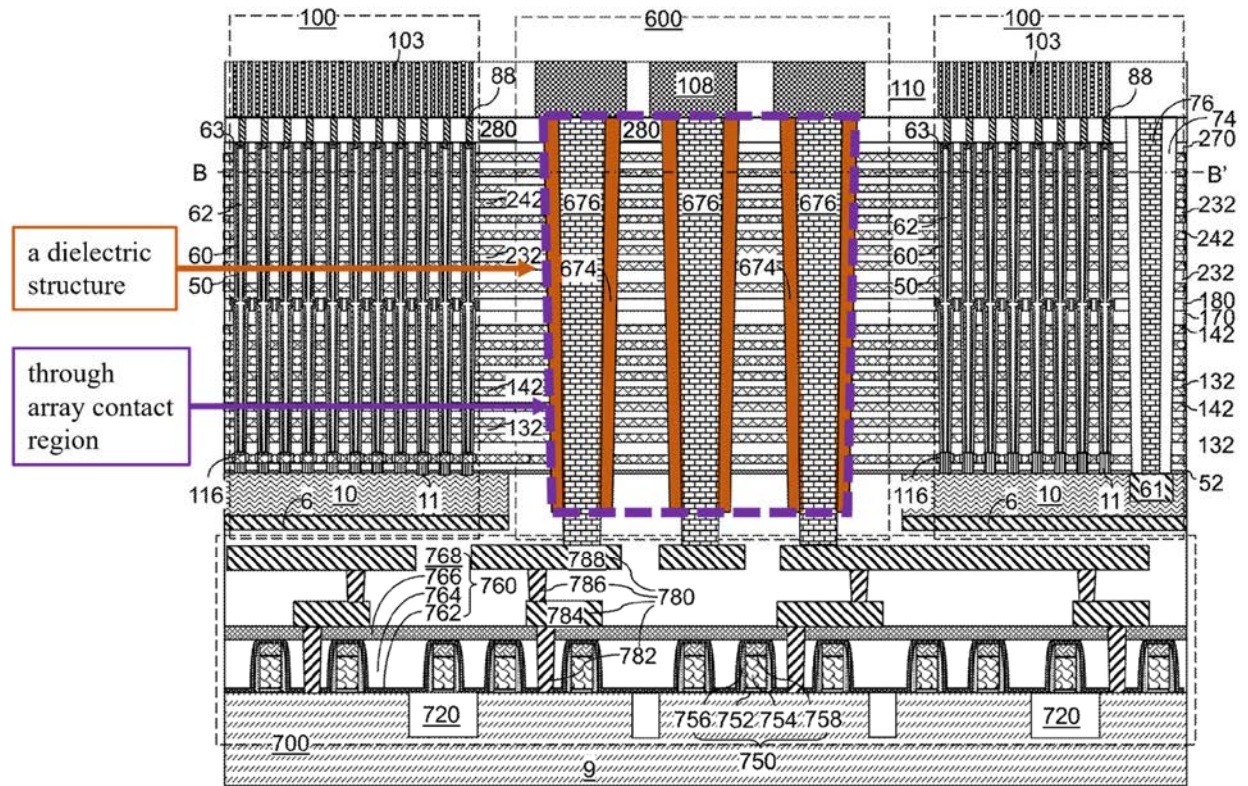


FIG. 49

Toyama, Figure 49; *id.*, [0333], [340], [352]; Lee ¶¶ 196-197. As “[i]n some embodiments” of the 378 Patent, the “dielectric structure ... defines the boundaries, the shape, and the size of [the] TAC region.” Ex. 1001, 10:21-23. Thus, the part of the dielectric structure (“insulating liners 674”) through which the *through array contacts* (“through-memory-level via structures 676”) extend is a *through array contact region* because the *through array contacts* extend through this region and, in doing so, are electrically isolated by the *dielectric structure*.

2. [15.A] “a substrate with an isolation structure;”

a. [15.A.i] “a substrate”

Toyama teaches or renders obvious *a substrate* (“planar semiconductor material layer 10”). §IX.A.2 (limitation [1.A]); Lee ¶¶ 201-203.

b. [15.A.ii] “... with an isolation structure”

Toyama teaches or renders obvious *an isolation structure* (in the Second Modification, the insulating material layer that fills “opening 151”;¹⁸ and in the first exemplary structure, the lower part of “dielectric fill material portion 430”¹⁹). §§IX.A.4.a.ii (Second Modification, limitation [1.C.ii]), IX.A.4.b.ii (first exemplary structure, limitation [1.C.ii]); Lee ¶¶ 205-212.

¹⁸ Although claim 1 recites “an isolation region” whereas claim 15 recites “an isolation structure,” this difference is immaterial for present purposes. The insulating material that fills “opening 151” is *an isolation structure* for all of the reasons that it is *an isolation region*, and also because it something that is constructed. Ex. 1022, 5 (Merriam-Webster’s definition of “structure” as “something (as a building) that is constructed”).

¹⁹ The lower part of “dielectric fill material portion 430” is *an isolation structure* for all of the same reasons that it is *an isolation region*, and also because it something that is constructed. Ex. 1022, 5.

3. **[15.B] “an alternating conductor/dielectric layer stack disposed on the substrate;”**

Toyama teaches or renders obvious *an alternating conductor/dielectric layer stack* (“alternating stack (132, 146, 232, 246”) *disposed on the substrate* (“planar semiconductor material layer 10”). §§IX.H.2.a (limitation [15.A.i]), IX.A.3 (limitation [1.B]), IX.D.1 (claim 4); Lee ¶¶ 214-to 16.

4. **[15.C] “a dielectric structure on the isolation structure and extending vertically through the alternating conductor/dielectric layer stack, wherein the alternating conductor/dielectric layer stack abuts a sidewall surface of the dielectric structure and the dielectric structure is formed of a dielectric material;”**

a. **Second Modification**

Toyama teaches or renders obvious *a dielectric structure* (“insulating liners 674”), §IX.A.4.a.i (limitation [1.C.i]):

- *on the isolation structure* (the insulating material layer that fills “opening 151”), §§IX.A.4.a.i, IX.A.4.a.ii (limitations [1.C.i], [1.C.ii]);
- *extending vertically through the alternating conductor/dielectric layer stack* (“alternating stack (132, 146, 232, 246”)”, §§IX.H.3, IX.A.4.a.iii (limitations [15.B], [1.C.iii]);
- *wherein the alternating conductor/dielectric layer stack* (“alternating stack (132, 146, 232, 246”)” *abuts a sidewall surface of the dielectric*

structure (a sidewall surface of “insulating liners 674”), §§IX.H.3, IX.A.4.a.iv (limitations [15.B], [1.C.iv]); and

- *formed of a dielectric material* (e.g., silicon oxide), §IX.A.4.a.v (limitation [1.C.v]). Lee ¶¶ 218-225.

b. First exemplary structure

Toyama teaches or renders obvious *a dielectric structure* (upper part of “dielectric fill material portion 430”), §IX.A.4.b.i (limitation [1.C.i]):

- *on the isolation structure* (lower part of “dielectric fill material portion 430”), §§IX.A.4.b.i, IX.A.4.b.ii (limitations [1.C.i], [1.C.ii]);
- *extending vertically through the alternating conductor/dielectric layer stack* (“alternating stack (132, 146, 232, 246)”), §§IX.H.3, IX.A.4.b.iii (limitations [15.B], [1.C.iii]);
- *wherein the alternating conductor/dielectric layer stack* (“alternating stack (132, 146, 232, 246)”) *abuts a sidewall surface of the dielectric structure* (a sidewall surface of the upper part of “dielectric fill material portion 430”), §§IX.H.3, IX.A.4.b.iv (limitations [15.B], [1.C.iv]); and
- *formed of a dielectric material* (e.g., silicon oxide), §IX.A.4.b.v (limitation [1.C.v]). Lee ¶¶ 226-236.

5. [15.D] “channel structures and slit structures extending vertically through the alternating conductor/dielectric layer stack;”

Toyama teaches *channel structures* (“memory stack structures 55”) *and slit structures* (“laterally-elongated contact via structures 76”) *extending vertically through the alternating conductor/dielectric layer stack* (“alternating stack (132, 146, 232, 246)”). §§IX.A.6, IX.A.10, IX.H.3 (limitations [1.E], [1.I], [15.B]); Lee ¶¶ 238-244.

6. [15.E] “a staircase structure disposed in the alternating conductor/dielectric layer stack, wherein the staircase structure comprises levels with each level having a conductor layer thereon;”

Toyama discloses *a staircase structure* (“staircase regions”) *disposed in the alternating conductor/dielectric layer stack* (“alternating conductor/dielectric layer stack”), *wherein the staircase structure comprises levels with each level having a conductor layer* (“electrically conductive layers 146, 246”) *thereon*. §§IX.A.9, IX.H.3 (limitations [1.H], [15.B]), Lee ¶¶ 245-247.

7. [15.F] “a word line contact disposed on the conductor layer of the each level;”

As shown below, Toyama discloses *a word line contact* (“word line contact via structures 86”) *disposed on the conductor layer of the each level* (“electrically conductive layers (146, 246)”):

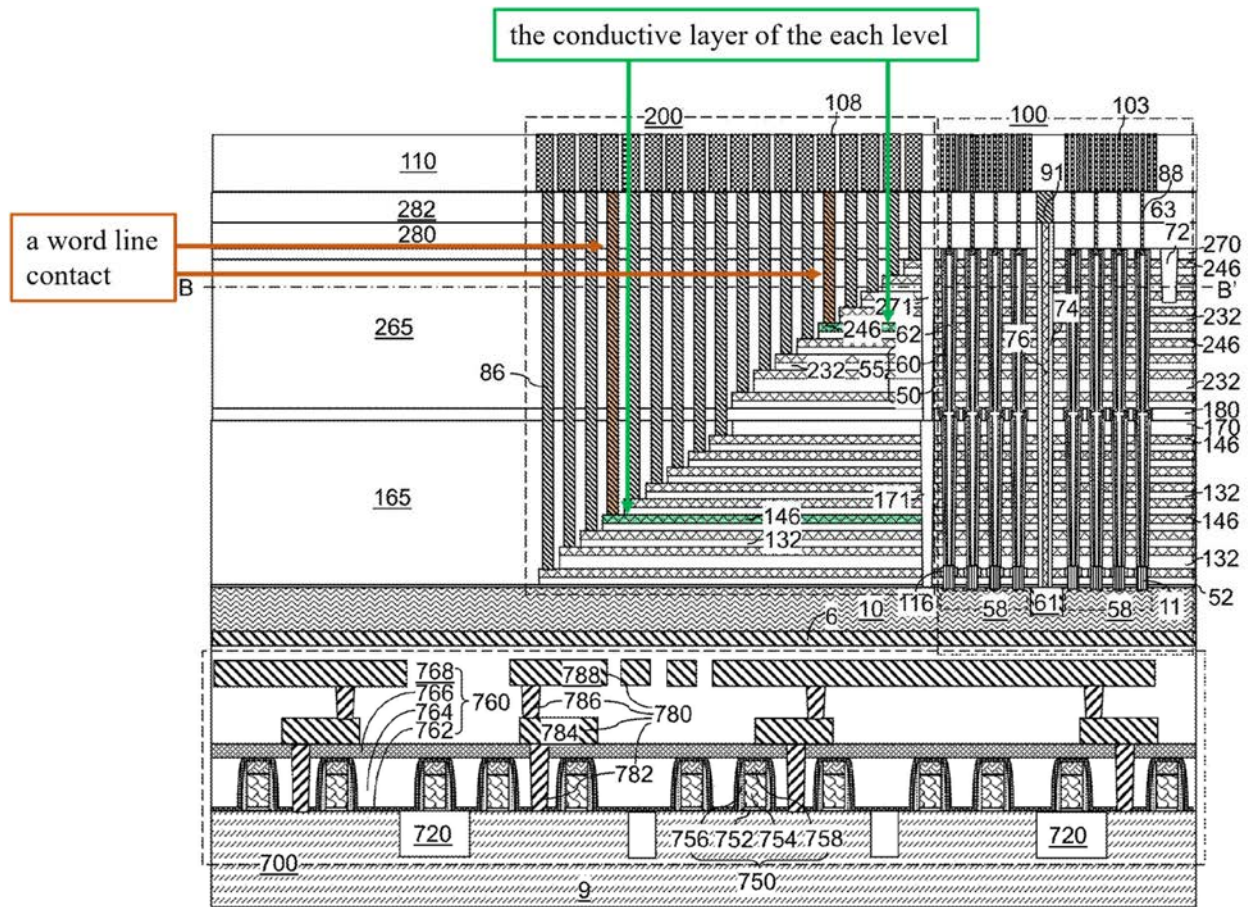


FIG. 17C

Toyama, Figure 17C; *id.*, [0260] (“[W]ord line contact via structures 86 ... can contact respective portions of electrically conductive layers (146, 246)”; Lee ¶ 248.

Although the citations above are for Toyama’s “first exemplary structure,” Toyama’s Second Modification also teaches this limitation for the same reason. In describing the fourth exemplary structure, Toyama notes that the *word line contacts* (“word line contact via structures”) “can be formed as in the first through third embodiments.” Toyama, [0322]. At the very least, a POSITA would have found it obvious to convey signals to electrically conductive layers (146, 246) using “word

line contact via structures” on “staircase regions” for the reasons described above.

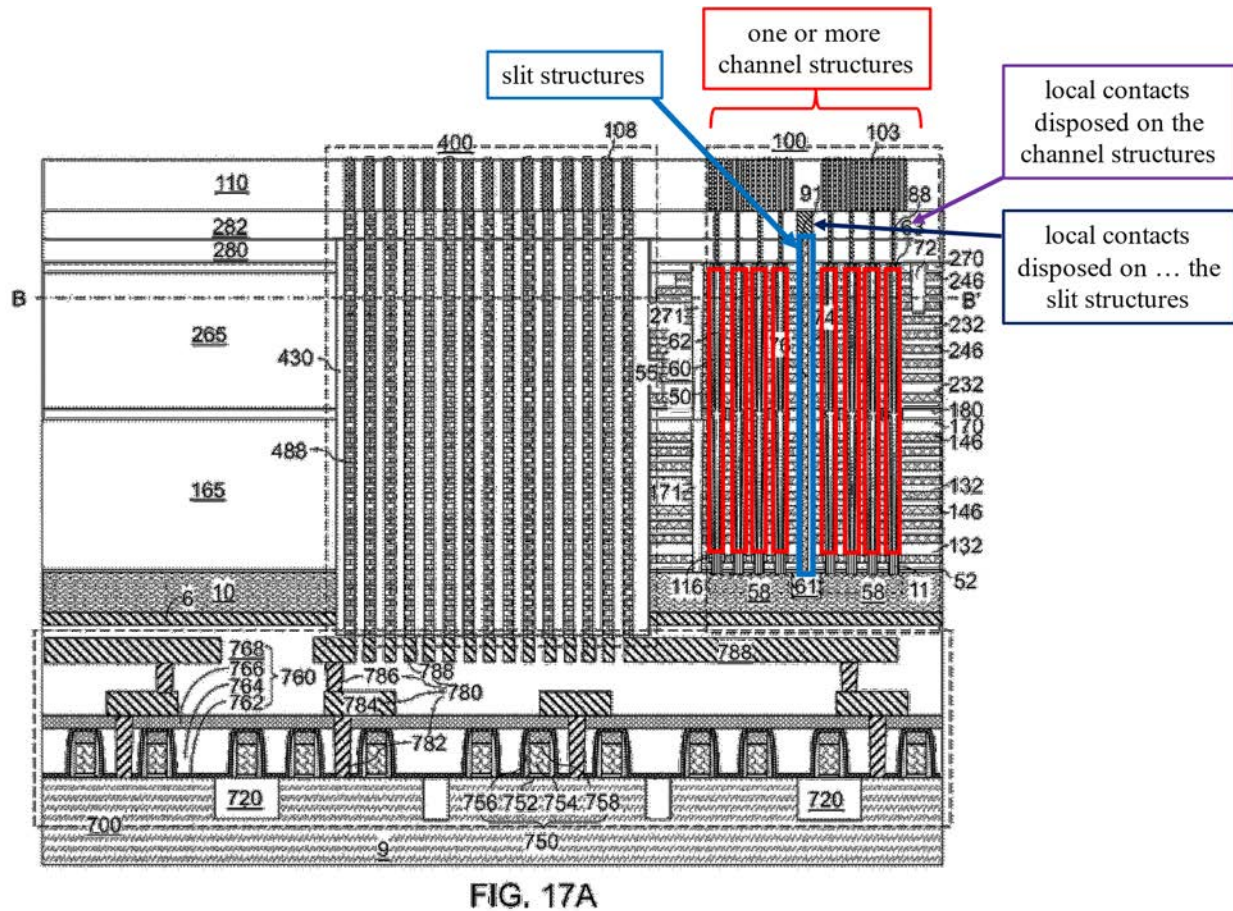
§IX.H.6 (limitation [15.E]). Lee ¶¶ 249-250.

8. [15.G] “local contacts disposed on the channel structures and the slit structures; and”

As an initial matter, the 378 Patent states that “[i]n some embodiments, 3D memory device 200 includes a plurality of ‘local contacts.’” Ex. 1001, 11:16-17. “The contacts are referred to herein as ‘local contacts’ because they are in direct contact with the memory array structures, and further because they are formed within dielectric layer 230.” *Id.*, 11:20-24.

a. First exemplary structure

Toyama discloses *local contacts* (“drain contact via structures 88”) *disposed on* (in contact with or extending above) *the channel structures* (“memory stack structures 55”), and *local contacts* (“source connection via structures 91”) *disposed on* (in contact with or extending above) *the slit structures* (“laterally-elongated contact via structures 76”):



Toyama, Figure 17A; *id.*, [0251] (“The bit lines 103 are formed over the memory-level assembly, and are electrically coupled to nodes (e.g., drain regions 63) of the memory stack structures 55 by the drain contact via structures 88.”); *id.*, [0241] (“A source connection via structure 91 can extend through the contact level dielectric layers (280, 282) to provide electrical connection to the laterally-elongated contact via structures 76.”); Lee ¶ 252.

b. Second Modification

Although the citations above are for Toyama's "first exemplary structure," Toyama's Second Modification also teaches (or, at the very least renders obvious) this limitation.

Toyama's Second Modification discloses *local contacts* ("drain contact via structures 88") *disposed on the channel structures* ("memory stack structures 55") for the reasons explained above for the first exemplary structure. Toyama, Figure 49, [0342] ("drain contact via structures 88 ... can be formed as in the first through third embodiments"); Lee ¶ 253.

Toyama does not expressly disclose *local contacts* ("source connection via structures 91") *disposed on the slit structures* ("laterally-elongated contact via structures 76") in the context of the Second Modification, likely because of where the cross section of Figure 49 is taken Lee ¶ 254. However, a POSITA would have understood the Second Modification to include *local contacts disposed on the slit structures* ("source connection via structures 91"). Indeed, in describing the Second Modification, Toyama notes "[t]he metal interconnect structures can include ... source connection line structures (not shown)." Toyama, [0342]. As expressly described in the first exemplary structure, "source connection line structures 101 ... contact the source connection via structures 91 to provide electrically conductive paths for biasing the source region 61 through the laterally-elongated contact via

structures 76.” Toyama, [0250]. A POSITA would have understood the Second Modification, which expressly includes “source connection line structures,” “source region 61,” and “laterally elongated contact via structure 76,” would also include “source connection via structures.” Lee ¶¶ 254-255.

At the very least, a POSITA would have found the use of *local contacts disposed on the slit structures* (“source connection via structures 91”) obvious. A POSITA would have understood “laterally-elongated contact via structures 76” serve as source lines for “source regions 61.” Toyama, [0382]. And a POSITA would have understood that for “via structures 76” to serve their purpose, they would connect to a higher-level source connection. Given that other of Toyama’s embodiments (from which the Second Modification derives) expressly disclose “source connection via structures 91” for this purpose, a POSITA would have been motivated to implement “source connection via structures 91” in the Second Modification, and would have had a reasonable expectation of success in doing so. Lee ¶ 256.

9. [15.H] “through array contacts (TACs) extending vertically through the dielectric and the isolation structures.”

a. Second Modification

Toyama discloses *through array contacts (TACs)* (“through-memory-level via structures 676”) *extending vertically through the dielectric structure* (“insulating liners 674”) *and isolation structure* (insulating material layer that fills “opening

151”). §§IX.A.5.a, IX.H.2.b, IX.H.4.a (limitations [1.D], [15.A.ii], [15.C]); Lee ¶¶ 257-259.

b. First exemplary structure

Toyama discloses *through array contacts (TACs)* (“through-memory-level via structures 488”) *extending vertically through the dielectric structure* (upper part of “dielectric fill material portion 430”) *and isolation structure* (lower part of “dielectric fill material portion 430”). §§IX.A.5.b, IX.H.2.b, IX.H.4.b (limitations [1.D], [15.A.ii], [15.C]); Lee ¶¶ 260-262.

I. Claim 18:

1. [18.PRE] “The 3D memory device of claim 15, further comprising:” [18.A] “an etch stop plug interposed between each local contact of the local contacts and each channel structure of the channel structures; and”

Toyama teaches *an etch stop plug* (“drain region 63”) *interposed between each local contact of the local contacts* (“drain contact via structures 88”) *and each channel structure of the channel structures* (“memory stack structures 55”):

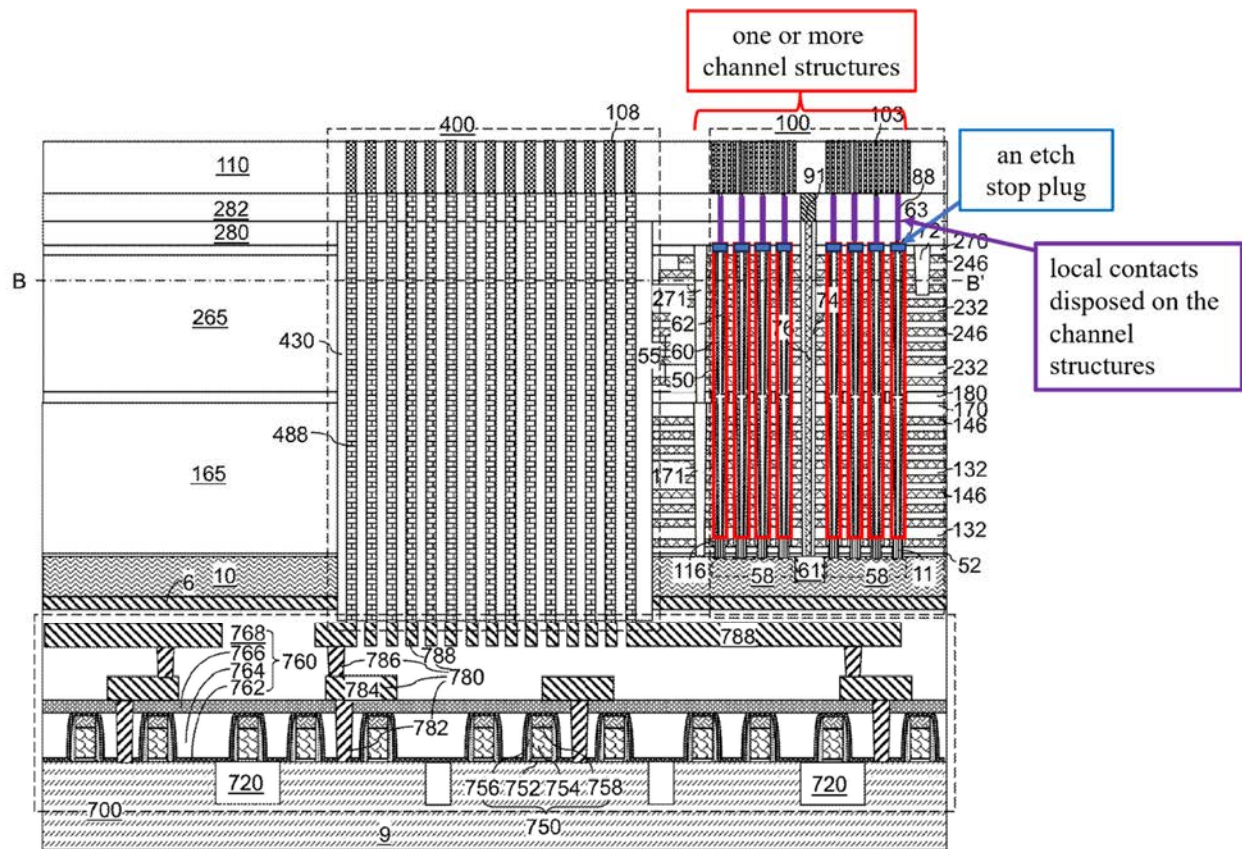


FIG. 17A

Toyama, Figure 17A; §§IX.A.8, IX.H.8, IX.H.5 (limitations [1.G], [15.G], [15.D]); Lee ¶¶ 263-266.

2. [18.B] “an epitaxial layer disposed between the channel structures and the substrate.”

As explained above, Toyama teaches *an epitaxial layer* (“pedestal channel portion 11”) *disposed between the channel structures* (“memory stack structures 55”) *and the substrate* (“planar semiconductor material layer 10”). §§IX.A.7, IX.H.2, IX.H.5 (limitations [1.F], [15.A], [15.D]); Lee ¶¶ 267-269. The minor wording differences between this limitation and limitation [1.F] are immaterial.

X. SECONDARY CONSIDERATIONS

There is no evidence in the prosecution history of this or any related application or patent that any arguments regarding secondary considerations exist. None were identified during prosecution. *See generally* Ex. 1002. Even if such considerations existed, none would overcome the strong *prima facie* showing of obviousness.

XI. CONCLUSION

Petitioner respectfully requests that the Board enter a final written decision finding the Challenged Claims unpatentable.

Respectfully submitted,

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CERTIFICATE OF COMPLIANCE

The undersigned certifies that the foregoing PETITION FOR *INTER PARTES* REVIEW complies with the type volume limitation in 37 C.F.R. § 42.24(a). According to the utilized word-processing system's word count, the petition—excluding the caption, table of contents, table of exhibits, mandatory notices, certificate of word count, and certificate of service—contains 13,588 words.

Dated: May 19, 2024

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CERTIFICATE OF SERVICE

The undersigned hereby confirms that the foregoing Petition for *Inter Partes* Review and associated exhibits were caused to be served on May 20, 2024 via overnight courier upon the following counsel of record for Patent Owner:

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