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Form Revision Date: August 26, 2013

PTO/AIA/15 (10-17)
Approved for use through 11/30/2017. OMB 0651-0032
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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	4123.0190001
First Named Inventor	Qian TAO
Title	See 1 in Addendum
Priority Mail Express® Label No.	

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. [ ] **Fee Transmittal Form** (PTO/SB/17 or equivalent)
2. [ ] **Applicant asserts small entity status.** See 37 CFR 1.27
3. [ ] **Applicant certifies micro entity status.** See 37 CFR 1.29. Applicant must attach form PTO/SB/15A or B or equivalent.
4. [X] **Specification** [*Total Pages* 36] Both the claims and abstract must start on a new page. *(See MPEP § 608.01(a) for information on the preferred arrangement)*
5. [X] **Drawing(s)** (35 U.S.C. 113) [*Total Sheets* 15]
6. **Inventor's Oath or Declaration** [*Total Pages* ____] *(including substitute statements under 37 CFR 1.64 and assignments serving as an oath or declaration under 37 CFR 1.63(e))*
   a. [ ] Newly executed (original or copy)
   b. [ ] A copy from a prior application (37 CFR 1.63(d))
7. [X] **Application Data Sheet** ** See note below.* See 37 CFR 1.76 (PTO/AIA/14 or equivalent)
8. **CD-ROM or CD-R** in duplicate, large table, or Computer Program (*Appendix*)
   [ ] Landscape Table on CD
9. **Nucleotide and/or Amino Acid Sequence Submission** (*if applicable, items a. – c. are required*)
   a. [ ] Computer Readable Form (CRF)
   b. [ ] Specification Sequence Listing on:
      i. [ ] CD-ROM or CD-R (2 copies); or
      ii. [ ] Paper
   c. [ ] Statements verifying identity of above copies

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Alexandria, VA 22313-1450

ACCOMPANYING APPLICATION PAPERS

10. [ ] **Assignment Papers** (cover sheet & document(s))
    Name of Assignee Yangtze Memory Technologies Co., Ltd.
11. [ ] **37 CFR 3.73(c) Statement** (*when there is an assignee*) [X] **Power of Attorney**
12. [ ] **English Translation Document** (*if applicable*)
13. [ ] **Information Disclosure Statement** (PTO/SB/08 or PTO-1449)
    [ ] Copies of citations attached
14. [ ] **Preliminary Amendment**
15. [ ] **Return Receipt Postcard** (*MPEP § 503*) (*Should be specifically itemized*)
16. [ ] **Certified Copy of Priority Document(s)** (*if foreign priority is claimed*)
17. [ ] **Nonpublication Request** Under 35 U.S.C. 122(b)(2)(B)(i). Applicant must attach form PTO/SB/35 or equivalent.
18. [X] **Other:** Authorization under 37 CFR 1.136(a)(3)

Note:* (1) Benefit claims under 37 CFR 1.78 and foreign priority claims under 1.55 **must be included in an Application Data Sheet (ADS).
(2) For applications filed under 35 U.S.C. 111, the application must contain an ADS specifying the applicant if the applicant is an assignee, person to whom the inventor is under an obligation to assign, or person who otherwise shows sufficient proprietary interest in the matter. See 37 CFR 1.46(b).

19. CORRESPONDENCE ADDRESS

[X] The address associated with Customer Number: 26111 **OR** [ ] Correspondence address below

Name					
Address					
City		State		Zip Code	
Country		Telephone		Email	

Signature	/Donald J. Featherstone/	Date	7/27/18
Name (Print/Type)	Donald J. Featherstone	Registration No. (Attorney/Agent)	33,876

This collection of information is required by 37 CFR 1.53(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Micron Ex. 1002, p. 2
Micron v. YMTC
IPR2024-00909

Addendum

1. THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES

Sterne Kessler
STERNE KESSLER GOLDSTEIN & FOX

DONALD J. FEATHERSTONE
DIRECTOR
(202) 772-8629
DONF@STERNEKESSLER.COM

July 27, 2018

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Re: U.S. Non-Provisional Patent Application under 37 C.F.R. § 1.53(b)
(Continuation of Appl. No. PCT/CN2018/085421; Filed: May 3, 2018)
Appl. No. *To Be Assigned*; Filed: *Herewith*
For: **THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES**
Inventors: TAO *et al.*
Our Ref: 4123.0190001

Commissioner:

The following documents are transmitted herewith for appropriate action by the U.S. Patent and Trademark Office:

1. Utility Patent Application Transmittal Form (PTO/AIA/15);

2. Authorization to Treat a Reply As Incorporating An Extension of Time Under 37 C.F.R. § 1.136(a)(3);

3. U.S. Utility Patent Application entitled:

   THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES

   and naming as inventors:

   Qian TAO
   Yushi HU
   Zhenyu LU
   Li Hong XIAO
   Xiaowang DAI
   Yu Ting ZHOU
   Zhao Hui TANG
   Mei Lan GUO
   ZhiWu TANG
   Qinxiang WEI
   Qianbing XU

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Micron v. YMTC
IPR2024-00909

Sha Sha LIU
Jian Hua SUN
Enbo WANG

the application consisting of:

a. An Application Data Sheet (37 C.F.R. § 1.76) (PTO/AIA/14);

b. A specification containing:

i. 31 pages of description prior to the claims;

ii. 4 pages of claims (20 claims);

iii. a one (1) page abstract;

c. 15 sheets of drawings: (*Figures 1A-1C and 2-13*);

4. An executed Power of Attorney by Applicant form (PTO/AIA/82B) and the Transmittal for Power of Attorney form (PTO/AIA/82A).

The above-listed documents are filed electronically.

Correspondence should be sent to Customer Number 26111.

This patent application is being submitted under 37 C.F.R. § 1.53(b) without Declaration and without the required fees.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

DJF/Y-G/tas
Enclosures

9714852_1.docx

Micron Ex. 1002, p. 5
Micron v. YMTC
IPR2024-00909

Electronic Acknowledgement Receipt

EFS ID:	33301095
Application Number:	16047182
International Application Number:	
Confirmation Number:	7800
Title of Invention:	THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES
First Named Inventor/Applicant Name:	Qian TAO
Customer Number:	26111
Filer:	Donald J. Featherstone
Filer Authorized By:	
Attorney Docket Number:	4123.0190001
Receipt Date:	27-JUL-2018
Filing Date:	
Time Stamp:	11:28:38
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		41230190001_Utility_Application_FILING_signed.pdf	2368256 897e0027762ccf2c0ff7fbef5743706bb32de59a	yes	71

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Power of Attorney	70	71
	Drawings-only black and white line drawings	55	69
	Abstract	54	54
	Claims	50	53
	Specification	19	49
	Application Data Sheet	6	18
	Authorization for Extension of Time all replies	5	5
	Transmittal of New Application	3	4
	Miscellaneous Incoming Letter	1	2
Warnings:			
Information:			
	Total Files Size (in bytes):	2368256	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc Code: PA..
Document Description: Power of Attorney

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Application Number	To Be Assigned
Filing Date	Herewith
First Named Inventor	Xiao Jun WANG
Title	METHODS FOR REPAIRING SUBSTRATE LATTICE AND SELECTIVE EPITAXY PROCESSING
Art Unit	To Be Assigned
Examiner Name	To Be Assigned
Attorney Docket Number	4123.0290001

SIGNATURE of Applicant or Patent Practitioner

Signature	/Donald J. Featherstone/	Date (Optional)	7/27/18
Name	Donald J. Featherstone	Registration Number	33,876
Title (if Applicant is a juristic entity)	Attorney for Applicant		
Applicant Name (if Applicant is a juristic entity)	Yangtze Memory Technologies Co., Ltd.		

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.

☑ *Total of one (1) forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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Document Description: Power of Attorney

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POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☑ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above: 26111

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

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☑ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number: 26111

OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

Yangtze Memory Technologies Co., Ltd.

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☑ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

✓ 1 **SIGNATURE of Applicant for Patent**

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature		Date (Optional)	
Name	Simon Shi-Ning Yang		
Title	CEO		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☐ Total of forms are submitted.

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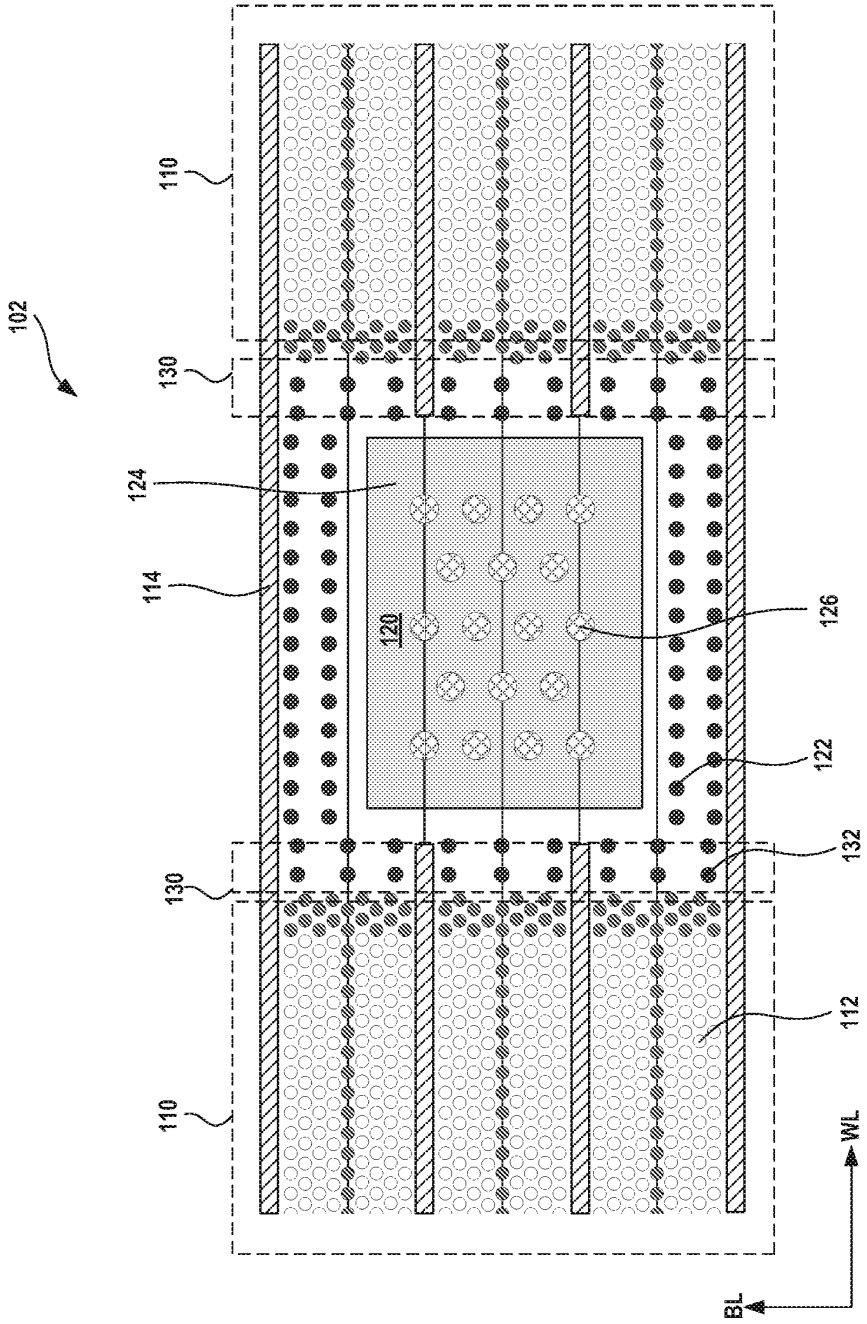

FIG. 1A

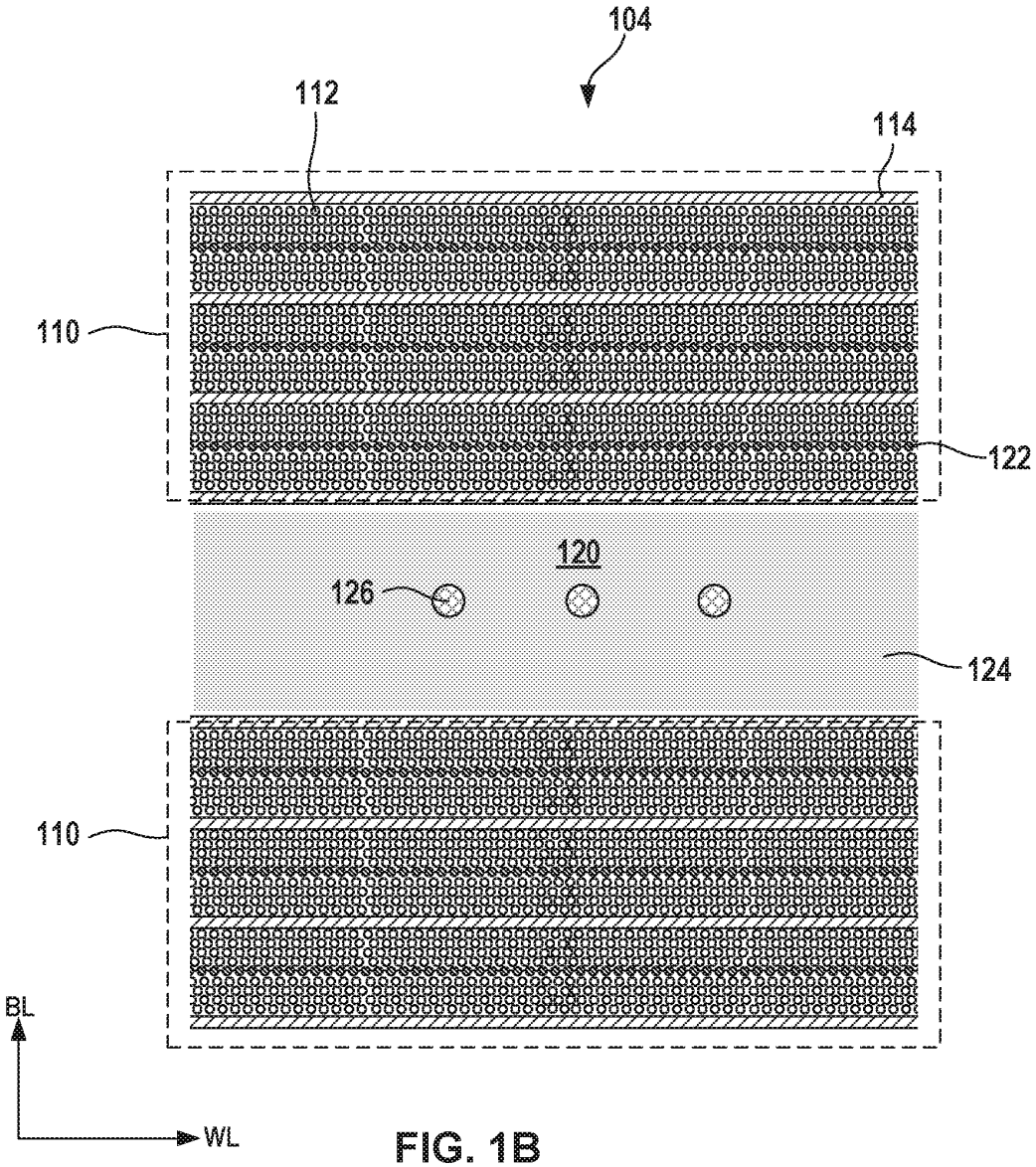

FIG. 1B

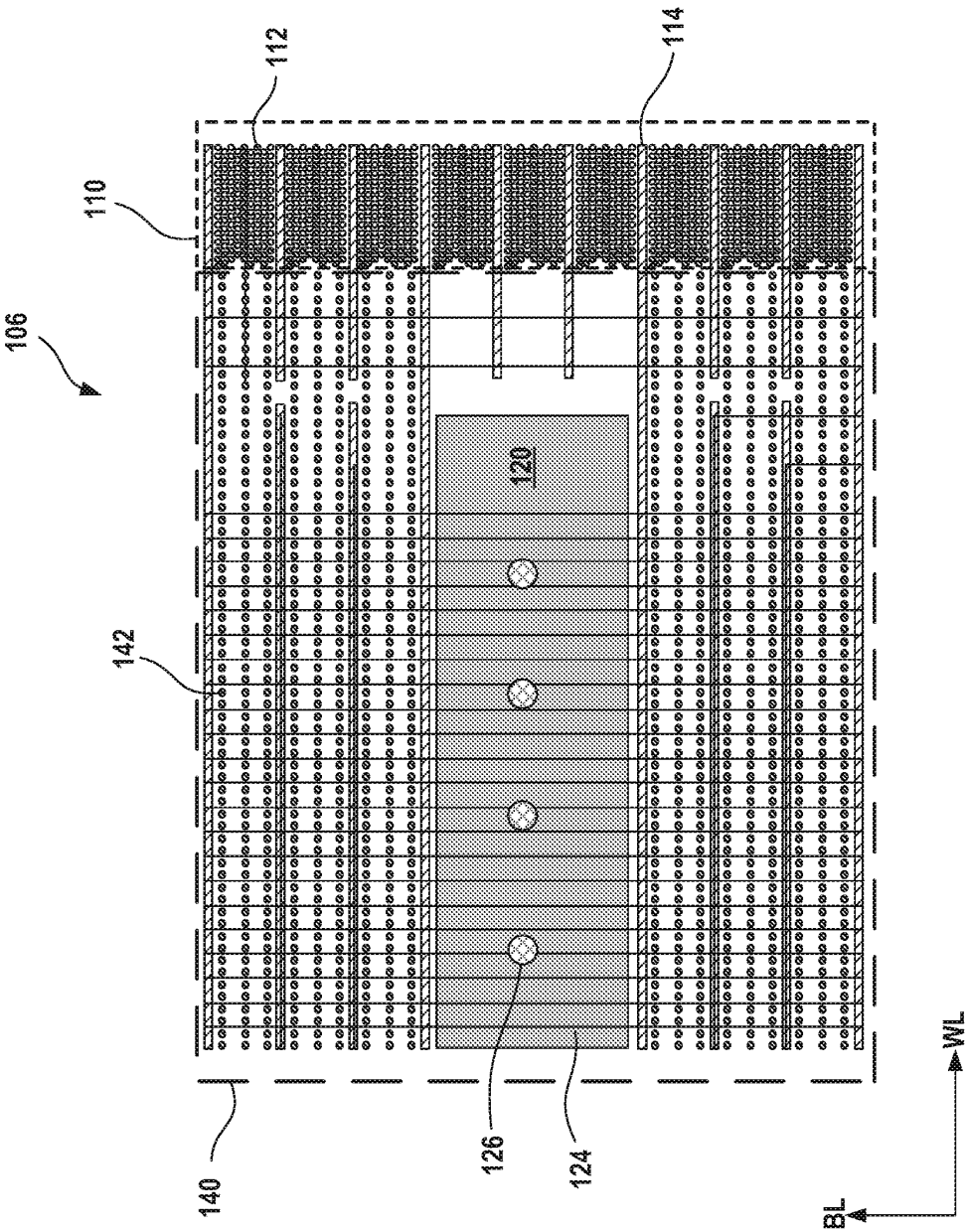

FIG. 1C

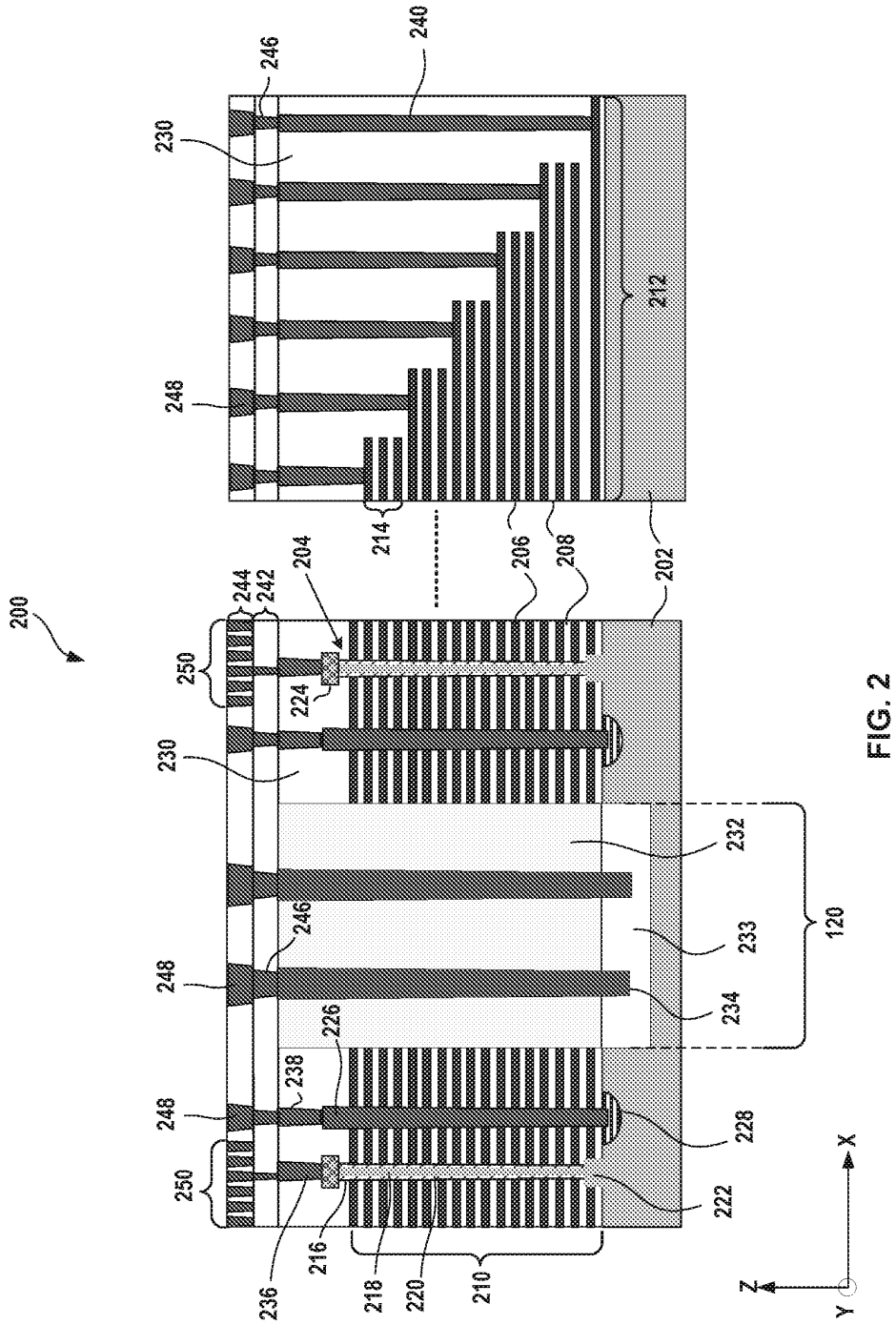
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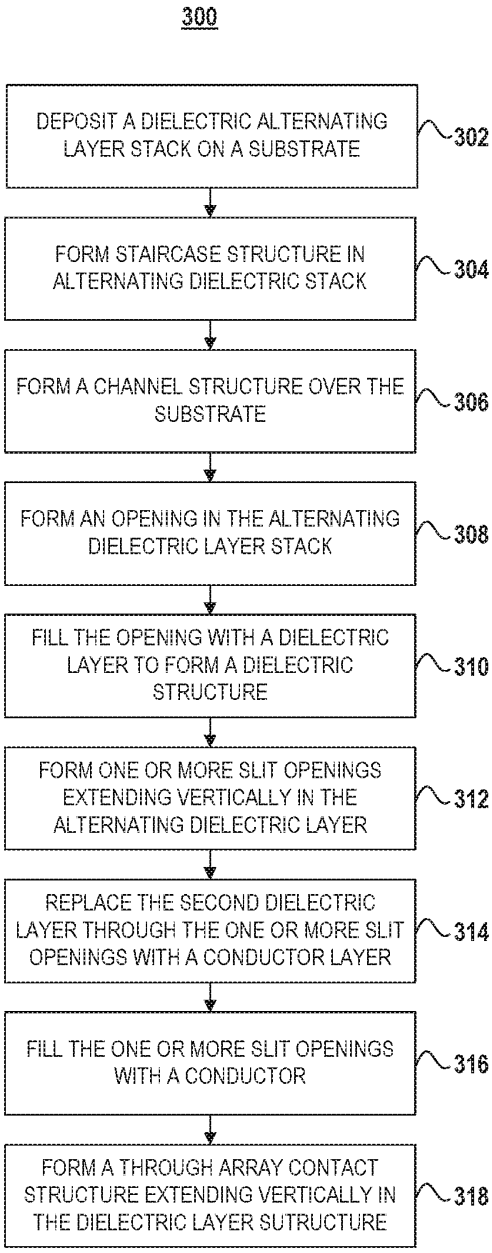
FIG. 2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DEPOSIT A DIELECTRIC ALTERNATING LAYER STACK ON A SUBSTRATE
302
FORM STAIRCASE STRUCTURE IN ALTERNATING DIELECTRIC STACK
304
FORM A CHANNEL STRUCTURE OVER THE SUBSTRATE
306
FORM AN OPENING IN THE ALTERNATING DIELECTRIC LAYER STACK
308
FILL THE OPENING WITH A DIELECTRIC LAYER TO FORM A DIELECTRIC STRUCTURE
310
FORM ONE OR MORE SLIT OPENINGS EXTENDING VERTICALLY IN THE ALTERNATING DIELECTRIC LAYER
312
REPLACE THE SECOND DIELECTRIC LAYER THROUGH THE ONE OR MORE SLIT OPENINGS WITH A CONDUCTOR LAYER
314
FILL THE ONE OR MORE SLIT OPENINGS WITH A CONDUCTOR
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FORM A THROUGH ARRAY CONTACT STRUCTURE EXTENDING VERTICALLY IN THE DIELECTRIC LAYER SUTRUCTURE
318

FIG. 3

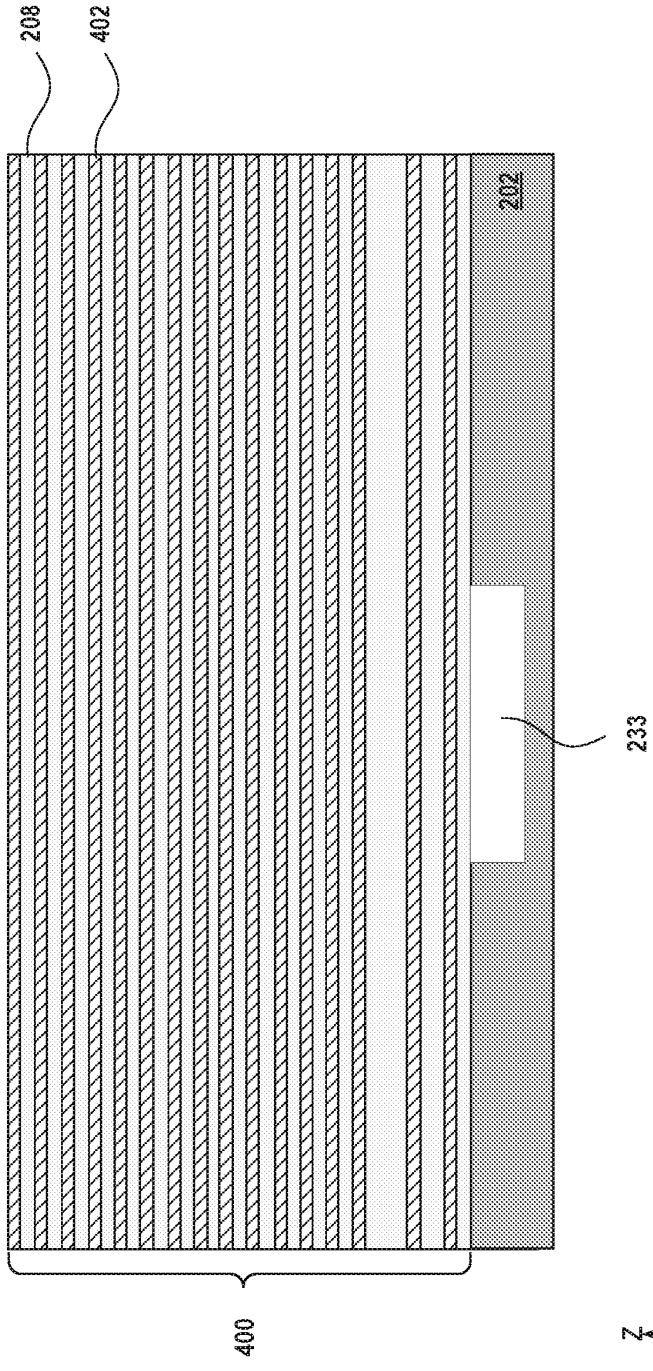

FIG. 4

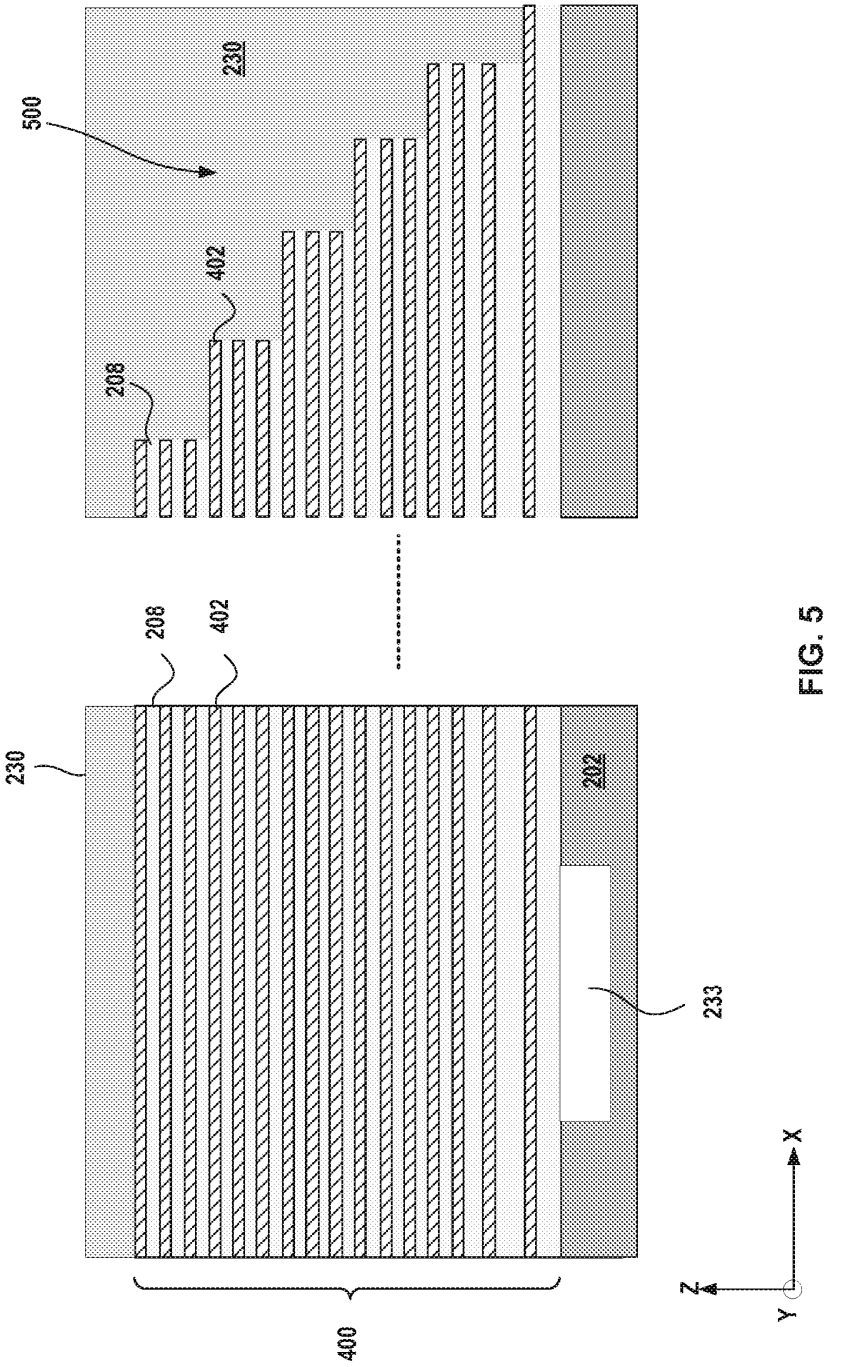

FIG. 5

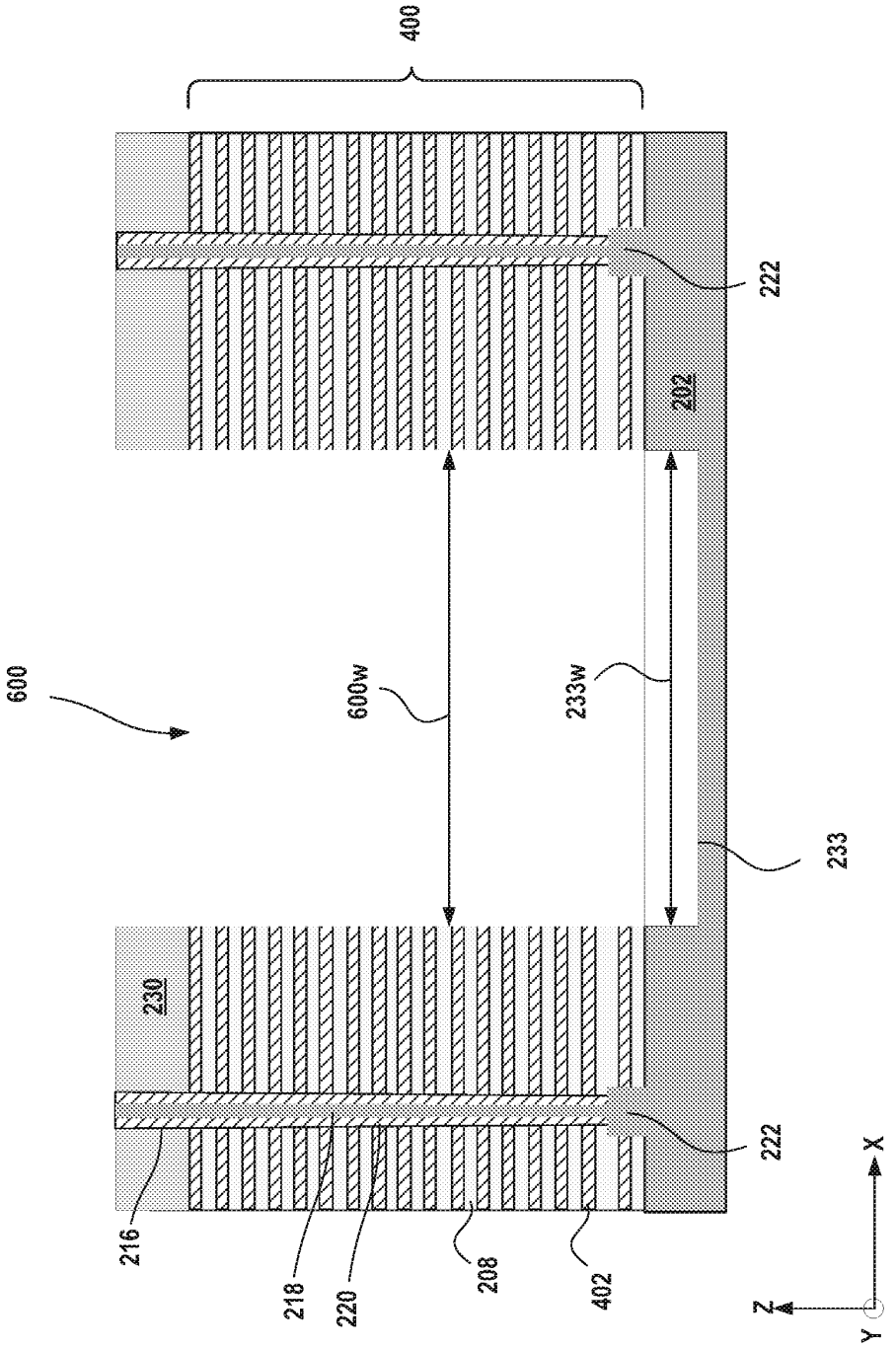

FIG. 6

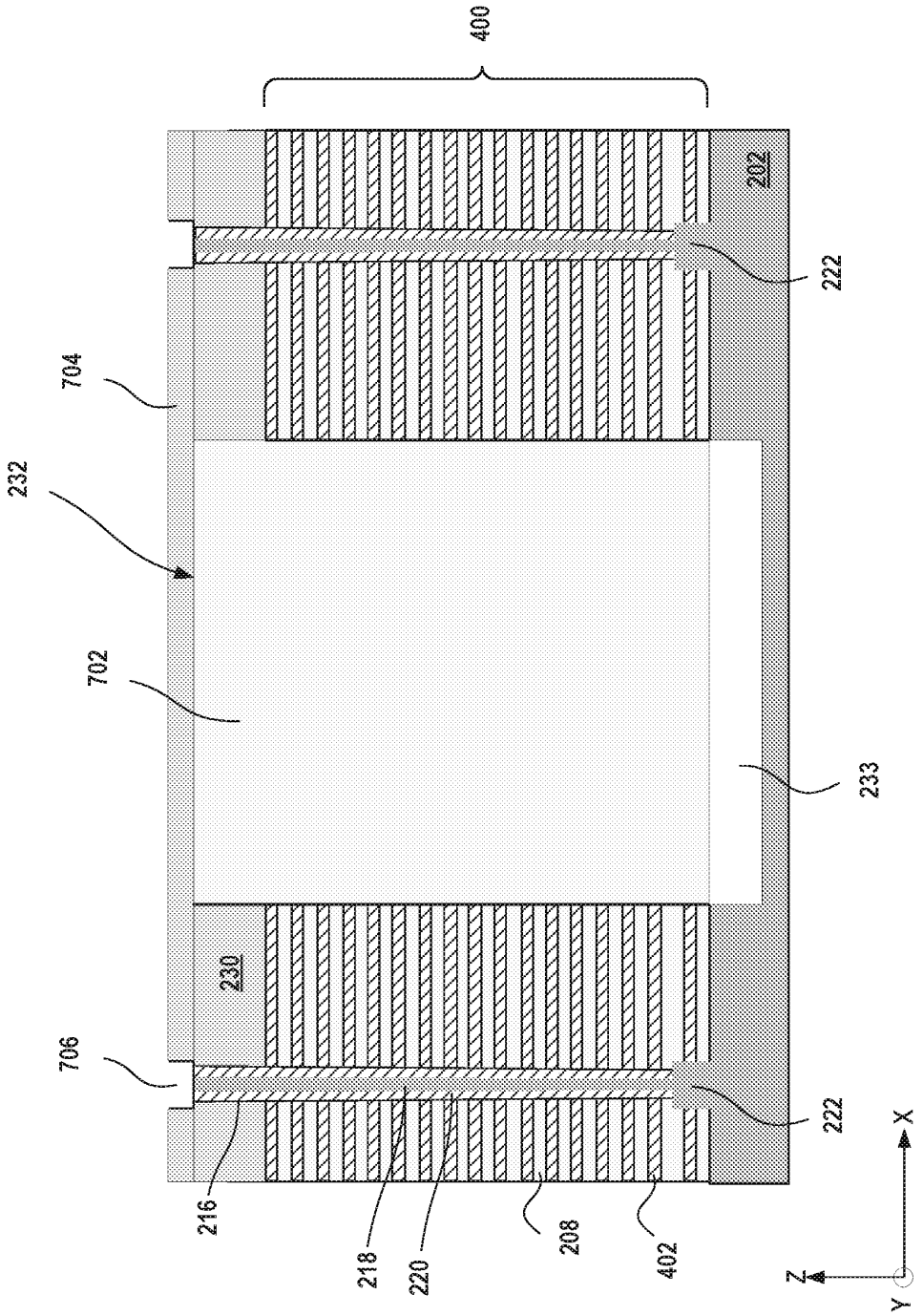

FIG. 7

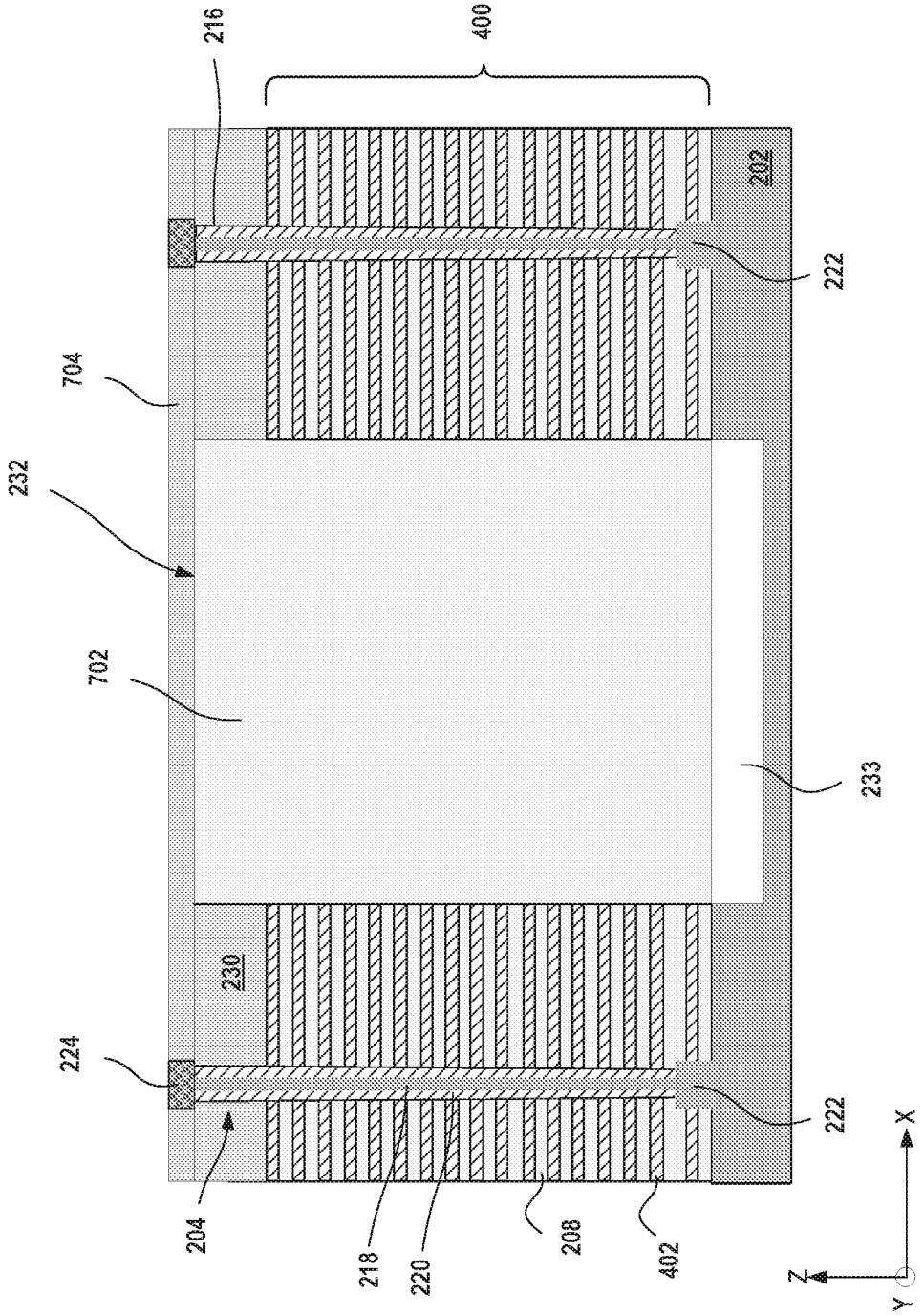
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FIG. 8

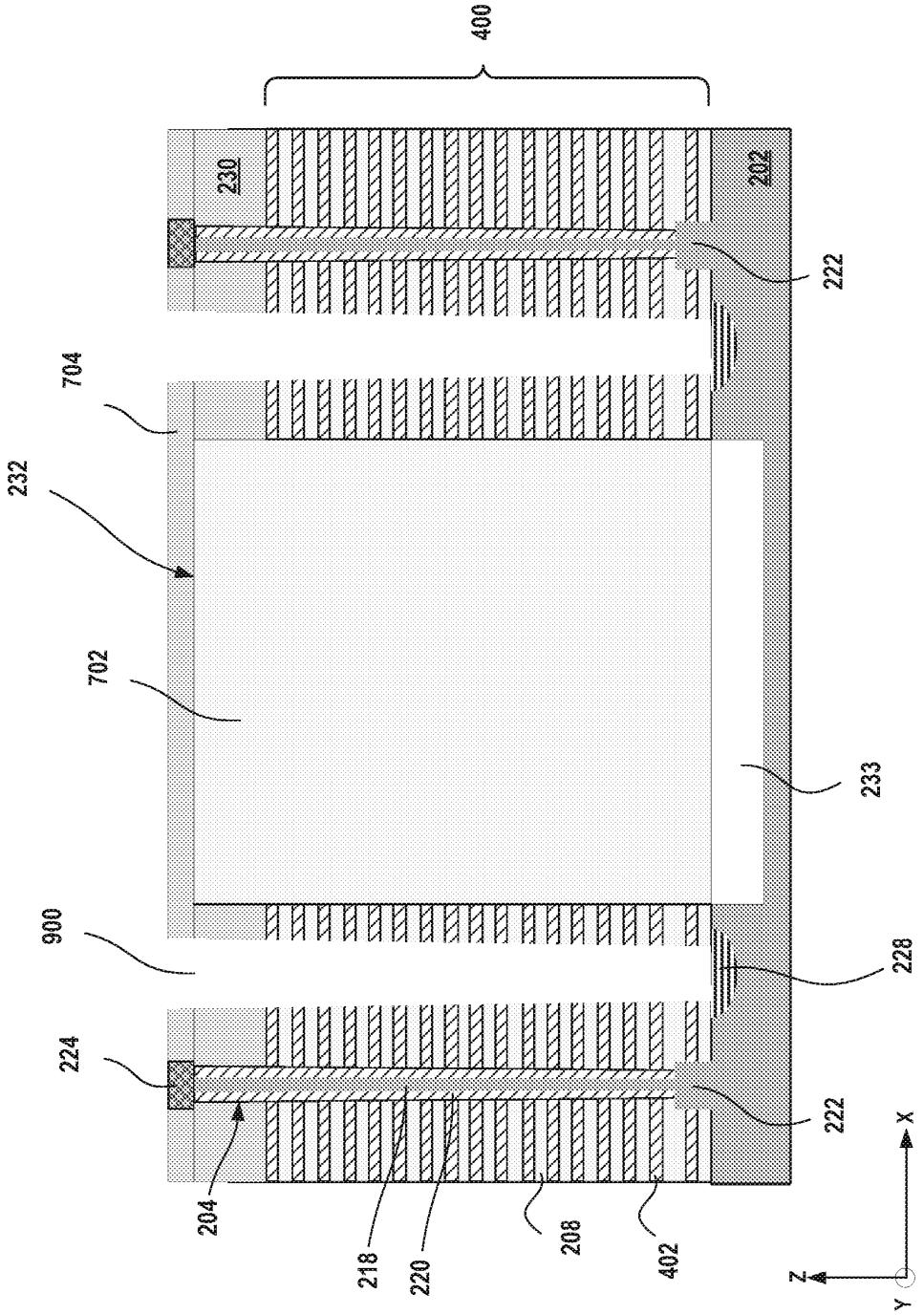
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FIG. 9

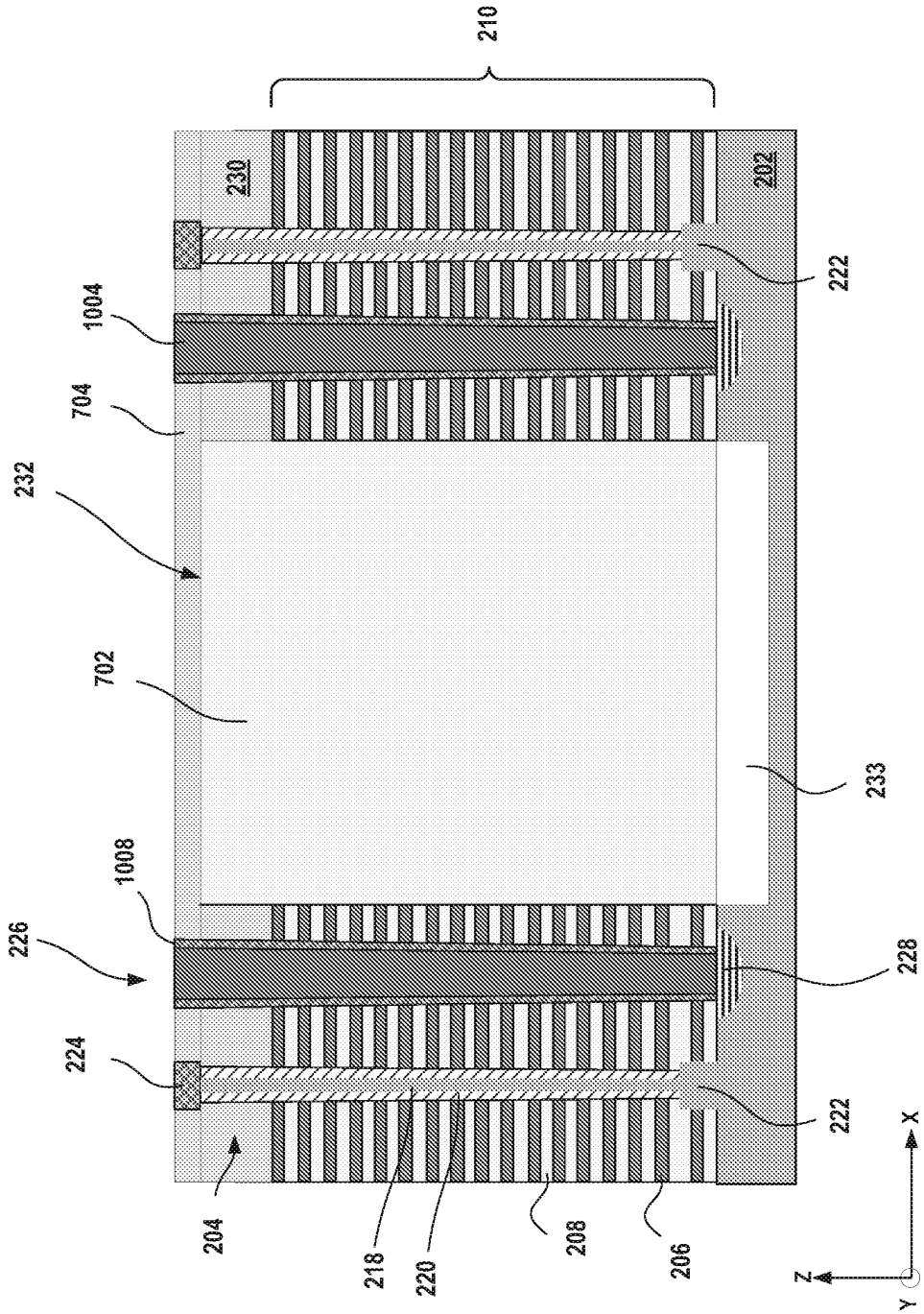
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FIG. 10

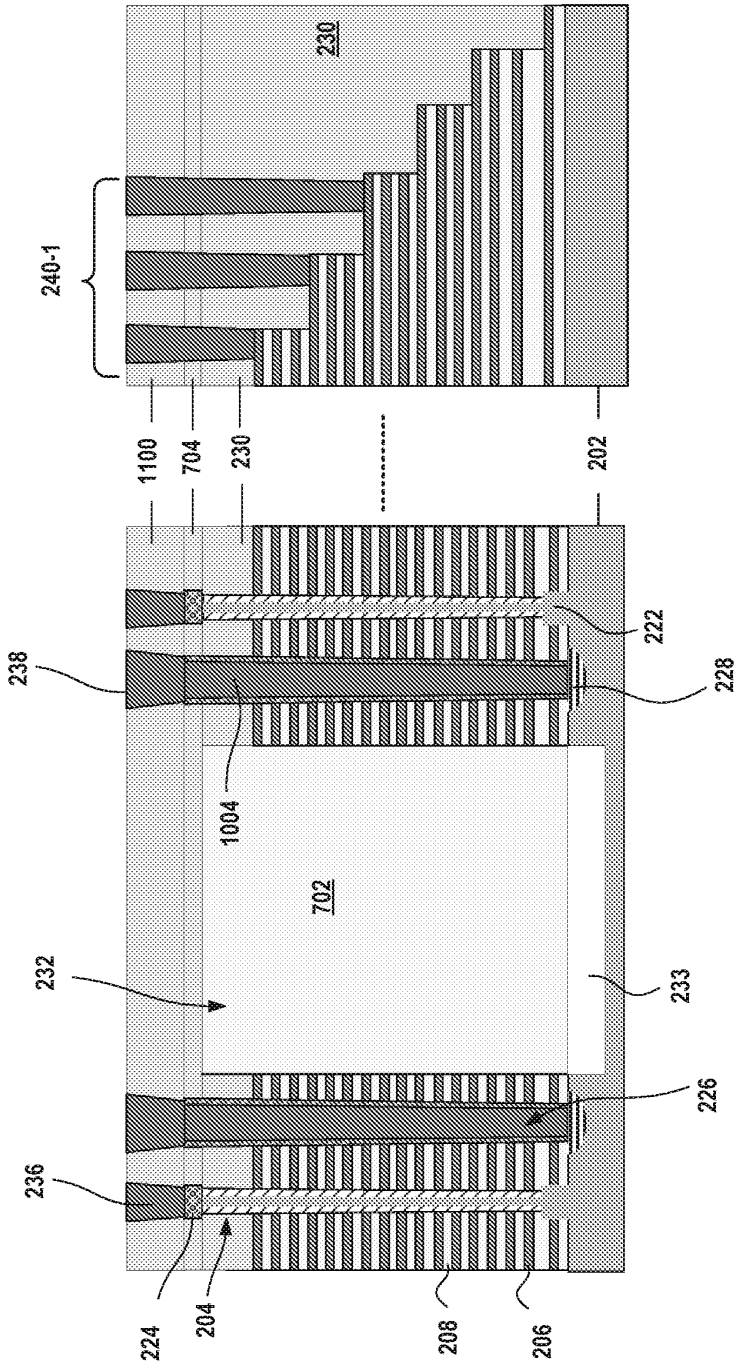
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FIG. 11

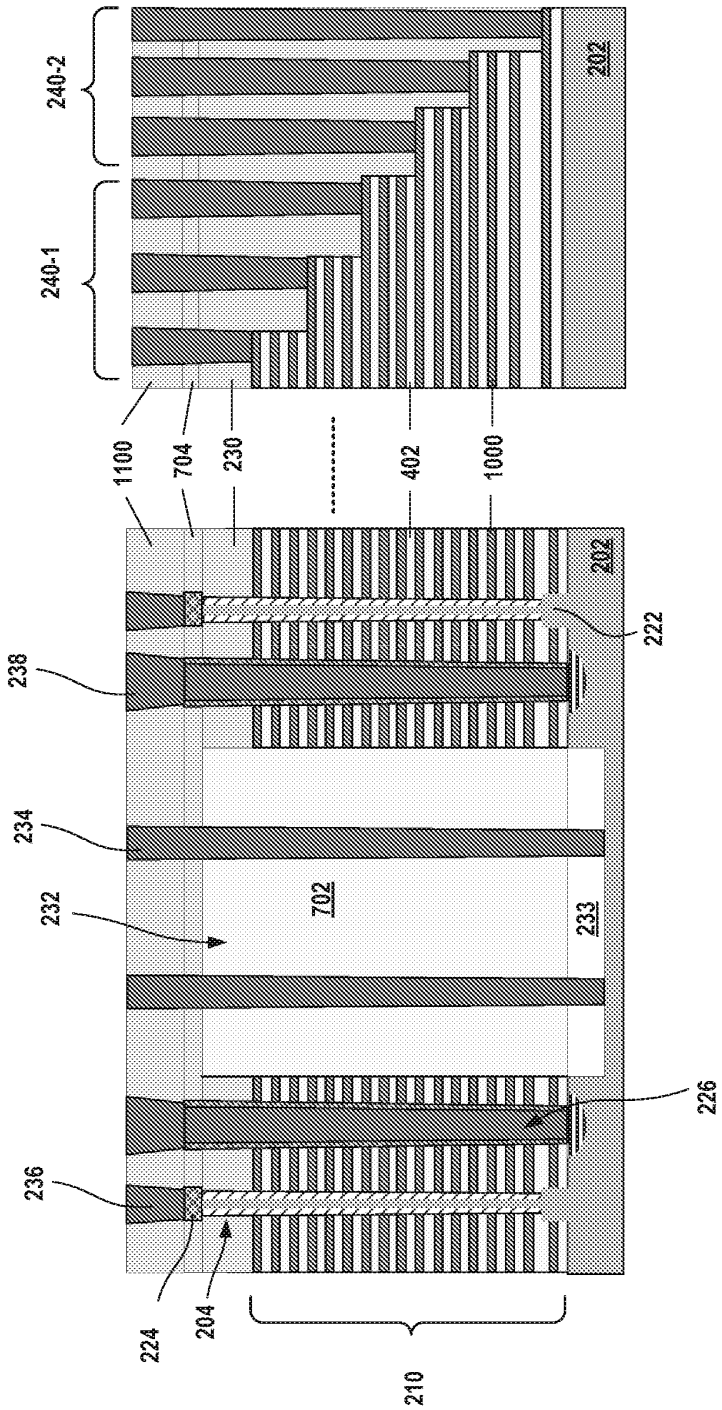
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FIG. 12

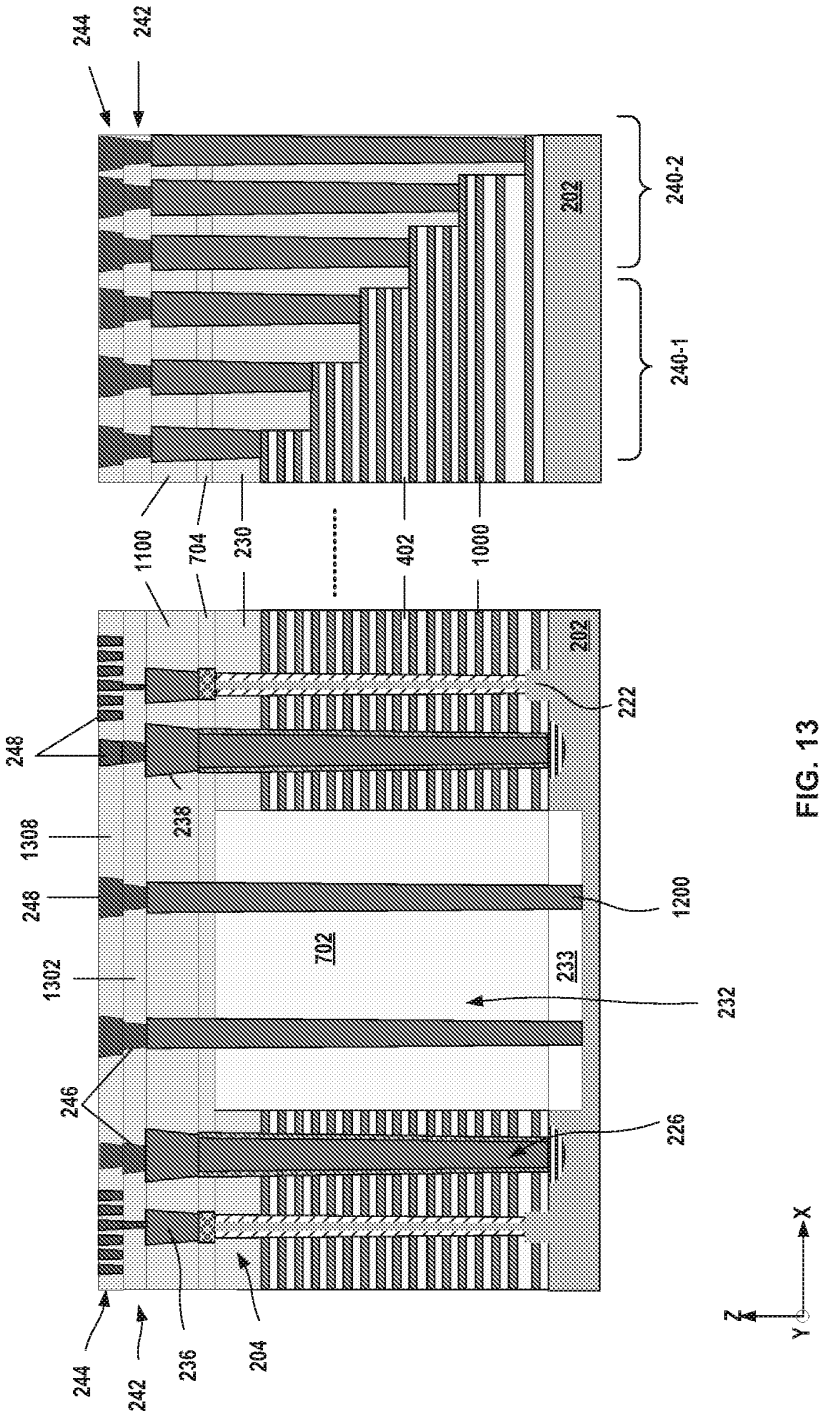
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FIG. 13

ABSTRACT

Embodiments of interconnect structures of a three-dimensional (3D) memory device and method for forming the interconnect structures are disclosed. In an example, a 3D NAND memory device includes a semiconductor substrate, an alternating layer stack disposed on the semiconductor substrate, and a dielectric structure, which extends vertically through the alternating layer stack, on an isolation region of the substrate. Further, the alternating layer stack abuts a sidewall surface of the dielectric structure and the dielectric structure is formed of a dielectric material. The 3D memory device additionally includes one or more through array contacts that extend vertically through the dielectric structure and the isolation region, and one or more channel structures that extend vertically through the alternating layer stack.

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WHAT IS CLAIMED IS:

1. A three-dimensional (3D) memory device, comprising:

a semiconductor substrate;

an alternating layer stack disposed on the semiconductor substrate;

a dielectric structure on an isolation region of the substrate and extending vertically through the alternating layer stack, wherein the alternating layer stack abuts a sidewall surface of the dielectric structure and the dielectric structure is formed of a dielectric material;

one or more through array contacts (TACs) extending vertically through the dielectric structure and the isolation region; and

one or more channel structures extending vertically through the alternating layer stack.

2. The 3D memory device of claim 1, further comprising:

an epitaxial layer formed between each of the one or more channel structures and the semiconductor substrate;

an etch stop plug disposed on each of the one or more channel structures;

a staircase structure disposed in the alternating layer; and

one or more contact layers disposed on the one or more TACs, channel structures, and slit structures.

3. The 3D memory device of claim 1, wherein the dielectric structure abuts a sidewall surface of the TACs.

4. The 3D memory device of claims 1 or 2, wherein the 3D memory device is a NAND 3D memory device.

5. The 3D memory device of claim 1, wherein the alternating layer stack comprises alternating pairs of a dielectric and a conductor layer.

6. The 3D memory device of claims 1, wherein the dielectric material is silicon oxide.

7. The 3D memory device of claims 1 or 3, wherein the dielectric structure comprises an oxide.

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8. The 3D memory device of claim 1, wherein the dielectric structure defines a through array contact region within the 3D memory device.

9. The 3D memory device of claim 1, wherein the dielectric structure has a footprint equal to or smaller than the isolation region.

10. A method for forming a 3D memory device, the method comprising:

forming an isolation structure on a substrate;

disposing an alternating dielectric layer stack on the substrate, the alternating dielectric layer stack comprising pairs of a first dielectric layer and a second dielectric layer different from the first dielectric layer;

forming a channel structure extending vertically in the alternating dielectric layer stack;

forming an opening in the alternating dielectric layer stack, wherein the opening exposes the isolation structure;

filling the opening with a dielectric layer to form a dielectric structure as a through array contact (TAC) region of the 3D memory device;

removing portions of the dielectric structure and the isolation structure until the substrate is exposed to form a TAC opening that vertically extends through the dielectric structure and the isolation structure; and

filling the TAC opening with a conductor to form a TAC structure in the TAC region, wherein the TAC structure is in contact with the substrate.

11. The method of claim 10, wherein before forming the TAC opening the method further comprises:

forming slit openings extending vertically in the alternating dielectric layer stack, wherein the slit openings expose a doped region of the substrate;

replacing the second dielectric layer through the one or more slit openings with a conductor layer to convert the alternating dielectric layer stack to an alternating dielectric/conductor layer stack; and

filling the one or more slit openings with a conductor to form one or more slit structures extending vertically in the alternating dielectric/conductor layer stack.

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12. The method of claim 10, wherein before forming the channel structure performing a trim-etch process to form a staircase structure in the alternating dielectric layer stack.

13. The method of claim 10, wherein filling the opening with the dielectric layer comprises depositing the dielectric layer with a chemical vapor deposition, a plasma-enhanced chemical vapor deposition, or a physical vapor deposition process.

14. The method of claim 10, wherein filling the opening with the dielectric layer comprises forming an oxide.

15. The method of claim 10, wherein the first dielectric layer comprises an oxide and the second dielectric layer comprises a nitride.

16. A three-dimensional (3D) memory device, comprising:

a substrate with an isolation structure;

an alternating conductor/dielectric layer stack disposed on the substrate;

a dielectric structure on the isolation structure and extending vertically through the alternating conductor/dielectric layer stack, wherein the alternating conductor/dielectric layer stack abuts a sidewall surface of the dielectric structure and the dielectric structure is formed of a dielectric material;

channel structures extending vertically through the alternating conductor/dielectric layer stack; and

through array contacts (TAC) extending vertically through the dielectric and the isolation structures.

17. The 3D memory device of claim 16, further comprising:

a staircase structure disposed in the alternating conductor/dielectric layer stack, wherein the staircase structures comprises levels with each level having a conductor layer thereon;

a word line contact disposed on each conductor layer of the staircase structure; and

a local contact disposed on each channel structure and slit structure.

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18. The 3D memory device of claim 16, wherein the dielectric structure abuts a sidewall of the each TAC.

19. The 3D memory device of claim 16, wherein the dielectric structure comprises a through array contact region of the 3D memory device.

20. The 3D memory device of claim 16, further comprising:
an etch stop plug interposed between each local contact and each channel structure; and
an epitaxial layer disposed between each channel structure and the substrate.

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THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES

CROSS-REFERENCES TO RELATED APPLICATIONS

[0001] This application claims the priority of PCT Patent Application No. PCT/CN2018/085421 filed on May 3, 2018, the entire content of which is incorporated herein by reference.

TECHNICAL FIELD

[0001] The present disclosure generally relates to the field of semiconductor technology, and more particularly, to a channel hole plug structure of three-dimensional (3D) memory devices and a method for forming the same.

BACKGROUND

[0002] Planar memory cells have been continuously scaled down from one technology generation to the next by improvements in circuit design, fabrication integration, and fabrication process. However, as the feature sizes of the memory cells continuously shrink, the density for planar memory cells increases. Consequently, the fabrication techniques can become challenging and costly.

[0003] A three-dimensional (3D) memory architecture (e.g., planar memory cells stacked on top of each other) can address the density limitation of planar memory cells. The 3D memory architecture includes a memory array and peripheral devices for controlling signals to and from the memory array.

BRIEF SUMMARY

[0004] Embodiments of 3D memory and fabrication methods thereof are disclosed herein.

[0005] According to some embodiments of the present disclosure, a 3D NAND memory device includes an alternating layer stack with a staircase structure and one or more dielectric structures surrounded by the alternating layer stack. The alternating layer stack can include a stack of alternating conductor and dielectric layers, and the dielectric structures can include a single dielectric layer. The memory device further includes multiple vertical structures that extend vertically through the alternating conductor/dielectric stack, and multiple vertical structures that

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extend vertically through the dielectric structures. By way of example and not limitation, vertical structures extending vertically through the alternating conductor/dielectric stack can include "channel" structures and "slit" structures. Vertical structures extending vertically through the dielectric structures can include through array contact structures, referred to herein as "through array contacts" ("TAC" structures or "TACs").

[0006] Additional elements of the 3D NAND memory device can include an etch stop layer disposed on each channel structure and a first contact layer with a plurality of first contacts. For example, each of the first contacts can be formed to physically connect to a respective conductor layer from each alternating conductor/dielectric stack in the staircase structure, a respective etch stop layer of the channel structures, and a respective slit structure.

[0007] In some embodiments, the etch stop layer includes polysilicon (e.g., polycrystalline silicon or "poly"), titanium (Ti), titanium nitride (TiN), tungsten (W), or combinations thereof. Further each of the plurality of conductor/dielectric layer pairs can include a metal and a silicon oxide (SiO_2) layer. The aforementioned materials are exemplary and are not limiting. As such, other appropriate materials can be used.

[0008] In some embodiments, the memory device includes dummy (e.g., electrically non-functional) channel structures extending vertically through the alternating conductor/dielectric stack.

[0009] In some embodiments, the memory device includes a second contact layer over the first contact layer and a third contact layer over the second contact layer. The second and third contact layers include respective second and third contacts. Some contacts of the third contact layer, via the respective second and first contacts, are electrically connected to the conductor layers from the alternating conductor/dielectric stack in the staircase structure, and to the channel and slit structures. In some embodiments, the first, second and third contact layers form an interconnect network for the 3D NAND memory device. The interconnect network can be used to transfer electrical signals between the various components of the 3D NAND memory device.

[0010] According to some embodiments of the present disclosure, a method for forming a 3D NAND memory device is disclosed herein. For example, an alternating dielectric stack can be formed over a substrate. The alternating dielectric stack can include a plurality of dielectric layer pairs, where each pair includes a first dielectric layer and a second dielectric layer different from the first dielectric layer. A first staircase structure can be subsequently formed in the alternating

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dielectric stack. Subsequently, channel structures and a dielectric structure—each extending vertically through the alternating dielectric stack—are formed.

[0011] In some embodiments, the dielectric material of the dielectric structure can be the same as the material of the second dielectric layer in the alternating dielectric stack. A sacrificial etch stop layer can be disposed on each channel structure. Slit openings extending through the alternating dielectric stack are subsequently formed and the first dielectric layers of the alternating dielectric stack are replaced with conductor layers through the slit openings to form a plurality of conductor/dielectric layer pairs. The slit openings are then filled with a conductor material. Further, a first contact layer with a plurality of first contacts can be formed so that each first conductor layer from the alternating conductor/dielectric stack in the first staircase structure is connected to a first contact. Additionally, each channel and slit structure can also be connected to a respective first contact of the first contact layer. In some embodiments, and prior to the formation of the first contact layer, the sacrificial etch stop layer over each channel structure can be replaced with a "permanent" etch stop layer.

[0012] In some embodiments, TAC openings are etched through the dielectric structure and subsequently filled with a metal to form respective TAC structures that extend through the dielectric structure and a portion of the substrate. In some embodiments, TAC structures are part of the first contact layer. In other words, the TAC structures can be formed concurrently with the first contact layer.

[0013] In some embodiments, a second contact layer with a plurality of second contacts can be formed over the first contact layer. Second contacts can be connected to respective first contacts of the first contact layer.

[0014] In some embodiments, a third contact layer with a plurality of third contacts can be formed over the second contact layer. The third contact layer, via the respective second and first contact layers, can electrically connect to the various components of the memory device including the first conductor layers of the alternating conductor/dielectric stack in the first staircase structure, the channel structures, and the slit structures.

[0015] In some embodiments, prior to forming the slit structure, a doped region can be formed in the substrate. The slit structure can be in contact with the doped region.

[0016] In some embodiments, the permanent etch stop layer includes one or more of polysilicon, titanium, titanium nitride, and tungsten. The dielectric structure can include silicon

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oxide. Each of the plurality of dielectric layer pairs can include a silicon oxide layer and a silicon nitride layer. Each of the plurality of conductor/dielectric layer pairs can include a metal layer and a silicon oxide layer.

[0017] Further features and advantages of the invention, as well as the structure and operation of various embodiments of the invention, are described in detail below with reference to the accompanying drawings. It is noted that the invention is not limited to the specific embodiments described herein. Such embodiments are presented herein for illustrative purposes only. Additional embodiments will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] The accompanying drawings, which are incorporated herein and form a part of the specification, illustrate embodiments of the present disclosure and, together with the description, further serve to explain the principles of the present disclosure and to enable a person skilled in the pertinent art to make and use the present disclosure.

[0019] FIGs. 1A-1C illustrate various regions of a 3D memory device in the plan-view, according to some embodiments of the present disclosure.

[0020] FIG. 2 illustrates a cross-section of a 3D memory device, according to some embodiments of the present disclosure.

[0021] FIG. 3 is a flowchart of an exemplary method for forming a 3D memory device, according to some embodiments of the present disclosure.

[0022] FIGs. 4–13 illustrate an exemplary fabrication process for forming a 3D memory device, according to some embodiments of the present disclosure.

[0023] The features and advantages of the present disclosure will become more apparent from the detailed description set forth below when taken in conjunction with the drawings, in which like reference characters identify corresponding elements throughout. In the drawings, like reference numbers generally indicate identical, functionally similar, and/or structurally similar elements. Additionally, generally, the left-most digit(s) of a reference number identifies the drawing in which the reference number first appears. Unless otherwise indicated, the drawings provided throughout the disclosure should not be interpreted as to-scale drawings.

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DETAILED DESCRIPTION

[0024] Although specific configurations and arrangements are discussed, it should be understood that this is done for illustrative purposes only. A person skilled in the art will recognize that other configurations and arrangements can be used without departing from the spirit and scope of the present disclosure. It will be apparent to a person skilled in the art that the present disclosure can also be employed in a variety of other applications.

[0025] It is noted that references in the specification to "one embodiment," "an embodiment," "an example embodiment," "some embodiments," etc., indicate that the embodiment described may include a particular feature, structure, or characteristic, but every embodiment may not necessarily include the particular feature, structure, or characteristic. Moreover, such phrases do not necessarily refer to the same embodiment. Further, when a particular feature, structure or characteristic is described in connection with an embodiment, it would be within the knowledge of a person skilled in the art to affect such feature, structure or characteristic in connection with other embodiments whether or not explicitly described.

[0026] In general, terminology may be understood at least in part from usage in context. For example, the term "one or more" as used herein, depending at least in part upon context, may be used to describe any feature, structure, or characteristic in a singular sense or may be used to describe combinations of features, structures or characteristics in a plural sense. Similarly, terms, such as "a," "an," or "the," again, may be understood to convey a singular usage or to convey a plural usage, depending at least in part upon context.

[0027] It should be readily understood that the meaning of "on," "above," and "over" in the present disclosure should be interpreted in the broadest manner such that "on" not only means "directly on" something but also includes the meaning of "on" something with an intermediate feature or a layer therebetween, and that "above" or "over" not only means the meaning of "above" or "over" something but can also include the meaning it is "above" or "over" something with no intermediate feature or layer therebetween (i.e., directly on something).

[0028] Further, spatially relative terms, such as "beneath," "below," "lower," "above," "upper," and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented

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(rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.

[0029] As used herein, the term "substrate" refers to a material onto which subsequent material layers are added, or otherwise "disposed." The substrate itself can be patterned. Materials disposed on (e.g., on top) the substrate can be patterned or can remain unpatterned. Furthermore, the substrate can include a wide array of semiconductor materials, such as silicon, germanium, gallium arsenide, indium phosphide, etc. Alternatively, the substrate can be made from an electrically non-conductive material, such as a glass, a plastic, or a sapphire wafer.

[0030] As used herein, the term "layer" refers to a material portion including a region with a thickness. A layer can extend over the entirety of an underlying or overlying structure, or may have an extent less than the extent of an underlying or overlying structure. Further, a layer can be a region of a homogeneous or inhomogeneous continuous structure that has a thickness less than the thickness of the continuous structure. For example, a layer can be located between any pair of horizontal planes between, or at, a top surface and a bottom surface of the continuous structure. As used herein, the term "top surface" or "front side" of a structure, a layer, or an element refers to a surface where subsequent elements or structures can be formed thereon. Conversely, as used herein, the term "bottom surface" or "backside" refers to the side of the structure, layer, or element that is opposite to the top surface. It is noted that the terms "top surface" or "front side" and "bottom surface" or "backside" are used merely for description purposes and not to limit the orientation of the elements, layers, or structures. A layer can extend horizontally, vertically, and/or along a tapered surface. A substrate can be a layer, can include one or more layers therein, and/or can have one or more layer thereupon, thereabove, and/or therebelow. A layer can include multiple layers. For example, an interconnect layer can include one or more conductor and contact layers (in which contacts, interconnect lines, and/or vias are formed) and one or more dielectric layers.

[0031] As used herein, the term "nominal/nominally" refers to a desired, or target, value of a characteristic or parameter for a component or a process operation, set during the design phase of a product or a process, together with a range of values above and/or below the desired value. The range of values can be due to slight variations in manufacturing processes or tolerances. As used herein, the term "about" indicates the value of a given quantity that can vary based on a particular technology node associated with the subject semiconductor device. Based on the particular

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technology node, the term "about" can indicate a value of a given quantity that varies within, for example, 10–30% of the value (e.g., ±10%, ±20%, or ±30% of the value).

[0032] As used herein, the term "3D memory device" refers to a semiconductor device with vertically-oriented strings of memory cell transistors (referred to herein as "memory strings," such as NAND strings) on a laterally-oriented substrate so that the memory strings extend in the vertical direction with respect to the substrate. As used herein, the term "vertical/vertically" means nominally perpendicular to the lateral surface of a substrate.

[0033] Various embodiments in accordance with the present disclosure provide a 3D memory device with interconnect structures for a memory array (also referred to herein as an "array device"). The interconnect structures allow contacts to various memory array structures (e.g., NAND strings, gate line slits, word lines, etc.) to be fabricated in a limited number of steps (e.g., in a single step or in two steps), thereby reducing the process complexity and manufacturing cost. In some embodiments, the interconnect structures disclosed herein include bit lines in the top interconnect layer, which are suitable for those 3D memory architectures where the array device and a peripheral device are formed on different substrates and are subsequently joined by hybrid bonding in a "face-to-face" configuration.

[0034] Moreover, the interconnect structures disclosed herein can include TAC structures for providing vertical interconnects between the stacked array device and a peripheral device (e.g., for power bus and metal routing), thereby reducing metal levels and shrinking die size. In some embodiments, the TAC structures, as part of the interconnect structures, are formed within "single-material" dielectric structures (e.g., dielectric structures that are made of a single dielectric as opposed to a stack of alternating dielectric layers). According to some embodiment, forming TAC structures in a single-material dielectric structure is advantageous compared to the formation of TAC structures in a stack of alternating dielectric layers in terms of etching capability and cost.

[0035] According to some embodiments, FIGs. 1A-1C are plan-views of various exemplary regions of a 3D memory device along a bit line (BL) and a word line (WL) direction as denoted by respective axes labeled BL and WL. For example, FIG. 1A is a plan-view of an exemplary WL TAC region 102 of the 3D memory device. TAC region 102 includes NAND string regions 110, a TAC region 120, and top selective gate (TSG) staircase regions 130. NAND string regions 110 can include an array of NAND strings 112, each including a plurality of stacked memory

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cells. TSG staircase regions 130 can be disposed on the sides of NAND string regions 110 and adjacent to TAC region 120 in the plan-view. TSG staircase regions 130 can include an array of TSG contacts 132 formed on a staircase structure having two levels or more. TSG contacts 132 can be electrically connected to the top selective gates of NAND strings 112 in NAND string region 110 through a network of interconnect contacts not shown in FIG. 1A.

[0036] In some embodiments, TAC region 120 is between two TSG staircase regions 130 in the WL direction of the 3D memory device. TAC region 120 can be defined by a single-material dielectric structure 124. Multiple TAC structures 126 can be formed within TAC region 120 in dielectric structure 124. In some embodiments, dummy (e.g., non-electrically functional) channel structures 122 are formed outside TAC region 120 to provide mechanical support to the memory array structures. By way of example and not limitation, dummy channel structures 122 can be formed in any regions outside TAC region 120, for example, along the edges of NAND string regions 110 adjacent to TSG staircase regions 130. As shown in FIG. 1A, WL TAC region 102 can also include a plurality of slit structures 114 with each extending in the WL direction. At least some slit structures 114 can function as the common source contact for an array of NAND strings 112 in NAND string regions 110. According to some embodiments, slit structures 114 can divide the 3D memory device into multiple memory blocks.

[0037] FIG. 1B is a plan-view of an exemplary bit line (BL) TAC region 104 of the 3D memory device, including NAND string regions 110 and a TAC region 120. NAND string regions 110 can include an array of NAND strings 112, each including a plurality of stacked memory cells. In some embodiments, TAC region 120 is disposed between two NAND string regions 110 in the bit line direction of the 3D memory device (labeled as "BL" in FIGs. 1A-1C). TAC region 120 can be defined by a single-material dielectric structure 124. More than one TAC structures 126 can be formed in TAC region 120 within dielectric structure 124, as shown in FIG. 1B. Further, BL TAC region 104 can also include slit structures 114 with each extending in the WL direction. At least some slit structures 114 can function as the common source contact for an array of NAND strings 112 in NAND string regions 110. Slit structures 114 can also divide the 3D memory device into multiple memory blocks. In some embodiments, dummy (e.g., non-electrically functional) channel structures 122 are formed in part of NAND string regions 110, for example, in the memory areas that are adjacent to TAC region 120 in the bit line direction.

[0038] FIG. 1C is a plan-view of an exemplary staircase TAC region 106 of the 3D memory device, including a NAND string region 110, a staircase region 140, and a TAC region 120.

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NAND string region 110 can include an array of NAND strings 112, each including a plurality of stacked memory cells. Staircase region 140 can include a staircase structure and an array of WL contacts 142 formed on the staircase structure. In some embodiments, TAC region 120 can be formed in staircase region 140. TAC region 120 is defined by the single-material dielectric structure 124. Multiple TAC structures 126 can be formed within TAC region 120 in single-material dielectric structure 124. As shown in FIG. 1C, staircase TAC region 106 can also include slit structures 114 with each extending in the WL direction. At least some slit structures 114 can function as the common source contact for an array of NAND strings 112 in NAND string region 110. Slit structures 114 can also divide the memory device into multiple memory blocks. In some embodiments, dummy (e.g., non-electrically functional) channel structures are formed in staircase region 140 outside TAC region 120 (not shown in FIG. 1C).

[0039] FIG. 2 is a cross-sectional view of an exemplary 3D memory device 200, according to some embodiments of the present disclosure. 3D memory device 200 can include a substrate 202. Substrate 202 can include single crystalline silicon (Si) or another elementary semiconductor such as, for example, (i) germanium (Ge); (ii) a compound semiconductor including silicon germanium (SiGe), silicon carbide (SiC), gallium arsenide (GaAs), gallium phosphide (GaP), indium phosphide(InP), indium arsenide (InAs), and/or indium antimonide (InSb); (iii) an alloy semiconductor including gallium arsenide phosphide (GaAsP), aluminum indium arsenide (AlInAs), aluminum gallium arsenide (AlGaAs), gallium indium arsenide (GaInAs), gallium indium phosphide (GaInP), and/or gallium indium arsenide phosphide (GaInAsP); or (iv) combinations thereof. Further, substrate 202 can be a "semiconductor-on-insulator" wafer, such as silicon on insulator (SOI) or germanium on insulator (GOI). For example purposes, substrate 202 will be described in the context of single crystalline Si (e.g., a Si wafer). Based on the disclosure herein, other materials, as discussed above, can be used. These materials are within the spirit and scope of this disclosure. In some embodiments, substrate 202 can be a thinned substrate, which was thinned by means of grinding, wet and/or dry etching, chemical mechanical planarization (CMP), or a combination thereof.

[0040] 3D memory device 200 can include an array device above substrate 202 (on a top surface of substrate 202). It is noted that x, y, and z axes are added in FIG. 2 to further illustrate the spatial relationship between the various components in 3D memory device 200. Substrate 202 includes two lateral surfaces (e.g., a top surface and a bottom surface) extending laterally in the x-direction (the lateral direction) and y-direction. As used herein, whether one component (e.g., a

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layer or a device) is "on," "above," or "below" another component (e.g., a layer or a device) of a semiconductor device (e.g., 3D memory device 200) is determined relative to substrate 202 in the z-direction (the vertical direction) when the substrate is positioned in the lowest plane of the semiconductor device in the z-direction. The same notion for describing spatial relationship is applied throughout the present disclosure. Further, the y-direction is pointing into the page of FIG. 2.

[0041] By way of example and not limitation, 3D memory device 200 can be part of a non-monolithic 3D memory device, in which components (e.g., the peripheral device and array device) can be fabricated independently on different substrates and then bonded in a "face-to-face" configuration. In some embodiments, the array device substrate (e.g., substrate 202) remains as the substrate of the bonded non-monolithic 3D memory device, and the peripheral device (e.g., any suitable digital, analog, and/or mixed-signal peripheral circuits used for facilitating the operation of 3D memory device 200, such as page buffers, decoders, and latches; not shown in FIG. 2) is positioned so that it faces the 3D memory device 200 prior to hybrid bonding. Alternatively, in some embodiments, 3D memory device 200 is positioned so that it faces the peripheral device (not shown in FIG. 2 merely for clarity) prior to hybrid bonding. The array device substrate (e.g., substrate 202) can be a thinned substrate and the back-end-of-line (BEOL) interconnects of the non-monolithic 3D memory device can be formed on the backside (e.g. bottom surface) of the thinned array device substrate 202.

[0042] In some embodiments, 3D memory device 200 can be part of a non-monolithic 3D memory device regardless of its relative position (e.g. above or below) with respect to the peripheral device. For ease of reference, FIG. 2 depicts a state of 3D memory device 200 in which substrate 202 (the array device substrate) is positioned below the array device in the x-y plane, regardless of whether substrate 202 is the substrate of the non-monolithic 3D memory device or a thinned substrate on which the BEOL interconnect layers of the non-monolithic 3D memory device are formed.

[0043] In some embodiments, 3D memory device 200 is a NAND Flash memory device in which memory cells are provided in the form of an array of NAND strings 204 extending vertically above substrate 202. The array device can include a plurality of NAND strings 204 that extend through a plurality of conductor layer 206 and dielectric layer 208 pairs. The plurality of conductor/dielectric layer pairs are also referred to herein as "alternating conductor/dielectric stack" 210. In some embodiments, the number of the conductor/dielectric layer pairs in

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alternating conductor/dielectric stack 210 (e.g., 32, 64, or 96) defines the number of memory cells in 3D memory device 200. Conductor layers 206 and dielectric layers 208 in alternating conductor/dielectric stack 210 alternate in the vertical direction (e.g., along the z-axis). In other words, except the layers at the top or bottom of alternating conductor/dielectric stack 210, each conductor layer 206 can be adjoined by two dielectric layers 208 on both sides, or each dielectric layer 208 can be adjoined by two conductor layers 206 on both sides. Conductor layers 206 can each have the same thickness or different thicknesses. Similarly, dielectric layers 208 can each have the same thickness or different thicknesses. By way of example and not limitation, the thickness of each conductor layer 206 can range from about 25 nm to about 40 nm, and the thickness of each dielectric layer 208 can range from about 20 nm to about 35 nm.

[0044] By way of example and not limitation, conductor layers 206 can include conductive materials such as tungsten (W), cobalt (Co), copper (Cu), aluminum (Al), doped polycrystalline Si (polysilicon), doped single crystalline Si, silicides, or any combination thereof. Dielectric layers 208 can include dielectric materials including, but not limited to, silicon oxide (Si_xO_y, thereafter "SiO_2"), silicon nitride (Si_xN_y, thereafter "SiN"), silicon oxynitride (SiON), or any combination thereof. In some embodiments, conductor layers 206 include metal layers, such as W, and dielectric layers 208 include SiO_2.

[0045] As shown in FIG. 2, at least on one side in the lateral direction (e.g., along the x-axis), alternating conductor/dielectric stack 210 can include a staircase structure 212. Each "level" or "step" 214 of staircase structure 212 can include one or more conductor/dielectric layer pairs on stacked top of each other. Each conductor/dielectric layer pair includes a conductor layer 206 and dielectric layer 208 respectively. The top layer in each level 214 of staircase structure 212 is a conductor layer 206 available for interconnection in the vertical direction (e.g., along the z-axis). In some embodiments, levels 214 in staircase structure 212 have the same height. Further, adjacent levels 214 of staircase structure 212 are being offset with one another by a nominally same distance in the x-direction. More specifically, for each two adjacent levels 214 of staircase structure 212, the first level that is closer to substrate 202 can extend laterally further than the second level, thereby forming a "landing area" or a "connection point" on the first level for interconnection in the vertical direction (e.g., along the z-axis).

[0046] As shown in FIG. 2, each NAND string 204 includes a channel structure 216 that extends through alternating conductor/dielectric stack 210. Channel structure 216 is filled with semiconductor materials (e.g., as a semiconductor channel 218) and dielectric materials (e.g., as a

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memory film 220). In some embodiments, semiconductor channel 218 includes Si, such as amorphous Si, polysilicon, single crystalline Si, etc. In some embodiments, memory film 220 is a composite stack of layers that includes a tunneling layer, a storage layer (also known as "charge trap/storage layer"), and a blocking layer. Each NAND string 204 can have a cylindrical shape (e.g., a pillar shape). Semiconductor channel 218, the tunneling layer, the storage layer, and the blocking layer are arranged along a direction from the center toward the outer surface of the pillar in this order, according to some embodiments. The tunneling layer can include SiO_2, SiN, or any combination thereof. The storage layer can include SiN, SiON, silicon, or any combination thereof. The blocking layer can include SiO_2, SiN, high dielectric constant (high-k) dielectrics (e.g., with a dielectric constant greater than 3.9), or any combination thereof.

[0047] In some embodiments, NAND strings 204 include a plurality of control gates (each being part of a WL). Conductor layer 206 in alternating conductor/dielectric stack 210 can act as the control gate for memory cells in NAND strings 204. Additionally, each conductor layer 206 can act as the control gate for multiple NAND strings 204 that can extend laterally (e.g., along the x-y plane) as a WL ending in staircase structure 212.

[0048] In some embodiments, each NAND string 204 includes an epitaxial layer 222 and an etch stop plug 224 at the respective bottom and top of NAND string 204, as shown in FIG. 2. For each NAND string 204, epitaxial layer 222 is referred to herein as an "epitaxial plug." Each of epitaxial plug 222 and etch stop plug 224 can be in contact with a respective end of channel structure 216. Epitaxial plug 222 can include, for example, a semiconductor material (e.g., single crystalline Si) that is epitaxially grown from substrate 202. Etch stop plug 224 can include semiconductor materials (e.g., polysilicon) or conductor materials (e.g., metals). In some embodiments, etch stop plug 224 includes an opening filled with a titanium/titanium nitride stack (barrier and adhesion layer) and W (conductor). As the name suggests, etch stop plug 224 is an etch stop layer that prevents etching of dielectrics in channel structure 216, such as SiO_2 and SiN, during subsequent etch operations. In some embodiments, etch stop plug 224 acts as the drain of NAND string 204.

[0049] In some embodiments, the array device further includes slit structures 226. Each slit structure 226 can extend vertically (e.g., along the z-axis) through alternating conductor/dielectric stack 210. Slit structures 226 also extend along the y-axis to separate alternating conductor/dielectric stack 210 into multiple blocks as discussed earlier for FIGs 1A-1C. Slit structures 226 are filled with conductor materials including, but not limited to, W, Co,

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Cu, Al, a silicide, or any combination thereof. Slit structures 226 further include a dielectric layer interposed between the conductor in slit structure 226 and alternating conductor/dielectric stack 210 to electrically insulate the conductor materials in the slit structure from the surrounding conductor layers in alternating conductor/dielectric stack 210. In some embodiments, slit structure 226 acts as the source contact for NAND strings 204 located in the same memory block. Consequently, a slit structure 226 can function as the "common source contact" of multiple NAND strings 204 within a memory block.

[0050] In some embodiments, substrate 202 includes doped regions 228 with p-type or n-type dopants at a desired doping level. Each doped region 228 is in contact with a respective slit structure 226, as shown in FIG. 2. In some embodiments, slit structures 226 are electrically coupled to NAND strings 204 through doped regions 228.

[0051] It has to be noted that NAND strings 204 and slit structures 226 are partially formed in a dielectric layer 230 that is disposed over alternating conductor/dielectric stack 210. In some embodiments, dielectric layer 230 can be a layer stack made of a single dielectric material—as opposed to being a stack of alternating dielectric layers. By way of example and not limitation, dielectric layer 230 is an oxide layer, such as SiO_2. In other words, dielectric layer 230 can be the same as dielectric layer 208. Further, and as shown in FIG. 2, dielectric layer 230 can extend over staircase structure 212.

[0052] As shown in FIG. 2, dielectric conductor/dielectric stack 210 is "disrupted" by single-material dielectric structure 232 (thereafter "dielectric structure 232") along the x-direction (and along the y-direction—not shown from FIG.2). In some embodiments, dielectric structure 232 defines the boundaries, the shape, and the size of TAC region 120 (e.g., shown in FIGS. 1A-1C). Consequently, as shown in the plan-views of FIGS. 1A-1C, dielectric structure 232 can be surrounded by conductor/dielectric stack 210. Further, dielectric structure 232 can extend in the x-y plane and be coplanar with dielectric layer 230 (e.g., the top surfaces of dielectric structure 232 and dielectric layer 230 are flushed). In some embodiments, dielectric structure 232 is formed so that it is aligned to or covers at least a portion of an underlying isolation structure or region 233 (thereafter "shallow trench isolation (STI) structure 233). Please note that, STI structure 233 is exemplary and is not limiting. As such, other isolation structures can be used. Further, dielectric structure 232 is in contact with STI structure 233. By way of example and not limitation, STI structure 233 is formed on a top portion of substrate 202 and is filled with a dielectric material, including but not limited to SiO_2, for example. In some embodiments, the

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footprint of dielectric structure 232 is smaller or equal to the footprint of STI structure 233. For example, in some embodiments, dielectric structure 232 can cover only portion of STI structure 233.

[0053] In some embodiments, dielectric structure 232 includes the same material with dielectric layer 230, and/or dielectric layer 208. For example, dielectric structure 232 can include SiO_2. However, this is not limiting and therefore dielectric structure 232 can include a different material than dielectric layer 208 or dielectric layer 230. In some embodiments, dielectric structure 232 can have different shapes. For example, as shown in the plan-views of FIGS. 1A-1C, TAC region 120 can have a rectangle or square shape. However, these shapes are not limiting and dielectric structures 232 can have any shape according to a design layout. Further, multiple dielectric structures, like dielectric structure 232, are possible across substrate 202.

[0054] As shown in FIG. 2, 3D memory device 200 further includes TACs 234, which extend vertically through dielectric structure 232. According to some embodiments, etching through dielectric structure 232 can be advantageous (e.g., involve fewer etch operations) compared to etching through a stack of alternating layers having the same overall thickness. For example, the formation of TACs 234 in an alternating layer stack with a thickness of about 6 μm or more (e.g., for a 64 tier 3D memory device) requires multiple etch and fill operations—therefore, increases the fabrication cost. Each TAC 234 can extend through the entire thickness of dielectric structure 232 and extend through at least a portion of STI structure 233 in substrate 202.

[0055] TACs 234 can carry electrical signals from and/or to 3D memory device 200, such as part of the power bus, with shorten interconnect routing. In some embodiments, TACs 234 can provide electrical connections between 3D memory device 200 and the peripheral device (e.g., on a CMOS chip; not shown in FIG. 2) and/or between BEOL interconnects (not shown in FIG. 2) and the peripheral device. Each TAC 234 is filled with conductor materials, including, but not limited to, W, Co, Cu, Al, doped Si, silicides, or any combination thereof. Since TACs 234 are embedded in dielectric structure 232, additional layers of dielectric are not required to insulate the conductor material.

[0056] In some embodiments, 3D memory device 200 includes a plurality of "local contacts" in physical and electrical contact with the various memory array structures disclosed herein, such as NAND strings 204, slit structures 226, and conductor layers or WL 206 in staircase structure 212. The contacts are referred to herein as "local contacts" because they are in direct contact with

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the memory array structures, and further because they are formed within dielectric layer 230. As shown in FIG. 2, local contacts can include NAND string contacts 236, slit structure contacts 238, and WL contacts 240. In some embodiments, TACs 234 are also considered local contacts. As used herein, the term "contact" can broadly include any suitable types of interconnects including vertical interconnect access (via) lines and lateral lines (interconnect lines).

[0057] In some embodiments, each local contact is coplanar with one another, e.g., on the top surface of a dielectric layer 230 (and dielectric structure 232 for TACs 234) in which the local contacts are formed. The lower end of each local contact can be in direct contact with the respective memory array structure. For example, the lower end of NAND string contact 236 can be in contact with etch stop plug 224 of NAND string 204, and the lower end of slit structure contact 238 can be in contact with the upper end of slit structure 226. The lower end of each WL contact 240 can be in contact with top conductor layer or WL 206 in a respective level of staircase structure 212. Each local contact is filled with conductor materials including, but not limited to, W, Co, Cu, Al, silicides, or any combination thereof. Some or all of the local contacts can be formed simultaneously in a single contact forming process as described below in detail.

[0058] As shown in FIG. 2, in addition to the local contacts, 3D memory device 200 can further include a contact layer 242 and an interconnect layer 244 as part of its interconnect structures. Contact layer 242 can include a dielectric layer and a plurality of contacts 246 (e.g., vias) in the dielectric layer. Interconnect layer 244 can be formed on contact layer 242 and can include another dielectric layer and a plurality of interconnect contacts 248 (e.g., interconnect lines) in the dielectric layer. The local contacts, contacts 246 in contact layer 242, and interconnect contacts 248 in interconnect layer 244 can be collectively referred to herein as the interconnect structures of 3D memory device 200.

[0059] In some embodiments, each contact 246 can be filled with conductor materials including, but not limited to, W, Co, Cu, Al, silicides, or any combination thereof. All contacts 246 can be formed simultaneously in a single contact forming process as described below in detail.

[0060] In some embodiments, each interconnect contact 248 can be filled with conductor materials including, but not limited to, W, Co, Cu, Al, silicides, or any combination thereof. All interconnect contacts 248 can be formed simultaneously in a single contact formation process as described below in detail.

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[0061] In some embodiments, interconnect contacts 248 in interconnect layer 244 can include bit lines 250, which are electrically connected to NAND strings 204, respectively, by corresponding contacts 246 and NAND string contacts 236. Bit lines 250 can be used to individually address a corresponding NAND string 204. Interconnect contacts 248 can further include source lines that are electrically connected to slit structures 226 (source contacts). Further, interconnect lines can be electrically connected to TACs 234 and to WL 206 in staircase structure 212 through respective contacts 246 and WL contacts 240. It is to be understood that the number of interconnect layers in 3D memory device 200 is not limited by the example in FIG. 2. Additional interconnect layer(s) with contacts can be formed to provide an interconnect network of structures for 3D memory device 200.

[0062] FIG. 3 is a flowchart of an exemplary method 300 for forming a 3D memory device similar to 3D memory device 200, according to some embodiments of the present disclosure. FIGs. 4-13 will be used to describe the exemplary fabrication process for forming a 3D memory device using method 300. By way of example and not limitation, the 3D memory device fabricated with method 300 can be the 3D memory device 200 depicted in FIG. 2. It should be understood that the operations shown in method 300 are not exhaustive and that other operations can be performed before, after, or between any of the operations. For example, other operations may include wet clean operations, dry etch operations, photolithography operations, etc. Further, the sequence of the operations in method 300 is not limiting, and some operations may be performed concurrently or in a different order.

[0063] Referring to FIG. 3 and FIG. 4, method 300 begins with operation 302, where an alternating dielectric stack 400 is disposed, or otherwise deposited, on a substrate 202. For example purposes, substrate 202 in method 300 will be described in the context of single crystalline Si. Based on the disclosure herein, other materials, as discussed above, can be used. These materials are within the spirit and scope of this disclosure. A plurality of first dielectric layer 208 and second dielectric layer 402 pairs can be formed on substrate 202 to form alternating dielectric stack 400. In some embodiments, each dielectric layer pair includes a SiO_2 layer and a SiN layer. For example, first dielectric layer 208 can be made of SiO_2 (same as dielectric layer 230 of alternating conductor/dielectric stack 210 of FIG. 2) and second dielectric layer 402 can be made of SiN. Alternating dielectric stack 400 can be formed by one or more thin-film deposition processes including, but not limited to, chemical vapor deposition (CVD), plasma-enhanced CVD (PECVD), physical vapor deposition (PVD), atomic layer deposition

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(ALD), plasma-enhanced ALD (PEALD), or any combination thereof. By way of example and not limitation, the height of dielectric stack 400 can range from about 4 μm to about 30 μm. In some embodiments, second dielectric layer 402 can be a sacrificial layer that will be replaced with a conductor in a subsequent operation so that alternating dielectric stack 400 can be converted to an alternating conductor/dielectric stack, similar to alternating conductor/dielectric stack 210 of FIG. 2.

[0064] According to some embodiments, substrate 202 includes isolation regions or structures, like STI structure 233 shown in FIG. 4. STI structure 233 in FIG. 4 can be formed on a top portion of substrate 202. By way of example, STI structure 233 can be formed prior to the formation of alternating dielectric stack 400. STI structures can be filled with a dielectric material, such as for example SiO_2.

[0065] Method 300 continues with operation 304, as illustrated in FIG 3, in which a staircase structure (like staircase structure 212 of FIG. 2) is formed from a portion of alternating dielectric stack 400. In some embodiments, a "trim-etch" process can be used on at least one side (in the lateral direction, x-direction) of alternating dielectric stack 400 to form a staircase structure with multiple levels (e.g., steps). By way of example and not limitation, a trim-etch process can be a multi-cycle process, where each cycle includes one or more photolithography operations followed by an etch operation. During the photolithography operations, a patterned photoresist (PR) layer masks a portion of dielectric stack 400. A subsequent first etch process removes a predetermined number of dielectric pairs from the exposed portion of dielectric stack 400 to form a first step (e.g., first level) in dielectric stack 400. The PR is then laterally trimmed (e.g., recessed in the x-direction) to expose an additional portion of dielectric stack 400. A subsequent second etch removes a predetermined number of dielectric pairs from the newly exposed dielectric stack 400 and the first step. Hence, a second step (e.g., second level) in dielectric stack 400 is formed. This step formation process continues in this fashion (e.g., a PR trim followed by an etch operation) until the desired number of steps in dielectric stack 400 is formed and the staircase structure is complete. As a result of this process, each level can include any desired number of dielectric layer pairs with alternating first dielectric layer 208 and second dielectric layer 402. After the staircase structure formation, the PR layer is removed (stripped) with a wet etch process. FIG. 5 shows the resulting staircase structure 500 made from alternating dielectric stack 400 according to the description of operation 304 of method 300.

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[0066] In some embodiments, the etch process used in operation 304 can be a dry etch process that uses a single etch gas chemistry for both dielectric layers 208 and 402. Alternatively, the etch process used in operation 304 can use different etch chemistries for each dielectric layer. Further, depending on the selectivity of the etch chemistry, the etch process can be timed, end-pointed, or a combination thereof.

[0067] After the staircase structure formation, dielectric layer 230 is deposited over staircase structure 500 and dielectric stack 400. In some embodiments, a CMP or a dry etch process can be used to planarize the top surface of dielectric layer 230, as shown in FIG. 5. By way of example and not limitation, dielectric layer 230 can be SiO_2 deposited by PECVD, CVD, or another suitable deposition process. The thickness of dielectric layer 230 over alternating dielectric stack 400 can range from about 10 to about 1000 nm. In some embodiments, dielectric layer 230 is the same as dielectric layer 208 of dielectric stack 400, e.g., SiO_2.

[0068] Method 300 continues with operation 306, as illustrated in FIG. 3, where a channel structure can be formed over substrate 202. However, this is not limiting and additional channel structures can be formed. Each channel structure can extend vertically through the alternating dielectric stack 400, as discussed earlier. Fabrication of each channel structure begins by etching a channel hole through dielectric layer 230 and alternating dielectric stack 400 until substrate 202 is exposed through the channel hole. Prior to filling the channel hole, an epitaxial plug 222 can be grown through the channel hole from substrate 202, as shown in FIG. 6. By way of example and not limitation, epitaxial plug 222 can be single crystalline Si. The height of epitaxial plug 222 can be controlled through the epitaxial growth process conditions. Channel structure 216 can be subsequently formed on epitaxial plug 222 by filling the channel hole.

[0069] By way of example and not limitation, a dry etch process can be used to form the channel hole. In some embodiments, the fabrication process of channel structure 216 further includes depositing memory film 220 and semiconductor channel 218 so that memory film 220 can be interposed between semiconductor channel 218 and the dielectric layer pairs 402 and 402 of alternating dielectric stack 400. Semiconductor channel 218 can include semiconductor materials, such as polysilicon. Memory film 220 can be a composite stack of dielectric layers including a combination of a tunneling layer, a storage layer, and a blocking layer (not individually shown in FIG. 6).

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[0070] By way of example and not limitation, the tunneling layer can include dielectric materials such as SiO_2, SiN, SiON, or a combination thereof. Electrons or holes from the semiconductor channel can tunnel into a storage layer through the tunneling layer. The storage layer can include materials for storing charge. The storage layer materials include, but are not limited to, SiN, SiON, a combination of SiO_2 and SiN, or a combination thereof. The blocking layer can include a single dielectric material, such as SiO_2, or a stack of dielectric materials, such as $SiO_2/SiN/SiO_2$ (ONO). The blocking layer can further include a high-k dielectric, such as aluminum oxide (Al_2O_3). Semiconductor channel 218 and memory film 220 can be formed by one or more thin-film deposition processes, such as ALD, CVD, PEALD, PECVD, any other suitable deposition processes, or a combination thereof.

[0071] In some embodiments, dummy channel structures (not shown in FIGs. 4-13; e.g., dummy channel structures 122 in FIGs. 1A-1B) are formed simultaneously with channel structures 216. The dummy channel structures can extend vertically through the alternating layer stack and can be filled with the same materials as those in channel structures 216. However, local contacts are not formed on the dummy channel structures to provide electrical connections with other components of the 3D memory device. Thus, the dummy channel structures cannot be used for forming memory cells in the 3D memory device, i.e., they are not electrically functional or otherwise operational. In some embodiments, the dummy channel structures are used as structural elements.

[0072] Referring to FIG. 3, method 300 continues with operation 308 and the formation of an opening in the alternating dielectric layer stack. Formation of the opening involves etching portions of dielectric layer 230 and dielectric stack 400 until STI structure 233 of substrate 202 is exposed (e.g., through the etched portions of dielectric layer 230 and dielectric stack 400), as shown in FIG. 6. In other words, the opening can be formed so that it is aligned to STI structure 233. In some embodiments, the opening cannot expose an area beyond the STI structure 233. For example, the opening cannot expose STI structure 233 and a portion of substrate 202. However, the opening can expose a portion of STI structure 233. This can be accomplished via photolithography and etch methods (patterning). For example, photolithography can be used to form a patterned PR structure or a patterned hard mask (HM) (not shown in FIG. 6) over dielectric layer 230. The patterned PR structure or patterned HM can have an opening that exposes an area of dielectric layer 230. The opening in the patterned PR structure or patterned HM can be positioned so that it is over an area of the underlying STI structure 233. Areas of

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dielectric layer 230, where the formation of a dielectric structure is not desired, are covered by the patterned PR structure or patterned HM. A subsequent dry etch process removes the exposed portions of dielectric layer 230 and dielectric stack 400—e.g., through the openings in the patterned PR structure or patterned HM—until STI structure 233 of substrate 202 is exposed. In some embodiments, the dry etch process can be a multi-step, anisotropic etch that can be terminated (e.g., stopped) when STI structure 233 is exposed. By way of example and not limitation, the dry etch process can include the same or different etch chemistry for each layer (e.g., dielectric layer 230 and alternating dielectric stack 400). As a result of operation 308, an opening 600 with width 600w is formed in dielectric stack 400 over STI structure 233, as shown in FIG. 6. As discussed above, width 600w of opening 600 can be equal or shorter than width 233w of STI structure 233 (e.g., $600w \leq 233w$). In some embodiments, opening 600 may extend partially into STI structure 233. In other words, the etch process used to form opening 600 may also remove (recess) portion of the top surface of STI structure 233. It is noted that opening 600 shown in FIG. 6 can also extend in the y-direction (not shown in the view of FIG. 6) and its size can be defined by the patterned PR structure or patterned HM and the process conditions during the etch process. In any direction, the area of opening 600 can be equal or smaller than the area of STI structure 233, according to some embodiments. Additionally, multiple openings, like opening 600, can be formed concurrently during operation 306 of method 300 in other areas of dielectric stack 400. Further, each opening 600 can be formed over an STI structure 233. In some embodiments, the aspect ratio of opening 600 can range from about 0.1 to about 10.

[0073] In some embodiments, opening 600 can be formed concurrently with channel structure 216. In an alternative embodiment, opening 600 can be formed after the formation of channel structure 216, or before the formation of channel structure 216. Each of the aforementioned sequence of operations may require additional number of photolithography, etch, or deposition operations. After the formation of opening 600, the patterned PR structure or patterned HM can be removed (stripped) with a wet etch process.

[0074] In referring to FIGs. 3 and 7, method 300 continues with operation 310, where opening 600 can be filled with a dielectric layer 702. In some embodiments, dielectric layer 702 includes a SiO_2 layer that can be deposited by a CVD, flowable CVD (FCVD), a PECVD process, or any other suitable process that can fill a high aspect ratio structure. By way of example and not limitation, dielectric layer 702 can be the same as dielectric layer 230, and/or first dielectric layer 208. A CMP process or a dry etch process can be used to planarize dielectric layer 702 so that the

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top surfaces of dielectric layer 230 and dielectric layer 702 are coplanar as shown in FIG. 7. As a result, dielectric structure 232 is formed in dielectric stack 400. In some embodiments, dielectric structure 232 defines the borders of TAC region 120 shown in FIGS. 1A-1C.

[0075] In some embodiments an etch stop layer is formed on the channel structures 216. For example a dielectric layer 704 can be deposited over dielectric layers 230 and 232 and be subsequently patterned to form plug openings 706 as shown in FIG. 7. Etch stop plug 224 can be subsequently formed on channel structures 216 by filling plug openings 708 using one or more thin-film deposition processes, such as ALD, CVD, PVD, any other suitable processes, or any combination thereof, as shown in FIG. 8. In some embodiments, polysilicon can be used to fill plug opening 706 followed by a CMP process to remove the excess polysilicon so that etch stop plug 224 can be coplanar with dielectric layer 704. In some embodiments, a metallic stack, such as Ti/ TiN/W, can be deposited to fill plug opening 706, followed by a CMP process to make the top surface of etch stop plug 224 and dielectric layer 704 coplanar. In some embodiments, etch stop plug 224 can be sacrificial so that it can be replaced in a subsequent operation. For example, a sacrificial etch stop plug 224 can include an oxide instead of polysilicon or a metallic stack. A sacrificial etch stop plug 224 can be removed at a later operation and replaced with a "permanent" etch stop plug made of polysilicon or a metallic stack.

[0076] In operation 312 of method 300, as illustrated in FIG. 3, one or more slit openings can be formed in alternating dielectric stack 400. For example, slit opening 900 can be formed by dry etching dielectric layers 208 and 402 (e.g., SiO_2 and SiN) in dielectric stack 400, as shown in FIG. 9. In some embodiments, doped regions 228 can be subsequently formed in substrate 202 under each slit by, for example, ion implantation and thermal diffusion through the slits. Alternatively doped regions 228 can be formed during an earlier fabrication stage, for example, prior to the formation of dielectric stack 400, according to some embodiments.

[0077] In operation 314 of method 300, slit openings 900, shown in FIG. 9, can be used for a "gate replacement" process (also known as the "WL replacement" process) in which second dielectric layers 402 (shown in FIG. 9; e.g., SiN) in stack 400 are replaced with conductor layers 206 (shown in FIG. 10; e.g., W). As a result, alternating dielectric stack 400 is converted to alternating conductor/dielectric stack 210 shown in FIG. 2.

[0078] The replacement of second dielectric layers 402 with conductor layers 206 can be achieved with the use of a wet etch process that is highly selective (e.g., with selectivity equal to,

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or greater than, 500:1) towards second dielectric layer 402 (e.g., SiN), in comparison to first dielectric layer 208 (e.g., SiO_2). By way of example and not limitation, the wet etch chemistry can include hot phosphoric acid (H_3PO_4). Since the wet etch chemistry is highly selective towards SiN, any layers or structures (including first dielectric layer 208 and dielectric structure 702) made of oxide (e.g., SiO_2) will not be etched or removed (i.e., will not be affected by the wet etch process).

[0079] Once second dielectric layers 402 are fully removed (e.g., etched), a conductive layer can be deposited by CVD, PECVD, ALD, PEALD, or combinations thereof to fill the space between first dielectric layers 208 through slit openings 900. As a result, conductor layers 206 can be formed between first dielectric layers 208 as shown in FIG. 10. By way of example and not limitation, the conductor materials can include W, Co, Cu, Al, polysilicon, silicides, or a combination thereof. In some embodiments, adhesion layers or barrier layers (not shown in FIG. 10) may also be deposited prior to the deposition of the conductor material. In some embodiments, conductive layers 206 can be deposited with a deposition–etch–deposition process to avoid partially filling slit openings 900 with the conductor material.

[0080] In operation 316 of method 300 shown in FIG. 3, the slit openings can be filled with a conductor material 1004 to form slit structures 226 as shown in FIG. 10. In some embodiments, conductor material 1004 can be the same as the conductor material in conductor layers 206. For example, slit structures 226 can be filed with W, Co, Cu, Al, polysilicon, silicides, or a combination thereof. In some embodiments, to electrically isolate conductor material 1004 of slit structure 226 from conductor layers 206, a dielectric layer 1008 (e.g., SiO_2) can be deposited therebetween. A CMP process can subsequent remove excess conductor material over dielectric layer 704 as shown in FIG. 10. The lower end of slit structure 226 can be in contact with doped region 228. In some embodiments, slit structure 226 can function as a source contact that is electrically connected to NAND string 204 through doped region 228 of substrate 202.

[0081] Referring to Fig. 11, a dielectric layer 1100 can be blanket deposited over dielectric layer 704 across substrate 202 so that local contacts can be formed in dielectric layer 1100. In some embodiments, the contact formation process can be divided into two separate photolithography/etch operations to accommodate the formation of contacts with different depths or heights. For example, the shortest local contacts (e.g., the NAND string contacts, the slit structure contacts, and the upper WL contacts of the staircase structure) can be formed first, and the tallest local contacts (e.g., the TACs and the lower WL contacts of the staircase structure) can

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be formed second. Merely for simplicity, the aforementioned shorter local contacts can be collectively referred to as first local contacts, and the aforementioned tallest local contacts can be collectively referred to as second local contacts.

[0082] Dielectric layer 1100 can be formed by one or more thin-film deposition processes, including ALD, CVD, PVD, any other suitable processes, or any combination thereof. Dielectric layer 1100 can include dielectric materials, including, but not limited to, SiO_2, SiN, SiON, or any combination thereof. First local contacts—such as NAND string contacts 236, slit structure contacts 238, and upper WL contacts 240-1—can be formed through dielectric layer 1100 by first etching vertical openings (e.g., with a dry etch), followed by filling the openings with conductor materials using ALD, CVD, PVD, any other suitable processes, or any combination thereof. By way of example and not limitation, the conductor materials used to fill the local contacts can include W, Co, Cu, Al, polysilicon, silicides, or a combination thereof. In some embodiments, prior to the conductor material fill, the openings can be filled with a barrier layer, an adhesion layer, and/or a seed layer. In some embodiments, prior to filing the openings, the oxide sacrificial etch stop plugs 224 can be replaced with permanent etch stop plugs made of polysilicon or a metallic stack, as discussed above.

[0083] Etching of dielectric layers to form the openings of first local contacts can be controlled via the "inherent" etch selectivity between the etched layer (e.g., a dielectric layer) and the underlying layer (a conductor, a nitride or oxide, etc.). For example, in the case of NAND string contacts 236, etch stop plug 224 filled with an oxide different from dielectric layer 1100 or a nitride can prevent further etching into NAND strings 204 during the formation of the first local contact openings. In the case of slit structure contacts 238 and upper WL contacts 240-1, further etching can be prevented due to the presence of conductor material 1004 and conductor layer 206, which can act as an etch stop layer for the dry etch process. As a result, formation of first local contacts with different heights can be possible.

[0084] A discussed earlier, first local contacts—such as NAND string contacts 236, slit structure contacts 238, and upper WL contacts 240-1—can be concurrently formed in the same contact forming process. The first local contact forming process can include multiple processes, for example, photolithography, etch, thin-film deposition, and CMP. In some embodiments, each process in the contact forming process can be performed only once for all the first local contacts. For example, a single lithography and etch process can be used to form all the openings of NAND string contacts 236, slit structure contacts 238, and upper WL contacts 240-1 and a single

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deposition process can be performed to fill all the openings of NAND string contacts 236, slit structure contacts 238, and upper WL contacts 240-1 with the same conductor materials. In some embodiments, a CMP process can remove excess deposited material from the top surface of dielectric layer 1100.

[0085] In Referring to FIG. 3 and method 300, the formation of the TAC structures (and the rest of the second local contacts) can be formed in operation 318. Referring to FIG. 12, and according to some embodiments, after forming the first set of local contacts (e.g., NAND string contacts 236, slit structure contacts 238, and upper WL contacts 240-1) a second set of local contacts can be formed, including TACs 234 and lower WL contacts 240-2 that are close to substrate 202. TACs 234 can be formed in dielectric layers 1100, 704, and 232—and lower WL contacts 240-2 can be formed in dielectric layers 1100, 704, and 230—by first etching vertical openings (e.g., by dry etching), followed by filling the openings with conductor materials using ALD, CVD, PVD, any other suitable processes, or any combination thereof. The conductor materials used for filling the local contacts can include, but are not limited to, W, Co, Cu, Al, polysilicon, silicides, or any combination thereof. In some embodiments, prior to the conductor material deposition, a barrier layer, an adhesion layer, and/or a seed layer can be formed.

[0086] TACs 234 can be formed by etching through the entire thickness of dielectric structure 702. Since both TACs 234 and lower WL contacts 240-2 are formed in oxide layers (e.g., dielectric layers 1100, 704, 232, and 230) the overall etching process can be simplified in terms of etching chemistry, etching process tooling, overall process integration, and cost. By way of example and not limitation, the openings for TACs 234 and lower WL contacts 240-2 can be formed by a deep reactive-ion etching (DRIE) process or with any other suitable anisotropic etch process. Forming TACs 234 in dielectric structure 232 can simplify the fabrication process and reduce the fabrication cost. This is because TACs 234 can be easily formed even after the gate replacement process together with the other local contacts in a common contact forming process.

[0087] In some embodiments, the lower end of TACs 234 can be formed in STI structure 233 and in contact with substrate 202, as shown in FIG. 12. For example, TACs 234 can extend through STI structure 233 and stop on substrate 202. The lower end of each lower WL contacts 240-2 can be in contact with the corresponding top conductor layer 206 (WL) of a corresponding level in the staircase structure, as shown in FIG. 12. The upper ends of all the local contacts (including both the first and second sets of local contacts) can be coplanar with one another at the top surface of dielectric layer 1100. The second set of local contacts (including TACs 234 and

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lower WL contacts 240-2) can be simultaneously formed in the same contact forming process after the formation of the first set of local contacts. That is, all the local contacts (including both the first and second sets of local contacts) can be formed in two contact forming processes as illustrated in FIGs. 11 and 12.

[0088] It is understood that in some embodiments, all the local contacts (including both the first and second sets of local contacts) can be simultaneously formed in a single contact forming process. That is, the two contact forming processes illustrated in FIGs. 11 and 12 can be combined into a single contact forming process. In some embodiments, each process in the contact forming process can be performed once for all of NAND string contacts 236, slit structure contacts 238, TACs 234, upper WL contacts 240-1, and lower WL contacts 240-2. For example, a single lithography process can be performed followed by a single etch process and a single deposition process.

[0089] In some embodiments, an additional contact layer with a plurality of contacts can be formed over the local contacts. As illustrated in FIG. 13, contact layer 242 (including a dielectric layer 1302 and contacts 246) can be formed over dielectric layer 1100. Dielectric layer 1302 can be formed by one or more thin-film deposition processes, including ALD, CVD, PVD, any other suitable processes, or any combination thereof. Dielectric layer 1302 can include dielectric materials, including, but not limited to, SiO_2, SiN, SiON, or any combination thereof. Contacts 246 can be formed through dielectric layer 1302 by first etching vertical openings (e.g., using dry etch), followed by filling the openings with conductor materials using ALD, CVD, PVD, any other suitable processes, or any combination thereof. The conductor materials used to fill contacts 246 can include, but are not limited to, W, Co, Cu, Al, polysilicon, silicides, or any combination thereof. In some embodiments, prior to the conductor material deposition, a barrier layer, an adhesion layer, and/or a seed layer can be deposited in the contact opening.

[0090] As shown in FIG. 13, the lower end of each contact 246 can be in contact with the upper end of a corresponding local contact, for example, NAND string contact 236, slit structure contact 238, TAC 1200, or WL contacts 240-1 and 240-2. In some embodiments, all contacts 246 in contact layer 242 can be simultaneously formed in the same contact forming process. In some embodiments, each contact 246 of contact layer 242 is a via. Further, contact layer 242 can be referred to as the "Via0 (V0)" level/ bottom level of the interconnect structures of 3D memory device 200.

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[0091] Subsequently, a plurality of third contacts in an interconnect layer can be formed. As illustrated in FIG. 13, interconnect layer 244 (including a dielectric layer 1308 and interconnect contacts 248) can be formed above contact layer 242. Dielectric layer 1308 can be formed by one or more thin-film deposition processes, such as ALD, CVD, PVD, any other suitable processes, or any combination thereof. Dielectric layer 1308 can include dielectric materials, including, but not limited to, SiO_2, SiN, SiON, or any combination thereof. By way of example and not limitation, interconnect contacts 248 can be formed through dielectric layer 1308 by first etching vertical openings (e.g., with a dry etch process), followed by filling the openings with conductor materials using ALD, CVD, PVD, any other suitable processes, or any combination thereof. The conductor materials used to fill interconnect contacts 248 can include, but are not limited to, W, Co, Cu, Al, polysilicon, silicides, or any combination thereof. In some embodiments, prior to the conductor material deposition, a barrier layer, an adhesion layer, and/or a seed layer is formed.

[0092] As shown in FIG. 13, the lower end of each interconnect contact 248 can be in contact with the upper end of corresponding contact 246 in contact layer 242, so that each interconnect contact 248 can be electrically connected to a corresponding memory array structure, such as NAND strings 204, slit structures 226, and WLs 240-1 and 240-2. In some embodiments, all interconnect contacts 248 in interconnect layer 244 can be concurrently formed in the same contact forming process. In some embodiments, each interconnect contact 248 can be an interconnect line, and interconnect layer 244 can be referred to as the "Metal0 (M0)" level/ bottom level of the interconnect structures of 3D memory device 200.

[0093] According to some embodiments, contacts 246 and interconnect contacts 248 can be formed in a single contact forming process, such as in a dual damascene process for forming Cu contacts. Nevertheless, as illustrated in FIG. 13, the interconnect structures including local contacts and contacts 246 and 248 can be formed in a limited number of fabrication steps to reduce the fabrication complexity and cost.

[0094] Various embodiments in accordance with the present disclosure provide a 3D memory device with interconnect structures for a memory array. The interconnect structures allow contacts for various memory array structures (e.g., NAND strings, gate line slits, WLs, etc.) to be fabricated in a limited number of operations (e.g., in a single operation or in two operations), thereby reducing the process complexity and manufacturing cost. In some embodiments, the interconnect structures disclosed herein can include bit lines in the top interconnect layer. These bit lines are suitable for 3D memory architectures in which the array device and the peripheral

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device are formed on different substrates and are subsequently joined by hybrid bonding in a face-to-face configuration.

[0095] Moreover, the interconnect structures disclosed herein include TACs for providing vertical interconnects between the stacked array device and peripheral device (e.g., for power bus and metal routing), thereby reducing the metal levels, improving the packing density and decrease the die size. In some embodiments, the TACs in the interconnect structures disclosed herein are formed in a dielectric structure that can be easily etched to form through holes therein compared to a stack of alternating dielectric layers or a stack of alternating conductor/dielectric layers. Therefore, fabrication complexity and cost can be reduced. The dielectric structure can be formed prior to the conversion of alternating layer stack of dielectrics to a conductor/dielectric layer stack.

[0096] In some embodiments, a 3D memory device includes a semiconductor substrate, an alternating layer stack disposed on the semiconductor substrate, and a dielectric structure, extending vertically through the alternating layer stack, on an isolation region of the substrate. Further, the alternating layer stack can abut a sidewall surface of the dielectric structure and the dielectric structure is formed of a dielectric material. The 3D memory device additionally can include one or more TACs that extend vertically through the dielectric and isolation region, and one or more channel structures that extend vertically through the alternating layer stack.

[0097] The 3D memory device further includes an epitaxial layer formed between each of the one or more channel structures and the semiconductor substrate, an etch stop plug disposed on each of the one or more channel structures, a staircase structure disposed in the alternating layer, and one or more contact layers disposed on the one or more TACs, channel structures, and slit structures.

[0098] In some embodiments, the dielectric structure abuts a sidewall surface of the TACs.

[0099] In some embodiments, the 3D memory device is a NAND 3D memory device.

[0100] In some embodiments, the alternating layer stack includes alternating pairs of a dielectric and conductor layers.

[0101] In some embodiments, the dielectric layer comprises silicon oxide and the conductor layer includes a metal.

[0102] In some embodiments, the conductor layers include a word line.

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[0103] In some embodiments, the dielectric material is silicon oxide.

[0104] In some embodiment, the dielectric structure includes an oxide.

[0105] In some embodiment, the dielectric structure defines a through array contact region within the 3D memory device.

[0106] In some embodiments, an area of the dielectric structure is equal to or smaller than an area of the isolation region.

[0107] In some embodiments a method for forming 3D memory device includes forming an isolation structure on a substrate, disposing an alternating dielectric layer stack on the substrate, where the alternating dielectric layer stack includes pairs of a first dielectric layer and a second dielectric layer different from the first dielectric layer. The method further includes forming a channel structure extending vertically in the alternating dielectric layer, forming an opening in the alternating dielectric layer stack, where the opening exposes the isolation structure. The method also includes filling the opening with a dielectric layer to form a dielectric structure as a TAC region of the 3D memory device, removing portions of the dielectric structure and the isolation structure until the substrate is exposed to form a TAC opening that vertically extends through the dielectric structure and the isolation structure, and filling the TAC opening with a conductor to form a TAC structure in the TAC region, wherein the TAC structure is in contact with the substrate.

[0108] In some embodiments, before forming the TAC opening the method further includes forming slit openings that expose a doped region of the substrate by extending vertically in the alternating dielectric layer, replacing the second dielectric layer through the one or more slit openings with a conductor layer to convert the alternating dielectric layer stack to an alternating dielectric/conductor layer stack, and filling the one or more slit openings with a conductor to form one or more slit structures extending vertically in the alternating dielectric/conductor layer stack.

[0109] In some embodiments, before forming a channel structure, performing a trim-etch process to form a staircase structure in the alternating dielectric layer stack.

[0110] In some embodiment, removing portions of the alternating dielectric layer stack includes performing a dry etch process.

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[0111] In some embodiments, filling the opening with the dielectric layer includes depositing the dielectric layer with a chemical vapor deposition, a plasma-enhanced chemical vapor deposition, or a physical vapor deposition process.

[0112] In some embodiments, filling the opening with the dielectric layer includes forming an oxide.

[0113] In some embodiments, filling the opening with the dielectric layer includes forming a silicon oxide.

[0114] In some embodiments, the first dielectric layer includes an oxide and the second dielectric layer comprises a nitride.

[0115] In some embodiments, the first dielectric layer includes a silicon oxide and the second dielectric layer comprises a silicon nitride.

[0116] In some embodiments a method for forming a 3D memory device includes disposing an alternating dielectric layer stack on a substrate, where the alternating dielectric layer stack includes pairs of a first dielectric layer and a second dielectric layer different from the first dielectric layer; forming channel structures extending vertically through the alternating dielectric layer; etching the alternating dielectric layer stack to form an opening, where the opening exposes an isolation region in the substrate; filling the opening with a dielectric layer to form a dielectric structure as a TAC region that is equal or smaller than the isolation region; etching through the dielectric structure and the isolation region to form TAC openings that expose the substrate; and filling the TAC openings with a conductor to form TAC structures in the TAC region.

[0117] In some embodiments a method for forming a 3D memory device further includes forming slit openings extending vertically through the alternating dielectric layer, where the slit openings expose a doped region of the substrate. The method further includes replacing the second dielectric layer through the slit openings with a conductor layer to convert the alternating dielectric layer stack to an alternating dielectric/conductor layer stack, filling the slit openings with a conductor to form slit structures, forming a staircase structure in the alternating dielectric layer stack, where the staircase structure comprises levels. Further the method includes, forming a world line contact on each of the levels of the staircase structure, forming local contacts over the channel and slit structures, and forming one or more contact layers over the local contacts, each word line, and each TAC structure.

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[0118] In some embodiments, forming the opening in the alternating dielectric layer stack includes performing a dry etch process.

[0119] In some embodiments, the alternating dielectric/conductor layer stack abuts a sidewall of the dielectric structure.

[0120] In some embodiments, the dielectric structure abuts a sidewall surface of each TAC structure.

[0121] In some embodiments, a 3D memory device includes a substrate with an isolation structure; an alternating conductor/dielectric layer stack disposed on the substrate; a dielectric structure extending vertically through the alternating conductor/dielectric layer stack over the isolation structure, where the alternating conductor/dielectric layer stack abuts a sidewall surface of the dielectric structure and the dielectric structure is formed of a dielectric material; channel structures extending vertically through the alternating conductor/dielectric layer stack; and through array contacts extending vertically through the dielectric and the isolation structures.

[0122] In some embodiments, a 3D memory device further includes a staircase structure disposed in the alternating conductor/dielectric layer stack, where the staircase structures includes levels with each level having a conductor layer thereon; a word line contact disposed on each conductor layer of the staircase structure; and a local contact disposed on each channel structure and slit structure.

[0123] In some embodiments, the dielectric structure abuts a sidewall of the each TAC.

[0124] In some embodiments, the dielectric structure includes a through array contact region of the 3D memory device.

[0125] The foregoing description of the specific embodiments will so fully reveal the general nature of the present disclosure that others can, by applying knowledge within the skill of the art, readily modify and/or adapt for various applications such specific embodiments, without undue experimentation, without departing from the general concept of the present disclosure. Therefore, such adaptations and modifications are intended to be within the meaning and range of equivalents of the disclosed embodiments, based on the teaching and guidance presented herein. It is to be understood that the phraseology or terminology herein is for the purpose of description and not of limitation, such that the terminology or phraseology of the present specification is to be interpreted by the skilled artisan in light of the teachings and guidance.

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[0126] Embodiments of the present disclosure have been described above with the aid of functional building blocks illustrating the implementation of specified functions and relationships thereof. The boundaries of these functional building blocks have been arbitrarily defined herein for the convenience of the description. Alternate boundaries can be defined so long as the specified functions and relationships thereof are appropriately performed.

[0127] The Summary and Abstract sections may set forth one or more but not all exemplary embodiments of the present disclosure as contemplated by the inventor(s), and thus, are not intended to limit the present disclosure and the appended claims in any way.

[0128] The breadth and scope of the present disclosure should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	4123.0190001
	Application Number	
Title of Invention	THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	4123.0190001
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Attorney Docket Number	4123.0190001	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	15	**Suggested Figure for Publication (if any)**	

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For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

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Customer Number	26111		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Continuation of	PCT/CN2018/085421	2018-05-03

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button.

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

			Remove
Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button.

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Micron v. YMTC
IPR2024-00909

PTO/AIA/14 (02-18)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	4123.0190001
	Application Number	
Title of Invention	THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES	

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

PTO/AIA/14 (02-18)
Approved for use through 11/30/2020. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	4123.0190001
	Application Number	
Title of Invention	THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

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PTO/AIA/14 (02-18)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	4123.0190001
	Application Number	
Title of Invention	THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

○ Assignee	○ Legal Representative under 35 U.S.C. 117	○ Joint Inventor
◉ Person to whom the inventor is obligated to assign.	○ Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

Organization Name	Yangtze Memory Technologies Co., Ltd.		
Mailing Address Information For Applicant:			
Address 1	18 Gaoxin 4th Road		
Address 2	East Lake High-Tech Development Zone		
City	Wuhan, Hubei	**State/Province**	
Country	CN	Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button.

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

PTO/AIA/14 (02-18)
Approved for use through 11/30/2020. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	4123.0190001
	Application Number	
Title of Invention	THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES	

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

If the Assignee or Non-Applicant Assignee is an Organization check here. ☒

Organization Name	Yangtze Memory Technologies Co., Ltd.

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1	18 Gaoxin 4th Road		
Address 2	East Lake High-Tech Development Zone		
City	Wuhan, Hubei	**State/Province**	
Country i	CN	Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button.

Signature:

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Donald J. Featherstone/			Date (YYYY-MM-DD)	2018-07-27
First Name	Donald	Last Name	Featherstone	Registration Number	33,876

Additional Signature may be generated within this form by selecting the Add button.

Micron Ex. 1002, p. 71
Micron v. YMTC
IPR2024-00909

PTO/AIA/14 (02-18)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	4123.0190001
	Application Number	
Title of Invention	THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES	

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1 The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3 A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent CooperationTreaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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Micron v. YMTC
IPR2024-00909

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors: TAO *et al.*	Confirmation No.: *To Be Assigned*
Applicant: Yangtze Memory Technologies Co., Ltd.	Art Unit: *To Be Assigned*
Application No.: *To Be Assigned*	Examiner: *To Be Assigned*
(Continuation of Appl. No. PCT/CN2018/085421; Filed: May 3, 2018)	Atty. Docket: 4123.0190001
Filing Date: *Herewith*	

Title: **THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES**

Authorization to Treat a Reply as Incorporating an Extension of Time Under 37 C.F.R. § 1.136(a)(3)

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Commissioner:

The U.S. Patent and Trademark Office is hereby authorized to treat any concurrent or future reply that requires a petition for an extension of time under this paragraph for its timely submission, as incorporating a petition for extension of time for the appropriate length of time. The U.S. Patent and Trademark Office is hereby authorized to charge all required extension of time fees to our Deposit Account No. 19-0036, if such fees are not otherwise provided for in such reply.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

Date: 7/27/18

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600
9714859_1.docx

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82A (07-13)
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TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5, unless the application number and filing date are identified in the Power of Attorney by Applicant form. If neither form PTO/AIA/82A nor form PTO/AIA82B identifies the application to which the Power of Attorney is directed, the Power of Attorney will not be recognized in the application.

Application Number	16/047,182
Filing Date	July 27, 2018
First Named Inventor	Qian TAO
Title	THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES
Art Unit	To Be Assigned
Examiner Name	To Be Assigned
Attorney Docket Number	4123.0190001

SIGNATURE of Applicant or Patent Practitioner

Signature	/Michael D. Specht/	Date (Optional)	
Name	Michael D. Specht	Registration Number	54,463
Title (if Applicant is a juristic entity)	Attorney for Applicant		
Applicant Name (if Applicant is a juristic entity)	Yangtze Memory Technologies Co., Ltd.		

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.

☑ *Total of one (1) forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82B (07-13)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☑ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above: 26111

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☑ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number: 26111

OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

Yangtze Memory Technologies Co., Ltd.

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☑ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

✓ 1 **SIGNATURE of Applicant for Patent**

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature		Date (Optional)	
Name	Simon Shi-Ning Yang		
Title	CEO		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☐ Total of forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt

EFS ID:	33321916
Application Number:	16047182
International Application Number:	
Confirmation Number:	7800
Title of Invention:	THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES
First Named Inventor/Applicant Name:	Qian TAO
Customer Number:	26111
Filer:	Michael David Specht/Angela Robertson
Filer Authorized By:	Michael David Specht
Attorney Docket Number:	4123.0190001
Receipt Date:	30-JUL-2018
Filing Date:	
Time Stamp:	17:29:16
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	41230190001_transmittal.pdf	164277 25976779e2f265413a6c46196a8de93c981fa20b	no	1
Warnings:					

Information:					
2	Power of Attorney	41230190001_Transmittal_POA.pdf	133464 34b3f3e4e971568244948f252e764f97d6e09ecf	no	1
Warnings:					
Information:					
3	Power of Attorney	4123POA.pdf	1272778 16c3979f1c50404839c539a781116cedec7f7467	no	1
Warnings:					
Information:					
			Total Files Size (in bytes):	1570519	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

MICHAEL D. SPECHT
DIRECTOR
(202) 772-8756
MSPECHT@STERNEKESSLER.COM

July 30, 2018

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Confirmation No. 7800
Art Unit To Be Assigned

Re: U.S. Utility Patent Application
Appl. No. 16/047,182; Filing Date: July 27, 2018
For: **THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES**
Inventors: TAO *et al.*
Our Ref: 4123.0190001

Commissioner:

Transmitted herewith for appropriate action is a document entitled ***An executed Power of Attorney by Applicant form (PTO/AIA/82B) and the Transmittal for Power of Attorney form (PTO/AIA/82A)***, which is submitted electronically.

In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency and any additional fees required to continue prosecution or appeal of this application (including issue fee, fees for net addition of claims or forwarding to appeal) or credit any overpayment to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Michael D. Specht/

Michael D. Specht
Attorney for Applicant
Registration No. 54,463

MDS/Y-G/amr
Enclosure

9737901_1.docx

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
16/047,182	07/27/2018	2872	0.00	4123.0190001	20	3

CONFIRMATION NO. 7800

26111
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

FILING RECEIPT

OC000000102086590

Date Mailed: 09/06/2018

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Qian TAO, Wuhan, CHINA;
Yushi HU, Wuhan, CHINA;
Zhenyu LU, Wuhan, CHINA;
Li Hong XIAO, Wuhan, CHINA;
Xiaowang DAI, Wuhan, CHINA;
Yu Ting ZHOU, Wuhan, CHINA;
Zhao Hui TANG, Wuhan, CHINA;
Mei Lan GUO, Wuhan, CHINA;
ZhiWu TANG, Wuhan, CHINA;
Qinxiang WEI, Wuhan, CHINA;
Qianbing XU, Wuhan, CHINA;
Sha Sha LIU, Wuhan, CHINA;
Jian Hua SUN, Wuhan, CHINA;
Enbo WANG, Wuhan, CHINA;

Applicant(s)

Yangtze Memory Technologies Co., Ltd., Wuhan, CHINA

Assignment For Published Patent Application

Yangtze Memory Technologies Co., Ltd., Wuhan, CHINA

Power of Attorney: The patent practitioners associated with Customer Number 26111

Domestic Priority data as claimed by applicant

This application is a CON of PCT/CN2018/085421 05/03/2018

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.

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Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 09/05/2018

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 16/047,182**

Projected Publication Date: To Be Determined - pending completion of Missing Parts

Non-Publication Request: No

Early Publication Request: No

Title

THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES

Preliminary Class

359

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign

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patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

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SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 16/047,182

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	300
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	660
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	760
TOTAL CLAIMS (37 CFR 1.16(i))	22 minus 20 =	* 2			OR	x 100 =	200
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*				x 460 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							820
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	2740

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/047,182	07/27/2018	Qian TAO	4123.0190001

CONFIRMATION NO. 7800

26111
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

FORMALITIES LETTER

OC000000102086591

Date Mailed: 09/06/2018

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
- The application search fee must be submitted.
- The application examination fee must be submitted.
- Additional claim fees of $ **1020** as an undiscounted entity, including any required multiple dependent claim fee, are required. Applicant must submit the additional claim fees or cancel the additional claims for which fees are due.
- Surcharge as set forth in 37 CFR 1.16(f) must be submitted.
  The surcharge is due for any one of:
  - late submission of the basic filing fee, search fee, or examination fee,
  - late submission of inventor's oath or declaration,
  - filing an application that does not contain at least one claim on filing, or
  - submission of an application filed by reference to a previously filed application.

SUMMARY OF FEES DUE:

The fee(s) required within **TWO MONTHS** from the date of this Notice to avoid abandonment is/are itemized below. No entity status discount is in effect. If applicant is qualified for small entity status, a written assertion of small entity status must be submitted to establish small entity status. (See 37 CFR 1.27). If applicant is qualified for micro entity status, an acceptable Certification of Micro Entity Status must be submitted to establish micro entity status. (See 37 CFR 1.29 and forms PTO/SB/15A and 15B.)

- $ **300** basic filing fee.
- $ **160** surcharge.
- $ **660** search fee.
- $ **760** examination fee.
- $ **200** for **2** total claims over 20.
- $ **820** for multiple dependent claim surcharge.

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- $(**0**) previous unapplied payment amount.
- $ **2900** TOTAL FEE BALANCE DUE.

Items Required To Avoid Processing Delays:

Applicant is notified that the above-identified application contains the deficiencies noted below. No period for reply is set forth in this notice for correction of these deficiencies. However, if a deficiency relates to the inventor's oath or declaration, the applicant must file an oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each actual inventor no later than the expiration of the time period set in the "Notice of Allowability" to avoid abandonment. See 37 CFR 1.53(f).

- A properly executed inventor's oath or declaration has not been received for the following inventor(s):
  Qian TAO
  Yushi HU
  Zhenyu LU
  Li Hong XIAO
  Xiaowang DAI
  Yu Ting ZHOU
  Zhao Hui TANG
  Mei Lan GUO
  ZhiWu TANG
  Qinxiang WEI
  Qianbing XU
  Sha Sha LIU
  Jian Hua SUN
  Enbo WANG

Replies must be received in the USPTO within the set time period or must include a proper Certificate of Mailing or Transmission under 37 CFR 1.8 with a mailing or transmission date within the set time period. For more information and a suggested format, see Form PTO/SB/92 and MPEP 512.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web, including a copy of this Notice and selecting the document description "Applicant response to Pre-Exam Formalities Notice". https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html

For more information about EFS-Web please call the USPTO Electronic Business Center at 1-866-217-9197 or visit our website at http://www.uspto.gov/ebc.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

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/rnegga/

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MULTIPLE DEPENDENT CLAIM FEE CALCULATION SHEET

Substitute for Form PTO-1360
(For use with Form PTO/SB/06)

Application Number	Filing Date
16047182	
Applicant(s) Qian TAO	

* May be used for additional claims or amendments

CLAIMS	AS FILED		AFTER FIRST AMENDMENT		AFTER SECOND AMENDMENT	
	Indep	Depend	Indep	Depend	Indep	Depend
1	1					
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Total Indep	3		0		0	
Total Depend	19	↵	0	↵	0	↵
Total Claims	22		0		0	

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PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT5269241

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
QIAN TAO	09/12/2018
YUSHI HU	09/12/2018
ZHENYU LU	09/12/2018
LI HONG XIAO	09/12/2018
XIAOWANG DAI	09/12/2018
YU TING ZHOU	09/12/2018
ZHAO HUI TANG	09/12/2018
MEI LAN GUO	09/12/2018
ZHIWU TANG	09/12/2018
QINXIANG WEI	09/12/2018
QIANBING XU	09/12/2018
SHA SHA LIU	09/12/2018
JIAN HUA SUN	09/12/2018
ENBO WANG	09/12/2018

RECEIVING PARTY DATA

Name:	YANGTZE MEMORY TECHNOLOGIES CO., LTD.
Street Address:	18 GAOXIN 4TH ROAD
City:	WUHAN, HUBEI
State/Country:	CHINA

PROPERTY NUMBERS Total: 1

Property Type	Number
Application Number:	16047182

CORRESPONDENCE DATA

Fax Number: (202)371-2540

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 202.371.2600
Email: ygao@sternekessler.com, ttopssecretary1@sternekessler.com
Correspondent Name: STERNE KESSLER GOLDSTEIN & FOX P.L.L.C
Address Line 1: 1100 NEW YORK AVENUE, N.W.

Address Line 4:	WASHINGTON, D.C. 20005
ATTORNEY DOCKET NUMBER:	4123.0190001
NAME OF SUBMITTER:	DONALD J. FEATHERSTONE
SIGNATURE:	/Donald J. Featherstone/
DATE SIGNED:	12/06/2018
	This document serves as an Oath/Declaration (37 CFR 1.63).

Total Attachments: 5
source=Assignment-4123-0190001#page1.tif
source=Assignment-4123-0190001#page2.tif
source=Assignment-4123-0190001#page3.tif
source=Assignment-4123-0190001#page4.tif
source=Assignment-4123-0190001#page5.tif

Atty. Docket No. 4123.0190001

COMBINED DECLARATION AND ASSIGNMENT

DECLARATION

As the below named inventors, I hereby declare that:

This declaration is directed to:

☐ The attached application, or

☒ United States application or PCT international application number 16/047,182

filed on July 27, 2018

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. § 1001 by fine or imprisonment of not more than five (5) years, or both.

ASSIGNMENT

In consideration of the sum of One Dollar ($1.00) or equivalent and other good and valuable consideration paid to each of the below named inventors, each of the below named inventors, hereby sell and assign to **Yangtze Memory Technologies Co., Ltd.**, a corporation formed under the laws of China, whose mailing address is 18 Gaoxin 4th Road, East Lake High-Tech Development Zone, Wuhan, Hubei, China (hereafter referred to as the Assignee), his/her entire right, title and interest, including the right to sue for past infringement and to collect for all past, present and future damages, for the United States of America (as defined in 35 U.S.C. § 100) and throughout the world,

(a) in the invention(s) known as **THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES** for which application(s) for patent in the United States of America is identified above, in any and all applications thereon, in any and all Letters Patent(s) therefor, and

(b) in any and all applications that claim the benefit of the patent application identified above in part (a), including non-provisional applications, continuing (continuation, divisional, or continuation-in-part) applications, reissues, extensions, renewals and reexaminations of the patent application or Letters Patent therefor listed above in part (a), to the full extent of the term or terms for which Letters Patents issue, and

(c) in any and all inventions described in the patent application identified above in part (a), and in any and all forms of intellectual and industrial property protection derivable from such patent application, and that are derivable from any and all continuing applications, reissues, extensions, renewals and reexaminations of such patent application, including, without limitation, patents, applications, utility models, inventor's certificates, and designs together with the right to file applications therefor; and including the right to claim the same priority rights from any previously filed applications under the International Agreement for the Protection of Industrial Property, or any other international agreement, or the domestic laws of the country in which any such application is filed, as may be applicable;

all such rights, title and interest to be held and enjoyed by the above-named Assignee, its successors, legal representatives and assigns to the same extent as all such rights, title and interest would have been held and enjoyed by the Assignor had this assignment and sale not been made.

The below named inventors agree to execute all papers necessary in connection with the application(s) and any non-provisional, continuing (continuation, divisional, or continuation-in-part), reissue, reexamination or corresponding application(s) thereof and also to execute separate assignments in connection with such application(s) as the Assignee may deem necessary or expedient.

The below named inventors agree to execute all papers necessary in connection with any patent enforcement action (judicial or otherwise) related to the application(s) or any non-provisional, continuing (continuation, divisional, or continuation-in-part), reissue or reexamination application(s) thereof and to cooperate with the Assignee in every way possible in obtaining evidence and going forward with such patent enforcement action.

The below named inventors hereby represent that he/she has full right to convey the entire interest herein assigned, and that he/she has not executed, and will not execute, any agreement in conflict therewith.

The below named inventors hereby represent that he/she understands that the patent practitioners associated with **CUSTOMER NUMBER 26111** are the legal representatives of, and attorneys for, the assignee, and are NOT the legal representatives of, and attorneys for, the inventors.

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IN WITNESS WHEREOF, executed by the below named inventors on the date opposite his/her name.

LEGAL NAME OF INVENTOR

Inventor: **Qian TAO** Date: 2018.9.12

Signature of Inventor: Qian Tao

LEGAL NAME OF INVENTOR

Inventor: **Yushi HU** Date: 2018 9 12

Signature of Inventor:

LEGAL NAME OF INVENTOR

Inventor: **Zhenyu LU** Date: 2018.09.12.

Signature of Inventor: Zhenyu Lu

LEGAL NAME OF INVENTOR

Inventor: **Li Hong XIAO** Date: 2018, 09, 12.

Signature of Inventor: Lihong Xiao.

LEGAL NAME OF INVENTOR

Inventor: **Xiaowang DAI** Date: 2018.9.12

Signature of Inventor: Xiaowang DAI

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Micron v. YMTC
IPR2024-00909

LEGAL NAME OF INVENTOR

Inventor: **Yu Ting ZHOU** Date: 2018.09.12

Signature of Inventor: Yu Ting ZHOU 2018.09.12

LEGAL NAME OF INVENTOR

Inventor: **Zhao Hui TANG** Date: 2018.09.12

Signature of Inventor: ZhaoHui TANG

LEGAL NAME OF INVENTOR

Inventor: **Mei Lan GUO** Date: 2018.9.12

Signature of Inventor:

LEGAL NAME OF INVENTOR

Inventor: **ZhiWu TANG** Date: 2018.09.12

Signature of Inventor: ZhiWu TANG 2018.09.12

LEGAL NAME OF INVENTOR

Inventor: **Qinxiang WEI** Date: 2018.09.12

Signature of Inventor: Qinxiang WEI

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Micron v. YMTC
IPR2024-00909

LEGAL NAME OF INVENTOR

Inventor: **Qianbing XU** Date: 2018.9.12

Signature of Inventor: Qianbing XU

LEGAL NAME OF INVENTOR

Inventor: **Sha Sha LIU** Date: 2018.9.12

Signature of Inventor: Sha Sha LIU

LEGAL NAME OF INVENTOR

Inventor: **Jian Hua SUN** Date: 2018/9/12

Signature of Inventor: Jian hua Sun

LEGAL NAME OF INVENTOR

Inventor: **EnBo WANG** Date: 2018.9.12

Signature of Inventor: Wang Enbo

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Micron v. YMTC
IPR2024-00909

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/047,182	07/27/2018	Qian TAO	4123.0190001

CONFIRMATION NO. 7800

26111
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

FORMALITIES LETTER

OC000000102086591

Date Mailed: 09/06/2018

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
- The application search fee must be submitted.
- The application examination fee must be submitted.
- Additional claim fees of $ **1020** as an undiscounted entity, including any required multiple dependent claim fee, are required. Applicant must submit the additional claim fees or cancel the additional claims for which fees are due.
- Surcharge as set forth in 37 CFR 1.16(f) must be submitted.
  The surcharge is due for any one of:
  - late submission of the basic filing fee, search fee, or examination fee,
  - late submission of inventor's oath or declaration,
  - filing an application that does not contain at least one claim on filing, or
  - submission of an application filed by reference to a previously filed application.

SUMMARY OF FEES DUE:

The fee(s) required within **TWO MONTHS** from the date of this Notice to avoid abandonment is/are itemized below. No entity status discount is in effect. If applicant is qualified for small entity status, a written assertion of small entity status must be submitted to establish small entity status. (See 37 CFR 1.27). If applicant is qualified for micro entity status, an acceptable Certification of Micro Entity Status must be submitted to establish micro entity status. (See 37 CFR 1.29 and forms PTO/SB/15A and 15B.)

- $ **300** basic filing fee.
- $ **160** surcharge.
- $ **660** search fee.
- $ **760** examination fee.
- $ **200** for **2** total claims over 20.
- $ **820** for multiple dependent claim surcharge.

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- $(**0**) previous unapplied payment amount.
- $ **2900** TOTAL FEE BALANCE DUE.

Items Required To Avoid Processing Delays:

Applicant is notified that the above-identified application contains the deficiencies noted below. No period for reply is set forth in this notice for correction of these deficiencies. However, if a deficiency relates to the inventor's oath or declaration, the applicant must file an oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each actual inventor no later than the expiration of the time period set in the "Notice of Allowability" to avoid abandonment. See 37 CFR 1.53(f).

- A properly executed inventor's oath or declaration has not been received for the following inventor(s):
  Qian TAO
  Yushi HU
  Zhenyu LU
  Li Hong XIAO
  Xiaowang DAI
  Yu Ting ZHOU
  Zhao Hui TANG
  Mei Lan GUO
  ZhiWu TANG
  Qinxiang WEI
  Qianbing XU
  Sha Sha LIU
  Jian Hua SUN
  Enbo WANG

Replies must be received in the USPTO within the set time period or must include a proper Certificate of Mailing or Transmission under 37 CFR 1.8 with a mailing or transmission date within the set time period. For more information and a suggested format, see Form PTO/SB/92 and MPEP 512.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web, including a copy of this Notice and selecting the document description "Applicant response to Pre-Exam Formalities Notice". https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html

For more information about EFS-Web please call the USPTO Electronic Business Center at 1-866-217-9197 or visit our website at http://www.uspto.gov/ebc.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

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/rnegga/

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PTO/AIA/22 (03-13)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PETITION FOR EXTENSION OF TIME UNDER 37 CFR 1.136(a)	Docket Number (Optional) 4123.0190001
Application Number 16/047,182	Filed July 27, 2018
For THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES	
Art Unit 2872	Examiner To Be Assigned

This is a request under the provisions of 37 CFR 1.136(a) to extend the period for filing a reply in the above-identified application.

The requested extension and fee are as follows (check time period desired and enter the appropriate fee below):

		Fee	Small Entity Fee	Micro Entity Fee	
☑	One month (37 CFR 1.17(a)(1))	$200	$100	$50	$ 200.00
☐	Two months (37 CFR 1.17(a)(2))	$600	$300	$150	$
☐	Three months (37 CFR 1.17(a)(3))	$1,400	$700	$350	$
☐	Four months (37 CFR 1.17(a)(4))	$2,200	$1,100	$550	$
☐	Five months (37 CFR 1.17(a)(5))	$3,000	$1,500	$750	$

☐ Applicant asserts small entity status. See 37 CFR 1.27.

☐ Applicant certifies micro entity status. See 37 CFR 1.29.
Form PTO/SB/15A or B or equivalent must either be enclosed or have been submitted previously.

☐ A check in the amount of the fee is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☐ The Director has already been authorized to charge fees in this application to a Deposit Account.

☑ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number 19-0036.

☑ Payment made via EFS-Web.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

I am the

☐ applicant.

☑ attorney or agent of record. Registration number 33,876.

☐ attorney or agent acting under 37 CFR 1.34. Registration number _____.

/Donald J. Featherstone/ — Signature

12/6/18 — Date

Donald J. Featherstone — Typed or printed name

(202) 371-2600 — Telephone Number

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. Submit multiple forms if more than one signature is required, see below*.

☑ * Total of 1 (one) forms are submitted.

This collection of information is required by 37 CFR 1.136(a). The information is required to obtain or retain a benefit by the public, which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 6 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop PCT, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Atty. Docket No. 4123.0190001

COMBINED DECLARATION AND ASSIGNMENT

DECLARATION

As the below named inventors, I hereby declare that:

This declaration is directed to:

☐ The attached application, or

☒ United States application or PCT international application number 16/047,182

filed on July 27, 2018

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. § 1001 by fine or imprisonment of not more than five (5) years, or both.

ASSIGNMENT

In consideration of the sum of One Dollar ($1.00) or equivalent and other good and valuable consideration paid to each of the below named inventors, each of the below named inventors, hereby sell and assign to **Yangtze Memory Technologies Co., Ltd.**, a corporation formed under the laws of China, whose mailing address is 18 Gaoxin 4th Road, East Lake High-Tech Development Zone, Wuhan, Hubei, China (hereafter referred to as the Assignee), his/her entire right, title and interest, including the right to sue for past infringement and to collect for all past, present and future damages, for the United States of America (as defined in 35 U.S.C. § 100) and throughout the world,

(a) in the invention(s) known as **THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES** for which application(s) for patent in the United States of America is identified above, in any and all applications thereon, in any and all Letters Patent(s) therefor, and

(b) in any and all applications that claim the benefit of the patent application identified above in part (a), including non-provisional applications, continuing (continuation, divisional, or continuation-in-part) applications, reissues, extensions, renewals and reexaminations of the patent application or Letters Patent therefor listed above in part (a), to the full extent of the term or terms for which Letters Patents issue, and

(c) in any and all inventions described in the patent application identified above in part (a), and in any and all forms of intellectual and industrial property protection derivable from such patent application, and that are derivable from any and all continuing applications, reissues, extensions, renewals and reexaminations of such patent application, including, without limitation, patents, applications, utility models, inventor's certificates, and designs together with the right to file applications therefor; and including the right to claim the same priority rights from any previously filed applications under the International Agreement for the Protection of Industrial Property, or any other international agreement, or the domestic laws of the country in which any such application is filed, as may be applicable;

all such rights, title and interest to be held and enjoyed by the above-named Assignee, its successors, legal representatives and assigns to the same extent as all such rights, title and interest would have been held and enjoyed by the Assignor had this assignment and sale not been made.

The below named inventors agree to execute all papers necessary in connection with the application(s) and any non-provisional, continuing (continuation, divisional, or continuation-in-part), reissue, reexamination or corresponding application(s) thereof and also to execute separate assignments in connection with such application(s) as the Assignee may deem necessary or expedient.

The below named inventors agree to execute all papers necessary in connection with any patent enforcement action (judicial or otherwise) related to the application(s) or any non-provisional, continuing (continuation, divisional, or continuation-in-part), reissue or reexamination application(s) thereof and to cooperate with the Assignee in every way possible in obtaining evidence and going forward with such patent enforcement action.

The below named inventors hereby represent that he/she has full right to convey the entire interest herein assigned, and that he/she has not executed, and will not execute, any agreement in conflict therewith.

The below named inventors hereby represent that he/she understands that the patent practitioners associated with **CUSTOMER NUMBER 26111** are the legal representatives of, and attorneys for, the assignee, and are NOT the legal representatives of, and attorneys for, the inventors.

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IN WITNESS WHEREOF, executed by the below named inventors on the date opposite his/her name.

LEGAL NAME OF INVENTOR

Inventor: **Qian TAO** Date: 2018.9.12

Signature of Inventor: Qian Tao

LEGAL NAME OF INVENTOR

Inventor: **Yushi HU** Date: 2018.9.12

Signature of Inventor:

LEGAL NAME OF INVENTOR

Inventor: **Zhenyu LU** Date: 2018.09.12.

Signature of Inventor: Zhenyu Lu

LEGAL NAME OF INVENTOR

Inventor: **Li Hong XIAO** Date: 2018.09.12.

Signature of Inventor: Li-hong Xiao

LEGAL NAME OF INVENTOR

Inventor: **Xiaowang DAI** Date: 2018.9.12

Signature of Inventor: Xiaowang DAI

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IPR2024-00909

LEGAL NAME OF INVENTOR

Inventor: **Yu Ting ZHOU** Date: 2018. 09. 12

Signature of Inventor: Yu Ting ZHOU 2018. 09. 12

LEGAL NAME OF INVENTOR

Inventor: **Zhao Hui TANG** Date: 2018. 09. 12

Signature of Inventor: ZhaoHui TANG

LEGAL NAME OF INVENTOR

Inventor: **Mei Lan GUO** Date: 2018. 9. 12

Signature of Inventor:

LEGAL NAME OF INVENTOR

Inventor: **ZhiWu TANG** Date: 2018. 09. 12

Signature of Inventor: ZhiWu TANG 2018. 09. 12

LEGAL NAME OF INVENTOR

Inventor: **Qinxiang WEI** Date: 2018. 09. 12

Signature of Inventor: Qinxiang WEI

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IPR2024-00909

LEGAL NAME OF INVENTOR

Inventor: **Qianbing XU** Date: 2018.9.12

Signature of Inventor: Qianbing XU

LEGAL NAME OF INVENTOR

Inventor: **Sha Sha LIU** Date: 2018.9.12

Signature of Inventor: Sha Sha LIU

LEGAL NAME OF INVENTOR

Inventor: **Jian Hua SUN** Date: 2018/9/12

Signature of Inventor: Jian hua Sun

LEGAL NAME OF INVENTOR

Inventor: **EnBo WANG** Date: 2018.9.12

Signature of Inventor: Wang Enbo

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors: TAO *et al.*	Confirmation No.: 7800
Applicant: Yangtze Memory Technologies Co., Ltd.	Art Unit: 2872
Application No.: 16/047,182	Examiner: *To Be Assigned*
Filing Date: July 27, 2018	Atty. Docket: 4123.0190001

Title: **THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES**

Preliminary Amendment Under 37 C.F.R. § 1.115

Mail Stop Amendment

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Commissioner:

In advance of prosecution, Applicant submits the following amendments and remarks.

It is not believed that extensions of time are required beyond those that may otherwise be provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any additional fees required to continue prosecution or appeal of this application (including issue fee, fees for net addition of claims or forwarding to appeal) are hereby authorized to be charged to our Deposit Account No. 19-0036.

Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Original) A three-dimensional (3D) memory device, comprising:

a semiconductor substrate;

an alternating layer stack disposed on the semiconductor substrate;

a dielectric structure on an isolation region of the substrate and extending vertically through the alternating layer stack, wherein the alternating layer stack abuts a sidewall surface of the dielectric structure and the dielectric structure is formed of a dielectric material;

one or more through array contacts (TACs) extending vertically through the dielectric structure and the isolation region; and

one or more channel structures extending vertically through the alternating layer stack.

2. (Original) The 3D memory device of claim 1, further comprising:

an epitaxial layer formed between each of the one or more channel structures and the semiconductor substrate;

an etch stop plug disposed on each of the one or more channel structures;

a staircase structure disposed in the alternating layer; and

one or more contact layers disposed on the one or more TACs, channel structures, and slit structures.

3. (Original) The 3D memory device of claim 1, wherein the dielectric structure abuts a sidewall surface of the TACs.

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4. (Currently Amended) The 3D memory device of ~~claims 1 or 2~~ claim 1, wherein the 3D memory device is a NAND 3D memory device.

5. (Original) The 3D memory device of claim 1, wherein the alternating layer stack comprises alternating pairs of a dielectric and a conductor layer.

6. (Currently Amended) The 3D memory device of [[claims]] claim 1, wherein the dielectric material is silicon oxide.

7. (Currently Amended) The 3D memory device of ~~claims 1 or 3~~ claim 1, wherein the dielectric structure comprises an oxide.

8. (Original) The 3D memory device of claim 1, wherein the dielectric structure defines a through array contact region within the 3D memory device.

9. (Original) The 3D memory device of claim 1, wherein the dielectric structure has a footprint equal to or smaller than the isolation region.

10. (Original) A method for forming a 3D memory device, the method comprising:

forming an isolation structure on a substrate;

disposing an alternating dielectric layer stack on the substrate, the alternating dielectric layer stack comprising pairs of a first dielectric layer and a second dielectric layer different from the first dielectric layer;

forming a channel structure extending vertically in the alternating dielectric layer stack;

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forming an opening in the alternating dielectric layer stack, wherein the opening exposes the isolation structure;

filling the opening with a dielectric layer to form a dielectric structure as a through array contact (TAC) region of the 3D memory device;

removing portions of the dielectric structure and the isolation structure until the substrate is exposed to form a TAC opening that vertically extends through the dielectric structure and the isolation structure; and

filling the TAC opening with a conductor to form a TAC structure in the TAC region, wherein the TAC structure is in contact with the substrate.

11. (Original) The method of claim 10, wherein before forming the TAC opening the method further comprises:

forming slit openings extending vertically in the alternating dielectric layer stack, wherein the slit openings expose a doped region of the substrate;

replacing the second dielectric layer through the one or more slit openings with a conductor layer to convert the alternating dielectric layer stack to an alternating dielectric/conductor layer stack; and

filling the one or more slit openings with a conductor to form one or more slit structures extending vertically in the alternating dielectric/conductor layer stack.

12. (Original) The method of claim 10, wherein before forming the channel structure performing a trim-etch process to form a staircase structure in the alternating dielectric layer stack.

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13. (Original) The method of claim 10, wherein filling the opening with the dielectric layer comprises depositing the dielectric layer with a chemical vapor deposition, a plasma-enhanced chemical vapor deposition, or a physical vapor deposition process.

14. (Original) The method of claim 10, wherein filling the opening with the dielectric layer comprises forming an oxide.

15. (Original) The method of claim 10, wherein the first dielectric layer comprises an oxide and the second dielectric layer comprises a nitride.

16. (Original) A three-dimensional (3D) memory device, comprising:

a substrate with an isolation structure;

an alternating conductor/dielectric layer stack disposed on the substrate;

a dielectric structure on the isolation structure and extending vertically through the alternating conductor/dielectric layer stack, wherein the alternating conductor/dielectric layer stack abuts a sidewall surface of the dielectric structure and the dielectric structure is formed of a dielectric material;

channel structures extending vertically through the alternating conductor/dielectric layer stack; and

through array contacts (TAC) extending vertically through the dielectric and the isolation structures.

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17. (Original) The 3D memory device of claim 16, further comprising:

a staircase structure disposed in the alternating conductor/dielectric layer stack, wherein the staircase structures comprises levels with each level having a conductor layer thereon;

a word line contact disposed on each conductor layer of the staircase structure; and

a local contact disposed on each channel structure and slit structure.

18. (Original) The 3D memory device of claim 16, wherein the dielectric structure abuts a sidewall of the each TAC.

19. (Original) The 3D memory device of claim 16, wherein the dielectric structure comprises a through array contact region of the 3D memory device.

20. (Original) The 3D memory device of claim 16, further comprising:

an etch stop plug interposed between each local contact and each channel structure; and

an epitaxial layer disposed between each channel structure and the substrate.

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Remarks

Upon entry of the foregoing amendment, claims 1-20 are pending in the application, with claims 1, 10, and 16 being the independent claims. Claims 4 and 7 are sought to be amended to remove the multiple claim dependency. Claim 6 is sought to be amended to correct a typological error. These changes are believed to introduce no new matter, and their entry is respectfully requested.

Conclusion

Prompt and favorable consideration of this Preliminary Amendment is respectfully requested. Applicant believes the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

Date: 12/6/18

1100 New York Avenue, N.W.
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(202) 371-2600

10401726_1.docx

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Electronic Patent Application Fee Transmittal

Application Number:	16047182
Filing Date:	27-Jul-2018
Title of Invention:	THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES
First Named Inventor/Applicant Name:	Qian TAO
Filer:	Donald J. Featherstone/Catherine Saunders
Attorney Docket Number:	4123.0190001

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	300	300
UTILITY SEARCH FEE	1111	1	660	660
UTILITY EXAMINATION FEE	1311	1	760	760
Pages:				
Claims:				
Miscellaneous-Filing:				
LATE FILING FEE FOR OATH OR DECLARATION	1051	1	160	160
Petition:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Extension - 1 month with $0 paid	1251	1	200	200
Miscellaneous:				
		Total in USD ($)		**2080**

Electronic Acknowledgement Receipt

EFS ID:	34502180
Application Number:	16047182
International Application Number:	
Confirmation Number:	7800
Title of Invention:	THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES
First Named Inventor/Applicant Name:	Qian TAO
Customer Number:	26111
Filer:	Donald J. Featherstone/Catherine Saunders
Filer Authorized By:	Donald J. Featherstone
Attorney Docket Number:	4123.0190001
Receipt Date:	06-DEC-2018
Filing Date:	27-JUL-2018
Time Stamp:	11:43:24
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$2080
RAM confirmation Number	120618INTEFSW11440600
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	2018-12-06-Cover-Letter-4123-0190001.PDF	229538 8e86f90740e77dec65168bcb68ccc973c6e782c4	no	2
Warnings:					
Information:					
2	Applicant Response to Pre-Exam Formalities Notice	Reply-Missing-Parts-4123-0190001.PDF	93973 f4df16e240a512e3b354ca942f3a630f4f0c2dee	no	3
Warnings:					
Information:					
3	Extension of Time	2018-12-06-EOT-4123-0190001.PDF	159107 7d13fec97a226f3f535b4dedd6843ac8a78a3c63	no	1
Warnings:					
Information:					
4	Oath or Declaration filed	2018-12-06-Declaration-4123-0190001.PDF	1447736 1eb2651d92690b5a87c1c4f32d34625798700244	no	5
Warnings:					
The page size in the PDF is too large. The pages should be 8.5 x 11 or A4. If this PDF is submitted, the pages will be resized upon entry into the Image File Wrapper and may affect subsequent processing					
Information:					
5		2018-12-06-Preliminary-Amendment-4123-0190001.PDF	126701 e99bf2e24bc326fd813f9bfb118e3d98b73d23d1	yes	7

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Preliminary Amendment	1	1
	Claims	2	6

	Applicant Arguments/Remarks Made in an Amendment		7	7	
Warnings:					
Information:					
6	Fee Worksheet (SB06)	fee-info.pdf	39265 c71e2e2eca8fa98c6f06ebfeff79284acea22d9c	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	2096320		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

DONALD J. FEATHERSTONE
DIRECTOR
(202) 772-8629
DONF@STERNEKESSLER.COM

December 6, 2018

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Confirmation No. 7800
Mail Stop Missing Parts

Re: U.S. Patent Application
Appl. No. 16/047,182; Filed: July 27, 2018
For: **THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES**
Inventors: TAO *et al.*
Our Ref: 4123.0190001

Commissioner:

In reply to the "Notice to File Missing Parts of Non-Provisional Application," dated September 6, 2018, Applicant transmit the following documents for appropriate action by the U.S. Patent and Trademark Office:

1. Online Credit Card Payment Authorization for **$2,080.00** to cover:

   $ 1,720.00 Patent Application fee (including basic filing, search and examination fees);
   $ 160.00 Surcharge for late filing fee or late Oath or Declaration;
   $ 200.00 Extension of time fees;

2. Petition for Extension of Time Under 37 C.F.R. § 1.136(a);

3. Combined Declaration and Assignment, executed by the inventors;

4. Preliminary Amendment Under 37 C.F.R. § 1.115; and

5. Copy of the Notice to File Missing Parts of Nonprovisional Application dated September 6, 2018.

The above-listed documents are filed electronically.

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Fee payment is provided through online credit card payment. The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036. If extensions of time under 37 C.F.R. § 1.136 other than those otherwise provided for herewith are required to prevent abandonment of the present patent application, then such extensions of time are hereby petitioned, and any fees therefor are hereby authorized to be charged to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

DJF/Y-G/cms
Enclosures
10401136_1.docx

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UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
16/047,182	07/27/2018	2872	1880	4123.0190001	20	3

CONFIRMATION NO. 7800

UPDATED FILING RECEIPT

26111
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

OC000000104327883

Date Mailed: 12/10/2018

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

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Applicant(s)

Yangtze Memory Technologies Co., Ltd., Wuhan, CHINA

Assignment For Published Patent Application

Yangtze Memory Technologies Co., Ltd., Wuhan, CHINA

Power of Attorney: The patent practitioners associated with Customer Number 26111

Domestic Priority data as claimed by applicant

This application is a CON of PCT/CN2018/085421 05/03/2018

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.

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IPR2024-00909

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 09/05/2018

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 16/047,182**

Projected Publication Date: 11/07/2019

Non-Publication Request: No

Early Publication Request: No

Title

THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES

Preliminary Class

359

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

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patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

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IPR2024-00909

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 16/047,182

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	300
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	660
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	760
TOTAL CLAIMS (37 CFR 1.16(i))	20 minus 20 =	*			OR	x 100 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*				x 460 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1720

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 2

Complete if Known	
Application Number	16/047,182
Filing Date	07-27-2018
First Named Inventor	Qian TAO
Art Unit	2812
Examiner Name	CHOI, CALVIN Y
Attorney Docket Number	4123.0190001

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	US1	US- 2016/0071861 A1	03-10-2016	Serov et al.	
	US2	US- 2017/0186758 A1	06-29-2017	Lee et al.	
	US3	US- 2017/0358593 A1	12-14-2017	Yu et al.	
	US4	US- 2019/0057974 A1	02-21-2019	Lu et al.	
	US5	US- 8,247,895 B2	08-21-2012	Haensch et al.	
	US6	US- 9,530,789 B2	12-27-2016	Lee et al.	
	US7	US- 9,595,531 B2	03-14-2017	Zhu et al.	
	US8	US- 9,595,667 B2	03-14-2017	Pio	
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]
	FP1	TW 201419449 A	05-16-2014	MICRON TECHNOLOGY INC		
	FP2	TW 201606388 A	02-16-2016	INTEL CORP		
	FP3	TW 201721921 A	06-16-2017	MACRONIX INT CO LTD		✓
	FP4	CN 105047668 A	11-11-2015	SAMSUNG ELECTRONICS CO LTD		
	FP5	CN 105826323 A	08-03-2016	MACRONIX INT CO LTD		✓
	FP6	CN 106910746 A	06-30-2017	YANGTZE MEMORY TECH CO LTD		

Examiner Signature		Date Considered	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 2 of 2

Complete if Known	
Application Number	16/047,182
Filing Date	07-27-2018
First Named Inventor	Qian TAO
Art Unit	2812
Examiner Name	CHOI, CALVIN Y
Attorney Docket Number	4123.0190001

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-			
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]
	FP7	CN 106920794 A	07-04-2017	YANGTZE MEMORY TECH CO LTD		✓
	FP8	CN 107887395 A	04-06-2018	YANGTZE MEMORY TECH CO LTD		
	FP9	WO 2019/104896 A1	06-06-2019	YANGTZE MEMORY TECH CO LTD		

Examiner Signature		Date Considered	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

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Application Number	16/047,182
Filing Date	07-27-2018
First Named Inventor	Qian TAO
Art Unit	2812
Examiner Name	CHOI, CALVIN Y
Attorney Docket Number	4123.0190001

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	NPL1	International Search Report and Written Opinion of the International Searching Authority directed to related International Patent Application No. PCT/CN2018/085421, mailed January 20, 2019; 9 pages.	

Examiner Signature		Date Considered	

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1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

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(19)中華民國智慧財產局
(12)發明說明書公開本 (11)公開編號：TW 201419449 A
(43)公開日： 中華民國 103 (2014) 年 05 月 16 日

(21)申請案號：102131392 (22)申請日： 中華民國 102 (2013) 年 08 月 30 日
(51)Int. Cl.： *H01L21/8239(2006.01)* *H01L27/105 (2006.01)*
H01L23/52 (2006.01)
(30)優先權：2012/08/31 美國 13/600,699
(71)申請人：美光科技公司 (美國) MICRON TECHNOLOGY, INC. (US)
美國
(72)發明人：皮歐 弗得瑞 PIO, FEDERICO (IT)
(74)代理人：陳長文
申請實體審查：有 申請專利範圍項數：30 項 圖式數：9 共 55 頁

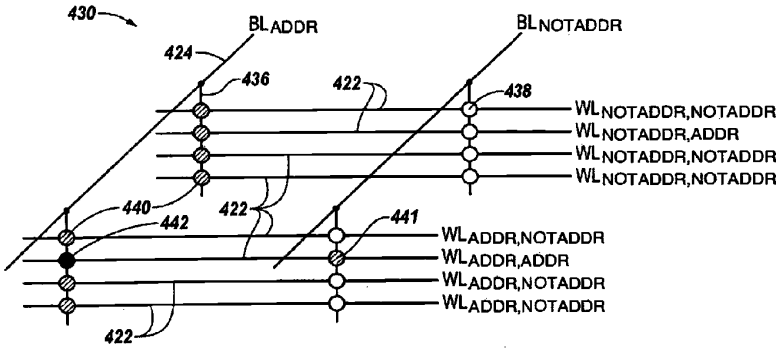
(54)名稱

三維記憶體陣列架構

THREE DIMENSIONAL MEMORY ARRAY ARCHITECTURE

(57)摘要

本發明提供三維記憶體陣列及其形成方法。一例示性三維記憶體陣列可包含：一堆疊，其包括藉由至少一絕緣材料而彼此分離之複數個第一導電線；及至少一導電延伸部，其經配置以實質上垂直於該複數個第一導電線延伸，使得該至少一導電延伸部與該複數個第一導電線之至少一者之一部分相交。圍繞該至少一導電延伸部形成儲存元件材料。圍繞該至少一導電部延伸形成單元選擇材料。



422：字線
424：位元線
430：記憶體陣列
436：導電延伸部
438：記憶體單元
440：記憶體單元
441：記憶體單元
442：記憶體單元

圖4

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Micron v. YMTC
IPR2024-00909

(19)中華民國智慧財產局
(12)發明說明書公開本 (11)公開編號：TW 201419449 A
(43)公開日： 中華民國 103 (2014) 年 05 月 16 日

(21)申請案號：102131392 (22)申請日： 中華民國 102 (2013) 年 08 月 30 日
(51)Int. Cl.： *H01L21/8239(2006.01)* *H01L27/105 (2006.01)*
H01L23/52 (2006.01)
(30)優先權：2012/08/31 美國 13/600,699
(71)申請人：美光科技公司 (美國) MICRON TECHNOLOGY, INC. (US)
美國
(72)發明人：皮歐 弗得瑞 PIO, FEDERICO (IT)
(74)代理人：陳長文
申請實體審查：有 申請專利範圍項數：30 項 圖式數：9 共 55 頁

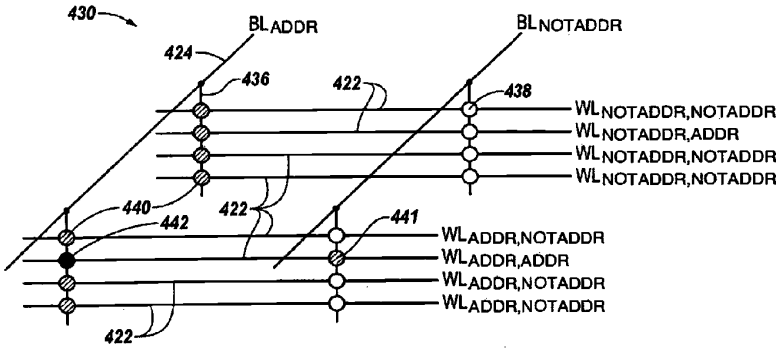
(54)名稱

三維記憶體陣列架構

THREE DIMENSIONAL MEMORY ARRAY ARCHITECTURE

(57)摘要

本發明提供三維記憶體陣列及其形成方法。一例示性三維記憶體陣列可包含：一堆疊，其包括藉由至少一絕緣材料而彼此分離之複數個第一導電線；及至少一導電延伸部，其經配置以實質上垂直於該複數個第一導電線延伸，使得該至少一導電延伸部與該複數個第一導電線之至少一者之一部分相交。圍繞該至少一導電延伸部形成儲存元件材料。圍繞該至少一導電部延伸形成單元選擇材料。



422：字線
424：位元線
430：記憶體陣列
436：導電延伸部
438：記憶體單元
440：記憶體單元
441：記憶體單元
442：記憶體單元

圖4

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發明專利說明書

（本說明書格式、順序，請勿任意更動）

【發明名稱】

三維記憶體陣列架構

THREE DIMENSIONAL MEMORY ARRAY ARCHITECTURE

相關申請案

本發明係關於特此申請之標題爲「THREE DIMENSIONAL MEMORY ARRAY ARCHITECTURE」之具有代理人檔案號碼1001.0690001之美國專利申請案13/600,777，且該案之全文以引用的方式併入本文中。

【技術領域】

本發明大體上係關於半導體裝置，且更特定言之係關於三維記憶體陣列架構及其形成方法。

【先前技術】

通常將記憶體裝置提供爲電腦或其他電子裝置中之內部半導體積體電路。存在許多不同類型之記憶體，包含隨機存取記憶體(RAM)、唯讀記憶體(ROM)、動態隨機存取記憶體(DRAM)、同步動態隨機存取記憶體(SDRAM)、電阻可變記憶體及快閃記憶體等。電阻可變記憶體之類型包含相變材料(PCM)記憶體、可程式化導體記憶體及電阻性隨機存取記憶體(RRAM)等。

對於需要高記憶體密度、高可靠性及無電力之資料保留之廣泛範圍之電子應用而言，記憶體裝置係用作爲非揮發性記憶體。非揮發性記憶體可用於(例如)個人電腦、攜帶型記憶棒、固態磁碟(SSD)、數位相機、蜂巢式電話、諸如MP3播放器之攜帶型音樂播放器、電影播放器及其他電子裝置中。

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關於記憶體裝置製造之不斷挑戰係減小一記憶體裝置之大小、增大一記憶體裝置之儲存密度及/或限制記憶體裝置成本。一些記憶體裝置包含配置成二維陣列之記憶體單元，其中記憶體單元皆配置於一相同平面中。相比之下，多種記憶體裝置包含配置成具有多個記憶體單元層級之三維(3D)陣列之記憶體單元。

【圖式簡單說明】

圖1繪示一先前技術二維記憶體陣列。

圖2繪示一先前技術三維記憶體陣列。

圖3繪示根據本發明之若干實施例之三維記憶體陣列。

圖4繪示用於根據本發明之若干實施例之三維記憶體陣列之偏壓之一方法。

圖5繪示根據本發明之若干實施例之定位於複數個導電線內之同心記憶體單元。

圖6A繪示根據本發明之若干實施例之在一導電線柵格內之同心記憶體單元之位置。

圖6B繪示根據本發明之若干實施例之部分處在一導電線柵格內之同心記憶體單元之位置。

圖6C繪示根據本發明之若干實施例之在一導電線柵格內具有同心加熱器材料之同心記憶體單元之位置。

圖6D繪示根據本發明之若干實施例之部分處在一導電線柵格內具有同心加熱器材料之同心記憶體單元之位置。

圖7A至7C繪示用於形成根據本發明之若干實施例之同心記憶體單元之三維記憶體陣列之一簡化程序流程。

圖8A至8C繪示用於形成根據本發明之若干實施例之同心記憶體單元之三維記憶體陣列之一簡化程序流程。

圖9A至9D繪示用於形成根據本發明之若干實施例之具有加熱器

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材料之同心記憶體單元之三維記憶體陣列之一簡化程序流程。

【實施方式】

本發明提供三維(3D)記憶體陣列及其形成方法。一例示性三維記憶體陣列可包含：一堆疊，其包括藉由至少一絕緣材料而彼此分離之複數個第一導電線；及至少一導電延伸部，其經配置以實質上垂直於該複數個第一導電線延伸，使得該至少一導電延伸部與該複數個第一導電線之至少一者之一部分相交。圍繞該至少一導電延伸部形成儲存元件材料。圍繞該至少一導電延伸部形成單元選擇材料。

本發明之實施例實施相變材料(PCM)記憶體之一垂直整合。所揭示之三維記憶體陣列比習知二維記憶體陣列更密緻。此外，例如藉由減小與形成一3D陣列相關聯之一遮罩計數以製造其中遮罩計數之數量減小之三維記憶體陣列，製造程序可比其他方法更不複雜且更便宜。因此，本發明之製造程序可比先前方法之製造程序便宜。

在本發明之以下詳細描述中，參考形成本發明之一部分且其中藉由圖解展示如何可實踐本發明之一或多項實施例之隨附圖式。足夠詳細地描述此等實施例以使一般技術者能夠實踐本發明之實施例且應瞭解，可利用其他實施例且可在不脫離本發明之範疇之情況下作出程序、電及/或結構改變。

本文中之圖遵循一編號慣例，其中第一數字或(若干)第一數字對應於圖式編號且剩餘數字識別圖式中之一元件或組件。可藉由使用類似數字識別不同圖之間之類似元件或組件。舉例而言，102可參考圖1中之元件「02」，且一類似元件可在圖2中表示爲202。再者，如本文中所使用，「若干」特定元件及/或特徵部可指代一或多個此等元件及/或特徵部。

如本文中所使用，術語「實質上」意指經修改特性未必係絕對的，但足夠接近以達成特性之優勢。舉例而言，「實質上平行」不限

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於絕對平行性，且可包含至少比一垂直定向更接近於一平行定向之定向。類似地，「實質上正交」不限於絕對正交，且可包含至少比一平行定向更接近於一垂直定向之定向。

圖1繪示一先前技術二維記憶體陣列100。多種記憶體裝置可包含一記憶體陣列100。記憶體陣列100可包含複數個字線102及若干位元線104。字線102實質上彼此平行配置在一層級處，且位元線104實質上彼此平行配置在一不同層級處。字線102及位元線104進一步配置成實質上彼此垂直(例如正交)。針對各字線102及位元線104展示之索引指示在一特定層級內各自線之排序。

在此等架構中，記憶體單元106可配置於列及行之一矩陣中。記憶體單元106可定位於字線102與位元線104之交叉處。即，記憶體單元106配置成一交叉點架構。記憶體單元106位於字線102與位元線104在彼此附近通過(例如交叉、重疊等)處。字線102與位元線104彼此不相交，此係因爲字線102及位元線104形成在不同層級處。

圖2繪示一先前技術三維記憶體陣列208。記憶體陣列208可包含複數個字線210、212及若干位元線214。字線210實質上彼此平行配置在一層級處，且字線212實質上彼此平行配置在一不同層級處。如圖2中所示，位元線214實質上彼此平行配置在不同於字線210及212所在之層級之任一者之一層級處(例如在字線210與字線212所在之層級之間)。位元線214進一步配置成實質上垂直(例如正交)於字線210、212。

在圖2中展示以一交叉點架構配置在字線210、212與位元線214之交叉處之記憶體單元216、218。記憶體單元216配置在字線210與位元線214之間，且記憶體單元218配置在字線212與位元線214之間。因而，記憶體單元配置在多個層級中，且各層級具有組織成一交叉點架構之記憶體單元。該等層級係形成在彼此不同之層級處，藉此經垂直

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堆疊。記憶體單元係形成在形成字線212及位元線214之層級之間之層級處。

在圖2中展示之三維記憶體陣列208包含具有一共同位元線214但個別字線210、212之記憶體單元216、218。即，相較於圖1中展示之記憶體陣列100，在記憶體陣列208中之記憶體單元之額外層級需要添加字線之另一層級(例如，記憶體單元218上方之字線212)。位元線214爲定位成垂直相鄰於位元線214(在位元線214正上方及正下方)之該等記憶體單元216、218所共有。此相鄰將位元線214限制爲爲至多兩個記憶體單元所共有。更一般言之，三維記憶體陣列可具有多於圖2中所展示(例如，如圖2中所展示般組態)之堆疊層級。然而，記憶體單元之更多層級之添加(諸如藉由將複數個記憶體陣列208堆疊在彼此之上)需要界定用於記憶體單元之每一額外層級之額外字線及用於額外記憶體單元之每一新層級(或至多層級對)之額外位元線。

針對各字線210、212展示之索引指示層級及一特定層級內之字線之排序。舉例而言，字線210($WL_{3,0}$)係展示爲定位於層級0內之位置3處，且字線212($WL_{3,1}$)係展示爲定位於層級1內之位置3處。因而，記憶體單元216在圖2中係展示爲定位於位元線214(即，BL_0)與位元線214下方之字線(即，$WL_{2,0}$)之間且記憶體單元218在圖2中係展示爲定位於位元線214(即，BL_0)與位元線214上方之字線(即，$WL_{2,1}$)之間。

圖3繪示根據本發明之若干實施例之三維記憶體陣列320。在若干實施例中，存取線(其等可稱作字線(WL))安置在複數個層級(例如，高地、甲板、平面)上。舉例而言，字線可安置在N個層級上。絕緣材料(例如，介電材料)使字線之層級分離。因而，藉由絕緣材料分離之字線之層級形成WL/絕緣材料之一堆疊。資料線(其等可稱作位元線(BL))係配置成實質上垂直於字線且定位於字線之N個層級上方之一層級處(例如在N+1層級處)。各位元線可具有靠近字線之若干導電

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延伸部(例如，垂直延伸部)，其中一記憶體單元形成在垂直延伸部與字線之間。

記憶體陣列320可包含在本文中可稱作字線之複數個導電線322(例如，存取線)及在本文中可稱作位元線之導電線324(例如，資料線)。字線322可配置成若干層級。字線322在圖3中係展示爲配置成四個層級。然而，字線322可配置成之層級之數量不限於此數量，且字線322可配置成更多或更少層級。字線322實質上彼此平行配置在一特定層級內。字線322可在一堆疊中垂直對準。即，在多個層級之各者中之字線322可定位於每一層級內之一相同相對位置處，以便與正上方及/或正下方之字線322對準。絕緣材料(圖3中未展示)可定位於形成字線322之層級之間及一特定層級處之字線322之間。

如圖3中所示，位元線324可實質上彼此平行配置在不同於字線322所在之層級(例如，在字線322所在之層級上方)之一層級處。即，位元線可定位於記憶體陣列320之頂部處。位元線324可進一步配置成實質上垂直(例如，正交)於字線322，以便具有位元線324與字線322之間之重疊(例如，在不同層級處之交叉)。然而，實施例不限於一嚴格平行/正交組態。

在圖3中針對各字線322展示之索引指示一特定層級內之字線之位置(例如排序)及層級。舉例而言，字線$WL_{2,0}$係展示爲定位於層級0內之位置2處(在定位於位置2處之字線之一堆疊之底部之一字線)，且字線$WL_{2,3}$係展示爲定位於層級3內之位置2處(在定位於位置2處之字線之一堆疊之頂部之一字線)。字線322可配置成之層級之數量及在每一層級處之字線322之數量可多於或少於圖3中展示之數量。

在一位元線324與字線322之一堆疊之每一重疊處，位元線324之一導電延伸部326經定向實質上垂直於位元線324及字線322，以便與該字線堆疊中之每一字線322之一部分相交。舉例而言，位元線324之

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導電延伸部326可經配置以自位元線324垂直延伸以與該位元線324下方之各自字線322之一部分相交，如圖3中所示。如所示，導電延伸部326可通過一字線322以便藉由字線322完全包圍。根據若干實施例，導電延伸部326可在字線322附近通過(例如，相鄰於字線322)使得可在導電延伸部326與字線322之間形成一記憶體單元。

記憶體單元328在圖3中係展示爲以一交叉點架構配置在一位元線324之導電延伸部326與字線322在不同層級處彼此靠近之位置附近。在若干實施例中，記憶體單元328係定位於導電延伸部326與字線322之間。舉例而言，在一導電延伸部326通過一字線322之一部分之情況下，一記憶體單元328可定位於導電延伸部326與字線322之間。

因而，記憶體單元328可配置成多個層級，各層級具有組織成一交叉點架構之記憶體單元。記憶體單元328之層級可形成在彼此不同之層級處，藉此經垂直堆疊。圖3中展示之三維記憶體陣列320可包含具有一共同位元線324但個別字線322之記憶體單元328。雖然在圖3中展示字線322之四個層級(及記憶體單元328之四個對應層級)，但本發明之實施例不限於此且可包含字線322之更多或更少層級(及記憶體單元328之對應層級)。記憶體單元可形成在實質上相同於形成字線之層級處。

根據本發明之若干實施例，記憶體單元328可係一電阻可變記憶體單元。舉例而言，記憶體單元328可包含例如硫族化物之一相變材料(PCM)。除其他類型之開關之外，每一記憶體單元328亦可包含例如MOS電晶體、BJT、二極體、雙向臨限值開關(OTS)之一開關。OTS可包含硫族化物材料，諸如不同於用於記憶體元件之硫族化物材料之硫族化物材料。

根據實施例，一記憶體單元328可包含與一各自單元選擇裝置(例如，單元存取裝置)串聯連接之一儲存元件，如下文關於圖5進一步詳

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細解釋，各記憶體單元同心地形成在導電延伸部326周圍。若干實施例包含相變材料(PCM)及開關記憶體單元之三維記憶體陣列，其可稱作一3D PCMS陣列。爲了簡單起見，圖3展示定位於一延伸部326與一字線322之一相交點處之一記憶體單元328。然而，本發明之實施例不限於此且一記憶體單元328可定位於一延伸部326與一字線322之一交叉附近。

圖4繪示用於根據本發明之若干實施例之三維記憶體陣列之偏壓之一方法。圖4展示一記憶體陣列430，其可係關於圖3描述之記憶體陣列320之一部分。記憶體陣列430可包含複數個字線422、經正交定向之位元線424及垂直於字線422及位元線424兩者之導電延伸部436，該等導電延伸部436經耦合且經配置以自位元線424垂直向下延伸。

爲了存取(例如，程式化或讀取)記憶體陣列430，採用一平衡偏壓方案。經定址字線422(即，在經定址層級上之經定址位置處之字線)及經定址位元線經偏壓使得跨其等之電壓差超過各自單元選擇裝置之臨限值電壓。未經定址字線422及未經定址位元線424經偏壓使得跨任何其他對經定址及/或未經定址之字線422及位元線424之電壓差不超過各自單元選擇裝置之臨限值電壓。舉例而言，可以例如一參考電壓(V_{REF})之一中間電壓(諸如經定址位元線與字線電壓之間之一中點電壓)加偏壓於所有其他字線422(包含定位於一相同層級中之不同字線422及定位於不同層級處之字線422)及其他位元線424。

在圖4中將經定址位元線424展示爲BL_{ADDR}且將未經定址位元線424展示爲$BL_{NOTADDR}$。在圖4中針對各字線422展示之索引對應於一特定層級內之字線之位置及該層級。針對一經定址層級或一層級內之位置，使用ADDR標注圖4中展示之字線422且針對一未經定址層級或一層級內之不同字線位置使用NOTADDR標注該等字線422。因此，在圖4中將經定址之字線422展示爲$WL_{ADDR,ADDR}$。在圖4中將未經定址之

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字線422展示爲$WL_{NOTADDR,NOTADDR}$、$WL_{NOTADDR,ADDR}$或$WL_{ADDR,NOTADDR}$之一者以指示未經定址之字線422定位於未經定址之一位置及/或一層級處。

根據若干實施例，未經定址之字線422及未經定址之位元線424可偏壓至一中間電壓以減小相對於經定址之字線422及經定址之位元線424之最大電壓降。舉例而言，中間電壓可經選取以在未經定址之字線422與未經定址之位元線之間之一中點處。然而，中間電壓可經選擇以不同於一中點電壓以最小化對字線422及位元線424之干擾。

圖4展示經定址之字線422與經定址之位元線424之間之記憶體單元442經完全加陰影以指示跨記憶體單元442之電壓差超過相關聯之單元選擇裝置之臨限值電壓V。圖4展示未經定址之字線422與未經定址之位元線424之間之未經干擾記憶體單元438無任何陰影以指示跨記憶體單元438之電壓差係可忽略的，例如空值、零。圖4亦展示未經定址之字線422與經定址之位元線424之間之經干擾記憶體單元440及經定址之字線422與未經定址之位元線424之間之經干擾記憶體單元441經部分加陰影以指示跨記憶體單元441之電壓差小於各自單元選擇裝置之臨限值電壓之某一中間電壓，例如V/2。將未經定址之字線422及未經定址之位元線424偏壓至一相同電壓可係有益的。

記憶體陣列結構與三維垂直通道NAND記憶體具有一些相似性。然而，存取一記憶體單元涉及使電流(其亦在經定址之位元線424及/或經定址之字線422中流動)通過記憶體單元(例如一電阻可變記憶體單元)。本發明之平衡偏壓方案容許僅在一經定址單元上(即，在經定址之字線、層級及位元線上)獲得高於臨限值之一電壓降，而僅干擾沿經定址之字線及位元線分別處在未經定址之位元線及字線之單元，例如至多一最小洩露電流流動通過未經定址之單元。

圖5繪示根據本發明之若干實施例之定位於複數個導電線內之同

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心記憶體單元。在本發明內，「同心」指代實質上彼此包圍之結構，且不限於確切或準確切圓形形狀或佔據面積，例如可形成橢圓形、正方形或矩形同心記憶體單元。圖5展示諸如圖3中繪示之記憶體陣列320之一記憶體陣列之一部分。圖5展示包含在藉由至少一絕緣材料(未展示但定位於導電線522之間548處)彼此分離之若干層級處之複數個導電線522(例如，字線)之一堆疊544。一導電延伸部554經配置以垂直於該複數個導電線522延伸。導電延伸部554在一端通信耦合至一位元線(圖5中未展示)。

圖5展示導電延伸部554通過導電線522之各者使得導電延伸部554之一橫截面完全由一各自導電線522包圍。然而，本發明之實施例不限於此，且導電延伸部554可經配置以便與一各自導電線522之一部分相交使得導電延伸部554不完全由導電線522包圍(關於圖6B對此進行進一步描述)。根據若干實施例，導電延伸部554靠近一各自導電線522通過而非通過該各自導電線522。

圖5進一步展示圍繞導電延伸部554同心配置之儲存元件材料552(例如相變材料(PCM))及單元選擇裝置材料550(雙向臨限值開關(OTS))。雖然圖5展示PCM 552經配置與導電延伸部554相鄰且OTS材料550經配置與PCM 552同心，但本發明之實施例不限於此。根據若干實施例，OTS材料550係配置成與導電延伸部554相鄰且PCM 552係配置成與OTS材料550同心。

雖然爲清楚起見在圖5中未展示，但可在導電延伸部554與一各自導電線522之間同心地形成額外材料，諸如關於圖6C進一步論述之一加熱器材料。另一實例係形成在儲存元件材料552與單元選擇裝置材料550之間以分離儲存元件材料552與單元選擇裝置550及/或提供儲存元件材料552與單元選擇裝置550之間之保護以(例如)減輕成分混合之一材料。

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在導電延伸部554、同心PCM 552及同心OTS材料550靠近一各自導電線522通過之情況下，包含與一各自單元選擇裝置串聯連接之一儲存元件之一同心記憶體單元形成在導電延伸部554與導電線522之間。同心記憶體單元可實質上形成在相同於形成字線之層級處，使得一同心記憶體單元與一導電線522實質上共面。

儲存元件可係一電阻可變儲存元件。例如，電阻可變儲存元件除了包含其他電阻可變儲存元件材料之外亦可包含PCM。在其中電阻可變儲存元件包括PCM之實施例中，除其他相變材料之外，相變材料亦可係硫族化物合金，諸如銦(In)-銻(Sb)-碲(Te)(IST)材料(例如$In_2Sb_2Te_5$、$In_1Sb_2Te_4$、$In_1Sb_4Te_7$等)或鍺(Ge)-銻(Sb)-碲(Te)(GST)材料(例如$Ge_8Sb_5Te_8$、$Ge_2Sb_2Te_5$、$Ge_1Sb_2Te_4$、$Ge_1Sb_4Te_7$、$Ge_4Sb_4Te_7$等)。如本文中使用之用連字符連接之化學組合物標記法指示包含於一特定混合物或化合物中之元素，且旨在表示涉及經指定元素之所有理想配比。例如，其他相變材料可包含Ge-Te、In-Se、Sb-Te、Ga-Sb、In-Sb、As-Te、Al-Te、Ge-Sb-Te、Te-Ge-As、In-Sb-Te、Te-Sn-Se、Ge-Se-Ga、Bi-Se-Sb、Ga-Se-Te、Sn-Sb-Te、In-Sb-Ge、Te-Ge-Sb-S、Te-Ge-Sn-O、Te-Ge-Sn-Au、Pd-Te-Ge-Sn、In-Se-Ti-Co、Ge-Sb-Te-Pd、Ge-Sb-Te-Co、Sb-Te-Bi-Se、Ag-In-Sb-Te、Ge-Sb-Se-Te、Ge-Sn-Sb-Te、Ge-Te-Sn-Ni、Ge-Te-Sn-Pd及Ge-Te-Sn-Pt。相變材料之其他實例包含過渡金屬氧化物材料或包含兩個或兩個以上金屬(例如過渡金屬、鹼土金屬及/或稀土金屬)之合金。實施例不限於一特定電阻可變材料或與記憶體單元之儲存元件相關聯之材料。舉例而言，可用於形成儲存元件之電阻可變材料之其他實例包含二元金屬氧化物材料、龐磁阻材料及/或多種以聚合物爲主之電阻可變材料等。

包括與一相變材料串聯之一單元選擇裝置之記憶體單元可稱作相變材料及開關(PCMS)記憶體單元。在若干實施例中，經同心配置

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之單元選擇裝置用作爲(例如)二端OTS。OTS材料可包含(例如)回應於跨OTS之一施加電壓之硫族化物材料。對於小於一臨限值電壓之一施加電壓，OTS保持在一「關斷」狀態(例如一不導電狀態)中。或者，回應於大於臨限值電壓之跨OTS之一施加電壓，OTS進入一「接通」狀態(例如一導電狀態)。回應於接近一臨限值電壓之一施加電壓，跨OTS之電壓可「折回」至一保持電壓。

在若干實施例中，經同心形成之儲存元件可用作爲二端相變儲存元件。然而，本發明之實施例不限於PCMS交叉點陣列或一特定單元選擇開關。舉例而言，本發明之方法及設備可應用於其他交叉點陣列，諸如除利用(例如)其他類型之記憶體單元之外亦利用電阻隨機存取記憶體(RRAM)單元、導電橋接隨機存取記憶體(CBRAM)單元及/或自旋轉移力矩隨機存取記憶體(STT-RAM)單元之陣列。

在若干實施例中，電阻可變儲存元件材料可包括與單元選擇裝置材料相同之(若干)材料之一或多者。然而，實施例不限於此。舉例而言，電阻可變儲存元件材料及單元選擇裝置材料可包括不同材料。

可藉由包含(但不限於)以下各者之多種薄膜技術形成本文中描述之材料：旋塗、毯覆式塗佈、化學氣相沉積(CVD)(諸如低壓CVD、電漿增強型化學氣相沈積(PECVD))、原子層沈積(ALD)、電漿增強型ALD、物理氣相沈積(PVD)、熱分解及/或熱生長等。或者，可就地生長材料。雖然本文中描述及繪示之材料可形成爲層，但是材料不限於此且可形成於其他三維組態中。關於圖7A至圖9C進一步論述製造技術。

圖6A繪示根據本發明之若干實施例之在一導電線柵格內之同心記憶體單元之位置。圖6A展示一記憶體陣列656之一部分之一俯視圖。記憶體陣列656包含複數個第一導電線622(例如，字線)及配置成垂直於第一導電線622之複數個第二導電線624(例如，位元線)。

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舉例而言，第一導電線622及第二導電線624可由一金屬材料、一多晶矽材料(例如經摻雜之多晶矽材料)等形成。其他層級之第一導電線622(例如其他層級之字線)可存在於圖6A中展示之層級j中之字線下方。第一導電線622與第二導電線624重疊且藉此形成一導電線柵格。

可藉由(例如)將交替導電材料及絕緣材料之一第一堆疊圖案化成若干離散堆疊而形成若干高地處之第一導電線622。即，可蝕刻交替導電材料及絕緣材料以在界定第一導電線之一佔據面積之導電/絕緣材料之若干堆疊之間(橫向)形成溝渠。可使用絕緣材料(例如介電質)填充因此形成之若干堆疊之間之溝渠，以使一特定高地處之第一導電線彼此分離。

每一堆疊可包括複數個第一導電線622，該等第一導電線622藉由絕緣材料彼此(垂直)分離且藉由用於填充溝渠之絕緣材料與(例如)其他堆疊中之其他第一導電線622(橫向)分離。例如，尤其關於圖7A展示一此堆疊之一輪廓視圖。

可藉由圖案化、蝕刻及在各自第二導電線之間形成絕緣材料而類似地形成第二導電線624。然而，由於(一次)可僅在一高地處形成第二導電線，使得此形成可不涉及交替導電及絕緣材料之一堆疊。如本文中所使用，一導電線之一「佔據面積」指代在經形成時一特定導電線之輪廓，例如包括第一導電線之一堆疊之輪廓。可在後續處理中形成通過第一導電線及第二導電線之部分之通孔，此可改變一導電線之所得邊界；然而，在本文中使用術語「佔據面積」以指代(例如)緊接在形成通過第一導電線之一通孔之前第一導電線之原始邊界。

如圖6A中所示，同心記憶體單元649(諸如關於圖5描述之同心記憶體單元)可形成在第一導電線622與第二導電線624重疊之位置處。即，同心記憶體單元649可形成於第一導電線622與第二導電線624看

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似相交處。因爲第一導電線622及第二導電線624形成在不同層級處，所以其等實際上彼此不相交。一記憶體單元649形成在每一字線-位元線重疊處，例如形成在複數個導電線層級之每一層級處(在圖6A中藉由j指示)。

導電延伸部654實質上正交於第一導電線622及第二導電線624，例如在圖6A中導電延伸部654延伸通過頁面。圖6A以橫截面(以平行於導電線622之一平面)展示通過各第一導電線622(例如通過一各自第一導電線622之一中心線)之一導電延伸部654。可圍繞導電延伸部654同心地配置一儲存元件材料652(例如，相變材料(PCM))及單元選擇裝置材料650(例如，雙向臨限值開關(OTS)材料)。雖然圖6A展示儲存元件材料652配置成與導電延伸部654相鄰且單元選擇裝置材料650配置成與儲存元件材料652同心，但本發明之實施例不限於此，且單元選擇裝置材料650可配置成與導電延伸部654相鄰，其中儲存元件材料652配置成與單元選擇裝置材料650同心。

如圖6A中所示，導電延伸部654亦可經配置以自第二導電線624之中心線上之一位置延伸。然而，實施例不限於此，且導電延伸部654可耦合至一各自第二導電線624以(例如)藉由自圖6A中展示之定位稍微改變水平定位而自一中心線位置偏移但仍通過第一導電線之一中心線。

圖6A展示同心記憶體單元649定位於每一層級處之第一導電線622之一佔據面積內(例如，結構之輪廓內)，其中第一導電線622形成於材料之堆疊中。即，導電延伸部654、儲存元件材料652及單元選擇裝置材料650之一橫截面全部定位於第一導電線622之一佔據面積內，因爲此等經同心配置之材料通過形成在複數個層級之各者處之一第一導電線622。在圖6A中展示之切割線A-A提供對圖7A至圖7C中展示之視圖之一參考。

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圖6B繪示根據本發明之若干實施例之部分處在一導電線柵格內之同心記憶體單元之位置。圖6B展示一記憶體陣列670之一部分之一俯視圖。記憶體陣列670包含複數個第一導電線622(例如，字線)及配置成垂直於第一導電線622之複數個第二導電線624(例如，位元線)。其他層級之第一導電線622(例如，其他層級之字線)可存在於圖6B中所展示之層級j中之字線下方。第一導電線622與第二導電線624重疊且藉此形成一導電線柵格。

如圖6B中所示，同心記憶體單元672(與關於圖5所描述之同心記憶體單元在結構上類似但在相對於第一導電線622之位置上不同)可形成在靠近第一導電線622與第二導電線624重疊之位置處。即，同心記憶體單元672可形成在第一導電線622與第二導電線624看似相交處附近(第一導電線622及第二導電線624形成在不同層級處，使得其等實際上彼此不相交)。一記憶體單元672可經形成靠近每一字線-位元線重疊處(例如，複數個導電線層級之每一層級處(在圖6B中藉由j指示)。

可圍繞導電延伸部654同心配置一儲存元件材料652及單元選擇裝置材料650。雖然圖6B展示儲存元件材料652配置成與導電延伸部654相鄰且單元選擇裝置材料650配置成與儲存元件材料652同心，但本發明之實施例不限於此，且單元選擇裝置材料650可配置成與導電延伸部654相鄰，其中儲存元件材料652配置成與單元選擇裝置材料650同心。

導電延伸部654實質上正交於第一導電線622及第二導電線624，例如在圖6B中導電延伸部654延伸通過頁面。圖6B以橫截面(以平行於導電線622之一平面)展示通過各第一導電線622之一部分之一導電延伸部654、儲存元件材料652及單元選擇裝置材料650，使得此等經同心配置之材料未藉由第一導電線622完全包圍(例如在各第一導電線

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622之層級處圍封)。因而，僅儲存元件材料652及/或單元選擇裝置材料650之圓周之一部分與第一導電線622接觸(在第一導電線622之層級處)。以此方式，在一相變中涉及之儲存元件材料652之體積小於儲存元件材料652及/或單元選擇裝置材料650全部通過第一導電線622時之體積。

例如如圖6B中所示，構成同心記憶體單元672之材料可經配置使得同心記憶體單元672之一中心線與一各自第一導電線622(例如沿著一最長尺寸)之一邊緣對準。即，構成同心記憶體單元672之材料可一半定位於一各自第一導電線622之一佔據面積內且一半定位於該佔據面積外部。然而，本發明之實施例不限於此，且構成同心記憶體單元672之材料可經定位以使一部分定位於一各自第一導電線622之一佔據面積內且使一剩餘部分定位於該佔據面積外部。

藉由此配置，僅構成同心記憶體單元672之材料之一部分定位於導電延伸部654與第一導電線622之間。因而，減小體積之儲存元件材料652有效地用於儲存資訊。因此，諸如在PCM中形成一非晶區域時，程式化及/或擦除減小體積之儲存元件材料652可需要更少能量。再者，相對於在導電延伸部654通過(例如)第一導電線622之一中心且由第一導電線622完全包圍(諸如圖6A中所示)之情況中相同寬度之第一導電線622，增大用於第一導電線622汲取電流之有用區段。或者，藉由針對每單位長度一給定電阻率使用一更小第一導電線622寬度而獲得一經減小之有效記憶體單元大小；然而，此一方法對同心記憶體單元672與第一導電線622之間之未對準更敏感。

圖6C繪示根據本發明之若干實施例在一導電線柵格內具有同心加熱器材料之同心記憶體單元647之位置。圖6C展示一記憶體陣列657之一部分之一俯視圖。記憶體陣列657包含複數個第一導電線622(例如，字線)及配置成垂直於第一導電線622之複數個第二導電線

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624(例如，位元線)。其他層級之第一導電線622(例如，其他層級之字線)可存在於圖6C中展示之層級j中之字線下方。第一導電線622與第二導電線624重疊且藉此形成一導電線柵格。

如圖6C中所示，同心記憶體單元647(其具有與關於圖5所描述之同心記憶體單元類似之結構但具有一額外同心材料)可形成在第一導電線622與第二導電線624重疊之位置處。即，同心記憶體單元647可形成在第一導電線622與第二導電線624看似相交處。然而，第一導電線622及第二導電線624係形成在不同層級處，所以其等實際上彼此不相交。一同心記憶體單元647可經形成靠近每一字線-位元線重疊處，例如複數個導電線層級之每一層級處(在圖6C中藉由j指示)。

圖6C以橫截面展示通過各第一導電線622(例如，通過一各自第一導電線622之一中心線)之一導電延伸部654。可圍繞導電延伸部654同心配置一儲存元件材料652(例如，相變材料(PCM))及/或單元選擇裝置材料650(例如，雙向臨限值開關(OTS)材料)。可圍繞導電延伸部654、儲存元件材料652及/或單元選擇裝置材料650同心地配置一加熱器材料645使得該加熱器材料645與儲存元件材料652相鄰，如圖6C中之一組態所展示。應注意，在圖6C中儲存元件材料652及單元選擇裝置材料650之相對定位與圖6A中展示之相對定位(例如，如關於圖6A所論述之一替代組態)反向(使得儲存元件材料652經定位與加熱器材料645相鄰)。

僅包含一PCM記憶體元件及一OTS之一同心記憶體單元(例如，圖6A中展示之同心記憶體單元649)之結構可需要相對較高電流量以在OTS與PCM之間之整個界面處完全形成一非晶區域。對於同心記憶體單元649之一圓形佔據面積，有效體積係大約2π r*tGST*tWL，其中2π r係垂直導電延伸部654之圓周，tGST係PCM材料652之厚度且tWL係第一導電線622之厚度。可以第一導電線622之增加電阻爲代價藉由s

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將第一導電線622製成更薄而減小有效體積。

根據本發明之若干實施例，可減小第一導電線622之有效厚度同時藉由形成(例如，沈積)與一厚第一導電線622材料(相對於加熱器材料645之厚度係厚)相鄰之一薄加熱器材料645(相對於第一導電線622材料之厚度係薄)而將大部分第一導電線622之總電阻實質上維持於可接受量值。

同心記憶體單元647可經組態使得僅該薄加熱器材料645與儲存元件材料652及/或單元選擇裝置材料650接觸，其用作使通過第一導電線622之電流集中(funnel)至一較小橫截面中，藉此增大儲存元件材料652中之局部化電流。第一導電線622之相對較厚輪廓提供第一導電線622之一較低電阻，且在儲存元件材料652附近之相對較薄加熱器材料645減小第一導電線622在同心記憶體單元647處之有效橫截面積以集中電流。因而，薄加熱器材料645有效減小正經受相變之有效體積(因爲相對較薄加熱器材料645之厚度)且可充當可藉由焦耳效應加熱之一加熱器，因此將更集中之能量及增大之溫度提供至相鄰儲存元件材料652。雖然在本發明使用術語「加熱器材料」以區別其他材料及結構，但本發明之實施例不限於自身溫度增大之加熱器材料。即，「加熱器材料」旨在指定可集中電流以限制在一相變中所涉及之儲存元件材料652之一體積且此電流集中可增大儲存元件材料652之一特定體積中之局部化溫度之一材料及/或結構。

歸因於儲存元件材料652及/或單元選擇裝置材料650之同軸配置及體積，本發明之一同心記憶體單元(例如，圖6A中展示之649、圖6B中展示之672及圖6C中展示之647)之有效大小相較於其他記憶體單元組態可爲大。因而，一單一同心記憶體單元可能並非一給定技術節點之一最小大小。然而，製造程序容許堆疊若干記憶體單元層級而不成比例增大陣列遮罩計數，此係因爲不必針對每一額外層級界定第一

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導電線622(例如，字線)及第二導電線624(例如，位元線)。

雖然圖6C展示單元選擇裝置材料650配置成與導電延伸部654相鄰且儲存元件材料652配置成與單元選擇裝置材料650同心，但本發明之實施例不限於此，且可(例如)以一反向順序配置單元選擇裝置材料650、儲存元件材料652及加熱器材料645。

如圖6C中所示，導電延伸部654亦可經配置以垂直延伸通過第二導電線624之中心線上之一位置。然而，實施例不限於此，且導電延伸部654可耦合至一各自第二導電線624以(例如)藉由自圖6C中展示之定位稍微改變水平定位而自一中心線位置偏移同時仍通過第一導電線之一中心線。

圖6C展示同心記憶體單元647定位於每一層級處之第一導電線622之一佔據面積內，其中第一導電線622形成於材料之堆疊中。即，導電延伸部654、單元選擇裝置材料650、儲存元件材料652及加熱器材料645之一橫截面全部定位於第一導電線之一佔據面積內，因爲此等經同心配置之材料通過形成在複數個層級之各者處之一第一導電線622。

根據若干實施例，爲了改良第一導電線622之導電性且最小化形成通過第一導電線622以便具有藉由某個層級處之第一導電線622之材料完全包圍之一橫截面之同心記憶體單元647之材料之未對準問題，可形成具有大於一可能最小大小之尺寸之第一導電線622，因爲儲存元件材料652及單元選擇裝置材料650比第一導電線622材料更具電阻性。

圖6C中展示之切割線B-B提供對圖9A至圖9C中展示之視圖之一參考。

圖6D繪示根據本發明之若干實施例部分處在一導電線柵格內具有同心加熱器材料之同心記憶體單元673之位置。圖6D展示一記憶體

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陣列671之一部分之一俯視圖。上文關於圖6C描述具有同心加熱器材料之同心記憶體單元。上文關於圖6B描述同心記憶體單元與第一導電線622及第二導電線624之重疊之未對準，使得同心記憶體單元以少於全部之同心記憶體單元藉由一特定第一導線622包圍之一方式與第一導電線622相交。如關於圖6D中之同心記憶體單元673所繪示，可組合此等特徵。以此方式，可同時獲得導電線622導電性改良及與減小之有效體積相關聯之減小之程式化能量需求。

圖7A至圖7C繪示用於形成根據本發明之若干實施例之同心記憶體單元(例如，圖6A中展示之同心記憶體單元649)之三維記憶體陣列760之一簡化程序流程。圖7A至圖7C中展示之視圖係沿著圖6A中展示之切割線A-A。圖7A展示在一蝕刻停止材料762(例如，基板材料)上方形成(例如，沈積)若干交替絕緣材料748(例如，介電質)及導電材料722(第一導電線由導電材料722形成)。

通孔764(例如，孔)可經形成(例如，蝕刻)通過交替絕緣材料748及導電材料722而(例如)停止在蝕刻停止材料762處。藉由形成通孔，可移除導電材料722之一部分使得第一導電材料722之所得區域可排除在形成通孔時移除之區域。然而，如先前所論述，術語第一導電材料722之「佔據面積」指代恰在形成通過第一導電材料722之一通孔之前第一導電材料722之邊界，例如一通孔可全部或部分通過第一導電線722之佔據面積。

圖7B展示可藉由隨後形成(例如，沈積)一單元選擇裝置材料750(例如，雙向臨限值開關(OTS)材料)、一儲存元件材料752(例如，相變材料(PCM))及一導電延伸部材料754(例如，金屬材料)而填充通孔764，使得結果係單元選擇裝置材料750及儲存元件材料752同心圍繞導電延伸部材料754(例如圖7B中所示)。如上文所述，可在單元選擇裝置材料750、儲存元件材料752及/或導電延伸部材料754之前、之

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後及/或之間形成(例如，沈積)其他材料(例如)以形成抗材料之相互擴散之黏著層或障壁。

圖7C展示可諸如藉由蝕刻及/或化學機械拋光(CMP)在上(例如，最後)絕緣材料748上方移除單元選擇裝置材料750、儲存元件材料752及導電延伸部材料754以使個別同心記憶體單元749彼此隔離。可在經填充之通孔上方形成第二導電線724(例如，位元線)，使得第二導電線724通信地耦合至導電延伸部材料754。

根據若干實施例，可替代地使用一自對準蝕刻(例如)藉由直接圖案化及蝕刻導電延伸部材料754以使單元選擇裝置材料750及儲存元件材料752留在上絕緣材料748上方及第二導電線724下方之適當位置中而形成第二導電線724。根據另一實施例，可使用一鑲嵌程序以形成第二導電線724。

圖8A至圖8C繪示用於形成根據本發明之若干實施例之具有分離開關裝置之同心記憶體單元之三維記憶體陣列866之一簡化程序流程。在圖7C中可見，沈積於同心記憶體單元之最外徑向位置處之單元選擇裝置材料750垂直鄰接於第一導電線722之不同層級之間。圖8A至圖8C中展示之程序流程導致與離散記憶體單元相關聯且沈積於同心記憶體單元之最外徑向位置處之單元選擇裝置材料在不同層級(對應於不同第一導電線)之間分離。

圖8A至圖8C中展示之視圖係沿著圖6A中展示之切割線A-A。雖然在此處關於單元選擇裝置材料描述不同同心記憶體單元之間之分離，但可交換單元選擇裝置材料與儲存元件材料之相對徑向位置使得儲存元件材料定位於同心記憶體單元之最外徑向位置處且儲存元件材料在不同同心記憶體單元之間分離。

圖8A展示在一蝕刻停止材料862上方沈積若干交替絕緣材料848(例如，介電質)及導電材料822。藉由形成通孔，可移除導電材料

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822之一部分使得第一導電材料822之所得區域可排除在形成通孔時移除之區域。然而，如先前所論述，術語第一導電材料822之「佔據面積」指代恰在形成通過第一導電材料822之一通孔之前第一導電材料822之邊界，例如一通孔可全部或部分通過第一導電材料822之佔據面積。通孔(例如，孔)可經蝕刻通過交替絕緣材料848及導電材料822而(例如)停止在蝕刻停止材料862處(類似於圖7A中針對通孔764所展示者)。在通孔形成期間或之後，使導電材料822凹入以導致圖8A中繪示之通孔868之組態。可使用選擇性蝕刻通孔868中之導電材料822之一曝露區域(諸如藉由一非定向蝕刻(例如，濕式蝕刻))而形成導電材料822中之凹槽869。

圖8B展示沈積至通孔868中其側壁上之單元選擇裝置材料855(其填充由構成第一導電線之凹入導電材料822所留下之區域)，如所示。

圖8C展示諸如藉由一定向蝕刻(例如，乾式蝕刻)自頂表面(即，上絕緣材料848上方)及通孔之側壁移除之單元選擇裝置材料855。此使單元選擇裝置材料855僅留在由凹入導電材料822留下之離散區域中。此後，可如所示般在通孔中形成儲存元件材料852(例如，PCM)及導電延伸部854(例如，金屬垂直位元線延伸部)材料。根據關於圖8A至圖8C繪示之程序，單元選擇裝置材料855僅作爲圍繞第二導電線之導電延伸部854及儲存元件材料852之複數個離散環狀結構而形成在第一導電線822之交叉處，藉此減小垂直相鄰同心記憶體單元867之間之電洩漏及干擾。可進一步處理儲存元件材料852及導電延伸部854材料且在其等上方形成第二導電線(例如，位元線)，如關於圖7C所述。

圖9A至圖9C繪示用於形成根據本發明之若干實施例之具有加熱器材料之同心記憶體單元994之三維記憶體陣列980之一簡化程序流程。關於圖9A至圖9C展示及描述之形成程序類似於關於圖8A至圖8C展示及描述之形成程序，惟包含一額外加熱器材料除外。圖9A至圖9C所展示之視圖係沿著圖6C中所展示之切割線B-B。如關於圖9C所論

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述，同心記憶體單元994之組態包含儲存元件材料950及加熱器材料945，其等相鄰以達成與減小之有效體積相關聯之減小之程式化能量需求。

圖9A展示在一蝕刻停止材料982上方沈積若干交替絕緣材料948(例如介電質)、加熱器材料945及導電材料922。藉由形成通孔，可移除導電材料922之一部分使得第一導電材料922之所得區域可排除在形成通孔時移除之區域。然而，如先前所論述，術語第一導電材料922之「佔據面積」指代恰在形成通過第一導電材料922之一通孔之前第一導電材料922之邊界，例如一通孔可全部或部分通過第一導電材料922之佔據面積。通孔990可經蝕刻通過交替絕緣材料948、加熱器材料945及導電材料922而(例如)停止在蝕刻停止材料982處。

在通孔990形成期間或之後(類似於圖8A中針對通孔868所展示者)，可使導電材料922凹入以導致圖9A中繪示之組態。可使用選擇性蝕刻(諸如非定向蝕刻(例如，濕式蝕刻))通孔中之導電材料922之一曝露區域而形成導電材料922中之凹槽969。非定向蝕刻可專用於導電材料922但不(或較少)專用於加熱器材料945(其可係不同於導電材料922之一材料)。

可將絕緣材料992沈積至通孔990中(包含沈積至其側壁上)，從而填充凹槽969，例如由凹入導電材料922(構成第一導電線)留下之區域。注意，此不同於如圖8B中所示般將單元選擇裝置材料855沈積至凹槽869中。可諸如藉由一定向蝕刻(例如，乾式蝕刻)自頂表面(即，上絕緣材料948上方)及通孔990之側壁移除絕緣材料992，此可使絕緣材料992僅留在凹槽969(例如，由凹入導電材料822留下之離散區域)中，同時曝露在通孔990之側壁處之加熱器材料945之一部分，如圖9B中所示。

根據若干替代實施例，可選擇性地氧化(形成或不形成凹槽969)導電材料922以形成絕緣材料992，而非在導電材料922中形成凹槽

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969、沈積絕緣材料992且蝕刻以移除除凹槽969中之絕緣材料992以外之全部絕緣材料992。

圖9C展示可藉由隨後形成(例如，沈積)例如相變材料(PCM)之儲存元件材料950(對應於圖6C中所展示之儲存元件材料652)、例如雙向臨限值開關(OTS)材料之一單元選擇裝置材料952(對應於圖6C中所展示之單元選擇裝置材料650)及例如金屬材料之一導電延伸部材料954(對應於圖6C中所示之導電延伸部654)而填充通孔990使得結果係單元選擇裝置材料952及儲存元件材料950在通孔990內同心圍繞導電延伸部材料954且儲存元件材料950與加熱器材料945相鄰。

因爲使用絕緣材料992填充藉由使第一導電線材料922凹入而留下之區域，所以將流動於第一導電線922中之電流全部投送至同心記憶體單元附近具有一相對較小橫截面積之加熱器材料945，藉此使電流集中朝向相變中涉及之儲存元件材料950之一較小體積，如圖9C中在999處所指示。如上文關於圖6C詳細論述，使用加熱器材料945有效地減小在儲存元件材料950附近之第一導電線922厚度，藉此在相變中涉及一較小有效體積，且亦增大在加熱器材料945(其歸因於焦耳效應加熱且傳送能量(即，升高溫度)至儲存元件材料950)中之電流密度。因而，如此命名加熱器材料945，因爲其可充當一加熱器。

單元選擇裝置材料952、儲存元件材料950及導電延伸部材料954可進一步予以處理，且可在其等上方形成第二導電線(例如，位元線)，如關於圖7C所描述。

圖9D繪示用於形成根據本發明之若干實施例之具有第一導電線(例如，字線)及一調解加熱器材料之同心記憶體單元993之三維記憶體陣列981之一程序流程之結果。在關於用於形成與同心記憶體單元相鄰之加熱器材料之一程序考量圖9A至圖9C之後，藉由相較於圖9C中所示之組態考量圖9D中所示之組態，將瞭解用於形成調解至第一導電線之加熱器材料之一替代程序。

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可藉由在一蝕刻停止材料982上方沈積絕緣材料948(例如，介電質)、導電材料985、加熱器材料945及導電材料985之若干例項而形成圖9D中所示之記憶體陣列981之組態。兩個導電材料985構成第一導電線(例如，字線)，在該等第一導電線之間安置有一加熱器材料945(例如，調解至第一導電線)。

通孔990可經蝕刻通過之絕緣材料948及具有調解加熱器材料之第一導電線(例如，導電材料985、加熱器材料945及導電材料985)之若干例項(類似於圖8A中針對通孔868所展示者)。可使用一非定向蝕刻(例如，濕式蝕刻)使導電材料985之各者凹入，類似於圖9A中所繪示之結果，惟各加熱器材料945可具有在加熱器材料945上方及下方相鄰導電材料985中之一凹槽969除外。非定向蝕刻可專用於導電材料985但不(或較少)專用於加熱器材料945(其可係不同於導電材料985之一材料)。

可將絕緣材料991沈積至通孔中(包含沈積至其側壁上)，從而填充在延伸超過導電材料985之末端之加熱器材料945上方及下方由凹入導電材料985留下之區域。可諸如藉由一定向蝕刻(例如，乾式蝕刻)自頂表面(即，上絕緣材料948上方)及通孔之側壁移除絕緣材料991，此可使絕緣材料991僅留在加熱器材料945正上方及正下方由凹入導電材料985留下之離散區域中。

可藉由隨後形成(例如，沈積)一儲存元件材料950(例如，相變材料(PCM))、一單元選擇裝置材料952(例如，雙向臨限值開關(OTS)材料)及一導電延伸部材料954(例如，金屬材料)而填充所得通孔，使得結果係單元選擇裝置材料952及儲存元件材料950同心圍繞導電延伸部材料954，如圖9D中所示。如上文關於圖6C詳細論述，使用加熱器材料945有效地減小在儲存元件材料950附近之第一導電線922厚度，藉此在相變中涉及一較小有效體積，且亦增大在歸因於焦耳效應加熱且

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傳送能量(即，升高溫度)至儲存元件材料950之加熱器材料945中之電流密度。因而，如此命名加熱器材料945，因爲其可充當一加熱器。

在操作期間，將流動於第一導電線(即，導電材料985)中之電流全部投送至在同心記憶體單元附近具有一相對較小橫截面積之加熱器材料945，藉此使電流集中朝向相變中所涉及之儲存元件材料950之一較小體積，如圖9D中在997處所指示。可進一步處理單元選擇裝置材料952、儲存元件材料950及導電延伸部材料954，且可在其等上方形成第二導電線(例如，位元線)，如關於圖7C所描述。

應注意，如關於圖9A至圖9D所述，使用加熱器材料可應用於在第一導電線及第二導電線之重疊內經形成以與第一導電線相交且藉由該等第一導電線完全包圍(例如，圖6C中所繪示之位置)之通孔，或應用於經形成而僅與第一導電線之一部分相交(且未藉由第一導電線完全包圍)(例如，圖6D中所繪示之位置)之通孔等。

具有一「未對準」垂直導電延伸部(未與一第一導電線相交以便藉由第一導電線完全包圍)之例示性實施例有效地減小有效體積，此係因爲僅通孔之圓周之一部分(例如，半圓周)與一給定第一導電線(例如，字線)相交。具有一「未對準」垂直導電延伸部之實施例亦可減小記憶體單元空間，此係因爲第一導電線寬度可因其寬度之一較小部分受通孔之形成影響而相對更窄。

雖然降低單元選擇裝置材料(例如，OTS)與儲存元件材料(例如，PCM)之間之表面積之量，但可使用此兩個材料之間之一相對較大電流以非晶化儲存元件材料之整個體積。有效體積係大約$2\pi r*tGST*tWL$，其中$2\pi r$係儲存元件材料在與相鄰材料之界面處之圓周之(部分)(其可經調整以用於其中僅圓周之一部分與儲存元件材料相交之組態)，tGST係有效儲存元件材料厚度且tWL係有效第一導電線(例如，字線)厚度。依照關於圖9A至圖9D所繪示之實施例，可使有效

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第一導電線厚度減小至一加熱器材料945之一厚度tH，同時維持可接受之總體第一導電線電阻。

根據一些實施例，對於每一甲板，可平面沈積一儲存元件材料(例如，諸如GST之PCM)薄層以便與第一導電線材料通信地耦合，例如類似於圖9C中所示之加熱器材料組態般與第一導電線材料直接接觸，或類似於圖9D中所示之加熱器材料組態般夾置於兩層第一導電線材料之間。可藉由選擇性蝕刻或氧化透過單元選擇裝置材料而使終止於一通孔之側壁處之第一導電線材料凹入及絕緣(如關於圖9A至圖9D先前所述，但具有延伸至垂直導電延伸部材料(例如圖9D中之954)之儲存元件材料)。爲清楚起見，所得結構類似於在圖9C及圖9D中所表示且在上文描述之結構，但具有以下修改：儲存元件材料將由對應於圖9C及圖9D中之參考數字945之部分表示且對應於參考數字952之部分將不存在。

根據一些實施例，一三維記憶體陣列可包含一堆疊，該堆疊包括在若干層級處藉由至少一絕緣材料而彼此分離之與儲存元件材料相鄰之複數個第一導電線。儲存元件材料諸如在其之一邊緣處形成相對於複數個第一導電線之各者之一突出部。至少一導電延伸部可經配置以實質上垂直於該複數個第一導電線及相鄰儲存元件材料而延伸。可在通孔內該儲存元件材料突出部與該至少一導電延伸部之間形成單元選擇材料。

此實施例可減小總體單元尺寸，因爲僅兩個材料(例如，單元選擇材料及導電延伸部材料)係在垂直BL部分中。此實施例亦將一記憶體單元之有效儲存元件材料體積限制於第一導電線與垂直導電延伸部之間，從而使有效儲存元件材料體積減小至2πr*tGST*EXTWL，其中2πr係儲存元件材料在與相鄰材料之界面處之圓周之(部分)(其可經進一步調整以用於其中僅圓周之一部分與儲存元件材料相交之組態)，

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tGST係有效儲存元件材料厚度且EXTWL係薄儲存元件材料(例如GST)自相對較厚低電阻第一導電線材料之延伸部。

雖然在本文中繪示及描述特定實施例，但一般技術者將瞭解，經計算以達成相同結果之一配置可取代所展示之特定實施例。本發明旨在涵蓋本發明之多種實施例之調適或變動。應瞭解，上述描述係以一闡釋性方式而非一限制性方式作出。熟習此項技術者在審閱上述描述後應明白上述實施例之組合及本文未明確描述之其他實施例。本發明之多種實施例之範疇包含其中使用上文結構及方法之其他應用。應參考隨附申請專利範圍連同此等申請專利範圍所授權之等效物之全範圍而判定本發明之多種實施例之範疇。

在前述實施方式中，爲簡化本發明之目的將一些特徵一起集合於一單項實施例中。本發明之此方法不應被解釋爲反映本發明之所揭示實施例必須使用比明確陳述於每一技術方案中更多之特徵之一意圖。實情係，如下列申請專利範圍反映，本發明標的在於少於一單項所揭示實施例之全部特徵。因此，特此將下列申請專利範圍併入實施方式中，其中每一技術方案獨立地作爲一單獨實施例。

【符號說明】

100	二維記憶體陣列
102	字線
104	位元線
106	記憶體單元
208	三維記憶體陣列
210	字線
212	字線
214	位元線
216	記憶體單元

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218	記憶體單元
320	三維記憶體陣列
322	導電線/字線
324	導電線/位元線
326	導電延伸部
328	記憶體單元
422	字線
424	位元線
430	記憶體陣列
436	導電延伸部
438	記憶體單元
440	記憶體單元
441	記憶體單元
442	記憶體單元
522	導電線
544	堆疊
550	單元選擇裝置材料/雙向臨限值開關(OTS)材料
552	儲存元件材料/相變材料(PCM)
554	導電延伸部
622	第一導電線
624	第二導電線
645	加熱器材料
647	同心記憶體單元
649	同心記憶體單元
650	單元選擇裝置材料
652	儲存元件材料

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654 導電延伸部

656 記憶體陣列

657 記憶體陣列

670 記憶體陣列

671 記憶體陣列

672 同心記憶體單元

673 同心記憶體單元

722 導電線材料/第一導電線

724 第二導電線

748 絕緣材料

749 同心記憶體單元

750 單元選擇裝置材料

752 儲存元件材料

754 導電延伸部材料

760 三維記憶體陣列

762 蝕刻停止材料

764 通孔

822 導電材料

848 絕緣材料

852 儲存元件材料

854 導電延伸部

855 單元選擇裝置材料

862 蝕刻停止材料

866 三維記憶體陣列

867 同心記憶體單元

868 通孔

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869	凹槽
922	導電材料/第一導電線材料
945	加熱器材料
948	絕緣材料
950	單元選擇裝置材料
952	儲存元件材料
954	導電延伸部材料
969	凹槽
980	三維記憶體陣列
981	三維記憶體陣列
982	蝕刻停止材料
985	導電材料
990	通孔
991	絕緣材料
992	絕緣材料
993	同心記憶體單元
994	同心記憶體單元
997	儲存元件材料之較小體積
999	儲存元件材料之較小體積

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發明摘要

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【發明名稱】

三維記憶體陣列架構

THREE DIMENSIONAL MEMORY ARRAY ARCHITECTURE

【中文】

本發明提供三維記憶體陣列及其形成方法。一例示性三維記憶體陣列可包含：一堆疊，其包括藉由至少一絕緣材料而彼此分離之複數個第一導電線；及至少一導電延伸部，其經配置以實質上垂直於該複數個第一導電線延伸，使得該至少一導電延伸部與該複數個第一導電線之至少一者之一部分相交。圍繞該至少一導電延伸部形成儲存元件材料。圍繞該至少一導電部延伸形成單元選擇材料。

【英文】

Three dimension memory arrays and methods of forming the same are provided. An example three dimension memory array can include a stack comprising a plurality of first conductive lines separated from one another by at least an insulation material, and at least one conductive extension arranged to extend substantially perpendicular to the plurality of first conductive lines, such that the at least one conductive extension intersects a portion of at least one of the plurality of first conductive lines. Storage element material is formed around the at least one conductive extension. Cell select material is formed around the at least one conductive extension.

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申請專利範圍

1. 一種三維記憶體陣列，其包括：

一堆疊，其包括在若干層級處藉由至少一絕緣材料而彼此分離之複數個第一導電線；

至少一導電延伸部，其經配置以實質上垂直於該複數個第一導電線延伸，使得該至少一導電延伸部與該複數個第一導電線之至少一者之一部分相交；

儲存元件材料，其圍繞該至少一導電延伸部而形成；及

單元選擇材料，其圍繞該至少一導電延伸部而形成。

2. 如請求項1之記憶體陣列，其中該儲存元件材料圍繞該至少一導電延伸部同心地形成。

3. 如請求項1之記憶體陣列，其中該單元選擇材料圍繞該至少一導電延伸部同心地形成。

4. 如請求項1之記憶體陣列，其中該至少一導電延伸部通過該複數個第一導電線之至少一者。

5. 如請求項1之記憶體陣列，其進一步包括經形成以在不同於該若干層級之一層級處實質上垂直於該複數個第一導電線延伸且經配置以實質上垂直於該至少一導電延伸部延伸之複數個第二導電線，

其中該至少一導電延伸部耦合至該複數個第二導電線之至少一者。

6. 如請求項1之記憶體陣列，其中該複數個第二導電線形成在該複數個第一導電線及該至少一導電延伸部上方。

7. 如請求項1之記憶體陣列，其中該儲存元件材料係相變材料(PCM)，且該單元選擇材料係雙向臨限值開關(OTS)材料。

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8. 如請求項7之記憶體陣列，其中該PCM及該OTS材料至少定位於該至少一導電延伸部與相交於該至少一導電延伸部之該複數個第一導電線之該至少一者之各者之間。

9. 如請求項1至8中任一項之記憶體陣列，其中複數個第二導電線經配置以在該複數個第一導電線上方之一層級處實質上垂直於該複數個第一導電線延伸。

10. 如請求項9之記憶體陣列，其中該至少一導電延伸部經配置以自該複數個第二導電線之一各自者垂直延伸以通過該複數個第一導電線之多者。

11. 如請求項1至8中任一項之記憶體陣列，其包括記憶體單元，其中每一各自記憶體單元包括至少一導電延伸部、該儲存元件材料及該單元選擇材料，且其中該複數個第一導電線之一各自者及該記憶體單元係在該若干層級中與該複數個第一導電線之該各自者相同之層級處。

12. 一種三維記憶體陣列，其包括：

複數個第一導電線，其等經配置以定位於若干層級之各者上之若干位置處，使得複數個第一導電線之多者在該若干位置之各者處堆疊在彼此之上；

複數個第二導電線，其等形成在該複數個第一導電線上方且配置成實質上垂直於該複數個第一導電線，其中該複數個第二導電線之各者耦合至經配置以實質上垂直於該複數個第二導電線及該複數個第一導電線延伸之至少一導電延伸部，使得該等導電延伸部之至少一部分通過在一各自位置處堆疊在彼此之上之該多個第一導電線之某一部分；

儲存元件材料，其圍繞該等導電延伸部之各者而形成；及

單元選擇材料，其圍繞該等導電延伸部之各者而形成，

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其中各導電延伸部僅耦合至該複數個第二導電線之一者。

13. 如請求項12之記憶體陣列，其中該等導電延伸部經定位以便在該複數個第一導電線之一者與該複數個第二導電線之一者之每一重疊處垂直延伸。

14. 如請求項12之記憶體陣列，其中該等導電延伸部之一各自者經定位以便與該複數個第一導電線之至少一者之部分相交，其中該複數個第一導電線之該至少一者與該等第二導電線重疊。

15. 如請求項12之記憶體陣列，其中該複數個第一導電線、該至少一導電延伸部及該複數個第二導電線係由一金屬材料形成。

16. 如請求項12之記憶體陣列，其中該至少一導電延伸部或該複數個第一導電線或該複數個第二導電線之至少一者包括一多晶矽材料。

17. 如請求項12至16中任一項之記憶體陣列，其中該儲存元件材料係配置成與該至少一導電延伸部相鄰，且該單元選擇材料係配置成與該儲存元件材料同心。

18. 如請求項12至16中任一項之記憶體陣列，其中該單元選擇材料係配置成與該至少一導電延伸部相鄰，且該儲存元件材料係配置與該單元選擇材料同心。

19. 如請求項12至16中任一項之記憶體陣列，其中該至少一導電延伸部、該儲存元件材料及該單元選擇材料之一橫截面全部在該複數個第一導電線之一者之一佔據面積內通過。

20. 如請求項12至16中任一項之記憶體陣列，其中該至少一導電延伸部、該儲存元件材料及該單元選擇材料之一橫截面之至少一部分部分定位於該複數個第一導電線之一者之一佔據面積內且部分定位於該佔據面積外部。

21. 如請求項12至16中任一項之記憶體陣列，其進一步包括與該複

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數個第一導電線之各者相鄰且通信地耦合之一加熱器材料，該加熱器材料具有小於該複數個第一導電線之一者之橫截面積之一橫截面積，該加熱器材料串聯配置在該複數個第一導電線之一各自者與該儲存元件材料之間。

22. 如請求項21之記憶體陣列，其中該加熱器材料安置於該複數個第一導電線之各者之一第一部分與一第二部分之間，該加熱器材料具有小於該複數個第一導電線之各者之該等第一及第二部分之橫截面積之一橫截面積，該加熱器材料串聯配置在該複數個第一導電線之一各自者之該等第一及第二部分與該儲存元件材料之間。

23. 一種三維記憶體陣列，其包括：

一堆疊，其包括在若干層級處藉由至少一絕緣材料而彼此分離之與儲存元件材料相鄰之複數個第一導電線，該儲存元件材料在其之一邊緣處自該複數個第一導電線之各者突出；

至少一導電延伸部，其經配置以實質上垂直於該複數個第一導電線及相鄰儲存元件材料而延伸；及

單元選擇材料，其形成在該儲存元件材料突出部與該至少一導電延伸部之間。

24. 一種形成一記憶體陣列之方法，其包括：

形成包括藉由絕緣材料而彼此分離之複數個第一導電線之一堆疊；

形成通過該堆疊之一通孔使得該通孔之至少一部分通過該複數個第一導電線之各者；

在該通孔內形成單元選擇材料；

在該通孔內形成儲存元件材料；

在該通孔內形成一導電延伸部；及

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在該導電延伸部上方形成實質上垂直於該第一導電線及該導電延伸部之第二導電線，

其中該導電延伸部通信地耦合至該等第二導電線以作爲該等第二導電線之一延伸部。

25. 如請求項24之方法，其中：

在該通孔內形成儲存元件材料包含在該通孔中該單元選擇材料上方形成儲存元件材料；及

在該通孔內形成該導電延伸部包含在該通孔內該儲存元件材料上方形成該導電延伸部。

26. 如請求項24之方法，其中：

在該通孔內形成該單元選擇材料包含在該通孔中該儲存元件材料上方形成該單元選擇材料；及

在該通孔內形成該導電延伸部包含在該通孔內該單元選擇材料上方形成該導電延伸部。

27. 一種形成一記憶體陣列之方法，其包括：

形成包括與加熱器材料相鄰之複數個第一導電線之一堆疊，與加熱器材料相鄰之該等第一導電線藉由絕緣材料彼此分離；

形成通過該堆疊之一通孔使得該通孔之至少一部分通過該複數個第一導電線之各者及相鄰加熱器材料；

在該通孔之一壁中該等第一導電線之各者之一曝露區域處形成一凹槽；

在該凹槽內形成一絕緣材料；

在該通孔內該絕緣材料上方形成與該加熱器材料接觸但不與該等第一導電線接觸之儲存元件材料；

在該儲存元件材料上方形成一單元選擇材料；及

在該通孔內單元選擇材料上方形成一導電延伸部。

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28. 如請求項27之方法，其中形成通過該堆疊之該通孔包括：形成與該複數個第一導電線之各者及相鄰加熱器材料之一最長尺寸切向相交之一通孔。

29. 如請求項27之方法，其中形成通過該堆疊之該通孔包括：形成未藉由一第一導電線及該複數個第一導電線之相鄰加熱器材料及相鄰加熱器材料完全包圍之一通孔。

30. 如請求項27至29中任一項之方法，其中形成包括與加熱器材料相鄰之該複數個第一導電線之該堆疊包括：形成與該等第一導電線調解之該加熱器材料。

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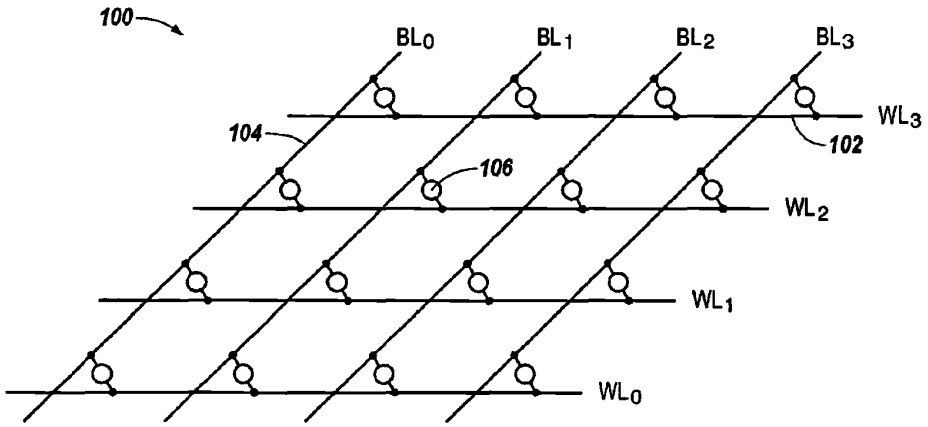
圖式



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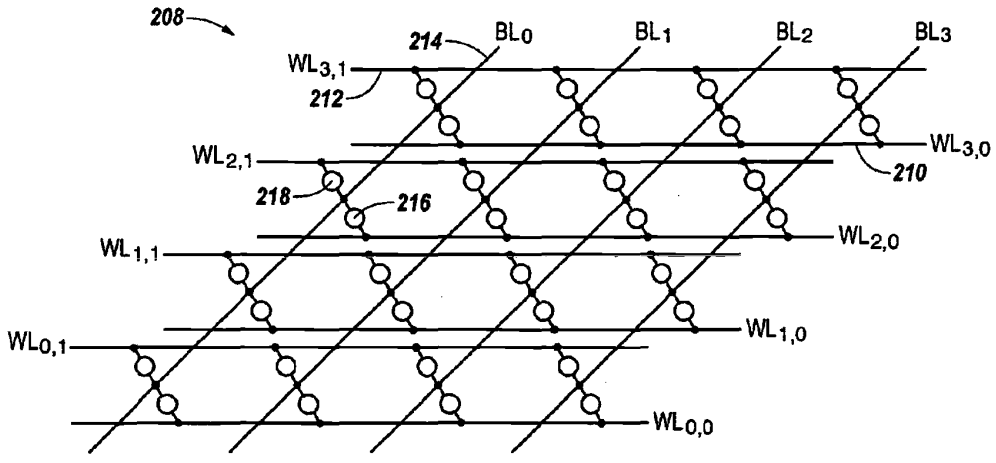

圖2

5

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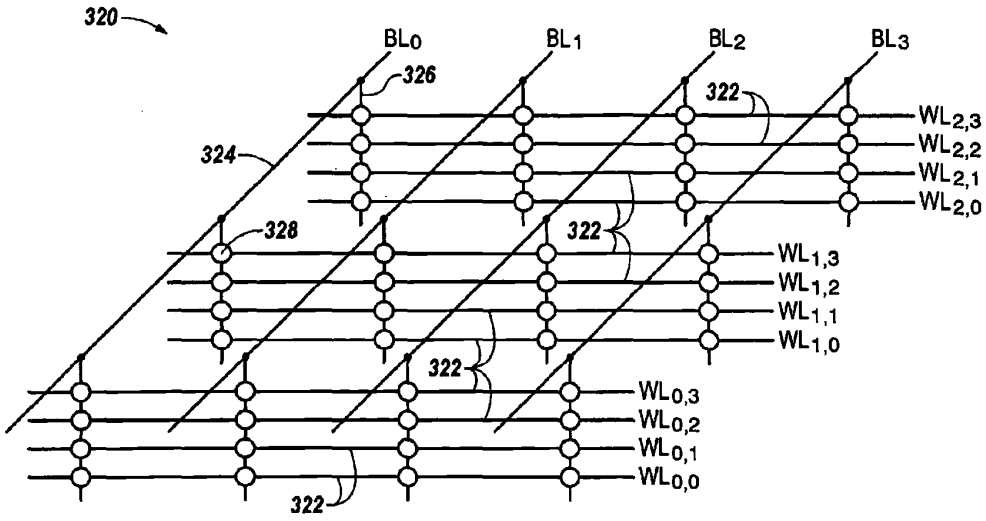

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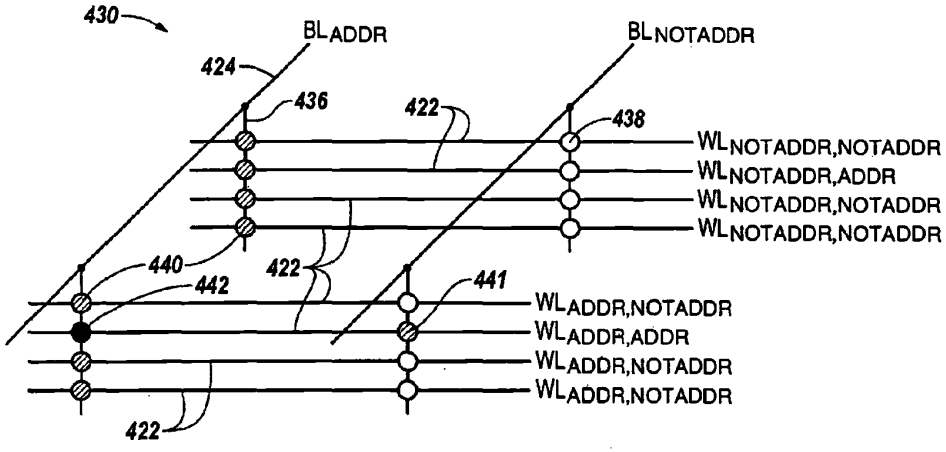

圖4

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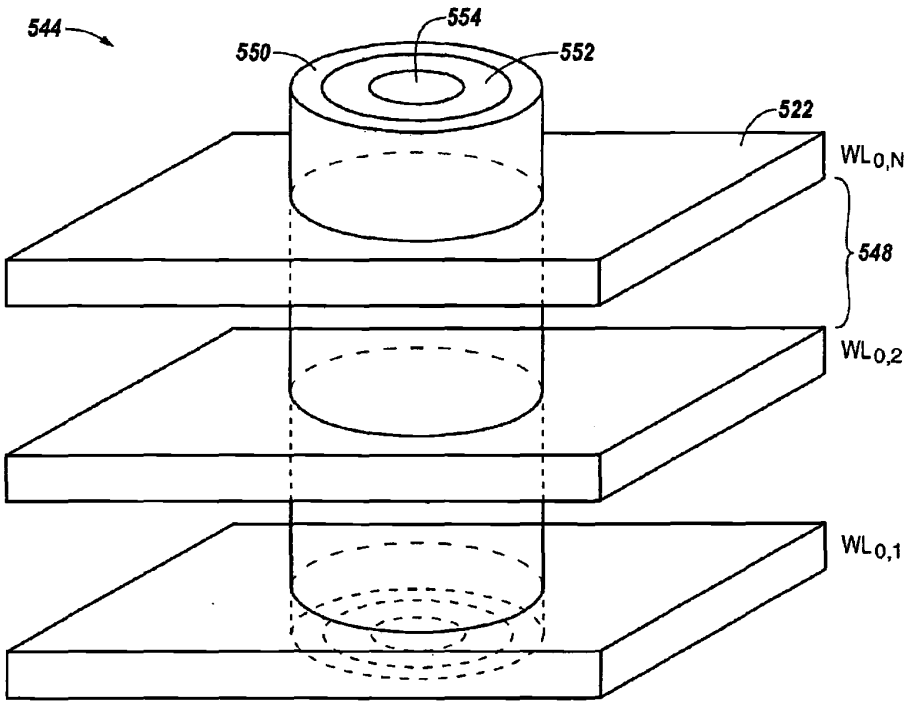

圖5

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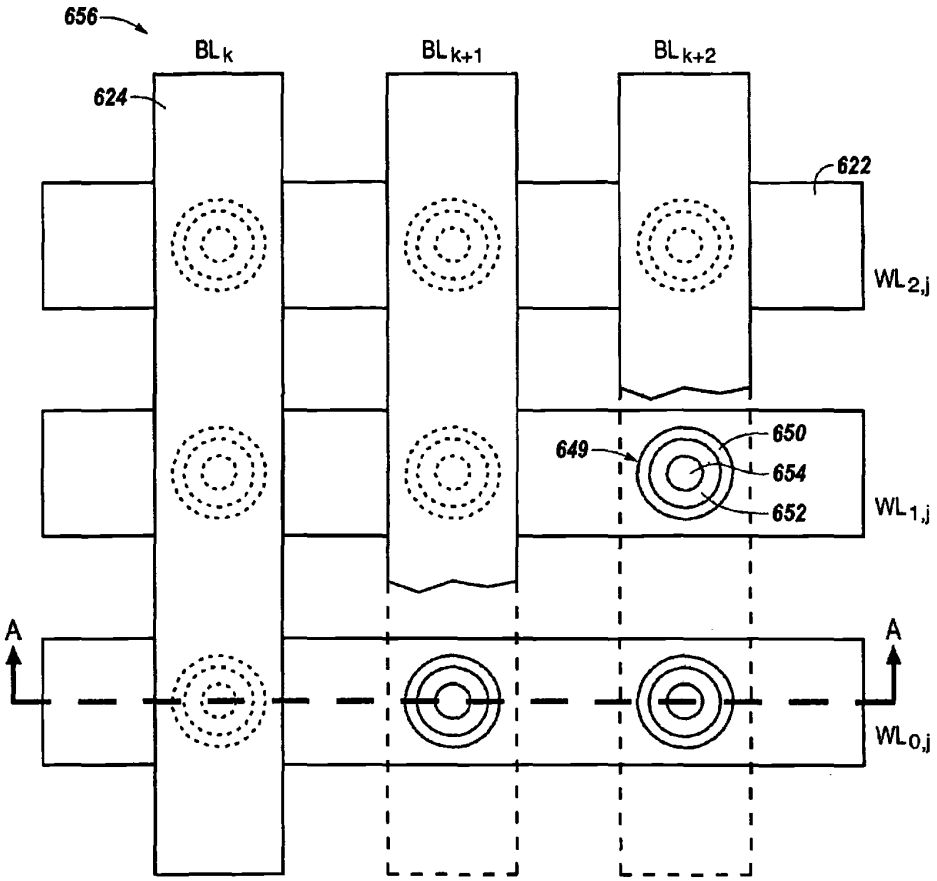

圖6A

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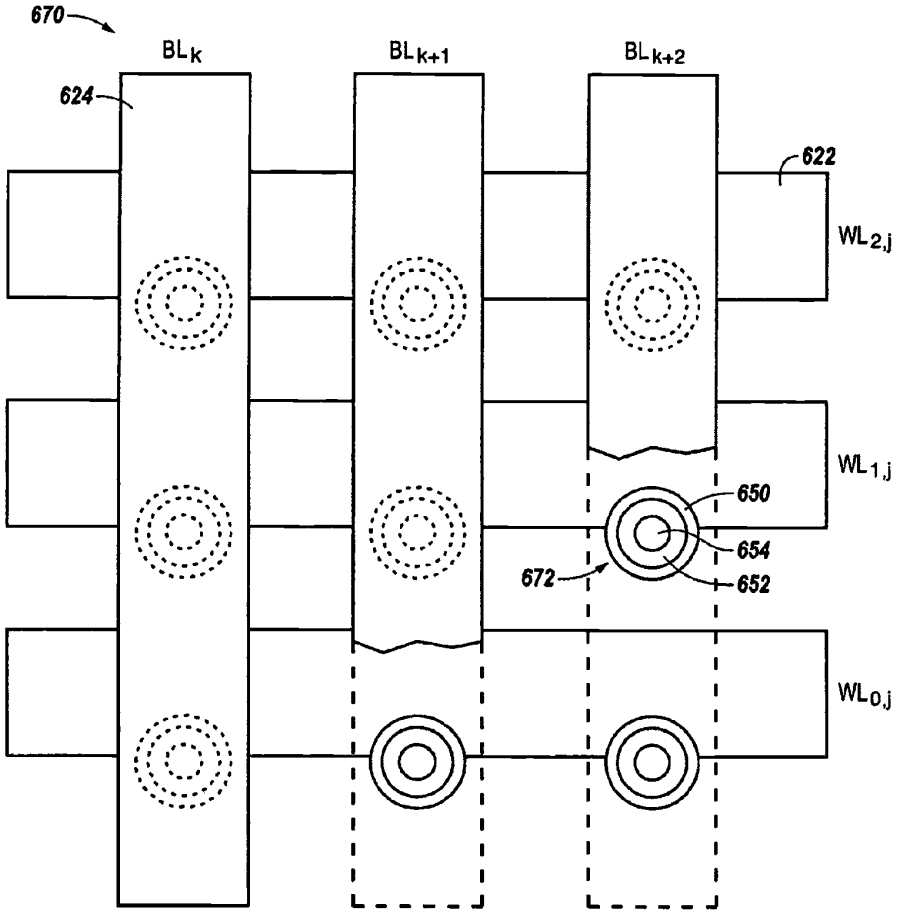

圖6B

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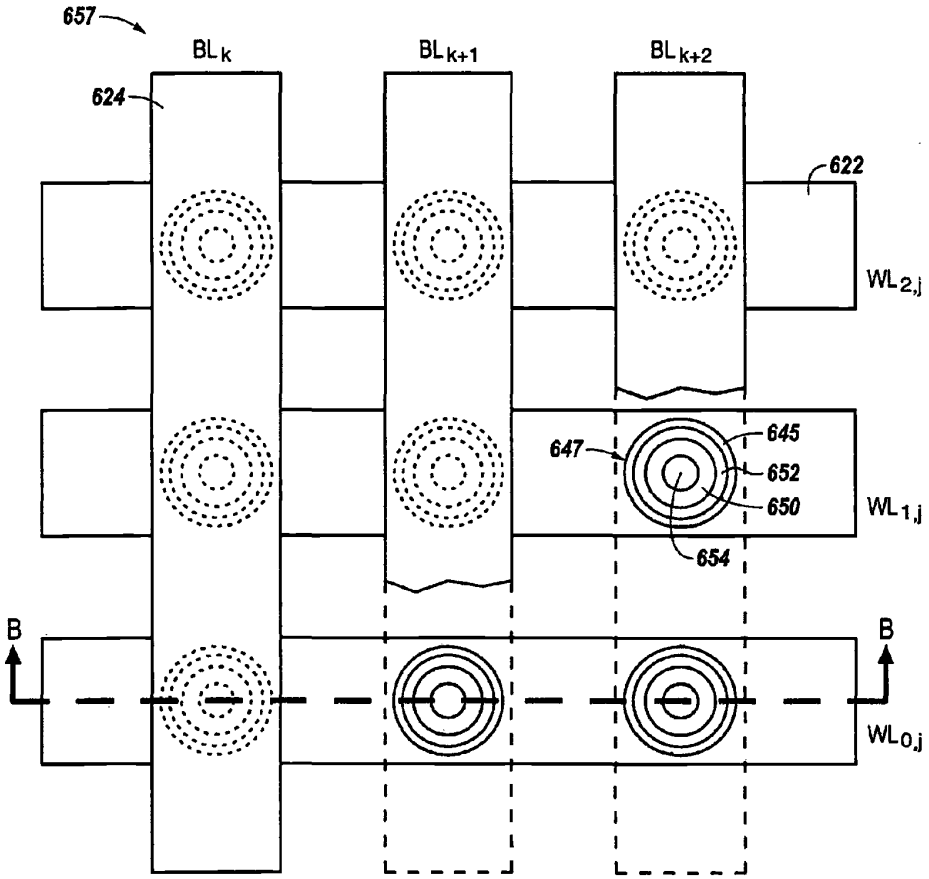

圖6C

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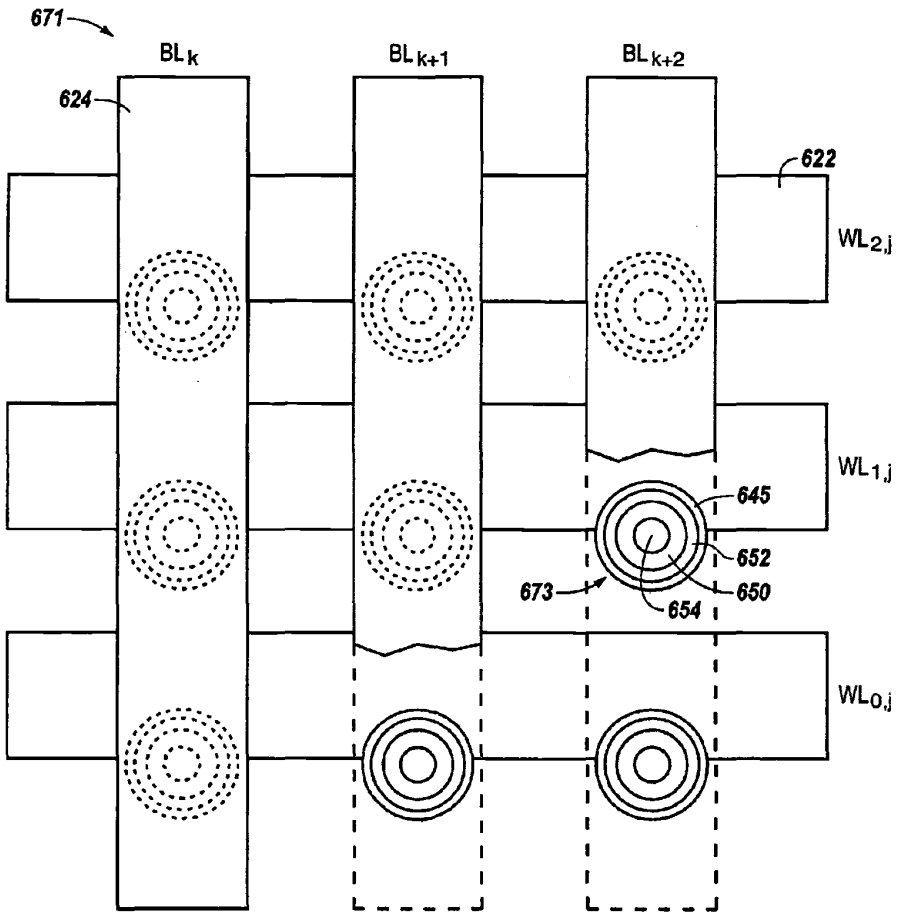

圖6D

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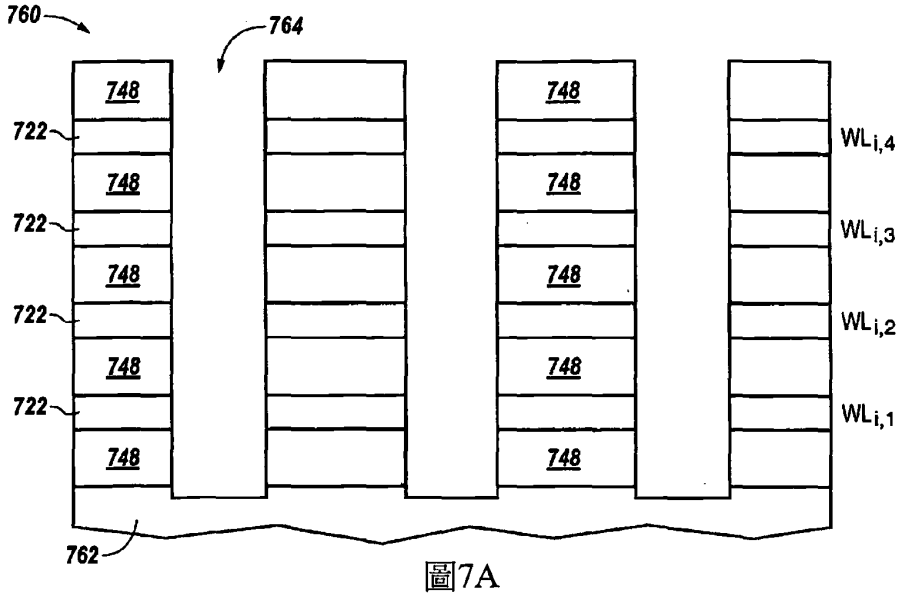

圖7A

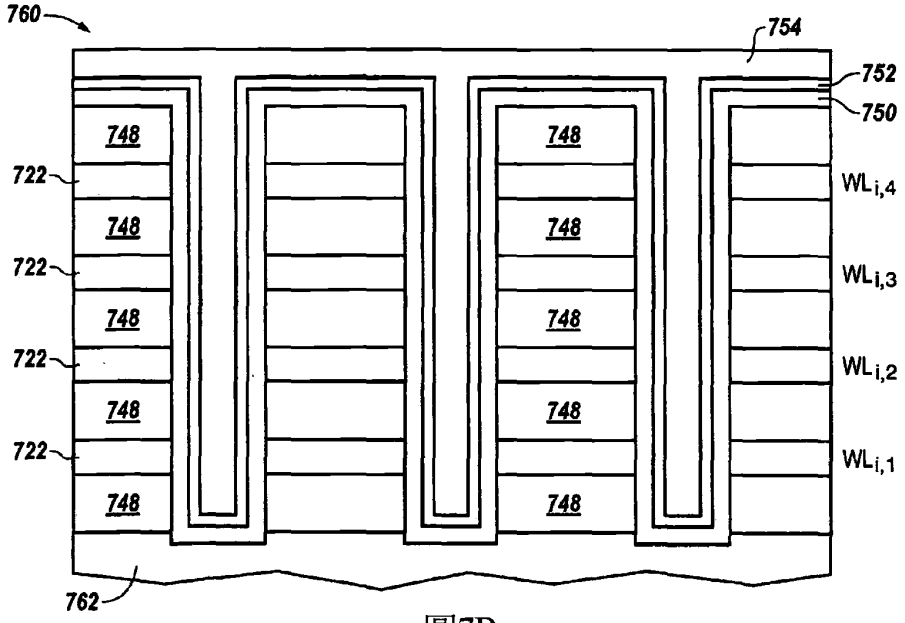

圖7B

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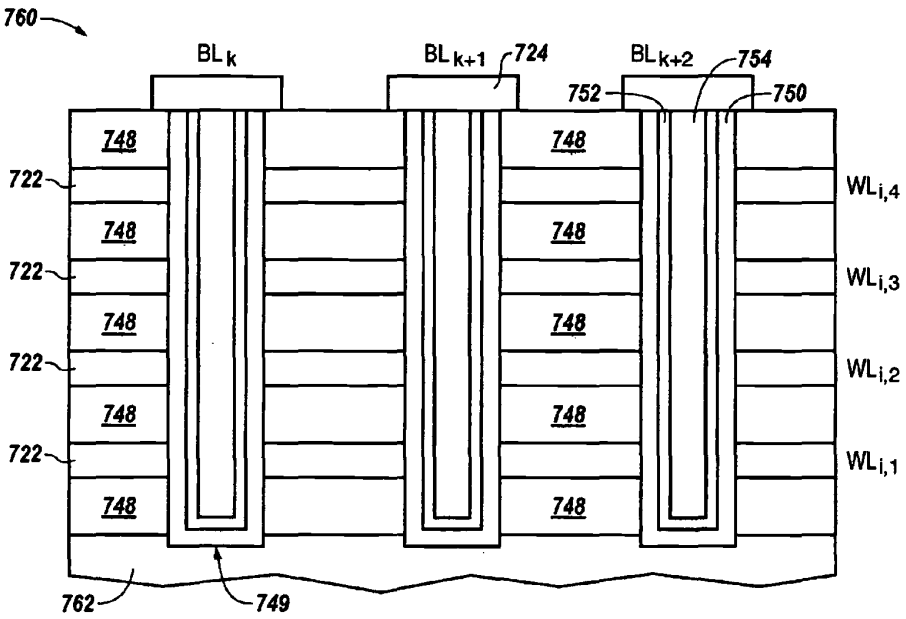

圖7C

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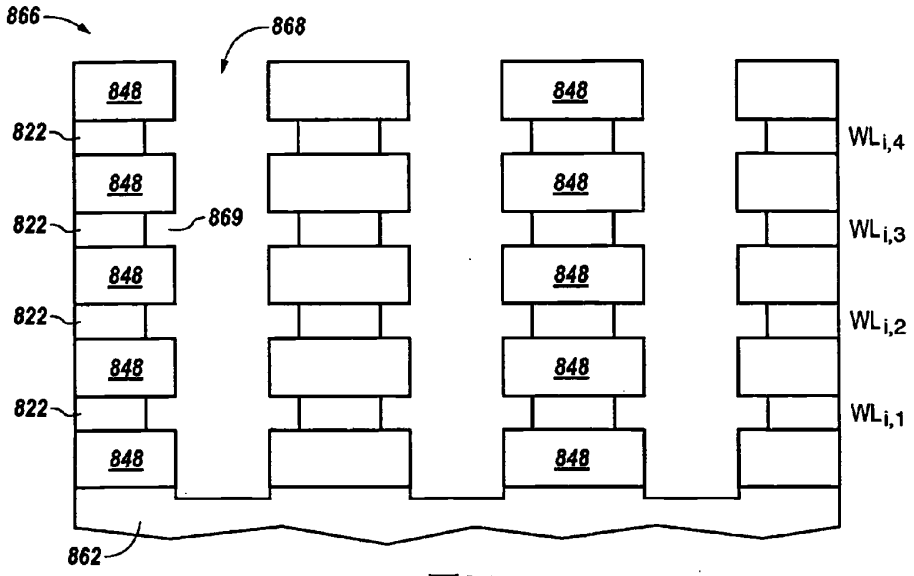

圖8A

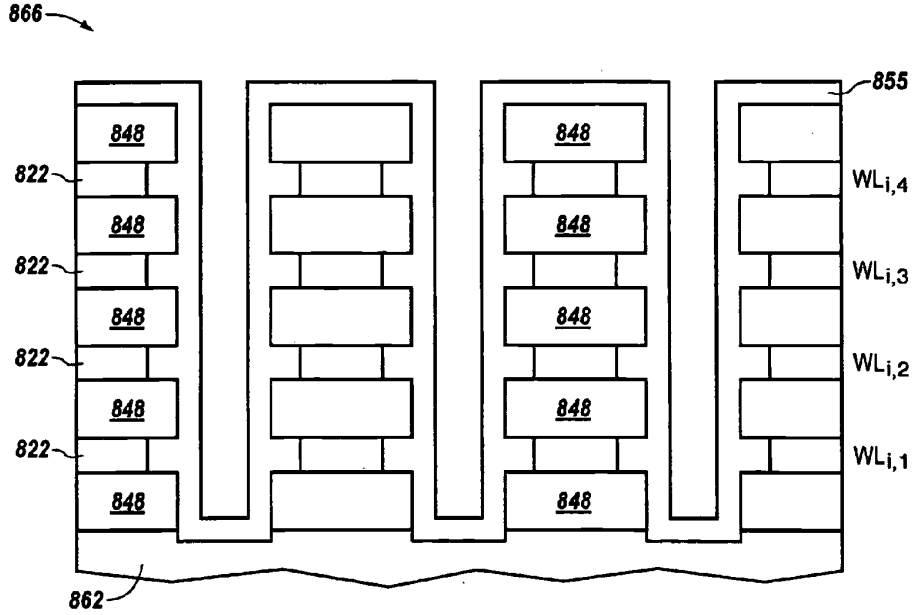

圖8B

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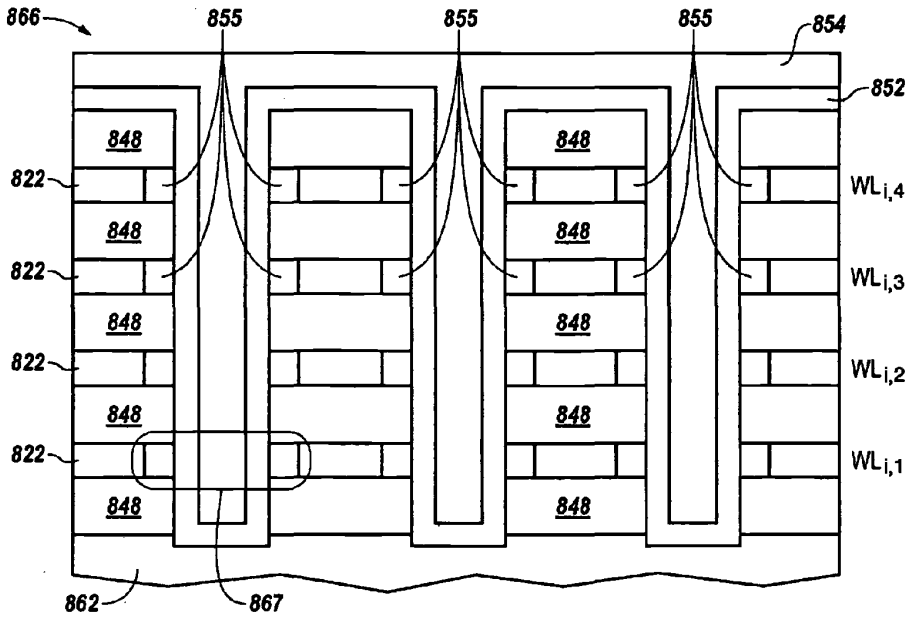

圖8C

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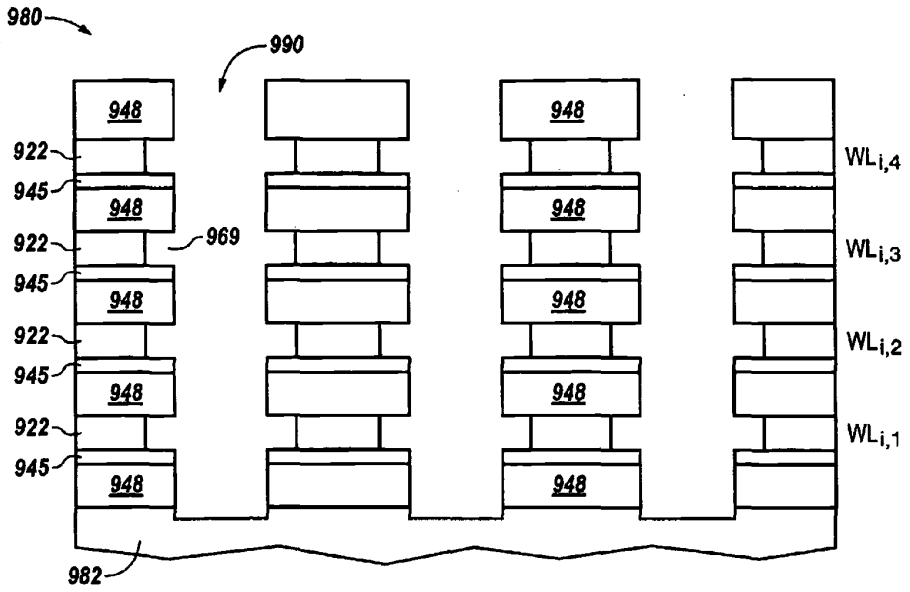

圖9A

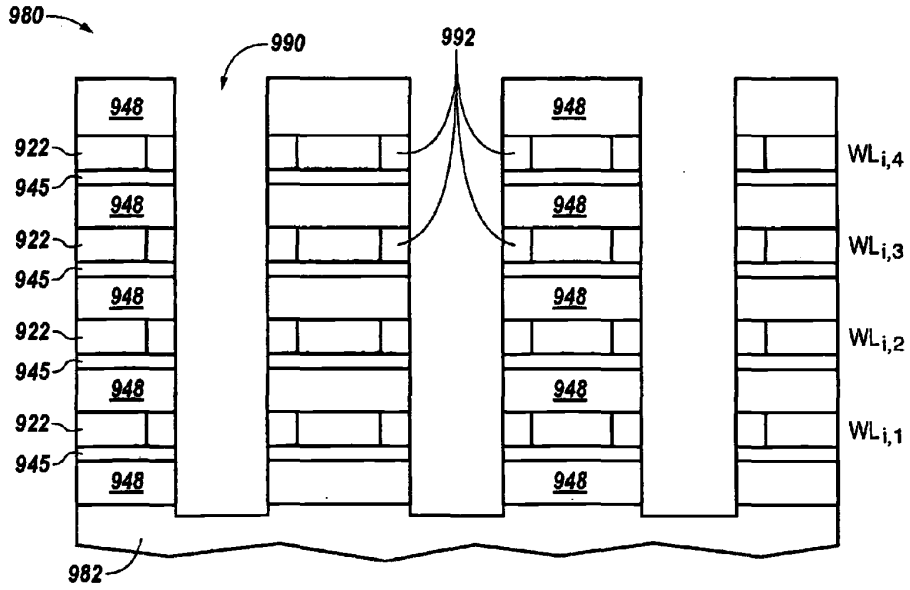

圖9B

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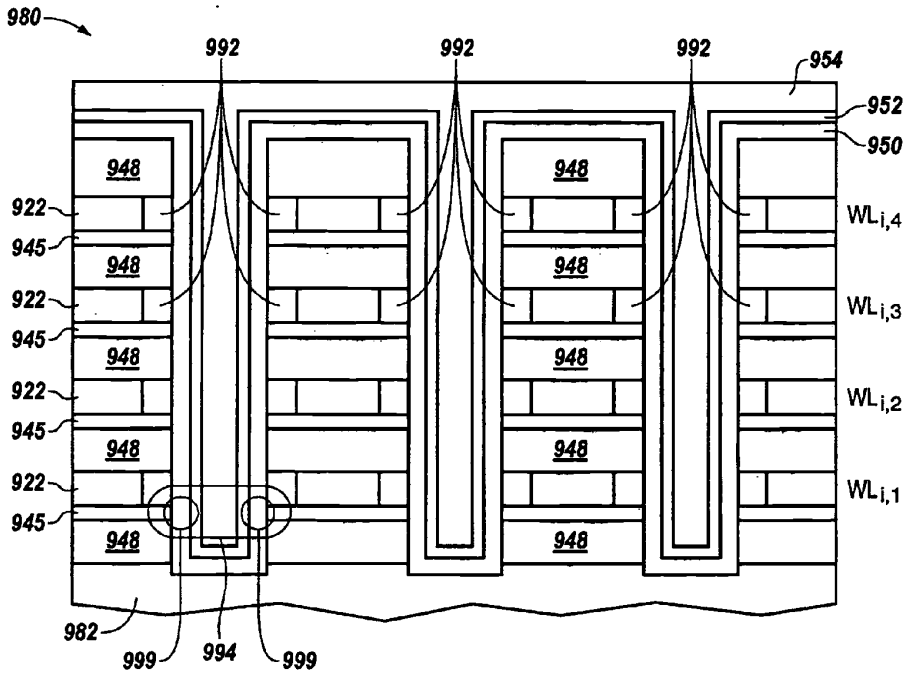

圖9C

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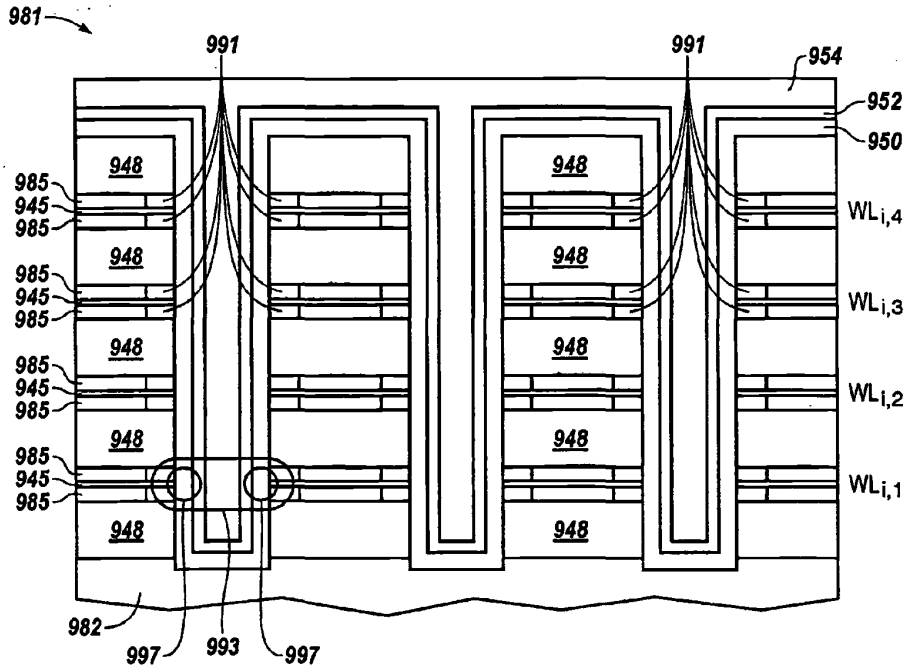

圖9D

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【代表圖】

【本案指定代表圖】：第（4）圖。

【本代表圖之符號簡單說明】：

422　字線

424　位元線

430　記憶體陣列

436　導電延伸部

438　記憶體單元

440　記憶體單元

441　記憶體單元

442　記憶體單元

【本案若有化學式時，請揭示最能顯示發明特徵的化學式】：

無

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(30)優先權：2014/07/11 美國 14/329,644

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申請實體審查：有 申請專利範圍項數：20 項 圖式數：6 共 52 頁

(54)名稱

用於三維電路裝置之供導電通道用的氧化鋁著陸層

ALUMINUM OXIDE LANDING LAYER FOR CONDUCTIVE CHANNELS FOR A THREE DIMENSIONAL CIRCUIT DEVICE

(57)摘要

一多層記憶體胞元堆疊體具有氧化鋁(AlOx)層作為貴 HiK 層以提供蝕刻停止選擇性。該堆疊體的各層包括一記憶體胞元裝置。該電路包括相鄰該多層記憶體胞元堆疊體的一源閘選擇多晶矽(SGS poly)層，其中該 SGS poly 層係用以給該多層堆疊體的該等記憶體胞元提供一閘極選擇信號。該電路也包括一導電源極層以給該堆疊體的該等層提供用於一通道之一源極導體。該 AlOx 層係位在該源極層與該 SGS poly 層間，且提供乾蝕刻選擇性及濕蝕刻選擇性兩者用以形成一通道而電氣耦合該等記憶體胞元至該源極層。

A multitier stack of memory cells having an aluminum oxide (AlOx) layer as a noble HiK layer to provide etch stop selectivity. Each tier of the stack includes a memory cell device. The circuit includes a source gate select polycrystalline (SGS poly) layer adjacent the multitier stack of memory cells, wherein the SGS poly layer is to provide a gate select signal for the memory cells of the multitier stack. The circuit also includes a conductive source layer to provide a source conductor for a channel for the tiers of the stack. The AlOx layer is disposed between the source layer and the SGS poly layer and provides both dry etch selectivity and wet etch selectivity for creating a channel to electrically couple the memory cells to the source layer.

指定代表圖：

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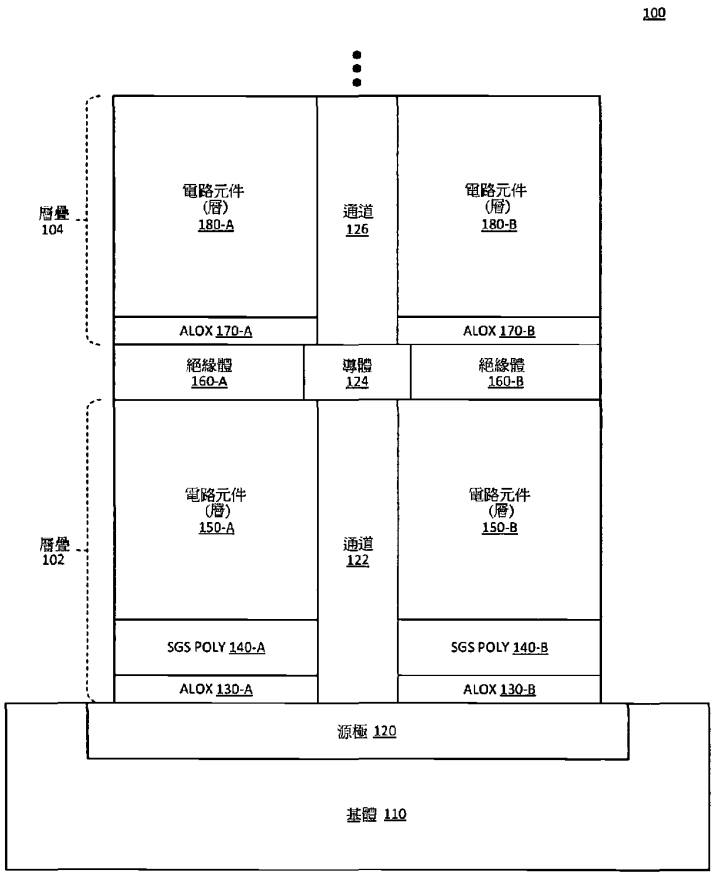

圖1

符號簡單說明：

100・・・系統

102、104・・・層疊

110・・・基體

120・・・源極、源極導體

122、126・・・通道

124・・・導體

130-A~B、170-A~B・・・ALOX、氧化鋁層

140-A~B・・・SGS POLY 層

150-A~B、180-A~B・・・電路元件

160-A~B・・・絕緣體

發明專利說明書

（本說明書格式、順序，請勿任意更動）

【發明名稱】（中文/英文）

用於三維電路裝置之供導電通道用的氧化鋁著陸層
ALUMINUM OXIDE LANDING LAYER FOR CONDUCTIVE CHANNELS FOR A THREE DIMENSIONAL CIRCUIT DEVICE

【技術領域】

發明領域

[0001]發明之實施例概略係有關於三維電路裝置，及更明確言之，提供用以對一三維電路裝置產生導體通道之氧化鋁著陸層。

著作權聲明/許可

[0002]本專利文件之部分揭示內容可能含有受著作權保護之材料。當本專利出現在專利商標局的專利檔案或記錄時，著作權擁有者並不反對任何人複製專利文件或專利揭示文，但仍然保有全部著作權權利。著作權聲明適用於後述全部資料及其附圖圖式，以及後述任何軟體：著作權©2014，英特爾公司(Intel Corporation)，版權所有。

【先前技術】

發明背景

[0003]一般期望計算及電子裝置及組件之大小持續地縮小，即便期望有來自裝置的更高效能與更大儲存容量亦復如此。此外，電路組件更加分開及使用的底板面積愈大，則裝置消耗的功率愈多。大小及功率消耗乃電子裝置及記

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憶體裝置的重要因素，特別對手持式應用及行動應用尤爲如此。晚近裝置製造上的發展提供了三維電路結構，形成具有較高密度的電子裝置。但各種材料及處理技術之物理學方面造成所得高密度裝置的故障及效能限制，因而妨礙了此等裝置的可行性。

【發明內容】

[0004]依據本發明之一實施例，係特地提出一種電路裝置，其包含：一多層記憶體胞元堆疊體，該堆疊體之各層包括有一記憶體胞元裝置；一源閘選擇多晶矽(SGS poly)層，其與該多層記憶體胞元堆疊體相鄰，該SGS poly層係用於針對該多層堆疊體之該等記憶體胞元提供一閘極選擇信號；一導電源極層，用以針對用於該堆疊體之該等層的一通道提供一源極導體；以及一氧化鋁(AlOx)層，其介在該源極層與該SGS poly層之間，該AlOx層提供用於使該SGS poly層與該源極層分開的一蝕刻停止層，其中，該AlOx層提供乾蝕刻選擇性也提供濕蝕刻選擇性，其中，一通道蝕刻處理蝕穿該多層記憶體胞元堆疊體及該SGS poly層並止於該AlOx層而不暴露出該源極層，並且其中，一選擇性閘極蝕刻處理蝕刻該等記憶體胞元中之閘極接點並蝕刻該AlOx層而暴露出該源極層。

【圖式簡單說明】

[0005]後文詳細說明部分包括藉由發明之實施例的體現例的討論附圖之例示。須瞭解附圖僅爲舉例說明而非限制性。如此處使用，須瞭解述及一或多個「實施例」係指

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包括於至少一個發明之體現中之一特定特徵、結構、及/或特性。如此，此處出現的片語諸如「於一個實施例中」或「於一替代實施例中」描述本發明之各種實施例及體現，且非必要全部皆係指相同實施例。但該等實施例及體現也非必然彼此互斥。

[0006]圖1爲具有AlOx著陸層之一堆疊電路之一實施例的方塊圖。

[0007]圖2A-2F爲具有AlOx蝕刻選擇性層的堆疊電路的各種階段之一實施例之方塊圖。

[0008]圖3爲具有AlOx著陸層帶有電流促進浮動閘極的一堆疊電路之一實施例的方塊圖。

[0009]圖4爲用以形成具有AlOx著陸層的堆疊中空通道電路之方法之一實施例的流程圖。

[0010]圖5爲計算系統之一實施例的方塊圖，其中可體現具有AlOx著陸層之一堆疊中空通道電路。

[0011]圖6爲行動裝置之一實施例的方塊圖，其中可體現具有AlOx著陸層之一堆疊中空通道電路。

[0012]後文某些細節及體現之描述包括圖式之描述可闡釋後述實施例之部分或全部，以及討論此處呈示之本發明之構想的潛在實施例及體現。

【實施方式】

較佳實施例之詳細說明

[0013]如此處描述，電路元件之一多層堆疊體包括氧化鋁(AlOx或ALOX)層作爲貴HiK層以提供蝕刻停止選擇

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性。藉由分享電路裝置之多層的一共用來源，該多層堆疊體許可更高密度的電子組件。多層堆疊體之應用包括記憶體裝置，其中各自包括記憶體胞元的多層能垂直堆疊。其它應用及其它組態亦屬可能。

[0014]於一個實施例中，堆疊體的各層包括一個記憶體胞元裝置或多個記憶體胞元裝置。利用此種多層堆疊體的一電路包括相鄰該多層記憶體胞元堆疊體的一源閘選擇多晶矽(SGS poly)層，該SGS poly層能給該多層堆疊體的該等記憶體胞元提供一閘極選擇信號。該電路也包括一導電源極層用以給該堆疊體的該等層提供用於一通道之一源極導體。如此，該等多個記憶體胞元各自能耦接至該源極。該AlOx層係設置於該源極層與該SGS poly層間且提供乾蝕刻選擇性及濕蝕刻選擇性兩者。蝕刻選擇性許可更有效處理一通道而電氣耦合該等記憶體胞元至該源極。

[0015]於一個實施例中，各層包括NAND記憶體胞元。如此，電路裝置爲三維(3D)記憶體裝置。於一個實施例中，處理建立了多層的一中空通道。傳統上用以形成此種柱體之化學在形成含多層電路元件之一期望柱體輪廓上有極限。更明確言之，形成電路元件之一多層堆疊體傳統上受缺乏蝕刻一致性(例如，蝕刻深度、蝕刻凹割)所限。舉例言之，以一記憶體裝置中多層字線堆疊在一起爲例，需要製程處理的一柱體具有比傳統上所能達成的更高的縱橫比。

[0016]形成堆疊電路或多層電路(又稱三維或3D電路)之其它辦法包括具有高介電常數之一層材料(HiK材料)。此

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種材料層傳統上設置於該SGS poly與電路元件層間，而非設置於該SGS poly與源極間。HiK材料提供電路內部之電氣絕緣以減少洩漏。曾經嘗試的HiK材料之例包括HfOx、ZrOx、及TanOx。須瞭解化學式表示型態諸如HfOx、ZrOx、TanOx、及AlOx(及也可能使用的其它者)爲氧化物化合物之通用表示型態而非特定化學式。各個表示型態係指包含第一元素之至少一個原子與氧之至少一個原子的氧化物化合物。各個元素的確切原子數目將隨體現及/或製程技術而異。AlOx乃對電路提供良好介電性質且比較其它HiK材料提供遠更佳的蝕刻性質之一種HiK材料。其它指示的HiK材料並不提供清潔材料或相對於標準以矽爲基礎的氧化物或多晶矽材料，許可濕蝕刻選擇性等良好性質。其它材料導致具有直徑顯著縮窄的導體通道，使得該通道更接近源極。此外或另外，其它材料允許凹割蝕刻，造成通道對通道短路。如此，其它材料無法獲得充分筆直的柱體。此等柱體瑕疵可能導致記憶體胞元的干擾及/或不同電路元件間的短路。

[0017] AlOx可被視爲「貴HiK」材料，表示其提供良好介電隔離，同時提供蝕刻選擇性。更明確言之，AlOx能提供濕蝕刻選擇性及乾蝕刻選擇性兩者。舉例言之，AlOx相較於用在字線堆疊體的多晶矽材料及氧化物提供良好選擇性。此種選擇性能改良SGS poly輪廓且改良蝕刻著陸以提供通道與源極導體層之接觸。如此，AlOx能提供較少程式干擾及較低捕陷。結果所得柱體比較使用傳統製程技術所

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能達成者具有更均一直徑。如所描述之AlOx層的使用也能增加導體通道的線串電流，且減少選擇閘臨界電壓(SG-Vt)之變化。此外，AlOx層於體現多層之多個層疊之應用中能改良柱體對柱體連續性。

[0018]後文詳細說明部分參照附圖。須瞭解附圖無需照比例繪製元件或組件。某些元件蓄意地不照比例繪製用於例示及討論目的。也須瞭解特定實施例係指層疊之垂直堆疊，彼此向上堆疊。於一個實施例中，電路可水平堆疊。

[0019]圖1爲具有AlOx著陸層之一堆疊電路之一實施例的方塊圖。系統100表示使用多層疊之電路元件層的電子電路裝置。替代處理於單一堆疊體內的全部電路元件且試圖形成一通道以操作全部電路元件，系統100係成層處理，使用多層疊之電路元件。

[0020]基體110表示於其上處理電子電路之一基體或半導體平台。系統100表示電子電路之一截面，且須瞭解典型地許多此等電路將在一半導體晶圓上同時處理。處理在基體110內或上形成(例如，沈積)源極導體120。源極導體120可致動或控制系統100之電路元件的電路操作。源極導體120爲高度導電材料，諸如金屬材料(例如，矽化鎢(WSix))或具有許多高遷移率載子的其它材料。於一個實施例中，源極導體120包括多層材料(例如，矽化鎢(WSix)層及高度摻雜多晶矽層)。須瞭解針對一功能電路並非全部電路元件皆例示於系統100。

[0021]ALOX(元件130-A及130-B)可提供源極導體120

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與源極閘極層SGS poly 140(元件140-A及140-B)間之電氣位障。層疊102包括電路元件150(元件150-A及150-B)，其係由SGS poly 140致動。須瞭解雖然顯示爲元件A及B，但層疊102可包括多個電路元件150，其係藉SGS poly 140透過通道122分開致動。A及B之標籤僅係用於例示目的。電路元件150在層疊102內部成層形成。如此，多個電路元件150可在層疊102內部彼此相鄰(例如，垂直相鄰)堆疊。層疊102可包括自數個電路元件至數十個電路元件(例如，36或38個記憶體胞元)。通道122將層疊102的全高/全長延伸至源極120，如此提供從源極120至電路元件150的電氣連結。通道122從層疊的一端延伸至層疊的另一端(例如，於垂直堆疊體的頂至底，或於水平堆疊體/列的邊至邊)。

[0022]於一個實施例中，系統100包括多個層疊，如由層疊104例示，層疊104係相鄰於層疊102建立或處理。層疊104包括電路元件180(元件180-A及180-B)。於一個實施例中，層疊104包括分開層疊104與層疊102的絕緣體160上之ALOX 170(元件170-A及170-B)。於一個實施例中，電路元件150及180在其個別層疊內部垂直堆疊爲電路元件層。於一個實施例中，形成電路元件180之處理係與形成電路元件150之處理相同，但於藉某些層疊處理操作分開的一不同層疊中執行。

[0023]於一個實施例中，處理在層疊102上產生絕緣體160(元件160-A及160-B)而提供一間隔體，層疊104可在該間隔體上被處理。導體124係在通道122末端處理，提供層疊

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104之通道126至層疊102之通道122並因而至源極120的電氣連結。須瞭解當源極120爲金屬層時，處理可包括蝕刻處理，其將產生具有一致性質的良好柱體而能夠生成通道122及126，而導體124爲高度導電材料或金屬材料。

[0024] ALOX 130及ALOX 170可對蝕刻製程提供著陸層，其分別爲通道122及126形成柱體。如此，ALOX 130及/或ALOX 170可致動系統100之處理而達成高度選擇性蝕刻操作。ALOX 130許可藉通道122良好電氣式接觸至源極120。ALOX 170許可藉通道126良好電氣式接觸至導體124。於一個實施例中，系統100之處理包括多個蝕刻操作，其可包括乾蝕刻處理及/或濕蝕刻處理。ALOX針對濕及乾蝕刻兩者提供高度選擇性蝕刻特性。特別述及層疊102，於一個實施例中，ALOX 130針對通道蝕刻其蝕穿電路元件150的多層堆疊體，提供一蝕刻停止層。ALOX 130可在ALOX層停止蝕刻而未暴露出源極120。該項處理可以閘極蝕刻選擇性地蝕刻ALOX 130，以蝕刻用於電路元件150及ALOX 130的閘極接點而暴露出源極120。

[0025] 系統100明確例示兩個層疊，層疊102及層疊104。須瞭解元件在不同層疊的分開，以及連結該等層疊之該等中空通道及停止層之高導電允許任何數目之層疊在系統100中堆疊。如此，基於該堆疊體，相對於該底板面積傳統上許可的數目，在系統100中之電路元件的總數可加倍、三倍、或以上。須瞭解此處描述的選擇性蝕刻可對層疊102執行，及系統100並不需要具有其它層疊(亦即，層疊104爲

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選擇性的)。於一個實施例中，層疊104經處理時，對層疊104的處理並不需要使用ALOX 170，但若層疊104中沒有多晶矽層，則能使用其它絕緣體。

[0026]圖2A-2F爲具有AlOx蝕刻選擇性層的堆疊電路的各種階段之一實施例之方塊圖。爲了舉例說明之目的，圖2A-2I例示具有多層記憶體胞元的三維堆疊記憶體裝置。更明確言之，圖2A-2F中之實例提出垂直堆疊記憶體裝置之一個具體實施例。於一個實施例中，此種處理可以「水平」方式出現，但係用於從半導體基體或半導體晶圓堆疊成的裝置。如此，於一個實施例中，「垂直」堆疊可指從該等裝置被處理及/或放置用於操作的半導體基體向外或向上遠離延伸電路的任何處理。處理包括AlOx層以提供選擇性蝕刻能力。

[0027]圖2A例示電路狀態202，其中多個電路元件層252係在源極220上方接受處理。於一個實施例中，ALOX 230係在源極220上接受處理。於一個實施例中，在源極220與ALOX 230間有氧化物層。於一個實施例中，氧化物層230係在ALOX 230上，在ALOX 230與SGS poly 240間處理。ALOX 230與源極220間之或在ALOX 230與SGS poly 240間之氧化物層能夠提供對通過該等各層至源極220處理的一柱體之蝕刻輪廓的控制。

[0028]於一個實施例中，源極層210包括一或多層材料。舉例言之，源極220可包括矽化鎢(WSix)、重度摻雜多晶矽、多晶矽化鎢（poly-tungsten silicide）、及/或其它高度

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導電材料。於一個實施例中，源極220包括自由載子導體，諸如n型摻雜多晶矽。須瞭解n型材料具有自由電子其提供電流流動(藉提供電荷)，而p型材料具有自由電洞其提供電流流動(藉接收電荷)。於一個實施例中，SGS poly 240包括p型摻雜多晶矽。具有多層252之層堆疊體250係在SGS poly 240上處理。層堆疊體250可包括絕緣體材料(例如，氧化物)及導電材料(例如，摻雜多晶矽)之交錯層。

[0029] 圖2B例示電路狀態204，其中處理形成用於通道導體之一或多柱體。於一個實施例中，一或多柱體260係藉衝壓蝕刻形成，衝壓蝕刻形成通過層堆疊體250，通過SGS poly 240，通過氧化物232，及進入ALOX 230的開口。ALOX 230可對形成柱體260提供蝕刻停止層。藉將ALOX 230置於SGS poly 240與源極220間，而非如傳統方式般置於SGS poly 240與層堆疊體250間，該項處理可改良SGS輪廓約百分之20至40。此種輪廓改良係指柱體260通過SGS poly層240的直徑地均勻一致。此外，具有ALOX層較爲接近源極220的ALOX 230之選擇性能夠改良接近源極的柱體260之直徑達約50%，其對導體提供遠更佳的輪廓。

[0030] 如於電路狀態204中表示，柱體260可蝕刻入ALOX 230且停止於ALOX層內部而不蝕刻入源極220。於一個實施例中，柱體260可藉乾蝕刻處理而蝕刻入ALOX 230。如此，ALOX 230可對極高縱橫比結構(例如，約25之縱橫比)提供乾蝕刻著陸窗而不孔蝕入源極220。於蝕刻柱體260入ALOX 230之後(例如，於乾蝕刻處理之後)，取決於

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製造中及/或製程中之堆疊體變化，柱體260可蝕刻入ALOX 230內部的任何位置。如使用兩個不同柱體260例示，蝕刻入ALOX可能蝕刻入相同裝置內部之不同柱體內部或深或淺，且在不同裝置上使用相同處理，可蝕刻不等量入ALOX。

[0031]電路狀態204也表示處理殘餘物262。殘餘物262表示蝕刻期間能回濺鍍入柱體260的物質。舉例言之，於乾蝕刻期間，來自ALOX 230之物質可回濺鍍入柱體260。柱體260中之HiK殘餘物除非能夠從柱體260內部被清除，否則能夠阻擋連續整合處理及晶胞的形成。

[0032]圖2C例示電路狀態206，其中製程潔淨了柱體260及暴露出源極220。如前文就圖2B之描述，蝕刻處理之完成可能導致柱體260內部之殘餘物料，及柱體不會完全蝕穿ALOX 230到源極220。於一個實施例中，處理包括接續乾蝕刻處理之後的濕蝕刻處理以對源極220做成接觸。於一個實施例中，ALOX 230爲或包括非晶形ALOX。於此一實施例中，習知濕蝕刻技術，諸如HF(氫氟酸蝕刻)及BOE(緩衝氧化物蝕刻，其包括用於蝕刻化學的緩衝劑)，能夠極其潔淨地清除濺鍍材料，以及對暴露出源極220提供高度選擇性。

[0033]使用ALOX 230作爲HiK材料層於源極220與SGS poly 240間能提供50:1 HF清潔選擇性，及約100:1 BOE清潔選擇性。此外，比較SGS poly 240之多晶矽及/或氧化物232，ALOX 230能提供10:1乾蝕刻選擇性。即便呈非晶形形式，相對選擇性地對ALOX 230而言亦爲真。於一個實施

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例中，藉於高溫(例如，950-1100℃範圍)結晶化ALOX膜，可提高ALOX 230之濕及乾蝕刻選擇性達約三倍。此種結晶化可對連續製程操作或步驟提供額外整合效果，例如，當期望ALOX層從裝置的某些部分不被蝕刻或清除時。

[0034]圖2D例示電路狀態208，其中製程凹陷了該等層用於浮動閘極處理。於一個實施例中，製程凹陷了ALOX 230也用於浮動閘極處理。於一個實施例中，製程不會在ALOX層內部形成浮動閘極。製程在各層252內部形成凹部264。於一個實施例中，製程在ALOX 230內部形成類似的凹部。凹部例如可藉蝕刻操作產生。於一個實施例中，形成凹部264的蝕刻操作可爲用以自柱體260清除ALOX殘餘物的相同處理程序，及處理程序之連續能產生凹部。

[0035]圖2E例示電路狀態210，其中製程在層252中形成浮動閘極270。於其中製程也在ALOX 230中形成浮動閘極的一個實施例中，製程在ALOX 230形成虛設浮動閘極272。浮動閘極270在操作上有功能，因而回應於一選擇信號，浮動閘極270操作爲閘極。虛設浮動閘極272也可回應於一選擇信號操作，且當致動時就提高電流流動之意義而言可具有功能性，但並非以浮動閘極270的相同意義具有操作功能性，在於ALOX 230並不包括回應於一選擇閘極信號被觸發的一記憶體胞元或其它電路元件。

[0036]圖2F例示電路狀態212，其中製程在柱體中形成導體通道。通道280表示有一導體形成於柱體260之壁面及底部(最接近源極120之部分)上的柱體(顯示於上圖)。於一

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個實施例中，通道280以絕緣體(例如，氧化物)填補，絕緣體係被導體環繞，因而稱作爲一中空通道。中空通道導體係指在壁面上有一薄層導體(例如，夠薄以縮小晶粒大小而控制導體材料的電阻係數)及通道內部有一絕緣體的一柱體。導體與源極220且與浮動閘極270(及在形成閘極272的一體現中之閘極272)形成歐姆接觸。如此，通道280提供自源極220至浮動閘極270的電氣連結。於一個實施例中，虛設閘極272可由如同浮動閘極270的相同閘極選擇信號觸發。如此，ALOX 272中之虛設閘極272可改良從源極220至通道280的電流流動，其可改良所得電路之電氣性質。於一個實施例中，電路元件層之其它層疊可在所顯示的電路上處理。

[0037]圖3爲具有AlOx著陸層帶有電流促進浮動閘極的一堆疊電路之一實施例的方塊圖。電路300可爲圖1之系統100的一例，或爲電路狀態202、204、206、208、210、212的一例。更明確言之，電路300提供相鄰該導體通道之一經處理的凹部特寫的表示型態。該製程在凹部形成元件390。

[0038]於一個實施例中，電路300包括源極層312及314，其可爲源極220之一例。於一個實施例中，源極312爲WSix或其它金屬材料。於一個實施例中，源極314爲源極多晶材料(諸如n型摻雜多晶矽)。須瞭解源極並非必然需要兩層材料，於一個實施例中，一種材料或另一種材料可作爲源極層。

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[0039]電路300包括SGS poly層340與源極間之ALOX層330。雖然於圖中並未特定顯示，但電路300可包括在ALOX 330與SGS poly 340間之氧化物層。於一個實施例中，電路300包括ALOX 330與源極間之氧化物層320。此種氧化物層(可爲極薄，例如ALOX 330之厚度之約1/8至1/20)可協助防止ALOX 330凹陷期間可能的凹刻柱體至柱體短路。於一個實施例中，ALOX 330的厚度可爲約40-100奈米，及氧化物320的厚度可爲約5奈米。於一個實施例中，SGS poly 340的厚度可爲約100-200奈米。

[0040]於一個實施例中，電路300包括氧化物350以隔離層之堆疊體與SGS poly 340，且在電路元件間包括隔離層370(諸如氧化物或氮化物)。各個隔離層360之厚度可爲約20奈米。於記憶體裝置之一體現中，該等電路元件可形成爲字線(WL)多晶矽360，如圖中例示，具有一浮動閘極及記憶體胞元。字線(WL)多晶矽360之厚度可爲約30奈米。電路300可包括由處理操作所支援的任何數目之層數。取決於層數，電路300之電路元件的一層疊自源極312至最後一層的總厚度可爲約2000-3000奈米，或甚至更厚。此外，於一個實施例中，電路300可包括多個堆疊層疊，各自具有多個堆疊層。

[0041]該圖的插圖到側邊例示電路元件390的特寫透視圖，於一個實施例中，其係形成於凹陷通道380中。針對透視圖，例示通道380、SGS poly 340、ALOX 330、及氧化物320部分。類似電路元件390的結構體也可形成於各層內，

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如電路300中顯示。於一個實施例中，於電路元件層中，該層可包括另一層電介質394以隔離該電路元件與字線(WL)多晶矽360。於一個實施例中，通道導體392沿著通道380且環繞電路元件390之浮動閘極及胞元組件延伸。電路元件390可包括在通道導體392與浮動閘極396間的電介質394。於一個實施例中，電路元件390包括相鄰浮動閘極396及電介質394的胞元398。ALOX層330可包括一個未被定址的虛設胞元，因而具有類似記憶體胞元的功能，但未儲存有用的資訊且不被存取用於讀或寫操作。但電路元件390的致動可改良電路300的線串電流及連續性。

[0042]圖4爲用以形成具有AlOx著陸層的堆疊中空通道電路之方法之一實施例的流程圖。方法400可以是產生電路及電路狀態的方法之一例，諸如類似圖2A-2F、圖1之系統100、及/或圖3之電路300。方法400可藉製造實體的處理設備執行。製造商組配處理設備，且在半導體晶圓上執行一串列的處理步驟或操作以形成電子電路。處理設備可包括執行任一類型材料處理操作(沈積、CMP、蝕刻、離子植入、退火、其它)的工具。此種處理設備包括執行處理的電腦設備及機械工具及電氣工具。處理設備由一或多個處理操作控制電路加以控制，該控制電路可包括硬體邏輯及/或軟體/韌體邏輯以控制該項處理。該設備可經規劃或組配以某個次序執行某些操作。集合而言，設備及處理或組態可稱作處理系統。爲了方法400之目的，操作被描述爲由「處理」執行，該處理間接地係指製造商及由製造商使用的處

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理系統。

[0043]處理在半導體基體諸如矽晶圓上或內形成一源極層，402。處理在源極上形成電子電路。源極爲一導體，該導體可被致動而在電路元件形成電氣活性。源極層可包括金屬材料，或摻雜多晶矽材料，或兩者。於一個實施例中，處理在源極上方沈積緩衝氧化物，404。緩衝氧化物爲絕緣體。處理形成AlOx蝕刻停止著陸層，406。AlOx層給濕蝕刻及乾蝕刻操作提供選擇性，且屬HiK介電材料。如此，AlOx層能提供HiK材料的基於其蝕刻選擇性的電氣效果(諸如前文描述)。

[0044]處理沈積或以其它方式給電子電路產生選擇閘源多晶矽層，408。於一個實施例中，選擇閘極乃在電路元件的多層堆疊體中用於全部電路元件的閘極。處理形成電路元件層的一層疊，410。於一個實施例中，處理沈積胞元層或其它電路元件層。於一個實施例中，處理形成電路元件層垂直堆疊在彼此。電路元件層可藉作爲層間絕緣體的氧化物材料分開。

[0045]於一個實施例中，處理形成一柱體，諸如藉衝壓蝕刻而暴露出胞元層疊下方的源極導體層，412。由於AlOx的高度選擇性及AlOx位在選擇閘極層與源極層間之位置故，柱體將停止在AlOx層上或AlOx層內而不暴露源極或孔蝕源極。

[0046]於一個實施例中，處理執行多重蝕刻處理(或子-處理)其可提供柱體的良好輪廓，414。柱體的良好輪廓係

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指柱體接近源極的直徑係與柱體接近堆疊體的多層的直徑可相媲美。須瞭解柱體直徑的顯著變異造成堆疊體的記憶體胞元或電路元件的效能變異。如此，良好的柱體輪廓允許堆疊體的全部電路元件在效能公差以內操作。於一個實施例中，良好的柱體輪廓具有柱體直徑沿柱體的長度自最遠離源極該層至最靠近源極該層不被掐掉或封閉。須瞭解在AlOx層的凹部中形成虛設胞元或虛設閘極用於評估通道的良好輪廓時係不被視爲改變柱體的直徑。

[0047]於一個實施例中，處理在AlOx層進行凹刻蝕刻而在AlOx層形成一浮動閘極，416。然後，該處理可處理在電路元件層以及在AlOx層中的一浮動閘極，418。處理可沈積一通道導體以沿通道自源極至電路元件的多層提供電氣式接觸，420。於一個實施例中，處理繼續形成電路元件之多層的層疊，422。

[0048]圖5爲計算系統之一實施例的方塊圖，於該計算系統中，可體現具有AlOx著陸層之一堆疊中空通道電路。系統500表示依據此處描述的任何實施例之計算裝置，而可以是膝上型電腦、桌上型電腦、伺服器、遊戲或娛樂控制系統、掃描器、影印機、列印器、路徑或切換裝置、或其它電子裝置。系統500包括處理器520，處理器520提供系統500的處理、作業管理、及指令執行。處理器520可包括任何型別的微處理器、中央處理單元(CPU)、處理核心、或其它處理硬體以提供系統500的處理。處理器520控制系統500之總體操作，且可以是或可包括一或多個可規劃通用或特

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用微處理器、數位信號處理器(DSP)、可規劃控制器、特定應用積體電路(ASIC)、可規劃邏輯裝置(PLD)等或此等裝置的組合。

[0049]記憶體子系統530表示系統500之主記憶體，提供欲藉處理器520執行的代碼之或欲用於執行一常式的資料值之暫時儲存。記憶體子系統530可包括一或多個記憶體裝置，諸如唯讀記憶體(ROM)、快閃記憶體、隨機存取記憶體(RAM)之一或多個變化、或其它記憶體裝置、或此等裝置的組合。記憶體子系統530儲存且主持作業系統(OS)536等以提供用以於系統500執行指令的一軟體平台。此外，其它指令538係自記憶體子系統530儲存與執行以提供系統500之邏輯及處理。作業系統(OS)536及指令538係藉處理器520執行。記憶體子系統530包括記憶體裝置532，在該記憶體裝置532儲存資料、指令、程式、或其它項目。於一個實施例中，記憶體子系統包括記憶體控制器534，其乃產生與簽發指令給記憶體裝置532的一記憶體控制器。須瞭解記憶體控制器534可爲處理器520的實體部件。

[0050]處理器520及記憶體子系統530耦合至匯流排/匯流排系統510。匯流排510是個抽象概念，表示由適當橋接器、配接器、及/或控制器連結的任一個或任多個分開實體匯流排、通訊線/介面、及/或點對點連結。因此，匯流排510可包括例如系統匯流排、周邊組件互連(PCI)匯流排、超傳輸或工業標準架構(ISA)匯流排、小型電腦系統介面(SCSI)匯流排、通用串列匯流排(USB)、或美國電機及電子工程師

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學會(IEEE)標準1394匯流排(俗稱「火線」)中之一或多者。匯流排510之該等匯流排也可相對應於網路介面550中之介面。

[0051]系統500也包括一或多個輸入/輸出(I/O)介面540、網路介面550、一或多個內部大容量儲存裝置560、及耦接至匯流排510的周邊介面570。I/O介面540可包括一或多個介面組件，使用者透過該等介面組件與系統500互動(例如，視訊、音訊、及/或文數介接)。於一個實施例中，I/O介面540可包括一高畫質(HD)顯示器，其提供輸出給一使用者。高畫質可指具有約100 PPI(每吋像素)的像素密度之一顯示器，且可包括諸如全HD(例如，1080p)、視網膜顯示器、4K(超高畫質或UHD)或其它格式。高畫質也可指具有與像素顯示器可相媲美的視覺品質之投影顯示器(例如，頭戴式顯示器)。網路介面550提供給系統500透過一或多個網路與遠端裝置(例如，伺服器、其它計算裝置)通訊的能力。網路介面550可包括乙太網路配接器、無線互連組件、通用串列匯流排(USB)、或其它以有線或無線標準爲基礎的或專有的介面。

[0052]儲存裝置560可以是或可包括以非依電性方式儲存大量資料的任何習知媒體，諸如一或多個以磁性、以固態、或以光學爲基礎之碟片、或其組合。儲存裝置560保有代碼或指令或資料562於持續狀態(亦即，儘管系統500的電力中斷但數值仍然保留)。儲存裝置560可籠統視爲一「記憶體」，但記憶體530才是提供指令給處理器520的執行記憶

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體或操作記憶體。雖然儲存裝置560爲非依電性，但530可包括依電性記憶體(亦即，若系統500的電力中斷，則資料之數值或狀態爲不確定)。

[0053]周邊介面570可包括前文未特別提及的任何硬體介面。周邊裝置通常係指附屬連結至系統500的裝置。附屬連結是系統500在其上執行操作，及一使用者與其互動的軟體平台及/或硬體平台。

[0054]於一個實施例中，記憶體子系統530(例如，記憶體裝置532)及/或系統500之其它組件包括形成爲堆疊電路的元件，該堆疊電路含有導體通道著陸在AlOx蝕刻停止著陸層上。藉由形成電路元件爲垂直層，系統500之硬體組件可在比傳統可能的底板面積更小的底板面積上體現。導體通道讓多個堆疊電路元件能夠電氣連結至一共通源極層。AlOx層提供讓堆疊電路跨不同處理變方發揮功能的一處理輪廓。

[0055]圖6爲行動裝置之一實施例的方塊圖，於該行動裝置中，可體現具有AlOx著陸層之一堆疊中空通道電路。裝置600表示行動計算裝置，諸如計算平板、行動電話或智慧型電話、無線電子閱讀器、穿戴式計算裝置、或其它行動裝置。須瞭解某些組件係概略顯示，並非此種裝置的全部組件皆顯示於裝置600。

[0056]裝置600包括處理器610，處理器610執行裝置600的主要處理操作。處理器610可包括一或多個實體裝置，諸如微處理器、應用處理器、微控制器、可規劃邏輯裝置、

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或其它處理裝置。由處理器610執行的處理操作包括作業平台或作業系統的執行，於其上執行應用程式及/或裝置功能。處理操作包括與使用人的輸入/輸出(I/O)相關操作、電源管理的相關操作、及/或裝置600連結至其它裝置的相關操作。處理操作也可操作音訊I/O及/或顯示I/O的相關操作。

[0057]於一個實施例中，裝置600包括音訊子系統620，其表示提供音訊功能給計算裝置相關聯的硬體組件(例如，音訊硬體及音訊電路)及軟體組件(例如，驅動程式、編碼譯碼器)。音訊功能可包括揚聲器及/或耳機輸出，以及麥克風輸入。此種功能之裝置可整合入裝置600，或可連結至裝置600。於一個實施例中，一使用者藉提供由處理器610接收的及處理的音訊指令而與裝置600互動。

[0058]顯示子系統630表示給一使用者提供視覺顯示及/或觸覺顯示而與計算裝置互動的硬體組件(例如，顯示裝置)及軟體組件(例如，驅動程式)。顯示子系統630包括顯示介面632，其包括用以給一使用者提供一顯示的特定螢幕或硬體裝置。於一個實施例中，顯示介面632包括與處理器610分開的邏輯以執行與該顯示相關的至少若干處理。於一個實施例中，顯示子系統630包括提供輸出及輸入兩者給一使用者的觸控螢幕裝置。於一個實施例中，顯示子系統630包括提供輸出給一使用者的高畫質(HD)顯示器。高畫質可指具有約100 PPI(每吋像素)的像素密度之一顯示器，且可包括諸如全HD(例如，1080p)、視網膜顯示器、4K(超高畫質或UHD)或其它格式。高畫質也可指具有與像素顯示器可相

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媲美的視覺品質之投影顯示器(例如，頭戴式顯示器)。

[0059]I/O控制器640表示與一使用者互動相關的硬體裝置及軟體組件。I/O控制器640可操作以管理硬體，該硬體屬於音訊子系統620及/或顯示子系統630之部件。此外，I/O控制器640例示連結至裝置600的額外裝置之一連結點，一使用者透過該連結點可與系統互動。舉例言之，可附接至裝置600的裝置可包括麥克風系統、揚聲器或立體聲系統、視訊系統或其它顯示裝置、鍵盤或數字小鍵盤裝置、或用於特定應用的其它I/O裝置，諸如卡片讀取器或其它裝置。

[0060]如前述，I/O控制器640可與音訊子系統620及/或顯示子系統630互動。舉例言之，經由麥克風或其它音訊裝置輸入可提供輸入或針對裝置600的一或多個應用程式或功能之指令。此外，替代或除了顯示輸出之外，可提供音訊輸出。於另一個實施例中，若顯示子系統包括觸控螢幕，則顯示裝置也可作爲輸入裝置，其可由I/O控制器640至少部分管理。在裝置600上也可有額外按鈕或開關以提供由I/O控制器640管理的I/O功能。

[0061]於一個實施例中，I/O控制器640管理裝置，諸如加速度計、相機、感光器或其它環境感測器、陀螺儀、全球定位系統(GPS)、或可含括於裝置600內的其它硬體。輸入可爲直接使用者互動部件，以及提供環境輸入給系統以影響其操作(諸如，過濾雜訊，調整用於亮度檢測之顯示，給相機施加閃光燈，或其它特性件)。於一個實施例中，裝

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置600包括電源管理650，電源管理650管理電池電力的使用，蓄電池的充電，及節電操作的相關特徵。

[0062]記憶體子系統660包括用以儲存資訊於裝置600中的記憶體裝置662。記憶體子系統660可包括非依電性(記憶體裝置的電力中斷時狀態不改變)及/或依電性(記憶體裝置的電力中斷時狀態不定)記憶體裝置。記憶體660可儲存應用程式資料、使用者資料、音樂、照片、文件、或其它資料、以及系統600之應用程式及功能執行相關系統資料(無論爲長期或短期)。於一個實施例中，記憶體子系統660包括記憶體控制器664(其也可視爲系統600之控制部件，可能潛在考慮爲處理器610部件)。記憶體控制器664包括一排程器以產生及簽發指令給記憶體裝置662。

[0063]連接性670包括硬體裝置(例如，無線及/或有線連接器及通訊硬體)及軟體組件(例如，驅動程式、協定堆疊)以便裝置600能與外部裝置通訊。外部裝置可爲分開裝置，諸如其它計算裝置、無線存取點或基地台，以及周邊裝置諸如頭戴式裝置、列印器、或其它裝置。

[0064]連接性670可包括多個不同類型的連接性。概略言之，裝置600例示有小區式連接性672及無線連接性674。小區式連接性672大致係指由無線載波提供的小區式網路連接性，諸如透過全球行動通訊系統(GSM)或變化或衍生、劃碼多向接取(CDMA)或變化或衍生、分時多工(TDM)或變化或衍生、長期演進(LTE，又稱4G)、或其它小區式服務標準。無線連接性674係指非屬小區式的無線連接性，且

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可包括個人區域網路(諸如藍牙)、區域網路(諸如WiFi)、及/或廣域網路(諸如WiMax)、或其它無線通訊。無線通訊係指經由調諧電磁輻射的使用透過半固態媒體傳輸資料。有線通訊經由固態通訊媒體發生。

[0065]周邊連接680包括硬體介面及連接器，以及軟體組件(例如，驅動程式、協定堆疊)以做周邊連接。須瞭解裝置600可以是其它計算裝置的周邊裝置(至682)，以及具有周邊裝置(自684)連接其上兩者。裝置600常見有一「對接」連接器以連接至其它計算裝置用於諸如管理(例如，下載及/或上傳、改變、同步化)裝置600上的內部之目的。此外，對接連接器許可裝置600連接至某些周邊裝置，許可裝置600控制內容輸出，例如輸出至影音系統或其它系統。

[0066]除了專有對接連接器或其它專有連接硬體之外，裝置600可透過常用的或以標準爲基礎的連接器做周邊連接680。常見類型可包括通用串列匯流排(USB)連接器(其可包括多種不同硬體介面中之任一者)、顯示埠包括迷你顯示埠(MDP)、高畫質多媒體介面(HDMI)、火線、或其它類型。

[0067]於一個實施例中，記憶體子系統660(例如，記憶體裝置662)及/或裝置600之其它組件包括被形成爲具有導體通道著陸在AlOx蝕刻停止層上的堆疊電路之元件。藉將電路元件形成爲垂直層，系統500之硬體組件可在比傳統可能的底板面積更小的底板面積上體現。導體通道讓多個堆疊電路元件能夠電氣連結至一共通源極層。AlOx層提供讓

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堆疊電路跨不同處理變數發揮功能的一處理輪廓。

[0068]於一個面向中，一種電路裝置包括：一多層記憶體胞元堆疊體，該堆疊體之各層包括一記憶體胞元裝置；相鄰該多層記憶體胞元堆疊體的一源閘選擇多晶矽(SGS poly)層，該SGS poly層用以給該多層堆疊體的該等記憶體胞元提供一閘極選擇信號；一導電源極層用以給該堆疊體的該等層提供用於一通道之一源極導體；及在該源極層與該SGS poly層間之一氧化鋁(AlOx)層，該AlOx層提供一蝕刻停止層以分開該SGS poly層與該源極層，其中該AlOx層提供乾蝕刻選擇性及濕蝕刻選擇性兩者，其中一通道蝕刻蝕穿該多層記憶體胞元堆疊體及該SGS poly層，且停止於該AlOx層而不會暴露出該源極層，及其中一選擇性閘極蝕刻蝕刻該等記憶體胞元中之閘極接點及蝕刻該AlOx層而暴露出該源極層。

[0069]於一個實施例中，該SGS poly層包含一p型摻雜多晶矽。於一個實施例中，該源極層包括矽化鎢、重度摻雜多晶矽、或多晶矽化鎢中之一或多者。於一個實施例中，該源極層包含一n型摻雜多晶矽。於一個實施例中，該AlOx層進一步包含：由該閘極選擇信號觸發之一浮動閘極用以提供自該源極層至該多層記憶體胞元堆疊體的電流。於一個實施例中，該通道包含延伸通過該多層堆疊體之一中空通道，該中空通道包括環繞一通道絕緣體的導電材料以提供電氣式接觸給該等記憶體胞元之閘極；其中該AlOx層浮動閘極提供自該源極層至該中空通道的電流。於一個實施

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例中，進一步包含：在該AlOx層與該SGS poly層間之一氧化物層。於一個實施例中，進一步包含：在該AlOx層與該源極層間之一氧化物層。

[0070]於一個面向中，一種電子裝置包括：一三維堆疊記憶體裝置用以儲存資料，該記憶體裝置包括：一多層記憶體胞元堆疊體，該堆疊體之各層包括一記憶體胞元裝置；相鄰該多層記憶體胞元堆疊體的一源閘選擇多晶矽(SGS poly)層，該SGS poly層用以給該多層堆疊體的該等記憶體胞元提供一閘極選擇信號；一導電源極層用以給該堆疊體的該等層提供用於一通道之一源極導體；及在該源極層與該SGS poly層間之一氧化鋁(AlOx)層，該AlOx層提供一蝕刻停止層以分開該SGS poly層與該源極層，其中該AlOx層提供乾蝕刻選擇性及濕蝕刻選擇性兩者，其中一通道蝕刻蝕穿該多層記憶體胞元堆疊體及該SGS poly層，且停止於該AlOx層而不會暴露出該源極層，及其中一選擇性閘極蝕刻蝕刻該等記憶體胞元中之閘極接點及蝕刻該AlOx層而暴露出該源極層；耦接一高畫質顯示器以基於儲存於該記憶體裝置中之資料而產生一顯示畫面。

[0071]於一個實施例中，該SGS poly層包含一p型摻雜多晶矽。於一個實施例中，該源極層包括矽化鎢、重度摻雜多晶矽、或多晶矽化鎢中之一或多者。於一個實施例中，該源極層包含一n型摻雜多晶矽。於一個實施例中，該AlOx層進一步包含：由該閘極選擇信號觸發之一浮動閘極用以提供自該源極層至該多層記憶體胞元堆疊體的電流。於一

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個實施例中，該通道包含延伸通過該多層堆疊體之一中空通道，該中空通道包括環繞一通道絕緣體的導電材料以提供電氣式接觸給該等記憶體胞元之閘極；其中該AlOx層浮動閘極提供自該源極層至該中空通道的電流。於一個實施例中，該記憶體裝置進一步包含：在該AlOx層與該SGS poly層間之一氧化物層。於一個實施例中，該記憶體裝置進一步包含：在該AlOx層與該源極層間之一氧化物層。

[0072]於一個面向中，一種用於形成具有一AlOx著陸層之一堆疊電路之方法包括：產生一多層記憶體胞元堆疊體，該堆疊體之各層包括一記憶體胞元裝置；相鄰該多層記憶體胞元堆疊體形成一源閘選擇多晶矽(SGS poly)層，該SGS poly層用以給該多層堆疊體的該等記憶體胞元提供一閘極選擇信號；在一半導體基體上形成一導電源極層用以給該堆疊體的該等層提供用於一通道之一源極導體；及在該源極層與該SGS poly層間形成一氧化鋁(AlOx)層，該AlOx層提供一蝕刻停止層以分開該SGS poly層與該源極層，其中該AlOx層提供乾蝕刻選擇性及濕蝕刻選擇性兩者，其中一通道蝕刻蝕穿該多層記憶體胞元堆疊體及該SGS poly層，且停止於該AlOx層而不會暴露出該源極層，及其中一選擇性閘極蝕刻蝕刻該等記憶體胞元中之閘極接點及蝕刻該AlOx層而暴露出該源極層。

[0073]於一個實施例中，形成該SGS poly層包含形成一p型摻雜多晶矽。於一個實施例中，形成該源極層包含形成一源極層其包括矽化鎢、重度摻雜多晶矽、或多晶矽化鎢

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中之一或多者。於一個實施例中，形成該源極層包含形成一n型摻雜多晶矽。於一個實施例中，形成該AlOx層進一步包含：形成一浮動閘極用以由該閘極選擇信號觸發以提供自該源極層至該多層記憶體胞元堆疊體的電流。於一個實施例中，形成延伸通過該多層堆疊體之一中空通道，該中空通道包括環繞一通道絕緣體的導電材料以提供電氣式接觸給該等記憶體胞元之閘極；其中該AlOx層浮動閘極提供自該源極層至該中空通道的電流。於一個實施例中，進一步包含在該AlOx層與該SGS poly層間形成一氧化物層。於一個實施例中，進一步包含在該AlOx層與該源極層間形成一氧化物層。

[0074]於一個面向中，一種包含具有內容儲存於其上之一電腦可讀取儲存媒體之製造物件，其當執行時從事操作用以形成具有一AlOx著陸層之堆疊電路，包括：產生一多層記憶體胞元堆疊體，該堆疊體之各層包括一記憶體胞元裝置；相鄰該多層記憶體胞元堆疊體形成一源閘選擇多晶矽(SGS poly)層，該SGS poly層用以給該多層堆疊體的該等記憶體胞元提供一閘極選擇信號；在一半導體基體上形成一導電源極層用以給該堆疊體的該等層提供用於一通道之一源極導體；及在該源極層與該SGS poly層間形成一氧化鋁(AlOx)層，該AlOx層提供一蝕刻停止層以分開該SGS poly層與該源極層，其中該AlOx層提供乾蝕刻選擇性及濕蝕刻選擇性兩者，其中一通道蝕刻蝕穿該多層記憶體胞元堆疊體及該SGS poly層，且停止於該AlOx層而不會暴露出

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該源極層，及其中一選擇性閘極蝕刻蝕刻該等記憶體胞元中之閘極接點及蝕刻該AlOx層而暴露出該源極層。

[0075]於一個實施例中，用於形成該SGS poly層之內容包含用於形成一p型摻雜多晶矽之內容。於一個實施例中，用於形成該源極層之內容包含用於形成一源極層之內容，該源極層包括矽化鎢、重度摻雜多晶矽、或多晶矽化鎢中之一或多者。於一個實施例中，用於形成該源極層之內容包含用於形成一n型摻雜多晶矽之內容。於一個實施例中，用於形成該AlOx層之內容進一步包含：用於形成一浮動閘極用以由該閘極選擇信號觸發以提供自該源極層至該多層記憶體胞元堆疊體的電流之內容。於一個實施例中，用於形成延伸通過該多層堆疊體之一中空通道之內容，該中空通道包括環繞一通道絕緣體的導電材料以提供電氣式接觸給該等記憶體胞元之閘極；其中該AlOx層浮動閘極提供自該源極層至該中空通道的電流。於一個實施例中，進一步包含用於在該AlOx層與該SGS poly層間形成一氧化物層之內容。於一個實施例中，進一步包含用於在該AlOx層與該源極層間形成一氧化物層之內容。

[0076]於一個面向中，一種用於形成具有一AlOx著陸層之堆疊電路之設備包括：用於產生一多層記憶體胞元堆疊體之構件，該堆疊體之各層包括一記憶體胞元裝置；用於相鄰該多層記憶體胞元堆疊體形成一源閘選擇多晶矽(SGS poly)層之構件，該SGS poly層用以給該多層堆疊體的該等記憶體胞元提供一閘極選擇信號；用於在一半導體基

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體上形成一導電源極層用以給該堆疊體的該等層提供用於一通道之一源極導體之構件；及用於在該源極層與該SGS poly層間形成一氧化鋁(AlOx)層之構件，該AlOx層提供一蝕刻停止層以分開該SGS poly層與該源極層，其中該AlOx層提供乾蝕刻選擇性及濕蝕刻選擇性兩者，其中一通道蝕刻蝕穿該多層記憶體胞元堆疊體及該SGS poly層，且停止於該AlOx層而不會暴露出該源極層，及其中一選擇性閘極蝕刻蝕刻該等記憶體胞元中之閘極接點及蝕刻該AlOx層而暴露出該源極層。

[0077]於一個實施例中，用於形成該SGS poly層之構件包含用於形成一p型摻雜多晶矽之構件。於一個實施例中，用於形成該源極層之構件包含用於形成一源極層之構件，該源極層包括矽化鎢、重度摻雜多晶矽、或多晶矽化鎢中之一或多者。於一個實施例中，用於形成該源極層之構件包含用於形成一n型摻雜多晶矽之構件。於一個實施例中，用於形成該AlOx層之構件進一步包含：用於形成一浮動閘極用以由該閘極選擇信號觸發以提供自該源極層至該多層記憶體胞元堆疊體的電流之構件。於一個實施例中，用於形成延伸通過該多層堆疊體之一中空通道之構件，該中空通道包括環繞一通道絕緣體的導電材料以提供電氣式接觸給該等記憶體胞元之閘極；其中該AlOx層浮動閘極提供自該源極層至該中空通道的電流。於一個實施例中，進一步包含用於在該AlOx層與該SGS poly層間形成一氧化物層之構件。於一個實施例中，進一步包含用於在該AlOx層與該

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源極層間形成一氧化物層之構件。

[0078]此處例示之流程圖提供各種方法動作之順序。流程圖可指示藉軟體或韌體常式執行的操作，以及實體操作。於一個實施例中，流程圖可例示有限狀態機(FSM)的狀態，該FSM可於硬體及/或軟體體現。雖然係以特定序列或順序顯示，但除非另行載明否則動作順序可經修改。如此，須瞭解例示實施例僅作爲一例，及該處理可以不同順序進行，及有些動作可並列執行。此外，於各種實施例中可刪除一或多個動作，並非每個實施例皆要求全部動作。其它處理流程亦屬可能。

[0079]至此處描述的各種操作或功能之程度，其可被描述或界定爲軟體碼、指令、組態、及/或資料。內容可直接執行(「目的」形式或「可執行」形式)、來源碼、或不同碼(δ碼或補片碼)。此處描述的實施例之軟體內容可透過有該內容儲存其上之一製造物件提供，或透過操作一通訊介面以透過該通訊介面發送資料之一方法提供。機器可讀取儲存媒體可使得機器執行所描述的功能或操作，且包括以機器(例如，計算裝置、電子系統等)可存取形式儲存資訊的任何機制，諸如可錄式/非可錄式媒體(例如，唯讀記憶體(ROM)、隨機存取記憶體(RAM)、磁碟儲存媒體、光學儲存媒體、快閃記憶體裝置等)。一通訊介面包括介接有線、無線、光學等中之任一者的任何機制，用以通訊至另一裝置的媒體，諸如記憶體匯流排介面、處理器匯流排介面、網際網路連結、碟片控制器等。通訊介面可藉提供組態參

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數及/或發送信號組配以準備該通訊介面提供描述該軟體內容之一資料信號。通訊介面可透過發送給該通訊介面的一或多個指令或信號而被存取。

[0080]此處描述之各種組件可以是用以執行所描述的操作或功能之構件。此處描述之各個組件包括軟體、硬體、或此等組合。該等組件可體現爲軟體模組、硬體模組、特用硬體(例如，特定應用硬體、特定應用積體電路(ASIC)、數位信號處理器(DSP)等)、嵌入式控制器、有線電路等。

[0081]除了此處描述者之外，不背離本發明之範圍可對本發明之揭示實施例及體現做出各種修改。因此，此處之例示及實例須被解譯爲例示性而非限制性意義。本發明之範圍須僅參考後文申請專利範圍度量。

【符號說明】

100、500...系統

102、104...層疊

110...基體

120、220、312、314...源極導體、源極

122、126、280、380...通道

124...導體

130-A~B、170-A~B、230、330...ALOX、氧化鋁層

140-A~B、240、340...SGS poly

150-A~B、180-A~B...電路元件

160-A~B...絕緣體

202、204、206、208、210、212...電路狀態

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232、320、350…氧化物、氧化物層

250…層堆疊體

252…層

260…柱體

262…殘餘物

270、396…浮動閘極

272…虛設浮動閘極、虛設閘極

360…字線(WL)多晶矽

370…絕緣層

390…元件

392…通道導體

394…電介質

400…處理

402-422…處理方塊

510…匯流排/匯流排系統

520…處理器

530…記憶體子系統、記憶體

532…記憶體裝置

534…記憶體控制器

536…作業系統(OS)

538…指令

540…輸入/輸出(I/O)介面

550…網路介面

560…儲存裝置

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562…資料

570…周邊介面

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發明摘要

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【發明名稱】(中文/英文)

用於三維電路裝置之供導電通道用的氧化鋁著陸層
ALUMINUM OXIDE LANDING LAYER FOR CONDUCTIVE CHANNELS FOR A THREE DIMENSIONAL CIRCUIT DEVICE

【中文】

一多層記憶體胞元堆疊體具有氧化鋁(AlOx)層作爲貴HiK層以提供蝕刻停止選擇性。該堆疊體的各層包括一記憶體胞元裝置。該電路包括相鄰該多層記憶體胞元堆疊體的一源閘選擇多晶矽(SGS poly)層，其中該SGS poly層係用以給該多層堆疊體的該等記憶體胞元提供一閘極選擇信號。該電路也包括一導電源極層以給該堆疊體的該等層提供用於一通道之一源極導體。該AlOx層係位在該源極層與該SGS poly層間，且提供乾蝕刻選擇性及濕蝕刻選擇性兩者用以形成一通道而電氣耦合該等記憶體胞元至該源極層。

【英文】

A multitier stack of memory cells having an aluminum oxide (AlOx) layer as a noble HiK layer to provide etch stop selectivity. Each tier of the stack includes a memory cell device. The circuit includes a source gate select polycrystalline (SGS poly) layer adjacent the multitier stack of memory cells, wherein the SGS poly layer is to provide a gate select signal for the memory cells of the multitier stack. The circuit also includes a conductive source layer to provide a source conductor for a channel for the tiers of the stack. The AlOx layer is disposed between the source layer and the SGS poly layer and provides both dry etch selectivity and wet etch selectivity for creating a channel to electrically couple the memory cells to the source layer.

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【代表圖】

【本案指定代表圖】：第（ 1 ）圖。

【本代表圖之符號簡單說明】：

100...系統
102、104...層疊
110...基體
120...源極、源極導體
122、126...通道
124...導體
130-A~B、170-A~B...ALOX、氧化鋁層
140-A~B...SGS POLY層
150-A~B、180-A~B...電路元件
160-A~B...絕緣體

【本案若有化學式時，請揭示最能顯示發明特徵的化學式】：

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申請專利範圍

1. 一種電路裝置，其包含：

一多層記憶體胞元堆疊體，該堆疊體之各層包括有一記憶體胞元裝置；

一源閘選擇多晶矽(SGS poly)層，其與該多層記憶體胞元堆疊體相鄰，該SGS poly層係用於針對該多層堆疊體之該等記憶體胞元提供一閘極選擇信號；

一導電源極層，用以針對用於該堆疊體之該等層的一通道提供一源極導體；以及

一氧化鋁(AlOx)層，其介在該源極層與該SGS poly層之間，該AlOx層提供用於使該SGS poly層與該源極層分開的一蝕刻停止層，其中，該AlOx層提供乾蝕刻選擇性也提供濕蝕刻選擇性，其中，一通道蝕刻處理蝕穿該多層記憶體胞元堆疊體及該SGS poly層並止於該AlOx層而不暴露出該源極層，並且其中，一選擇性閘極蝕刻處理蝕刻該等記憶體胞元中之閘極接點並蝕刻該AlOx層而暴露出該源極層。

2. 如請求項1之電路裝置，其中，該SGS poly層包含一p型摻雜多晶矽。

3. 如請求項1之電路裝置，其中，該源極層包括下列中之一或多者：矽化鎢、重度摻雜多晶矽、或多晶矽化鎢。

4. 如請求項1之電路裝置，其中，該源極層包含一n型摻雜多晶矽。

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5. 如請求項1之電路裝置，其中，該AlOx層進一步包含：

由該閘極選擇信號觸發的一浮動閘極，用以提供從該源極層至該多層記憶體胞元堆疊體的電流。

6. 如請求項5之電路裝置，其中，該通道包含延伸通過該多層堆疊體的一中空通道，該中空通道包括環繞一通道絕緣體的導電材料，用以提供至該等記憶體胞元之閘極的電氣式接觸；

其中，該AlOx層浮動閘極提供自該源極層至該中空通道的電流。

7. 如請求項1之電路裝置，其進一步包含：

在該AlOx層與該SGS poly層之間的一氧化物層。

8. 如請求項1之電路裝置，其進一步包含：

在該AlOx層與該源極層之間的一氧化物層。

9. 一種電子裝置，其包含：

用於儲存資料的一三維堆疊記憶體裝置，該記憶體裝置包括：

一多層記憶體胞元堆疊體，該堆疊體之各層包括一記憶體胞元裝置；

與該多層記憶體胞元堆疊體相鄰的一源閘選擇多晶矽(SGS poly)層，該SGS poly層係用於針對該多層堆疊體之該等記憶體胞元提供一閘極選擇信號；

一導電源極層，用以針對用於該堆疊體之該等層的一通道提供一源極導體；以及

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在該源極層與該SGS poly層之間的一氧化鋁(AlOx)層，該AlOx層提供用於使該SGS poly層與該源極層分開的一蝕刻停止層，其中，該AlOx層提供乾蝕刻選擇性也提供濕蝕刻選擇性，其中，一通道蝕刻處理蝕穿該多層記憶體胞元堆疊體及該SGS poly層並止於該AlOx層而不暴露出該源極層，並且其中，一選擇性閘極蝕刻處理蝕刻該等記憶體胞元中之閘極接點並蝕刻該AlOx層以暴露出該源極層；以及

一高畫質顯示器，其係耦接來基於儲存在該記憶體裝置中的資料而產生一顯示畫面。

10. 如請求項9之電子裝置，其中，該源極層包括下列中之一或多者：矽化鎢、重度摻雜多晶矽、或多晶矽化鎢。

11. 如請求項9之電子裝置，其中，該AlOx層進一步包含：

由該閘極選擇信號觸發的一浮動閘極，用以提供從該源極層至該多層記憶體胞元堆疊體的電流。

12. 如請求項11之電子裝置，其中，該通道包含延伸通過該多層堆疊體的一中空通道，該中空通道包括環繞一通道絕緣體的導電材料，用以提供至該等記憶體胞元之閘極的電氣式接觸；

其中，該AlOx層浮動閘極提供自該源極層至該中空通道的電流。

13. 如請求項9之電子裝置，其中，該記憶體裝置進一步包含：

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在該AlOx層與該SGS poly層之間的一氧化物層。

14. 如請求項9之電子裝置，其中，該記憶體裝置進一步包含：

在該AlOx層與該源極層之間的一氧化物層。

15. 一種方法，其包含下列步驟：

產生一多層記憶體胞元堆疊體，該堆疊體之各層包括一記憶體胞元裝置；

創造與該多層記憶體胞元堆疊體相鄰的一源閘選擇多晶矽(SGS poly)層，該SGS poly層係用於針對該多層堆疊體之該等記憶體胞元提供一閘極選擇信號；

創造在一半導體基體上的一導電源極層，用以針對用於該堆疊體之該等層的一通道提供一源極導體；及

創造在該源極層與該SGS poly層之間的一氧化鋁(AlOx)層，該AlOx層提供用於使該SGS poly層與該源極層分開的一蝕刻停止層，其中，該AlOx層提供乾蝕刻選擇性也提供濕蝕刻選擇性，其中，一通道蝕刻處理蝕穿該多層記憶體胞元堆疊體及該SGS poly層並止於該AlOx層而不暴露出該源極層，並且其中，一選擇性閘極蝕刻處理蝕刻該等記憶體胞元中之閘極接點並蝕刻該AlOx層以暴露出該源極層。

16. 如請求項15之方法，其中，創造該源極層之步驟包含：

創造一源極層，該源極層包括下列中之一或多者：矽化鎢、重度摻雜多晶矽、或多晶矽化鎢。

17. 如請求項15之方法，其中，創造該AlOx層之步驟進一步

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包含：

創造一浮動閘極，該浮動閘極可由該閘極選擇信號觸發以提供從該源極層至該多層記憶體胞元堆疊體的電流。

18. 如請求項17之方法，其進一步包含下列步驟：

形成延伸通過該多層堆疊體的一中空通道，該中空通道包括環繞一通道絕緣體的導電材料，用以提供至該等記憶體胞元之閘極的電氣式接觸；

其中，該AlOx層浮動閘極提供自該源極層至該中空通道的電流。

19. 如請求項15之方法，其進一步包含下列步驟：

創造在該AlOx層與該SGS poly層之間的一氧化物層。

20. 如請求項15之方法，其進一步包含下列步驟：

創造在該AlOx層與該源極層之間的一氧化物層。

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圖式

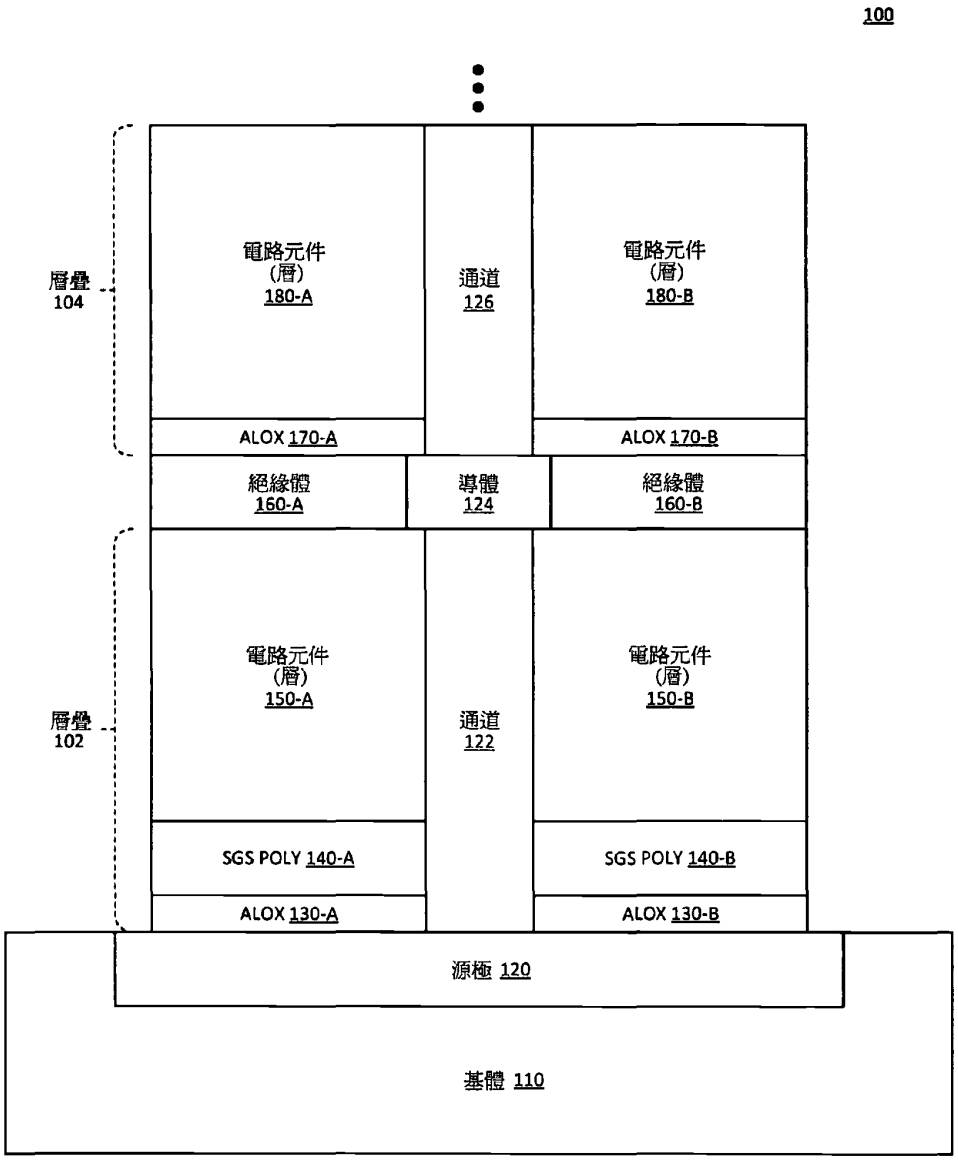
100
層疊
104
電路元件
(層)
180-A
通道
126
電路元件
(層)
180-B
ALOX 170-A
ALOX 170-B
絕緣體
160-A
導體
124
絕緣體
160-B
層疊
102
電路元件
(層)
150-A
通道
122
電路元件
(層)
150-B
SGS POLY 140-A
SGS POLY 140-B
ALOX 130-A
ALOX 130-B
源極 120
基體 110

圖1

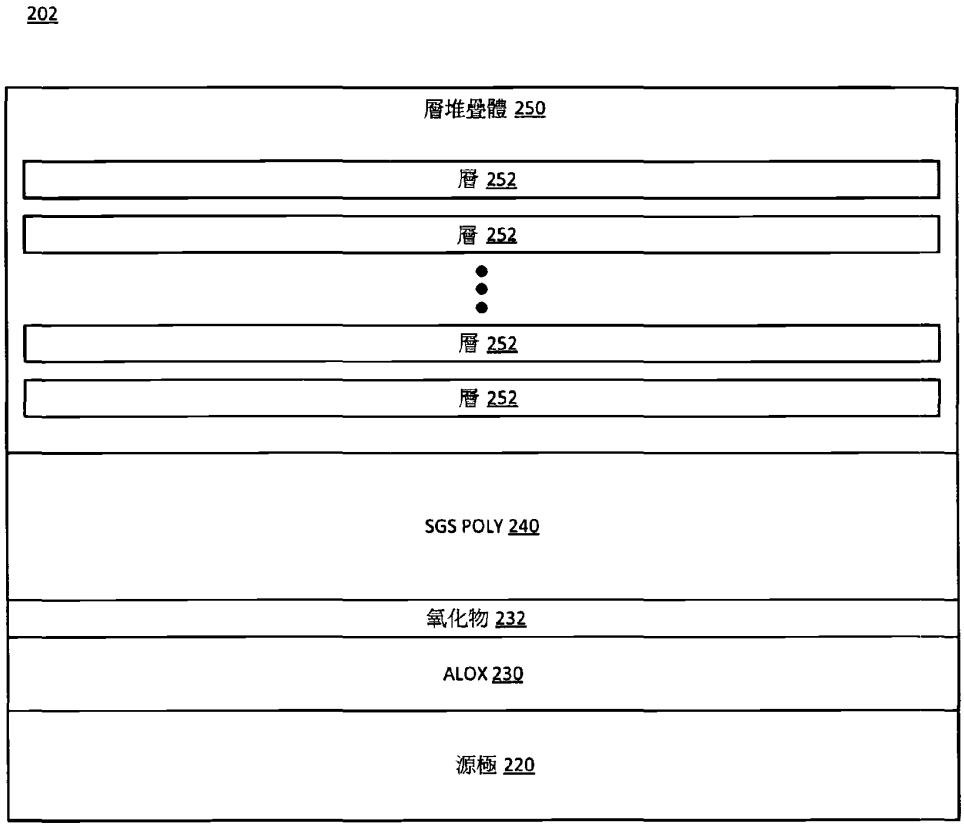
202
層堆疊體 250
層 252
層 252
層 252
層 252
SGS POLY 240
氧化物 232
ALOX 230
源極 220

圖2A

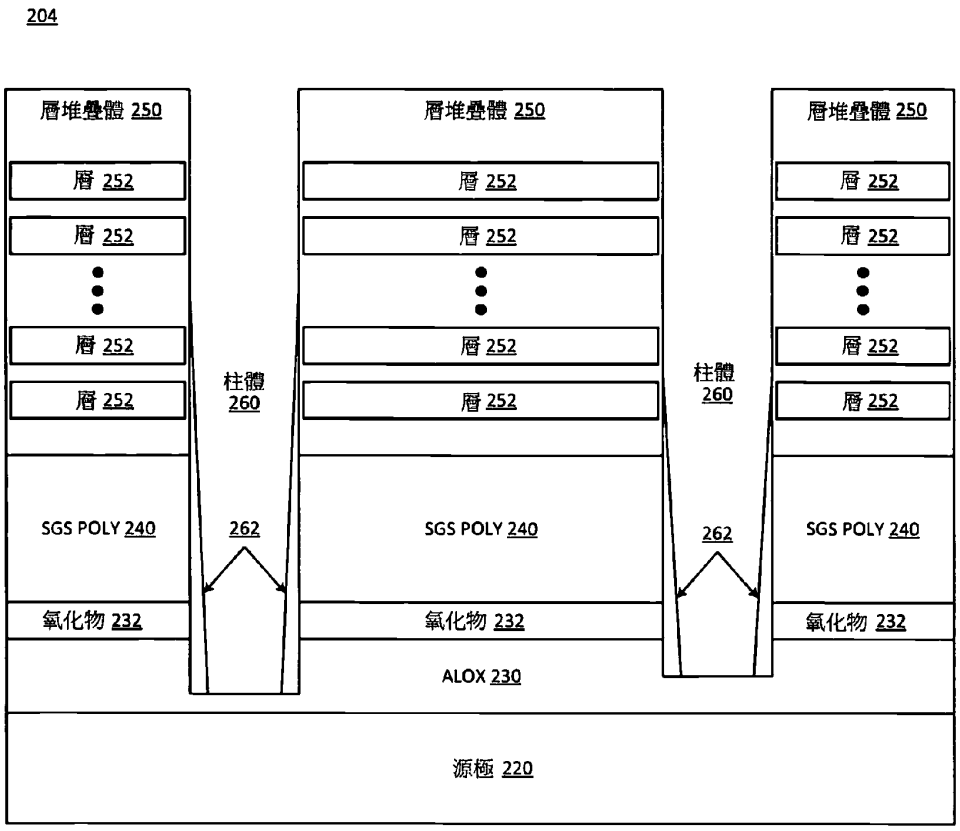

圖2B

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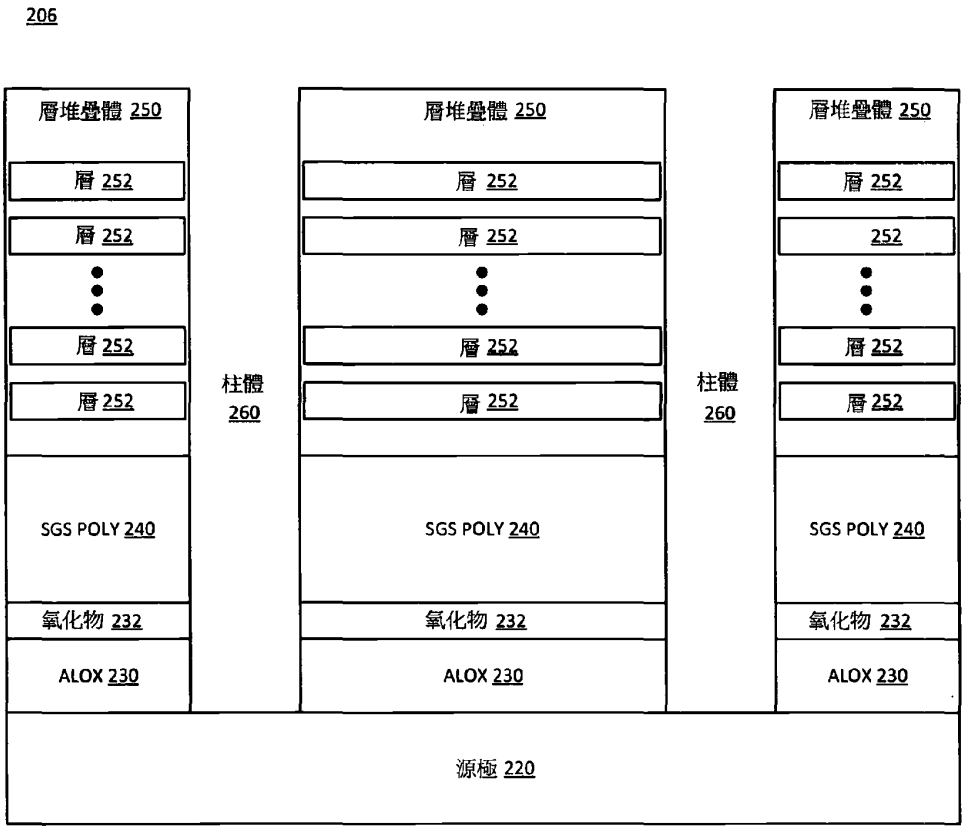
206
層堆疊體 250
層 252
層 252
層 252
層 252
柱體 260
層堆疊體 250
層 252
層 252
層 252
層 252
柱體 260
層堆疊體 250
層 252
252
層 252
層 252
SGS POLY 240
SGS POLY 240
SGS POLY 240
氧化物 232
氧化物 232
氧化物 232
ALOX 230
ALOX 230
ALOX 230
源極 220

圖2C

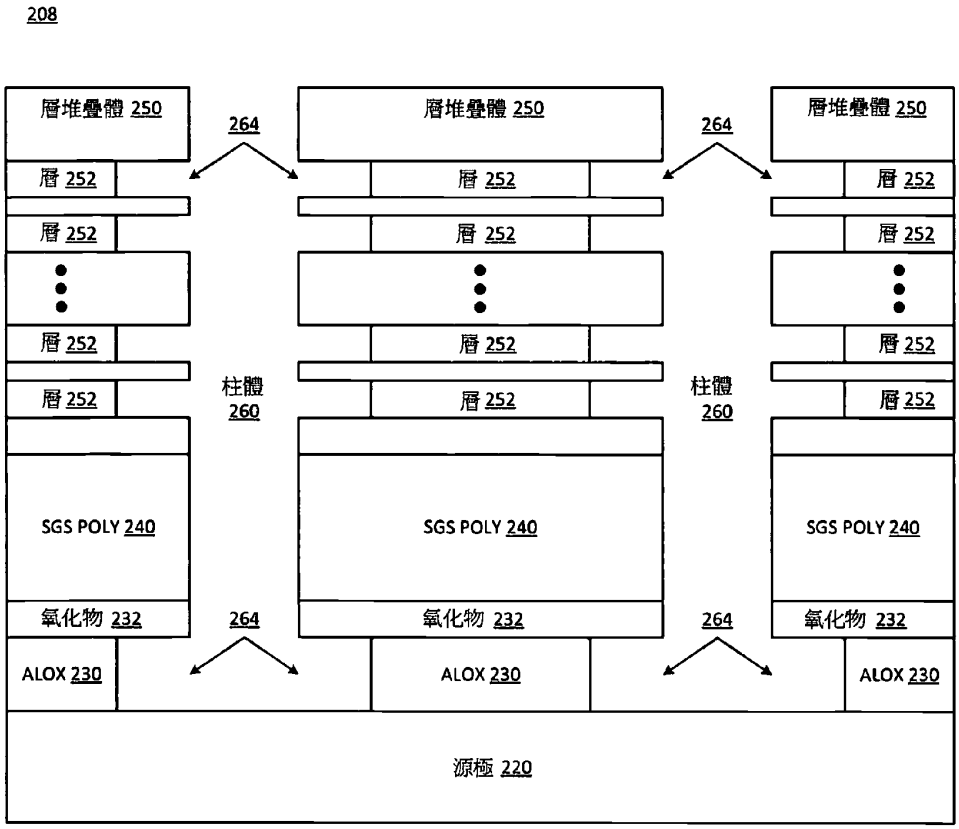

圖2D

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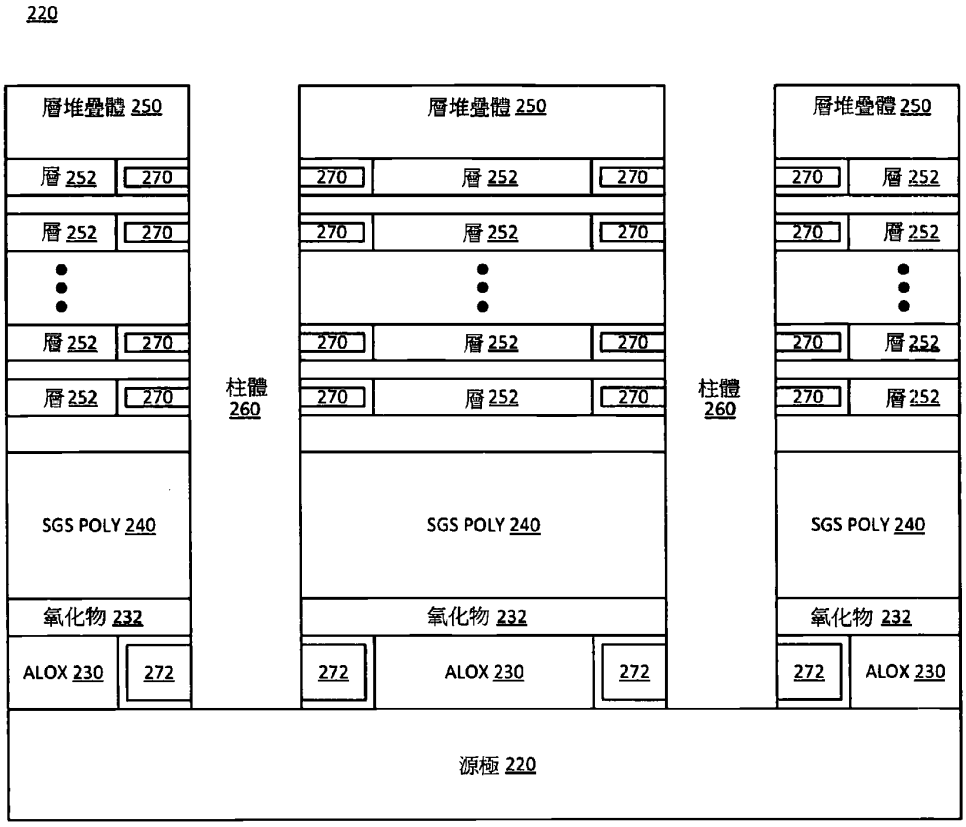
220
層堆疊體 250
層堆疊體 250
層堆疊體 250
層 252
270
層 252
270
層 252
270
層 252
270
層 252
270
層 252
270
層 252
270
層 252
270
層 252
270
層 252
270
層 252
270
層 252
270
層 252
270
層 252
270
層 252
柱體 260
柱體 260
SGS POLY 240
SGS POLY 240
SGS POLY 240
氧化物 232
氧化物 232
氧化物 232
ALOX 230
272
272
ALOX 230
272
272
ALOX 230
源極 220

圖2E

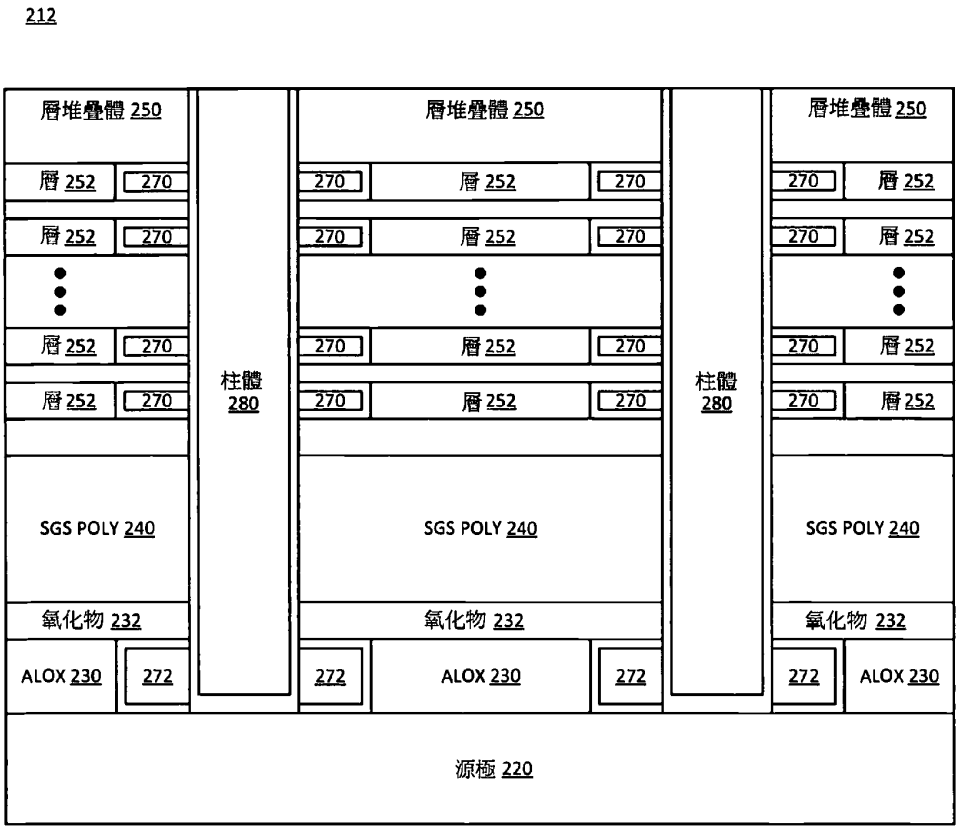

圖2F

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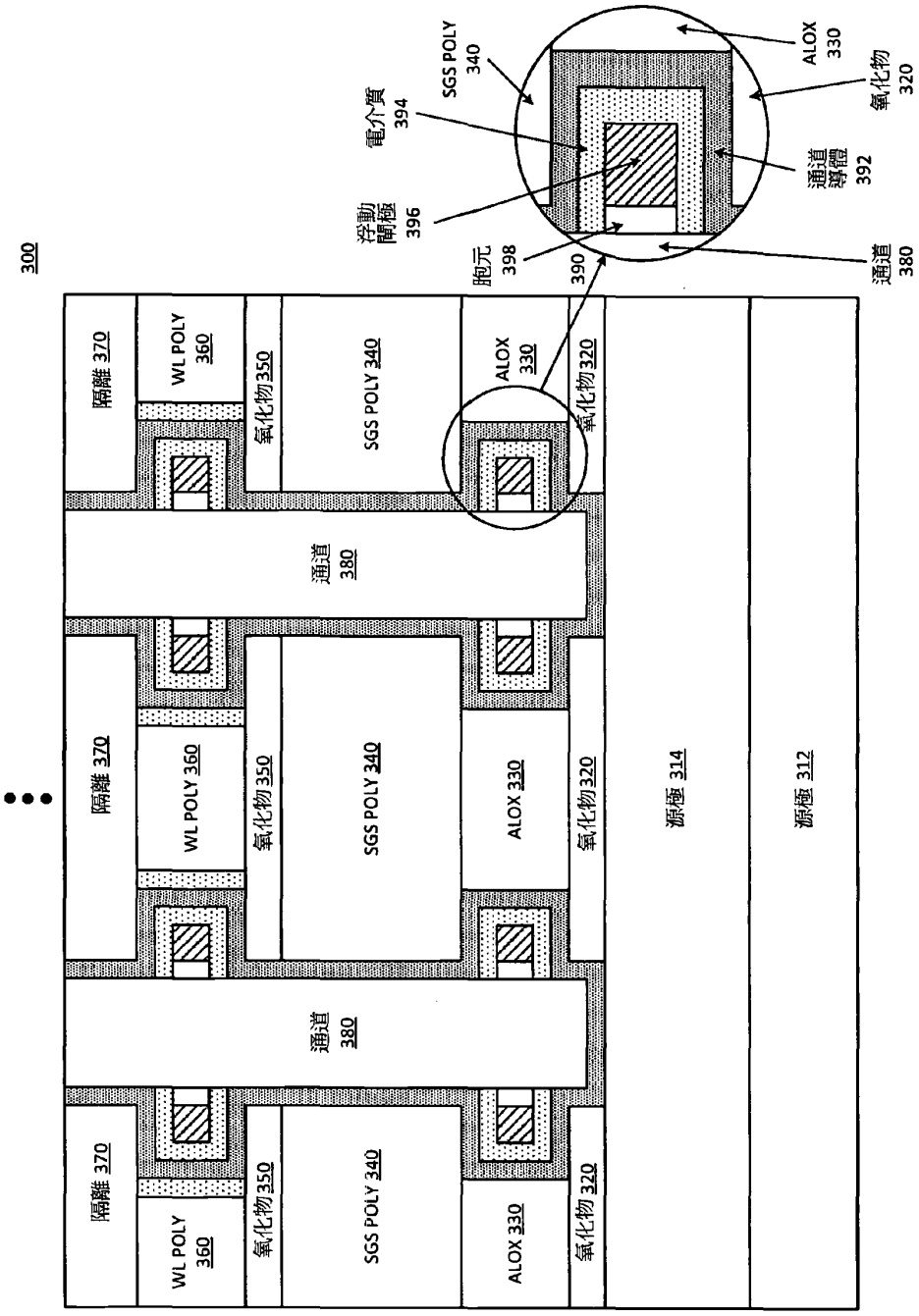
300
隔離 370
WL POLY 360
氧化物 350
SGS POLY 340
ALOX 330
氧化物 320
通道 380
源極 314
源極 312
浮動閘極 396
電介質 394
SGS POLY 340
ALOX 330
氧化物 320
通道導體 392
胞元 398
390
通道 380

圖3

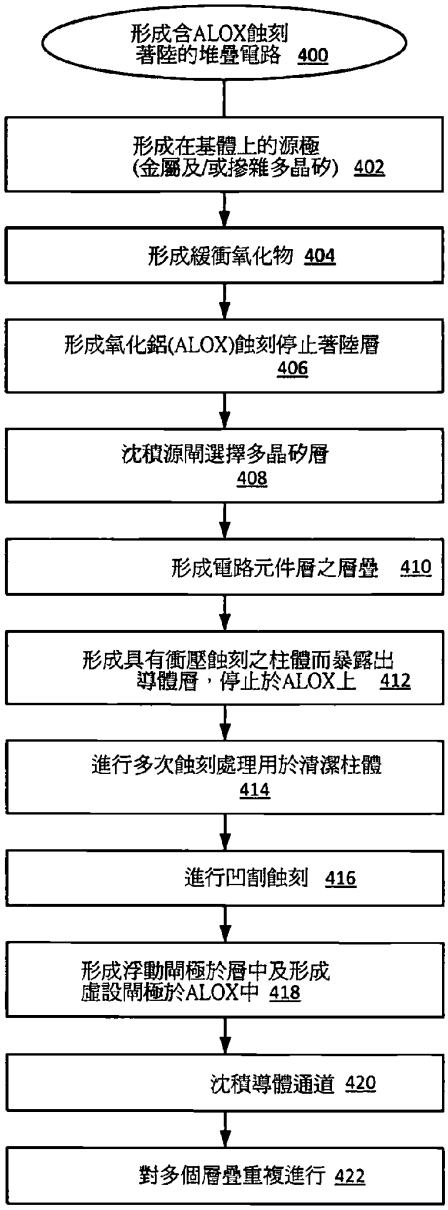

圖4

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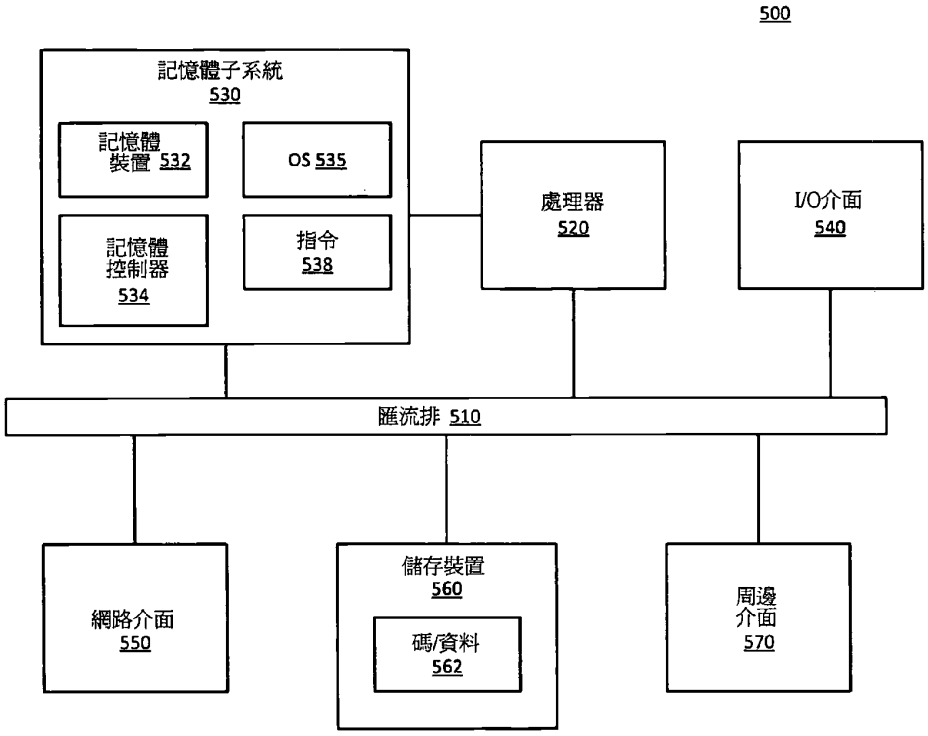
500
記憶體子系統
530
記憶體
裝置 532
OS 535
記憶體
控制器
534
指令
538
處理器
520
I/O介面
540
匯流排 510
網路介面
550
儲存裝置
560
碼/資料
562
周邊
介面
570

圖5

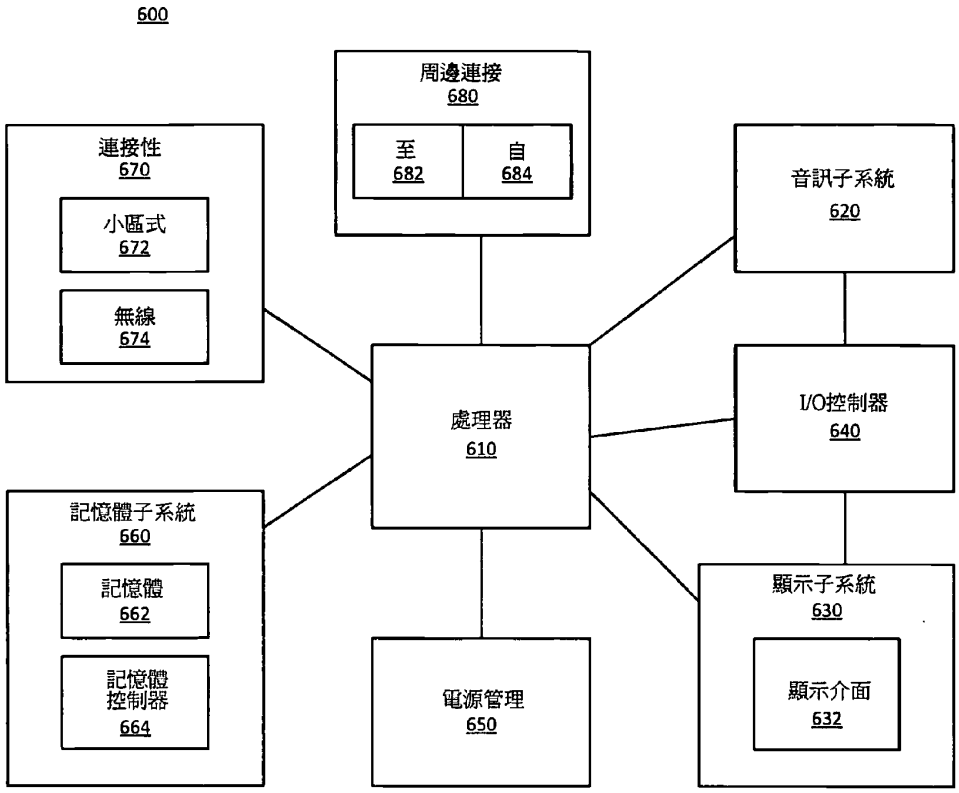

圖6

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201721921

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(12)發明說明書公開本 (11)公開編號：TW 201721921 A

(43)公開日： 中華民國 106 (2017) 年 06 月 16 日

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(71)申請人：旺宏電子股份有限公司 (中華民國) MACRONIX INTERNATIONAL CO., LTD. (TW)

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(74)代理人：祁明輝；林素華

申請實體審查：有 申請專利範圍項數：10 項 圖式數：6 共 37 頁

(54)名稱

三維記憶體元件

THREE DIMENSIONAL MEMORY DEVICE

(57)摘要

一種三維記憶體元件，包括多層堆疊結構多層堆疊結構包括複數個導電條帶及複數條溝槽，以定義出第一、第二、第三和第四脊狀堆疊；位於第一脊狀堆疊上的第一串列選擇線開關；位於第二脊狀堆疊上的第一接地選擇線開關；第一 U 形記憶胞串列，串接第一串列選擇線開關和第一接地選擇線開關；位於第三脊狀堆疊上的第二串列選擇線開關；位於第四脊狀堆疊上的第二接地選擇線開關；第二 U 形記憶胞串列，串接第二串列選擇線開關和第二接地選擇線開關。第一字元線接觸結構與第一脊狀堆疊的導電條帶接觸。第二字元線接觸結構與第二脊狀堆疊的導電條帶接觸；第三字元線接觸結構與第三和第四脊狀堆疊的導電條帶接觸。

A 3D memory device includes a multi-layer stacks structure having a plurality of conductive strips and a first, a second, a third and a fourth ridge stack; a first SSL switch, a first GSL switch, a second SSL switch and a second GSL switch respectively disposed on the first, the second the third and the fourth ridge stack; a first U-shaped memory cells string connecting the first SSL switch with the first GSL switch; a second U-shaped memory cells string connecting the second SSL switch with the second GSL switch; a first word lines contact in contact with the conductive strips disposed in the first ridge stack; a second word lines contact in contact with the conductive strips disposed in the second ridge stack; and a third word lines contact in contact with the conductive strips disposed in the third ridge stack and the fourth ridge stack.

指定代表圖：

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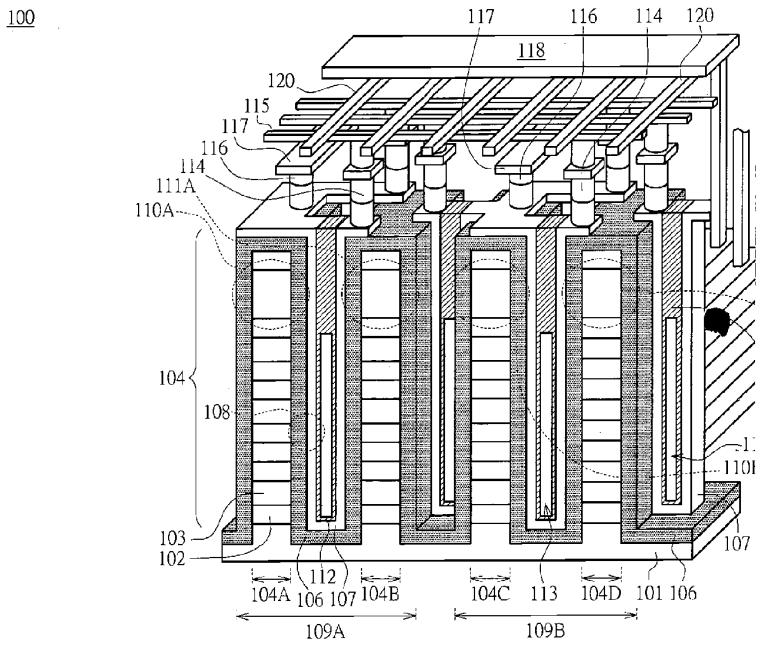

符號簡單說明：

100・・・記憶體元件

101・・・基材

102・・・導電層

103・・・絕緣層

104・・・多層堆疊結構

104A、104B、104C、104D・・・脊狀堆疊

106・・・記憶材料層

107・・・半導體通道層

108・・・記憶胞

109A、109B・・・U形記憶胞串列

110A、110B・・・接地選擇線開關

111A、111B・・・串列選擇開關

112・・・介電材質層

113・・・空氣間隙

114、116・・・接觸插塞

115・・・位元線

117・・・金屬導線

118・・・共同源極線

119B・・・字元線接觸結構

120・・・字元線

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【發明說明書】

【中文發明名稱】三維記憶體元件

【英文發明名稱】THREE DIMENSIONAL MEMORY DEVICE

【技術領域】

【0001】 本發明是有關於一種高密度記憶體元件。特別是一種三維(Three Dimemsional，3D)記憶體元件。

【先前技術】

【0002】 非揮發性記憶體元件，例如快閃記憶體，具有在移除電源時亦不丟失儲存於記憶單元中之資訊的特性。已廣泛運用於用於可攜式音樂播放器、移動電話、數位相機等的固態大容量存儲應用。為了達到具有更高密度儲存容量的需求，目前已經有各種不同結構的三維記憶體元件，例如具有單閘極(single-gate)記憶胞、雙閘極(double gate)記憶胞，和環繞式閘極(surrounding gate)記憶胞的三維快閃記憶體元件，被提出。

【0003】 典型的三維非揮發性記憶體元件包含複數個建構於多層堆疊結構(multi-layer stacks)之中具有垂直通道的記憶胞立體陣列。以具有 U 形記憶胞串列結構的單閘極垂直通道(Single-Gate Vertical Channel，SGVC) NAND 記憶體元件為例，一般係採用多晶矽材質的堆疊導電條帶來作為記憶胞的閘極。由於多晶矽的阻值較大，因此在建構記憶胞陣列時，需要將導電條

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帶跟隔成多個區段，並過階梯狀的字元線接觸結構字元線接觸結構，將位於同一階層的導電條與位於記憶胞陣列上方的金屬字元線電性連接。

【0004】 由於，字元線接觸結構佔據記憶體元件相當大的面積，加上記憶胞陣列上方容納金屬字元線的佈線空間有限。隨著記憶體元件記憶容量的擴充，使得多層堆疊層結構中導電條帶階層的數量相對增加，需要設置更多字元線和字元線接觸結構。目前只能藉由縮小字元線的線徑和間距(pitch)，或者增加記憶區塊的面積尺寸，來加以因應。

【0005】 然而，縮小字元線的線徑和間距會導致製程裕度(process window)減少、良率降低而大幅增加製程成本，甚至因導致氧化層擊穿(oxide breakdown)現象產生。增加記憶區塊的面積尺寸並不符合目前元件微縮的趨勢。

【0006】 因此，有需要提供一種先進的記憶體元件，以解決上述襲之技術所面臨的問題。

【發明內容】

【0007】 本說明書的一實施例是提供一種三維記憶體元件。此三維記憶體元件包括：多層堆疊結構(multi-layer stacks)、第一串列選擇線(String Select Line，SSL)開關、第一接地選擇線(Ground Selection Line，GSL)開關、第二串列選擇線開關、第二接地選擇線開關、第一 U 形記憶胞串列、第二 U 形記憶胞串列、

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第一字元線接觸結構、第二字元線接觸結構以及第三字元線接觸結構。多層堆疊結構包括彼此隔離的複數個導電條帶以及複數條溝槽(trench)，用以至少定義出第一脊狀堆疊 (ridge stacks)、第二脊狀堆疊、第三脊狀堆疊以及第四脊狀堆疊。第一串列選擇線開關位於第一脊狀堆疊之上。第一接地選擇線開關位於第二脊狀堆疊之上。第一 U 形記憶胞串列串接第一串列選擇線開關和第一接地選擇線開關。第二串列選擇線開關位於第三脊狀堆疊之上。第二接地選擇線開關位於第四脊狀堆疊之上。第二 U 形記憶胞串列串接第二串列選擇線開關和第二接地選擇線開關。第一字元線接觸結構與位於第一脊狀堆疊上的導電條帶接觸。第二字元線接觸結構與位於第二脊狀堆疊上的導電條帶接觸；第三字元線接觸結構與位於第三脊狀堆疊和第四脊狀堆疊上的導電條帶接觸。

【0008】 根據上述實施例，本說明書是提供一種具有多個脊狀堆疊的三維記憶體元件，其中每一個脊狀堆疊包含，分別具有位於頂部的一個串列選擇線開關或一個接地選擇線開關以及位於該串列選擇線開關或該接地選擇線開關下方的複數個記憶胞。藉由串接位於兩個脊狀堆疊上的第一串列選擇線開關和第一接地選擇線開關，以及位於第一串列選擇線開關和第一接地選擇線開關下方的記憶胞來形成第一 U 形記憶胞串列；同時藉由串接位於另外兩個不同脊狀堆疊上的第二串列選擇線開關和第二接地選擇線開關，以及位於第二串列選擇線開關和第二接地選擇線開關下方的記憶胞來形成第二 U 形記憶胞串列。

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【0009】 其中，位於第一 U 形記憶胞串列之第一串列選擇線開關下方的記憶胞與第一字元線接觸結構連接；位於第二 U 形記憶胞串列之第二串列選擇線開關下方的記憶胞與第二字元線接觸結構連接；而位於第一 U 形記憶胞串列之第一接地選擇線開關下方的記憶胞以及位於第二 U 形記憶胞串列之第二接地選擇線開關下方的記憶胞，則連接至相同的第三字元線接觸結構。換句話說，三維記憶體元件中，用來連接位於接地選擇開關下方之記憶胞的字元線接觸結構數量小於用來連接位於串列選擇開關下方之記憶胞的字元線接觸結構。若與先前技術中的三維記憶體元件相比，在不改變記憶容量的前提下，可以減少字元線接觸結構的設置。

【0010】 藉由減少字元線接觸結構的設置，可以減少記憶體元件的面積尺寸；更可在不影響製程裕度的前提下，擴充記憶體元件的記憶容量，大幅降低製程成本，並防止氧化層擊穿現象產生，增加垂直通道記憶體元件的製程良率。

【圖式簡單說明】

【0011】 本發明的其他目的、特徵和優點可見於下述實施例和申請專利範圍，並配合所附圖式，作詳細說明如下:

第 1A 圖至 1D 圖係根據習知技術所繪示的一種單閘極垂直通道 NAND 記憶體元件的局部結構透視圖；

第 2 圖係根據第 1D 圖所繪示之單閘極垂直通道 NAND 記憶

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體元件的局部結構上視圖；

第 3 圖係根據本發明的另一實施例所繪示之單閘極垂直通道 NAND 記憶體元件的局部結構上視圖；

第 4 圖係繪示以第 1C 圖之單閘極垂直通道 NAND 記憶體元件進行寫入操作(program operation)時的等效電路圖；

第 5 圖係繪示以第 1C 圖之單閘極垂直通道 NAND 記憶體元件進行讀取操作(read operation)時的等效電路圖；以及

第 6 圖係繪示以第 1C 圖之單閘極垂直通道 NAND 記憶體元件進行抹除操作(erase operation)時的等效電路圖。

【實施方式】

【0012】 本發明是提供一種記憶體元件，可解決習知記憶體元件製程裕度不足的問題，並且同時節省製造成本提高製程良率。為讓本發明之上述和其他目的、特徵和優點能更明顯易懂，下文特舉數個較佳實施例，並配合所附圖式，作詳細說明如下。

【0013】 但必須注意的是，這些特定的實施案例，並非用以限定本發明。本發明仍可採用其他特徵、元件、方法及參數來加以實施。較佳實施例的提出，僅係用以例示本發明的技術特徵，並非用以限定本發明的申請專利範圍。該技術領域中具有通常知識者，將可根據以下說明書的描述，在不脫離本發明的精神範圍內，作均等的修飾與變化。在不同實施例與圖式之中，相同的元件，將以相同的元件符號加以表示。

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【0014】 請參照第 1A 圖至第 1C 圖，第 1A 圖至第 1C 圖係根據本發明的一實施例所繪示製作單閘極垂直通道 NAND 記憶體元件 100 的製程結構透視圖。製作單閘極垂直通道 NAND 記憶體元件 100 的方法，包括下述步驟：首先在基材 101 的表面上形成多層堆疊結構 104(如第 1A 圖所繪示)。在本實施例中，多層堆疊結構 104 包括沿著第 1A 圖所繪示的 Z 軸方向，在基材 101 上彼此交錯堆疊的複數個導電層 102 以及複數個絕緣層 103。

【0015】 本發明的一些實施例中，導電層 102 的材質，可以包含摻雜有磷或砷的 n 型多晶矽(或 n 型磊晶單晶矽)、摻雜有硼的 p 型多晶矽(或 p 型磊晶單晶矽)、無摻雜的的多晶矽、金屬矽化物(silicides)，例如矽化鈦(TiSi)、矽化鈷(CoSi)或矽鍺(SiGe)、氧化物半導體(oxide semiconductors)，例如氧化銦鋅(InZnO)或氧化銦鎵鋅(InGaZnO)、金屬，例如鋁(Al)、銅(Cu)、鎢(W)、鈦(Ti)、鈷(Co)、鎳(Ni)、氮化鈦(TiN)、氮化鉭(TaN)或氮化鉭鋁(TaAlN)，或兩種或多種上述材質之組合物所構成。絕緣層 103 可以由介電材料，例如矽氧化物(oxide)、矽氮化物(nitride)、矽氮氧化物(oxynitride)、矽酸鹽(silicate)或其他材料，所構成。

【0016】 接著，對多層堆疊結構 104 進行一圖案化製程，以形成複數個脊狀堆疊 104A、104B、104C 和 104D。在本發明的一些實施例中，係採用非等向蝕刻製程(anisotropic etching process)，例如反應離子蝕刻(Reactive Ion Etching，RIE)製程，對多層堆疊結構 104 進行蝕刻。藉以在多層堆疊結構 104 之中形成

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沿著 X 橫向延伸且沿 Z 軸縱向延伸的溝槽 105，將多層堆疊結構 104 分割成複數個脊狀堆疊 104A、104B、104C 和 104D，並將基材 101 的部分區域經由溝槽 105 曝露於外(如第 1B 圖所繪示)。

【0017】 每一個脊狀堆疊 104A、104B、104C 和 104D 都包含複數個條狀的導電條帶。例如在本實施例中，脊狀堆疊 104A 具有沿著 Z 軸方向向上堆疊的導電條帶 104A1、104A2、104A3、104A4、104A5 和 104A6；脊狀堆疊 104B 具有沿著 Z 軸方向向上堆疊的導電條帶 104B1、104B2、104B3、104B4、104B5 和 104B6；脊狀堆疊 104C 具有沿著 Z 軸方向向上堆疊的導電條帶 104C1、104C2、104B3、104C4、104C5 和 104C6；以及脊狀堆疊 104D 具有沿著 Z 軸方向向上堆疊的導電條帶 104D1、104D2、104D3、104D4、104D5 和 104D6。其中，位於脊狀堆疊 104A、104B、104C 和 104D 之頂部平面的導電條帶 104A6、104B6、104C6 和 104D6 具有比位於相同脊狀堆疊 104A、104B、104C 和 104D 的其他平面之導電條帶 104A1-104A5、104B1-104B5、104C1-104C5 和 104D1-104D5 還大的厚度。

【0018】 之後，於脊狀堆疊 104A、104B、104C 和 104D 的側壁上方以及溝槽 105 底部形成具有電荷捕捉結構(charge trapping structure)，的記憶材料層 106。並於記憶材料層 106 上形成圖案化的半導體通道層 107。進而在脊狀堆疊 104A、104B、104C 和 104D 的導電條帶 104A1-A6、104B1-B6、104C1-C6 和 104D1-D6 與記憶材料層 106 和通道層 107 三者重疊的位置(cross point)，分

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別定義出複數個記憶胞 108(如第 1C 圖所繪示)。

【0019】 在本發明的一些實施例中，記憶材料層 106 的電荷捕捉結構可以是一種複合多疊層，其係選自於由矽氧化物-氮化矽-矽氧化物(oxide-nitride-oxide、ONO)結構、一矽氧化物-氮化矽-矽氧化物-氮化矽-矽氧化物(oxide-nitride-oxide-nitride-oxide，ONONO)結構、一矽-矽氧化物-氮化矽-矽氧化物-矽(silicon-oxide-nitride-oxide-silicon，SONOS)結構、一能隙工程矽-矽氧化物-氮化矽-矽氧化物-矽(bandgap engineered silicon-oxide-nitride-oxide-silicon，BE-SONOS)結構、一氮化鉭-氧化鋁-氮化矽-矽氧化物-矽(tantalum nitride, aluminum oxide, silicon nitride, silicon oxide, silicon，TANOS)結構以及一金屬高介電係數能隙工程矽-矽氧化物-氮化矽-矽氧化物-矽(metal-high-k bandgap-engineered silicon-oxide-nitride-oxide-silicon，MA BE-SONOS)結構所組成之一族群。半導體通道層 107 可以由摻雜有磷或砷的 n 型多晶矽，或 n 型磊晶單晶矽所構成。此外，半導體通道層 107 也可以由摻雜有硼的 p 型多晶矽，或 p 型磊晶單晶矽所構成。

【0020】 在本實施例中，圖案化的半導體通道層 107 係由 n 型多晶矽所構成，且圖案化的半導體通道層 107 至少包括彼此分離的兩個部分。其中一部分的半導體通道層 107 覆蓋在相鄰之脊狀堆疊 104A 和 104B 以及用來隔離脊狀堆疊 104A 和 104B 之溝槽 105 的底部。藉以分別在脊狀堆疊 104A 和 104B 之間形成一個

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U 形通道薄膜，用來串接形成於脊狀堆疊 104A 和 104B 上的複數個記憶胞 108，進而形成第一 U 形記憶胞串列 109A。另一部分的半導體通道層 107 覆蓋在相鄰之脊狀堆疊 104C 和 104C 以及用來隔離脊狀堆疊 104C 和 104D 之溝槽 105 的底部。並且在脊狀堆疊 104C 和 104D 之間形成另一個 U 形通道薄膜，用來串接形成於脊狀堆疊 104C 和 104D 上的複數個記憶胞 108，進而形成第二 U 形記憶胞串列 109B。

【0021】 其中，位於脊狀堆疊 104A 之頂部的記憶胞，可以作為第一 U 形記憶胞串列 109A 的第一接地選擇線開關 110A；位於脊狀堆疊 104B 之頂部的記憶胞，可以作為第一 U 形記憶胞串列 109A 的第一串列選擇開關 111A。位於脊狀堆疊 104C 之頂部的記憶胞，可以作為第二 U 形記憶胞串列 109B 的第二接地選擇線開關 110B；位於脊狀堆疊 104D 之頂部的記憶胞，可以作為第二 U 形記憶胞串列 109B 的第二串列選擇開關 111B。

【0022】 另外值得注意的是，雖然第 1C 圖僅繪示由四個脊狀堆疊(脊狀堆疊 104A、104B、104C 和 104D)所形成的二條 U 形記憶胞串列(第一 U 形記憶胞串列 109A 和第二 U 形記憶胞串列 109B)。但其僅係為了清楚描述起見而繪示，並非用以限定本發明。在本發明的一些實施例之中，單閘極垂直通道 NAND 記憶體元件 100 可以包括更多的脊狀堆疊以及更多的 U 形記憶胞串列，進而形成一個立體記憶胞陣列。

【0023】 之後，在溝槽 105 中填充介電材質層 112。在本發

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明的一些實施例中，形成介電材質層 112 的材質可以包含二氧化矽、氮化矽、氮氧化矽、高介電係數(high-k)材料或上述材料的任意組合。在本實施例中，較佳還包含在溝槽 105 中形成空氣間隙(air gap)113，用來降低位於不同脊狀堆疊 104A、104B、104C 和 104D 側壁上記憶胞 108 相互之間的干擾。

【0024】 後續如第 1D 圖所繪示，在脊狀堆疊 104A、104B、104C 和 104D 頂部形成接觸插塞(contact plug)114，分別使第一串列選擇線開關 111A 和第二串列選擇線開關 111B 連接至一條位元線 115；並形成接觸插塞 116 使第一接地選擇線開關 110A 和第二接地選擇線開關 110B 分別通過金屬導線 117 連接至一共同源極線 118。並在立體記憶胞陣列的周邊區形成階梯狀的複數個字元線接觸結構(例如，第 1D 圖所繪示的 119B)，使位於脊狀堆疊 104A、104B、104C 和 104D 之相同階層中用來形成層記憶胞 108 的導電條帶 104A1-D1、104A2-D2、104A3-D3、104A4-D4、104A5-D5 和 104A6-D6，分別連接至不同的字元線 120。

【0025】 字元線接觸結構，例如字元線接觸結構 119A、119B 和 119C，的詳細配置請參照第 2 圖，第 2 圖係根據第 1D 所繪示單閘極垂直通道 NAND 記憶體元件 100 的局部結構上視圖。字元線接觸結構 119A、119B 和 119C 係分別配置在脊狀堆疊 104A、104B、104C 和 104D 的長軸兩側。在本實施例中，字元線接觸結構 119A 包含階梯狀堆疊的多個接觸層，分別用來與位於脊狀堆疊 104B 中不同階層的導電條帶接觸；字元線接觸結構 119B 包含

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階梯狀堆疊的多個接觸層，分別用來與位於脊狀堆疊 104D 中不同階層的導電條帶接觸。字元線接觸結構 119C 包含階梯狀堆疊的多個接觸層，分別用來與脊狀堆疊 104A 和 104C 中位於相同階層的導電條帶接觸。

【0026】 換句話說，脊狀堆疊 104A 和 104C 中位於相同平面層的導電條帶，共用一個字元線接觸結構 119C。詳言之，脊狀堆疊 104A 和 104C 中位於第一平面層的導電條帶 104A1 和 104C1，與階梯狀字元線接觸結構 119C 的第一接觸層(未繪示)接觸；位於第二平面層的導電條帶 104A2 和 104C2，與階梯狀字元線接觸結構 119C 得第二接觸層(未繪示)接觸；位於第三平面層的導電條帶 104A3 和 104C3，與階梯狀字元線接觸結構 119C 的第三接觸層(未繪示)接觸；位於第四平面層的導電條帶 104A4 和 104C4，與階梯狀字元線接觸結構 119C 的第四接觸(未繪示)層接觸；位於第五平面層的導電條帶 104A5 和 104C5，與階梯狀字元線接觸結構 119C 的第五接觸層(未繪示)接觸；以及位於第六平面層的導電條帶 104A6 和 104C6，與階梯狀字元線接觸結構 119C 的第六接觸層(未繪示)接觸。由於字元線接觸結構已為習知，故其詳細的構造與製作方法不在此贅述。

【0027】 但字元線接觸結構的配置方式並不以此為限，在本發明的一些實施例中，位於多於兩個以上不同 U 形記憶胞串列中之串列選擇線開關下方的導電條帶，會分別與不同的字元線接觸結構；位於此多於兩個以上不同 U 形記憶胞串列中之接地選擇線

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開關下方的導電條帶會共用一個字元線接觸結構。

【0028】 在本發明的一些實施例之中，單閘極垂直通道NAND記憶體元件100還包括複數個串列選擇線接觸墊121和一個共用的接地選擇線接觸墊122分別用來將串列選擇線開關(例如，第一串列選擇線開關111A和第二串列選擇線開關111B)和接地選擇開關(例如，第一接地選擇線開關110A和第二接地選擇線開關110B)連接至解碼器(未繪示)。例如在本實施例中，每一個串列選擇線接觸墊121分別位於具有第一串列選擇線開關111A和第二串列選擇線開關111B之脊狀堆疊104B和104D的一端，鄰接字元線接觸結構119A和119B，並且與用來形成第一串列選擇線開關111A和第二串列選擇線開關111B的導電條帶104B6和104D6接觸。共用的接地選擇線接觸墊122則位於具有第一接地選擇線開關110A和第二接地選擇線開關110B之脊狀堆疊104A和104C的一端，鄰接字元線接觸結構119C，並且與用來形成第一接地選擇線開關110A和第二接地選擇線開關110B的導電條帶104A6和104C6接觸。

【0029】 被共用的字元線接觸結構119C的形狀可以隨著單閘極垂直通道NAND記憶體元件的設計而有所不同。例如請參照第3圖，第3圖係根據本發明的另一實施例所繪示之單閘極垂直通道NAND記憶體元件300的局部結構上視圖。單閘極垂直通道NAND記憶體元件300的結構大致與單閘極垂直通道NAND記憶體元件100相同，差別僅在於，鄰接接地選擇線接觸墊122的字

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元線接觸結構 319C 的形狀不同。在本實施例之中，被位於脊狀堆疊 104A 和 104C 之第一接地選擇線開關 110A 和第二接地選擇線開關 110B 下方的導電條帶 104A6 和 104C6 所共用的字元線接觸結構 319C，可以配置成縱向階梯結構。進一步節省單閘極垂直通道 NAND 記憶體元件 300 的橫向寬度。

【0030】 為了防止具有共用字元線接觸結構 119C 之不同 U 形記憶胞串列 109A 和 109B 在寫入操作、讀取操作和抹除操作中產生訊號干擾，在本發明的一些實施例之中，單閘極垂直通道 NAND 記憶體元件 100 可以包括一個位於 U 形記憶胞串列 109A 之第一串列選擇線開關 111A 和第一接地選擇線開關 110A 之間的第一控制開關 IG_1A，以及一個位於 U 形記憶胞串列 109B 之第二串列選擇線開關 111B 和第二接地選擇線開關 110B 之間的第二控制開關 IG_1B。

【0031】 例如請參照第 4 圖，第 4 圖係繪示以第 1C 圖之單閘極垂直通道 NAND 記憶體元件 100 進行寫入操作時的等效電路圖。在本實施例中，第一控制開關 IG_1A 可以包括一種互補式切換電路(complementary switch circuit)123 與脊裝堆疊 104B 的底部導電條帶 104B1 連接，用以控制位於脊裝堆疊 104B 底部之記憶胞 108 的啟閉。第二控制開關 IG_1B 與位於脊裝堆疊 104D 的底部導電條帶 104D1 連接，用以控制位於脊裝堆疊 104D 底部之記憶胞 108 的啟閉。由於，第二控制開關 IG_1B 的結構可以與第一控制開關 IG_1A 相同，故第二控制開關 IG_1B 的結構不再繪示於

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第 4 圖中。但在其他實施例中，第二控制開關 IG_1B 的結構仍可以與第一控制開關 IG_1A 不同。

【0032】 另外在一些較佳的實施例中，單閘極垂直通道 NAND 記憶體元件 100 還可以包括一個位於第一接地選擇線開關 110A 和第一控制開關 IG_1A 之間的第一輔助開關 IG_0A，以及一個位於第二接地選擇線開關 110B 和第二控制開關 IG_1B 之間的第二輔助開關 IG_0B。同樣的，第一輔助開關 IG_0A 和第二輔助開關 IG_0B 的結構可以與第一控制開關 IG_1A 相同或不同。

【0033】 在本實施例中，第一輔助開關 IG_0A 係與脊裝堆疊 104A 的底部導電條帶 104A1 連接，用以控制位於脊裝堆疊 104A 底部之記憶胞 108 的啟閉；第二輔助開關 IG_0B 係與脊裝堆疊 104C 底部的導電條帶 104C1 連接，用以控制位於脊裝堆疊 104C 底部之記憶胞 108 的啟閉。

【0034】 當以第一串列選擇開關 111A 選擇第一 U 形記憶胞串列 109A 中的記憶胞 108P 進行寫入操作時，會開啟第一串列選擇線開關 111A、第一控制開關 IG_1A 和第一輔助開關 IG_0A；並關閉第一接地選擇線開關 110A。以位元線 115 和共同源極線 118 同時對第一串列選擇線開關 111A 和第一接地選擇線開關 110A 施加 0 伏電壓(0V)；再藉由字元線 120 對被選取記憶胞 108P 施加一閘極寫入電壓 Vpgm；以及對位於第一 U 型記憶胞串列 109A 上的其他記憶胞 108 施加一閘極通過電壓 Vpass。其中，閘極寫入電壓 Vpgm 大於閘極通過電壓 Vpass，藉以引發電子 e-產

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生 Fowler–Nordheim 穿隧效應，將資料寫入記憶胞 108P 之中。

【0035】 未被選擇的第二 U 形記憶胞串列 109B 在進行寫入操作時，使位於脊狀堆疊 104D 上之第二串列選擇線開關 111B 和其下方的記憶胞的閘極保持浮置(floating)。由於脊狀堆疊 104A 和 104C 中的導電條帶共用一個字元線接觸結構 119C；且第一接地選擇線開關 110A 和第二接地選擇線開關 110B 也共用接地選擇線接觸墊 122。因此，施加在脊狀堆疊 104C 上之第二接地選擇線開關 110B 以及其下方之記憶胞 108(包含記憶胞 108P')的閘極電壓，會和施加在脊狀堆疊 104A 上之第一接地選擇線開關 110A 以及其下方之記憶胞 108(包含記憶胞 108P)的閘極電壓完全相同。關閉第二控制開關 IG_1B，可使第二 U 形記憶胞串列 109B 內之 104C 形成局部自我電位抬升(local self-boosting)以維持足夠的電位，防止位於脊狀堆疊 104C 上之記憶胞 108P'受到寫入電壓 Vpgm 的影響而被寫入。

【0036】 請參照第 5 圖，第 5 圖係繪示以第 1C 圖之單閘極垂直通道 NAND 記憶體元件 100 進行讀取操作時的等效電路圖。在本實施例中，當以第一串列選擇線開關 111A 選擇位於第一 U 形記憶胞串列 109A 上的記憶胞 108R 進行讀取操作時，會開啟第一串列選擇線開關 111A、第一接地選擇線開關 110A、第一控制開關 IG_1A 和第一輔助開關 IG_0A。使位元線 115 和共同源極線 118 同時對第一串列選擇線開關 111A 和第一接地選擇線開關 110A 分別施加 1 伏特(1V)及 0 伏電壓(0V)；再藉由字元線 120 對

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被選取的記憶胞 108R 施加一閘極讀取電壓 Vref；以及對位於第一 U 型記憶胞串列 109A 上的其他記憶胞 108 施加一閘極通過電壓 Vpass。即可由被選取的記憶胞 108R 中讀取資料。

【0037】 未被選擇的第二 U 形記憶胞串列 109B 在進行讀取操作時，位於脊狀堆疊 104D 上的第二串列選擇線開關 111B 和其下方的記憶胞 108 閘極保持浮置。由於脊狀堆疊 104A 和 104C 中的導電條帶共用一個字元線接觸結構 119C；且第一接地選擇線開關 110A 和第二接地選擇線開關 110B 也共用接地選擇線接觸墊 122。因此，施加在脊狀堆疊 104C 上之第二接地選擇線開關 110B 以及其下方之記憶胞 108(包含記憶胞 108R')的閘極電壓，會和施加在脊狀堆疊 104A 上之第一接地選擇線開關 110A 以及其下方之記憶胞 108(包含記憶胞 108R)的閘極電壓完全相同。關閉第二控制開關 IG_1B，並且使第二 U 形記憶胞串列 109B 中的第二串列選擇線開關 111B 和其下方的記憶胞 108 之閘極保持浮置，可防止未被選取之第二 U 形記憶胞串列 109B 中的記憶胞 108R'被閘極讀取電壓 Vref 所讀取。

【0038】 請參照第 6 圖，第 6 圖係繪示以第 1C 圖之單閘極垂直通道 NAND 記憶體元件 100 進行抹除操作時的等效電路圖。在本實施例中，當選擇第一 U 形記憶胞串列 109A 進行抹除操作時，會對第一串列選擇線開關 111A、第一控制開關 IG_1A 和第一輔助開關 IG_0A 的閘極施加 7 伏電壓(7V)，藉以將其開啟；以共同源極線 118 對第一接地選擇線開關 110A 施加 0 伏電壓(0V)，

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將第一接地選擇線開關 110A 的閘極保持浮置；對位於第一 U 型記憶胞串列 109A 上的所有記憶胞 108 的閘極施加 0 伏電壓(0V)；再以位元線 115 對第一串列選擇線開關 111A 施加 20 伏特(20V)的抹除電壓。藉以使位於第一 U 型記憶胞串列 109A 上的記憶胞 108 產生閘極誘發汲極漏電流(Gated-Induce Drain Leakage，GIDL) GIDL。

【0039】 未被選擇的第二 U 形記憶胞串列 109B 在進行抹除操作時，位於脊狀堆疊 104D 上的第二串列選擇線開關 111B 和其下方的記憶胞 108 以及第二控制開關 IG_1B 和第二接地選擇開關 110B 的閘極都保持浮置。由於脊狀堆疊 104A 和 104C 中的導電條帶共用一個字元線接觸結構 119C；且第一接地選擇線開關 110A 和第二接地選擇線開關 110B 也共用接地選擇線接觸墊 122。因此，施加在脊狀堆疊 104C 上之第二接地選擇線開關 110B 以及其下方之記憶胞 108 的閘極電壓，會和施加在脊狀堆疊 104A 上之第一接地選擇線開關 110A 以及其下方之記憶胞 108 的閘極電壓完全相同。使位於脊狀堆疊 104D 上的第二串列選擇線開關 111B 和其下方的記憶胞 108 以及第二控制開關 IG_1B 的閘極都保持浮置，可延遲抹除時間，防止第二 U 形記憶胞串列 109B 中的記憶胞 108 在奈秒抹除時間內被抹除。

【0040】 根據上述實施例，本說明書是提供一種具有多個脊狀堆疊的三維記憶體元件，其中每一個脊狀堆疊包含，分別具有位於頂部的一個串列選擇線開關或一個接地選擇線開關以及位

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於串列選擇線開關或接地選擇線開關下方的複數個記憶胞。藉由串接位於兩個脊狀堆疊上的第一串列選擇線開關和第一接地選擇線開關，以及位於第一串列選擇線開關和第一接地選擇線開關下方的記憶胞來形成第一 U 形記憶胞串列；同時藉由串接位於另外兩個不同脊狀堆疊上的第二串列選擇線開關和第二接地選擇線開關，以及位於第二串列選擇線開關和第二接地選擇線開關下方的記憶胞來形成第二 U 形記憶胞串列。

【0041】 其中，位於第一 U 形記憶胞串列之第一串列選擇線開關下方的記憶胞與第一字元線接觸結構連接；位於第二 U 形記憶胞串列之第二串列選擇線開關下方的記憶胞與第二字元線接觸結構連接；而位於第一 U 形記憶胞串列之第一接地選擇線開關下方的記憶胞以及位於第二 U 形記憶胞串列之第二接地選擇線開關下方的記憶胞，則連接至相同的第三字元線接觸結構。換句話說，三維記憶體元件中，用來連接位於接地選擇開關下方之記憶胞的字元線接觸結構數量小於用來連接位於串列選擇開關下方之記憶胞的字元線接觸結構。若與先前技術中的三維記憶體元件相比，在不改變記憶容量的前提下，可以減少字元線接觸結構的設置。

【0042】 藉由減少字元線接觸結構的設置，可以減少記憶體元件的面積尺寸；更可在不影響製程裕度的前提下，擴充記憶體元件的記憶容量，大幅降低製程成本，並防止氧化層擊穿現象產生，增加垂直通道記憶體元件的製程良率。

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【符號說明】

【0043】

100、300：記憶體元件

101：基材

102：導電層

103：絕緣層

104：多層堆疊結構

104A、104B、104C、104D：脊狀堆疊

104A1-104A6、104B1-104B6、104C1-104C6、104D1-104D6：導電條帶

105：溝槽

106：記憶材料層

107：半導體通道層

108、108P、108R：記憶胞

109A、109B：U形記憶胞串列

110A、110B：接地選擇線開關

111A、111B：串列選擇開關

112：介電材質層

113：空氣間隙

114：接觸插塞

115：位元線

116：接觸插塞

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117：金屬導線

118：共同源極線

119A、119B、119C、319C：字元線接觸結構

120：字元線

121、122：接觸墊

IG_1A、IG_1B 控制開關

IG_0A、IG_0B：輔助開關

Vpgm：寫入電壓

Vpass：閘極通過電壓

Vref：閘極讀取電壓 floating：浮置

GIDL：閘極誘發汲極漏電流

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201721921 專利案號：104142185

申請日：104. 12. 15

201721921

IPC分類：
H01L 51/00 (2006.01)
H01L 21/8239 (2006.01)

【發明摘要】

【中文發明名稱】三維記憶體元件

【英文發明名稱】THREE DIMENSIONAL MEMORY DEVICE

【中文】

一種三維記憶體元件，包括多層堆疊結構多層堆疊結構包括複數個導電條帶及複數條溝槽，以定義出第一、第二、第三和第四脊狀堆疊；位於第一脊狀堆疊上的第一串列選擇線開關；位於第二脊狀堆疊上的第一接地選擇線開關；第一 U 形記憶胞串列，串接第一串列選擇線開關和第一接地選擇線開關；位於第三脊狀堆疊上的第二串列選擇線開關；位於第四脊狀堆疊上的第二接地選擇線開關；第二 U 形記憶胞串列，串接第二串列選擇線開關和第二接地選擇線開關。第一字元線接觸結構與第一脊狀堆疊的導電條帶接觸。第二字元線接觸結構與第二脊狀堆疊的導電條帶接觸；第三字元線接觸結構與第三和第四脊狀堆疊的導電條帶接觸。

【英文】

A 3D memory device includes a multi-layer stacks structure having a plurality of conductive strips and a first, a second, a third and a fourth ridge stack; a first SSL switch, a first GSL switch, a second SSL switch and a second GSL switch respectively disposed on the first, the second the third and the fourth ridge stack; a first

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U-shaped memory cells string connecting the first SSL switch with the first GSL switch; a second U-shaped memory cells string connecting the second SSL switch with the second GSL switch; a first word lines contact in contact with the conductive strips disposed in the first ridge stack; a second word lines contact in contact with the conductive strips disposed in the second ridge stack; and a third word lines contact in contact with the conductive strips disposed in the third ridge stack and the fourth ridge stack.

【指定代表圖】：第 (1D) 圖。

【代表圖之符號簡單說明】：

100：記憶體元件

101：基材

102：導電層

103：絕緣層

104：多層堆疊結構

104A、104B、104C、104D：脊狀堆疊

106：記憶材料層

107：半導體通道層

108：記憶胞

109A、109B：U 形記憶胞串列

110A、110B：接地選擇線開關

111A、111B：串列選擇開關

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112：介電材質層

113：空氣間隙

114、116：接觸插塞

115：位元線

117：金屬導線

118：共同源極線

119B：字元線接觸結構

120：字元線

【特徵化學式】：無。

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【發明申請專利範圍】

【第 1 項】一種三維(Three Dimemsional，3D)記憶體元件，包括：

一多層堆疊結構(multi-layer stacks)，包括彼此隔離的複數個導電條帶(conductive strips)以及複數條溝槽(trench)，用以至少定義出一第一脊狀堆疊 (ridge stacks)、一第二脊狀堆疊、一第三脊狀堆疊以及一第四脊狀堆疊；

一第一串列選擇線(String Selection Line，SSL)開關，位於該第一脊狀堆疊之上；

一第一接地選擇線(Ground Selection Line，GSL)開關，位於該第二脊狀堆疊之上；

一第一 U 形記憶胞串列(U-shaped cell string)，串接該第一串列選擇線開關和該第一接地選擇線開關；

一第二串列選擇線開關，位於該第三脊狀堆疊之上；

一第二接地選擇線開關，位於該第四脊狀堆疊之上；

一第二 U 形記憶胞串列，串接該第二串列選擇線開關和該第二接地選擇線開關；

一第一字元線接觸結構，與位於該第一脊狀堆疊上的該些導電條帶接觸；

一第二字元線接觸結構，與位於該第二脊狀堆疊上的該些導電條帶接觸；以及

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一第三字元線接觸結構，與位於該第三脊狀堆疊和該第四脊狀堆疊上的該些導電條帶接觸。

【第 2 項】如申請專利範圍第 1 項所述之三維記憶體元件，更包括

一第一串列選擇線接觸墊，與位於該第一脊裝堆疊的一頂部導電條帶接觸；

一第二串列選擇線接觸墊，與位於該第三脊裝堆疊的一頂部導電條帶接觸；以及

一接地選擇線接觸墊，與位於該第二脊裝堆疊和該的四脊裝堆疊的二頂部導電條帶接觸。

【第 3 項】如申請專利範圍第 1 項所述之三維記憶體元件，更包括：

一記憶材料層，位於該些溝槽的複數個側壁上；

一圖案化通道膜，覆蓋於該記憶材料層以及該些溝槽的複數個底部上；以及

複數個記憶胞，形成於該記憶材料層和該圖案化通道膜與該些導電條帶三者重疊的複數個位置(cross point)。

【第 4 項】如申請專利範圍第 3 項所述之三維記憶體元件，其中：

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該第一 U 形記憶胞串列係藉由一部分該圖案化通道膜串接該第一串列選擇線開關、位於該第一脊狀堆疊和該第二脊狀堆疊上的該些記憶胞以及該第一接地選擇線開關所形成；以及

該第二 U 形記憶胞串列係藉由另一部分該圖案化通道膜串接該第二串列選擇線開關、位於該第三脊狀堆疊和該第四脊狀堆疊上的該些記憶胞以及該第二接地選擇線開關所形成。

【第 5 項】如申請專利範圍第 3 項所述之三維記憶體元件，更包括：

一第一控制開關，位於該第一串列選擇線開關和該第一接地選擇線開關之間；以及

一第二控制開關，位於該第二串列選擇線開關和該第二接地選擇線開關之間。

【第 6 項】如申請專利範圍第 5 項所述之三維記憶體元件，其中：

該第一控制開關與該第一脊裝堆疊的一底部導電條帶連接；以及

該第二控制開關與該第三脊裝堆疊的一底部導電條帶連接。

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【第 7 項】如申請專利範圍第 6 項所述之三維記憶體元件，更包括：

一第一輔助開關，位於該第一控制開關和該第一接地選擇線開關之間；以及

一第二輔助開關，位於該第二控制開關和該第二接地選擇線開關之間。

【第 8 項】如申請專利範圍第 7 項所述之三維記憶體元件，其中：

該第一輔助開關與該第二脊裝堆疊的一底部導電條帶接觸；以及

該第二輔助開關與該第四脊裝堆疊的一底部導電條帶接觸。

【第 9 項】如申請專利範圍第 5 項所述之三維記憶體元件，其中當選擇該第一 U 形記憶胞串列進行一寫入操作(program operation)時，該寫入操作包括：

開啟該第一串列選擇線開關和該第一控制開關；

關閉該第一接地選擇線開關、第二接地選擇線開關和該第二控制開關；以及

對位於該第一 U 型記憶胞串列上的該些記憶胞之一者施加一寫入電壓(Vpgm)；以及

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對位於該第一 U 型記憶胞串列上的其他該些記憶胞施加一通過電壓(Vpass)，其中該寫入電壓大於該導通電壓。

【第 10 項】如申請專利範圍第 9 項所述之三維記憶體元件，其中在進行該寫入操作時，該第二串列選擇線開關的一閘極係保持浮置(floating)。

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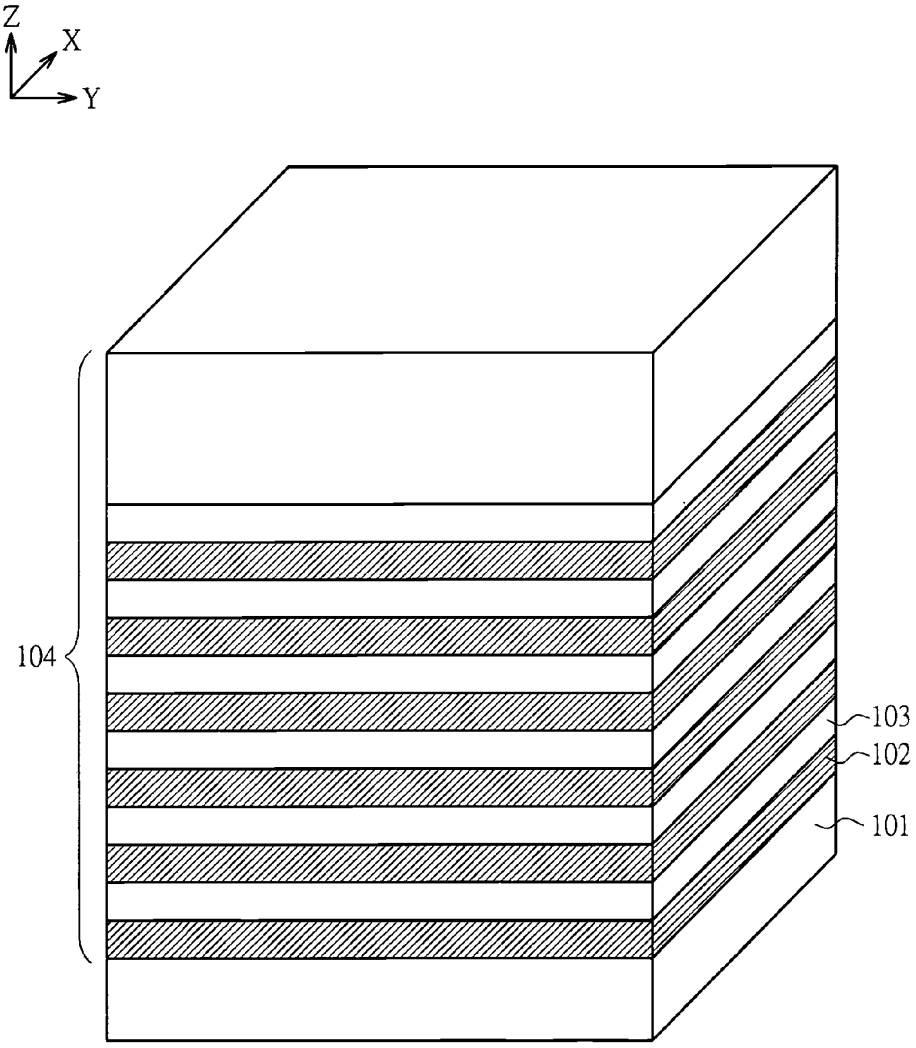
【發明圖式】



第 1A 圖

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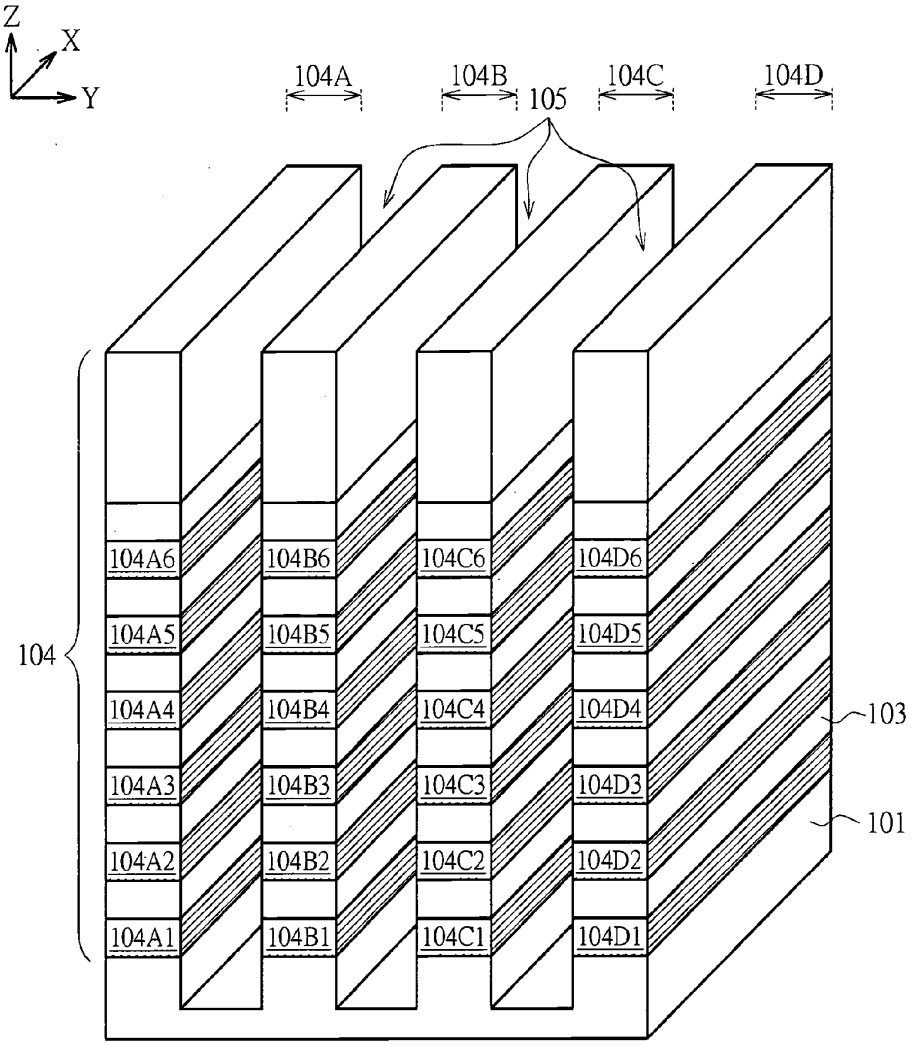

第 1B 圖

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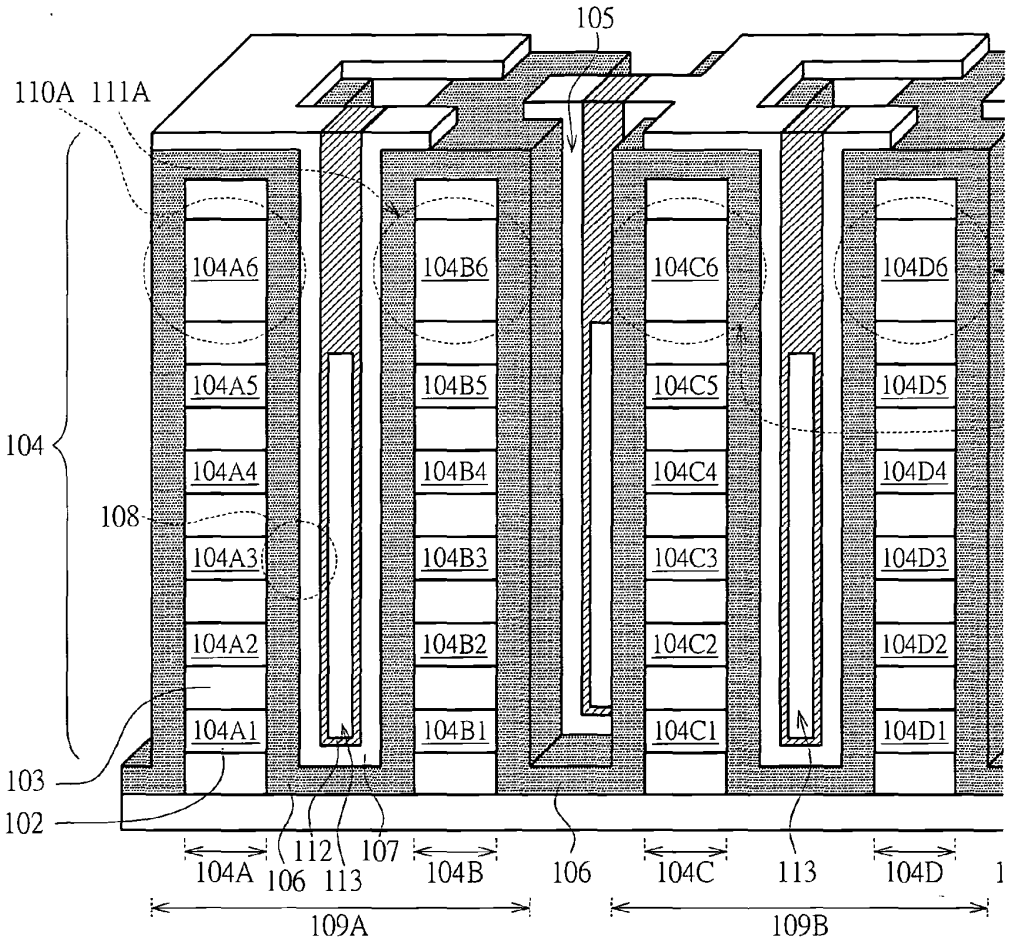
105
110A 111A
104A6
104B6
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104B5
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104C2
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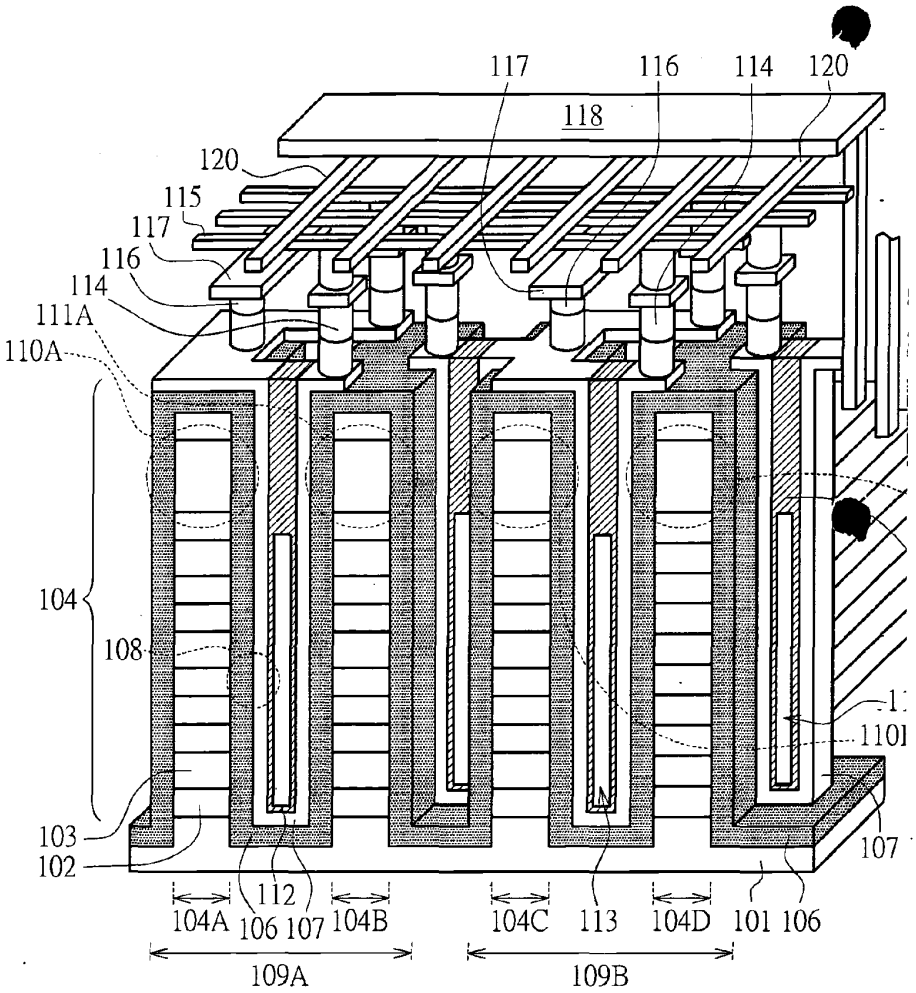
104D
109A
109B



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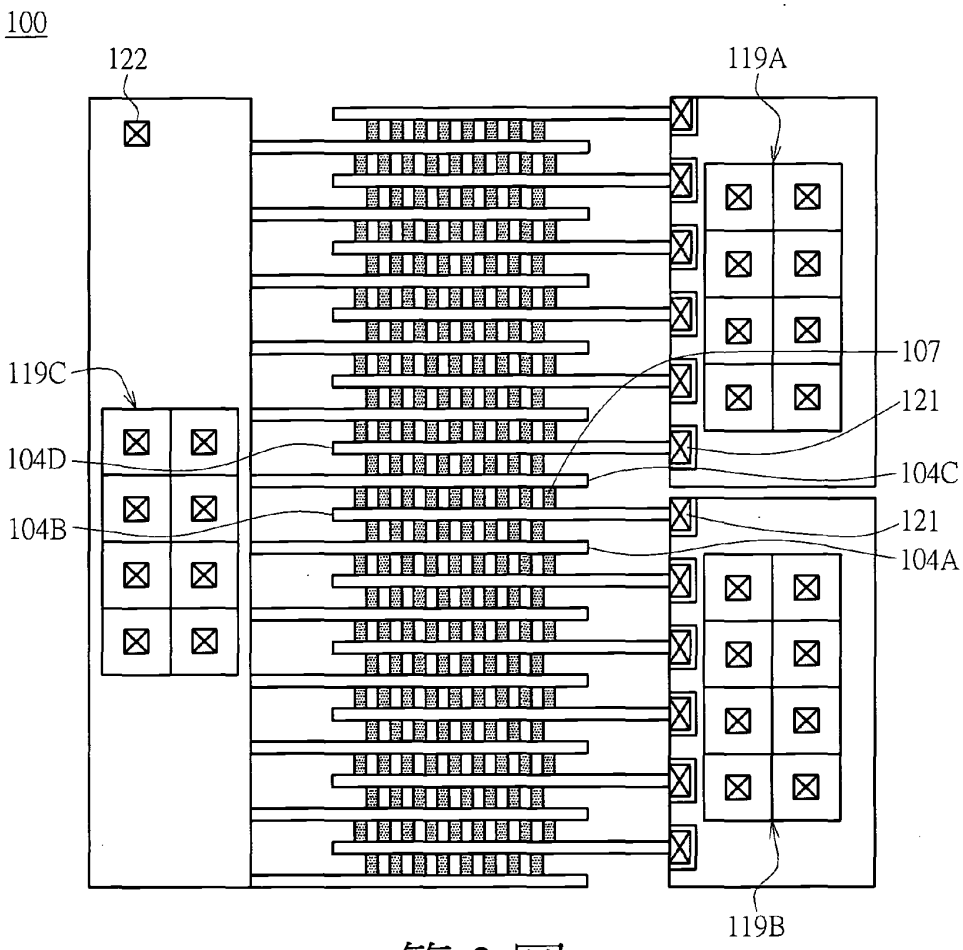

第 2 圖

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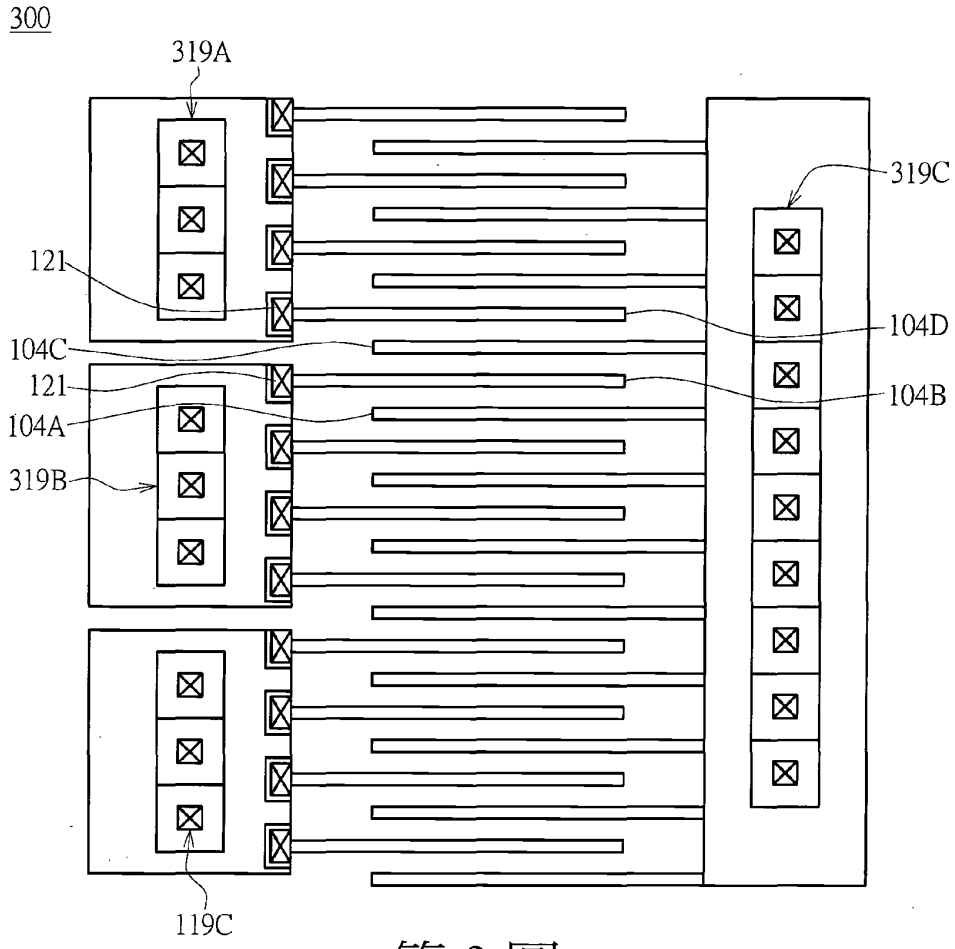

第 3 圖

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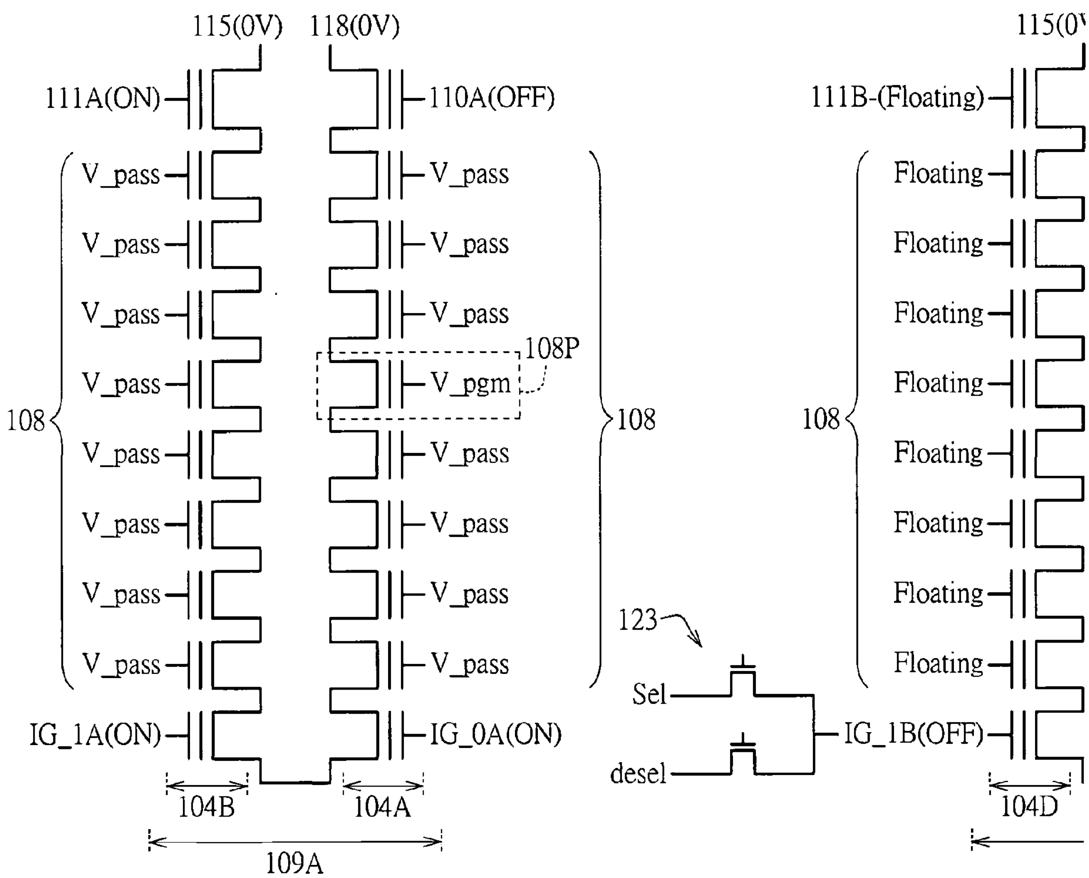

第 4 圖

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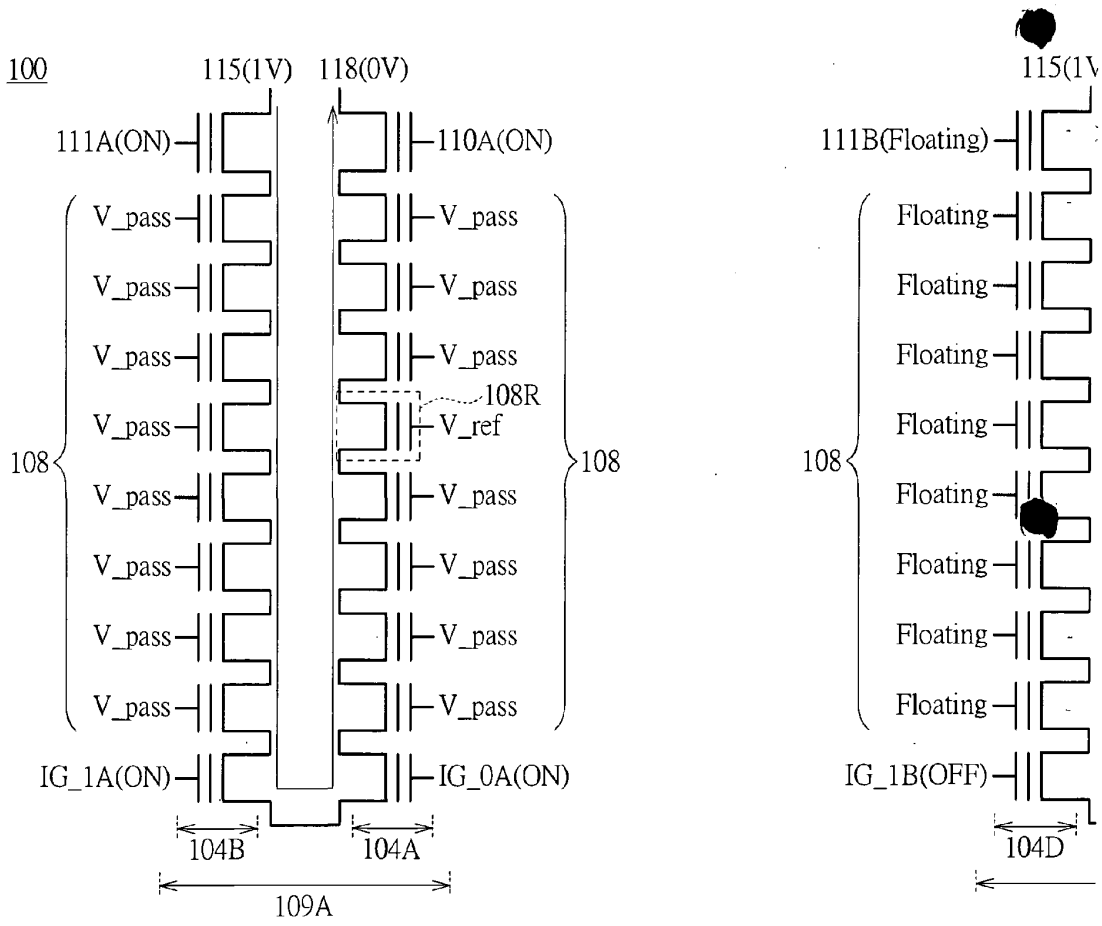

第 5 圖

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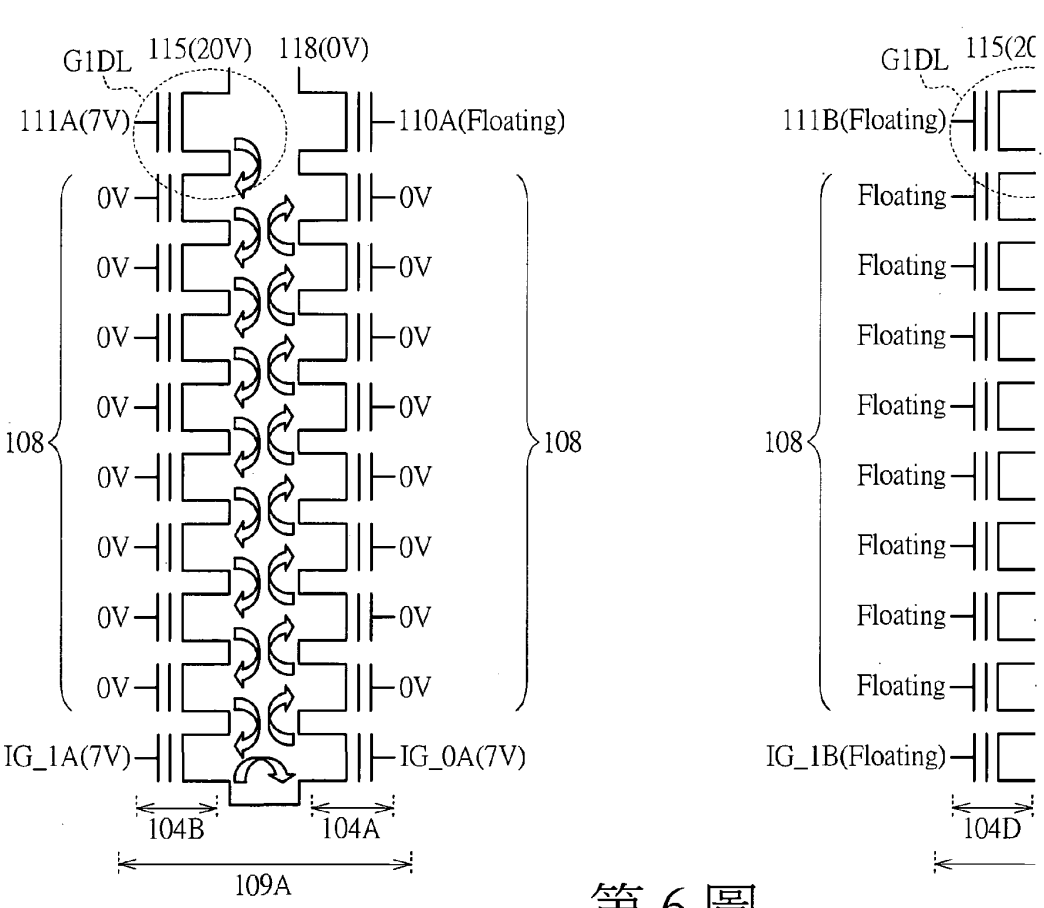

第 6 圖

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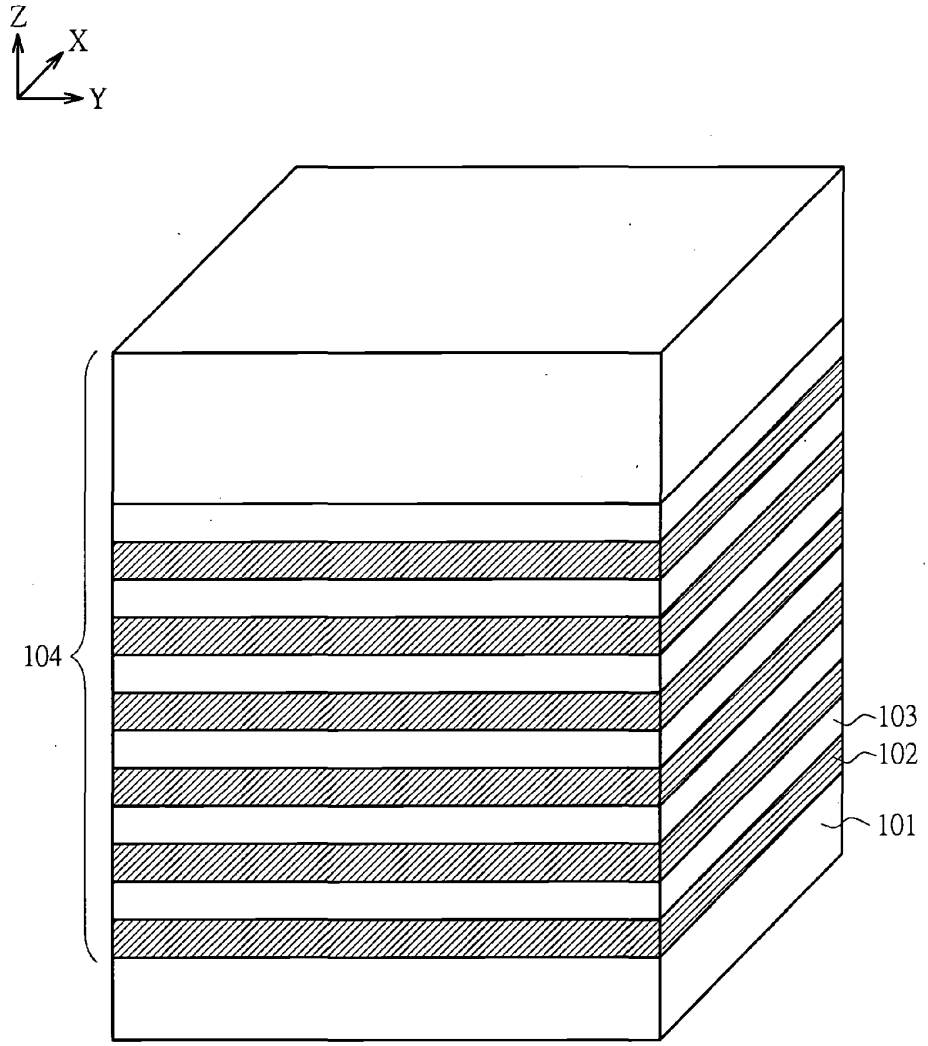
【發明圖式】

修正
104年12月21日
(全份)



第 1A 圖

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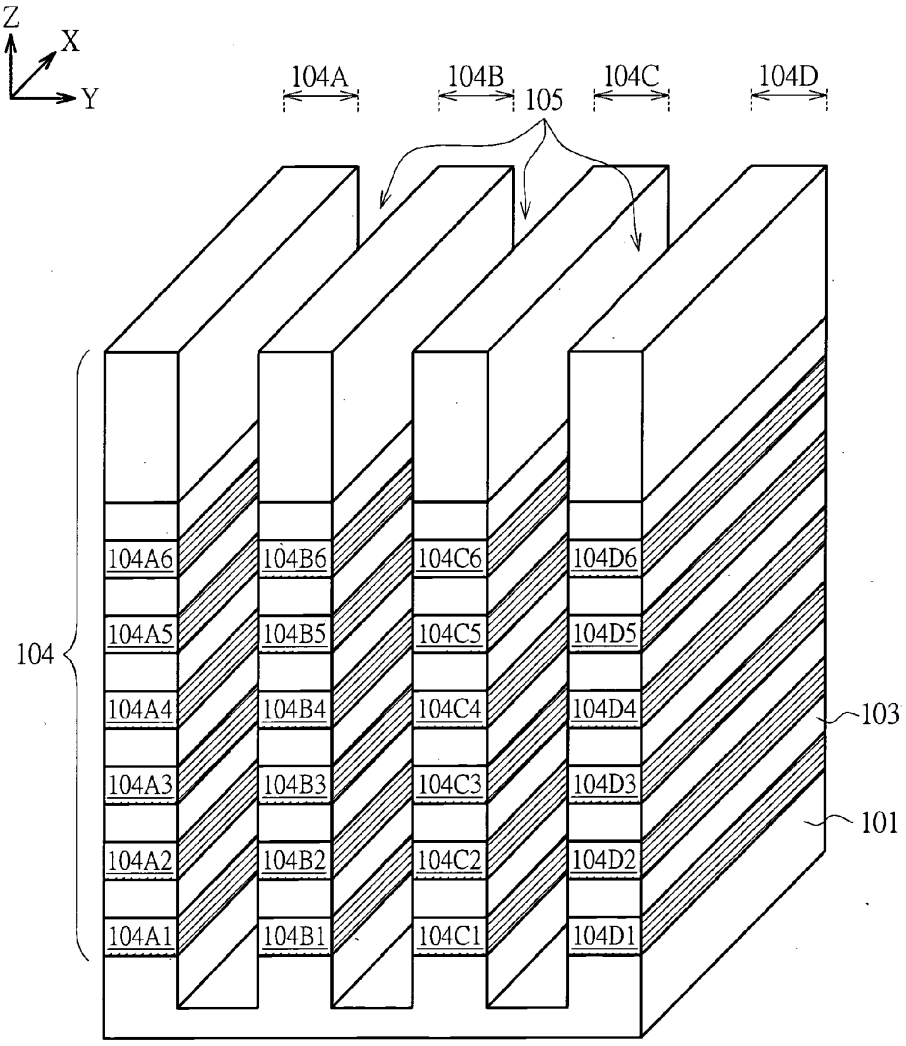

第 1B 圖

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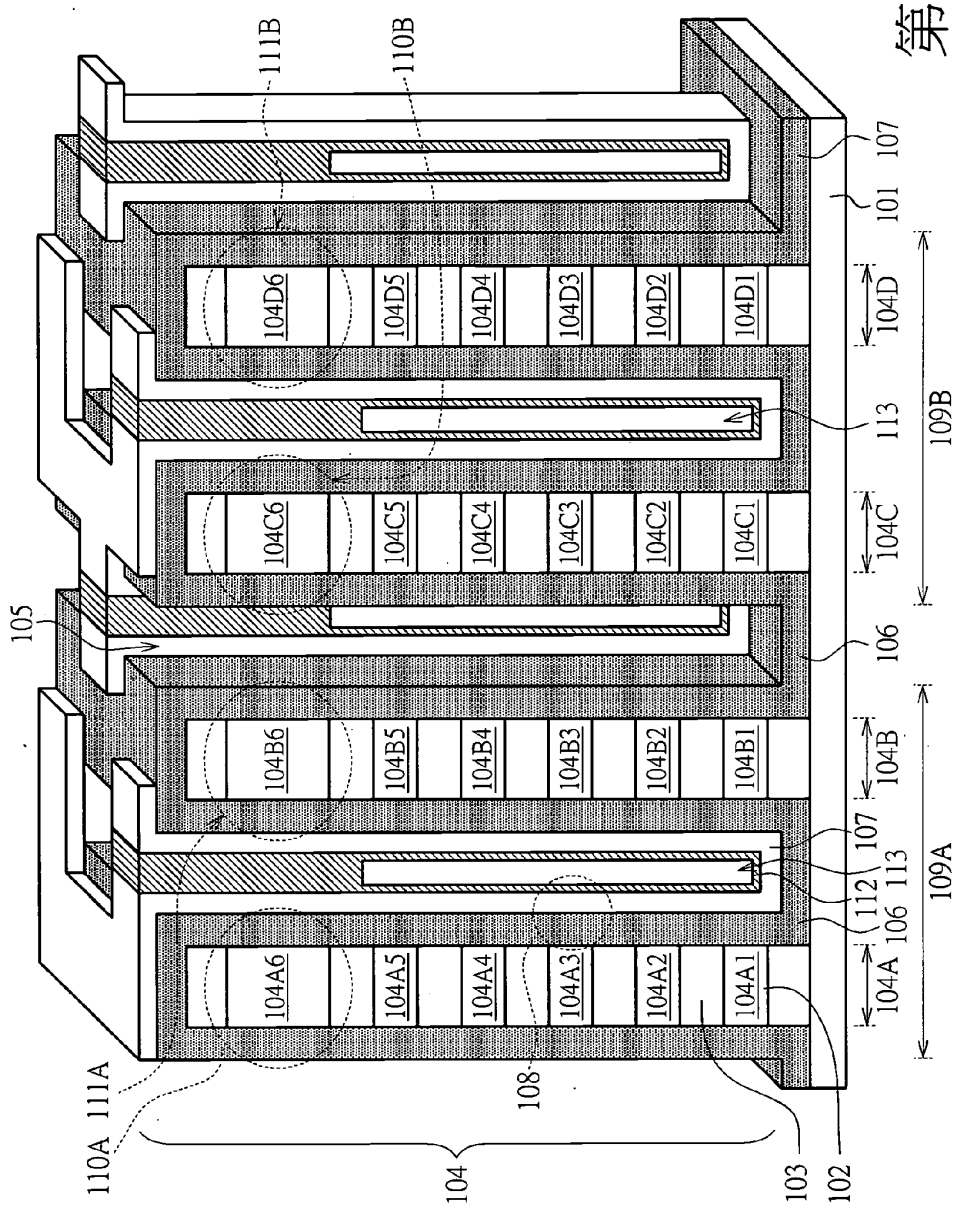
第1C圖



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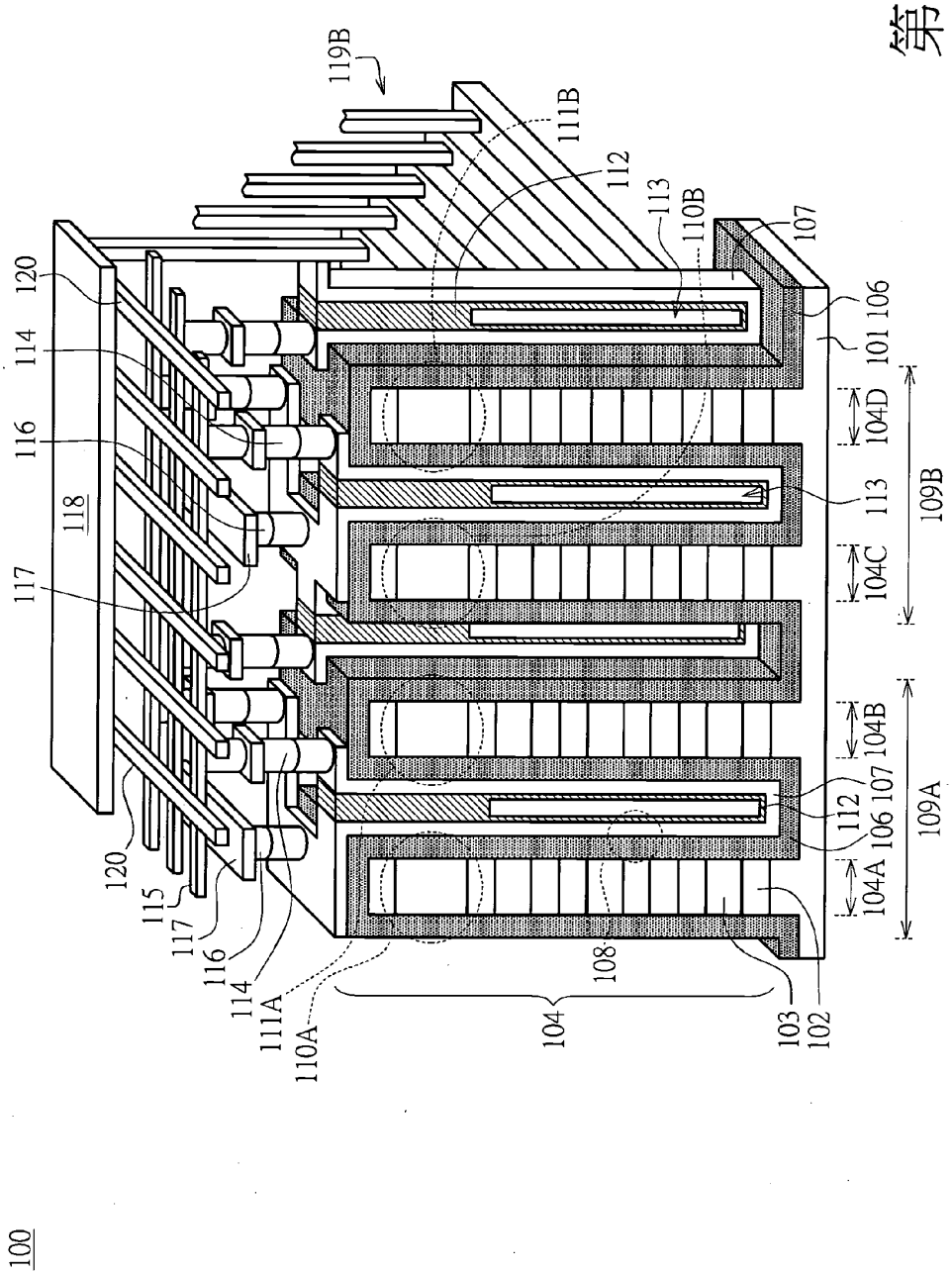
第1D圖



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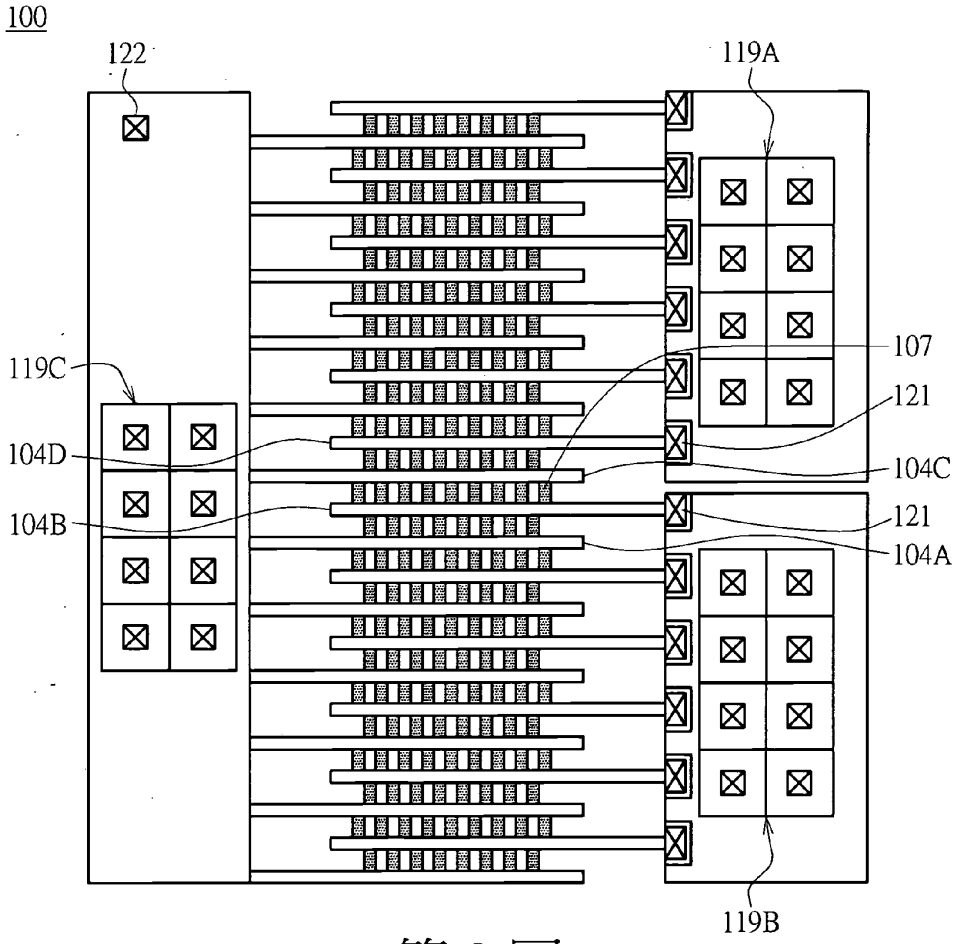

第 2 圖

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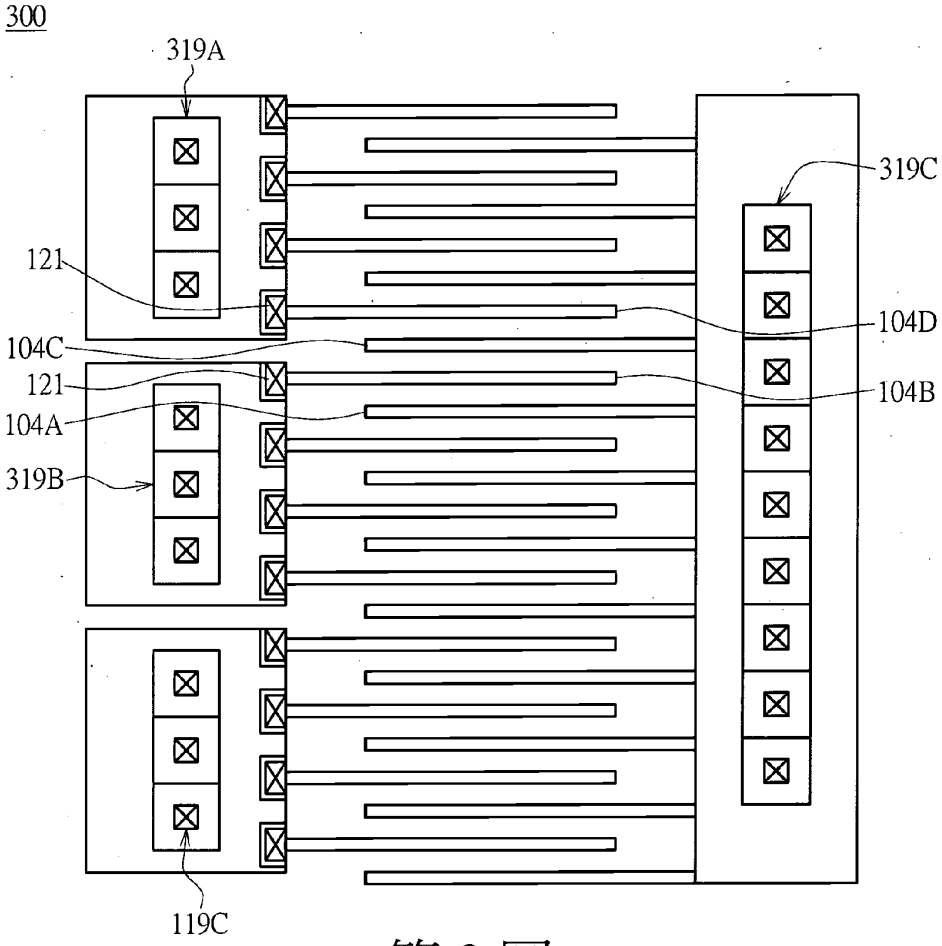

第 3 圖

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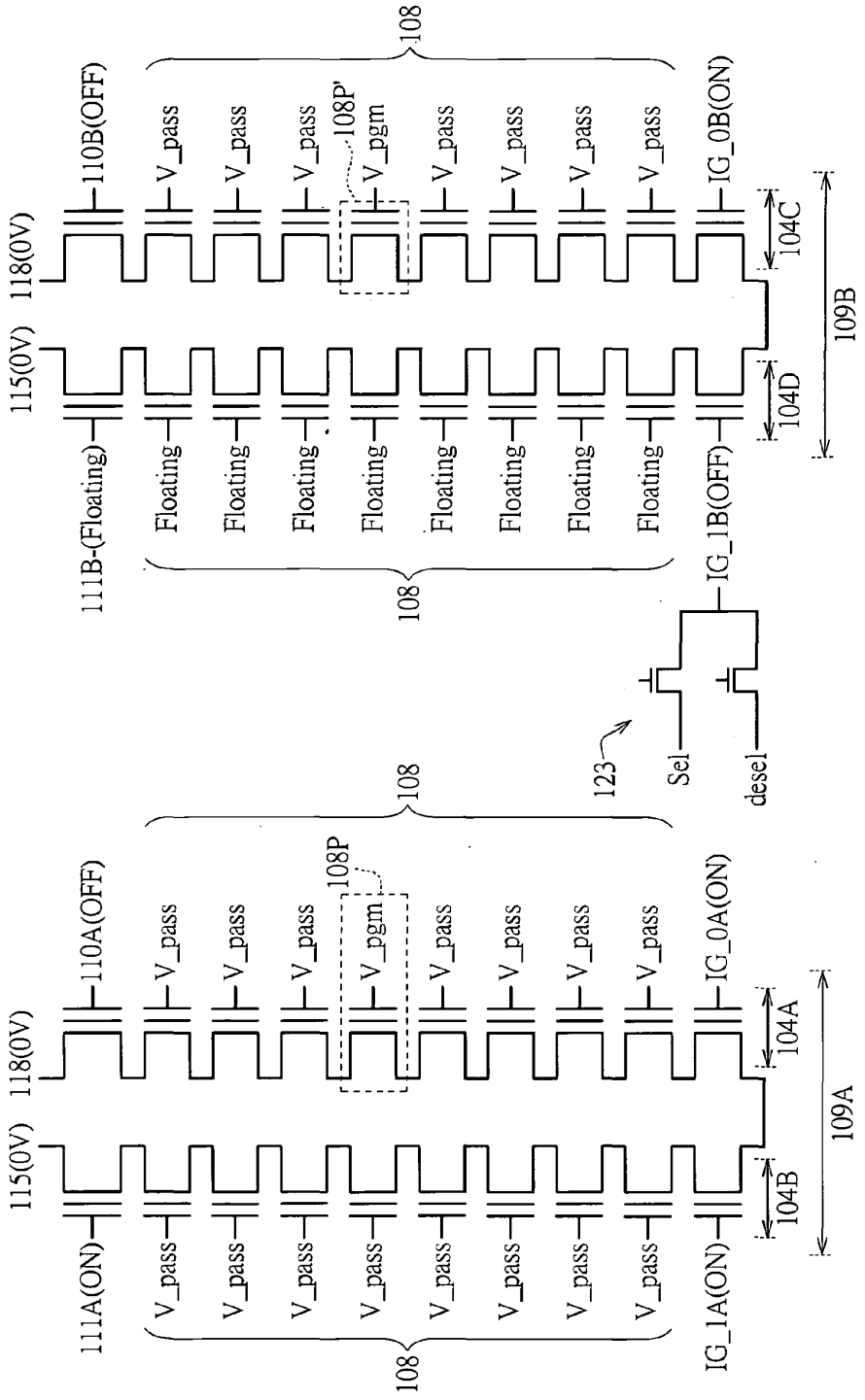

第 4 圖

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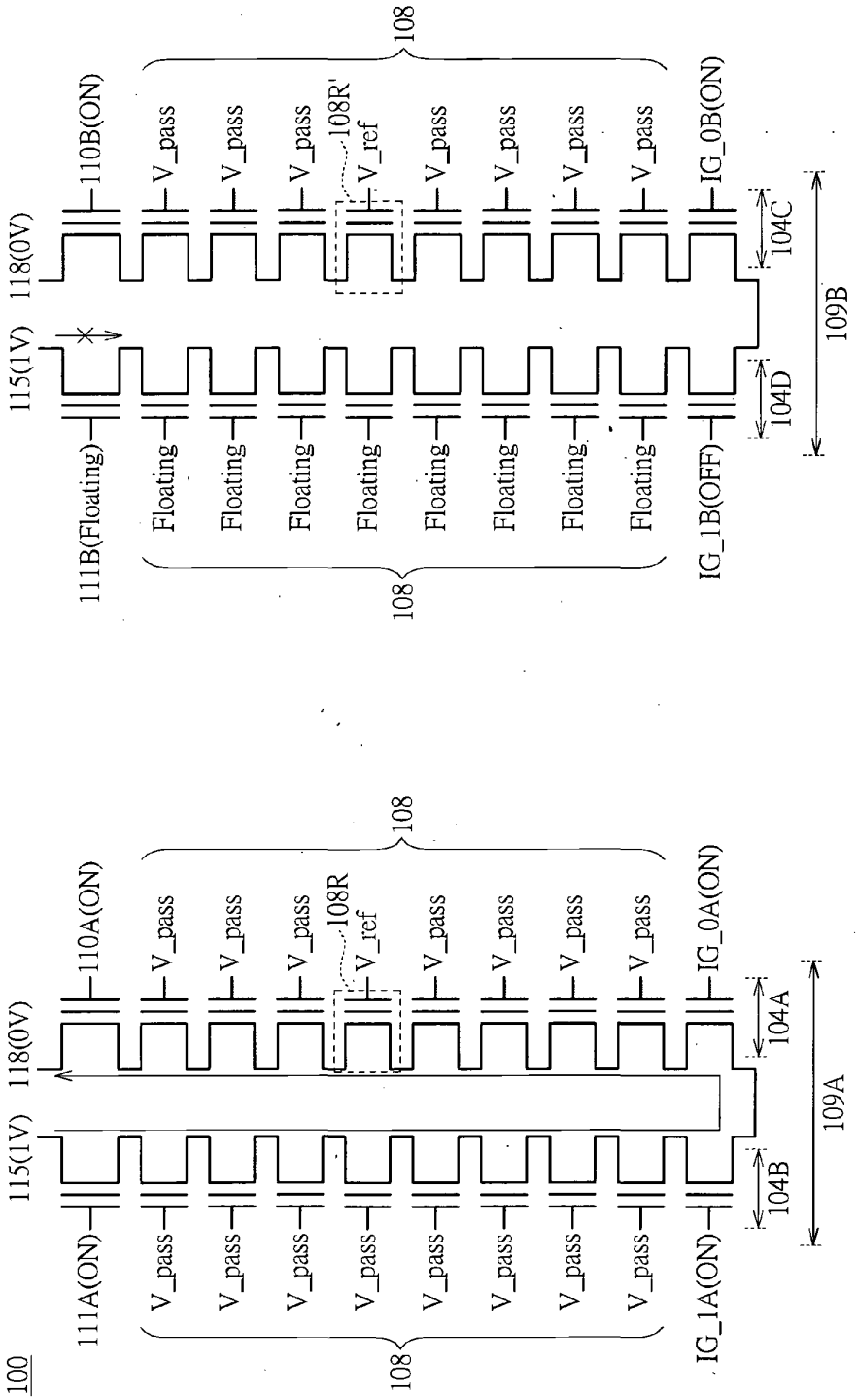

第 5 圖

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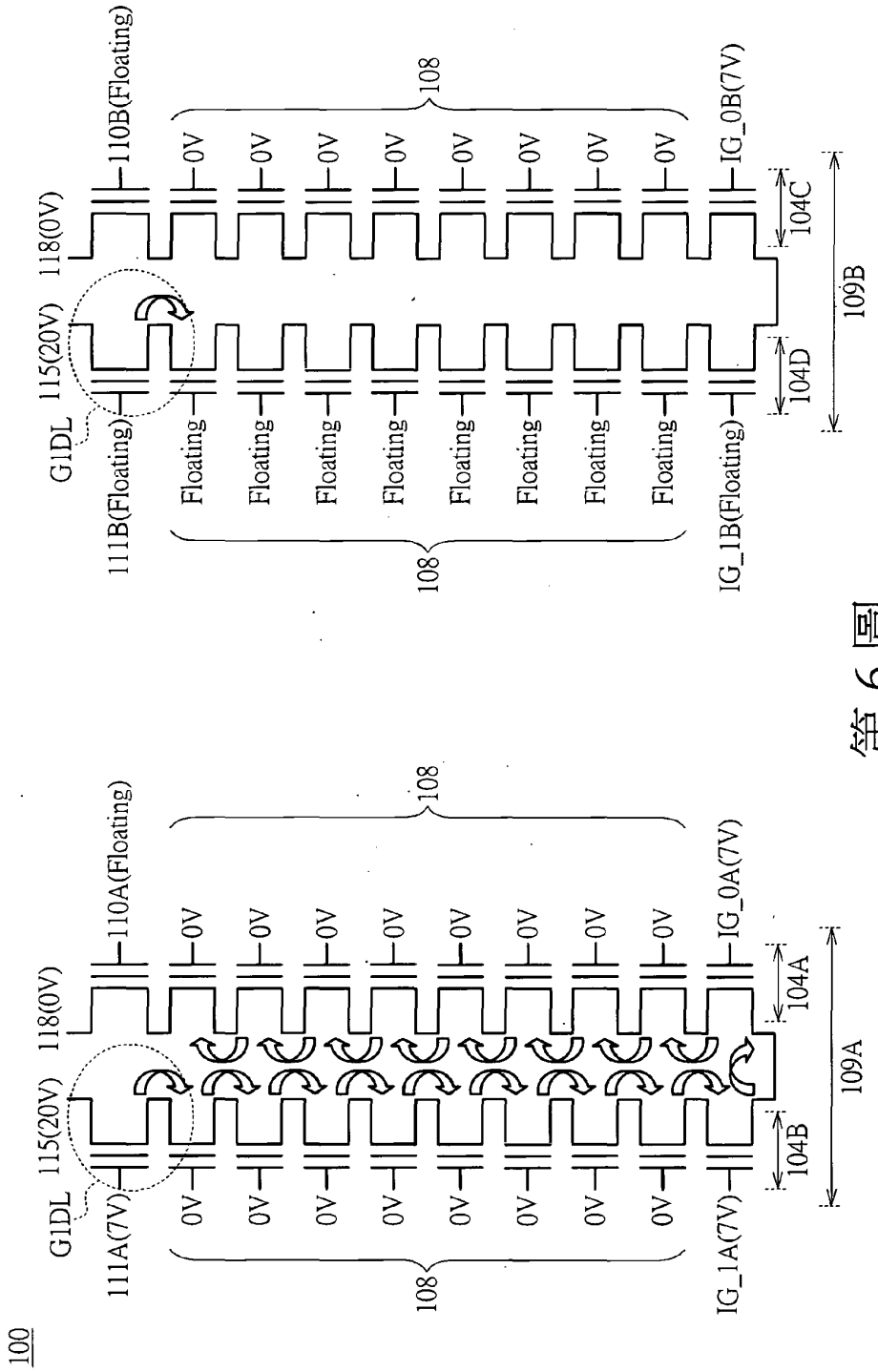

第6圖

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(72)发明人 李俊熙 朴镇泽

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代理人 张帆 陈源

(51)Int.Cl.
H01L 27/115(2006.01)
H01L 21/8247(2006.01)

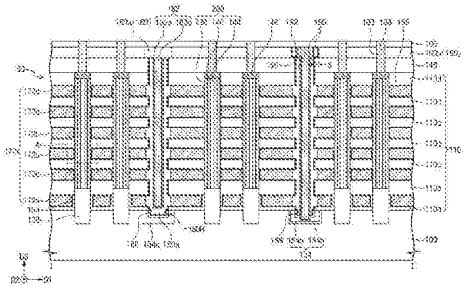
权利要求书3页 说明书21页 附图48页

(54)发明名称

半导体存储器装置及其制造方法

(57)摘要

本发明提供了半导体存储器装置及其制造方法。一种半导体存储器装置包括堆叠栅极结构，其沿着与衬底水平的第一方向彼此间隔开。堆叠栅极结构中的每一个包括交替和重复地堆叠在衬底上的绝缘层和栅电极。垂直沟道结构穿透堆叠栅极结构。源极插线设置在堆叠栅极结构之间。源极插线与衬底接触并且沿着与第一方向交叉的第二方向延伸。与源极插线接触的衬底包括沿着第二方向形成的多个突出区。突出区中的每一个具有第一宽度，并且突出区以大于第一宽度的第一距离彼此间隔开。



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1. 一种半导体存储器装置，包括：

衬底；

多个堆叠栅极结构，其沿着与所述衬底的主表面平行的第一方向彼此间隔开，所述堆叠栅极结构中的每一个包括交替和重复地堆叠在所述衬底上的绝缘层和栅电极；

多个垂直沟道结构，其穿透所述堆叠栅极结构中的每一个；以及

源极插线，其设置在所述堆叠栅极结构之间，所述源极插线与所述衬底接触，并且沿着与第一方向交叉的第二方向延伸，

其中，与所述源极插线接触的衬底包括沿着所述第二方向排列的多个突出区，

其中，所述突出区中的每一个具有第一宽度，并且

其中，所述突出区以大于所述第一宽度的第一距离彼此间隔开。

2. 根据权利要求 1 所述的半导体存储器装置，其中，所述垂直沟道结构中的每一个包括隧道介电层、电荷存储层、阻挡介电层和包括半导体材料的垂直沟道图案。

3. 根据权利要求 2 所述的半导体存储器装置，其中，所述垂直沟道图案包括从所述衬底垂直突出的第一垂直沟道图案以及垂直设置在所述第一垂直沟道图案上的第二垂直沟道图案，并且

其中，所述隧道介电层、所述电荷存储层和所属阻挡介电层布置在所述第二垂直沟道图案与所述多个堆叠栅极结构之间。

4. 根据权利要求 2 所述的半导体存储器装置，其中，所述源极插线包括势垒层和所述势垒层上的导电层。

5. 根据权利要求 1 所述的半导体存储器装置，还包括：

隔离绝缘图案，其设置在所述源极插线与所述堆叠栅极结构之间。

6. 根据权利要求 5 所述的半导体存储器装置，还包括：

选择性地设置在所述多个突出区上的下隔离绝缘图案，

其中，所述下隔离绝缘图案与所述源极插线的底表面直接接触，并且

其中，所述下隔离绝缘图案连接至所述隔离绝缘图案。

7. 根据权利要求 5 所述的半导体存储器装置，还包括：

设置在所述堆叠栅极结构上的支撑图案，

其中，所述支撑图案包括：多个桥，其沿着所述第一方向跨越所述源极插线，并且沿着所述第二方向彼此间隔开；以及固定部分，各固定部分分别连接至所述桥并设置在所述堆叠栅极结构上。

8. 根据权利要求 7 所述的半导体存储器装置，其中，所述桥沿着所述第一方向按照 z 字形排列。

9. 根据权利要求 7 所述的半导体存储器装置，其中，所述桥中的每一个与所述突出区中的每一个实质上垂直地重叠。

10. 根据权利要求 7 所述的半导体存储器装置，其中，所述支撑图案具有沿着所述第一方向延伸的直线形状。

11. 根据权利要求 1 所述的半导体存储器装置，其中，所述源极插线包括：上部，其包括沿着所述第二方向排列的多个凹槽区。

12. 根据权利要求 1 所述的半导体存储器装置，还包括：

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公共源极区，其与所述源极插线接触，并且设置在所述衬底中。

13. 一种半导体存储器装置，包括：

多个堆叠栅极结构，其设置在衬底上，所述堆叠栅极结构中的每一个包括交替和重复地堆叠在所述衬底上的绝缘层和栅电极，并且所述堆叠栅极结构沿着第一方向彼此间隔开；

多个垂直沟道结构，其穿透所述堆叠栅极结构中的每一个；

源极插线，其设置在所述多个堆叠栅极结构之间，所述源极插线包括导电材料并且沿着与所述第一方向交叉的第二方向延伸；以及

公共源极区，其与所述源极插线接触，并且设置在所述衬底中，

其中，所述公共源极区包括沿着所述第二方向交替地形成的第一掺杂物区和第二掺杂物区，

其中，所述第一掺杂物区具有第一高度，并且所述第二掺杂物区具有第二高度，并且

其中，所述第一高度大于所述第二高度。

14. 根据权利要求 13 所述的半导体存储器装置，还包括：

设置在所述第二掺杂物区中的第三掺杂物区，

其中，所述第三掺杂物区的掺杂物的浓度高于所述第一掺杂物区和所述第二掺杂物区的掺杂物的浓度。

15. 根据权利要求 13 所述的半导体存储器装置，还包括：

设置在所述第一掺杂物区上的下隔离绝缘图案。

16. 根据权利要求 15 所述的半导体存储器装置，还包括：

隔离绝缘图案，其设置在所述源极插线与所述堆叠栅极结构之间，

其中，所述隔离绝缘图案连接至所述下隔离绝缘图案。

17. 根据权利要求 13 所述的半导体存储器装置，还包括：

设置在所述堆叠栅极结构上的支撑图案，

其中，所述支撑图案包括：多个桥，其沿着所述第一方向跨越所述源极插线，并且沿着所述第二方向彼此间隔开；以及固定部分，各固定部分分别连接至所述桥并设置在所述堆叠栅极结构上。

18. 一种半导体存储器装置，包括：

多个垂直沟道结构，其设置在衬底上，并且沿着与所述衬底垂直的方向延伸；

多个堆叠栅极结构，其包围所述垂直沟道结构，并且包括沿着与所述衬底垂直的方向堆叠的栅电极，所述堆叠栅极结构沿着平行于所述衬底的第一方向彼此间隔开；以及

公共源极区，其形成在所述衬底中并包括多个突出区，所述多个突出区沿着与所述第一方向交叉的第二方向形成在所述堆叠栅极结构之间，

其中，所述突出区中的每一个具有在所述第二方向上的第一宽度，并且

其中，所述突出区以大于所述第一宽度的第一距离彼此间隔开。

19. 根据权利要求 18 所述的半导体存储器装置，还包括：

源极插线，其设置在所述公共源极区上，所述源极插线与所述公共源极区接触并且沿着所述第二方向延伸。

20. 根据权利要求 18 所述的半导体存储器装置，还包括：

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设置在所述堆叠栅极结构上的支撑图案，

其中，所述支撑图案包括：多个桥，其沿着所述第一方向跨越所述源极插线，并且沿着所述第二方向彼此间隔开；以及固定部分，各固定部分分别连接至所述桥并设置在所述堆叠栅极结构上。

21. 一种制造半导体存储器装置的方法，包括步骤：

形成从衬底垂直延伸的多个垂直沟道结构；

形成包围所述垂直沟道结构的多个堆叠栅极结构，所述多个堆叠栅极结构包括沿着与所述衬底垂直的方向堆叠的栅电极，并且所述堆叠栅极结构沿着平行于所述衬底的第一方向彼此间隔开；以及

在所述衬底中形成公共源极区，所述公共源极区在所述多个堆叠栅极结构之间，

其中，所述公共源极区包括沿着与所述第一方向交叉的第二方向交替地形成的第一掺杂物区和第二掺杂物区，所述第一掺杂物区具有第一高度，并且所述第二掺杂物区具有小于所述第一高度的第二高度。

22. 根据权利要求 21 所述的方法，还包括步骤：

在所述第二掺杂物区中形成第三掺杂物区，

其中，所述第三掺杂物区的掺杂物的浓度高于所述第一掺杂物区和所述第二掺杂物区的掺杂物的浓度。

23. 根据权利要求 21 所述的方法，还包括步骤：

在所述第一掺杂物区上形成下隔离绝缘图案。

24. 根据权利要求 23 所述的方法，还包括步骤：

在所述多个堆叠栅极结构之间形成源极插线，所述源极插线与所述公共源极区接触并且沿着所述第二方向延伸；以及

在所述源极插线与所述堆叠栅极结构之间形成隔离绝缘图案，

其中，所述隔离绝缘图案连接至所述下隔离绝缘图案。

25. 根据权利要求 24 所述的方法，还包括步骤：

在所述堆叠栅极结构上形成支撑图案，

其中，所述支撑图案包括：多个桥，其沿着所述第一方向跨越所述源极插线，并且沿着所述第二方向彼此间隔开；以及固定部分，各固定部分分别连接至所述桥并设置在所述堆叠栅极结构上。

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半导体存储器装置及其制造方法

[0001] 相关申请的交叉引用

[0002] 本申请要求于2014年5月2日在韩国知识产权局提交的韩国专利申请No.10-2014-0053601的优先权，该申请的公开全文以引用方式并入本文中。

技术领域

[0003] 本发明构思涉及半导体存储器装置及其制造方法。更具体地说，本发明构思涉及三维(3D)半导体存储器装置及其制造方法。

背景技术

[0004] 半导体装置正变得更加高度集成以提供高性能和低成本。半导体存储器装置的集成密度直接影响半导体存储器装置的成本，从而导致对高度集成的半导体装置的需求。常规二维(2D)的或平面的存储器装置的集成度主要由单位存储器单元占据的面积来确定。因此，形成细微图案的技术会极大地影响常规2D存储器装置的集成密度。然而，因为形成细微图案需要极高价格的设备，所以，2D存储器装置的集成密度尽管继续增大却仍然受限。因此，已针对包括垂直排列的存储器单元的3D半导体存储器装置进行了研究。

发明内容

[0005] 本发明构思的实施例可提供能够提高集成度以及改进结构和电特性的半导体存储器装置。

[0006] 本发明构思的实施例还可提供制造能够提高集成度以及改进结构和电特性的半导体存储器装置的方法。

[0007] 在一个方面，一种半导体存储器装置可包括：衬底；多个堆叠栅极结构，其沿着与衬底的主表面平行的第一方向彼此间隔开，堆叠栅极结构中的每一个包括交替和重复地堆叠在衬底上的绝缘层和栅电极；多个垂直沟道结构，其穿透堆叠栅极结构中的每一个；以及源极插线，其设置在堆叠栅极结构之间，源极插线与衬底接触，并且沿着与第一方向交叉的第二方向延伸。与源极插线接触的衬底可包括沿着第二方向排列的多个突出区。突出区中的每一个可具有第一宽度，并且突出区可以以大于第一宽度的第一距离彼此间隔开。

[0008] 在另一方面，一种半导体存储器装置可包括：多个堆叠栅极结构，其设置在衬底上，堆叠栅极结构中的每一个包括交替和重复地堆叠在衬底上的绝缘层和栅电极，并且堆叠栅极结构沿着第一方向彼此间隔开；多个垂直沟道结构，其穿透堆叠栅极结构中的每一个；源极插线，其设置在所述多个堆叠栅极结构之间，源极插线包括导电材料并且沿着与第一方向交叉的第二方向延伸；以及公共源极区，其与源极插线接触，并且设置在衬底中。公共源极区可包括沿着第二方向交替地形成的第一掺杂物区和第二掺杂物区。第一掺杂物区可具有第一高度，并且第二掺杂物区可具有第二高度。第一高度可大于第二高度。

[0009] 在另一方面，一种半导体存储器装置可包括：多个垂直沟道结构，其设置在衬底上，并且沿着与衬底垂直的方向延伸；多个堆叠栅极结构，其包围垂直沟道结构，并且包括

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沿着与衬底垂直的方向堆叠的栅电极，堆叠栅极结构沿着平行于衬底的第一方向彼此间隔开；以及公共源极区，其形成在衬底中并包括多个突出区，所述多个突出区沿着与第一方向交叉的第二方向形成在堆叠栅极结构之间。突出区中的每一个可具有在第二方向上的第一宽度，并且突出区可以以大于第一宽度的第一距离彼此间隔开。

[0010] 在另一方面，一种制造半导体存储器装置的方法可包括：形成包括交替和重复地堆叠在衬底上的绝缘层和牺牲层的模制结构；形成穿透模制结构的多个垂直沟道结构；在模制结构中形成沟槽，该沟槽使得垂直沟道结构中的一些与垂直沟道结构中的另一些在平行于衬底的第一方向上隔离，并且沟槽沿着与第一方向交叉的第二方向延伸；在模制结构上形成包括多个桥和固定部分的支撑图案，所述桥沿着第一方向与沟槽交叉并且沿着第二方向彼此间隔开，并且固定部分连接至桥；去除模制结构的牺牲层以形成开口；分别在各开口中形成栅电极；在沟槽的侧壁上形成隔离绝缘图案；在通过沟槽暴露的衬底上形成多个突出区，突出区中的每一个沿着第二方向具有第一宽度，并且突出区沿着第二方向以大于第一宽度的第一距离彼此间隔开；以及在沟槽中形成源极插线，源极插线与所述多个突出区之间的衬底接触并且沿着第二方向延伸。

[0011] 在另一方面，一种制造半导体存储器装置的方法可包括：在衬底上形成多个垂直沟道结构，所述垂直沟道结构沿着与衬底垂直的方向延伸；形成多个堆叠栅极结构，所述多个堆叠栅极结构包围垂直沟道结构并包括沿着与衬底垂直的方向堆叠的栅电极，堆叠栅极结构沿着平行于衬底的第一方向彼此间隔开；以及在所述多个堆叠栅极结构之间的衬底中形成公共源极区。公共源极区可包括沿着与第一方向交叉的第二方向交替地形成的第一掺杂物区和第二掺杂物区。第一掺杂物区可具有第一高度，并且第二掺杂物区可具有小于第一高度的第二高度。

附图说明

[0012] 鉴于附图和随后的详细描述，本发明构思将变得更加清楚。

[0013] 图 1A 是示出根据本发明构思的示例实施例的半导体存储器装置的平面图；

[0014] 图 1B 是示出包括在根据本发明构思的示例实施例的半导体存储器装置中的支撑图案的实施例的平面图；

[0015] 图 2A 和图 2B 分别是沿着图 1A 的线 I-I' 和 II-II' 截取的剖视图，以示出根据本发明构思的示例实施例的半导体存储器装置；

[0016] 图 3A 是图 2A 的部分 'A' 的放大图；

[0017] 图 3B 和图 3C 分别是图 2B 的部分 'B' 和部分 'C' 的放大图；

[0018] 图 4 是示出包括在根据本发明构思的示例实施例的半导体存储器装置中的支撑图案的另一实施例的平面图；

[0019] 图 5A 和图 5B 分别是沿着图 1A 的线 I-I' 和 II-II' 截取的剖视图，以示出根据本发明构思的示例实施例的半导体存储器装置；

[0020] 图 6A 和图 6B 分别是沿着图 1A 的线 I-I' 和 II-II' 截取的剖视图，以示出根据本发明构思的示例实施例的半导体存储器装置；

[0021] 图 7A 和图 7B 分别是沿着图 1A 的线 I-I' 和 II-II' 截取的剖视图，以示出根据本发明构思的示例实施例的半导体存储器装置；

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[0022] 图 8A 和图 8B 分别是图 7B 的部分‘B’和部分‘C’的放大图；

[0023] 图 9、图 10、图 11A、图 12、图 13、图 14A 至图 21A 和图 14B 至图 21B 是示出制造根据本发明构思的示例实施例的半导体存储器装置的方法的一些处理的剖视图；

[0024] 图 11B 是图 11A 的部分‘A’的放大图；

[0025] 图 19C 和图 19D 分别是图 19B 的部分‘B’和部分‘C’的放大图；

[0026] 图 22A 和图 22B 分别是沿着图 1A 的线 I-I’和 II-II’截取的剖视图，以示出制造图 5A 和图 5B 的半导体存储器装置的方法的一些处理；

[0027] 图 23A 和图 23B 分别是沿着图 1A 的线 I-I’和 II-II’截取的剖视图，以示出制造图 6A 和图 6B 的半导体存储器装置的方法的一些处理；

[0028] 图 24A 和图 25A 是沿着图 1A 的线 I-I’截取的剖视图，以示出制造图 7A、图 7B、图 8A 和图 8B 的半导体存储器装置的方法的一些处理；

[0029] 图 24B 和图 25B 是沿着图 1A 的线 II-II’截取的剖视图，以示出制造图 7A、图 7B、图 8A 和图 8B 的半导体存储器装置的方法的一些处理；

[0030] 图 26 是示出包括根据本发明构思的示例实施例的半导体存储器装置的半导体装置系统的示意性框图；以及

[0031] 图 27 是示出包括根据本发明构思的示例实施例的半导体存储器装置的电子系统的示意性框图。

具体实施方式

[0032] 现在，将在下文中参照其中示出了本发明构思的示例性实施例的附图更完全地描述本发明构思。从以下将参照附图更详细地描述的示例性实施例中，本发明构思和实现它们的方法的优点和特征将变得清楚。然而，应该注意，本发明构思不限于以下示例性实施例，并且可按照各种形式实现。因此，提供示例性实施例仅用于公开本发明构思并且使得本领域技术人员知晓本发明构思的类别。在附图中，本发明构思的实施例不限于本文提供的具体示例，并且为了清楚起见进行了夸大。

[0033] 本文使用的术语仅是为了描述特定实施例的目的而非旨在限制本发明。如本文所用，除非上下文清楚地表示不是这样，否则单数形式“一个”、“一”和“该”也旨在包括复数形式。如本文所用，术语“和/或”包括相关所列项之一或多个的任何和所有组合。应该理解，当一个元件被称作“连接”或“耦接”至另一元件时，该元件可直接连接或耦接至所述另一元件，或者可存在中间元件。

[0034] 相似地，应该理解，当诸如层、区或衬底的元件被称作“位于”另一元件“上”时，其可直接位于所述另一元件上或可存在中间元件。相反，术语“直接”意味着不存在中间元件。还应该理解，术语“包括”、“包括……的”、“包含”、和/或“包含……的”当用于本文时，其指明存在所列特征、整体、步骤、操作、元件和/或组件，但不排除存在或添加一个或多个其它特征、整体、步骤、操作、元件、组件和/或它们的组。

[0035] 本文中可使用诸如“在……下方”、“在……之下”、“下”、“在……之上”、“上”等的空间相对术语，以描述附图中所示的一个元件或特征与其他元件或特征的关系。应该理解，空间相对术语旨在涵盖使用或操作中的装置的除图中所示的取向之外的不同取向。例如，如果图中的装置颠倒，则被描述为“在其它元件或特征之下”或“在其它元件或特征下方”的

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元件将因此被取向为“在其它元件或特征之上”。因此，术语“在……之下”可涵盖在……之上和在……之下这两个取向。装置可按照其它方式取向（旋转 90 度或位于其它取向），并且可相应地解释本文所用的空间相对描述语。

[0036] 另外，将通过作为本发明构思的理想示例图的剖视图来描述具体实施方式中的实施例。因此，可根据制造技术和 / 或容许误差修改示例图的形状。因此，本发明构思的实施例不限于示例图中示出的特定形状，而是可包括可根据制造工艺产生的其它形状。图中例示的区域具有一般特性，并且用于示出元件的特定形状。因此，这不应理解为限制本发明构思构思。

[0037] 还应该理解，虽然本文中可使用术语第一、第二、第三等来描述各个元件，但是这些元件不应由这些术语限制。这些术语仅用于将一个元件与另一元件区分开。因此，一些实施例中的第一元件可在其它实施例中被称作第二元件，而不脱离本发明的教导。本文中解释和示出的本发明构思的各方面的示例性实施例包括它们的互补的对应部分。在整个说明书中，相同的附图标记或相同的参考指示符指示相同的元件。

[0038] 而且，本文中参照作为理想化的示例图的剖视图和 / 或平面图描述示例性实施例。因此，作为例如制造技术和 / 或公差的结果，可以预见图中的形状的变化。因此，示例性实施例不应理解为限于本文示出的区的形状，而是包括例如由制造导致的形状的偏差。例如，示为矩形的蚀刻区将通常具有圆形或弯曲特征。因此，图中示出的区实际上是示意性的，并且它们的形状不旨在示出装置的区的实际形状，并且不旨在限制示例实施例的范围。

[0039] 除非另外限定，否则本文中使用的所有术语（包括技术和科学术语）具有与本发明构思所属领域的普通技术人员之一通常理解的含义相同的含义。还应该理解，除非本文中明确这样定义，否则诸如在通用词典中定义的那些的术语应该被解释为具有与它们在相关技术的上下文和本说明书中的含义一致的含义，而不应该理想化地或过于正式地解释它们。

[0040] 如通过本发明的实体的理解，根据本文所述的各个实施例的装置和形成装置的方法可在诸如集成电路的微电子装置中实现，其中根据本文所述的各个实施例的多个装置集成在同一个微电子装置中。因此，本文所示的剖视图可在微电子装置中沿着两个不同方向（不需要是正交的）复制。因此，实现根据本文所述的各个实施例的装置的微电子装置的平面图可基于微电子装置的功能性包括阵列中和 / 或二维图案中的多个装置。

[0041] 根据本文所述的各个实施例的装置可根据微电子装置的功能性散布在其它装置之间。而且，根据本文所述的各个实施例的微电子装置可沿着可与所述两个不同方向正交的第三方向复制，以提供三维集成电路。

[0042] 因此，本文所示的剖视图提供了用于沿着平面图中的两个不同方向和 / 或立体图中的三个不同方向延伸的根据本文所述的各个实施例的多个装置的支撑件。例如，当在装置 / 结构的剖视图中示出单个有源区时，装置 / 结构可包括其上的多个有源区和晶体管结构（或适于该情况的存储器单元结构、栅极结构等），如装置 / 结构的平面图所示。

[0043] 图 1A 是示出根据本发明构思的示例实施例的半导体存储器装置的平面图。图 1B 是示出包括在根据本发明构思的示例实施例的半导体存储器装置中的支撑图案的实施例的平面图。图 2A 和图 2B 分别是沿着图 1A 的线 I-I’ 和 II-II’ 截取的剖视图。图 3A 是图 2A 的部分 ‘A’ 的放大图，并且图 3B 和图 3C 分别是图 2B 的部分 ‘B’ 和部分 ‘C’ 的放大图。

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图 4 是示出包括在根据本发明构思的示例实施例的半导体存储器装置中的支撑图案的另一实施例的平面图。

[0044] 参照图 1A 至图 3C，根据示例实施例的半导体存储器装置可包括堆叠栅极结构 30 和垂直沟道结构 200。堆叠栅极结构 30 可包括交替和重复地堆叠在衬底 100 上的绝缘层 110 和栅电极 172。垂直沟道结构 200 可穿透堆叠栅极结构 30，并且可沿着与衬底 100 的主表面平行的第一方向 D1 彼此间隔开。垂直沟道结构 200 可沿着与衬底 100 的主表面垂直的第三方向 D3 从衬底 100 延伸。衬底 100 可包括半导体材料。例如，衬底 100 可为硅单晶衬底、锗单晶衬底或硅锗单晶衬底。可替换地，衬底 100 可为绝缘体上硅 (SOI) 衬底。例如，衬底 100 可包括设置在绝缘层上的半导体层（例如，硅层、硅锗层或锗层），所述绝缘层保护设置在半导体衬底上的晶体管。衬底 100 可为具有第一导电类型（例如，P 型）的半导体衬底。

[0045] 如图 1A 所示，堆叠栅极结构 30 可具有沿着与第一方向 D1 交叉并且与衬底 100 的主表面平行的第二方向 D2 延伸的直线形状。例如，被包括在堆叠栅极结构 30 中的绝缘层 110 和栅电极 172 可为沿着第二方向 D2 延伸的直线图案。绝缘层 110 可沿着第三方向 D3 堆叠在衬底 100 上。绝缘层 110 的厚度可小于栅电极 172 的厚度。在其它实施例中，绝缘层 110 中的至少一个的厚度可大于栅电极 172 中的每一个的厚度。例如，从衬底 100 开始第二个堆叠的绝缘层 110b、最上面的绝缘层 110d 以及与最上面的绝缘层 110d 直接相邻的绝缘层 110c 可比栅电极 172 厚。在另一些实施例中，绝缘层 110 的厚度可约等于栅电极 172 的厚度。与衬底 100 接触的最下面的绝缘层 110a 可比设置在其上的其它绝缘层 110b、110c 和 110d 更薄。例如，绝缘层 110 中的每一个可包括二氧化硅层。

[0046] 栅电极 172 可沿着第三方向 D3 堆叠，并且可设置在绝缘层 110 之间。栅电极 172 可包括被包括在三维 (3D) 半导体存储器装置（例如，垂直 NAND 闪速存储器装置）中的存储器单元的控制栅电极。例如，设置在最上面的栅电极 172c 与最下面的栅电极 172a 之间的栅电极 172b 可为对应于控制栅电极的字线。控制栅电极 172b 可耦接至垂直沟道结构 200 以形成存储器单元。因此，垂直存储器单元串可设置在衬底 100 上。垂直存储器单元串中的每一个可包括沿着第三方向 D3 排列的存储器单元。

[0047] 最下面的栅电极 172a 和最上面的栅电极 172c 可用作选择晶体管的栅电极。例如，最上面的栅电极 172c 可用作用于对位线（未示出）与垂直沟道结构 200 之间的电连接进行控制的串选择晶体管的栅电极，并且最下面的栅电极 172a 可用作用于对形成在衬底 100 中的公共源极区 154 与垂直沟道结构 200 之间的电连接进行控制的地选择晶体管的栅电极。

[0048] 栅电极 172 可包围垂直沟道结构 200。栅电极 172 中的每一个可包括栅极导电层。栅极导电层可包括金属硅化物层、金属层、金属氮化物层或它们的任何组合。例如，金属硅化物层可包括硅化钴、硅化钛、硅化钨或硅化钽中的至少一个。金属层可包括（但不限于）钨、镍、钴、钛或钽中的至少一个。例如，金属氮化物层可包括氮化钛，氮化钨或氮化钽中的至少一个。

[0049] 垂直沟道结构 200 可穿透堆叠栅极结构 30 中的每一个，以电连接至衬底 100。参照图 1A，耦接至堆叠栅极结构 30 中的每一个的垂直沟道结构 200 可沿着平行于第二方向 D2 的第一列①和第二列②排列。第一列①的第一垂直沟道结构 200a 可沿着第一方向 D1 与第二列②的第二垂直沟道结构 200b 间隔开。第一和第二垂直沟道结构 200 可按照 z 字形

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排列。第一垂直沟道结构 200a 和第二垂直沟道结构 200b 沿着第一方向 D1 不对称。例如，第一垂直沟道结构 200a 可沿着第二方向 D2 分别从第二垂直沟道结构 200b 移位第二垂直沟道结构 200b 的间距的一半。

[0050] 另外，第三列③的第三垂直沟道结构 200c 和第四列④的第四垂直沟道结构 200d 还可耦接至堆叠栅极结构 30 中的每一个。第三垂直沟道结构 200c 和第四垂直沟道结构 200d 可沿着第一方向 D1 设置在第一垂直沟道结构 200a 和第二垂直沟道结构 200b 的一侧。第一垂直沟道结构 200a 和第二垂直沟道结构 200c 可关于第二列②对称。第二垂直沟道结构 200b 和第四垂直沟道结构 200d 可关于第三列③对称。包括沿着四列排列的垂直沟道结构 200 的组可沿着第一方向 D1 重复地设置。当从平面图中看时，公共源极线（即源极插线）182 可设置在彼此相邻的组之间。然而，本发明构思不限于沿着四列排列的垂直沟道结构 200。在其它实施例中，垂直沟道结构 200 可沿着数量不为四的多列排列。例如，列数可为二或可大于或等于五。

[0051] 垂直沟道结构 200 可穿透多个栅电极 172。栅电极 172 可包围垂直沟道结构 200。垂直沟道结构 200 中的每一个可包括第一垂直沟道图案 128、数据存储图案 130、第二垂直沟道图案 140 和填充绝缘图案 144。数据存储图案 130、第二垂直沟道图案 140 和填充绝缘图案 144 可设置在第一垂直沟道图案 128 上。

[0052] 第一垂直沟道图案 128 可延伸至衬底 100 中。第一垂直沟道图案 128 的一部分可设置在衬底 100 中，第一垂直沟道图案 128 的另一部分可具有从衬底 100 垂直地突出的柱形。第一垂直沟道图案 128 可设置在堆叠栅极结构 30 的下部分中。例如，第一垂直沟道图案 128 的顶表面可高于与衬底 100 相邻的最下面的栅电极 172a 的顶表面（例如，地选择晶体管的栅电极的顶表面）。第一垂直沟道图案 128 可包括半导体材料。例如，第一垂直沟道图案 128 可包括硅 (Si)、锗 (Ge)、硅锗 (SiGe)、III-V 族化合物或 II-VI 族化合物中的至少一个。例如，第一垂直沟道图案 128 可为包括单晶硅的外延层。第一垂直沟道图案 128 可包括未掺杂的半导体材料，或掺杂有导电类型与衬底 100 的导电类型相同的掺杂物的半导体材料。

[0053] 可在第一垂直沟道图案 128 的侧壁上设置栅极氧化物层 164。栅极氧化物层 164 可设置在最下面的栅电极 172a 与第一垂直沟道图案 128 之间。

[0054] 沿着第三方向 D3 延伸的第二垂直沟道图案 140 可设置在第一垂直沟道图案 128 上。第二垂直沟道图案 140 可电连接至第一垂直沟道图案 128。第二垂直沟道图案 140 可设置在数据存储图案 130 与填充绝缘图案 144 之间。第二垂直沟道图案 140 可具有顶端敞开的中空的通心粉形状。在一些实施例中，第二垂直沟道图案 140 可具有带敞开的顶端和底端的管状。在其它实施例中，第二垂直沟道图案 140 可具有填充的圆柱形形状，并且可省略填充绝缘图案 144。第二垂直沟道图案 140 可包括多晶半导体材料、非晶半导体材料或单晶半导体材料。例如，第二垂直沟道图案 140 可包括硅 (Si)、锗 (Ge)、硅锗 (SiGe)、III-V 族化合物或 II-VI 族化合物中的至少一个。例如，第二垂直沟道图案 140 可为包括单晶硅的外延层。例如，第二垂直沟道图案 140 可包括未掺杂的半导体材料、半导体材料、或者掺杂有导电类型与衬底 100 的导电类型相同的掺杂物的多晶硅。

[0055] 数据存储图案 130 可设置在堆叠栅极结构 30 和第二垂直沟道图案 140 之间。数据存储图案 130 可具有开口顶端和底端。数据存储图案 130 可包括能够存储数据的薄层。

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例如，可利用通过垂直沟道结构 200 与栅电极 172 之间的电压差导致的 Fowler-Nordheim 隧穿效应改变存储在数据存储图案 130 中的数据。然而，本发明构思不限于此。可替换地，数据存储图案 130 可具有能够基于另一操作原理存储数据的薄层（例如，用于相变存储器装置的薄层或用于可变电阻存储器装置的薄层）。

[0056] 参照图 3A，数据存储图案 130 可包括与栅电极 172 相邻的第一阻挡介电层 132、与第二垂直沟道图案 140 相邻的隧道介电层 136 和设置在第一阻挡介电层 132 与隧道介电层 136 之间的电荷存储层 134。例如，隧道介电层 136 可包括二氧化硅层。电荷存储层 134 可包括陷阱介电层（trap dielectric layer）或者具有导电纳米点的介电层。例如，陷阱介电层可包含氮化硅层。第一阻挡介电层 132 可包括二氧化硅层和 / 或高 k 介电层（例如，氧化铝层或二氧化铪层）。第一阻挡介电层 132 可包括单层或多个薄层。在一些实施例中，第一阻挡介电层 132 可为具有二氧化硅层的单层。在其它实施例中，第一阻挡介电层 132 可包括包含二氧化硅层、氧化铝层或二氧化铪层中的至少两个的多个薄层。

[0057] 可额外在堆叠栅极结构 30 与第二垂直沟道图案 140 之间设置第二阻挡介电层 168，并且第二阻挡介电层 168 可在绝缘层 110 与栅电极 172 之间延伸。例如，第二阻挡介电层 168 可沿着相对于衬底 100 基本水平的方向延伸，以覆盖栅电极 172 的顶表面和底表面。例如，第二阻挡介电层 168 可为单层或多层。例如，第二阻挡介电层 168 可包括高 k 介电层（例如，氧化铝层和 / 或二氧化铪层）。在一些实施例中，可不形成第二阻挡介电层 168。

[0058] 填充绝缘图案 144 可填充垂直沟道结构 200 的内空间。填充绝缘图案 144 可包括二氧化硅层或氮化硅层。

[0059] 可在垂直沟道结构 200 中的每一个上设置导电焊盘 146。导电焊盘 146 可包括导电材料。可替换地，导电焊盘 146 可为掺杂有掺杂物的掺杂物区。垂直沟道结构 200 的与导电焊盘 146 接触的一端可为漏极区。可在堆叠栅极结构 30 上设置焊盘保护层 148 以覆盖导电焊盘 146。

[0060] 可在堆叠栅极结构 30 之间设置第一沟槽 150 以将堆叠栅极结构 30 彼此分离。例如，第一沟槽 150 可形成在各自包括沿着第一方向 D1 布置的四列的垂直沟道结构 200 的组之间。第一沟槽 150 可从焊盘保护层 148 的顶表面延伸至衬底 100 中。因此，第一沟槽 150 可包括延伸至衬底 100 中的凹进区 150R。当形成第一沟槽 150 时，可将衬底 100 过度蚀刻以形成凹进区 150R。凹进区 150R 可具有正向倾斜的侧壁。

[0061] 可在凹进区 150R 中设置缓冲氧化物层 166。例如，缓冲氧化物层 166 可形成在凹进区 150R 的侧壁和底表面上。缓冲氧化物层 166 和栅极氧化物层 164 可通过相同的氧化工艺同时形成。第二阻挡介电层 168 还可设置在缓冲氧化物层 166 上。第二阻挡介电层 168 可保形地形成在凹进区 150R 中。

[0062] 公共源极区 154 可形成在衬底 100 中，并且可包围凹进区 150R。换句话说，当从平面图看时，公共源极区 154 可设置在堆叠栅极结构 30 之间。例如，公共源极区 154 可在通过第一沟槽 150 暴露的衬底 100 中沿着第二方向 D2 延伸。换句话说，当从平面图看时，公共源极区 154 可设置在堆叠栅极结构 30 之间，以沿着第二方向 D2 延伸。公共源极区 154 可包括与衬底 100 的第一导电类型不同的第二导电类型的掺杂物。例如，公共源极区 154 可包括诸如砷（As）或磷（P）的 N 型掺杂物。公共源极区 154 可包括第一掺杂物区 154a 和第二掺杂物区 154b。例如，第一掺杂物区 154a 可为低浓度掺杂物区，第二掺杂物区 154b 可为

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高浓度掺杂物区。例如，第一掺杂物区 154a 的掺杂物浓度的范围可为约 10^{14}atoms/cm^{3}至约 10^{17}atoms/cm^3，并且第二掺杂物区 154b 的掺杂物浓度的范围可为约 10^{19}atoms/cm^{3}至约 10^{21}atoms/cm^3。

[0063] 参照图 2B 和图 3B，其中形成有公共源极区 154 的衬底 100 可包括沿着第二方向 D2 排列的多个突出区 100a。突出区 100a 可具有顶表面，该顶表面设置为与设置在突出区 100a 之间的衬底 100 的顶表面相距高度 PH。换句话说，突出区 100a 可具有高度 PH。例如，突出区 100a 可沿着第二方向 D2 以距离 PL 彼此间隔开，并且突出区 100a 中的每一个可具有沿着第二方向 D2 的宽度 PW。在一些实施例中，距离 PL 可为宽度 PW 的几倍至几十倍大。形成在包括突出区 100a 的衬底 100 中的公共源极区 154 可包括突出公共源极区 CSP 和凹进公共源极区 CSR。可将突出公共源极区 CSP 限定为形成在突出区 100a 和突出区 100a 下方的衬底 100 中的掺杂物区。可将凹进公共源极区 CSR 中的每一个限定为形成在设置在突出区 100a 之间的衬底 100 中的掺杂物区。因此，突出公共源极区 CSP 中的每一个沿着第二方向 D2 可具有宽度 PW，并且突出公共源极区 CSP 可沿着第二方向 D2 以与凹进公共源极区 CSR 的宽度基本对应的距离 PL 彼此间隔开。突出公共源极区 CSP 可包括第一掺杂物区 154a，并且凹进公共源极区 CSR 可包括第一掺杂物区 154a 和第二掺杂物区 154b。第二掺杂物区 154b 可延伸至突出公共源极区 CSP 的一部分中。公共源极区 154 的第一掺杂物区 154a 可沿着第二方向 D2 连续延伸。第二掺杂物区 154b 可沿着第二方向 D2 不连续地排列。例如，沿着第二方向 D2 排列的第二掺杂物区 154b 可彼此间隔开。第一掺杂物区 154a 可包括具高度彼此不同的区。例如，第一掺杂物区 154a 可具有沿着第二方向 D2 交替排列的第一区和第二区。第一区具有第一高度，并且第二区具有与第一高度不同的第二高度。在一些实施例中，第一掺杂物区 154a 在突出公共源极区 CSP 中的每一个中可具有第一高度 SH1，并且在凹进公共源极区 CSR 中的每一个中可具有第二高度 SH2。第一高度 SH1 可大于第二高度 SH2。第二掺杂物区 154b 可形成在第一掺杂物区 154a 中。然而，本发明构思不限于此。在其它实施例中，第二掺杂物区 154b 可穿透第一掺杂物区 154a，并且可延伸至衬底 100 中。

[0064] 包括下隔离绝缘图案 180a 的绝缘层可设置在突出公共源极区 CSP 中的每一个上。例如，缓冲氧化物层 166、第二阻挡介电层 168 和下隔离绝缘图案 180a 可按顺序堆叠在衬底 100 的突出区 100a 上。下隔离绝缘图案 180a、第二阻挡介电层 168 和缓冲氧化物层 166 的侧壁可与突出区 100a 的侧壁基本对齐。因此，下隔离绝缘图案 180a、第二阻挡介电层 168 和缓冲氧化物层 166 的宽度（例如，PW）可沿着第二方向 D2 彼此基本相同或相似。另外，分别设置在突出区 100a 上的各下隔离绝缘图案 180a（或各第二阻挡介电层 168 或各缓冲氧化物层 166）可以按与距离 PL 基本相同或相似的距离彼此间隔开。

[0065] 如图 2A 所示，下隔离绝缘图案 180a 和隔离绝缘图案 180 可构成一个联合主体，并且下隔离绝缘图案 180a 可对应于隔离绝缘图案 180 的底部。下隔离绝缘图案 180a 可填充凹进区 150R 的至少一部分，并且可设置在第一掺杂物区 154a 上。设置在下隔离绝缘图案 180a 下方的缓冲氧化物层 166 和第二阻挡介电层 168 可设置在凹进区 150R 中。

[0066] 隔离绝缘图案 180 可设置在堆叠栅极结构 30 与源极插线（plug line）182 之间。例如，隔离绝缘图案 180 可设置在源极插线 182 与栅电极 172 之间。隔离绝缘图案 180 可部分地填充第一沟槽 150 和凹进区 150R，并且可与栅电极 172 接触。隔离绝缘图案 180 可填充形成在绝缘层 110 之间的空间，以保护栅电极 172 的侧壁。狭缝形开口可穿透隔离绝

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缘图案 180，并且源极插线 182 可设置在狭缝形开口中。在第二方向 D2 上，隔离绝缘图案 180 的一部分可保留，以作为衬底 100 上的下隔离绝缘图案 180a，并且隔离绝缘图案 180 的另一部分可与其它绝缘层（例如，缓冲氧化物层 166 和第二阻挡介电层 168）一起被去除，以暴露出公共源极区 154。隔离绝缘图案 180 可包括氮化物层、氧氮化物层或氧化物层。

[0067] 源极插线 182 可设置在公共源极区 154 上。源极插线 182 可设置在第一沟槽 150 中。另外，源极插线 182 可延伸至凹进区 150R 中，以连接至公共源极区 154。源极插线 182 可降低公共源极区 154 的电阻。源极插线 182 可为沿着第二方向 D2 连续延伸的线形图案。源极插线 182 可穿透第二阻挡介电层 168 和缓冲氧化物层 166，以连接至公共源极区 154。源极插线 182 的底表面的一部分可与公共源极区 154 接触，并且源极插线 182 的另一部分可与公共源极区 154 分离并和间隔开。例如，源极插线 182 可与凹进公共源极区 CSR 的顶表面接触，并且可通过多个绝缘层 180a、168 和 166 与突出公共源极区 CSP 的顶表面间隔开。源极插线 182 可与突出公共源极区 CSP 的侧壁的一部分接触。换句话说，源极插线 182 的底表面的一部分可与下隔离绝缘图案 180a 直接接触，并且源极插线 182 的底表面的另一部分可与公共源极区 154 的第二掺杂物区 154b 直接接触。源极插线 182 可包括导电材料。例如，源极插线 182 可包括势垒层 182a 和导电层 182b。例如，势垒层 182a 可与第二掺杂物区 154b 接触，并且可包围导电层 182b 的侧壁和底表面。

[0068] 势垒层 182a 可包括金属和金属氮化物中的至少一个。例如，势垒层 182a 可包括钛 (Ti)、钽 (Ta)、氮化钛 (TiN)、氮化钨 (WN)、氮化钽 (TaN) 或它们的任何组合中的至少一个。例如，导电层 182b 可包括诸如钨或铜的金属。硅化物层（未示出）可形成在源极插线 182 与公共源极区 154 之间。

[0069] 支撑图案 160 可设置在堆叠栅极结构 30 上。在一些实施例中，跨越源极插线 182 的支撑图案 160 可设置在焊盘保护层 148 上。如图 1A 所示，支撑图案 160 可包括设置在堆叠栅极结构 30 上的固定部分 160b 和将固定部分 160b 彼此连接的多个桥 160a。固定部分 160b 可防止堆叠栅极结构 30 倾斜。桥 160a 中的每一个沿着第二方向 D2 可具有宽度 BW。例如，宽度 BW 可与突出区 100a 的宽度 PW 基本相同或相似。桥 160a 可沿着第二方向 D2 通过例如与突出区 100a 之间的距离 PL 基本相同或相似的距离 BL 彼此间隔开。因此，沿着第二方向 D2 具有宽度 BL 的第二沟槽 162 可设置在支撑图案 160 中。第二沟槽 162 可具有狭缝形。在第一方向 D1 上，第二沟槽 162 的宽度可大于第一沟槽 150 的宽度。第二沟槽 162 和第一沟槽 150 的宽度之间的差可为图 1A 中所述的距离 S 的两倍。因此，源极插线 182 可填充桥 160a 之间的第二沟槽 162，并且源极插线 182 的填充第二沟槽 162 的沿第一方向 D1 的宽度可大于源极插线 182 的设置在桥 160a 下方的宽度。桥 160a 可在源极插线 182 上沿着第一方向 D1 与源极插线 182 交叉。

[0070] 在一些实施例中，桥 160a 可按照 z 字形排列，如图 1B 所示。例如，沿着第一方向 D1 彼此邻近的桥 160a 可不对称。因此，邻近的公共源极区 154 的突出区 100a 可不对称，但是可沿着第一方向 D1 按照 z 字形排列。在一些实施例中，支撑图案 160 可具有沿着第一方向 D1 延伸的直线形状，如图 4 所示。支撑图案 160 可包括沿着第二方向 D2 排列的多个桥 160a 和从桥 160a 延伸至堆叠栅极结构 30 上的多个固定部分 160b。桥 160a 和固定部分 160b 可将堆叠栅极结构 30 彼此连接。固定部分 160b 可与桥 160a 具有相同的直线形状。然而，本发明构思不限于此。在其它实施例中，固定部分 160b 的宽度可大于桥 160a 的宽度，

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或者可具有各种形状。桥 160a 中的每一个沿着第二方向 D2 可具有宽度 BW。桥 160a 可沿着第二方向 D2 以距离 BL 彼此间隔开。支撑图案 160 可包括氧化物层、氮化物层、氧氮化物层、未掺杂的多晶硅层或它们的任何组合中的至少一个。可利用化学气相沉积 (CVD) 工艺或原子层沉积 (ALD) 工艺形成支撑图案 160。

[0071] 上层间绝缘层 186 可设置在支撑图案 160 上。上层间绝缘层 186 可包括氧化物层、氧氮化物层或氮化物层。漏极触点 190 可设置在穿透上层间绝缘层 186、支撑图案 160 和焊盘保护层 148 的漏极接触孔 188 中。漏极触点 190 可连接至导电焊盘 146。漏极触点 190 可连接至位线 (未示出)。漏极触点 190 可包括诸如金属、金属氮化物或掺杂有掺杂物的多晶硅的导电材料。

[0072] 根据实施例的半导体存储器装置的支撑图案 160 可防止栅电极 172 由于栅电极 172 的形状的非均匀性而沿着第一方向 D1 倾斜。例如，如图 1A 和图 2A 所示，栅电极 172 可能被图案化为使得从堆叠栅极结构 30 的左侧壁至最靠近左侧壁的第一列①的第一垂直沟道结构 200a 的距离 T1 大于从堆叠栅极结构 30 的右侧壁至最靠近右侧壁的第四列④的第四垂直沟道结构 200d 的距离 T2。在这种情况下，位于第一列①的第一垂直沟道结构 200a 的左侧的栅电极 172 的总量可能会大于位于第四列④的第四垂直沟道结构 200d 的右侧的栅电极 172 的总量。堆叠栅极结构 30 的平衡会由于栅电极 172 的左右非对称量而打破，从而堆叠栅极结构 30 会倾斜。随着堆叠的栅电极 172 的数量增加，堆叠栅极结构 30 的倾斜现象会变得更加严重。因此，可提供支撑图案 160 以防止堆叠栅极结构 30 的倾斜现象。可通过支撑图案 160 的桥 160a 防止堆叠栅极结构 30 的倾斜现象，从而防止导电焊盘 146 与漏极触点 190 之间的不良连接和源极插线 182 与公共源极区 154 之间的不良连接。因此，可提高半导体存储器装置的结构稳定性和电可靠性。

[0073] 图 5A 和图 5B 分别是沿着图 1A 的线 I-I' 和 II-II' 截取的剖视图，以示出根据本发明构思的示例实施例的半导体存储器装置。下文中，将省略或简单描述如参照图 1A 至图 4 描述的对相同元件的描述。换句话说，将主要描述当前实施例与前述实施例之间的差异。

[0074] 参照图 1A、图 5A 和图 5B，根据示例实施例的半导体存储器装置可包括上层间绝缘层 186，其设置在焊盘保护层 148 上，并覆盖源极插线 182。例如，上层间绝缘层 186 可设置在通过选择性地去除参照图 1A 至图 4 描述的半导体存储器装置的支撑图案 160 而形成的结构上。因此，上层间绝缘层 186 可与焊盘保护层 148 接触，并且可填充通过去除支撑图案 160 的桥 160a 形成的桥凹槽区 184。另外，上层间绝缘层 186 可覆盖源极插线 182。桥凹槽区 184 可沿着第二方向 D2 排列在源极插线 182 上。因此，源极插线 182 的顶表面可不为平坦的。在一些实施例中，可去除设置在源极插线 182 的侧壁的上部上的隔离绝缘图案 180 和第二阻挡介电层 168。当从平面图看时，衬底 100 的桥凹槽区 184、下隔离绝缘图案 180a 和突出区 100a 可基本彼此重叠。换句话说，衬底 100 的桥凹槽区 184、下隔离绝缘图案 180a 和突出区 100a 可基本彼此垂直地重叠。例如，桥凹槽区 184 的侧壁、下隔离绝缘图案 180a 的侧壁和突出区 100a 的侧壁可基本彼此对齐。源极插线 182 的底表面的一部分可与设置在衬底 100 的突出区 100a 上的下隔离绝缘图案 180a 接触。源极插线 182 的底表面的另一部分可与第二掺杂物区 154b 接触，并且可沿着第二方向 D2 延伸。缓冲氧化物层 166 和第二阻挡介电层 168 可设置在下隔离绝缘图案 180a 与突出区 100a 之间。

[0075] 图 6A 和图 6B 分别是沿着图 1A 的线 I-I' 和 II-II' 截取的剖视图，以示出根据本

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发明构思的示例实施例的半导体存储器装置。下文中，将省略或简单描述如参照图 1A 至图 4 描述的对相同元件的描述。换句话说，将主要描述当前实施例与前述实施例之间的差异。

[0076] 参照图 1A、图 6A 和图 6B，在根据示例实施例的半导体存储器装置中，上层间绝缘层 186 可设置在焊盘保护层 148 和具有平坦顶表面的源极插线 182 上。例如，可通过不在源极插线 182 的上部中形成图 5A 和图 5B 的桥凹槽区 184 的方式来使得源极插线 182 平坦化。因此，源极插线 182 的顶表面可与焊盘保护层 148 的顶表面基本共面。源极插线 182 的底表面的一部分可与设置在衬底 100 的突出区 100a 上的下隔离绝缘图案 180a 接触。源极插线 182 的底表面的另一部分可与第二掺杂物区 154b 接触，并且可沿着第二方向 D2 延伸。缓冲氧化物层 166 和第二阻挡介电层 168 可设置在下隔离绝缘图案 180a 与突出区 100a 之间。

[0077] 图 7A 和图 7B 分别是沿着图 1A 的线 I-I' 和 II-II' 截取的剖视图，以示出根据本发明构思的示例实施例的半导体存储器装置。图 8A 和图 8B 分别是图 7B 的部分 'B' 和部分 'C' 的放大图。下文中，将省略或简单描述如参照图 1A 至图 4 描述的对相同元件的描述。换句话说，将主要描述当前实施例与前述实施例之间的差异。

[0078] 参照图 1A、图 7A、图 7B、图 8A 和图 8B，根据示例实施例的半导体存储器装置可包括具有平坦化的顶表面的源极插线 182 和与源极插线 182 的整个底表面接触的公共源极区 154。例如，可去除图 6A 和图 6B 的下隔离绝缘图案 180a、第二阻挡介电层 168 和缓冲氧化物层 166，并且源极插线 182 的底表面可与其中形成有公共源极区 154 的突出区 100a 直接接触。突出区 100a 可具有高度 PH'。因此，源极插线 182 可沿着第二方向 D2 延伸，并且可与沿着第二方向 D2 排列的突出区 100a 和突出区 100a 之间的衬底 100 接触。形成在包括突出区 100a 的衬底 100 中的突出公共源极区 CSP' 可包括具有低浓度的第一掺杂物区 154a 和具有高浓度的第二掺杂物区 154b。另外，形成在突出区 100a 之间的衬底 100 中的凹进公共源极区 CSR' 还可包括具有低浓度的第一掺杂物区 154a 和具有高浓度的第二掺杂物区 154b。例如，高浓度的第二掺杂物区 154b 可由低浓度的第一掺杂物区 154a 包围。第一掺杂物区 154a 可包括高度彼此不同的区。第一掺杂物区 154a 可具有沿着第二方向 D2 交替排列的第一区和第二区。第一区具有高度 SH1，第二区具有与高度 SH1 不同的高度 SH2。例如，第一掺杂物区 154a 在突出公共源极区 CSP' 中的每一个中可具有高度 SH1，并且在凹进公共源极区 CSR' 中的每一个中可具有高度 SH2。高度 SH1 可大于高度 SH2。第二掺杂物区 154b 可形成在第一掺杂物区 154a 中。然而，本发明构思不限于此。在其它实施例中，第二掺杂物区 154b 可穿透第一掺杂物区 154a，以延伸至衬底 100 中。在一些实施例中，突出区 100a 可沿着第一方向 D1 按照 z 字形排列。另外，公共源极区 154 的突出公共源极区 CSP' 沿着第一方向 D1 可不对称，并且可沿着第一方向 D1 按照 z 字形排列。源极插线 182 可沿着第二方向 D2 延伸以与具有高浓度的第二掺杂物区 154b 直接接触，并且形成在包括沿着第二方向 D2 排列的突出区 100a 的衬底 100 中。

[0079] 图 9、图 10、图 11A、图 12、图 13、图 14A 至图 21A 和图 14B 至图 21B 是示出制造根据本发明构思的示例实施例的半导体存储器装置的方法的一些处理的剖视图。图 9、图 10、图 11A、图 12、图 13 和图 14A 至图 21A 是对应于图 1A 的线 I-I' 的剖视图，并且图 14B 至图 21B 是对应于图 1A 的线 II-II' 的剖视图。图 11B 是图 11A 的部分 'A' 的放大图。图 19C 和图 19D 分别是图 19B 的部分 'B' 和部分 'C' 的放大图。

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[0080] 参照图 9，模制结构 10 可形成在衬底 100 上。例如，模制结构 10 可包括交替和重复地堆叠在衬底 100 上的绝缘层 110 和牺牲层 112。在一些实施例中，绝缘层 110 和牺牲层 112 中的每一个可包括多个层。

[0081] 衬底 100 可包括半导体材料。例如，衬底 100 可为硅单晶衬底、锗单晶衬底或硅锗单晶衬底。可替换地，衬底 100 可为绝缘体上硅 (SOI) 衬底。例如，衬底 100 可包括设置在对设置在半导体衬底上的晶体管进行保护的绝缘层上的半导体层（例如，硅层、硅锗层或锗层）。衬底 100 可包括具有第一导电类型（例如，P 型）的掺杂物区。

[0082] 牺牲层 112 可由相对于绝缘层 110 具有蚀刻选择性的材料形成。例如，在利用化学溶液的湿蚀刻工艺中，牺牲层 112 的蚀刻率可高于绝缘层 110 的蚀刻率。例如，绝缘层 110 中的每一个可为二氧化硅层或氮化硅层，并且牺牲层 112 中的每一个可为二氧化硅层、氮化硅层、碳化硅层、硅层或硅锗层之一。此时，牺牲层 112 由相对于绝缘层 110 具有蚀刻选择性的材料形成。在一些实施例中，绝缘层 110 可为二氧化硅层，并且牺牲层 112 可为氮化硅层。

[0083] 可利用热 CVD 工艺，等离子体增强的 CVD 工艺或 ALD 工艺形成绝缘层 110 和牺牲层 112。

[0084] 牺牲层 112 的厚度可彼此相等。在其它实施例中，与衬底 100 接触的绝缘层 110a 可为通过热氧化工艺或沉积工艺形成的二氧化硅层，并且绝缘层 110a 的厚度可小于其它绝缘层 110b、110c 和 110d 的厚度。在另一些实施例中，从衬底 100 开始第二个堆叠的绝缘层 110b、最上面的绝缘层 110d 和直接与最上面的绝缘层 110d 相邻的绝缘层 110c 可比其它绝缘层 110c 或牺牲层 112 更厚。

[0085] 参照图 10，沟道孔 124 可形成为穿透模制结构 10。沟道孔 124 可暴露衬底 100。

[0086] 可通过各向异性地蚀刻模制结构 10 形成沟道孔 124。沟道孔 124 可与图 1A 所示的垂直沟道结构 200 按照相同形式排列。例如，沿着平行于第二方向 D2 的四列排列的沟道孔 124 可构成一组，并且多个组可设置为沿着第一方向 D1 彼此间隔开。本发明构思不限于四列沟道孔 124。在其它实施例中，沟道孔 124 可沿着两列或五列或更多列排列。当形成沟道孔 124 时，可将衬底 100 过度蚀刻以形成凹进区。例如，凹进区的深度的范围可为 10nm 至 200nm。

[0087] 参照图 11A 和图 11B，垂直沟道结构 200 可形成在衬底 100 上。垂直沟道结构 200 可穿透模制结构 10，并且可沿着第三方向 D3 延伸。各垂直沟道结构 200 可分别填充沟道孔 124。另外，垂直沟道结构 200 可延伸至衬底 100 中（例如，设置在沟道孔 124 下方的凹进区）。垂直沟道结构 200 中的每一个可包括第一垂直沟道图案 128、数据存储图案 130、第二垂直沟道图案 140 和填充绝缘图案 144。第一垂直沟道图案 128 可填充凹进区，并且可像柱形那样从衬底 100 垂直地突出。第一垂直沟道图案 128 可填充沟道孔 124 中的每一个的下部分。例如，第一垂直沟道图案 128 可突出，以与模制结构 10 的最下面的绝缘层 110a 和最下面的牺牲层 112a 的侧壁接触。另外，第一垂直沟道图案 128 还可突出，以覆盖从衬底 100 开始第二个堆叠的绝缘层 110b 的侧壁的一部分。例如，第一垂直沟道图案 128 的顶表面可比从衬底 100 开始第二个堆叠的绝缘层 110b 的顶表面更低。第一垂直沟道图案 128 可包括半导体材料。例如，第一垂直沟道图案 128 可包括硅 (Si)、锗 (Ge)、硅锗 (SiGe)、III-V 族化合物或 II-VI 族化合物中的至少一个。例如，第一垂直沟道图案 128 可包括通过选择

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性外延生长 (SEG) 工艺形成的半导体材料。第一垂直沟道图案 128 可包括其导电类型与衬底 100 的导电类型相同的掺杂物。例如，在 SEG 工艺中，第一垂直沟道图案 128 可原位掺杂掺杂物。可替换地，第一垂直沟道图案 128 可通过离子注入工艺掺杂掺杂物。

[0088] 接着，穿透模制结构 10 的数据存储图案 130、第二垂直沟道图案 140 和填充绝缘图案 144 可形成在第一垂直沟道图案 128 上。

[0089] 数据存储图案 130 可覆盖沟道孔 124 的内侧壁。例如，数据存储图案 130 在沟道孔 124 的内侧壁上可具有间隔件形状，并且可从沟道孔 124 的顶端延伸至第一垂直沟道图案 128 的顶表面。例如，数据存储图案 130 可具有敞开的顶端和底端。数据存储图案 130 可与模制结构 10 的绝缘层 110 和牺牲层 112 接触。数据存储图案 130 可包括能够存储数据的薄层。例如，数据存储图案 130 可包括能够利用 Fowler-Nordheim 隧穿效应来存储数据的薄层。然而，本发明构思不限于此。可替换地，数据存储图案 130 可具有能够基于另一操作原理存储数据的薄层（例如，用于相变存储器装置的薄层或用于可变电阻存储器装置的薄层）。数据存储图案 130 可由多个薄层形成。

[0090] 例如，数据存储图案 130 可包括第一阻挡介电层 132、电荷存储层 134 和隧道介电层 136，如图 11B 所示。例如，第一阻挡介电层 132、电荷存储层 134 和隧道介电层 146 可按顺序形成在沟道孔 124 的内侧壁上。第一阻挡介电层 132 可包括二氧化硅层和 / 或高 k 介电层（例如，氧化铝层或二氧化铪层）。第一阻挡介电层 132 可包括单层或多个薄层。在一些实施例中，第一阻挡介电层 132 可为由二氧化硅层形成的单层。在其它实施例中，第一阻挡介电层 132 可包括具有二氧化硅层、氧化铝层和 / 或二氧化铪层中的至少两个的多个薄层。

[0091] 电荷存储层 134 可包括陷阱介电层或具有导电纳米点的介电层。例如，陷阱介电层可包括氮化硅层。例如，隧道介电层 136 可包括二氧化硅层。可利用等离子体增强的 CVD 工艺或 ALD 工艺形成第一阻挡介电层 132 和电荷存储层 134。可利用等离子体增强 CVD 工艺、ALD 工艺或热氧化工艺形成隧道介电层 136。隧道介电层 136 可与第二垂直沟道图案 140 接触。

[0092] 第二垂直沟道图案 140 可电连接至第一垂直沟道图案 128，并且可与数据存储图案 130 接触。第二垂直沟道图案 140 可保形地形成在沟道孔 124 中，以具有直线形状。第二垂直沟道图案 140 可沿着第三方向 D3 延伸。第二垂直沟道图案 140 可具有带开口顶端的中空的通心粉形状。在一些实施例中，第二垂直沟道图案 140 的顶端和底端可敞开。在其它实施例中，第二垂直沟道图案 140 可具有填充沟道孔 124 而不具有填充绝缘图案 144 的圆柱形。第二垂直沟道图案 140 可包括半导体材料。例如，第二垂直沟道图案 140 可包括多晶半导体材料、非晶半导体材料或单晶半导体材料。例如，第二垂直沟道图案 140 可包括硅 (Si)、锗 (Ge)、硅锗 (SiGe)、砷化镓 (GaAs)、III-V 族化合物、II-VI 族化合物或它们的任何混合物中的至少一个。第二垂直沟道图案 140 可包括未掺杂的半导体材料或掺杂有其导电类型与衬底 100 的导电类型相同的掺杂物的半导体材料。可利用 ALD 工艺、CVD 工艺或外延生长工艺形成第二垂直沟道图案 140。

[0093] 可形成填充绝缘图案 144 以填充具有第二垂直沟道图案 140 的沟道孔 124。填充绝缘图案 144 可包括二氧化硅层或氮化硅层。还可在形成填充绝缘图案 144 之前执行氢退火工艺，从而固化可能存在于第二垂直沟道图案 140 中的晶体缺陷。

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[0094] 导电焊盘 146 可分别形成在垂直沟道结构 200 上。例如，垂直沟道结构 200 中的每一个的上部可凹进，随后，凹进区可填充有导电材料以形成导电焊盘 146。可替换地，可通过将掺杂物注射至第二垂直沟道图案 140 中形成导电焊盘 146。漏极区可形成在设置在导电焊盘 146 下方的第二垂直沟道图案 140 中。焊盘保护层 148 可形成在导电焊盘 146 和最上面的绝缘层 110d 上。

[0095] 参照图 12，可将模制结构 10 图案化，以在彼此相邻的垂直沟道结构 200 之间形成第一沟槽 150。第一沟槽 150 可暴露出衬底 100。公共源极区的第一掺杂物区 154a 可形成在通过第一沟槽 150 暴露的衬底 100 中。例如，模制结构 10 可被各向异性地蚀刻，以形成第一沟槽 150。例如，第一沟槽 150 可形成在各自包括沿着与第二方向 D2 平行的四列排列的垂直沟道结构 200 的各个组之间。在其它实施例中，第一沟槽 150 可形成在各自包括沿着两列或五列或更多列排列的垂直沟道结构 200 的各个组之间。第一沟槽 150 可沿着第二方向 D2 延伸。图 11A 的模制结构 10 可通过第一沟槽 150 被划分为多个模制结构 10，如图 12 所示。当形成第一沟槽 150 时，可将衬底 100 过度蚀刻以形成凹进区 150R。例如，凹进区 150R 的深度范围可为 5nm 至 150nm。凹进区 150R 可具有正向倾斜的侧壁。第一掺杂物区 154a 可形成为包围凹进区 150R。第一掺杂物区 154a 可包围凹进区 150R 的侧壁和底表面。第一掺杂物区 154a 可包括与衬底 100 的第一导电类型不同的第二导电类型（例如，N 型）的掺杂物。第一掺杂物区 154a 可为低浓度掺杂物区。例如，可将 N 型掺杂物离子（例如，砷 (As) 离子或磷 (P) 离子）以约 10KeV 至约 40KeV 的能量和约 10^{12}atoms/cm^2至约 10^{13}atoms/cm^2的剂量注入衬底 100 中，从而形成第一掺杂物区 154a。

[0096] 参照图 13，牺牲填充图案 158 可形成在第一沟槽 150 中。例如，牺牲填充层可形成在焊盘保护层 148 上，以填充第一沟槽 150，然后可通过回蚀工艺或化学机械抛光 (CMP) 工艺将牺牲填充层平坦化直至暴露焊盘保护层 148 的顶表面为止。因此，牺牲填充图案 158 可形成在第一沟槽 150 中。牺牲填充图案 158 可包括绝缘层、多晶硅层或它们的任何组合。例如，牺牲填充图案 158 的绝缘层可为氮化物层、硅基旋涂硬掩模 (SOH) 层或碳基 SOH 层。可利用 CVD 工艺、ALD 工艺或旋涂工艺形成牺牲填充图案 158。

[0097] 参照图 1A、图 14A 和图 14B，支撑图案 160 可形成在模制结构 10 上。例如，支撑图案 160 可形成在焊盘保护层 148 和牺牲填充图案 158 上。如图 1A 所示，可形成支撑图案 160 以包括多个桥 160a 和连接至桥 160a 的固定部分 160b。例如，形成在焊盘保护层 148 上的支撑图案 160 可包括设置在模制结构 10 上的固定部分 160b 和将模制结构 10 彼此连接的桥 160a。桥 160a 可沿着第一方向 D1 跨越牺牲填充图案 158。桥 160a 中的每一个沿着第二方向 D2 可具有宽度 BW。桥 160a 可沿着第二方向 D2 以距离 BL 彼此间隔开。因此，暴露出牺牲填充图案 158 的第二沟槽 162 可设置在支撑图案 160 中。第二沟槽 162 可具有沿着第二方向 D2 具有宽度 BL 的狭缝形。例如，距离 BL 可比宽度 BW 大几倍至几十倍。在第一方向 D1 上，第二沟槽 162 的宽度可大于第一沟槽 150 的宽度。第二沟槽 162 和第一沟槽 150 的沿着第一方向 D1 的宽度之间的差距可为图 14A 所示的距离 S 的两倍。

[0098] 在一些实施例中，支撑图案 160 的桥 160a 可按照 z 字形排列，如图 1B 所示。例如，沿着第一方向 D1 彼此相邻的桥 160a 可不对称并且可按照 z 字形排列。在其它实施例中，支撑图案 160 可具有沿着第一方向 D1 延伸的直线形状，如图 4 所示。在图 4 中，支撑图案 160 可设置为多个，并且支撑图案 160 可沿着第二方向 D2 排列在焊盘保护层 148 上。支撑

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图案 160 可包括多个桥 160a，所述多个桥 160a 沿着第一方向 D1 跨越牺牲填充图案 158，并延伸至焊盘保护层 148 上。例如，与桥 160a 具有基本相同的形状的固定部分 160b 可形成在模制结构 10 上。然而，本发明构思不限于此。固定部分 160b 的宽度可大于桥 160a 的宽度，或者可具有各种形状。桥 160a 中的每一个可具有在第二方向 D2 上的宽度 BW，并且桥 160a 可通过距离 BL 沿着第二方向 D2 彼此间隔开。

[0099] 参照图 15A 和图 15B，开口区 OA 可形成在模制结构 10 中。可通过第一沟槽 150 和第二沟槽 162 去除牺牲层 112 和牺牲填充图案 158，以在绝缘层 110 之间形成开口区 OA。例如，如果牺牲层 112 和牺牲填充图案 158 由氮化硅层形成并且绝缘层 112 由二氧化硅层形成，则可利用包括磷酸的蚀刻溶液各向同性地蚀刻牺牲层 112 和牺牲填充图案 158，以形成开口区 OA。例如，如果牺牲层 112 是氮化硅层并且牺牲填充图案 158 是 SOH 层，则可通过灰化工艺去除牺牲填充图案 158，并且可利用包括磷酸的蚀刻溶液去除牺牲层 112。开口区 OA 可为其中将形成栅电极的区。可通过开口区 OA 暴露垂直沟道结构 200 的一些部分。例如，可通过开口区 OA 暴露出垂直沟道结构 200 的数据存储图案 130。例如，可通过开口区 OA 暴露数据存储图案 130 的第一阻挡介电层（图 11B 的 132）。另外，可通过开口区 OA 中的至少一个暴露第一垂直沟道图案 128 的侧壁。对应于牺牲层 112 中的每一个的开口区 OA 可沿着第一方向 D1 和第二方向 D2 延伸。

[0100] 栅极氧化物层 164 可形成在第一垂直沟道图案 128 的侧壁上，并且缓冲氧化物层 166 可形成在凹进区 150R 中。例如，可将第一垂直沟道图案 128 的通过开口区 OA 暴露的侧壁氧化以形成栅极氧化物层 164。同时，还可将通过凹进区 150R 暴露的衬底 100 氧化以形成缓冲氧化物层 166。例如，可通过相同的热氧化工艺将通过凹进区 150R 暴露的第一垂直沟道图案 128 的侧壁和衬底 100 氧化。通过热氧化工艺形成的栅极氧化物层 164 可用作地选择晶体管的栅极氧化物层。缓冲氧化物层 166 可保护包括通过凹进区 150R 暴露的第一掺杂物区 154a 的衬底 100。

[0101] 参照图 16A 和图 16B，第二阻挡介电层 168 和栅极导电层 170 可按次序形成在衬底 100 上，以填充开口区 OA。可形成第二阻挡介电层 168 以保形地覆盖开口区 OA 的内表面。例如，第二阻挡介电层 168 可与绝缘层 110 的顶表面和底表面接触。第二阻挡介电层 168 可与垂直沟道结构 200 的侧壁接触。例如，第二阻挡介电层 168 可与第一阻挡介电层 132 接触。另外，第二阻挡介电层 168 可与第一垂直沟道图案 128 的栅极氧化物层 164 接触。第二阻挡介电层 168 可延伸至凹进区 150R 中，以形成在缓冲氧化物层 166 上。例如，第二阻挡介电层 168 可包括单层或多个薄层。例如，第二阻挡介电层 168 可包括高 k 介电层（例如，氧化铝层或二氧化铪层）。在其它实施例中，可不形成而是可省略第二阻挡介电层 168。

[0102] 可形成栅极导电层 170 以填充具有第二阻挡介电层 168 的开口区 OA。例如，栅极导电层 170 可包括包含金属的导电层。例如，栅极导电层 170 可包括金属层、金属硅化物层或金属氮化物层中的至少一个。例如，金属层可包括镍、钴、铂、钛、钽或钨中的至少一个。可利用 ALD 工艺或 CVD 工艺形成金属层。例如，金属硅化物层可包括硅化镍、硅化钴、硅化铂、硅化钛、硅化钽或硅化钨中的至少一个。在一些实施例中，可沉积多晶硅层和金属层以填充开口区 OA，并且沉积的多晶硅层和金属层可通过热处理工艺彼此反应以形成金属硅化物层。例如，金属氮化物层可包括氮化钛、氮化钨或氮化钽中的至少一个。栅极导电层 170 可填充凹进区 150R 的至少一部分。

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[0103] 参照图 17A 和图 17B，堆叠栅极结构 30 可形成在衬底 100 上。堆叠栅极结构 30 中的每一个可包括按顺序堆叠在衬底 100 上的栅电极 172。在一些实施例中，可将栅极导电层 170 各向同性地蚀刻以形成沿着第三方向 D3 彼此分离的堆叠的栅电极 172。例如，栅电极 172 可具有沿着第一方向 D1 从绝缘层 110 的侧壁朝着垂直沟道结构 200 横向凹进的被截顶的端部。因此，沿着第三方向 D3 彼此相邻的栅电极 172 可在物理上彼此分离以防止它们之间短路。结果，堆叠栅极结构 30 中的每一个可包括交替和重复地堆叠在衬底 100 上的绝缘层 110 和栅电极 172。

[0104] 同时，如果如参照图 1A、图 2A 和图 2B 描述的那样，垂直沟道结构 200 与堆叠栅极结构 30 的左侧壁之间的栅电极 172 的数量和垂直沟道结构 200 与堆叠栅极结构 30 的右侧壁之间的栅电极 172 的数量不同，则堆叠栅极结构 30 会朝着栅电极 172 的数量更大的侧壁倾斜。随着堆叠的栅电极 172 的数量增加，堆叠栅极结构 30 的倾斜现象会变得更加严重。然而，根据本发明构思的实施例，可通过支撑图案 160 减轻或防止堆叠栅极结构 30 的倾斜现象。例如，堆叠栅极结构 30 可通过支撑图案 160 的桥 160a 彼此连接，从而可确保堆叠栅极结构 30 的结构稳定性，以减轻或防止堆叠栅极结构 30 的倾斜现象。结果，堆叠栅极结构 30 可减小或防止可在后续工艺中导致的工艺误差。

[0105] 参照图 18A 和图 18B，隔离绝缘层 178 可形成在堆叠的栅极结构 30 之间的第一沟槽 150 中。例如，隔离绝缘层 178 可具有在支撑图案 160、以及第一沟槽 150 和第二沟槽 162 的内表面上形成的直线形状。隔离绝缘层 178 可填充凹进区 150R。隔离绝缘层 178 还可填充绝缘层 110 之间的空间，以保护栅电极 172 的端部。隔离绝缘层 178 可包括氮化物层、氧化物层或氧氮化物层。可利用 CVD 工艺或 ALD 工艺形成隔离绝缘层 178。

[0106] 参照图 19A、图 19B、图 19C 和图 19D，隔离绝缘图案 180 可形成在堆叠栅极结构 30 之间的第一沟槽 150 的内侧壁上。隔离绝缘图案 180 还可形成在第二沟槽 162 的内侧壁上。突出区 110a 可形成在通过第一沟槽 150 暴露的衬底 100 上，并且下隔离绝缘图案 180a 可形成在突出区 100a 中的每一个上。例如，可通过各向异性蚀刻工艺回蚀隔离绝缘层 178，以在第一沟槽 150 和第二沟槽 162 中形成隔离绝缘图案 180。此时，可将第二阻挡介电层 168 和缓冲氧化物层 166 与隔离绝缘层 178 一起蚀刻，以暴露第一掺杂物区 154a。另外，可例如以深度 PH 将衬底 100 过度蚀刻。在隔离绝缘层 178 的该回蚀工艺中，支撑图案 160 的桥 160a 可保护隔离绝缘层 178 的一些部分，以形成下隔离绝缘图案 180a。换句话说，下隔离绝缘图案 180a 可对应于在桥 160a 下方保留的隔离绝缘层 178 的所述部分。下隔离绝缘图案 180a 可在平面图中与桥 160a 基本重叠，并且可沿着第二方向 D2 排列。例如，下隔离绝缘图案 180a 中的每一个的侧壁可与桥 160a 中的每一个的侧壁对齐。第二阻挡介电层 168 的一部分和缓冲氧化物层 166 的一部分可保持在下隔离绝缘图案 180a 中的每一个的下方，并且衬底 100 的突出区 100a 可形成在缓冲氧化物层 166 的其余部分下方。第二阻挡介电层 168 和缓冲氧化物层 166 的其余部分的宽度可与下隔离绝缘图案 180a 的宽度基本相同。衬底 100 的突出区 100a 可具有高度 PH，并且设置在下隔离绝缘图案 180a 中的每一个的下方。高度 PH 可对应于突出区 100a 的顶表面与经蚀刻的衬底 100 的顶表面之间的垂直距离。换句话说，衬底 100 的突出区 100a 可沿着第二方向 D2 排列。下隔离绝缘图案 180a 和隔离绝缘图案 180 可彼此连接以构成一个联合主体。隔离绝缘图案 180 可具有在第一沟槽 150 和第二沟槽 162 的内侧壁上形成的间隔件形状，并且下隔离绝缘图案 180a 可形成在第

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一沟槽 150 的底表面上，以分别对应于支撑图案 160 的各个桥 160a。下隔离绝缘图案 180a 可连接至隔离绝缘图案 180。例如，隔离绝缘图案 180 可沿着第一方向 D1 将栅电极 172 彼此隔离。下隔离绝缘图案 180a 和突出区 100a 沿着第二方向 D2 可具有宽度 PW。下隔离绝缘图案 180a 可沿着第二方向 D2 通过距离 PL 彼此间隔开。突出区 110a 还可沿着第二方向 D2 通过距离 PL 彼此间隔开。宽度 PW 可基本等于宽度 BW，并且距离 PL 可与距离 BL 基本相等。

[0107] 接着，可在设置在突出区 100a 之间的衬底 100 中形成第二掺杂物区 154b。第二掺杂物区 154b 可沿着第二方向 D2 排列，并且可形成在沿着第二方向 D2 连续地形成的第一掺杂物区 154a 中。第二掺杂物区 154b 可彼此间隔开。在一些实施例中，第二掺杂物区 154b 可穿透第一掺杂物区 154a，以延伸至衬底 100 中。

[0108] 第二掺杂物区 154b 和第一掺杂物区 154a 可构成公共源极区 154。可将掺杂物离子大量注入至具有第一掺杂物区 154a 的衬底 100 中，以形成第二掺杂物区 154b。例如，第二掺杂物区 154b 可包括其导电类型与第一掺杂物区 154b 的掺杂物的导电类型相同的掺杂物。换句话说，第二掺杂物区 154b 可具有第二导电类型的掺杂物。例如，可以以约 5KeV 至约 30KeV 的能量和约 10^{14}atoms/cm^{2}至约 10^{15}atoms/cm^{2}的剂量将 N 型掺杂物离子（例如，砷 (As) 离子或磷 (P) 离子）注入到衬底 100 中，从而形成第二掺杂物区 154b。公共源极区 154 可包括突出公共源极区 CSP 和凹进公共源极区 CSR。突出公共源极区 CSP 中的每一个可形成在其下方的突出区 110a 和衬底 100 中的每一个中，并且凹进公共源极区 CSR 中的每一个可形成在突出区 100a 之间的衬底 100 中，或形成在与突出区 100a 相邻的衬底 100 中。突出公共源极区 CSP 中的每一个可包括第一掺杂物区 154a 的一部分，并且凹进公共源极区 CSR 中的每一个可包括第一掺杂物区 154a 的一部分和第二掺杂物区 154b。第二掺杂物区 154b 可延伸至与突出区 100a 的侧壁相邻的突出公共源极区 CSP 中。

[0109] 第一掺杂物区 154a 可包括高度彼此不同的区。例如，第一掺杂物区 154a 可具有沿着第二方向 D2 交替排列的第一区和第二区。第一区具有第一高度，并且第二区具有与第一高度不同的第二高度。在一些实施例中，第一掺杂物区 154a 在突出公共源极区 CSP 中的每一个中可具有第一高度 SH1，并且在凹进公共源极区 CSR 中的每一个中可具有第二高度 SH2。例如，第一高度 SH1 可大于第二高度 SH2。

[0110] 在一些实施例中，设置在如图 1B 所示沿着第一方向 D1 按照 z 字形排列的桥 160a 下方的下隔离绝缘图案 180a 和突出区 100a 可沿着第一方向 D1 按照 z 字形排列。另外，公共源极区 154 的突出公共源极区 CSP 沿着第一方向 D1 可不对称，而是可沿着第一方向 D1 按照 z 字形排列。

[0111] 参照图 20A 和图 20B，源极插线 182 可形成在第一沟槽 150 和第二沟槽 162 中。源极插线 182 可延伸至凹进区 150R 中，以连接至公共源极区 154，并且可沿着第二方向 D2 延伸。源极插线 182 可包括势垒层 182a 和导电层 182b。势垒层 182a 可以与第二掺杂物区 154b 接触并且可包围导电层 182b 的侧壁和底表面。势垒层 182a 和导电层 182b 可沿着第二方向 D2 连续地延伸。例如，可形成势垒层 182a 和导电层 182b，以填充具有隔离绝缘图案 180 的第一沟槽 150 和第二沟槽 162，并且可将势垒层 182a 和导电层 182b 平坦化直至暴露支撑图案 160 为止，从而形成源极插线 182。势垒层 182a 可包括金属和金属氮化物中的至少一个。例如，势垒层 182a 可包括钛 (Ti)、钽 (Ta)、氮化钛 (TiN)、氮化钨 (WN) 或氮化钽

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(TaN) 中的至少一个。例如，导电层 182b 可包括诸如钨或铜的金属。源极插线 182 的底表面的一部分可与公共源极区 154 接触，并且源极插线 182 的底表面的另一部分可与公共源极区 154 分离开。例如，源极插线 182 可与凹进公共源极区 CSR 的顶表面接触，但是可通过下隔离绝缘图案 180a、第二阻挡介电层 168 的一些部分和缓冲氧化物层 166 的一些部分与突出公共源极区 CSP 的顶表面间隔开。源极插线 182 可与突出公共源极区 CSP 的侧壁的一些部分接触，并且可具有沿着第二方向 D2 连续地延伸的直线形状。换句话说，源极插线 182 的底表面的一些部分可与下隔离绝缘图案 180a 直接接触，并且源极插线 182 的底表面的其它部分可与第二掺杂物区 154b 直接接触。源极插线 182 可沿着第二方向 D2 延伸。

[0112] 参照图 21A 和图 21B，可形成上层间绝缘层 186 以覆盖源极插线 182，并且可形成漏极触点 190 以连接至导电焊盘 146。在一些实施例中，上层间绝缘层 186 可覆盖源极插线 182 并且可形成在支撑图案 160 上。上层间绝缘层 186 可由氧化物层、氧氮化物层、和氮化物层中的至少一个形成。漏极触点 190 可穿透上层间绝缘层 186、支撑图案 160 和焊盘保护层 148，以连接至导电焊盘 146。例如，可形成漏极接触孔 188 以穿透上层间绝缘层 186、支撑图案 160 和焊盘保护层 148。漏极接触孔 188 将导电焊盘 146 暴露出来。可沉积导电材料以填充漏极接触孔 188，并且可通过回蚀工艺或化学机械抛光 (CMP) 工艺将沉积的导电材料平坦化以形成漏极触点 190。漏极触点 190 可包括诸如金属、金属氮化物和 / 或掺杂有掺杂物的多晶硅的导电材料。漏极触点 190 可连接至将在后续工艺中形成的位线 (未示出)。

[0113] 可通过上述支撑图案 160 减轻或防止堆叠栅极结构 30 的倾斜现象，从而减小或防止工艺误差。例如，如果堆叠栅极结构 30 由于与堆叠栅极结构 30 的左侧壁和右侧壁相邻的栅电极 172 的数量之间的差异而倾斜，则当将隔离绝缘层 178 蚀刻以形成隔离绝缘图案 180 时可能无法暴露公共源极区 154。因此，在后续工艺中形成的源极插线 182 不会连接至公共源极区 154。另外，可能会将与栅电极 172 相邻的隔离绝缘层 178 蚀刻，从而会暴露出栅电极 172 以导致源极插线 182 与栅电极 172 之间的短路。此外，当形成漏极接触孔 188 时，会无法暴露导电焊盘 146 或者仅会暴露出导电焊盘 146 的一小部分，从而导致漏极触点 190 与导电焊盘 146 之间的连接错误。然而，根据本发明构思的示例实施例，可通过支撑图案 160 减轻或防止堆叠栅极结构 30 的倾斜现象，从而提高了半导体存储器装置的结构稳定性和电可靠性。

[0114] 图 22A 和图 22B 分别是沿着图 1A 的线 I-I' 和 II-II' 截取的剖视图，以示出制造图 5A 和图 5B 的半导体存储器装置的方法的一些处理。在当前实施例中，制造半导体存储器装置的方法可包括参照图 9 至图 20B 描述的模制结构 10 的形成工艺至源极插线 182 的形成工艺。

[0115] 参照图 22A 和图 22B，可在形成源极插线 182 之后去除支撑图案 160。例如，可通过各向异性或各向同性蚀刻工艺选择性地去除支撑图案 160，从而将焊盘保护层 148 和源极插线 182 暴露出来。在一些实施例中，当去除支撑图案 160 时，可将形成在第二沟槽 162 的内侧壁上的隔离绝缘图案 180 和第二阻挡介电层 168 一起去除。可通过支撑图案 160 的去除在源极插线 182 的上部中形成桥凹槽区 184。因此，源极插线 182 的顶表面可不平坦。桥凹槽区 184 的内侧壁可与下隔离绝缘图案 180a 的侧壁和突出区 100a 的侧壁对齐。例如，当从平面图看时，桥凹槽区 184 可与下隔离绝缘图案 180a 和突出区 100a 分别重叠。可通

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过上层间绝缘层 186 填充桥凹槽区 184，如图 5A 和图 5B 所示。接着，可在穿透上层间绝缘层 186 和焊盘保护层 148 的漏极接触孔 188 中形成漏极触点 190。漏极触点 190 可连接至导电焊盘 146。

[0116] 图 23A 和图 23B 分别是沿着图 1A 的线 I-I' 和 II-II' 截取的剖视图，以示出制造图 6A 和图 6B 的半导体存储器装置的方法的一些处理。在当前实施例中，制造半导体存储器装置的方法可包括参照图 9 至图 20B 描述的模制结构 10 的形成工艺至源极插线 182 的形成工艺。

[0117] 参照图 23A 和图 23B，在形成源极插线 182 之后可去除源极插线 182 的一部分和支撑图案 160。例如，可通过平坦化工艺将支撑图案 160 和源极插线 182 的上部的一部分去除，从而可将源极插线 182 的顶表面平坦化。例如，可利用 CMP 工艺将支撑图案 160 和源极插线 182 的上部的该部分去除，以暴露出焊盘保护层 148 的顶表面以及形成具有基本平坦的顶表面的源极插线 182。因此，源极插线 182 的顶表面可与焊盘保护层 148 的顶表面基本共面。然后，如图 6A 和图 6B 所示，上层间绝缘层 186 可形成在焊盘保护层 148 和具有基本平坦的顶表面的源极插线 182 上，并且漏极触点 190 可形成在穿透上层间绝缘层 186 和焊盘保护层 148 的漏极接触孔 188 中。漏极触点 190 可连接至导电焊盘 146。

[0118] 图 24A 和图 25A 是沿着图 1A 的线 I-I' 截取的剖视图，以示出制造图 7A、图 7B、图 8A 和图 8B 的半导体存储器装置的方法的一些处理。图 24B 和图 25B 是沿着图 1A 的线 II-II' 截取的剖视图，以示出制造图 7A、图 7B、图 8A 和图 8B 的半导体存储器装置的方法的一些处理。在当前实施例中，制造半导体存储器装置的方法可包括参照图 9 至图 18B 描述的模制结构 10 的形成工艺至隔离绝缘层 178 的形成工艺。

[0119] 参照图 24A 和图 24B，当在隔离绝缘层 178 上执行回蚀工艺以形成隔离绝缘图案 180 时可去除支撑图案 160。例如，支撑图案 160 和隔离绝缘层 178 由相同材料形成，可利用相同蚀刻条件去除隔离绝缘层 178 的一部分和支撑图案 160。因此，可去除填充凹进区 150R 的隔离绝缘层 178、第二阻挡介电层 168 和缓冲氧化物层 166，并且隔离绝缘图案 180 可形成在第一沟槽 150 和第二沟槽 162 的内侧壁上。隔离绝缘图案 180 可沿着第二方向 D2 连续地暴露具有第一掺杂物区 154a 的衬底 100 的顶表面。此时，因为还蚀刻设置在与桥 160a 重叠的区中的隔离绝缘层 178，所以衬底 100 可被过度蚀刻。因此，可将与桥 160a 相似的突出区 100a 形成为具有高度 PH' 和宽度 PW'。突出区 100a 可通过距离 PL' 彼此间隔开。例如，高度 PH' 可基本等于或大于图 19C 所示的高度 PH。例如，宽度 PW' 和距离 PL' 可分别与图 19B 所示的宽度 PW 和距离 PL 基本相似或相等。第二掺杂物区 154b 可沿着第二方向 D2 连续地形成在具有第一掺杂物区 154a 的衬底 100 中。第二掺杂物区 154b 和第一掺杂物区 154a 可构成公共源极区 154。可将掺杂物离子大量注入至具有第一掺杂物区 154a 的衬底 100 中，从而形成第二掺杂物区 154b。例如，第二掺杂物区 154b 可包括与第一掺杂物区 154b 的掺杂物的导电类型相同的第二导电类型的掺杂物。例如，可以以约 10KeV 至约 40KeV 的能量和约 10^{14}atoms/cm^{2}至约 10^{15}atoms/cm^{2}的剂量将 N 型掺杂物离子（例如，砷 (As) 离子或磷 (P) 离子）注入至衬底 100 中，从而形成第二掺杂物区 154b。

[0120] 形成在包括突出区 100a 的衬底 100 中的突出公共源极区 CSP' 可包括具有低浓度的第一掺杂物区 154a 和具有高浓度的第二掺杂物区 154b。形成在设置在突出区 100a 之间的衬底 100 中的凹进公共源极区 CSR' 还可包括具有低浓度的第一掺杂物区 154a 和具有高

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浓度的第二掺杂物区 154b。例如，具有高浓度的第二掺杂物区 154b 可由具有低浓度的第一掺杂物区 154a 包围。然而，本发明构思不限于此。在其它实施例中，第二掺杂物区 154b 可穿透第一掺杂物区 154a 以延伸至衬底 100 中。第一掺杂物区 154a 可包括其高度彼此不等的区。例如，第一掺杂物区 154a 可包括沿着第二方向 D2 交替排列的第一区和第二区。第一区可具有第一高度 SH1，并且第二区可具有与第一高度 SH1 不同的第二高度 SH2。例如，第一掺杂物区 154a 在突出公共源极区 CSP' 中的每一个中可具有第一高度 SH1，并且在凹进公共源极区 CSR' 中的每一个中可具有第二高度 SH2。例如，第一高度 SH1 可大于第二高度 SH2（见图 8A 和图 8B）。

[0121] 在一些实施例中，如果去除如图 1B 所示具有按照 z 字形排列的桥 160a 的支撑图案 160，则突出区 100a 可沿着第一方向 D1 按照 z 字形排列。另外，公共源极区 154 的突出公共源极区 CSP' 沿着第一方向 D1 可不对称，但是可沿着第一方向 D1 按照 z 字形排列。

[0122] 参照图 25A 和图 25B，可形成源极插线 182 以填充第一沟槽 150。源极插线 182 可包括势垒层 182a 和导电层 182b。源极插线 182 的势垒层 182a 可与第二掺杂物区 154b 接触并且可包围导电层 182b 的侧壁和底表面。势垒层 182a 和导电层 182b 可沿着第二方向 D2 连续地延伸。例如，可形成势垒层 182a 和导电层 182b 以填充具有隔离绝缘图案 180 的第一沟槽 150，并且可将势垒层 182a 和导电层 182b 平坦化直至暴露出焊盘保护层 148 为止，从而形成源极插线 182。包括在源极插线 182 中的导电材料可与参照图 20A 和图 20B 描述的相同。

[0123] 源极插线 182 的底表面可与具有高度 PH' 的突出区 100a 直接接触。因此，源极插线 182 可与沿着第二方向 D2 排列的突出区 100a 和它们之间的衬底 100 接触。源极插线 182 可沿着第二方向 D2 延伸。换句话说，源极插线 182 可沿着第二方向 D2 延伸，以与第二掺杂物区 154b（其连续地形成在包括沿着第二方向 D2 排列的突出区 100a 的衬底 100 中）直接接触。接着，如图 7A 和图 7B 所示，上层间绝缘层 186 可形成在焊盘保护层 148 和具有基本平坦的顶表面的源极插线 182 上。连接至导电焊盘 146 的漏极触点 190 可形成在穿透上层间绝缘层 186 和焊盘保护层 148 的漏极接触孔 188 中。

[0124] 图 26 是示出包括根据本发明构思的示例实施例的半导体存储器装置的半导体装置系统的示意性框图。

[0125] 参照图 26，根据本发明构思的示例实施例的存储器系统 1000 可为半导体存储装置。例如，存储器系统 1000 可为存储卡或固态盘 (SSD)。存储器系统 1000 可包括设置在壳体 1100 中的控制器 1200 和存储器装置 1300。控制器 1200 可与存储器装置 1300 交换电信号。例如，控制器 1200 和存储器装置 1300 可响应于控制器 1200 的命令彼此交换数据。因此，存储器系统 1000 可将数据存储在存储器装置 1300 中，或者可将数据从存储器装置 1300 输出至外部系统。存储器装置 1300 可包括根据本发明构思的示例实施例的半导体存储器装置中的至少一个。

[0126] 图 27 是示出包括根据本发明构思的示例实施例的半导体存储器装置的电子系统的示意性框图。

[0127] 参照图 27，电子系统 2000 可包括控制器 2200、存储器装置 2300 和输入 / 输出装置 2400。控制器 2200、存储器装置 2300 和输入 / 输出装置 2400 可通过数据总线 2100 彼此耦接。数据总线 2100 可对应于发送数据的路径。例如，控制器 2200 可包括微处理器、数

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字信号处理器、微控制器或其它逻辑装置中的至少一个。其它逻辑装置的功能可与微处理器、数字信号处理器和微控制器中的任一个相似。输入/输出装置2400可包括键区、键盘或显示装置中的至少一个。存储器装置2300是能够存储数据的装置。存储器装置2300可存储将通过控制器2200执行的数据和/或命令。存储器装置2300可包括易失性存储器装置和/或非易失性存储器装置。可替换地，存储器装置2300可包括闪速存储器装置。闪速存储器装置可实现为固态盘(SSD)。在这种情况下，电子系统2000可将大量数据稳定地存储在存储器装置2300中。存储器装置2300可包括根据本发明构思的示例实施例的半导体存储器装置中的至少一个。电子系统2000还可包括将数据发送至通信网络或者从通信网络接收数据的接口单元2500。接口单元2500可通过无线方式或通过线缆操作。例如，接口单元2500可包括天线或无线/线缆收发器。

[0128] 可利用各种封装技术将根据本发明构思的示例实施例的半导体存储器装置包封。例如，可利用以下封装技术中的任一个将根据本发明构思的前述实施例的半导体存储器装置包封，所述封装技术有：层叠封装(PoP)技术、球栅阵列(BGA)技术、芯片级封装(CSP)技术、塑料引线芯片载体(PLCC)技术、塑料双列直插式封装(PDIP)技术、窝伏尔组件式裸晶技术、晶圆式裸晶技术、板上芯片(COB)技术、陶瓷双列直插式封装(CERDIP)技术、塑料方形扁平封装(PMQFP)技术、塑料四边扁平封装(PQFP)技术、小外型封装(SOC)技术、缩小外型封装(SSOP)技术、薄型小外型封装(TSOP)技术、薄型四方扁平封装(TQFP)技术、系统级封装(SIP)技术、多芯片封装(MCP)技术、晶圆级制造封装(WFP)技术和晶圆级处理堆叠封装(WSP)技术。其中安装了根据以上实施例之一的半导体存储器装置的封装件还可包括控制半导体存储器装置的至少一个半导体装置(例如，控制器和/或逻辑装置)。

[0129] 根据本发明构思的示例实施例，可减轻或防止堆叠栅极结构的倾斜现象，以提高半导体存储器装置的结构稳定性和电可靠性。

[0130] 根据本发明构思的示例实施例，可形成支撑图案以减轻或防止包围垂直沟道结构的堆叠栅极结构的倾斜，从而可在后续工艺中减小或防止工艺误差。结果，可提供能够提高可靠性的制造半导体存储器装置的方法。

[0131] 虽然已经参照示例实施例描述了本发明构思，但是本领域技术人员应该理解，在不脱离本发明构思的精神和范围的情况下，可作出各种改变和修改。因此，应该理解以上实施例非限制性的而是例示性的。因此，通过对以下权利要求及其等同物的可允许的最宽的解释来确定本发明构思的范围，而不应通过以上描述来局限或限制本发明构思的范围。

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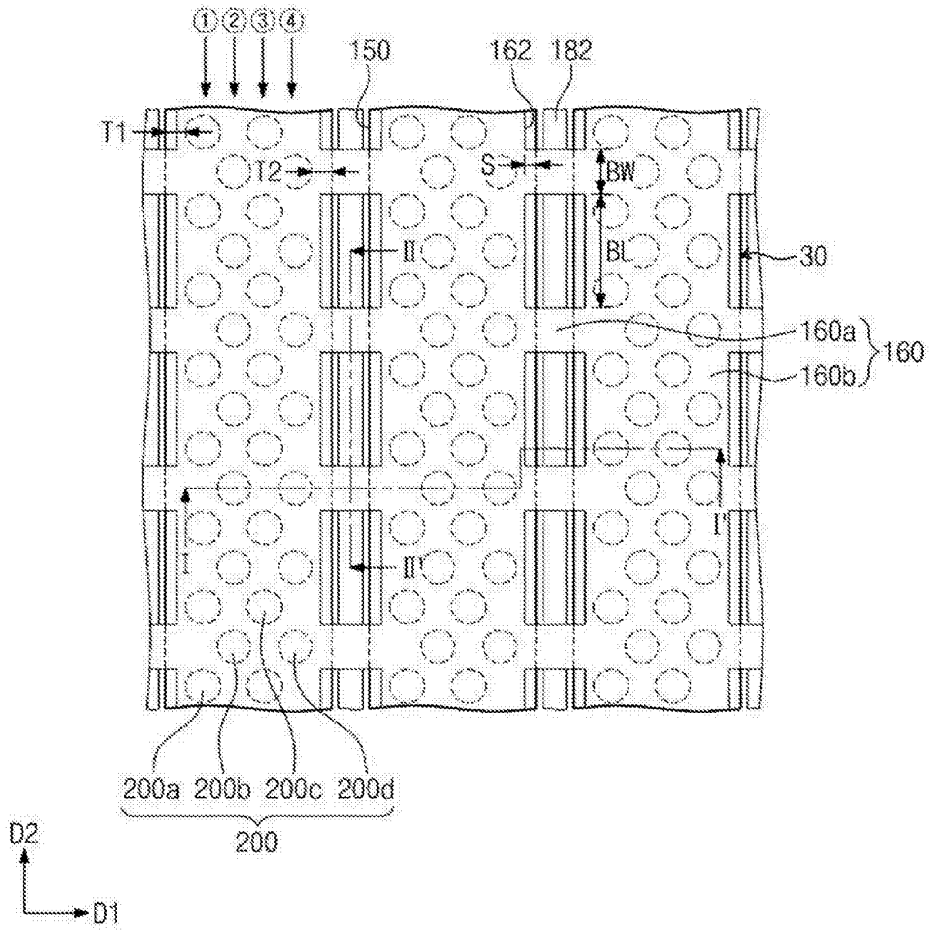

图 1A

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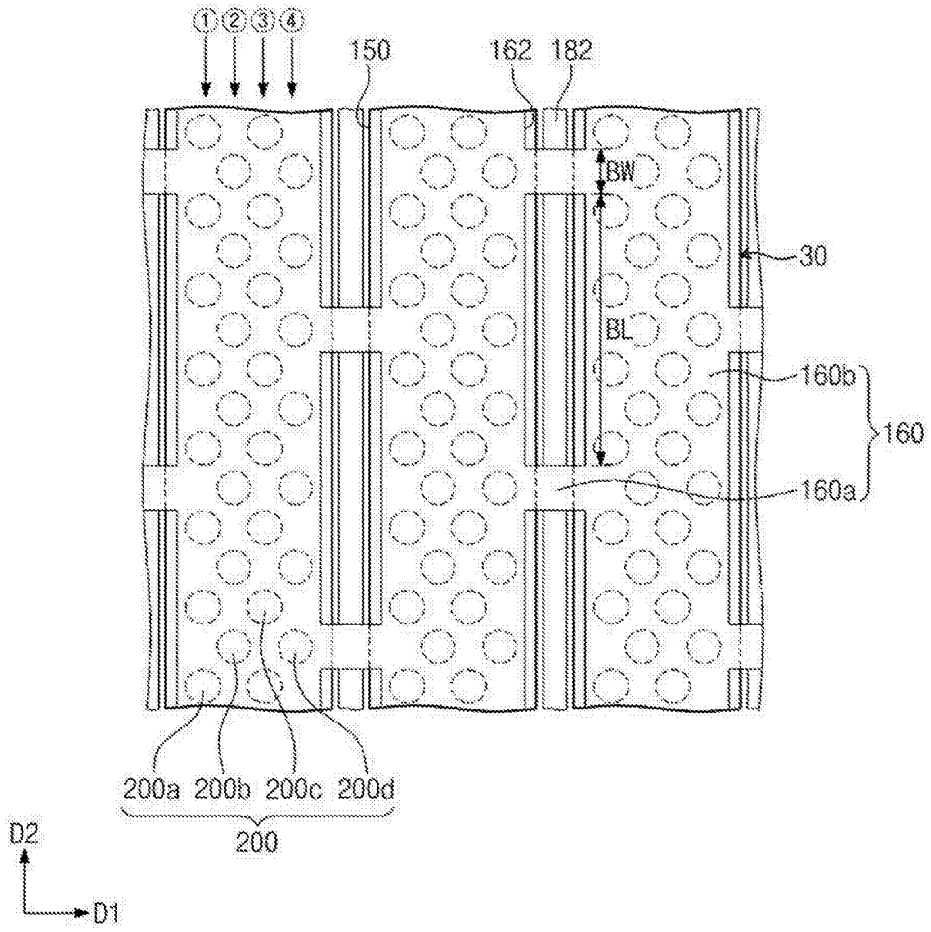

图 1B

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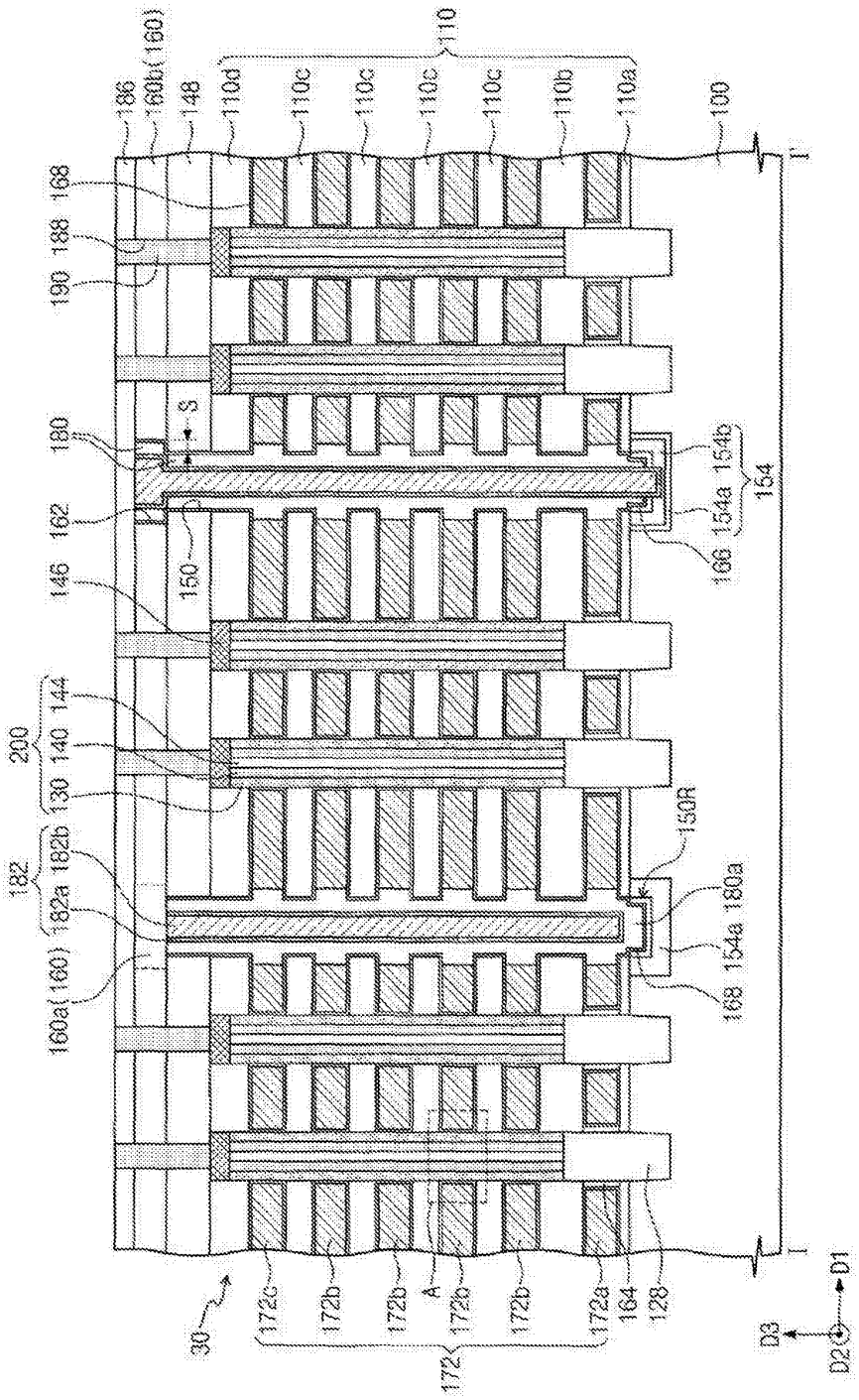

图 2A

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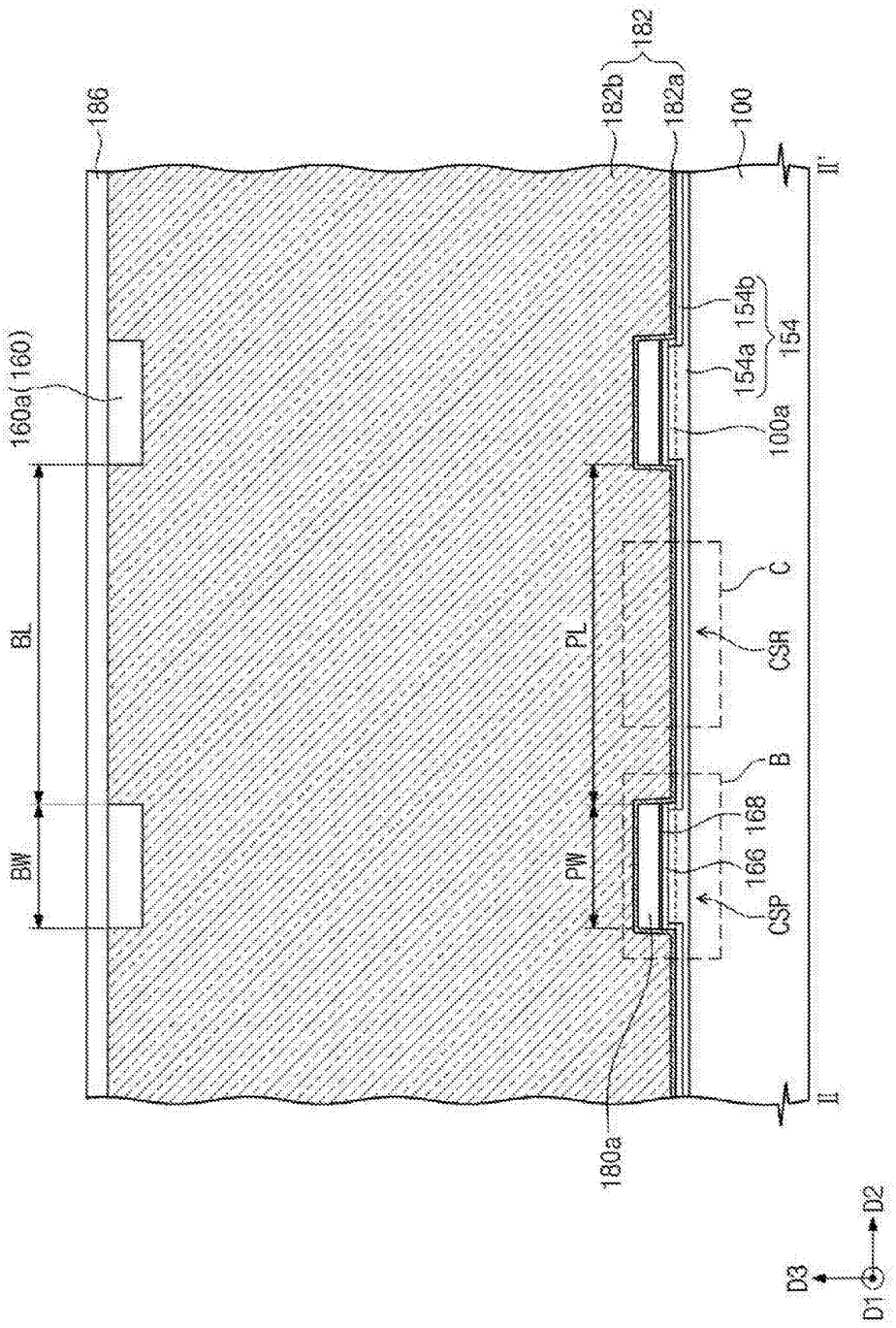

图 2B

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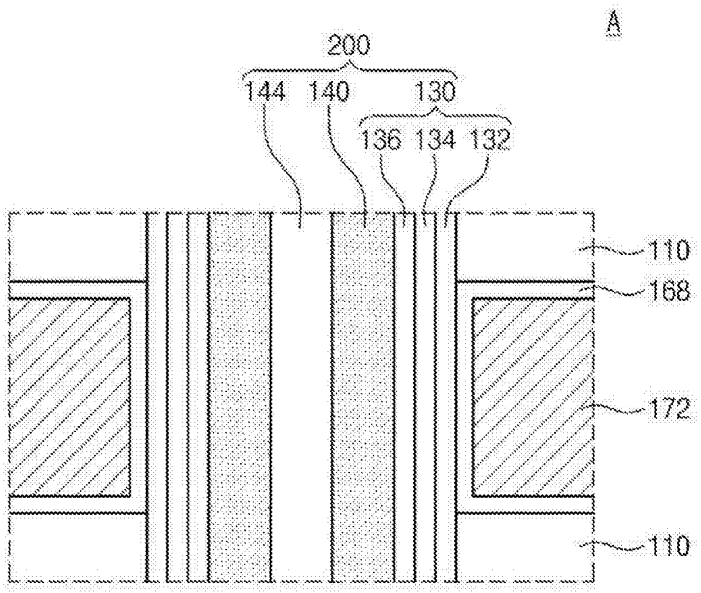

图 3A

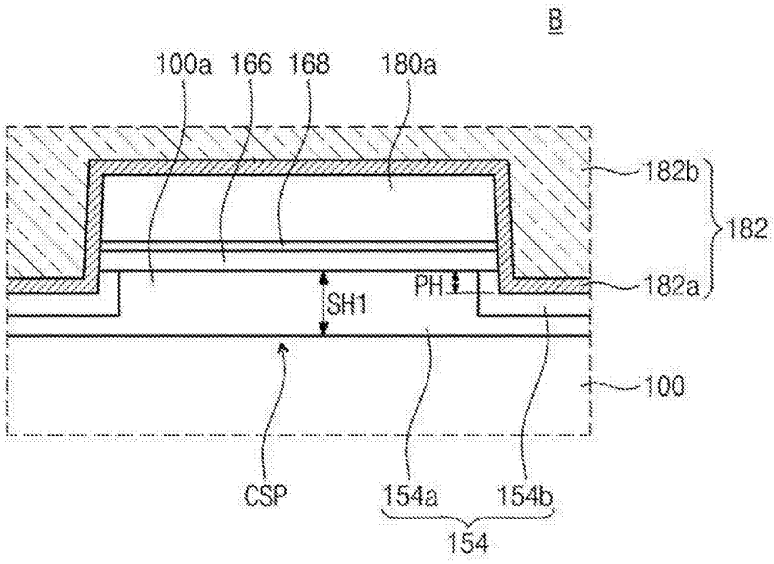

图 3B

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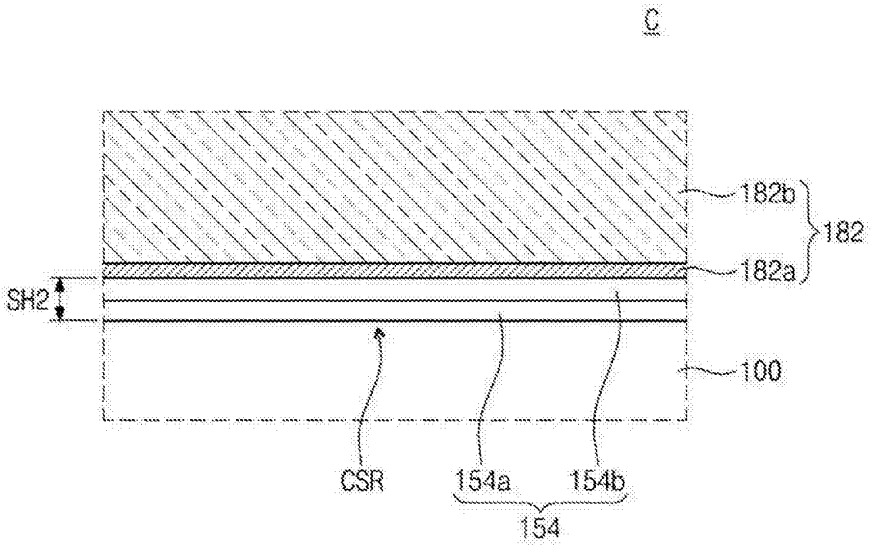

图 3C

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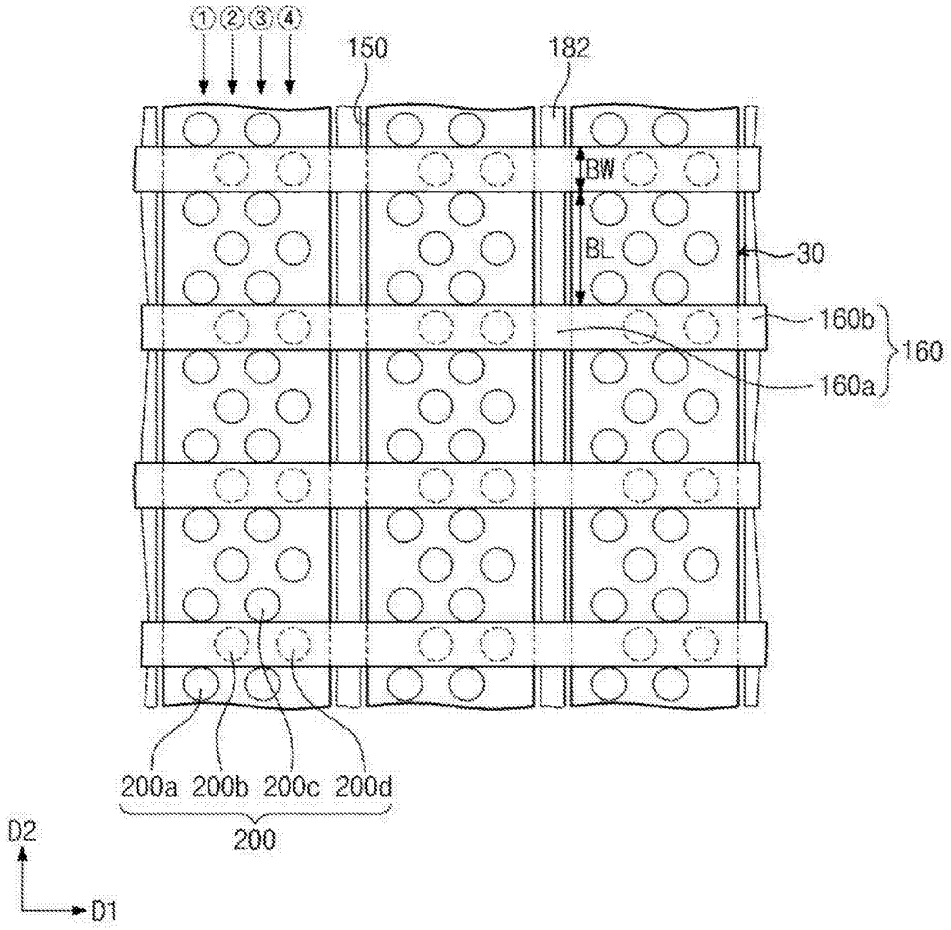

图 4

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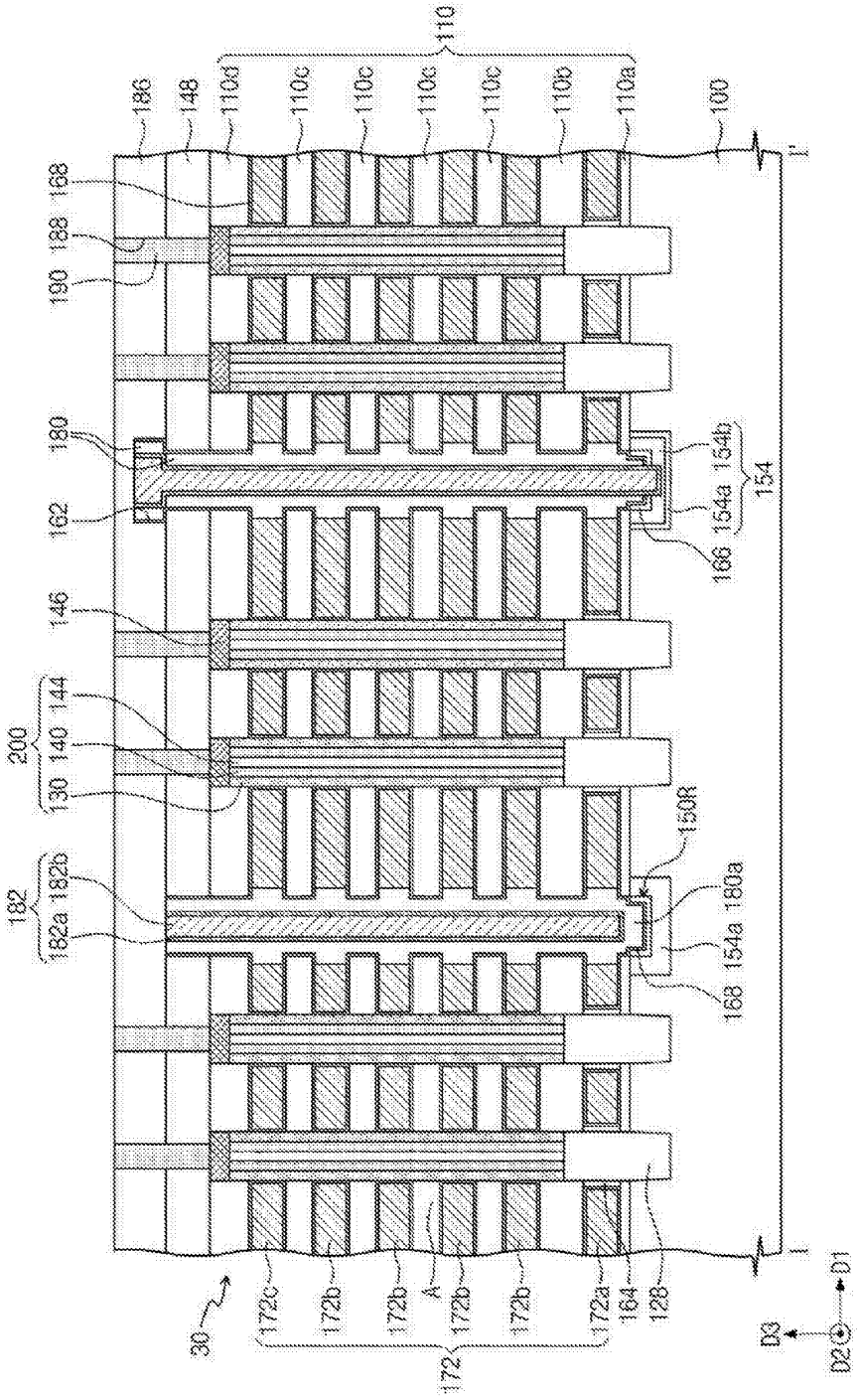

图 5A

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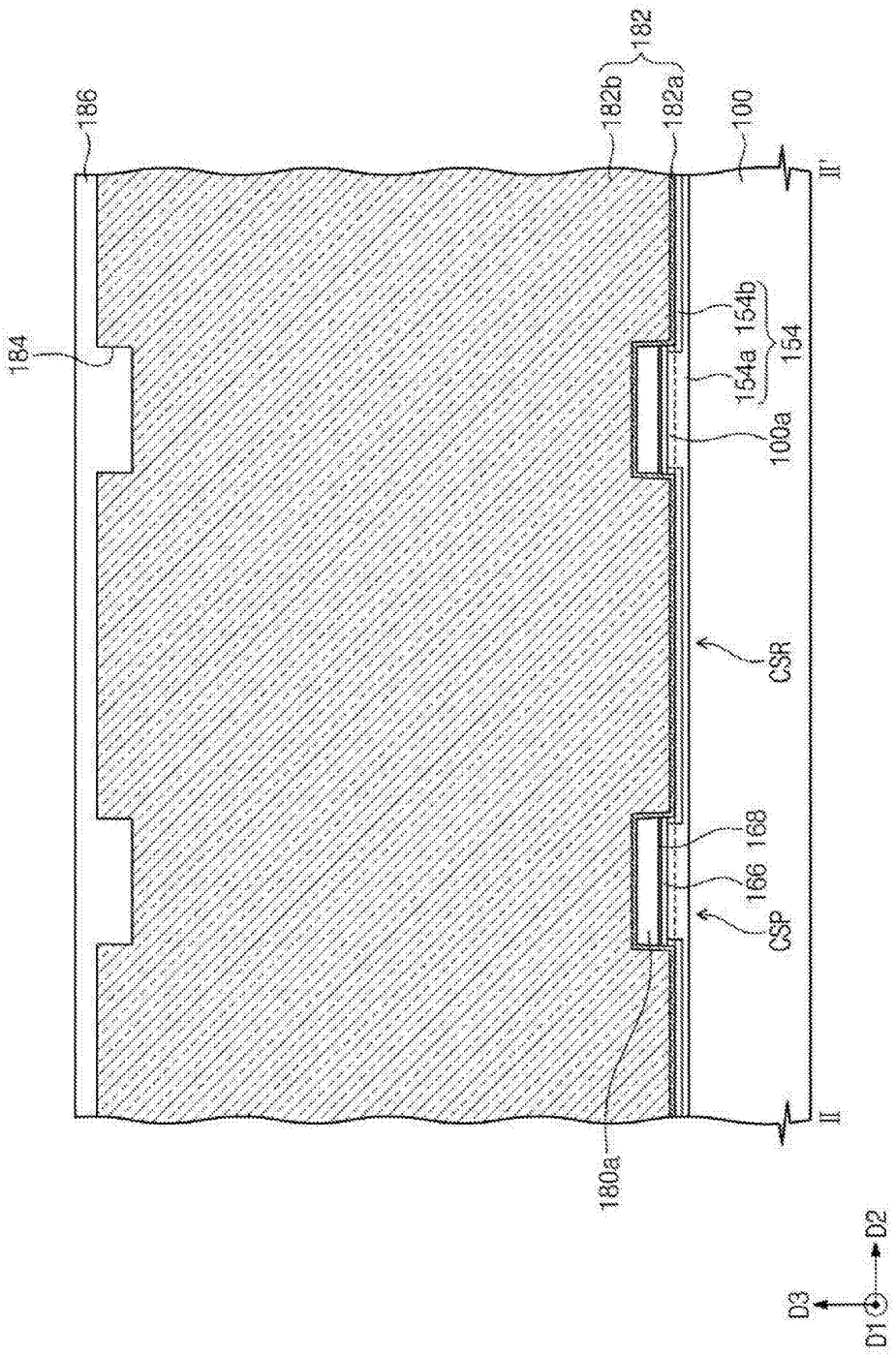

图 5B

Micron Ex. 1002, p. 317
Micron v. YMTC
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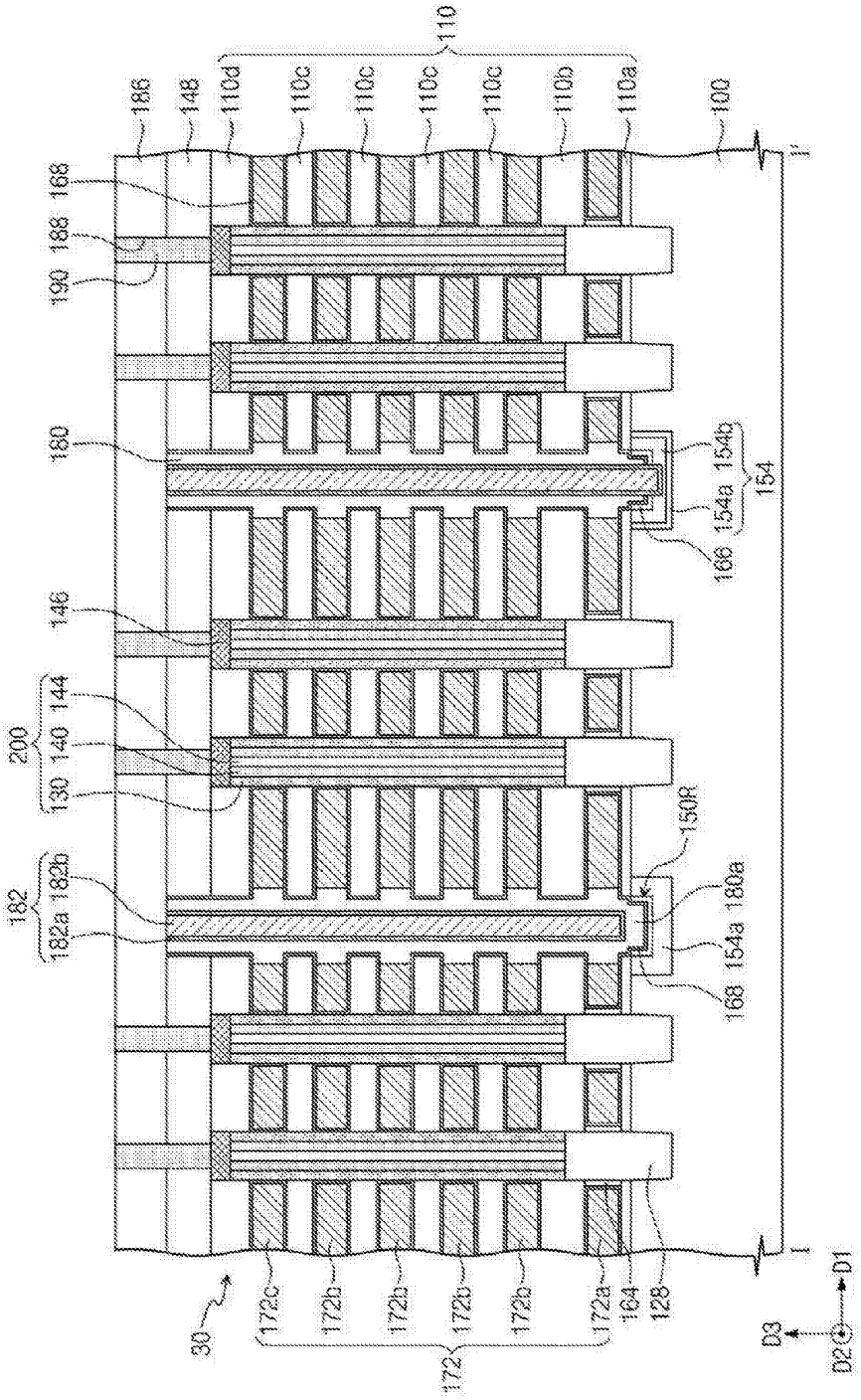

图 6A

Micron Ex. 1002, p. 318
Micron v. YMTC
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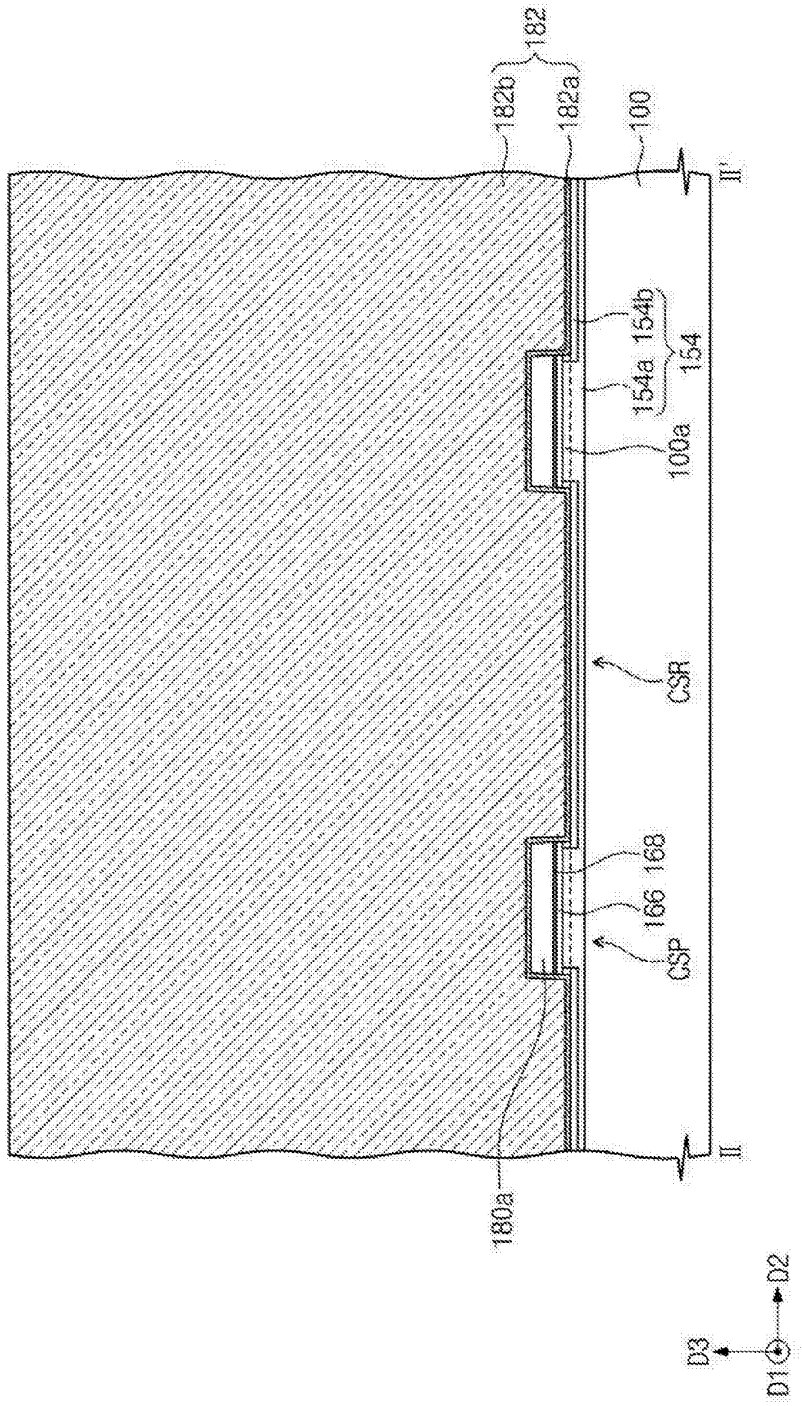

图 6B

Micron Ex. 1002, p. 319
Micron v. YMTC
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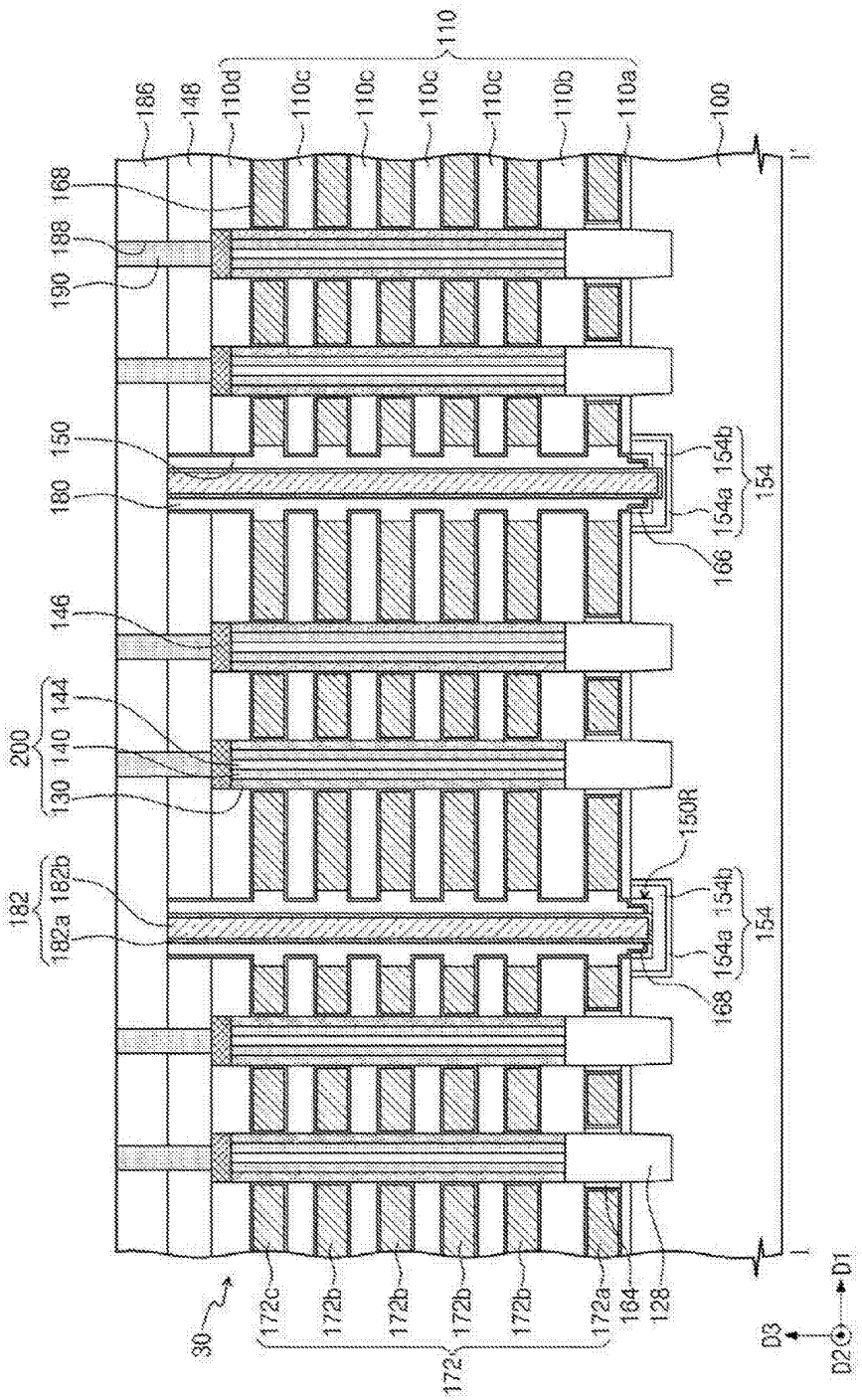

图 7A

Micron Ex. 1002, p. 320
Micron v. YMTC
IPR2024-00909

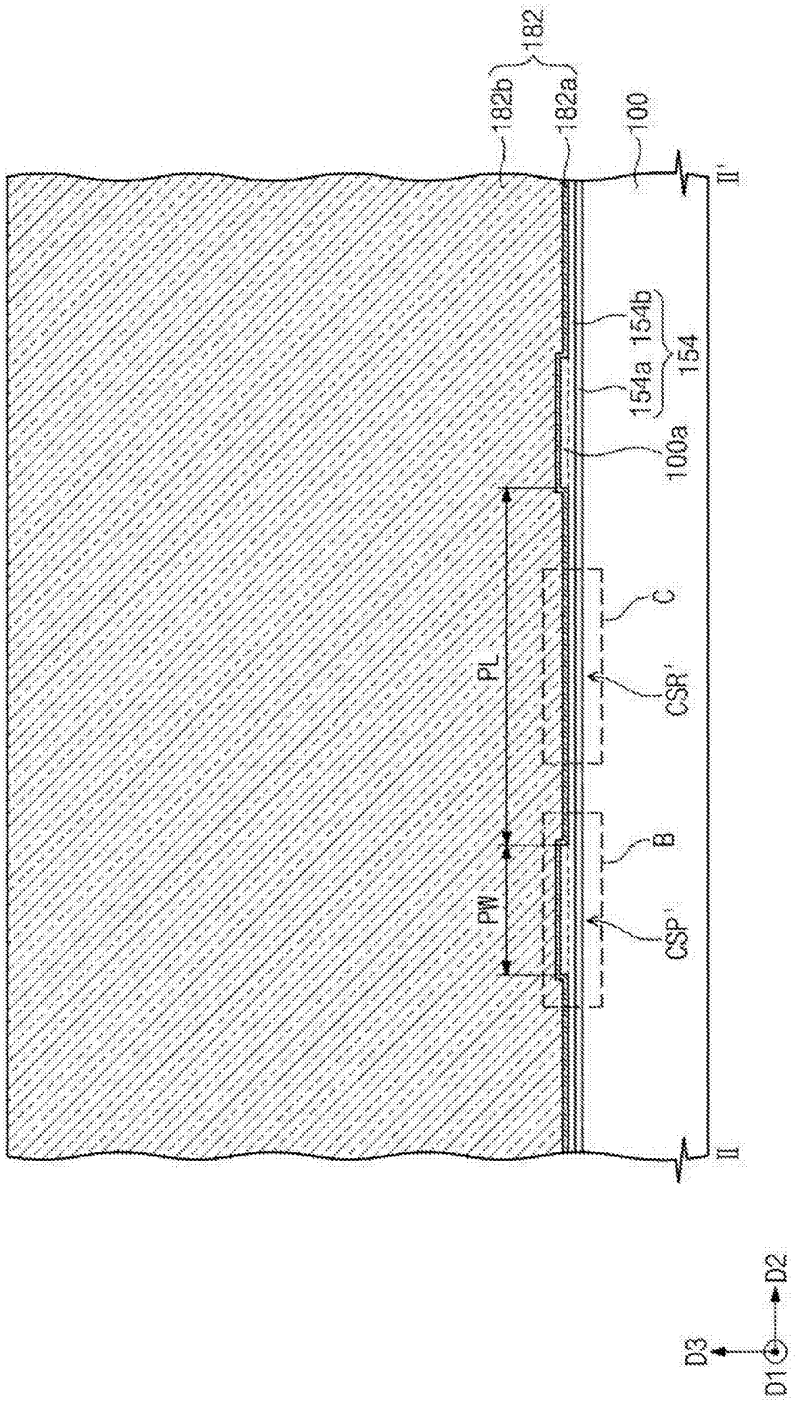

图 7B

Micron Ex. 1002, p. 321
Micron v. YMTC
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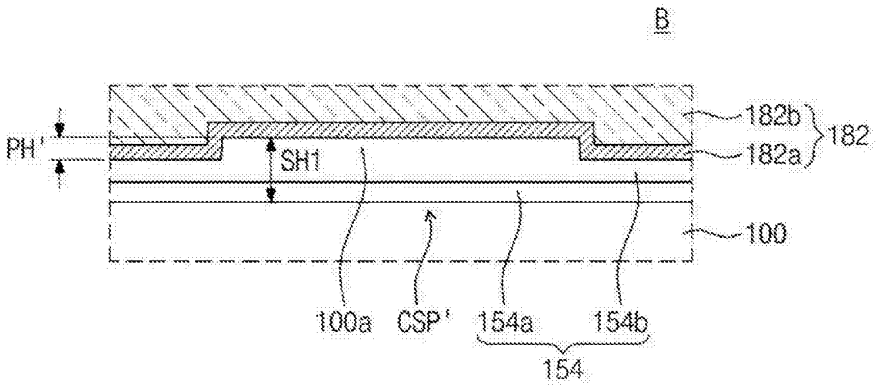

图 8A

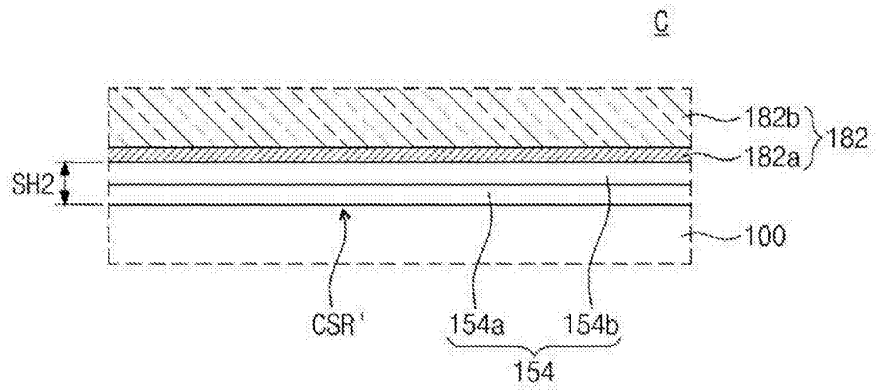

图 8B

Micron Ex. 1002, p. 322
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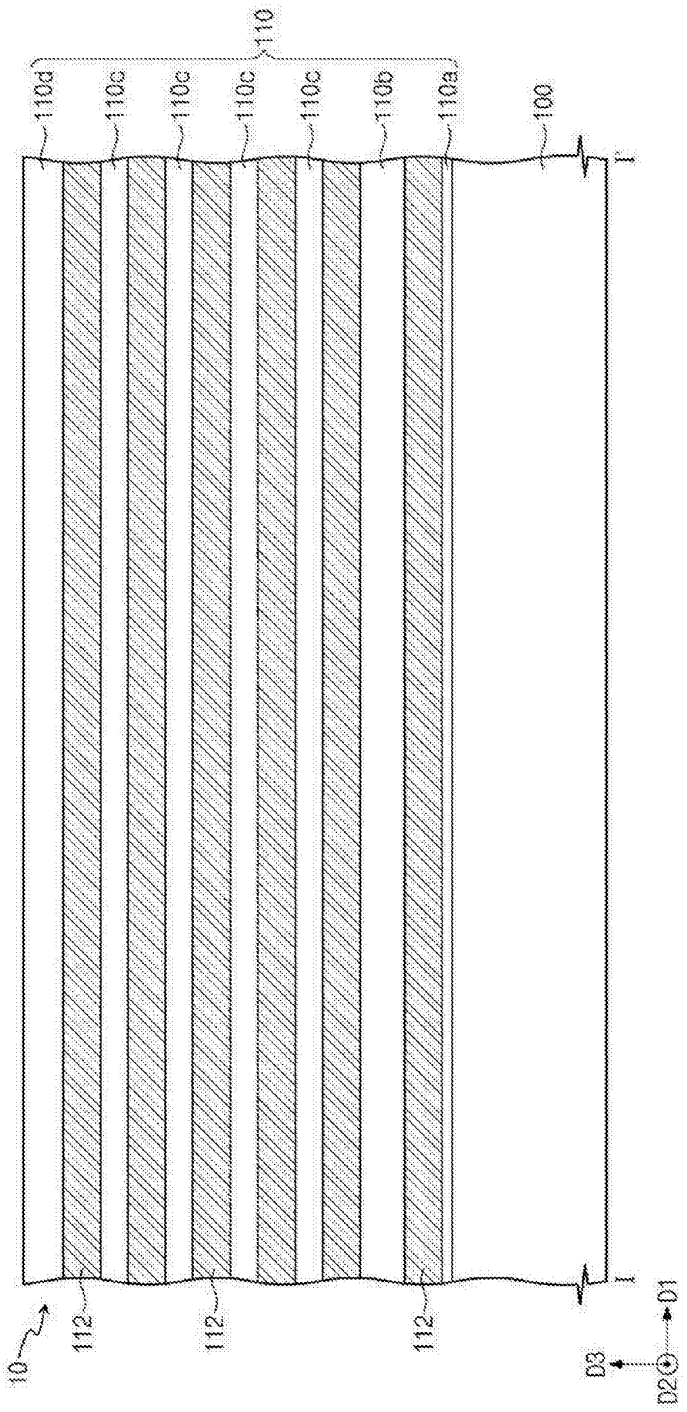

图 9

Micron Ex. 1002, p. 323
Micron v. YMTC
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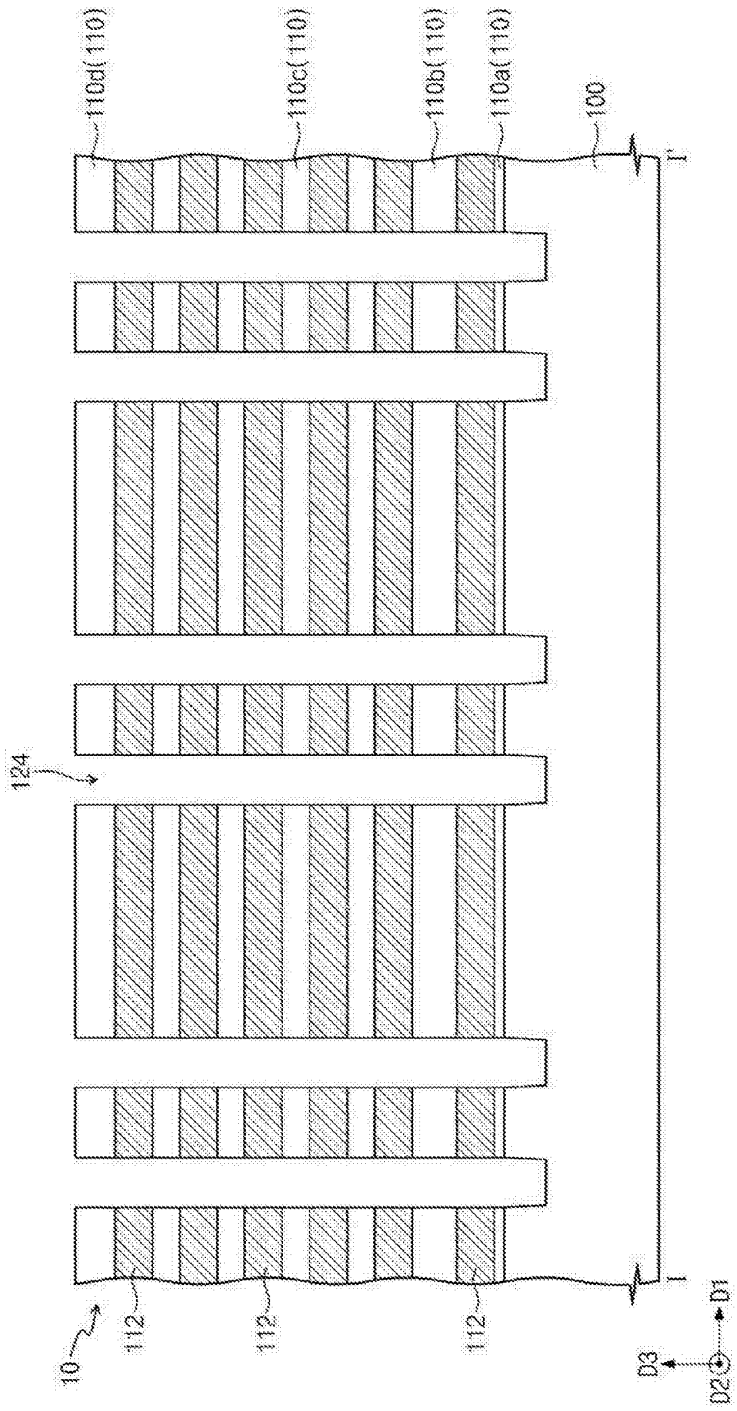

图 10

Micron Ex. 1002, p. 324
Micron v. YMTC
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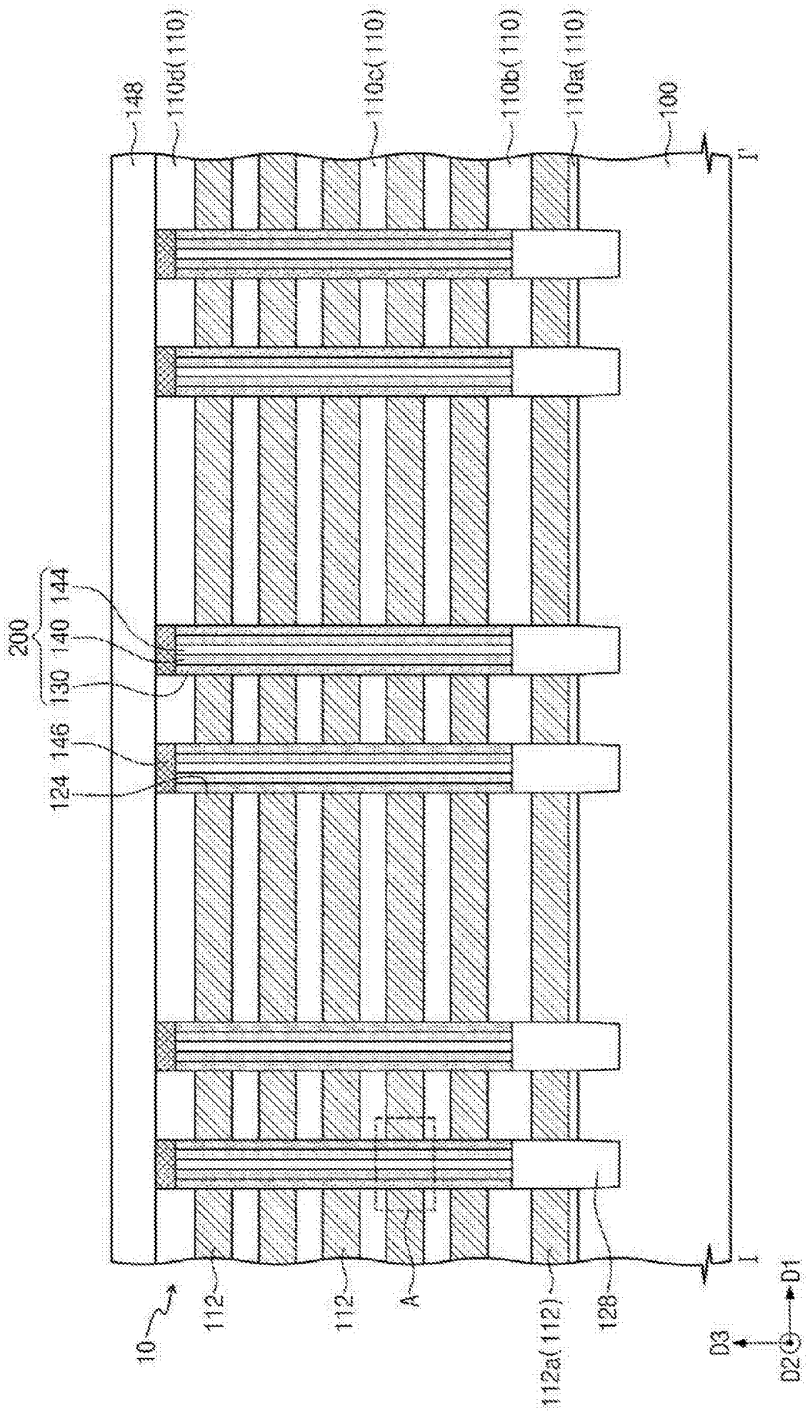

图 11A

Micron Ex. 1002, p. 325
Micron v. YMTC
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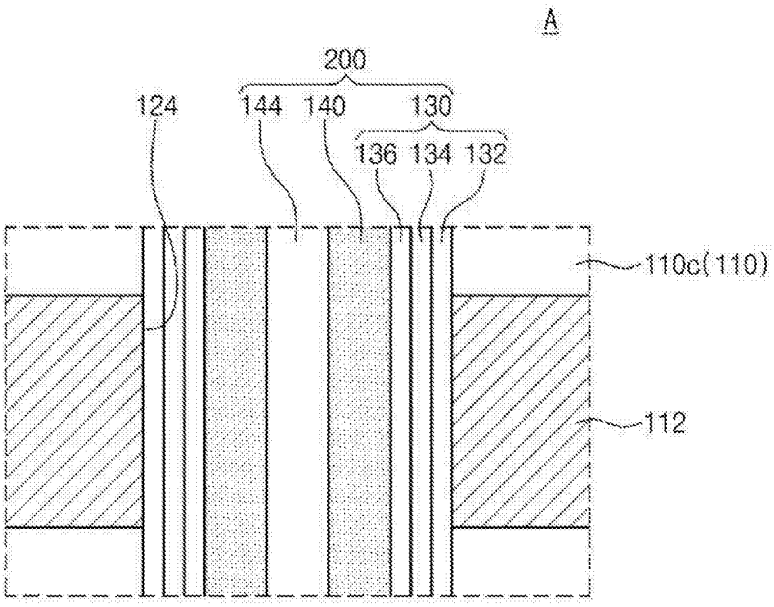

图 11B

Micron Ex. 1002, p. 326
Micron v. YMTC
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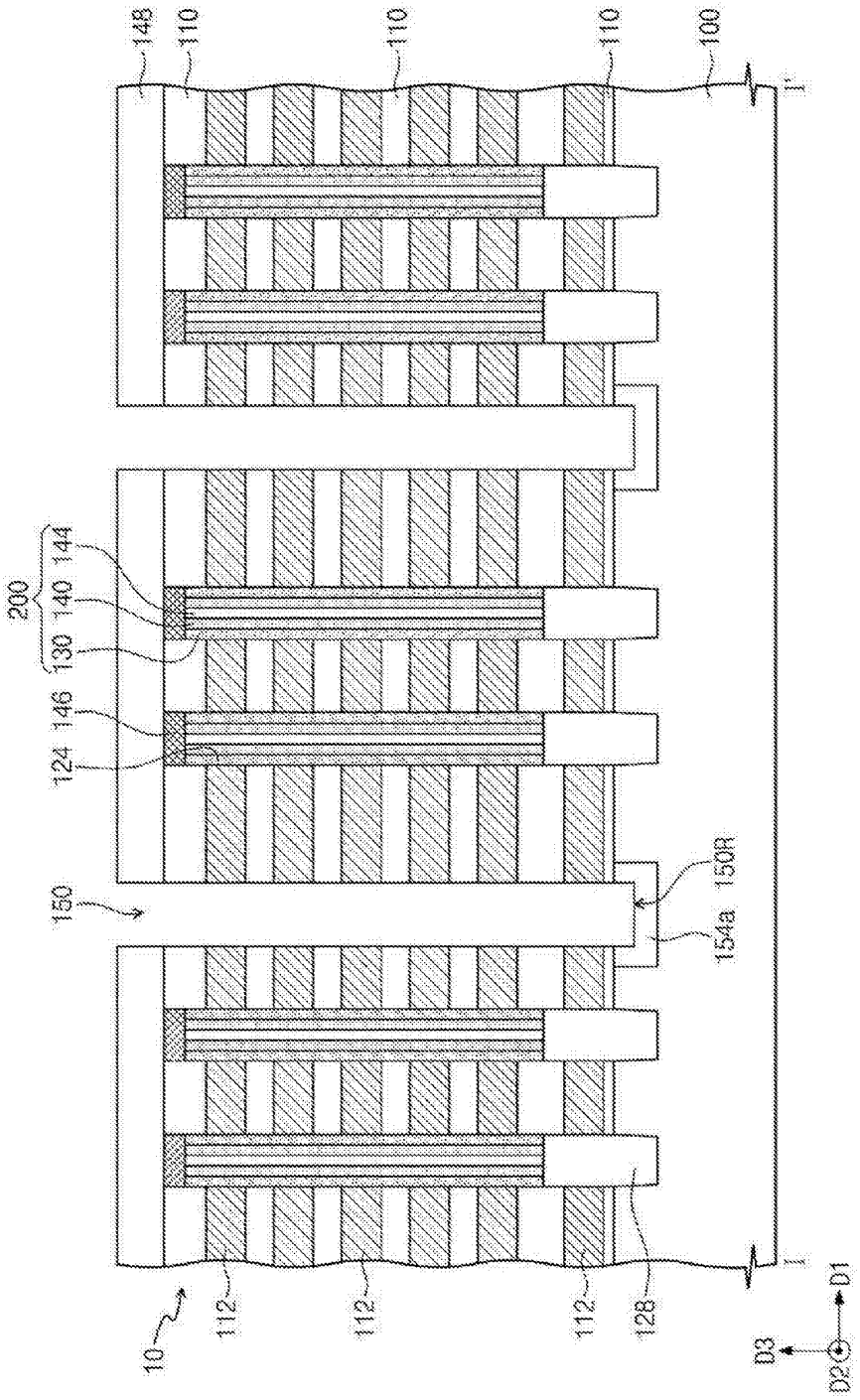

图 12

Micron Ex. 1002, p. 327
Micron v. YMTC
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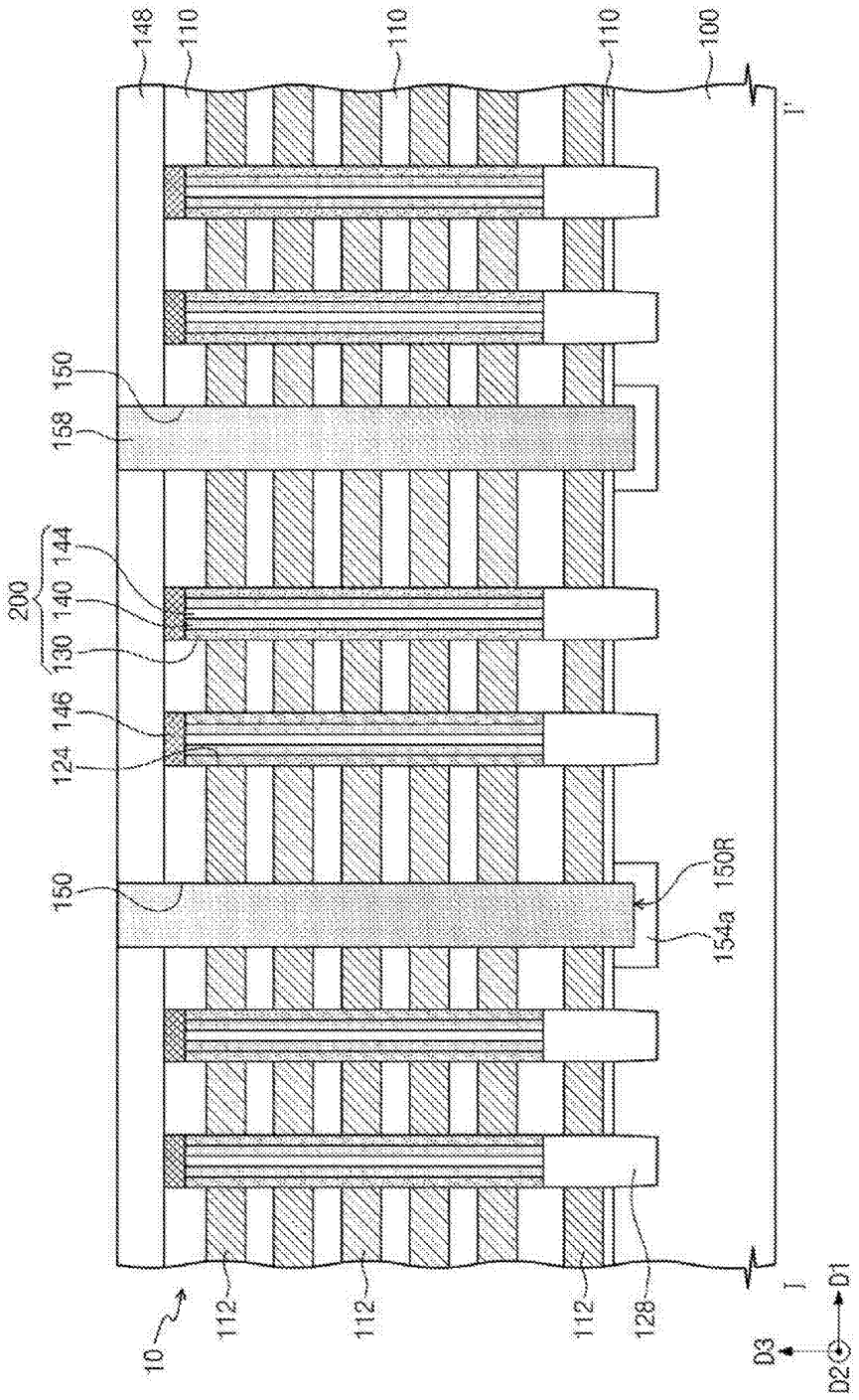

图 13

Micron Ex. 1002, p. 328
Micron v. YMTC
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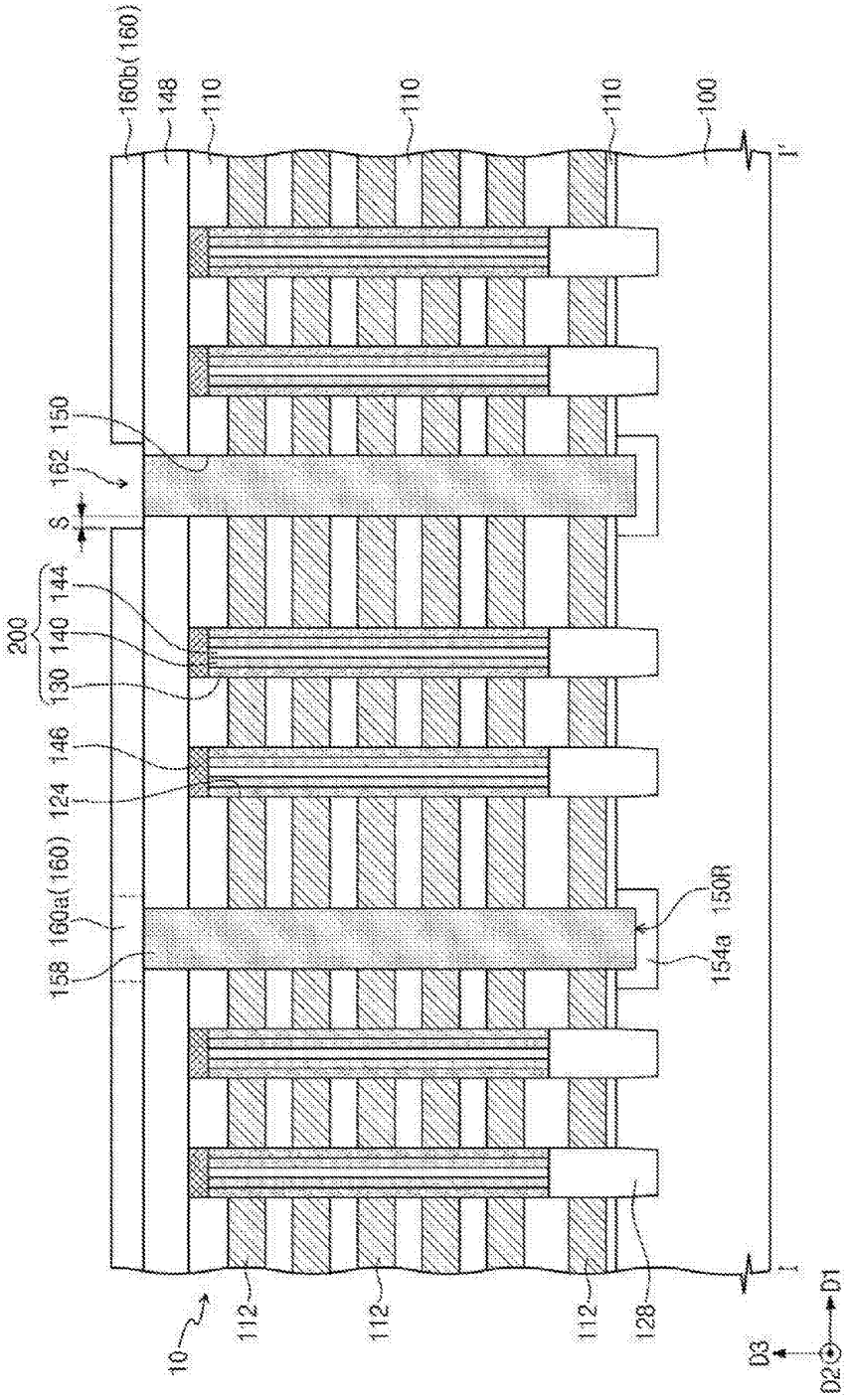

图 14A

Micron Ex. 1002, p. 329
Micron v. YMTC
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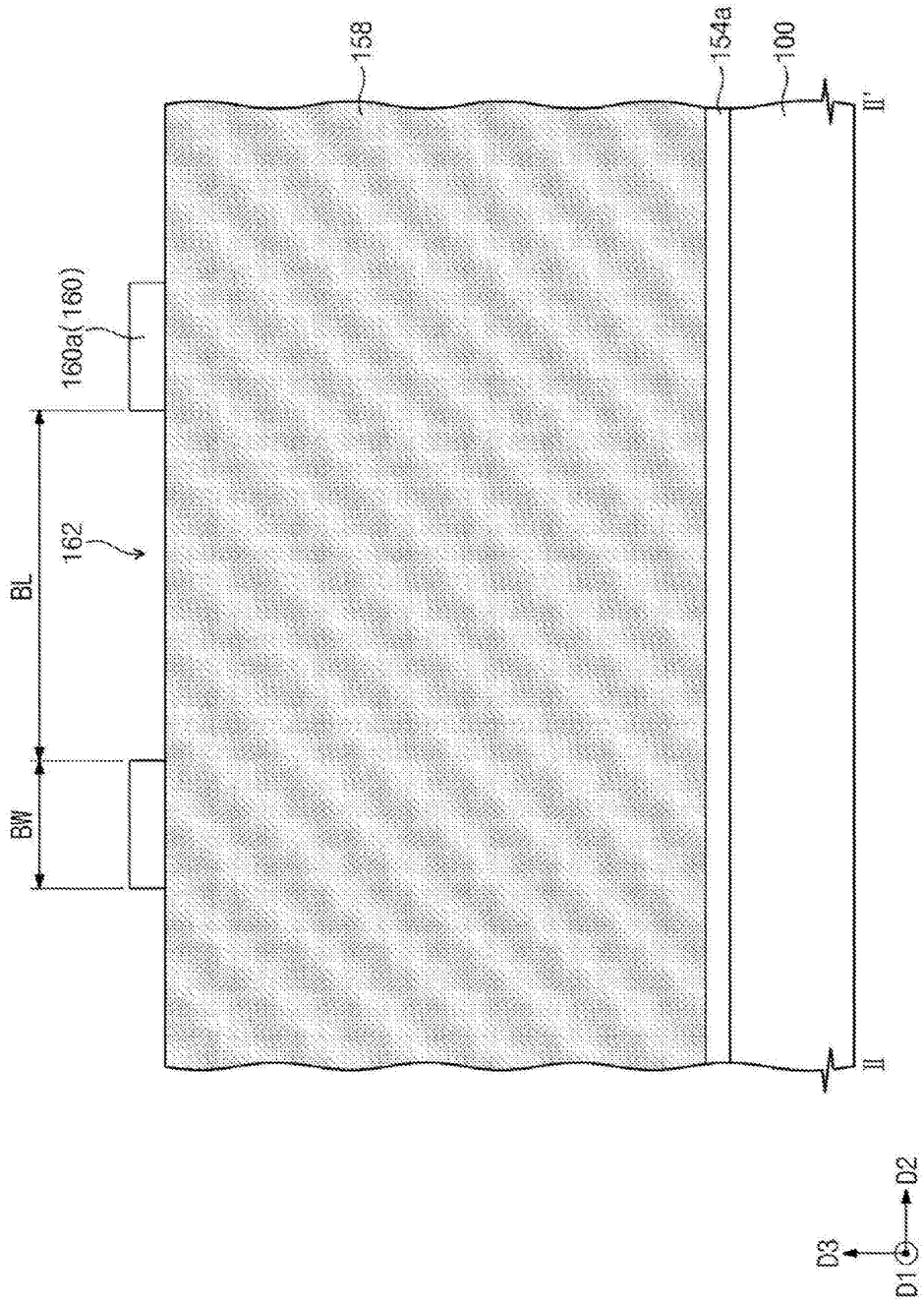

图 14B

Micron Ex. 1002, p. 330
Micron v. YMTC
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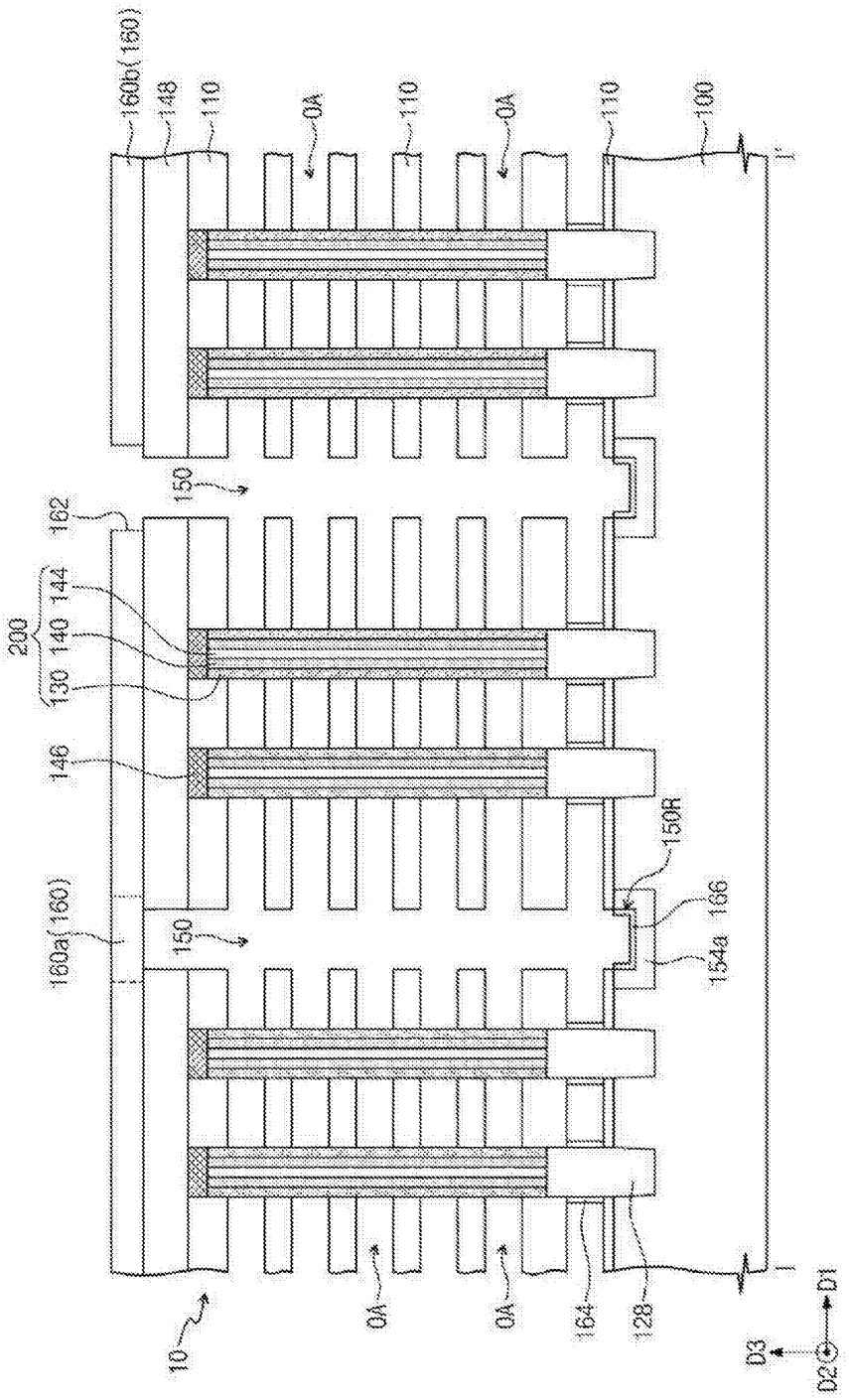

图 15A

Micron Ex. 1002, p. 331
Micron v. YMTC
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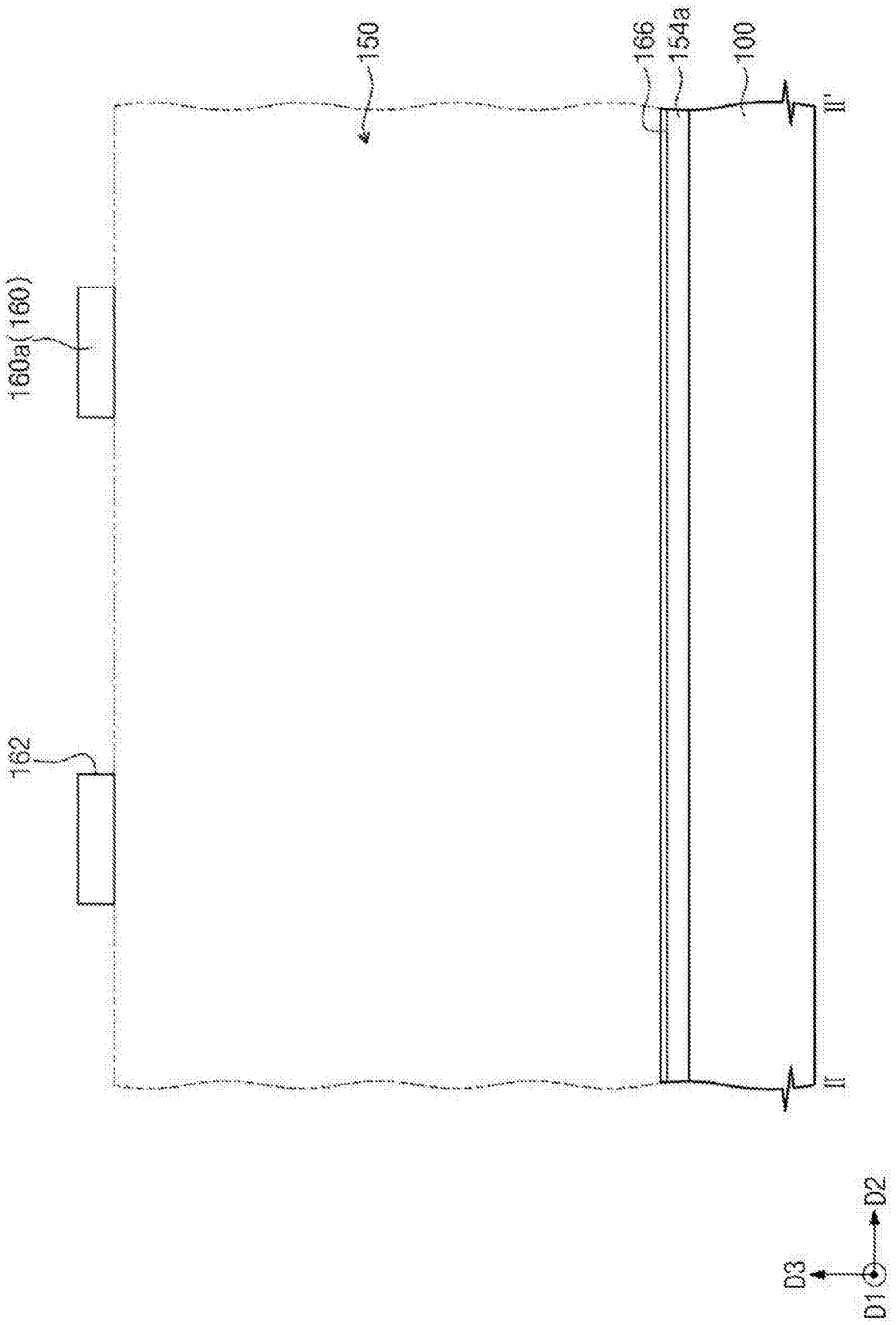

图 15B

Micron Ex. 1002, p. 332
Micron v. YMTC
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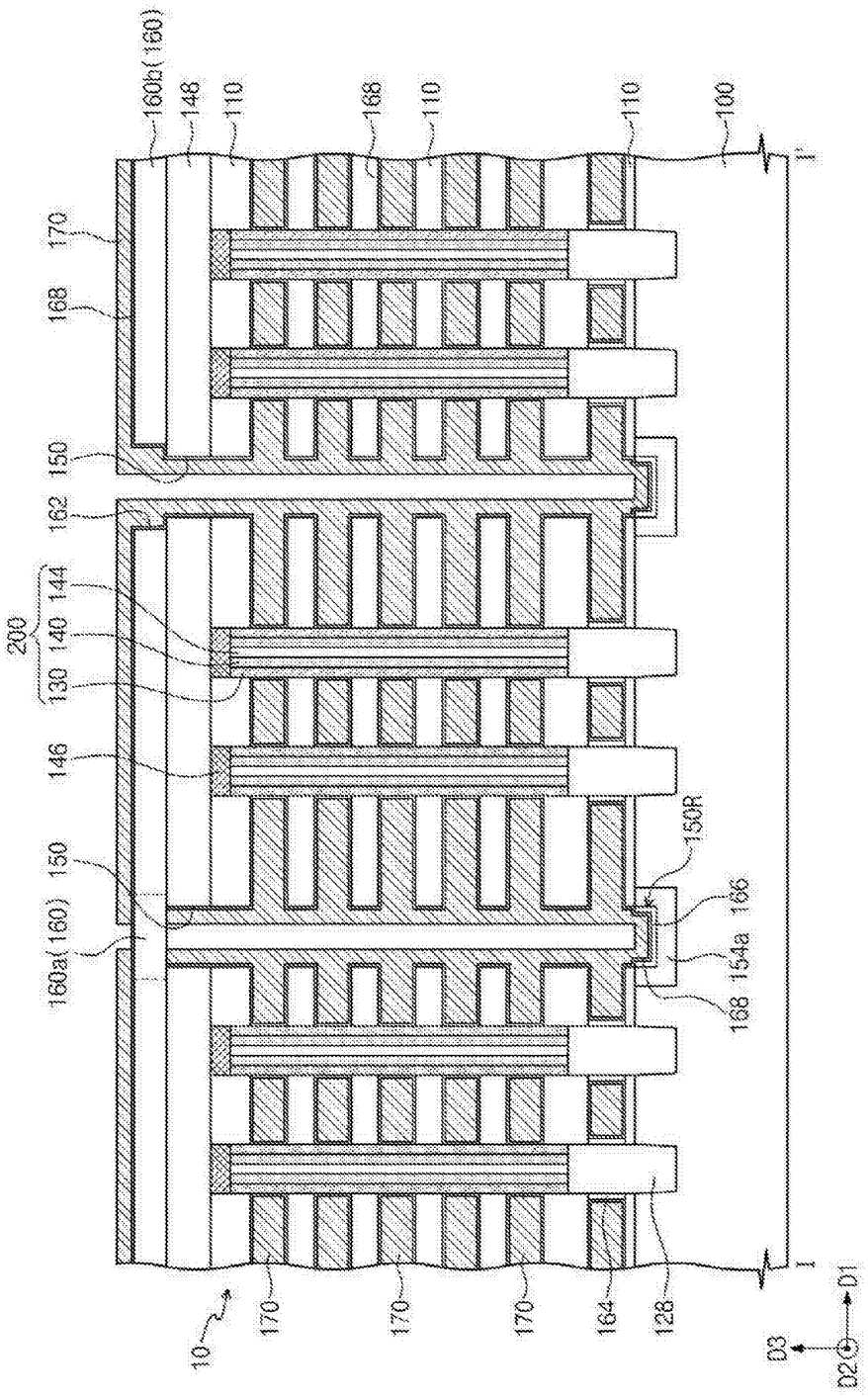

图 16A

Micron Ex. 1002, p. 333
Micron v. YMTC
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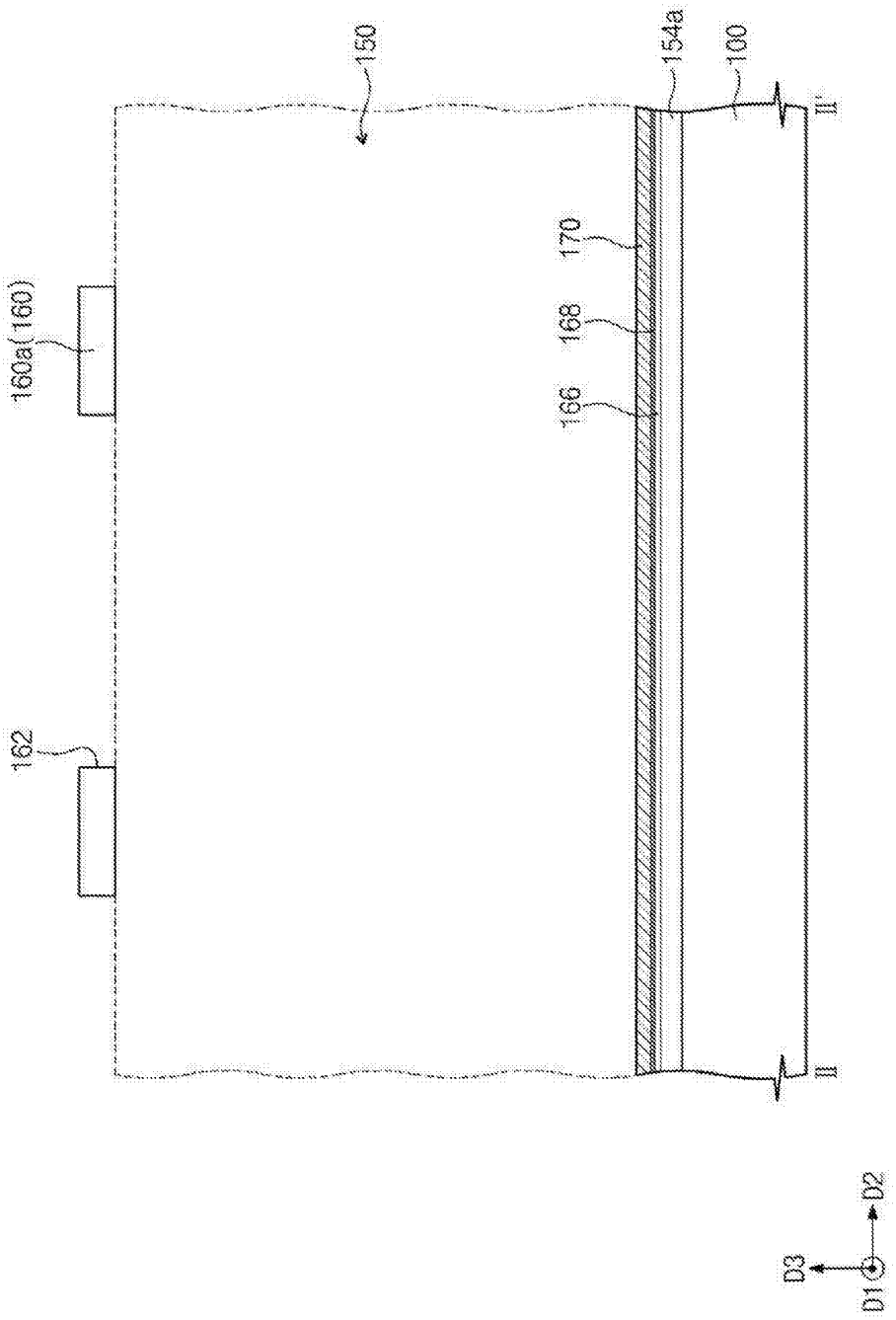

图 16B

Micron Ex. 1002, p. 334
Micron v. YMTC
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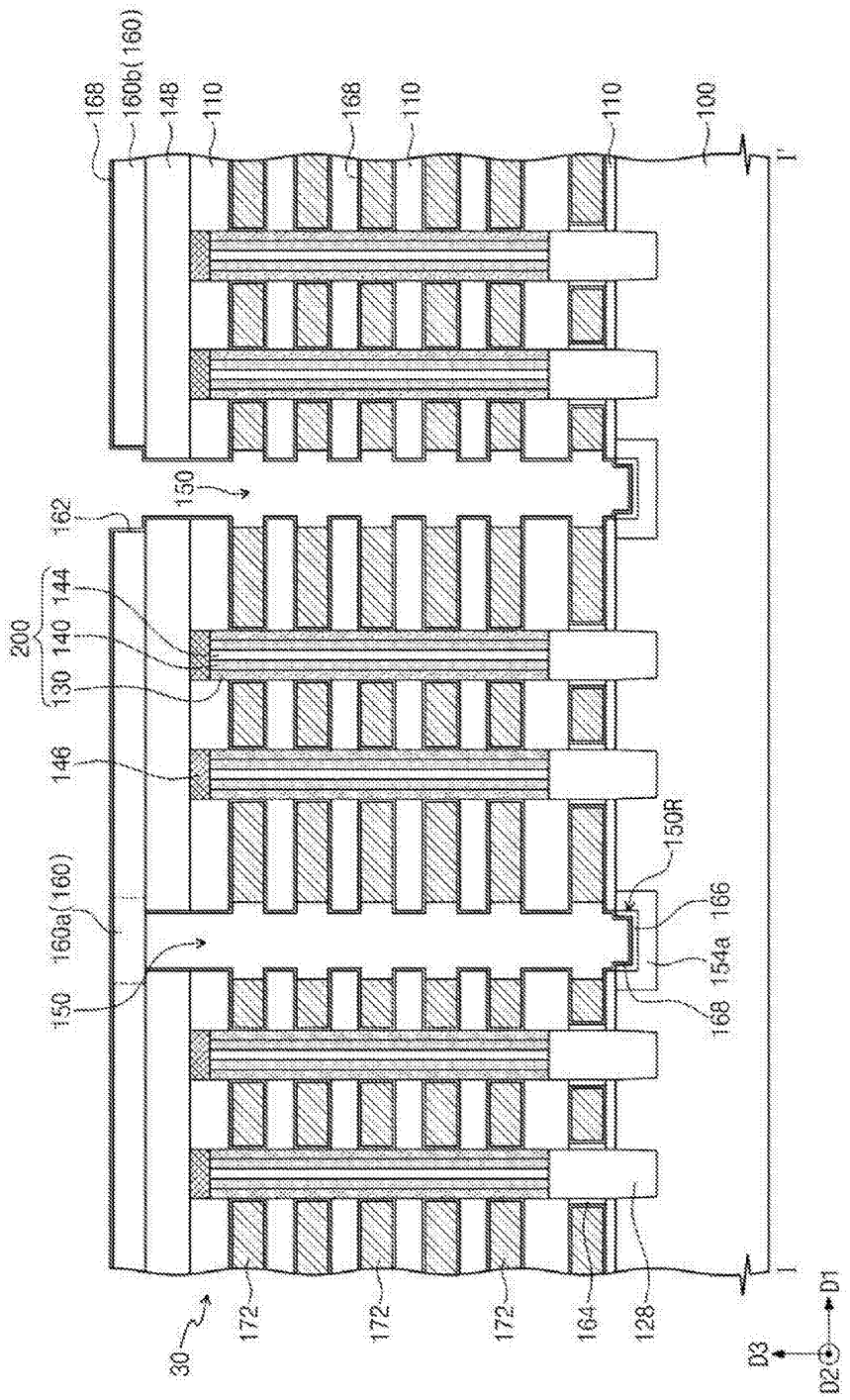

图 17A

Micron Ex. 1002, p. 335
Micron v. YMTC
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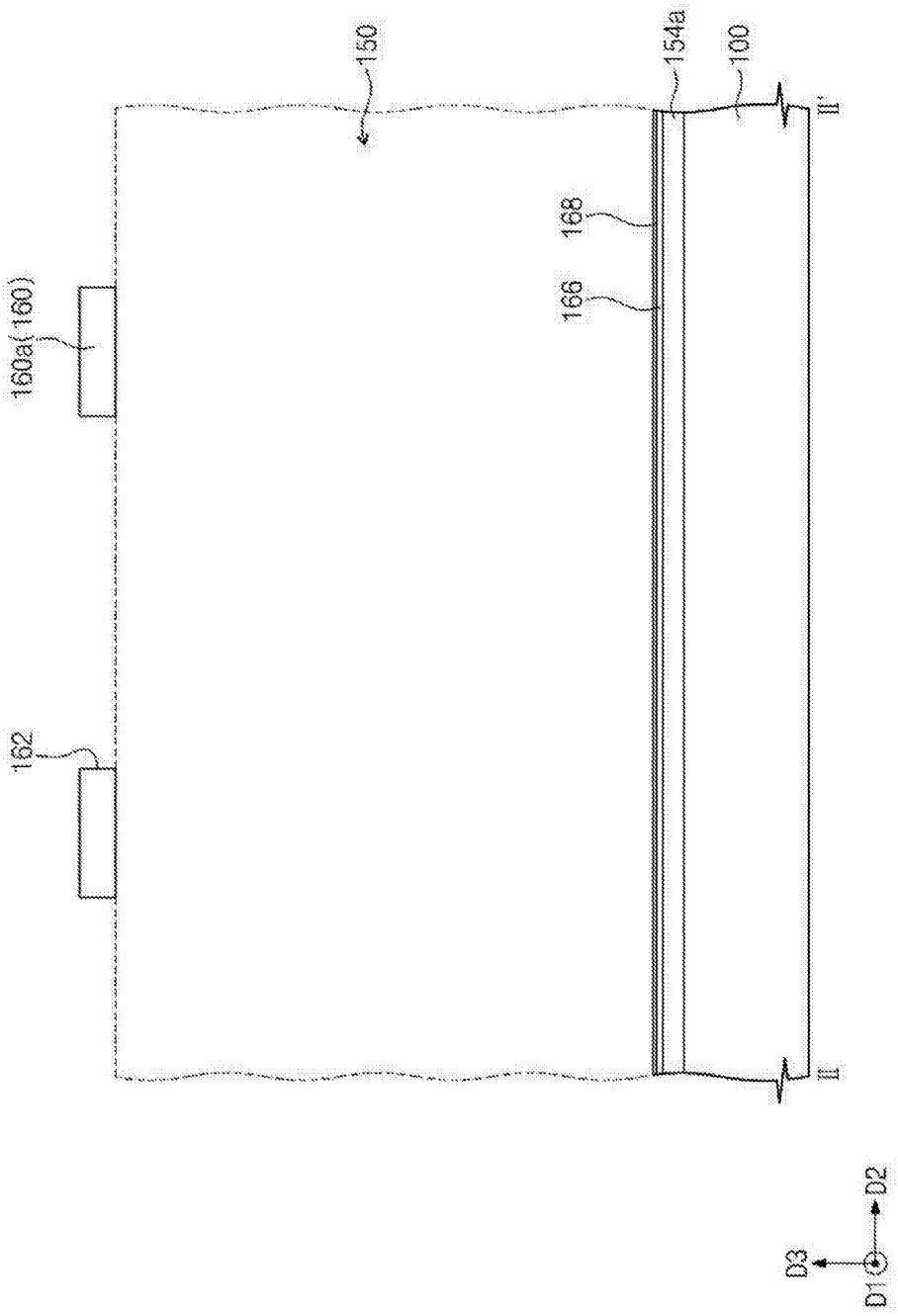

图 17B

Micron Ex. 1002, p. 336
Micron v. YMTC
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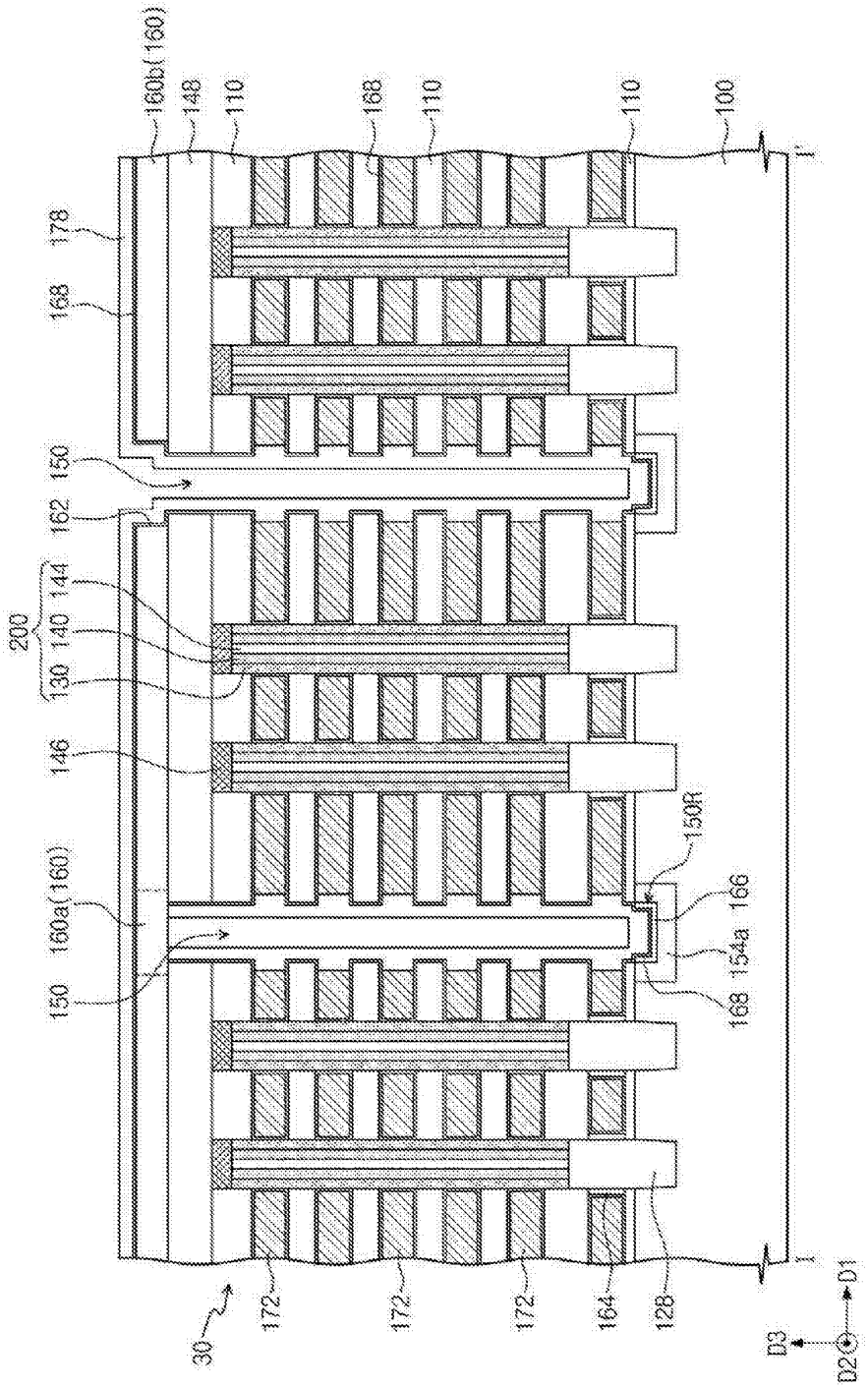

图 18A

Micron Ex. 1002, p. 337
Micron v. YMTC
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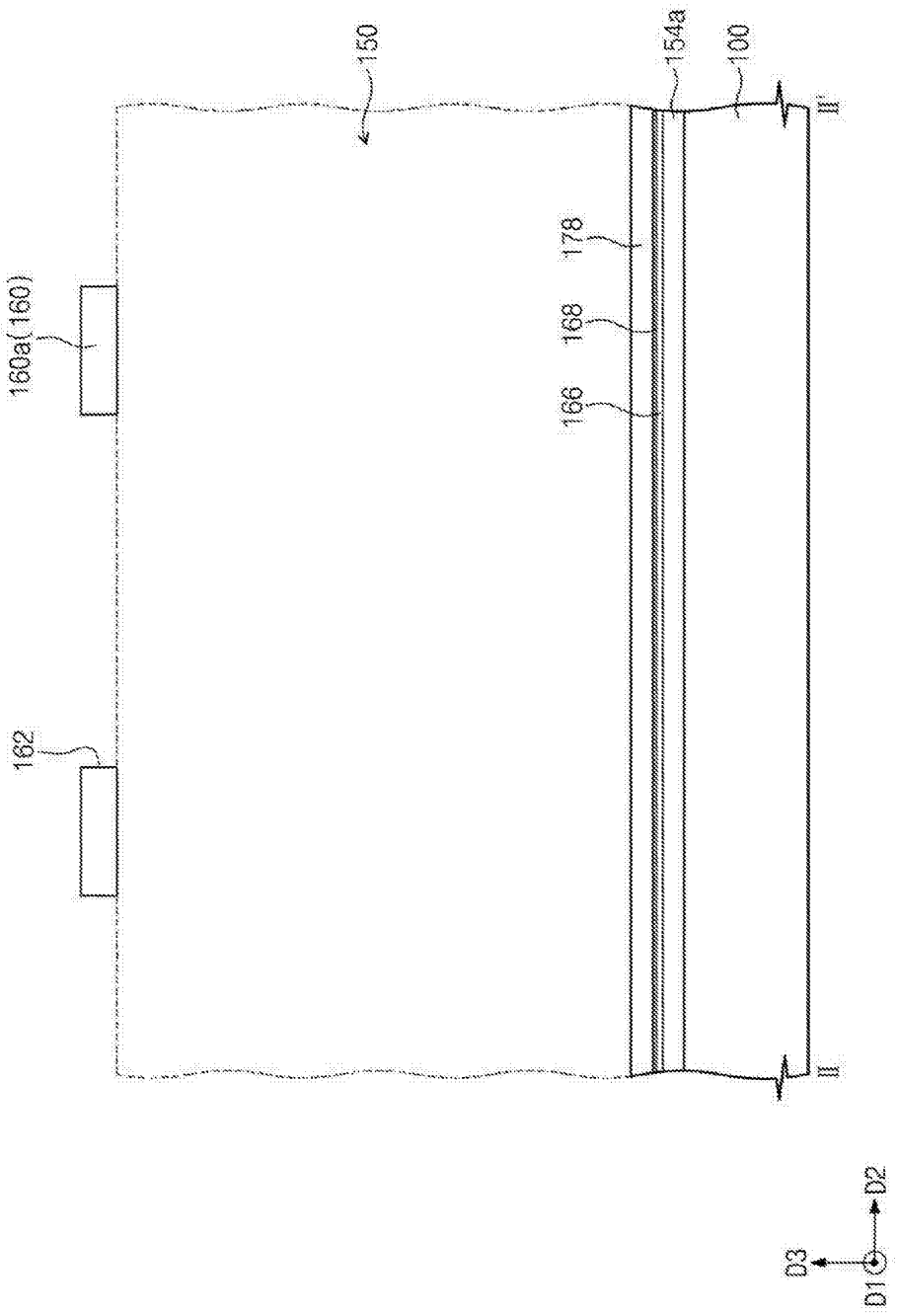

图 18B

Micron Ex. 1002, p. 338
Micron v. YMTC
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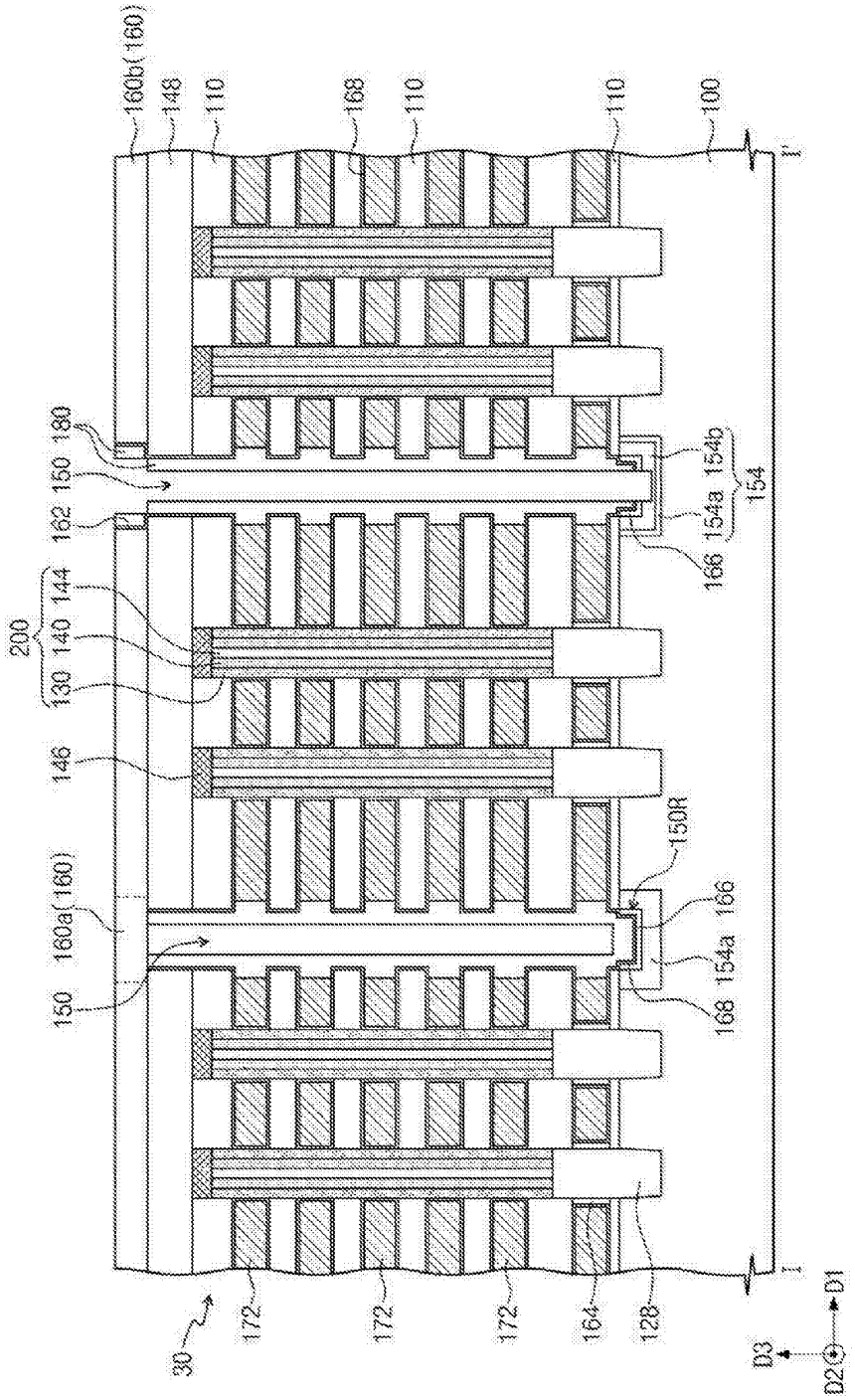

图 19A

Micron Ex. 1002, p. 339
Micron v. YMTC
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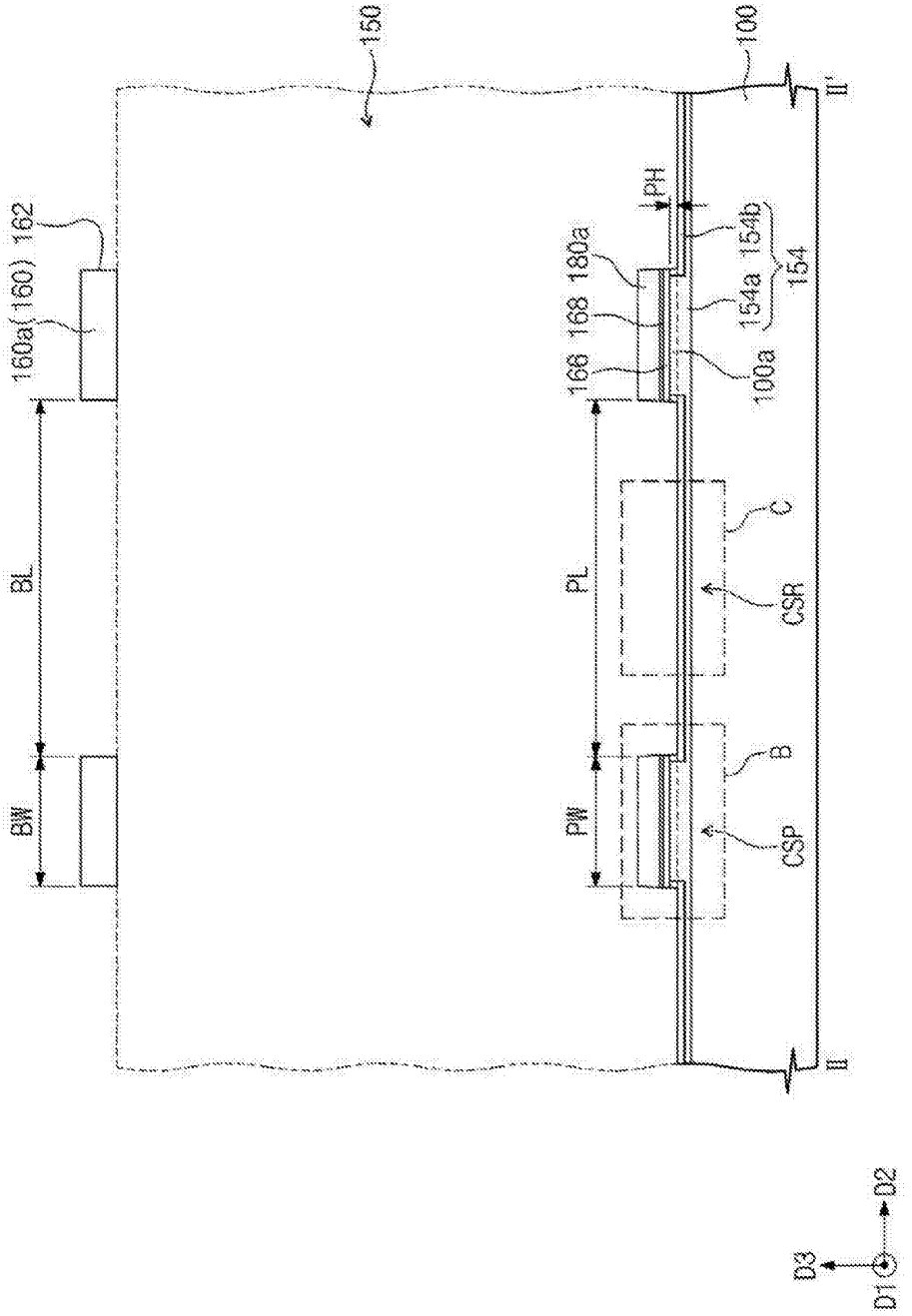

图 19B

Micron Ex. 1002, p. 340
Micron v. YMTC
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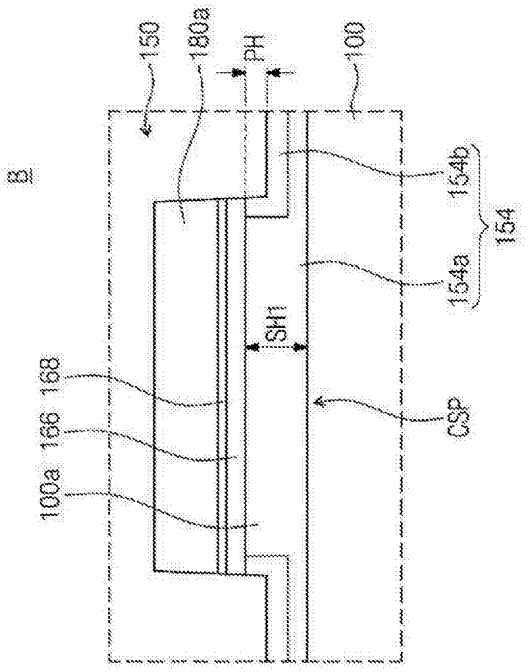

图 19C

Micron Ex. 1002, p. 341
Micron v. YMTC
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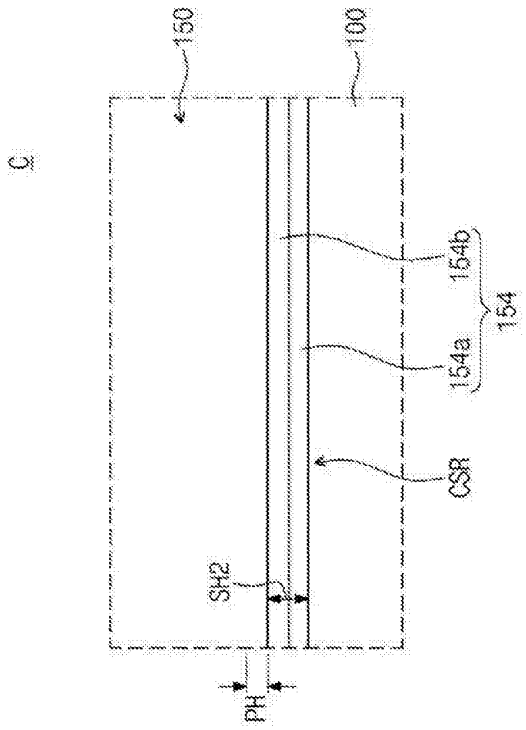

图 19D

Micron Ex. 1002, p. 342
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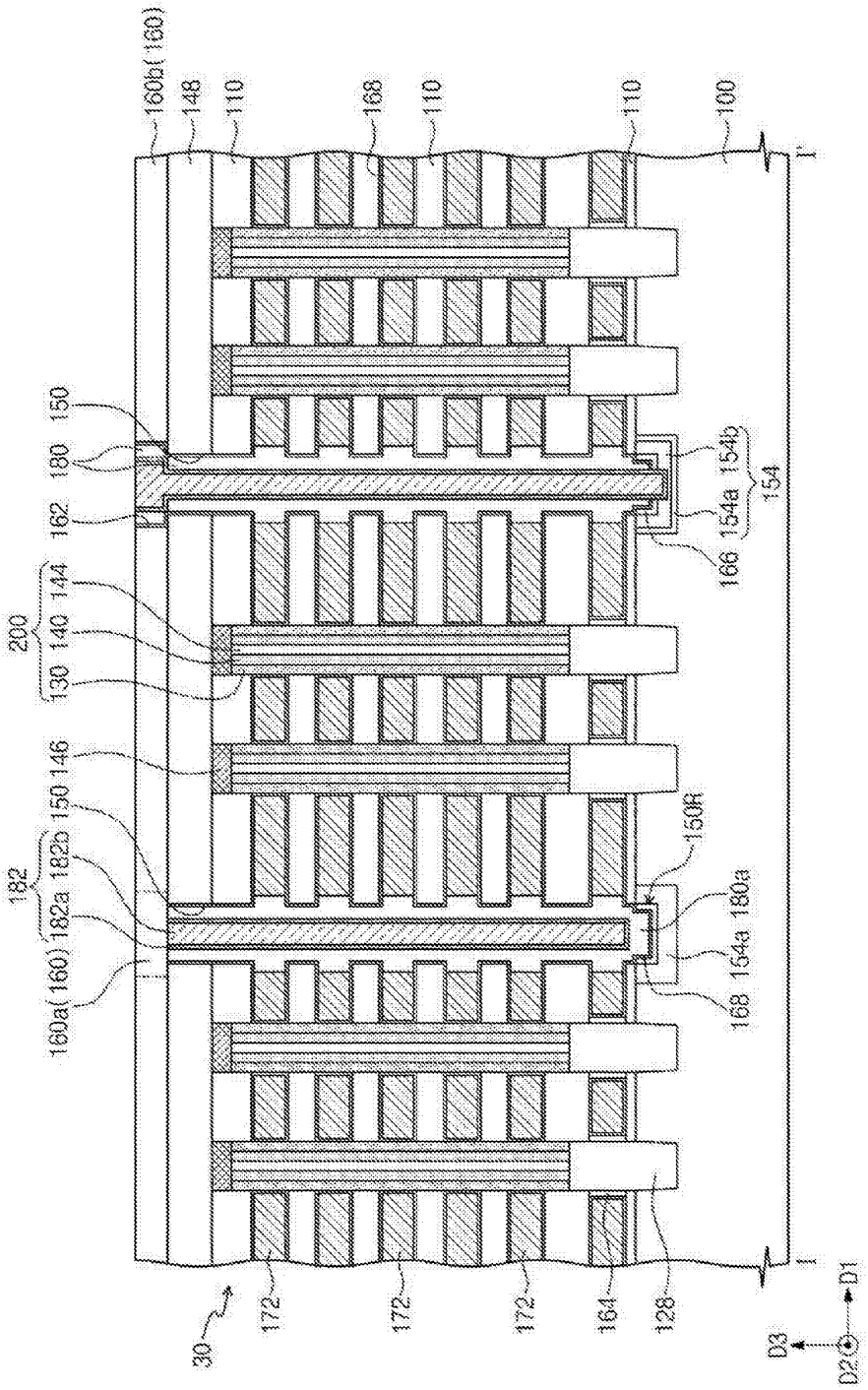

图 20A

Micron Ex. 1002, p. 343
Micron v. YMTC
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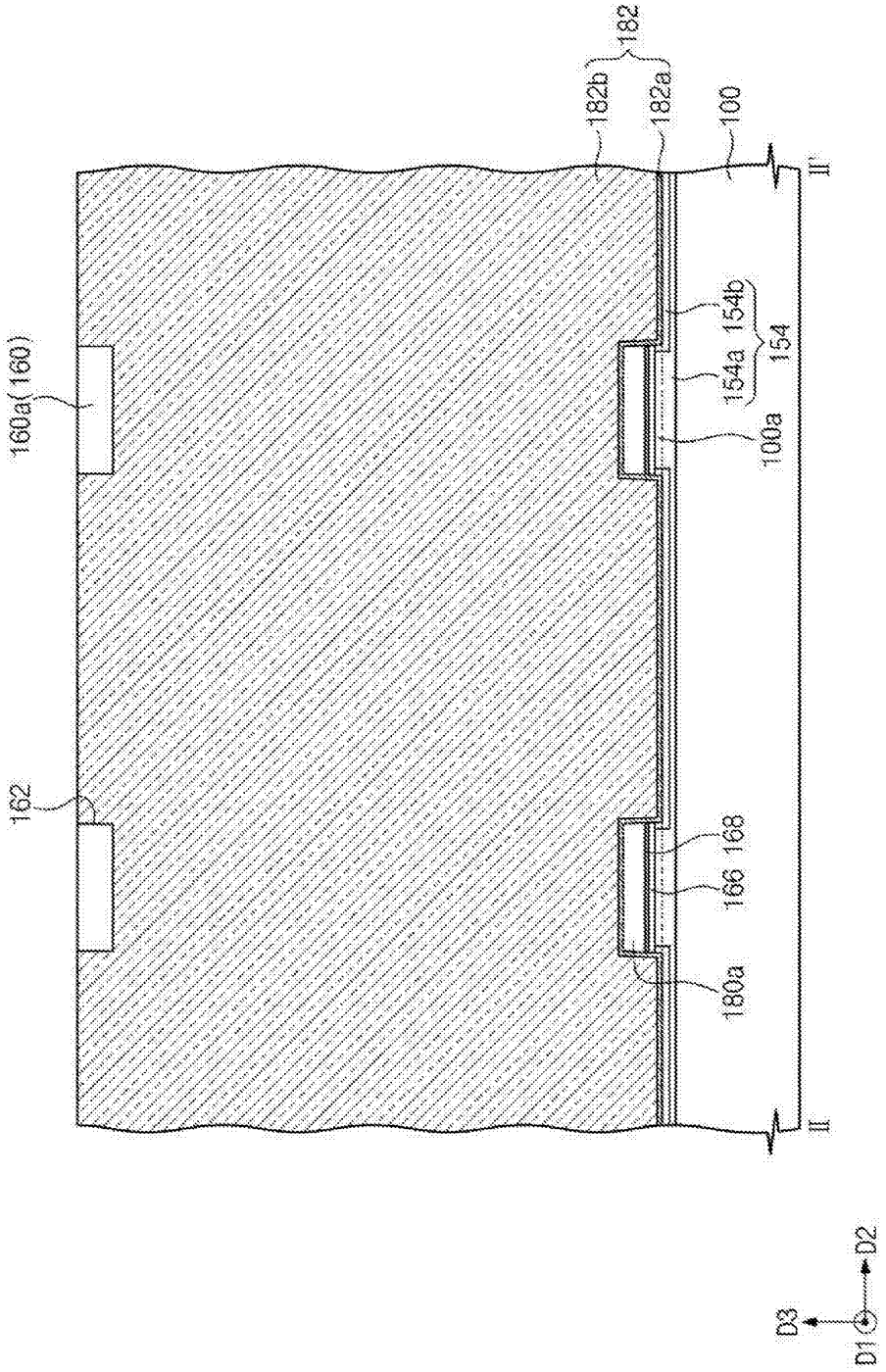

图 20B

Micron Ex. 1002, p. 344
Micron v. YMTC
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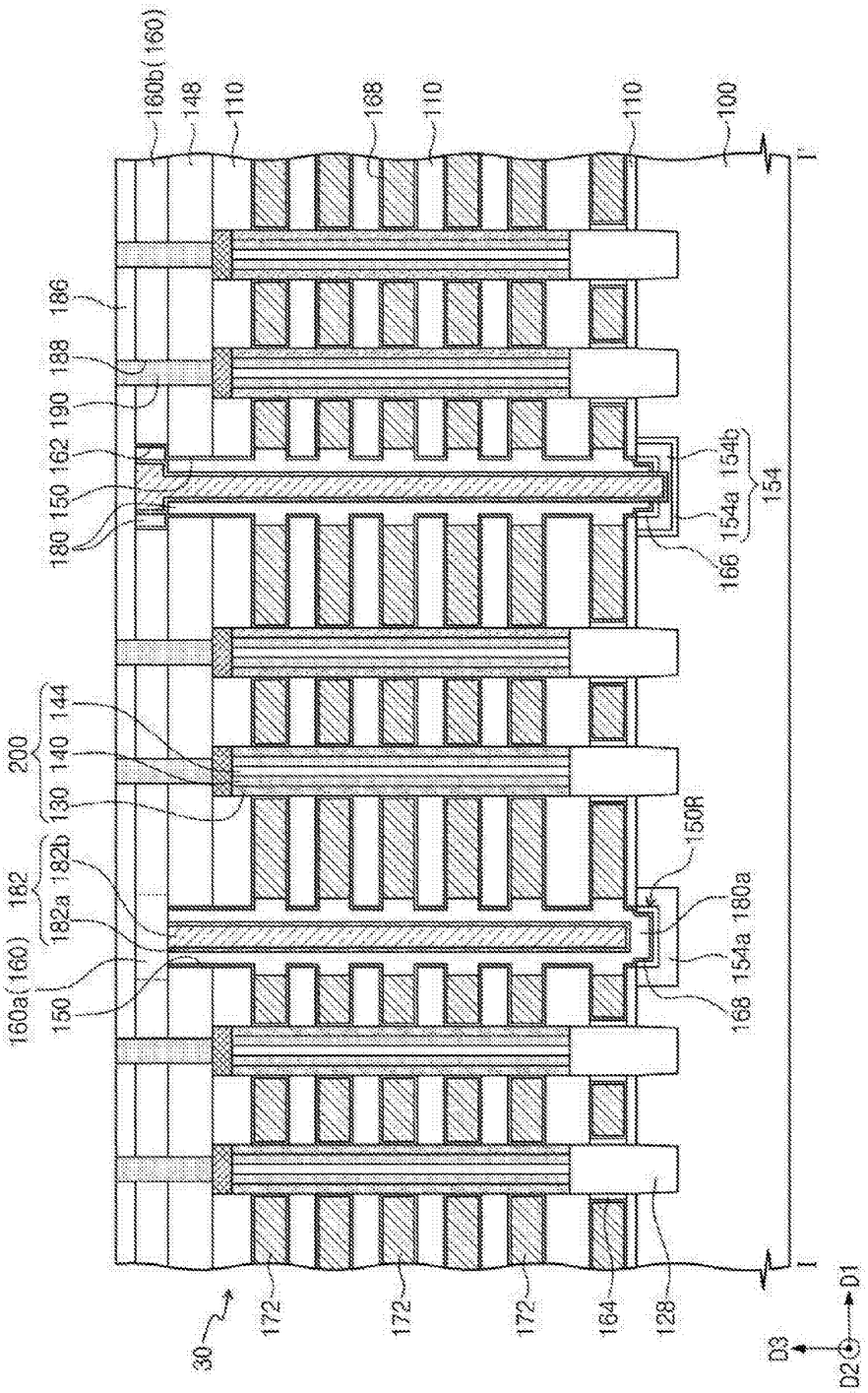

图 21A

Micron Ex. 1002, p. 345
Micron v. YMTC
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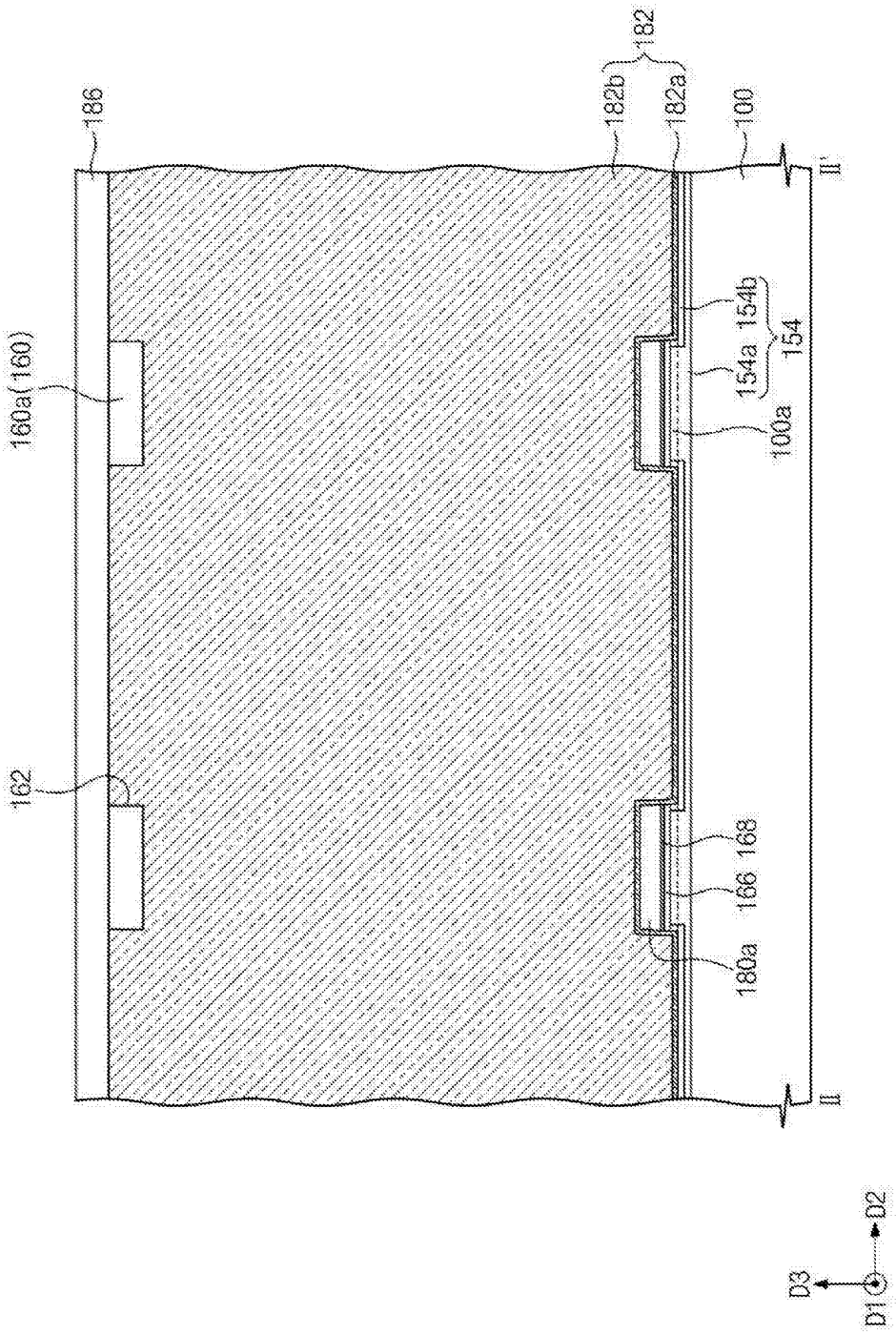

图 21B

Micron Ex. 1002, p. 346
Micron v. YMTC
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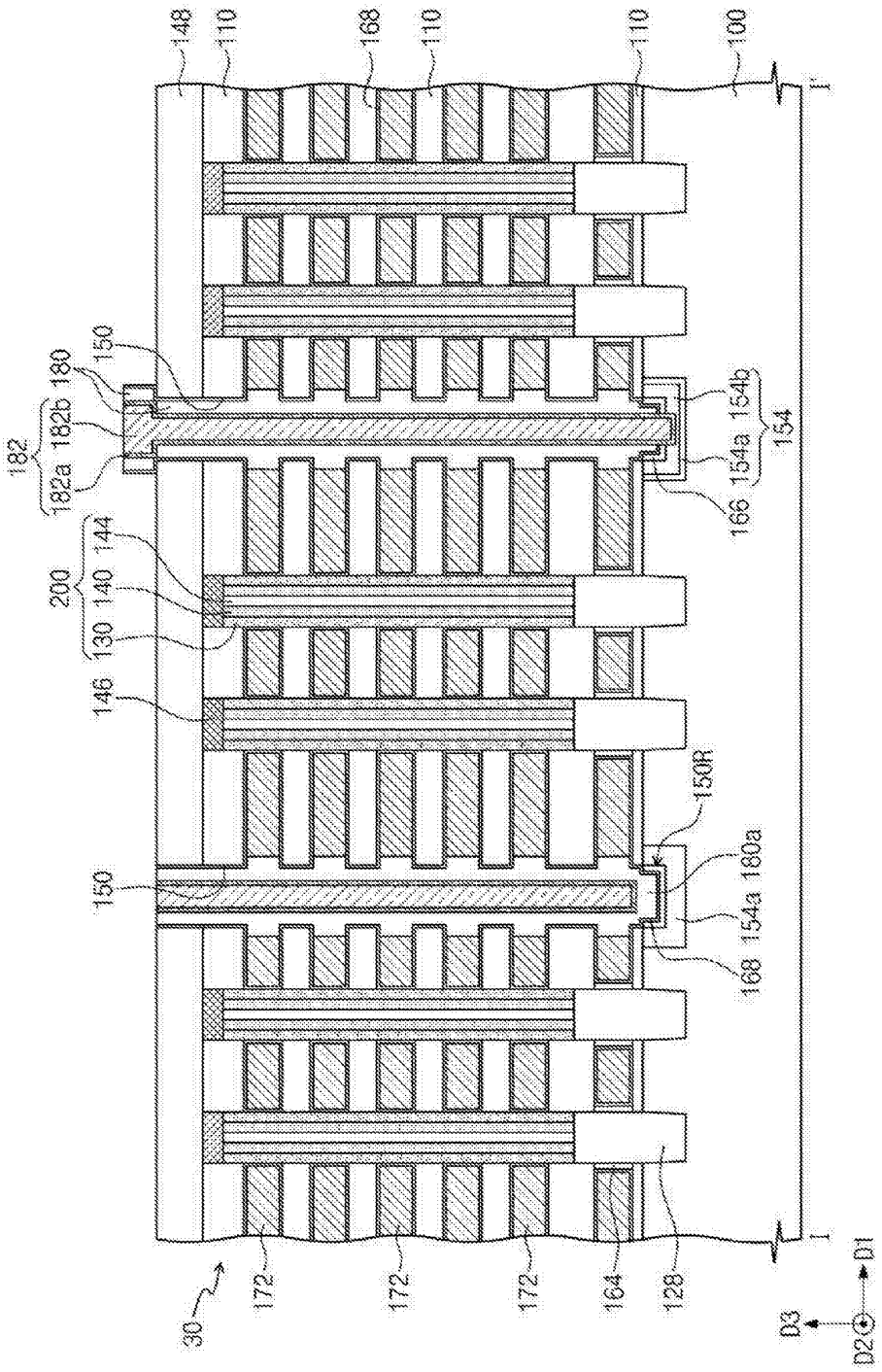

图 22A

Micron Ex. 1002, p. 347
Micron v. YMTC
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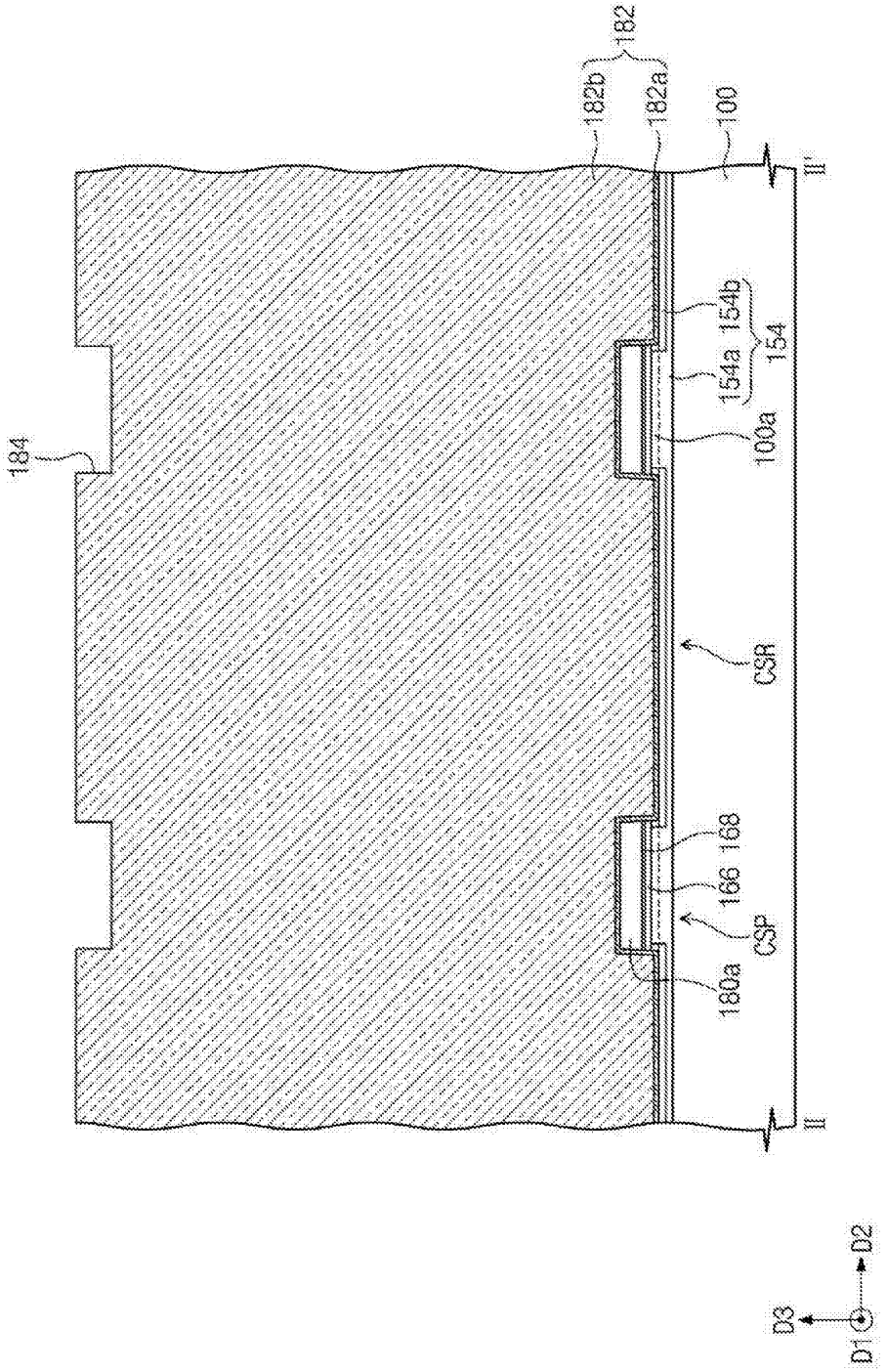

图 22B

Micron Ex. 1002, p. 348
Micron v. YMTC
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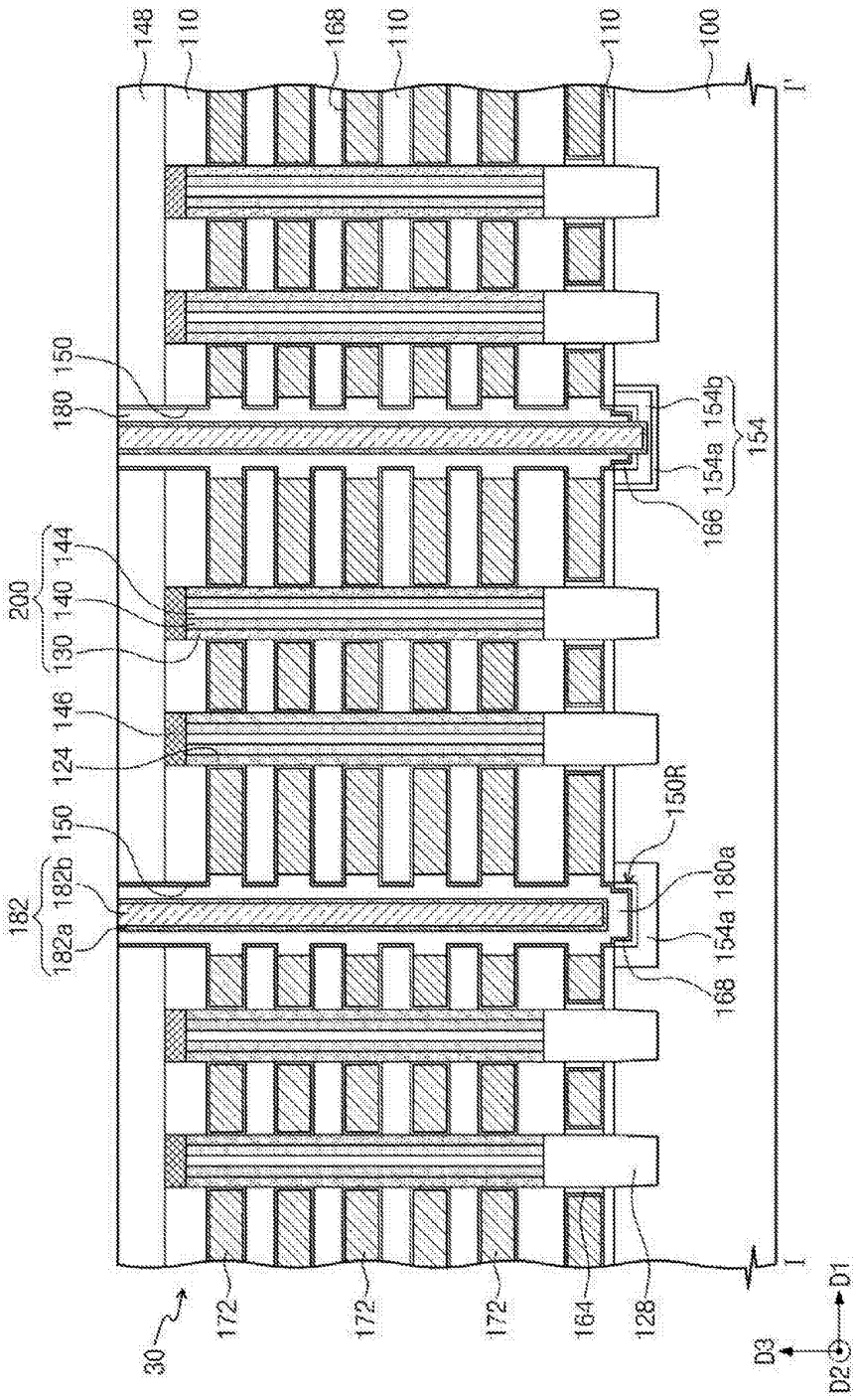

图 23A

Micron Ex. 1002, p. 349
Micron v. YMTC
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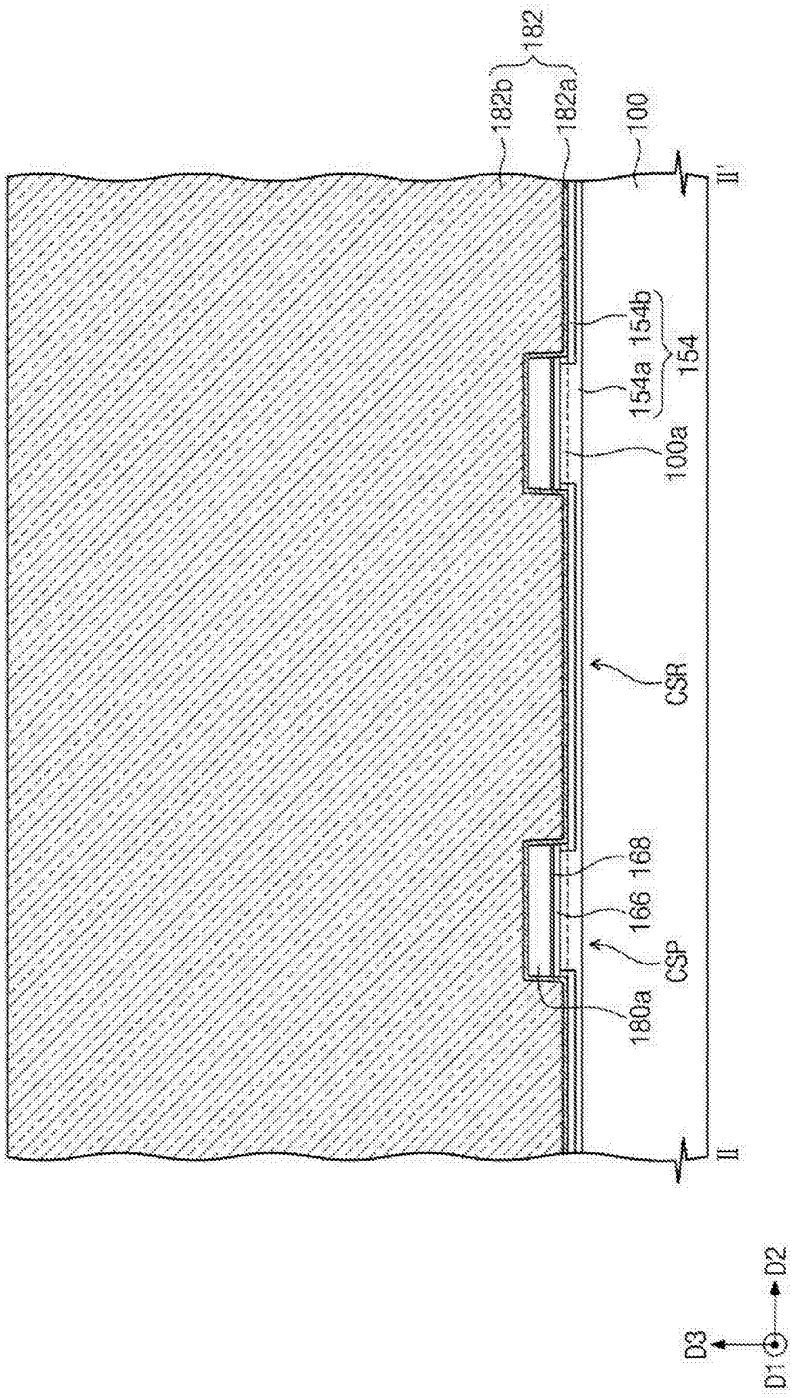

图 23B

Micron Ex. 1002, p. 350
Micron v. YMTC
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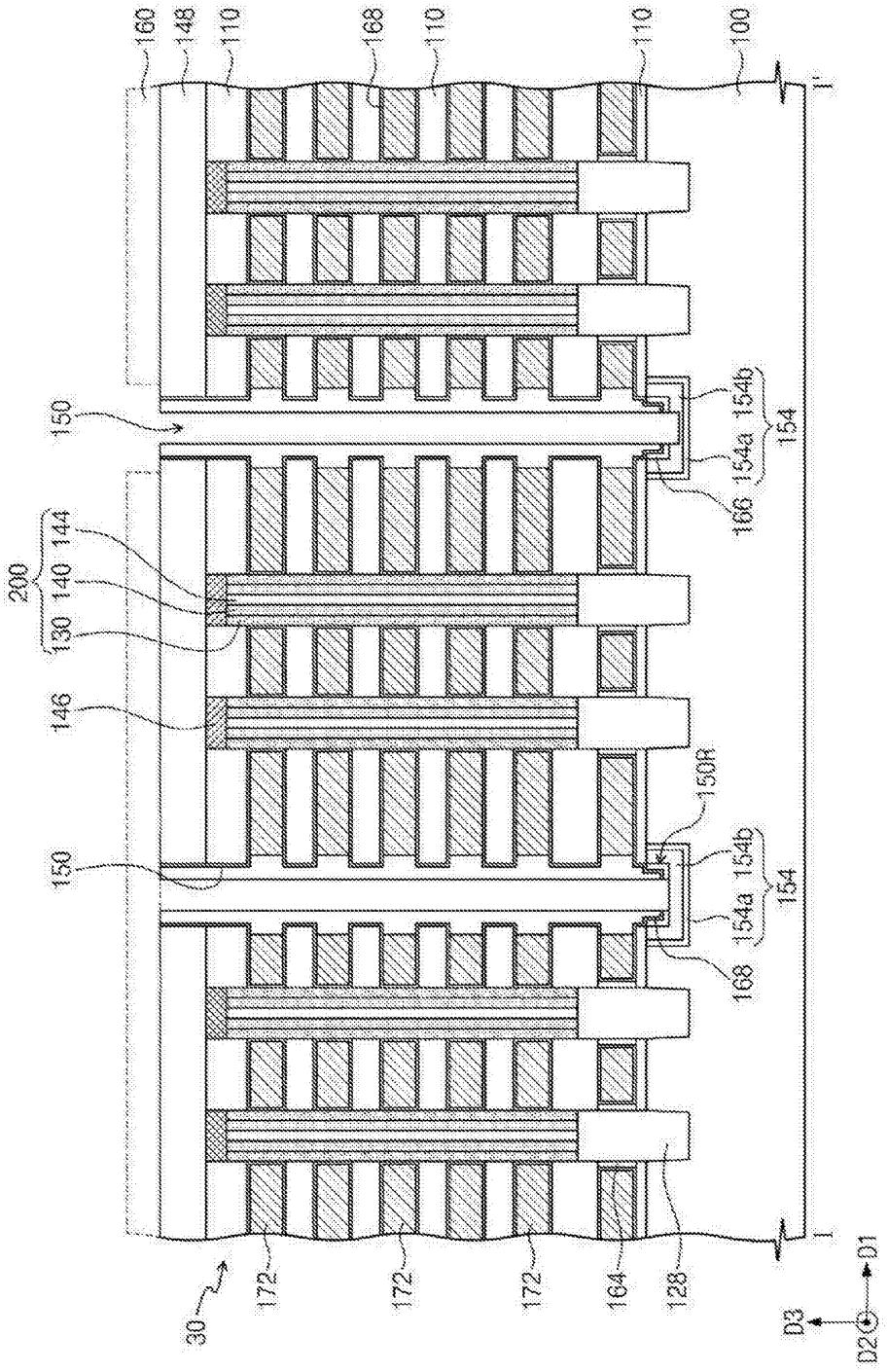

图 24A

Micron Ex. 1002, p. 351
Micron v. YMTC
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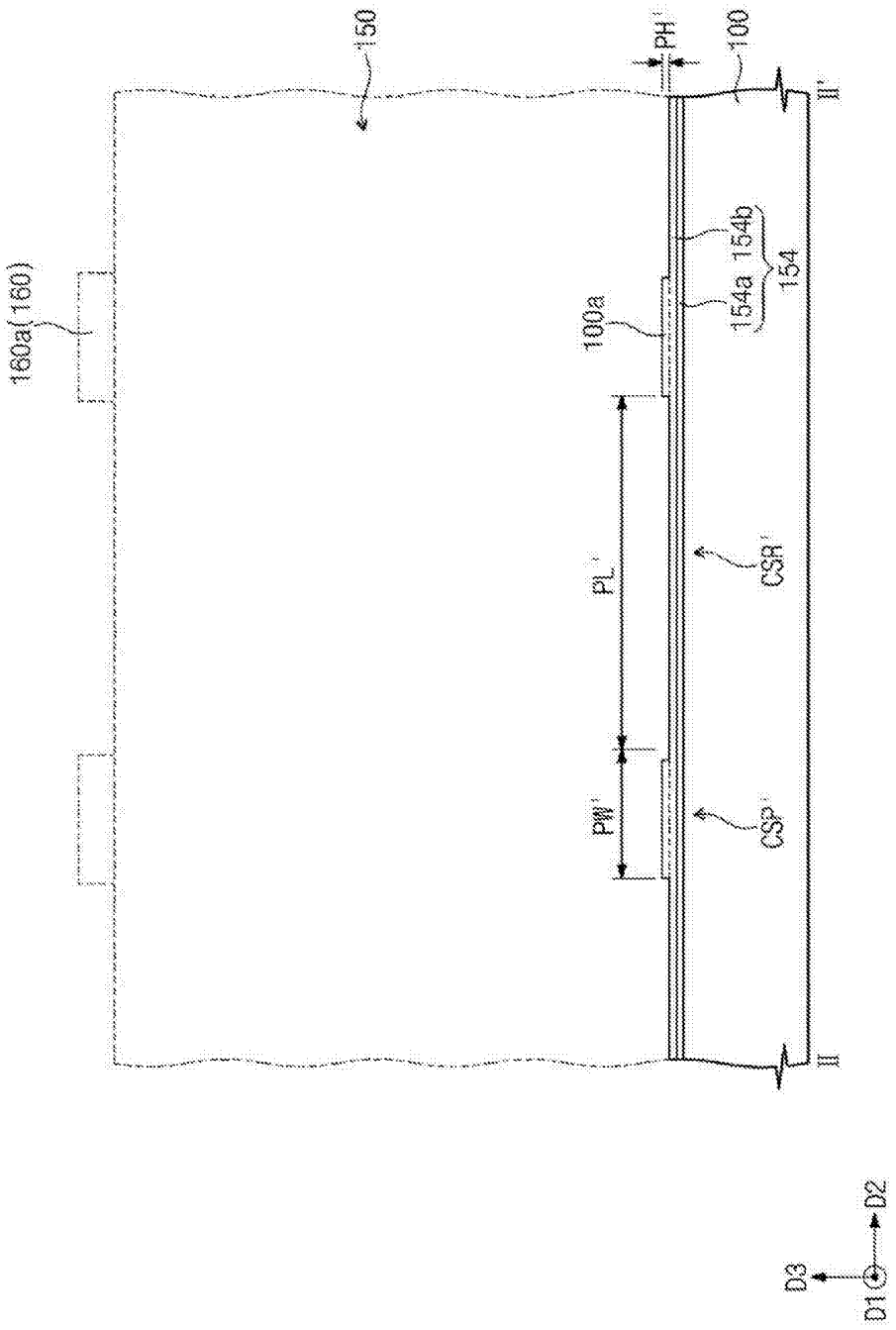

图 24B

Micron Ex. 1002, p. 352
Micron v. YMTC
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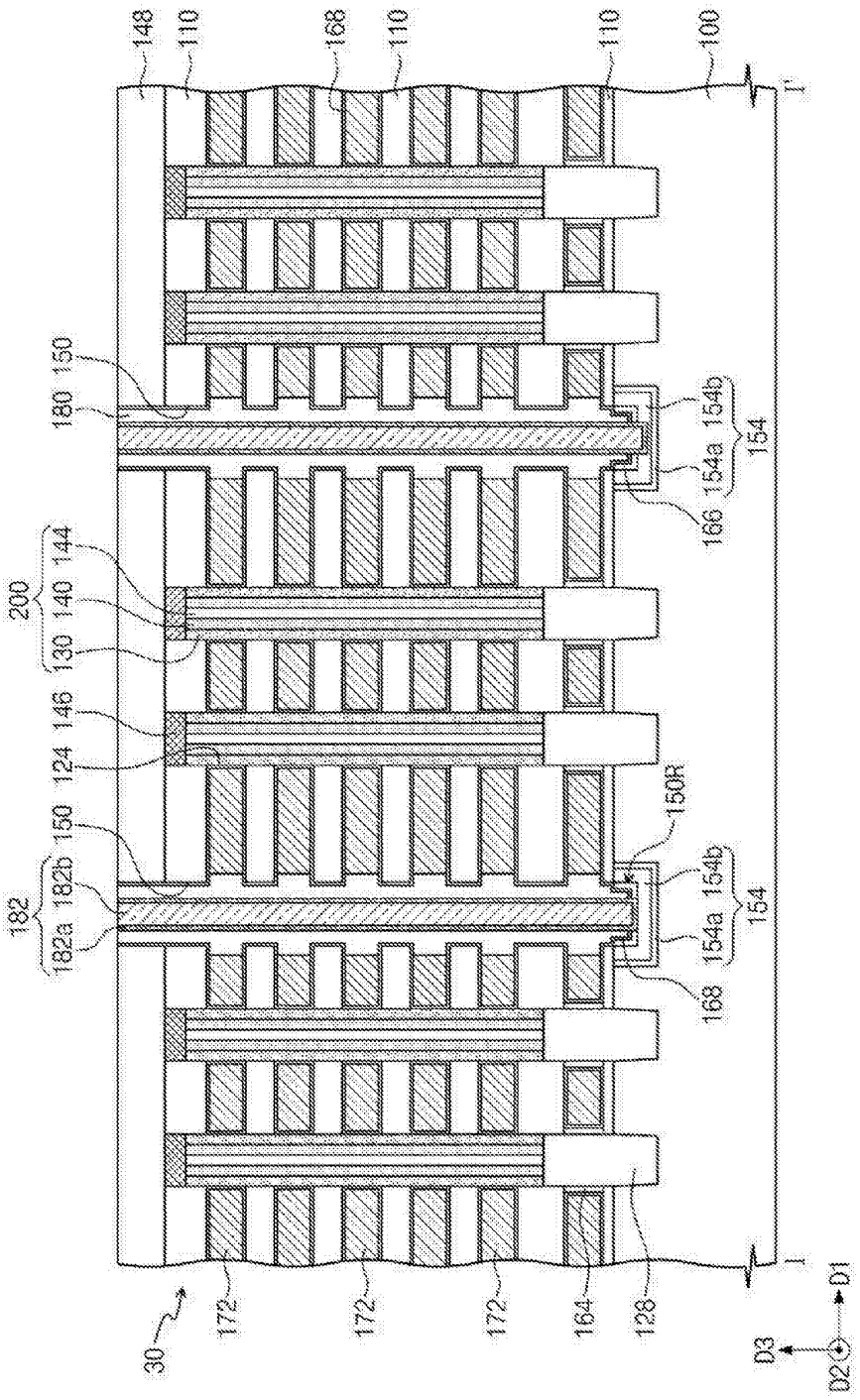

图 25A

Micron Ex. 1002, p. 353
Micron v. YMTC
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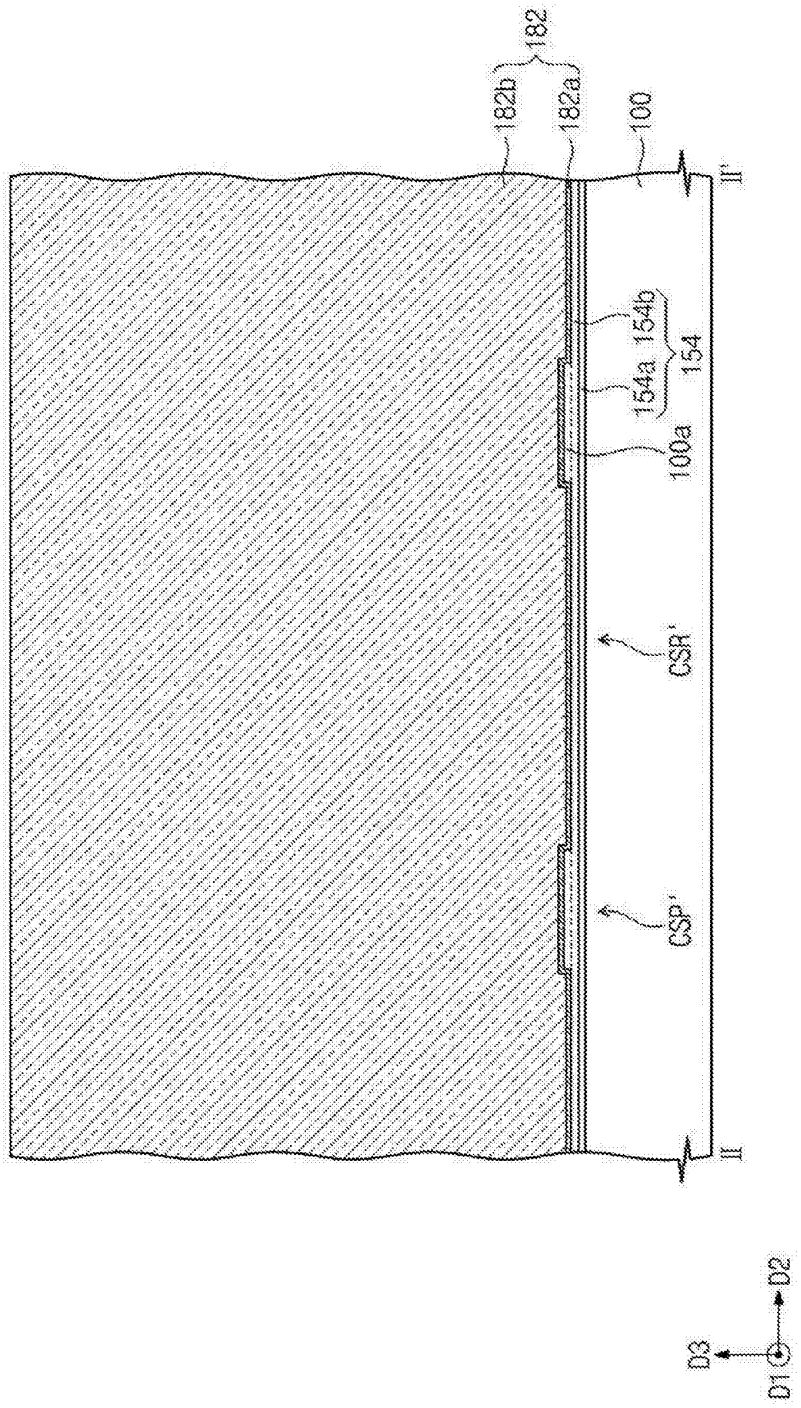

图 25B

Micron Ex. 1002, p. 354
Micron v. YMTC
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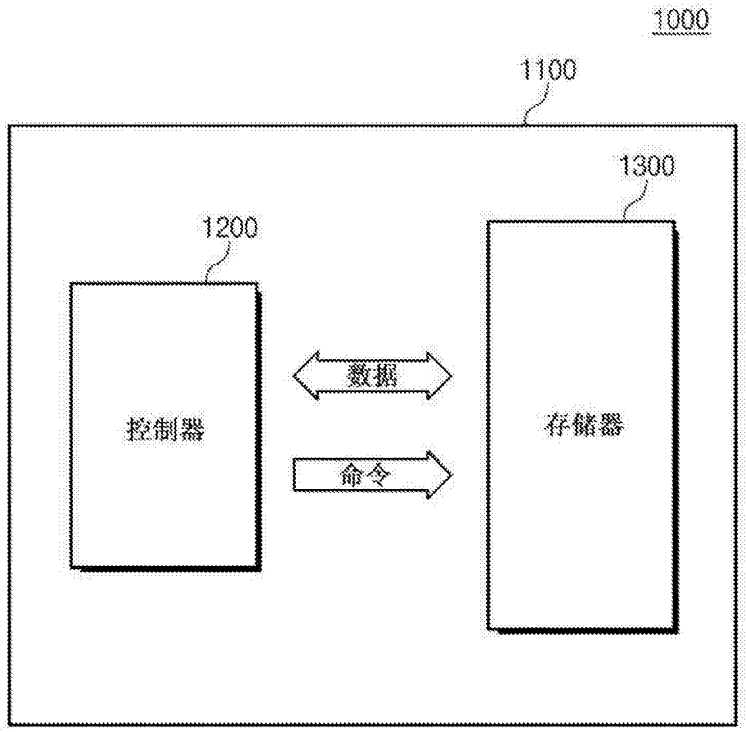

图 26

Micron Ex. 1002, p. 355
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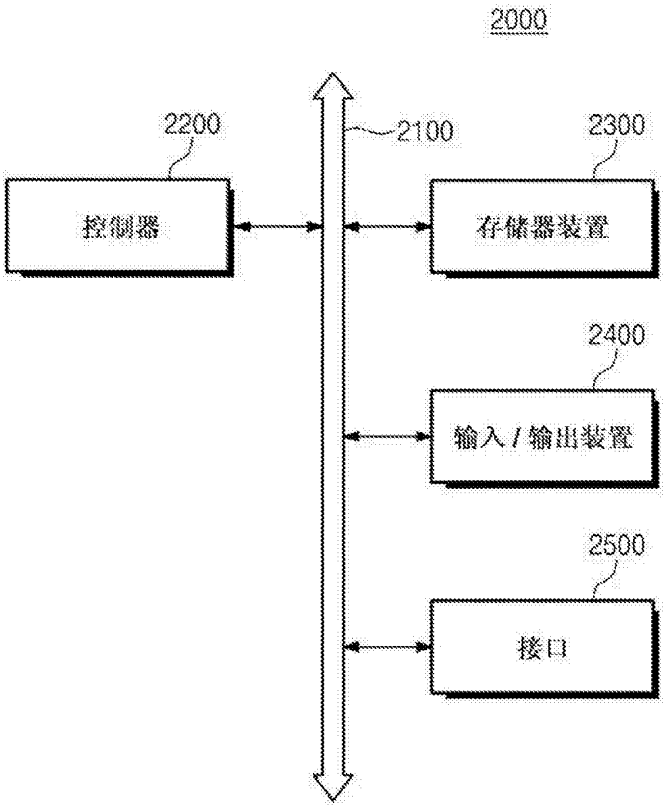

图 27

Micron Ex. 1002, p. 356
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