

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner
v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner

Case No.: IPR2024-00909
U.S. Patent No. 10,658,378
Issue Date: May 19, 2020

Title: THROUGH ARRAY CONTACT (TAC) FOR
THREE-DIMENSIONAL MEMORY DEVICES

DECLARATION OF DR. JACK C. LEE

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I, Dr. Jack C. Lee, declare as follows:

I. INTRODUCTION

1. I have been retained by Micron Technology, Inc. (“Micron”) as an independent expert consultant in this proceeding before the United States Patent and Trademark Office (“PTO”). I am not an employee of Micron or any affiliate or subsidiary of Micron.

2. I have been asked to consider whether certain references disclose or teach the features recited in claims 1-7 and 18 of U.S. Patent No. 10,658,378, which I refer to herein as the ’378 patent.

3. My opinions and the bases for my opinions are set forth below.

4. On April 30, 2024, I signed a declaration relating to the ’378 patent in connection with IPR2024-00788. That declaration addressed claims 15-17 and 19-20, while this declaration addresses claims 1-7 and 18. Claim 18 depends from claim 15, so my discussion of claim 15 here parallels my discussion of claim 15 in my April 30 declaration.

5. I am being compensated at my standard consulting rate of \$680 per hour for my time. My compensation is based solely on the amount of time that I devote to activity related to this case and is in no way contingent on the nature of my findings, the presentation of my findings in testimony, or the outcome of this or any other proceeding. I have no other financial interest in this proceeding.

II. BACKGROUND AND EXPERT QUALIFICATIONS

6. My curriculum vitae (“CV”) is attached hereto as Ex. 1004 and provides an accurate identification of my background, experience, and qualifications as an expert in electronics and NAND memory technology.

7. I received a B.S. degree in Electrical Engineering, with highest honors, in 1980, and an M.S. degree in Electrical Engineering in 1981, both from University of California, Los Angeles. I received a Ph.D. degree in Electrical Engineering in 1988 from University of California, Berkeley (“UC Berkeley”).

8. From 1979 to 1984, I was a Member of Technical Staff at the TRW Microelectronics Center, in the High-Speed Bipolar Device Program. I worked on bipolar device/circuit design, fabrication, and testing. I was promoted to Engineering Group Leader level in 1983.

9. I received several academic honors while at UC Berkeley. For example, I won the Best Paper Award from the Institute of Electrical and Electronics Engineers (“IEEE”) International Reliability Physics Symposium in 1988. I was also awarded a Lectureship with my own teaching assistant from UC Berkeley.

10. After receiving my Ph.D. in August 1988, I joined the faculty at The University of Texas at Austin (“UT Austin”). As a faculty member, I have taught numerous courses in semiconductor device fabrication and design, at both the undergraduate and graduate levels. This includes classes relating to, among other

things, 3D NAND technology. I have supervised over 40 students who received their doctoral degrees under my guidance. Since September 2000, I have held the Cullen Trust for Higher Education Endowed Professorship in Engineering in the Department of Electrical and Computer Engineering at UT Austin. In September 2023, I was promoted to the Professor Emeritus level.

11. My current research and teaching interests include semiconductor devices, semiconductor memory applications (including non-volatile memory), fabrication processes, silicon-on-insulator technologies, electrical and material characterization, reliability and modeling, packaging technologies, dielectric and passivation processes, display technologies, photovoltaic and solar cell technologies, high-K gate dielectrics and electrode, and alternative channel materials. I routinely encounter and address topics relating to NAND flash memory, and more specifically 3D NAND flash memory, in my research. My research has been partially supported by grants from the National Science Foundation, the Texas Advanced Research Program, the Semiconductor Research Corporation (SRC), SEMATECH, Texas Emerging Technology Funds, and others.

12. I have authored over 600 journal publications and conference proceeding papers and have coauthored 8 books and book chapters on semiconductor technologies. Many of these relate to the structure and operation of memory devices, including non-volatile memory such as NAND flash memory and

3D NAND flash memory. I am a named inventor of 9 U.S. patents. I have also received numerous teaching and research awards, e.g., inventor recognition and best paper awards.

13. In 2002, I became an IEEE fellow for my “contributions to the understanding and development of ultra-thin dielectrics and their application to silicon devices.” I was also an IEEE Electron Devices Society Distinguished Lecturer from 2004 to 2016.

14. I have served in various technology consulting and business advisor roles. For example, I have taught short courses on semiconductor device physics and technologies at various semiconductor companies and consortiums (e.g., SEMATECH). I have also organized several international conferences and have given lectures at numerous conferences and symposia, including the International Symposium on VLSI Technologies, the IEEE Symposia on VLSI Technology, and the IEEE International Electron Devices Meeting. These conferences are some of the most prestigious in the field.

III. ASSIGNMENT AND MATERIALS CONSIDERED

15. I have been asked to provide analysis and explain the subject matter of the '378 patent, including the state of the art when the application underlying the '378 patent was filed. I have also been asked to consider, analyze, and explain certain prior art to the '378 patent including how that art relates to claims 1-7 and 18

(which I refer to as the “challenged claims”) of the ’378 patent and to provide my opinions regarding whether that art invalidates the challenged claims.

16. The opinions expressed in this declaration are not exhaustive of opinions I may offer in the future regarding the unpatentability of the challenged claims of the ’378 patent. Therefore, the fact that I do not address a particular point should not be understood to indicate an agreement on my part that any claim complies with the requirements of any other applicable rule.

17. I reserve the right to amend and supplement this declaration in light of additional evidence, arguments, or testimony presented during this IPR or related proceedings on the ’378 patent.

18. In forming the opinions set forth in this declaration, I have considered and relied upon my education, knowledge of the relevant field, knowledge of scientific and engineering principles, and my experience. I have also reviewed and considered the ’378 patent (Ex. 1001), its prosecution history (Ex. 1002), and the following additional materials:

Exhibit	Description
1005	U.S. Patent Publ. No. 2017/0179026 A1 (“Toyama”)
1011	CN109075169A Office Action, dated November 14, 2019
1012	Certified Translation of CN109075169A Office Action, dated November 14, 2019

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Exhibit	Description
1013	CN109075169A Reexamination Decision, dated November 25, 2021
1014	Certified Translation of CN109075169A Reexamination Decision, dated November 25, 2021
1015	Micheloni, “3D Flash Memories” (2016)
1016	Aritome, “NAND Flash Memory Technologies” (2016)
1017	U.S. Patent No. 9,620,512 to Nishikawa et al.
1018	U.S. Patent Publ. No. 2016/0056188 A1 to Lee et al.
1019	U.S. Patent No. 9,293,348 to Lai et al.
1020	U.S. Patent No. 10,169,169 to Ge et al.
1021	U.S. Patent No. 8,697,519 to Jee et al.
1022	Excerpts from “Merriam-Webster’s Collegiate Dictionary,” Eleventh Edition (2014)
1023	Chang, “ULSI Technology” (1996)
1024	Chen, “CMS Devices & Technology for VLSI” (1988)
1025	Jaeger, “Volume V: Introduction to Microelectronic Fabrication” (1988)
1026	Wagner, “The Use of HBr in Polysilicon Etching,” Gases & Instrumentation International, Vol. 7, Issue 4, July/August (2013) printed from https://www.pall.com/content/dam/pall/microelectronics/literature-library/non-gated/HBr_Polysilicon.pdf
1027	Baker, “CMOS Circuit Design, Layout, and Simulation,” Third Ed. (2010)
1028	U.S. Patent No. 5,776,808 to Muller et al.

Exhibit	Description
1029	U.S. Patent No. 9,236,393 to Cernea
1030	Excerpt from YMTC’s Exemplary Infringement Claim Chart for U.S. Patent No. 10,658,378 – 128L (Ex D-1 to YMTC’s Disclosure of Asserted Claims and Infringement Contentions), dated May 6, 2024 [PROTECTIVE ORDER MATERIAL – FILED UNDER SEAL]
1031	Kim et al., “Three-Dimensional NAND Flash Architecture Design Based on Single-Crystalline Stacked Array,” IEEE Transactions on Electron Devices, Vol. 59, No. 1, Jan. 2012, pp. 35-45
1032	Capogreco et al., “Integration and electrical evaluation of epitaxially grown Si and SiGe channels for vertical NAND Memory applications,” 2015 IEEE International Memory Workshop, 2015

IV. UNDERSTANDING OF THE LAW

19. I am not an attorney, but have been instructed in and applied the law as described in this section.

20. I understand that the first step in comparing a challenged claim to the prior art is for the claim to be properly construed. I address how a person of ordinary skill in the art (POSITA) would have understood the challenged claims of the alleged invention in Section VIII below.

21. I have been further instructed and understand that a patent claim is unpatentable and invalid as obvious if the subject matter of the claim as a whole would have been obvious to a POSITA of the claimed subject matter as of the time

of the invention at issue. I understand that when assessing the obviousness of claimed subject matter, the following factors are evaluated: (1) the scope and content of the prior art; (2) the difference or differences between each claim of the patent and the prior art; and (3) the level of ordinary skill in the art at the time the patent was filed.

22. I understand that claimed subject matter may be obvious in view of more than one item of prior art. I understand, however, that it is not enough to show simply that all the limitations of the claimed subject matter are spread throughout the prior art. Instead, for claimed subject matter to be obvious over multiple references, there must be some reason or motivation for a POSITA to combine the prior art references to arrive at the claimed subject matter.

23. I have been informed that, in seeking to determine whether an invention that is a combination of known elements would have been obvious to a POSITA at the time of the invention, one must consider the references in their entirety to ascertain whether the disclosures in those references render the combination obvious to such a person.

24. I have been informed and understand that, while not required, the prior art references themselves may provide a teaching, suggestion, motivation, or reason to combine. The motivation linking two or more prior art references can also come

from other sources, including, for instance, economic or market demand or the common sense of a POSITA at the time of the invention.

25. I understand that a particular combination may be proven obvious by showing that it was obvious to try the combination. I have been informed that, if a technique has been used to improve one device, and a POSITA would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.

26. I further understand that an obviousness analysis recognizes that market demand, rather than scientific literature, often drives innovation, and that a motivation to combine references also may be supplied by the direction of the marketplace. For example, when there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a POSITA has good reason to pursue the known options within his or her technical grasp because the result is likely the product not of innovation but of ordinary skill and common sense.

27. I have been informed that the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. Thus, where all the elements of a claim are used in substantially the same manner, in devices in the same field of endeavor, the claim is likely obvious.

28. Additionally, I understand that a patent is likely to be invalid for obviousness if a POSITA can implement a predictable variation or if there existed at the time of the invention a known problem for which there was an obvious solution encompassed by the patent's claims. Therefore, when a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one.

29. I further understand that combining embodiments related to each other in a single prior art reference would not ordinarily require a leap of inventiveness.

30. I also understand that a POSITA must have had a reasonable expectation of success when combining references for claimed subject matter to be obvious.

31. I have been informed and I understand that factors referred to as "objective indicia of non-obviousness" or "secondary considerations" are also to be considered when assessing obviousness when such evidence is available. I understand that these factors can include: (1) commercial success; (2) long-felt but unresolved needs; (3) copying of the invention by others in the field; (4) initial expressions of disbelief by experts in the field; (5) failure of others to solve the problem the claimed subject matter solved; and (6) unexpected results.

32. I also understand that evidence of objective indicia of non-obviousness must be commensurate in scope with the claimed subject matter. I further

understand that there must be a relationship, sometimes referred to as a “nexus,” between any such secondary indicia and the claimed invention.

33. Finally, I have been informed that one cannot use hindsight to determine that an invention was obvious.

34. I provide my opinions in this declaration based on the guidelines set forth above.

V. LEVEL OF SKILL IN THE ART

35. I have been informed and understand that the level of ordinary skill in the relevant art at the time of the invention is relevant to inquiries such as the meaning of claim terms, the meaning of disclosures found in the prior art, and the reasons a POSITA may have for combining references.

36. I have been informed and understand that factors that may be considered in determining the level of ordinary skill include: (1) the education of the inventor; (2) the type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology; and (6) education level of active workers in the relevant field. I have been further informed and understand that a person of ordinary skill in the art (POSITA) is also a person of ordinary creativity.

37. In my opinion, a POSITA in the field of the '378 patent would have had a bachelor of science degree in electrical engineering or a similar discipline, along

with 2-3 years of professional experience working with (e.g., researching, designing, or teaching) NAND flash memory devices, or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may replace some of the professional experience).

38. In my opinion, this POSITA would also have been aware of and generally knowledgeable about semiconductor manufacturing and 3D NAND's structure, its component parts, how it operates, and how it is controlled.

39. In view of my educational background and decades of experience working with semiconductor memory—including non-volatile 3D NAND flash memory—I was a person of more than the ordinary level of skill in the art as of May 2018. In forming my opinion, I have drawn on my academic background and professional experiences. My opinions herein, however, were formed taking into account the perspective of an ordinarily skilled artisan.

VI. TECHNOLOGY BACKGROUND AND STATE OF THE ART

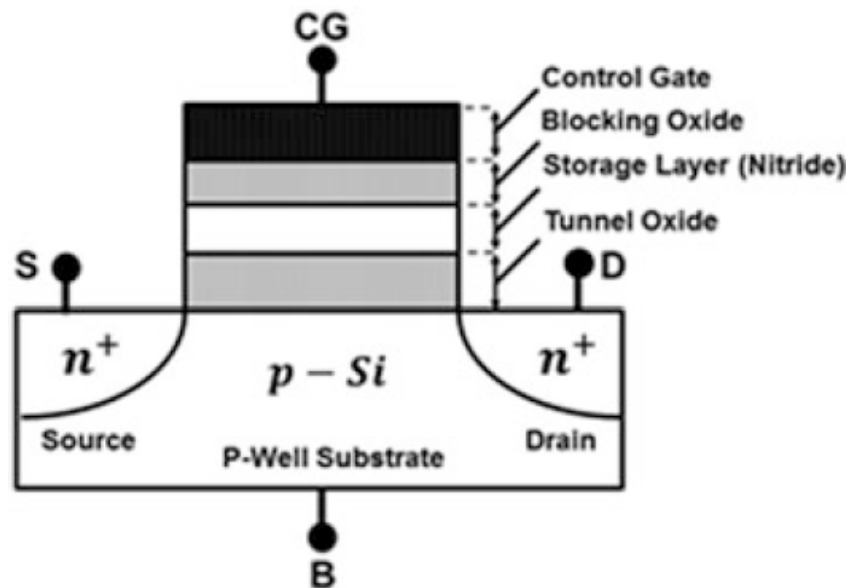
A. 3D NAND Flash Memories

40. I have been asked to provide a brief overview of the technology relevant to the '378 patent and the state of the art when the '378 priority application was filed.

41. The '378 patent (and the prior art I discuss herein) relate to three-dimensional (3D) NAND flash memory. "Flash memory" has been known for many

decades and is a type of memory that stores information even when power is removed (*viz.*, when the device is turned off).

42. At the heart of flash memory is the “memory cell,” which stores information as electrical charge. An example memory cell is below:



Ex. 1015, 41. In a memory cell, current flows from the “drain” of the device to the “source” of the device, which is typically connected to a low voltage, such as ground. *Id.*, 150 (“[T]he Source Line ... plays the role of the ‘local ground’ for each memory cell.”).

43. The acronym “NAND” refers to a “not-AND” logic gate, and NAND flash memory is a particular type of flash memory where the memory cells form a structure similar to that of a NAND gate. Ex. 1015, at 14. The other most common

type of flash memory is NOR flash, but NAND offers a higher integration density and occupies a larger market than NOR flash.

44. A NAND flash memory device, like most flash memory devices, has an associated memory controller that controls the read, write, and erase operations on a memory cell by applying a voltage to that cell's "control gate," labeled as "CG" in the above figures. Ex. 1015, 41.

45. For many years, a NAND flash memory was "planar," that is, two-dimensional (2D). In 2D NAND flash memory, all memory cells lie on a 2D plane (*i.e.*, the x-y plane) on the surface of a memory chip as shown below:

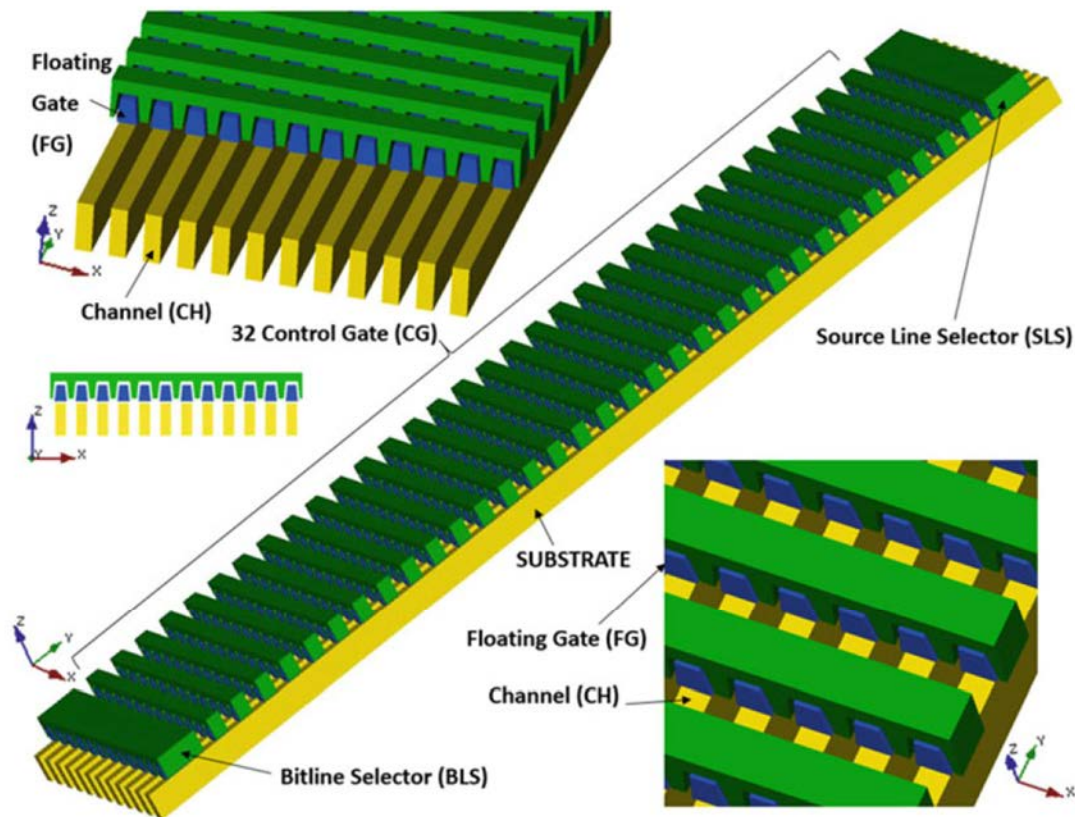


Fig. 3.9 Bird's-eye view of a planar NAND string

Ex. 1015, at 86.

46. To boost data storage densities and reduce cost per gigabit, the art developed so-called “three-dimensional (3D) NAND flash cells” starting in about 2006. Ex. 1016, 292. Unlike planar 2D NAND flash memory, in 3D NAND flash memory the memory cells are arranged in vertical, cylindrical NAND flash columns, often referred to as “memory strings.” Conceptually, a modern 3D NAND structure could be conceived by starting from the 2D NAND string building block and turning

the 2D NAND string on its side, resulting in a 3D structure with a vertical channel.

The following image provides an example:

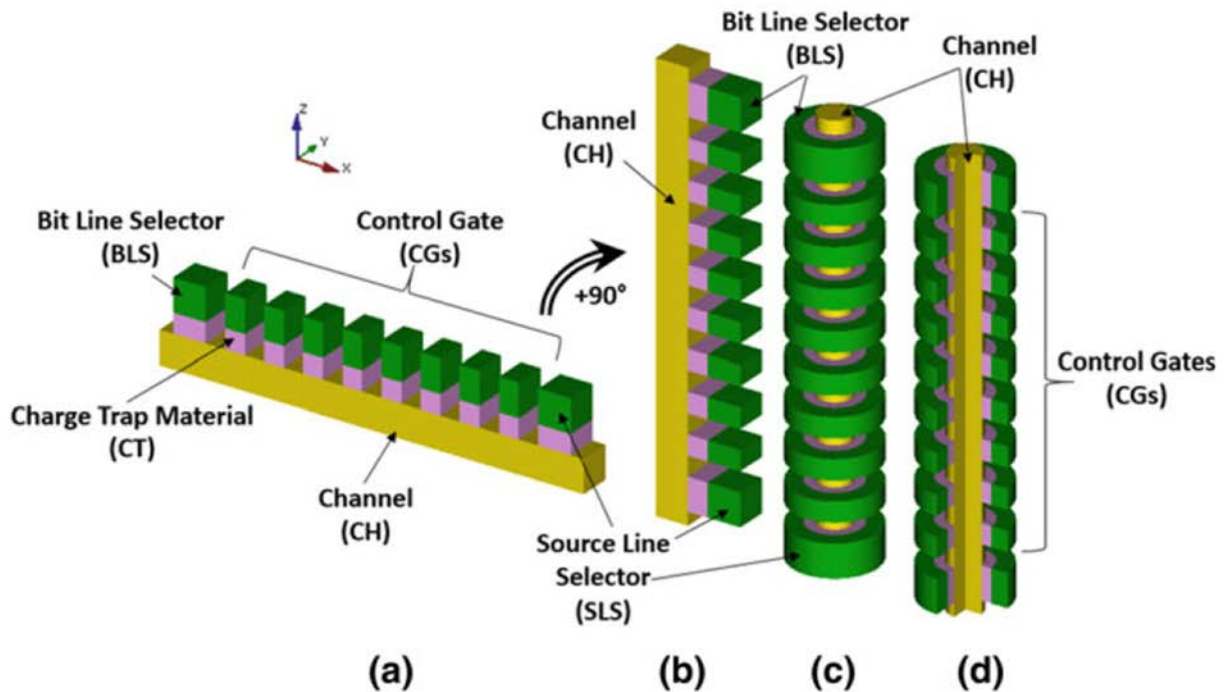


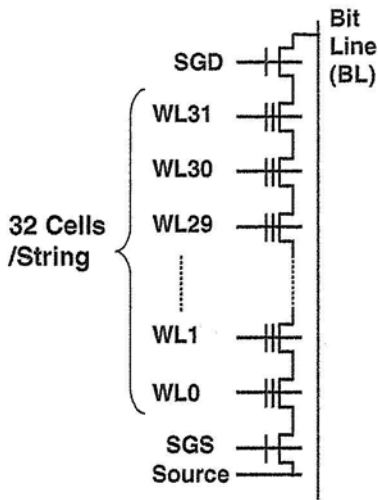
Fig. 4.1 NAND Flash string with horizontal gate and vertical channel: **a** planar, **b** planar rotated by 90°, **c** vertical channel with cylindrical shape and **d** its cross section

Ex. 1015, 102. As labeled in Figure 4.1, above, each NAND string includes a “cylindrical channel.” *Id.*, 58. The concept of a “channel” was well-known in semiconductor devices and refers to a thin and layer of charge that is formed between the source and drain of a transistor when a voltage is applied to the gate. The “channel” is highly conductive and allows current to easily flow between the source and drain. The “cylindrical channel” in 3D NAND devices also provides the means for current to flow in a memory string.

47. Multiple of such vertical channels are then repeated in a three-dimensional array. Ex. 1016, 296.

48. As can be seen above, the NAND flash memory “strings” each contain multiple cells “connected in series.” Ex. 1016, 38. The source of one cell is connected to the drain of the next one. Depending on the technology, typically a string consists of 32 to 128 NAND cells.

49. Each end of a string is terminated with a “select transistor.” One is often called the “SGD” (drain-end select gate transistor) and the other one is often called “SGS” (source-end select gate transistor). The “SGD connects” at the string’s drain side “to isolate it from the bit line (BL).” Ex. 1016, 38. Hence, the SGD is also known as the “bit line select transistor” or the “upper select gate.” The SGS connects at the string’s source side “to isolate it from a source line (SL).” *Id.* Since the source line is commonly connected to the ground terminal, SGS is also known as the “ground select transistor” or the “lower select gate.” Word lines are connected to each memory cell control gate. *Id.*, 38-39. A schematic representation of a memory string is shown below:



Id., 39.

50. Various architectures for constructing 3D NAND flash memory were known in the art. One such example is the well-known BiCS (Bit Cost Scalable) architecture, where various “contacts” (electrical connections) are formed on top of the memory array. Below are two illustrations of the BiCS architecture show top and bottom perspective views.

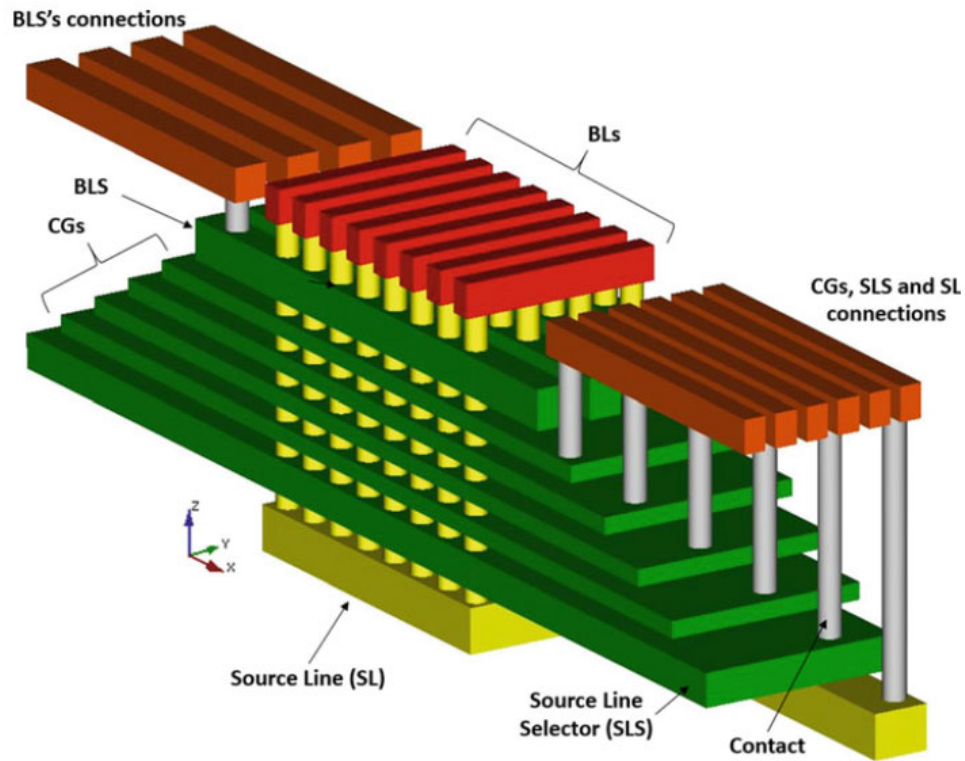


Fig. 4.13 Top bird's eye view of BiCS with gate connections

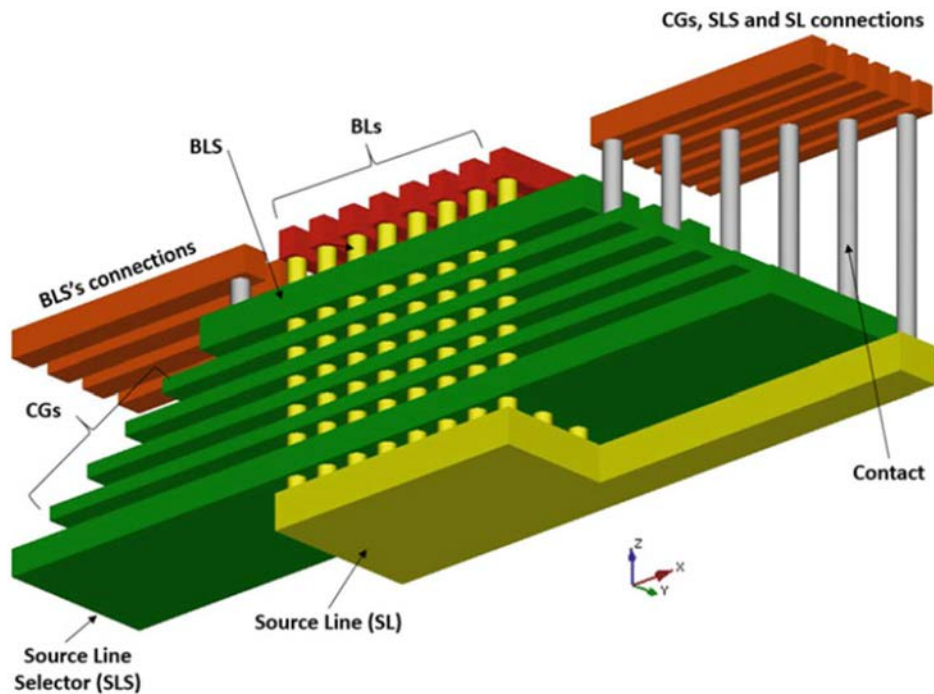


Fig. 4.14 Bottom bird's-eye view of BiCS with gate connections

Ex. 1015, 109-110. As is traditional in MOSFET transistors, the “source” terminal connects to a low voltage, such as ground. The same holds true in 3D NAND design, and the BiCS architecture includes source line contacts for providing a low voltage (*e.g.*, ground) connection to the memory strings. This is shown in yellow in the figures above.

51. The individual memory cells in a memory string are accessed by word lines that typically extend horizontally and connect to a control gate for a given cell on each memory string. On the periphery of the 3D NAND device, the word lines form a staircase structure, where each subsequent word line protrudes a short distance beyond the word line above it, like a staircase, as shown below in green.

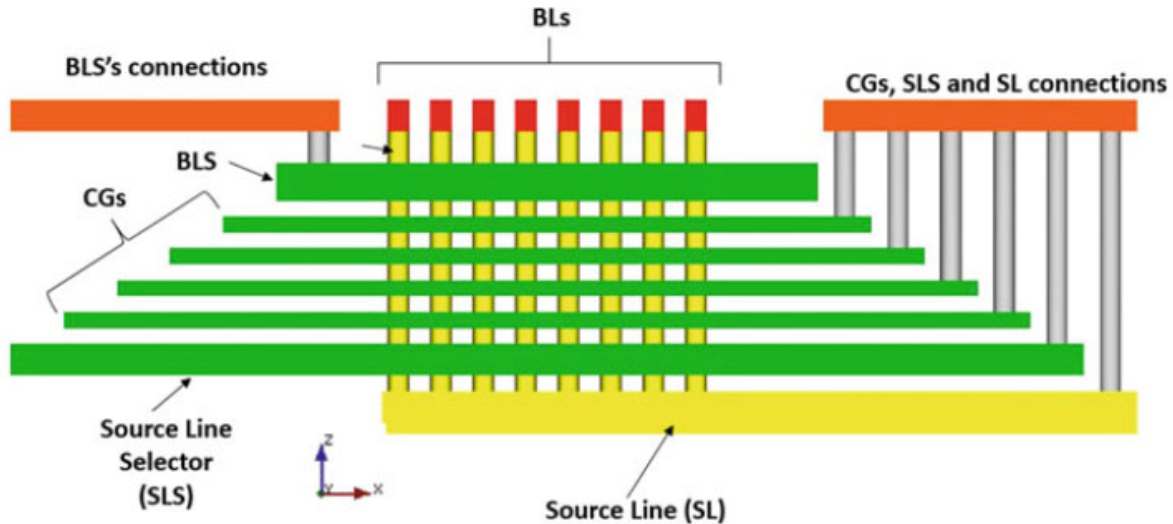


Fig. 4.12 Vertical cross section of BiCS with gate connections

Ex. 1015, 109 (green control gates forming a staircase). As noted, each word line delivers a control signal to a number of memory cells at the same horizontal level in the 3D NAND memory device.

52. The collection of memory cells controlled by a common signal together constitute a “word,” and the control gate is a “word line.” Ex. 1015, 109; Ex. 1016, 41. The grey columns in the figure above, often referred to as “local contacts,” show how the word lines can be controlled by signals on the top surface of the 3D NAND device. In the context of 3D NAND chips, “local contacts” refer to the electrical connections made within the memory device to link various components such as the word lines and source lines. In facts, local contacts are also often referred to as “vias,” which have been widely known and used in all sorts of semiconductor devices for many decades. These vias create vertical electrical connections between

the different layers within the 3D NAND stack. They are integral to the architecture of semiconductor devices generally, including 3D NAND technology where they enable the functional linkage of stacked memory cells across multiple layers. Note that these local contacts can be of various lengths – some long and some very short. For example, the local contacts (the grey columns in the figure above) that connect to the word lines located near the top of the memory stack are very short while the grey column that connect to the source line is much longer. Where local contacts are connecting an existing vertical structure, such as a memory string or slit, the local contacts tend to be relative short. I note in this regard that the '378 patent gives examples of long local contacts (*e.g.*, an entire TAC) and short local contacts (*e.g.*, atop channel structures and slits). See Ex. 1001, 11:16-30.

53. A variety of modifications to the BiCS architecture were known, including the use of slit structures to serve as source line contacts for the NAND strings. Exemplary slit structures are shown in purple below. These particular slit structures function as contacts for connecting to the source (which may be shared by some, or all, memory strings) located on the bottom of the 3D NAND device.

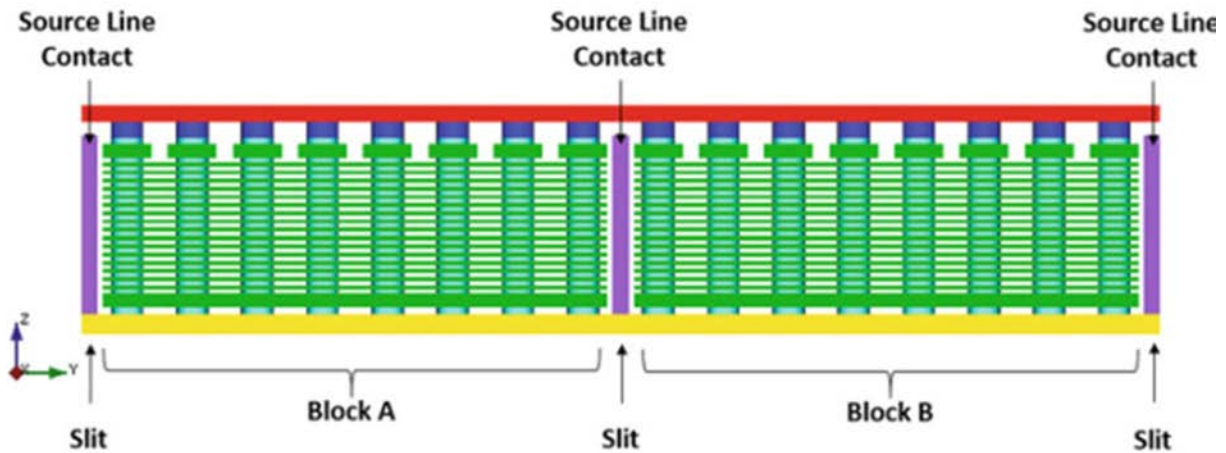


Fig. 6.8 Side view of Fig. 6.7

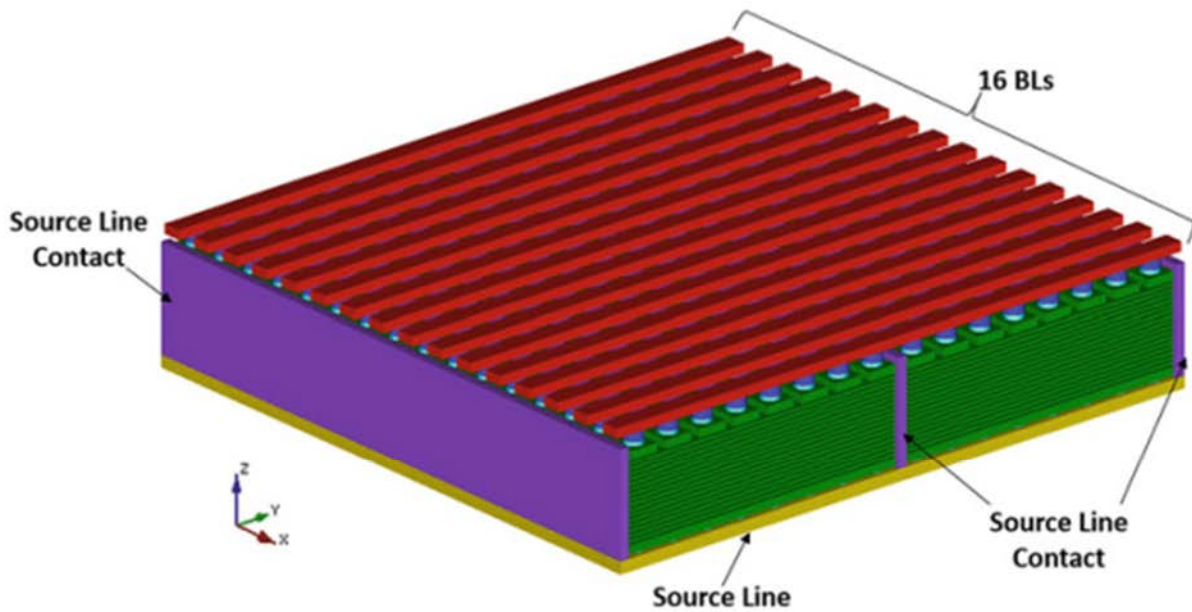


Fig. 6.7 Array slits

Ex. 1015, 185.

54. In both figures above, gaps are shown between the various structures. In actual 3D NAND memory devices, these “gaps” are not empty space; rather, they are filled with insulating material (known as “dielectric” material). Among other

things, dielectrics serve to isolate electrical signals and prevent one conductive structure from interfering with another other. Another function performed by the dielectric is mechanical support to prevent the other structures from collapsing.

55. Well before the effective filing date of the '378 patent, companies (including Micron) had developed various techniques for manufacturing 3D NAND flash memory, many of which leveraged fabrication principles and materials that had been in use generally in the semiconductor manufacturing industry for decades.

56. Stacking multiple chips, also known as 3D integration, was just one of many advancements in semiconductor technology that have happened over the years. The concept of 3D integration should not be confused with 3D NAND. Although 3D integration has application to 3D NAND chips, the concept of vertically stacking multiple dies/chips predates 3D NAND by many years and has been used extensively in a variety of chip technologies. This method significantly enhances device performance and functionality while conserving space, addressing the limitations faced by traditional planar scaling methods. Naturally, when stacking multiple dies on top of one another, via structures (also called through-silicon vias (TSVs) or through-array contacts (TACs)) were implemented to provide connections between different chips in the stack. The concept of TACs predates 2018 and was developed to meet the growing demands for increased functionality and higher performance without expanding the chip's footprint. These vertical connections are

essential for shortening the path electrical signals must travel compared to traditional methods like wire bonding or flip-chip techniques. By reducing the length of interconnects, TACs enhance signal speed and reduce power consumption. Before 2018, the semiconductor industry recognized the potential of through-array contacts to mitigate the slowing pace of enhancements afforded by Moore's Law due to physical and economic limits.

57. In summary, techniques for manufacturing 3D NAND memory devices were well-known in the art before the '378 patent's effective filing date.

B. Epitaxy

58. As of 2018, a POSITA would have well understood the semiconductor manufacturing process called "epitaxy."

59. Epitaxial growth in semiconductor manufacturing processes involves depositing a crystalline layer of material onto a crystalline substrate in a way that the crystallographic orientation of the deposited material matches that of the substrate. Ex. 1023 (Chang, ULSI Technology), 132 (in epitaxy, material is "grown" on a substrate). Using an epitaxial process results in high-quality deposited layer, which can be useful for advanced integrated circuits including 3D NAND memory devices.

60. Well before 2018, use of the epitaxial growth process in 3D NAND structures was well known. For example, an epitaxial layer had been disposed

between the substrate and the first channel structures primarily for enhancing the device's performance and reliability, as illustrated in the below figure:

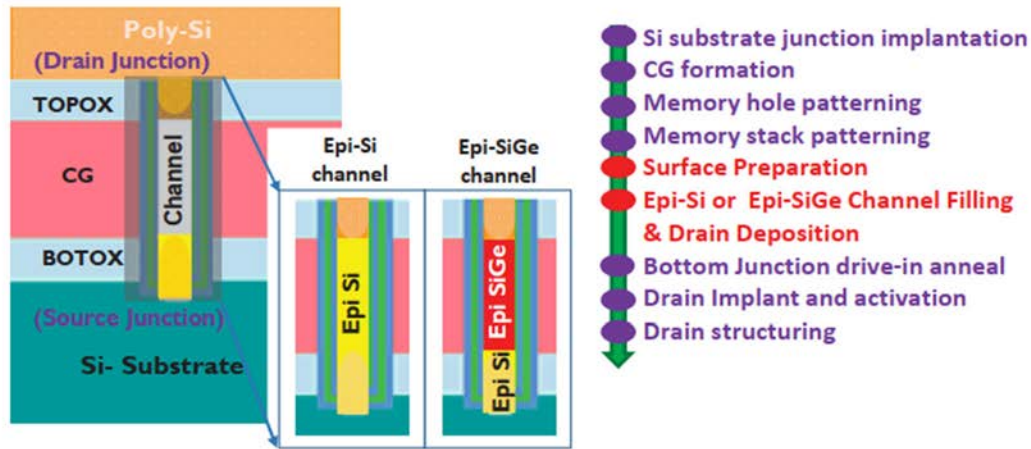


Fig. 1: Schematic view of our vertical NAND single test vehicle. Added/modified steps w.r.t. poly-Si-based process flow are highlighted in red.

Ex. 1032 (Capogreco, Integration and Electrical Evaluation), at 1.

61. This epitaxial layer serves several functions. It provides a high-quality interface between the channel structures and the underlying substrate, which can reduce device degradation over time. It also serves as a barrier, preventing impurities from the substrate from contaminating the channel materials, thus ensuring consistent device behavior and longevity. The epitaxial process provides a stable crystalline template that matches the crystal structure of the underlying substrate. This alignment helps minimize defects that could propagate through the subsequent layers. These defects can potentially degrade the electrical performance

and reliability of the 3D NAND device. The epitaxial layer also provides consistent and uniform electrical properties. The uniformity can help minimize variability of charge mobility and carrier lifetimes. See, e.g., Ex. 1031 (Kim, 3-Dimensional NAND Flash), at 2 (“Flash memory having the single-crystalline channel is expected to have the better performance such as a uniform threshold voltage distribution and stable bit-line (BL) current.”); Ex. 1032 (Capogreco, Integration and electrical evaluation), at 4 (epitaxially-grown silicon has superior conductivity).

62. “The success of an epitaxial growth relies heavily on the chemistry used in the process,” which may include “hydrogen and chlorosilanes, such as silicon tetrachloride (SiCl_4), trichlorosilane (SiHCl_3), and dichlorosilane (SiH_2Cl_2). In addition, silane (SiH_4) has also been used when a lower growth temperature is desired. The choice of each source gas is based on the growth conditions and layer requirements.” Ex. 1023 (Chang), 143.

C. Etching

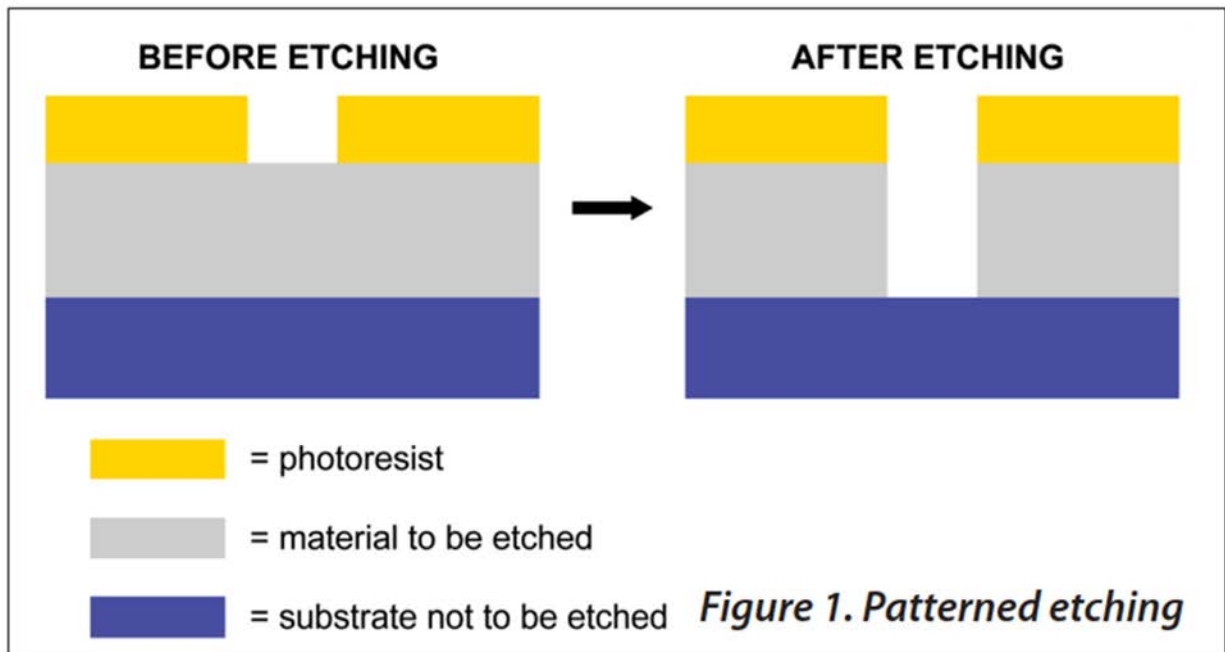
63. The fabrication of 3D NAND memory chips involves etching techniques to construct vertical, high-density storage architectures. These etching processes, fundamental to semiconductor manufacturing, have been well established prior to 2018 but have been adapted for 3D NAND. Here are just a few examples of etching processes used for 3D NAND. Channel hole etching which typically makes use of a dry etching process, e.g., deep reactive ion etching (DRIE) to create

vertical channels through the NAND stack. DRIE was developed in the mid-1990s, allows for etching with high aspect ratios, essential for the vertical structures in 3D NAND. Staircase etching involves sequential etching steps to create a staircase-like structure for accessing word lines across each memory layer. This process leverages standard lithographic and etching techniques known long before 2018, adapted to create the precise, repetitive structures needed for multi-layer access. Hard-mask etching process, well-known long before 2018, involves depositing a durable material like nitrides which is then patterned using photolithography to serve as a mask. The hard mask protects underlying layers during subsequent etching.

64. A POSITA would have well understood techniques for “etching,” a well-known semiconductor manufacturing technique used to remove material. Ex. 1023 (Chang, ULSI Technology), 356-57; Ex. 1025 (Jaeger, Introduction to Microelectronic Fabrication), 35-36. A chemical that is used to etch material is known as an “etchant.” Well before 2018, a POSITA would have known of etchants that are “selective.” A selective etchant is one that reacts to (and thus removes) some materials preferentially to others. Ex. 1025 (Jaeger, Introduction to Microelectronic Fabrication), 35. For example, it has long been known that carbon tetrafluoride (CF₄), when paired with a concentration of hydrogen (H₂) greater than 40%, can selectively etch silicon dioxide over silicon, by forming volatile compounds that can

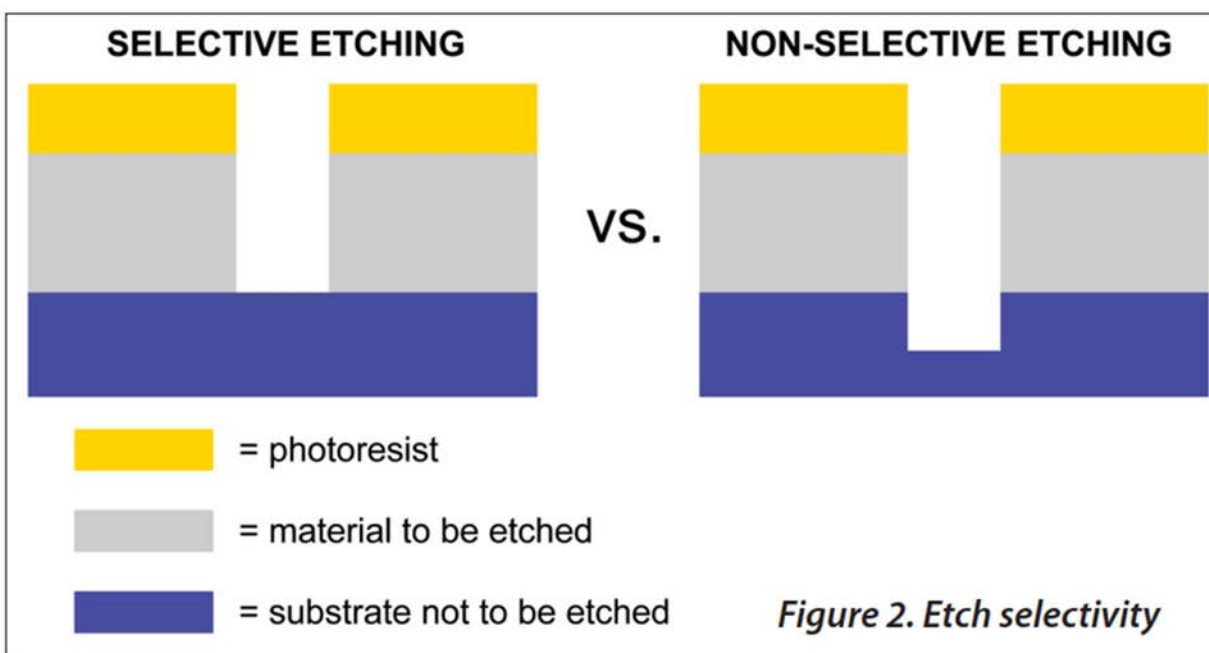
be easily removed, leaving the silicon substrate largely unaffected. Ex. 1023 (Chang, ULSI Technology), 363-64.

65. The etching process is illustrated in the following figure:



Ex. 1026 (HBr), at 1. As Figure 1, above, shows, “patterned etching” involves placing a photoresist (a material resistant to etching that is typically formed using photolithography) to shield certain material from the etching process. Then, an etchant is applied to the exposed surface. As a result, the material to be etched is removed but the material covered by the photoresist remains intact.

66. Figure 2, below, shows the difference between a selective etch and a non-selective etch:



Ex. 1026 (HBr), at 2. As Figure 2 shows, a non-selective etch may result in material being removed not only from the material to be etched but also from the substrate.

67. Selective etching, which is used to remove specific materials without damaging others by using different chemistries to target certain layers of materials, again was well-known long before 2018. Spacer etching involves depositing and then partially removing the material developed to define narrow, uniform spacers (gaps) for cell isolation. Spacer etching processes were developed for lightly-doped drain (LDD) MOSFETs back in the 1980's and adapted for 3D NAND manufacturing process. Each of these processes originates from fundamental techniques known in semiconductor manufacturing well before 2018, adapted for the advanced architecture of 3D NAND.

68. Prior to 2018, the application of selective etching in 3D NAND fabrication was already well known. This process enabled manufacturers to develop multi-layered NAND structures, significantly increasing storage capacity and efficiency. By precisely removing specific materials without damaging others, this technique allowed for the construction of vertical channels and intricate interconnects between the stacked arrays of memory cells. For example, selective etching enables the creation of very fine structures, such as the staircases for wordline connections. A POSITA would have known that any deviation in etching could lead to defects that impair the functionality of the memory chip and reduce its data retention capabilities. Thus, the accuracy of selective etching governed the uniformity and performance of the final product, directly impacting yield rates and reliability.

69. A POSITA would have known of the common use of a material to which an etchant is **not** selective as an “etch stop,” that is, to prevent the etch from removing material not intended to be removed. Ex. 1027 (Baker, CMOS Circuit Design), 48 (an “etchant stop layer is used”). For example, a POSITA would have known of the use of polysilicon to stop an etch through silicon oxide. Ex. 1028 (U.S.

Pat. No. 5,776,808), 4:25-35 (polysilicon used as “etch stop layer”);¹ Ex. 1029 (U.S. Pat. No. 9,236,393), 17:20-24 (“[t]he isotropic etch creates a trench ... that stops at the doped polysilicon layer”).

VII. THE ’378 PATENT

A. Effective Filing Date

70. I understand that the application leading to the ’378 patent was filed on July 27, 2018.

71. Based on my review of the ’378 patent, I note that it also references a PCT application on its face, which was filed May 3, 2018.

72. For purposes of this declaration, I have been asked to assume that May 3, 2018 is the effective filing date of the ’378 patent. My opinions in this declaration were formed from the perspective of a POSITA as of May 3, 2018, including both the knowledge of a POSITA at that time as well as how a POSITA would have understood the ’378 patent and the prior art.

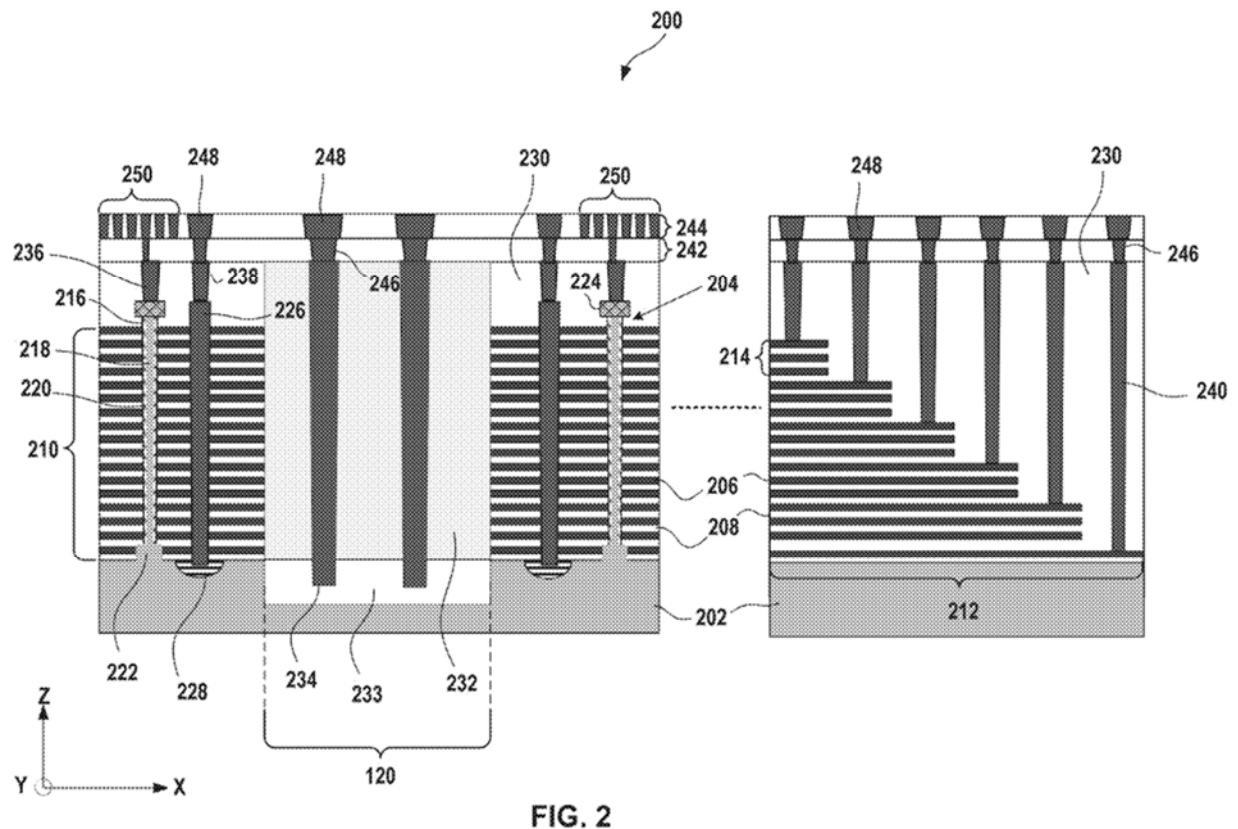
B. Overview

73. The ’378 patent relates to “three-dimensional (3D) memory devices.” Ex. 1001, 1:13-16. The title of the ’378 Patent is “Through Array Contact (TAC)

¹ This prior art reference etches through a TEOS layer, which a POSITA would have understood to consist of silicon oxide.

For Three-Dimensional Memory Devices.” In particular, the specification describes and illustrates various “[e]mbodiments of interconnect structures of a three-dimensional (3D) memory device and method[s] for forming the interconnect structures.” *Id.*, Abstract.

74. To begin, as seen in Fig. 2 of the '378 patent below, the specification describes and illustrates a “3D memory device 200” with an overall 3D NAND architecture similar to that of the conventional BiCS architecture (*e.g.*, vertical memory strings, staircase region for word line access, etc.) that I discussed previously in the Technology Background.



Ex. 1001, Fig. 2.

77. The alleged point of novelty in the '378 patent is a 3D memory device containing “vertical interconnects” that are located between a “stacked array device” (such as “3D memory device 200”) and a “peripheral device.” Ex. 1001, 5:32-59. In other words, the TACs may provide connections between separately fabricated chips (e.g., a memory chip and a controller chip) that are physically stacked on top of each other to form an overall 3D NAND memory device. *Id.*, 11:5-9. The '378 patent refers to these vertical interconnects as “through array contacts” (“TACs”). *Id.*, 1:51-55; *see also id.*, Title (“Through Array Contact (TAC) For Three-Dimensional Memory Devices”). In Fig. 2 above, element 234 is a TAC. *Id.*, 10:57-59. According to the specification, “[t]he interconnect structures allow contacts to various memory array structures (e.g., NAND strings, gate line slits, word lines, etc.) to be fabricated in a limited number of steps (e.g., in a single step or in two steps), thereby reducing the process complexity and manufacturing cost.” *Id.*, 5:35-40. The cross-sectional profile of the TACs resembles that of a via and tapers slightly from top to bottom, as is common with semiconductor etch processes, which have long been well-known to POSITAs.

78. “In some embodiments, TACs 234 can provide electrical connections between 3D memory device 200 and the peripheral device (e.g., on a CMOS chip; not shown in FIG. 2).” Ex. 1001, 11:3-9. “Each TAC 234 can extend through the entire thickness of dielectric structure 232 and extend through at least a portion of

STI structure 233 in a substrate 202.” *Id.*, 10:67-11:2. Given that the TACs may “provide electrical connections,” it is unsurprising that the specification teaches that “[e]ach TAC 234 is filled with conductor materials, including, but not limited to, W, Co, Cu, Al, doped Si, silicides, or any combination thereof.” *Id.*, 11:9-12. All of these materials were well-known to POSITAs for their conductive properties and had been used long before the ’378 patent.

79. The ’378 patent’s 3D memory device includes an “[e]pitaxial plug” (element 222 in Figure 2) between each “channel structure” (labeled as element 216 in Figure 2) and the “substrate” (labeled as element at 202 in Figure 2). Ex. 1001, Figure 2. The ’378 patent explains that the “epitaxial plug” “can include, for example, a semiconductor material (e.g., single crystalline [silicon]) that is epitaxially grown from the substrate.” *Id.*, 9:37-39.

80. The ’378 patent’s 3D memory device also includes an “etch stop plug” (labeled as element 224 in Figure 2) between each “channel structure” 216 and “NAND string contact” (labeled as element 236 in Figure 2). Ex. 1001, Figure 2. The ’378 patent explains that the “etch stop plug” is “an etch stop layer” made of a material such as polysilicon “that prevents etching of dielectrics,” “such as SiO₂ and SiN,” “in channel structure 216.” *Id.*, 9:44-46. “In some embodiments, etch stop plug 224 acts as the drain of NAND string 204.” *Id.*, 9:47-48.

C. Prosecution History

81. As noted above, I have reviewed the '378 patent's file history. I focus my discussion of the file history as it relates to the challenged claims. In this regard, the file history is quite short. In particular, in the first Office Action, the Examiner indicated that then-pending dependent claims 2 and 17 would be allowable if rewritten in independent form. Ex. 1002, 536. The Applicant did just this. *Id.*, 570 ("Applicant thanks the Examiner for indicating the allowability of claims 2 and 17 if they were rewritten in independent form including all limitations of the base claim and any intervening claims. Applicant has amended claims 1 and 16 to respectively recite features of claims 2 and 17."). Thus, the limitations of claim 2 were incorporated into independent claim 1 in the as-issued '378 patent. *Id.* And the limitations of claim 17 were incorporated into independent claim 16, which was subsequently renumbered to be independent claim 15 in the as-issued '378 patent. *Id.*, 589 (showing renumbering). Challenged claims 2-7 depends on claim 1, and challenged claim 18 depends on independent claim 15. Thus, all challenged claims resulted from a First Action allowance.

82. The limitation of dependent claim to that were incorporated into claims 1 to obtain allowance were: *an epitaxial layer, an etch stop plug, a staircase structure, slit structures, and contact layers*. The limitations of dependent claim 17 that were incorporated into the independent claim 15 to obtain allowance were: *a*

staircase structure ... , a word line contact disposed on each conductor layer of the staircase structure, and a local contact disposed on each channel structure and slit structure. Ex. 1002, 110. As I discuss in the Technology Background, these elements were all well-known to POSITAs and conventional in 3D NAND devices by 2018.

83. I note that other claims in the '378 application (none of which I analyze in this declaration) were rejected by the Examiner as obvious in view of U.S. Pat. No. 9,620,512 ("Nishikawa," Ex. 1017) combined with U.S. Pat. Publ. No. 2016/0056188 ("the 188 Publication," Ex. 1018). Ex. 1002, 530.

84. The prior art references I discuss in this declaration are not cumulative of those that the Examiner discussed. I note that U.S. Pub. 2017/0179026 (Ex. 1005, "Toyama") was cited in an IDS, but was not used as the basis for a rejection or otherwise discussed by the Examiner in the file history. With respect to Nishikawa, the Examiner found that it did **not** disclose *through array contacts*, instead relying on the 188 Publication. Ex. 1002, 531 ("Nishikawa appears to be silent as to, but does not preclude, the elements of one or more through array contacts (TACs) extending vertically through the dielectric structure and the isolation region. [The 188 Publication] teaches the elements of: one or more through array contacts (TACs) (83) extending vertically through the dielectric structure and the isolation region [0067]. It would have been obvious to one having ordinary skill in the art at the time

the application at hand was filed to modify the device taught by Nishikawa with the aforementioned elements taught by [the 188 Publication]”). But the 188 Publication is titled “IMAGE SENSOR HAVING SHIELDING STRUCTURE” and does not even relate to memory, let alone a 3D NAND memory device. Ex. 1018, Abstract; *see also id.*, [0028] (“Referring to FIGS. 1A to 1C, the image sensor 10A includes a pixel array PA, peripheral circuit areas PCA, an interface areas IA, and a shielding structure 50 formed in the interface areas IA.”), [0097] (“FIG. 10A is a schematic block diagram for describing a camera system including one of the image sensors”). By contrast, the primary reference in this Petition (Toyama) both discloses this and renders obvious ***all*** claim elements, including the claimed *through array contacts*.

D. Claims

85. For reference, I have reproduced below the challenged claims (*i.e.*, claims 1-7 and 18) of the '378 patent as well as claim 15, on which challenged claim 18 depends:

1. [1.PRE] A three-dimensional (3D) memory device, comprising:
 - [1.A] a semiconductor substrate;
 - [1.B] an alternating layer stack disposed on the semiconductor substrate;
 - [1.C] a dielectric structure on an isolation region of the substrate and extending vertically through the alternating layer stack, wherein the alternating layer stack abuts a sidewall surface of the

dielectric structure and the dielectric structure is formed of a dielectric material;

[1.D] one or more through array contacts (TACs) extending vertically through the dielectric structure and the isolation region;

[1.E] one or more channel structures extending vertically through the alternating layer stack;

[1.F] an epitaxial layer between the one or more channel structures and the semiconductor substrate;

[1.G] an etch stop plug on each of the one or more channel structures;

[1.H] a staircase structure in the alternating layer;

[1.I] slit structures extending vertically in the alternating layer stack; and

[1.J] one or more contact layers on the one or more TACs, the one or more channel structures, and the slit structures.

2. The 3D memory device of claim 1, wherein the dielectric structure abuts a sidewall surface of the TACs.

3. The 3D memory device claim 1, wherein the 3D memory device is a NAND 3D memory device.

4. The 3D memory device of claim 1, wherein the alternating layer stack comprises alternating pairs of a dielectric and a conductor layer.

5. The 3D memory device of claim 1, wherein the dielectric material is silicon oxide.

6. The 3D memory device of claim 1, wherein the dielectric structure comprises an oxide.

7. The 3D memory device of claim 1, wherein the dielectric structure defines a through array contact region within the 3D memory device.

15. [15.PRE] A three-dimensional (3D) memory device, comprising:

[15.A] a substrate with an isolation structure;

[15.B] an alternating conductor/dielectric layer stack disposed on the substrate;

[15.C] a dielectric structure on the isolation structure and extending vertically through the alternating conductor/dielectric layer stack, wherein the alternating conductor/dielectric layer stack abuts a sidewall surface of the dielectric structure and the dielectric structure is formed of a dielectric material;

[15.D] channel structures and slit structures extending vertically through the alternating conductor/dielectric layer stack;

[15.E] a staircase structure disposed in the alternating conductor/dielectric layer stack, wherein the staircase structure comprises levels with each level having a conductor layer thereon;

[15.F] a word line contact disposed on the conductor layer of the each level;

[15.G] local contacts disposed on the channel structures and the slit structures; and

[15.H] through array contacts (TACs) extending vertically through the dielectric and the isolation structures.

18. [18.PRE] The 3D memory device of claim 15, further comprising:

[18.A] an etch stop plug interposed between each local contact of the local contacts and each channel structure of the channel structures; and

[18.B] an epitaxial layer disposed between the channel structures and the substrate.

VIII. CLAIM CONSTRUCTION

86. I am not a legal expert or an attorney and offer no opinions on the law. I understand that claim construction is a matter of law. However, I have been informed by counsel of the legal standards that apply to claim construction in an *inter partes* review, and I have applied them in forming my opinions. I understand that during an *inter partes* review, the same claim construction standard used in federal district court is applied when addressing the meaning of claim terms.

87. I have been informed that the words of a claim are generally given their plain and ordinary meaning that the term or phrase would have to POSITA at the time of the invention in view of the surrounding claim language, the specification and the file history (collectively, the “intrinsic evidence” or “intrinsic record”).

88. I also understand that courts may consider extrinsic evidence, such as expert and inventor testimony, dictionaries, and learned treatises (collectively, the “extrinsic evidence” or the “extrinsic record”), but that such extrinsic evidence should be given less weight than the intrinsic evidence.

A. “a staircase structure in the alternating layer”

89. Limitation [1.H] of claim 1 recites the following: “*a staircase structure in the alternating layer.*” A POSITA would have recognized that this limitation has a typographical error, and would have understood the limitation to mean “a staircase structure in the alternating layer **stack**.” This interpretation is the only reasonable interpretation of that limitation.

90. To start, the claim limitation does not make sense as written. The claim lacks antecedent basis for *the alternating layer*, but does provide an antecedent for *the alternating layer stack*. The claim (at limitation [1.B]) recites *an alternating layer stack disposed on the semiconductor substrate*. From the context of the claim, a POSITA would have understood that the Patent Owner intended for the subsequent limitation [1.H] to refer to the alternating layer stack recited earlier at limitation [1.B].

91. The specification confirms to a POSITA that the patent owner intended limitation [1.H] to refer to the *alternating layer stack* recited at limitation [1.B]. As I explain in this declaration, a staircase structure is a commonly used structure in 3D

NAND flash memories that is part of the alternating conductor/dielectric layer stack. *E.g.*, Section VI.A (technical background). Consistent with this general knowledge in the field, the specification always describes the staircase structure as being part of the alternating conductor/dielectric layer stack. *E.g.*, Ex. 1001, 8:48-50. By contrast, the specification never describes an “alternating layer” except in the context of an alternating layer stack.

92. The prosecution history, which I discuss above, does not suggest any different interpretation. The prosecution of claim 1 did not focus on limitation [1.H], so there is essentially no relevant discussion of that specific limitation.

B. Other Terms

93. In my opinion, other than the limitation above the challenged claims do not require further construction and can be afforded their plain and ordinary meaning for purposes of the analysis of the prior art that I am conducting in this declaration.

IX. UNPATENTABILITY ANALYSIS

94. For the reasons I explain in greater detail below, it is my opinion that as of the effective filing date of the '378 patent, claims 1-7 and 18 of the '378 patent are unpatentable as obvious over the prior art discussed in this declaration.

A. Overview of Toyama

95. Toyama (U.S. Pub. 2017/0179026) is titled “Through-Memory-Level Via Structures for a Three-Dimensional Memory Device.” Ex. 1005. Toyama was

filed September 19, 2016, and issued on June 22, 2017. *Id.* Toyama claims priority to December 22, 2015. *Id.* I am informed that Toyama is prior art under at least 35 U.S.C. §102(a)(1) and §102(a)(2). Toyama is the principal prior art reference that I discuss in this declaration.

96. Toyama is generally directed to “[a] three dimensional NAND memory device” that includes conventional 3D NAND memory features such as “an alternating stack of word lines and insulating layers located over the word line driver devices” and “a plurality of memory stack structures extending through the alternating stack.” Ex. 1005, Abstract. Toyama also discloses “through-memory-level via structures” that “extend through a through-memory-level via region located between a staircase region of the first memory block and a staircase region of another memory block.” *Id.*

97. Toyama is a lengthy reference, including 76 figures (many with sub-parts) and over 60 columns of text. Much of Toyama describes the manufacturing processes and techniques used to form the 3D NAND memory structures it describes. I will highlight here only two of Toyama’s embodiments, which are the focus of my substantive invalidity analysis. The first is Toyama’s “first exemplary structure,” which is depicted in Figs. 1-17, and described in the accompanying text. *See generally* Ex. 1005, [0014]-[0049], [0163]-[0260]. The second is Toyama’s “second modification to [its] fourth exemplary structure,” which I refer to hereafter

as Toyama's "Second Modification" for shorthand. Toyama's Second Modification is depicted in Figs. 44-49, and described in the accompanying text. *Id.*, [0093]-[0103], [0332]-[0342]. I note that other figures and text are also relevant as some of Toyama's disclosure and teachings are generally applicable to all embodiments, and certain aspects of one embodiment are simply expanded upon by other embodiments. Each of Toyama's first exemplary structure and Second Modification independently discloses, or renders obvious, all of the challenged claims for the reasons I discuss in Section IX.B.

98. ***First Exemplary Structure.*** Many of the features of Toyama's first exemplary structure (*e.g.*, alternating layers of conductor/dielectric, memory array region 100 containing memory strings that extend through the stack of alternating conductors 146, 246 and dielectrics 132, 232, a staircase structure, word line contacts 86 on the staircase structure, etc.) can be seen in the cross-sectional diagram of Fig. 17C below.

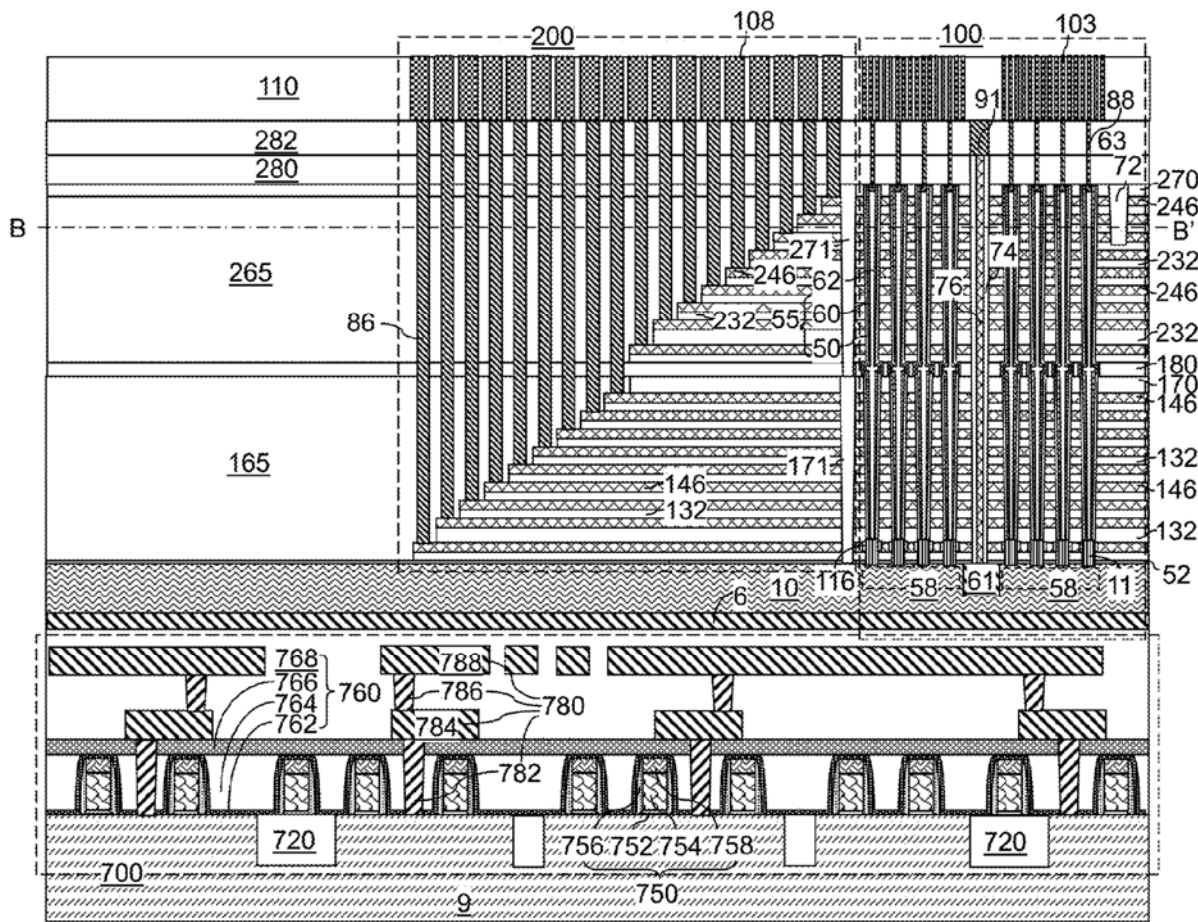


FIG. 17C

Ex. 1005, Fig. 17C.

99. And, like the '378 patent's *through array contacts*, Toyama's first exemplary embodiment discloses 3D NAND memory devices with "through-memory-level via structures," which are vias that extend through the memory array to provide electrical connection to "peripheral" devices. Ex. 1005, [0164] (discussing "peripheral device region 700" located underneath the "memory-level assembly").

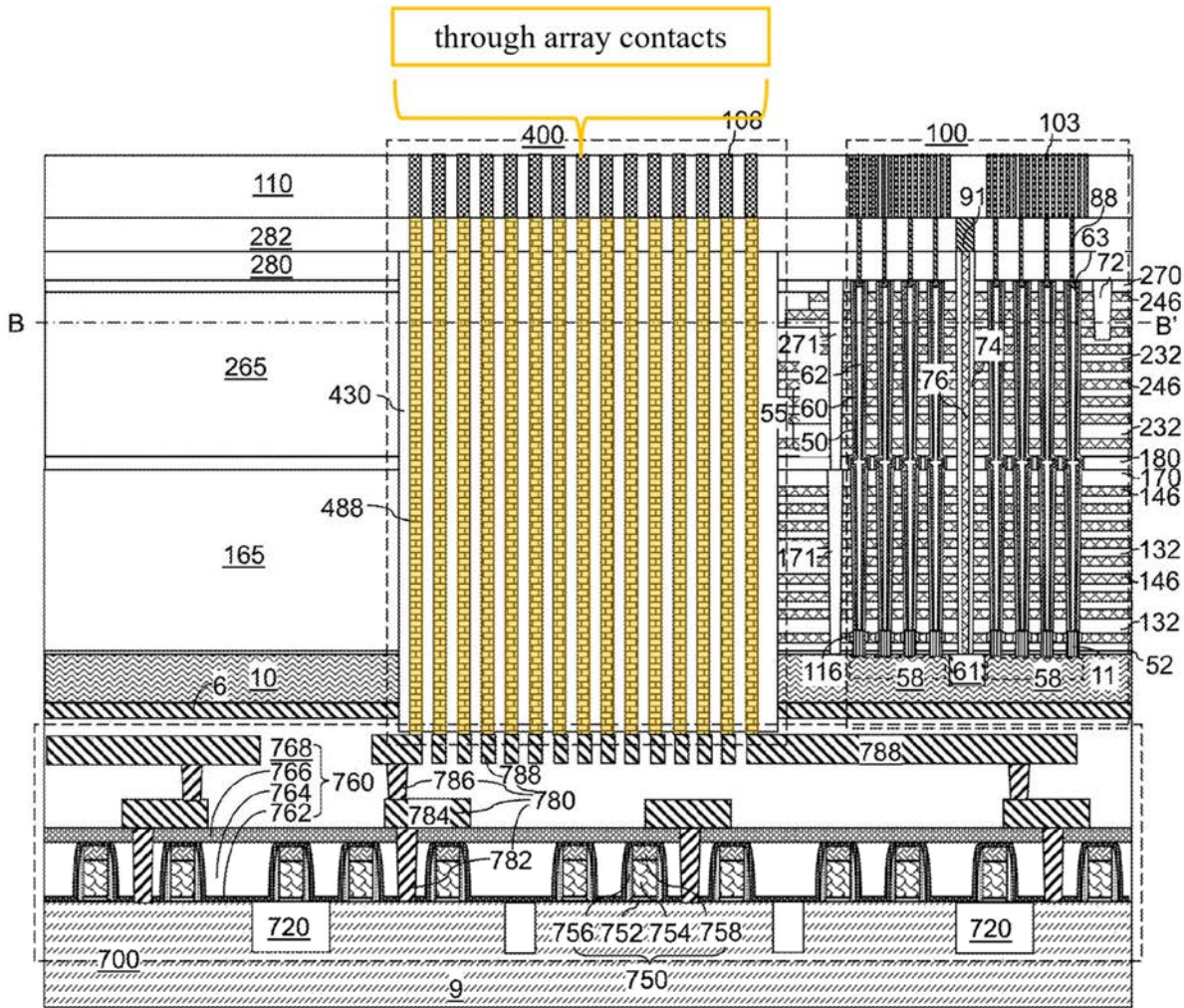


FIG. 17A

Id., Fig. 17A (annotated).

100. As I mentioned in my introduction to this declaration, this is the second declaration I have provided on the '378 patent. The claims to which this declaration pertains include two primary limitations not discussed in my prior declaration: the “epitaxial layer” limitation, and the “etch stop plug” limitation. Toyama discloses both of these limitations.

101. Toyama discloses a layer between its substrate (“planar semiconductor material layer 10”) and its “memory stack structures 55” that it calls “pedestal channel portions 11” or “epitaxial channel portions 11.” Ex. 1005, Figures 17A, [0202], [0208]. The latter name would have confirmed to a POSITA that element 11 is formed using an epitaxial process, and that “portions 11” is an *epitaxial layer*.

102. Toyama also discloses an element between each of “memory stack structure 55” and “drain contact via structure 88” that Toyama calls a “drain region 63.” Ex. 1005, Figure 17A, [0209], [0241]. Toyama’s “drain regions 63” are made of a material such as polysilicon, and the POSITA would have recognized that they act as an etch-stop and prevent etching of dielectrics within “memory stack structure 55.” (For more detail, see my discussion of limitation [1.G].) A POSITA would have recognized that “drain regions 63” serve as the drains of “memory stack structures 55.” *Id.*, [0209], [0241], [0251]. As explained in further detail at limitation [1.G], because “drain regions 63” are plugs that stop an etch from reaching “memory stack structures 55,” they are *etch stop plugs*.

103. **Second Embodiment.** Many of the features of Toyama’s Second Embodiment (*e.g.*, alternating layers of conductor/dielectric, memory array region 100 containing memory strings that extend through the stack of alternating conductors, etc.) can be seen in the cross-sectional diagram of the 3D NAND memory device in Fig. 49 below. And, like the ’378 patent’s *through array contacts*,

Toyama's Second Embodiment discloses "through-memory-level via structures 676" (highlighted in yellow below) that extend through the memory array to provide electrical connection to "peripheral" devices. Ex. 1005, [0341], [0164] (discussing "peripheral device region 700" located underneath the "memory-level assembly").

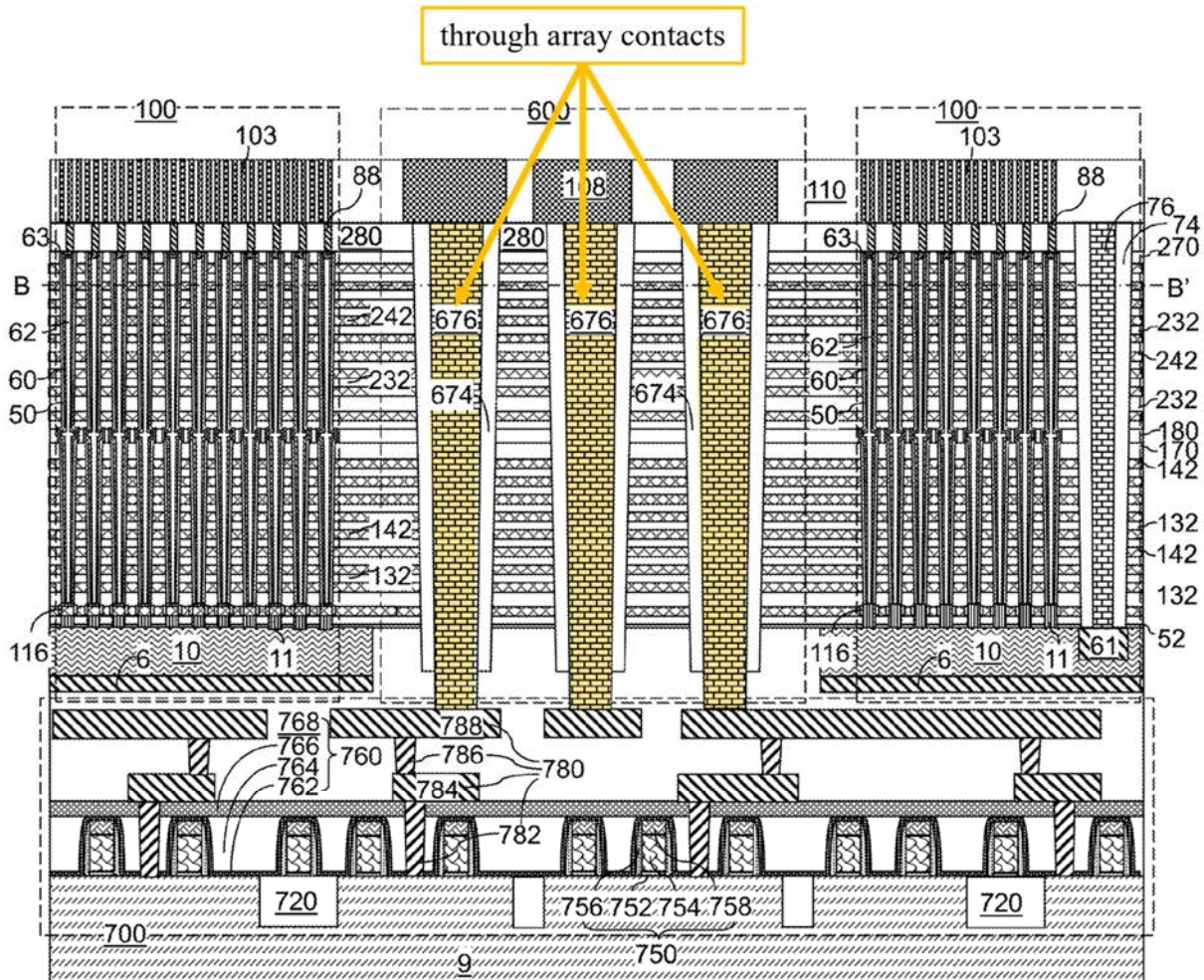


FIG. 49

Id., Fig. 49. As the above figure shows, Toyama's Second Modification—like its first exemplary structure—includes *an epitaxial layer* ("pedestal channel portions 11") and *an etch stop plug* ("drain region 63").

104. The last observation I will make here is that many of Toyama's figures build on one another to illustrate various steps in the fabrication process (*e.g.*, one figure will show an etch step to create a cavity and the next figure will show the cavity being filled with a dielectric or conductor). This is helpful to know, especially when initially reviewing Toyama.

B. Ground 1: Toyama in View of the Knowledge of a POSITA

105. In my opinion, when viewed and considered in light of the knowledge of a POSITA, Toyama's "second modification of the fourth exemplary structure" (which I refer to as Toyama's "Second Modification" for shorthand) and its first exemplary structure each independently render claims 1-7 and 18 of the '378 patent obvious. I note at the outset that Toyama's Second Modification and its first exemplary structure share some commonalities and I sometimes analyze them together where appropriate (*e.g.*, where Toyama contains general disclosure that applies equally to both embodiments), but frequently provide sub-headings for each and analyze them separately.

1. Claim 1

[1.Pre] "A three-dimensional (3D) memory device, comprising"

106. I offer no opinion on whether the preamble is or is not limiting. However, if the preamble is considered to be a limitation, my opinion is that Toyama discloses it. Indeed, the first sentence of Toyama's detailed description states that

“the present disclosure is directed to three-dimensional non-volatile memory devices, such as vertical NAND strings and other three-dimensional devices, and methods of making the same.” Ex. 1005, [0156]. This disclosure applies to both Toyama’s first exemplary embodiment and its Second Embodiment.

[1.A] “a semiconductor substrate”

107. Toyama’s first exemplary structure and Second Embodiment both have a *semiconductor substrate*. As a preliminary point, the ’378 patent explains that a “substrate” is “a material onto which subsequent material layers are added, or otherwise ‘disposed.’” Ex. 1001, 4:41-43. The ’378 patent further states that “[a] substrate can be a layer, can include one or more layers therein, and/or can have one or more layer thereupon, thereabove, and/or therebelow.” *Id.*, 5:4-6. This is reflected in certain embodiments in the ’378 specification in which “the array device and a peripheral device are formed on different substrates.” *Id.*, 5:40-45.

i. First Exemplary Structure

108. In Toyama’s first exemplary structure, the *semiconductor substrate* is the “planar semiconductor material layer” 10, highlighted in Fig. 17A below. *See, e.g.*, Ex. 1005, [0169]-[0170].

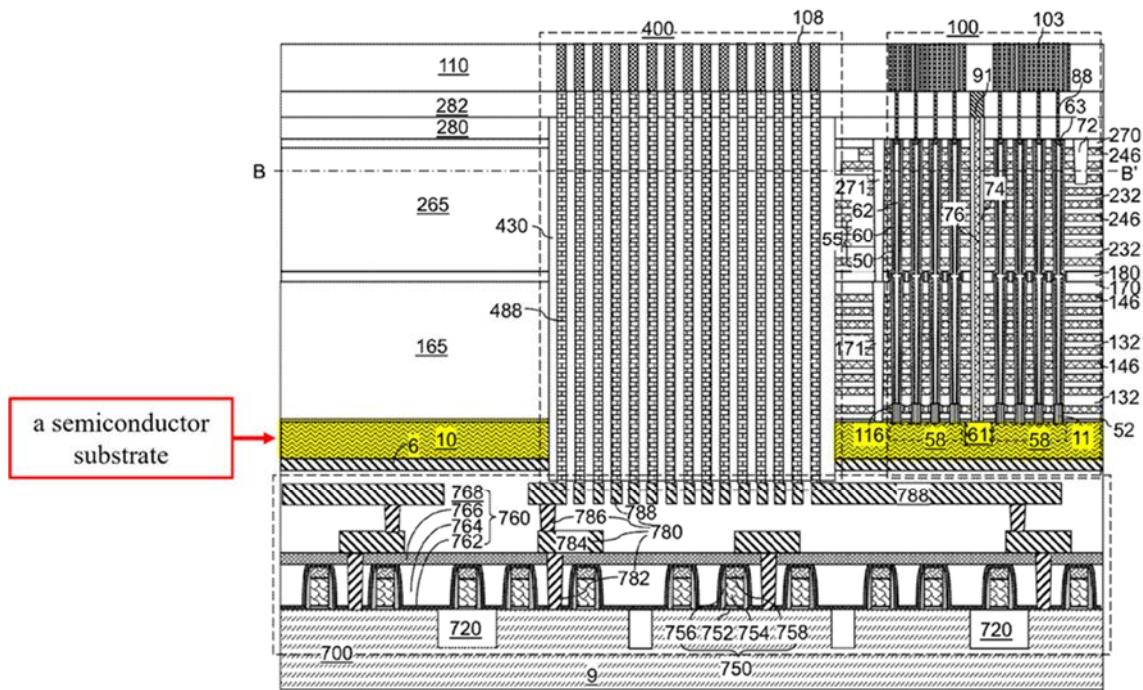


FIG. 17A

Id., Fig. 17A (annotated). Toyama Figs. 2 through 17 depict how various layers are disposed on top of “planar semiconductor material layer 10.” As one example, Toyama notes that “[a]n alternating plurality of the first insulating layers 132 and first sacrificial material layers 142 [are] formed over the planar semiconductor material layer 10.” *Id.*, [0173]. As another example, Toyama explains that “at least one retro-stepped dielectric material portion (165, 265) can be formed over the staircase regions on the at least one alternating stack (132, 142, 232, 242).” *Id.*, [0196]. Because the “planar semiconductor material layer 10” in Toyama is a semiconductor material onto which other materials and layers are added, it is *a semiconductor substrate*.

ii. Second Modification

109. Although the cites above are for Toyama's "first exemplary structure," Toyama's Second Embodiment likewise includes a "planar semiconductor material layer 10" as shown in Fig. 49 below, and thus teaches this limitation for the same reason.

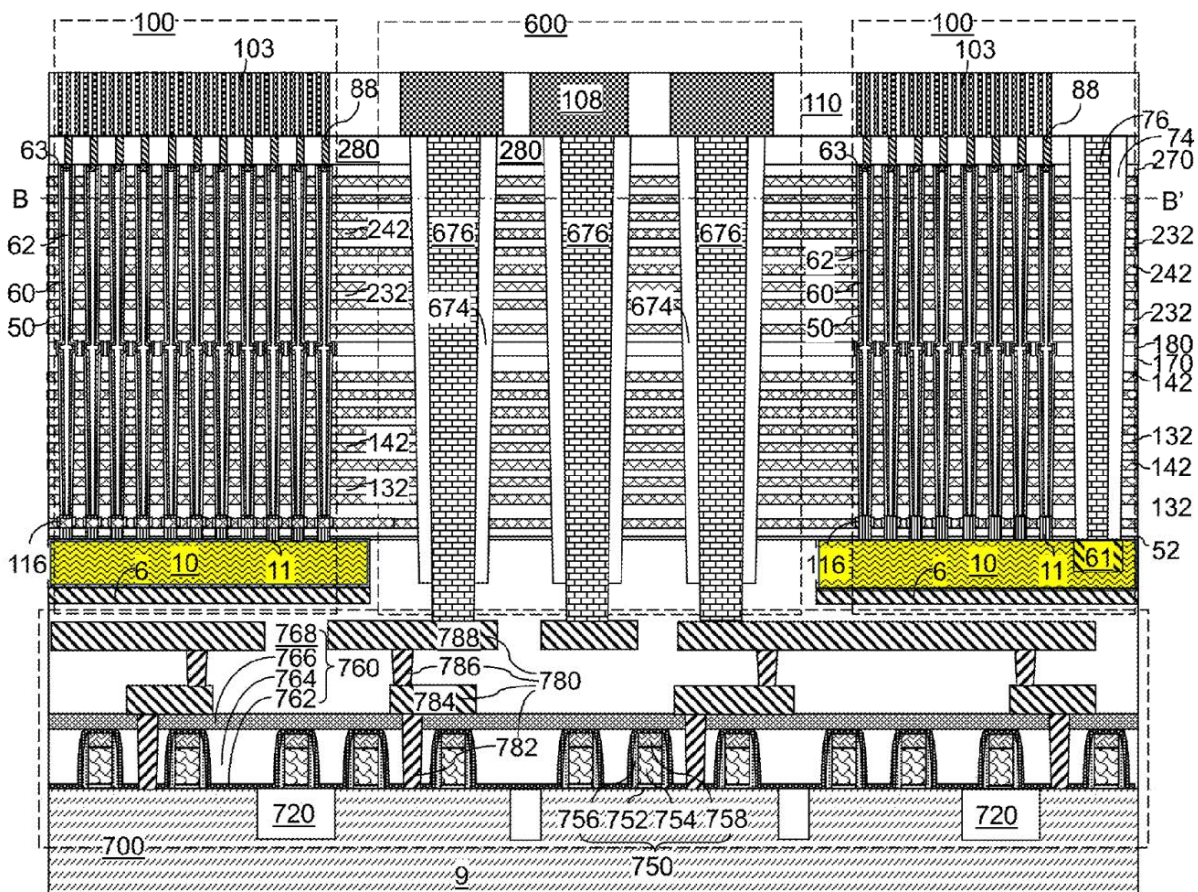


FIG. 49

Ex. 1005, Fig. 49 (annotated).

[1.B] “an alternating layer stack disposed on the semiconductor substrate;”

110. Toyama’s first exemplary structure and Second Embodiment each disclose this limitation. As a preliminary matter that applies to both, the ’378 patent teaches that the term “‘on’ not only means ‘directly on’ something but also includes the meaning of ‘on’ something with an intermediate feature or a layer therebetween.” Ex. 1001, 4:20-25.

ii. First Exemplary Structure

111. As can be seen in Fig. 17A below, Toyama’s “alternating stack (132, 146, 232, 246)” is the claimed *alternating layer stack disposed on the semiconductor substrate*. I note that only some of the alternating conductors (green) and dielectric (yellow) layers are highlighted to avoid cluttering the figure.

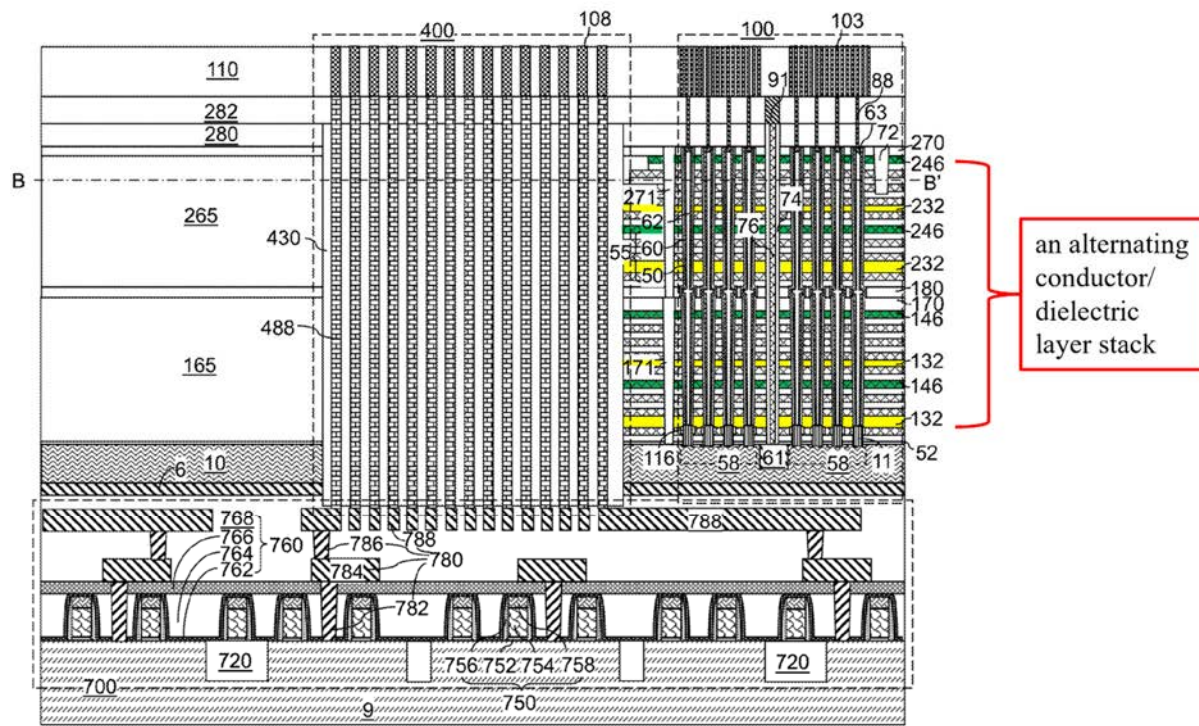


FIG. 17A

Ex. 1005, Fig. 17A (annotated). Toyama “alternating stack” comprises “first and second conductive material layers (146, 246),” “first insulating layers 132,” and “second insulating layers 232.” *Id.*, [0172], [0190], [0228], [0232].

112. Toyama’s “alternating stack” is *disposed on the semiconductor substrate*, per the broad meaning of “on” set forth in the ’378 patent itself. As noted for limitation [1.A], above, Toyama’s “planar semiconductor material layer 10” is a *semiconductor substrate*. Ex. 1005, [0170]-[0171]. As shown in Fig. 17A, above, Toyama’s alternating stack is *disposed on* (above) “planar semiconductor material layer 10.”

ii. Second Modification

113. While the discussion above is for Toyama's "first exemplary structure," Toyama's Second Modification also teaches this limitation (as can be seen in Fig. 49 below) for the same reasons.

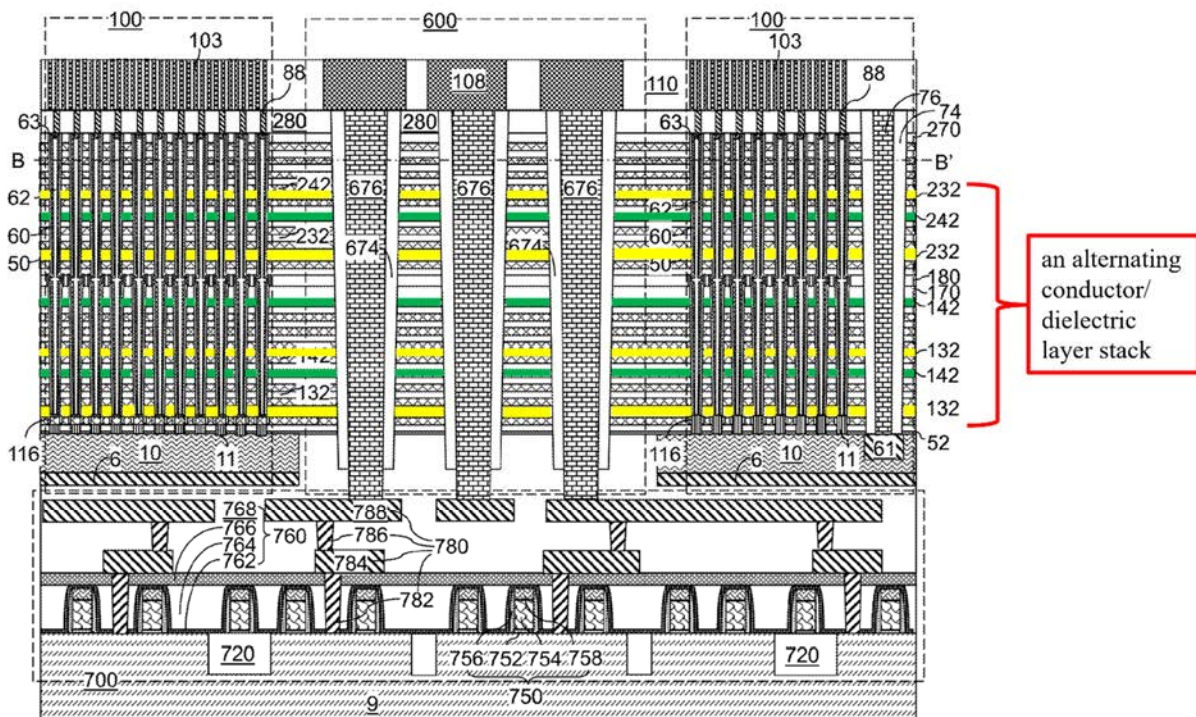


FIG. 49

See, e.g., Ex. 1005, Fig. 49, [0337] ("An alternating stack (132, 146, 232, 246) of insulating layers ([1]32, 232) and electrically conductive layers (146, 246) is thus formed."). In what amounts to a clear typographical error, Fig. 49 labels its *alternating layer stack* as elements 132, 142, 232, 242. Elements 142, 242 are "sacrificial material layers" which, in a process step prior to Fig. 49, were removed and replaced with "electrically conductive layers (146, 246)." *Id.*, [0337], [0340].

That is also reflected in the figures, which depict how the sacrificial material layers (shaded in gray, as in Fig. 45A) are replaced by electrically conductive layers (cross-hatched, as in Fig. 46A).

[1.C] “[i] a dielectric structure [ii] on an isolation region of the substrate and [iii] extending vertically through the alternating layer stack, [iv] wherein the alternating layer stack abuts a sidewall surface of the dielectric structure and [v] the dielectric structure is formed of a dielectric material;”

114. For ease of analysis, I separate this limitation into five sub-parts labelled [i]-[v] and address how Toyama’s Second Modification and first exemplary structure teach each one in turn.

i. Second Modification

[1.C.i] “a dielectric structure”

115. The “insulating liners 674” in Toyama’s Second Modification, shown below in Fig. 49, are the claimed *dielectric structure*. Ex. 1005, [0340].

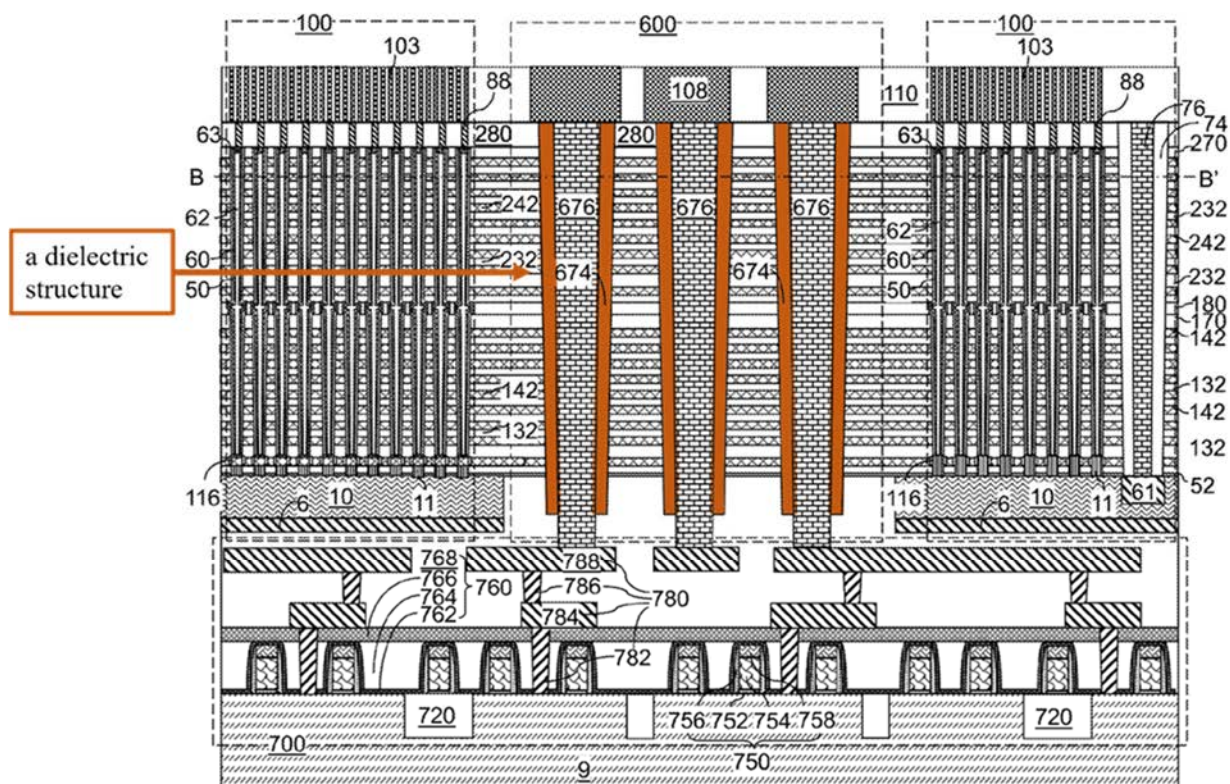


FIG. 49

Id., Fig. 49 (annotated).

116. The “insulating liners 674” are *dielectric*. Toyama forms “insulating liners 674” by depositing “a conformal insulating material layer” in “through-memory-level openings 679.”² Ex. 1005, [0338]-[0340]. Toyama discloses that

² I note that Toyama [0338] refers to “through-memory-level openings 689,” but that appears to be a typographical error. All of the relevant figures (*e.g.*, Figs. 47A-B to 49) and the other textual description refer to the elements as “through-memory-level openings 679.”

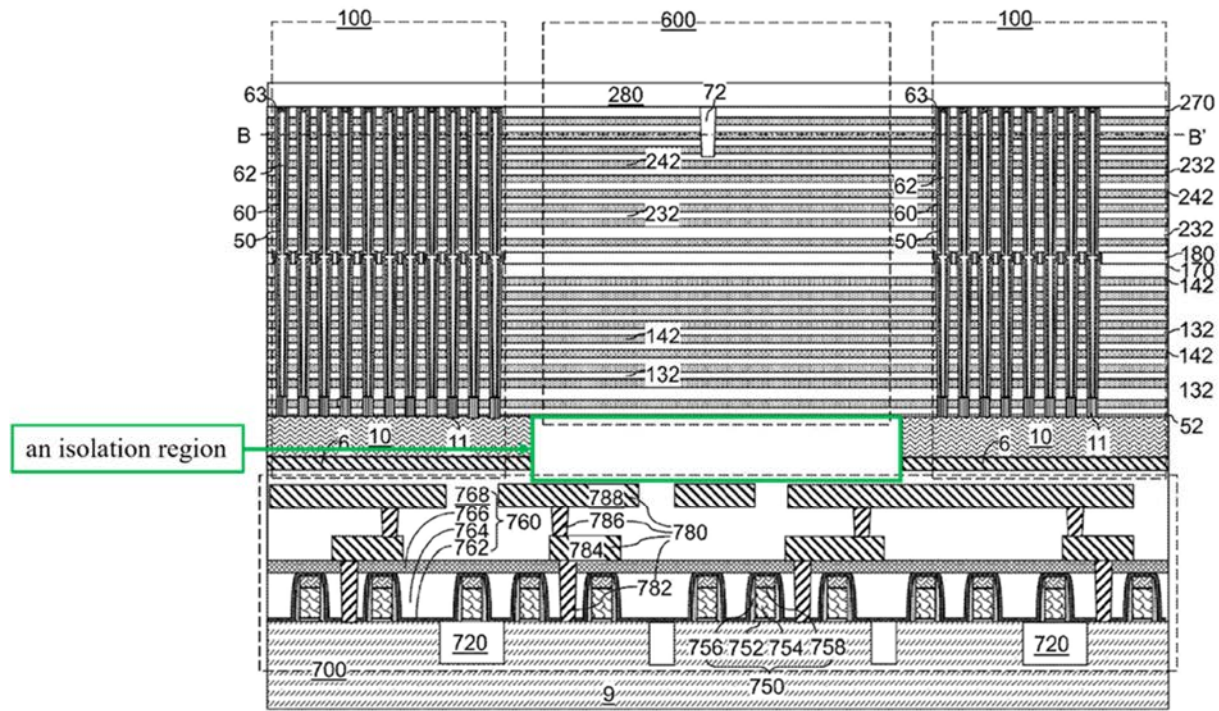
insulating liner 674 may be a “dielectric material.” *Id.*, [0233] (“[a]n insulating spacer 74 including a dielectric material”), [0381] (“insulating liner 674 having a same material composition and a same thickness as the insulating spacer 74”).

117. The challenged claims do not recite, or otherwise require, a “single-material” dielectric structure. This is confirmed by the ’378 patent which contemplates a “single-material” dielectric structure only “[i]n some embodiments.” Ex. 1001, 5:50-59. Regardless, Toyama contemplates that its “insulating liners 674” are made of a single material (e.g., silicon oxide). See claim 5 analysis.

118. Toyama’s “insulating liners 674” are, individually and collectively, a *structure*, which is not an art-specific term and is given its plain and ordinary meaning. See Ex. 1022, 5 (Merriam-Webster’s definition of “structure” as “something (such as a building) that is constructed”). As explained above, they are constructed together, and all have the same function of insulating and electrically isolating the *through array contacts* (“through-memory-level via structures 676”) as they pass through the *alternating layer stack* (“alternating stack (132, 146, 232, 246).” A POSITA would thus have understood that “insulating liners 674” are individually and collectively *a dielectric structure*.

[1.C.ii] “... on an isolation region of the substrate”

119. Toyama’s *isolation region* in the Second Modification is shown in Fig. 44A below.



Ex. 1005, Fig. 44A (annotated).

120. Toyama describes its Second Modification starting after the alternating stack of conductors/insulators has already been formed. See Ex. 1005, Fig. 44A. Toyama states that the “alternating stack of insulating layers (132, 232) and dielectric spacer layers (which can be the sacrificial material layers (142, 242)) can be formed over the semiconductor substrate 9 as in previously described embodiments.” *Id.*, [0332]. Toyama further states that its Second Modification “can be formed concurrently with the formation of any of the first, second, and third exemplary structures or modifications thereof.” *Id.*

121. A POSITA would have thus understood that Toyama's Second Modification would use the process described for the third exemplary structure to create "opening 151" and fill it with an insulating material. Ex. 1005, [0277] ("The optional planar conductive material layer 6 and the planar semiconductor material layer 10 may be patterned to form an opening 151 extending through these layers to the underlying insulating layer 760. The opening 151 ... may be filled with another insulating material layer (e.g., a silicon oxide or doped silicate glass) 760."). The "opening 151" is illustrated in Toyama Fig. 24A below.

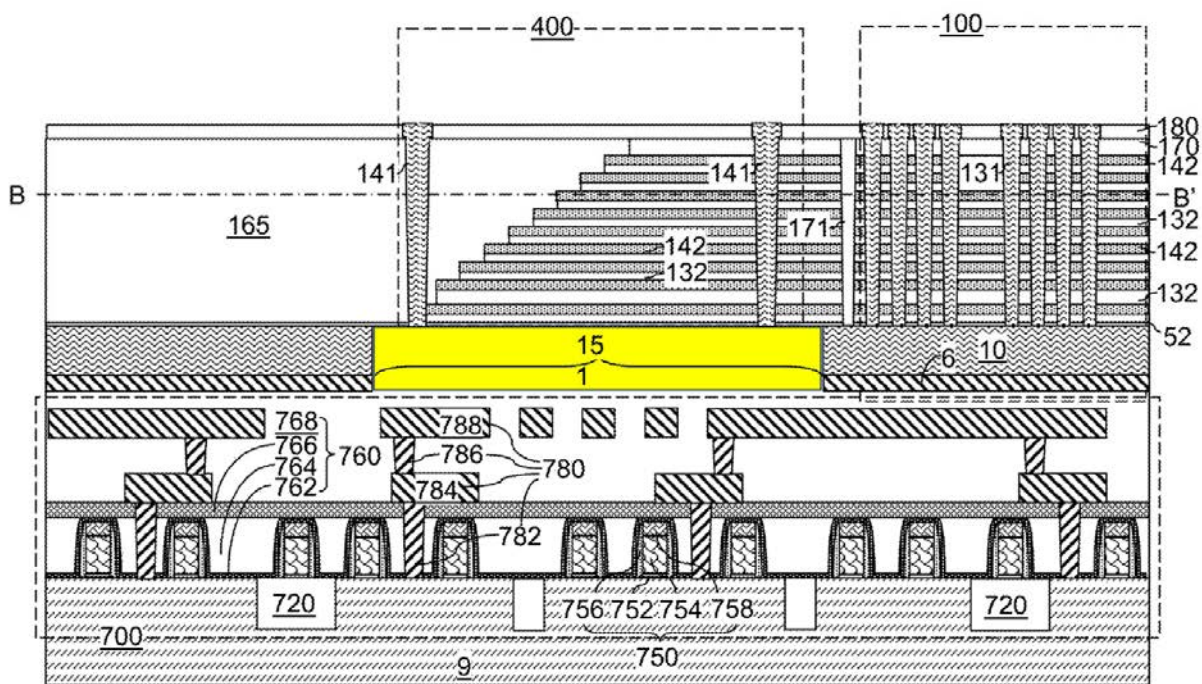


FIG. 24A

Id., Fig. 24A (annotated).

122. A POSITA would therefore have understood that, in the context of Toyama's Second Modification, the insulating material layer that fills "opening 151" is *an isolation region*. Claim element [1.C.ii] requires not only a *semiconductor substrate* and an *isolation region*, but *an isolation region of the substrate*. That Toyama's *isolation region* (the insulating material layer that fills "opening 151") is *of* its *substrate* ("planar semiconductor material layer 10") is apparent because Toyama's *isolation region* (the insulating material layer that fills "opening 151") is formed by removing portions of the substrate and is subsequently formed within the *substrate* ("planar semiconductor material layer 10"). Accordingly, Toyama's Second Modification teaches *an isolation region* (the insulating material layer that fills "opening 151") *of the substrate* ("planar semiconductor material layer 10").

123. As illustrated in Figure 49, below, Toyama further teaches the *dielectric structure* ("insulating liners 674") is *on* the *isolation region* (the insulating material layer filling "opening 151"):

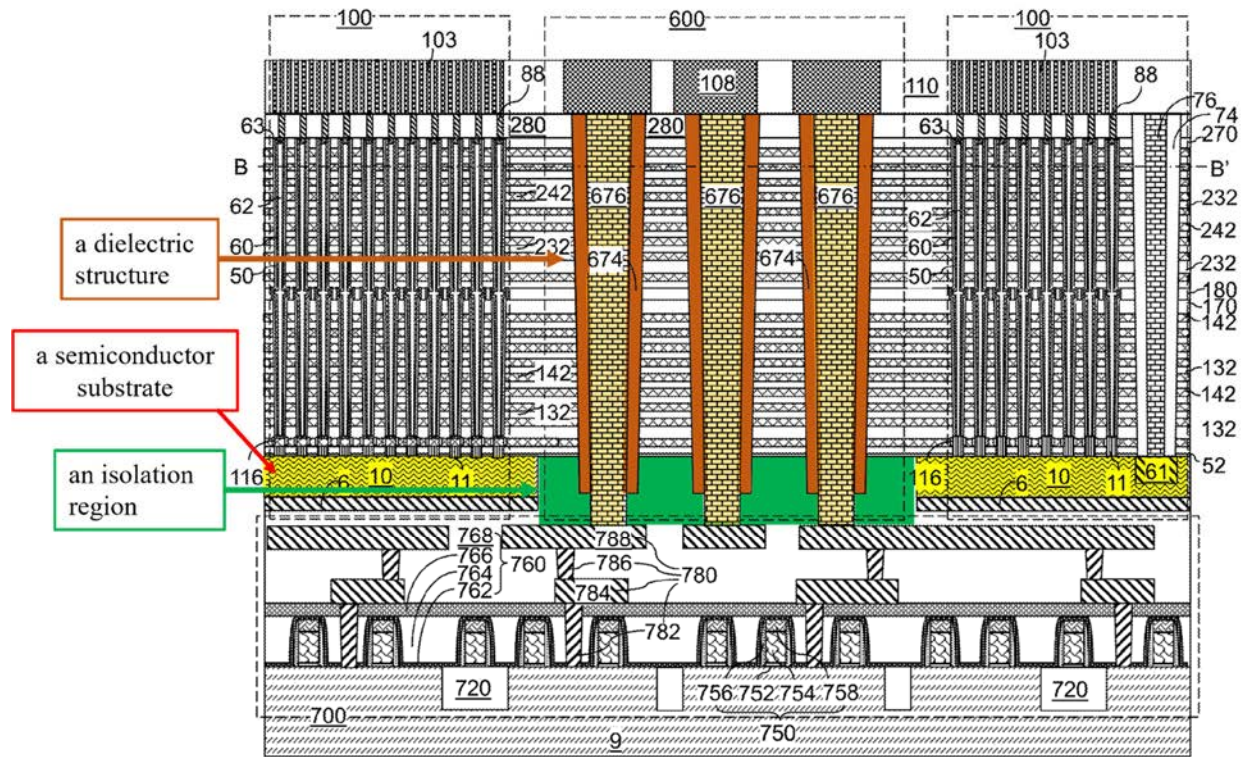


FIG. 49

Ex. 1005, Figure 49; Ex. 1001, 4:20-29 (defining “on”).

[1.C.iii] “a dielectric structure ... extending vertically through the alternating layer stack”

124. As I discuss in the section above, Toyama’s “insulating liners 674” are individually and collectively the claimed *dielectric structure*. And, as I noted above with reference to claim element [1.B], Toyama’s “alternating stack (132, 146, 232, 246)” is *the alternating layer stack*. Accordingly, as shown in Fig 49 below, Toyama discloses *a dielectric structure* (“insulating liners 674”) *extending vertically through the alternating layer stack* (“alternating stack 132, 146, 232, 246”).

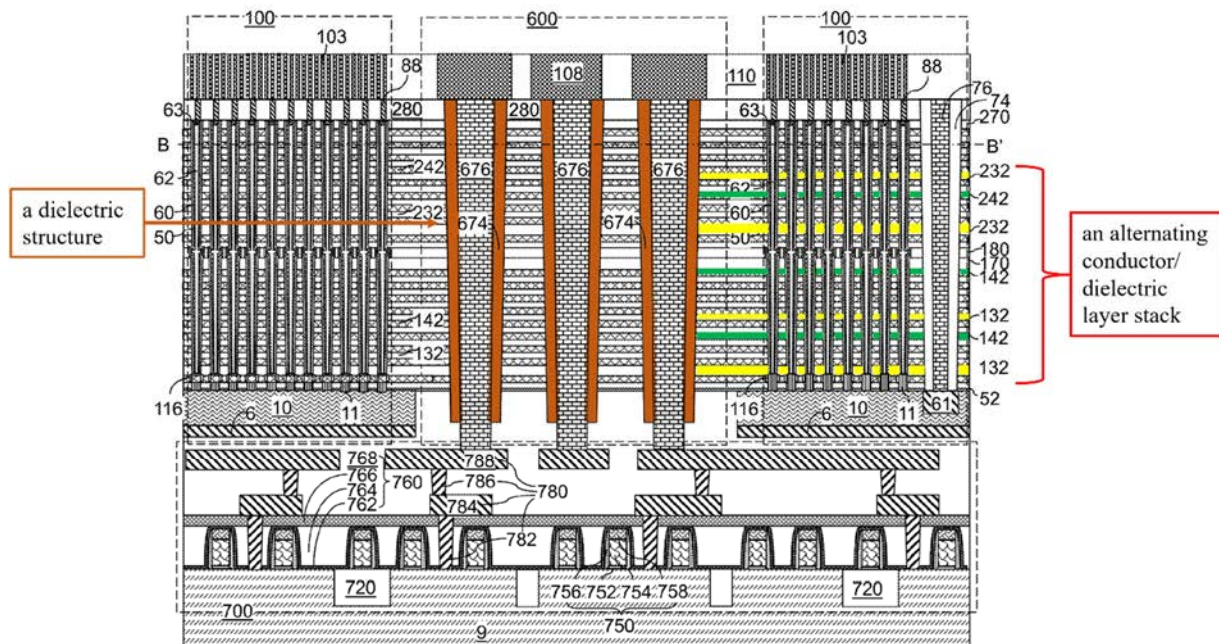


FIG. 49

Ex. 1005, Fig. 49 (annotated). As I noted previously, labels 142 and 242 are properly understood to refer to conductive material layers (146, 246).

[1.C.iv] “a dielectric structure ... wherein the alternating layer stack abuts a sidewall surface of the dielectric structure”

125. As highlighted below in Fig. 49, Toyama discloses *a dielectric structure* (“insulating liners 674”) *wherein the alternating layer stack* (“alternating stack (132, 146, 232, 246)”) *abuts a sidewall surface of the dielectric structure* (a sidewall surface of “insulating liner 674”):

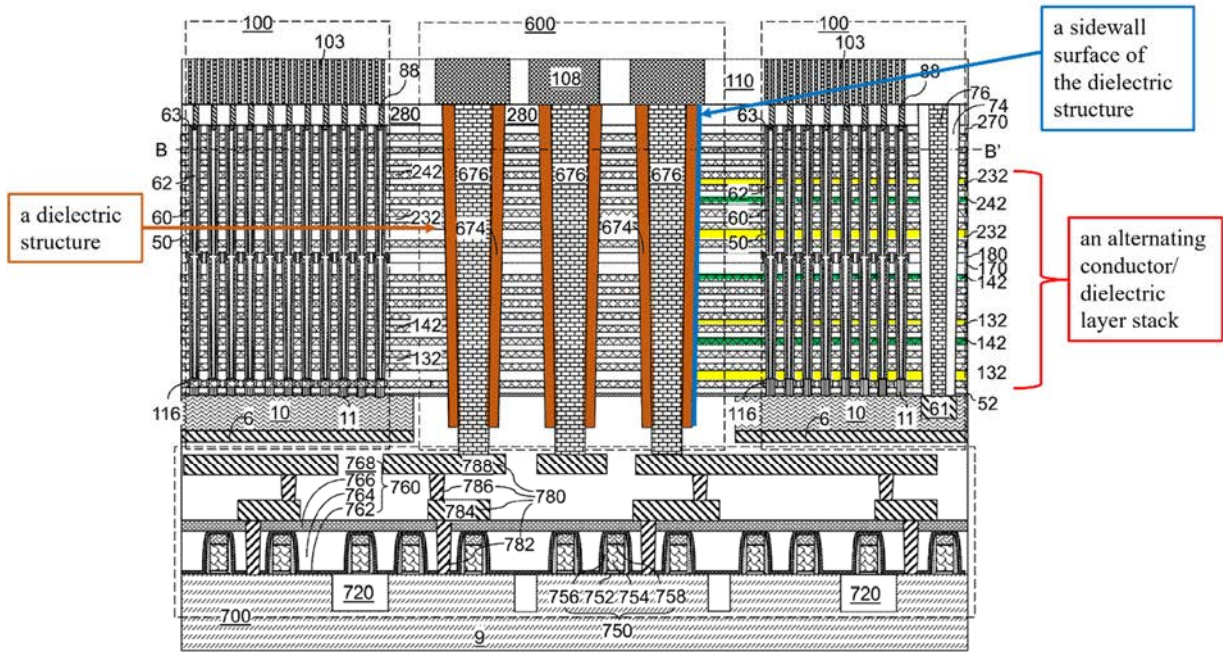


FIG. 49

Ex. 1005, Fig. 49 (annotated). As I noted previously, labels 142 and 242 are properly understood to refer to conductive material layers (146, 246).

[1.C.v] “... wherein ... the dielectric structure is formed of a dielectric material;”

126. As I discussed above, Toyama’s “insulating liners 674” are individually and collectively the claimed *dielectric structure*. And, as I discussed for element [1.C.i], each of these elements is a dielectric material. Toyama thus discloses *a dielectric structure* (“insulating liners 674”) *wherein the dielectric structure is formed of a dielectric material*.

ii. First Exemplary Structure

[1.C.i] “a dielectric structure”

127. As shown below in Fig. 15A, in Toyama’s first exemplary structure the upper part of “dielectric fill material portion 430” (viz., above the top of substrate 10) is the claimed *dielectric structure*:

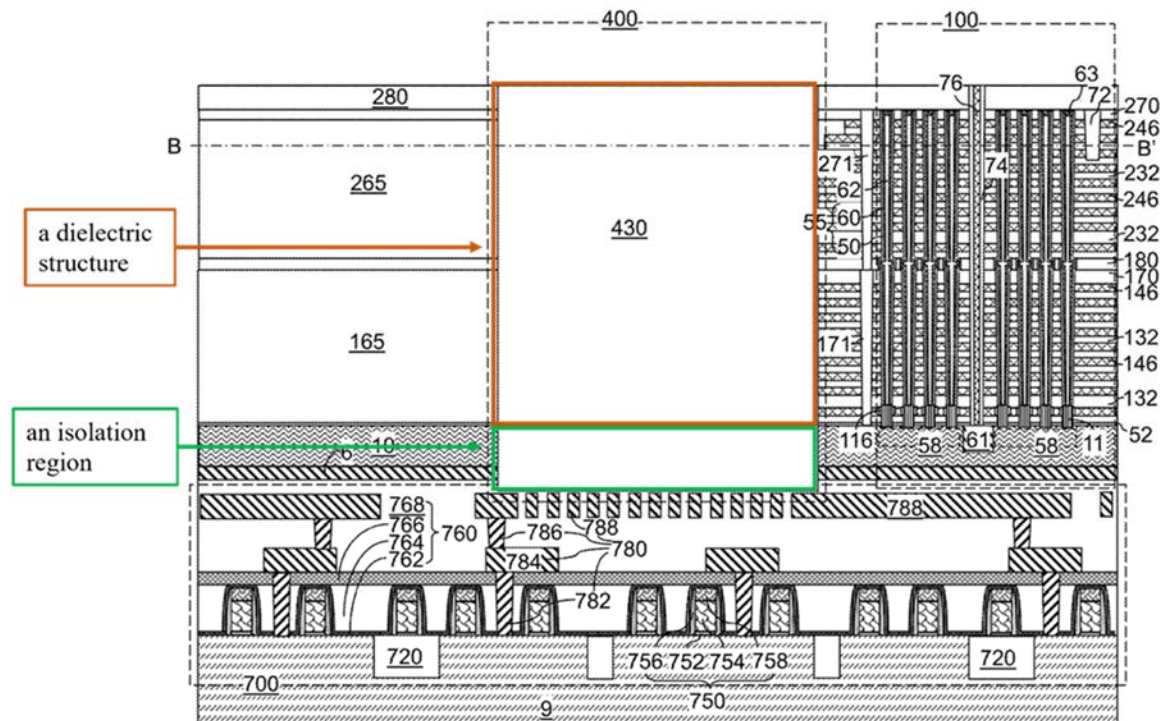


FIG. 15A

Ex. 1005, Fig. 15A (annotated). Toyama explains that “a dielectric fill material portion 430 is formed within each through-memory-level opening 769, for example, by deposition of a dielectric fill material.” *Id.*, [0216]. Thus, the upper section of the “dielectric fill material portion 430” is *a dielectric structure* because it is composed of “a dielectric fill material.” *Id.*

128. As I will discuss below, Toyama’s *dielectric structure* (upper part of “dielectric fill material portion 430”) has the function of electrically isolating Toyama’s *through array contacts* (“through-memory-level via structures 488”) from the *alternating layer stack* (“alternating stack (132, 146, 232, 246)”).

[1.C.ii] “... on an isolation region of the substrate”

129. For Toyama’s first exemplary structure, the lower part of Toyama’s “dielectric fill material portion 430” is *an isolation region*. See, e.g., Ex. 1005, [0216]. Figs. 10A-12A show the formation of this structure. To begin, “through-memory-level via region 400” includes the staircase structure of layers 132, 142, 232, 242:

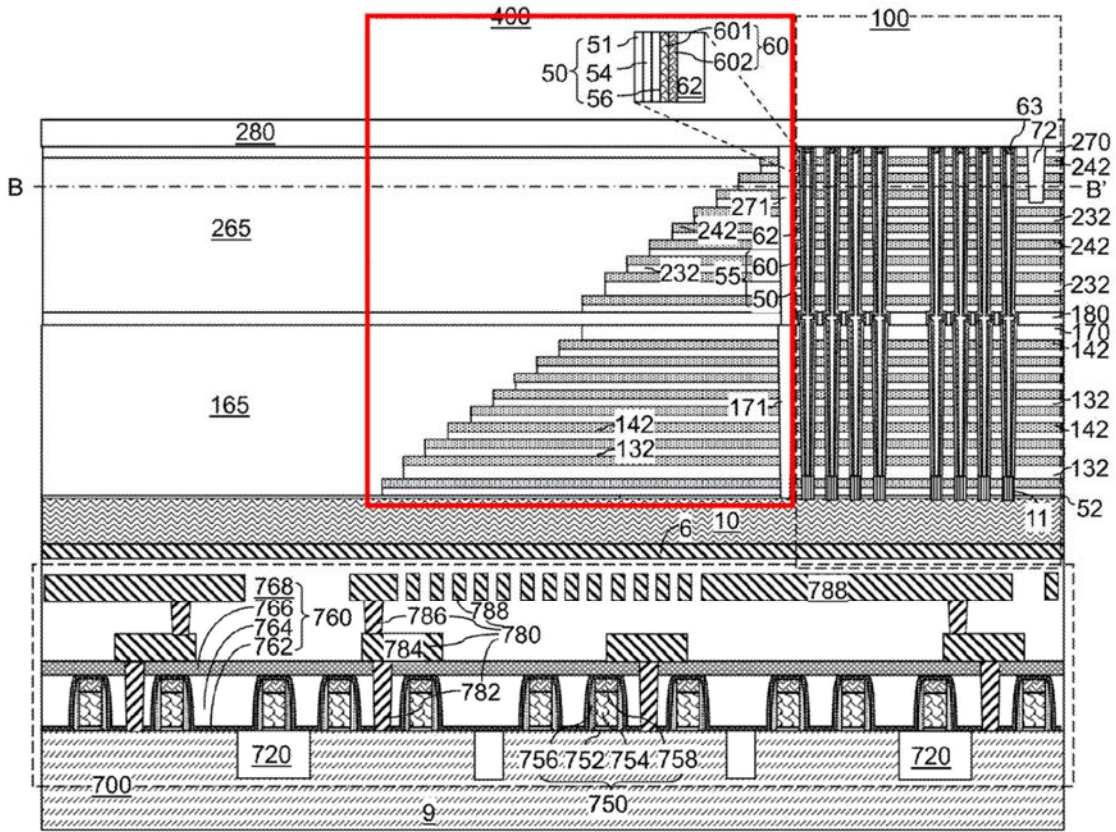


FIG. 10A

Id., Fig. 10A (annotated), [0192]-[0194]. These layers are removed, resulting in “through-memory-level opening 769”:

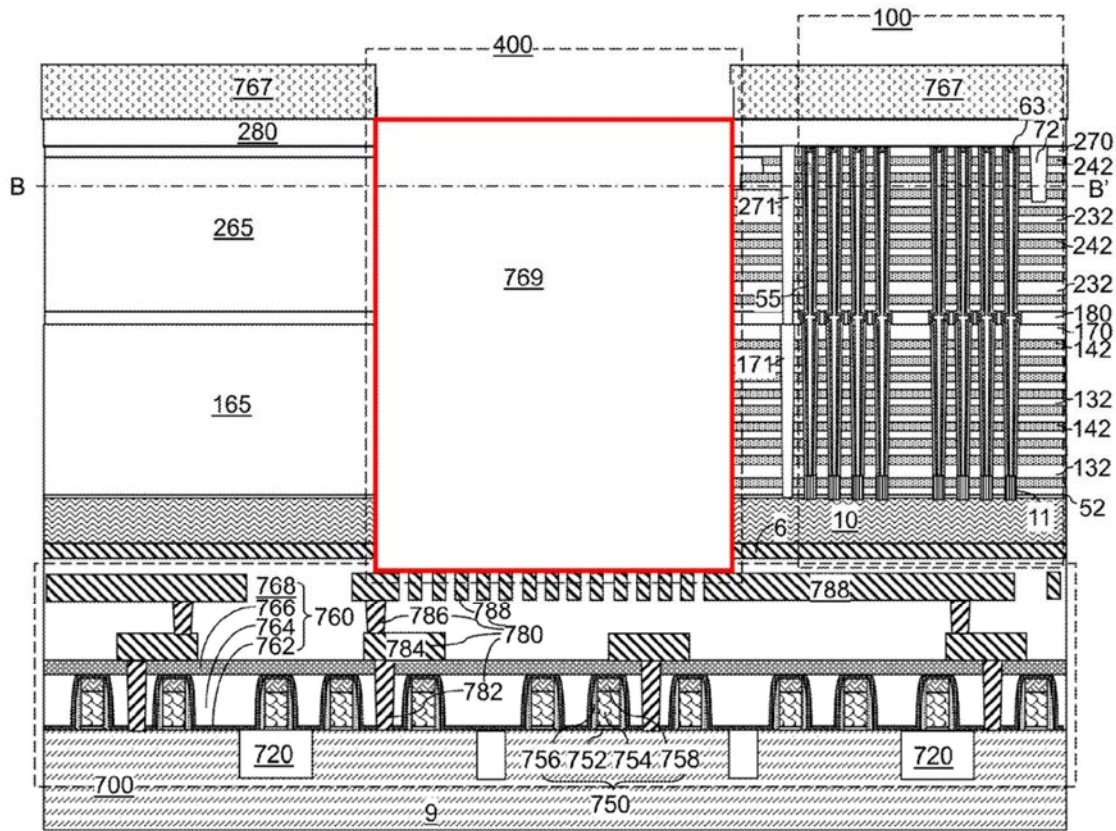


FIG. 11A

Id., Fig. 11A (annotated); [0213]. Next, “opening 769” is filled with a dielectric to form “dielectric fill material portion 430”:

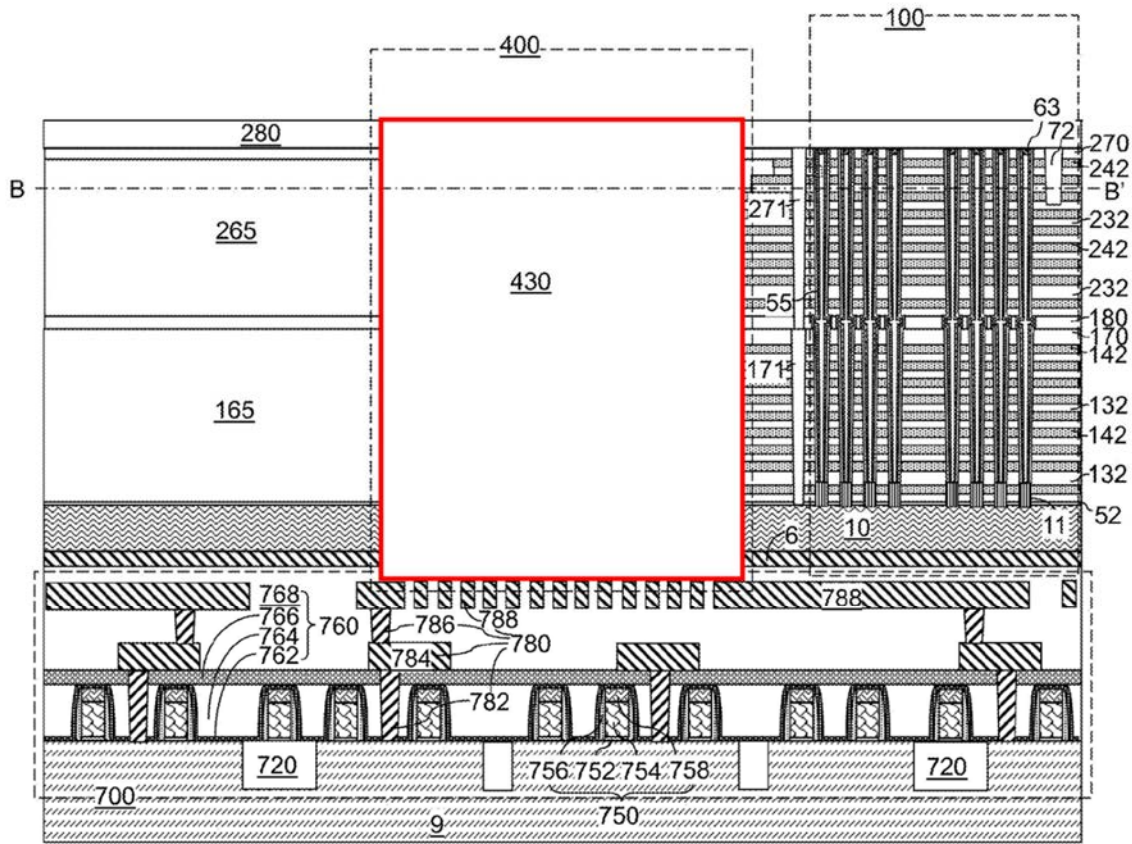


FIG. 12A

Id., Fig. 12A (annotated); [0216]. The lower portion of “dielectric fill material portion 430” (*viz.*, the portion level with and below the top of “planar semiconductor material layer 10”) is the claimed *isolation region*, as shown below:

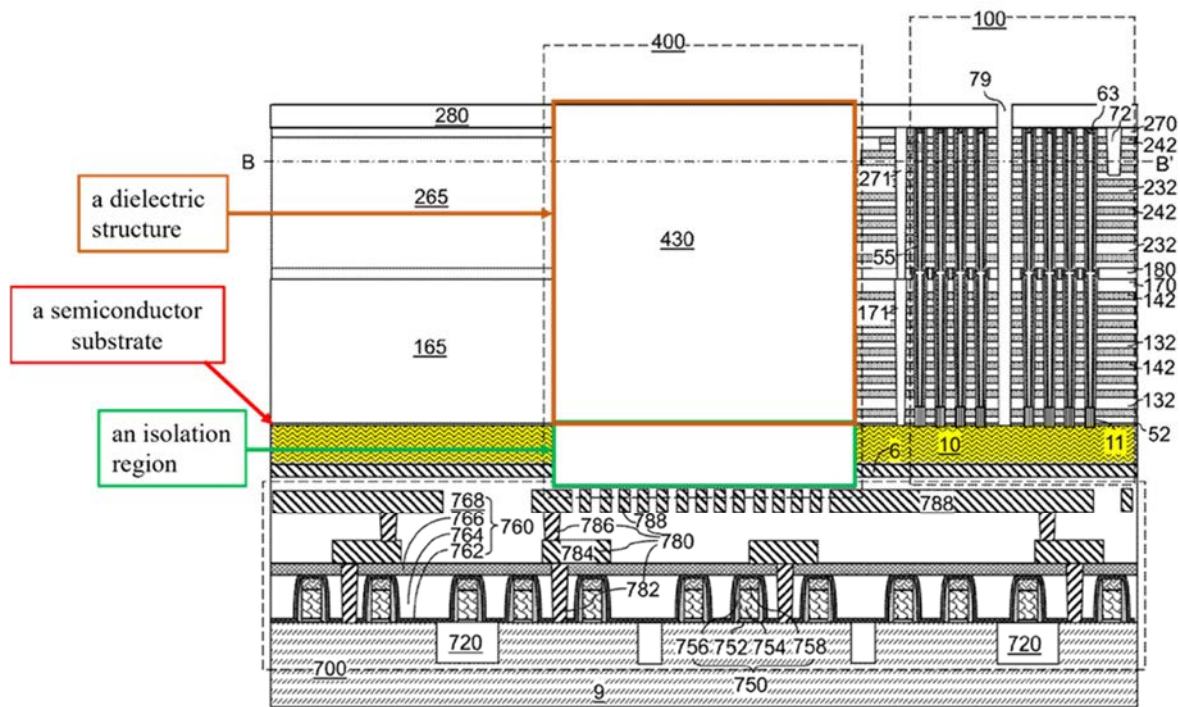


FIG. 13A

Id., Fig. 13A (annotated).

130. Toyama discloses that its “dielectric fill material portion 430 includes a dielectric material such as undoped silicate glass (e.g., silicon oxide.)” Ex. 1005, [0216]. A POSITA would have understood that “dielectric fill material portion 430” is *an isolation region* because it electrically isolates conductors from each other and from electrical interference from the *substrate* (“planar semiconductor material layer 10”).

131. Toyama’s *isolation region* (lower part of “dielectric fill material portion 430”) is *of* its *substrate* (“planar semiconductor material layer 10”) because it is formed by removing a portion of, and is surrounded by, the *substrate* (“planar

semiconductor material layer 10”). Ex. 1005, Figs. 10A-12B (forming “opening 769” in “layer 10,” then filling the opening to form “portion 430”). Indeed, Toyama’s *isolation region* is within the substrate and isolates portions of the substrate from one another.

132. In summary, Toyama’s first exemplary structure discloses *an isolation region* (lower portion of “dielectric fill material portion 430”) *of a substrate* (“planar semiconductor material layer 10”).

133. Recall that Toyama’s *isolation region* is the portion of “dielectric fill material portion 430” at or below the top of substrate 10. Toyama discloses that the first exemplary structure’s *dielectric structure* (upper part of “dielectric fill material portion 430”) is *on the isolation region* (lower portion of “dielectric fill material portion 430”).

134. I note that nothing in the claim requires forming the *dielectric structure* and *isolation region* in different steps or from different materials, nor does the specification prohibit or disavow this. On the contrary, the ’378 specification broadens “isolation structure” (the term primarily used in the specification) beyond the disclosed embodiment when it states that “STI structure 233 is exemplary and not limiting. As such, other isolation structures can be used.” Ex. 1001, 10:34-35. The purpose of the “dielectric structure” in the ’378 patent is to electrically insulate a “through array contact” as it extends through the *alternating layer stack*. *Id.*,

11:12-14. One purpose of the “isolation structure” in the ’378 patent is to electrically insulate a “through array contact” as it extends through the “substrate.” The upper and lower portions of Toyama’s “dielectric fill material portion 430,” respectively, fulfill these same purposes.

135. Even if the claim language did require separately forming *the isolation region* and *the dielectric structure* (which it does not), Toyama’s first exemplary structure nevertheless renders the claim element obvious. Using isolation region’s on a substrate to electrically isolate components was well-known and commonplace prior to the effective filing date of the ’378 patent priority date. Indeed, Toyama’s third exemplary structure teaches just that, as I described in connection with element [1.A.ii] for Toyama’s Second Embodiment. As it relates to Toyama’s first exemplary structure, forming the *isolation region* and the *dielectric structure* separately would be no more than the mere substitution of a known process (forming an isolation region in “opening 151” before forming the dielectric structure, as in Toyama’s third exemplary structure) for another process (forming the isolation and dielectric structures at the same time, as in Toyama’s first exemplary structure) to obtain predictable results (the insulating material layer that fills “opening 151” electrically isolates the conductors embedded within).

[1.C.iii] “a dielectric structure ... extending vertically through the alternating layer stack”

136. As I discussed in the previous section, the upper part of Toyama’s “dielectric fill material portion 430” is the claimed *dielectric structure*. And, as I discussed in connection with element [1.B], Toyama’s “alternating stack (132, 146, 232, 246)” is *the alternating layer stack*. Accordingly, as shown in Fig. 15A below, Toyama discloses *a dielectric structure* (upper part of “dielectric fill material portion 430”) *extending vertically through the alternating layer stack* (“alternating stack 132, 146, 232, 246”):

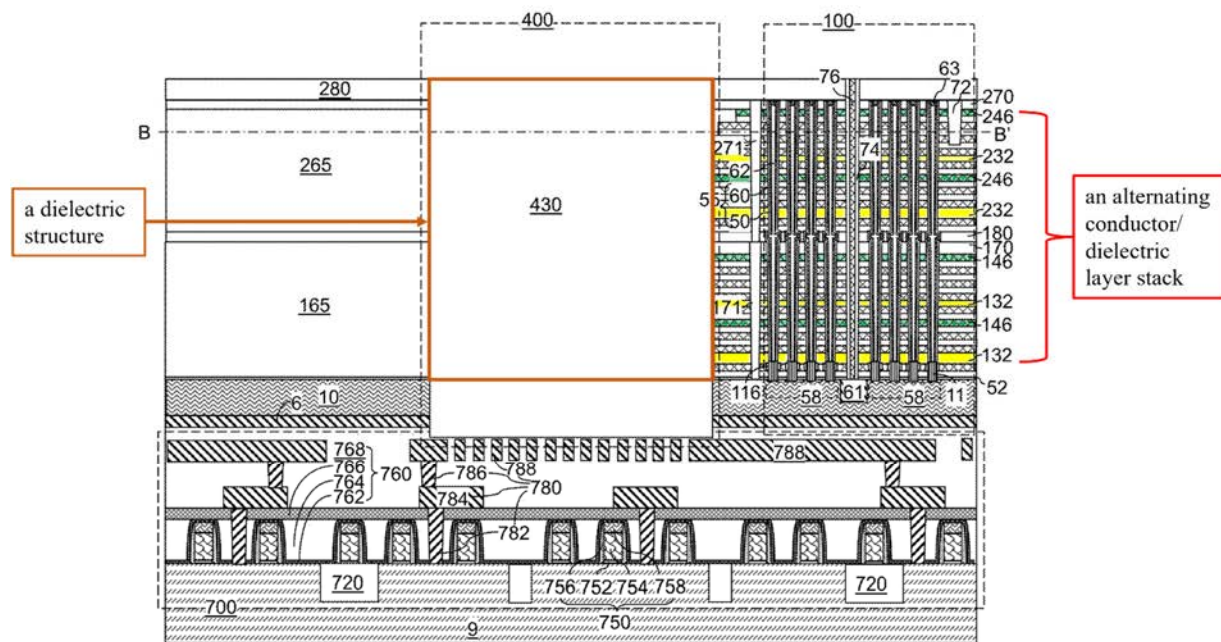


FIG. 15A

Ex. 1005, Fig. 15A (annotated).

137. I note here that Toyama's first exemplary structure satisfies this limitation in substantially the same way as one of the embodiments in the '378

patent. In particular, the '378 specification shows an embodiment where dielectric structure 124 is surrounded on three sides by an alternating layer stack. This can be seen in Fig. 1C below, which is a top view of a 3D NAND device (with memory region 110 on the right and staircase region on the left):

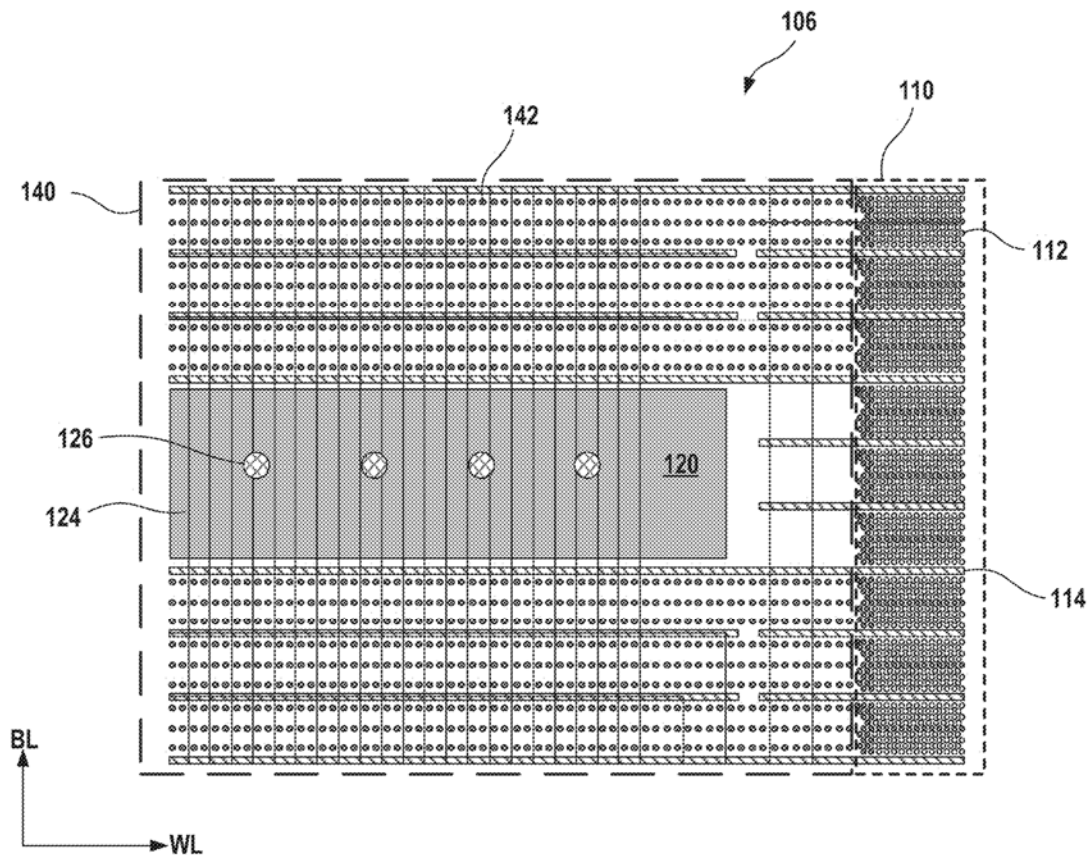
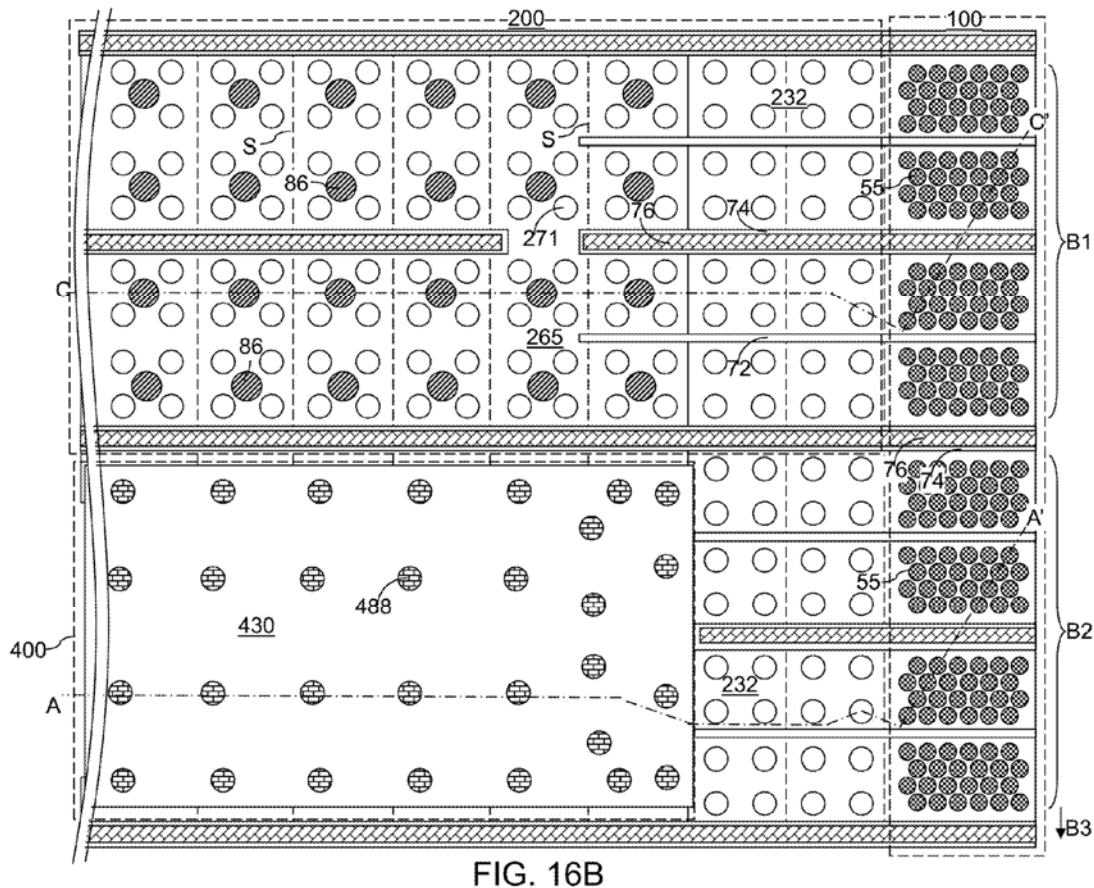


FIG. 1C

Ex. 1001, Fig. 1C.

138. Toyama's first exemplary structure is similar: the *dielectric structure* ("dielectric fill material portion 430") borders three regions including an alternating layer stack. This is shown in Toyama Fig. 16B below, which is a top view of a 3D

NAND device (with “memory array region 100” on the right and staircase regions (“word line contact via region 200”) on the left). Although not illustrated in Fig. 16B, I note that region 200 extends on the bottom of the figure as well.



Ex. 1005, Fig. 16B.

139. Toyama forms its *dielectric structure* (“dielectric fill material portion 430”) in the same way as the ’378 patent forms its dielectric layer 702. The “dielectric fill material portion 430” in Toyama and “dielectric layer 702” in the ’378 specification are both formed by removing part of the dielectric stack before

replacing the sacrificial layers with electrically conductive layers. In particular, the '378 patent removes part of “dielectric stack 400” to form “opening 600”:

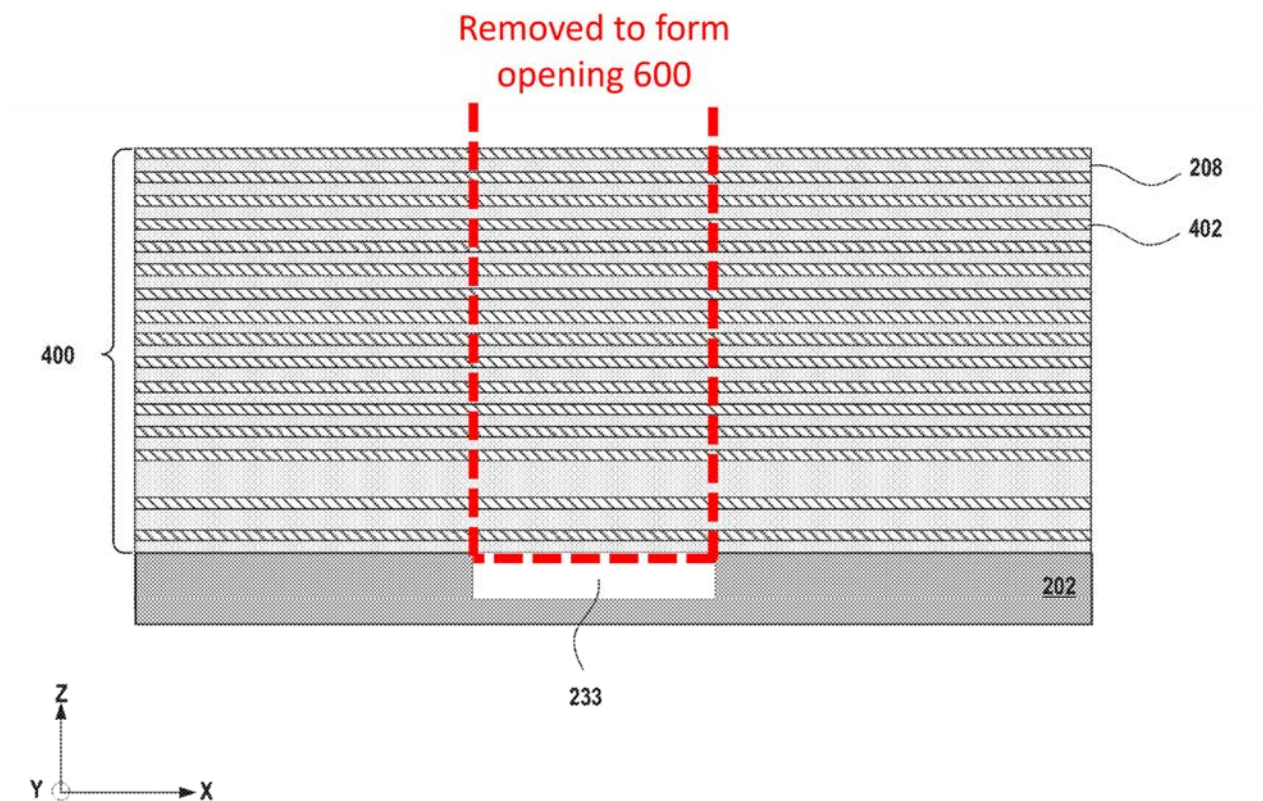


FIG. 4

Ex. 1001, Fig. 4 (annotated); *see also id.*, Fig. 6, 15:12-14. The '378 patent then fills “opening 600” with “dielectric layer 702.” *Id.*, 15:42-44.

140. In like manner, Toyama’s first exemplary structure removes “insulating layers” 132, 232 and “sacrificial material layers” 142, 242 to form “opening 769,” as shown below in Fig. 10A:

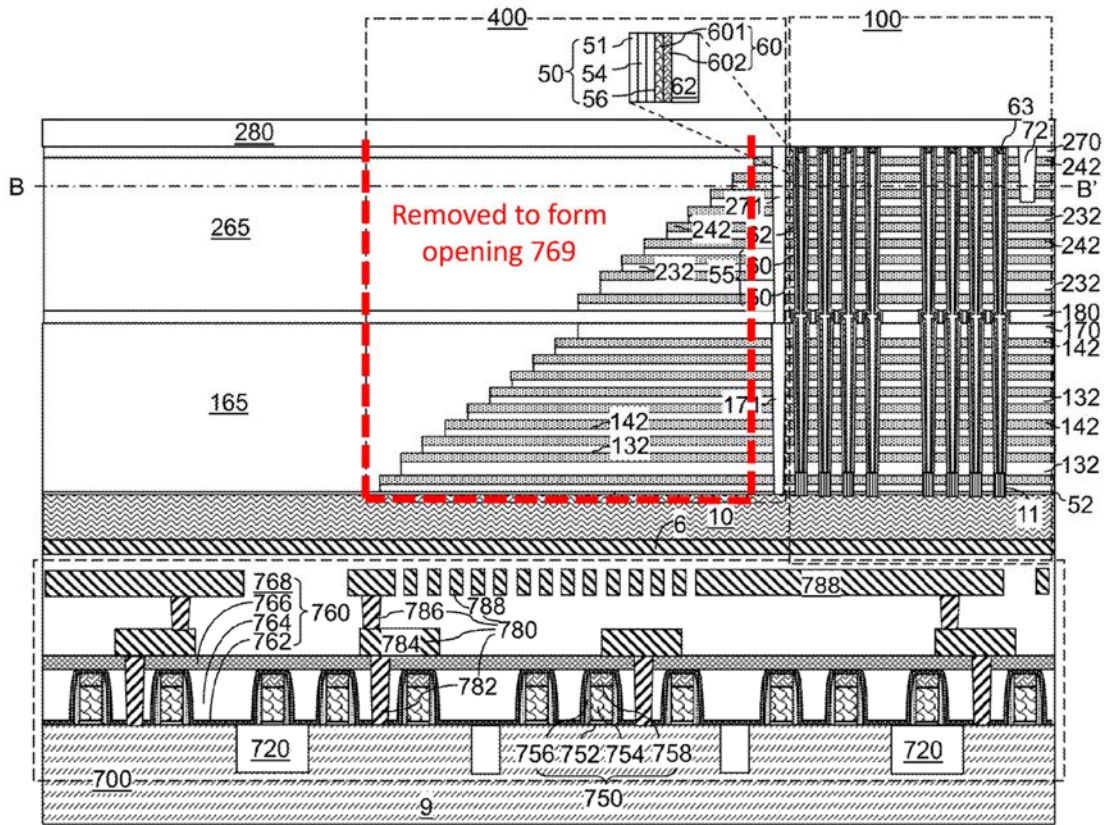


FIG. 10A

Ex. 1005, Fig. 10A (annotated), [0173], [0189]. Toyama then fills “opening 769” with “dielectric fill material portion 430.” Thus, Toyama’s first exemplary structure discloses this limitation.

[1.C.iv] “a dielectric structure ... wherein the alternating layer stack abuts a sidewall surface of the dielectric structure”

141. As highlighted in Fig. 15A below, Toyama discloses *a dielectric structure* (upper part of “dielectric fill material portion 430” in brown) *wherein the alternating layer stack* (“alternating stack (132, 146, 232, 246)” in red) *abuts*

(touches) *a sidewall surface of the dielectric structure* (sidewall (in blue) of upper part of “dielectric fill material portion 430”):

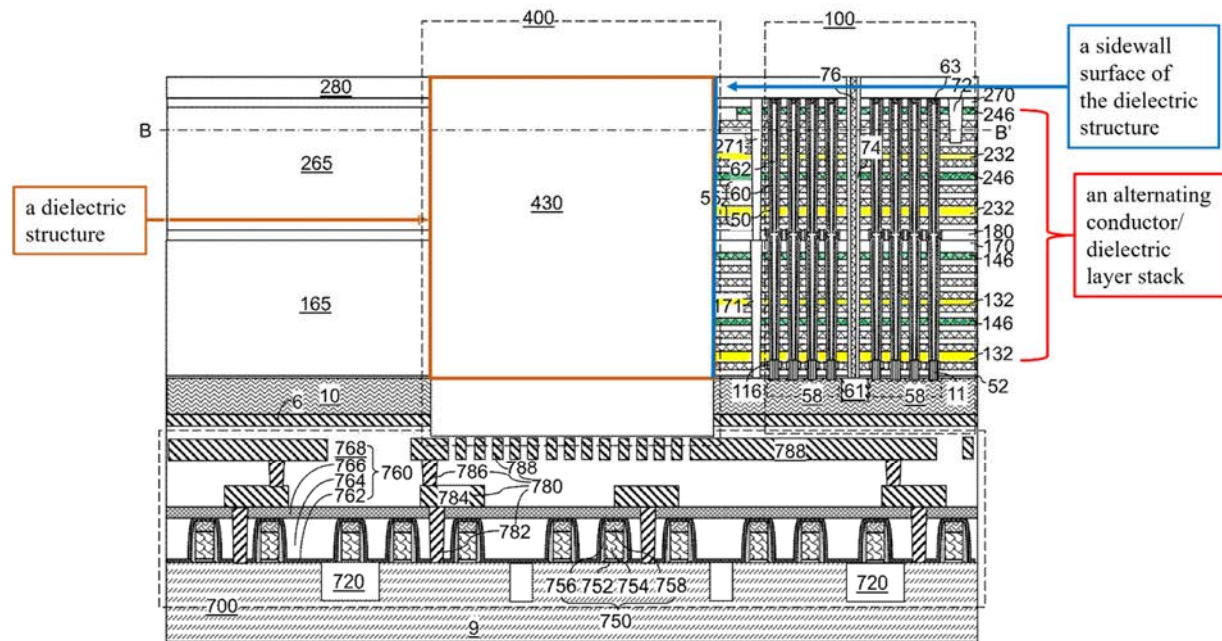


FIG. 15A

Ex. 1005, Fig. 15A (annotated).

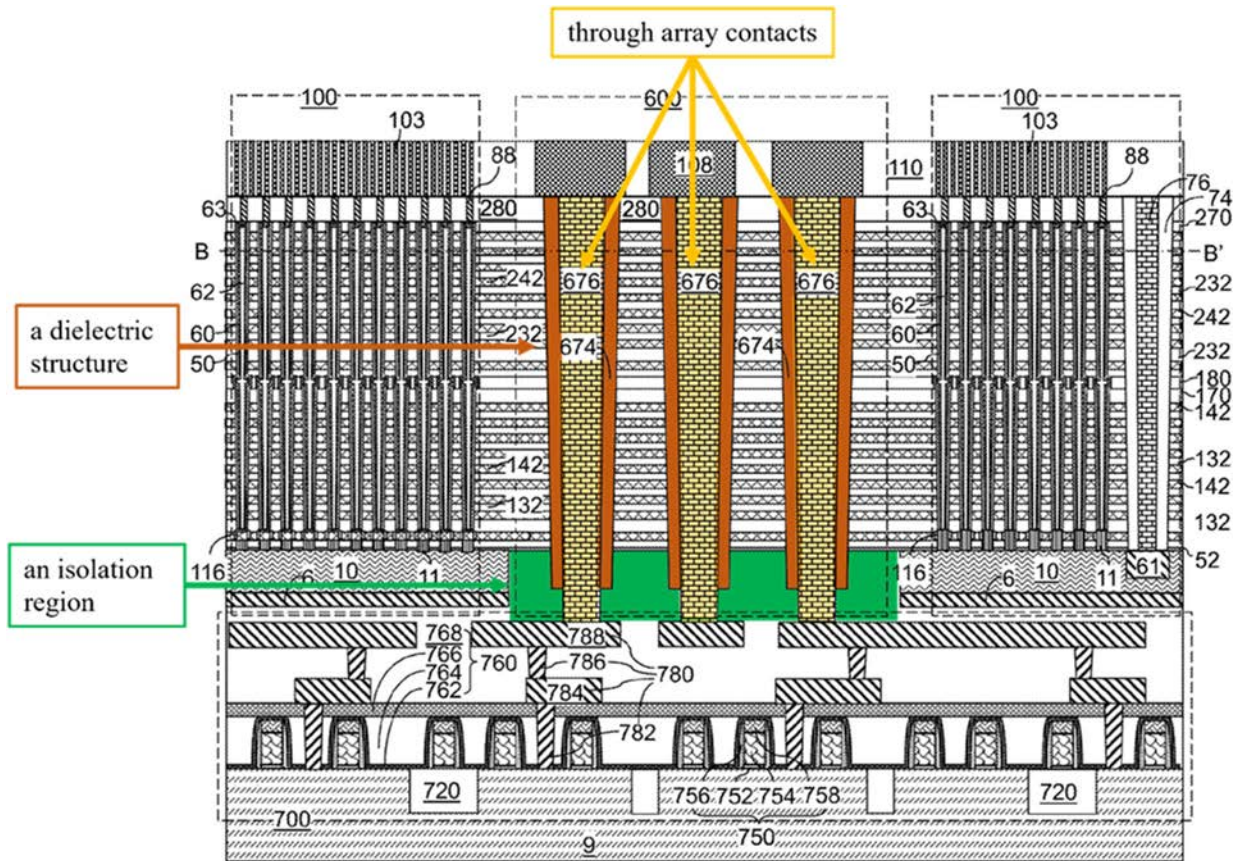
[1.C.v] “... wherein ... the dielectric structure is formed of a dielectric material;”

142. As I discussed previously, the upper portion of Toyama’s “dielectric fill material portion 430” is the claimed *dielectric structure*. And Toyama discloses that “dielectric fill material portion 430 is formed ... for example, by deposition of a dielectric fill material.” Ex. 1005, [0216]. Accordingly, Toyama thus discloses *a dielectric structure* (upper part of “dielectric fill material portion 430”) *wherein the dielectric structure is formed of a dielectric material* (the “dielectric fill material” that forms “dielectric fill material portion 430”).

[1.D] “one or more through array contacts (TACs) extending vertically through the dielectric structure and the isolation region;”

i. Second Modification

143. In Toyama’s Second Modification, the “through-memory-level via structures 676” are the claimed *through array contacts*. And, as can be seen in Fig. 49 below, *they extend[]vertically through the dielectric structure and the isolation region* (respectively shown in red and green below).



Ex. 1005, Fig. 49 (annotated); [0341]-[0342].

144. As discussed for claim element [1.C.i], “insulating liners 674” are individually and collectively *the dielectric structure* in Toyama’s Second Modification. And as discussed for claim element [1.C.ii], the insulating material layer that fills “opening 151” is *the isolation region* in Toyama’s Second Modification.

145. Like water that travels *through* a hose or a pipe that extends *through* a wall, Toyama’s “through-memory-level via structures 676” extend *through* “insulating liners 674,” and the insulating material layer that fills “opening 151.” Thus, Toyama discloses *through array contacts* (“through-memory-level via structures 676”) *extending vertically through the dielectric* (“insulating liners 674”) *and isolation* (the insulating material layer that fills “opening 151”) *structures*. Ex. 1005, [0340]-[0342].

ii. First Exemplary Structure

146. In Toyama’s first exemplary structure, “through-memory-level via structures 488” are the *through array contacts (TACs)*, as shown in Fig. 17A below.

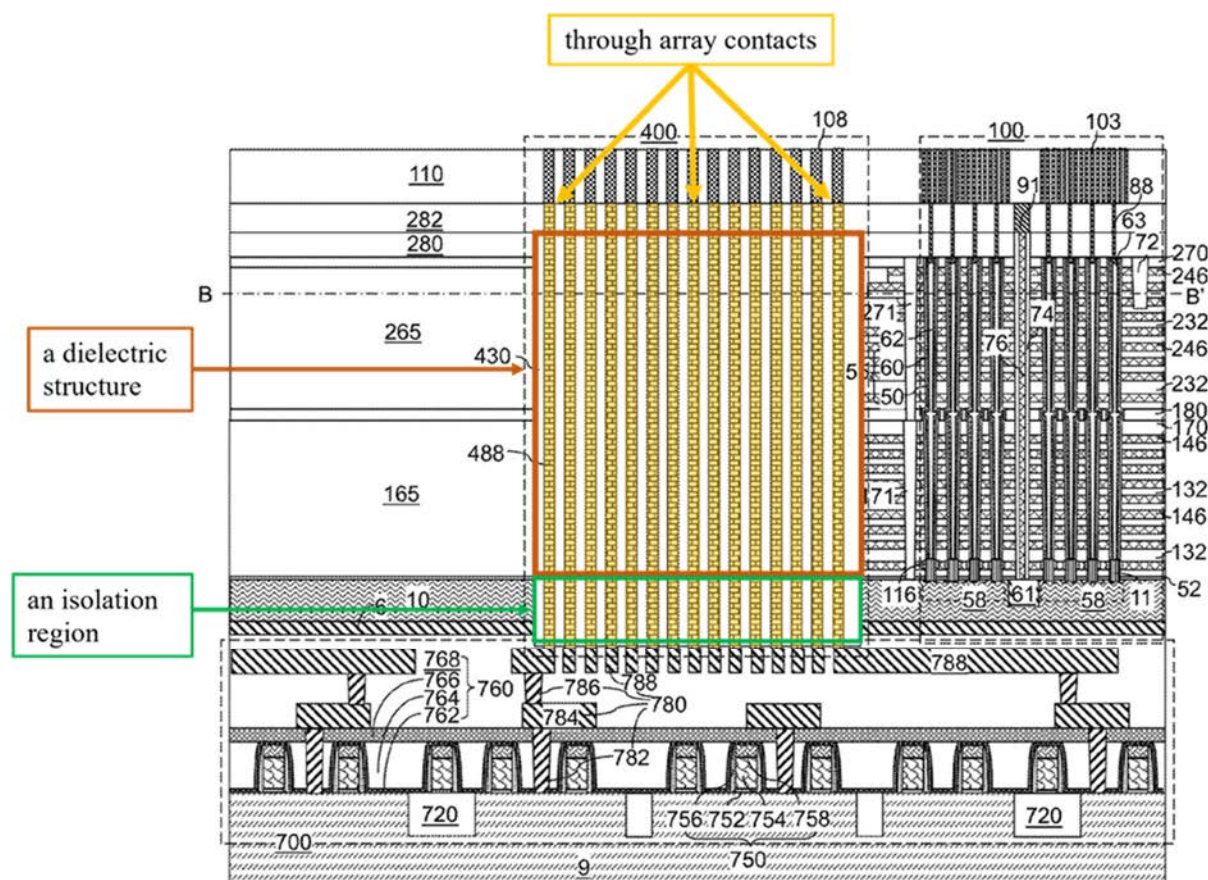


FIG. 17A

Ex. 1005, Fig. 17A (annotated); *id.*, [0239].

147. As I discussed for element [1.C.i], in Toyama’s first exemplary structure the upper part of “dielectric fill material portion 430” is *the dielectric structure*. And as I discussed for element [1.C.ii], the lower part of Toyama’s “dielectric fill material portion 430” is *the isolation region* in Toyama’s first exemplary structure.

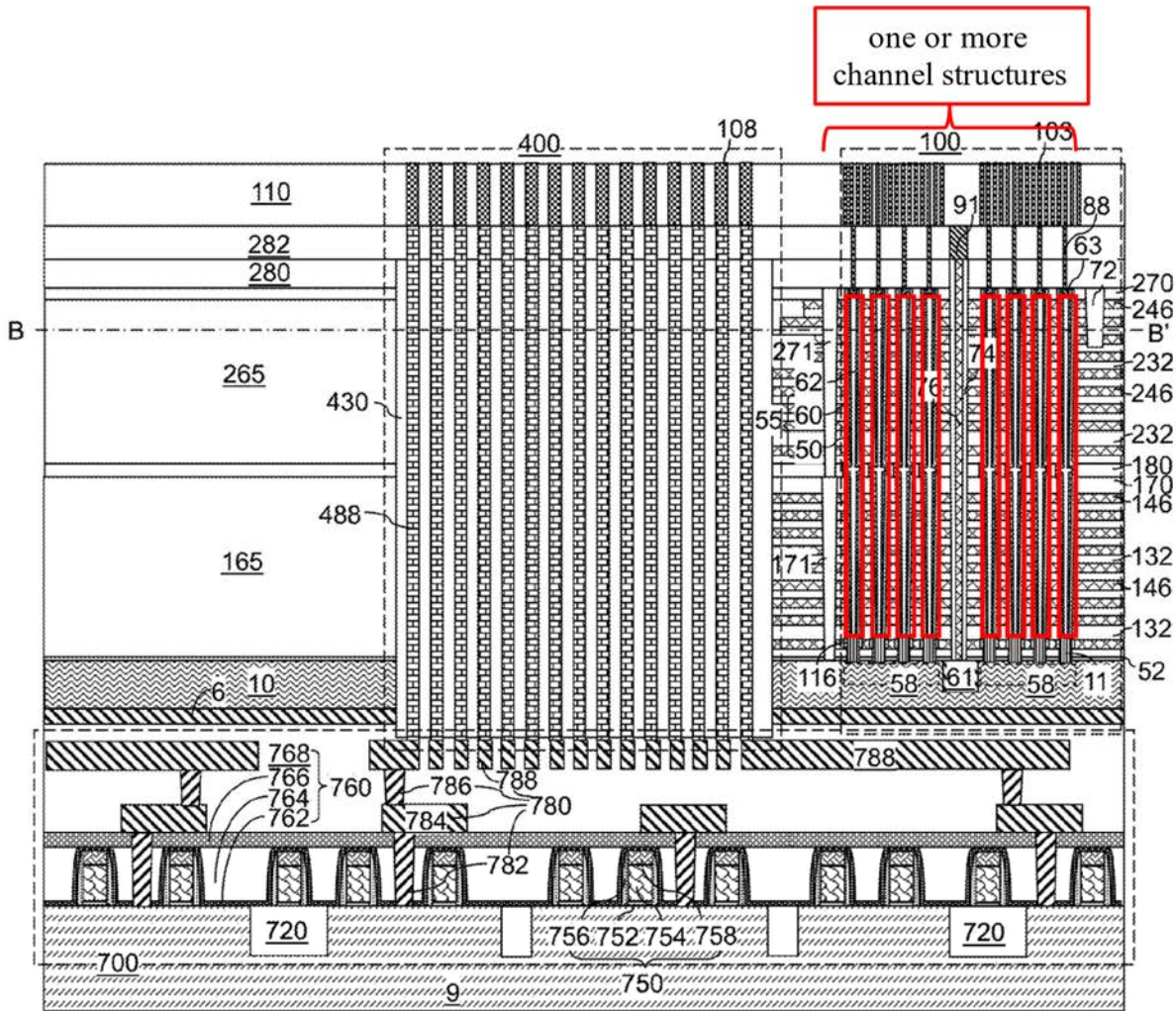
148. Accordingly, Toyama’s first exemplary structure discloses *through array contacts* (“through-memory-level via structures 488”) *extending vertically*

through the dielectric (upper part of “dielectric fill material portion 430”) *and isolation* (lower part of “dielectric fill material portion 430”) *structures*. Ex. 1005, [0239].

[1.E] “one or more channel structures extending vertically through the alternating layer stack;”

i. First Exemplary Structure

149. In Toyama’s first exemplary structure, the “memory stack structures 55” are the claimed *channel structures*, and they *extend[] vertically through the alternating layer stack* (“alternating stack (132, 146, 232, 246)”) as shown in red in Fig. 17A below:



Ex. 1005, Fig. 17A (annotated).³ Toyama describes its “memory stack structures 55 vertically extending through the at least one alternating stack (132, 146, 232, 246).” *Id.*, [0232].

³ Here, as in my declaration filed in IPR2024-00788, I explain that Toyama’s “memory stack structures 55” are the claimed *channel structures*. I note, however,

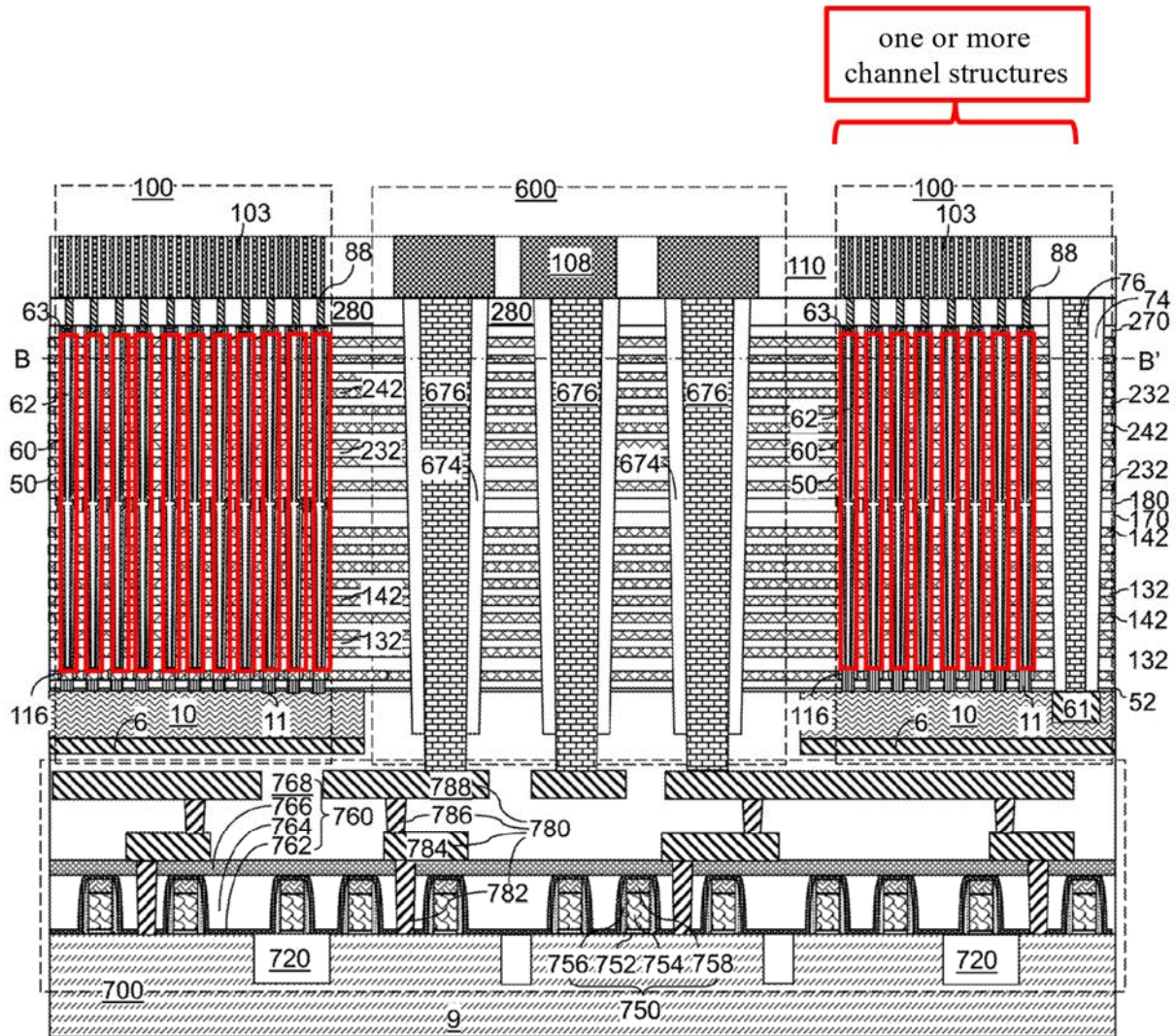
150. Even though the claim element places no other functional or structural requirements on the claimed *channel structures*, I note that Toyama’s “memory stack structures 55” perform the same function and are composed of the same components as the channel structures in the ’378 patent. With respect to function, both serves as memory elements. *Compare* Ex. 1001, 14:4-31 (“channel structure” includes a “memory film”) *with* Ex. 1005, [0388] (“The memory stack structures 55 can comprise memory elements of a vertical NAND device.”). And both are constructed from the same components. *Compare* Ex. 1001, 9:1-6 (“[c]hannel structure 216 is filled with semiconductor materials (e.g., as a semiconductor channel 218) and dielectric materials (e.g., as a memory film 220)”) *with* Ex. 1005,

that the red boxes drawn around the *channel structures* in my earlier declaration were drawn slightly larger than they are here, such that in the prior declaration each box encompassed not just a “memory stack structure 55,” but arguably other structures (e.g., “pedestal channel portion 11,” the *epitaxial layer*, and “drain region 63,” the *etch stop plug*). This overinclusive annotation was of no moment in the prior case because the challenged claims in that case did not recite *an epitaxial layer* or *an etch stop plug*. The boundaries of the box drawn here make clear that the *channel structures* include “memory stack structures 55” but **not** “pedestal channel portions 11” or “drain regions 63.”

[0210] (“[e]ach of the memory stack structures 55 comprises a memory film 50 and a vertical semiconductor channel 60”). This supports my opinion that Toyama’s first exemplary structure discloses *channel structures* (“memory stack structures 55”) *extending vertically through the alternating layer stack* (“alternating stack (132, 146, 232, 246)”).

ii. Second Modification

151. Although the discussion above relates to Toyama’s first exemplary structure, it is equally applicable to Toyama’s Second Modification which meets this limitation for the same reasons. As shown below in Toyama Fig. 49, the *channel structures* (“memory stack structures 55”) *extend[]vertically through the alternating layer stack* (“alternating stack (132, 146, 232, 246)”).



Ex. 1005, Fig. 49 (showing “memory stack structures 55”).

[1.F] “an epitaxial layer between the one or more channel structures and the semiconductor substrate;”

i. First Exemplary Structure

152. As I explained above in limitations [1.E] and [1.A], respectively, Toyama discloses *channel structures* (“memory stack structures 55”) and *a semiconductor substrate* (“planar semiconductor material layer 10”).

153. Toyama further teaches *an epitaxial layer* (“pedestal channel portions 11”) *between the one or more channel structures* (“memory stack structures 55”) *and the semiconductor substrate* (“planar semiconductor material layer 10”), as shown in Fig. 17A below:

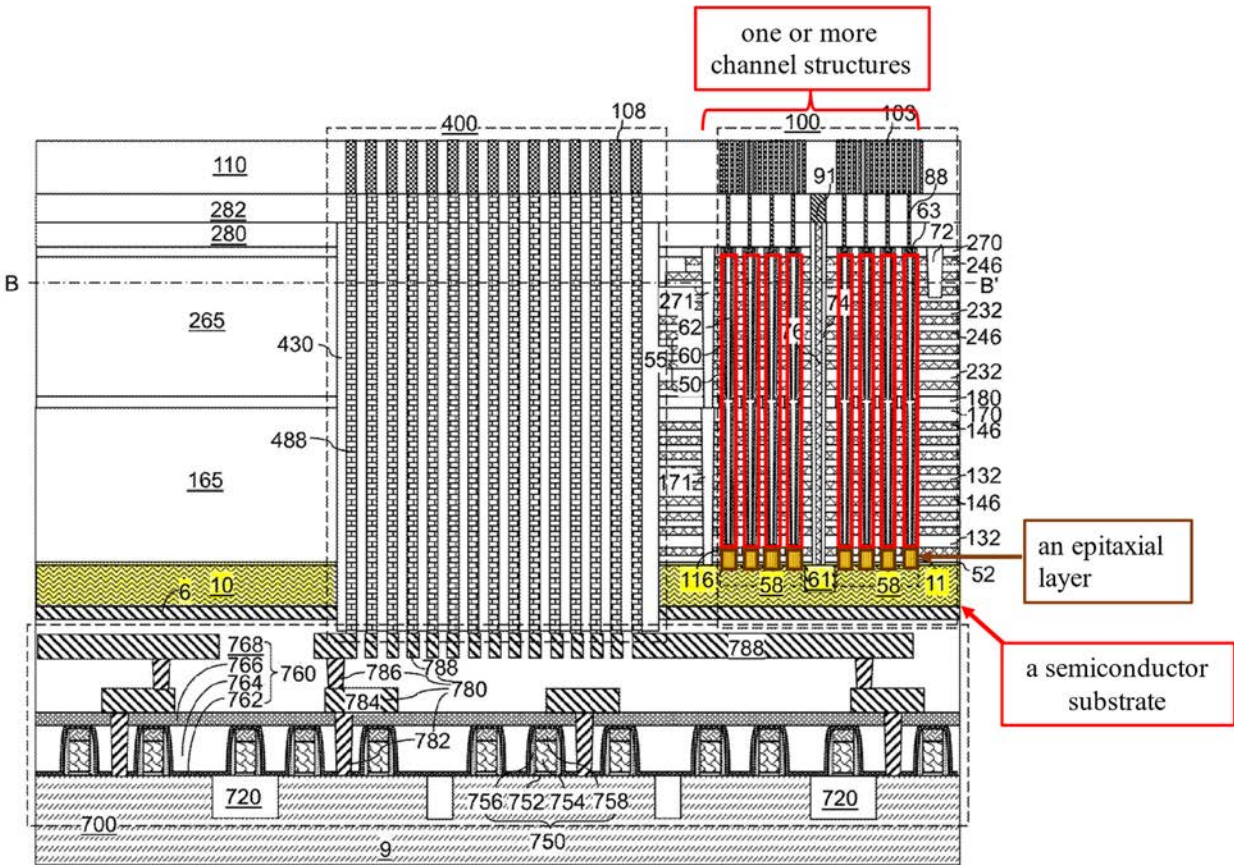


FIG. 17A

Ex. 1005, Figure 17A, [0208].

154. Toyama also refers to “pedestal channel portions 11” as “epitaxial channel portions 11,” which a POSITA would understand to mean that “pedestal channel portions 11” are formed epitaxially. Ex. 1005, [0202], [0208]. Indeed, a POSITA would have found Toyama’s description of how it forms “portions 11” to be consistent with an epitaxial process. *Id.*, [0202] (“The selective semiconductor deposition **grows a semiconductor material**. ... During a selective semiconductor deposition process, a reactant (such as silane, dichlorosilane, trichlorosilane,

disilane, etc.) can be flowed into a deposition chamber simultaneously with, or, alternatively with, an etchant (such as hydrogen chloride).”) (emphasis added).

155. At the very least, a POSITA would have found it obvious to form “pedestal channel portions 11” epitaxially, thus rendering obvious the claimed *epitaxial layer*. As I explained in the background section, above, techniques for epitaxy in 3D NAND flash memories were well-known and within the skill of a POSITA. And a POSITA would have known of the benefits of an epitaxial pedestal including improved performance and reliability characteristics. Thus, implementing “pedestal channel portions 11” using epitaxy would be nothing more than applying a known technique (“epitaxy”) to a known device (Toyama) to yield predictable results (e.g., performance and reliability characteristics).

ii. Second Modification

156. Although the discussion above relates to Toyama’s first exemplary structure, it applies equally to Toyama’s Second Modification and meets this limitation for the same reasons. As shown below in Fig. 49, Toyama discloses *an epitaxial layer* (“pedestal channel portions 11”) *between the one or more channel structures* (“memory stack structures 55”) *and the semiconductor substrate* (“planar semiconductor material layer 10”):

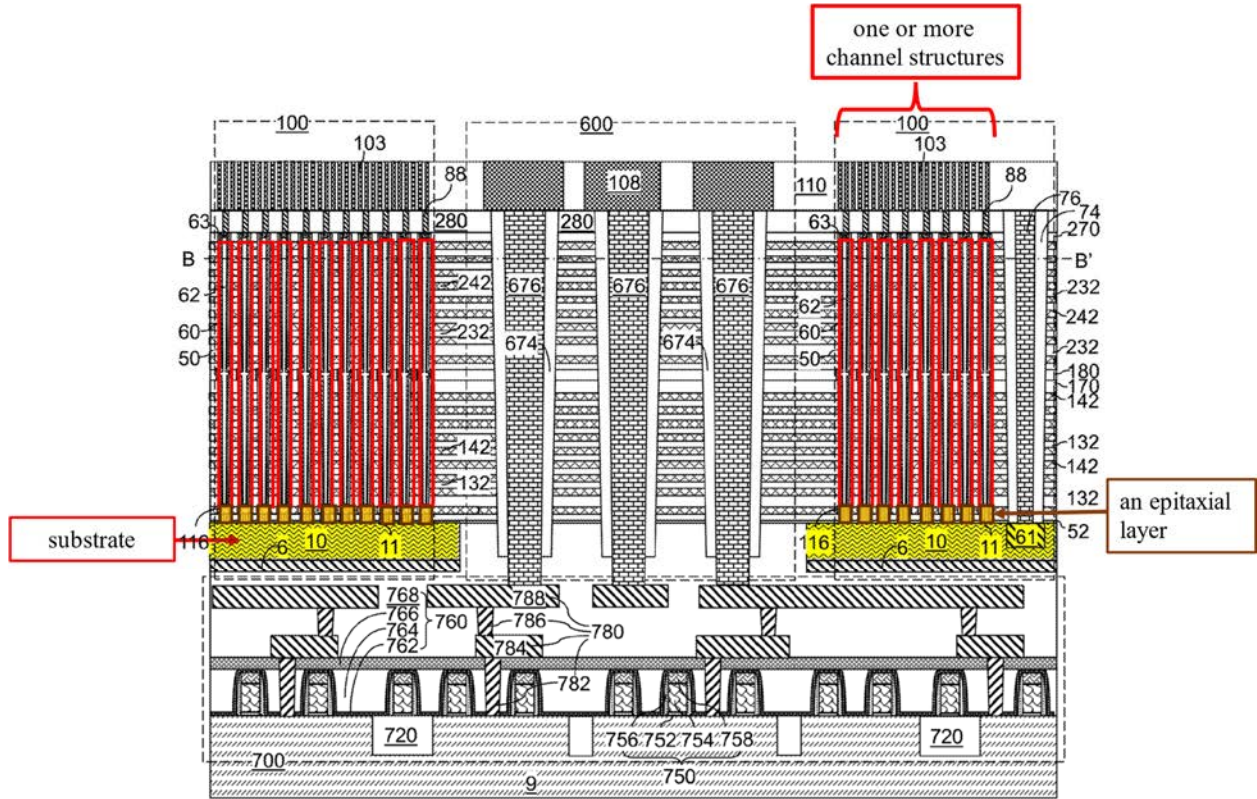


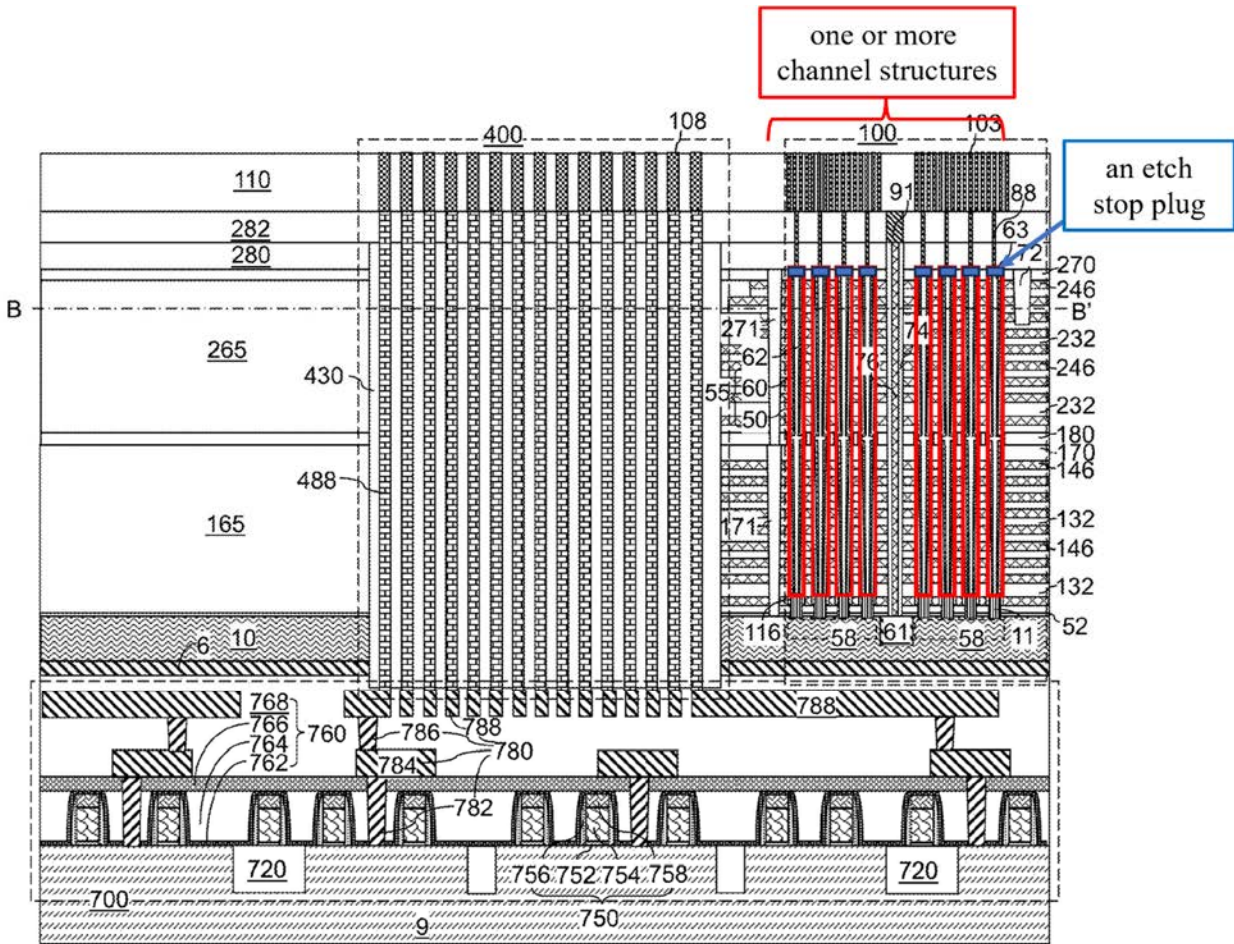
FIG. 49

Ex. 1005, Fig. 49 (annotated).

[1.G] “an etch stop plug on each of the one or more channel structures;”

i. First Exemplary Structure

157. As the below figure illustrates, Toyama teaches (or at least renders obvious) *an etch stop plug* (“drain regions 63”) *on each of the one or more channel structures* (“memory stack structures 55”):



Ex. 1005, Fig. 17A; Ex. 1001, 4:20-25 (defining “on”).

158. Toyama does not expressly describe “drain regions 63” as “etch stop plugs.” Even so, a POSITA would have understood that drain regions 63 are plugs that serve the purpose of stopping an etch and are therefore *etch stop plugs*.

159. To start, the meaning of the term *plug* in the field of flash memory is consistent with its ordinary meaning, which Merriam-Webster’s dictionary defines as “a piece used to fill a hole.” Ex. 1022, 3. In describing “drain regions 63,”

Toyama explains that “[a] doped semiconductor material ... can be deposited over the dielectric cores 62 and within *the cavities in the memory openings* to form drain regions 63. The doped semiconductor material can be, for example, doped polysilicon. Excess portions of the deposited semiconductor material can be removed from above the top of the second insulating tier cap layer 270 ... to form the drain regions 63.” Ex. 1005, [0209]. Toyama’s “drain regions 63” are thus plugs because they fill the “cavities in the memory openings.” *Id.*

160. For the reasons I explain below, a POSITA would have appreciated that Toyama’s “drain regions 63” are etch stops because they have an *etch stop* function.

161. As Figure 17A shows below, Toyama forms contacts (“drain contact via structures 88”) in the *contact layers on the one or more channel structures* (“memory stack structures 55”) by etching through dielectric layers 280 and 282, and then filling the etched opening with a conductor:

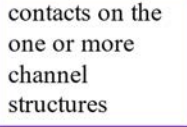


FIG. 17A

Ex. 1005, Fig. 17A. “Drain contact via structures 88 contacting the drain regions 63 can extend through the contact level dielectric layers (280, 282).” *Id.*, [0241]. Toyama further explains that “drain contact via structures 88” “may be formed employing a respective set of patterning processes and fill processes.” *Id.*, [0241]-[0242].

162. As explained in the background section, above, the process of “patterning” generally involves forming a photoresist layer to protect certain material from etching, etching the exposed material, and then removing the photoresist.

163. A POSITA would thus have understood from Toyama's disclosure that part of the "patterning" process includes a step of etching an opening in dielectric layers 280 and 282. Ex. 1005, [0241]. And a POSITA would have understood from Toyama's disclosure (or at least would have found it obvious) that the dielectric layers 280, 282 would be formed of a dielectric material such as silicon oxide.⁴

⁴ Toyama states that "second contact level dielectric layer 282 includes a dielectric material such as silicon oxide." Ex. 1005, [0238]. Toyama does not expressly state that "dielectric layer 280" is made of silicon oxide, but a POSITA would have understood Toyama to contemplate doing so. At the very least, forming layer 280 of silicon oxide would have been obvious to a POSITA. Toyama expressly notes that "dielectric layer 180" could be made of "a dielectric material such as silicon oxide." *Id.*, [0183]. A POSITA would have understood from Toyama's disclosure that "dielectric layer 280" would similarly be made of silicon oxide, which was a well-known dielectric material with recognized advantages such as being formed easily and using well-practice to techniques. And a POSITA would have found it desirable to form "dielectric layer 280" out of silicon oxide where layer 282 is formed out of silicon dioxide because that would allow a silicon-oxide-selective etchant to etch through both layers.

Whether or not dielectric layers 280, 282 are formed of silicon oxide, however, Toyama contemplates (and a POSITA would certainly have found it obvious, given Toyama's express disclosure of patterning) that a dielectric-selective etchant would be used to form the opening that is ultimately filled by "drain contact via structures 88." As the textbooks and other materials I cite in the background section indicate, such selective etches were well-known and routine to implement.

164. With that context (which a POSITA would have known) in mind, the reason that the "drain regions 63" serve as *an etch stop* is evident. Namely, without "drain regions 63," the etch to form "drain contact via structures 88" may risk damaging elements of "memory stack structures 55." That is because "memory stack structures 55" may include dielectric elements (e.g., "blocking dielectric layer 51") that are formed of the same materials (e.g., silicon oxide) as layers 280 and 282. Ex. 1005, [0204]. Thus, if the etchant that is used to etch through the dielectric layers 280 and 282 were to contact the memory stack structures, the etchant may damage the dielectric elements in the memory stack structures.

165. "Drain regions 63," which are between the opening that is filled to form "drain contact via structures 88" and the "memory stack structures 55," thus protect "memory stack structures 55" from damage. "Drain regions 63" function as an etch stop because they are made of a material like doped polysilicon, which a POSITA would have understood would **not** react significantly with the etchant used to

selectively etch the dielectric layers 280 and 282. Carbon tetrafluoride (with hydrogen) is one such etchant that etches silicon oxide but does not appreciably etch polysilicon. Ex. 1023 (Chang, ULSI Technology), 363-364. Even if the etchant were to remove a portion of “drain regions 63,” the thickness of “regions 63” acts as a buffer, so that the etchant might partially etch and stop before etching through to the memory elements. Thus, “drain regions 63” serve to protect the dielectric materials in the memory stack from the etching process used to form “drain contact via structures 88.” In other words, because “drain regions 63” effectively stop the etch that ultimately forms the holes for “drain contact via structures 88,” each of “drain regions 63” is *an etch stop plug* that beneficially protects the channel structure.

ii. Second Modification

166. Although the discussion above relates to Toyama’s first exemplary structure, it applies equally to Toyama’s Second Modification and meets this limitation for the same reasons. As shown below in Fig. 49, Toyama discloses *an etch stop plug* (“drain region 63”) *on each of the one or more channel structures* (“memory stack structures 55”):

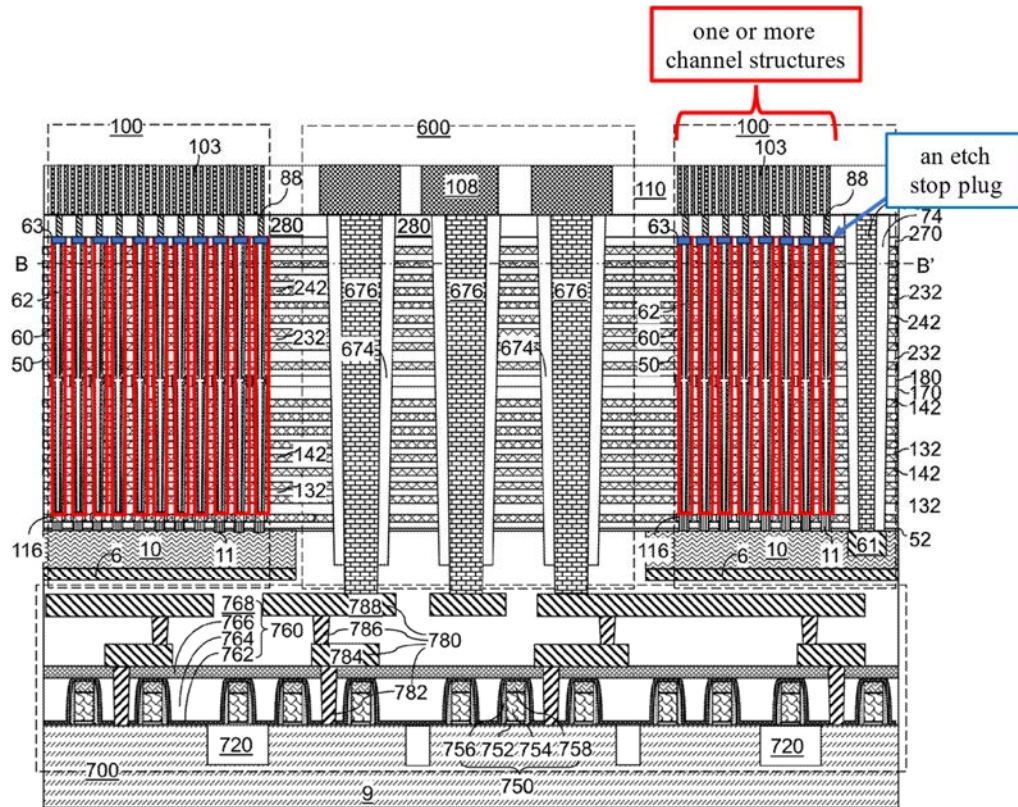


FIG. 49

Ex. 1005, Fig. 49 (annotated).

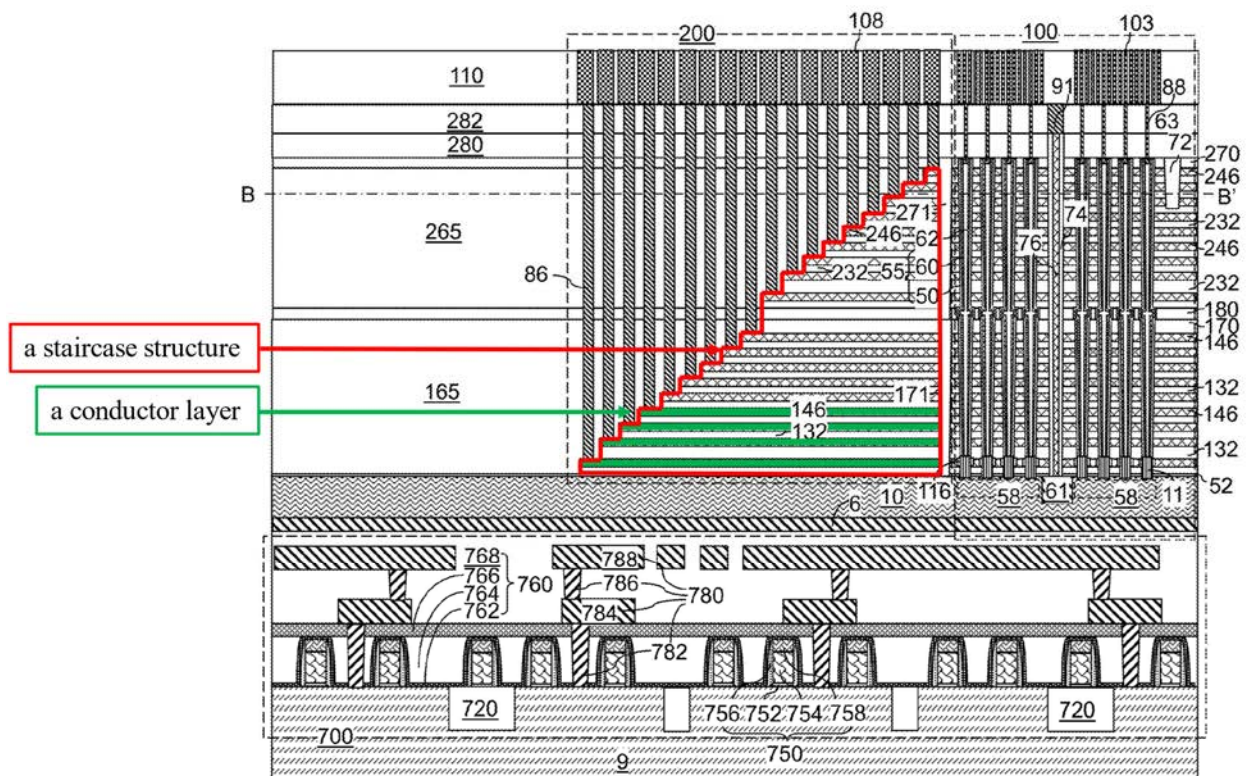
[1.H] “a staircase structure in the alternating layer;”

167. As I explained above in my discussion of claim construction, a POSITA would have understood this limitation to mean “a staircase structure in the alternating layer *stack*.” Both Toyama’s first exemplary structure and its Second Modification disclose or render obvious this limitation.

i. First Exemplary Structure

168. The “staircase region” highlighted in Toyama Fig. 17C below is *a staircase structure* that is *disposed in the alternating layer stack* (“alternating stack (132, 146, 232, 246)”). Moreover, *the staircase structure* (“staircase region”)

comprises levels with each level having a conductor layer (“electrically conductive layers 146, 246”) *thereon*:



Ex. 1005, Fig. 17C (annotated). Toyama explains that “[t]he at least one alternating stack (132, 146, 232, 246) comprises staircase regions that include terraces in which each underlying electrically conductive layer (146, 246) extends farther along the first horizontal direction hd1 than any overlying electrically conductive layer (146, 246).” *Id.*, [0232].

ii. Second Modification

169. While the discussion above was in the context of Toyama's first exemplary structure, a POSITA would have understood that Toyama's Second Modification also teaches this limitation for substantially the same reasons. With respect to Toyama's fourth exemplary structure (to which the Second Modification pertains), Toyama notes that "word line contact via structures [86] can be formed as in the first through third embodiments." Ex. 1005, [0322]. Recall that the word line contacts are in Toyama's staircase region. *See id.*, Fig. 17C, [0243]. Thus, although not explicitly depicted in Figs. 44-49, a POSITA would therefore have understood that Toyama's fourth exemplary structure (and modifications thereof including the Second Modification) includes *a staircase structure* ("staircase regions").

170. At a minimum, it would have been obvious to a POSITA to use *a staircase structure* ("staircase regions") in Toyama's Second Modification. For the memory device to be functional, a POSITA would have understood that there needed to be some way to transmit signals to the "electrically conductive layers (146, 246)," because these layers serve as the word lines for accessing (*e.g.*, reading, writing, and erasing) the memory elements in the channel structures. Ex. 1005, [0323]. And it would have been obvious to a POSITA to use the well-known *staircase structure* ("staircase regions") architecture to provide access to Toyama's word lines. Not only is this true in view of the knowledge of a POSITA, but also in view of the

teachings in Toyama itself regarding its first, second, and third exemplary structures, from which the Second Modification derives. *See, e.g., id.*, Fig. 17C.

[1.I] “slit structures extending vertically in the alternating layer stack; and”

i. First Exemplary Structure

171. The claimed *slit structures* in Toyama’s first exemplary structure are the “laterally-elongated contact via structures 76,” and they *extend[] vertically through the alternating layer stack* (“alternating stack (132, 146, 232, 246)”) as shown in Fig. 17A below:

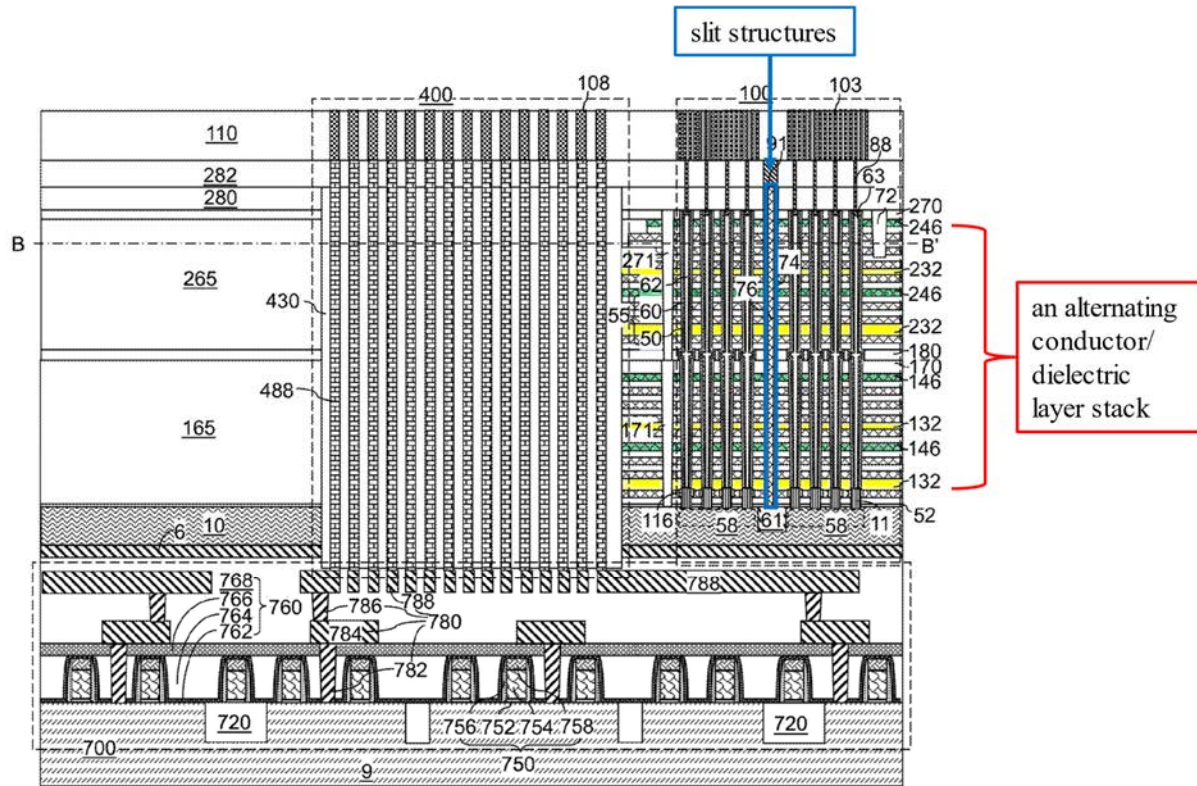
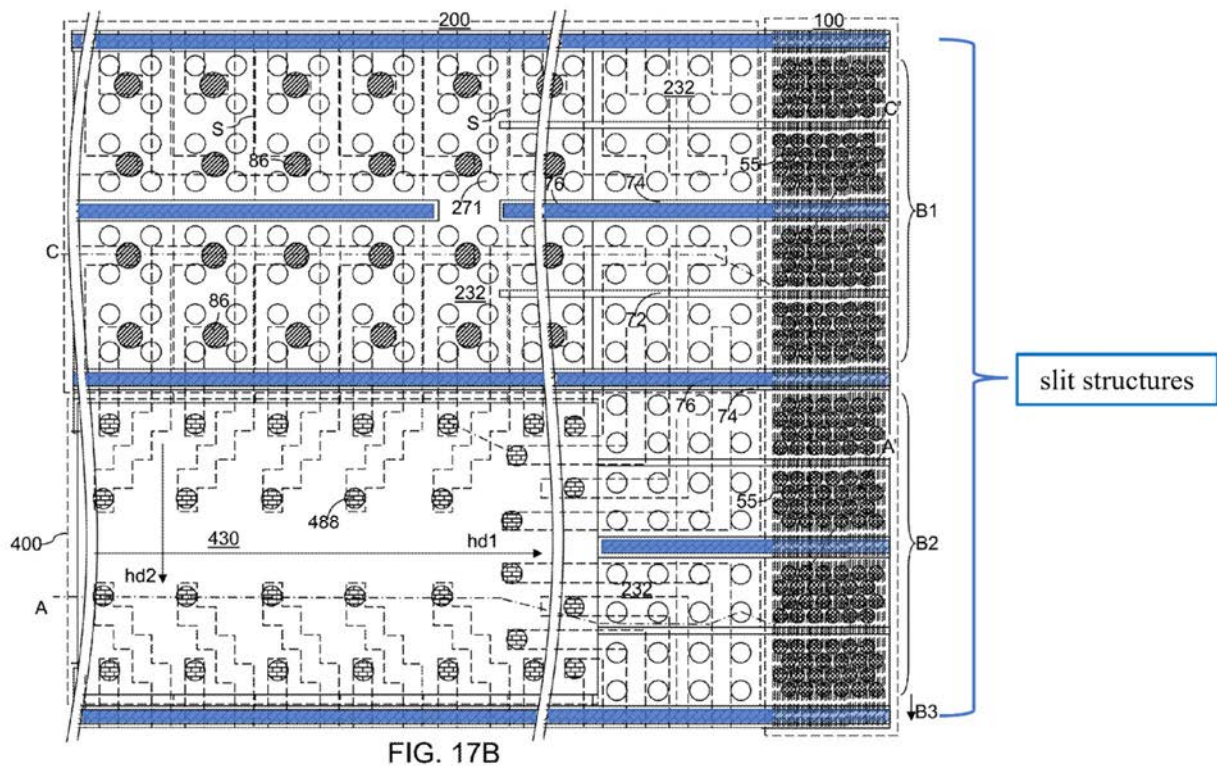


FIG. 17A

Ex. 1005, Fig. 17A (annotated). The lateral elongated shape of the “laterally-elongated contact via structures 76” *slit structures* is most easily observed in the top view of Fig. 17B:



Id., Fig. 17B (annotated). It is of no import that Toyama refers to the claimed *slit structures* as “laterally-elongated contact via structures 76.” Indeed, the plain meaning of “slit” is a laterally-elongated structure. See Ex. 1022, 4 (Merriam-Webster’s definition of “slit” as “a long narrow cut or opening”).

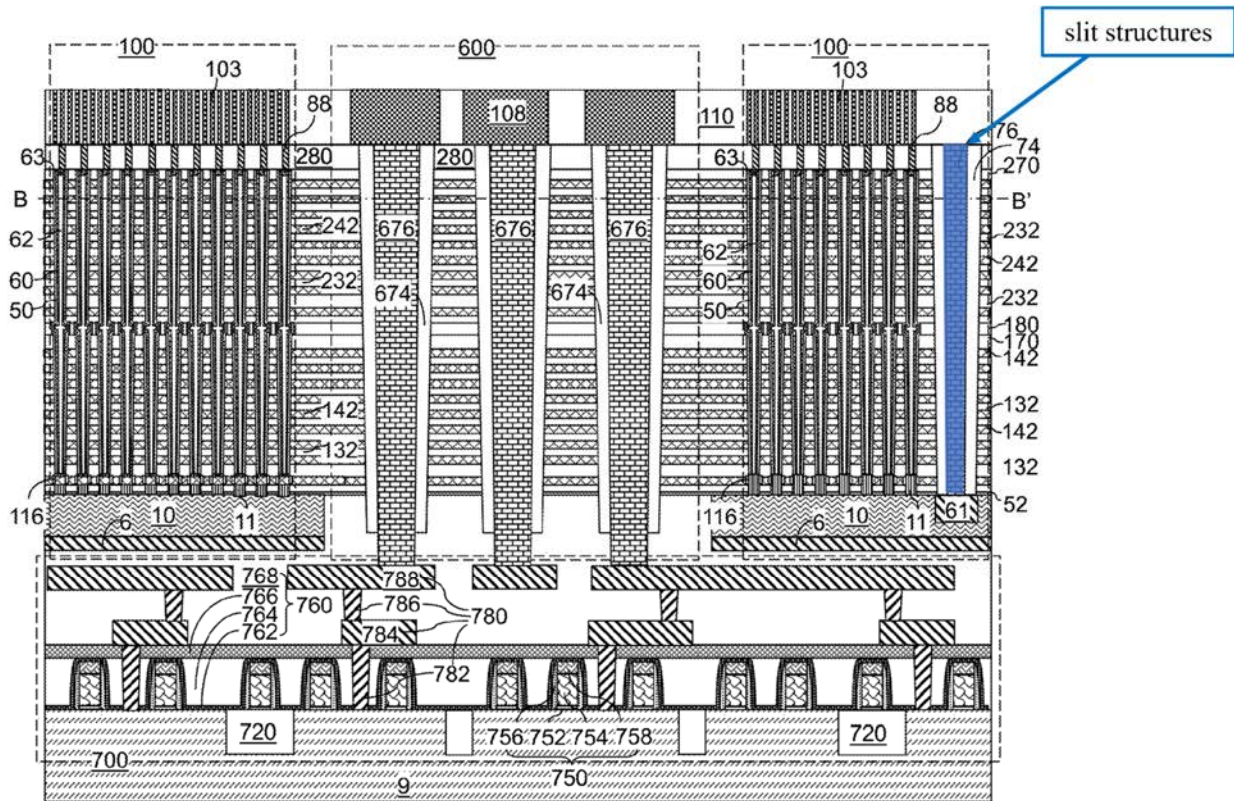
172. And, as can be seen in Toyama Fig. 17A above, Toyama “laterally-elongated contact via structure 76” *extend[s] vertically in the alternating layer stack* (“alternating stack (132, 146, 232, 246)”), as required by the claim.

173. Even though the claim places no functional limitation on the “slit structure,” Toyama’s “laterally-elongated contact via structures 76” perform the same function as the ’378 patent’s “slit structures.” The ’378 specification explains

that each “slit structure 226 acts as a source contact for NAND strings 204.” Ex. 1001, 9:63-67. Likewise, Toyama’s “laterally-elongated contact via structures 76” serves as “source connection[s].” Ex. 1005, [0241]. And the *slit structures* in Toyama and the ’378 patent both define memory “blocks” in their respective 3D memory arrays. *Compare* Ex. 1001, 9:52-54 (“[s]lit structures 226 ... extend along the y-axis to separate alternating conductor/dielectric stack 210 into multiple blocks.”) *with* Ex. 1005, [0237] (“laterally-elongated contact via structures 76 laterally extend along the first horizontal direction ... and laterally divide the at least one alternating stack ... into a plurality of laterally spaced-apart blocks.”). This reinforces my opinion that Toyama’s first exemplary embodiment meets the claim language.

ii. Second Modification

174. Although the discussion above relates to Toyama’s first exemplary structure, it applies equally to Toyama’s Second Modification and meets this limitation for the same reasons. As shown below in Fig. 49, Toyama’s “laterally-elongated contact via structures 76” are the claimed *slit structures* and they *extend[] vertically through the alternating layer stack* (“alternating stack (132, 146, 232, 246)”).



Ex. 1005, Fig. 49 (annotated) (showing “laterally-elongated contact via structures 76”). In this regard, it is important not to mistake the structure 676 (in the middle of the figure) for the “laterally-elongated contact via structures 76” (on the right hand side of the figure).

[1.J] “one or more contact layers on the one or more TACs, the one or more channel structures, and the slit structures.”

175. Toyama’s first exemplary structure and its Second Modification each disclose this element.

176. Before turning to my analysis, I first note that the ’378 patent teaches that “the 3D memory device 200 can further include a contact layer 242.” Ex. 1001,

11:48-49. “Contact layer 242 can include a dielectric layer and a plurality of contacts 246 (e.g., vias) in the dielectric layer.” *Id.*, 11:51-53. A POSITA would understand from the ’378 patent’s description of “contact layer 242” that the claimed *contact layer* may include both a dielectric layer and contacts in the dielectric layer.

i. First Exemplary Structure

177. As I have already explained in discussing claim 1, Toyama’s first exemplary structure discloses *TACs* (“through-memory-level via structures 488”), *one or more channel structures* (“memory stack structures 55”), and *slit structures* (“laterally elongated contact via structures 76”).

178. The first exemplary structure further discloses the claimed *contact layers* on these structures. Specifically, Toyama discloses *a contact layer* (including “line level dielectric layer 110” and “upper-level metal interconnect structures 108”) *on* (in contact with or extending above) *the one or more TACs* (“through-memory-level via structures 488”). Toyama discloses *a contact layer* (including “contact level dielectric layers (280, 282)” and “drain contact via structures 88”) *on the one or more channel structures* (“memory stack structures 55”). And Toyama discloses *a contact layer* (including “second contact level dielectric layer 282” and “source connection via structures 91”) *on the slit structures* (“laterally-elongated contact via structures 76”). The claimed structures can be seen in Fig. 17A, below:

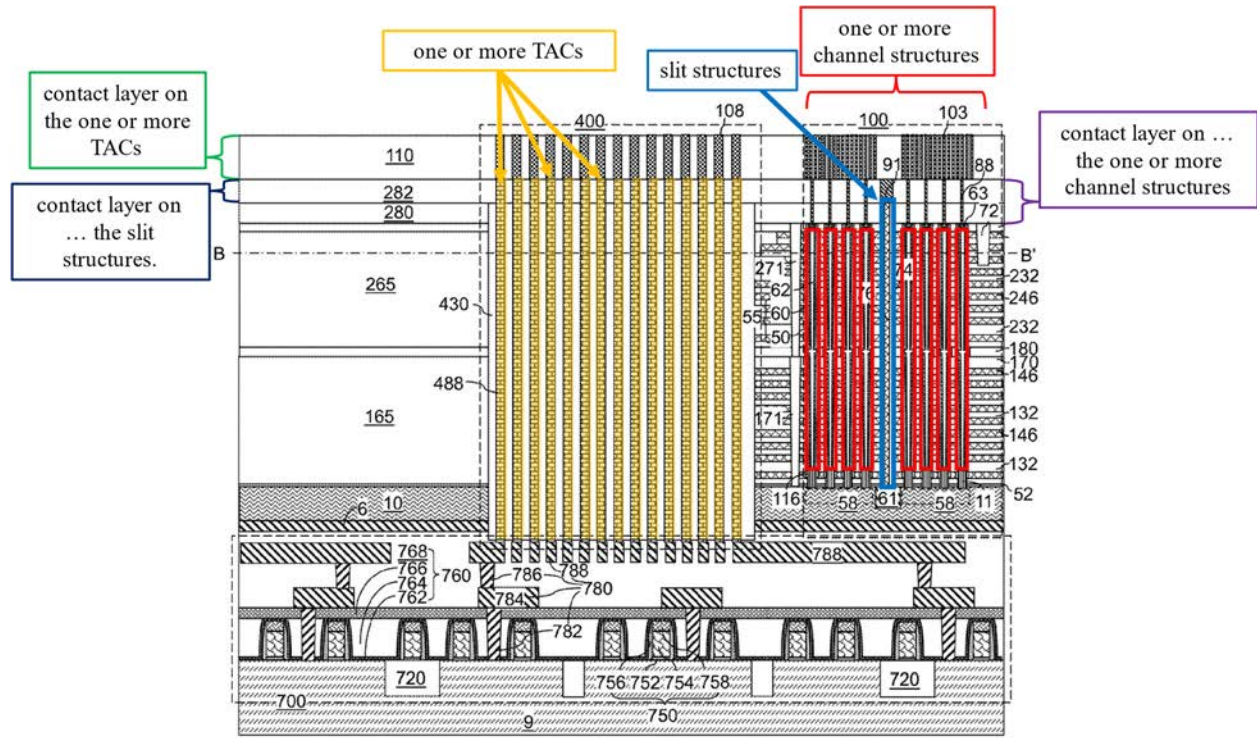


FIG. 17A

Ex. 1005, Fig. 17A (annotated); *id.*, [0251] (“The bit lines 103 are formed over the memory-level assembly, and are electrically coupled to nodes (e.g., drain regions 63) of the memory stack structures 55 by the drain contact via structures 88.”); *id.*, [0241] (“A source connection via structure 91 can extend through the contact level dielectric layers (280, 282) to provide electrical connection to the laterally-elongated contact via structures 76.”); *id.*, [0250] (“Various metal interconnect structures (108, 103, 101) can be formed in the line level dielectric layer 110. ... [U]pper-level metal interconnect structures 108 ... are electrically coupled to ... through-memory-level via structure[s] 488”).

ii. Second Modification

179. Although the discussion above was in the context of Toyama's first exemplary structure, Toyama's Second Modification also teaches (or, at the very least renders obvious) this limitation for substantially the same reasons.

180. As I have already explained in discussing claim 1, Toyama's Second Modification discloses *TACs* ("through-memory-level via structures 676"), *one or more channel structures* ("memory stack structures 55"), and *slit structures* ("laterally elongated contact via structures 76"). The second modification further discloses the claimed *contact layers* on these structures.

181. Specifically, Toyama discloses *a contact layer* (including "line level dielectric layer 110" and "upper-level metal interconnect structures 108") *on the one or more TACs* ("through-memory-level via structures 676").

182. Toyama further discloses *a contact layer* (including "first contact level dielectric layer 280" and "drain contact via structures 88") *on the one or more channel structures* ("memory stack structures 55"). And Toyama discloses *a contact layer* ("second contact level dielectric layer 282" and "source connection via structures 91") *on the slit structures* ("laterally-elongated contact via structures 76").

The claimed structures can be seen in Fig. 49, below:

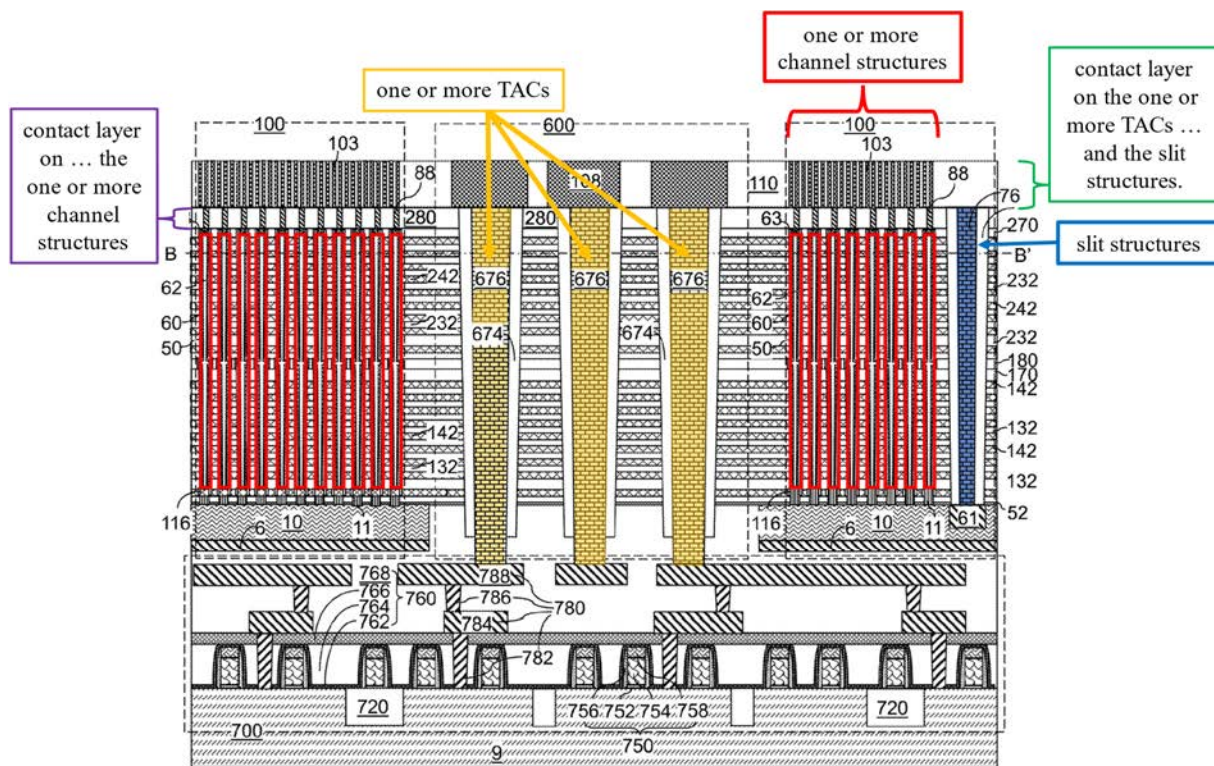


FIG. 49

Ex. 1005, Fig. 49, [0342].

183. Indeed, these contact layers are *on* the recited structures under '378 patent's definition, which is that "on" "should be interpreted in the broadest manner such that 'on' not only means 'directly on' something but also includes the meaning of 'on' something with an intermediate feature or a layer therebetween." Ex. 1001, 4:20-25.

184. A POSITA would not understand limitation [1.J] to require a contact on *the slit structures*, only a contact layer on the slit structures. Regardless, for the reasons I discuss for limitation [15.G], a POSITA would have understood—and at the very least found obvious—that local contacts (e.g., “source connection via

structures 91”) would be disposed on Toyama’s *slit structures* (“laterally elongated contact via structures 76”) in a contact layer (e.g., “line level dielectric layer 110”). Indeed, as I explain for limitation [15.G], for “via structures 76” to serve their purpose they would connect to a higher-level source connection and an obvious technique for achieving this would be to use “source connection via structures 91” in “line level dielectric layer 110.”

2. Claim 2

[2] “The 3D memory device of claim 1, wherein the dielectric structure abuts a sidewall surface of the TACs.”

185. Toyama’s Second Modification and Toyama’s first exemplary structure both teach this limitation.

i. Second Modification

186. As shown in Toyama Fig. 49 below, *the dielectric structure* (“insulating liners 674”) in Toyama’s Second Modification *abuts a sidewall surface of the TACs* (a sidewall of the “through-memory-level via structures 676”):

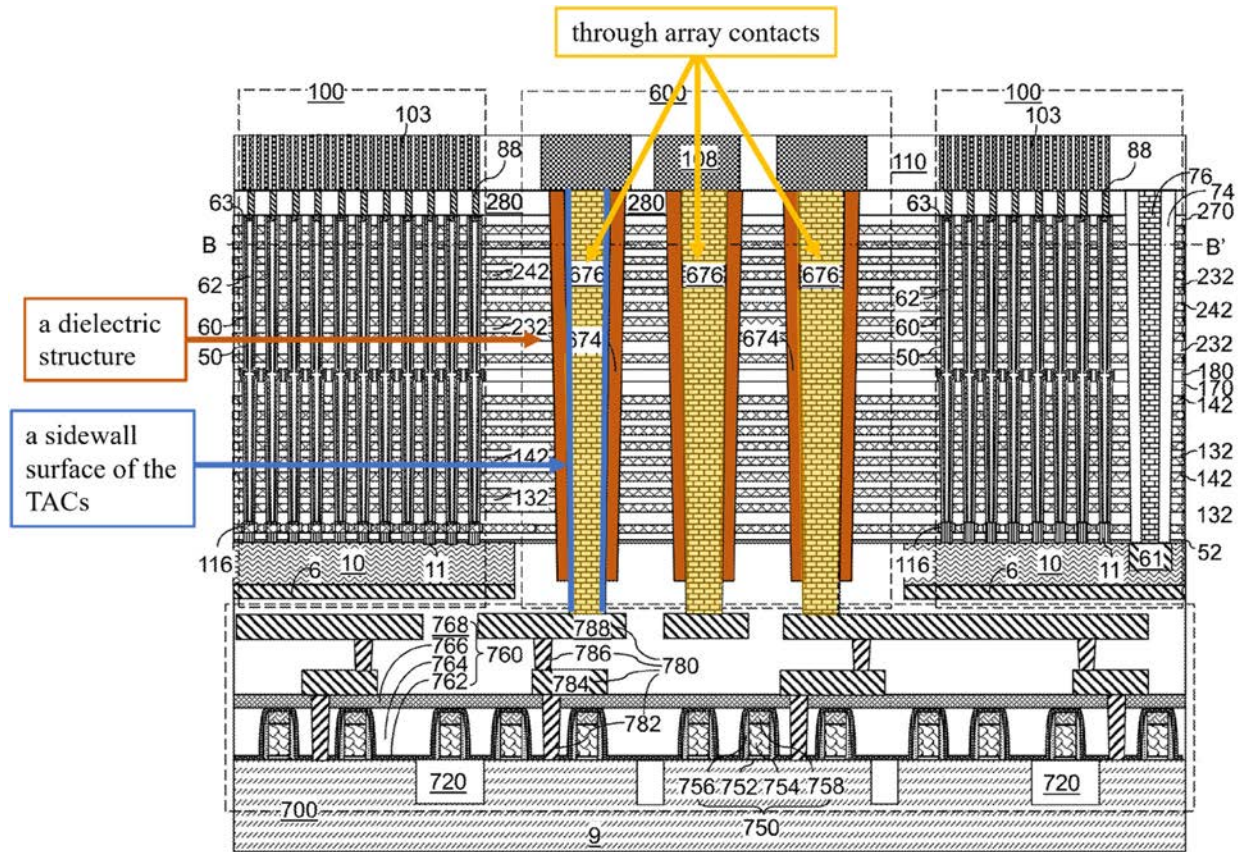
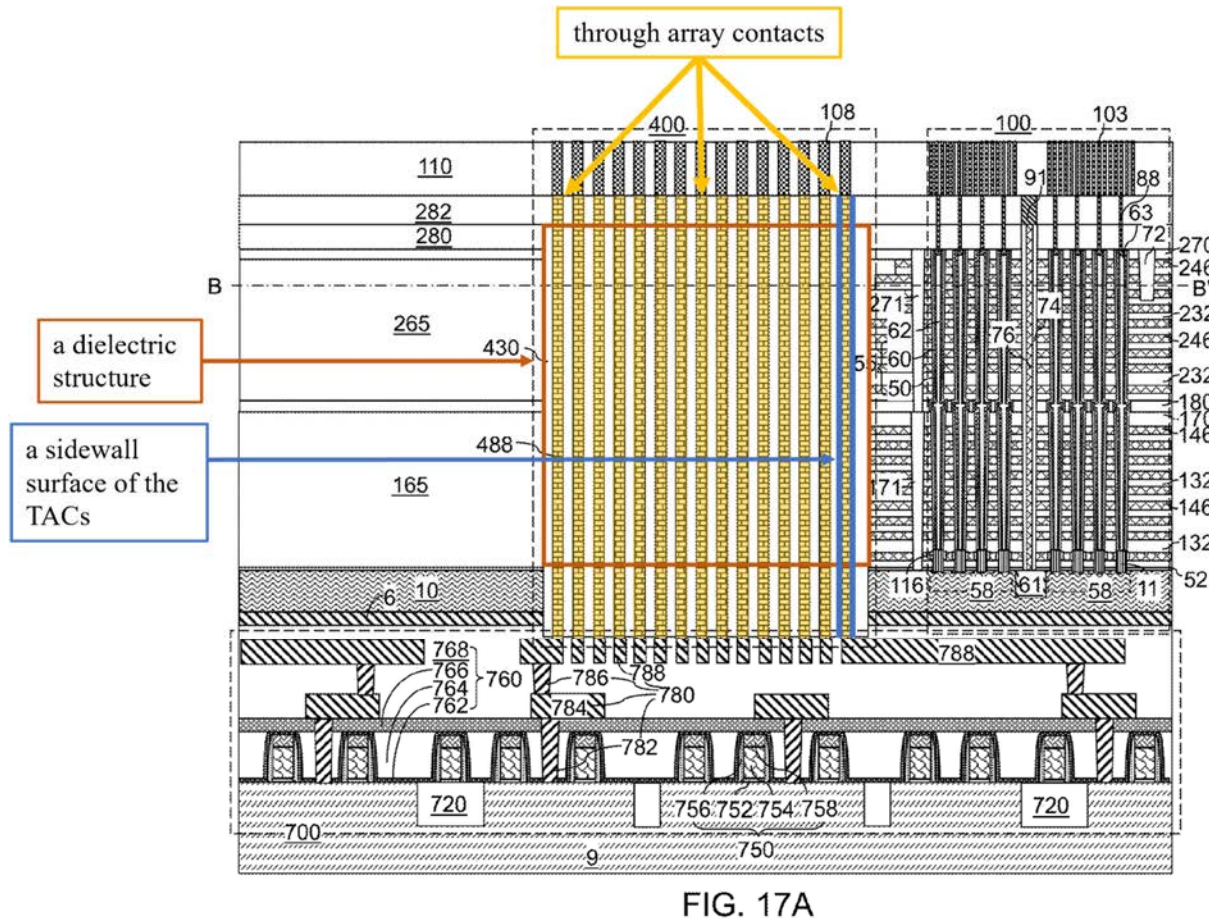


FIG. 49

Ex. 1005, Fig. 49 (annotated).

ii. First Exemplary Structure

187. As shown in Fig. 17A below, *the dielectric structure* (upper part of “dielectric fill material portion 430”) in Toyama’s first exemplary structure *abuts a sidewall surface of the TACs* (“sidewall surface of “through-memory-level via structures 488”):



Ex. 1005, Fig. 17A.

3. Claim 3

[3] “The 3D memory device claim 1, wherein the 3D memory device is a NAND 3D memory device.”

188. For the reasons I explained for limitation [1.PRE], A POSITA would have readily appreciated that Toyama’s exemplary structures are each *a 3D NAND memory device*. Ex. 1005, Abstract.

4. Claim 4

[4] “The 3D memory device of claim 1, wherein the alternating layer stack comprises alternating pairs of a dielectric and a conductor layer.”

189. For the reasons explained for limitation [1.B], above, and limitation [15.B], below, Toyama discloses that its *alternating layer stack* (“alternating stack (132, 146, 232, 246)”) *comprises alternating pairs of a dielectric layer and a conductor layer* (“insulating layers (132, 232)” and “electrically conductive layers (146, 246),” respectively. Ex. 1005, Figs. 17A (first exemplary structure), 49 (Second Modification); *id.*, [0172], [0190], [0228], [0232] [0337].

5. Claim 5

[5] “The 3D memory device of claim 1, wherein the dielectric material is silicon oxide.”

190. Toyama’s Second Modification and Toyama’s first exemplary structure meet this requirement.

i. Second Modification

191. As a reminder, in Toyama’s Second Modification “insulating liners 674” are *a dielectric structure*. See limitation [1.C.i]. Toyama contemplates that the dielectric material from which the dielectric structure is made *comprises silicon oxide*. In particular, Toyama discloses that “insulating liner 674” may “hav[e] a same material composition ... as the insulating spacer 74.” Ex. 1005, [0381]. The “insulating spacer 74” in Toyama is described as including “an insulating material such as silicon oxide.” *Id.*, [0234]. Accordingly, Toyama teaches that *the dielectric*

material (a material out of which “insulating liners 674” are made) *comprises silicon oxide*.

192. At a minimum, it would have been obvious to a POSITA that Toyama’s insulating liners 674 comprised silicon oxide. As its name reflects, Toyama’s “insulating liner 674” is insulating. The properties of silicon oxide were well-characterized and had been studied extensively. It was well-known to POSITAs that silicon oxide was a suitable insulating material from which an insulating liner could be made and it was commonly used for that purpose. This knowledge is reflected in numerous references, including: Ex. 1019 (U.S. Pat. No. 9,293,348), 2:61-65 (“dielectric structure” may comprise an “oxide” such as “silicon oxide”); Ex. 1020 (U.S. Pat. No. 10,103,169), Figs. 11-12, 3:1-8 and 21:1-61 (discussing “formation of a conformal silicon oxide liner” in 3D-NAND memory devices”); Ex. 1021 (U.S. Pat. No. 8,697,519), 7:29-40 (“the liner insulating layer may include a silicon oxide layer”). Because silicon oxide had been used extensively in semiconductor manufacturing, a POSITA would have had more than a reasonable expectation of success in using it for Toyama’s insulating liners 674. Thus, a POSITA would have found it obvious to use silicon oxide as *the dielectric material* in Toyama’s insulating liners 674.

ii. First Exemplary Structure

193. As a reminder, in Toyama’s first exemplary structure *the dielectric material* is the “dielectric fill material” that forms “dielectric fill material portion 430.” See limitation [1.C.v] discussion. Toyama discloses that “dielectric fill material portion 430 includes a dielectric material such as undoped silicate glass (e.g., *silicon oxide*), doped silicate glass, or a spin-on glass (SOG).” Ex. 1005, [0216] (emphasis added).

6. Claim 6

[6] “The 3D memory device of claim 1, wherein the dielectric structure comprises an oxide.”

194. For the reasons I explain above, Toyama teaches that *the dielectric structure* (“insulating liners 674” in the Second Modification, and the upper part of “dielectric fill material portion 430” in the first example structure) *comprises an oxide* (e.g., silicon oxide). See, specifically, my discussions for limitation [1.C.v] and claim 5.

7. Claim 7

[7] “The 3D memory device of claim 1, wherein the dielectric structure defines a through array contact region within the 3D memory device.”

195. Toyama’s Second Modification and Toyama’s first exemplary structure both meet this requirement. One preliminary matter that applies to both embodiments is that the ’378 patent broadly characterizes the *through array contact*

region. Ex. 1001, 10:49-56. The '378 specification says it “can have a rectangle or square shape,” but these are only examples. *Id.* The '378 specification goes on to say that “these shapes are not limiting and dielectric structure 232 can have any shape according to a design layout,” and that “multiple dielectric structures ... are possible across [the] substrate.” *Id.* This is consistent with the plain and ordinary meaning of *region*, which does not denote any particular shape.

i. Second Modification

196. The claimed *through array contact region* in Toyama Second Modification is highlighted in Fig. 49 below. As a reminder, Toyama’s *dielectric structure* is formed by “insulating liners 674” as I discussed for claim element [1.C]. Toyama’s through array contact region that comprises a through array contact region of the 3D memory device is a part of “through-memory-level via region 600” as shown below:

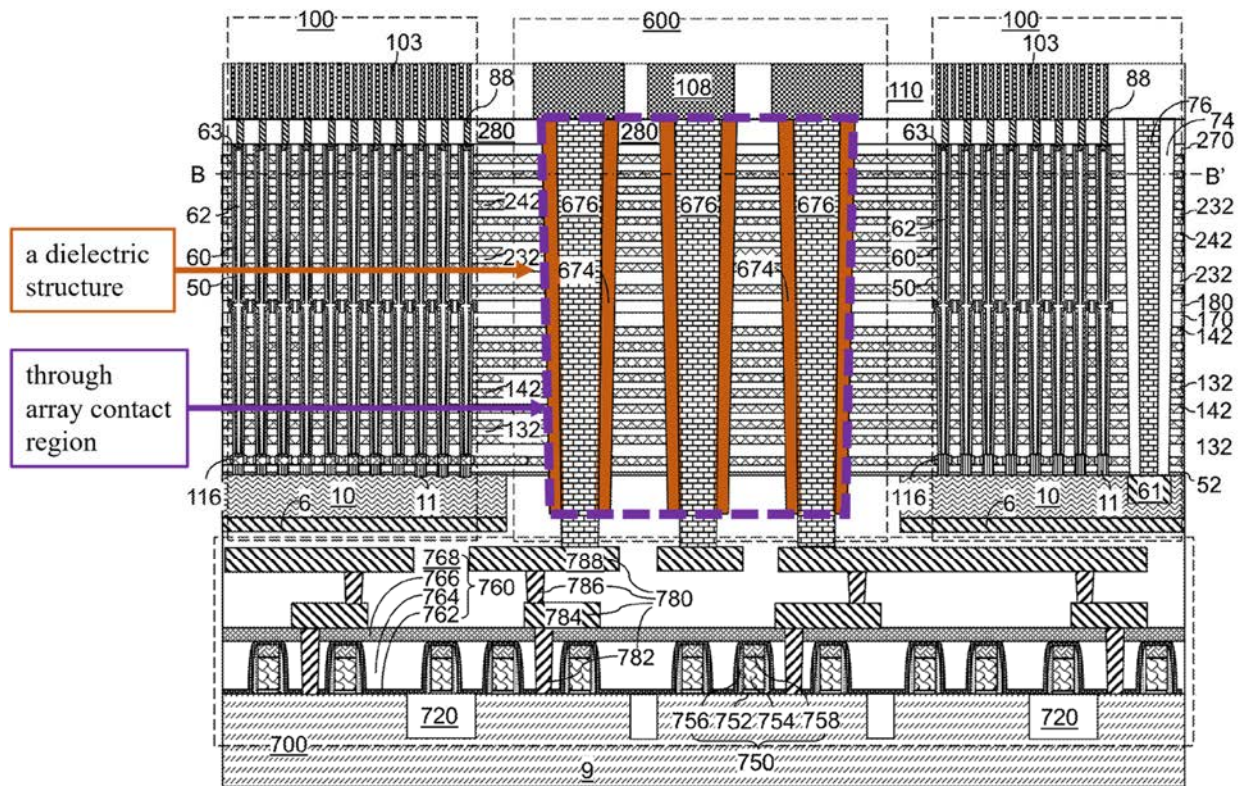


FIG. 49

Ex. 1005, Fig. 49 (annotated); *id.*, [0333], [0340], [0352].

197. “In some embodiments” of the ’378 specification, the “dielectric structure ... defines the boundaries, the shape, and the size of [the] TAC region.”

Ex. 1001, 10:21-23. According to this teaching, the portion of *the dielectric structure* (“insulating liners 674”) through which the *through array contacts* (“through-memory-level via structures 676”) pass constitutes *a through array contact region*. In this manner, the *through array contacts* (“through-memory-level via structures 676”) are electrically isolated by *the dielectric structure* (“insulating liners 674”).

8. Claim 15

[15.Pre] “A three-dimensional (3D) memory device, comprising:”

199. I offer no opinion on whether the preamble is or is not limiting. However, if the preamble is considered to be a limitation, my opinion is that Toyama discloses it. Indeed, the first sentence of Toyama’s detailed description states that “the present disclosure is directed to three-dimensional non-volatile memory devices, such as vertical NAND strings and other three-dimensional devices, and methods of making the same.” Ex. 1005, [0156]. This disclosure applies to both Toyama’s first exemplary embodiment and its Second Embodiment.

[15.A] “a substrate with an isolation structure;”

200. For ease of analysis, I separate this limitation into two sub-parts.

[15.A.i] “a substrate”

201. Toyama’s first exemplary structure and Second Embodiment both have a *substrate*. As a preliminary point, the ’378 patent explains that a “substrate” is “a material onto which subsequent material layers are added, or otherwise ‘disposed.’” Ex. 1001, 4:41-43. The ’378 patent further states that “[a] substrate can be a layer, can include one or more layers therein, and/or can have one or more layer thereupon, thereabove, and/or therebelow.” *Id.*, 5:4-6. This is reflected in certain embodiments in the ’378 specification in which “the array device and a peripheral device are formed on different substrates.” *Id.*, 5:40-45.

i. First Exemplary Structure

202. In Toyama's first exemplary structure, the *substrate* is the “planar semiconductor material layer” 10, highlighted in Fig. 17A below. See, e.g., Ex. 1005, [0169]-[0170].

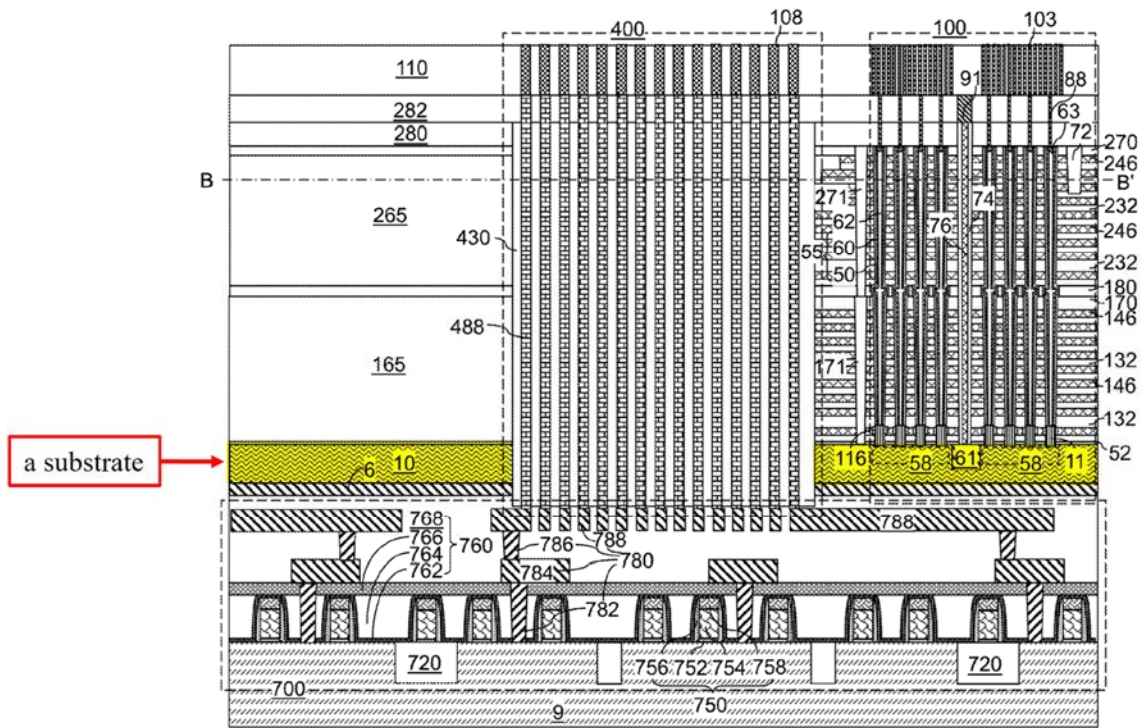


FIG. 17A

Id., Fig. 17A (annotated). Toyama Figs. 2 through 17 depict how various layers are disposed on top of “planar semiconductor material layer 10.” As one example, Toyama notes that “[a]n alternating plurality of the first insulating layers 132 and first sacrificial material layers 142 [are] formed over the planar semiconductor material layer 10.” *Id.*, [0173]. As another example, Toyama explains that “at least one retro-stepped dielectric material portion (165, 265) can be formed over the

staircase regions on the at least one alternating stack (132, 142, 232, 242).” *Id.*, [0196]. Because the “planar semiconductor material layer 10” in Toyama is a material onto which other materials and layers are added, it is *a substrate*.

iii. Second Modification

203. Although the cites above are for Toyama’s “first exemplary structure,” Toyama’s Second Embodiment likewise includes a “planar semiconductor material layer 10” as shown in Fig. 49 below, and thus teaches this limitation for the same reason.

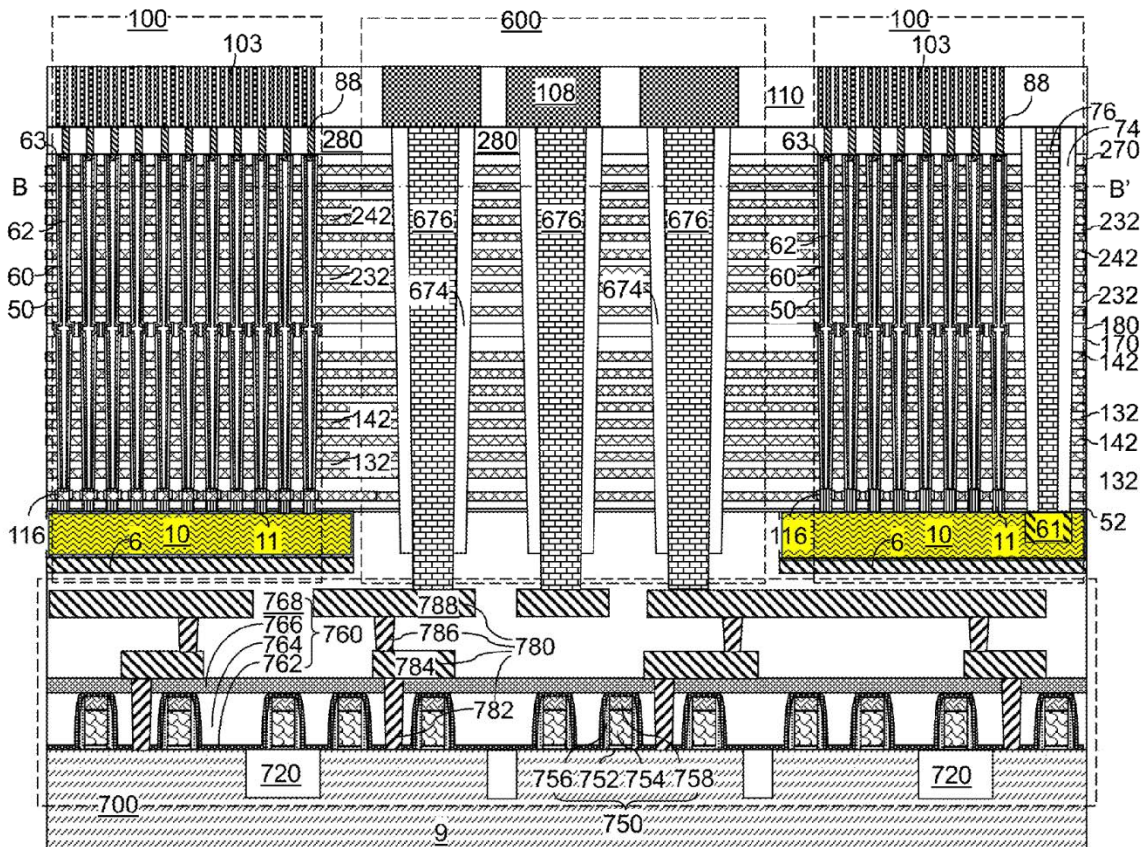


FIG. 49

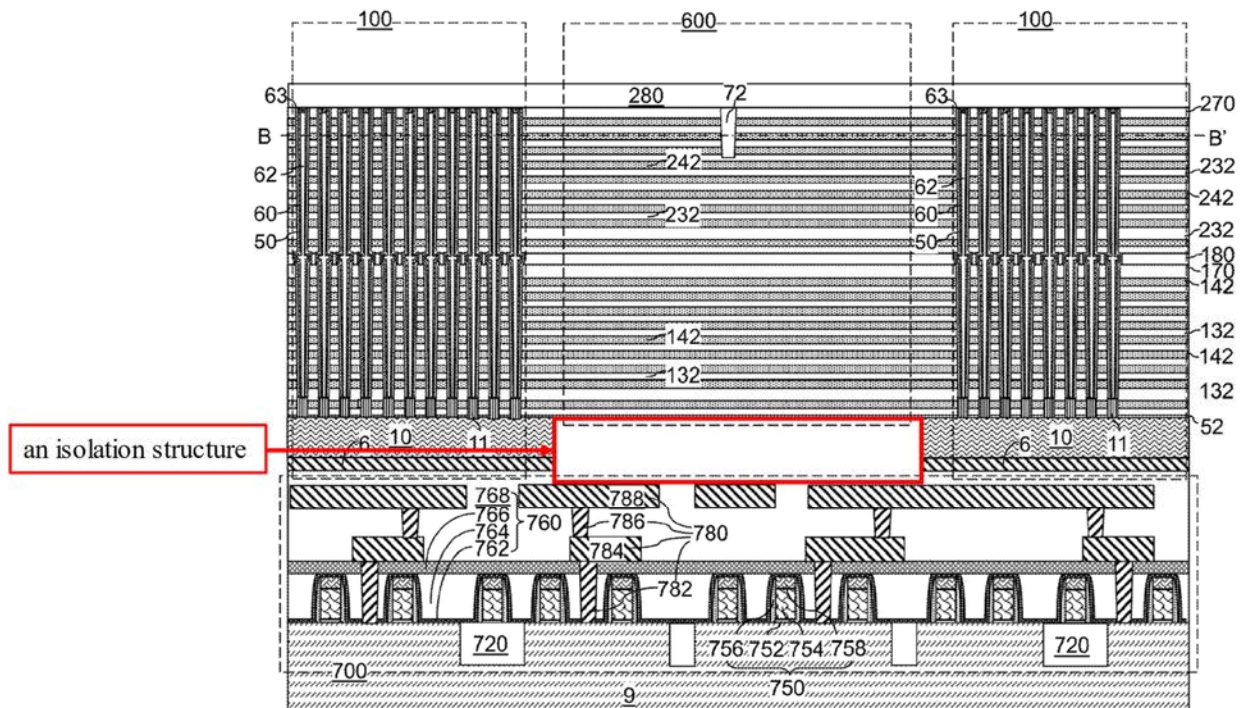
Ex. 1005, Fig. 49 (annotated).

[15.A.ii] “... with an isolation structure”

204. Both Toyama’s Second Modification and Toyama’s first exemplary structure teach this limitation.

i. Second Modification

205. Toyama’s *isolation structure* in the Second Modification is shown in Fig. 44A below.



Ex. 1005, Fig. 44A (annotated).

206. Toyama describes its Second Modification starting after the alternating stack of conductors/insulators has already been formed. See Ex. 1005, Fig. 44A. Toyama states that the “alternating stack of insulating layers (132, 232) and

dielectric spacer layers (which can be the sacrificial material layers (142, 242)) can be formed over the semiconductor substrate 9 as in previously described embodiments.” *Id.*, [0332]. Toyama further states that its Second Modification “can be formed concurrently with the formation of any of the first, second, and third exemplary structures or modifications thereof.” *Id.*.

207. A POSITA would have thus understood that Toyama’s Second Modification would use the process described for the third exemplary structure to create “opening 151” and fill it with an insulating material. Ex. 1005, [0277] (“The optional planar conductive material layer 6 and the planar semiconductor material layer 10 may be patterned to form an opening 151 extending through these layers to the underlying insulating layer 760. The opening 151 ... may be filled with another insulating material layer (e.g., a silicon oxide or doped silicate glass) 760.”). The “opening 151” is illustrated in Toyama Fig. 24A below.

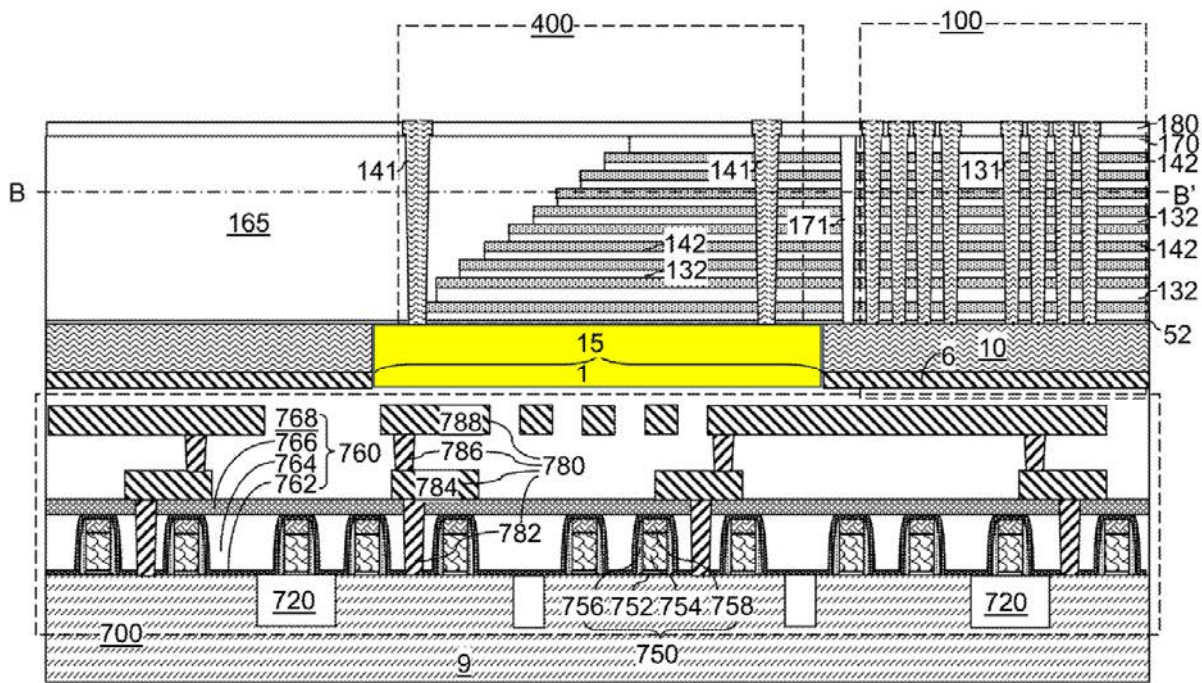


FIG. 24A

Id., Fig. 24A (annotated).

208. A POSITA would therefore have understood that, in the context of Toyama's Second Modification, the insulating material layer that fills "opening 151" is *an isolation structure*. Claim element [15.A] requires not only a *substrate* and an *isolation structure*, but *a substrate with an isolation structure*. That Toyama's *substrate* ("planar semiconductor material layer 10") is *with* its *isolation structure* (the insulating material layer that fills "opening 151") is apparent because Toyama's *isolation structure* (the insulating material layer that fills "opening 151") is formed by removing portions of the substrate and is subsequently formed within the *substrate* ("planar semiconductor material layer 10"). Accordingly, Toyama's

Second Modification teaches *a substrate* (“planar semiconductor material layer 10”) *with an isolation structure* (the insulating material layer that fills “opening 151”).

ii. First Exemplary Structure

209. For Toyama’s first exemplary structure, the lower part of Toyama’s “dielectric fill material portion 430” is *an isolation structure*. See, e.g., Ex. 1005, [0216]. Figs. 10A-12A show the formation of this structure. To begin, “through-memory-level via region 400” includes the staircase structure of layers 132, 142, 232, 242:

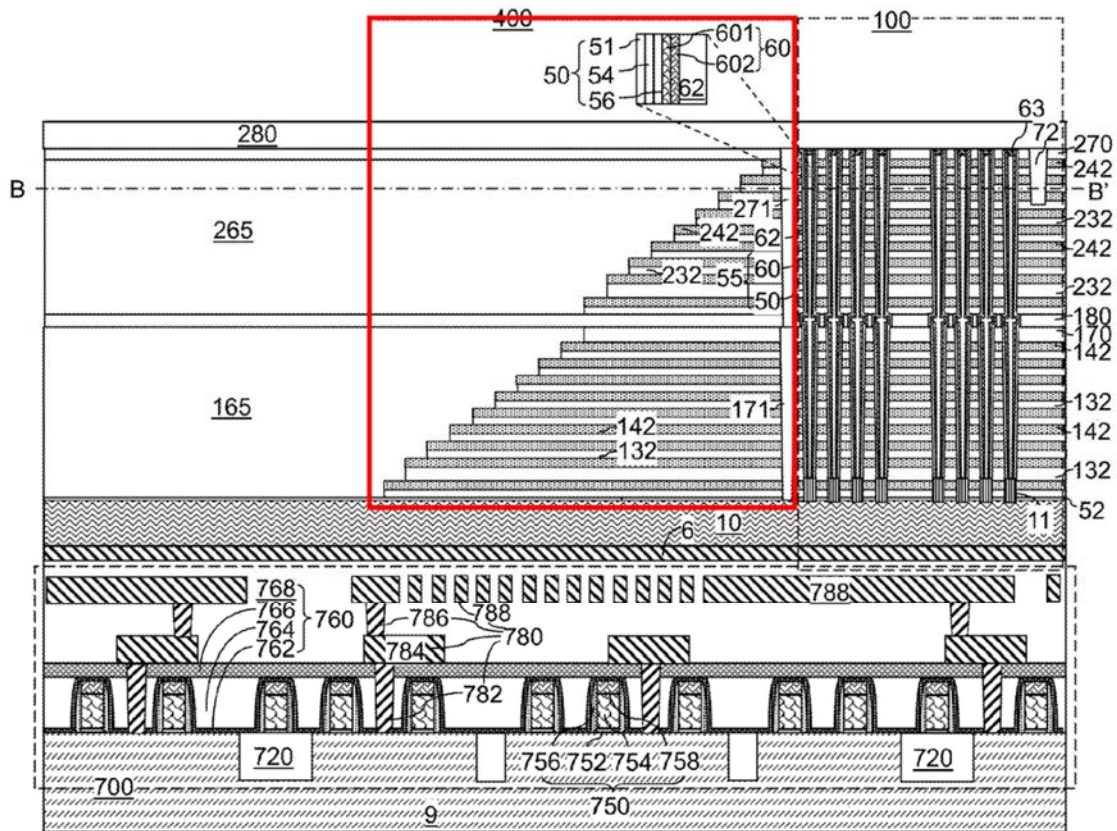
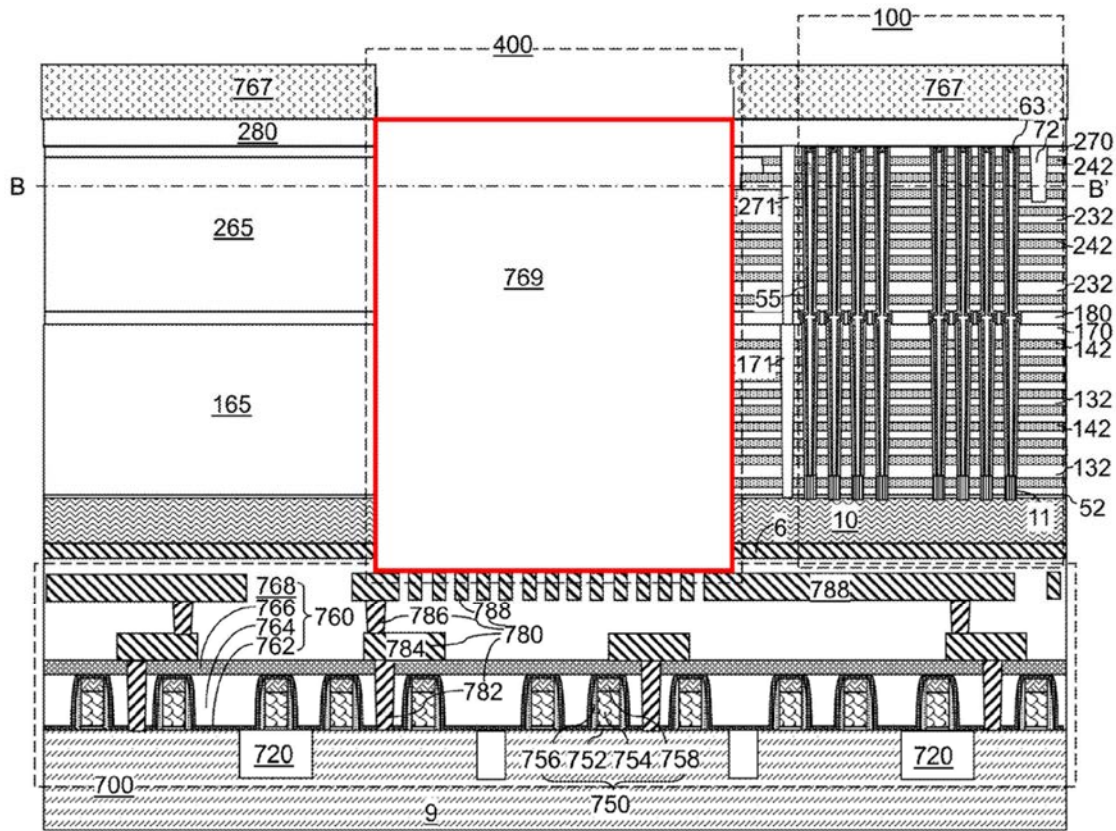


FIG. 10A

Id., Fig. 10A (annotated), [0192]-[0194]. These layers are removed, resulting in “through-memory-level opening 769”:



Id., Fig. 11A (annotated); [0213]. Next, “opening 769” is filled with a dielectric to form “dielectric fill material portion 430”:

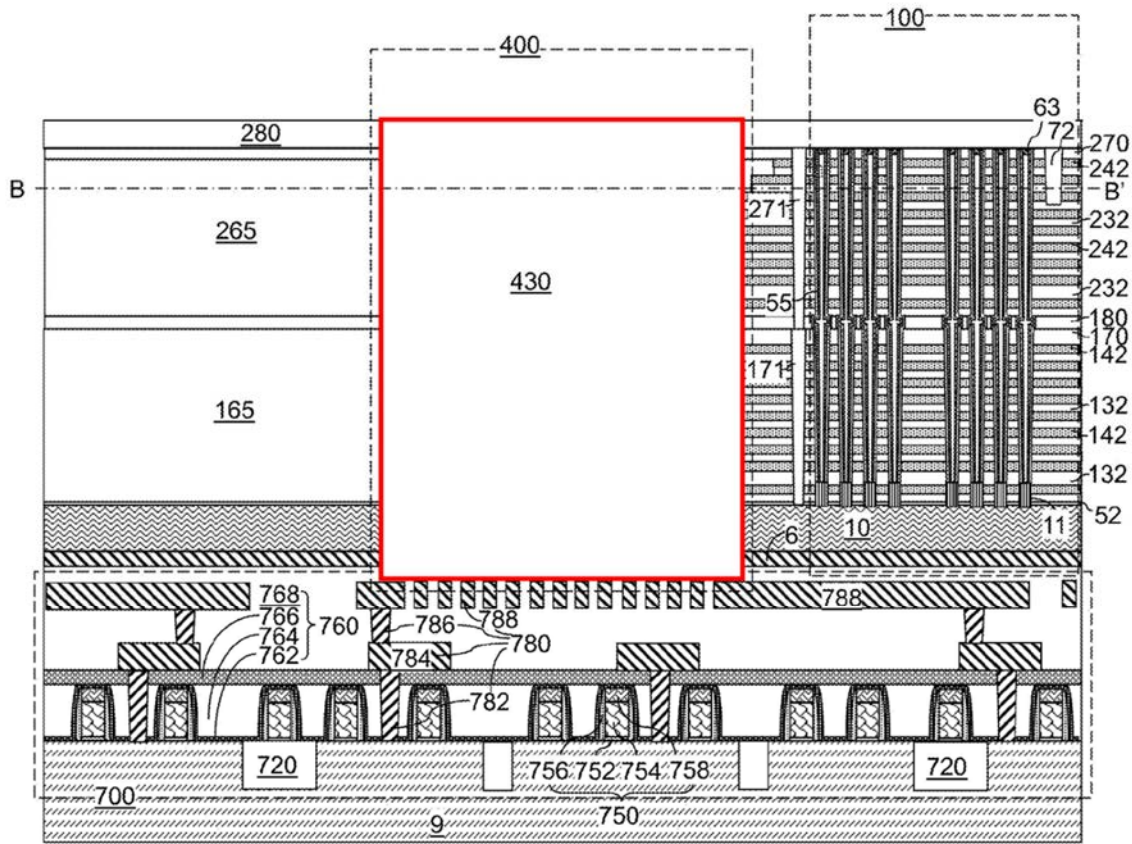


FIG. 12A

Id., Fig. 12A (annotated); [0216]. The lower portion of “dielectric fill material portion 430” (*viz.*, the portion level with and below the top of “planar semiconductor material layer 10”) is the claimed *isolation structure*, as shown below:

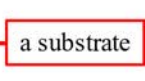


FIG. 13A

Id., Fig. 13A (annotated).

210. Toyama discloses that its “dielectric fill material portion 430 includes a dielectric material such as undoped silicate glass (e.g., silicon oxide.)” Ex. 1005, [0216]. A POSITA would have understood that “dielectric fill material portion 430” is *an isolation structure* because it electrically isolates conductors from each other and from electrical interference from the *substrate* (“planar semiconductor material layer 10”).

211. Toyama's *substrate* (“planar semiconductor material layer 10”) is *with* its *isolation structure* (lower part of “dielectric fill material portion 430”) because it is formed by removing a portion of, and is surrounded by, the *substrate* (“planar

semiconductor material layer 10”). Ex. 1005, Figs. 10A-12B (forming “opening 769” in “layer 10,” then filling the opening to form “portion 430”). Indeed, Toyama’s isolation structure is within the substrate and isolates portions of the substrate from one another.

212. In summary, Toyama’s first exemplary structure discloses *a substrate* (“planar semiconductor material layer 10”) *with an isolation structure* (lower portion of “dielectric fill material portion 430”).

[15.B] “an alternating conductor/dielectric layer stack disposed on the substrate;”

213. Toyama’s first exemplary structure and Second Embodiment each disclose this limitation. As a preliminary matter that applies to both, the ’378 patent teaches that the term “‘on’ not only means ‘directly on’ something but also includes the meaning of ‘on’ something with an intermediate feature or a layer therebetween.” Ex. 1001, 4:20-25.

ii. First Exemplary Structure

214. As can be seen in Fig. 17A below, Toyama’s “alternating stack (132, 146, 232, 246)” is the claimed *alternating conductor/dielectric layer stack disposed on the substrate*. I note that only some of the alternating conductors (green) and dielectric (yellow) layers are highlighted to avoid cluttering the figure.

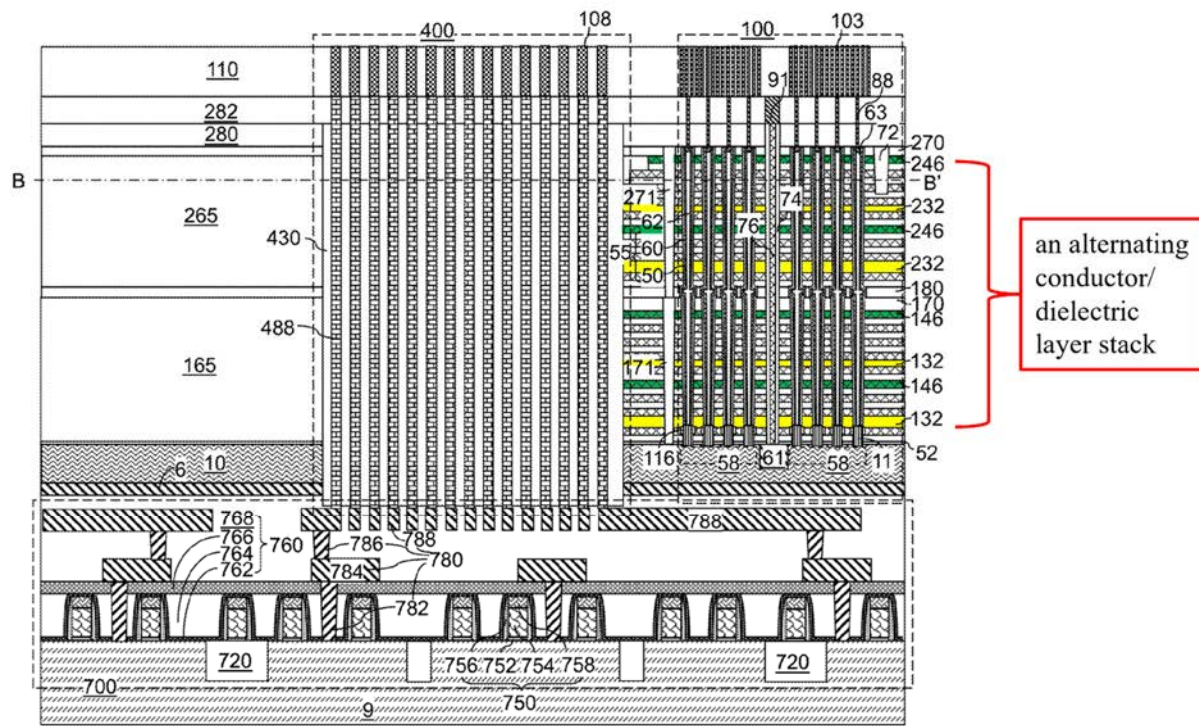


FIG. 17A

Ex. 1005, Fig. 17A (annotated). Toyama “alternating stack” comprises “first and second conductive material layers (146, 246),” “first insulating layers 132,” and “second insulating layers 232.” *Id.*, [0172], [0190], [0228], [0232].

215. Toyama’s “alternating stack” is *disposed on the semiconductor substrate*, per the broad meaning of “on” set forth in the ’378 patent itself. As noted for limitation [15.A], above, Toyama’s “planar semiconductor material layer 10” is a *semiconductor substrate*. Ex. 1005, [0170]-[0171]. As shown in Fig. 17A, above, Toyama’s alternating stack is *disposed on* (above) “planar semiconductor material layer 10.”

iii. Second Modification

216. While the discussion above is for Toyama's "first exemplary structure," Toyama's Second Modification also teaches this limitation (as can be seen in Fig. 49 below) for the same reasons.

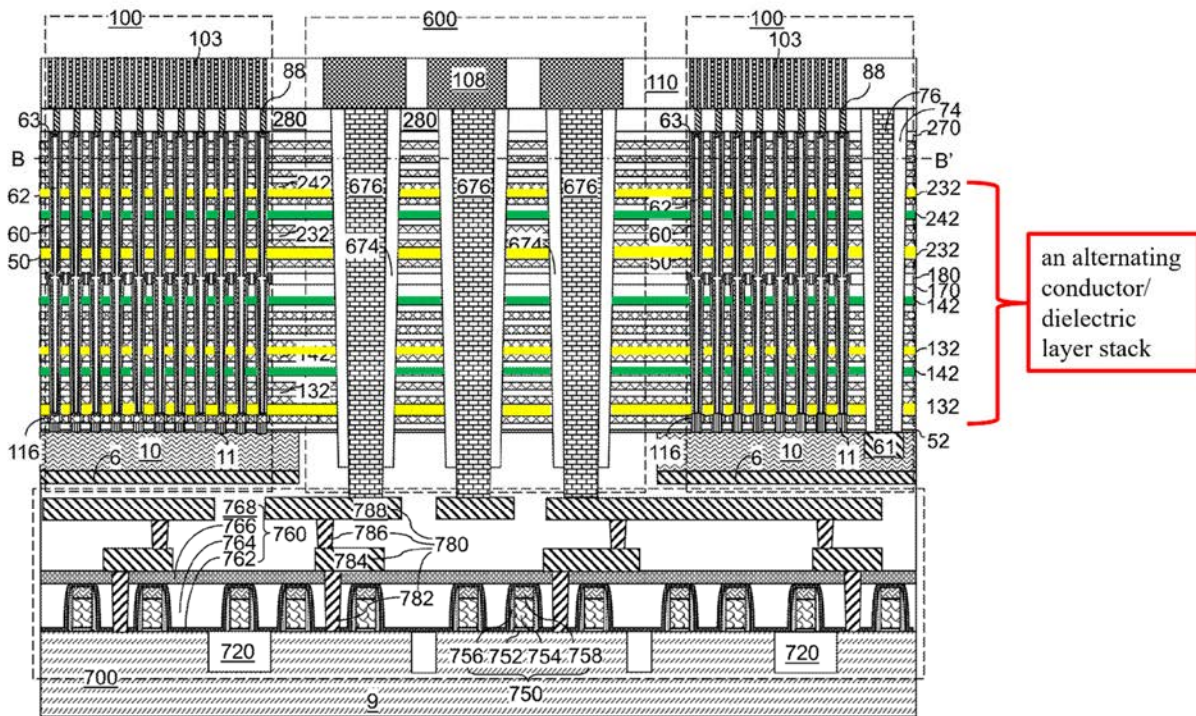


FIG. 49

See, e.g., Ex. 1005, Fig. 49, [0337] ("An alternating stack (132, 146, 232, 246) of insulating layers ([1]32, 232) and electrically conductive layers (146, 246) is thus formed."). In what amounts to a clear typographical error, Fig. 49 labels its alternating conductor/dielectric layer stack as elements 132, 142, 232, 242. Elements 142, 242 are "sacrificial material layers" which, in a process step prior to Fig. 49, were removed and replaced with "electrically conductive layers (146, 246)."

Id., [0337], [0340]. That is also reflected in the figures, which depict how the sacrificial material layers (shaded in gray, as in Fig. 45A) are replaced by electrically conductive layers (cross-hatched, as in Fig. 46A).

[15.C] “[i] a dielectric structure on the isolation structure and [ii] extending vertically through the alternating conductor/dielectric layer stack, [iii] wherein the alternating conductor/dielectric layer stack abuts a sidewall surface of the dielectric structure and [iv] the dielectric structure is formed of a dielectric material;”

217. For ease of analysis, I separate this limitation into four sub-parts labelled [i]-[iv] and address how Toyama’s first exemplary structure and Second Embodiment teach each one in turn.

i. Second Modification

[15.C.i] “a dielectric structure on the isolation structure”

218. The “insulating liners 674” in Toyama’s Second Modification, shown below in Fig. 49, are the claimed *dielectric structure*. Ex. 1005, [0340].

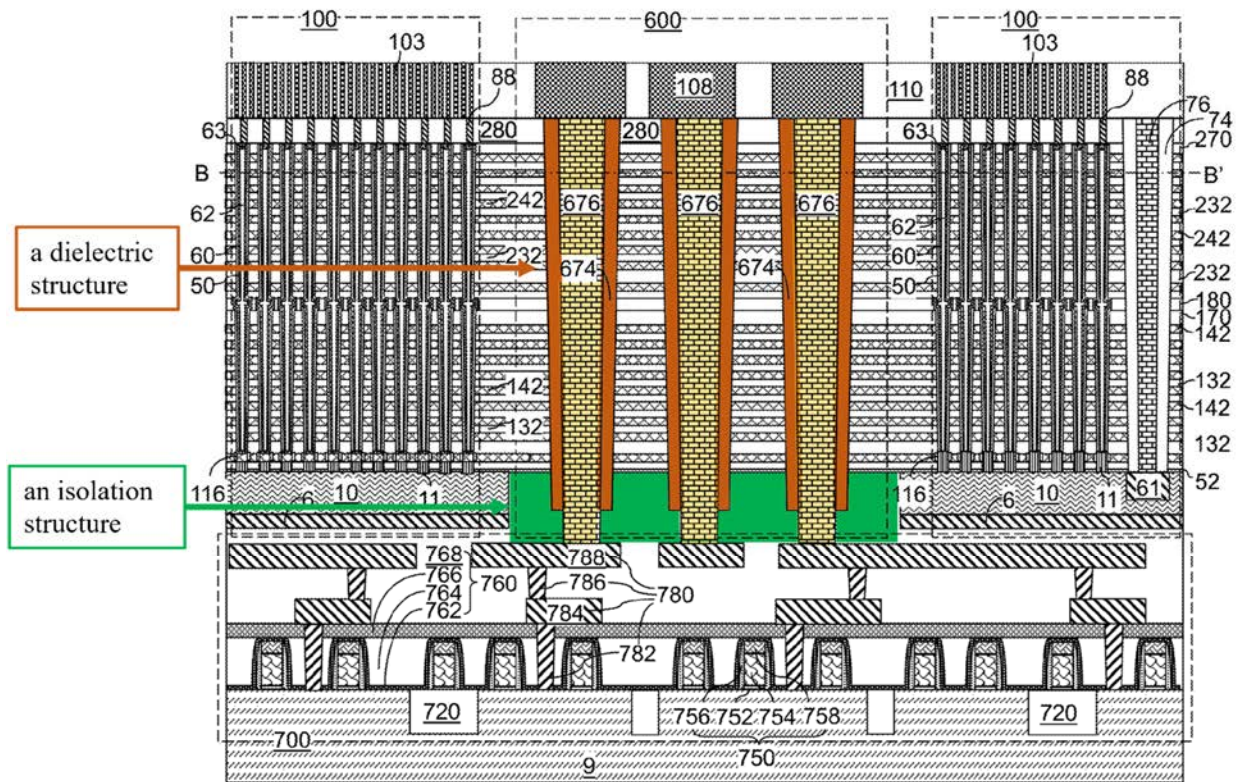


FIG. 49

Id., Fig. 49 (annotated).

219. The “insulating liners 674” are *dielectric*. Toyama forms “insulating liners 674” by depositing “a conformal insulating material layer” in “through-memory-level openings 679.”⁵ Ex. 1005, [0338]-[0340]. Toyama discloses that

⁵ I note that Toyama [0338] refers to “through-memory-level openings 689,” but that appears to be a typographical error. All of the relevant figures (*e.g.*, Figs. 47A-B to 49) and the other textual description refer to the elements as “through-memory-level openings 679.”

insulating liner 674 may be a “dielectric material.” *Id.*, [0233] (“[a]n insulating spacer 74 including a dielectric material”), [0381] (“insulating liner 674 having a same material composition and a same thickness as the insulating spacer 74”).

220. The challenged claims do not recite, or otherwise require, a “single-material” dielectric structure. This is confirmed by the ’378 patent which contemplates a “single-material” dielectric structure only “[i]n some embodiments.” Ex. 1001, 5:50-59. Regardless, Toyama contemplates that its “insulating liners 674” are made of a single material (e.g., silicon oxide). See claim 19 analysis.

221. Toyama’s “insulating liners 674” are, individually and collectively, a *structure*, which is not an art-specific term and is given its plain and ordinary meaning. See Ex. 1022, 5 (Merriam-Webster’s definition of “structure” as “something (as a building) that is constructed”). As explained above, they are constructed together, and all have the same function of insulating and electrically isolating the *through array contacts* (“through-memory-level via structures 676”) as they pass through the *alternating conductor/dielectric layer stack* (“alternating stack (132, 146, 232, 246).” A POSITA would thus have understood that “insulating liners 674” are individually and collectively *a dielectric structure*.

222. As explained above for element [15.A], Toyama’s Second Modification contemplates forming *the isolation structure* (the insulating material layer that fills “opening 151”) using the process described for the third exemplary structure.

Toyama further teaches that the *dielectric structure* (“insulating liners 674”) is *on* the *isolation structure* (the insulating material layer that fills “opening 151”) because “insulating liners 674” make contact with and extend above the isolation structure. Ex. 1001, 4:20-29 (defining “on”).

[15.C.ii] “a dielectric structure ... extending vertically through the alternating conductor/dielectric layer stack”

223. As I discuss in the section above, Toyama’s “insulating liners 674” are individually and collectively the claimed *dielectric structure*. And, as I noted above with reference to claim element [15.B], Toyama’s “alternating stack (132, 146, 232, 246)” is *the alternating conductor/dielectric layer stack*. Accordingly, as shown in Fig 49 below, Toyama discloses *a dielectric structure* (“insulating liners 674”) *extending vertically through the alternating conductor/dielectric layer stack* (“alternating stack 132, 146, 232, 246”).

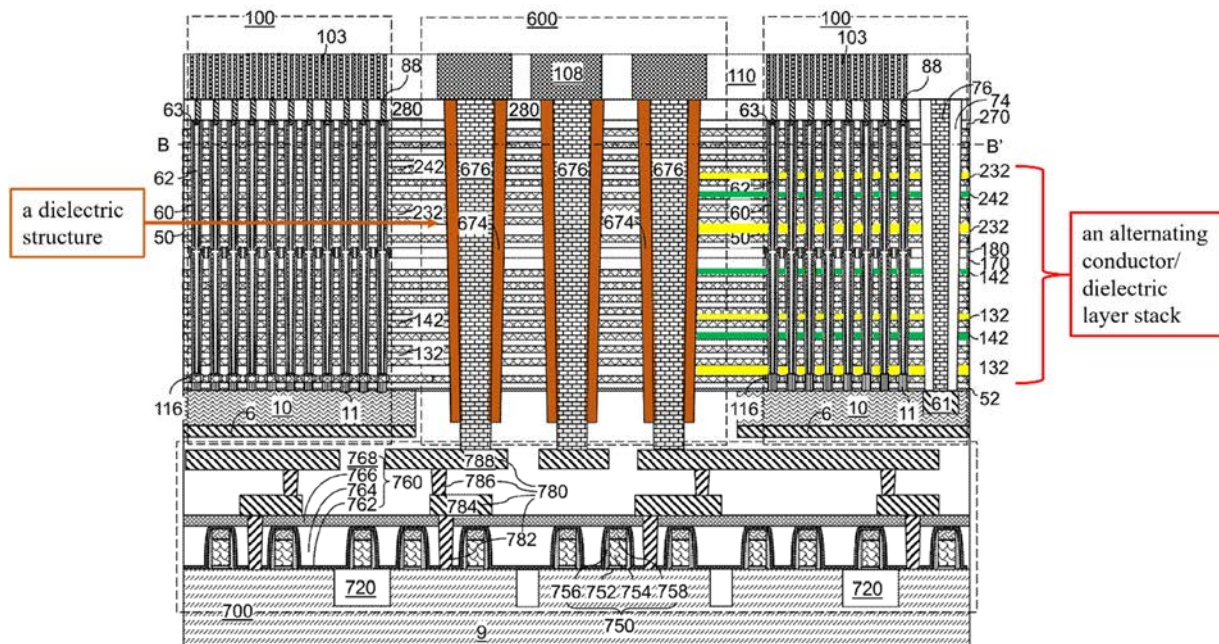


FIG. 49

Ex. 1005, Fig. 49 (annotated). As I noted previously, labels 142 and 242 are properly understood to refer to conductive material layers (146, 246).

[15.C.iii] “a dielectric structure ... wherein the alternating conductor/dielectric layer stack abuts a sidewall surface of the dielectric structure”

224. As highlighted below in Fig. 49, Toyama discloses *a dielectric structure* (“insulating liners 674”) *wherein the alternating conductor/dielectric layer stack* (“alternating stack (132, 146, 232, 246)”) *abuts a sidewall surface of the dielectric structure* (a sidewall surface of “insulating liner 674”):

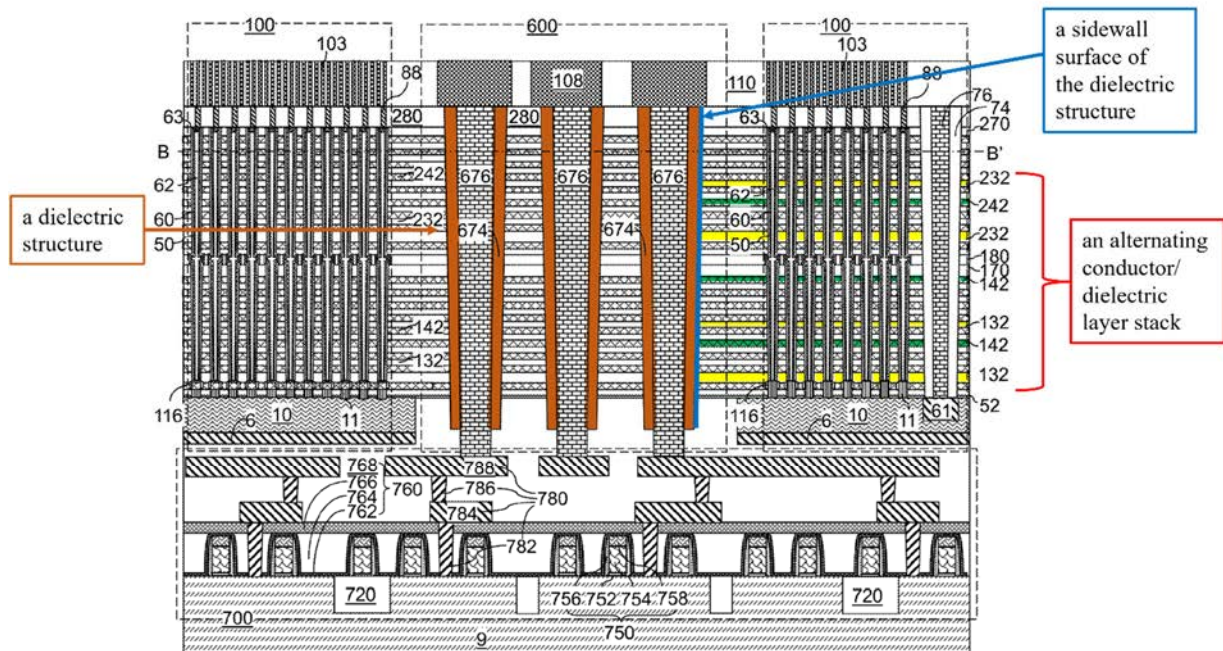


FIG. 49

Ex. 1005, Fig. 49 (annotated). As I noted previously, labels 142 and 242 are properly understood to refer to conductive material layers (146, 246).

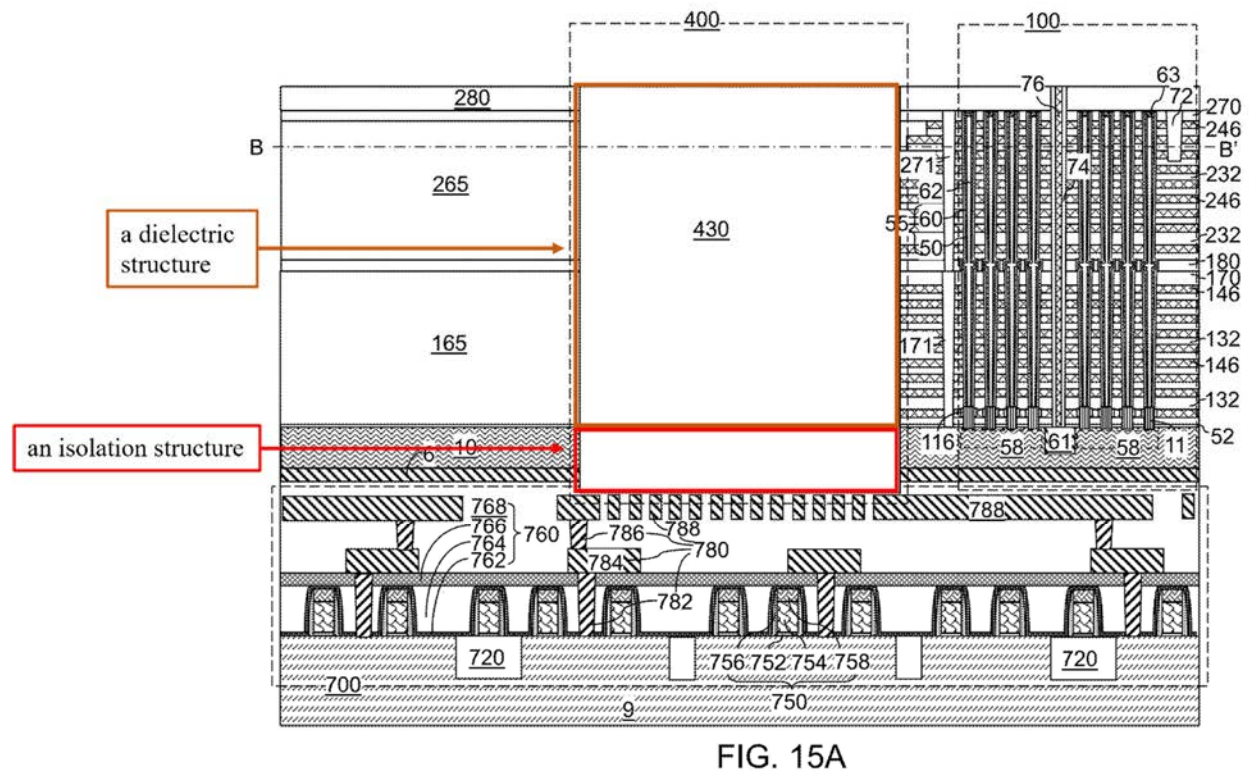
[15.C.iv] “... wherein ... the dielectric structure is formed of a dielectric material”

225. As I discussed above, Toyama’s “insulating liners 674” are individually and collectively the claimed *dielectric structure*. And, as I discussed for element [15.C.i], each of these elements is a dielectric material. Toyama thus discloses *a dielectric structure* (“insulating liners 674”) *wherein the dielectric structure is formed of a dielectric material*.

b. First Exemplary Structure

[15.C.i] “a dielectric structure on the isolation structure”

226. I discussed in connection with claim element [15.A] that *the isolation structure* is the portion of “dielectric fill material portion 430” at and below the top surface of semiconductor substrate 10. As shown below in Fig. 15A, in Toyama’s first exemplary structure the upper part of “dielectric fill material portion 430” (viz., above the top of substrate 10) is the claimed *dielectric structure*:



Ex. 1005, Fig. 15A (annotated). Toyama explains that “a dielectric fill material portion 430 is formed within each through-memory-level opening 769, for example, by deposition of a dielectric fill material.” *Id.*, [0216]. Thus, the upper section of

the “dielectric fill material portion 430” is *a dielectric structure* because it is composed of “a dielectric fill material.” *Id.*

227. Recall that Toyama’s isolation structure is the portion of “dielectric fill material portion 430” at or below the top of substrate 10. Toyama discloses that the first exemplary structure’s *dielectric structure* (upper part of “dielectric fill material portion 430”) is *on the isolation structure* (lower portion of “dielectric fill material portion 430”).

228. I note that nothing in the claim requires forming the *dielectric structure* and *isolation structure* in different steps or from different materials, nor does the specification prohibit or disavow this. On the contrary, the ’378 specification broadens “isolation structure” beyond the disclosed embodiment when it states that “STI structure 233 is exemplary and not limiting. As such, other isolation structures can be used.” Ex. 1001, 10:34-35. The purpose of the “dielectric structure” in the ’378 patent is to electrically insulate a “through array contact” as it extends through the alternating conductor/dielectric layer stack. *Id.*, 11:12-14. The purpose of the “isolation structure” in the ’378 patent is to electrically insulate a “through array contact” as it extends through the “substrate.” The upper and lower portions of Toyama’s “dielectric fill material portion 430,” respectively, fulfill these same purposes. Moreover, the language of claim element [15.A], which recites *a substrate with an isolation structure*, supports my opinion. This claim language suggests that

only the portion of an isolation structure that is *with* the *substrate* is the claimed *isolation structure*. By extension, a portion of a dielectric structure (such as the upper portion of dielectric 430 in Toyama), that is located above the level of the substrate is properly considered *a dielectric structure on the isolation structure* (because the upper bound of the claimed *isolation structure* is determined by reference to the substrate).

229. Even if the claim language did require separately forming *the isolation structure* and *the dielectric structure* (which it does not), Toyama’s first exemplary structure nevertheless renders the claim element obvious. Using isolation structures on a substrate to electrically isolate components was well-known and commonplace prior to the effective filing date of the ’378 patent priority date. Indeed, Toyama’s third exemplary structure teaches just that, as I described in connection with element [15.A.ii] for Toyama’s Second Embodiment. As it relates to Toyama’s first exemplary structure, forming the *isolation structure* and the *dielectric structure* separately would be no more than the mere substitution of a known process (forming an isolation structure in “opening 151” before forming the dielectric structure, as in Toyama’s third exemplary structure) for another process (forming the isolation and dielectric structures at the same time, as in Toyama’s first exemplary structure) to obtain predictable results (the insulating material layer that fills “opening 151” electrically isolates the conductors embedded within).

[15.C.ii.] “a dielectric structure ... extending vertically through the alternating conductor/dielectric layer stack”

230. As I discussed in the previous section, the upper part of Toyama’s “dielectric fill material portion 430” is the claimed *dielectric structure*. And, as I discussed in connection with element [15.B], Toyama’s “alternating stack (132, 146, 232, 246)” is *the alternating conductor/dielectric layer stack*. Accordingly, as shown in Fig.15A below, Toyama discloses *a dielectric structure* (upper part of “dielectric fill material portion 430”) *extending vertically through the alternating conductor/dielectric layer stack* (“alternating stack 132, 146, 232, 246”):

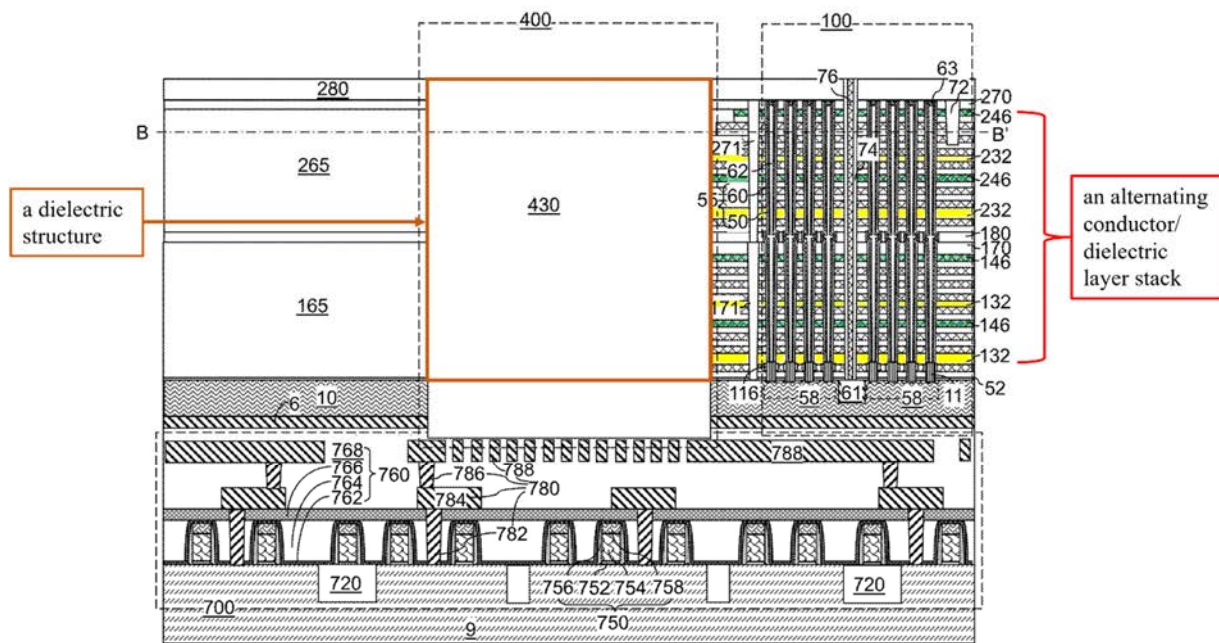


FIG. 15A

Ex. 1005, Fig. 15A (annotated).

231. I note here that Toyama's first exemplary structure satisfies this limitation in substantially the same way as one of the embodiments in the '378

patent. In particular, the '378 specification shows an embodiment where dielectric structure 124 is surrounded on three sides by an alternating conductor/dielectric layer stack. This can be seen in Fig. 1C below, which is a top view of a 3D NAND device (with memory region 110 on the right and staircase region on the left):

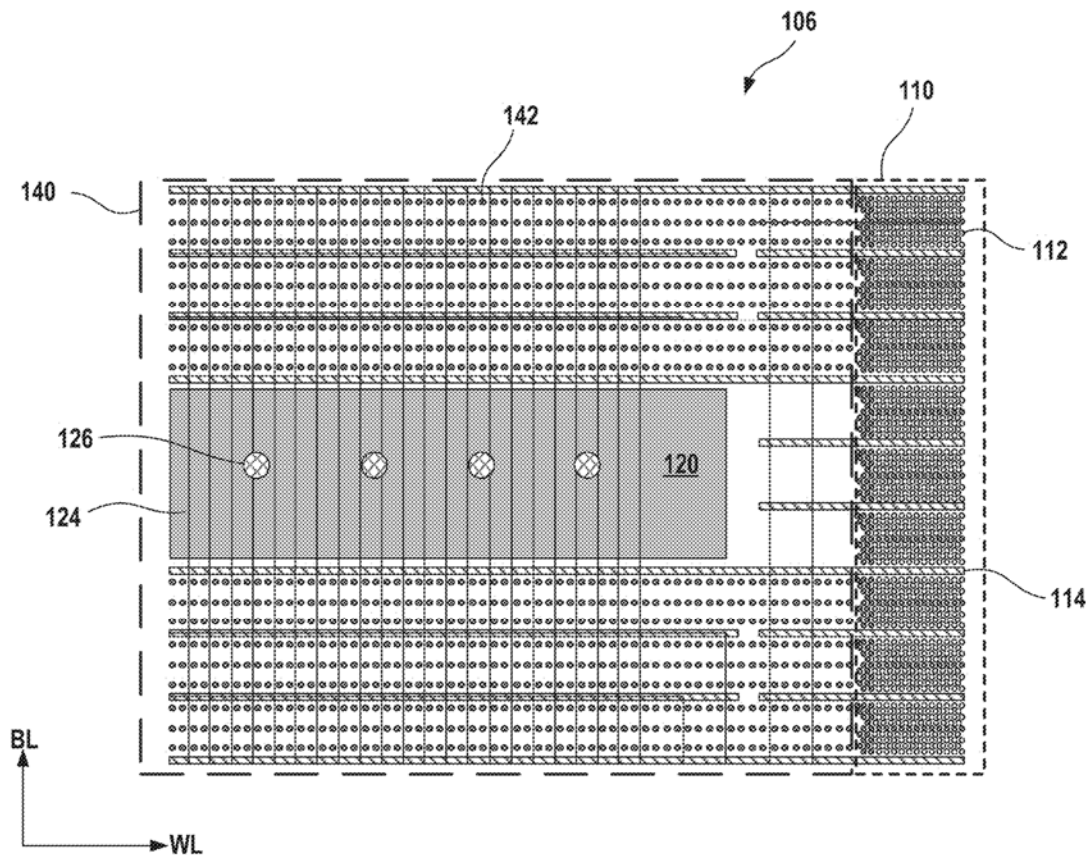
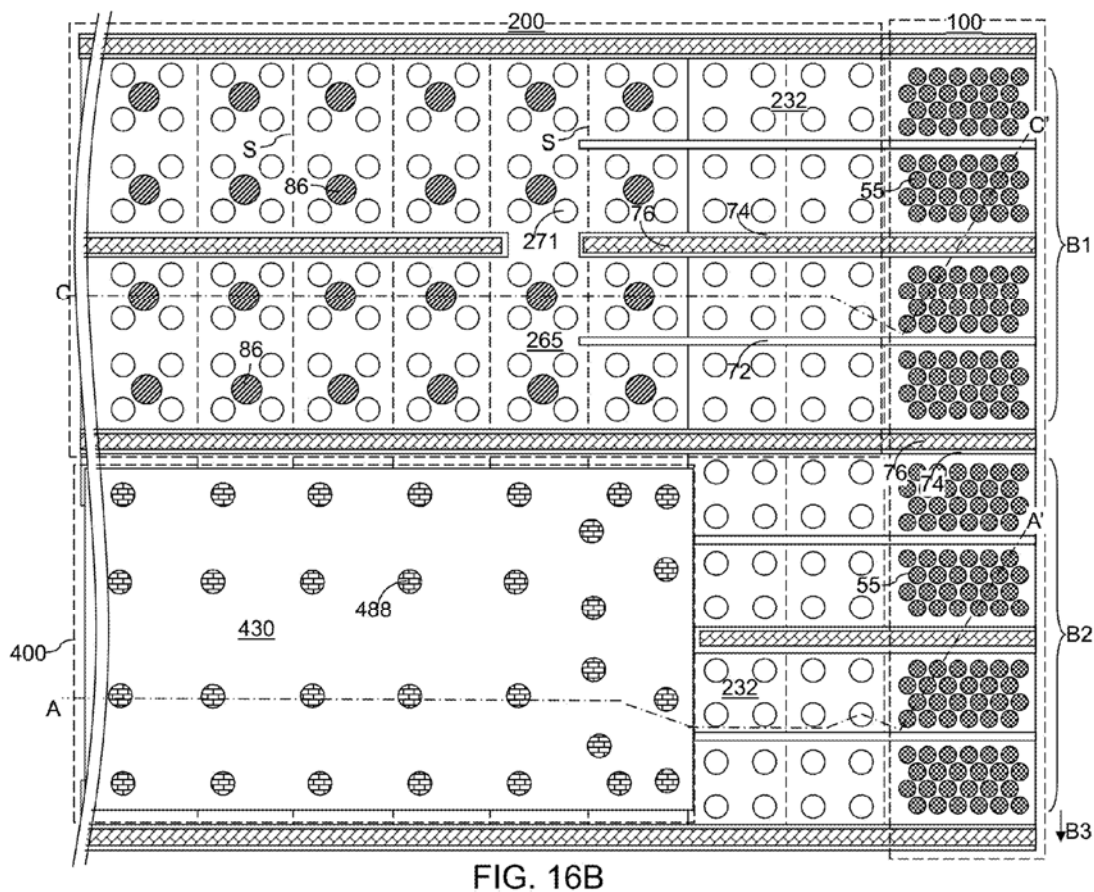


FIG. 1C

Ex. 1001, Fig. 1C.

232. Toyama's first exemplary structure is similar: the *dielectric structure* ("dielectric fill material portion 430") borders three regions including an alternating conductor/dielectric layer stack. This is shown in Toyama Fig. 16B below, which is

a top view of a 3D NAND device (with “memory array region 100” on the right and staircase regions (“word line contact via region 200”) on the left). Although not illustrated in Fig. 16B, I note that region 200 extends on the bottom of the figure as well.



Ex. 1005, Fig. 16B.

233. Toyama forms its *dielectric structure* (“dielectric fill material portion 430”) in the same way as the ’378 patent forms its dielectric layer 702. The “dielectric fill material portion 430” in Toyama and “dielectric layer 702” in the ’378 specification are both formed by removing part of the dielectric stack before

replacing the sacrificial layers with electrically conductive layers. In particular, the '378 patent removes part of “dielectric stack 400” to form “opening 600”:

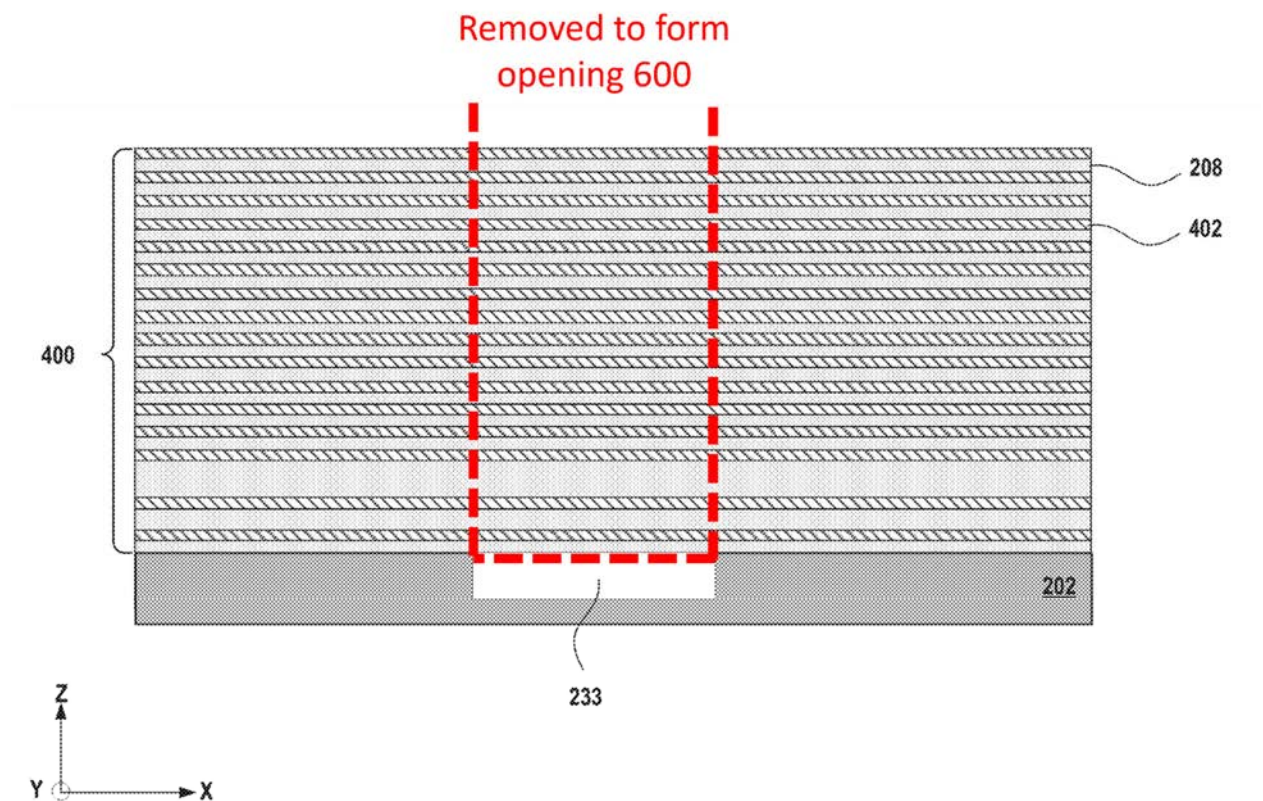


FIG. 4

Ex. 1001, Fig. 4 (annotated); *see also id.*, Fig. 6, 15:12-14. The '378 patent then fills “opening 600” with “dielectric layer 702.” *Id.*, 15:42-44.

234. In like manner, Toyama’s first exemplary structure removes “insulating layers” 132, 232 and “sacrificial material layers” 142, 242 to form “opening 769,” as shown below in Fig. 10A:

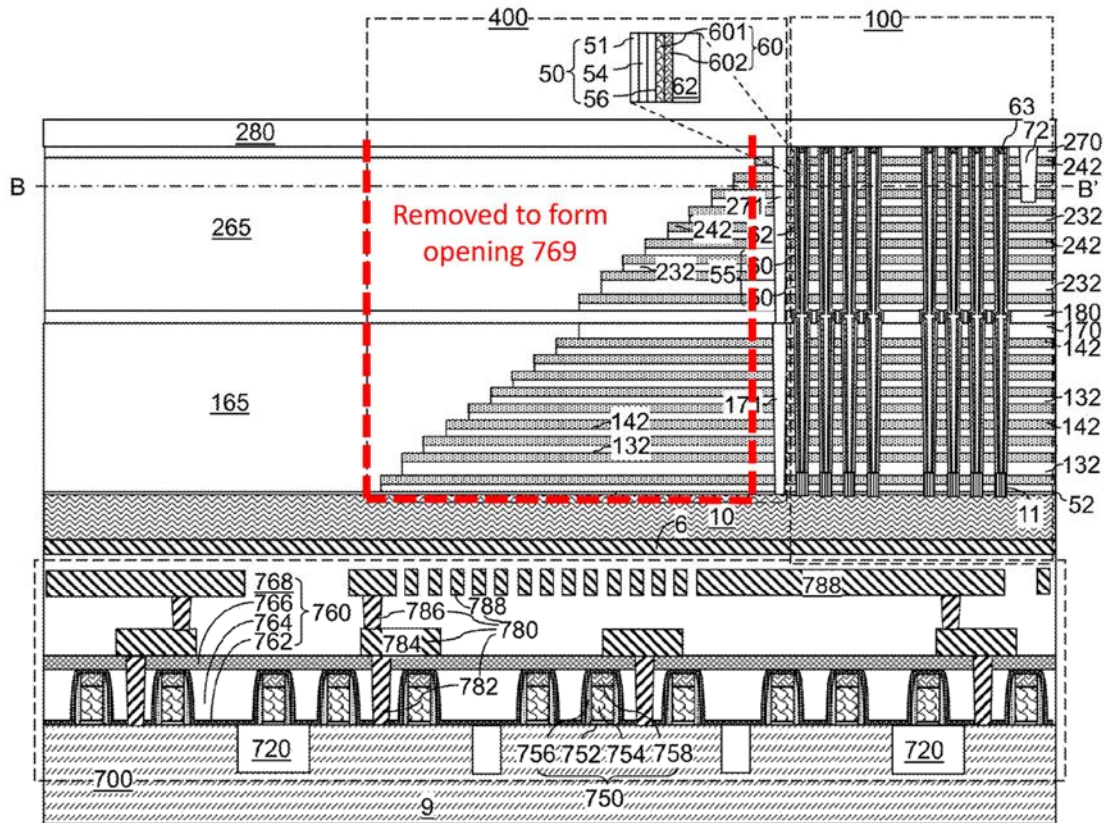


FIG. 10A

Ex. 1005, Fig. 10A (annotated), [0173], [0189]. Toyama then fills “opening 769” with “dielectric fill material portion 430.” Thus, Toyama’s first exemplary structure discloses this limitation.

[15.C.iii] “A dielectric structure ... wherein the alternating conductor/dielectric layer stack abuts a sidewall surface of the dielectric structure”

235. As highlighted in Fig. 15A below, Toyama discloses *a dielectric structure* (upper part of “dielectric fill material portion 430” in brown) *wherein the alternating conductor/dielectric layer stack* (“alternating stack (132, 146, 232, 246)”

in red) *abuts* (touches) *a sidewall surface of the dielectric structure* (sidewall (in blue) of upper part of “dielectric fill material portion 430”):

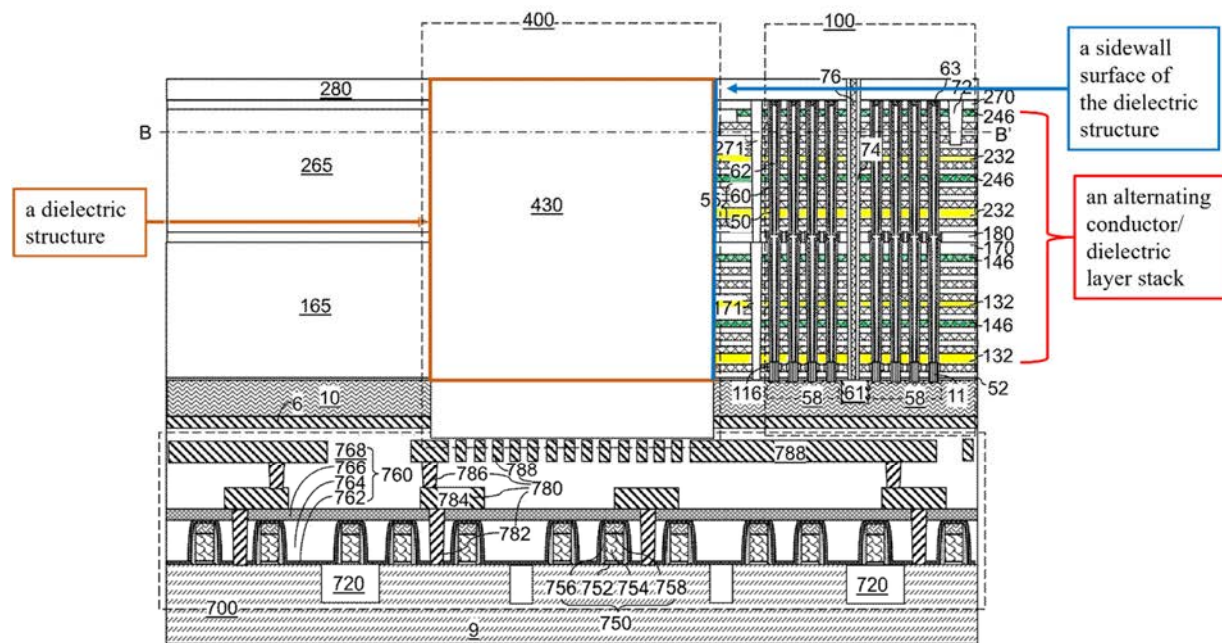


FIG. 15A

Ex. 1005, Fig. 15A (annotated).

[15.C.iv] “... wherein ... the dielectric structure is formed of a dielectric material”

236. As I discussed previously, the upper portion of Toyama’s “dielectric fill material portion 430” is the claimed *dielectric structure*. And Toyama discloses that “dielectric fill material portion 430 is formed ... for example, by deposition of a dielectric fill material.” Ex. 1005, [0216]. Accordingly, Toyama thus discloses *a dielectric structure* (upper part of “dielectric fill material portion 430”) *wherein the dielectric structure is formed of a dielectric material* (the “dielectric fill material” that forms “dielectric fill material portion 430”).

[15.D] “channel structures and slit structures extending vertically through the alternating conductor/dielectric layer stack;”

237. For ease of analysis, I separate this limitation into two sub-parts.
Toyama’s first exemplary structure and Second Embodiment disclose each sub-part.

[15.D.i] “channel structures ... extending vertically through the alternating conductor/dielectric layer stack”

i. First Exemplary Structure

238. In Toyama’s first exemplary structure, the “memory stack structures 55” are the claimed *channel structures*, and they *extend[] vertically through the alternating conductor/dielectric layer stack* (“alternating stack (132, 146, 232, 246)”) as shown in red in Fig. 17A below:

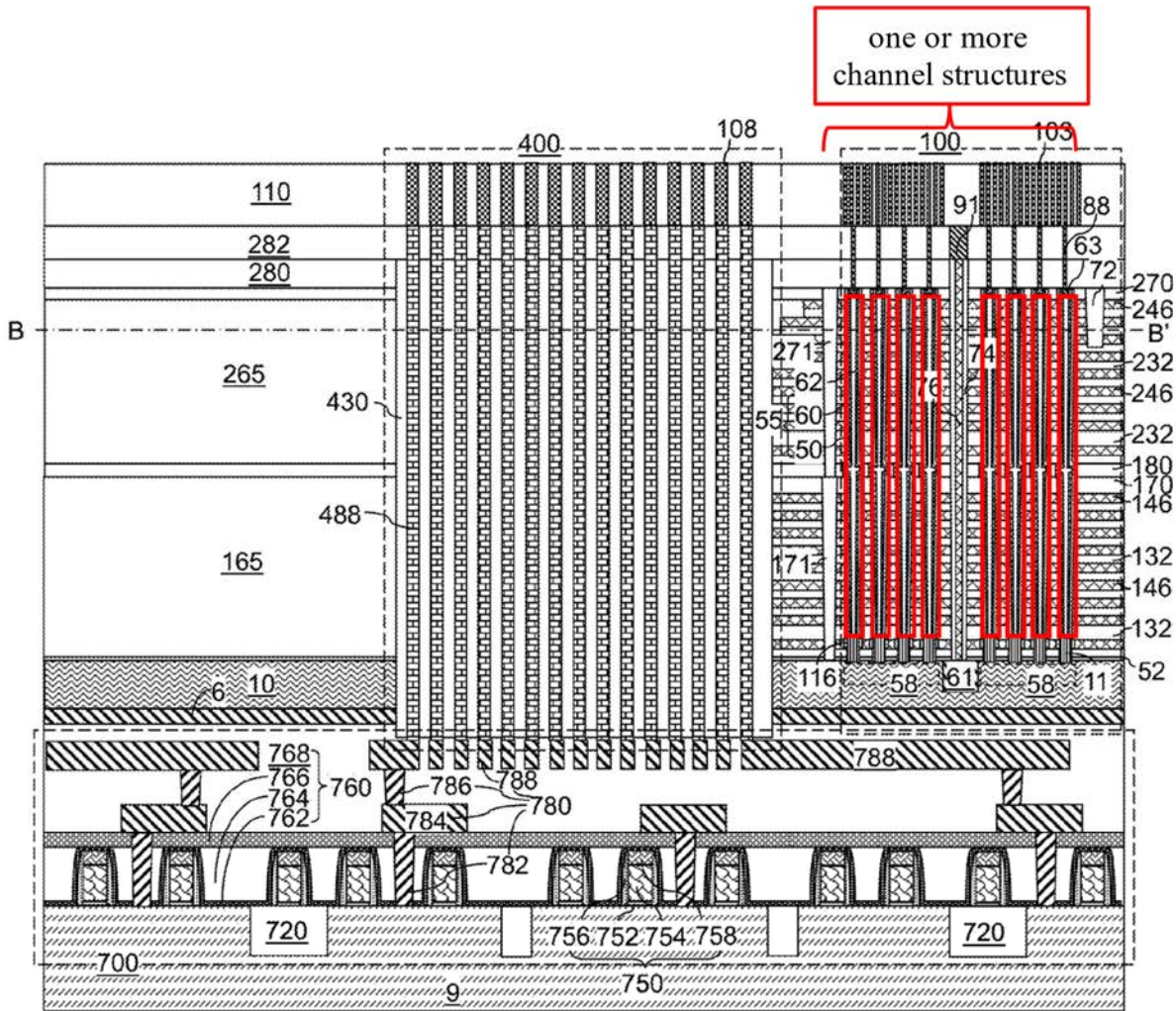


FIG. 17A

Ex. 1005, Fig. 17A (annotated). Toyama describes its “memory stack structures 55 vertically extending through the at least one alternating stack (132, 146, 232, 246).” *Id.*, [0232].

239. Even though the claim element places no other functional or structural requirements on the claimed *channel structures*, I note that Toyama’s “memory stack structures 55” perform the same function and are composed of the same

components as the channel structures in the '378 patent. With respect to function, both serves as memory elements. *Compare* Ex. 1001, 14:4-31 (“channel structure” includes a “memory film”) *with* Ex. 1005, [0388] (“The memory stack structures 55 can comprise memory elements of a vertical NAND device.”). And both are constructed from the same components. *Compare* Ex. 1001, 9:1-6 (“[c]hannel structure 216 is filled with semiconductor materials (e.g., as a semiconductor channel 218) and dielectric materials (e.g., as a memory film 220)”) *with* Ex. 1005, [0210] (“[e]ach of the memory stack structures 55 comprises a memory film 50 and a vertical semiconductor channel 60”). This supports my opinion that Toyama’s first exemplary structure discloses *channel structures* (“memory stack structures 55”) *extending vertically through the alternating layer stack* (“alternating stack (132, 146, 232, 246)”).

ii. Second Modification

240. Although the discussion above relates to Toyama’s first exemplary structure, it is equally applicable to Toyama’s Second Modification which meets this limitation for the same reasons. As shown below in Toyama Fig. 49, the *channel structures* (“memory stack structures 55”) *extend[]vertically through the alternating layer stack* (“alternating stack (132, 146, 232, 246)”).

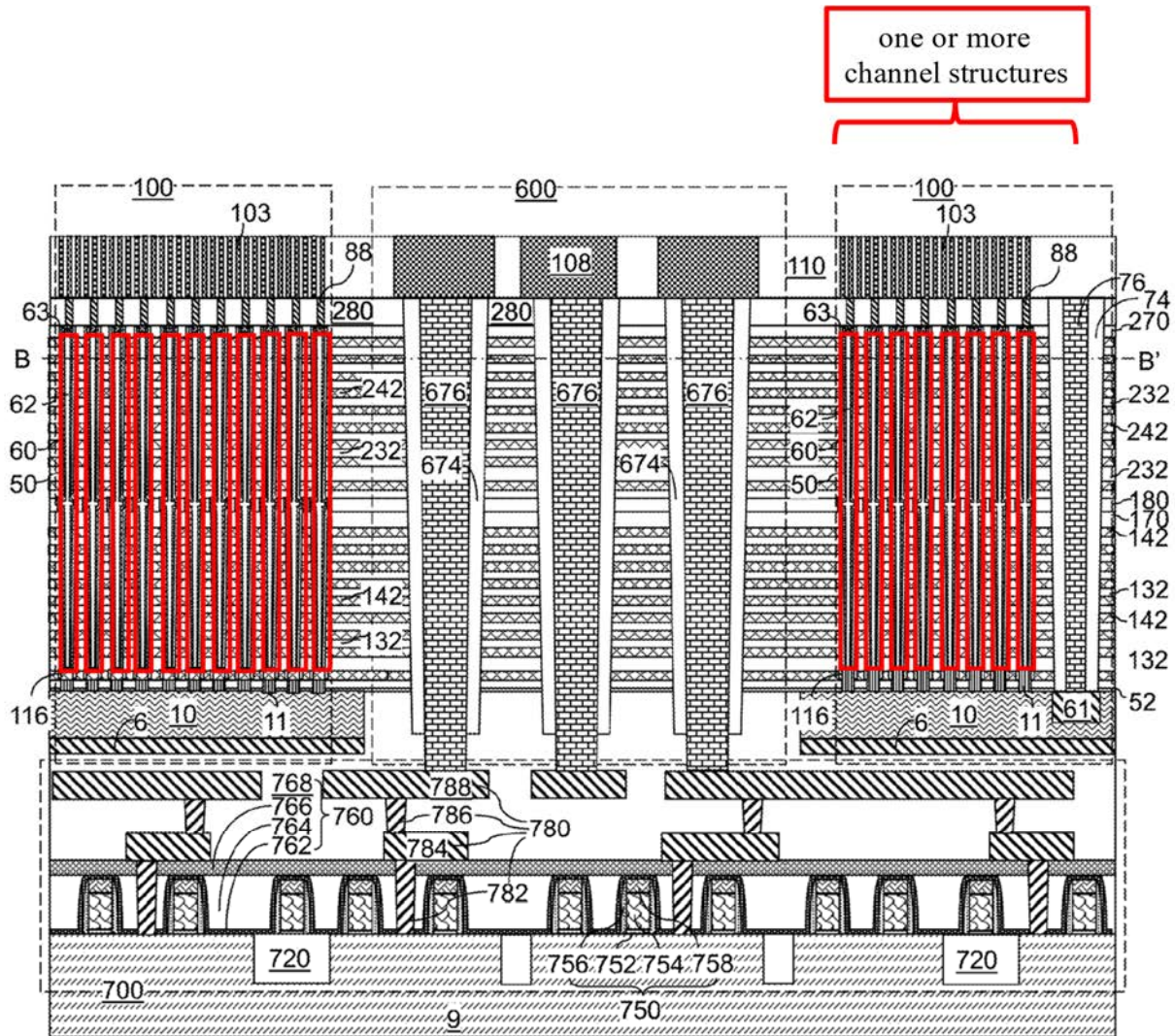


FIG. 49

Ex. 1005, Fig. 49 (showing “memory stack structures 55”).

[15.D.ii] “slit structures extending vertically through the alternating conductor/dielectric layer stack”

i. First Exemplary Structure

241. The claimed *slit structures* in Toyama’s first exemplary structure are the “laterally-elongated contact via structures 76,” and they *extend[] vertically*

through the alternating conductor/dielectric layer stack (“alternating stack (132, 146, 232, 246)”) as shown in Fig. 17A below:

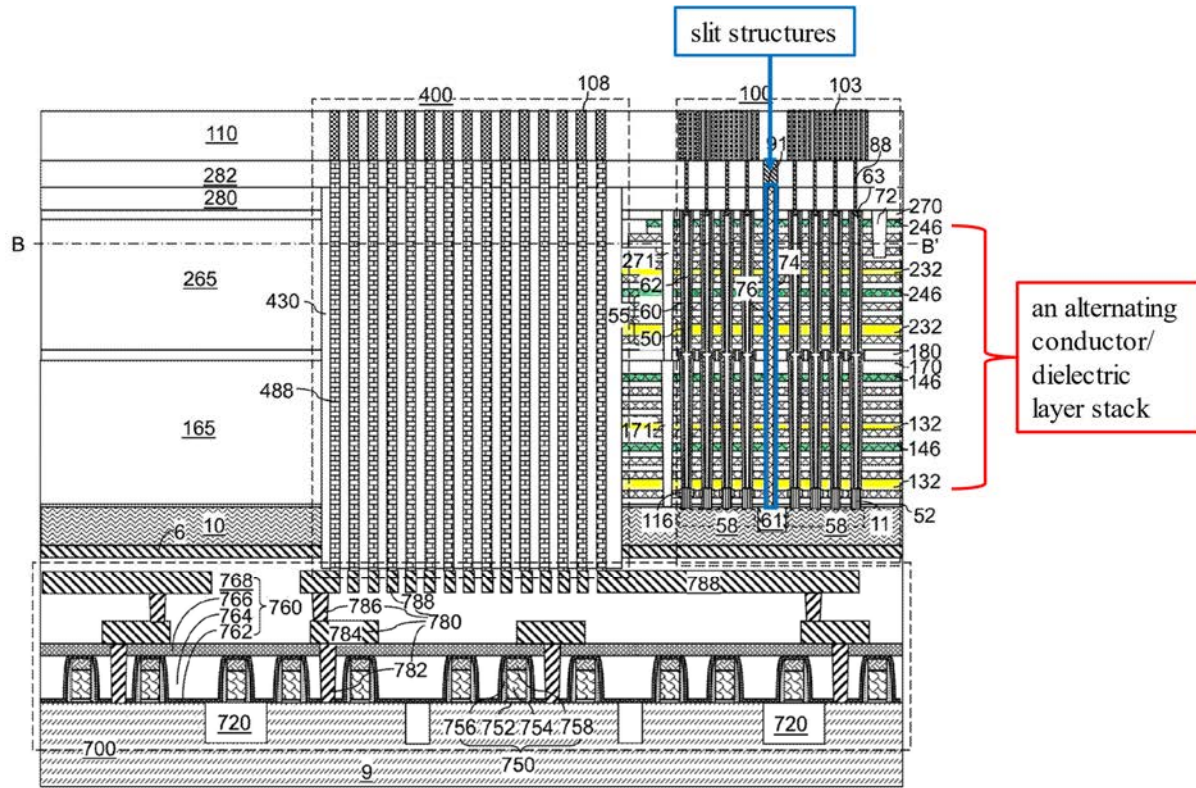
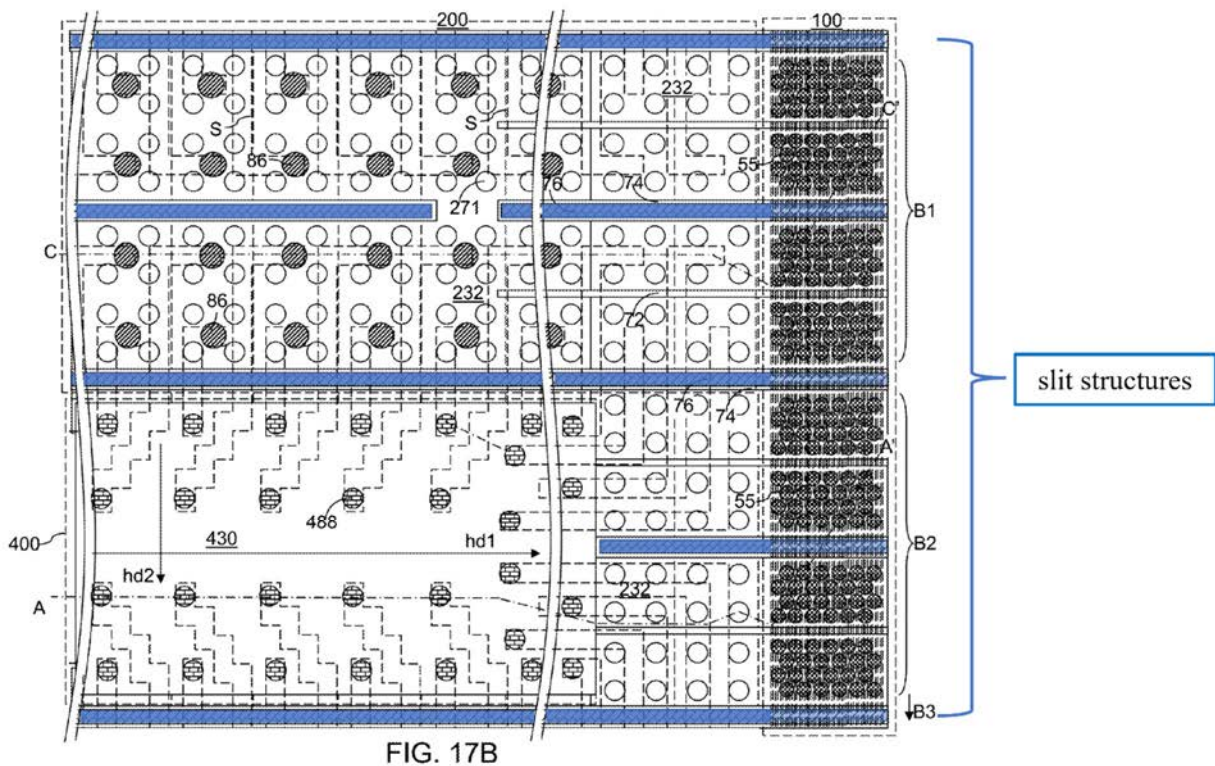


FIG. 17A

Ex. 1005, Fig. 17A (annotated). The lateral elongated shape of the “laterally-elongated contact via structures 76” *slit structures* is most easily observed in the top view of Fig. 17B:



Id., Fig. 17B (annotated). It is of no import that Toyama refers to the claimed *slit structures* as “laterally-elongated contact via structures 76.” Indeed, the plain meaning of “slit” is a laterally-elongated structure. See Ex. 1022, 4 (Merriam-Webster’s definition of “slit” as “a long narrow cut or opening”).

242. And, as can be seen in Toyama Fig. 17A above, Toyama “laterally-elongated contact via structure 76” *extend[s] vertically in the alternating layer stack* (“alternating stack (132, 146, 232, 246)”), as required by the claim.

243. Even though the claim places no functional limitation on the “slit structure,” Toyama’s “laterally-elongated contact via structures 76” perform the same function as the ’378 patent’s “slit structures.” The ’378 specification explains

that each “slit structure 226 acts as a source contact for NAND strings 204.” Ex. 1001, 9:63-67. Likewise, Toyama’s “laterally-elongated contact via structures 76” serves as “source connection[s].” Ex. 1005, [0241]. And the *slit structures* in Toyama and the ’378 patent both define memory “blocks” in their respective 3D memory arrays. *Compare* Ex. 1001, 9:52-54 (“[s]lit structures 226 ... extend along the y-axis to separate alternating conductor/dielectric stack 210 into multiple blocks.”) *with* Ex. 1005, [0237] (“laterally-elongated contact via structures 76 laterally extend along the first horizontal direction ... and laterally divide the at least one alternating stack ... into a plurality of laterally spaced-apart blocks.”). This reinforces my opinion that Toyama’s first exemplary embodiment meets the claim language.

ii. Second Modification

244. Although the discussion above relates to Toyama’s first exemplary structure, it applies equally to Toyama’s Second Modification and meets this limitation for the same reasons. As shown below in Fig. 49, Toyama’s “laterally-elongated contact via structures 76” are the claimed *slit structures* and they *extend[] vertically through the alternating conductor/dielectric layer stack* (“alternating stack (132, 146, 232, 246)”).

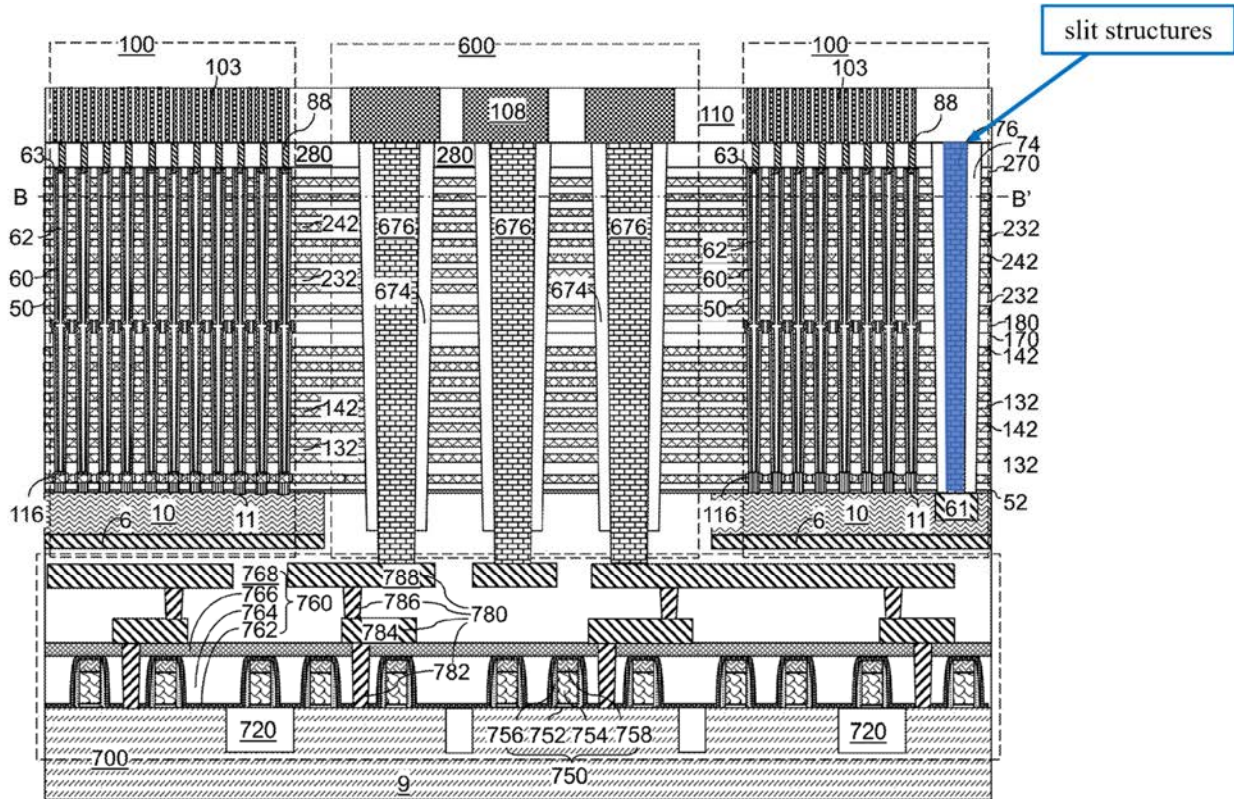


FIG. 49

Ex. 1005, Fig. 49 (annotated) (showing “laterally-elongated contact via structures 76”). In this regard, it is important not to mistake the structure 676 (in the middle of the figure) for the “laterally-elongated contact via structures 76” (on the right hand side of the figure).

[15.E] “a staircase structure disposed in the alternating conductor/dielectric layer stack, wherein the staircase structure comprises levels with each level having a conductor layer thereon;”

i. First Exemplary Structure

245. The “staircase region” highlighted in Toyama Fig. 17C below is *a staircase structure* that is *disposed in the alternating conductor/dielectric layer stack* (“alternating stack (132, 146, 232, 246)”). Moreover, *the staircase structure*

(“staircase region”) *comprises levels with each level having a conductor layer*
(“electrically conductive layers 146, 246”) *thereon*:

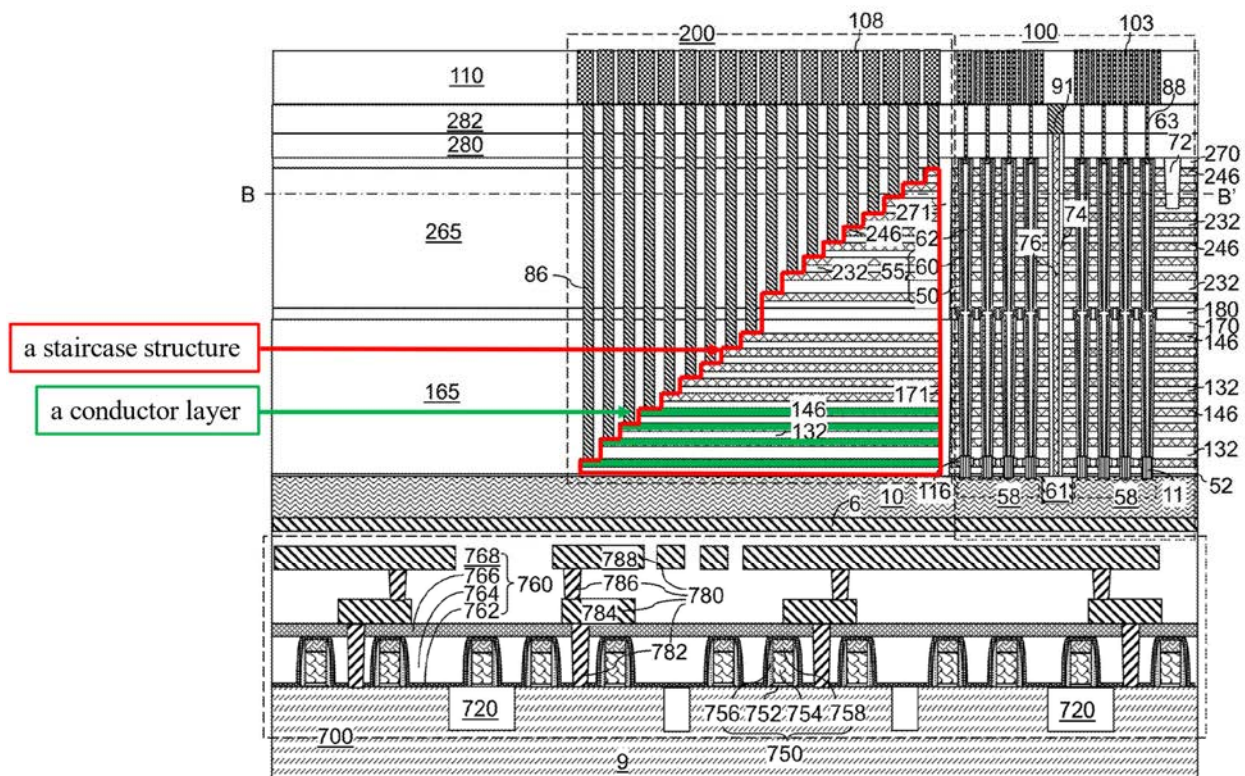


FIG. 17C

Ex. 1005, Fig. 17C (annotated). Toyama explains that “[t]he at least one alternating stack (132, 146, 232, 246) comprises staircase regions that include terraces in which each underlying electrically conductive layer (146, 246) extends farther along the first horizontal direction hd1 than any overlying electrically conductive layer (146, 246).” *Id.*, [0232].

ii. Second Modification

246. While the discussion above was in the context of Toyama's first exemplary structure, a POSITA would have understood that Toyama's Second Modification also teaches this limitation for substantially the same reasons. With respect to Toyama's fourth exemplary structure (to which the Second Modification pertains), Toyama notes that "word line contact via structures [86] can be formed as in the first through third embodiments." Ex. 1005, [0322]. Recall that the word line contacts are in Toyama's staircase region. *See id.*, Fig. 17C, [0243]. Thus, although not explicitly depicted in Figs. 44-49, a POSITA would therefore have understood that Toyama's fourth exemplary structure (and modifications thereof including the Second Modification) includes *a staircase structure* ("staircase regions").

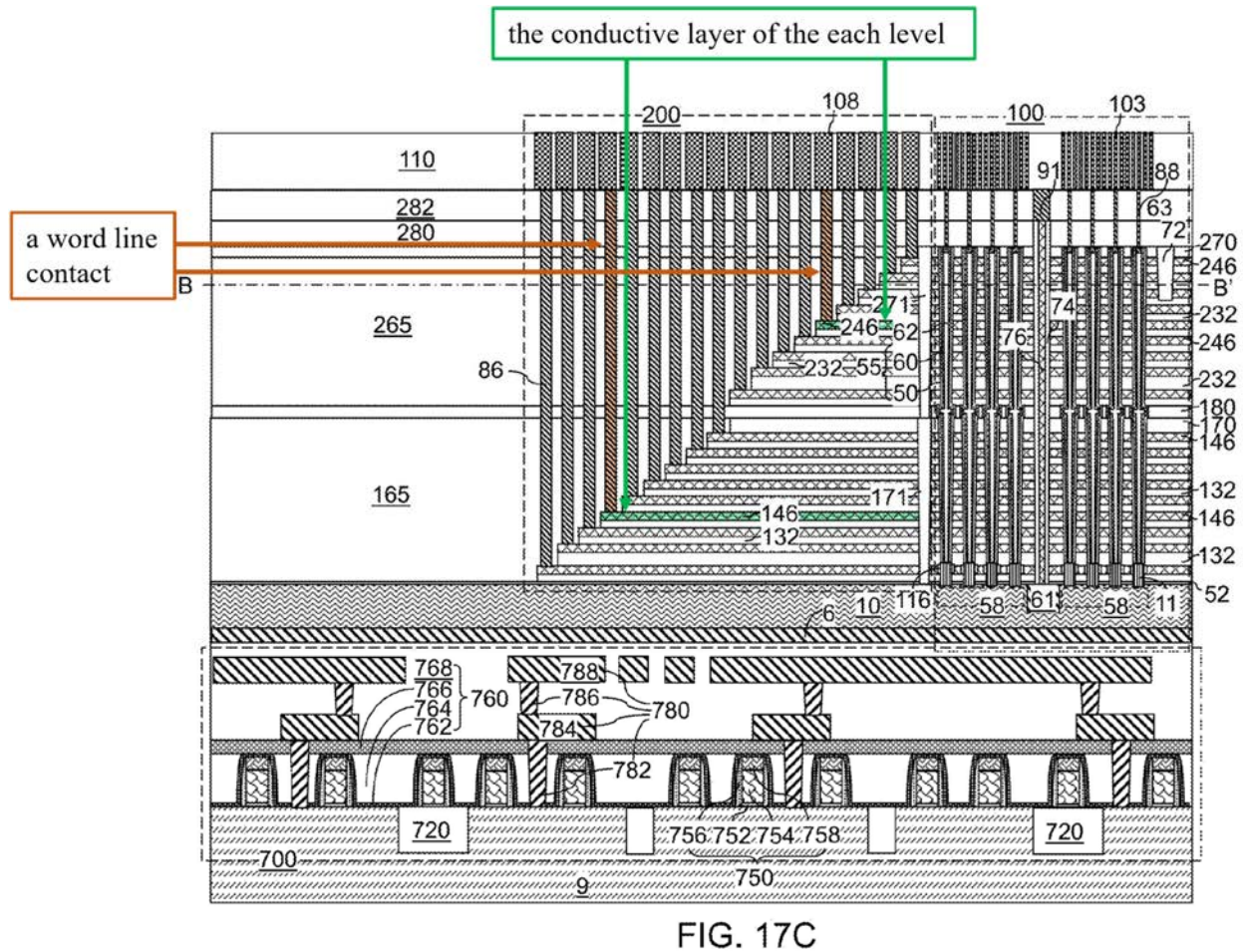
247. At a minimum, it would have been obvious to a POSITA to use a staircase structure ("staircase regions") in Toyama's Second Modification. For the memory device to be functional, a POSITA would have understood that there needed to be some way to transmit signals to the "electrically conductive layers (146, 246)," because these layers serve as the word lines for accessing (*e.g.*, reading, writing, and erasing) the memory elements in the channel structures. Ex. 1005, [0323]. And it would have been obvious to a POSITA to use the well-known *staircase structure* ("staircase regions") architecture to provide access to Toyama's word lines. Not only is this true in view of the knowledge of a POSITA, but also in view of the

teachings in Toyama itself regarding its first, second, and third exemplary structures, from which the Second Modification derives. *See, e.g., id.*, Fig. 17C.

[15.F] “a word line contact disposed on the conductor layer of the each level;”

i. First Exemplary Structure

248. As shown below, Toyama discloses *a word line contact* (“word line contact via structures 86”) *disposed on the conductor layer of the each level* (“electrically conductive layers (146, 246)”). Note that only representative examples are highlighted to avoid cluttering the image.



Ex. 1005, Fig. 17C (annotated); *id.*, [0260] (“[W]ord line contact via structures 86 ... can contact respective portions of electrically conductive layers (146, 246)”).

ii. Second Modification

249. While the discussion above was in the context of Toyama’s first exemplary structure, a POSITA would have understood that Toyama’s Second Modification also teaches this limitation for substantially the same reasons. Toyama notes that the *word line contacts* (“word line contact via structures”) in its fourth exemplary structure (of which the Second Modification is a part) “can be formed as

in the first through third embodiments.” Ex. 1005, [0322]. Thus, my analysis for the first exemplary structure applies equally here.

250. At a minimum, a POSITA would have found it obvious to transmit signals to electrically conductive layers (146, 246) in the “staircase regions” using “word line contact via structures” for the reasons I explained relative to claim element [15.E].

[15.G] “local contacts disposed on the channel structures and the slit structures; and”

251. Toyama’s first exemplary structure and its Second Modification each disclose this element. Before turning to my analysis, I first note that the ’378 patent teaches that “[i]n some embodiments, 3D memory device 200 includes a plurality of ‘local contacts.’” Ex. 1001, 11:16-17. “The contacts are referred to herein as ‘local contacts’ because they are in direct contact with the memory array structures, and further because they are formed within dielectric layer 230.” *Id.*, 11:20-24.

i. First Exemplary Structure

252. The “drain contact via structures 88” in Toyama’s first exemplary structure are the claimed *local contacts*, that are *disposed on* (in contact with or extending above) *the channel structures* (“memory stack structures 55”), and Toyama’s “source connection via structures 91” are the *local contacts* that are *disposed on* (in contact with or extending above) *the slit structures* (“laterally-elongated contact via structures 76”), as shown in Fig. 17A below:

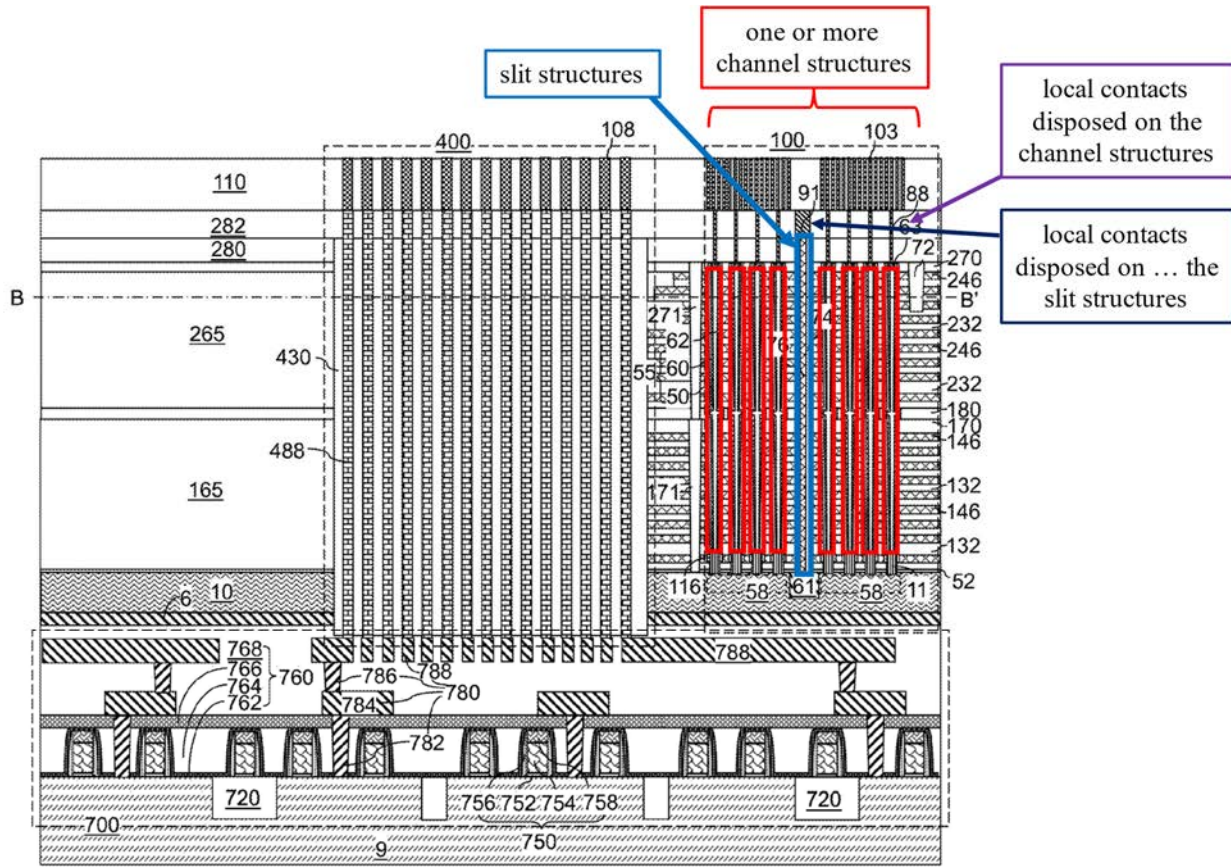


FIG. 17A

Ex. 1005, Fig. 17A (annotated); *id.*, [0251] (“The bit lines 103 are formed over the memory-level assembly, and are electrically coupled to nodes (e.g., drain regions 63) of the memory stack structures 55 by the drain contact via structures 88.”); *id.*, [0241] (“A source connection via structure 91 can extend through the contact level dielectric layers (280, 282) to provide electrical connection to the laterally-elongated contact via structures 76.”).

ii. Second Modification

253. Although the discussion above was in the context of Toyama's first exemplary structure, Toyama's Second Modification also teaches (or, at the very

least renders obvious) this limitation for substantially the same reasons. Toyama's "drain contact via structures 88" in the Second Modification are the *local contacts* that are *disposed on the channel structures* ("memory stack structures 55"). Ex. 1005, Fig. 49, [0342] ("drain contact via structures 88 ... can be formed as in the first through third embodiments").

254. Toyama Fig. 49 (showing the cross-section of the Second Modification) does not expressly illustrate that "source connection via structures 91" are used to connect to "laterally-elongated contact via structures 76," but a POSITA would have understood the Second Modification to include *local contacts disposed on the slit structures* ("source connection via structures 91"). The fact that Fig. 49 does not show any connection to Toyama's "laterally-elongated contact via structures 76" appears to merely be an artifact of where the cross-section was taken. Indeed, in describing the Second Modification, Toyama notes that "[t]he metal interconnect structures can include ... source connection line structures (not shown)." Ex. 1005, [0342]. Because Toyama's *slit structures* are "**laterally-elongated** contact via structures 76," they extend some length in the horizontal direction. As such, there is no need to have a single, continuous local contact that spans the entire length of the slit. Rather, a POSITA would have understood that periodic/intermittent local contacts would suffice. This explains why a particular cross-section (such as Fig.

49) does not illustrate the local contacts. But taking a cross-section at a different location would reveal such contacts.

255. As Toyama's expressly states in connection with its first exemplary structure, "source connection line structures 101 ... contact the source connection via structures 91 to provide electrically conductive paths for biasing the source region 61 through the laterally-elongated contact via structures 76." Ex. 1005, [0250]. A POSITA would thus have understood that the Second Modification, which expressly includes "source connection line structures," "source region 61," and "laterally elongated contact via structure 76," also includes "source connection via structures." Thus, Toyama discloses *local contacts* ("source connection via structures 91") *disposed on the slit structures* ("laterally-elongated contact via structures 76") in the context of the Second Modification.

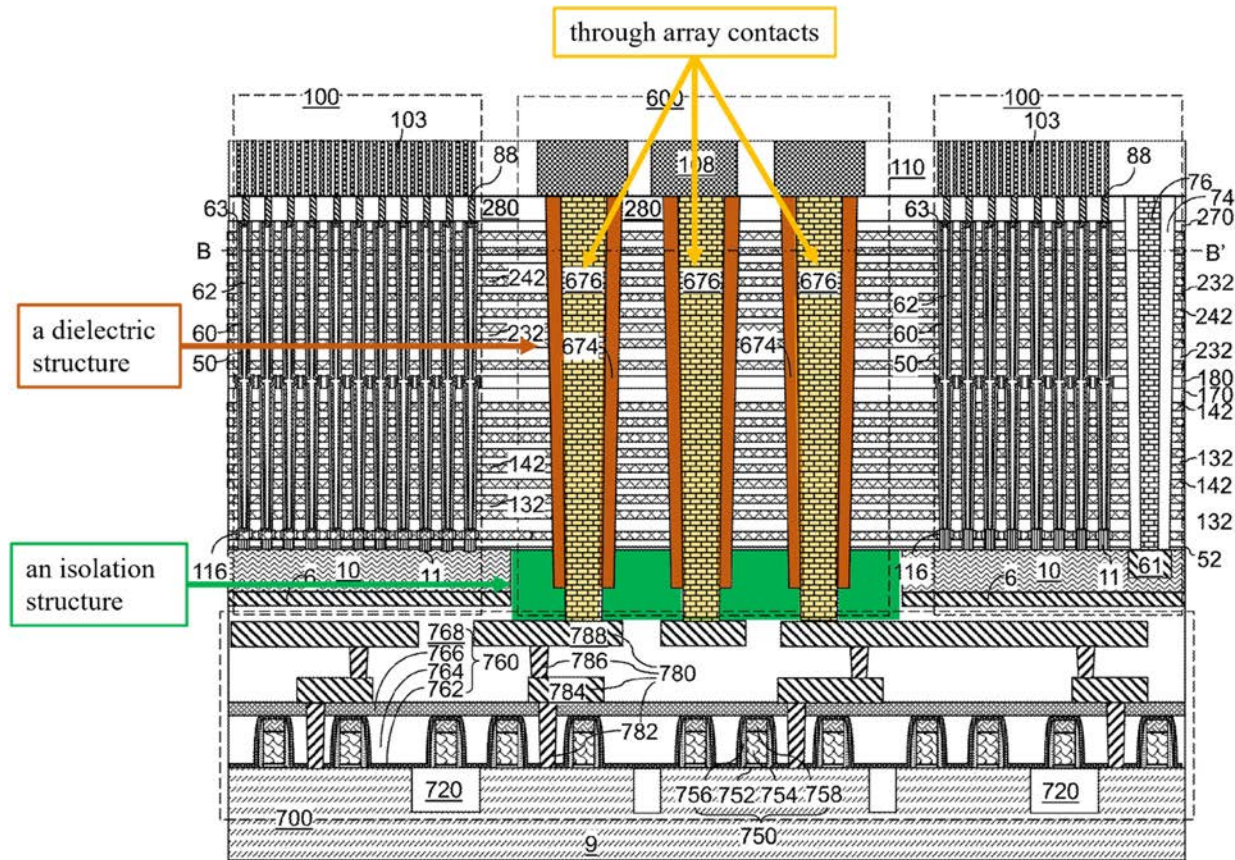
256. At a minimum, it would have been obvious to a POSITA to use *local contacts* ("source connection via structures 91") *disposed on the slit structures* ("laterally elongated contact via structure 76"). To begin, a POSITA would have understood that "laterally-elongated contact via structures 76" function as the source lines for "source regions 61" in Toyama's Second Modification. Ex. 1005, [0382]. And a POSITA would have further known that "via structures 76" require a higher-level source connection to serve their purpose. Given Toyama's express disclosure in other embodiments of "source connection via structures 91" for the same purpose,

a POSITA would have been motivated to implement “source connection via structures 91” in the Second Modification (which is largely derivative of Toyama’s first, second, and third exemplary structures). Similarly, given Toyama’s express disclosure in other embodiments of using “source connection via structures 91” for the same purpose, a POSITA would have had a reasonable expectation of success in using the same (or substantially identical) manufacturing steps (which as discussed in Section VI were very well-known) to create local contacts on Toyama’s slit structures in its Second Embodiment. This is even more the case because Toyama’s Second Embodiment is largely derivative of Toyama’s first, second, and third embodiments, which expressly disclose local contacts on slit structures.

[15.H] “through array contacts (TACs) extending vertically through the dielectric and the isolation structures.”

i. Second Modification

257. In Toyama’s Second Modification, the “through-memory-level via structures 676” are the claimed *through array contacts*. And, as can be seen in Fig. 49 below, *they extend[]vertically through the dielectric and the isolation structures* (respectively shown in red and green below).



Ex. 1005, Fig. 49 (annotated); [0341]-[0342].

258. As discussed for claim element [15.C], “insulating liners 674” are individually and collectively *the dielectric structure* in Toyama’s Second Modification. And as discussed for claim element [15.A.ii], the insulating material layer that fills “opening 151” is *the isolation structure* in Toyama’s Second Modification.

259. Like water that travels *through* a hose or a pipe that extends *through* a wall, Toyama’s “through-memory-level via structures 676” extend *through* “insulating liners 674,” and the insulating material layer that fills “opening 151.”

Thus, Toyama discloses *through array contacts* (“through-memory-level via structures 676”) *extending vertically through the dielectric* (“insulating liners 674”) *and isolation* (the insulating material layer that fills “opening 151”) *structures*. Ex. 1005, [0340]-[0342].

ii. First Exemplary Structure

260. In Toyama’s first exemplary structure, “through-memory-level via structures 488” are the *through array contacts (TACs)*, as shown in Fig. 17A below.

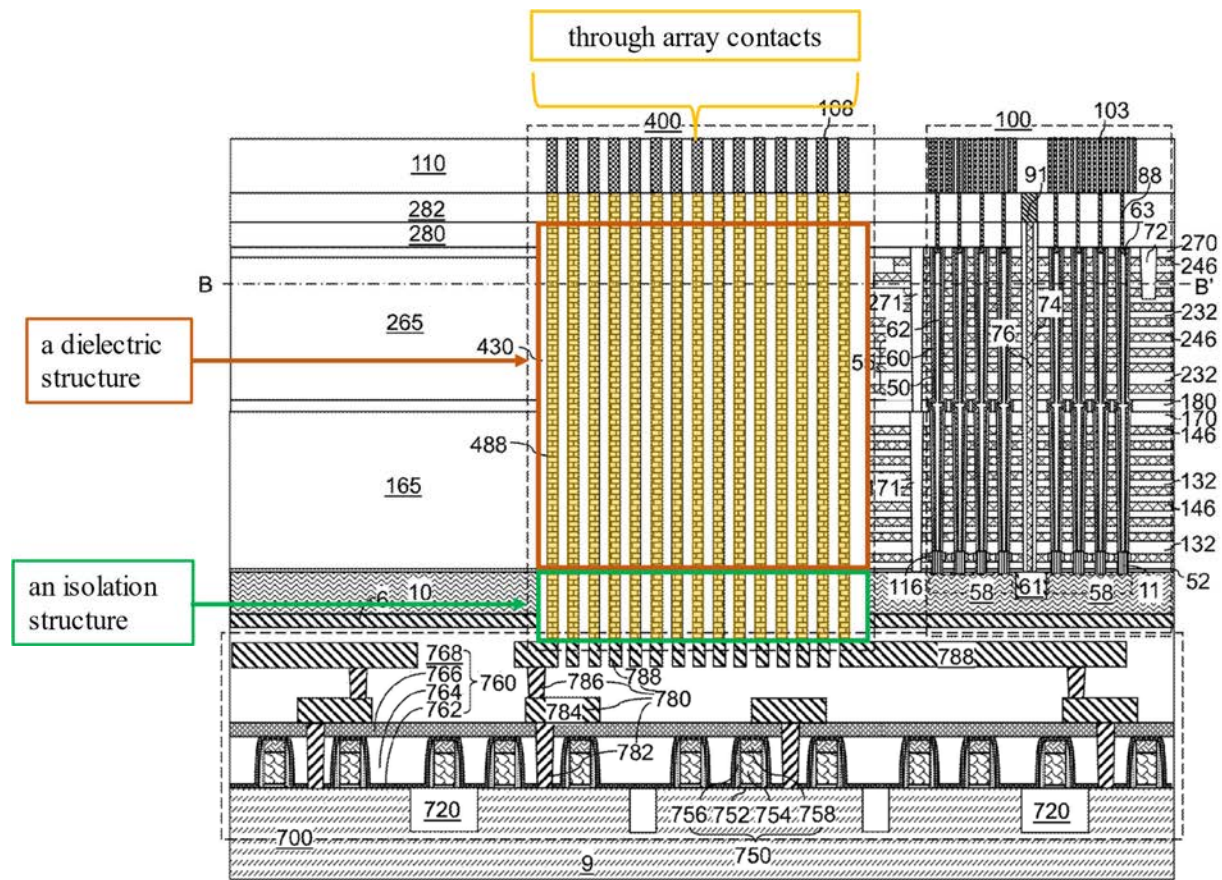


FIG. 17A

Ex. 1005, Fig. 17A (annotated); *id.*, [0239].

261. As I discussed for element [15.C], in Toyama’s first exemplary structure the upper part of “dielectric fill material portion 430” is *the dielectric structure*. And as I discussed for element [15.A.ii], the lower part of Toyama’s “dielectric fill material portion 430” is *the isolation structure* in Toyama’s first exemplary structure.

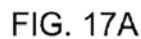
262. Accordingly, Toyama’s first exemplary structure discloses *through array contacts* (“through-memory-level via structures 488”) *extending vertically through the dielectric* (upper part of “dielectric fill material portion 430”) *and isolation* (lower part of “dielectric fill material portion 430”) *structures*. Ex. 1005, [0239].

9. Claim 18

[18.Pre] “The 3D memory device of claim 15, further comprising:” [18.A] “an etch stop plug interposed between each local contact of the local contacts and each channel structure of the channel structures; and”

263. As I explained in limitations [15.D] and [15.G], Toyama discloses—both in its Second Modification and in its first exemplary structure—*channel structures* (“memory stack structures 55”) *and local contacts disposed on the channel structures* (“drain contact via structures 88”).

264. As the below figure shows, Toyama teaches or at the very least renders obvious *an etch stop plug* (“drain regions 63”) *interposed between each local contact*

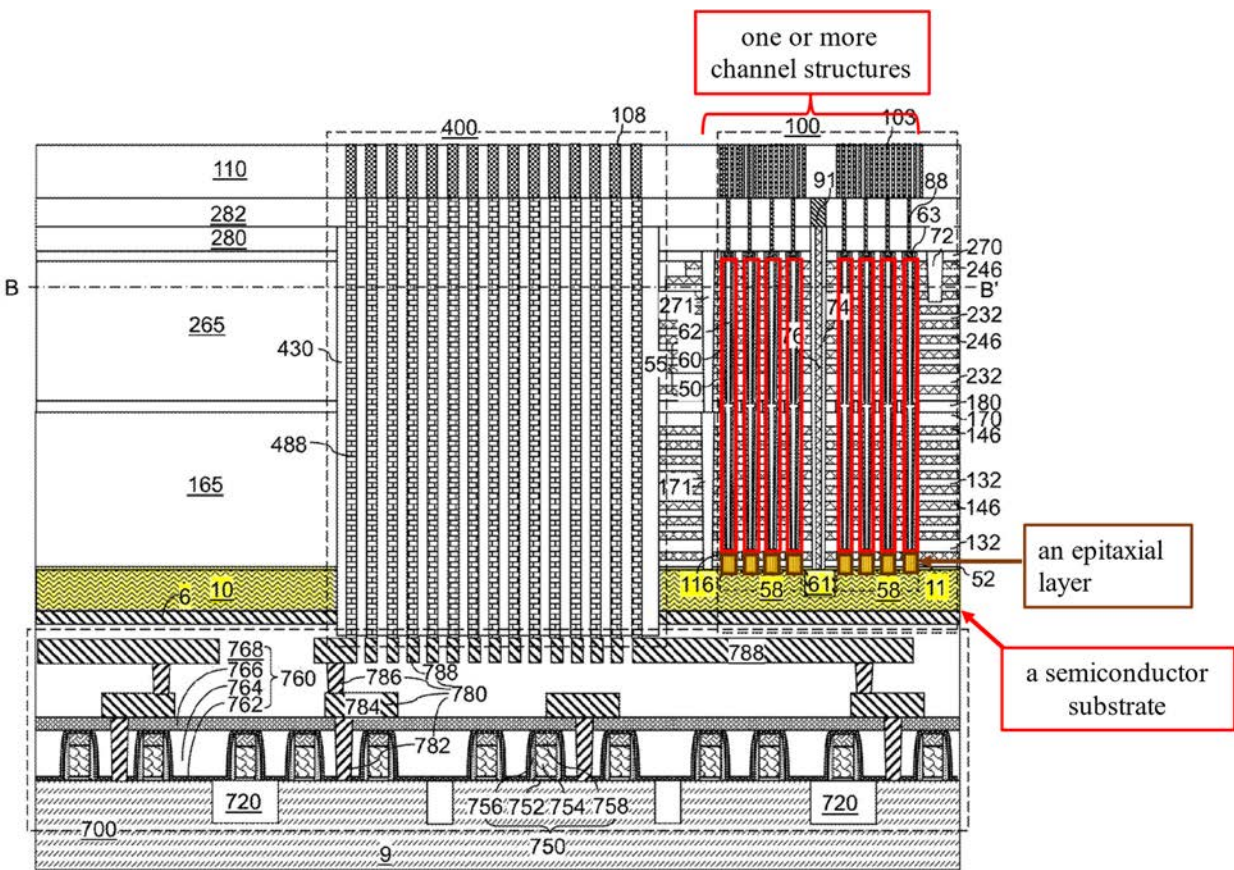


265. Each of “drain regions 63” is *an etch stop plug* for the reasons I explained in limitation [1.G]. The minor wording differences between this limitation and limitation [1.G] do not alter my analysis or opinions.

266. Although Figure 17A pertains to Toyama’s first exemplary structure, Toyama’s Second Modification also discloses this limitation for the same reason. *Id.*, Figure 49 (also including “drain regions 63”).

[18.B] “an epitaxial layer disposed between the channel structures and the substrate.”

267. As I explained in limitations [15.A] and [15.D], Toyama’s “memory stack structures 55” are *channel structures*, and Toyama’s “planar semiconductor material layer 10” is *a substrate*. As the below figure shows, Toyama teaches *an epitaxial layer* (“pedestal channel portions 11”) *disposed between the channel structures* (“memory stack structures 55”) *and the substrate* (“planar semiconductor material layer 10”):



Ex. 1005, Fig. 17A (annotated); *id.*, [0208].

268. “Pedestal channel portions 11” are an epitaxial layer for the reasons I explained for limitation [1.F]. The minor wording differences between this limitation and limitation [1.F] do not alter my analysis or opinions.

269. Although Figure 17A pertains to Toyama’s first exemplary structure, Toyama’s Second Modification also discloses this limitation for the same reason. *Id.*, Figure 49 (also including “pedestal channel portions 11”).

C. Secondary Considerations of Non-Obviousness

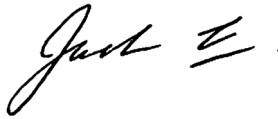
270. Based on my review of the ’378 patent’s file history, I note that no secondary considerations of non-obviousness were identified in connection with the patent’s claims. Nor am I otherwise aware of any evidence of commercial success, skepticism, failure of others, industry praise, unexpected results, or the like relating to the ’378 patent. Instead, as discussed above, it is my opinion that the subject matter embraced by the challenged claims was known in and obvious over the prior art.

Petition for *Inter Partes* Review of U.S. Patent No. 10,658,378
Declaration of Dr. Jack C. Lee

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willfully false statements and the like so made are punishable by fine or imprisonment, or both, under its 1101 of Title 18 of the United States Code.

Date: May 19, 2024

Location: Austin TX

Signature: 
DR. JACK C. LEE