

Three-Dimensional NAND Flash Architecture Design Based on Single-Crystalline STacked ARray

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Abstract—Various critical issues related with 3-D stacked NAND Flash memory are examined in this paper. Our single-crystalline STacked ARray (STAR) has many advantages such as better scalability, possibility of single-crystal channel, less sensitivity to 3-D interference, stable virtual source/drain characteristic, and more extendability over other stacked structures. With STAR, we proposed a unit 3-D structure, i.e., “building.” Then, using this new component, 3-D block and full chip architecture are successfully designed. For the first time, the structure and operation methods of the “full” array are considered. The fully designed 3-D NAND Flash architecture will be the novel solution of reliable 3-D stacked NAND Flash memory for terabit density.

Index Terms—Channel-channel (Ch-Ch) coupling, single-crystalline STacked ARray (STAR), 3-D memory, 3-D block, 3-D stacked NAND Flash memory.

I. INTRODUCTION

AS THE MARKET size of NAND Flash memory is exploding with extensive applications such as smart phone, tablet PC, and solid-state drive, the need for low bit cost and ultrahigh density is increasing. However, many challenges (e.g., limitation of lithography technology, short-channel effects, decreased number of stored electrons, and floating-gate coupling) impede further scaling of planar NAND Flash technology beyond a 20-nm design rule. Thus, the 3-D stacked NAND Flash memory devices [1]–[6] have caught great attention as a solution.

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There are some important issues related with 3-D stacked NAND Flash memory as follows.

- 1) Stack type: There are two types of 3-D stacked NAND Flash architecture. One is the gate stack type (pipe-shaped bit cost scalable (P-BiCS) [1] and terabit cell array transistor (TCAT) [2]), and the other is the channel stack type (vertical gate (VG) NANDs [3], [4]).
- 2) Unit cell structure: The channel material [polycrystalline silicon (poly-Si) or single-crystalline Si] and the gate structure [double-gate or gate-all-around (GAA)] are important issues that can determine operation performance. In our previous work [5], we successfully fabricated STacked ARray (STAR) having a single-crystalline channel and GAA structure. In this paper, we conclude that the STAR is a very promising structure for 3-D stacked NAND Flash memory.
- 3) Full array structure and operation scheme: The full array structure and its operation scheme are the critical issues of 3-D stacked NAND Flash memory. For the first time, we designed 3-D NAND Flash architecture based on the viewpoint of a “full” array. By introducing the 3-D metal line and concept of the “building” with an improved structure, the designed architecture is able to use conventional NAND operation scheme without degradation of performance throughput and penalty of memory density.

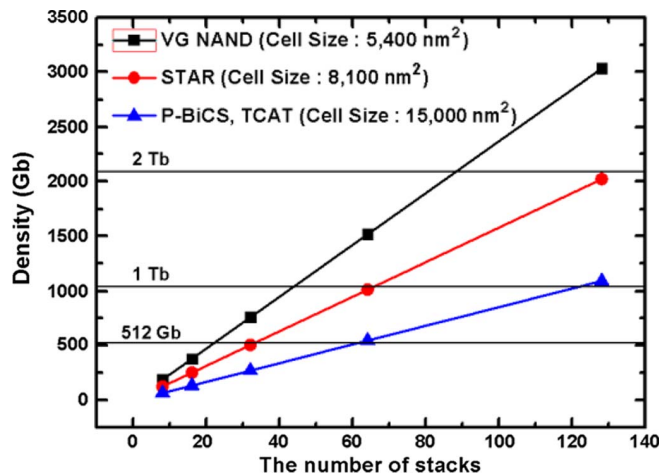
In this paper, we demonstrated the suitability and superiority of STAR for 3-D stack NAND Flash memory through the systematic comparison and examination by using 3-D TCAD simulation (ATLAS from SILVACO). Finally, we proposed 3-D NAND architecture featuring a single-crystalline STAR, including structure, operation, and process methods.

II. COMPARISON BETWEEN THE GATE STACK TYPE AND THE CHANNEL STACK TYPE

Fig. 1 summarizes the comparison between the gate stack type and the channel stack type. The minimal unit cell size for the gate stack type (P-BiCS and TCAT) should be around $6F^2$ because of the “word line (WL)-cut” process [1], [2]. In addition, since polychannel and core filler are plugged in the punched deep hole for the macaroni channel structure in P-BiCS and TCAT, the possible minimal feature size is ~ 50 nm. Consequently, the unit cell size of the gate stack type can be estimated as $15\,000\text{ nm}^2$. On the other hand, the unit cell size of channel stack type is smaller than that of gate stack type

	Gate Stack Type		Channel Stack Type	
	P-BiCS [1]	TCAT [2]	VG NAND [4]	STAR [5]
Structure				
Unit Cell Size				
Device Structure	Macaroni & GAA	Macaroni & GAA	Double Gate	Gate-All-Around
Channel	Macaroni poly-Si channel	Macaroni poly-Si channel	poly-Si channel	Single-Crystalline channel
Limitation of the number of stacks	Low read current	Low read current	No degradation of read current	No degradation of read current

Fig. 1. Summary of gate stack type and channel stack type.

Fig. 2. Memory density trend of various 3-D stacked NAND Flash architectures. The gate stack type (P-BiCS and TCAT) can be realized for 1-Tb density with ~ 120 layers. The VG NAND and STAR (channel stack type) can achieve a 1-Tb density with ~ 45 layers and ~ 65 layers, respectively.

because top layout resembles the conventional planar NAND Flash memory [6]. If we assume that the physical thickness of Oxide/Nitride/Oxide (O/N/O) gate dielectrics is 20 nm and the minimal feature size is 30 nm, then the possible minimal unit cell size of channel stack type will be 5400 nm² (VG NAND) or 8100 nm² (STAR). The unit cell size of STAR is larger than that of VG NAND because O/N/O gate dielectric layers are formed along oxide buttress during damascene gate process [5]. As shown in Fig. 2, the channel stack-type NAND Flash architecture has a large memory density with smaller stacked layers than gate stack.

As the number of stacks increases, more notable differences between the gate stack type and the channel stack type can be found. Therefore, we can conclude that the channel stack type can attain terabit density more quickly.

In the channel stack type, a single-crystalline Si channel can be used using the Si/SiGe epitaxial growth process [5]–[7]. The gate stack type, on the other hand, uses only poly-Si as a channel material since the epitaxial growth in the narrow deep hole is very difficult. Therefore, the channel stack-type NAND Flash memory having the single-crystalline channel is expected to have better performance such as uniform threshold voltage distribution and stable bit-line (BL) current than the gate stack-type one.

The other criterion is extendability. The gate stack type has the limitation of the number of stacked layers due to an inherent vertical channel structure. NAND Flash architecture consists of strings of a number of storage devices. Long BL strings reduce the overhead BL transistors and increase the package density, however, at the expense of higher overall resistance and, consequently, lower read current. The number of WLs in a BL string has increased from 16 to 32 and now to 64 in recent nodes. According to the International Roadmap for Semiconductors [8], BL strings will stay at 64 owing to read current drivability. Accordingly, it is difficult to stack the gate layers over 64 in gate stack type (32 in P-BiCS). To overcome this limitation and achieve a terabit-level density with over 120 stacked layers, the gate stack type should solve the degradation of read current drivability by additional architecture design. On the other hand, the read current drivability of the channel stack type is independent of the number of stacks. In addition, the total number of cells in one WL in the channel stack-type NAND has no limitation. Therefore, the channel stack-type architecture can be extended without limitation of the number of stacks.

To sum up, the channel stack type has smaller unit cell size, better performance with single-crystal channel, and more extendability. Therefore, we adopted the channel stack type for the 3-D NAND design.

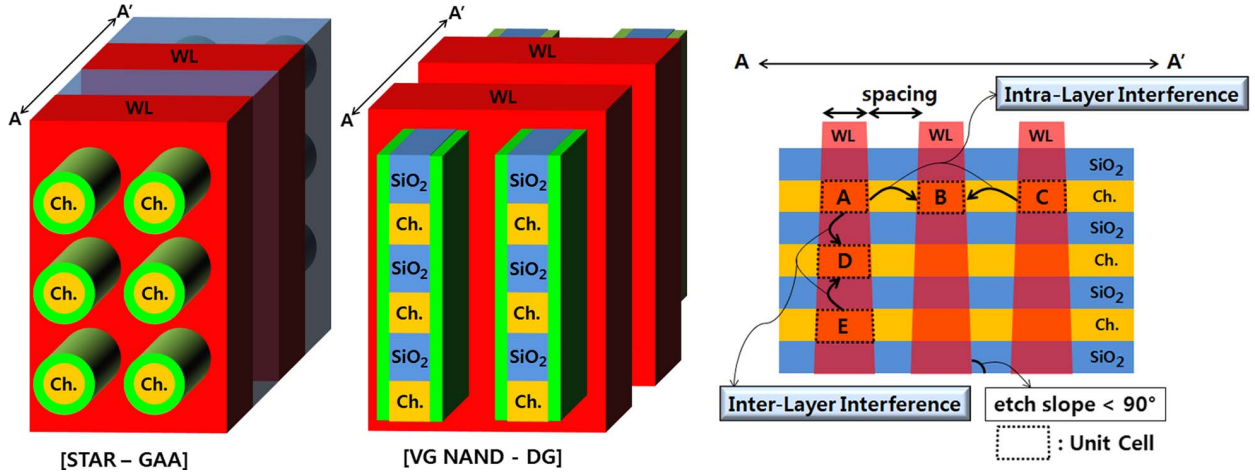


Fig. 3. Bird's eye view of STAR and VG NAND and cross-sectional view along A–A'. There are two types of interference between the cells in the 3-D stacked NAND structure, namely, intralayer and interlayer interferences.

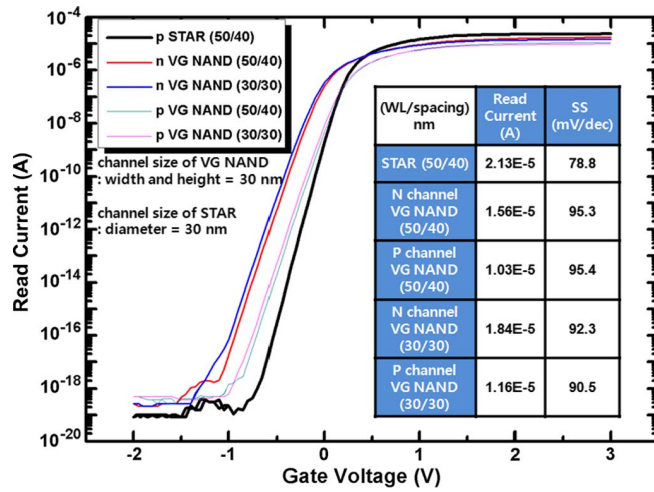


Fig. 4. I_d – V_g characteristic of STAR and VG NAND (TCAD simulation results). For convenience, we used a single-crystal Si channel for both STAR and VG NAND.

III. PERFORMANCE OF STAR FOR 3-D NAND ARCHITECTURE

The unit array structures of the STAR and the VG NAND are shown in Fig. 3. To evaluate the performance of the STAR, we used a 3-D TCAD simulation in which various models were put to execute such as *fermidirac* for carrier statistics model, *cvt* based on the inversion layer mobility theory, *srh* for taking the Shockley–Read–Hall recombination model into account, and *auger* for auger recombination. The advantages of STAR over VG NAND are summarized as follows.

- 1) Single-crystal channel: As aforementioned, cells in STAR having a single-crystal channel are expected to have uniform distribution of cell performance because of the absence of the defects associated with grain boundaries. Instead, the subthreshold characteristics of poly-Si FETs are quite dependent on trap density at grain boundaries in poly-Si. Thus, STAR can have better performance with a uniform and stable characteristic.
- 2) Current drivability and subthreshold swing: The STAR has large BL read current and small subthreshold

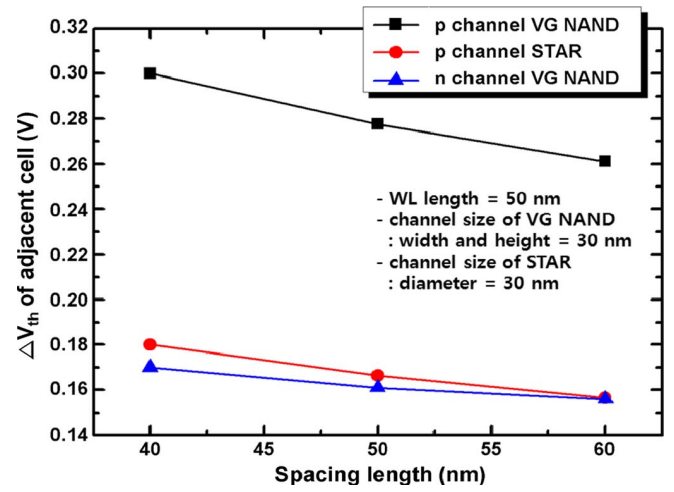


Fig. 5. Intralayer interference characteristics of STAR and VG NAND. Both neighbor cells (A and C) are programmed with $4 \cdot 10^{19} \text{ cm}^{-3}$.

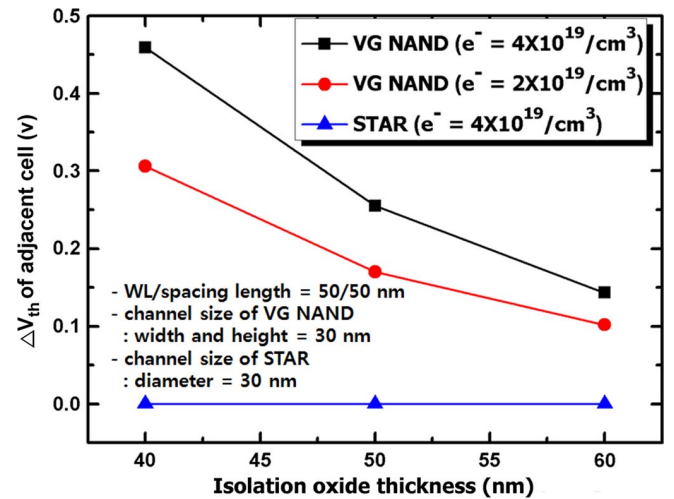


Fig. 6. Interlayer interference characteristics of STAR and VG NAND.

swing owing to the GAA structure. Fig. 4 shows the initial I_d – V_g characteristic of VG NAND and STAR structure.

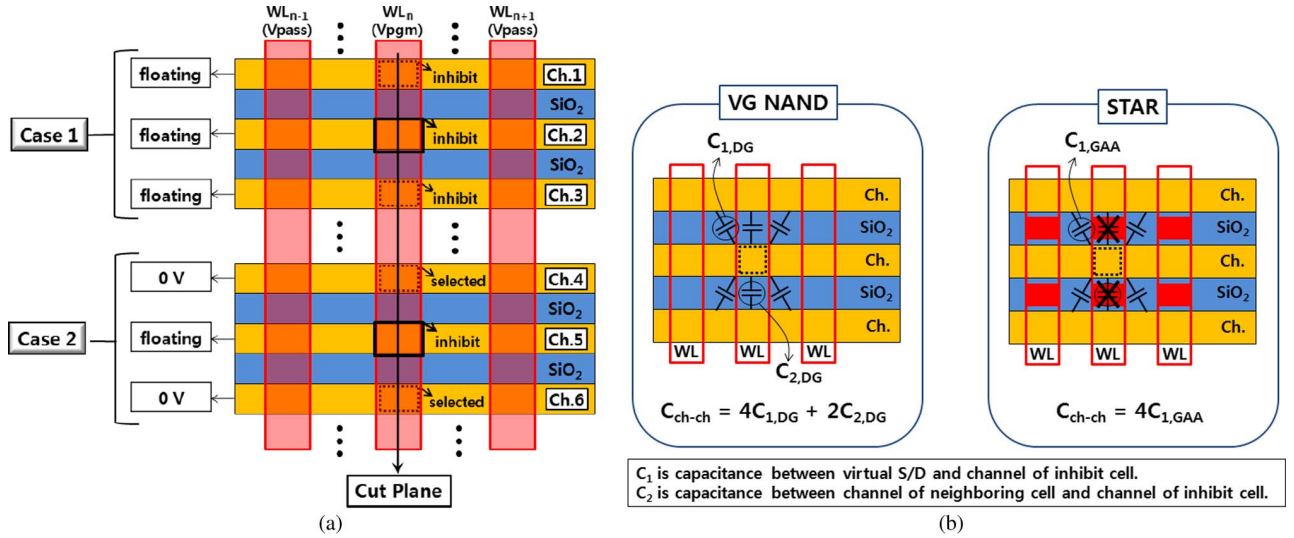


Fig. 7. (a) Cross-sectional view of channel stack-type 3-D NAND Flash memory. The Ch-Ch coupling phenomenon between stacked channels occur. In the page program mode, the self-boosted potential of inhibit cells is different according to neighbor channel condition. (b) New capacitance model for the Ch-Ch coupling phenomenon in VG NAND and STAR structures.

- 3) Stable virtual source/drain (S/D) characteristic: 3-D NAND structures use virtual S/D using the fringing field of neighbor gates because ion implantation is difficult [9], [10]. Furthermore, our previous research demonstrated that the electric field concentration effect of the GAA structure enables us to achieve stable virtual S/D characteristics such as higher on-current and less sensitive threshold voltage to the WL and spacing length variation [11]. Each layer of the 3-D stacked structure, in particular, has a different WL and spacing length due to an etch slope, which is several degrees off the vertical. (see Fig. 3) As a result, the GAA structure is more suitable for the 3-D stacked NAND structure.
- 4) Small intralayer interference: A virtual S/D structure has some interference of threshold voltage due to the fringing field induced by charges of programmed neighbor cells. As the worst case, the programmed charges in both neighbor cells (cells A and C) disturb the inversion of the virtual S/D region. Therefore, the threshold voltage of cell B increases, as illustrated in Fig. 3. It is shown in Fig. 5 that STAR has smaller interference than VG NAND on account of the field concentration effect.
- 5) Immunity to interlayer interference (Z-interference): A new important interference mode of 3-D stacked NAND Flash is the interlayer interference (Z-interference) caused by crosstalk of stored charges between the neighbor layers, as illustrated in Fig. 3 [4]. The height scaling of the 3-D stacked VG NAND structure is limited by this Z-interference.

Fig. 6 shows that, when the isolation oxide thickness is 40 nm, the simulated interference of cell D in VG NAND may be 460 mV, considering the worst case where both adjacent cells (cells A and E) are fully programmed with concentration of electrons = $4 \cdot 10^{19} \text{ cm}^{-3}$ [12]. However, there is no Z-interference in the STAR structure because adjacent cells are shielded by the conducting gate material, as shown in Fig. 6.

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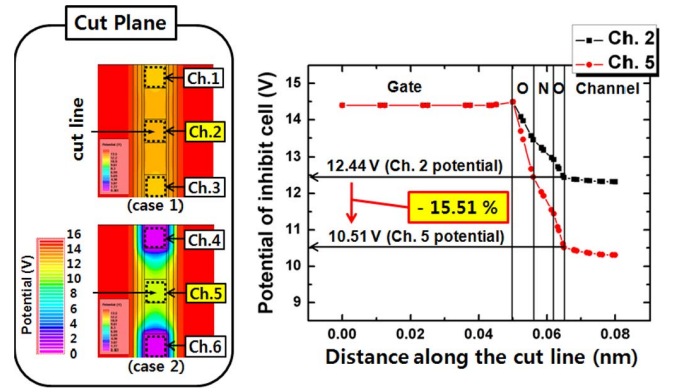


Fig. 8. Comparison of self-boosting potential of inhibit cells between cases 1 and 2 in VG NAND. (channel width = 30 nm, oxide gap size between channels = 40 nm, O/N/O = 3 nm/6 nm/6 nm, WL length/spacing = 50 nm/40 nm, and channel doping concentration = $5 \cdot 10^{17} \text{ cm}^{-3}$.)

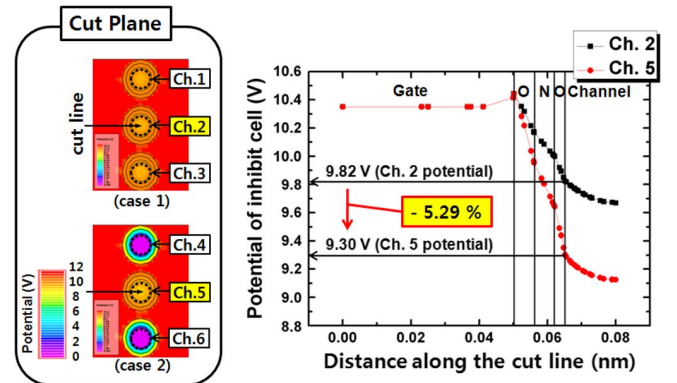


Fig. 9. Comparison of self-boosting potential of inhibit cells between cases 1 and 2 in STAR. (channel diameter = 30 nm, oxide gap size between channels = 40 nm, O/N/O = 3 nm/6 nm/6 nm, WL length/spacing = 50 nm/40 nm, and channel doping concentration = $5 \cdot 10^{17} \text{ cm}^{-3}$.)

- 6) Small channel-channel (Ch-Ch) coupling: In addition to interference due to stored electrons in neighbor storage nodes, Ch-Ch coupling is a new serious problem. For the

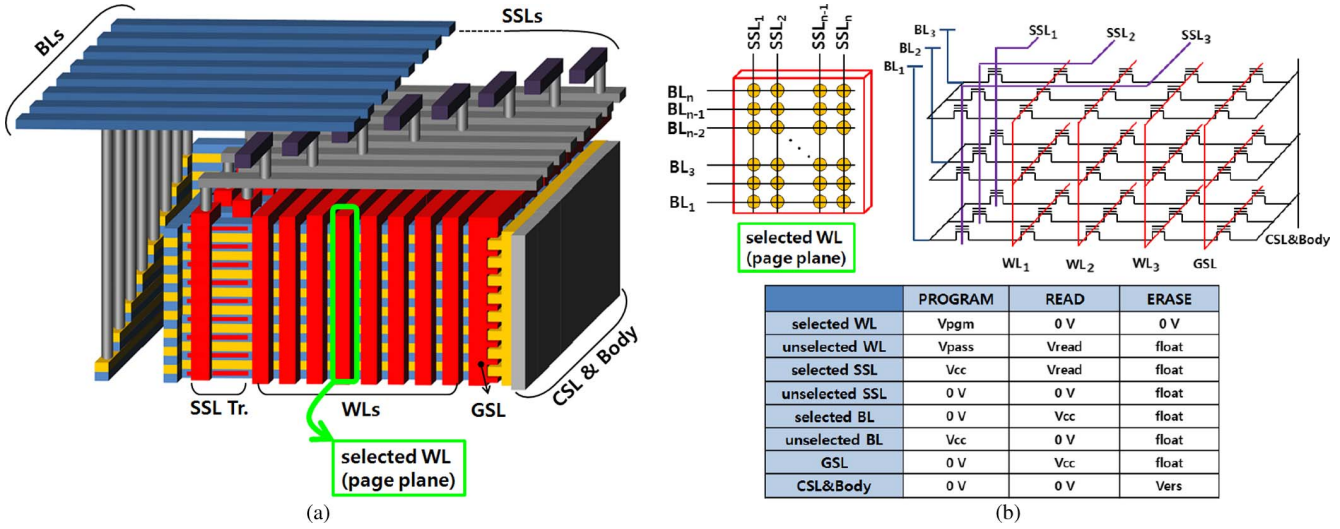


Fig. 10. (a) Unit structure of 3-D NAND Flash memory based on STAR, i.e., “building.” (b) Equivalent circuit of the building and operation voltage scheme table.

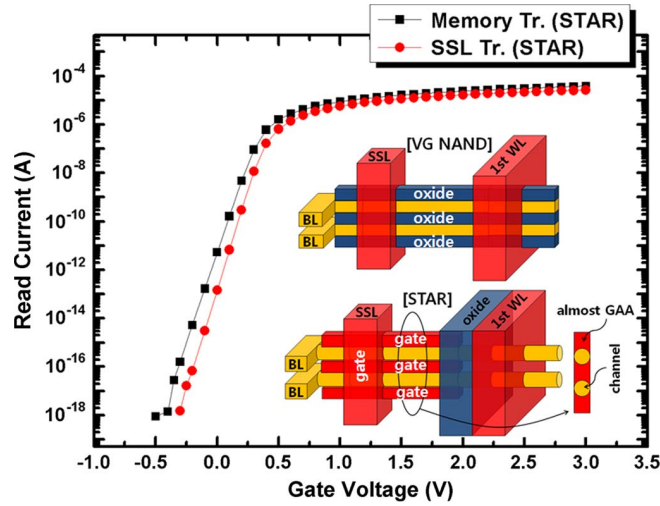


Fig. 11. Designed SSL structure and its I_d - V_g characteristic. (WL length of memory Tr./SSL Tr. = 40 nm/200 nm and channel concentration = $5 \cdot 10^{17} \text{ cm}^{-3}$.)

first time, we investigated “Ch–Ch coupling” phenomenon in 3-D channel stacked NAND Flash architecture.

Conventional NAND Flash uses the self-boosted inhibit scheme. In program-inhibit cells, the BL with V_{cc} voltage initially precharges the associated channel, and the floating channel voltage is raised when a high program voltage is applied to the selected WL [13]. This boosted channel voltage should be high enough to decrease program disturbance. However, as NAND Flash memory device is scaled down, the potential of the boosted channel is reduced due to a smaller capacitive coupling ratio from WL to the channel, leakage current generated by gate-induced drain leakage [14], and drain-induced barrier lowering [15].

As a result, an appropriate regulation of program disturbance is very important for improving the reliability of NAND Flash memory.

In the 3-D channel stacked NAND Flash, electric interaction between stacked channels (Ch–Ch coupling) is a new risk factor

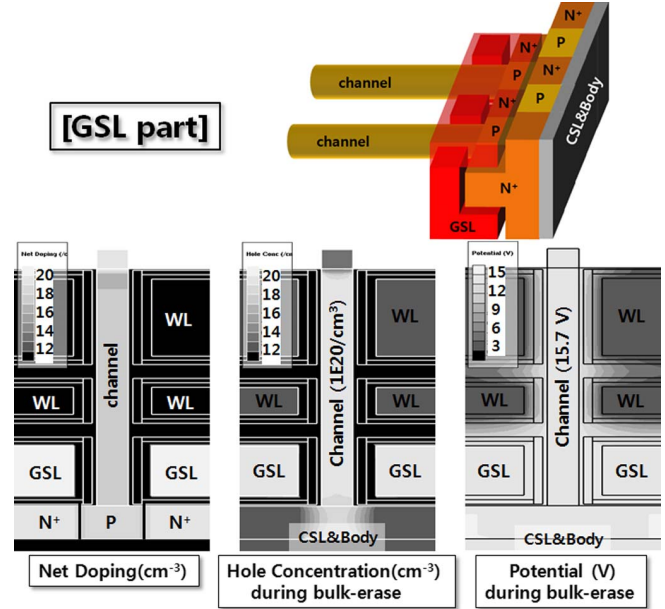


Fig. 12. Structure of GSL part and simulated profile during bulk erase operation (V_{ers} = 16 V, CSL N⁺ region concentration = $1 \cdot 10^{20} \text{ cm}^{-3}$, body concentration = $1 \cdot 10^{18} \text{ cm}^{-3}$, and channel concentration = $5 \cdot 10^{17} \text{ cm}^{-3}$). Higher brightness shows a higher level.

reducing the self-boosting efficiency of inhibit cells. As shown in Fig. 7, the voltage of the program-inhibit channel is affected by the potential of neighbor channels. In other words, there is additional capacitance $C_{\text{ch-ch}}$ that determines the boosted channel voltage. The $C_{\text{ch-ch}}$ of the STAR is smaller than that of VG NAND since the conducting gate material between the neighbor cells can eliminate C_2 (capacitance between the channel of the neighboring cell and the channel of the inhibit cell).

We verified the characteristic of Ch–Ch coupling by using a 3-D TCAD simulation. For reasonable comparison between VG NAND and STAR, the program voltage of each structure is determined for the same electric field at the tunneling oxide–channel interface, in which the program speed is same.

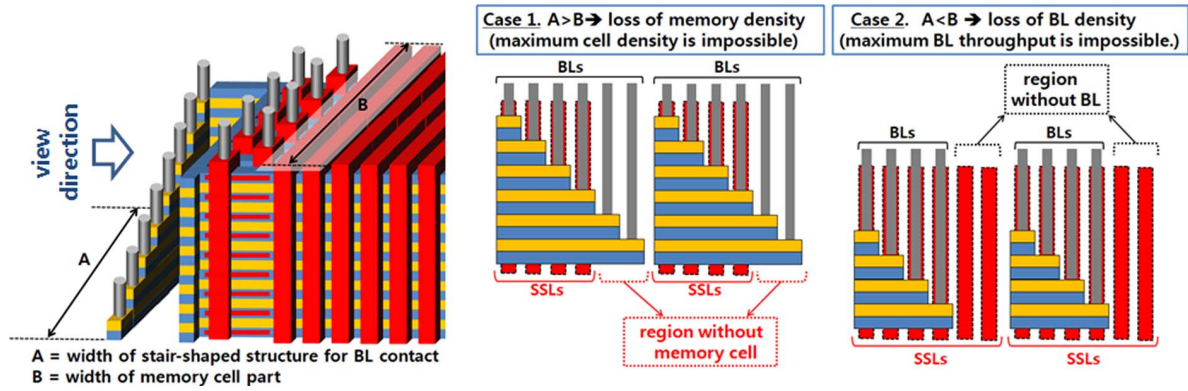


Fig. 13. Determination of building size for maximum memory density and BL throughput.

The pass voltage is 5 V, and the program voltages of VG NAND and STAR are 14.4 and 10.35 V, respectively. Figs. 8 and 9 show the potential of self-boosted channel related with Ch–Ch coupling. In addition, case 1 indicates the condition where all neighboring channels are floating. In case 1, there is no self-boosting efficiency degradation by Ch–Ch coupling. However, case 2 represents the worst case of the inhibit channel (Ch.5) in which the voltage of neighboring channels of Ch.4 and Ch.6 is 0 V for programming selected cells. Compared with case 1, the self-boosting efficiency is fallen by 15.51% and 5.29% in VG NAND and STAR, respectively.

Consequently, the STAR is a more reliable 3-D stacked NAND structure that can effectively reduce the program disturbance.

From the above discussion, the STAR has stable current drivability and immunity to degradation from various 3-D interferences. Therefore, the STAR is a more adequate structure for 3-D stacked NAND Flash memory. In the next section, we designed 3-D NAND Flash architecture based on STAR.

IV. FULL ARRAY DESIGN BASED ON STAR

We designed full chip architecture based on the following points.

First, additional process steps and extra area in memory array part should be minimized. The previous VG NAND [3] has the penalty of memory unit area since it needs several string select line (SSL) transistors in one channel string. In addition, photolithography and ion-implantation steps are added at each stacked layer to make the SSLs, the combination of depletion and enhancement transistors.

Second, same operation method with conventional NAND Flash memory should be utilized, which means good compatibility with peripheral memory functional block. For example, GIDL erase of BiCS Flash and negative erase voltage of gate in VG NAND [4] may require extensive changes in circuits. Thus, a conventional bulk erase method is more desirable.

Third, there should not be a throughput penalty related with page program, block erase, and page read. Since NAND Flash memory is used for applications requiring fast bulk data transfer, it uses page-based operations for both read and program tasks to achieve high throughput. In particular, in the all BL (ABL) architecture [16], all data of a page are simultaneously

transferred through the ABLs connected to the page buffer. As a consequence, the connection to the peripheral page buffer and decoder block should be considered to satisfy full throughput capacity. The previous work [4] did not show the detailed connection of BL and full array operation method. For the first time, we designed the 3-D stacked NAND Flash memory based on the “full” array chip.

Fig. 10 shows the proposed basic unit structure of 3-D stacked NAND Flash memory. We defined this unit structure as “building.” The specific descriptions about each part of the building are as follows.

The 3-D stacked NAND Flash memory, unlike conventional 2-D planar NAND Flash memory, needs one more address that is determined by SSLs. In conventional 2-D NAND, the WL selects a “page (line),” whereas the WL of 3-D stacked NAND selects a “page plane,” as shown in Fig. 10(b). Then, the column and row in the selected page plane are determined by the BL and SSL, respectively. The BLs are formed on the top floor of a building. In addition, BLs are perpendicular to other lines (WLs and SSLs). In full array, all BLs of each block are connected with those of other blocks to the page buffer. Consequently, there must not be any overlapping with other metal lines or contact holes in the BL region. The WLs and SSLs are parallel with different levels, and they will be connected with each decoder at the opposite end site.

Fig. 11 shows the SSL structure in detail. In the previous VG NAND [4], the long underlap channel region (3–5F size) that is not covered with the SSL gate exists between the BL and the first WL. Therefore, additional ion implantation is needed to avoid electrical disconnection. However, the gate of SSL in the proposed STAR is connected between the BL and the first WL (dummy WL) without the underlap region. In addition, the gate length of the SSL transistor is usually longer than that of the memory cell transistor in order to reduce leakage current that brings about degradation of self-boosting efficiency. The designed SSL can have longer gate length without extra area. In addition, almost GAA structure of SSL can maintain excellent current drivability of STAR, as shown in Fig. 11. The detailed structure of ground select line (GSL) part is displayed in Fig. 12. The N^+ doped common source line (CSL) and p-type body are electrically tied (CSL&body). Since the gate of the GSL transistor covers the N^+ region, sufficient electron supply is possible during read or program operation. In

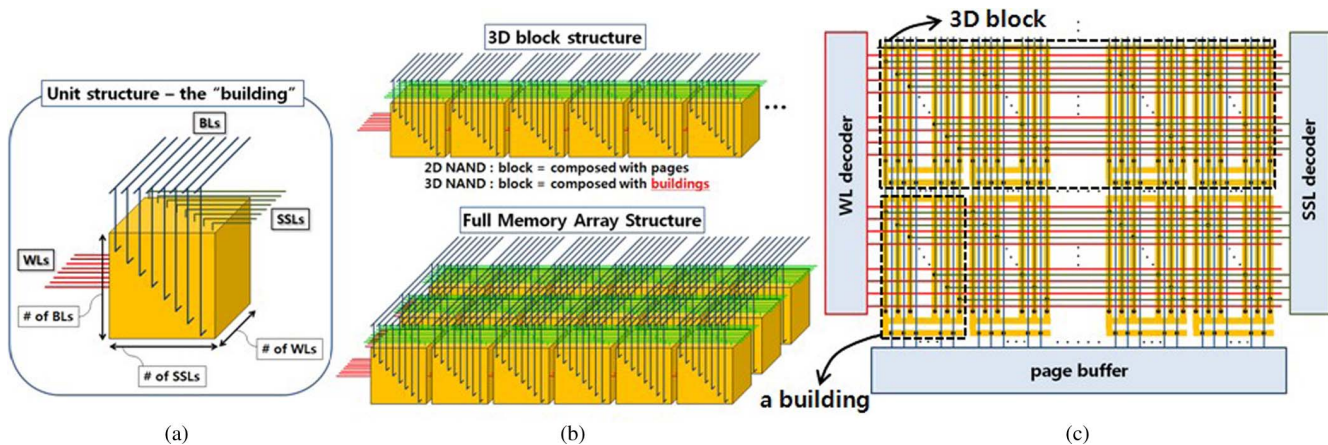


Fig. 14. (a) Simplified building structure. (b) Three-dimensional block and full array structure based on building. (c) Simplified full chip architecture.

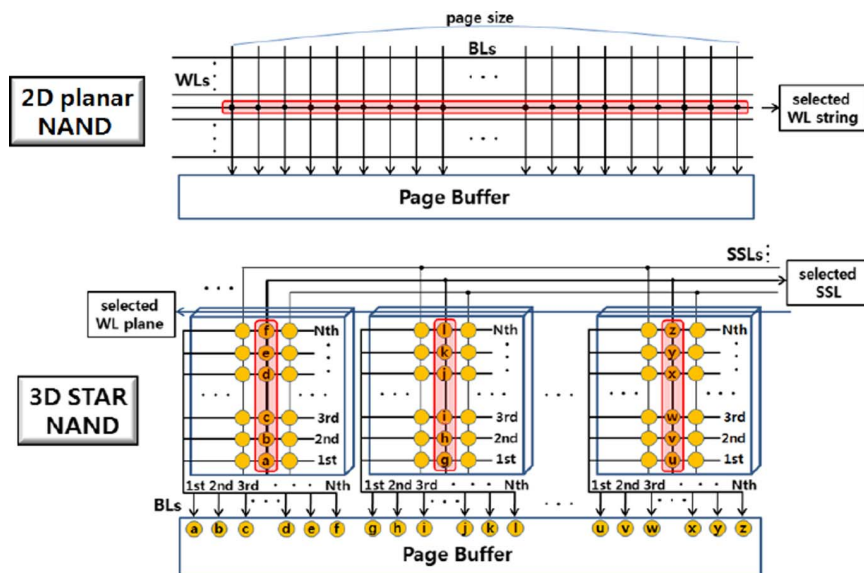


Fig. 15. Full array operation during page read or program for maximum parallelism.

addition, the channel of STAR is connected to a p-type body. As a consequence, conventional bulk erase operation can be achieved, as shown in the simulated results of Fig. 12.

Fig. 13 shows the optimized size condition of building for compact 3-D block composition. The widths of A and B should be same for maximum memory density and BL throughput. If the widths of A and B are different, the wasted space reduces the space efficiency, as described in Fig. 13. Using the optimized building structure, the 3-D block and the full memory array, including peripheral block (decoders and page buffer), can be composed, as shown in Fig. 14. In the next section, we will discuss the operation scheme with successfully designed full array architecture.

V. FULL ARRAY OPERATION METHOD

In the 2-D NAND array, the cells are organized in page, which is the unit for the simultaneous program and read operations, as shown in Fig. 15. To maintain maximum throughput of the previous 2-D NAND Flash memory, the designed 3-D stacked architecture should satisfy the following conditions. First, there

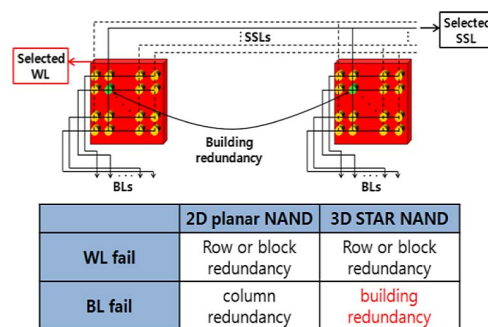


Fig. 16. Redundancy scheme of 3-D stacked NAND Flash architecture. To solve WL fail, block redundancy can be adopted similar to conventional 2-D NAND. On the other hand, when defects are found in BL, designed 3-D stacked NAND Flash supports interchange building repair.

should be no loss of the total number of BL connected to the page buffer. In the previous section, we designed a full array structure satisfying this first condition. Second, all information should be transferred through the BLs simultaneously. This second requirement can be fulfilled, as shown in Fig. 15.

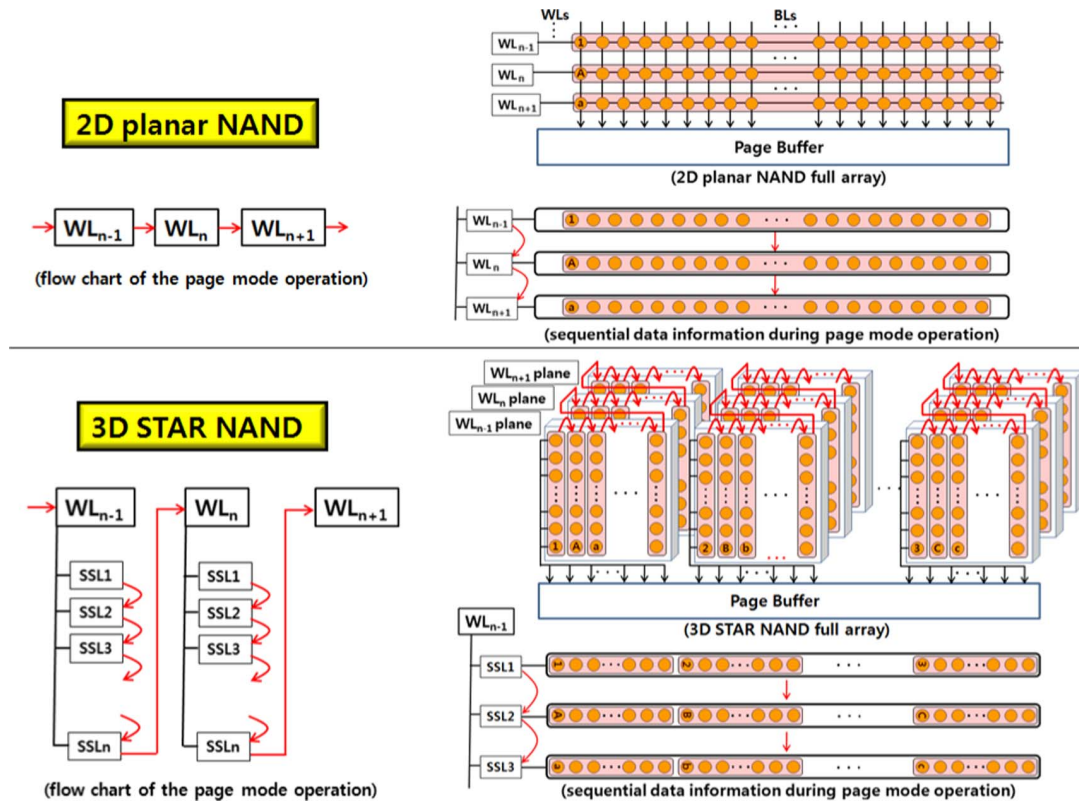


Fig. 17. Sequential flow during page read or program operation in 2-D and 3-D NAND Flash memory. In the 2-D planar NAND, data processing of each page is carried out along with the WL being sequentially selected. However, the 3-D STAR NAND needs a new sequential operation method to manipulate data stored in 3-D space. Using the proposed method, parallel page operation in 3-D STAR NAND can be achieved without degradation of data processing efficiency.

When the rows are selected by the SSL in the page plane, the data of rows are transferred along the BLs in parallel. Therefore, maximum throughput of read and program of designed 3-D stacked NAND Flash architecture is possible without penalty in comparison with conventional 2-D NAND Flash memory. In addition, the redundancy scheme in 3-D NAND Flash memory is another important issue [17]. Fig. 16 shows the concept diagram of 3-D redundancy. As conventional 2-D planar NAND, block interchange is possible in 3-D STAR NAND. In addition, BL failure can be repaired by building unit redundancy.

In addition, 3-D stacked NAND Flash memory has a different sequential flow during page read or program operation, as shown in Fig. 17. Each row data is transferred to the page buffer (or transferred from the page buffer during program) along the sequential flow of SSL address. After all data of selected WL plane are transferred to the page buffer, the sequential flow goes on to the next WL plane. ($WL_n \rightarrow WL_{n+1}$).

VI. FABRICATION PROCESS OF DESIGNED 3-D STACKED NAND FLASH ARCHITECTURE

Fig. 18 depicts the critical fabrication steps of designed 3-D stacked NAND Flash architecture. The specific method of each step is summarized as follows.

Fig. 18(a): At first, SiGe/Si/SiGe/SiGe/... layers that are sequentially epitaxially grown on the Si substrate and active channel are formed. Oxide/poly-Si/oxide layers are used as a

hard mask for etch. Then, n- and p-type ion implantations are carried out for the BL region and body, respectively.

Fig. 18(b): The screening oxide is deposited for preventing the donor from penetrating into the active channel. Next, high-dose n-type ion implantation is performed to make the N^+ CSL region.

Fig. 18(c): Oxide deposition is followed by patterning the oxide buttress, which sustains the long channels not to be collapsed or adhered. Then, selective SiGe etching process is carried out. If SC1 solution is used for SiGe removal, silicon fin is rounded as NH_4OH and H_2O_2 solution also slightly etches silicon [5].

Fig. 18(d): Oxide redeposition to fill the gap between Si channels is performed. As a consequence, conductive SiGe is replaced with an oxide insulator.

Fig. 18(e): Oxide patterning carried out for making WLs.

Fig. 18(f): Isotropic oxide etch is carried out. The key point of this process is that the channel width (A) must be smaller than the oxide buttress width (B) for preventing oxide buttress from being removed during oxide etch. After isotropic recess, the width of oxide buttress decreases ($B \rightarrow C$) and the silicon channel for unit cell is exposed.

Fig. 18(g): Growth of ONO dielectrics is followed by tungsten deposition and planarization for the gate of WL, SSL, and GSL. If tunnel barrier engineering is used for tunneling oxide formation, more reliable memory characteristics can be achieved [18]. Using this damascene gate process, all gates of cell, SSL, and GSL transistors are self-aligned.

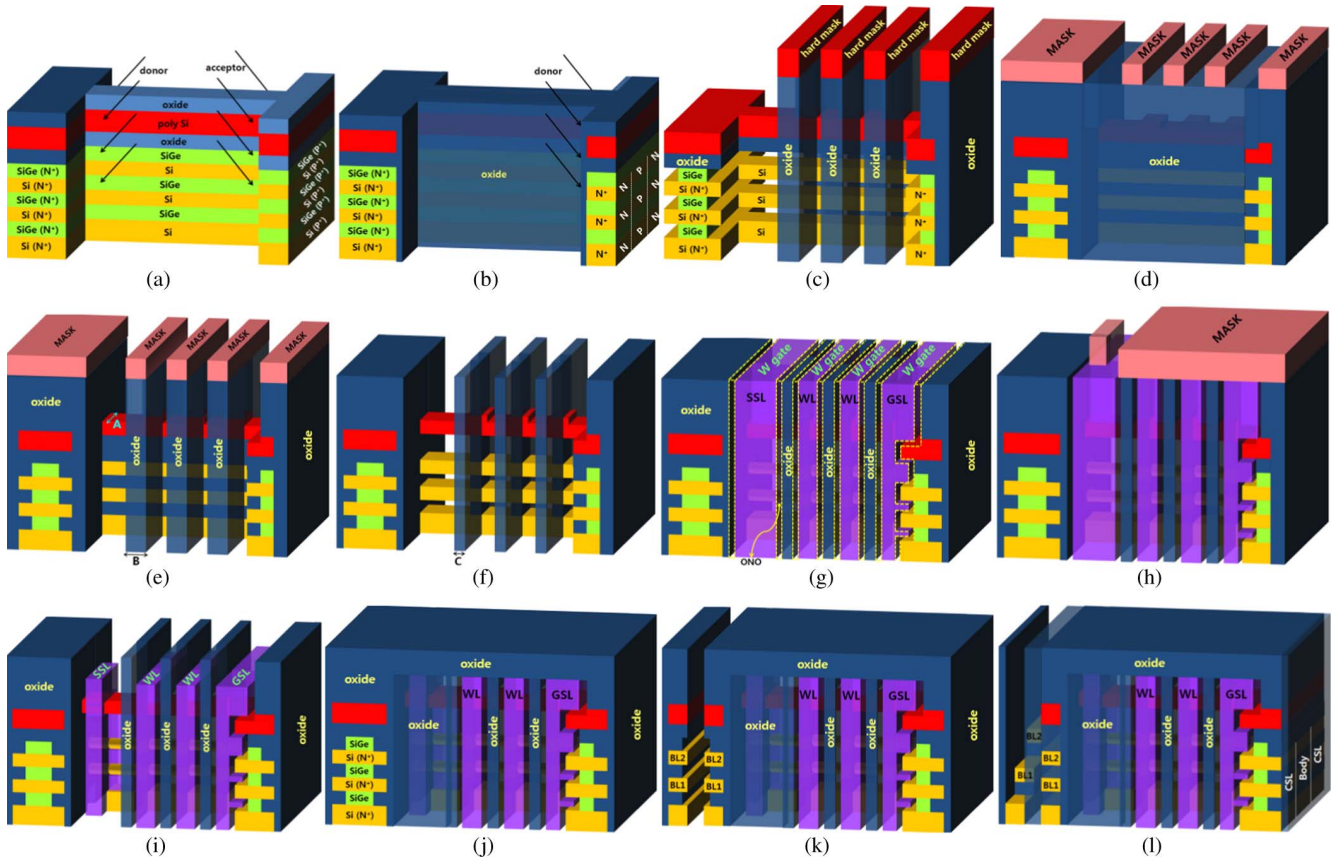


Fig. 18. Critical fabrication steps of designed 3-D stacked NAND Flash architecture based on STAR.

Fig. 18(h) and (i): SSL transistors are made by lithography.

Fig. 18(j) and (k): To make the BL region, trench etch is carried out. Next, SiGe selective etch is performed for perfect isolation between the BLs.

Fig. 18(l): Stair-like BL structure is made.

VII. CONCLUSION

We have demonstrated the suitability and superiority of STAR for 3-D stacked NAND Flash memory through the systematic comparison and examination using 3-D TCAD simulation. In addition, new 3-D interference phenomena in stacked Flash memory are examined. For the first time, we designed full array architecture based on structure, operation, and process methods. The proposed 3-D stacked NAND architecture based on single-crystalline STAR will be the promising technology for opening the terabit era.

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