

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,

Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,

Patent Owner.

Case No.: IPR2024-00909
U.S. Patent No. 10,658,378

**PATENT OWNER'S RESPONSE
UNDER 37 C.F.R. § 42.120**

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LIST OF EXHIBITS

Exhibit	Description
Ex. 2001	Joint Claim Construction Statement
Ex. 2002	<i>Reserved</i>
Ex. 2003	Micron’s Preliminary Claim Constructions
Ex. 2004	YMTC’s Proposed Claim Constructions
Ex. 2005	Declaration of Dr. Yang (“Yang”)
Ex. 2006	Decision Granting Institution of <i>Inter Partes Review</i> of U.S. Patent No. 10,937,806 (IPR2024-00791, Paper 11)
Ex. 2007	Deposition Transcript of Dr. Lee
Ex. 2008	U.S. Patent No. 10,937,806 (“’806”)
Ex. 2009	Petitioner’s Preliminary Reply for <i>Inter Partes Review</i> of U.S. Patent No. 10,937,806 (IPR2024-00911, Paper 10)
Ex. 2010	Patent Owner’s Preliminary Sur-Reply for <i>Inter Partes Review</i> of U.S. Patent No. 10,937,806 (IPR2024-00911, Paper 11)
Ex. 2011	Decision Granting Institution of <i>Inter Partes Review</i> of U.S. Patent No. 10,937,806 (IPR2024-00911, Paper 12)
Ex. 2012	Decision Granting Institution of <i>Inter Partes Review</i> of U.S. Patent No. 10,658,378 (IPR2024-00788, Paper 13)

LIST OF ABBREVIATIONS

Abbreviation	Term
'378	U.S. Pat. No. 10,658,378
'378FH	File History of U.S. Pat. No. 10,658,378
Challenged Claims	Ex. 1001, Claims 1-7, 18
DI	Decision Granting Institution for <i>Inter Partes</i> Review of U.S. Patent No. 10,658,378 (IPR2024-00909, Paper 12)
Office	U.S. Patent and Trademark Office
Parallel district court litigation	<i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , NDCA-3-23-cv-05792 (N.D. Cal.)
Patent Owner or PO	Yangtze Memory Technologies Co. Ltd.
Petition or Pet.	Petition for <i>Inter Partes</i> Review of U.S. Patent No. 10,658,378 (IPR2024-00909, Paper 1)
Petitioner	Micron Technology, Inc.
POSITA	Person of ordinary skill in the art
Toyama	U.S. Patent Publication No. 2017/0179026

I. INTRODUCTION

The sole reference in Petitioner’s Grounds fails to disclose or render obvious the Challenged Claims of U.S. Patent No. 10,658,378 (“’378,” Ex. 1001). Petitioner has filed two IPRs to challenge the ’378. In this second IPR, Petitioner challenges independent claim 1 and dependent claims 2-7, as well as dependent claim 18 (“Challenged Claims”) which depends from claim 15 that Petitioner also challenges in the first IPR (IPR2024-00788). Petitioner raises the same grounds based on the Toyama reference as in the first IPR. The Grounds rely on two embodiments of Toyama and fail to disclose or render obvious at least three separate limitations: [1.c.ii]/[15.a] (“an isolation region of the substrate”/“a substrate with an isolation structure”), [1.c.i-ii]/[15.c.i] (“a dielectric structure on [an/the] isolation [region/structure]”), and [1.d]/[15.h] (“[one or more] through array contacts (TACs) extending vertically through [the dielectric structure and the isolation region]/[the dielectric and the isolation structures]”). In addition, Petitioner fails to show that the art discloses or renders obvious claim 7, which depends from claim 1 and further requires “the dielectric structure defines a through array contact region of the 3D memory device,” and claim 18, which depends from claim 15 and further requires “an etch stop plug interposed between each local contact of the local contacts and each channel structure of the channel structures.”

The '378 is directed to a novel three-dimensional (3D) memory device having through array contacts and methods related to manufacturing such a device. As memory cells are scaled down and the density of memory cells increases, it becomes challenging to collect and route signals to the peripheral circuitry efficiently. The '378 provides a solution by forming through array contacts (TACs) in a dedicated region where they provide vertical interconnects to the peripheral devices. '378, 1:20-32, 2:19-21, 5:46-50, 11:3-9, 19:55-60.

Fabrication of 3D NAND memory devices generally involves stacks of alternating dielectric and conductive layers, through which vertical structures, such as channels and vias, are formed. '378, 1:38-55. The prior art at the time of filing of the '378 formed vertical vias within the alternating dielectric and conductive layers, which "increases the fabrication cost." '378, 10:59-66, 18:27-33. The '378 simplifies the fabrication process of these TACs by forming them in a dedicated dielectric structure. '378, 18:27-33. The '378 thereby avoids the issues in the prior art such as using a complex and costly etching process due to having to etch through alternating dielectric and conductive layers for individual TACs. '378, 5:35-39, 10:59-66, 18:27-41, 20:9-16. The '378 further uses an isolation structure (*e.g.*, a "shallow trench isolation") in the substrate on which the dielectric structure is placed and through which the lower portions of the TACs extend. '378, 10:30-33, 21:17-25.

The '378 introduced a 3D memory device in which TACs “extend vertically through” the “dielectric structure” and the “isolation structure,” and methods of manufacturing such a device. '378, Abstract, 10:57-59, 21:17-25. The claimed invention recites “a substrate with an isolation structure,” a “dielectric structure on the isolation structure and extending vertically through the alternating conductor/dielectric layer stack,” and “through array contacts (TACs) extending vertically through the dielectric and the isolation structures.” See '378, Claim 15. As a result, the claimed invention avoids the issues arising from forming TACs through alternating dielectric/conductor stacks and “simplif[ies] the fabrication process and reduce[s] the fabrication cost.” '378, 18:36-41.

The Petition fails to establish that any of the Challenged Claims is disclosed or rendered obvious. Specifically, Petitioner sets forth the following obviousness grounds challenging '378 independent claim 1 and its dependent claims 2-7 and claim 18 (which depends from claim 15):

Ground 1A: Toyama's (Ex. 1005) “First Exemplary Structure;”

Ground 1B: Toyama's “second modification of the fourth exemplary structure” (“Second Modification”).

Petitioner does not assert that any of the cited references anticipates the Challenged Claims, and instead raises obviousness based on a mix of contradictory assertions, faulty analysis, and pure hindsight.

Petitioner’s Ground 1A relies on Toyama’s First Exemplary Structure, but the First Exemplary Structure does not teach, for example, “an isolation region of the substrate”/“a substrate with an isolation structure” as required by limitation [1.c.ii]/[15.a] because the feature of Toyama that Petitioner maps to the “isolation [region/structure]” is not “part of” the alleged substrate as required under the proper construction of this term—instead it is located in a region that cuts through the entire substrate. In addition, Toyama’s First Exemplary Structure does not disclose or render obvious “a dielectric structure on [an/the] isolation [region/structure]” as required by limitation [1.c.i-ii]/[15.c.i] because Petitioner arbitrarily and improperly divides Toyama’s single dielectric structure into two regions and maps different regions to two separate, distinctive features of the Challenged Claims: the “dielectric structure” and the “isolation [region/structure].”

Petitioner’s Ground 1B relies on Toyama’s Second Modification, but the Second Modification does not teach, for example, “an isolation region of the substrate”/“a substrate with an isolation structure” as required by limitation [1.c.ii]/[15.a] for the same reasons as for Toyama’s First Exemplary Structure. In addition, Toyama’s Second Modification does not disclose or render obvious “through array contacts (TACs) extending vertically through the dielectric and the isolation structures” as required by limitation [15.h] because Toyama’s alleged TACs do not extend through the same structure (the claimed “dielectric structure”).

Furthermore, both of Petitioner's grounds fail to disclose or render obvious the additional requirement of claim 7 that "the dielectric structure defines a through array contact region within the 3D memory device" because the alleged TAC region identified in each ground is not defined by the alleged dielectric structure.

Finally, both grounds fail to disclose or render obvious "an etch stop plug interposed between each local contact of the local contacts and each channel structure of the channel structures" as required by claim 18 because the alleged etch stop plugs are not interposed between "each" of the local contacts Petitioner mapped to limitation [15.g] and the alleged channel structures.

Because the prior art fails to disclose or render obvious any of the Challenged Claims, the Board should find in favor of Patent Owner and uphold the validity of all Challenged Claims.¹

II. THE CLAIMED INVENTION OF THE '378 PATENT

The claimed invention of the '378 is directed to a "three-dimensional (3D) memory device" and related methods that address issues arising from the fabrication

¹ This Patent Owner Response is supported by the declaration of Dr. Yang. *See* Ex. 2005 ("Yang"), ¶¶1-29. All emphasis and color annotations have been added unless otherwise noted.

techniques known in the prior art and “simplif[y] the fabrication process and reduce[s] the fabrication cost.” ’378, Abstract, 18:36-41. Yang, ¶30.

Specifically, the ’378 is directed to an improved 3D memory device and methods for forming such a device in which “through array contacts (TACs)” “extend vertically through” the “dielectric structure” and the “isolation structure.” ’378, Abstract, 10:57-59, 21:17-25. 3D memory devices in the prior art at the time of filing of the ’378 involved through array vias that form connections between various components of the device to reduce size and increase density. ’378, 1:20-32. These vias were placed within the alternating dielectric and conductive layers, which required a complex etching process and “increase[d] the fabrication cost.” ’378, 10:59-66. Yang, ¶31.

The novel device the ’378 teaches and recites in the Challenged Claims is characterized by “a **substrate** with an **isolation structure**” and **TACs** that “extend vertically through” the “**dielectric structure**” and the “**isolation structure.**” ’378, Abstract, 10:57-59, 21:17-25, Claim 15. This novel configuration of elements allows for easier and less costly manufacture of 3D memory devices. ’378, 5:55-59, 18:27-33, 20:29-37.

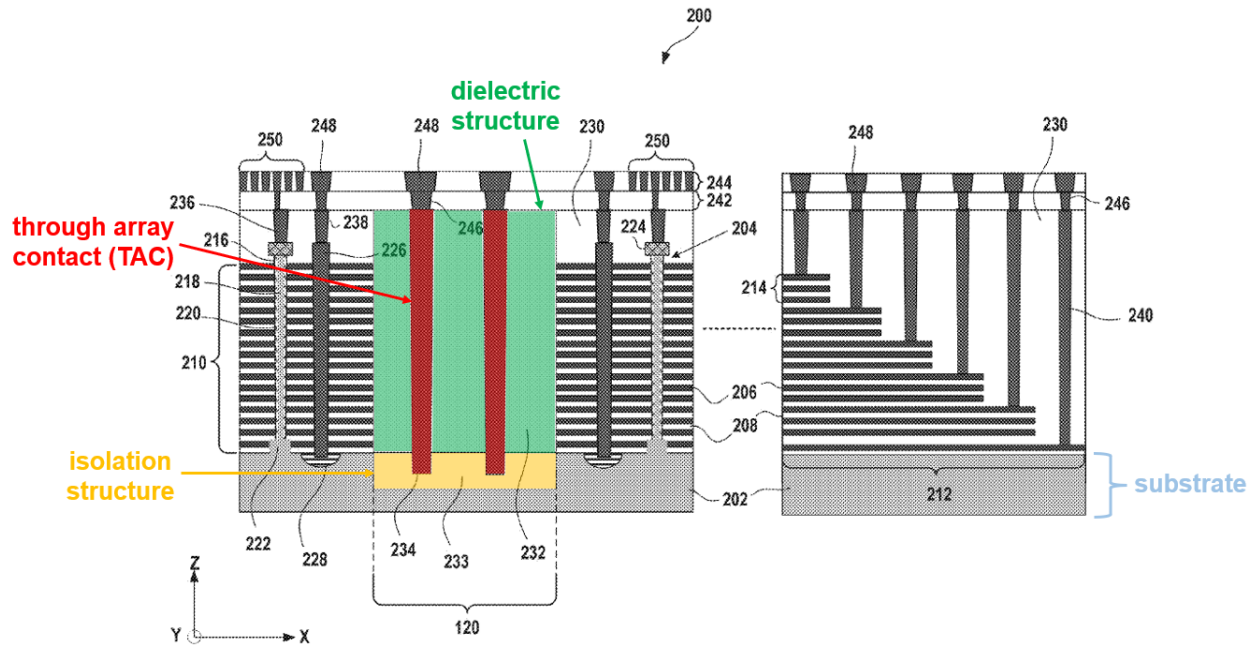
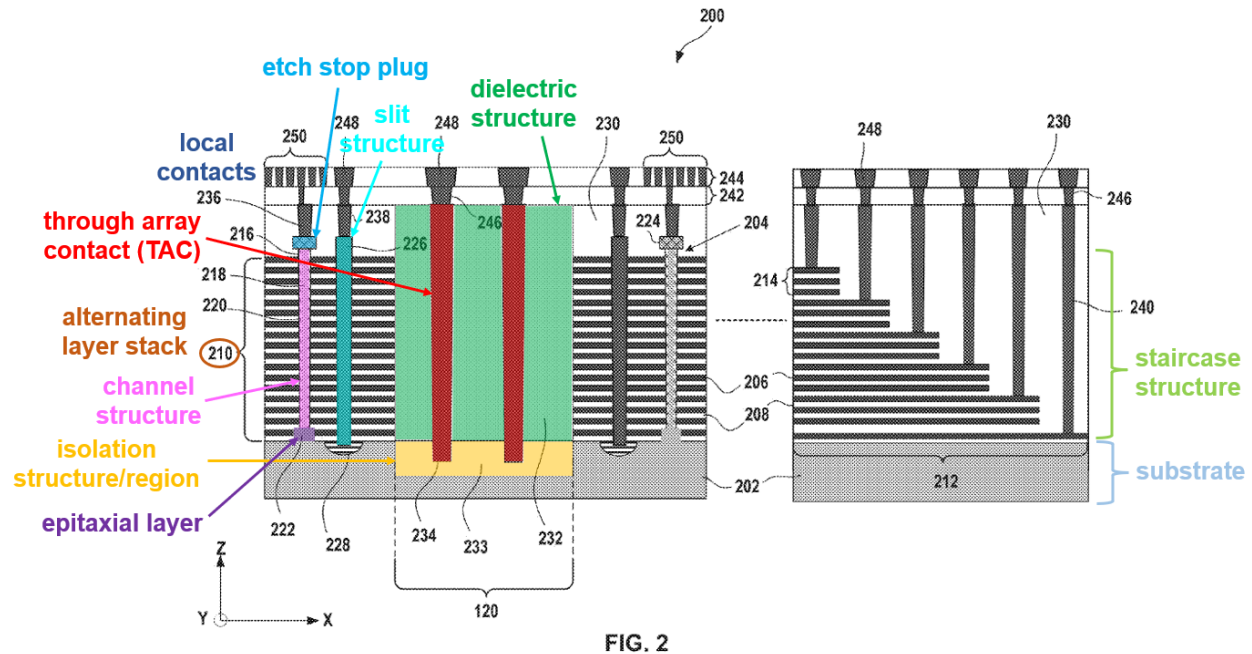


FIG. 2

'378, Fig. 2 (annotated). Yang, ¶32.

A representative embodiment of the '378's memory device includes: (1) "substrate 202" with "isolation structure or region 233"/ ('378, 10:30-35, 22:27-38); (2) "alternating conductor/dielectric layer stack 210" ('378, 8:17-25); (3) "dielectric structure 232" on "isolation structure or region 233" ('378, 10:18-29); (4) "channel structures 216" and "slit structures 226" extending vertically through "alternating conductor/dielectric layer stack 210" ('378, 9:1-6, 10:1-6); (5) "staircase structure 212" ('378, 8:48-55); (6) "word line contacts 240" (11:24-26); (7) "local contacts" on "channel structures 216" and "slit structures 226" (11:24-26); (8) "TACs 234" extending vertically through "dielectric structure 232" and "isolation structure or region 233" ('378, 10:57-59, 20:45-48); (9) an "etch stop plug 224" between each "local contact" and each "channel

structure 216” (’378, 9:31-48, Fig. 2); and (10) an “epitaxial layer 222” between “substrate 202” and “channel structures 216” (’378, 9:31-35, Fig. 2). A cross-section view of the memory device is below.



’378, Fig. 2 (annotated). Yang, ¶¶33-34.

Independent claim 1, from which all but one (claim 18) of the Challenged Claims depend, is directed to aspects of the above-described invention:

[1.pre] A three-dimensional (3D) memory device, comprising:

[1.a] a semiconductor substrate;

[1.b] an alternating layer stack disposed on the semiconductor substrate;

[1.c] [i] a dielectric structure [ii] on an isolation region of the substrate and [iii] extending vertically through the alternating

layer stack, [iv] wherein the alternating layer stack abuts a sidewall surface of the dielectric structure and [v] the dielectric structure is formed of a dielectric material;

[1.d] one or more through array contacts (TACs) extending vertically through the dielectric structure and the isolation region;

[1.e] one or more channel structures extending vertically through the alternating layer stack;

[1.f] an epitaxial layer between the one or more channel structures and the semiconductor substrate;

[1.g] an etch stop plug on each of the one or more channel structures;

[1.h] a staircase structure in the alternating layer;

[1.i] slit structures extending vertically in the alternating layer stack; and

[1.j] one or more contact layers on the one or more TACs, the one or more channel structures, and the slit structures.

The remaining Challenged Claim (claim 18) depends from claim 15, and is directed to similar aspects of the above-described invention:

[15.pre] A three-dimensional (3D) memory device, comprising:

[15.a] a substrate with an isolation structure;

[15.b] an alternating conductor/dielectric layer stack disposed on the substrate;

[15.c] [i] a dielectric structure on the isolation structure and [ii] extending vertically through the alternating conductor/dielectric layer stack, [iii] wherein the alternating conductor/dielectric layer stack abuts a sidewall surface of the dielectric structure and [iv] the dielectric structure is formed of a dielectric material;

[15.d] channel structures and slit structures extending vertically through the alternating conductor/dielectric layer stack;

[15.e] a staircase structure disposed in the alternating conductor/dielectric layer stack, wherein the staircase structure comprises levels with each level having a conductor layer thereon;

[15.f] a word line contact disposed on the conductor layer of the each level;

[15.g] local contacts disposed on the channel structures and the slit structures; and

[15.h] through array contacts (TACs) extending vertically through the dielectric and the isolation structures.

[18.pre] The 3D memory device of claim 15, further comprising:

[18.a] an etch stop plug interposed between each local contact of the local contacts and each channel structure of the channel structures; and

[18.b] an epitaxial layer disposed between the channel structures and the substrate.

III. FILE HISTORY

The claims of the '378 remain patentable over the prior art for at least the same reason identified during prosecution. As discussed further below in §§VI-IX, the prior art does not disclose or render obvious, *inter alia*, the '378 claim elements “a substrate with an isolation structure,” “a dielectric structure on the isolation structure and extending vertically through the alternating conductor/dielectric layer stack, wherein the alternating conductor/dielectric layer stack abuts a sidewall surface of the dielectric structure and the dielectric structure is formed of a dielectric material,” and “through array contacts (TACs) extending vertically through the dielectric and the isolation structures.” Claims directed to these limitations were allowed after thorough prosecution and consideration of numerous prior art references.

The '378 was filed on July 27, 2018. After a preliminary amendment where Applicant removed multiple claim dependency and corrected a typographical error, the application included 3 independent claims (pending claims 1, 10, and 16) and 17 dependent claims (pending claims 2-9 which depended from claim 1, claims 11-15 which depended from claim 10, and claim 17-20 which depended from claim 16). Ex. 1002, 105-111 (12/06/2018 Preliminary Amendment). Yang, ¶35.

In a non-final office action, the Examiner rejected pending claims 1, 3-16, and 18-20 under 35 U.S.C. §103 as being allegedly obvious over U.S. Patent 9,620,512 (“Nishikawa”) in view of U.S. Patent Publication No. 2016/0056188 (“Lee”), but found that pending claims 2 and 17 “would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.” Ex. 1002, 529-537 (08/22/2019 Office Action). Yang, ¶36.

Applicant followed the Examiner’s suggestion “[w]ithout acquiescing to the propriety of the rejection” and rewrote pending claims 2 and 17 in independent form. Applicant also amended pending claim 10 “[w]ithout acquiescing to the propriety of the rejection” to “recite features that further distinguish it from Nishikawa and Lee.” Ex. 1002, 569 (12/23/2019 Amendment and Reply). Having placed the independent claims in allowable form, Applicant requested that their respective dependent claims also be allowed. Applicant further added two new claims that depend from pending claim 16. Ex. 1002, 563-571 (12/23/2019 Amendment and Reply). The Examiner subsequently allowed all pending claims. Ex. 1002, 579-586 (01/13/2020 Notice of Allowance). The ’378 issued on May 19, 2020 with twenty claims, including the renumbered independent claims 1, 9, and 15. Ex. 1002, 602 (04/29/2020 Issue Notification). Yang, ¶37.

After the first office action and before Applicant’s response, Applicant filed an information disclosure statement (IDS) that notified the Examiner of U.S. Patent

Publication No. 2017/0179026 (“Toyama”). Ex. 1002, 555 (12/03/2019 Information Disclosure Statement). The Examiner considered Toyama and explicitly cited it as a “reference[] considered.” Ex. 1002, 593 (01/13/2020 List of References Cited by Applicant and Considered by Examiner). Petitioner’s assertion that “Patent Owner only gave Examiner a haystack” (Pet. 15) is belied by the fact that Applicant submitted an IDS solely to cite Toyama, which was then explicitly considered by the Examiner. Moreover, the ’378 was issued with only sixteen references (nine U.S. patent documents and six foreign patent documents) one of which is Toyama. ’378, (56). Thus, the Examiner duly considered Toyama, but found it lacking as should the Board here. Yang, ¶¶38.

IV. LEVEL OF ORDINARY SKILL IN THE ART

For purposes of this proceeding only, Patent Owner does not object to the definition of a person of ordinary skill in the art (“POSITA”) proffered by Petitioner and adopted by the Board at institution. Pet. 33. The Challenged Claims are valid regardless of the precise definition used for a POSITA. Yang, ¶¶39-43.

V. CLAIM CONSTRUCTION

Other than the terms identified below, Patent Owner submits that constructions of the claim terms are not necessary to assess whether the prior art reads on the Challenged Claims for the purposes of the *inter partes* review. Patent Owner, however, reserves the right to modify or elaborate on its proposed

constructions and to raise further claim construction issues in the parallel district court proceedings. Yang, ¶44.

The parties recently exchanged proposed claim constructions in the parallel district court proceeding. Exs. 2003-2004. The claim construction disputes in district court do not impact the issues raised in this Response.

A. “an isolation region of the substrate” (Claim 1) and “a substrate with an isolation structure” (Claim 15)

The terms “an isolation region of the substrate” and “a substrate with an isolation structure” should be construed as requiring that *the isolation [region/structure] is “part of” the substrate*. Yang, ¶45.

1. The Intrinsic Record Supports Construing the Terms to Mean That the Isolation Region/Structure Is “Part of” the Substrate

First, the ’378 claims support the construction that the isolation [region/structure] is “part of” the substrate. Rather than listing the “isolation [region/structure]” as its own claim limitation, the “isolation [region/structure]” is introduced only in reference to the recited substrate. Specifically, claim 1 recites “an isolation region of the substrate” and claim 15 recites “a substrate with an isolation structure.” Yang, ¶46.

Second, the ’378 specification also supports the construction that the isolation region/structure is “part of” the substrate. The ’378 consistently depicts the isolation

Figure 2:



The '378 repeatedly describes the isolation region/structure as part of the substrate. See, e.g., '378, 12:54-66 (“According to some embodiments, **substrate 202 includes isolation regions or structures**, like STI structure 233 shown in FIG. 4.”), 20:38-42 (“In some embodiments, a 3D memory device includes a semiconductor substrate, an alternating layer stack disposed on the semiconductor

substrate, and a dielectric structure, extending vertically through the alternating layer stack, on ***an isolation region of the substrate***”), 21:64 (“an isolation region in the substrate”), 22:27-28 (“In some embodiments, a 3D memory device includes ***a substrate with an isolation structure***”). Yang, ¶48.

In the Institution Decision, the Board took the position that the isolation region/structure may “extend[] completely through the substrate” (DI, 15), but the Board’s statements are contrary to the ’378 specification, which does not support an interpretation that the isolation region/structure can extend vertically through the full depth of the substrate, but is not “part of” the substrate. For example, the specification nowhere discloses an isolation region/structure through a cut entirely through the substrate. This at most is creating a structure that is next to or abuts the substrate, but is not “with” or “of” the substrate. Yang, ¶49.

Thus, the terms “an isolation region of the substrate” and “a substrate with an isolation structure” should be construed as requiring that the isolation region/structure is “part of” the substrate. The terms do not encompass structures that extend vertically through the full depth, but are not “part of,” of the substrate. Yang, ¶50.

2. “Part of” Does Not Encompass an Isolation Region/Structure That Is Merely “on” the Substrate, and Even if It Did, the “on” Spatial Relationship Is Defined in the Vertical Direction

The Board in the first IPR for the ’378 (IPR2024-00788) appeared to agree in its Institution Decision that the isolation region/structure is part of the substrate, but took the preliminary position that an isolation structure could be located “on” the substrate in any position relative to the substrate. Ex. 2012, 12-13 (“Taken together, these passages of the ’378 patent indicate that for a substrate having additional layers or structures added or disposed thereon, such layers or structures could be considered part of, or ‘with’ the substrate.”). In this proceeding, however, the Board does not discuss an “on” relationship” in connection with “part of” or “with.” Yang, ¶51.

To the extent the Board still holds its earlier view that “part of” or “with” includes structures that are merely “on” the substrate, this interpretation is inconsistent with the claim language, which specifically invokes the term “with” and “of” (i.e., part of) rather than “on.” Indeed, the Board’s preliminary interpretation would lead to the result that any components or layers positioned “on” the substrate would become “part of” the substrate such that the entire memory device would be subsumed by this unreasonably broad interpretation. For example, the alternating conductor/dielectric layer stack is disposed “on” the substrate (’378, Abstract, 22:27-29), which under the Board’s preliminary interpretation, would somehow become a ***part of*** the substrate. Yang, ¶52. Essentially, the Board’s preliminary interpretation

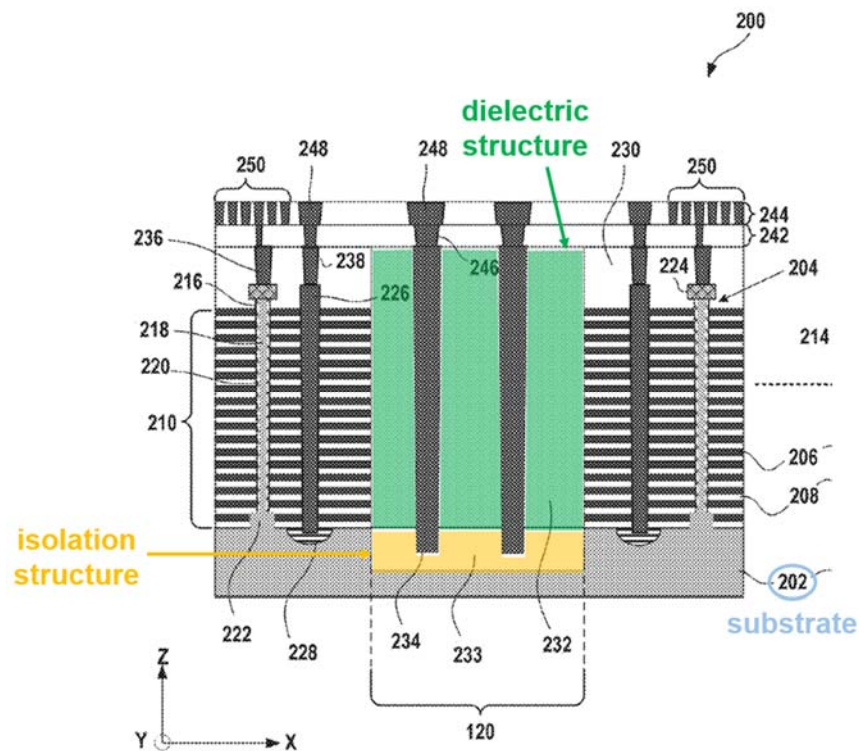
would render the claim language superfluous, which is “highly disfavored.” See *Wasica Fin. GmbH v. Cont’l Auto. Sys., Inc.*, 853 F.3d 1272, 1288 n.10 (Fed. Cir. 2017) (“It is highly disfavored to construe terms in a way that renders them void, meaningless, or superfluous.”).

The Board in the first IPR for the ’378 quoted a passage from the specification stating that an “STI structure 233 is formed on a top portion of substrate 202 and filled with a dielectric material” (Ex. 2012, 12 (citing ’378, 10:30-40)), but in the context of this discussion, “on a top portion of [the] substrate” is referring to removing a part of the substrate, which is then “filled with a dielectric material,” so as to form the “STI structure” “on a top portion of [the] substrate.” ’378, 10:30-44. Thus, this teaching of the specification supports the claim’s recitation of “with” or “of” (i.e., part of) instead of “on,” consistent with the other portions of the specification discussed above. Nothing in the specification suggests that the STI structure is merely “on” the substrate. Yang, ¶53.

Even if, *arguendo*, the term “with” or “of” could somehow be interchanged with the term “on,” which it cannot, the term “on” means “above” in the z-direction (the vertical direction) when the substrate is positioned in the lowest plane of the semiconductor device and thus precludes any other reorientations. The specification expressly defines the term “on” in this way:

As used herein, whether one component (e.g., a layer or a device) is “on,” “above,” or “below” **another component** (e.g., a layer or a device) **of a semiconductor device** (e.g., 3D memory device 200) **is determined relative to substrate 202 in the z-direction (the vertical direction) when the substrate is positioned in the lowest plane of the semiconductor device in the z-direction.**

'378, 7:37-43. The specification likewise describes and shows the isolation structure as above the substrate. For example, Figure 2 shows the isolation structure above the substrate:



'378, Fig. 2 (annotated and excerpted); see also '378, 10:37-38 (“...STI structure 233 is formed on a top portion of substrate 202...”), 12:66-67 (“STI structure 233 in FIG. 4 can be formed on a top portion of substrate 202.”), 20:40-42 (“...a dielectric

structure, extending vertically through the alternating layer stack, on an isolation region of the substrate”), Figs. 4-13. Yang, ¶54.

Patent Owner’s interpretation of “on” is also consistent with the vertically-oriented description of the ’378’s claimed “three-dimensional (3D) memory device.” The “three-dimensional (3D) memory device” of the claim is described as “refer[ring] to a semiconductor device with vertically-oriented strings of memory cell transistors (referred to herein as “memory strings,” such as NAND strings) *on* a laterally-oriented substrate so that the memory strings extend in the vertical direction with respect to the substrate.” ’378, 5:24-29. The ’378 explains that “the term ‘vertical/vertically’ means nominally perpendicular to the lateral surface of a substrate.” *Id.*, 5:29-31; *see also* Ex. 2007 (Depo. Tr. of Dr. Lee (Petitioner’s expert)), 64:5-12 (“‘Vertically’ means 90 degree with respect to the orientation of the substrate.”). Therefore, in the context of the ’378, a component being on another component requires the former to be vertically above the latter, where the vertical direction is the direction perpendicular to the substrate. Yang, ¶55.

In contrast, the ’378 uses the terms “abut” and “on the side” to indicate a horizontal spatial relationship. For example, the alternating dielectric/conductor stack “abuts” a sidewall of the dielectric structure. ’378, 20:42-45. While “on the side” includes the word “on” and refers to a horizontal spatial relationship, the term

“on” by itself is never used to indicate a lateral or other relationship besides above. Yang, ¶56.

The Board cited disclosures from the ’378 and preliminarily concluded that “a structure will be considered to be on the substrate even if it is not on the substrate in the displayed orientation so long as it is on the substrate in any possible rotation.” Ex. 2012, 12-13 (citing ’378, 4:34-40). The cited passage states:

The spatially relative terms are intended to encompass ***different orientations of the device in use or operation*** in addition to the orientation depicted in the figures. ***The apparatus may be otherwise oriented*** (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.

’378, 4:34-40. Yang, ¶57.

This passage merely ensures that the orientation of ***the entire device (“the apparatus”)*** may be rotated “***in use or operation***” while remaining within the scope of the claims—it does not change the claimed relative spatial relationships between the components within the device. This is also consistent with how the vertical direction is used within the ’378 as the direction perpendicular to the substrate. For example, if the entire vertically-oriented memory device shown in Fig. 2 were rotated 90 degrees, the isolation structure is still above the substrate because the vertically-oriented direction has been rotated by 90 degrees along with the substrate. As this example illustrates, ***the spatial configuration of various components within***

this device itself has not changed, and the same isolation structure is still “on” the substrate. The word “on” is “interpreted accordingly” to account for the rotation and the vertically-oriented direction of the whole 3D memory cell device. Yang, ¶58.

Accordingly, the cited disclosure does not support an interpretation that regardless of the orientation of the z-axis in reference to the substrate, any two components can be deemed to be “on” each other after “a possible rotation” is made to reorient these two components. Indeed, Petitioner’s expert, Dr. Lee, conceded that this interpretation is so broad that “any layers or any structure in the device perhaps can be considered on other layers or any structures of the device.” Ex. 2007, 45:10-47:5; *see generally* Ex. 2007, 33:1-47:5. Such an interpretation would thus render the patentee’s choice of terms such as “with” or “of” meaningless, if those terms are read as encompassing “on” under such a broad interpretation of that term. Yang, ¶59.

Thus, the terms “an isolation region of the substrate” and “a substrate with an isolation structure” do not encompass regions/structures that are merely positioned “on” the substrate, and even if did, that would not permit reorienting the direction of the “on” spatial relationship to encompass any relative position. Yang, ¶60.

B. “the dielectric and the isolation structures” (Claim 15)

The phrase “the dielectric and the isolation structures” in “through array contacts (TACs) extending vertically through the dielectric and the isolation structures” should be construed, consistent with its antecedent terms, as “the dielectric structure and the isolation structure.” In other words, the term refers back to the same “dielectric structure” and the same “isolation structure” recited earlier in the claim. Yang, ¶61.

The phrase “the dielectric and the isolation structures” in [15.h] has its antecedent basis in “a dielectric structure” and “an isolation structure” from [15.a] and [15.c], confirming that the phrase is simply shorthand for “the dielectric structure” and “the isolation structure.” There are no other terms in the claim, aside from “a dielectric structure” and “an isolation structure,” that could provide the necessary antecedent basis for “the dielectric and the isolation structures.” Yang, ¶62.

The claim language is plural (“the dielectric and the isolation **structures**”) because it refers to both the isolation structure and the dielectric structure. The antecedent for these terms is “a dielectric structure” and “an isolation structure”—not multiple dielectric structures or multiple isolation structures as these are not recited earlier in the claim. An example of the claimed configuration is shown in Fig. 2 of the ’378.

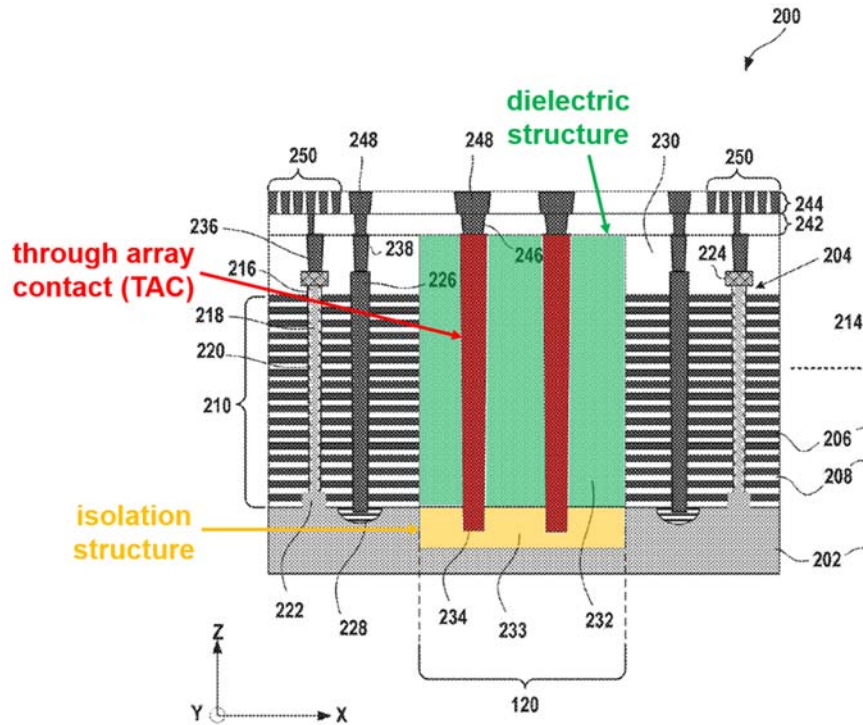


FIG. 2

'378, Fig. 2 (annotated and excerpted). As shown in the figure, a plurality of TACs extend through the same dielectric structure and the same isolation structure. Yang, ¶63.

While the claims do not preclude multiple dielectric structures or multiple isolation structures, the limitation “through array contacts (TACs) extending vertically through the dielectric and the isolation structures” requires that the plurality of TACs extend through at least one particular dielectric structure and one particular isolation structure—i.e., the previously recited dielectric structure and isolation structure—regardless of whether additional dielectric structure or isolation structures are also present in the device. Yang, ¶64.

Patent Owner respectfully submits that the Board’s preliminary analysis in its Institution Decision in the first IPR for the ’378 misinterprets the claim language.

The DI of the first IPR states:

Limitation [15.H] requires TACs (multiple) extending through “the dielectric and the isolation structures” (multiple). Being plural, the phrase “the dielectric and the isolation structures” is not limited to a single dielectric and a single isolation structure; it may include multiple dielectric structures and/or multiple isolation structures.

Ex. 2012, 23. As discussed above, the claims and specification support construing this term as referring to the same specific dielectric structure and isolation structure previously recited in the claim, rather than multiple dielectric structures and/or multiple isolation structures. For example, the claims would not encompass each of the TACs extending through different dielectric structures instead of the same dielectric structure. Yang, ¶65.

The Board’s reliance on “a single TAC extending through a single respective dielectric structure” (Ex. 2012, 23 (citing ’378, 21:17–25)) is misplaced. The cited passage states:

The method also includes filling the opening with a dielectric layer to form a dielectric structure as a TAC region of the 3D memory device, removing portions of the dielectric structure and the isolation structure until the substrate is exposed to form a TAC opening that vertically extends through the dielectric structure and the isolation structure, and

filling the TAC opening with a conductor to form a TAC structure in the TAC region, wherein the TAC structure is in contact with the substrate.

'378, 21:17–25. This passage describes the formation of a single TAC, not a plurality of TACs that extend through the dielectric structure and the isolation structure as claimed. The cited passage does not support an interpretation that each TAC in a group of TACs may extend through separate, discontinuous dielectric structures. As discussed above, the specification consistently describes and depicts the **plurality of TACs** as extending through the same dielectric structure. Regardless, even if the Board's interpretation of this passage were correct (respectfully, it is not), a claim need not be construed to encompass all disclosed embodiments. As explained, claim 15 is directed to a plurality of TACs that extend through a dielectric structure, for example as shown in Fig. 2 of the '378. Yang, ¶166.

Under the correct interpretation of “the dielectric and isolation structures” as “the dielectric structure and the isolation structure,” limitation [15.h] requires that multiple TACs extend through the same dielectric structure. The Federal Circuit has made clear that even if the claims cover “one or more” of an element, there must still be at least one instance of the element, e.g., in the accused system or the prior art, that meets all the requirements of the claim for that element. *See Finjan LLC v. SonicWall, Inc.*, 84 F.4th 963, 974-975 (Fed. Cir. 2023) (“Even if an infringing system can use ‘one or more computers,’ the plain language of the claims requires

at least one of those computers to perform all the functions listed in the claims of the ARB Patent.”). Here, the claim requires that a single “dielectric structure” must have multiple “through array contacts (TACs) extending vertically through” it. Yang, ¶67.

C. “each local contact of the local contacts” (Claim 18)

The term “each local contact of the local contacts” of claim 18 should be construed, according to its plain and ordinary meaning, as referring to the “local contacts disposed on the channel structures *and the slit structures*” as recited in independent claim 15, from which claim 18 depends. The Board should reject Petitioner’s attempt to limit “each local contact of the local contacts” to only some of the claimed local contacts—those disposed on the channel structures. Yang, ¶68.

The claim language compels Patent Owner’s construction. Claim 18 recites “each local contact of the local contacts” (limitation [18.a]), and the antecedent basis for this term is independent claim 15’s recitation of “local contacts disposed on the channel structures and the slit structures” (limitation [15.g]). Moreover, there is nothing in the phrase “each local contact of the local contacts” to limit it to merely a subset of the previously recited local contacts. Thus, “*each* local contact of the local contacts” refers to *all* of the local contacts that are mapped to satisfy the “local contacts” of limitation [15.g], including those above the slit structures as well as

those above the channel structures. *See ResONet.com, Inc. v. Lansa, Inc.*, 346 F.3d 1374, 1379 (Fed. Cir. 2003) (defining “each” as “each and every”); Yang, ¶69.

Petitioner also filed an IPR (IPR2024-00911) of U.S. Patent No. 10,937,806 (the ’806 patent; Ex. 2008), which is a continuation of the ’378 patent, and in its Preliminary Reply, argued that the same term refers to only the “local contacts disposed on the ... channel structures” and not the “local contacts disposed on ... the slit structures” (Ex. 2009, 1), but this construction is contrary to the express language of the claim and ignores the antecedent basis for the term. Just like for the ’806, to satisfy claim 18 of the ’378, which recites “***an etch stop plug interposed between each local contact of the local contacts and each channel structure of the channel structures,***” it is not sufficient to show an etch stop plug interposed between “***some*** local contacts” of the local contacts and each channel structure of the channel structures—rather the claim recites “***each*** local contact.” Petitioner’s interpretation, therefore, improperly reads out the term “each.” *Merck & Co. v. Teva Pharms. USA, Inc.*, 395 F.3d 1364, 1372 (Fed. Cir. 2005) (“A claim construction that gives meaning to all the terms of the claim is preferred over one that does not do so.”); Yang, ¶70.

In arguing for its erroneous construction, Petitioner mischaracterizes Patent Owner’s position as requiring “an etch stop plug interposed between each local contact of the local contacts and each channel structure of the ... channel structures

[and each of the slit structures].” Ex. 2009, 3-4. Patent Owner proposes no such additional limitation. Claim 18 requires an etch stop plug located between two things: (1) each local contact of the local contacts and (2) each channel structure of the channel structures. The parties are in agreement regarding the scope of (2)—i.e., the channel structures. Instead, it is the scope of “each local contact of the local contacts” that is at issue. The antecedent for this term supports Patent Owner’s construction, and so no modification of the claim language of claim 18 is necessary (unlike Petitioner’s construction). Yang, ¶71.

Petitioner argues that the claim language supports its construction because the etch stop plug is “between” the local contacts and the channel structures, which is “referring to an area for the etch stop that is above the channel structure and beneath the local contact” (Ex. 2009, 4), but this argument is based on an incorrect assumption that it is not possible to have an etch stop plug between the channel structures and the local contacts disposed on the slit structures. Similarly, Petitioner incorrectly argues that the claims require that “[o]nly the local contacts for the channel structures are above the channel structures.” Ex. 2009, 4. The claims never recite this limitation—nor is there any support for reading such a negative limitation into the claims. There is nothing precluding a local contact from being above both the channel structures and the slit structures. Yang, ¶72.

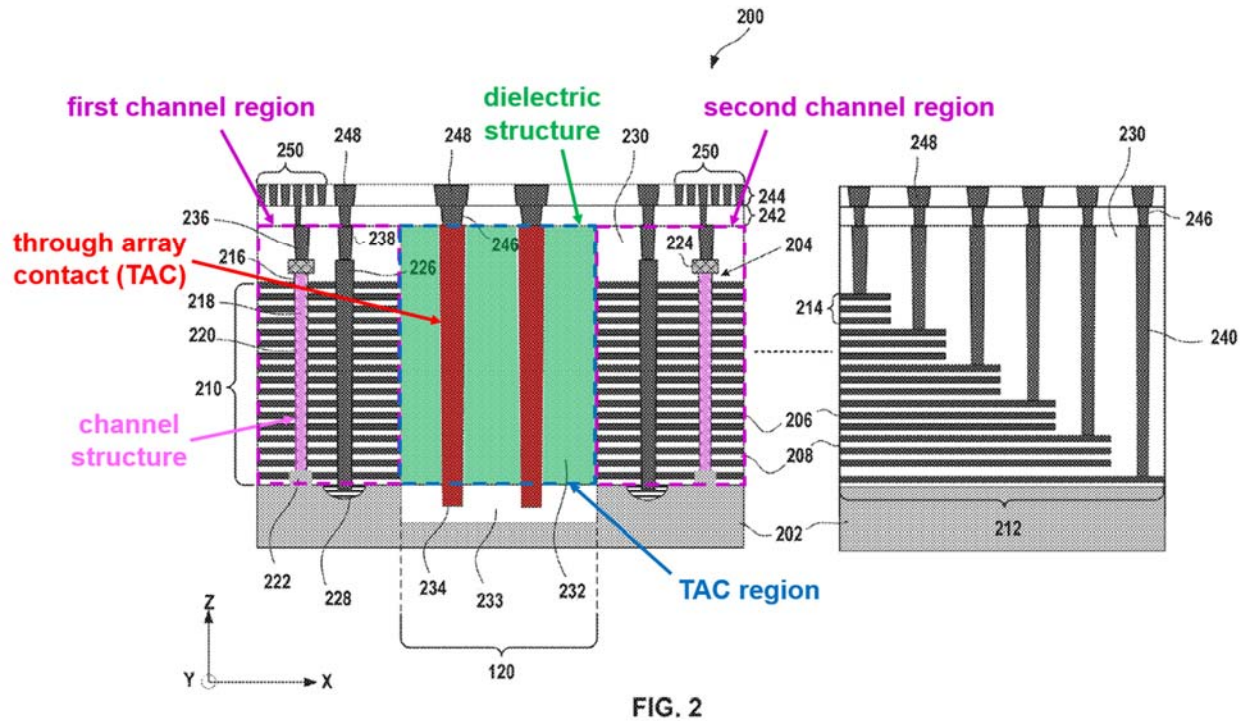
As one example of a structure that would read on claim 18 as properly construed, a “local contact” may be disposed on both a channel structure and a slit structure, with an etch stop plug in between the local contact and the channel structure. The ’378 limitation [15.g], which introduces the term “local contact,” recites “local contacts disposed on the channel structures and the slit structures,” which does not require a local contact to be disposed **only** on a channel structure or **only** a slit structure—it may be disposed on both. Yang, ¶73.

The ’378 specification provides such examples (discussed below), and does not limit the meaning of the term “local contact” to exclude local contacts that are disposed on both a channel structure and a slit structure. The ’378 does not expressly define the term “local contact,” but provides several examples of local contacts. ’378, 11:20-24, 11:27-30. The closest the ’378 comes to a definition of “local contact” is as follows:

The contacts are referred to herein as “local contacts” because they are in direct contact with the memory array structures, and further because they are formed within dielectric layer 230. ... As used herein, the term “contact” can broadly include any suitable types of interconnects including vertical interconnect access (via) lines and lateral lines (interconnect lines).

’378, 11:20-30. However, this passage does not define the outer boundaries of the term “local contact” because, for example, the ’378 also describes **TACs 234** as local

contacts ('378, 11:26-27) even though they are formed in **dielectric structure 232** instead of dielectric layer 230.



'378, Fig. 2 (annotated). Furthermore, as the above quote indicates, “contacts” can be “lateral lines (interconnect lines)” and thus a local contact may be disposed on two or more “memory array structures” such as channel structures and slit structures. For example, the '378 discloses such lateral contacts in the form of “interconnect contacts 248,” e.g. “bit lines 250, which are electrically connected to NAND strings” (channel structures) in the NAND string region. '378, 12:4-9. As illustrated in the figure below, which has been annotated to show an example bit line, a bit line

extends along the “bit line (BL) direction” in the NAND string region 110 and therefore is disposed on channel structures as well as slit structures.² '378, 5:60-67.

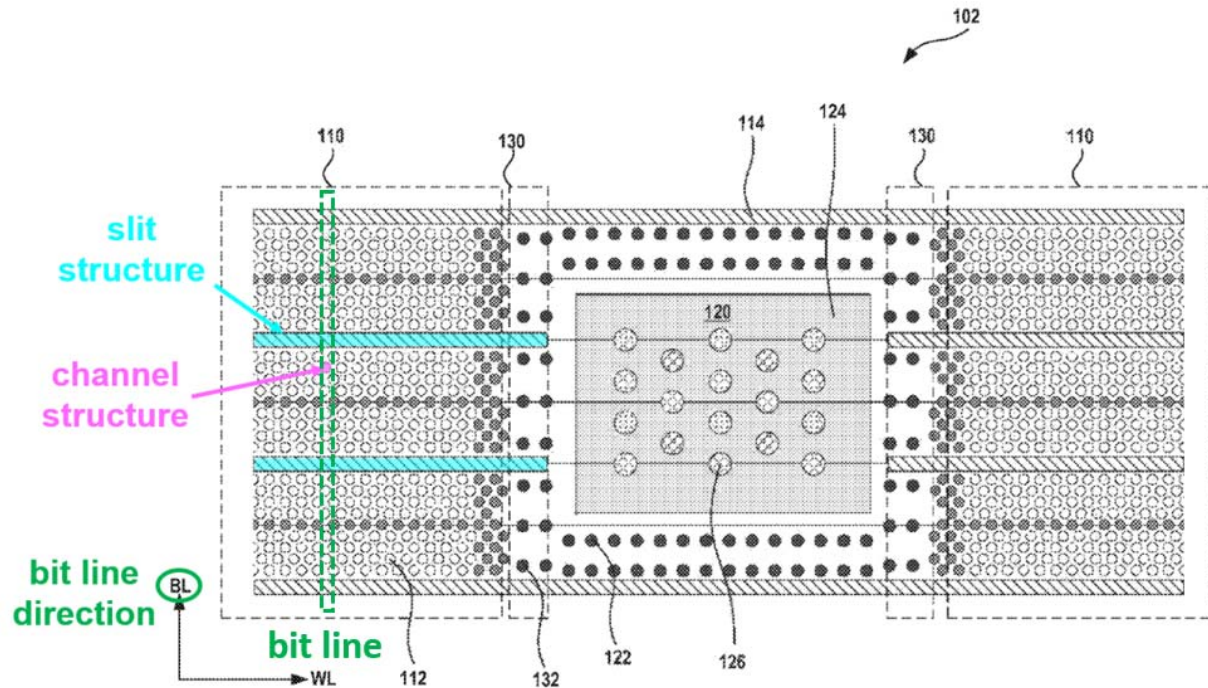


FIG. 1A

'378, Fig. 1A (annotated). Yang, ¶74.

Dr. Lee's testimony also confirms that an interconnect such as a bit line is a local contact in the context of the '378 specification:

² The bit line green dotted box had been added to the figure. The precise placement of the bit line in the NAND string region does not matter because the location of the slit structures and channel structures means that the bit lines will be disposed over both. Yang, ¶74.

So in column 11 line 15, around 15, it says that ***local contact is essentially provide*** [sic] ***a conducting layer with memory array structures***, such as the NAND string 204, S-T-R-I-N-G-S, 204, slit structures 226, conductive layer or word line 206, and the staircase structure 212. So ***the local contact basically is an interconnect to connect the memory array structure to, for example, external – external input, outputs.***

Ex. 2007, 66:11-14 (emphasis added). Yang, ¶75.

For all of these reasons, the Board’s preliminary conclusion in its Decision on Institution for IPR2024-00911 that “the plain and ordinary meaning of ‘each local contact’ ... refer[s] to each channel structure local contact and not to each slit structure local contact” (Ex. 2011, 12) is inconsistent with claims and specification. Specifically, the Board repeatedly assumed that there must be two separate types of local contacts—“slit structure local contacts” and “channel structure local contacts” (Ex. 2011, 12)—even though those terms are not recited in the claims, and the Board did not consider that the above-described lateral local contacts located above ***both*** the slit and channel structures, as disclosed in the specification, would read on the claims. Similarly, the Board incorrectly concluded that “the slit structure local contact is not located above a channel structure,” which again wrongly assumes that there must be separate “slit structure local contacts” and “channel structure local contacts.” A local contact located on a slit structure may also be located on a channel structure, as illustrated above. Yang, ¶76.

Accordingly, the term “each local contact of the local contacts” of claim 18 should be construed, according to its plain and ordinary meaning, as referring to the “local contacts disposed on the channel structures and the slit structures,” as recited in claim 15. Yang, ¶77.

VI. BACKGROUND OF THE ASSERTED PRIOR ART³

A. U.S. Patent Publication No. 2017/0179026 (“Toyama”) (Ex. 1005)

Petitioner does not contend that Toyama anticipates the Challenged Claims, and instead argues only that it renders obvious the Challenged Claims in view of the knowledge of a POSITA. Pet. 18, 34-103. Yang, ¶78.

Toyama teaches a 3D NAND memory device with four exemplary structures and their modifications. Ex. 1005, [0004]. Only two of these exemplary structures are relied on by Petitioner: (1) “the ‘first exemplary structure,’ illustrated in Figures 1A-B to 17A-F,” and (2) “the ‘second modification of the fourth exemplary structure,’ illustrated in Figures 44A-B to 49.” Pet. 31. Yang, ¶79.

Toyama’s first exemplary structure includes, among other elements: “**semiconductor substrate 9**” (Ex. 1005, [0163]); “**planar semiconductor material layer 10**” (Ex. 1005, [0170]); “**alternating stack (132, 146, 232, 246)**”

³ For the purposes of the present IPR proceeding only, Patent Owner does not contest that the Toyama qualifies as prior art to the ’378.

(Ex. 1005, [0232]); “**channels**” (Ex. 1005, [0211]); “**laterally-elongated contact via structures 76**” (Ex. 1005, [0236]); “**drain contact via structures 88**” (Ex. 1005, [0241]); “**source connection via structures 91**” (Ex. 1005, [0250]); “**dielectric fill material portion 430**” (Ex. 1005, [0216]); and “**through-memory-level via structures 488**” (Ex. 1005, [0244]). A cross-section view of Toyama’s first exemplary structure is below.

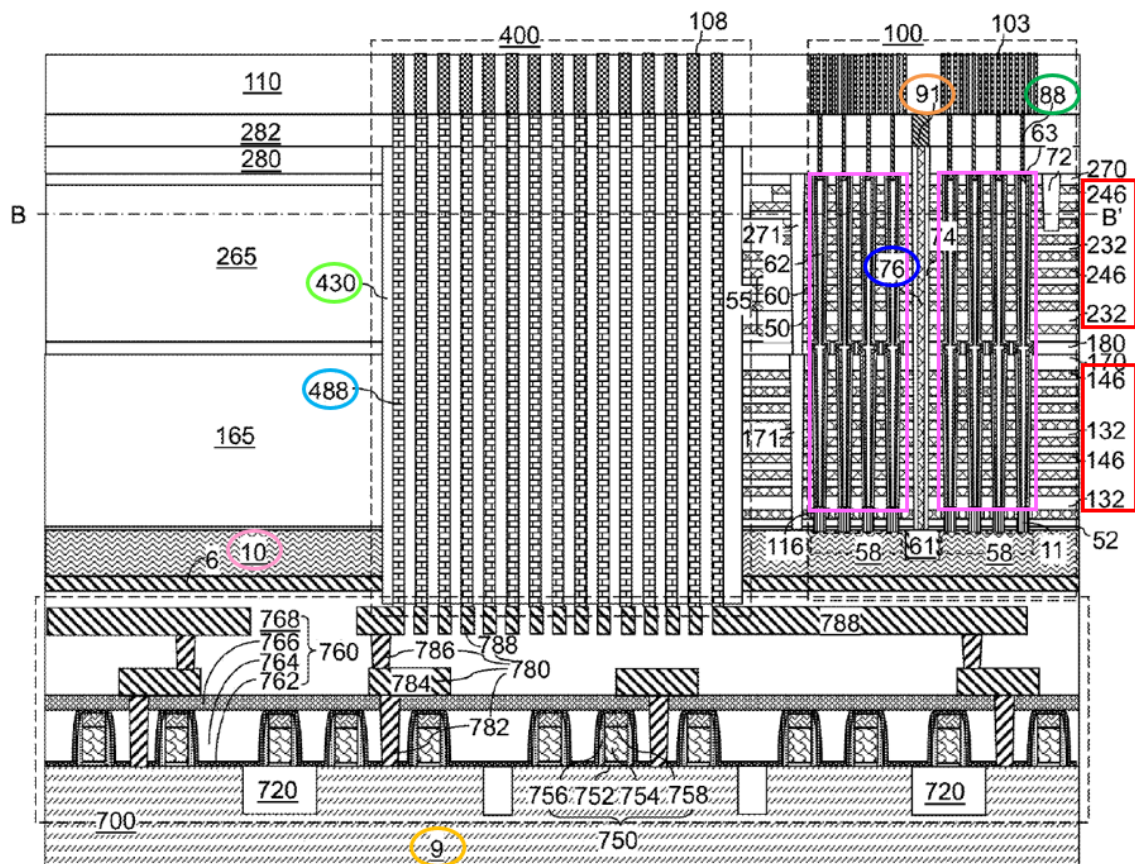


FIG. 17A

Ex. 1005, Fig. 17A (annotated). Yang, ¶80.

In Toyama’s first exemplary structure, **dielectric fill material portion 430** forms a hole in **planar semiconductor material layer 10**, which allows **through-**

memory-level via structures 488 to form vertical interconnects. Toyama's planar semiconductor material layer 10 lacks the claimed isolation structure. While Toyama's semiconductor substrate 9 seems to comprise "shallow trench isolation structures 720," they do not host through-memory-level via structures 488 or similar via structures. Yang, ¶81.

Toyama's second modification of the fourth exemplary structure includes, among other elements: "semiconductor substrate 9" (Ex. 1005, [0163]); "planar semiconductor material layer 10" (Ex. 1005, [0170]); "alternating stack (132, 146, 232, 246)" (Ex. 1005, [0232]); "channels" (Ex. 1005, [0211]); "laterally-elongated contact via structures 76" (Ex. 1005, [0236]); "drain contact via structures 88" (Ex. 1005, [0241]); "insulating liners 674" (Ex. 1005, [0340]); and "through-memory-level via structure 676" (Ex. 1005, [0341]). A cross-section view of Toyama's second modification of the fourth exemplary structure is below.

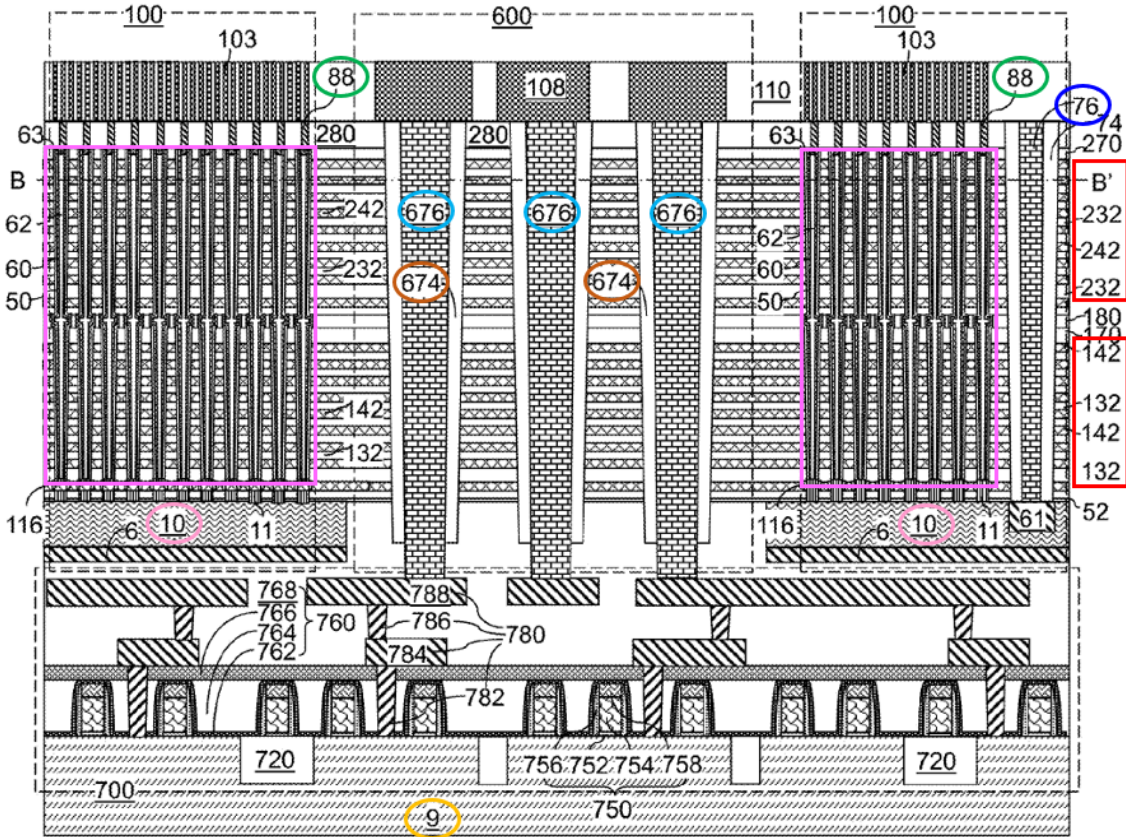


FIG. 49

Ex. 1005, Fig. 49 (annotated).⁴ Yang, ¶82.

⁴ Petitioner states: “In a clear typographical error, Figure 49 labels its alternating conductor/dielectric layer stack as elements 132, 142, 232, 242. Elements 142, 242 are ‘sacrificial material layers’ which, in a process step prior to Figure 49, were removed and replaced with ‘electrically conductive layers (146, 246).’ Toyama, [0337], [0340].” Pet. 39. Patent Owner does not challenge this assertion for purposes of the POR. Yang, ¶82.

In Toyama's second modification of the fourth exemplary structure, Toyama's **planar semiconductor material layer 10** again lacks an isolation structure. In addition, **through-memory-level via structures 676** are not formed through a dielectric structure; instead, they are formed through **alternating stack (132, 146, 232, 246)** and as a result, they require separate **insulating liners 674** around each individual **through-memory-level via structure 676**. Yang, ¶83.

VII. GROUND 1A: TOYAMA'S FIRST EXEMPLARY STRUCTURE DOES NOT DISCLOSE OR RENDER OBVIOUS CLAIMS 1-7 AND 18

In Ground 1A, Petitioner relies on Toyama's First Exemplary Structure as allegedly rendering obvious all Challenged Claims (Pet. 34-103), but Petitioner fails to show that Toyama's First Exemplary Structure discloses or renders obvious three separate groups of independent claim limitations: (1) "***an isolation region of the substrate***" [1.c.ii] and "***a substrate with an isolation structure***" [15.a], (2) "***a dielectric structure on [a/the] isolation [region/structure]***" [1.c.i-ii]/[15.c.i], and (3) "***[one or more] through array contacts (TACs) extending vertically through the dielectric and the isolation structures***" [1.d]/[15.h]. In addition, Petitioner fails to show that Toyama's First Exemplary Structure discloses or renders obvious the additional limitations of claim 7, which depends from claim 1 and further requires "***the dielectric structure defines a through array contact region within the 3D memory device,***" and claim 18, which depends from claim 15 and further requires

“an etch stop plug interposed between each local contact of the local contacts and each channel structure of the channel structures.” Yang, ¶84.

A. Independent Claims 1 and 15: Toyama’s First Exemplary Structure Does Not Disclose or Render Obvious Limitations [1.c.ii]/[15.a], [1.c.i-ii]/[15.c.i], and [1.d]/[15.h]

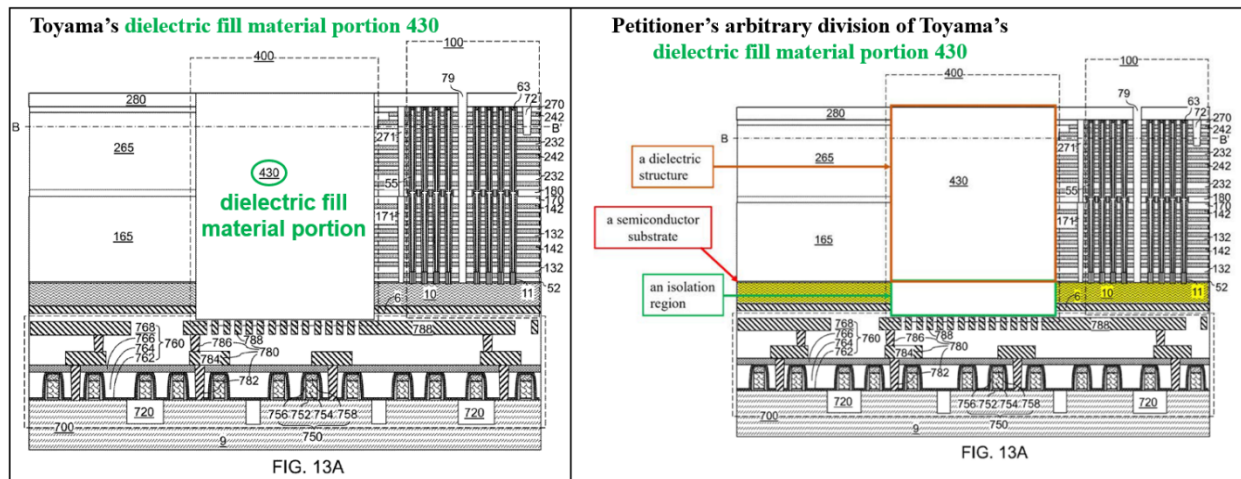
1. Petitioner Fails to Show That Toyama’s First Exemplary Structure Discloses or Renders Obvious “an Isolation Region of the Substrate” (Limitation [1.c.ii]) / “a Substrate With an Isolation Structure” (Limitation [15.a])

Toyama’s First Exemplary Structure does not disclose or render obvious *“an isolation region of the substrate”* as required by limitation [1.c.ii] or *“a substrate with an isolation structure”* as required by limitation [15.a] because the feature of Toyama that Petitioner maps to the “isolation [region/structure]” is, at most, located in the region of a cut through the alleged substrate, and is not “part of” the substrate as required under the proper construction of this term. Yang, ¶85.

As discussed in §V.A, claim 1 requires “an isolation region **of** the substrate” and claim 15 requires “a substrate **with** an isolation structure,” which means that the isolation region/structure is **part of** the substrate. This construction of the term does not encompass a structure that extends all the way through the substrate, which is merely next to or abutting, but not part of, the substrate. And as further discussed in §V.A, even if the term “with” is construed as encompassing “on,” the term “on” means “above” in the z-direction (the vertical direction) when the substrate is positioned in the lowest plane of the semiconductor device in the z-direction, and

the patent does not permit reorienting the direction of the “on” spatial relationship to encompass any relative position between components. Yang, ¶86.

Toyama’s First Exemplary Structure includes “dielectric fill material portion 430,” which Petitioner divides into two parts, one of which it then maps to the isolation region/structure of the ’378. Pet. 47-54.



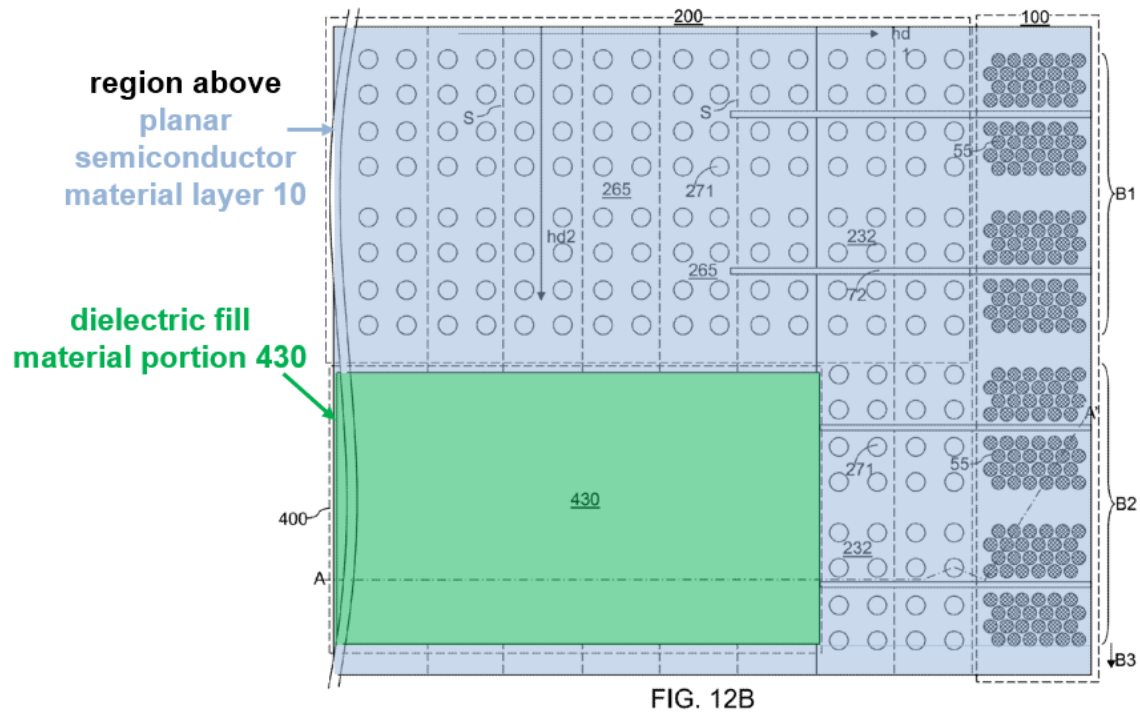
Ex. 1005, Fig. 13A (left image annotated by Patent Owner; right image showing Petitioner’s annotation at Pet. 51, with top heading added by Patent Owner). Yang, ¶87.

Petitioner’s alleged isolation region/structure (lower part of “dielectric fill material portion 430”) is not part of the alleged substrate (“planar semiconductor

material layer 10”).⁵ Petitioner argues that “Toyama’s isolation region [...] **is formed by removing and is surrounded by** substrate [...]” and “the isolation region is within the substrate and isolates portions of the substrate from one another” (Pet. 52 (emphasis original) (citing Ex. 1003, ¶ 131 which repeats the same language); Pet. 93 (cross-referencing the claim 1 analysis for claim 15), but Petitioner’s arguments are misplaced. Yang, ¶88.

As a preliminary matter, Petitioner’s assertion that Toyama’s First Exemplary Structure’s alleged isolation region/structure “is surrounded by” its alleged substrate is unfounded. Toyama’s relevant figures (Figs. 1A-B to 17A-F) do not depict that dielectric fill material portion “430” is surrounded by other regions. As can be seen below, 430 is shown to extend all the way to the left.

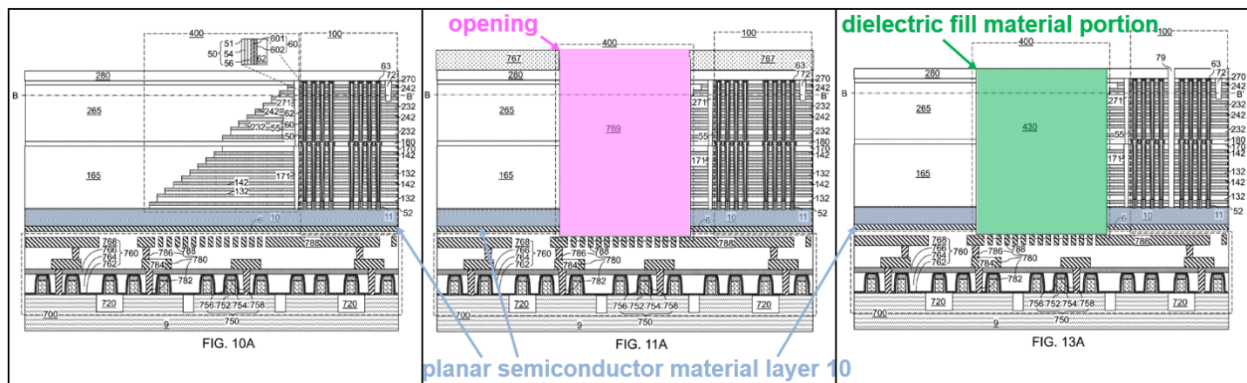
⁵ For the purposes of this POR, Patent Owner does not dispute Petitioner’s mapping of the claimed “substrate” to Toyama’s “planar semiconductor material layer 10” in Ground 1A.



Ex. 1005, Fig. 12B (annotated). Even if the alleged isolation region/structure were surrounded by the alleged substrate, that would not make it a part of the substrate, just as two structures that are merely adjacent would not meet this requirement. Yang, ¶89.

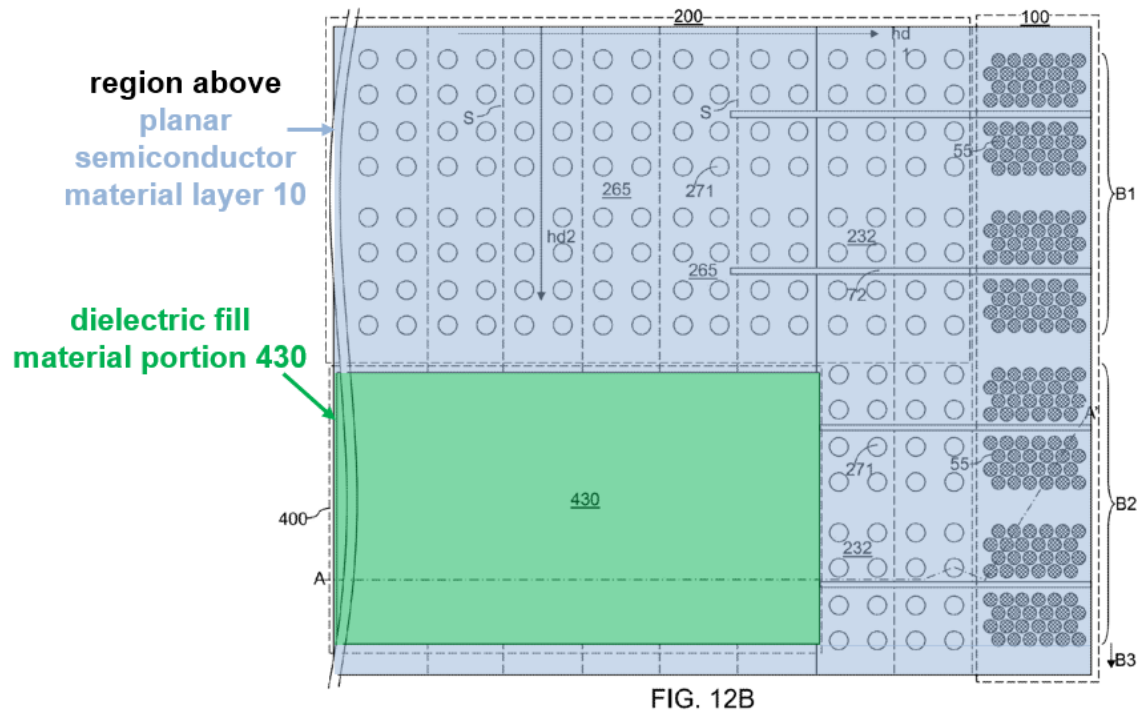
The fact that the opening is formed by removing the alleged substrate (Pet. 52) does not support Petitioner’s argument because after the substrate is removed there is no longer any portion of the alleged substrate in the relevant region. To further illustrate this, unlike the substrate of ’378, which spans the horizontal area of the memory device and “onto which subsequent material layers are added, or otherwise ‘disposed’” (’378, 4:41-43), Toyama’s “planar semiconductor material layer 10” is completely removed in the relevant region, and is **replaced** by “opening 769.” Ex.

1005, [0213]-[0215], Figs. 12A, 13A. After this step, there is simply no substrate in the region labeled “400.” *Id.*, Fig. 14A. As illustrated below, by forming “opening 769,” Toyama creates a region outside and merely abutting the alleged substrate (“planar semiconductor material layer 10”). It is in this newly opened space, where the alleged substrate has been entirely removed, that “dielectric fill material portion 430” is added. Thus, there is no alleged substrate “with” that dielectric fill material, or dielectric material “of” the substrate.



Ex. 1005, Figs. 10A, 11A, 13A (annotated). Moreover, these steps that Petitioner cites relate to the manufacturing process, not the final structure, and the Challenged Claims are apparatus claims. Yang, ¶190.

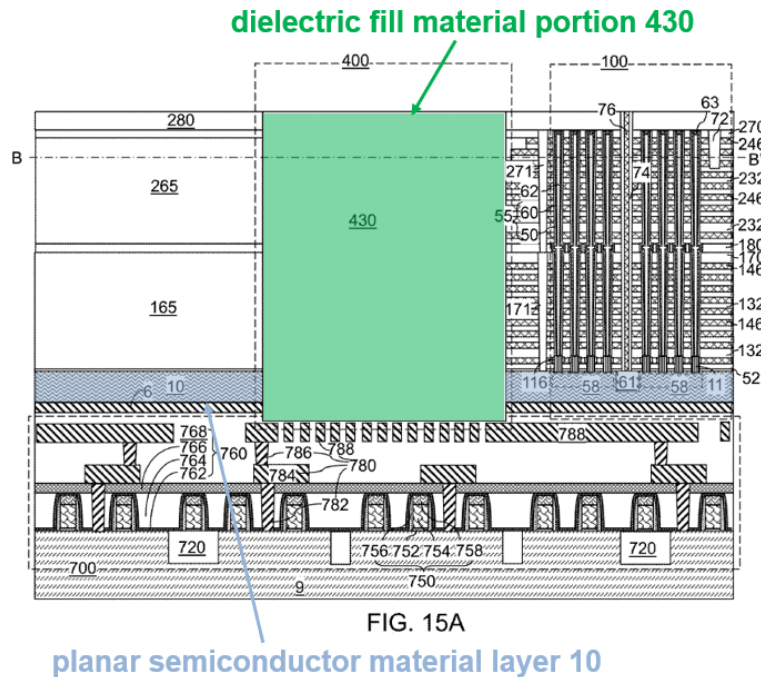
Finally, Petitioner’s assertion that “the isolation structure [...] isolates portions of the substrate from one another” (Pet. 52) is false. As seen in Toyama’s Fig. 12B, the alleged substrate is not divided into isolated portions; *i.e.* it remains connected. Therefore, the alleged isolation region/structure does not actually isolate portions of the alleged substrate from one another.



Ex. 1005, Fig. 12B (annotated). Yang, ¶91.

The Board in its Institution Decision preliminarily concluded that “on the current record,” the limitation “a substrate with an isolation structure” is taught by Toyama’s First Exemplary Structure, but, respectfully, the conclusion was based on its incorrect construction that “the claim requires only ‘an isolation region of the substrate,’ which does not restrict the region from extending through the substrate.” DI, 14-15. As discussed in §V.A, respectfully, this construction is incorrect—as properly construed, the limitation does not encompass an isolation structure that extends vertically through the full depth of, but is not part of, the substrate. Yang, ¶92.

The Board in its Institution Decision in the first IPR for the '378 further concluded that the term encompasses “an isolation structure ‘formed on’ the substrate, in which ‘on’ may be considered in any orientation of the device.” Ex. 2012, 15. But even if “a substrate with an isolation structure” encompassed an isolation structure that is merely “on” the substrate, Toyama’s alleged isolation structure is not “on” the alleged substrate because it is not “above” the substrate in the z-direction (the vertical direction) when the substrate is positioned in the lowest plane of the semiconductor device in the z-direction (*see* §V.A). The term “on” does not permit reorienting the direction of the “on” spatial relationship to encompass any relative position for the reasons discussed in §V.A, and so Toyama’s alleged isolation structure is not “on” the alleged substrate. Specifically, dielectric fill material portion 430 (the alleged isolation structure) is not “on” the alleged substrate because there is simply no alleged substrate below the alleged isolation structure, as shown in Figure 13A. None of the dielectric fill material is above the alleged substrate.



Ex. 1005, Fig. 13A (annotated). Yang, ¶93.

For all of these reasons, Toyama’s First Exemplary Structure does not disclose or render obvious “*an isolation region of the substrate*” as required by limitation [1.c.ii] or “*a substrate with an isolation structure*” as required by limitation [15.a]. Yang, ¶94.

2. Petitioner Fails to Show That Toyama’s First Exemplary Structure Discloses or Renders Obvious “a Dielectric Structure on [an/the] Isolation [Region/Structure]” (Limitations [1.c.i-ii]/[15.c.i])

Toyama’s First Exemplary Structure does not disclose or render obvious “*a dielectric structure on an isolation region*” as required by limitations [1.c.i-ii] or “*a dielectric structure on the isolation structure*” as required by limitation [15.c.i] because Petitioner arbitrarily and improperly divides Toyama’s single dielectric

structure into two regions and maps different regions to two separate features of the Challenged Claims: the “dielectric structure” and the “isolation [region/structure].” Yang, ¶95.

As an initial matter, for all the reasons explained in §VII.A.1, Toyama’s First Exemplary Structure does not disclose or render obvious the claimed isolation region/structure, and as a result, it does not disclose or render obvious the claimed dielectric structure on the isolation region/structure. Yang, ¶96.

Further, Petitioner’s only argument for this limitation is to improperly rely on the same substructure for two separate terms in the claim—the claimed dielectric structure and the claimed isolation region/structure. In the ’378, the dielectric structure is a separate structure on the isolation structure. This is expressly recited in the claims, and is shown, for example, in Figure 2 of the ’378 which illustrates the two separately claimed structures:

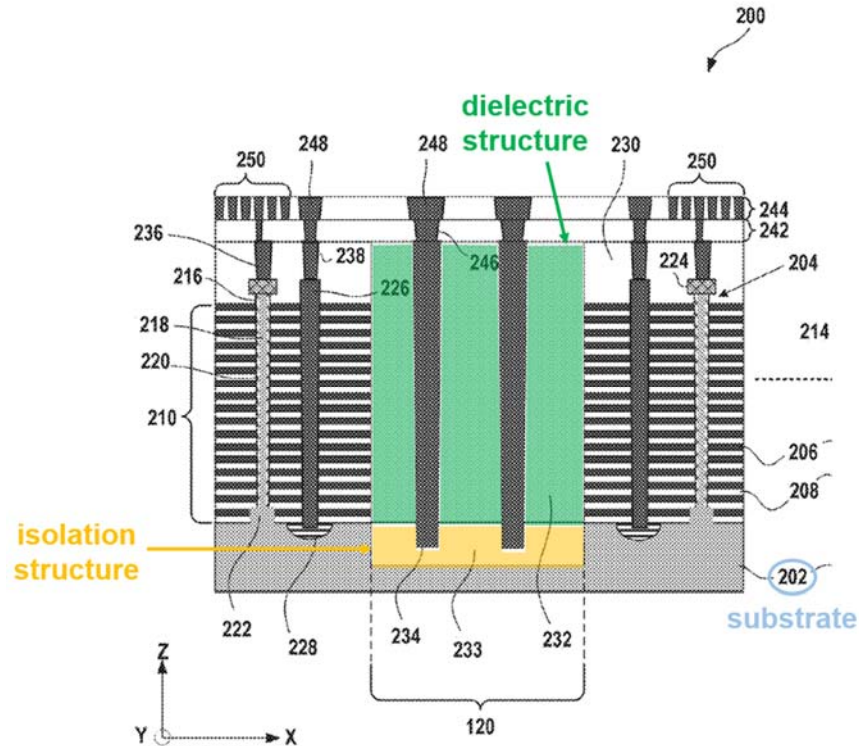
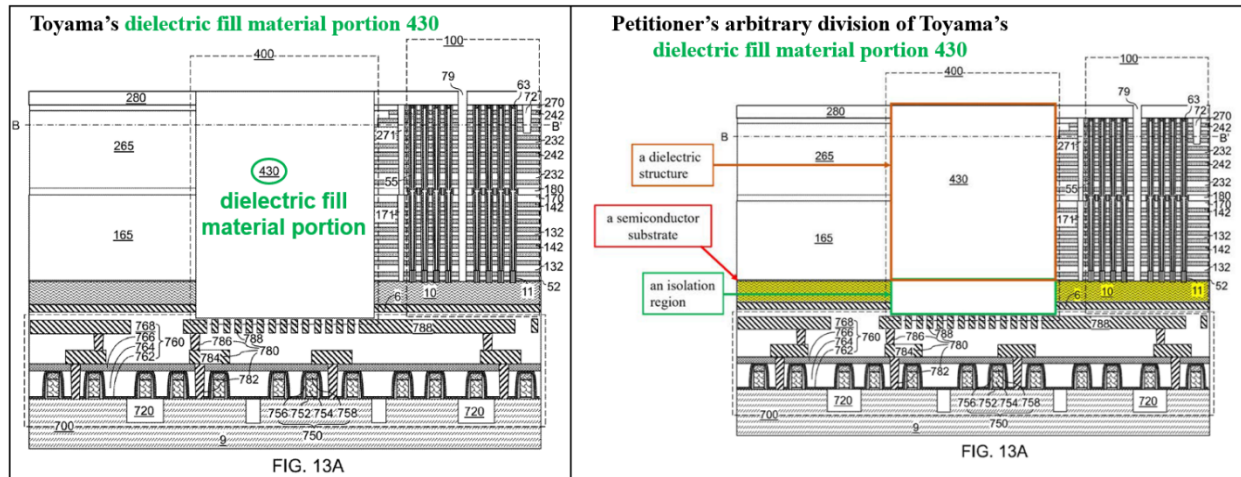


FIG. 2

'378, Fig. 2. Yang, ¶197.

In contrast, Toyama's First Exemplary Structure includes only a single "dielectric fill material portion 430," which, as illustrated below, Petitioner arbitrarily divides into two parts which it then maps to the separate dielectric structure and isolation region/structure of the '378. Pet. 47-54, 95.



Ex. 1005, Fig. 13A (left image annotated by Patent Owner; right image annotated by Petitioner at Pet. 51, with top heading added by Patent Owner). In Toyama, the “fill material portion 430” is a single integral structure. There are not two structures in Toyama and thus there is no dielectric structure that is “on” an isolation region/structure as required by the Challenged Claims. Yang, ¶98.

Petitioner asserts that the specification would not preclude the two structures from being formed during the same process step (Pet. 52), but the issue is not how the device is made, it is whether it has both a dielectric structure ***and*** an isolation region/structure with the claimed relationship—Toyama’s First Exemplary Structure does not. The ’378 consistently claims, describes, and depicts the isolation structure and the dielectric structure to be separate structures with a specific spatial relationship. ’378, 10:30-43, Figs. 2-13. For example, the dielectric structure is “formed so that it is aligned to or covers at least a portion of” the isolation structure (’378, 10:30-33); the dielectric structure is “in contact with” the isolation structure

(’378, 10:35-36); and the dielectric structure “can cover only portion of” the isolation structure (’378, 10:42-43). Yang, ¶99.

Petitioner argues that the function of the isolation structure is limited to electrically insulating the TACs (Pet. 53), but this argument ignores the claims, which are not directed to two functions of a single structure. Rather, the claims recite two structures with a claimed spatial relationship. Yang, ¶100.

The fact that the ’378 allows for “other isolation structures” than “STI structure” (’378, 10:34-35; Pet. 52-53) is irrelevant and does not mean that a single “dielectric fill material portion” can be arbitrarily divided to purportedly create both the claimed “dielectric structure” and the claimed “isolation structure,” or the claimed spatial relationship that is absent from Toyama. Yang, ¶101.

Petitioner next cites *Retractable Techs., Inc. v. Becton, Dickinson & Co.*, 653 F.3d 1296, 1303 (Fed. Cir. 2011) to argue that “different parts of the same structure can meet distinct claim elements” (Pet. 53), but this case is inapposite. In *Retractable Techs.*, the Federal Circuit cited clear claim language conveying that “retainer member” can be part of “needle holder,” and a passage from the specification that suggested that they “could be formed as an integral structure in the first instance.” 653 F.3d at 1303. None of that evidence applies here, and Petitioner has cited none. Moreover, the retainer member and the needle holder of *Retractable Techs.* were “distinct” portions (*id.*), whereas there are no “distinct” portions of the

dielectric fill material portion of Toyama absent Petitioner's arbitrary and hindsight-based annotations. Yang, ¶102.

Patent Owner respectfully disagrees with the Board's analysis of *Retractable Techs.* In *Retractable Techs.*, the Federal Circuit determined, based on claim language and specification, that the claimed elements in that case need not be "separately molded pieces." 653 F.3d at 1303. The Board here concluded that isolation structure and dielectric structure in the '378 also need not be separately formed structures (DI, 17-18), but the facts here are not analogous to *Retractable Techs.* **First**, unlike in *Retractable Techs.*, there is no teaching here that the two components may be formed as a single integral structure. *Cf.* 653 F.3d at 1303 ("could be formed as an integral structure in the first instance"). Yang, ¶102.

Second, the Board cites the '378 disclosures that SiO₂ can be used for both the isolation structure and dielectric structure (DI, 18), but even when the same material is used, the isolation structure and dielectric structure are described in the '378 as two separate structures such that one structure is "in contact with" another. '378, 10:35-36. Furthermore, the '378 consistently describes the isolation structure and the dielectric structure to be formed at different steps and never describes the two structures to be formed together. *See* '378, Figs. 4-7, 15:12-50. Even if the same material (e.g., SiO₂) were used for both the dielectric structure and

the isolation structure, there are still two separately identifiable structures. Yang, ¶103.

Third, based on the '378's statement that "the dielectric structure may be 'aligned to' and 'in contact with' the isolation structure" (DI, 18 (citing '378, 10:30-36)), the Board concludes that the two structures "may appear as two aligned and contacting structures" (*id.*), but this statement does not teach that the structures may be a single integral structure. In fact, it teaches the opposite—there are two separate structures that are "in contact" with each other. Yang, ¶104.

Fourth, the Board cites passages from the '378 specification regarding the etching process and concludes that "the dielectric structure and a top portion of the isolation structure may be formed in the same deposition step" (DI, 18), but that is not what the specification states. The cited passages state that "the **etch process** used to form opening 600 may also remove (recess) portion of the top surface of STI structure 233" ('378, 15:18-19) and "opening 600 can be **filled with a dielectric layer 702**" ('378, 15:42-43). Thus, after the isolation structure has already been created, a separate etch process removes a portion of the insulation structure, and then a separate filling process is used to deposit the dielectric structure—the isolation structure and dielectric structure are formed in different steps. Moreover, "whether this results in a dielectric structure that extends into the isolation structure or an isolation structure re-filled to its original height" (DI, 18) is irrelevant. In either case,

there are two separate structures. '378, 15:42-56. The structures are not “molded together” like the components in *Retractable Techs.* Yang, ¶105.

Fifth, while the Board also found that Toyama’s “dielectric fill material portion 430 performs the isolation functions common to both the isolation structure and the dielectric structure” and as a result “can be considered as both the isolation structure and the dielectric structure thereon” (DI, 19), this ignores the etch stop function of the isolation structure. Specifically, the isolation structure provides an etch stop for the formation of the dielectric structure, allowing for the formation of “opening 600” that is subsequently filled to form the dielectric structure. '378, 15:6-14 (“[T]he dry etch process can be a multi-step, anisotropic etch that can be terminated (e.g., stopped) when STI structure 233 is exposed. ... As a result of operation 308, **an opening 600 ... is formed ... over STI structure 233**, as shown in FIG. 6.”). Moreover, the '378’s dielectric structure insulates different structures than the isolation structures. And even if there were some overlapping functions, that does not change that the '378 claims and specification consistently describe two separate structures. Yang, ¶106.

Finally, Petitioner asserts that Toyama’s First Exemplary Structure renders the claims obvious because a different embodiment (third exemplary structure) teaches forming an isolation structure in “opening 151” before forming a dielectric structure (Pet. 53-54 (citing Ex. 1003, ¶121)), but the structure formed in Toyama’s

“opening 151” is not the claimed isolation region/structure that must be part of the substrate for the same reasons explained in §VII.A.1, *supra* (First Exemplary Structure), and §VIII.A.1, *infra* (Second Modification). In addition, apart from conclusory statements by its expert (Ex. 1003, ¶135), Petitioner has not identified a motivation for making the proposed changes to the First Exemplary Structure, which are motivated purely by hindsight. Moreover, the proposed modification changes First Exemplary Structure’s processing steps, which Petitioner leaves unaddressed. For example, splitting up the process of forming dielectric fill portion 430 to instead form two separate structures would involve a longer and more complicated manufacturing process with more opportunities for defects and failure. Petitioner leaves these disadvantageous changes to the manufacturing process wholly unaddressed. Pet. 53-54. Yang, ¶107.

Thus, Toyama’s First Exemplary Structure does not disclose or render obvious “***a dielectric structure on an isolation region***” as required by limitation [1.c] or “***a dielectric structure on the isolation structure***” as required by limitation [15.c.i]. Yang, ¶108.

3. Petitioner Fails to Show That Toyama’s First Exemplary Structure Discloses or Renders Obvious “[One or More] TACs Extending Vertically Through the Dielectric and the Isolation Structures” (Limitations [1.d]/[15.h])

Toyama’s First Exemplary Structure does not disclose or render obvious “***one or more through array contacts (TACs) extending vertically through the dielectric***

structure and the isolation region” as required by limitation [1.d] or “*through array contacts (TACs) extending vertically through the dielectric and the isolation structures*” as required by limitation [15.h] because, for all the reasons explained in §§VII.A.1-2, Toyama’s First Exemplary Structure does not disclose or render obvious the claimed isolation region/structure or the claimed dielectric structure on the isolation region/structure. Yang, ¶109.

B. Petitioner Fails to Show That Toyama’s First Exemplary Structure Discloses or Renders Obvious “the Dielectric Structure Defines a Through Array Contact Region within the 3D Memory Device” (Claim 7)

Toyama’s First Exemplary Structure does not disclose or render obvious “*the dielectric structure defines a through array contact region within the 3D memory device*” as required by claim 7, because for all the reasons explained in §VII.A.2, Toyama’s First Exemplary Structure does not disclose or render obvious the claimed dielectric structure, and as a result, does not disclose or render obvious a through array contact region that is defined by the dielectric structure. Yang, ¶110.

C. Petitioner Fails to Show That Toyama’s First Exemplary Structure Discloses or Renders Obvious “an Etch Stop Plug Interposed Between Each Local Contact of the Local Contacts and Each Channel Structure of the Channel Structures” (Limitation [18.a])

Toyama’s First Exemplary Structure does not disclose or render obvious “*an etch stop plug interposed between each local contact of the local contacts and each channel structure of the channel structures*” as required by claim 18 because

Toyama’s alleged etch stop plugs are not interposed between “**each**” of the alleged local contacts and alleged channel structures. Indeed, Petitioner’s analysis for dependent claim 18 omits one of the types of structures that Petitioner mapped to the “local contacts” of independent claim 15. This is because Toyama’s alleged etch stop plugs are plainly not interposed between that purported local contact and the purported channel structures. Yang, ¶¶112-113.

As explained in §V.C, the plain meaning of the term “each local contact of the local contacts” refers to each of the “local contacts disposed on the channel structures and the slit structures” as recited in limitation [15.g]. Yang, ¶114.

Petitioner’s mapping for claim 18 in the Petition does not even attempt to address “each local contact.” For independent claim 15, Petitioner contends that Toyama’s “**memory stack structures 55**” are the claimed “channel structures” and “**laterally-elongated contact via structures 76**” are the claimed “slit structures.” Pet. 96. Petitioner further alleges that Toyama’s “**drain contact via structures 88**” **and** “**source connection via structures 91**” are the claimed “local contacts disposed on the channel structures and the slit structures.” Pet. 98-99.

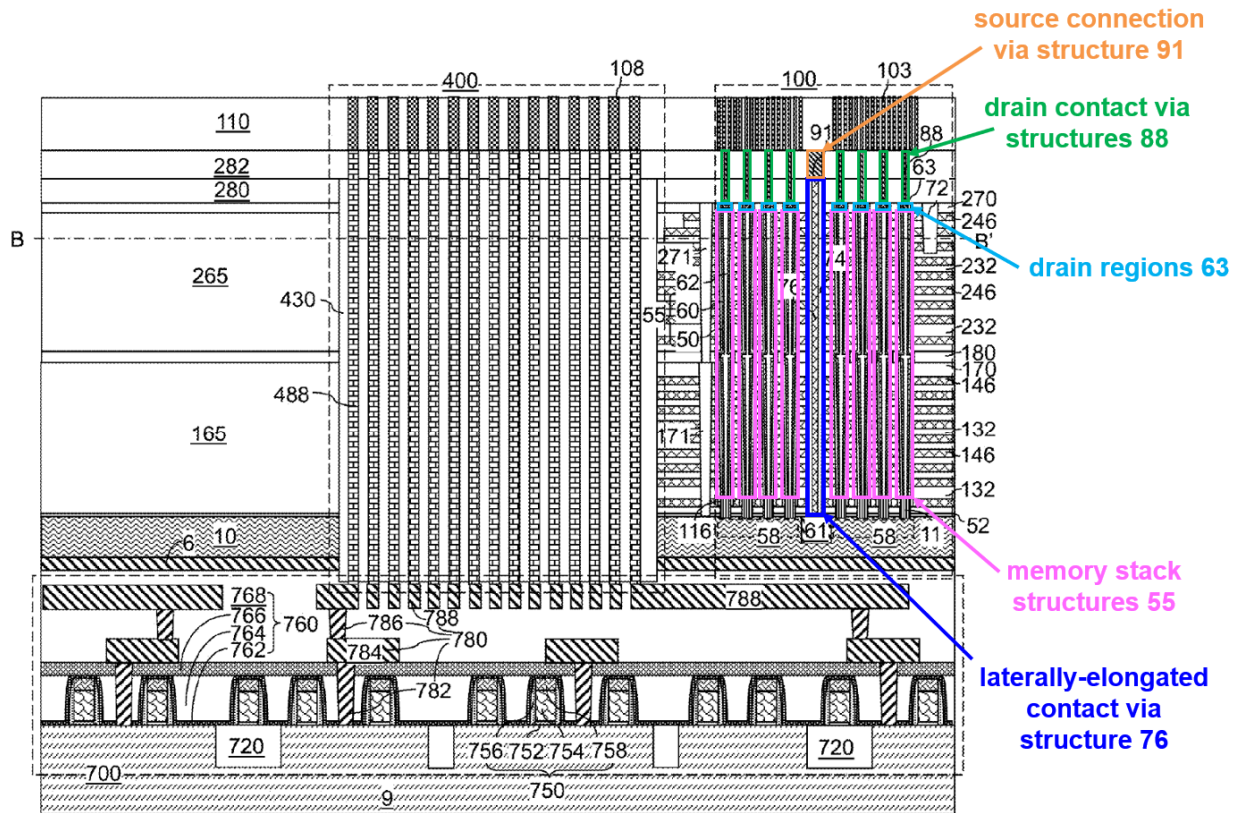


FIG. 17A

Ex. 1005, Fig. 17A (annotated by Patent Owner). Specifically, to meet limitation [15.g], Petitioner argues that Toyama’s “**drain contact via structures 88**” are local contacts disposed on the alleged channel structures (“**memory stack structures 55**”) and “**source connection via structures 91**” are local contacts disposed on the alleged slit structures (“**laterally-elongated contact via structures 76**”). Pet. 98-99. Yang, ¶115.

With regards to claim 18, Petitioner argues that Toyama’s “**drain regions 63**” meet the limitation of “an etch stop plug interposed between each local contact of

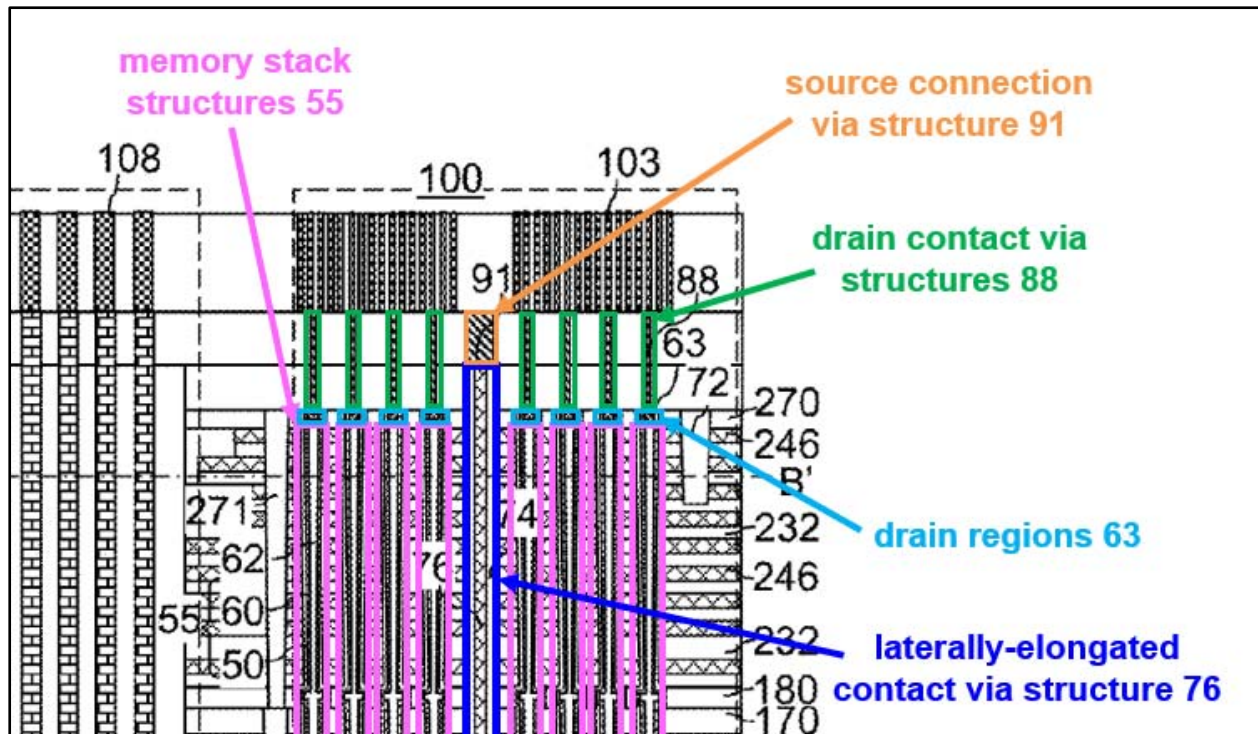
the local contacts and each channel structure of the channel structures”⁶ (Pet. 102-103, referring to the analysis of limitations [1.g], [15.g], and [15.d]), but Petitioner’s analysis discusses only **drain contact via structures 88** (a subset of the purported local contacts). Petitioner entirely ignores **source connection via structures 91**, which Petitioner mapped to one of the claimed local contacts to meet limitation [15.g]. Yang, ¶116.

Because claim 18 requires an etch stop plug interposed between **each local contact of the local contacts** and each channel structure of the channel structures, Petitioner was required to identify an etch stop plug that is also interposed between the **source connection via structures** (alleged local contacts) and **memory stack structures** (alleged channel structures)—but failed to do so. While Petitioner’s mapping discusses whether there is an etch stop plug interposed between the **drain contact via structures** and **memory stack structures**, Petitioner does not even attempt to address whether there is an etch stop plug interposed between the **source connection via structures** and **memory stack structures**. Arguing that Toyama discloses an etch stop plug interposed between the channel structures and **some** of

⁶ For the purposes of this POR, Patent Owner does not dispute Petitioner’s assertion that “a POSITA would have understood, or at least found obvious, that ‘drain regions 63’ are plugs that serve the purpose of stopping an etch.” Pet. 70.

the purported local contacts that Petitioner mapped to the claimed local contacts is not sufficient. Petitioner simply failed to show that Toyama's First Exemplary Structure teaches each element of limitation [18.a]. Yang, ¶117.

Toyama's alleged etch stop plug, **drain regions 63**, is **not** interposed between **source connection via structures 91** (one of the alleged local contacts) and **memory stack structures 55** (the alleged channel structures) as required by claim 18. Indeed, Petitioner has not even alleged that the alleged etch stop plug is between those structures. As shown in Fig. 17A of Toyama annotated below, the **drain regions 63** are, at most, "interposed between" the **drain contact via structures 88** and **memory stack structures 55**. None of the **drain regions 63**, however, is "interposed between" the **source connection via structures 91** and **memory stack structures 55** as required by limitation [18.a]:



Ex. 1005, Fig. 17A (excerpted and annotated by Patent Owner). Petitioner relies for limitation [15.g] on both **drain contact via structures 88** (“local contacts disposed on the channel structures”) and **source connection via structures 91** (“local contacts disposed on...the slit structures”), and *cannot* meet this limitation without relying on both structures. As a result, the alleged etch stop plug of Toyama is not interposed between “each” purported local contact of the local contacts and each purported channel structure of the channel structures as required by limitation [18.a]. Yang, ¶118.

Therefore, Petitioner has failed to show that Toyama’s First Exemplary Structure discloses or renders obvious limitation [18.a]. Yang, ¶119.

VIII. GROUND 1B: TOYAMA’S SECOND MODIFICATION DOES NOT DISCLOSE OR RENDER OBVIOUS CLAIMS 1-7 AND 18

In Ground 1B, Petitioner relies on Toyama’s Second Modification (of the fourth exemplary structure) as allegedly rendering obvious all Challenged Claims (Pet. 34-103), but Petitioner fails to show that Toyama’s Second Modification discloses or renders obvious three separate groups of claim limitations: (1) “*an isolation region of the substrate*” [1.c.ii] and “*a substrate with an isolation structure*” [15.a], (2) “*a dielectric structure on [a/the] isolation [region/structure]*” [1.c.i-ii]/[15.c.i], and (3) “*[one or more] through array contacts (TACs) extending vertically through the dielectric and the isolation structures*” [1.d]/[15.h]. In addition, Petitioner fails to show that Toyama’s Second Modification discloses or renders obvious the additional limitations of claim 7, which depends from claim 1 and further requires “*the dielectric structure defines a through array contact region within the 3D memory device,*” and claim 18, which depends from claim 15 and further requires “*an etch stop plug interposed between each local contact of the local contacts and each channel structure of the channel structures.*” Yang, ¶120.

A. Independent Claims 1 and 15: Toyama’s Second Modification Does Not Disclose or Render Obvious Limitations [1.c.ii]/[15.a], [1.c.i-ii]/[15.c.i], and [1.d]/[15.h]

1. Petitioner Fails to Show That Toyama’s Second Modification Discloses or Renders Obvious “an Isolation Region of the Substrate” (Limitation [1.c.ii]) / “a Substrate With an Isolation Structure” (Limitation [15.a])

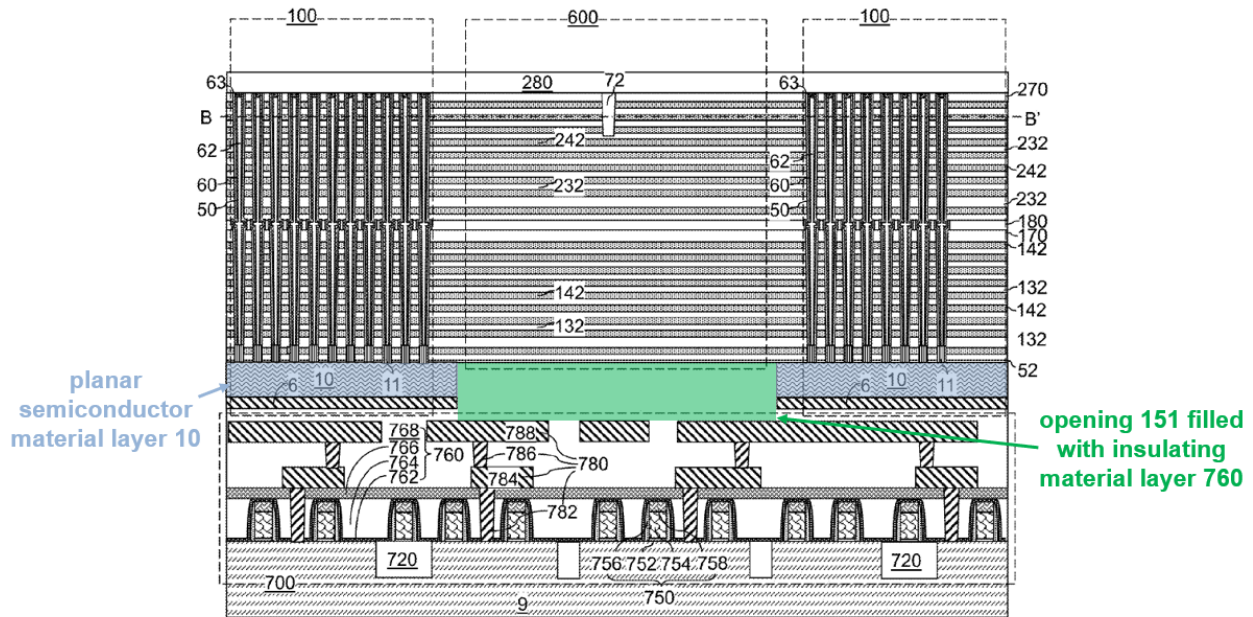
Toyama’s Second Modification does not disclose or render obvious “*an isolation region of the substrate*” as required by limitation [1.c.ii] or “*a substrate with an isolation structure*” as required by limitation [15.a] because—just like with Toyama’s First Exemplary Structure—the feature of Toyama that Petitioner maps to the “isolation [region/structure]” is, at most, located in the region of a cut through the alleged substrate, and is not “part of” the substrate as required by the Challenged Claims under the proper construction of this term (*see* §V.A). Yang, ¶121.

As discussed in §V.A, claim 1 requires “an isolation region *of* the substrate” and claim 15 requires “a substrate *with* an isolation structure,” which means that the isolation structure is *part of* the substrate. This construction of the term does not encompass a structure that extends all the way through the substrate, which is merely next to or abutting, but not part of, the substrate. And as further discussed in §V.A, even if the term “with” is construed as encompassing “on,” the term “on” means “above” in the z-direction (the vertical direction) when the substrate is positioned in the lowest plane of the semiconductor device in the z-direction, and the patent does

not permit reorienting the direction of the “on” spatial relationship to encompass any relative position between components. Yang, ¶122.

Toyama’s Second Modification includes “opening 151” that “may be filled with another insulating material layer [...] 760,” which Petitioner erroneously maps to the isolation region/structure of the ’378. Pet. 30-31. For the same reasons discussed in §VI.A.1, Petitioner’s alleged isolation region/structure (“opening 151” filled with “insulating material layer 760”) in Toyama’s Second Modification’s is not part of the alleged substrate (“planar semiconductor material layer 10”).⁷ Specifically, contrary to Petitioner’s misplaced arguments about how the device is made, as illustrated below, the alleged substrate is completely removed in the relevant region, thereby creating a region outside and merely abutting the alleged substrate, and the “insulating material layer 760” is added in that through-opening.

⁷ For the purposes of this POR, Patent Owner does not dispute Petitioner’s mapping of the claimed “substrate” to Toyama’s “planar semiconductor material layer 10” in Ground 1B.



Ex. 1005, Fig. 44A (annotated). Thus, there is no alleged substrate “with” that “insulating material layer 760” or insulating material “of” the alleged substrate. In the context of Toyama’s Second Modification, Petitioner never addresses the relationship between two claim limitations, *i.e.*, that “a substrate” must be ***part of*** “an isolation structure” and simply asserts that it is shown. Pet. 43, 93. Yang, ¶123.

Petitioner’s additional arguments relevant to this limitation made in the context of Toyama’s First Exemplary Structure (Pet. 52-54) fail for the same reasons discussed in §VII.A.1 above. Yang, ¶124.

Therefore, Petitioner has failed to show that Toyama’s Second Modification discloses or renders obvious ***“an isolation region of the substrate”*** as required by limitation [1.c.ii] or ***“a substrate with an isolation structure”*** as required by limitation [15.a]. Yang, ¶125.

2. Petitioner Fails to Show That Toyama’s Second Modification Discloses or Renders Obvious “a Dielectric Structure on [an/the] Isolation [Region/Structure]” (Limitations [1.c.i-ii]/[15.c.i])

Toyama’s Second Modification does not disclose or render obvious “*a dielectric structure on an isolation region*” as required by limitation [1.c.i-ii] or “*a dielectric structure on the isolation structure*” as required by limitation [15.c.i]. For all the reasons explained in §VIII.A.1, Toyama’s Second Modification does not disclose or render obvious the claimed isolation region/structure. As a result, Toyama’s Second Modification does not disclose or render obvious the claimed dielectric structure on the isolation region/structure. Yang, ¶126.

3. Petitioner Fails to Show That Toyama’s Second Modification Discloses or Renders Obvious “[One or More] TACs Extending Vertically Through the Dielectric and the Isolation Structures” (Limitations [1.d]/[15.h])

Toyama’s Second Modification does not disclose or render obvious “*one or more through array contacts (TACs) extending vertically through the dielectric structure and the isolation region*” as required by limitation [1.d] or “*through array contacts (TACs) extending vertically through the dielectric and the isolation structures*” as required by limitation [15.h] because, for all the reasons explained in §§VII.A.2.a-b, Toyama’s Second Modification does not disclose or render obvious the isolation region/structure or a dielectric structure on the isolation region/structure. Yang, ¶127.

In addition, Toyama's Second Modification does not disclose or render obvious ***“through array contacts (TACs) extending vertically through the dielectric and the isolation structures”*** as required by limitation [15.h] because Toyama's alleged TACs do not extend through the same structure (the claimed “dielectric structure”). As discussed in §V.B, the phrase “through array contacts (TACs) extending vertically through the dielectric and the isolation structures” means “through array contacts (TACs) extending vertically through the dielectric structure and the isolation structure”—i.e., through the same “a dielectric structure” recited earlier in the claim. The alleged TACs of Toyama's Second Modification fail to meet this requirement. Yang, ¶128.

Petitioner maps “insulating liners 674” of “through-memory-level via structures 676” to the “dielectric structure” of the '378 (Pet. 39-42), but this mapping relies on a separate insulating liner (i.e., a separate alleged dielectric structure) for each TAC. In other words, in Toyama's Second Modification, only a single “through-memory-level via structure 676” extends through a given “insulating liner 674.” Realizing this problem, Petitioner attempts to map multiple insulating liners 674 to a single “dielectric structure.” Pet. 41 (alleging that “the ‘insulating liners 674’ are collectively a *structure*”).

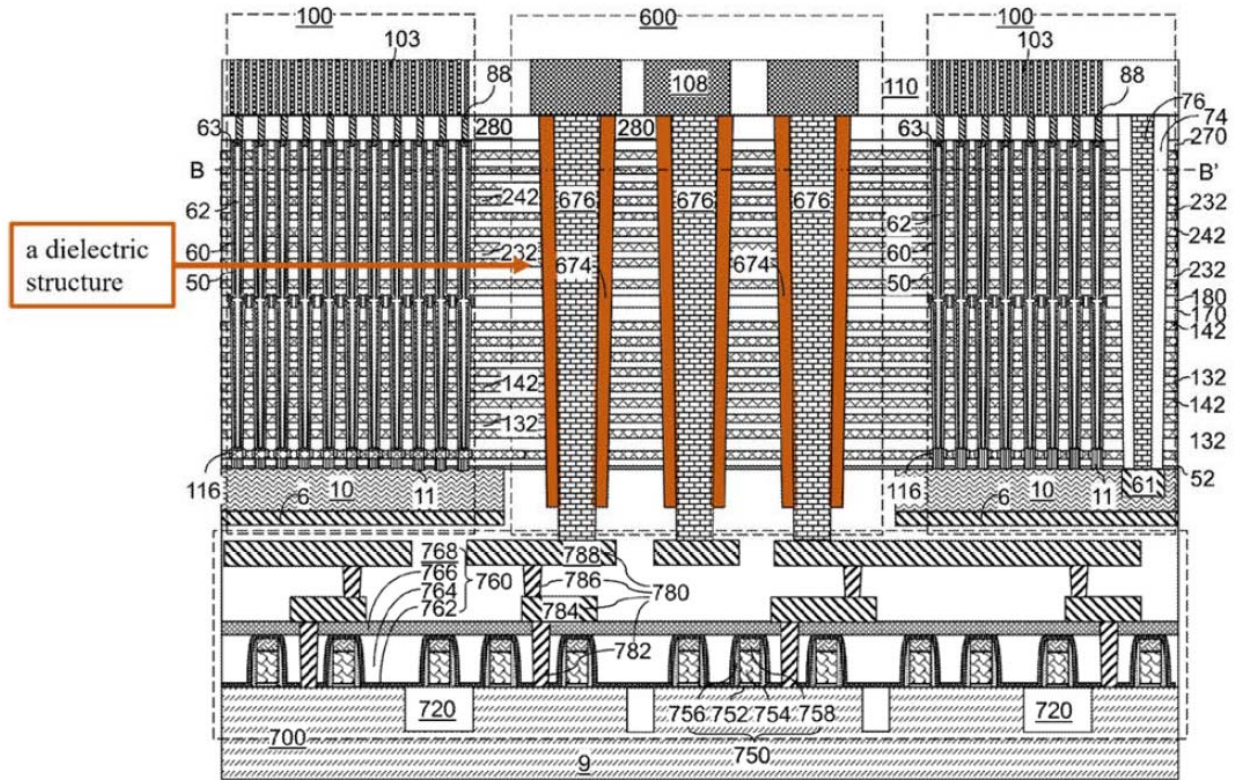


FIG. 49

Ex. 1005, Fig. 49 (annotated by Petitioner at Pet. 40). Yang, ¶129.

Petitioner’s attempt to rely on separate dielectric structures as a single claimed “dielectric structure” is improper. The Federal Circuit has made clear that multiple occurrences of a claim element cannot be used satisfy a limitation that must be satisfied by a single occurrence of the element—here, the claimed “dielectric structure.” See *Finjan*, 84 F.4th at 974-975. In its subsequent decision for IPR2024-00791 (an IPR of the ’806 patent, which is a continuation of the ’378 patent) (Ex. 2006), the Board correctly “disagree[d] [with Petitioner’s assertion] that merely because the three insulating liners are each constructed, that three constructed liners together constitute a single dielectric structure.” Ex. 2006, 17. As a result, the Board

found that Toyama's Second Modification does not show "a plurality of through array contacts (TACs) extending vertically through the dielectric structure" because "Petitioner has not sufficiently shown that Toyama's three insulating liners are a single dielectric structure." Ex. 2006, 17. The '378 limitation at issue here, just like the '806 limitation, requires that multiple TACs extend through a single dielectric structure, and so the Board's correct reasoning in IPR2024-00791 is equally applicable here. Yang, ¶130.

Petitioner misinterprets the Federal Circuit decision *KCJ Corp. v. Kinetic Concepts, Inc.* in which the court found that "an indefinite article 'a' or 'an' in patent parlance carries the meaning of 'one or more' in open-ended claims containing the transitional phrase 'comprising.'" 223 F.3d 1351, 1356 (Fed. Cir. 2000). This principle merely means that in a memory structure that reads on the claims there could be more than one dielectric structure in the memory structure, and does **not** mean that more than one dielectric structure can be combined together for any claimed requirements imposed on the claimed "dielectric structure" (singular). Indeed, as discussed, the Federal Circuit has made clear that multiple occurrences of a claim element cannot be used satisfy a limitation that must be satisfied by a single occurrence of the element. *Finjan*, 84 F.4th at 974-975. Here, the claim, when correctly interpreted (see §V.C), requires that a single "dielectric structure" must

have multiple “through array contacts (TACs) extend[] vertically through” it, which Toyama’s “insulating liner 674” fails to show. Yang, ¶131.

Finally, in its attempt to map multiple separate liners to a single structure, Petitioner cites a dictionary to assert that they “are collectively a structure,” because “they are constructed together.” (Pet. 41), but this argument conflicts with the above-discussed Federal Circuit precedent, and does not comport with the claims and specification of the ’378. Yang, ¶132.

Therefore, Petitioner has failed to show that Toyama’s Second Modification discloses or renders obvious “through array contacts (TACs) extending vertically through the dielectric and the isolation structures” as required by limitation [15.h]. Yang, ¶133.

B. Petitioner Fails to Show That Toyama’s Second Modification Discloses or Renders Obvious “the Dielectric Structure Defines a Through Array Contact Region within the 3D Memory Device” (Claim 7)

Toyama’s Second Modification does not disclose or render obvious “*the dielectric structure defines a through array contact region within the 3D memory device*” as required by claim 7 because the alleged TAC region of Toyama’s Second Modification is not defined by the alleged dielectric structure as required by claim 7. Yang, ¶134.

The limitation “the dielectric structure defines a through array contact region of the 3D memory device” expressly requires that the TAC region is defined by the

dielectric structure, and the claim further requires that “one or more through array contacts (TACs) extend[] vertically through the dielectric structure.” Moreover, because independent claim 1 requires that the “dielectric structure ... extend[s] vertically through the alternating layer stack, the TAC region does not include the alternating conductor/dielectric layer stack. Yang, ¶135.

Petitioner’s alleged TAC region in Toyama’s Second Modification is not defined by the alleged dielectric structure as required by claim 7. Instead, Petitioner’s **alleged TAC region** is an arbitrarily defined region that includes **multiple alleged dielectric structures**, **TACs**, and large portions of **alternating conductor/dielectric layers**. Petitioner’s mapping of the TAC region (cf. Pet. 91) is reproduced below with further annotations:

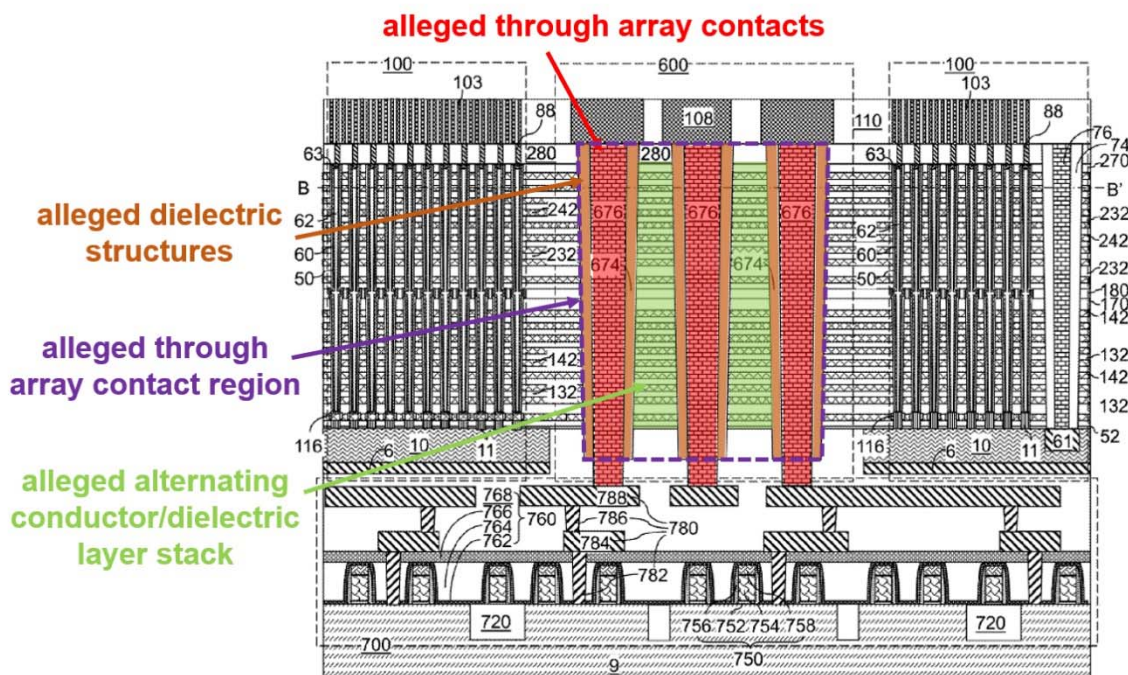


FIG. 49

Ex. 1005, Fig. 49 (annotated). Yang, ¶136.

First, Petitioner’s mapping fails to meet the claim because, as shown, the alleged TAC region extends beyond the alleged dielectric structure, and thus is not defined by the alleged dielectric structure. In other words, because the alleged TAC region extends beyond the alleged structure, the alleged dielectric structure does not “define” the TAC region as required by the claim—rather, Petitioner points to an alleged TAC region that extends beyond a dielectric structure. Second, Petitioner’s alleged TAC region includes the alternating conductor/dielectric layers, which the claim does not permit. As discussed above, because the dielectric structure extends through the alternating conductor/dielectric layer stack (independent claim 1) and the TAC region is defined by the dielectric structure, the TAC region does not include the alternating conductor/dielectric layer stack. Petitioner’s mapping does not address these issues. Pet. 90-91. Yang, ¶137.

Therefore, Petitioner has failed to show that Toyama’s Second Modification discloses or renders obvious “*the dielectric structure defines a through array contact region within the 3D memory device*” as required by claim 7. Yang, ¶138.

C. Petitioner Fails to Show That Toyama’s Second Modification Discloses or Renders Obvious “an Etch Stop Plug Interposed Between Each Local Contact of the Local Contacts and Each Channel Structure of the Channel Structures” (Limitation [18.a])

As with Toyama’s First Exemplary Structure, Toyama’s Second Modification does not disclose or render obvious “*an etch stop plug interposed between each*

local contact of the local contacts and each channel structure of the channel structures” as required by claim 18 because Toyama’s alleged etch stop plugs are not interposed between “**each**” of the alleged local contacts and the alleged channel structures. Indeed, Petitioner’s analysis for dependent claim 18 omits one of the types of structures that Petitioner mapped to the “local contacts” of independent claim 15. This is because those alleged etch stop plugs are plainly not interposed between that purported local contact and the purported channel structures. Yang, ¶139.

As explained in §V.C, the plain meaning of the term “each local contact of the local contacts” refers to each of the “local contacts disposed on the channel structures and the slit structures” as recited in limitation [15.g]. Yang, ¶140.

Petitioner’s mapping for claim 18 in the Petition does not even attempt to address “each local contact.” For independent claim 15, Petitioner contends that Toyama’s “**memory stack structures 55**” are the claimed “channel structures” and “**laterally-elongated contact via structures 76**” are the claimed “slit structures.” Pet. 96. Petitioner further alleges that Toyama’s “**drain contact via structures 88**” *and* “**source connection via structures 91**” are the claimed “local contacts disposed on the channel structures and the slit structures.” Pet. 98-101.



FIG. 49

Ex. 1005, Fig. 49 (annotated by Patent Owner). Although the Petition does not annotate the location of **source connection via structures 91** in Figure 49, Petitioner argues that a POSITA would have understood **source connection via structures 91** to be disposed on the **laterally-elongated contact via structures 76**, as shown above.⁸ Pet. 100-101. Thus, Petitioner has alleged that “**drain contact**

⁸ For the purposes of this POR, Patent Owner does not dispute Petitioner’s claim that Toyama’s “Second Modification ... would also include ‘source connection via structures’” or that a “POSITA would have found the use of local contacts disposed on the slit structures (‘source connection via structures 91’) obvious.” Yang, ¶141.

via structures 88” are local contacts disposed on the alleged channel structures (“**memory stack structures 55**”) and “**source connection via structures 91**” are local contacts disposed on the alleged slit structures (“**laterally-elongated contact via structures 76**”). Yang, ¶141.

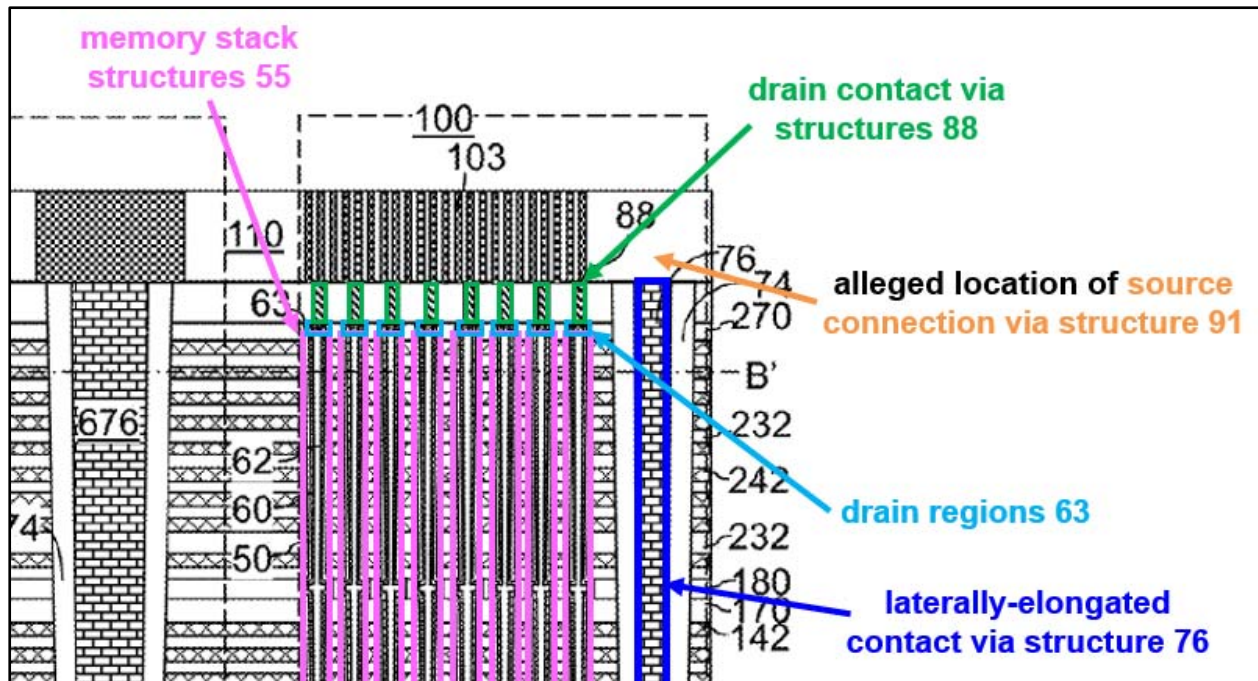
With regards to claim 18, Petitioner argues that Toyama’s “**drain regions 63**” meet the limitation of “an etch stop plug interposed between each local contact of the local contacts and each channel structure of the channel structures”⁹ (Pet. 102-103, referring to the analysis of limitations [1.g], [15.g], and [15.d]), but Petitioner’s analysis discusses only **drain contact via structures 88** (a subset of the purported local contacts). Petitioner entirely ignores **source connection via structures 91**, which Petitioner mapped to one of the claimed local contacts to meet limitation [15.g]. Yang, ¶142.

Because claim 18 requires an etch stop plug interposed between **each local contact of the local contacts** and each channel structure of the channel structures, Petitioner was required to identify an etch stop plug that is interposed between the **source connection via structures** (alleged local contacts) and **memory stack**

⁹ For the purposes of this POR, Patent Owner does not dispute Petitioner’s claim that “a POSITA would have understood, or at least found obvious, that ‘drain regions 63’ are plugs that serve the purpose of stopping an etch.” Pet. 70. Yang, ¶142.

structures (alleged channel structures)—but failed to do so. While Petitioner’s mapping discusses whether there is an etch stop plug interposed between the **drain contact via structures** and **memory stack structures**, Petitioner does not even attempt to address whether there is an etch stop plug interposed between the **source connection via structures** and **memory stack structures**. Arguing that Toyama discloses an etch stop plug interposed between the channel structures and some of the purported local contacts that Petitioner mapped to the claimed local contacts is not sufficient. Petitioner simply failed to show that Toyama’s Second Modification teaches each element of limitation [18.a]. Yang, ¶143.

Toyama’s alleged etch stop plug, **drain regions 63**, is **not** interposed between **source connection via structures 91** (one of the purported local contacts) and **memory stack structures 55** (the alleged channel structures) as required by claim 10. Indeed, Petitioner has not even alleged that the alleged etch stop plug is between those structures. As shown in Fig. 49 of Toyama annotated below, the **drain regions 63** are, at most, “interposed between” the **drain contact via structures 88** and **memory stack structures 55**. None of the **drain regions 63**, however, is “interposed between” the **source connection via structures 91** and **memory stack structures 55** as required by limitation [18.a]:



Ex. 1005, Fig. 49 (excerpted and annotated by Patent Owner). Petitioner relies for limitation [15.g] on both **drain contact via structures 88** (“local contacts disposed on the channel structures”) and **source connection via structures 91** (“local contacts disposed on...the slit structures”), and **cannot** meet this limitation without relying on both structures. As a result, the alleged etch stop plug of Toyama is not interposed between “each” purported local contact of the local contacts and each purported channel structure of the channel structures as required by limitation [18.a]. Yang, ¶144.

Therefore, Petitioner has failed to show that Toyama’s Second Modification discloses or renders obvious limitation [18.a]. Yang, ¶145.

IX. CONCLUSION

For the reasons above, Petitioner has failed to demonstrate by a preponderance of the evidence that any of the Challenged Claims of the '378 is anticipated or obvious. Yang, ¶¶146-148. Accordingly, the Board should find in favor of Patent Owner and uphold the validity of all Challenged Claims.

Dated: April 2, 2025

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CERTIFICATE OF WORD COUNT

The undersigned certifies that the foregoing PATENT OWNER'S RESPONSE UNDER 37 C.F.R. § 42.120 complies with the type-volume limitation in 37 C.F.R. § 42.24(a)-(b). According to the word-processing system's word count, the brief contains 13,928 words, excluding the parts of the brief exempted by 37 C.F.R. § 42.24(c).

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CERTIFICATE OF SERVICE

The undersigned certifies that the foregoing PATENT OWNER'S RESPONSE UNDER 37 C.F.R. § 42.120 was served in its entirety by filing through the Patent Trial and Appeal Case Tracking System (P-TACTS), as well as providing a courtesy copy via e-mail to the following attorneys of record for Petitioner listed below:

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