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Paper 12
Date: January 7, 2025

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

IPR2024-00911
Patent 10,937,806 B2

Before JO-ANNE M. KOKOSKI, KIMBERLY McGRAW, and MICHAEL T. CYGAN, *Administrative Patent Judges.*

McGRAW, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Micron Technology, Inc. ("Petitioner") filed a Petition to institute an *inter partes* review of claim 10 of U.S. Patent No. 10,937,806 B2 ("the '806 patent," Ex. 1001). Paper 1 ("Pet."). Petitioner also filed a paper explaining why it filed multiple petitions challenging the '806 patent as well as ranking the petitions. Paper 3 ("Ranking"). Yangtze Memory Technologies Company, Ltd. ("Patent Owner") filed a Preliminary Response. Paper 10 ("Prelim. Resp."). With prior approval from the Board, Petitioner filed a Preliminary Reply brief to address claim construction issues (Paper 10, "Prelim. Reply"), to which Patent Owner filed a Preliminary Sur-reply (Paper 11, "Prelim. Sur-reply").

Institution of an *inter partes* review is authorized by statute when "the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314 (2018); *see also* 37 C.F.R. § 42.4 (2023). For the reasons discussed below, we determine that at least one of Petitioner's arguments regarding Toyama (alternative argument 2[1]) establishes a reasonable likelihood of prevailing in showing unpatentability of the challenged claim. Accordingly, we institute an *inter partes* review of claim 10 of the '806 patent on all of Petitioner's asserted arguments regarding Toyama.

A. Real Parties in Interest

Petitioner identifies itself and its subsidiaries, including Micron Consumer Products Group LLC, as the real parties in interest. Pet. 5. Patent

[1] *See* Pet. 27–61 (alternative argument 1), 61–100 (alternative argument 2), 100–126 (alternative argument 3).

Owner identifies itself as the real party in interest. Paper 3 (Mandatory Notice), 2.

B. Related Matters

The parties state that the ’806 patent is asserted in *Yangtze Memory Techs. Co., Ltd. v. Micron Tech. Inc.*, Case No. 3:23-cv-05792-RFL (N.D. Cal.) (“the District Court Litigation”). Pet. 5; Paper 3, 2.

Claims 8, 9, 11, and 12 of the ’806 patent are challenged by Petitioner in IPR2024-00791 (“the 791 IPR”), which was instituted on November 27, 2024. *See Micron Technology, Inv. v. Yangtze Memory Technologies Co., Ltd.*, IPR2024-00791, Paper 11 (PTAB Nov. 27, 2024).

Petitioner also states it filed IPRs challenging other patents asserted in the District Court Litigation, namely U.S. Patent Nos. 10,950,623 (IPR2024-00794 (instituted)), 10,658,378 (IPR2024-00788 (instituted), IPR2024-00909 (instituted)), 10,861,872 (IPR2024-00789 (instituted), IPR2024-00910 (institution denied)), 10,868,031 (IPR2024-00790 (instituted)), 11,501,822 (IPR2024-00795 (instituted)), 11,468,957 (IPR2024–00792 (instituted)), and 11,600,342 (IPR2024-00793 (institution denied, request for rehearing pending), IPR2024-00912 (institution denied, request for rehearing pending)). Pet. 5–6.

C. The ’806 Patent

The ’806 patent, titled “Through Array Contact (TAC) for Three-Dimensional Memory Devices” relates to “a channel hole plug structure of three-dimensional (3D) memory devices and a method for forming the same.” Ex. 1001, code (54), 1:18–20. An embodiment of the 3D memory device is illustrated in Figure 2 of the ’806 patent and is reproduced below.

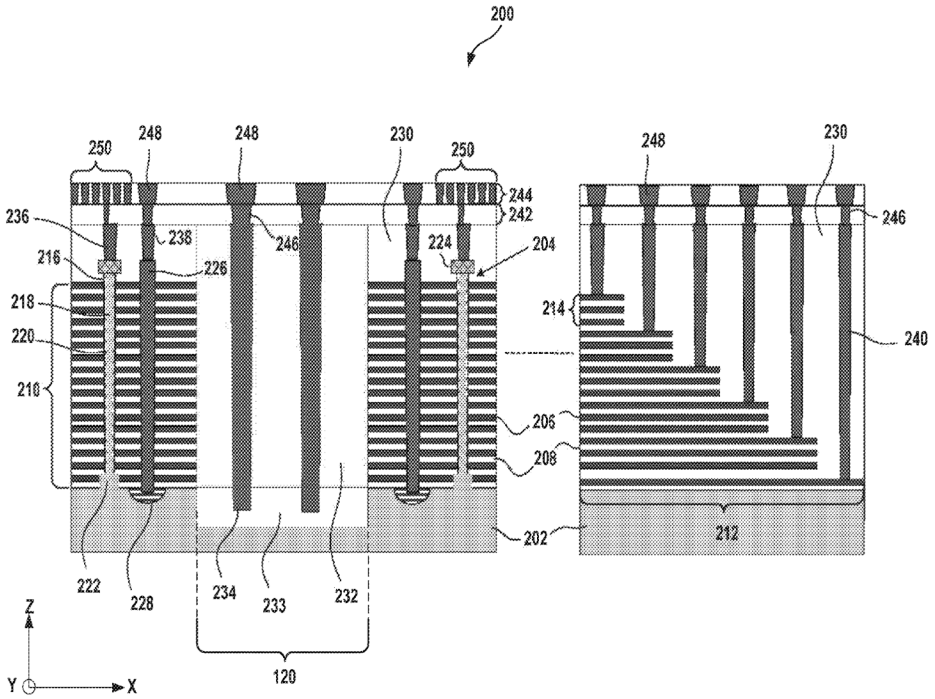


FIG. 2

Figure 2 "is a cross-sectional view of an exemplary 3D memory device 200" disclosed in the '806 patent. Ex. 1001, 3:41–42.

Memory device 200 can be a "NAND Flash memory device[2] in which memory cells are provided in the form of an array of NAND strings 204 extending vertically above substrate 202." *Id.* at 8:17–20. "The array device can include a plurality of NAND strings 204 that extend through a plurality of conductor layer 206 and dielectric layer 208 pairs" that alternate in the vertical direction, also referred to as " 'alternating conductor/dielectric stack' 210." *Id.* at 8:20–31. Alternating conductor/dielectric stack 210 can include staircase structure 212, where each "level" or "step" 214 can include

[2] Though not explicitly defined in the specification, Petitioner's declarant states that "[t]he acronym 'NAND' refers to a 'not-AND' logic gate, and NAND flash memory is a particular type of flash memory where the memory cells form a structure similar to that of a NAND gate." Ex. 1003 ¶ 43.

one or more conductor/dielectric layer pairs stacked. *Id.* at 8:54–59. "The top layer in each level 214 of staircase structure 212 is a conductor layer 206 available for interconnection in the vertical direction (e.g., along the z-axis)." *Id.* at 8:61–63. Figure 2 also shows "channel structure 216 that extends through alternating conductor/dielectric stack 210" that is filled with semiconductor materials and dielectric materials. *Id.* at 9:7–12. The embodiment illustrated in Figure 2 also includes slit structures 226 that also extend through alternating conductor/dielectric stack 210 and may extend along the y-axis to separate alternating conductor/dielectric stack into multiple blocks. *Id.* at 9:54–58.

Figure 2 also illustrates through array contacts ("TACs") 234, extending vertically through dielectric structure 232, which are within a TAC region 120 that can have, but are not limited to, a rectangle or square shape. *Id.* at 10:55–64. "TACs 234 can carry electrical signals from and/or to 3D memory device 200" and "can provide electrical connections between the 3D memory device 200 and the peripheral device." *Id.* at 11:8–14.

D. Illustrative Claim

Petitioner challenges dependent claim 10 in this proceeding. Claim 10 depends upon independent claim 8, which is challenged in IPR2024-00791. Claims 8 and 10 are reproduced below.

> 8. [1.PRE] A three-dimensional (3D) memory device, comprising:
>
> [8.A] an alternating conductor/dielectric layer stack;
>
> [8.B.i] a dielectric structure [8.B.ii] extending vertically through the alternating conductor/dielectric layer stack;
>
> [8.C] first and second channel regions comprising first and second pluralities of channel structures, respectively;

[8.D] slit structures extending vertically through the alternating conductor/dielectric layer stack;

[8.E] a staircase structure disposed in the alternating conductor/dielectric layer stack, wherein the staircase structure comprises levels with each level having a conductor layer thereon;

[8.F] local contacts disposed on the first and second channel structures and the slit structures;

[8.G] a through array contact (TAC) region formed between the first and second channel regions, wherein the TAC region comprises a plurality of through array contacts (TACs) extending vertically through the dielectric structure; and

[8.H] a plurality of non-electrically functional channel structures surrounding the TAC region and between the first and second channel regions.

Ex. 1001, 23:54–24:8 (bracketed material added).

10. [10.PRE] The 3D memory device of claim 8, further comprising:

[10.A] a substrate;

[10.B] an etch stop plug interposed between each local contact of the local contacts and each channel structure of the first and second channel structures; and;

[10.C] an epitaxial layer disposed between the substrate and the first or second channel structures.

Id. at 24:13–20 (bracketed material added).

E. Asserted Ground

Petitioner asserts that claim 10 would have been unpatentable on the following ground:

Claim Challenged	35 U.S.C. §	Reference(s)/Basis
10	103[3]	Toyama[4]

Pet. 15[5]. In the present Petition, Petitioner states that it maintains the same three alternative arguments that claim 8 would have been obvious over various embodiments of Toyama that it presented in the 791-Petition. Pet. 1; *see also id.* at 27–61 (alternative argument 1 relying on Toyama's Second Modification"), 61–100 (alternative argument 2 relying on Toyama's First Exemplary Structure), 100–126 (alternative argument 3 relying on Toyama's First Exemplary Structure in combination with the Second Modification).

Petitioner relies on the Declaration of Jack C. Lee, Ph. D. ("Lee Dec.," Ex. 1003) in support of its contentions.

II. ANALYSIS

A. Level of Ordinary Skill in the Art

Petitioner contends that a person of ordinary skill in the art ("POSITA") would have had "a bachelor of science degree in electrical engineering or a similar discipline" with "2–3 years of professional experience working with (e.g., researching, designing, or teaching) NAND

[3] The Leahy-Smith America Invents Act ("AIA"), Pub. L. No. 112–29, 125 Stat. 284 (2011), revised 35 U.S.C. §§ 102 and 103 effective March 16, 2013. Because the '806 patent has an effective filing date after March 16, 2013 (Ex. 1001, codes (22), (63)), we refer to the AIA version of Sections 102 and 103.

[4] Toyama, US Pub. No. 2017/0179026 A1, published June 22, 2017 (Ex. 1005).

[5] Petitioner characterizes its alternative arguments of unpatentability of claim 10 as based on three "grounds." *See* Pet. 15. Because each of Petitioner's arguments are based on the same reference, albeit different embodiments, we characterize Petitioner's challenges as three alternative arguments based on a single ground because each argument relies on the same reference.

flash memory devices, or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may replace some of the professional experience)." Pet. 26 (citing Ex. 1003 ¶¶ 35–39). Petitioner further contends that a "POSITA would also have been aware of and generally knowledgeable about semiconductor manufacturing and 3D NAND's structure, its component parts, how it operates, and how it is controlled." *Id*.

At this stage of the proceeding, Patent Owner neither responds to Petitioner's proposed definition, nor provides a definition of its own. *See generally*, Prelim. Resp. Petitioner's undisputed proposed definition appears to be consistent with the cited prior art and the disclosure of the '806 patent, and we adopt it for purposes of this Decision.

B. Claim Construction

We construe claims challenged in an *inter partes* review proceeding, "using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. [§] 282(b)," including construing the claims "in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent." 37 C.F.R. § 42.100(b). Under this standard, claim terms are generally given their plain and ordinary meaning as would have been understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc). Only those terms in controversy need to be construed, and only to the extent necessary to resolve the controversy. *Realtime Data LLC v. Iancu*, 912 F.3d 1348, 1375 (Fed. Cir. 2019).

Although both parties initially stated no claim construction was necessary at this stage of the proceeding (*see* Pet. 26; Prelim. Resp. 13), the

parties' patentability arguments raise claim construction issues regarding the term "dielectric structure" recited in claim 8 and "each local contact" recited in claim 10.

Because the claim construction arguments regarding "dielectric structure" are intertwined with the parties' patentability arguments, for efficiency and completeness, we address this claim construction issue in the context of the patentability decision below.

1. "each local contact"

Claim element [10.B] recites "an etch stop plug interposed between each local contact of the local contacts and each channel structure of the first and second channel structures." Ex. 1001, 24:15–18. Claim 8, from which claim 10 depends, recites a memory device comprising, *inter alia*, "local contacts disposed on the first and second channel structures and the slit structures." *Id.* at 23:66–67. The parties dispute whether the "each local contact" recited in claim 10 refers only to each local contact on the channel structures (a "channel structure local contact"), as asserted by Petitioner, or refers to each local contact on the channel structures as well as each local contact on the slit structures (a "slit structure local contact"), as asserted by Patent Owner. *See, e.g.,* Pet. 54–59; Prelim. Resp. 36–40. The parties filed authorized additional briefing to address this claim construction issue. *See* Ex. 1042; Pet. Reply; PO Sur-reply.

Petitioner asserts that the plain language of claim 8 requires two sets of local contacts (i.e., local contacts on channel structures and local contacts on slit structures) and claim 10 necessarily refers to only the local contacts on the channel structure. Pet. Reply 4. Petitioner explains that this is shown in Figure 2 of the '806 patent, reproduced below, which depicts channel local contact 236 located on etch stop 224 located on channel structure 216

(highlighted red) and slit local contact 238 directly on slit structure 226 (highlighted blue).

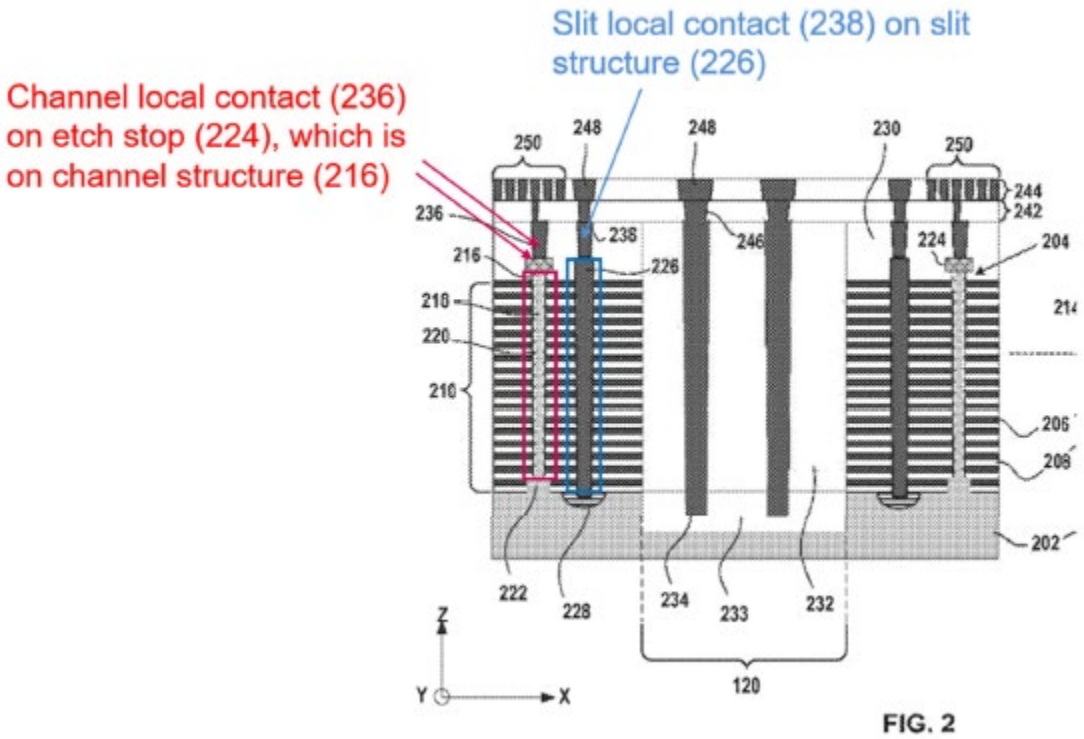


Figure 2 of the '806 patent, with Petitioner's color annotations added, illustrates a cross-section of a 3D memory device having NAND string contact 236 "in contact with etch stop plug 224 of NAND string 204" and slit structure contact 238 "in contact with the upper end of slit structure 226." Ex. 1001, 3:41–42, 7:11–12, 11:40–43; Pet. Reply 1.

Petitioner contends that because claim 10 refers to an etch stop plug that is interposed *between* each local contact of the local contacts and each channel structure, claim 10 is referring to an area for the etch stop that is above the channel structure and beneath the local contact. *See* Pet. Reply 4; *see also id*. (stating that, in the '806 patent, only the local contacts for the channel structures are above the channel structures). Therefore, Petitioner contends, the local contact referred to in claim 10 must be above the channel structure in order for the etch stop plug to be located between the local contact and the channel structure. *See* Pet. Reply 4. Petitioner contends that

the specification supports this reading because the ’806 patent “only describes etch stop plugs as being ‘between’ channel local contacts and channel structures.” *Id.* at 4–5 (citing Ex. 1001, 1:60–65, 11:40–43, 2:38–56, 9:36–53, 15:61–16:15, 17:53–52, 20:53–59); *see also id.* at 2 (stating the ’806 patent never discloses an etch stop on the slit structure).

Patent Owner responds that the plain meaning of “each local contact of the local contacts” should apply and refer to “each” of the previously recited local contacts recited in claim 8, namely the “each local contact” disposed on the first and second channel structures *and* the slit structures. Sur-reply 4; *see also id.* at 1 (stating that it is undisputed that the antecedent basis for “the local contacts” recited in claim 10 is claim 8’s local contacts disposed on the channel structures and the slit structures). Patent Owner asserts that it is not sufficient to show an etch stop plug interposed between only “some local contacts” and each channel structure, as claim 10 requires “each local contact.” *Id.* at 1–2. Rather, Patent Owner contends claim 10 requires that an etch stop plug be interposed between each channel structure local contact and each channel structure of the first and second channel structures *and* between each slit structure local contact and each channel structure. *See id.* 1–2; *see also id.* at 3 (explaining that its construction does not require an etch stop plug interposed between local contacts and the slit structures).

Patent Owner also states that, contrary to Petitioner’s assertion, the ’806 patent does disclose an etch stop plug (or layer) for the slit structure contacts. *Id.* at 2. In particular, Patent Owner cites to column 17, lines 57 through 61, as stating that in “the case of slit structure contacts 238 and upper WL contacts 240-1, further etching can be prevented due to the presence of conductor material 1004 and conductor layer 206, which can act

as an etch stop layer for the dry etch process." *See also id.* at 2–3 (further citing Ex. 1001, 9:44–46, 16:62–17:1, 17:49–53 and stating that none of the passages cited by Petitioner precludes an etch stop plug for the slit structure).

At this stage of the proceeding, we construe "the local contacts" recited in claim element [10.B] to refer to the local contacts that are disposed on the first and second channel structures (i.e., a "channel structure local contact") and not to the local contacts disposed on slit structures (a "slit structure local contact"). Claim 8 refers to two different types of local contacts, local contacts that are located above (i.e., "disposed on") channel structures ("channel structure local contacts") and local contacts that are located (disposed on) above slit structures ("slit structure local contacts"). Ex. 1001, 23:66–67. Although claim element [10.B] does not explicitly refer to channel structure local contacts, the claim does require that the etch stop plug is "interposed between" a local contact and a channel structure. *Id.* at 24:13–20. At this stage of the proceeding, Petitioner persuasively explains that the only way for an etch stop plug to be interposed between a local contact and a channel structure is if the local contact is located on the channel structure, i.e., the local contact is a channel structure local contact. *See, e.g.*, Pet. Reply 4–5. Thus, we understand the plain and ordinary meaning of "each local contact" recited in claim 10 to refer to each channel structure local contact and not to each slit structure local contact. Stated another way, because the slit structure local contact is not located above a channel structure, we do not understand claim 10, which requires the etch stop plugs to be *interposed between* a local contact and a channel structure, to refer to the slit structure local contacts.

Our construction that claim 10 does not require an etch stop plug interposed between each slit structure local contact and each channel structure is supported by the prosecution history. The Examiner rejected then pending claim 12, which ultimately issued as claim 10, over the combination of Pachamuthu and Lee. *See* Ex. 1002, 108–109. In doing so, the Examiner stated the prior art taught etch stop plugs interposed between the channel structure local contacts and the channel structures but did not assert that the prior art suggested an etch stop plug interposed between slit structure local contact and a channel structure. *See id.* (stating Pachamuthu teaches an etch stop plug over each channel structure of the channel structures and Lee teaches local contacts disposed on a channel structure). Thus, the Examiner did not consider the claim to require an etch stop plug disposed between a *slit structure local contact* and a channel structure.

Petitioner also argues that the ’806 patent “defines” the function of the etch stop plug as protecting the channel *and* serving as the channel’s drain. Pet. Reply 2–3. At this stage of the proceeding, we disagree that the ’806 patent defines the etch stop plug as serving as the channel’s drain. The ’806 patent states that “[i]n *some embodiments,* each etch stop plug 224 acts as the drain of NAND string 204.” Ex. 1001, 9:40–53 (emphasis added). Thus, at this stage of the proceeding, we understand the ’806 patent to contemplate embodiments in which the etch stop plug does not act as the channel’s drain.

The parties are invited to address the construction of “each local contact of the local contacts” recited in claim 10 during trial to the extent permitted under our rules.

No other terms require express construction to resolve any issue in dispute at this stage of the proceeding. *See Vivid Techs., Inc. v. Am. Sci. &*

Eng'g, Inc., 200 F.3d 795, 803 (Fed. Cir. 1999); *see also Nidec Motor Corp. v. Zhongshan Board Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (applying *Vivid Techs.* in the context of an *inter partes* review).

C. Obviousness over Toyama

As noted above, Petitioner presents three alternative arguments that challenged claim 10, and its base claim 8, would have been obvious over Toyama. We address Toyama and each of these arguments below.

1. Toyama

Toyama is titled "Through-Memory-Level Via Structures For a Three-Dimensional Memory Device." Ex. 1005, code (54). Toyama relates to three-dimensional NAND memory devices, such as vertical NAND strings, and describes four exemplary structures and modifications thereof. *Id.* ¶¶ 4, 14–155. Toyama's "first exemplary structure" is illustrated in Figures 1 through 17. *Id.* ¶¶ 14–48, 163–260, Figs. 1–17. Figure 11A, reproduced below, depicts the first exemplary structure after formation of a through-memory-level opening. *Id.* ¶ 30.

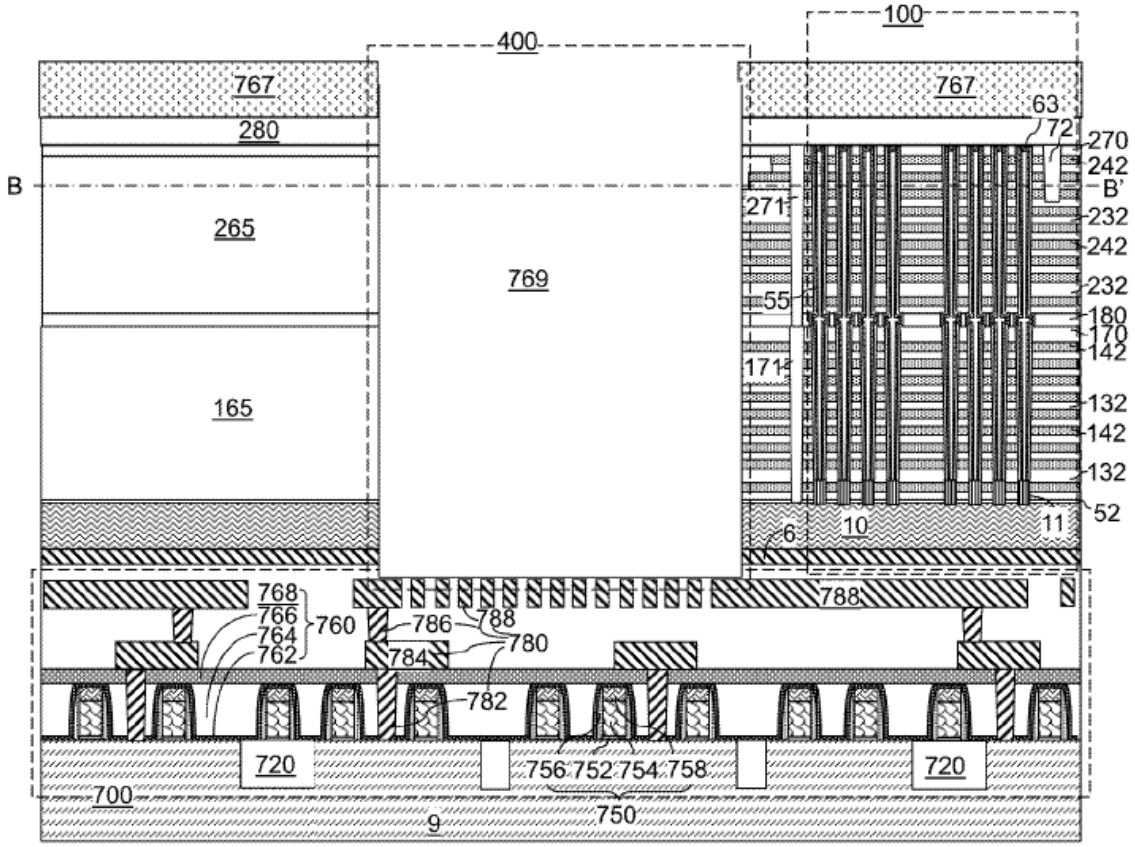


FIG. 11A

Figure 11A is a vertical cross-sectional view of the first exemplary structure according to the first embodiment of the disclosure. *Id.* ¶ 30.

At least one dielectric layer 760 is formed over the semiconductor devices, and lower level metal interconnect structures 780 formed thereon to function as landing pads for through-memory-level via structures. *Id.* ¶ 164. Upon these structures in underlying peripheral region 700 (those having numbers in the 700s), a planar semiconductive layer 10 is formed. *See id.* ¶ 165. On semiconductor layer 10 is an alternating stack of conductive layers 146, 246 (replacing sacrificial material layers 142, 242) and insulating layers 132, 232. *Id.* ¶¶ 172, 196, 228. In portions of the alternating stack, supporting pillar structures 171 are formed, and other portions of the dielectric stack appear as a stepped region. *Id.* ¶ 182, Fig. 4B. In the

stepped region, a through-memory-level opening 769 can extend from the top of the device down to the lower level metal interconnect structures 780 in peripheral region 700. *Id.* ¶ 213. A dielectric fill material portion is formed within each through-memory-level opening 769. *Id.* ¶ 216.

Toyama also describes a "second modification of [a] fourth exemplary structure" ("Second Modification") illustrated in Figures 44A through 49. *Id.* ¶¶ 93–103. Figure 49 is shown below:

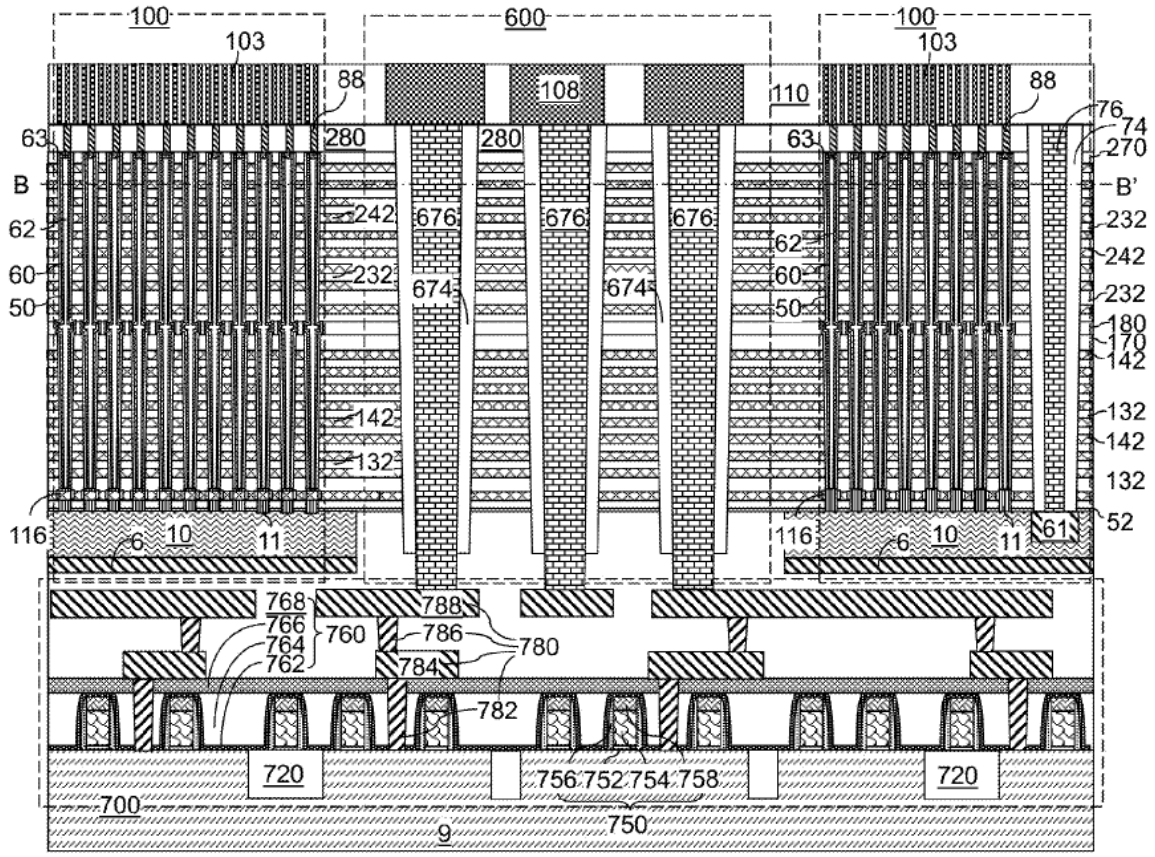


FIG. 49

Figure 49 is a vertical cross-sectional view of Toyama's second modification of its fourth exemplary structure after formation of upper level metal interconnect structures. *Id.* ¶ 103. Shown in Figure 49 is semiconductor substrate 9 having peripheral region 700, upon which planar semiconductive layer 10 is formed having an alternating stack of conductive

layers 146, 246 (replacing sacrificial material layers 142, 242) and insulating layers 132, 232. *Id.* ¶¶ 310–311, 332. Multiple through-memory-level openings 676, surrounded by insulating liners 674, are created within the alternating stack. *Id.* ¶¶ 339–341.

2. Asserted Obviousness over Toyama's Second Modification to its Fourth Exemplary Structure (Alternative Argument 1)

Petitioner argues that claim 10, which depends from claim 8, would have been obvious over Toyama's second modification to its fourth exemplary structure ("Second Modification"). Pet. 26–60. Patent Owner opposes. Because Petitioner has not shown a reasonable likelihood that claim 8 would have been obvious over Toyama's Second Modification, and Petitioner's arguments regarding claim 10 do not remedy this deficiency, Petitioner has not shown a reasonable likelihood that claim 10 would have been obvious over Toyama's Second Modification.

(1) Petitioner's Contentions

Petitioner contends that Toyama's Second Modification discloses or suggests all elements of independent claim 8. Pet. 26–53. In particular, Petitioner asserts that Toyama's Second Modification is a "three-dimensional non-volatile memory device[]" having an "alternating stack (132, 146, 232, 246)" of "electrically conductive layers" and "insulating layers" as recited in the preamble and claim element [8.A]. *Id.* at 27–28 (citing Ex. 1005 ¶¶ 156, 337, 340, Figs. 45A, 46A, 47A, 48A, 49; Ex. 1003 ¶¶ 105, 107–108).

Petitioner asserts that Toyama's "insulating liners 674," highlighted orange in Toyama's Figure 49 below, are "a dielectric structure" extending vertically" through the alternating conductor/dielectric stack (highlighted green and yellow), as recited in claim element [8.B.i–8.B.ii]. Pet. 28–32

(citing, *inter alia*, Ex. 1005, Fig. 49, ¶¶ 233, 338–340, 381; Ex. 1003 ¶¶ 110–116).

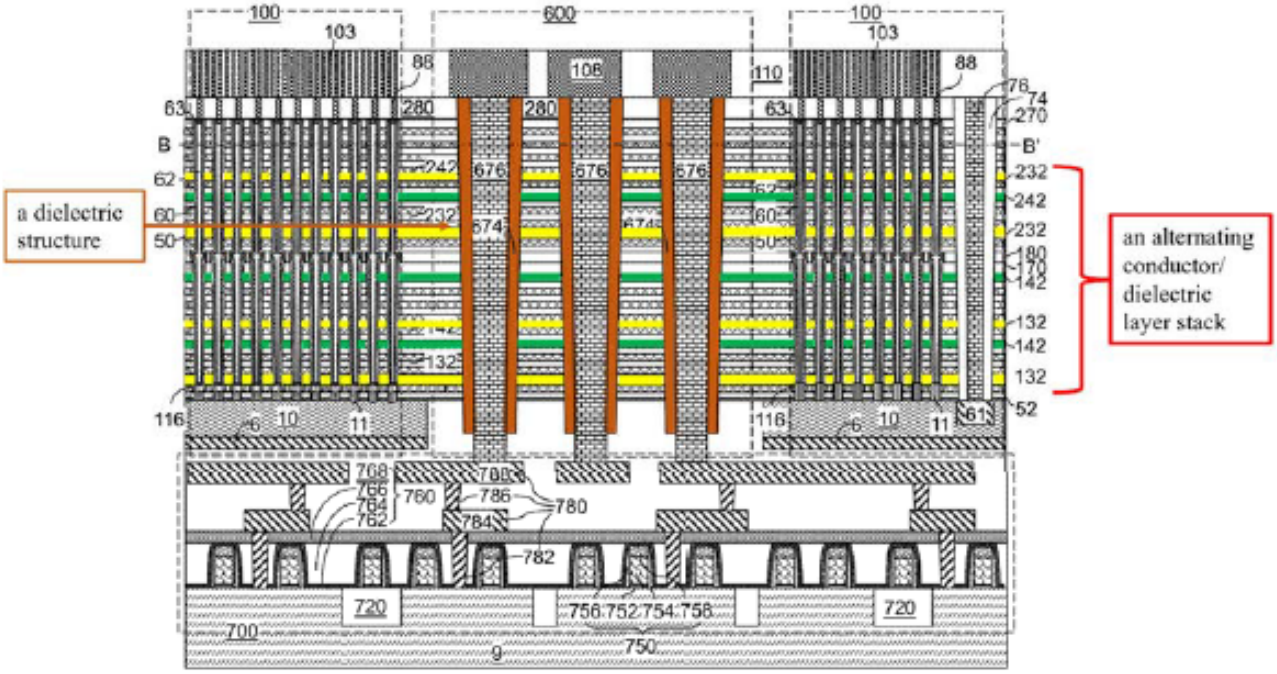


FIG. 49

Toyama's Figure 49, with Petitioner's annotations added, depicts alternating stack 132, 142/146, 232, 242/236[6] (green and yellow) and insulating liners 674 (orange). Pet. 31–32; Ex. 1005, Fig. 49; Ex. 1003 ¶ 116.

Petitioner states that the three insulating liners (elements 674) in Toyama together are a single dielectric structure as recited in claim element [8.B] at least because the liners "have the same function" and the "components together are something 'that is constructed.'"[7] Pet. 30–31 (citing Ex. 1021, 5; Ex. 1003 ¶ 113). Petitioner also states that although the

[6] Petitioner asserts that a POSITA would have understood that elements 142 and 242 in Figure 49, as well as Figures 47A and 48A, were mislabeled and were intended to be labeled 146 and 246 respectively. Pet. 28 n.2 (citing Ex. 1003 ¶ 88).

[7] Petitioner cites to Merriam-Webster's definition of a structure as "something ([such] as a building) that is constructed." Pet. 30 (modifications in Pet.) (citing Ex. 1021, 5).

three insulating liners 674 are collectively a single structure, not multiple structures, the claim is opened ended and, therefore, encompasses a device with multiple dielectric structures. *Id.* at 30 n.4 (citing *KCJ Corp. v. Kinetic Concepts, Inc.*, 223 F.3d 1351, 1356 (Fed. Cir. 2000) as stating that use of an indefinite article "a" or "an" means "one or more" in open-ended claims containing the transitional phrase comprising).

Regarding claim element [8.C], Petitioner maps Toyama's "memory array region 100" and "memory stack structures 55," shown in Figures 48B and 49, to the "first and second channel regions comprising first and second pluralities of channel structures, respectively." *Id.* at 32–35 (citing Ex. 1005 ¶¶ 210, 323, 333, 388, Figs. 48B, 49; Ex. 1003 ¶¶ 118–120). Petitioner asserts that the "slit structures extending vertically through the alternating conductor/dielectric layer stack" as recited in claim element [8.D] maps to the "laterally-elongated contact via structures 76" in Toyama and that the slit structures extend vertically through the "alternating stack (132, 146, 232, 246)." *Id.* at 35–38 (citing, *inter alia*, Ex. 1005 ¶¶ 237, 241, 318–320, Figs. 48B, 49; Ex. 1003 ¶¶ 121–123).

Petitioner also contends that Toyama's staircase regions, which contain "conductor layer[s]," shown in Figure 17C, discloses or suggests the "staircase structure disposed in the alternating conductor/dielectric layer stack, wherein the staircase structure comprises levels with each level having a conductor layer thereon" recited in claim element [8.E]. *Id.* at 38–40 (citing Ex. 1005 ¶ 232, Fig. 17C; Ex. 1003 ¶¶ 124–126); *see also id.* at 40 (stating a POSITA would have understood that Toyama's Second Modification also teaches the above citations to Toyama's first exemplary structure, depicted in Figure 17C).

Claim element [8.F] recites "local contacts disposed on the first and second channel structures and the slit structures." Petitioner asserts that Toyama's "drain contact via structures 88" contacting or extending above the "memory stack structures 55" discloses the recited "local contacts disposed on the first and second channel structures." Pet. 40–41 (mapping Toyama's drain contact structures 88 to "local contacts" and Toyama's memory stack structures to "channel structures" and citing Ex. 1005 ¶ 251, Fig. 49; Ex. 1003 ¶ 128).

Petitioner admits that Toyama's description of its Second Modification does not expressly disclose local contacts (source connection via structures 91) disposed on the slit structures ("laterally-elongated contact via structures 76) as recited in claim element [8.F]. Pet. 42. Petitioner, however, asserts that a POSITA would have understood that the Second Modification includes, or would have rendered obvious, local contacts disposed on the slit structures (source connection via structures 91) to provide a higher-level source connection in order for via structures to serve as source lines for source region 61. *Id.* at 42–44 (citing Ex. 1005 ¶¶ 250, 342, 382; Ex. 1003 ¶¶ 129–131).

Claim element [8.G.i–iii] requires: [i] "a through array contact (TAC) region" [ii] "formed between the first and second channel regions" [iii] "wherein the TAC region comprises a plurality of through array contacts (TACs) extending vertically through the dielectric structure." Ex. 1001, 24:1–5. Petitioner asserts Toyama's Second Modification, shown in Figure 49 below, depicts a through array contact (TAC) region (part of

"through-memory-level via region 600")[8] that is formed between first and second channel regions ("first and second parts of 'memory array region 100'"). Pet. at 44–48 (citing Ex. 1005 ¶¶ 334, 378, Figs. 48B, 49; Ex. 1003 ¶¶ 133–136).

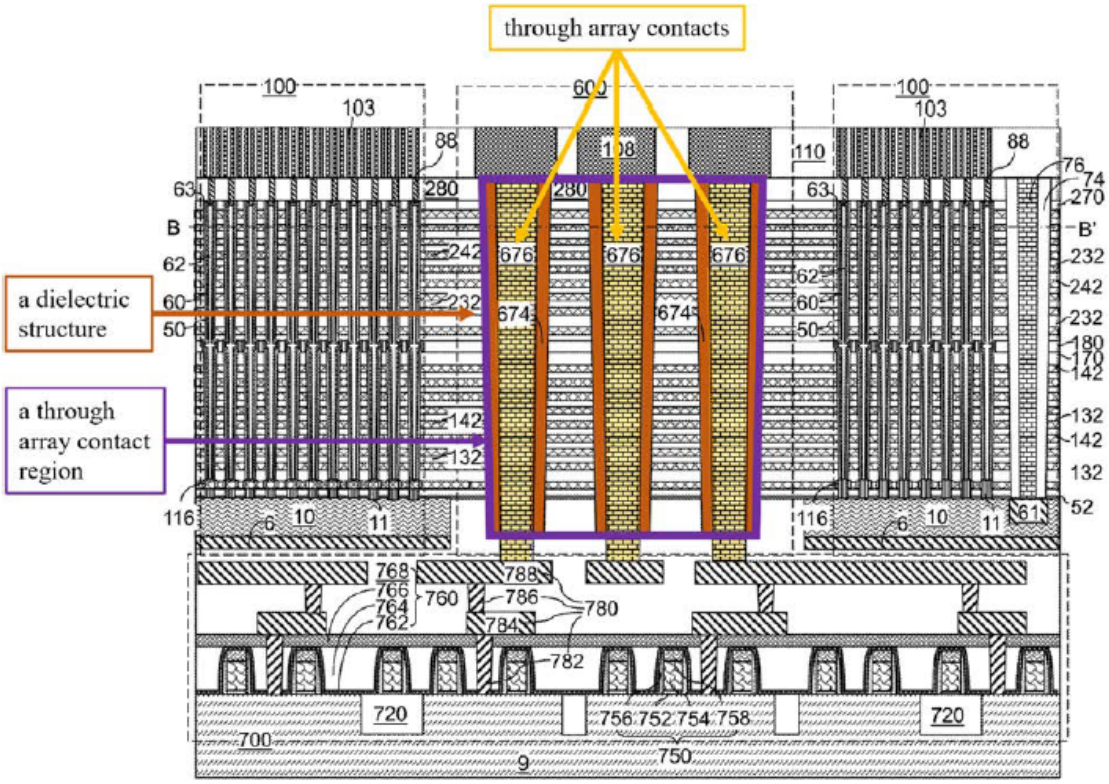


FIG. 49

Toyama's Figure 49 above, with Petitioner's annotations added, depicts though-memory-level via structures 676 (yellow), insulating liners 674 (orange), and through-memory-level via region 600. *See* Pet. 49; Ex. 1005 ¶¶ 341–342, Fig. 49). Petitioner asserts that Toyama's through array contacts (though-memory-level via structures 676 (yellow)) extend

[8] The "through-memory-level via region 600" in Toyama contains the "through-memory-level via structures 676," which Petitioner maps to the TAC region and TACs, respectively. *See* Pet. 44–46.

vertically through the dielectric structure (insulating liners 674 (orange)). Pet. 49–50 (citing Ex. 1005 ¶¶ 341–342, Fig. 49; Ex. 1003 ¶¶ 133–134).

Lastly, Petitioner argues that Toyama's "dummy memory stack structures 55D" surrounding the "through-memory-level via region 600" between the "first and second parts of 'memory array region 100'" disclose a "plurality of non-electrically functional channel structures surrounding the TAC region and between the first and second channel regions" as recited in claim element [8.H]. *Id.* at 50–53 (citing Ex. 1005 Fig. 48B; Ex. 1003 ¶ 137–1408). Petitioner also states that claim 8 does not require non-electrically functional channel structures on four sides of the TAC region, but that a POSITA would have understood (1) that Toyama's dummy memory stack structures 55D encircle Toyama's TAC region or (2) that it would have been obvious to do so. Pet. 52–54 (citing Ex. 1005 ¶¶ 182, 333, Fig. 48B; Ex. 1003 ¶¶ 139–140).

(2) Patent Owner's Response

At this stage of the proceeding, Patent Owner does not challenge many of Petitioner's contentions. Patent Owner, however, does contend that Toyama does not disclose or suggest a *plurality* of TACs extending vertically through *the dielectric structure* as required by claim element [8.G] because Petitioner improperly maps multiple insulating liners 674 to a single dielectric structure. Prelim. Resp. 32–35. Specifically, Patent Owner argues that claim 8 requires that a *plurality of through array contacts* (TACs) extend vertically through a *single dielectric structure*. *Id.* at 34.

(3) Analysis – Claims 8 and 10

Based on the preliminary record, it appears Patent Owner' arguments have merit. As noted above, claim element [8.G] recites "a through array contact (TAC) region formed between first and second channel regions,

wherein the TAC region comprises a *plurality of through array contacts (TACs)* extending vertically through *the dielectric structure*." Ex. 1001, 24:1–5 (emphasis added). A plain reading of claim element 8.G requires *more than one* (i.e., "a plurality") TAC in the TAC region to extend vertically through a *single dielectric structure* (i.e., "*the* dielectric structure"). *Id.*

Based on the present record, it appears Petitioner has not sufficiently shown that Toyama's three insulating liners are a single dielectric structure. *See, e.g.*, Pet. 28–31. Petitioner asserts that because "these components together are something 'that is constructed,' they are a structure." Pet. 30 (citing Ex. 1021, 4; Ex. 1003 ¶ 113); *see also id*. at 30–31 (stating that all insulating liners 674 have the same function as they pass through the alternating stack). We disagree that merely because the three insulating liners are each constructed, that three constructed liners together constitute a single dielectric structure. Petitioner does not sufficiently explain how multiple constructed items can be considered to constitute a single structure just because each one of the multiple items is itself constructed.

We are also not persuaded, at this stage of the proceeding, by Petitioner's argument that, even if dielectric lines 674 are not considered to be a "structure," that the claim encompasses embodiments in which each through array contact extends vertically through a different dielectric structure. Petitioner asserts that because claim 8 uses an open-ended transitional phrase ("comprising") and an indefinite article ("a") preceding "dielectric structure," the claim encompasses a device with multiple dielectric structures. Pet. 31 n.4 (citing *KCJ Corp.*, 223 F.3d at 1356). *KCJ Corp.*, however, does not stand for the proposition that open-ended language with an indefinite article is "patent parlance" for allowing multiple separate

structures to be read "collectively [as] a single structure." While the open-ended language may permit the claimed memory device to have more than one dielectric structure, this does not change the claim language that requires multiple TACs to extend vertically through a single dielectric structure. In other words, even if the claim language's use of indefinite article "a" or "an" or the open-ended transitional phrase "comprising" permits more than one dielectric structure in the memory device, the claim still requires that a plurality of TACs must extend through a single dielectric structure.

Thus, based on the present record, we do not understand Toyama's Second Modification to disclose or suggest a plurality of TACs that extend vertically through a single dielectric structure as required by claim element [8.G].

Petitioner provides additional arguments regarding claim 10, which depends from claim 8. Pet. 53–61. None of Petitioner's arguments address the deficiencies set forth above regarding claim 8. *Id.* Accordingly, Petitioner does not show a reasonable likelihood that claim 10, which depends on claim 8, would have been obvious over Toyama's Second Modification.

However, because we determine that Petitioner has made a sufficient showing that claim 10 would have been obvious over Toyama's First Exemplary Structure (*see* Section II.C.3 below addressing Petitioner's alternative argument 2), we institute *inter pates* review of Petitioner's challenge to claim 10 based on Toyama's Second Modification. *See SAS Inst., Inc. v. Iancu*, 138 S.Ct. 1348, 1359–60 (2018); *PGS Geophysical AS v. Iancu*, 891 F.3d 1354, 1360 (Fed. Cir. 2018) (interpreting the statute to require "a simple yes-or-no institution choice respecting a petition, embracing all challenges included in the petition").

3. Asserted Obviousness over Toyama's First Exemplary Structure (Alternative Argument 2)

Petitioner also contends that claim 10, which depends upon independent claim 8, would have been obvious over Toyama's first exemplary structure ("First Exemplary Structure"). Pet. 61–100. Patent Owner opposes. Prelim. Resp. 40–52. For the reasons stated below, Petitioner has shown a reasonable likelihood that claim 10 would have been obvious over Toyama's First Exemplary Structure.

Because claim 10 depends from claim 8, we first address Petitioner's assertions that claim 8 would have been obvious over Toyama's First Exemplary Structure.

(a) Claim 8

(1) Petitioner's Contentions

Petitioner contends that Toyama's First Exemplary Structure[9] teaches or renders obvious all elements of independent claim 8. Pet. 61–97. For example, Petitioner asserts that Toyama discloses a three dimensional non-volatile memory device having an alternating conductor/dielectric layer stack ("alternating stack (132, 146, 232, 246)") as recited in the preamble and claim element [8.A]. *Id.* at 61–62 (citing Ex. 1005 ¶¶ 156, 172, Fig. 17A; Ex. 1003 ¶ 159).

Petitioner asserts that, as shown in Toyama's Figure 15A reproduced below, the upper part of "dielectric fill material portion 430" is a dielectric structure that extends vertically through alternating conductor/dielectric stack, (elements 132, 146, 232, 246 highlighted in green and yellow) as required by claim element [8.B]. *Id.* at 63–69 (citing, *inter alia*, Ex. 1005,

[9] Toyama's First Exemplary Structure is depicted in Figures 1–17 of Toyama. *See* Ex. 1005 ¶¶ 14–49.

126, 173, 190, 213, 216, Figs. 10A, 15A, 16B; Ex. 1003 ¶¶ 162–166); *see also id.* at 68–69 (stating that Toyama's First Exemplary Structure removes layers 132, 142, 232, 242 to form opening 769, which is then filled with dielectric fill material portion 430).

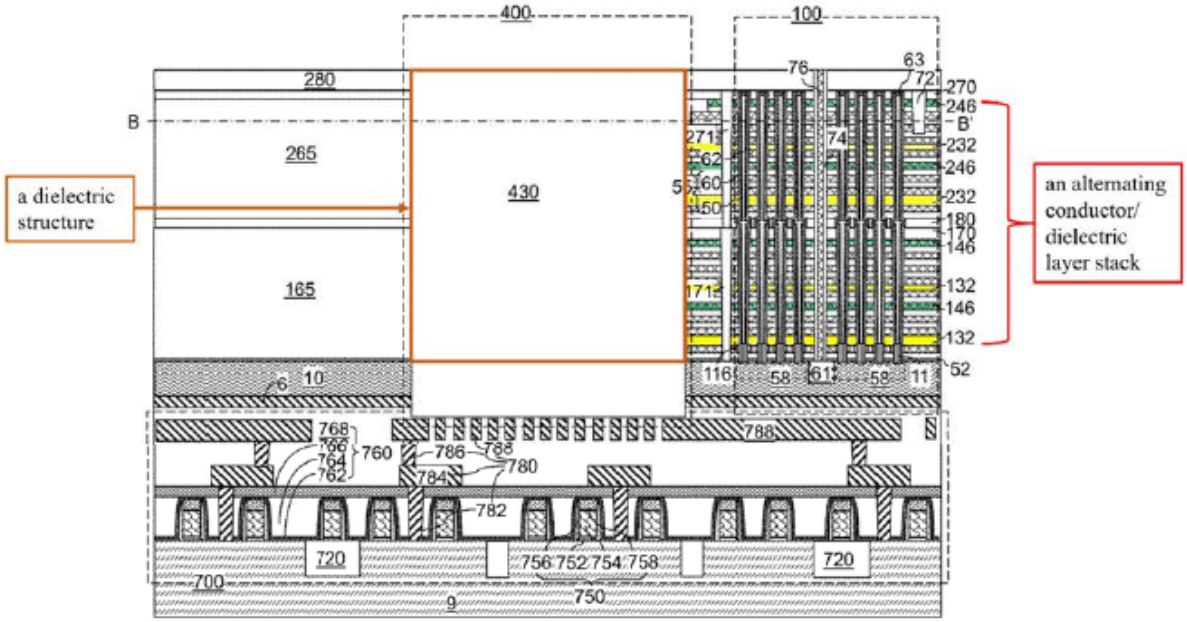


FIG. 15A

Toyama's Figure 15A above, with Petitioner's annotations added, "is a vertical cross-sectional view of the first exemplary structure after formation of electrically conductive layers, insulating spacers, and backside contact via structures." Pet. 65; Ex. 1005 ¶ 39, Fig. 15A.

Petitioner asserts that Toyama renders obvious the "first and second channel regions comprising first and second pluralities of channel structures, respectively" recited in claim element [8.C]. Pet. 70–83. Pointing to, *inter alia,* Toyama Figure 16B reproduced below, Petitioner asserts that each of Toyama's memory stack structures 55 (green) is a channel structure and that part of Toyama's memory array region 100 (red) form a channel region. *Id.* at 70–71.

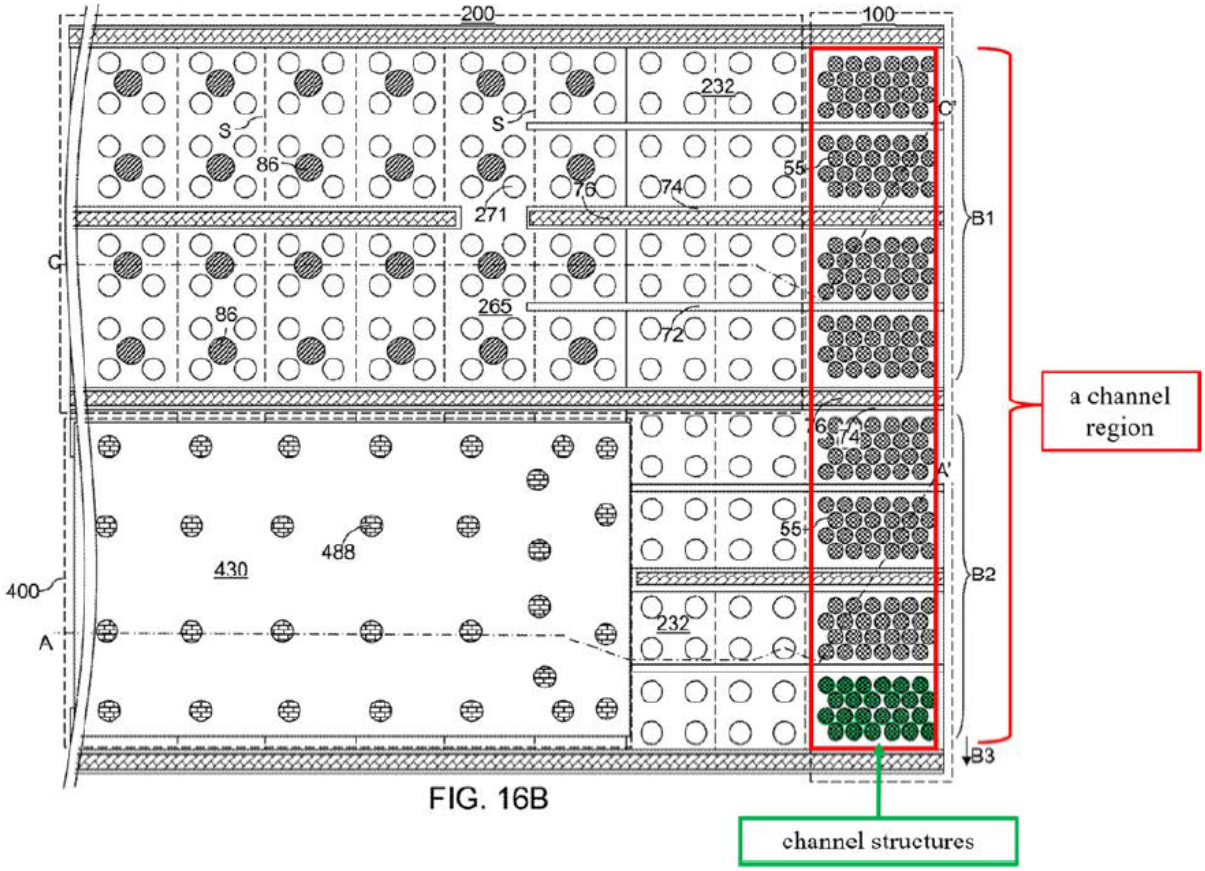
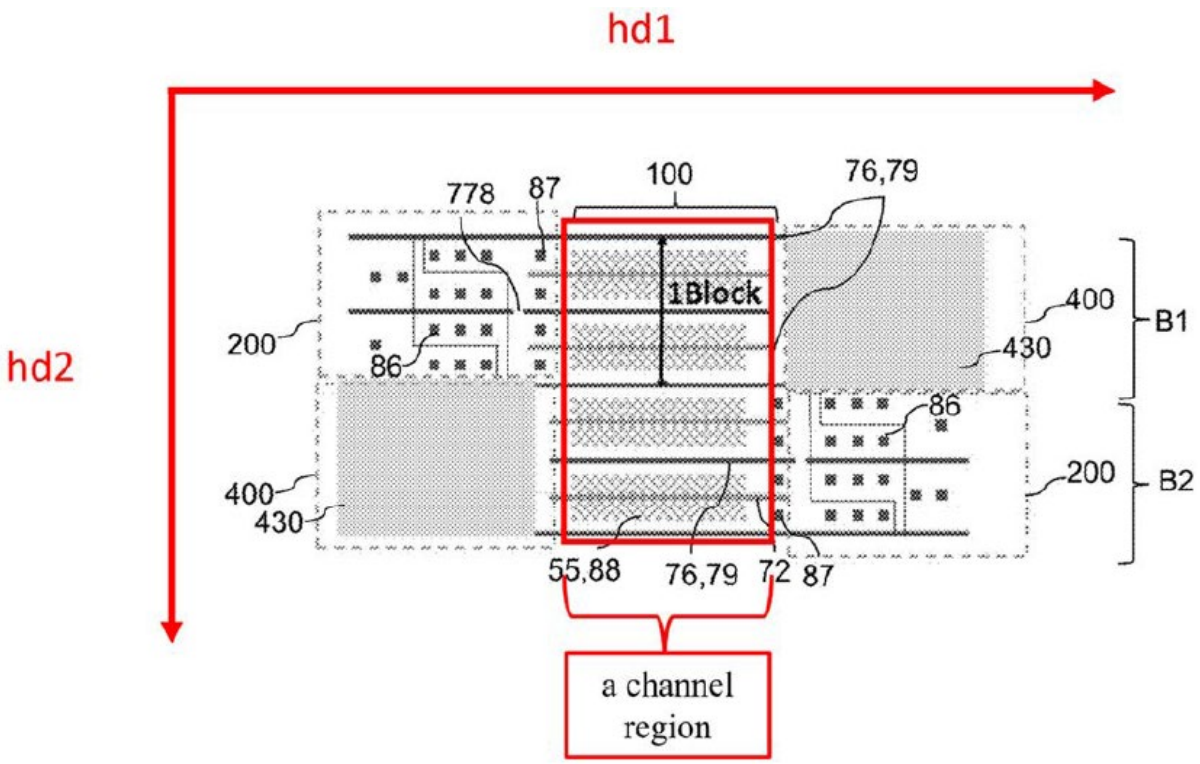


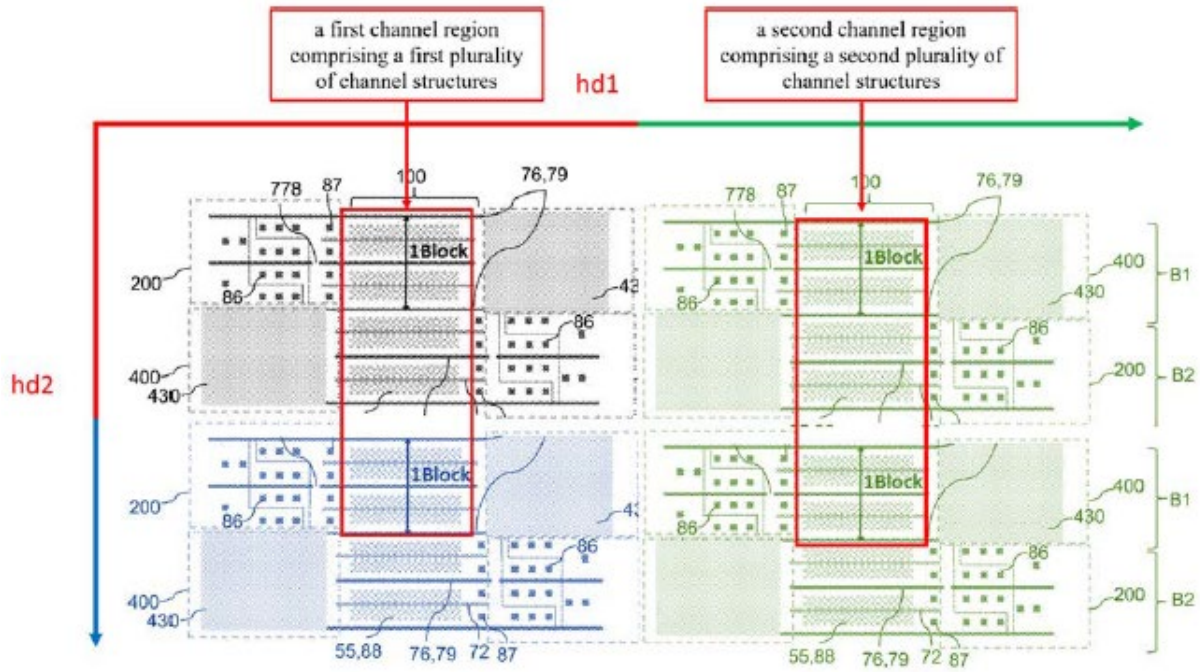
Figure 16B is a horizontal cross-sectional view of the first exemplary structure along the horizontal plane B-B' in Figure 16A. Ex. 1005 ¶ 43, Fig. 16B; Pet. 71.

Petitioner further asserts that memory array region 100 (red) in Toyama's Figure 17E, reproduced below, is also a channel region.



Toyama's Figure 17E, with Petitioner's annotations added, is a top-down view of an alternative exemplary structure according to the first embodiment of the present invention, that Petitioner asserts may be used with Toyama's first exemplary structure. Ex. 1005 ¶ 49; Pet. 71–72.

Petitioner asserts that Toyama expressly shows that the layout in Figure 17E repeats in the hd2 (up-down) direction and that a POSITA would have found it obvious to also repeat the layout in the hd1 (left-right direction), as shown in the modified Figure 17E below. Pet. 72–73 (citing Ex. 1005 ¶ 220; Ex. 1003 ¶ 170), 82 (citing Ex. 1003 ¶ 181).



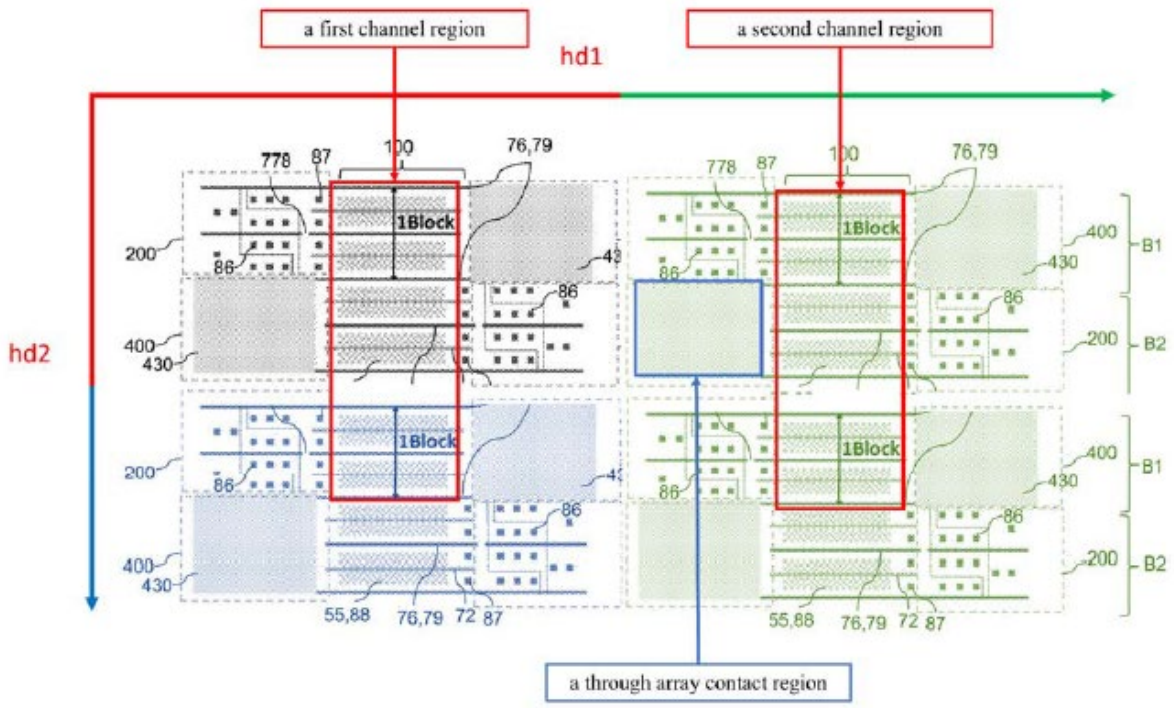
Petitioner's Modified Figure 17E depicts the layout of Figure 17E repeated in both the hd1 (left-right) and hd2 (top-down) direction. *See* Pet. 74, 83.

Petitioner asserts that modified Figure 17E depicts first and second channel regions (first and second parts of memory array regions 100 (red)) comprising first and second pluralities of channel structures (first and second pluralities of memory stack structures 55) as required by claim element [8.C]. Pet. 83 (citing Ex. 1003 ¶¶ 183–184). Petitioner contends that a POSITA would have known to implement, and the numerous benefits of, such a multi-plane flash memory device. *See id.* at 74–80 (citing, *inter alia*, Ex. 1003 ¶¶ 172–178). Petitioner asserts that a multi-plane memory device renders it possible to issue a read command on multiple planes simultaneously, improves the throughput of program operations, i.e., writing data to the flash memory), and improves the performance of NAND based systems. *Id.* at 79–80 (citing Ex. 1025, 42, 44–45, 171; Ex. 1003 ¶¶ 172–178). Petitioner also asserts that a POSITA would have had a reasonable

expectation of success in implementing multiple planes of Toyama's first exemplary structure in the hd1 direction because NAND flash memory devices with multiple planes existed for many years before the priority date of the '806 patent and repeating the layout in Figure 17E for each plane would have been straightforward and predictable. *Id.* at 81–82 (citing Ex. 1003 ¶ 181); *see also id.* at 76–80 (providing examples of multi-plane flash memory devices). Dr. Lee testifies that this modification is nothing more than applying a known technique (implementing multiple planes of a NAND flash memory array) to a known device (Toyama's first exemplary structure) to yield predictable results (a NAND flash device with improved performance). *See, e.g.*, Ex. 1003 ¶ 182.

With respect to claim element [8.D], Petitioner asserts that Toyama's laterally-elongated contact via structures 76 are the "slit structures" that extend vertically through the alternating conductor/dielectric layer stack ("alternating stack 132, 146, 232, 246"). Pet. 84–85 (citing Ex. 1005, Fig. 17A, 17B; Ex. 1003 ¶¶ 185–187; Pet. § IX.A.5). Petitioner also asserts that Toyama discloses staircase regions (a "staircase structure") that is disposed in alternating stack 132, 146, 232, 246 (an "alternating conductor/dielectric stack layer") as required by claim element [8.E]. *Id.* at 85–86 (citing Ex. 1003 ¶ 188; Ex. 1005, Fig. 17C). Petitioner also contends that Toyama discloses local contacts ("drain contact via structures 88") disposed on (in contact with and extending above) the channel structures ("memory stack structures 55"), and local contacts ("source connection via structures 91") disposed on (above) the slit structures ("laterally-elongated contact via structures 76") as recited in claim element [8.F]. *Id.* at 86–87 (citing Ex. 1005 ¶ 251, Fig. 17A; Ex. 1003 ¶¶ 189–190; Pet. § IX.A.7).

Claim element [8.G] recites "a through array contact (TAC) region formed between the first and second channel regions, wherein the TAC region comprises a plurality of through array contacts (TACs) extending vertically through the dielectric structure." Petitioner admits that Toyama does not expressly disclose a TAC region formed between the first and second channel regions, but asserts that the limitation would have been obvious to implement in the multiple planes of Toyama's first exemplary structure in the hd1 direction. Pet. 89. Petitioner asserts that, as shown in Toyama's modified Figure 17E below, the TAC region is formed between the first and second channel regions. *Id.*



Toyama's modified Figure 17E, with Petitioner's modifications and annotations added, depicts a top-down view of an alternative exemplary structure according to the first embodiment of the invention, having first and second channel regions (red) and a through array contact (TAC) region (blue). Ex. 1005 ¶ 50; Pet. 89–90 (citing Ex. 1003 ¶¶ 196–197).

Petitioner asserts that Toyama's through-memory level via structures 488 are through array contacts that extend vertically through part of dielectric fill material portion 430 (dielectric structure) as recited in claim element [8.G]. Pet. 90–91 (citing Ex. 1005 ¶ 239, Fig. 17A; Ex. 1003 ¶¶ 193–194).

Claim element [8.H] recites a "plurality of non-electrically functional channel structures surrounding the TAC region and between the first and second channel regions." Petitioner asserts that Toyama's "first-tier support pillar structures 171" and "second-tier support pillar structures 271" are, or render obvious, a plurality of non-electrically functional channel structures. Pet. 92–97 (citing Ex. 1005 ¶¶ 182, 197, 203, 311, Figs. 16B, 17A, 17E; Ex. 1003 ¶¶ 199–201, 203–204, 206; Ex. 1016 ¶ 162; Ex. 1017, 9:50–67; Ex. 1015 ¶¶ 73–81). In particular, Petitioner contends that a POSITA would have understood Toyama's first-tier support pillar structures, which "comprise dummy stack structures [that] are not electrically connected to bit lines" are non-electrically functional channel structures. Pet. 93–94 (citing Ex. 1005 ¶ 200). Petitioner also asserts that a POSITA would have understood that (1) Toyama's second-tier support pillar structures 271 are also dummy memory stack structures or (2) it would have been obvious to form Toyama's support pillar structures 171, 271 as dummy stack structures because they provide structural support and can be formed in the same process steps as the functional channel structures. Pet. 94–95 (citing Ex. 1005 ¶ 311; Ex. 1016 ¶ 162; Ex. 1017, 9:50–67; Ex. 1015 ¶¶ 73–81; Ex. 1003 ¶¶ 201, 203)).

(2) Patent Owner's Response

At this stage of the proceeding, Patent Owner does not challenge many of Petitioner's contentions. Patent Owner, however, does argue that Toyama's First Exemplary Structure does not disclose or suggest "a through

array contact (TAC) region formed between the first and second channel regions" as required by claim element [8.G] because the TAC region only has a channel region on one side. Prelim. Resp. 40–47. Patent Owner asserts that a POSITA would not modify Toyama to repeat portions of the device in the hd1 direction and add a second channel region, as asserted by Petitioner, because doing so would omit necessary neighboring structures, such as the driver circuit that connects to the memory structure on the second side. *Id.* at 42–42; *see also id.* at 45–47 (stating Toyama's layout cannot be repeated in the hd1 direction because Toyama includes peripheral circuitry, such as "driver circuitry," beyond the alleged TAC region and citing Ex. 1005 ¶ 163); Ex. 1005 ¶ 163 (stating the "semiconductor devices can include any semiconductor circuitry to support operation of a memory structure to be subsequently formed, which is typically referred to as a driver circuitry, which is also known as peripheral circuitry).

Patent Owner asserts that Petitioner's proposed modification "ignores the peripheral circuitry, including the driver circuit, and therefore would not work." Prelim. Resp. 46; *see also id.* at 47 (stating "none of the circuitry needed to operate each memory array is included in Petitioner's analysis" and that Petitioner's modification "lacks the necessary support circuitry for a functioning memory device").

(3) Analysis

Based on the preliminary record, we determine Petitioner shows a reasonable likelihood of prevailing on its second alternative argument that claim 8, from which challenged claim 10 depends, would have been obvious over Toyama's First Exemplary Embodiment.

With respect to claim element [8.G]'s requirement that the memory device comprise a TAC region formed between the first and second channel

regions, Petitioner provides sufficient argument with supporting evidence that a POSITA would have reason to modify Toyama First Exemplary Structure, which has a channel region (memory array region 100) on only one side of the TAC region (part of "through-memory-level via region 400"), to extend the device in the hd1 region and that such a modified device, having multiple planes, would have a TAC region formed between the first and second channel regions as required by claim element [8.G]. Pet. 71–83, 87–91.

Patent Owner's contention that Petitioner's arguments are based on hindsight and that a POSITA would not modify Toyama to repeat in the hd2 direction—because doing so "does not account for the necessary driver circuitry" and that Petitioner's proposed modification would not work—raises factual issues that are best resolved on a full record. Prelim. Resp. 40–47.

Petitioner provides sufficient argument and evidence at this stage of the proceeding that a POSITA would have modified Toyama to provide a multi-plane flash memory device that could issue a read command on multiple planes simultaneously, thereby improving the throughput of program operations and the performance of NAND based systems. *Id.* at 74–80 (citing, *inter alia,* Ex. 1023, 144; Ex. 1014, 308, 313–314). Petitioner also provides sufficient arguments and evidence that this solution was quite common because power issues related to this kind of solution are still manageable inside the chip and optimized versus two separate NAND devices active at the same time. *Id.* at 79–80 (citing Ex. 1025, 44–45, 171).

Petitioner also provides sufficient argument and evidence that a POSITA would have had a reasonable expectation of success in implementing multiple planes of Toyama's First Exemplary Structure in the

hd1 direction because NAND devices having multiple planes existed for many years before the priority date of the ’806 patent and that implementation of such a structure would have been straightforward as it merely applies a known technique (implementing multiple planes of NAND flash memory array) to a known device (Toyama’s first exemplary structure) to yield predictable results (a NAND flash device with improved performance). Pet. 74–82 (citing, *inter alia*, Ex. 1003 ¶¶ 179–182); *see also* Ex. 1003 ¶¶ 172–182 (stating a POSITA would have known how to implement multiple planes in Toyama’s memory device using the same approach discussed earlier in the declaration); *see also* Ex. 1003 ¶¶ 172–178 (citing, *inter alia*, Ex. 1023, 144, 247, Fig. 6.1; Ex. 1024, 13:37–44; Ex. 1014, 308, 313–314; Ex. 1025, 42, 44–45, 171).

Accordingly, at this stage of the proceeding, Petitioner sufficiently shows that a POSITA would have had reason to modify Toyama’s First Exemplary Structure to repeat portions of the device in the hd1 direction in order, *inter alia*, to improve performance of the device and would have done so with a reasonable expectation of success, and that such a modification results in a TAC region formed between first and second channel regions as required by claim element [8.G], notwithstanding Patent Owner’s arguments to the contrary, which raise issues best resolved on a full record.

At this stage of the proceeding, Patent Owner does not address Petitioner’s specific contentions with respect to the other limitations of claim 8. We reviewed Petitioner’s contentions for the remaining limitations and determine Petitioner sufficiently shows that Toyama teaches or suggests these remaining limitations. Pet. 61–87, 92–97.

Accordingly, based on the record before us, we are persuaded that Petitioner sufficiently shows a reasonable likelihood that claim 8, from

which challenged claim 10 depends, would have been obvious over Toyama's First Exemplary Structure.

(b) Claim 10

Claim 10 depends from claim 8 and further requires, in general, a substrate [10.A], an etch stop plug [10.B], and an epitaxial layer [10.C]. *See* Ex. 1001, 23:13–20.

(1) Claim elements [10.A] and [10.C]

Petitioner asserts that Toyama's planar semiconductor material layer 10 discloses the substrate recited in claim element [10.A]. Pet. 98 (citing Pet. 53–54; Ex. 1005 ¶ 211; Fig. 17A; Ex. 1003 ¶ 207). Petitioner also asserts that Toyama's pedestal channel portions 11 disclose or suggest the "epitaxial layer disposed between the substrate and the first or second channel structures" recited in claim element [10.C]. Pet. 99–100 (citing Pet. 59–61; Ex. 1005 ¶¶ 202, 208, 225, Fig. 17A; Ex. 1003 ¶¶ 217–220). Petitioner further asserts that a POSITA would have known to form Toyama's pedestal channel portions 11, which are known to improve memory channel reliability, as an epitaxial layer because an epitaxy is a known and desirable method of forming crystalline material. Pet. 61 (citing Ex. 1003 ¶ 156).

At this stage of the proceeding, Patent Owner does not dispute these assertions. We have reviewed Petitioner's assertions and determine that Petitioner sufficiently shows that Toyama's First Exemplary Structure discloses or suggests the limitations recited in claim elements [10.A] and [10.C].

(2) Claim element [10.B]

Claim element [10.B] recites "an etch stop plug interposed between each local contact of the local contacts and each channel structure of the first and second channel structures." Ex. 1001, 24:16–18.

Petitioner asserts that Toyama Figure 17A (reproduced below) shows drain region 63 ("an etch stop plug") highlighted in blue that is interposed between drain contact via structures 88 (" a local contact") highlighted in purple on memory stack structures 55 ("one or more channel structures") highlighted in red. Pet. 98–99 (citing Pet. 54–59 (§ IX.B.3); Ex. 1005, 209, 241–242, Fig. 19A; Ex. 1003 ¶¶ 208–216); *see also id.* at 54–59 (discussing, *inter alia*, Toyama Fig. 49) .

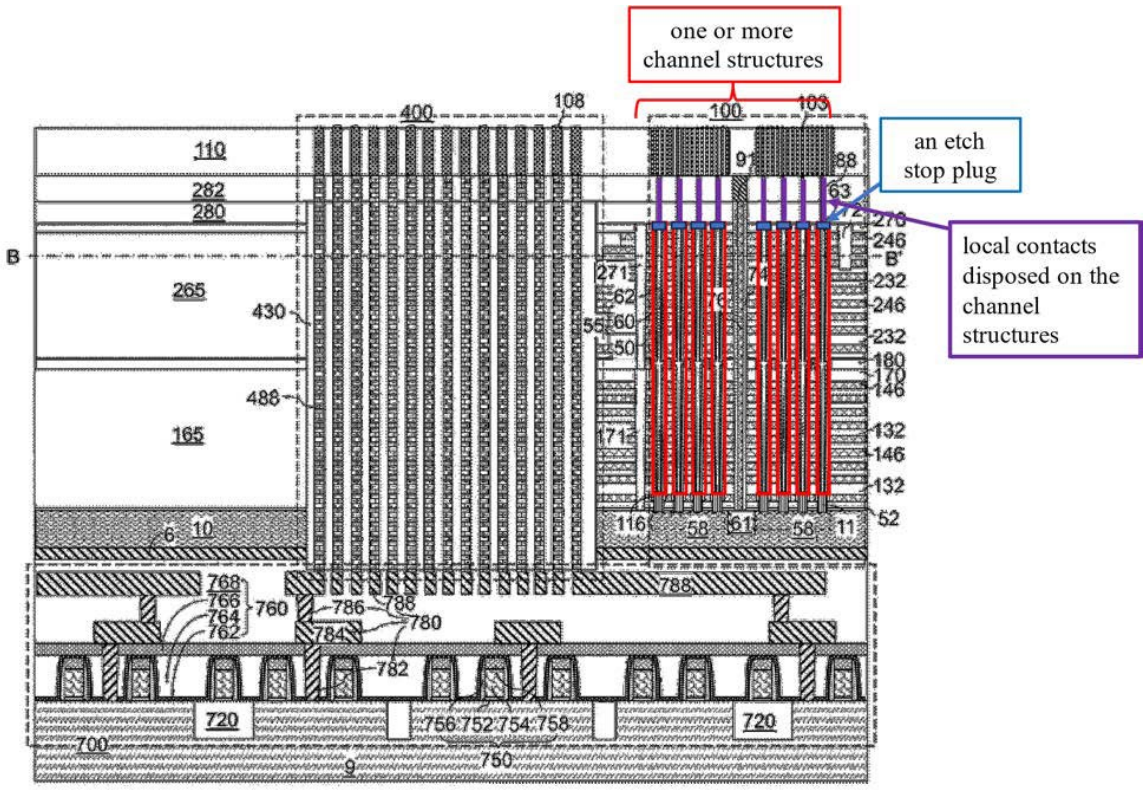


FIG. 17A

Toyama's Figure 17A, with Petitioner's color annotations added, is a vertical cross-sectional view of the first exemplary structure after formation of upper level line structures. Ex. 1005 ¶ 45; Pet. 98–99.

Petitioner states that each of Toyama's drain regions 53 is an etch stop because drain regions 53 stop the etch that forms drain contact via structures 88. Pet. 99.

Patent Owner responds that Toyama does not disclose or suggest claim element [10.B] because the asserted etch stop plugs are not interposed between *each* of the purported local contacts and channel structures. Prelim. Resp. 48. Referring to Patent Owner's annotated version of Toyama Figure 17A (reproduced below), Patent Owner states Petitioner asserts that Toyama's *source connection via structures 91* (highlighted in orange), in addition to the drain contact via structure 88, are the claimed local contacts disposed on the first and second channel structures and the slit structures. *Id.* (citing Pet. 70–85, 86–87).

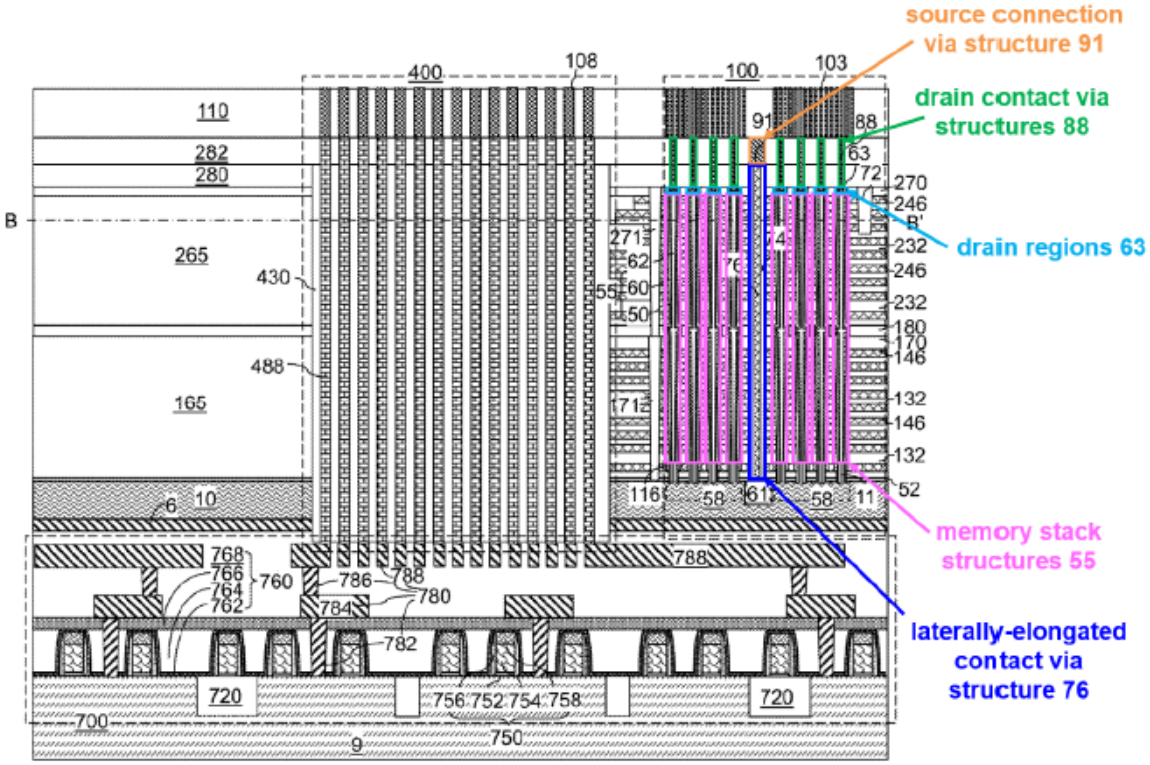


FIG. 17A

Toyama's Figure 17A, with Patent Owner's color annotations added, is a vertical cross-sectional view of the first exemplary structure after formation of upper level line structures. Ex. 1005 ¶ 45; Prelim. Resp. 49.

Patent Owner asserts that Petitioner only addresses Toyama's *drain contact via structures 88 (green)* but not *source connection via structures 91 (orange)*. Prelim. Resp. 50. Patent Owner states that because claim 10 requires an etch stop plug interposed between each local contact of the local contacts and each channel structure of the first and second channel structures, Petitioner needed to identify an etch stop plug that is also interposed between the *source connection via structures (orange)* and the *memory stack structures (purple)*, but failed to do so. *Id.* Patent Owner states that Petitioner maps the antecedent basis for "the local contacts" to **both** the drain contact via structures (green) and the source connection via structures (orange) and therefore needs to identify etch stop plugs between *both of these structures* and the purposed channel structures. *Id.*

Patent Owner further states that "[n]one of the drain regions 63 [highlighted in blue], however, is 'interposed between' the source connection via structures 91 [highlighted in orange] and memory stack structures 55 [highlighted in purple] as required by limitation [10.B]." Prelim. Resp. 51 (referring to Toyama Fig. 17A with Patent Owner's highlighting added).

We disagree with Patent Owner's argument as it is based on a claim construction that we do not adopt at this stage of the proceeding. As explained above in Section II.B.1, we construe the "each local contact of the local contacts" recited in claim 10 to refer to each channel structure local contact and not to each slit structure local contact.

Petitioner provides sufficient argument and evidence that Toyama's drain region 63 is an etch stop plug that is interposed between drain contact via structures 88 (each channel structure local contact of the local contacts) and memory stack structures 55 (each channel structure of the first and second channel structures) as required by claim 10. Pet. 98–99; Ex. 1005, ¶¶ 209, 241–242, Fig. 17A; Ex. 1003 ¶¶ 208–216.

Accordingly, based on the record before us, we are persuaded that Petitioner sufficiently shows a reasonable likelihood that claim 10 would have been obvious over Toyama's First Exemplary Structure.

4. Asserted Obviousness over Toyama's First Exemplary Structure in View of Toyama's Second Modification of its Fourth Exemplary Structure (Alternative Argument 3)

Petitioner argues that claim 10, which depends from claim 8, would have been obvious over Toyama's First Exemplary Structure in view of Toyama's Second Modification. Pet. 100–125. Patent Owner opposes. Prelim. Resp. 52–61.

Having already determined that Petitioner demonstrates a reasonable likelihood that at least one claim would have been obvious, we need not address this ground in full. We offer the following comments in response to the parties' arguments and evidence to provide guidance to the parties.

(a) Claim 8

(1) Parties' Arguments

Petitioner argues that a POSITA would have found it obvious to modify "Toyama's Second Modification that forms the 'through-memory-level structures' within a unitary dielectric fill material (as in Toyama's first exemplary structure) instead of using the Second Modification's 'insulating liners 674." Pet. 100. Petitioner relies on Toyama's statement that

"'through-memory-level via structures' can be electrically isolated from the 'alternating stack' by a unitary 'dielectric fill material portion 430.'" *Id.* at 101–102 (pointing to annotated Figure 17A). Petitioner further argues that a POSITA would have been motivated to substitute the insulating liners 674 with a unitary dielectric fill material portion 430 because it would "isolate[] the 'through-memory-level via structures,'" which would be "desirable because otherwise the 'through-memory-level via structures' may electrically interfere with each other and/or with other of the Second Modification's conductive elements." *Id.* at 106. Petitioner also argues that such modification would "reduce capacitive coupling"[10] because it would increase the separation of the conductive elements. *Id.* at 107–108. Lastly, Petitioner argues that the proposed modification would have an additional benefit over Toyama's first exemplary structure, namely that "placing the 'through-memory-level via structures' [would be] closer to the elements that use the signals carried by the [via structures]," leading to benefits that include "reducing signal propagation delays and electrical losses." *Id.* at 108–109 (citing Ex. 1003 ¶ 231).

Petitioner also argues that a POSITA would have had a reasonable expectation of success of combining the teachings because "Toyama notes that the 'second modification of the fourth exemplary structure can be formed concurrently with the formation of any of the first, second, and third exemplary structures or modifications thereof, or can be formed as a stand-alone structure." *Id.* at 109–110 (quoting Ex. 1005 ¶ 332). Petitioner states

[10] Petitioner describes capacitive coupling as "an undesirable phenomenon that causes a signal in one conductive element to affect a signal in a different conductive element where the two conductive elements are separated by an insulator." Pet. 107 (citing Ex. 1003 ¶ 228).

that "Toyama further notes that 'where an embodiment employing a particular structure and/or configuration as illustrated in the present disclosure, it is understood that the present disclosure may be practiced with any other compatible structures and/or configurations that are functionally equivalent provided that substitutions are not explicitly forbidden or otherwise known to be impossible to a [POSITA].'" *Id.* at 110 (quoting Ex. 1005 ¶ 390). In other words, Petitioner argues that even if Toyama does not explicitly disclose Petitioner's proposed combination it, nonetheless, would have been obvious because Toyama contemplates employing functionally equivalent substitutions of its disclosed structures. Petitioner argues that a POSITA "would have [also] understood how to manufacture a device implementing the obviousness combination" and that the elements of the proposed combination "are compatible with each other" in part because these are "largely the same [structures]" with "a similar purpose." *Id.* at 110–111 (citing Ex. 1003 ¶¶ 236–239).

Patent Owner responds that Petitioner's modifications to Toyama's First Exemplary Structure in view of Toyama's Second Modification are mere "hindsight . . . as it replaces conductive material . . . with a large dielectric (an insulator), and Petitioner does not even attempt to address the impact that these changes would have had on Toyama's memory structure." Prelim. Resp. 53. According to Patent Owner, "[a] POSITA would not have added a unitary dielectric fill material to Toyama's [Second Modification] because this modification removes large portions of the conductive layers in the active region that form the word lines and replaces them with an insulator." *Id.* at 55. The impact of such modification, argues Patent Owner, is that replacing the "[conductive] word lines" with "a large insulator would eliminate [the current that controls the memory]." *Id.* Such

dielectric fill modification would "cause the device to fail," which is why, Patent Owner argues, Toyama "does not teach forming a unitary dielectric block in the memory array region between two channel regions." *Id.* at 57–58.

Patent Owner also disagrees with Petitioner's argument that reducing "capacitive coupling" is a motivation to combine the structures because "Toyama's Second Modification already 'minimizes' capacitive coupling [with the dielectric liners [674]]." *Id.* at 58–59 (citing Ex. 1005 ¶ 377). Furthermore, Patent Owner attacks Petitioner declarant's testimony because "he fails to address that capacitive coupling is also a function of the length (or area) of overlap" between conductive elements and not just a function of the "distance between conductive elements." *Id.* (citing Ex. 1003 ¶ 228).

Patent Owner further disagrees with Petitioner's alleged benefits of "placing the through-memory-level via structures (the alleged TACs) in the memory array region 100," stating that "Toyama's Second Modification . . . already has through-memory level via structures (the alleged TACs) in the memory array region." Prelim. Resp. 59. Because "Petitioner is not proposing moving the alleged TACs . . . any benefits of having the alleged TACs in [the memory array region] are irrelevant to whether a POSITA would [add a unitary dielectric fill material]." *Id.* Lastly, Patent Owner argues that the proposed modification is not shown to be "compatible" by Petitioner and a showing that "a POSITA could ***manufacture*** the device" has no bearing on a "motivation to make the proposed combination." *Id.* at 59–60 (emphasis in Prelim. Resp.).

(2) Analysis – Claim 8 and 10

On this record, we find that Patent Owner's arguments may have merit. As Patent Owner points out, based on the present record, Petitioner

does not appear to address the impact of replacing the region containing conductive word lines with dielectric fill material. Based on the preliminary record, it appears that replacing the conductive word lines with insulating material would eliminate the current that controls the memory, resulting in a non-functioning device. *See, e.g.*, Prelim. Resp. 53–56.

Petitioner provides additional arguments regarding claim 10, which depends from claim 8. Pet. 124–125. None of Petitioner's arguments address the deficiencies set forth above regarding claim 8. *Id.* However, because we determine that Petitioner has made a sufficient showing that claim 10 would have been obvious over Toyama's First Exemplary Structure (*see* Section II.C.3 above addressing Petitioner's alternative argument 2), we institute *inter partes* review of Petitioner's challenge to claim 10 based on Toyama's First Exemplary Structure in view of Toyama's Second Modification.

D. Discretion under 35 U.S.C. § 325(d)

Patent Owner argues that the Board should exercise its discretion to deny institution under 35 U.S.C. § 325(d) because the asserted reference, Toyama, was previously presented to the Office and the Examiner did not err in a manner material to patentability in allowing the claims over Toyama. Prelim. Resp. at 18–29.

1. Legal Framework

Under Section 325(d), the Director has the discretion to deny a petition that presents the same or substantially the same prior art or arguments as previously presented to the Office. The Board uses the following two-part framework for evaluating arguments under Section 325(d):

> (1) whether the same or substantially the same art previously was presented to the Office or whether the same or substantially the same arguments previously were presented to the Office; and
>
> (2) if either condition of first part of the framework is satisfied, whether the petitioner has demonstrated that the Office erred in a manner material to the patentability of challenged claims.

Advanced Bionics, LLC v. Med-El Elektromedizinische Geräte GmbH, IPR2019-01469, Paper 6, 8 (PTAB Feb. 13, 2020) (precedential) ("*Advanced Bionics*"). In applying this two-part framework, we consider the following non-exclusive factors:

> (a) the similarities and material differences between the asserted art and the prior art involved during examination;
>
> (b) the cumulative nature of the asserted art and the prior art evaluated during examination;
>
> (c) the extent to which the asserted art was evaluated during examination, including whether the prior art was the basis for rejection;
>
> (d) the extent of the overlap between the arguments made during examination and the manner in which Petitioner relies on the prior art or Patent Owner distinguishes the prior art;
>
> (e) whether Petitioner has pointed out sufficiently how the Examiner erred in its evaluation of the asserted prior art; and
>
> (f) the extent to which additional evidence and facts presented in the Petition warrant reconsideration of prior art or arguments.

Becton, Dickinson & Co. v. B. Braun Melsungen AG, IPR2017-01586, Paper 8 at 17–18 (PTAB Dec. 15, 2017) (precedential). Factors (a), (b), and (d), relate to whether the same or substantially the same art or arguments were previously presented to the Office, and factors (c), (e), and (f) relate to whether the petitioner demonstrates that the Office erred in a manner material to the patentability of the claims. *Advanced Bionics*, Paper 6 at 9–11. Only if the same or substantially the same art or arguments were

previously presented to the Office do we then consider whether the petitioner has demonstrated a material error by the Office. *Id.*

2. Part One of the Advanced Bionics *Framework*

Patent Owner argues, and Petitioner does not dispute, that part one of the *Advanced Bionics* framework is met because Toyama was cited on an Examiner initialed Information Disclosure Statement ("IDS") and therefore was previously presented to the Office. *See* Pet. 10; Prelim. Resp. 20–21. Accordingly, we move on to part two of the framework.

3. Part Two of the Advanced Bionics *Framework*

Patent Owner contends Petitioner fails to show that the Office erred in a manner material to the patentability of the challenged claims, as required by part two of the *Advanced Bionics* framework. Prelim. Resp. 21–29. For example, Patent Owner asserts Toyama does not disclose forming TACs in a dedicated TAC region hosted by a dielectric structure between two channel regions. *Id.* at 22. Patent Owner asserts that Toyama's First Exemplary Structure lacks first and second channel regions such that a TAC region is between the first and second channel regions. *Id.* at 25. Patent Owner further asserts that Toyama intentionally does not teach repeating blocks in the hd1 direction to provide a TAC region between two channel regions, as asserted by Petitioner, because the inactive staircase regions are on the sides of Toyama's device and multiplying the inactive space is "non-sensical," repeating blocks in the hd1 direction would eliminate necessary circuitry on the side of the array, and there is no motivation to make such a change. *Id.* at 26. Patent Owner also argues that Petitioner fails to propose a mapping in accordance with the plain language of claim 10, which requires each of the local contacts to have etch stop plugs interposed between it and a channel structure. Prelim. Resp. 28.

As described above in Section II.C.3 above, Petitioner provides arguments and evidence, including declaration testimony not before the Office, to show that a POSITA would have had reason to modify Toyama to repeat blocks in the hd1 direction with a reasonable expectation of success and that such a modification would suggest the subject matter of independent claim element 8. We also note that, although Toyama was cited on an IDS, the reference was not expressly addressed by the Examiner nor used as the basis for a rejection. For at least these reasons, we find that Petitioner demonstrates that the Examiner erred in a manner material to the patentability of the challenged claims by misapprehending or overlooking whether a POSITA would have had reason to modify Toyama to repeat blocks in the hd1 direction to arrive at the subject matter of independent claim 8, from which challenged claim 10 depends. Additionally, we disagree with Patent Owner's argument regarding the patentability of claim 10 because it is based on a claim construction that we do not adopt at this stage of the proceeding. *See* Prelim. Resp. 28.

Accordingly, we determine that the Petition establishes that the Office erred in a manner material to the patentability under the second part of the *Advanced Bionics* framework. As such, we decline to exercise our discretion to deny institution under § 325(d).

E. Discretion under 35 U.S.C. § 314(a) Due to Parallel Petitions

As noted above, the present Petition is the second petition filed by Petitioner challenging the patentability of the '806 patent. Petitioner asserts that institution of the present Petition, in addition to the earlier filed 791 IPR, is warranted because (1) the 791 IPR did not challenge dependent claim 10 because Patent Owner had not yet alleged infringement of this claim when the petition was filed and there is no overlap in claims between the two sets

of petitions, and (2) any additional burden on the Board or on Patent Owner resulting from multiple petitions in this case should be negligible. Paper 3, 2–3.

Patent Owner does not oppose Petitioner's claim that Petitioner needs a second petition. Prelim. Resp. 1 n.2.

Based on the particular circumstances presented here, we determine Petitioner has presented a reasonable explanation that a second petition is warranted in order to challenge claim 10, which was asserted in the district court litigation after the earlier petition was filed.

We also note that the present proceeding and the 791 IPR proceeding can be coordinated and that a similar or common schedule can be adopted, thus decreasing the inconvenience to the Patent Owner. The parties may seek to consolidate the two proceedings, including requesting a consolidated briefing schedule, and/or oral hearing, which would result in even more efficiencies for the parties.

Thus, given the particular circumstances of this case, Petitioner has sufficiently shown that it requires more than one petition to challenge the '806 patent. Accordingly, we decline to exercise our discretion to deny the instant Petitioner under § 314(a) on the basis of Petitioner's filing of multiple petitions.

III. CONCLUSION

Based on the arguments and evidence presented, we determine that Petitioner establishes a reasonable likelihood that it will prevail on at least one of its alternative arguments as to the unpatentability of claim 10 of the '806 patent. Accordingly, we institute an *inter partes* review of claim 10 on all arguments presented.

The factual findings set forth in this Decision, including any claim construction matters, are preliminary and provided for the sole purpose of deciding whether to institute a review. Any final findings will be based on the full trial record, including any information presented in a timely filed response to the Petition. *See Trivascular, Inc. v. Samuels*, 812 F.3d 1056, 1068 (Fed. Cir. 2016) (noting that "there is a significant difference between a petitioner's burden to establish a 'reasonable likelihood of success' at institution, and actually proving invalidity by a preponderance of the evidence at trial") (quoting 35 U.S.C. § 314(a); comparing *id*., with § 316(e)).

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that that that an *inter partes* review is instituted with respect to all of the arguments for the ground asserted in the Petition; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial, which shall commence on the entry date of this Decision.

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