

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner
v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner

Case No.: IPR2024-00909
U.S. Patent No. 10,658,378
Issue Date: May 19, 2020

Title: THROUGH ARRAY CONTACT (TAC) FOR
THREE-DIMENSIONAL MEMORY DEVICES

REPLY DECLARATION OF DR. JACK C. LEE

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I, Dr. Jack C. Lee, declare as follows:

I. INTRODUCTION

1. My name is Jack Lee. I have been retained on behalf of Micron Technology, Inc. (“Micron”) as an independent consultant in this proceeding before the United States Patent and Trademark Office (“USPTO”).

2. I have already submitted a declaration in this proceeding, which I understand to be Exhibit 1003. I refer to that declaration as my “Initial Declaration” and also cite simply as “Lee.” My Initial Declaration opined on claims 1-7 and 18 (“Challenged Claims”) of U.S. Pat. No. 10,658,378 (“the ’378 patent”).

3. A summary of my education, professional experience, and other qualifications is included within paragraphs 6-14 of my Initial Declaration, and in my CV (Exhibit 1004).

4. I have been asked to review the Patent Trial and Appeal Board’s Institution Decision (Paper 12) (“ID”), which instituted this IPR proceeding. I have also been asked to review the Patent Owner Response (“POR”) filed by Yangtze Memory Technology Co. Ltd. (“Patent Owner” or “YMTC”), and the accompanying exhibits and declarations, and provide my opinions on some of the statements and arguments offered in YMTC’s materials. My opinions and the bases for my opinions are set forth below.

5. I am being compensated for my time at my standard consulting rate of \$680 per hour. My compensation is based solely on the amount of time that I devote to activity related to this case and is no way contingent on the nature of my findings, the presentation of my findings and testimony, or the outcome of this or any proceeding. I have no other financial interest in this proceeding.

6. In this declaration, which I may refer to as my “Reply Declaration,” I do not address every argument or opinion that appears in YMTC’s Patent Owner Response or in Dr. Yang’s declaration (Exhibit 2005, “Yang Decl.”) with which I disagree. Instead, I focus on arguments and opinions that are most likely to be relevant to the outcome of this proceeding. For this reason, the opinions that are expressed in this Reply Declaration are not exhaustive of my opinions regarding the unpatentability of the Challenged Claims. My opinions should be understood to be from the perspective of a person of ordinary skill in the art (“POSITA”) as defined in my Initial Declaration.

II. MATERIALS CONSIDERED

7. In preparing this Reply Declaration, I reviewed and considered the following materials, along with any other materials referenced in the body of my Initial Declaration and this Reply Declaration:

Inter Partes Review of U.S. Patent No. 10,658,378
Reply Declaration of Dr. Jack C. Lee

Exhibit	Description
1001	U.S. Patent No. 10,658,378 to Tao et al.
1002	File History of U.S. Patent No. 10,658,378 to Tao et al.
1005	U.S. Patent Publ. No. 2017/0179026 A1 (“Toyama”)
1011	CN109075169A Office Action, dated November 14, 2019
1012	Certified Translation of CN109075169A Office Action, dated November 14, 2019
1013	CN109075169A Reexamination Decision, dated November 25, 2021
1014	Certified Translation of CN109075169A Reexamination Decision, dated November 25, 2021
1015	Micheloni, “3D Flash Memories” (2016)
1016	Aritome, “NAND Flash Memory Technologies” (2016)
1017	U.S. Patent No. 9,620,512 to Nishikawa et al.
1018	U.S. Patent Publ. No. 2016/0056188 A1 to Lee et al.
1019	U.S. Patent No. 9,293,348 to Lai et al.
1020	U.S. Patent No. 10,103,169 to Ge et al.
1021	U.S. Patent No. 8,697,519 to Jee et al.
1022	Excerpts from “Merriam-Webster’s Collegiate Dictionary,” Eleventh Edition (2014)
1038	Additional excerpts from “Merriam-Webster’s Collegiate Dictionary,” Eleventh Edition (2014)
1039	Decision Granting Institution of <i>Inter Partes</i> Review, in <i>Micron Technology, Inc. v. Yangtze Memory Technologies Company, Ltd.</i> Case No. IPR2024-00788, Paper 13 (“378-1 ID”)

Inter Partes Review of U.S. Patent No. 10,658,378
Reply Declaration of Dr. Jack C. Lee

Exhibit	Description
1040	Transcript of the deposition of Woodward Yang, dated April 22, 2025, in Case Nos. IPR2024-00788, -00909
1041	Woodward Yang, Deposition Exhibit 3, in Case Nos. IPR2024-00788, -00909
1042	Woodward Yang, Deposition Exhibit 4, in Case Nos. IPR2024-00788, -00909
1043	Woodward Yang, Deposition Exhibit 5, in Case Nos. IPR2024-00788, -00909
1044	Print out of https://boundarystones.org/
1045	Decision Granting Institution of <i>Inter Partes</i> Review, in <i>Micron Technology, Inc. v. Yangtze Memory Technologies Company, Ltd.</i> Case No. IPR2024-00911, Paper 12 (“806-2 ID”)
1046	Patent Owner’s Response in <i>Micron Technology, Inc. v. Yangtze Memory Technologies Company, Ltd.</i> Case No. IPR2024-00788, Paper 17 (“378-1 POR”)
1047	Declaration of Dr. Jack C. Lee in <i>Micron Technology, Inc. v. Yangtze Memory Technologies Company, Ltd.</i> Case No. IPR2024-00791, Ex. 1003 (“806-1 Lee Decl.”)

8. As stated above, I also reviewed and considered the Board’s Institution Decision (Paper 12), issued on January 7, 2025; YMTC’s Patent Owner Response (Paper 15), filed on April 2, 2025; and the exhibits that YMTC submitted with its Patent Owner Response, including Dr. Yang’s declaration (Ex. 2005).

III. UNDERSTANDING OF THE GOVERNING LAW

9. I am not an attorney but I have been instructed on and applied the law as described in my Initial Declaration.

IV. CLAIM CONSTRUCTION

A. “an isolation region of the substrate” (claim 1) and “a substrate with an isolation structure” (claim 15)

10. Claim 1 recites “an isolation region of the substrate.” Claim 15 recites “a substrate with an isolation structure.” I understand that YMTC and Dr. Yang contend that these terms should be construed as requiring that the isolation structure is “part of” the substrate. Yang Decl. ¶ 45. I disagree. The limitation encompasses an “isolation region” or “isolation structure” that serves to isolate the conductive elements within it from the “substrate” even if the “isolation structure” is not part of the “substrate.”

11. Merriam-Webster’s dictionary defines “with” as “used as a function word to indicate combination, accompaniment, presence, or addition.” Ex. 1038, 8 (Merriam-Webster’s definition of “with”). Merriam-Webster’s provides the examples of “heat milk *with* honey” and “went there *with* her.” That is the sense of “with” that a POSITA would have understood to have been used in the term “a substrate with an isolation structure.”

12. Merriam-Webster’s dictionary defines “of” as “used as a function word to indicate belonging or a possessive relationship.” Ex. 1038, 6 (Merriam-Webster’s definition of “of”). That is the sense of “of” that a POSITA would have understood to have been used in the term “an isolation region of the substrate.”

13. To a POSITA, the plain meaning of “with” would **not** have been synonymous with “part of.” A first object can be “with” a second object even if the second object is not part of the first. In the sentence “Alice went to school **with** Bob,” it would be nonsensical to interpret that to mean that Bob is **part of** Alice. An understanding of “substrate” in the semiconductor context, which I discuss below, makes this very clear.

14. A POSITA would not have seen anything in the intrinsic record suggesting that the ’378 patent intended to depart from the ordinary meaning of “with” and “of,” as YMTC’s construction would require. The patent repeatedly describes the substrate as distinct from—not part of—the isolation structure. Figures 2 and 13, for example, label the substrate and isolation structure using separate numbers; 202 and 233, respectively. And when the patent describes the relationship between these elements, it explains that “STI structure 233 is formed **on** a top portion of the substrate 202.” ’378 patent, 10:36-40, Figures 2, 13.

15. Indeed, POSITA would have understood that “STI structure 233” would typically be formed by starting with a substrate, removing a part of the

substrate to create an opening, and “fill[ing it] with a dielectric material, such as for example SiO₂”—exactly the same process that Toyama and Mushiga disclose. ’378 patent, 12:66-13:3.

16. The patent further discloses that “[i]n some embodiments a method for forming [a] 3D memory device includes forming an isolation structure **on** [the] substrate.” ’378 patent, 21:7-8. An “isolation structure” formed **on** a “substrate” is not **part of** the substrate just as a book placed **on** a table is not **part of** the table. Indeed, it makes little sense to argue the isolation structure must be part of the substrate, because the isolation structure and the substrate are formed of different materials. The isolation structure, because its purpose is to electrically isolate the conductive components, should be constructed of an insulating (e.g., dielectric) material. On the other hand, a substrate is typically made of a semiconducting material such as silicon. Indeed, the ’378 patent says that its substrate 202 is formed of a an “elementary semiconductor.” ’378 patent, 7:5-24.

17. I have reviewed the passages that YMTC and Dr. Yang cite but none of these passages support requiring the isolation structure to be part of the substrate. Yang Decl. ¶¶ 45-60. The specification uses the phrase “an isolation region **of** the substrate.” But an isolation region **of** a substrate need not be **part of** the substrate just as a pencil **of** the artist is not **part of** the artist. Although the specification at times describes a substrate that “includes” an isolation

structure, '378 patent, 12:64-66, that is best understood as indicating that the isolation structure is “between or within” parts of the substrate, not that the isolation structure is part of the substrate. Ex. 1038, 5 (Merriam-Webster’s definition of “include” as “to contain between or within”).

18. Moreover, there is nothing about the '378 patent’s purported invention that would suggest that the “isolation structure” must be part of the “substrate.” As I explained and YMTC does not dispute, the purpose of the isolation structure is to “electrically isolate[] conductors from each other and from electrical interference from the substrate.” Lee ¶ 130. Nothing about that purpose requires the isolation structure to be “part of” the substrate. On the contrary, an isolation structure can isolate conductors from each other and from electrical interference from the substrate even if the isolation structure is not part of the substrate. Indeed, the specification notes that “STI structure 233 is exemplary and is not limiting,” and that “other isolation structures can be used.” '378 patent, 10:33-35.

B. “through array contacts (TACs) extending vertically through the dielectric and the isolation structures” (Claim 15)

19. As I understand, YMTC argues that the claim requires that multiple “through array contacts” that extend through a single dielectric structure. I disagree. A POSITA would have understood that in claim 15 the “through array

contacts” may extend vertically through multiple dielectric structures. Moreover, a single “dielectric structure” may include multiple noncontiguous components.

20. As an initial matter, the claim phrase “the dielectric and the isolation structures” is plural, which expressly includes the possibility of there being multiple dielectric structures and/or multiple isolation structures. Indeed, the specification expressly discloses an embodiment in which each of the device’s dielectric structures includes only one TAC. A POSITA would have understood that such a device with multiple TACs would necessarily have multiple dielectric structures. ’378 patent, 21:7-25. YMTC’s construction would exclude this embodiment.

21. **Second**, there is nothing about the intrinsic record (e.g., the specification or the prosecution history) that suggests—let alone requires—that the phrase “a dielectric structure” must exclude multiple dielectric structures.

22. The specification expressly provides that “terms, such as ‘a,’ ‘an,’ or ‘the,’ ... may be understood to convey a singular usage or to convey a plural usage, depending at least in part upon context.” ’378 patent, 4:17-19. A POSITA would have understood this passage to define “a” in such a way as to include plurals, reinforcing what I understand to be the general rule of patent law that “a” means “one or more.”

23. There is nothing about the context of the “dielectric structure” in the ’378 patent that would require multiple TACs extend through a single dielectric structure. As I explained in my Initial Declaration, the purpose of the dielectric structure is to electrically isolate the through array contacts from each other and the alternating conductor/dielectric layer stack, through which the through array contacts extend. That purpose can be served by a unitary block of material (as disclosed expressly in the ’378 patent), and can also be served by multiple noncontiguous liners, each electrically isolating one through array contact.

24. Indeed, as explained above, a POSITA would have understood the ’378 patent to contemplate embodiments with multiple dielectric structures (each of which includes a single TAC). ’378 patent, 21:7-25.

25. I understand that Dr. Yang and YMTC contend that using a unitary block as a dielectric structure offers some cost savings. Yang Decl. ¶ 131. (citing ’378 patent, 10:59-66). Dr. Yang, however, seems to ignore that this would require more oxide (versus individual liners) and the duration of the deposition to create such a large oxide block. Dr. Yang also ignores the benefit of leaving more of the gate layers (via the individual thin liners). But, even accepting that asserted cost savings as true, a POSITA would have recognized that dielectric liners, like a unitary dielectric block, are an acceptable and desirable way to insulate through array contacts. Ex. 1047, (IPR2024-00791, Exhibit 1003) (“806-1 Lee Decl.”)

¶¶ 180-197. Indeed, the '378 patent itself uses dielectric liners to insulate its slit structures (e.g., slit structures 226 are insulated with dielectric layer 1008). '378 patent, 16:63-66.

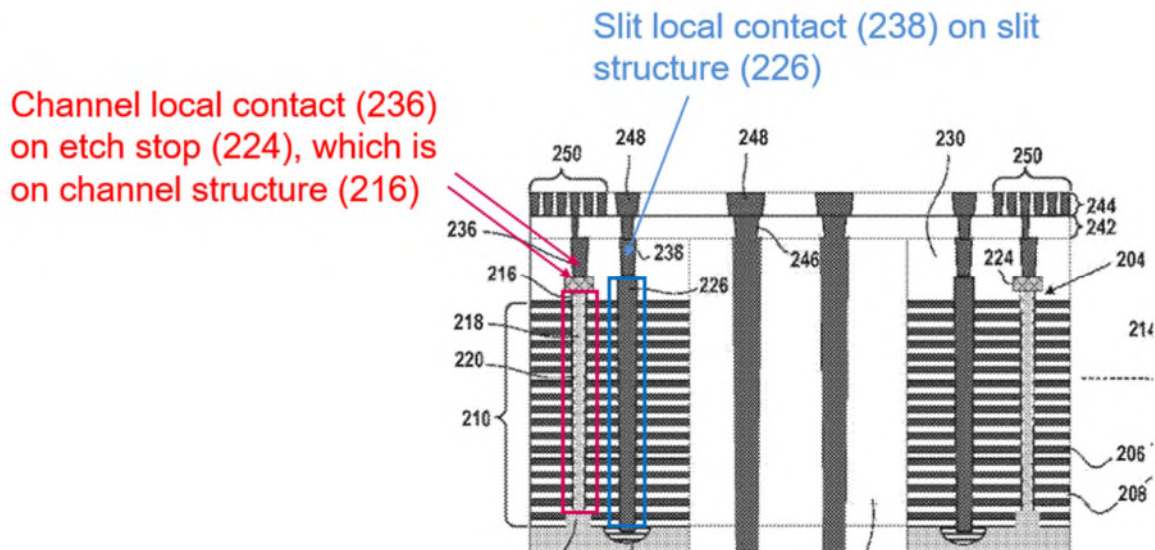
26. A POSITA would not interpret the phrase “the dielectric structure” as requiring a single, monolithic dielectric block. In my experience, it is common for a structure to be referred to functionally or collectively even if it includes multiple components or substructures, particularly when they work together to perform a shared role such as electrical isolation.

C. “an etch stop plug interposed between each local contact of the local contacts, and each channel structure of the channel structures” (claim 18)

27. As I understand, Micron and YMTC’s dispute with respect to this limitation is whether the term “each local contact” refers to local contacts on the channel structures (Micron’s position) or refers to local contacts on the channel structures **and** on the slit structures (YMTC’s position). I agree with Micron’s position. A POSITA reading the limitation in the context of the claim as a whole and the specification would have understood that the claim requires etch stop plugs between channel structures and the channel structure local contacts, and does not require etch stop plugs between channel structures and slit structure local contacts.

28. Before discussing the claim construction issue, I place the relevant claim terms in context. As shown below, the '378 patent discloses local contacts

(236) for channel structures (216) and local contacts (238) for the slit structures (226). There are etch stops (224) only between the channel local contacts and the channel structures.



'378 patent, Figure 2 (partial), 11:24-26 ("As shown in FIG. 2, local contacts can include NAND string contacts 236, slit structure contacts 238, and WL contacts 240."), 9:31-35 ("In some embodiments, each NAND string 204 includes an epitaxial layer 222 and an etch stop plug 224 at the respective bottom and top of NAND string 204, as shown in FIG. 2.").

29. Notably, the '378 patent never discloses an etch stop on the slit structures. In fact, the Patent distinguishes the channels that have etch stops and slit structures that do not. '378 patent, 11:37-40 (local contacts connecting to channel etch stops and connecting directly to slits), 2:35-51 (only channels have etch stops), 9:31-48 (same), 15:57-16:11 (same), 17:48-57 (same). This is unsurprising,

because the '378 patent defines the function of the “etch stop plug” as protecting the channel and serving as the channel’s drain: “As the name suggests, etch stop plug 224 is an etch stop layer that prevents etching of dielectrics in channel structure 216, such as SiO₂ and SiN, during subsequent etch operations. In some embodiments, etch stop plug 224 acts as the drain of NAND string 204.” *Id.*, 9:40-54.

30. YMTC’s construction, which would require “etch stop plugs” between slit structure local contacts (“local contacts disposed on ... the slit structures”) and the “channel structures” is contrary to a POSITA’s understanding.

31. **First**, not a single embodiment of the '378 patent meets YMTC’s construction. The '378 patent repeatedly, consistently, and exclusively describes “NAND string contacts” (236) as the “local contacts” for the “channel structures” (216),¹ and “slit structure contacts” (238) as the “local contacts” for the “slit

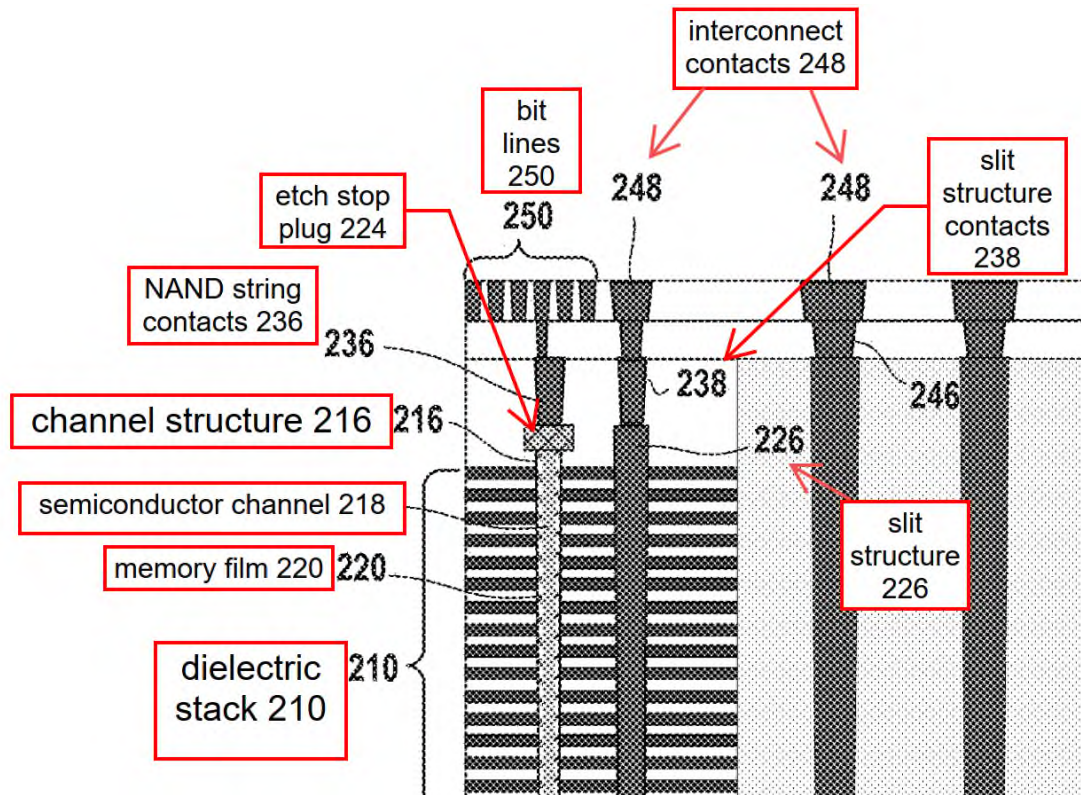
¹ More specifically, the “lower end of NAND string contacts 236” is described as “in contact with the etch stop plug 224 of NAND string 204.” Each “NAND string 204” includes an “etch stop plug 224,” a “channel structure 216,” and potentially an “epitaxial layer 222.” '378, Figure 2, 9:1-3, 9:31-37. Thus, a POSITA would have recognized that “NAND string contacts” (236) are the local contacts for the “channel structures” (216).

structures” (226). ’378 patent, 11:24-26, 11:35-40. The ’378 patent’s “etch stop plugs” (224) are **always** described as being between the channel structure local contacts (236) and the channel structures (216). ’378 patent, 11:37-39. Indeed, the point of an “etch stop” is to protect **channel** structures; I agree with Dr. Yang that an etch stop plug on a **slit** structure is unnecessary because “the material composition of [slit structure] 226 in and of itself can actually stop the etch that’s required for the formation of [slit structure contacts] 238.” Ex. 1040 (4/22/25 Yang Dep.) 121:14-16; ’378 patent, 9:44-46. And the ’378 patent **never** identifies any “etch stop plugs” that are interposed between slit structure local contacts (238) and channel structures (216). YMTC’s construction, therefore, cannot be correct.

32. **Second**, YMTC’s assertion that there is ’378 patent embodiment meeting its construction is incorrect. YMTC’s argument is premised on its nonsensical assertion that “bit lines 250” are “local contacts disposed on ... the slit structures.” POR 31-34.

33. As an initial matter, “bit lines 250” are not “local” contacts. Consistent with a POSITA’s general understanding, the ’378 patent explains that “local contacts” are “in physical and electrical contact with the various memory array structures disclosed herein, such as ... slit structures 226.” ’378 patent, 11:16-20. Thus, “the lower end of slit structure contact[s] 238 [*i.e.*, the slit structure local contacts] can be in contact with the upper end of slit structure[s]

226.” ’378 patent, 11:35-40. As Figure 2 shows, “bit lines 250,” in contrast, are not in **physical** contact with “slit structures 226”:



’378 patent, Figure 2 (cropped, annotated). Nor are “bit lines 250” in **electrical** contact with slit structures 226; instead, they are in (indirect) electrical contact with channel structure 216. ’378 patent, 12:4-7. That “bit lines 250” are not “local” contacts is confirmed by the ’378 patent’s description of them as “interconnect contacts.” ’378 patent, 12:4-7. The patent describes “local contacts” as distinct from “interconnect contacts.” ’378 patent, 11:56-59. Indeed, bit lines are the very opposite of local to the slit structures: they are “in the top interconnect layer.” ’378 patent, 5:40-45.

34. My deposition testimony is consistent with this understanding. I was asked: “And what is the function of the local contact recited in line 15 of the '378 patent?” Ex. 2007, 66:1-3. I answered: “So in column 11 line 15, around 15, it says that local contact is essentially provide a conducting layer with memory array structures, such as the NAND string 204, S-T-R-I-N-G-S, 204, slit structures 226, conductive layer or word line 206, and the staircase structure 212. So the local contact basically is an interconnect to connect the memory array structure to, for example, external -- external input, outputs.” *Id.*, 66:4-14

35. I was not asked for, nor did not I provide, a definition of the term “local contact.” And I did not state that every component electrically connected to a “memory array structure,” no matter how indirectly connected, is a local contact. On the contrary, the '378 patent itself defines “local” contacts in relevant part as contacts that are “in direct contact with the memory array structures.” '378 patent, 11:20-24.

36. **Third**, the plain claim language undermines PO’s interpretation. Independent claim 15 requires two sets of local contacts: (1) local contacts on channel structures, and (2) local contacts on slit structures. Dependent claim 18 then recites that there is “an etch stop plug interposed between each local contact of the local contacts and each channel structure.” Plainly, dependent claim 18 refers to the local contacts on the channel structures, not those on the slit

structures, because it positions the etch stop above the channel structure and beneath the local contact (by its use of “interposed between”). A POSITA would not have read the limitation at issue divorced from the rest of the claim and the specification, as YMTC seems to suggest.

V. GROUND 1: TOYAMA RENDERS THE CHALLENGED CLAIMS OBVIOUS

A. Limitations [1.C.ii] and [15.A]: “an isolation region of the substrate” and “a substrate with an isolation structure”

1. Under Micron’s Construction, Toyama Renders Limitations [1.C.ii] and [15.A] Obvious

37. As mentioned above, it is my understanding that YMTC proposes a claim construction that improperly requires that the *isolation structure*² must be “part of” the *substrate*.³ For the reasons explained above, that interpretation is incorrect. Section IV.A. Under the correct interpretation, the *isolation structure* need not be *part of* the *substrate*. Accordingly, both Toyama’s first exemplary structure and Second Modification disclose *an isolation region of the substrate*

² YMTC separately argues that Toyama’s first exemplary structure does not disclose *a dielectric structure on the isolation structure*. I address this argument in my discussion of limitations [1.C.i-ii] and [15.C.i].

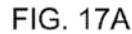
³ I have rendered the claim language in italics and red.

([1.C.ii]), and a *substrate with an isolation structure* ([15.A]), as explained in detail in my Initial Declaration. Lee ¶¶ 119-123, 200-212.

**2. Limitations [1.C.ii] and [15.A] Would Have Been Obvious
Even Under YMTC’s Erroneous Construction**

38. Even if one were to accept YMTC’s erroneous position that the *isolation structure* must be “part of” the *substrate*, Toyama’s first exemplary structure and Second Modification each disclose the limitation. That is because the structural relationship between the isolation structure and the substrate in those embodiments is materially the same as in the ’378 patent. In other words, if YMTC’s logic were to be applied consistently, the same reasoning that would require the ’378 patent’s isolation structure to be part of its substrate would likewise require Toyama’s isolation structures to be considered part of its substrate.

39. The ’378 patent defines “substrate” as “a material onto which subsequent material layers are added, or otherwise ‘disposed.’” ’378 patent, 4:41-43. YMTC apparently contends that the combination of “STI structure 233” and “substrate 202” in the ’378 patent meet this definition. But, if that interpretation were correct, then by the same logic, Toyama’s first exemplary structure’s “planar semiconductor material layer 10” together with the lower part of “dielectric fill material portion 430” would likewise collectively qualify as a *substrate*:



Micron Ex. 1037, p. 23
Micron v. YMTC
IPR2025-00909

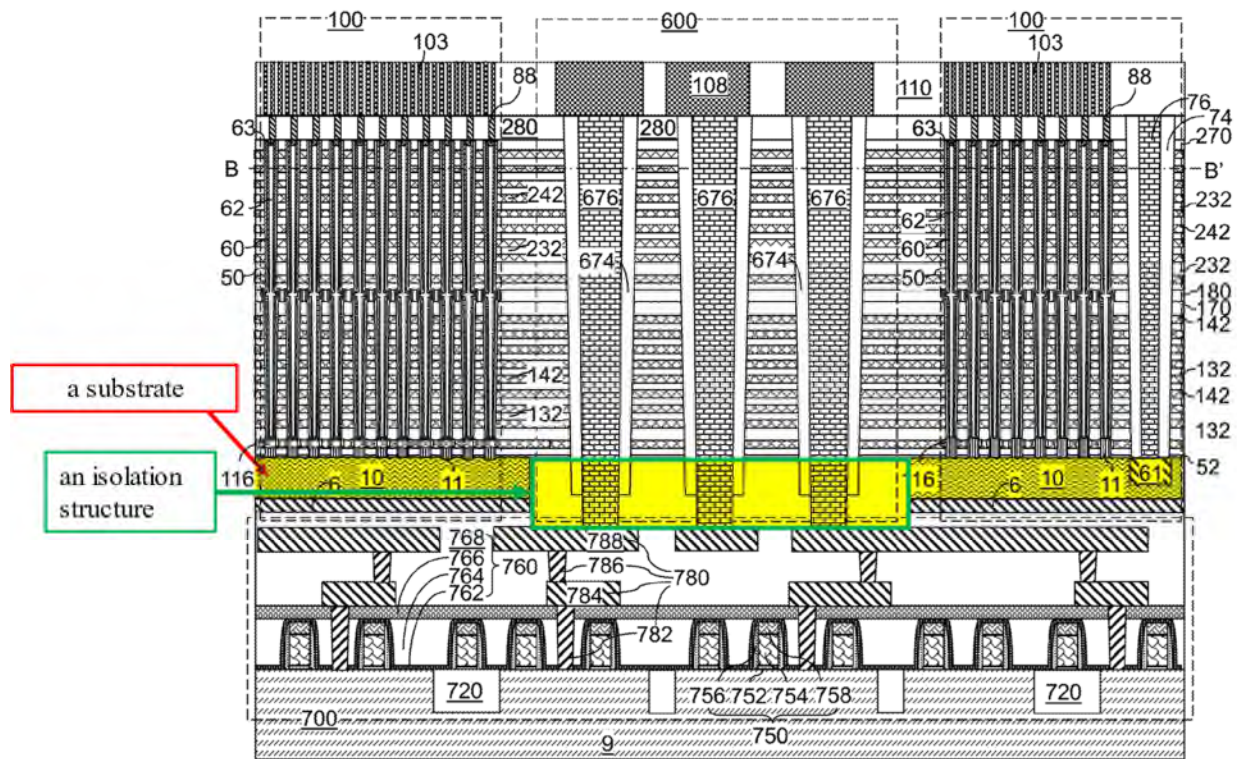


FIG. 49

Toyama, Figure 49 (annotated). Under this mapping, the *isolation structure* in both Toyama's first exemplary structure and its Second Modification is *part of* the *substrate*. Lee ¶¶ 119-123, 200-212. As the Board observed in a related proceeding, "Toyama's dielectric-filled substrate cavity and the dielectric-filled structure of [the] Figure 2 of the '378 patent have the same structure except that Toyama's dielectric extends completely through the substrate whereas the dielectric of the '378 patent extends only partway through the substrate." ID 15. However, "this distinction is not determinative because the claim," even under

YMTC's interpretation, "does not restrict the region from extending through the substrate." *Id.*

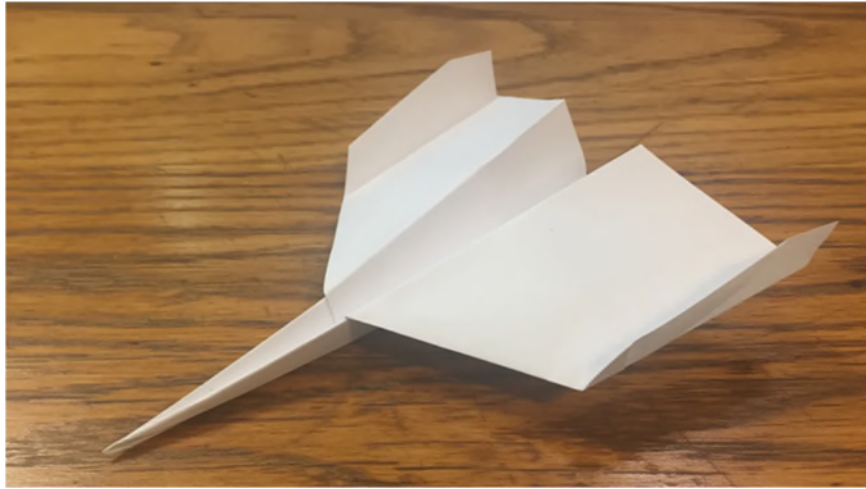
B. Limitations [1.C.i-ii] and [15.C.i]: "a dielectric structure on an isolation region" and "a dielectric structure on the isolation structure"

1. First Exemplary Structure

a. A POSITA Would Have Understood That The "Dielectric Structure" And The "Isolation Structure" Need Not Be Separately Formed

40. I understand that YMTC contends that the term "a dielectric structure on the isolation structure" requires separate depositions for the isolation structure and the dielectric structure thereon. I disagree. A POSITA would have understood that the *dielectric structure* and the *isolation structure* may be formed simultaneously from a unitary material, or each structure may be composed of multiple components.

41. Indeed, to a POSITA, the plain meaning of "structure" allows a unitary material to include multiple structures, just as the below paper airplane folded from a single piece of paper could be said to include a "nose structure," a "wing structure," and a "wing tip" structure, each with its own function.



Ex. 1041 (4/22/25 Yang Dep., Ex. 3), 7.

42. A POSITA's ordinary understanding of the word "structure" as encompassing a part of a would be bolstered by the '378 patent's disclosure. Indeed, the '378 patent admits that its own boundaries are "arbitrarily defined." The specification explains:

The boundaries of these functional building blocks have been arbitrarily defined herein for the convenience of the description. Alternate boundaries can be defined so long as the specified functions and relationships thereof are appropriately performed.

'378 patent, 22:65-23:5. So long as different parts of a unitary material perform components' respective functions, the specification contemplates that "alternate boundaries can be defined."

43. The specification provides several other disclosures that support the dielectric and isolation structures being parts of a unitary material. **First**, the '378 patent indicates that both the dielectric structure and the isolation structure may be

formed of the same material, such as SiO₂. '378 patent, 10:37-40, 10:46-47. Thus, the specification contemplates that the dielectric and isolation structures could be different parts of a single crystal of SiO₂.

44. **Second**, the '378 patent indicates that the dielectric structure may be “aligned to” and “in contact with” the isolation structure, such that the structures form “a single column, of the same material.” '378 patent, 10:30-36. As a POSITA would have understood, there is little if any functional or structural difference between a “single column, of the same material” formed using successive steps (which YMTC seems to agree is encompassed by the claim), and a single column of the same material formed together using a single deposition. ID 18.

45. **Third**, the '378 specification describes that the dielectric structure and a top portion of the isolation structure may be formed in the same deposition step. That is because the specification discloses that “[i]n some embodiments, opening 600 may extend partially into STI structure 233.” '378 patent, 15:16-18. “In other words, the etch process used to form opening 600 may also remove (recess) [a] portion of the top surface of STI structure 233.” '378 patent, 15:18-20. A POSITA would have understood this disclosure to reflect the patent’s indifference to the exact boundary between the structures.

46. **Fourth**, the '378 patent does not indicate—nor would a POSITA understand—any purpose served by the dielectric and isolation structures being formed in separate steps that would not be equally served by these structures being formed at the same time, such that the dielectric and isolation structures were different parts of a unitary dielectric material.

**b. If Under Micron's Construction, Limitations
[1.C.i-ii] and [15.C.i] Would Have Been Obvious**

47. As I understand, YMTC's argument regarding this limitation relies on its claim construction position that different parts of a unitary material cannot satisfy the roles of both *dielectric structure* and the *isolation structure*. POR 23. But, as explained above, the specification imposes no such restriction. Section V.B.1.a. As I explained, and the PTAB agreed, "dielectric fill material portion 430 performs the isolation functions common to both the isolation structure and the dielectric structure." ID 19; Lee ¶¶ 128, 130 (explaining how different parts of "dielectric fill material portion 430" perform the functions of the *dielectric structure* and the *isolation structure*). It is therefore undisputed that, under Micron's construction, Toyama's first exemplary structure discloses *a dielectric structure* (upper part of "dielectric fill material portion 430") *on the isolation region/structure* (lower part of "dielectric fill material portion 430").

**c. Limitations [1.C.i-ii] and [15.C.i] Would Have
Been Obvious Even under YMTC’s Erroneous
Construction**

48. Even under YMTC’s (incorrect) construction, which requires the *dielectric structure* to be formed separately from the *isolation structure*, Toyama nevertheless renders the limitation obvious.

49. As I explained in my Initial Declaration, “forming the *isolation structure* and the *dielectric structure* separately would be no more than the mere substitution of a known process ... for another process ... to obtain predictable results.” Lee ¶ 229.

50. Contrary to YMTC’s apparent arguments (POR 54), I did identify a clear motivation to combine: “electrically isolat[ing] the conductors embedded within” the isolation structure. Pet. 54; Lee ¶ 229.

51. YMTC contends that the proposed modification changes First Exemplary Structure’s processing steps. However, I explained that a POSITA would have understood how to make such substitution because “using isolation structures on a substrate to electrically isolate components was well-known and commonplace prior to the effective filing date of the ’378 patent priority date.” Lee ¶ 229; ID 20 (crediting my testimony).

2. Second Modification

52. YMTC's argument regarding limitation [15.C.i] must fail because it is based solely on YMTC's earlier argument that the Second Modification does not render limitation [15.A] obvious. That argument fails for reasons explained in Section V.A (limitation [15.A]).

C. Limitations [1.D] and [15.H]: "one or more through array contacts (TACs) extending vertically through the dielectric structure and the isolation region" and "through array if contacts (TACs) extending vertically through the dielectric and the isolation structures"

1. Second Modification

a. Under Micron's Construction Limitation [15.H] Would Have Been Obvious

53. YMTC argues that this limitation requires multiple *through array contacts* to extend through a singular *dielectric structure*. For the reasons discussed in Section IV.B, I disagree. If limitation [15.H] is properly construed to allow the *through array contacts* to extend through multiple *dielectric structures* (as the limitation should be interpreted), then Toyama's Second Modification discloses this limitation, as explained in my Initial Declaration. Lee ¶¶ 257-259.

b. Limitation [15.H] Would Have Been Obvious Even under YMTC's Construction

54. Even accepting YMTC's incorrect construction that multiple *through array contacts* must extend through a "single" *dielectric structure*, Toyama's

Second Modification renders limitation [15.H] obvious. As I explained in my Initial Declaration, the “insulating liners 674” in Toyama function together and are collectively understood by a POSITA to form a single *dielectric structure*.⁴ Lee ¶¶ 118, 124.

55. Importantly, the term “structure” does not require all its elements to be contiguous. For example, Merriam-Webster’s defines a structure as “something arranged in a definite pattern of organization.” Ex. 1022, 5.⁵ Consistently with that definition, as YMTC’s own expert agreed, a structure such as the wall (pictured below) can consist of spaced-apart elements, i.e. its components are not all touching each other, and still be considered a structure:

⁴ My position here is consistent with my position that each of the “insulating liners 674” qualifies individually as a dielectric structure because, as Dr. Yang acknowledged when he stated that, “a structure ... can be composed of other structures.” Ex. 1040, 43:23-44:3.

⁵ Although my Initial Declaration focused on a different Merriam-Webster definition -- “something (as a building) that is constructed” -- I now reference an additional definition, as it has become apparent from the parties’ arguments that the original definition alone does not fully resolve the dispute.

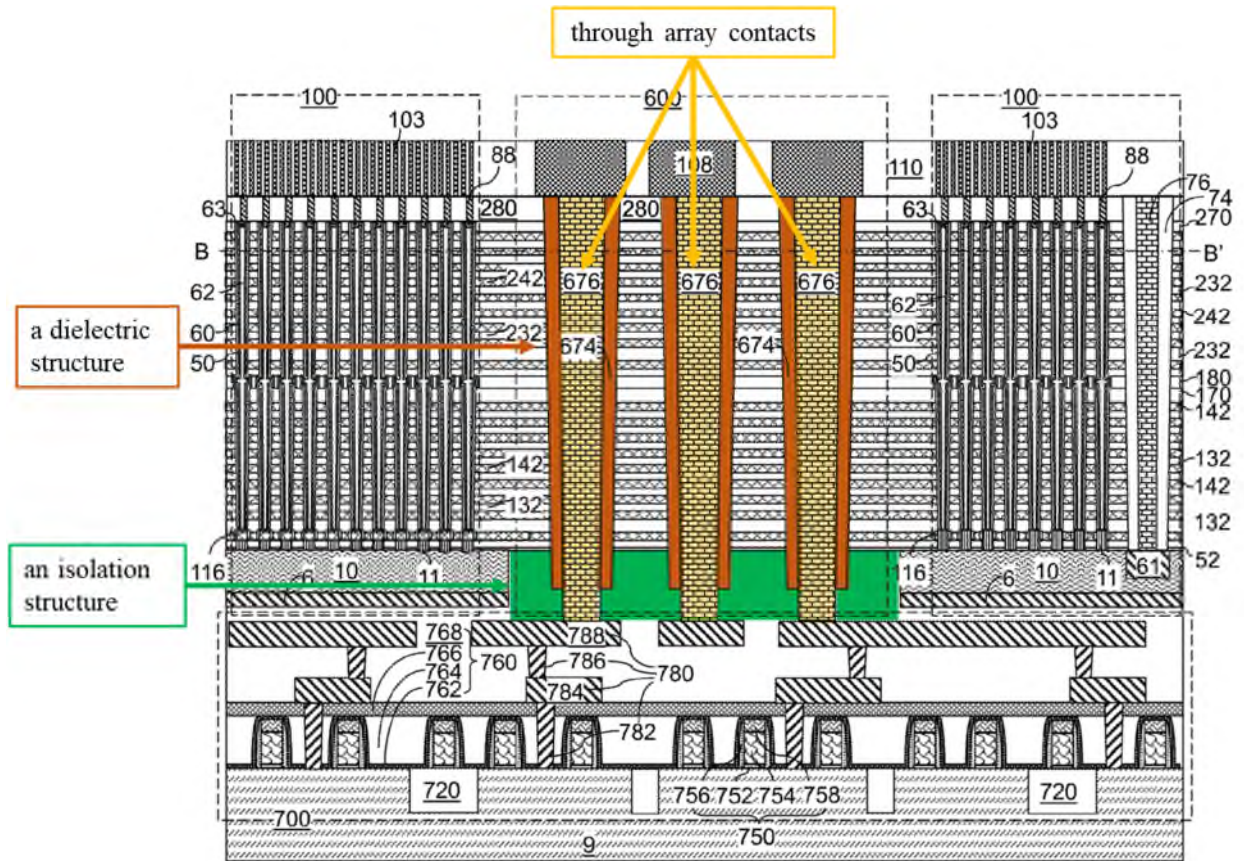


Ex. 1042 (4/22/25 Yang Dep., Ex. 4); Ex. 1040, 45:3-4, 47:3-6 (identifying the “wooden posts” as a “wall structure”). Similarly, the staircase below is considered a structure even though the stairs do not contact each other:



Ex. 1043 (4/22/25 Yang Dep., Ex. 5). I understand Dr. Yang’s position is that there may be anchors embedded within the wall that are also form part of the staircase structure. But the point remains, even if those anchoring structures did not touch each other, this would still be a staircase **structure**. The definition of a structure focuses on functional arrangement, not physical continuity. In other words, a POSITA would understand that what qualifies something as a “structure” is not necessarily physical continuity, but rather functional arrangement and organization toward a common purpose—just as the steps collectively enable vertical movement despite being spaced apart.

56. As explained in my Initial Declaration, a POSITA would have understood the “insulating liners 674” in Toyama’s Second Modification to be both individually ***and collectively*** a dielectric structure:



Toyama, Figure 49 (annotated); Lee ¶¶ 115-123. Like the wall posts and staircase steps discussed above, each of “insulating liners 674” is arranged and organized in a definite and purposeful pattern. Importantly, all the liners perform the same function: insulating the **TACs** as they pass through the **alternating ... layer stack**. Lee ¶ 118. Thus, a POSITA would have understood that the “insulating liners

674” are collectively a (single) *dielectric structure* even though they may be physically separated.

c. YMTC Has Not Rebutted Micron’s Showing For Limitation [1.D]

57. In my opinion, for limitation [1.D] for the same reasons as discussed above: (1) the term “the dielectric structure” may encompass one or more dielectric structures (Sections IV.B, V.C.1.a); and (2) multiple “liners 674” are collectively a single dielectric structure (Section V.C.1.b). And, even under PO’s position that a single “liner 674” is a dielectric structure, the plain language of limitation [1.D] encompasses *one* or more *through array contacts* (one “structure 676”) *extending vertically through the dielectric structure* (one “liner 674”).

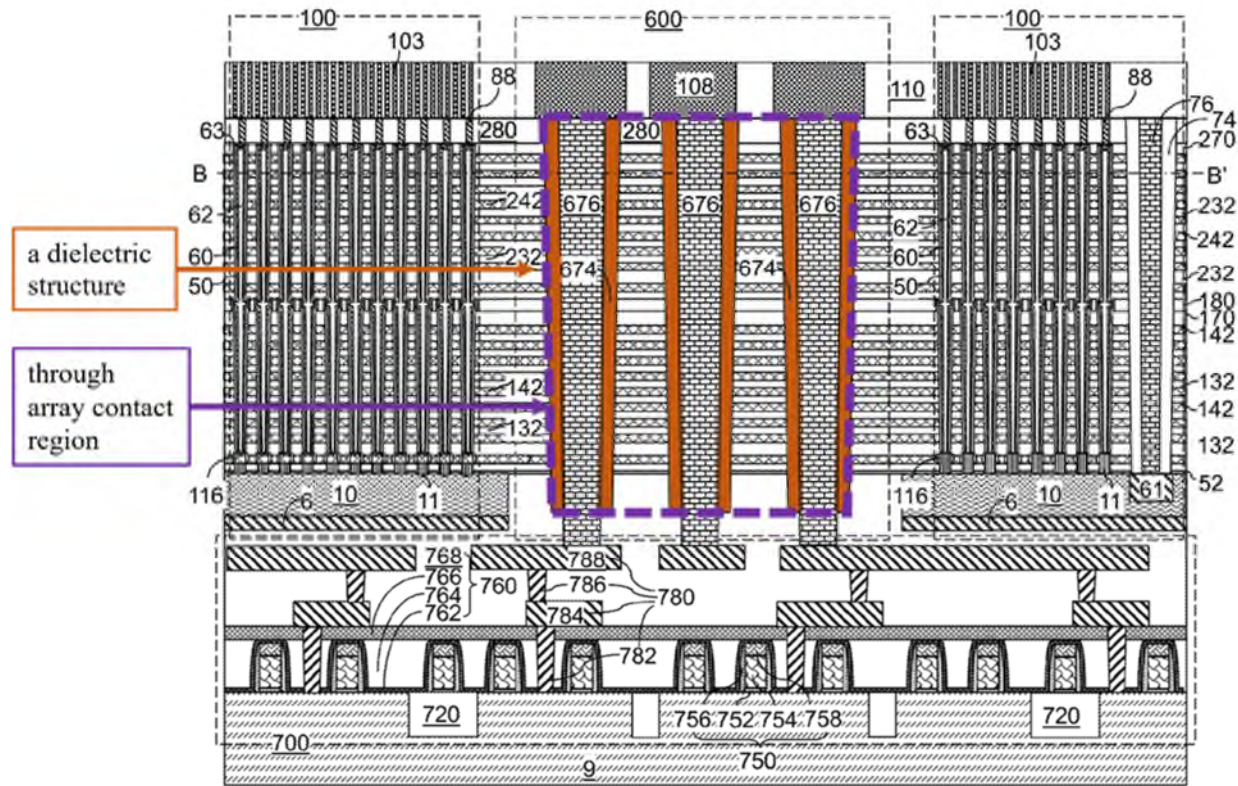
2. First Exemplary Structure

58. I understand YMTC’s argument regarding limitation [15.H] to merely reiterate its earlier arguments that Toyama’s first exemplary structure does not render limitations [15.A] and [15.C.i] obvious. However, as explained in Sections V.A (limitation [15.A]), V.B (limitation [15.C.i]), those arguments are incorrect for the reasons. Accordingly, YMTC’s argument regarding limitation [15.H] fails for the same reasons.

D. Claim 7: “wherein the dielectric structure defines a through array contact region within the 3D memory device”

1. Second Modification

59. As I understand, YMTC argues that the Second Modification’s *dielectric structure* does not *define[]* the *TAC region* that I identified in my original declaration (reproduced below):



Toyama, Figure 49 (annotated); Lee ¶¶ 195-197; POR 69-71. I disagree. The borders of the identified *TAC region* correspond to the borders of the Second

Modification's *dielectric structure*, namely, the “insulating liners 674”.⁶ This is also evident from a top-down view:

⁶ Either the TAC region's borders are defined by a single dielectric structure that encompassing all of the “insulating liners 674” (*see* Section V.C.1.b, addressing how Toyama's Second Modification satisfies limitation [15.C.i] under YMTC's construction,) or the TAC region's borders are defined by a collection of dielectric structures, each comprising an individual “liner 674” (*see* Section V.C.1.a discussing how Toyama's Second Modification satisfies the proper construed limitation [15.C.i]).

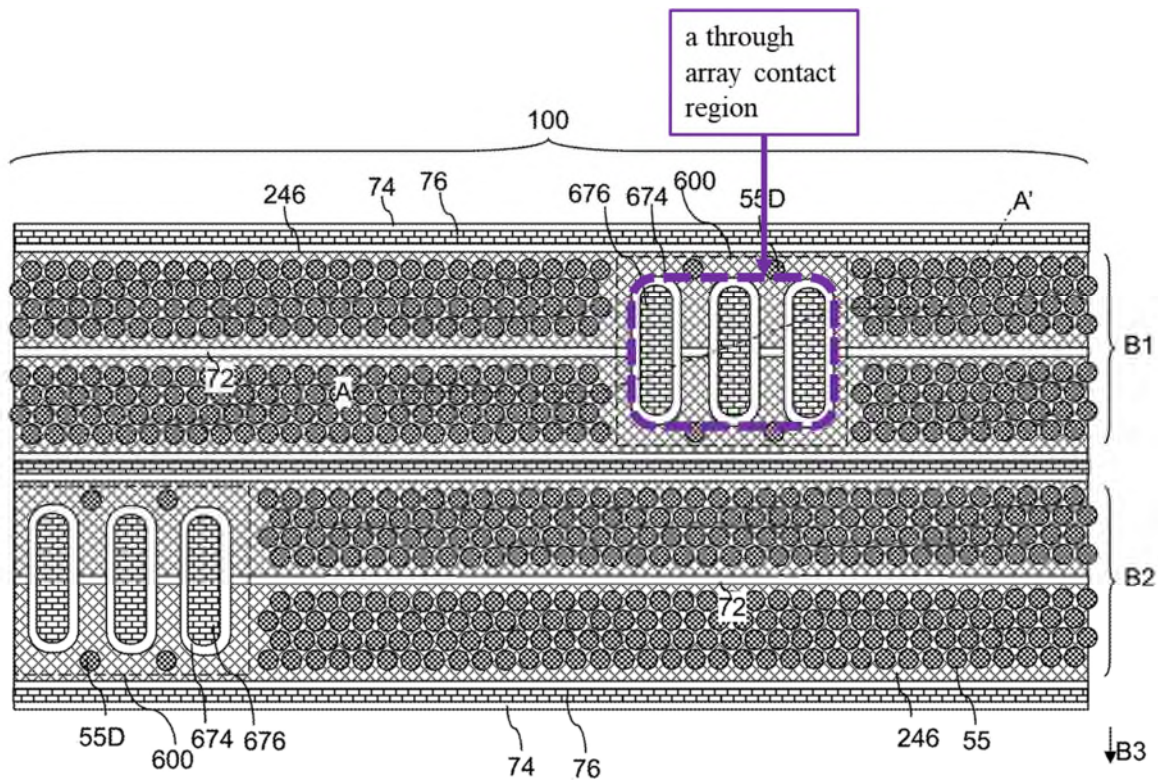


FIG. 48B

Toyama, Figure 48B (annotated).

60. YMTC in effect asserts that the *TAC region* must be “coextensive” with the *dielectric structure*. Ex. 1046, (Patent Owner’s Response, IPR2024-00788, Paper 17) (“378-1 POR”) at 27-28. But that is inconsistent with the plain meaning of claim 7, which requires only that the TAC region be “within or defined by” the dielectric structure. The plain meaning of “define” includes “to fix or mark the limits of.” Ex. 1038, 3 (Merriam-Webster’s definition of “define”). For example, the original borders of Washington, DC were “defined” by a number of “boundary stones” placed by surveyors, but clearly the District of Columbia

encompassed far more than just those stones and was not **coextensive** with the small footprint of the stones themselves. Ex. 1044 (<https://boundarystones.org/>).

Similarly, a POSITA would have understood that the dielectric structure may define the limits of a TAC region without being coextensive with it. In other words, the **TAC region** may be defined by the **dielectric structure** even if the **TAC region** does not share the exact same spatial scope as the **dielectric structure**.

61. YMTC’s assertion that the **TAC region** “cannot include the alternating conductor/dielectric layer stack” is inconsistent with the plain meaning of claim 7 for the same reason. Just as Washington, DC can include more than stones that define its border, a **TAC region**, even under YMTC’s construction, may include additional elements (e.g., an alternating conductor/dielectric stack) beyond the **dielectric structure** that defines it.

62. YMTC’s implicit construction is also contrary to the ’378 patent’s specification. The specification repeatedly and consistently uses the formulation “[component] region” to describe an area that includes more than just that component. For example, the patent’s “NAND string region 110” includes “NAND strings 112,” “slit structures 114,” and may also include “dummy channel structures 122.” ’378 patent, Figure 1B; *see also* Ex. 1040 (4/22/25 Yang Dep.) 69:16-20 (agreeing that NAND string region 110 includes more than just NAND strings). Indeed, Dr. Yang agreed that “NAND string region 110” in the ’378

patent's final device includes an alternating conductor/dielectric layer stack. Ex. 1040, 69:11-13. Similarly, "staircase regions 130" includes not just "TSG contacts 132," but also "slit structures 114." '378 patent, Figure 1A. Thus, although a POSITA would have understood that a region that is called a "[component] region" includes that component, the region does not necessarily exclude every other component.

63. The specification's use of the phrase "TAC region" confirms that it is not intended to exclude other components. The specification's first use of the term is with reference to "an exemplary TAC region 102 of the 3D memory device." '378 patent, 5:63-65. As illustrated below, "TAC region 102 includes NAND string regions 110, a TAC region 120, and top selective gate (TSG) staircase regions 130," each of which includes multiple elements. '378 patent, 5:65-6:5.

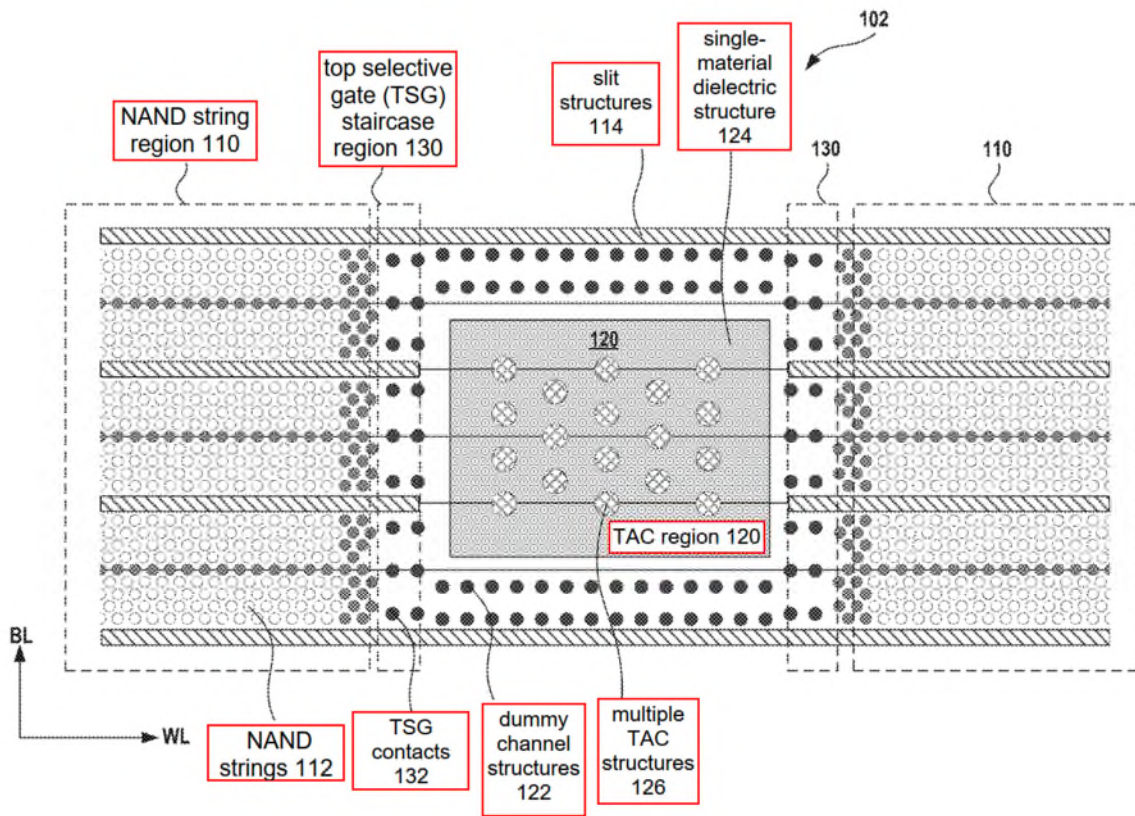


FIG. 1A

'378 patent, Figure 1A (annotated). Thus, a "TAC region" includes elements other than a "dielectric structure" (124) and TACs (126). Indeed, a TAC region (102) can include **another** TAC region (120). And a "TAC region" can include "NAND string region 110." As Figure 2 shows, and as both Dr. Yang and I agree, the "NAND string region 110" includes an alternating conductor/dielectric layer stack. Ex. 1040, 69:11-13. Figures 1B-C disclose TAC regions 104 and 106, which also include other elements such as an alternating conductor/dielectric layer stack. A POSITA would have known that TAC regions 104 and 106 include an alternating conductor/dielectric layer stack because those regions include NAND strings 112,

and a POSITA would have known that for NAND strings 112 to be functional, they must be formed within an alternating conductor/dielectric layer stack.

64. The '378 patent does not include any lexicography or disclaimer that would limit the meaning of the phrase “through array contact region.” I understand that YMTC has pointed to certain passages that it contends narrow the plain meaning of “through array contact region.” But a POSITA would have understood these passages to be non-limiting, for example, “TAC region 120 **can be** defined by a ... dielectric structure” and “[i]n **some embodiments**, dielectric structure 232 defines the boundaries ... of TAC region 120”. 378-1 POR 28-29 (emphasis added). The specification, therefore, contradicts and undercuts YMTC’s assertions that “in all [of the specification’s embodiments] the TAC region is within or defined by the dielectric structure,” and that a TAC region “ does not include the alternating conductor/dielectric layer stack.” POR 70.

2. First Exemplary Structure

65. YMTC’s argument regarding claim 7 is based solely on YMTC’s earlier argument that Toyama’s first exemplary structure does not disclose a dielectric structure. POR 55. For the reasons explained above, that argument is incorrect. Section V.B (limitation [15.C.i]).

E. Limitation [18.A]: “an etch stop plug interposed between each local contact of the local contacts and each channel structure of the channel structures”

1. Under Micron’s Construction, Limitation [18.A] Would Have Been Obvious

66. YMTC argues that limitation [18.A] requires an *etch stop plug* interposed between each slit structure local contacts (that is, the *local contacts disposed on ... the slit structures*) and the *channel structures*. For the reasons explained above (Section IV.C), I disagree. If limitation [18.A] is understood to only require etch stop plugs between the channel structure local contacts (that is, the *local contacts disposed on the channel structures*) and the channel structures, then Toyama renders limitation [18.A] obvious for the reasons explained in my initial declaration. Lee ¶¶ 263-266.

2. Toyama Discloses Limitation [18.A] Even Under YMTC’s Construction

67. Toyama’s First Exemplary Structure and Second Modification render the claim 18 obvious even accepting PO’s construction. That is because Toyama discloses the claim in exactly the same way that, under PO’s erroneous theory, the ’378 discloses it. In other words, the faulty logic underlying YMTC’s proposed construction would similarly require concluding that Toyama discloses

68. PO asserts (POR 31-32) that the ’378’s “bit lines 250” are *local contacts disposed on the channel structures and the slit structures* (limitation

[15.G]), such that the '378 discloses *an etch stop plug* (“etch stop plug 224”) *interposed between each local contact of the local contacts* (“bit lines 250”) *and each channel structure of the channel structures* (“channel structure 216”). POR 31-32. PO annotates Figure 1A with its apparent theory:

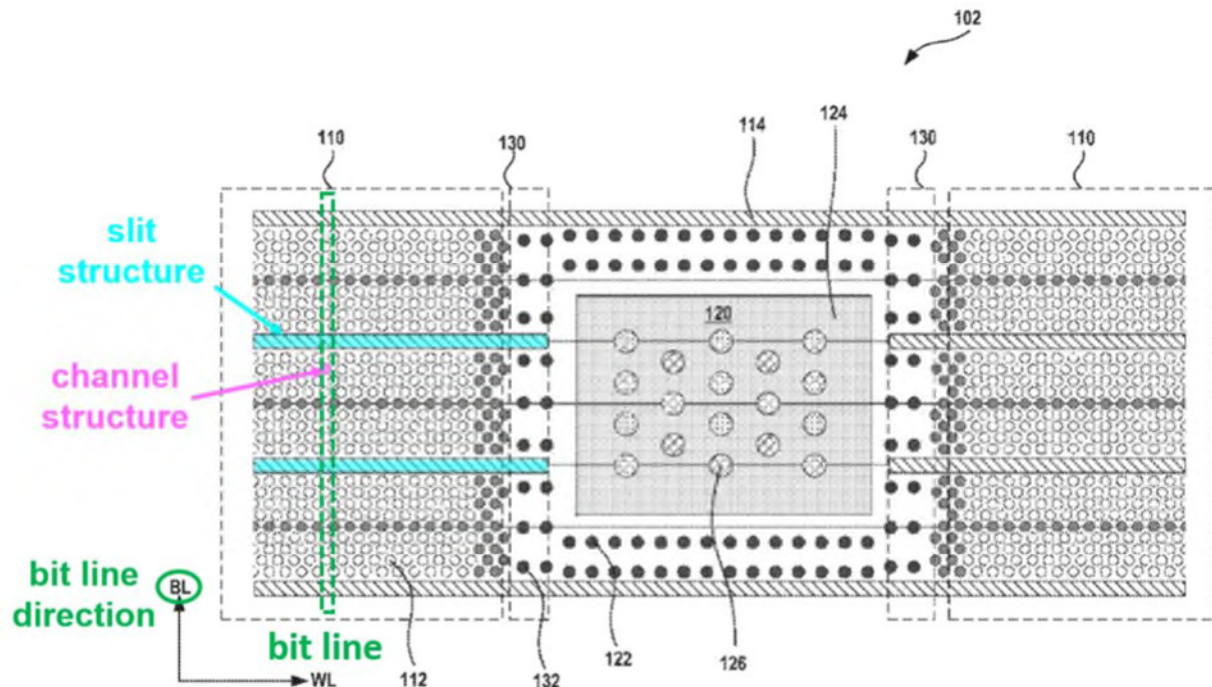
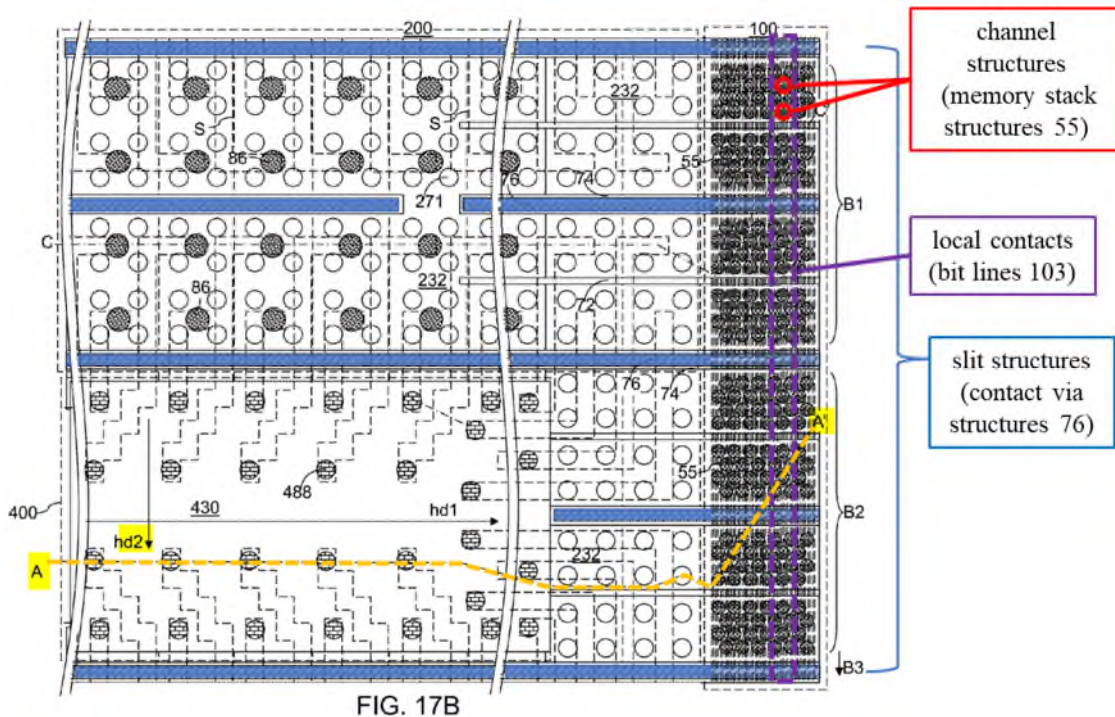


FIG. 1A

POR 32 (annotating '378 patent, Figure 1A).

69. By the same logic, Toyama discloses limitation [18.A]. Specifically, each of Toyama's embodiments discloses *local contacts* (“bit lines 103”) *disposed on the channel structures* (“memory stack structures 55”) *and the slit structures* (“laterally elongated contact via structures 76”) (limitation [15.G]), such that

Toyama discloses *an etch stop plug* (“drain region 63”) *interposed between each* *who local contact of the local contacts* (“bit lines 103”) *and each channel structure* *of the channel structures* (“memory stack structures 55”). Pet. 102-103. Figure 17B illustrates this disclosure in Toyama’s First Exemplary Structure:

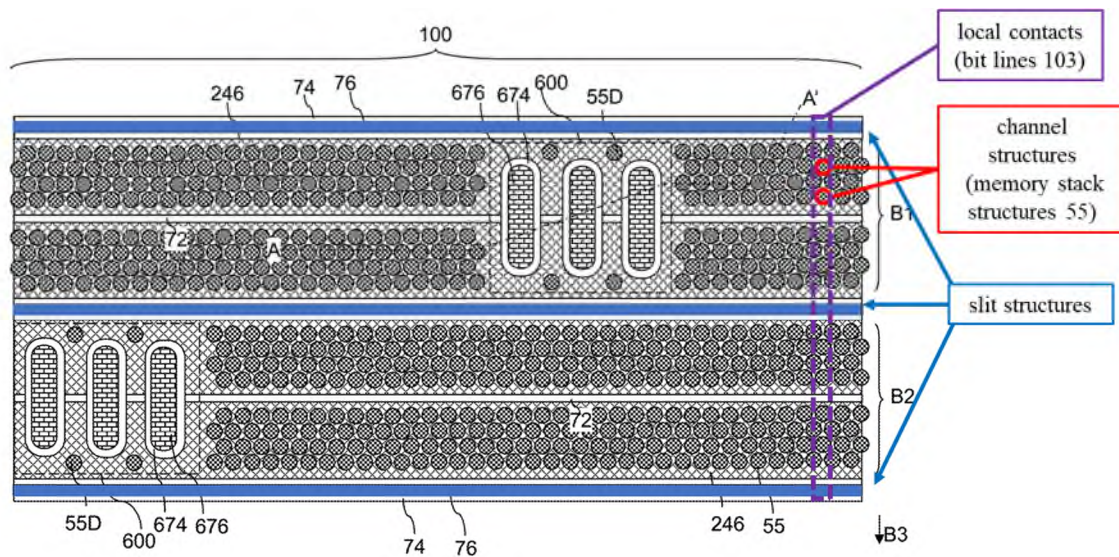


Toyama, Figure 17B (annotated). Although “bit lines 103” are not expressly labeled in Figure 17B, a POSITA would have understood that Toyama’s First Exemplary Structure includes bit lines as indicated in the annotated figure. For example, Toyama states (at [0250]) that “bit lines 103 extend along at the second horizontal direction hd2.” Figure 17B depicts the second horizontal direction (hd2), as is highlighted in the annotated figure. Confirming this, Toyama states (at [0251]) that “bit lines 103 are illustrated in dotted lines” in Figure 17B. Further

confirming this, Figure 17D expressly labels “bit lines 103” where they are indicated in the annotated version of Figure 17B.

70. As the annotated version of Figure 17B shows, “bit lines 103” (in purple) are above “memory stack structures 55” (in red), and Toyama explains (and a POSITA would have understood) that in between “memory stack structures 55” and “bit lines 103” are “drain regions 63.” Toyama, [0251], Figure 17A.

71. Figure 48B similarly depicts this disclosure in Toyama’s Second Modification:



Toyama, Figure 48B (annotated).

72. Although Figure 48B does not expressly label “bit lines 103,” a POSITA would have understood that Toyama’s Second Modification includes bit lines 103 as indicated in the annotated figure. For example, Toyama (at [0342])

explains that “bit lines 103 ... extend along the second horizontal direction.” A POSITA would have understood that the second horizontal direction is the direction indicated by the purple annotation at least in part because the “laterally-elongated contact via structures 76” (that is, the “slit structures” labeled above in blue) are described as “extending along the first horizontal direction hd1,” and “the second horizontal direction hd2” is described as “perpendicular to the first horizontal direction hd1.” Toyama, [0329], [0331].

73. A POSITA would have further understood that the etch stop plugs (“drain regions 63”) are interposed between “bit lines 103” and “memory stack structures 55.” Toyama, [0251], Figure 49.

VI. CONCLUSION

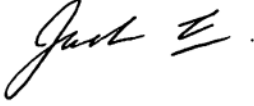
74. For the reasons explained above, it is my opinion that each of the Grounds above renders all Challenged Claims obvious.

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willfully false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1101 of Title 18 of the United States Code.

Inter Partes Review of U.S. Patent No. 10,658,378
Reply Declaration of Dr. Jack C. Lee

Date: June 25, 2025

Location: Austin TX

Signature: 
DR. JACK C. LEE