

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner

Case No.: IPR2024-00910
U.S. Patent No. 10,861,872
Issue Date: December 8, 2020

Title: THREE-DIMENSIONAL MEMORY DEVICE AND METHOD
FOR FORMING THE SAME

**PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 10,861,872
PURSUANT TO 35 U.S.C. §§311-319 AND 37 C.F.R. §42**

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LISTING OF EXHIBITS

Exhibit	Description
1001	U.S. Patent No. 10,861,872 B2 to Liu et al.
1002	File History of U.S. Patent No. 10,861,872 to Liu et al.
1003	Declaration of Dr. Sanjay Banerjee (“Banerjee”)
1004	<i>Curriculum Vitae</i> of Dr. Sanjay Banerjee
1005	U.S. Patent No. 9,859,297 B2 to Park et al. (“Park”)
1006	U.S. Patent Publ. No. 2019/0081061 A1 to Tessariol et al.
1007	Aritome, “NAND Flash Memory Technologies” (2016)
1008	Silvagni, “3D NAND Flash Based on Planar Cells,” Computers 2017
1009	Micheloni et al., “Inside Solid State Drives (SSDs)” (2 nd Ed. 2018)
1010	U.S. Patent No. 10,381,369 B2 to Kim et al.
1011	U.S. Patent No. 10,475,737 B2 to Tang et al.
1012	Certified English Translation of Chinese Patent Application Publ. No. CN108766971 to Liu (“Liu”)
1013	Chinese Patent Application Publ. No. CN108766971 to Liu
1014	U.S. Patent No. 8,945,996 B2 to Tang et al.
1015	YMTC’s Exemplary Infringement Claim Chart for U.S. Patent No. 10,861,872 – 128L (Ex. 49) [PROTECTIVE ORDER MATERIAL – FILED UNDER SEAL]
1016	YMTC’s Exemplary Infringement Claim Chart for U.S. Patent No. 10,861,872 – 176L (Ex. 50) [PROTECTIVE ORDER MATERIAL – FILED UNDER SEAL]

Petition for *Inter Partes* Review of U.S. Patent No. 10,861,872

Exhibit	Description
1017	YMTC’s Exemplary Infringement Claim Chart for U.S. Patent No. 10,861,872 – 232L (Ex. 51) [PROTECTIVE ORDER MATERIAL – FILED UNDER SEAL]
1018	Print out from Geographic Wiki, https://www.studycountry.com/wiki/what-is-a-piece-of-land-surrounded-by-water-on-2-side (last visited Mar. 28, 2024)
1019	U.S. Patent No. 9,530,492 to Lee
1020	Minute Order, Dkt. No. 42, dated February 22, 2024 in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1021	Combined Civil and Criminal Federal Court Management Statistics (December 31, 2023), available at https://www.uscourts.gov/sites/default/files/data_tables/fcms_na_distcomparison1231.2023.pdf
1022	Docket from <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1023	Micheloni, “3D Flash Memories” (2016)
1024	U.S. Patent No. 9,953,992 to Ogawa et al. (“Ogawa”)
1025	U.S. Patent No. 10,290,643 to Kai et al. (“Kai”)
1026	YMTC’s Exemplary Infringement Claim Chart for U.S. Patent No. 10,861,872 – 232L (Ex G-3 to YMTC’s Disclosure of Asserted Claims and Infringement Contentions), dated May 6, 2024 [PROTECTIVE ORDER MATERIAL – FILED UNDER SEAL]
1027	U.S. Patent No. 10,115,632 to Masamori et al.
1028	U.S. Patent No. 5,945,717 to Chevallier

Petition for *Inter Partes* Review of U.S. Patent No. 10,861,872

Exhibit	Description
1029	U.S. Patent No. 10,347,487 to Lee et al.
1030	Ronse, “Optical lithography—a historical perspective,” C. R. Physique 7 (2006)
1031	Complaint for Patent Infringement, Dkt. No. 1, filed Nov. 9, 2023, in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1032	First Amended Complaint for Patent Infringement, Dkt. No. 29, filed Feb. 2, 2024, in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1033	Plaintiff and Counterclaim Defendant Yangtze Memory Technologies Company, Ltd.’s Disclosure of Asserted Claims and Infringement Contentions, dated May 6, 2024, in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL

I. INTRODUCTION

Pursuant to 35 U.S.C. §§311-319 and 37 C.F.R. §42, Petitioner Micron Technology, Inc. (“Micron” or “Petitioner”) respectfully requests *Inter Partes* Review (“IPR”) of claims 7-10 (“the Challenged Claims”) of U.S. Patent Number 10,861,872, titled “Three-Dimensional Memory Device and Method for Forming the Same” (Ex. 1001, “the ’872 Patent”), and cancel those claims as unpatentable. Micron previously filed IPR2024-00789, which challenges a different set of claims from the ’872 Patent than this Petition. *See* §II.D. Concurrently filed herewith, Micron’s Explanation for and Ranking of Two Petitions explains the basis for filing this second Petition. Challenged Claims 7-10 depend on claims 1 and 5. This Petition relies on Ground 1 (the “Park Ground”) from IPR2024-00789 to demonstrate that the elements of claims 1 and 5 are disclosed or rendered obvious.¹ The Petition

¹ In this Petition’s claim construction section, Petitioner also points out that Patent Owner’s interpretation of “surrounding” is consistent with Petitioner’s, which only came to light when Petitioner received Patent Owner’s infringement contentions in district court after the filing of IPR2024-00789. *See* §VII.B. Because claims 7-10 rely on claim 5 and introduce additional requirements, this Petition also offers an additional mapping to claim 5 for the purposes of these new dependent claims.

relies on Park in view of the knowledge of a POSITA (e.g., Ogawa) to demonstrate that claims 7-10 are unpatentable.

The '872 Patent relates to 3D NAND. The '872 Patent's earliest priority date is February 26, 2019, which follows more than a decade of 3D NAND development. The claims of the '872 Patent recite conventional 3D NAND components (i.e., substrate, memory stack, staircase structure, and a staircase contact) and “dummy source structures” that surround a staircase contact. Ex. 1001, Abstract. The dummy source structures allegedly improve the process known as the gate-line replacement process. *Id.*, 5:17-34. In that process, a stack is first built with alternating sacrificial layers (which are typically dielectric) and insulating layers. *Id.*, 4:30-33. Then, voids (e.g., gate line slits) in the stack are formed, and the sacrificial layers are removed and replaced with conductive gate layers using the voids (i.e., the voids are the openings through which the etch and deposition materials are delivered into the stack). *Id.*, 4:46-55. Finally, the voids are filled, e.g., with a dielectric material. *Id.*, 4:44-46. The '872 Patent alleges that the prior art voids (i.e., gate line slits) create problems when replacing the sacrificial layers with the conductive gate layers. *Id.*, 4:46-55. To solve these alleged problems, the '872 Patent proposes “replacing the [gate line slits] with dummy source structures.” *Id.*, 5:30-34.

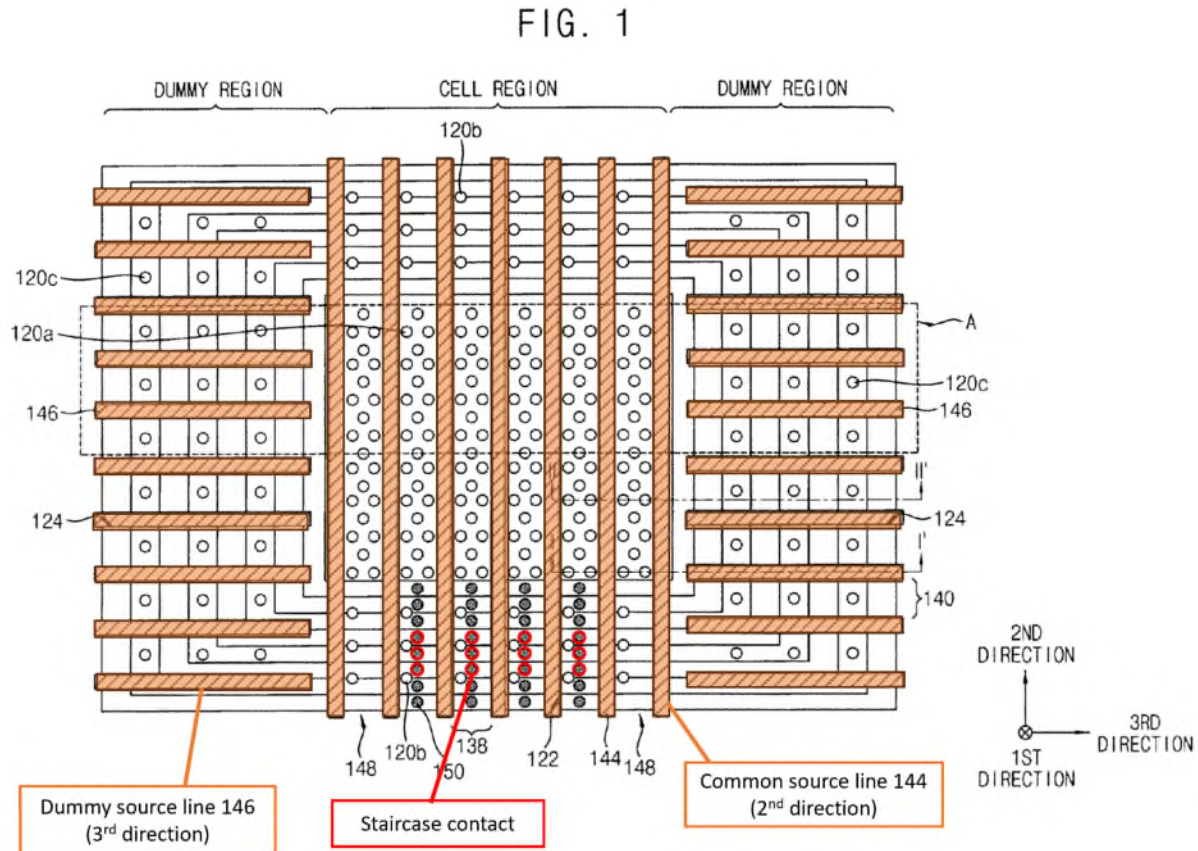
The '872 Patent describes the structure of the “dummy source structures” in broad terms. For example, the structures (1) may or may not be formed using the

same etch process as the process for forming channel structures, (2) may or may not be circular, but may extend laterally to separate the memory stack into smaller units, and (3) may not even be inoperable (which is what “dummy” suggests) but, instead, may be operative structures such as interconnects. Ex. 1001, 2:14-17, 13:3-5, 11:44-49. What is clear is that the structures must occupy the openings that are used in the gate replacement process.

During the brief prosecution of the '872 Patent, the Examiner rejected the pending claims over the prior art, specifically identifying an alleged “dummy source structures.” See Ex. 1002, 467-78. To distinguish this prior art, Applicant had to amend the claims to require that the “dummy source structures” comprise “a ***conductive contact***.” *Id.*, 510-517.

Notwithstanding this amendment, nothing in the Challenged Claims is new or nonobvious. This Petition relies on Park as the primary reference. Park’s dummy and common source lines are “dummy source structures.” To start, Park’s dummy and common source lines include the limitation added during prosecution: that the dummy source structures include a conductive contact. Park, 3:23-24 (“The dummy source lines and the common source lines may include a same conductive material.”). And just like the '872 Patent, Park’s dummy and common source lines (1) occupy the voids that are used in the gate line replacement process, and (2) surround the staircase contacts. What’s more, Park’s dummy and common

source lines divide the memory stack, which the '872 Patent discloses as an example of dummy source structures. Below is a plan view of Park's memory device, with its dummy and common source lines annotated in orange and the staircase contacts annotated in red.

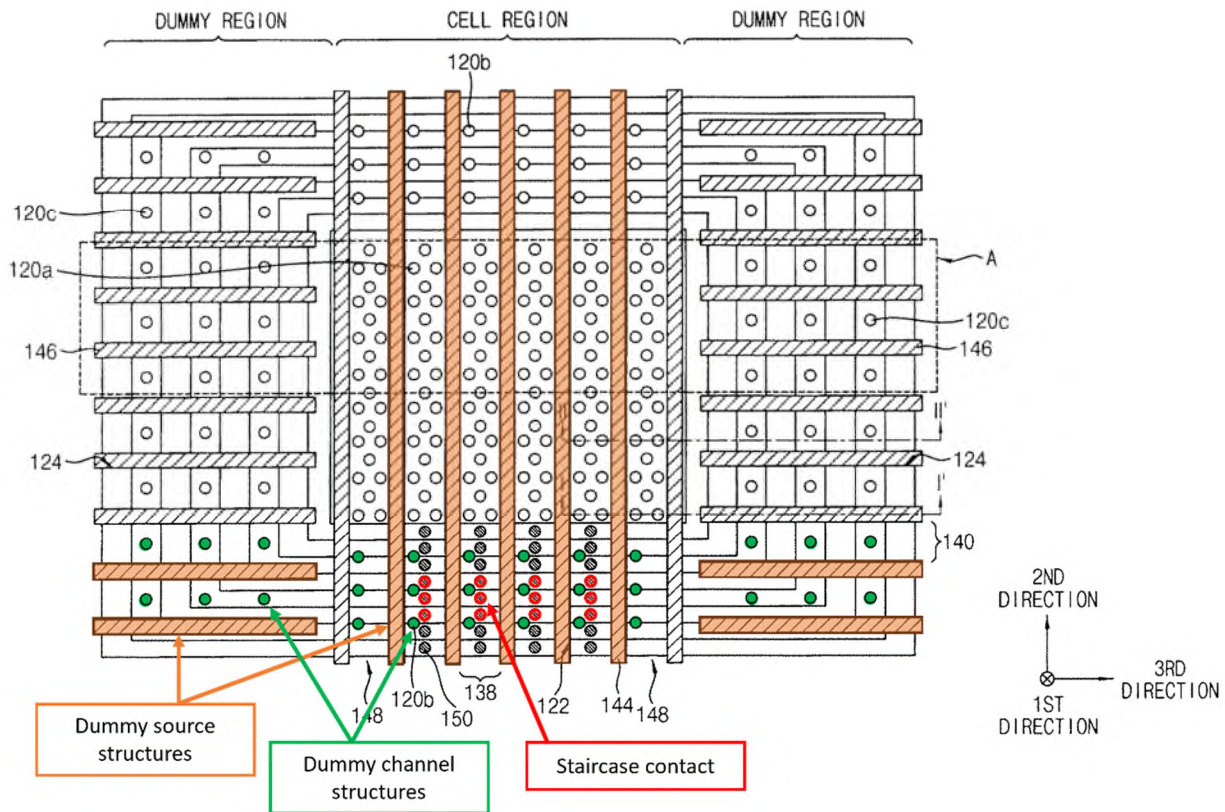


Id., Fig. 1.²

Claims 7-10 relate to using dummy *channel* structures, in addition to dummy source structures, to surround a staircase contact. Park discloses that dummy channel structures 120b also surround a staircase contact(s):

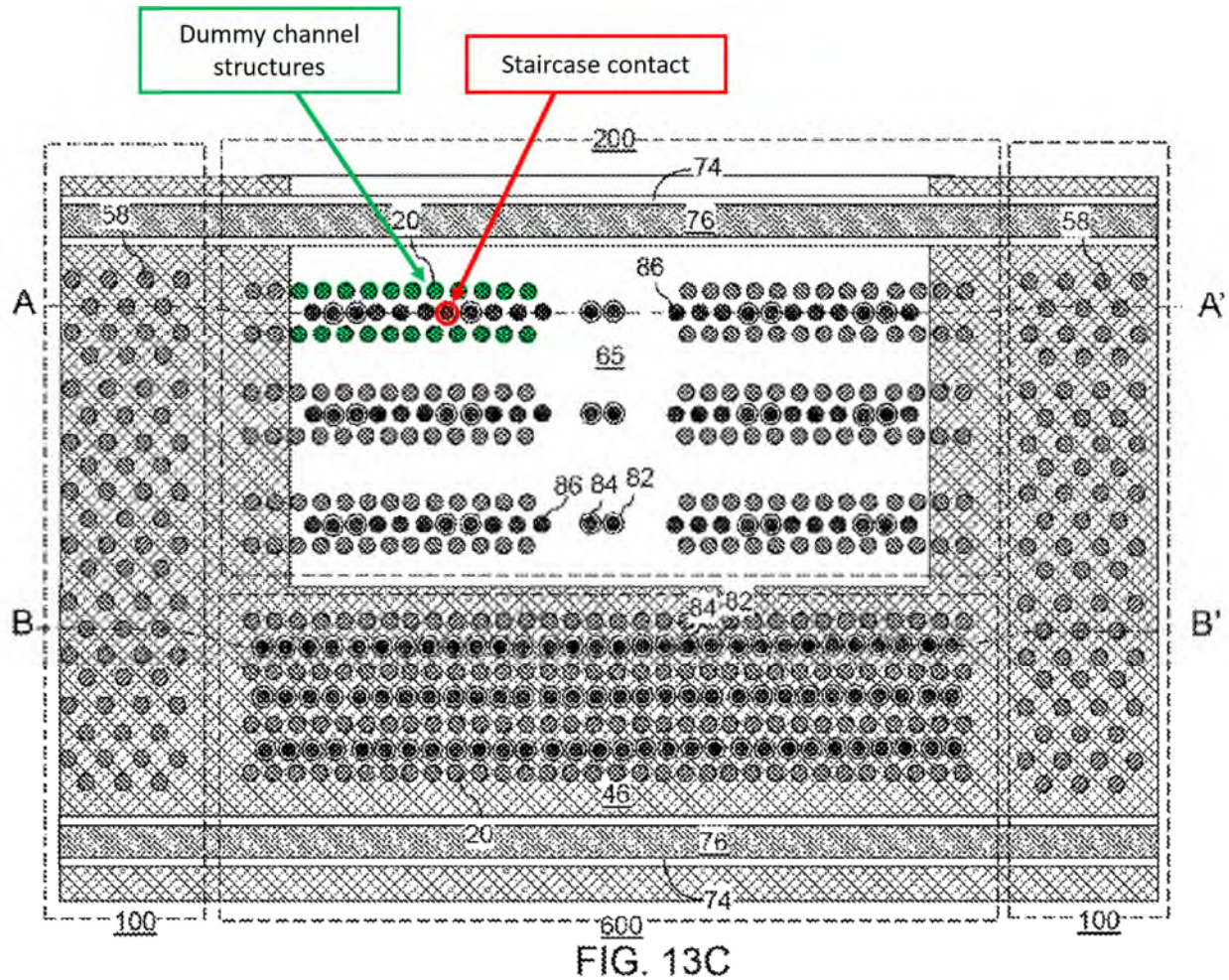
² All annotations are added herein unless otherwise noted.

FIG. 1



Id., Fig. 1.

This Petition also demonstrates that a POSITA was well aware (1) of the need for these dummy channel structures (a support structure is necessary in view of the sacrificial gate replacement process), and (2) that multiple arrangements of the dummy source structures were suitable to serve this need. For example, a common arrangement was to line both sides of a staircase contact with rows of dummy channel structures:



Ex. 1024 (“Ogawa”), Fig. 13C.

Petitioner requests that the Board institute trial and find the Challenged Claims unpatentable as obvious under §103.

II. REQUIREMENTS FOR PETITION FOR INTER PARTES REVIEW

A. Grounds for Standing (37 C.F.R. §42.104(a))

Petitioner certifies that the '872 Patent is available for IPR and that Petitioner is not barred or estopped from requesting IPR of the Challenged Claims of the '872 Patent on the grounds identified herein.

B. Notice of Lead and Backup Counsel and Service Information (37 C.F.R. §§42.8(b)(3-4), 41.10(a))

Pursuant to 37 C.F.R. §§42.8(b)(3-4) and 42.10(a), Petitioner provides the following designation of Lead and Back-Up counsel.

Lead Counsel	Back-Up Counsel
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Petitioner consents to service by electronic mail at the following addresses: PTABDocketJL2@orrick.com, P52PTABDocket@orrick.com, PTABDocketJ3B3@orrick.com, and micron-ymtc_ohs@orrick.com. Pursuant to 37 C.F.R. §42.10(b), Petitioner's Power of Attorney is attached.

C. Notice of Real-Parties-in-Interest (37 C.F.R. §42.8(b)(1))

Petitioner Micron Technology, Inc. and its subsidiaries, including Micron Consumer Products Group LLC, are the real-parties in interest.

D. Notice of Related Matters (37 C.F.R. §42.8(b)(2))

According to USPTO assignment records, the '872 Patent is currently assigned to Yangtze Memory Technologies, Co., Ltd. ("YMTC" or "Patent Owner"). YMTC has asserted the '872 Patent and U.S. Patent Nos. 10,658,378, 10,868,031, 10,937,806, 10,950,623, 11,468,957, 11,501,822 and 11,600,342 in a co-pending litigation, *Yangtze Memory Technologies Co., Ltd. v. Micron Technology, Inc. & Micron Consumer Products Group, LLC*, Case No. 3:23-cv-05792-RFL (N.D. Cal., filed Nov. 9, 2023) ("Co-Pending Litigation").

In addition to this Petition, Petitioner is filing (or has filed) petitions for *inter partes* review of each asserted patent in the Co-Pending Litigation:

Petition for *Inter Partes* Review of U.S. Patent No. 10,861,872

Patent	PTAB Proceeding	Wave 1/Wave 2
10,658,378 (claims 15-17 and 19-20)	IPR2024-00788	Wave 1 Petitions
10,861,872 (claims 1-6 and 11-13)	IPR2024-00789	
10,868,031	IPR2024-00790	
10,937,806 (claims 8-9 and 11-12)	IPR2024-00791	
10,950,623	IPR2024-00794	
11,468,957	IPR2024-00792	
11,501,822	IPR2024-00795	
11,600,342 (claims 1-6 and 8-20)	IPR2024-00793	
10,658,378 (claims 1-7 & 18)	IPR2024-00909	Wave 2 Petitions
10,861,872 (claims 7-10)	IPR2024-00910	
10,937,806 (claim 10)	IPR2024-00911	
11,600,342 (claim 7)	IPR2024-00912	

The Director and the Board should allow this Petition under 35 U.S.C. §314(a), 35 U.S.C. §325(d), and/or 37 C.F.R. §42.108(a). Concurrently filed herewith, Micron’s Explanation for and Ranking of Two Petitions explains the basis for filing this second Petition challenging a different set of claims of the ’872 Patent.

E. Fee for *Inter Partes* Review

The Director is authorized to charge the fee specified by 37 C.F.R. §42.15(a), and any other required fees, to Deposit Account No. 15-0665.

F. Proof of Service

Proof of service of this Petition on the Patent Owner at the correspondence addresses of record for the '872 Patent is attached.

III. IDENTIFICATION OF CLAIMS BEING CHALLENGED (§42.104(B))

Petitioner requests IPR of claims 7-10. This Petition discusses claim construction, explains why the claims are unpatentable, provides details regarding where the various claim limitations are found in the prior art, and is supported by the accompanying Declaration of Dr. Sanjay Banerjee (“Banerjee,” Ex. 1003), a leading expert in the 3D NAND field. Ex. 1004.

Ground #1: Claims 7-10 are obvious over U.S. Patent No. 9,859,297 (Ex. 1005, “Park”).

This reference is prior art. *See* §IX.

IV. INSTITUTION SHOULD BE GRANTED

Petitioner has established a reasonable likelihood of success on the merits. All other requirements for IPR have been met. The Board should institute IPR.

A. There Are No Grounds For A §314 Discretionary Denial In This Case

There is a pending district court action involving the '872 Patent. The PTAB has explained that it “will not ... discretionarily deny institution in view of a parallel district court litigation where a petition presents compelling evidence of unpatentability.” 6/21/22 Interim Procedure, 2, 4-5. Petitioner submits that it

presents a compelling case here: the claims of the '872 Patent are unambiguously unpatentable.

Petitioner also notes that the factors considered by the Board when assessing whether to institute IPR in light of a parallel proceeding collectively weigh in favor of institution. *See Apple Inc. v. Fintiv, Inc.*, Case No. IPR2020-00019, Paper No. 11 (Mar. 20, 2020) (precedential) (“Fintiv”). In particular: the district court may stay the case, any potential trial will occur after the deadline for a final written decision, little district court work has occurred, petitioner diligently prepared this petition, and the petition is substantively strong.

1. Possibility of a Stay

Petitioner intends to seek a stay if the Board institutes IPR. Until this issue is adjudicated, any attempt to predict the outcome would require speculation. This factor is neutral. *See Sand Revolution II, LLC v. Continental Intermodal Group – Trucking LLC*, IPR2019-01393, Paper 24 at 7 (PTAB June 16, 2020) (informative) (“*Sand Revolution*”); *Fintiv* at 12 (similar).

2. Proximity of the Court’s Trial Date

On February 22, 2024, the district court entered a scheduling order which set a trial date of December 1, 2025. *See* Ex. 1020. As a result, if IPR proceedings are instituted, they should be completed well before the scheduled trial date. *See also* Ex. 1021 (statistics indicating that it takes on average 48.9 months to reach trial in

district). This weighs strongly in favor of institution.

3. Investment in the Parallel Proceeding

To date, the parties and the district court have invested very little in the parallel proceeding. Indeed, beyond engaging in some motion practice regarding the pleadings, no substantive progress has been made. The parties are over a month away from completing the exchange of contentions and have not taken any depositions. Fact discovery is in its infancy. No claim construction positions have been exchanged, no claim construction order has issued, no infringement or invalidity expert discovery has occurred, and no summary judgment motions have been filed. This weighs in favor of institution. *See Sand Revolution* at 11.

The Board also has explained that institution is appropriate where “the petitioner filed the petition expeditiously....” *Fintiv* at 11. Here, Patent Owner asserted eight different patents against Petitioner. Ex. 1022. Petitioner proceeded with diligence, filing eight petitions approximately six months after being served with the original complaint and approximately three months after the filing of an amended complaint. *Id.*, Exs. 1031-32. After Petitioner filed these eight petitions, Patent Owner asserted new claims against Petitioner in district court on May 6, 2024. Ex. 1033. Petitioner has filed petitions on these new claims—claims that Petitioner could not have foreseen would be asserted—within two weeks. This also weighs strongly in favor of institution.

4. Issue Overlap

The wave 1 and wave 2 Petitions challenge all asserted claims in the Co-Pending Litigation. Should the Board institute, Micron stipulates that it will not advance in District Court any invalidity defense that formed the basis of any of the grounds in this Petition. Micron submits that this eliminates any potential overlap in issues between the proceedings here and in District Court. The Board has found that such stipulations weigh in favor of institution. *Sand Revolution* at 11-12.

5. Party Overlap

Both Petitioner and Patent Owner are parties in the parallel proceeding. This, however, is of little moment as there is often party overlap when there is a parallel proceeding.

6. Other Circumstances

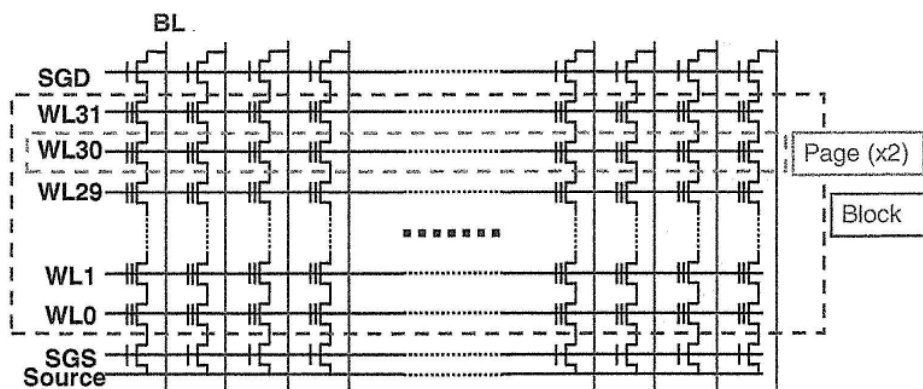
Here, Petitioner submits that its petition has significant substantive merit. It is premised on clear, understandable prior art that the Patent Office did not previously consider. Thus, this factor also weighs in favor of institution.

B. Denial Under §325(d) Would Be Inappropriate

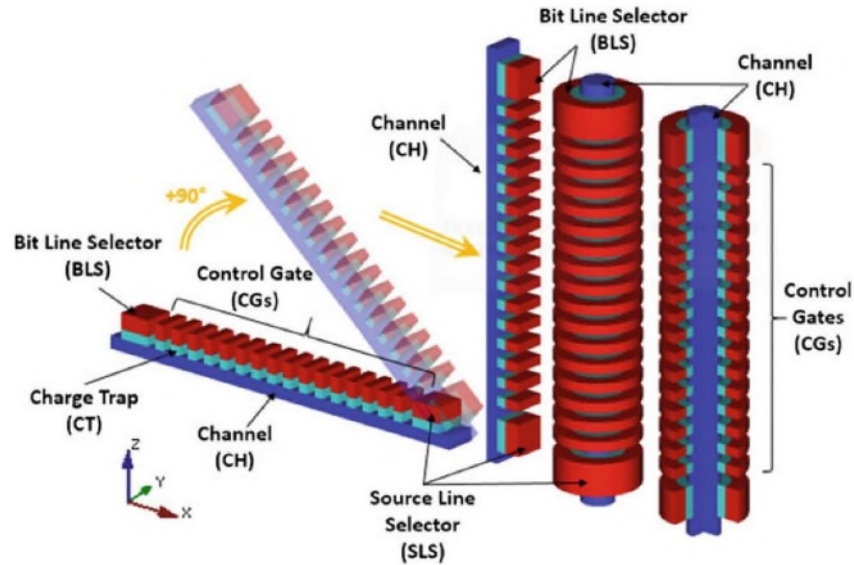
Neither PO nor the Examiner cited or discussed Park during prosecution of the '872 Patent. *See generally* Ex. 1002. Moreover, as §VI.B explains, the Examiner allowed the claims because the Applicant amended them to require that the “dummy source structures” include conductive elements. Park’s “dummy source structures” have conductive contacts (a conductive core). *See* §X.A.7.

V. TECHNOLOGY BACKGROUND

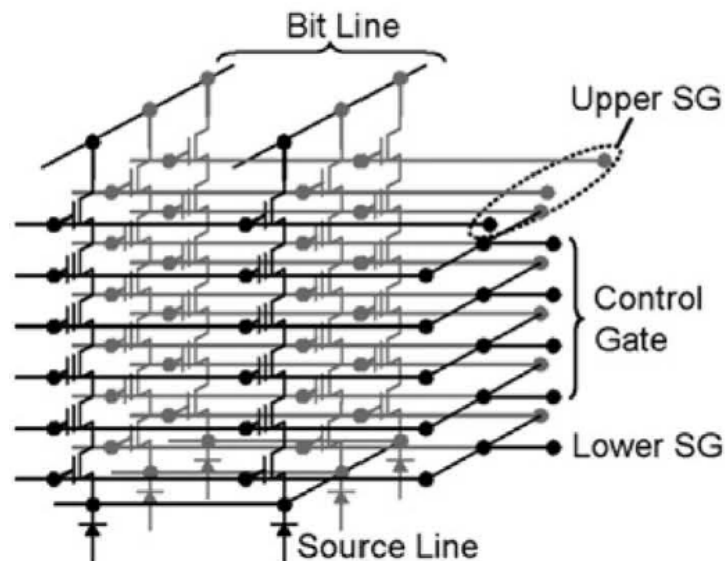
The '872 Patent and the prior art discussed in this Petition relate to three-dimensional (3D) memory devices, *e.g.*, 3D NAND memory devices. In NAND memory devices, NAND cells are arranged in “strings” with multiple cells “connected in series.” Ex. 1007, 38. Early NAND devices were formed as two-dimensional arrays of cells on a substrate surface. *Id.*, 58.



Id., 40. As shown, the cells are grouped into “page[s]” extending along the word lines and “block[s].” *Id.* “[T]o further scale down the memory cell size,” “three-dimensional (3D) NAND flash cells” were developed. *Id.*, 292. “Conceptually, a modern 3D NAND structure could be conceived by starting from the 2D NAND string building block” and “turning the 2D NAND string upside,” “resulting” in a “3D structure” with a “vertical channel.” Ex. 1008, 3.



Ex. 1009, 122. Multiple such vertical channels are then repeated in a three-dimensional array:



Ex. 1007, 296; *see also* Banerjee ¶¶ 46-53.

3D NAND includes “multi-stacked layers of gate (plate)” material alternated with “dielectric” in a “[s]tack.” Ex. 1007, 294. A “through-hole[.]” channel (also known as a channel structure) “filled by memory film ... and channel poly-Si” passes

through the layers to form the string of vertically arranged memory cells. *Id.*, 295.

“Each” layer of “electrode plate acts as a control gate.” *Id.* A particular vertical

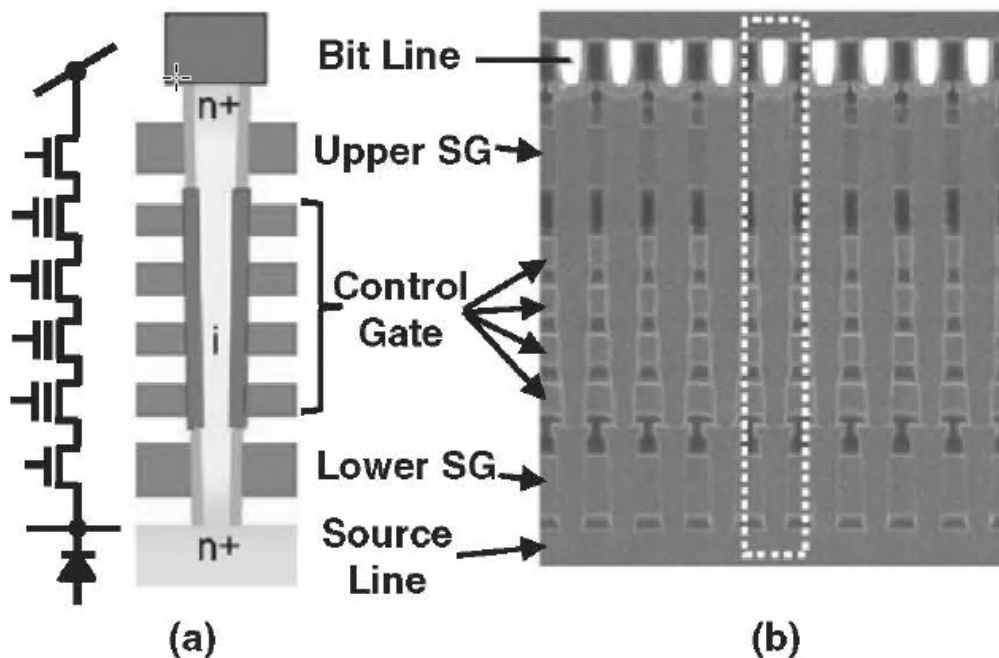
memory cell “string is selected by a bit line and an upper select gate (upper SG).”

Id., 295-296. A memory cell “is located in the intersection of a control gate plate”

and the memory film/poly-Si channel. *Id.* The lowest layer is a “select gate (lower

SG)” allowing the strings to connect to a lower “common source.” *Id.*, 295, 297.

An example 3D NAND vertical memory cell string is shown below:



Id., 296; Banerjee ¶ 54.

The stacked structure in 3D NAND devices typically include a core region, which includes the memory cells, and a peripheral region, which includes a connection region known as the staircase region. Ex. 1010 (U.S. Pat. No.

10,381,369), 5:43-6:11, 12:20-27. Staircase structures were well known and structurally provide landing areas on the control gates for contacts (below, the contacts 60 connect to different control gates):

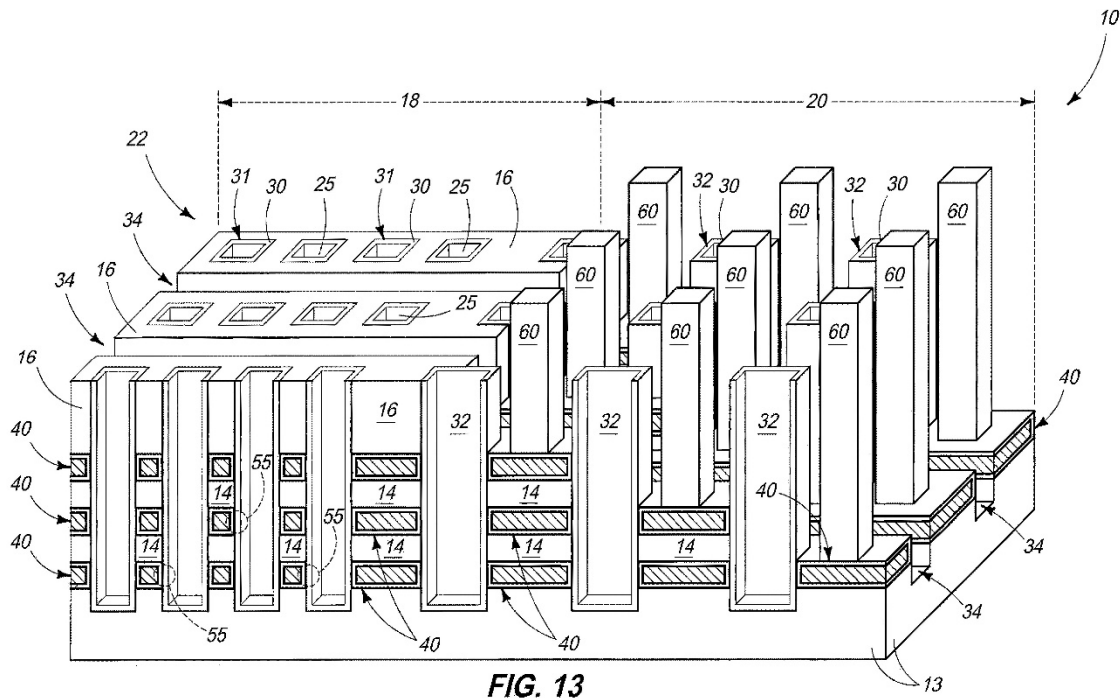
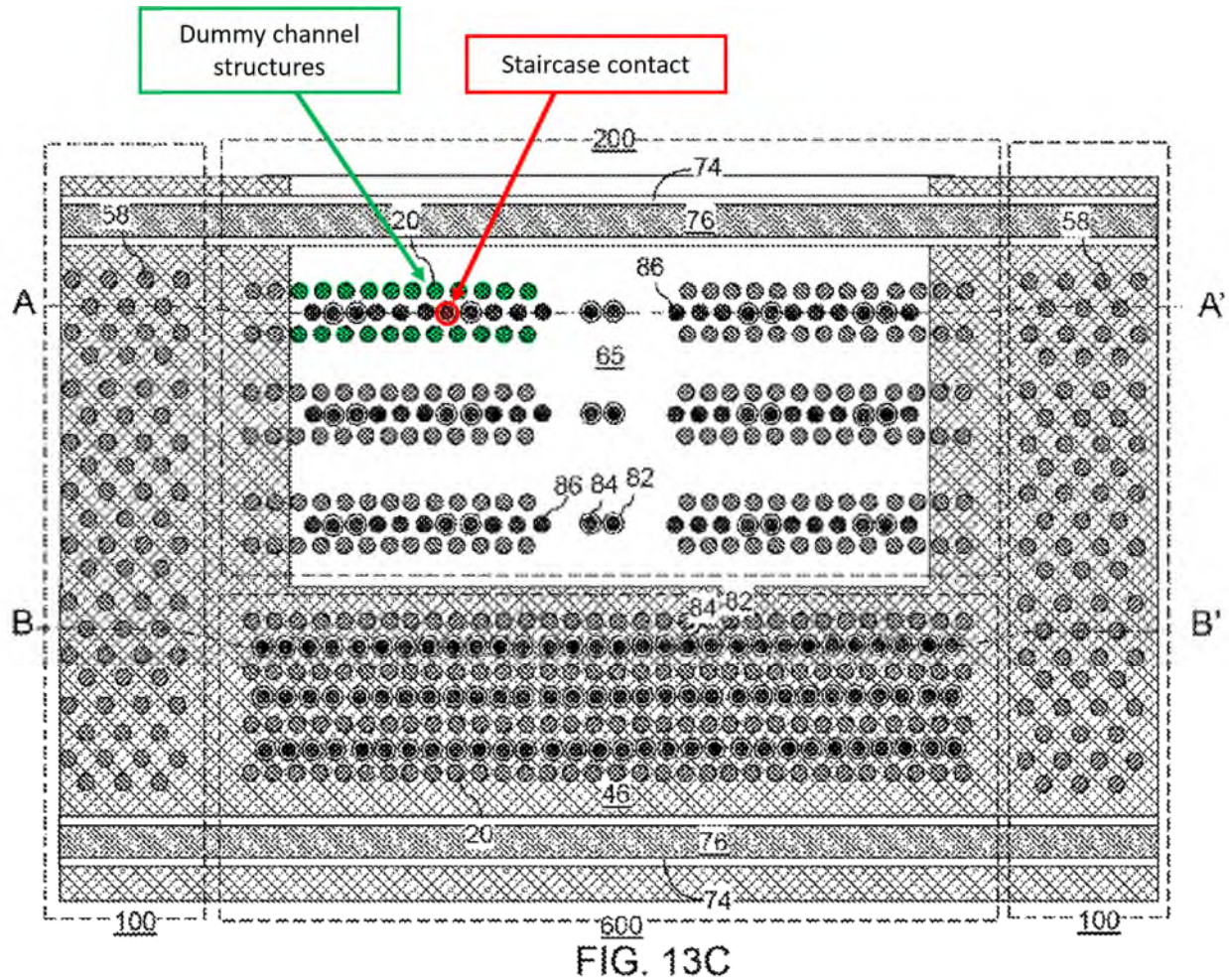


FIG. 13

Ex. 1011 (U.S. Pat. No. 10,475,737), Fig. 13, 4:56-64, 8:45-56; Banerjee ¶¶ 55-57.

One method of forming 3D NAND memory devices is to form the alternating stack of sacrificial gate layers and dielectric layers, and then replace the sacrificial gate layers with metal layers. Ex. 1012, [0062]. This is known as a gate replacement process. It was known that to perform this gate replacement process, “support pillars” were necessary to be included in the staircase structure (the support pillars extend through the stacked structure) to “prevent the stacked structure from collapsing.” *Id.* [0002], [0062]; *see also* Ex. 1014, 5:64-6:2 (“dummy” structures

have been used for a “load carrying ability of an operative structure”). Support pillars may be made with different materials, e.g., materials of a conductive via or materials of a channel structure, and may be a dummy structure (serve no other role than a supporting member) or an active structure (e.g., also serve as an interconnect to connect two circuit elements). *Id.*, 6:5-38, 7:19-23; Ex. 1012, [0044]; Ex. 1006, [0037], [0038], [0041]. One common approach was to line the location of the staircase contacts with rows of dummy channel support structures. For example, Ogawa discloses using rows of support pillars 20, which are dummy channels, on each side of staircase contacts 86 to surround those contacts:



Ogawa, Fig. 13C (annotated); 20:4-24 (“support pillar structure 20”), 28:22-24 (“word line contact via structures 86”), 13:51-14:61 (filling support openings 19, which become support pillars 20, with memory channel materials); *see also* Ex. 1025 (“Kai”), Fig. 15B (same configuration), 9:45-48, 25:58-26:2, 16:29-39; Banerjee ¶¶ 58-59.

VI. THE '872 PATENT AND ITS PROSECUTION HISTORY

A. The '872 Patent

The application that matured into the '872 Patent was filed on May 2, 2019 and is a continuation of application No. PCT/CN2019/076186, filed on February 26, 2019. Ex. 1001. This Petition therefore assumes that February 26, 2019, is the priority date for the '872 Patent (the “Priority Date”).

The '872 Patent is directed to “[t]hree-dimensional (3D) memory devices and methods for forming the 3D memory devices.” Ex. 1001, Abstract. Three-dimensional (3D) memory devices include basic elements such as a substrate, a memory stack comprised of interleaved conductive layers and dielectric layers formed on the substrate, a staircase structure, staircase electrical contacts, and dummy structures. *Id.*, 1:34-43; Banerjee, ¶¶ 60-61.

The '872 Patent addresses the traditional gate replacement process. Ex. 1001, 1:56-58, 4:30-33; 4:46-55; 5:17-28. As §V discusses, during this process, the sacrificial layers are etched away and replaced with conductive layers to form gate layers (also known as word lines). *Id.*, 1:56-58, 4:30-33; 4:46-55. The '872 Patent alleges that as three-dimensional (3D) memory devices continued to scale down, the gate replacement process would be more challenging. *Id.*, 4:37-38. The '872 Patent discusses the use of gate line slits (“GLS”) in the gate replacement process. GLS divide the interleaved sacrificial/dielectric stack (also known as a memory stack)

into smaller memory stacks. *Id.*, 4:37-46. A GLS has “large dimensions and is filled with an insulation structure formed in a trench.” *Id.* To form the GLS structure, trenches (voids) are etched through the stack. *Id.*, 4:44-49. These trenches are used in the gate-line replacement process, namely, they are used to etch the sacrificial gate layers and are used to deposit the gate lines (in other words, the etch and deposition material is sourced through the trench). *Id.*, 4:46-48. Annotated Figure 5 below shows a top view of a memory stack that is split into smaller memory stacks by GLSs. Banerjee, ¶¶ 62-63.

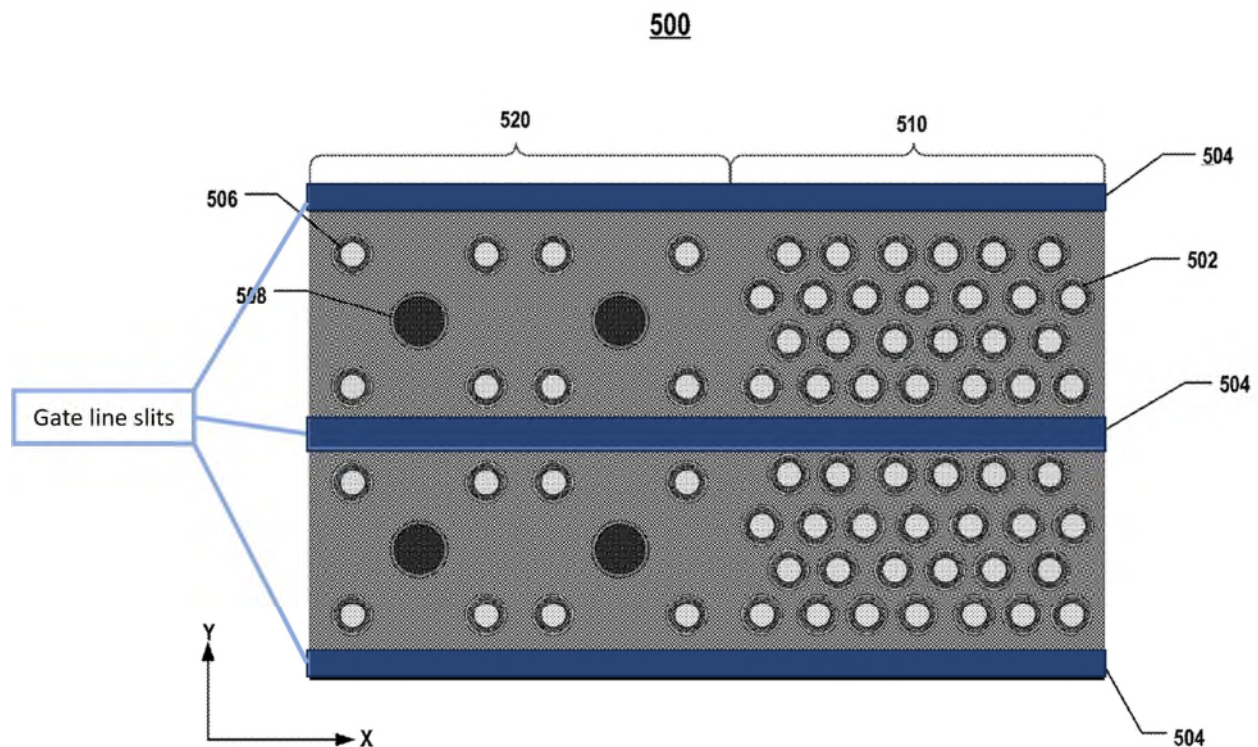
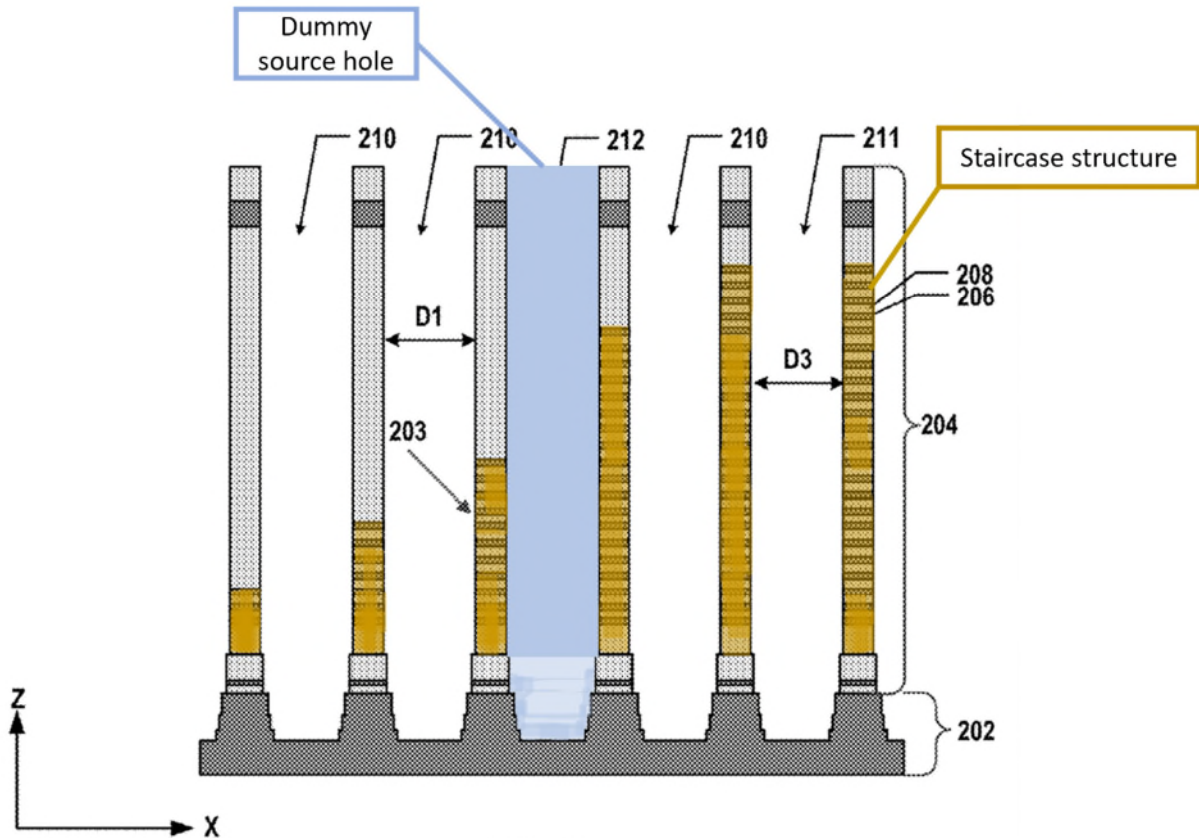


FIG. 5

The '872 Patent alleges that “[u]sing GLSs to perform the gate-replacement process has drawbacks. For example, in the staircase region, the large lateral distance between adjacent GLSs can cause conductive material to be unevenly filled in the lateral recesses formed after the removal of the sacrificial layers, resulting in voids in the formed gate electrodes.” Ex. 1001, 4:49-55. Allegedly, this is because “conductive materials for forming the gate electrodes need to travel a relatively long distance between adjacent GLSs 504 to fill in the lateral recesses formed after the removal of sacrificial layers.” *Id.*, 5:17-20; Banerjee ¶ 64.

The '872 Patent purports to solve this problem by replacing the GLSs in the gate replacement process with “dummy source structures.” Ex. 1001, 5:31-34. Annotated Figure 2A below shows the etched dummy source hole in the staircase structure.



Id., Fig. 2A. The '872 Patent discloses using this void for the gate replacement process. *Id.*, 15:16-25; Banerjee ¶¶ 65-66.

After the gate replacement process is complete, the '872 Patent discloses that dummy source structures “may include an insulating spacer layer in a dummy source hole and a conductive contact within the spacer layer.” Ex. 1001, 5:37-43. An insulating spacer (177) first lines the dummy source hole and then conductive material is deposited to form a dummy source structure (179), shown below in Figure 1D:

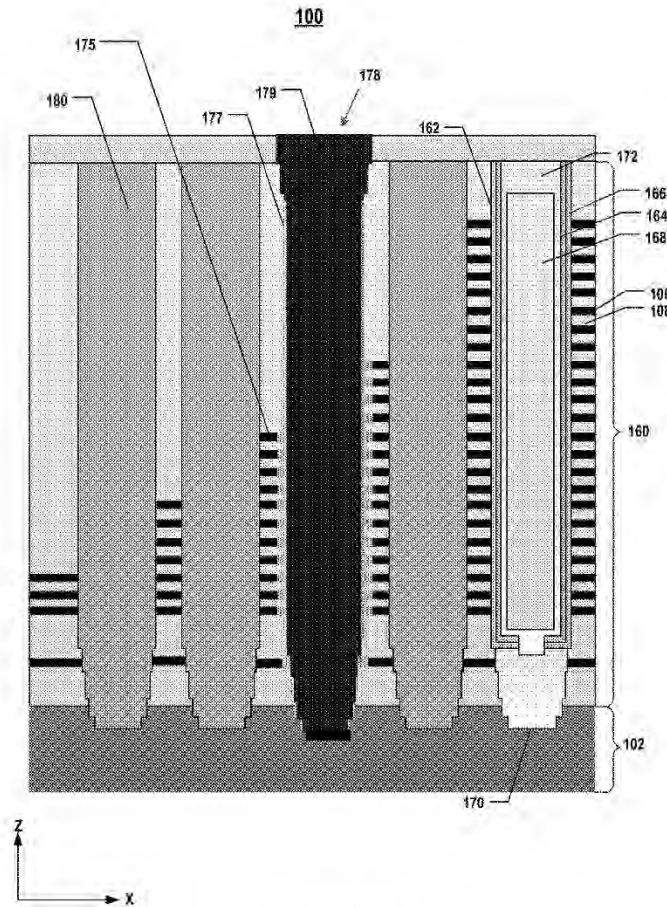


FIG. 1D

Id., Fig. 1D, 5:37-40; Banerjee ¶ 67.

The '872 Patent claims that using dummy source structures instead of GLSs may allow gate electrodes “to be formed with improved uniformity and quality, reducing the resistivity of the gate electrodes/word lines.” Ex. 1001, 5:49-52. Because conductive material “travels shorter distances to fill up the lateral recesses for forming the gate electrodes, the gate electrodes are less susceptible to voids or density nonuniformity.” *Id.*, 5:55-58; Banerjee ¶ 68.

The '872 Patent also discloses dummy channel structures. Channel structures are well-known elements that form the memory strings. *See* §V. The '872 Patent discloses that “memory string 104 can include a channel structure 162 extending vertically through memory stack 160. Channel structure 162 can include a channel hole filled with semiconductor materials (e.g., as a semiconductor channel 164) and dielectric materials (e.g., as a memory film 166). In some embodiments, semiconductor channel 164 includes silicon, such as amorphous silicon, polysilicon, or single crystalline silicon. In some embodiments, memory film 166 is a composite layer including a tunneling layer, a storage layer (also known as a ‘charge trap layer’), and a blocking layer.” Ex 1001, 10:13-23. The '872 Patent states that “[m]ethod 300 proceeds to operation 306, as illustrated in FIG. 3, in which a dummy channel structure is formed in each of the dummy channel holes. In the example of method 400 in FIG. 4, at operation 406, a sealing layer is formed in each of the dummy source holes. In some embodiments, a channel structure is formed in each of the channel hole.” *Id.*, 13:44-52. “Dummy” typically refers to an inoperable element (though for “dummy source structures,” the '872 patent departs from this common meaning, *see* §VII.A). Banerjee ¶ 71. The '872 Patent describes that the dummy source and dummy channel structures may surround the staircase contacts.

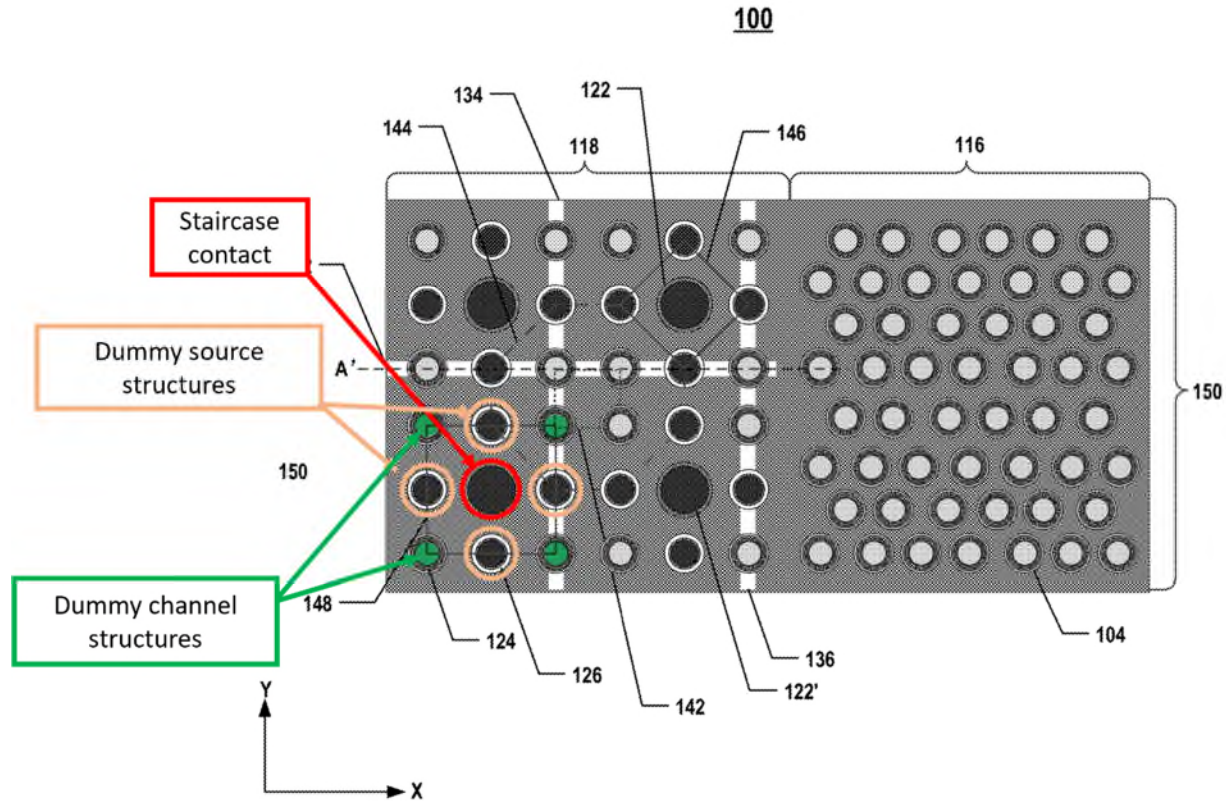


FIG. 1A

Ex 1001, Fig. 1A, 6:31-50; Banerjee ¶¶ 69-72.

B. Prosecution History

There was only one substantive Office Action during prosecution.

On June 11, 2020, the Examiner rejected claims 1-13 under 35 U.S.C. §102(a)(1) as anticipated by U.S. Pub. No. 2016/0293622A1 (“Jeong”). The Examiner found that Jeong disclosed a three-dimensional (3D) memory device with a substrate, a memory stack comprising interleaved conductive/dielectric layers on the substrate, a staircase structure on one side of the memory stack, a staircase contact in the staircase structure, and a plurality of dummy source structures extending vertically through the staircase structure and surrounding the staircase

contact. Ex. 1002, 470. The Examiner found that Jeong discloses “dummy pillars DP1 and DP2” that “function as a mechanical support for conductive layers” which were akin to “dummy source structures.” *Id.* The Examiner additionally found that Jeong’s dummy pillars DP1 and DP2 could also be dummy channel structures. *Id.*, 472.

On August 14, 2020, the Examiner and the Applicant discussed during a telephone interview the distinction between “dummy source” and “dummy channel” as contrasted with Jeong’s “dummy pillar” structure and possible amendments. Ex. 1002, 505. Based on the interview, the Applicant amended claims 1 and 8 on August 18, 2020 to add the limitation “wherein each of the dummy source structures comprises a conductive contact.” *Id.*, 510-511, 513. The Applicant argued that this feature is “not found in Jeong” because Jeong’s “dummy pillars do not include conductive contacts” whereas, citing the specification, “[a] dummy source structure 178 includes a dummy source hole filled with conductive materials” *Id.*, 513-514. The Applicant further emphasized the specification passage that states: “dummy source structures 178 can [also] laterally separate 3D memory device 100 into multiple memory regions, such as memory blocks,” and an exemplary dummy source structure is shown in Figure 1D. *Id.*, 514. In the same amendment and

request for reconsideration, the Applicant cancelled claims 15-20 and added claims 21-26.³ *Id.*, 513.

The Examiner did not consider any other prior art references in connection with or following the August 14, 2020 claim amendments, and allowed claims 1-14 and 21-26 on October 26, 2020. Ex. 1002, 524. The reasons for allowance were that Jeong did not disclose a dummy structure that comprised a conductive contact and that Jeong's dummy pillars DP1 and DP2 could be "considered as the dummy channel structures." *Id.*, 525-26.

VII. CLAIM CONSTRUCTION⁴

The Board in IPR proceedings applies the same *Phillips* claim construction standard that is used in federal district court cases. *See Phillips v. AWH Corp.*, 415

³ Application claims 21-23 correspond to '872 Patent claims 8-10 and application claims 24-25 correspond to '872 Patent claims 11-12.

⁴ Petitioner expressly reserves the right to challenge in district court litigation one or more claims (and claim terms) of the '872 Patent for failure to satisfy the requirements of 35 U.S.C §112, which cannot be raised in these proceedings. *See* 35 U.S.C. § 311(b). Nothing in this Petition shall be construed as a waiver of such challenge or agreement that the requirements of 35 U.S.C. §112 are met for any claim of the '872 Patent.

F.3d 1303 (Fed. Cir. 2005). For purposes of institution, Petitioner submits that only “dummy source structure” requires construction and that the rest of the terms of the ’872 Patent’s claims should be afforded their plain and ordinary meaning. The discussion below, however, also addresses the term “surrounding” to clarify that “surrounding” does require fully encircling.

A. “dummy source structure” (Claims 1, 5, 7-10)

The term “dummy source structure” is a limitation of all Challenged Claims.

Petitioner contends that the term “dummy source structure” would have been understood to mean a “structure that occupies the void that was used for the gate replacement process.” In the Co-Pending Litigation, PO appears to be interpreting this limitation to mean that the dummy source structure need not be formed in the voids that are used for the gate line replacement process. This is apparent from PO’s infringement contentions that map the dummy source structures to structures that occupy voids that have nothing to do with gate-line replacement. Ex. 1015 [128L chart], 3; Ex. 1016 [176L chart], 3-4; Ex. 1017 [232L chart], 3-6.

Petitioner’s construction is supported by the specification and file history of the ’872 Patent. The ’872 Patent seeks to address 3D memory structural issues that arise during the gate replacement process “by replacing the [gate line slits] with dummy source structures.” Ex. 1001, 5:30-34. The ’872 Patent explains that gate replacement processes can become more challenging as three-dimensional memory

devices scale down because gate line slits “ha[ve] large dimensions” that, when used to perform the gate replacement process, create problems such as unevenness and gaps in gate electrodes. *Id.*, 4:44-50. In the staircase region, “the large lateral distance between adjacent [gate line slits] can cause conductive material to be unevenly filled in the lateral recesses formed after the removal of the sacrificial layers, resulting in voids in the formed gate electrodes.” *Id.*, 4:50-55. The large area of gate line slits also “limit[s] the usable space on the wafer surface to place other components, such as staircase contacts.” *Id.*, 4:65-67; Banerjee ¶¶ 79-80.

Replacing gate line slits with “dummy source structures” allegedly solves the aforementioned issues. For example, the gate replacement process performed with dummy source holes results in gate electrodes “less susceptible to voids or density nonuniformity.” Ex. 1001, 5:49-58. Since the “gate-replacement process can be performed to deposit a conductive material through the dummy source holes that subsequently form the dummy source structures,” the “conductive material travels shorter distances to fill up the lateral recesses for forming the gate electrodes.” *Id.*; Banerjee ¶ 81.

Note that the '872 Patent describes solving the alleged problems by using the voids that are later occupied by the “dummy source structures,” namely, “dummy source holes.” For example, the '872 Patent discloses that because the “gate-replacement process can be performed to deposit a conductive material **through the**

dummy source holes that subsequently form the dummy source structures,” the “conductive material travels shorter distances to fill up the lateral recesses for forming the gate electrodes.” Ex. 1001, 5:49-58. Nonetheless, the specification defines the “dummy source structures” as what occupies the “dummy source holes”: “dummy source holes that subsequently form the dummy source structures.” *Id.* Thus, when the ’872 Patent states that it is “replacing the [gate line slits] with dummy source structures” (*Id.*, 5:30-34), what it means is that it is “replacing the [gate lines slits] with [dummy source holes in which the dummy source structures are subsequently formed].” *Id.*, 4:65-67; Banerjee ¶¶ 81-82.

While the specification makes clear that a “dummy source structure” occupies the void used for the gate replacement process, the specification does not impose any meaningful limitation on the actual structure of the dummy source structure (the claims only require that the structures include a conductive contact). In fact, the specification states that “[d]ifferent layouts, patterns, and designs” for the dummy source structure may be adopted “based on the size of the staircase region.” Ex. 1001, 8:51-53. And the specification states that the dummy source holes, which the dummy source structures occupy, may or may not be made using the same process that makes the dummy channel holes. *Id.*, 13:3-5. The dummy source structures and dummy channel structures also may be the same size. *Id.*, 8:11-19. Notably, the dummy source structure may assume the same shape as a gate line slit, because

the specification states that “dummy source structures 178 can *laterally separate* 3D memory device 100 into multiple memory regions, such as memory blocks.” *Id.*, 11:44-46 (emphasis added). This is precisely what the ’872 Patent admits that gate line slits do: “[f]or example, in some 3D memory devices such as charge trap 3D NAND memory devices, gate line slits (GLSs) are formed to divide an array of memory strings (e.g., in the inner region of a 3D memory device) and/or dummy channel structures (e.g., in the staircase region of the 3D memory device) into different memory regions.” *Id.*, 4:38-44. Further, while the claim term includes the word “dummy,” the specification explains that the structure might not even be an inoperable structure. Rather, the specification states that “dummy source structures” can “contact with the substrate and may provide interconnect between the 3D memory device and peripheral devices.” *Id.*, 5:40-43, 16:63-66; Banerjee ¶¶ 83-85.

During prosecution, the Applicant further emphasized the portion of the specification which states: “dummy source structures 178 can [also] laterally separate 3D memory device 100 into multiple memory regions, such as memory blocks.” Ex. 1002, 514. This again illustrates that a dummy source structure may assume many forms, including those that are, or resemble, gate line slits. Banerjee ¶ 86.

As demonstrated below, Ground 1 renders the Challenged Claims obvious under Petitioner’s and Patent Owner’s construction.

B. “surrounding” (Claims 1, 5, 7-10)

The term “surrounding” is a limitation of all Challenged Claims.

Independent claim 1 recites “the plurality of dummy source structures surrounding the staircase contact.” Petitioner contends that “surrounding,” in the context of the ’872 Patent, does not require that the dummy source structures form a border that fully encloses the staircase contact. This is evident from the specification, claims, and extrinsic evidence. Patent Owner agrees.

To start, the specification and claims make clear that “surround” does not even require that four dummy source structures surround the staircase contact (e.g., radially around the staircase contact at angles 0, 90, 180, and 270 degrees). The specification discloses that “the number of dummy source structures surrounding one or more dummy channel structure 124 may be more or less than eight, six, or four.” Ex. 1001, 8:8-11. In other words, there may be less than four dummy source structures that “surround” a word line contact. The claims use “surround” in the same way. Dependent claim 15, which depends on claim 14, recites: “wherein at least one dummy channel structure is surrounded by at least four dummy source structures.” *Id.*, Claim 15. Under the doctrine of claim differentiation, this implies that “surrounded” in independent claim 14 covers implementations in which fewer than four dummy source structures surround a single dummy channel structure. As shown below, a preferred embodiment employs four dummy source structures (126)

around staircase contact (122). If one of these dummy source structures were removed, there would be only three dummy source structures left, leaving even more openings around the staircase contact.

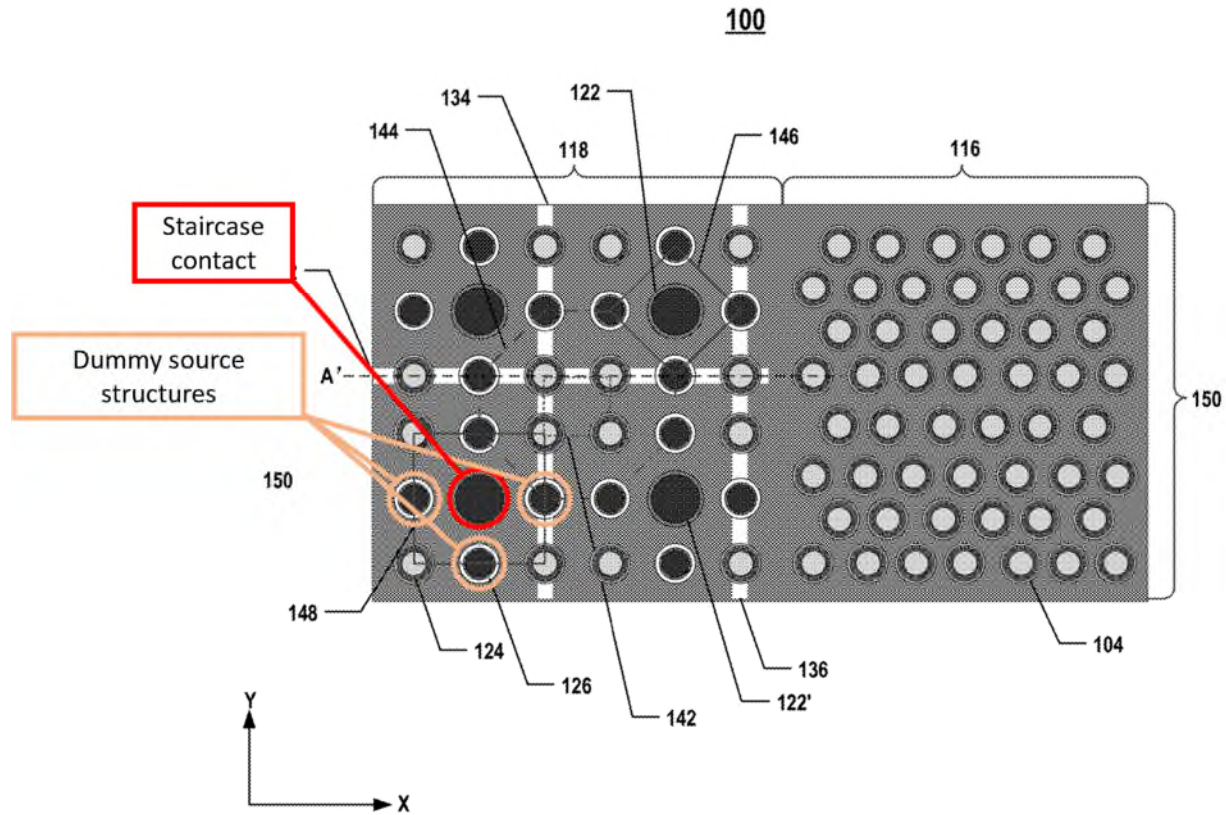
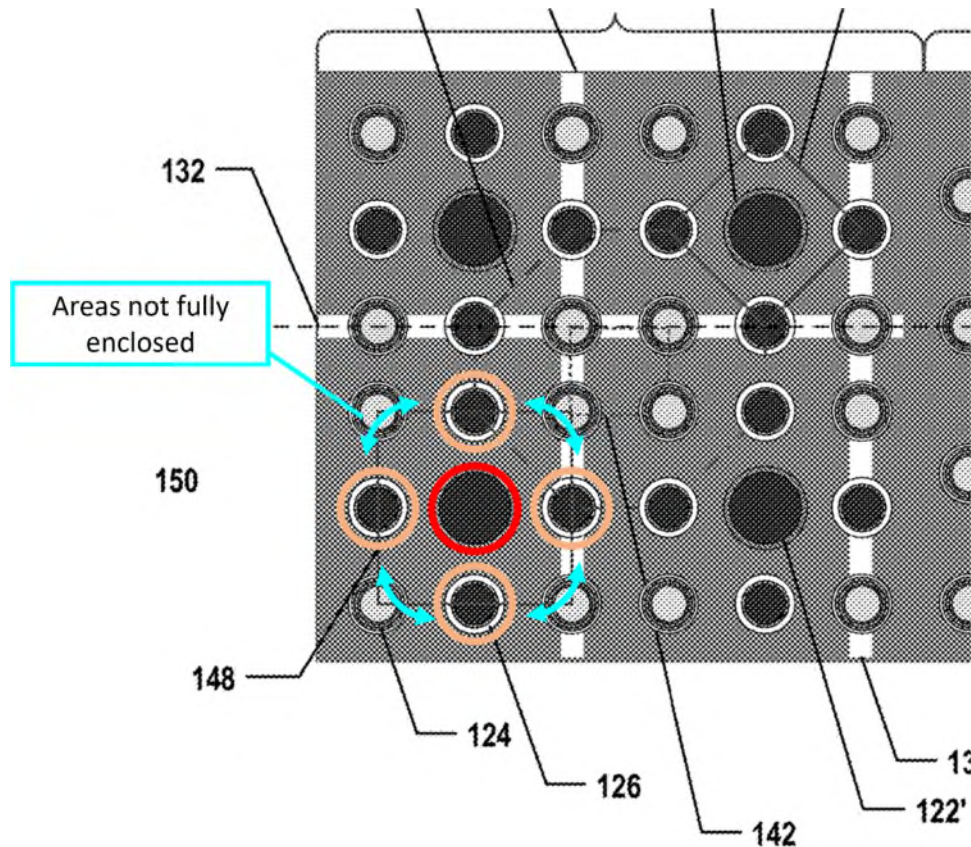


FIG. 1A

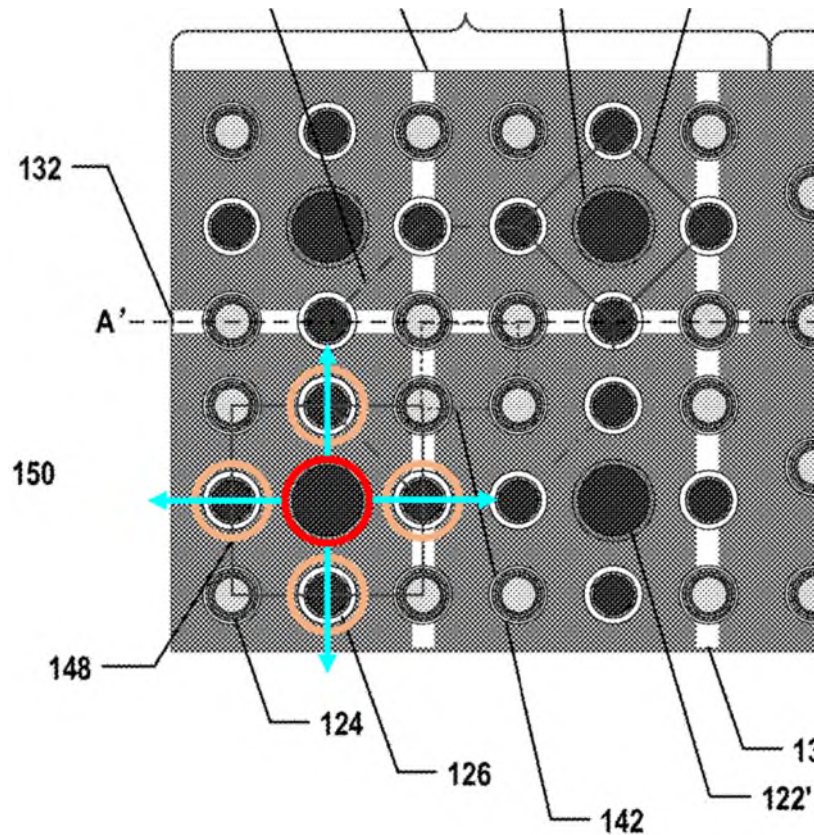
Id., Fig. 1A; Banerjee ¶¶ 89-94.

Indeed, even taking the case of four dummy source structures, these four structures do not come close to fully encircling the staircase contact. As shown below, there are large gaps between the dummy source structures (126), but those structures nonetheless “surround” the staircase contact (122).



Ex. 1001, Fig. 1A (partial) (annotated); Banerjee ¶ 95.

In this preferred embodiment, as shown below, “surrounded” includes being able to draw four lines outward from the staircase contact with each line being separated from the others by 90 degrees and intersecting a dummy source structure.



Ex. 1001, Fig. 1A (annotated); Banerjee ¶¶ 95-96.

What’s more, the specification makes clear that the number of a particular structure, e.g., dummy source structures, is not relevant to whether that structure “surrounds” another object. For example, the specification states that “[a]ny suitable number of dummy channel structures may be surrounded by any suitable number of dummy source structures.” Ex. 1001, 7:40-43. In other words, there could be fewer, larger dummy source structures that surround the staircase contact, e.g., only two dummy source structures such that when drawing four lines outward from the staircase contact, those lines intersect the dummy source structure

Using “surrounding” to not require fully encircling is simply a common usage of the term. “An isthmus is a thin strip of land surrounded by water on two sides, which connects two larger land masses.” Ex. 1018 (<https://www.studycountry.com/wiki/what-is-a-piece-of-land-surrounded-by-water-on-2-sides>). The same is true in the context of 3D NAND. For example, two lateral elements on each side of a structure “surround” that structure. Ex. 1019 (U.S. Pat. No. 9,530,492), 2:14-16 (“In other words, the conventional SBPI operations are strongly affected by the stored Vts of two surrounding NAND cells dispersed in the adjacent left and right BLs.”); Banerjee ¶ 97.

Patent Owner agrees with Petitioner’s interpretation that an object can be “surrounded” on two sides. This is evident from Patent Owner’s infringement contentions. For the limitation “a plurality of dummy channel structures surrounding the staircase contact,” Patent Owner identifies alleged dummy channel structures that run along only two sides of a staircase contact. Ex. 1026, 20-21.

An express construction of this term is not necessary, because as demonstrated below, the Park prior art reference discloses (1) dummy source structures such that drawing four lines outward from the staircase contact with each line separated by 90 degrees (e.g., at 45, 135, 225, and 315 degrees) will result in each line intersecting a dummy source structure, and (2) dummy source structures that create a border with fewer gaps than shown above in Figure 1A of the ’872 Patent. The dummy channel

structures similarly surround the staircase contact(s). And in any event, as discussed above, “surround” is not even so limited, because the specification and claims make clear that other embodiments include fewer than four dummy source structures shown in the above figures.

VIII. LEVEL OF ORDINARY SKILL IN THE ART

A POSITA in the field of the '872 Patent would have had a bachelor of science degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (e.g., researching, designing, or teaching) monolithic 3D structures and NAND memory devices, or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may replace some of the professional experience). This POSITA would have been aware of and generally knowledgeable about 3D NAND's structure, how it is manufactured, and its component parts. *See Banerjee*, ¶¶ 40-43.

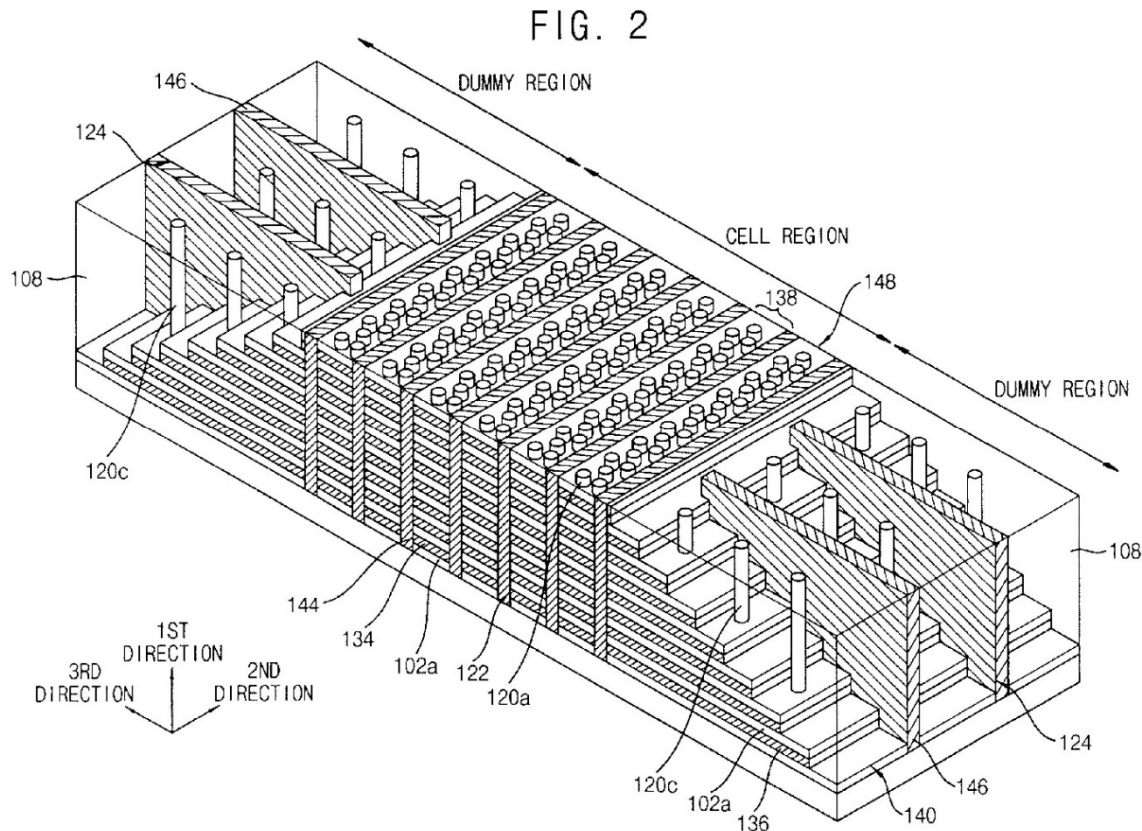
IX. DESCRIPTION OF THE PRIOR ART

A. Park

Park was filed on February 19, 2016, and is prior art under AIA §102(a)(2). Park, Cover. Park, like the '872 Patent, is directed to, and teaches the basic structural components of, a three-dimensional memory device and methods for making them. Those basic components include a substrate, interleaved conductive gate lines and insulating layers, and dummy components. *Id.*, 1:39-59. Park also teaches the use of common source lines 144 and dummy source lines 146 (i.e., dummy source

structures) to “improve[] structural and electrical reliability” issues. *Id.*, 1:37-38.

Figure 2 below shows a portion⁵ of Park’s exemplary three-dimensional memory device.

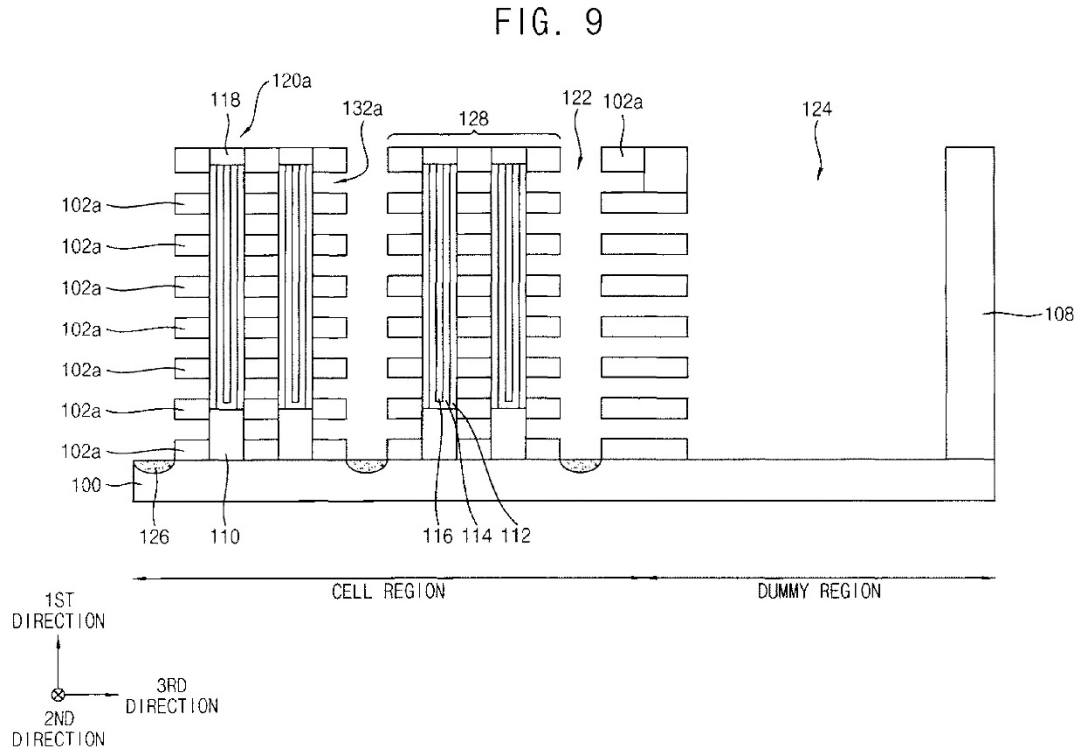


Id., Fig. 2.

Park teaches a method of forming a three-dimensional memory device, similar to the '872 Patent’s method, in which an interleaved insulating and sacrificial layer stack is first formed on the substrate, the stack including a cell region and a stepped dummy region. Park, 9:36-46 (discussing Fig. 5). First and second openings (122,

⁵ “FIG. 2 is an enlarged perspective view of a portion ‘A’ in FIG. 1.” Park, 5:48-51.

124) are etched in the insulating/sacrificial layer stack during the gate replacement process. *Id.*, 11:66-12:4. The first opening 122 is formed in the cell region and the second opening 124 is formed in the dummy region.



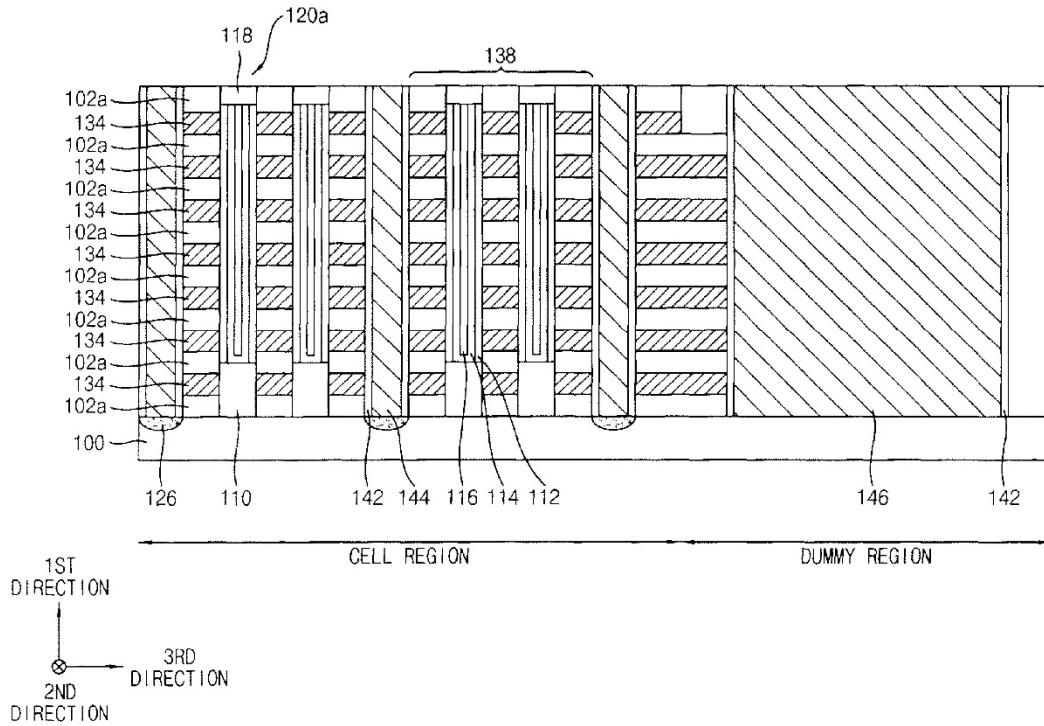
Id., Fig. 9.

The first and second openings (122, 124) are just like the '872 Patent's dummy source holes. Banerjee, ¶¶ 101-07. Specifically, these openings allow for the etching and deposition steps that replace the sacrificial gates. Park, 12:44-13:13.

After the gate replacement process, an insulation layer is formed on the sidewalls of the first and second openings (122, 124), and a conductive layer fills the rest of the opening to form a common source line and dummy source line (144 and

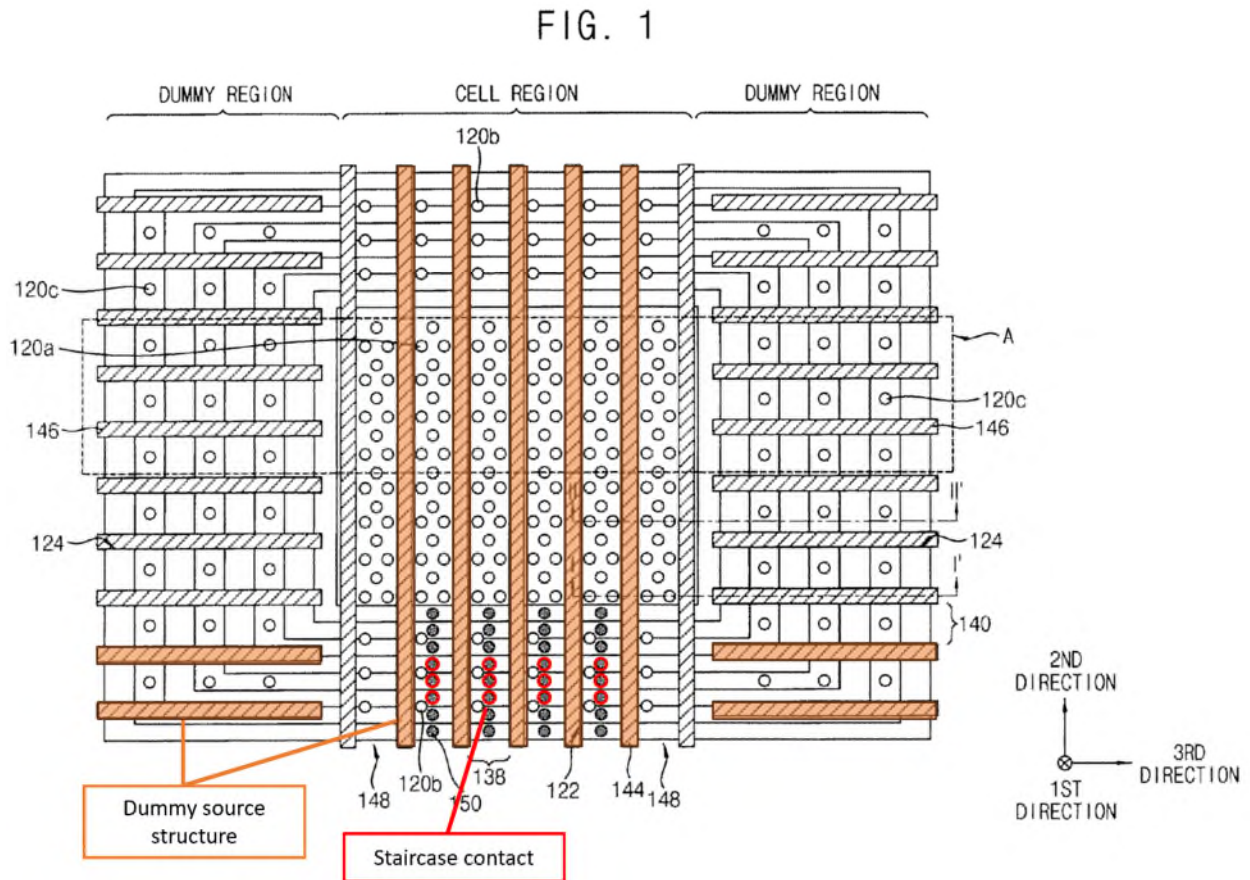
146, respectively). Park, 7:63-64 (“The CSL 144 may be in the first opening 122...”); 13:42-59; 14:67-15:2 (“The dummy source line 146a may be disposed in the second opening 124a...”).

FIG. 13



Id., Fig. 13.

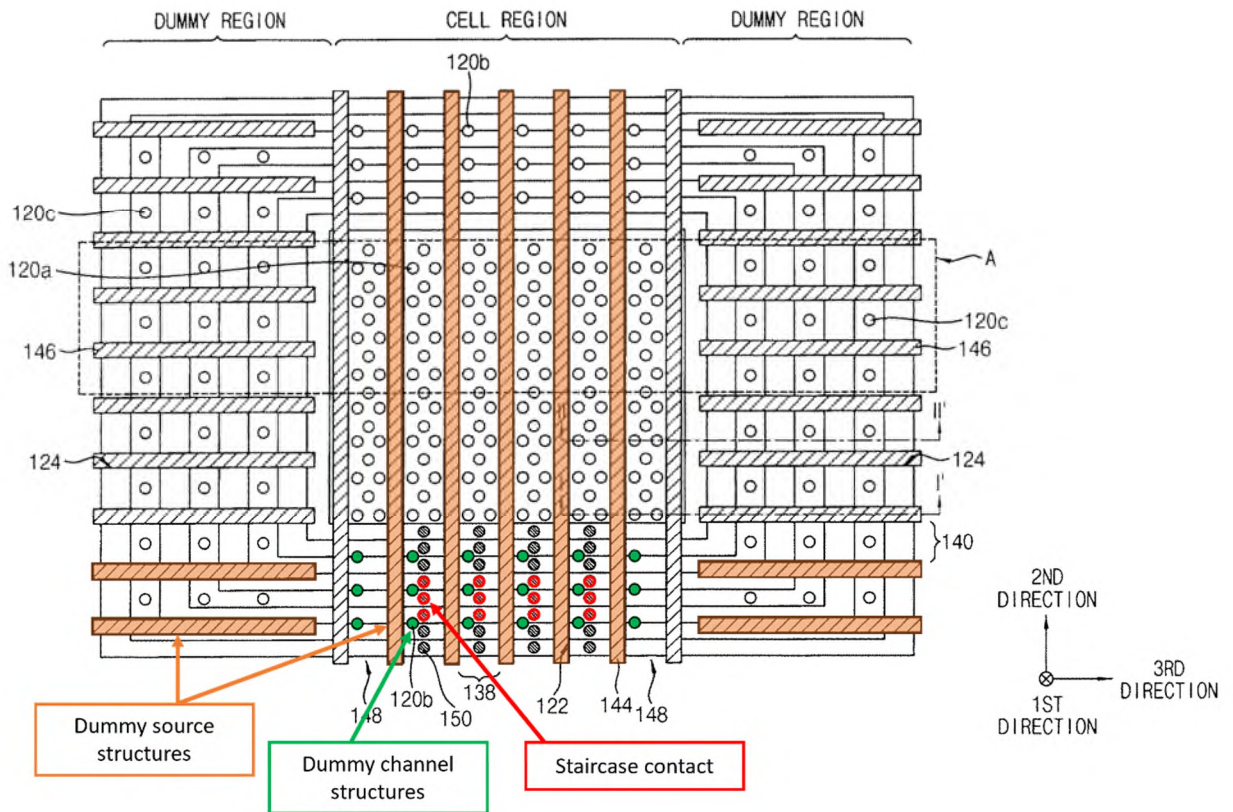
As shown below, the common source lines 144 (shown in orange in the first figure) and dummy source lines 146 (shown in orange in the second figure) surround the staircase contacts:



Park, Fig. 1 (annotated); Banerjee ¶¶ 108-09.

Park discloses *dummy channel structures* 120b that also surround the staircase contacts.

FIG. 1



Park, Fig. 1; Banerjee ¶ 110.

Structures 120b are *channel structures*. Park, 6:19-26 (“The first and second channel structures 120a and 120b may each include a semiconductor pattern 110, a channel layer 114 extending from a top surface of the semiconductor pattern 110 in the first direction, a dielectric layer structure 112 surrounding an outer sidewall of the channel layer 114, a filling pattern 116 in the channel layer 114, and a pad 118 disposed on the dielectric layer 112, the channel layer 114, and the filling pattern 116.”). And structures 120b are *dummy structures*. *Id.*, 7:45-51 (“A plurality of the second channel structures 120b may not be in contact with the wirings, or may be

spaced apart from the wirings.”). Specifically, structures 120b are not operable, and thus dummies, because they are not connected to the wiring. *Id*; Banerjee ¶¶ 111-12

Park does not limit the arrangement of the dummy channels 120b to any specific arrangement and makes clear that its figures are example embodiments. Park, 7:47-51 (“The second channel structures 120b may have an arrangement different from that of the first channel structures 120a. In example embodiments, a density in a unit area of the second channel structures 120b may be less than that of the first channel structures 120a.”); Banerjee ¶ 113.

X. GROUND 1: CLAIMS 7-10 ARE OBVIOUS OVER PARK

Park (Ex. 1005), when considered in view of the knowledge of a POSITA, renders claims 7-10 obvious. Banerjee ¶ 114. Claims 7-10 are dependent claims that depend on independent claim 1 and dependent claim 5.

A. Claim 1:

The figures from Park that are discussed below illustrate different views of a three-dimensional semiconductor device, and the manufacturing stages of the device. Figures 1-4 show different views (top plan view, perspective view, and cross-sectional views) of a three-dimensional semiconductor device, in which memory cells are formed on the top surface of a substrate. Park, 5:46-51. Figures

5-13 show the various manufacturing stages involved in forming the semiconductor device depicted by Figures 1-4. *Id.*, 9:29-37; Banerjee ¶ 115.

1. [1.PRE] “A three-dimensional (3D) memory device, comprising:”

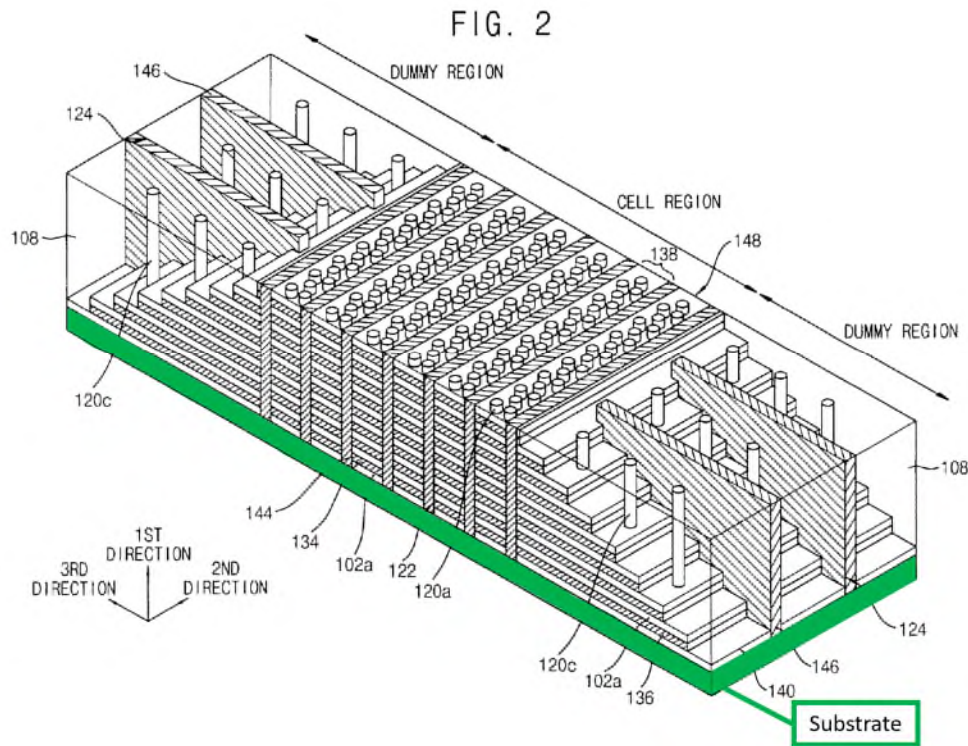
To the extent the preamble is limiting, Park discloses it. Specifically, Park discloses “[a] semiconductor device includes a substrate including cell and dummy regions ...” Park, Abstract. Park further discloses “[i]n example embodiments, a nonvolatile memory may be embodied to include a three dimensional (3D) memory array.” *Id.*, 23:13-22.

Thus, Park discloses *a three-dimensional (3D) memory device*⁶ (e.g., 3D semiconductor device with cell region). Banerjee ¶¶ 116-18.

2. [1.A] “a substrate;”

Park discloses this limitation. Specifically, Park discloses that “a semiconductor device may include a memory cell structure disposed on a cell region of a substrate 100.” Park, 6:1-4; *see also id.*, 23:15-22 (“[t]he 3D memory array may be monolithically formed on a substrate (e.g., semiconductor substrate such as silicon, or semiconductor-on-insulator substrate).”). This substrate is annotated in green below.

⁶ This Petition uses red and italics for claim language in the claim mapping portion for convenience of the Board.



Id., Fig. 2 (annotated), *see also* Fig. 3 (showing a cross-section view of Fig. 2 and depicting a “substrate 100”); Banerjee ¶¶ 119-21.

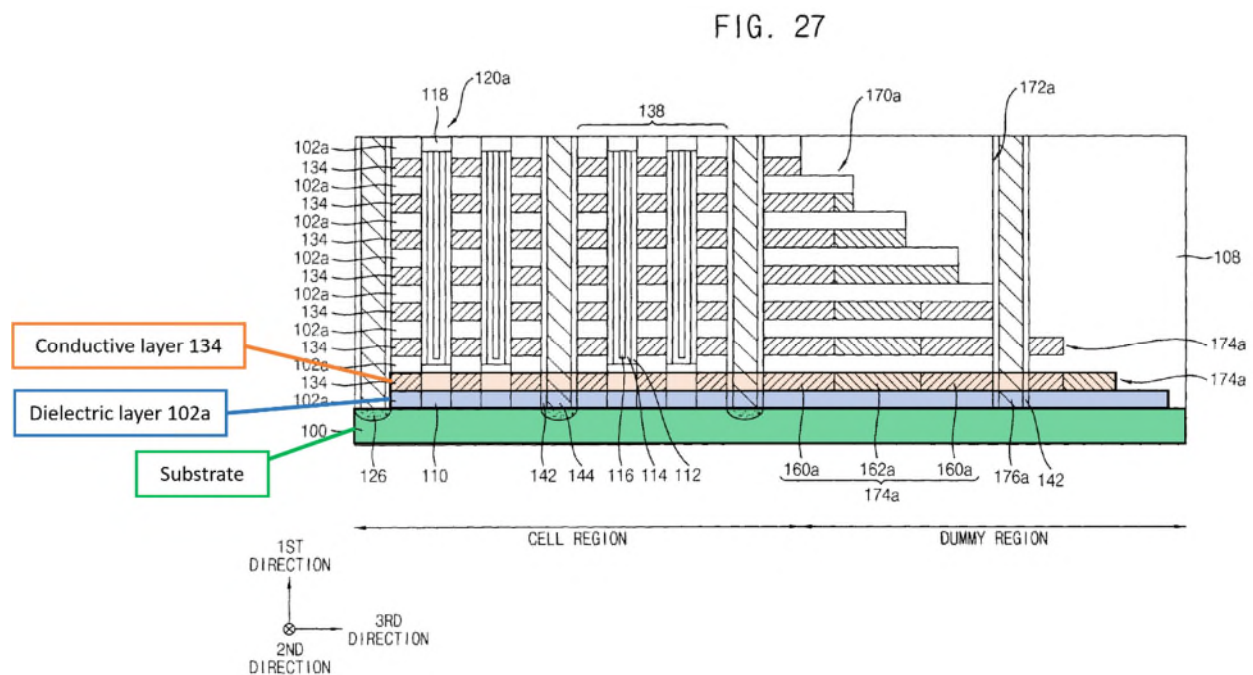
Thus, Park discloses a *substrate* (e.g., substrate 100).

3. [1.B] “a memory stack comprising interleaved conductive layers and dielectric layers on the substrate;”

Park discloses this limitation.

First, Park discloses conductive gate lines 134 that may include a metal, such as “tungsten (W), tungsten nitride, titanium (Ti), titanium nitride, tantalum (Ta), tantalum nitride, platinum (Pt), or the like.” Park, 7:6-10. Second, Park discloses that insulating interlayer patterns 102a are formed on the substrate 100, and act as an insulating layer between the gate lines 134, where the insulating layer 102a may

be “a silicon oxide-based material.” *Id.*, 7:19-22. Silicon oxide is a known dielectric. Banerjee ¶ 124. Third, Park discloses that these gate lines 134 (i.e., conductive layers) and insulating interlayer pattern 102a (i.e., dielectric layers) are alternately stacked or interleaved on the substrate. Park, 7:23-31 (“The insulating interlayer patterns 102a and the gate lines 134 may be alternately stacked...”). This memory stack is in the “cell region”:



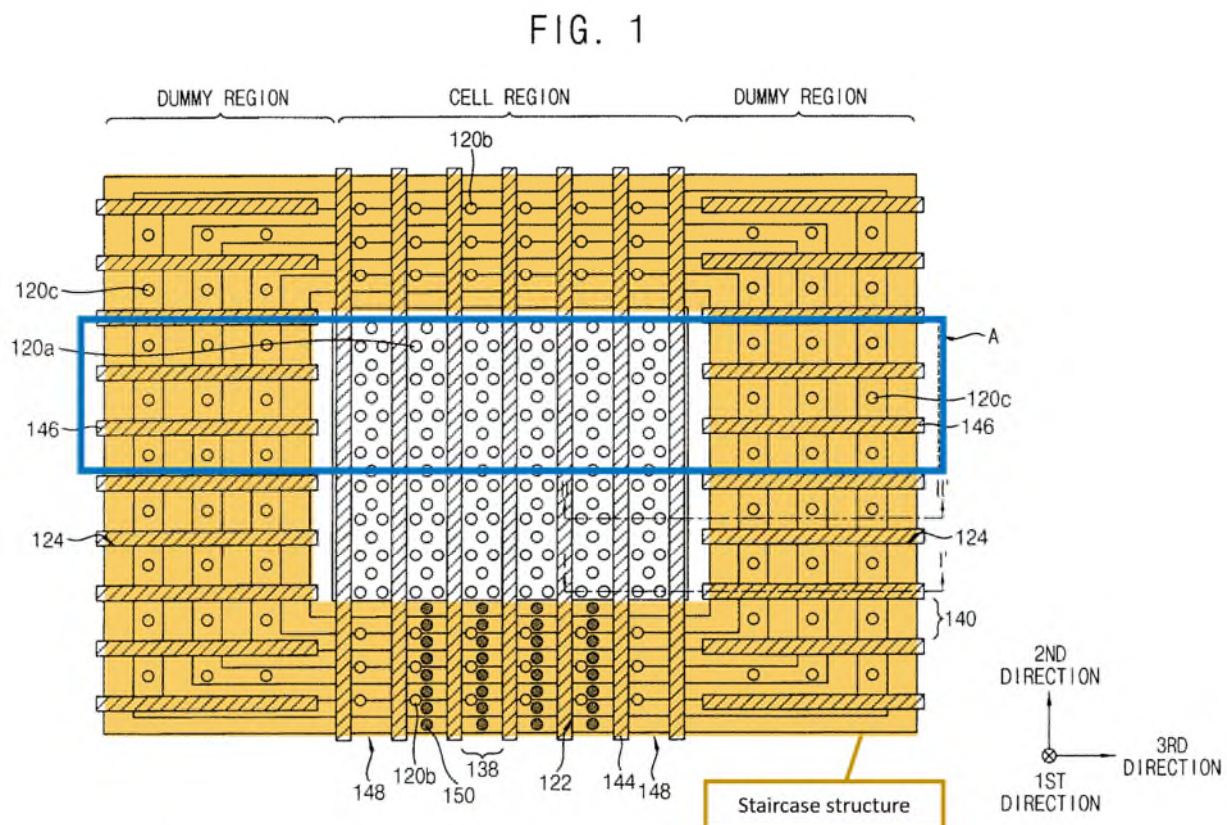
Id., Fig. 3; Banerjee ¶¶ 124-25.

Thus, Park discloses *a memory stack comprising interleaved conductive layers and dielectric layers on the substrate* (e.g., in the cell region, layers 102a and 134, which is a stack on substrate 100).

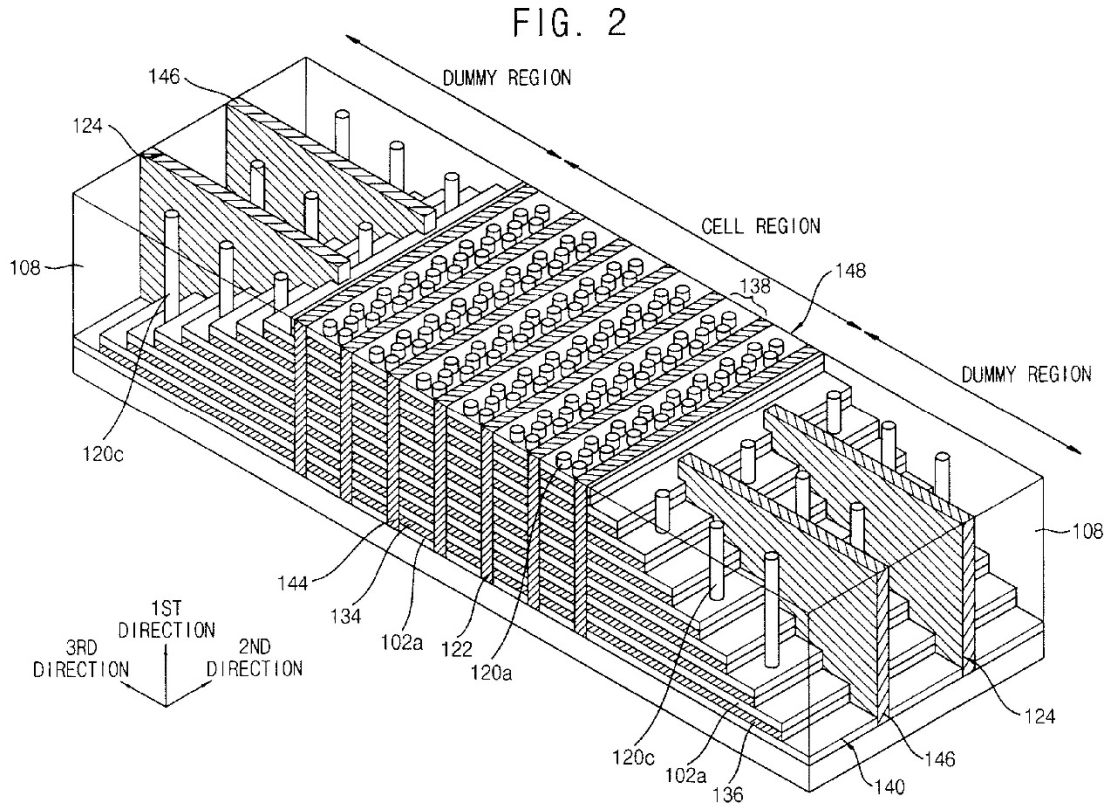
4. [1.C] “a staircase structure on one side of the memory stack;”

Park discloses this limitation.

As shown in limitation [1.B], Park discloses an interleaved stack of conductor/dielectric layer pairs in the cell region. For context, the complete view of Park’s device is shown in Figure 1 below:



Park, Fig. 1 (annotated). Park also discloses a cross section of area A of Figure 1 (shown above in the blue box) in Figure 2:



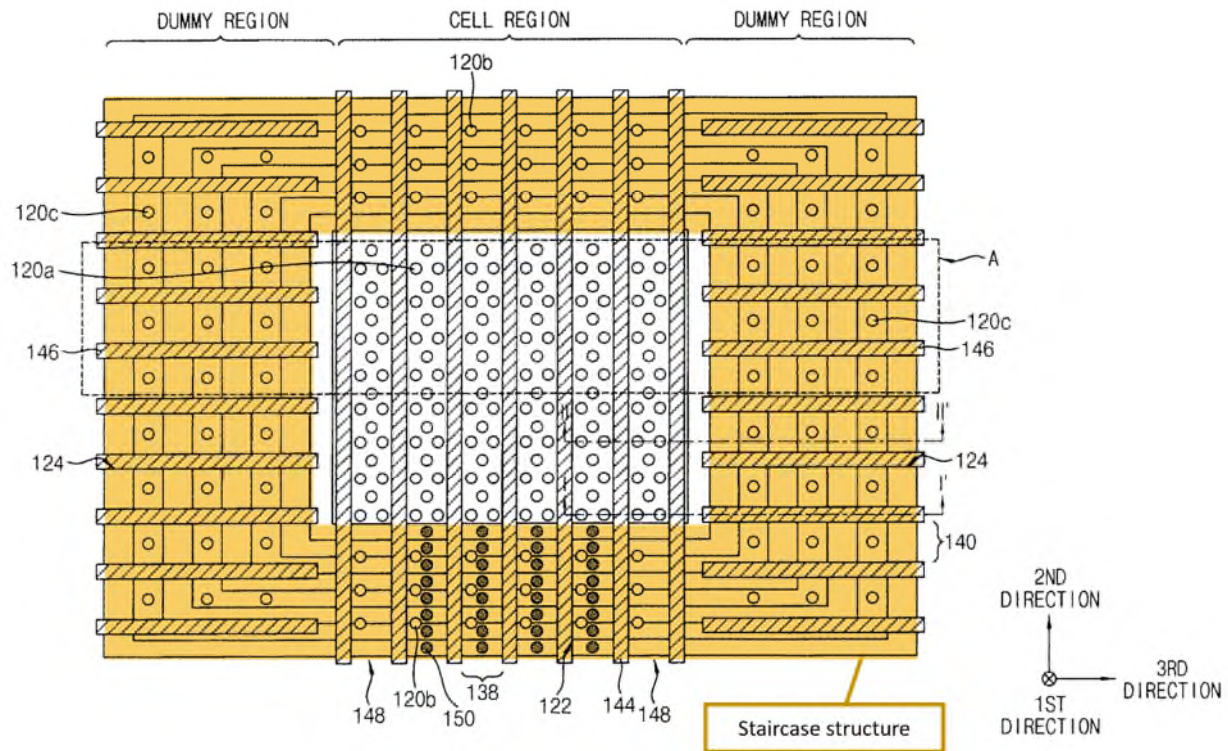
Id., Fig. 2, *id.*, 5:48-50 (stating Figure 2 shows area A of Figure 1).

As can be seen in the above figures, Figure 2 does not depict the regions with respect to the second direction, above and below the uncolored cell region in Figure 1. Park makes clear, however, that the staircase region is the entire orange-colored region in Figure 1 above and the “main cell region” is in the uncolored portion of Figure 1 above, which includes the active channel structures. Park, Fig. 2, 7:25-27, 9:43-46. First, in discussing the manufacturing of the stack, Park refers to the stack as “first structure 138.” *Id.*, 7:23-31. Park explains: “[t]he first structure 138 may extend in the second direction. Both lateral portions of the first structure 138 in the second direction may serve as a wiring region and have a stepped shape.” *Id.*, 7:25-

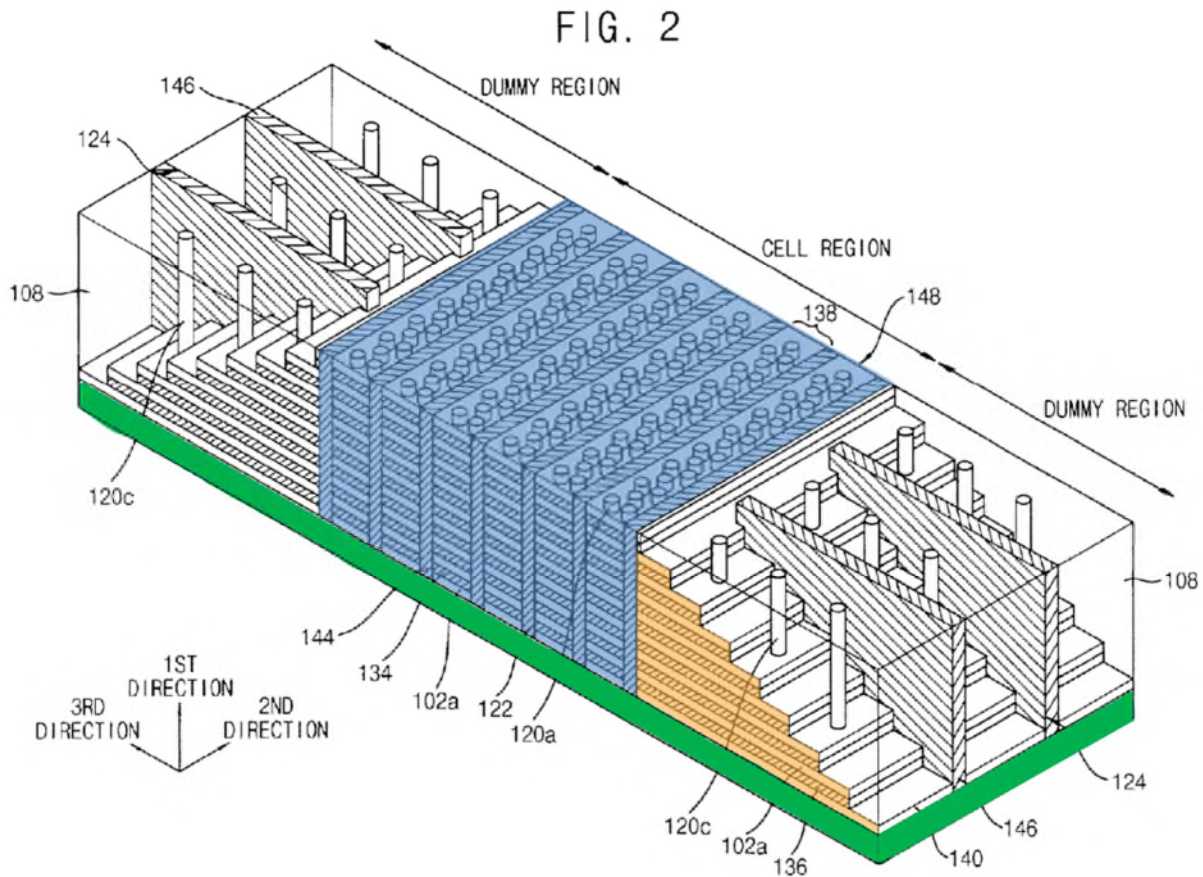
27. Further, “[a] central portion of the first structure 138 which may not have the stepped shape may serve as a main cell region, and the lateral portion having the stepped shape may serve as the wiring region.” *Id.*, 7:32-35. Second, in discussing the manufacturing of the stack, Park refers to the resulting structure after the gate replacement process as the “mold structure 106.” *Id.*, 9:38-46. Park explains that “[e]nd portion of the mold structure 106 in the second and third directions may have stepped structures.” *Id.*, 9:43-46. And Park explains again “[a] portion of the mold structure 106 on the cell region may include stepped structures at both end portions in the second direction.” *Id.*, 10:7-10. Third, as the analysis under limitation [1.D] demonstrates, the word line contacts, which extend down to steps of a staircase structure, are in the second direction of the main cell area. *Id.*, 7:32-37. Word line contacts extend to steps in a staircase region.

Accordingly, annotated Figure 1 below marks in orange all portions of the memory stack with a stepped shape – the lateral portions in the second direction and the dummy region in the third direction. Banerjee ¶¶ 128-34.

FIG. 1



Annotated Figure 2 below shows a perspective view of an exemplary “stepped structure” in the third direction, but as discussed above, such stepped structure exists in the second direction of the main cell (a portion of which is shown in blue below) region as well. Park, 5:48-49; Banerjee ¶ 135.



Park, Fig. 2 (annotated).

Thus, Park discloses *a staircase structure on one side of the memory stack* (e.g., the stepped regions on each side of the main cell region).

5. [1.D] “a staircase contact in the staircase structure; and”

Park discloses this limitation or at least renders it obvious.

As discussed in limitation [1.C], Park discloses a “staircase structure” in the second direction to the main cell region (as shown in yellow below, in the second direction with respect to figure 2), i.e., the wiring region. Park, 7:33-35. Park also discloses that, within the wiring region, there are interconnects to individual gate

lines: “[T]he lateral portion having the stepped shape may serve as the wiring region.

The wirings may include contact plugs 150 that may be in contact with gate lines

134, and conductive lines electrically connected to the contact plugs 150.” *Id.*, 7:32-

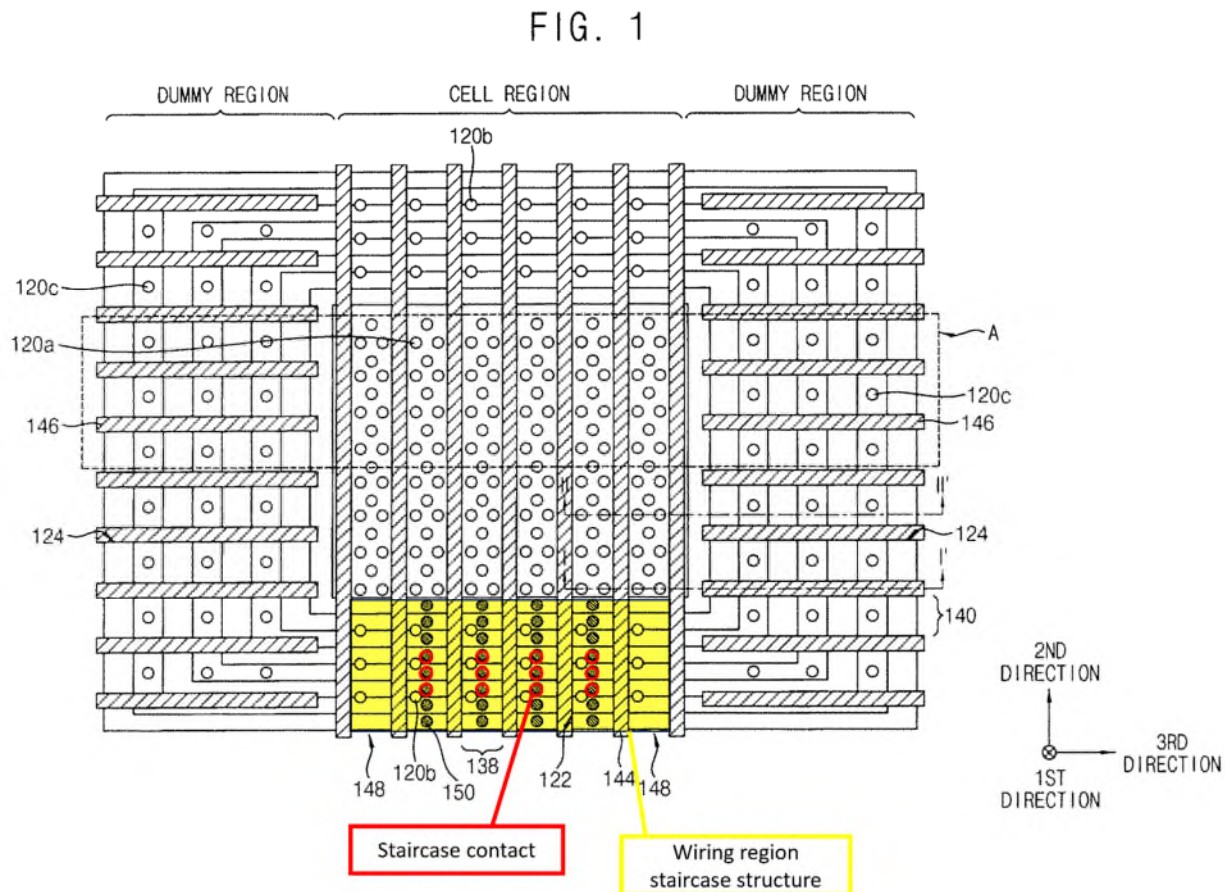
37 (emphasis added). In other words, in the staircase structure, there are *staircase*

contacts (contact plugs 150) that extend and contact the individual steps of the

staircase structure, thereby providing a connection to each gate line. Banerjee

¶¶ 138-39. Annotated Figure 1 below illustrates the contact plug 150 (in red) and

the wiring region (in yellow).



Park, Fig. 1, Banerjee ¶¶ 137-139.

To the extent that PO argues that Park does not disclose a staircase region in the main wiring area, it would have at least been obvious to have one. First, §X.A.4 illustrates that Park describes the wiring area under the main cell region as having a staircase region. Second, Park describes contacts to the gate lines in this region. A POSITA knew that the region that includes contacts to the gate lines is a staircase region. *See* §V. The staircase region beneficially provides landing pads for the gate line contacts. *Id.* And implementing such staircase regions, as Park shows in Figure 2, was routine. *Id.*; Banerjee ¶ 140.

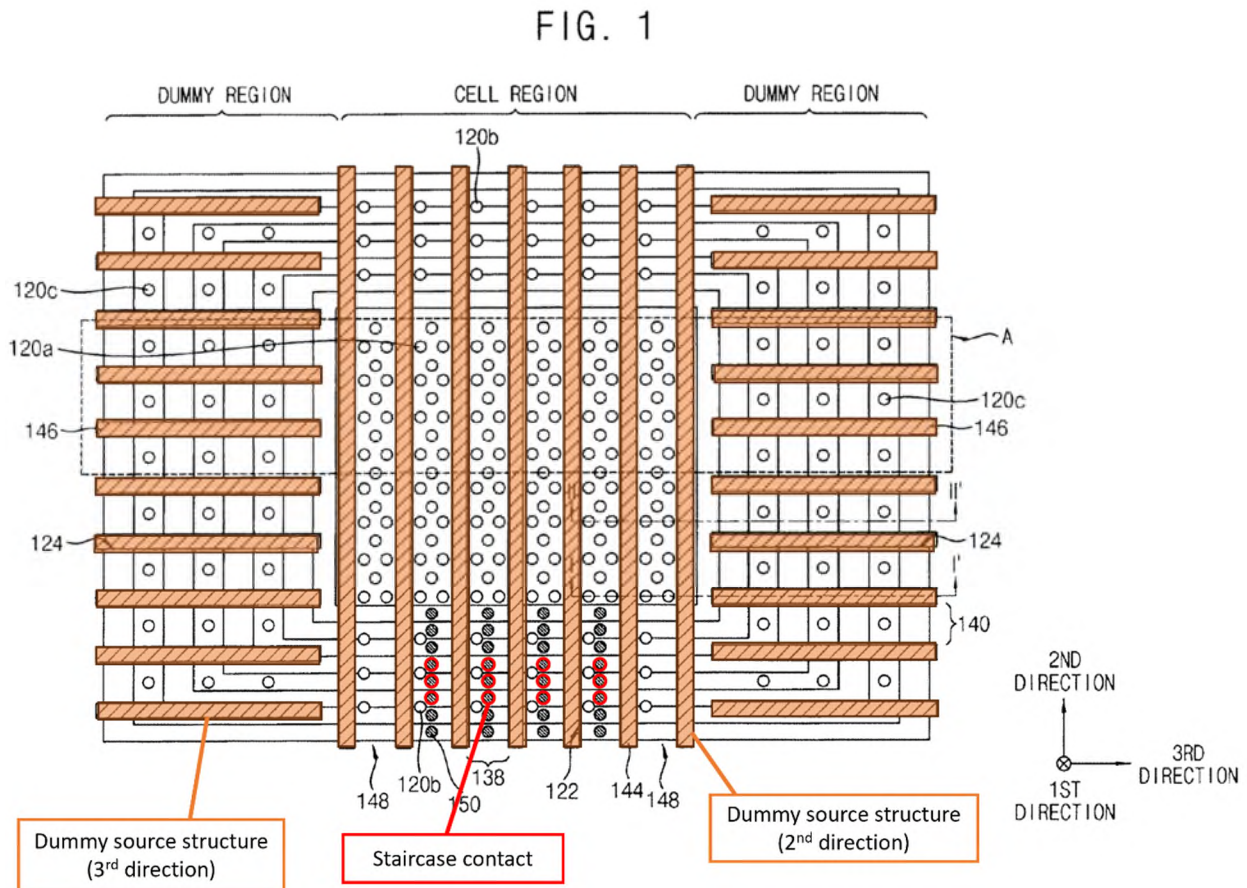
Thus, Park discloses, or renders obvious, *a staircase contact* (e.g., contact plug 150) *in the staircase structure* (e.g., step structure in wiring area).

6. [1.E] “a plurality of dummy source structures each extending vertically through the staircase structure, the plurality of dummy source structures surrounding the staircase contact,”

Park discloses this limitation under both parties’ constructions. Recall that Petitioner’s construction is “structure that occupies the void that was used for the gate replacement process” and PO’s apparent interpretation does not require that the structure occupy the void that is used for the gate replacement process. *See* §VII.A.

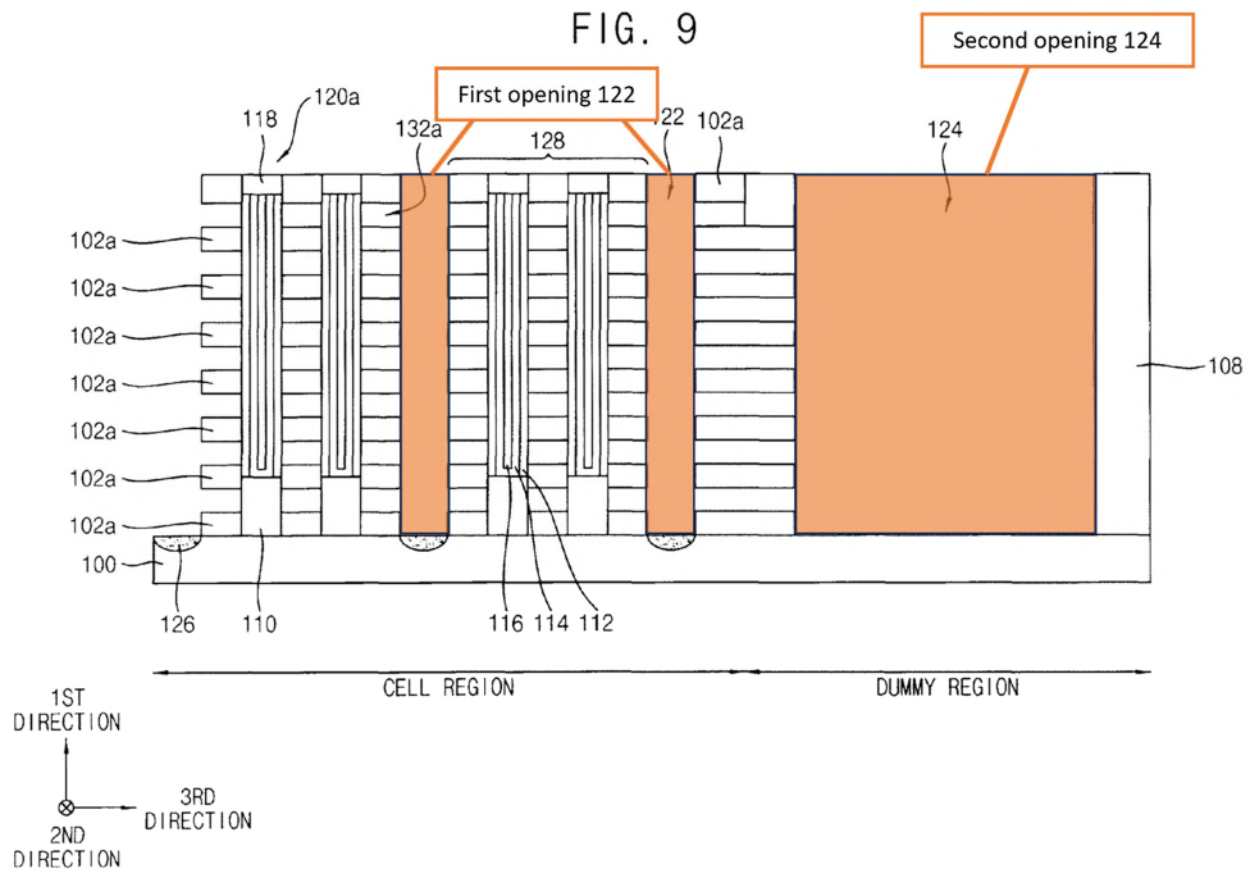
First, as to *a plurality of dummy source structures*, Park discloses common source lines 144 and dummy source lines 146, which are “structures that occupy the void that was used for the gate replacement process.” *See* VII.A. Annotated Figure

1 below shows, in orange, the position of the common source lines 144 and dummy source lines 146.



Park, Fig. 1 (annotated).

During the gate replacement process, first openings 122 and second openings 124 are etched in the insulating/sacrificial layer stack. Park, 11:66-12:4, Fig. 9. Annotated Figure 9 below shows the first openings 122 and second openings 124 after etching.

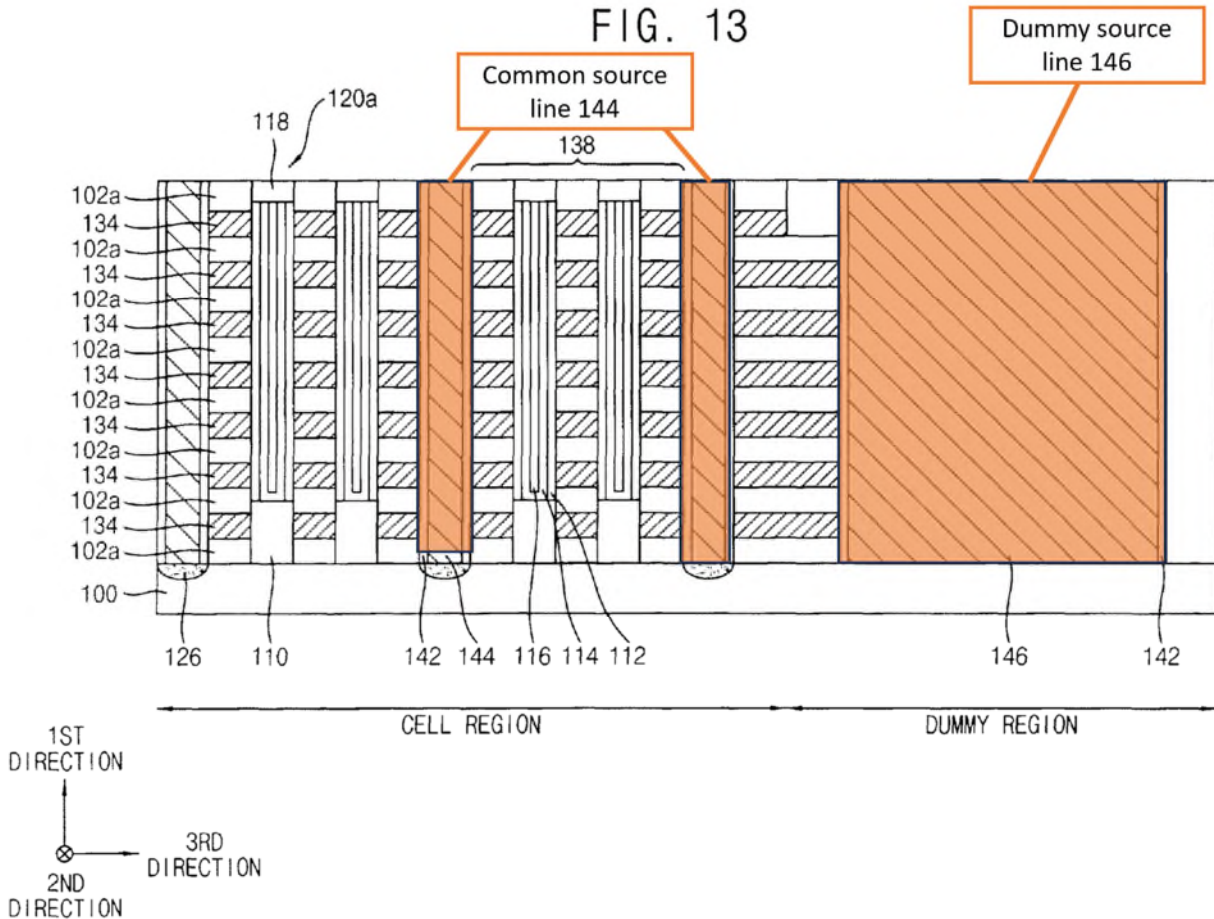


Id., Fig. 9 (annotated); Banerjee ¶¶ 144-45.

The first openings 122 and second openings 124 are the voids that are used for the gate replacement process. Specifically, the etch occurs through these voids: “[r]eferring to FIGS. 9 and 10, the sacrificial patterns 104a exposed through the first and second openings 122 and 124 may be removed to form first gaps 132a and second gaps 132b. In example embodiments, the sacrificial patterns 104a may be removed by a wet etching process using, e.g., phosphoric acid and/or sulfuric acid as an etchant solution. ... Referring to FIGS. 11 and 12, gate lines 134 may be

formed in the first gaps 132a, and dummy patterns 136 may be formed in the second gaps 132b.” Park, 12:44-13:5.

After the gate replacement process, the first opening 122 and the second opening 124 are each lined with an insulating layer and then filled with conductive material to form a common source line 144 and a dummy source line 146, respectively. Park, 13:39-41 (“The CSL 144 and the dummy source line 146 filling the first opening 122 and the second opening 124, respectively, may be formed”); *see also* 7:63-64 (“The CSL 144 may be in the first opening 122...”), 13:50-59 (same), 14:67-15:1 (“The dummy source line 146a may be disposed in the second opening 124a...”). Annotated Figure 13 below shows the filling of the first opening 122 and the second opening 124, in orange, with conductive material to form the common source line 144 and the dummy source line 146 (in orange).

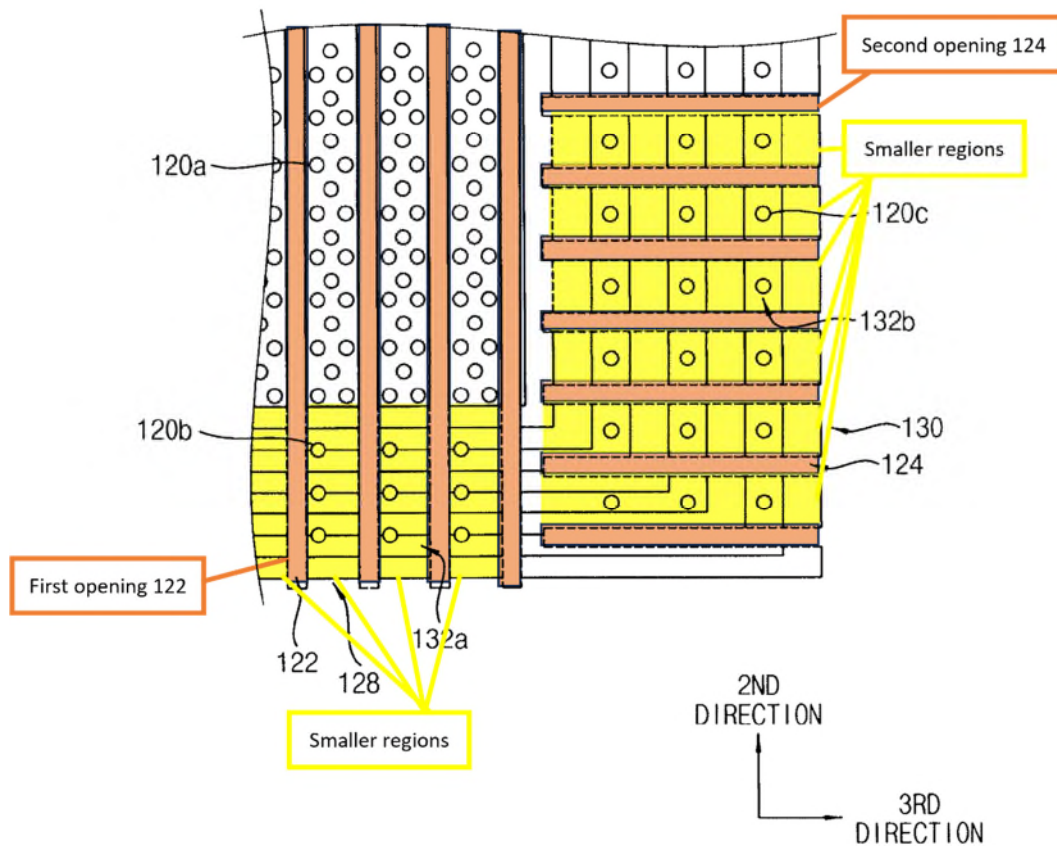


Id., Fig. 13 (annotated); Banerjee ¶¶ 146-48.

The '872 Patent describes almost identical *dummy source structures* to those of Park, i.e., Park's common source lines 144 and dummy source lines 146. Recall that the '872 Patent states that "dummy source structures 178 can laterally separate 3D memory device 100 into multiple memory regions, such as memory blocks." Ex. 1001, 11:44-46. Park's common source lines 144 and dummy source lines 146 do the same. Specifically, these structures may "cut" the stack. Park, 12:5-18; *see also* 6:15-18 ("The CSL 144 may extend through the gate lines 134, and may extend in

the second direction. The CSL 144 may serve as a cutting line intersecting the gate lines 134”); Banerjee ¶ 149. Annotated Figure 10 below shows that the first openings 122 and second openings 124 divide the staircase structure into smaller regions.

FIG. 10

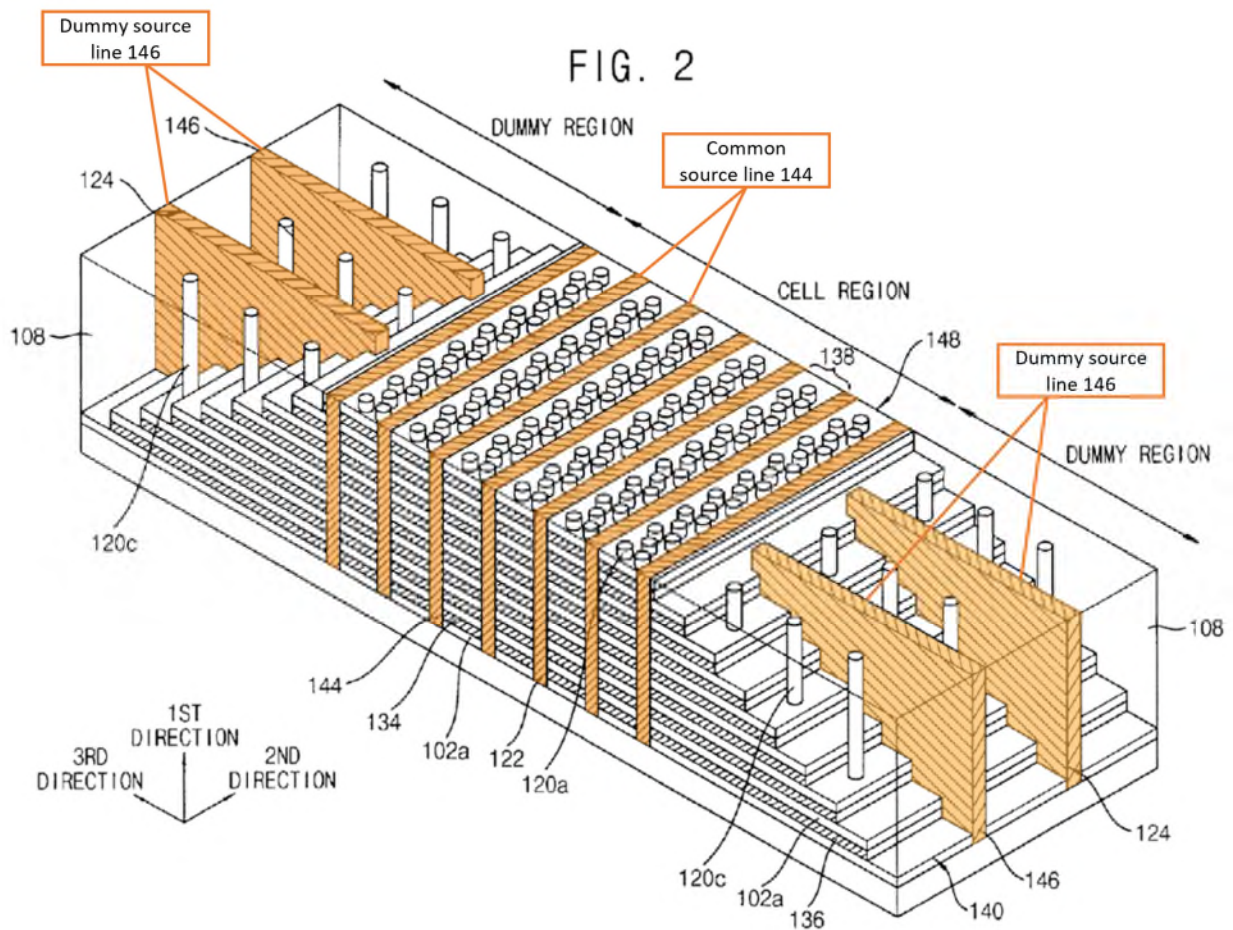


Park, Fig. 10 (annotated).

Further, recall that the '872 Patent explains that “dummy source structures” can “contact with the substrate and may provide interconnect between the 3D

memory device and peripheral devices.” Ex. 1001, 5:41-43, 16:63-66. Similarly, the common source lines 144 in Park are an interconnect for a source connection. Park, 7:63-64 (“The CSL 144 may be in the first opening 122...”); Banerjee ¶ 150. And unlike the gate line slits that the ’872 patent describes, which have an insulator material in them (Ex. 1001, 4:38-44), Park’s common source lines 144 and dummy source lines 146 have a conductive core. *See* §X.A.7.

Second, as to *each extending vertically through the staircase structure*, Park discloses that both the common source line 144 and dummy source line 146 extend vertically through the stepped region (i.e., “staircase structure”):

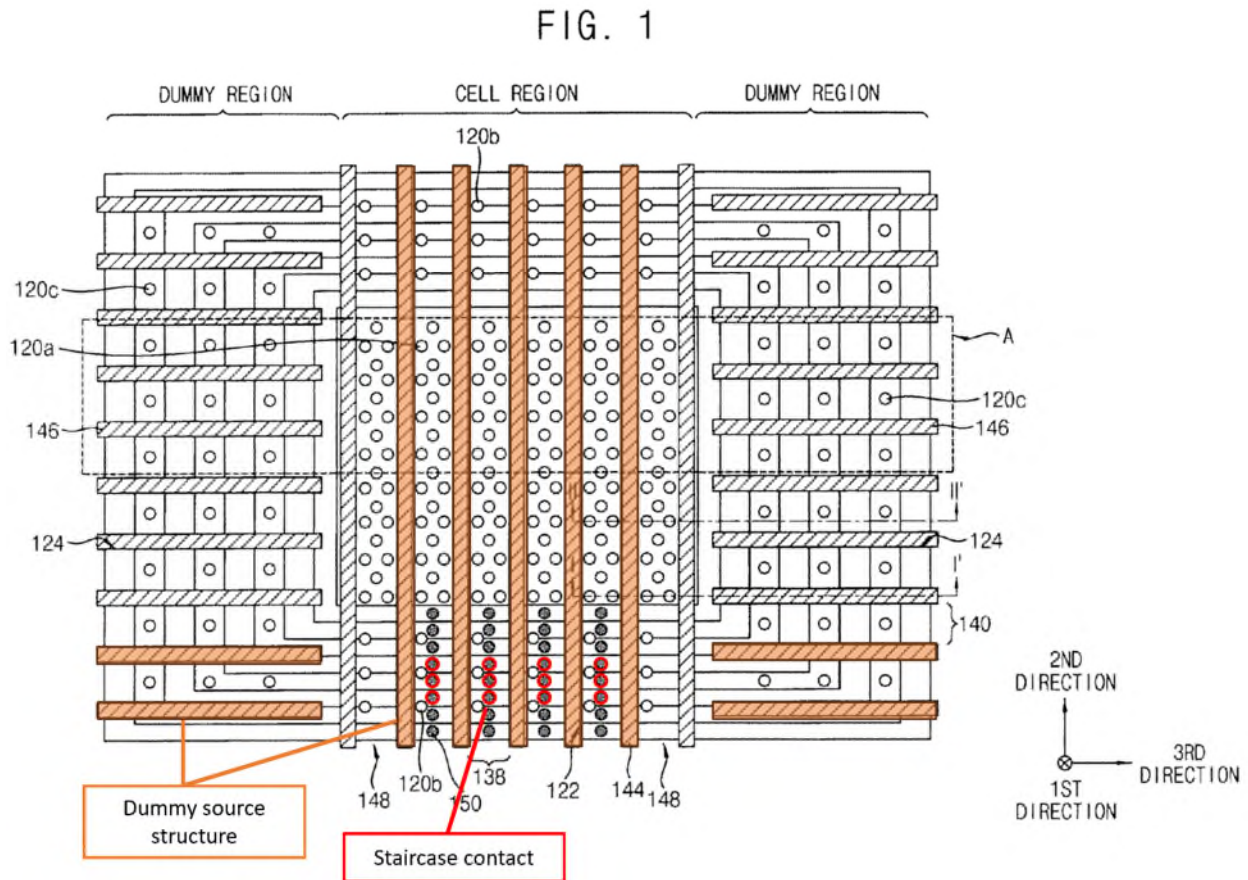


Park, Fig. 2 (annotated). All the embodiments in Park show common source lines 144 and dummy source lines 146 that extend vertically through the staircase structure. *See, e.g., id.*, Fig. 19, Fig. 21, and Fig. 26 (showing different embodiments of common source line 144 and dummy source line 146 configurations that all extend vertically through the staircase structure.). Specifically, these structures may “cut” the stack. Park, 12:5-18, *see also* 6:15-18; Banerjee ¶ 151.

Third, as to *the plurality of dummy source structures surrounding the staircase contact*, recall that the '872 Patent does not use “surround” to mean fully

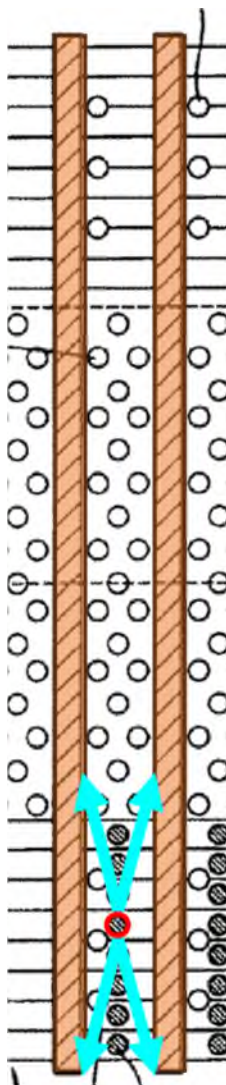
and continuously encircling, because in all embodiments, the dummy source structures do not do so. *E.g.*, Ex. 1001, Fig. 1A (dummy source structures 124 do not fully surround word line contacts 122); *see also* §VII.B. Instead, in every embodiment, there are large gaps between the dummy source structures.

As discussed under limitation [1.D], Park discloses a *staircase contact* (contact plugs 150). *See* [1.D]. As shown in the two annotated versions of Figure 1 below, the common source line 144 and the dummy source line 146 (*dummy source structures*) both surround the contact plugs 150 (i.e., *staircase contacts*). These *dummy source structures surround* the staircase contacts. Indeed, the common source lines 144 *surround* the *staircase contacts* alone. Banerjee ¶¶ 152-53.

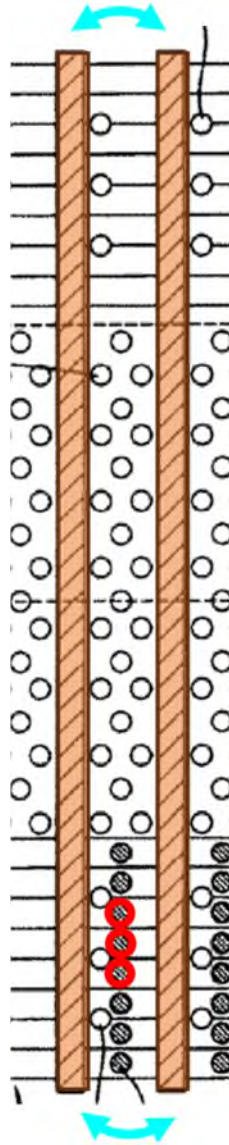


Park, Fig. 1.

Common source lines 144 alone surround the *staircase contacts*, and that is all that is necessary to satisfy claim 1. By way of example, two of the *dummy source structures surround* a *staircase contact* like the '872 Patent, namely, when drawing four lines (each equally radially spread out), each line will intersect one of the *dummy source structures*. See §VII.B. As shown below, when drawing such lines from the *staircase contact* at 45, 135, 225, and 315 degrees (or from a different orientation, at 0, 90, 180, and 270 degrees), each line intersects a *dummy source structure*:



By way of another example, as shown below, two of the *dummy source structures* create a larger angular border around the *staircase contact* than the '872 Patent creates with four *dummy source structures*. See §VII.B; Banerjee ¶¶ 154-56.



Were PO to argue that Park only discloses dummy source structures on two sides (which would be inaccurate, because in the above figure a line from the contact intersects a dummy source structure at four different angles separated by 90 degrees (e.g., 45, 135, and 225, and 315 degrees), the argument fails because an object may be surrounded by structures on two sides, just like an isthmus is surrounded on two

sides by water or like a nitride layer is surrounded on two sides by oxide layers in an ONO dielectric structure. Banerjee ¶ 157.

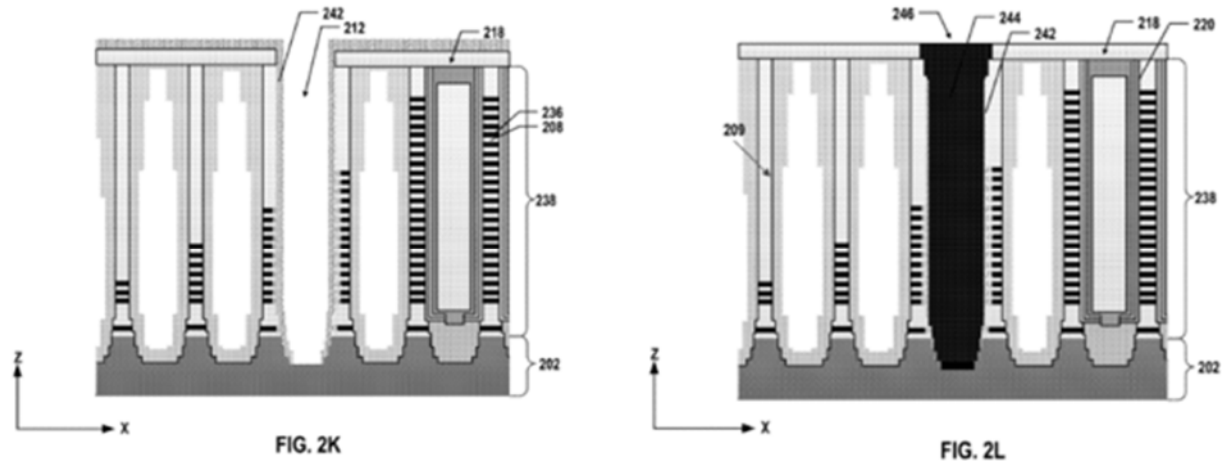
Thus, Park discloses *a plurality of dummy source structures* (e.g., common source lines 144 and dummy source lines 146) *each extending vertically through the staircase structure* (e.g., through the stairstep regions), *the plurality of dummy source structures surrounding the staircase contact* (e.g., contact plugs 150).

7. [1.F] “wherein each of the dummy source structures comprises a conductive contact.”

Park discloses this limitation.

As an initial matter, the '872 Patent provides as an example of a *contact* a uniform vertical conductive member that extends down towards the substrate, *i.e.*, *contact* need not be a separate element on top of a conductive member. The '872 Patent recites that “[a]s illustrated in FIG. 2L, *a contact 244* is formed within spacer 242 in dummy source hole 212 (shown in FIG. 2K). *Contact 244* can be formed by depositing conductive materials including, not limited to, W, Co, Cu, Al, polysilicon, silicides, or any combination thereof, over spacer 242 in the dummy source hole using one or more thin film deposition processes, such as ALD, CVD, PVD, any other suitable processes, or any combination thereof. *A dummy source structure 246 including spacer 242 and contact 244* is thereby formed in the dummy source hole, surrounded by a plurality of dummy channel structures 209.” Ex. 1001, 16:21-

32 (emphasis added). As shown below, the “contact” is simply a fill of conductive metal (246) into a hole (212) with an insulating liner (242):



Id., Figs. 2K, 2L; Banerjee ¶ 160.

In Park, each of common source line 144 and dummy source line 146, i.e., “dummy source structures”) comprises *a conductive contact*, namely, each includes conductive core that extend through the stack. See Park, 1:63-65 (“In example embodiments, the dummy lines may include a conductive material the same as that included in the cutting lines.”); 7:65-67 (“The CSL 144 may include a metal having a low resistance, e.g., W, Ti, Ta, Pt, etc...”); 3:23-24 (“The dummy source lines and the common source lines may include a same conductive material.”). See also Limitation [1.E] (describing the common source line 144 and dummy source line 146 “cut” through the stack); Banerjee ¶ 161.

Thus, Park discloses *wherein each of the dummy source structures comprises a conductive contact* (e.g., a metal or other conductive material).

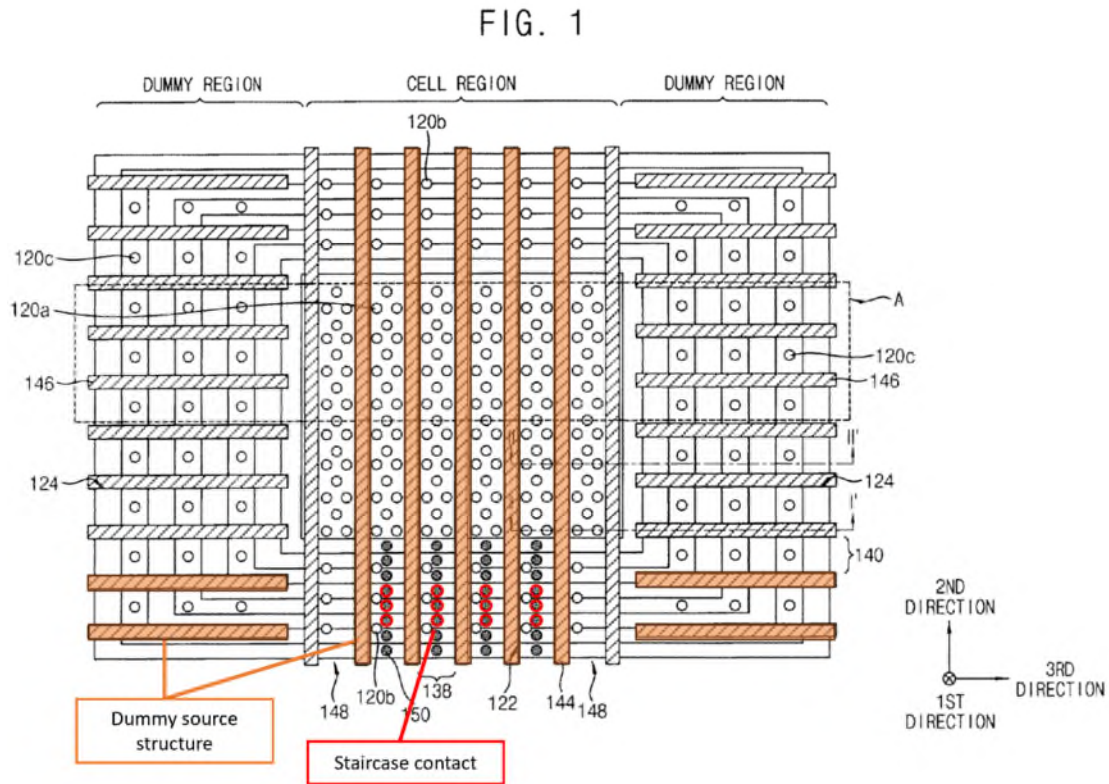
B. Claim 5:

1. [5] “The 3D memory device of claim 1, wherein in a plan view, at least two of the plurality of dummy source structures are arranged in a first row that extends along a first lateral direction.”

Park discloses this limitation.

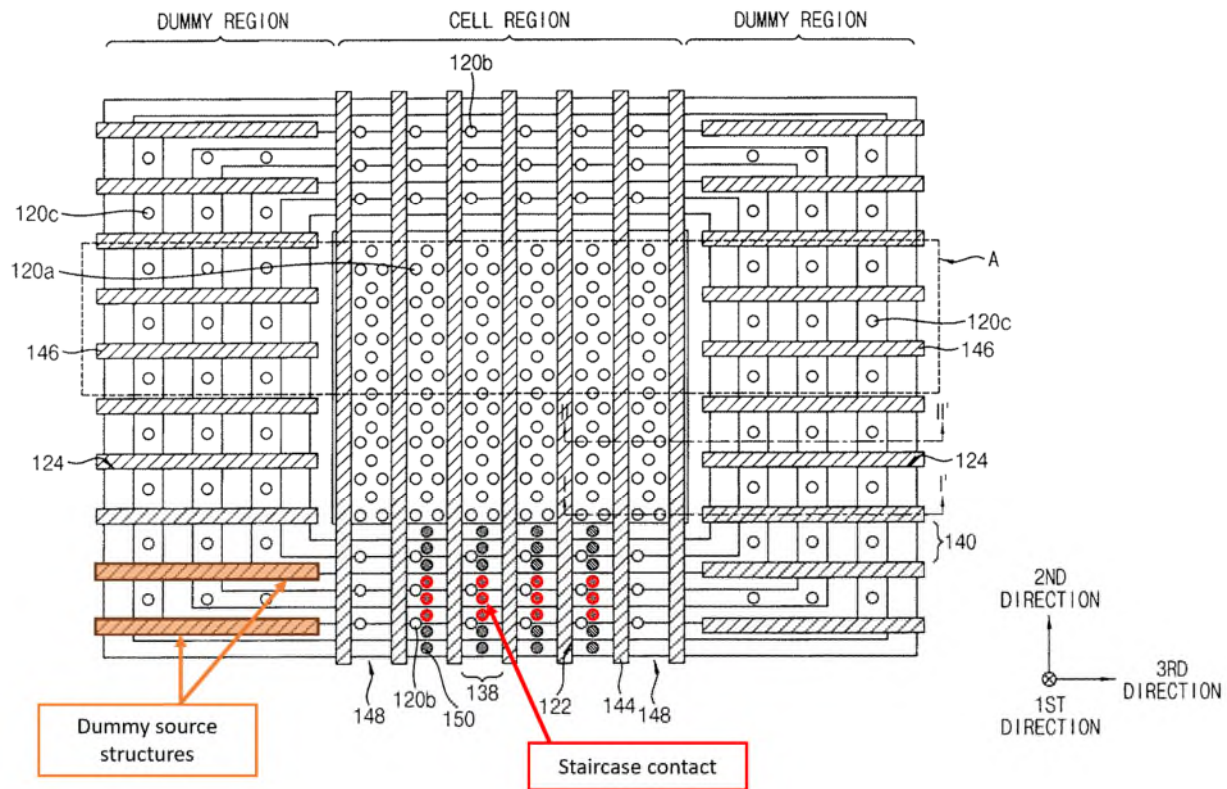
As claims 7-9 depend upon claim 5 and add additional limitations, this claim analysis presents two claim mappings (the first mapping is from the first wave petition and the second is unique to this second wave petition). For claims 7-10, the first mapping is relevant to 7, 9, and 10, and the second mapping is relevant to claims 7-10.

Under the first mapping, the *plurality of dummy source structures* (in orange) are shown in annotated Figure 1 below:



Park, Fig. 1. As shown in annotated Figure 1 below, there are *at least two of the plurality of dummy source structures* (in orange) arranged in *a first row that extends along a first lateral direction*. See Park, 26:26-29.

FIG. 1

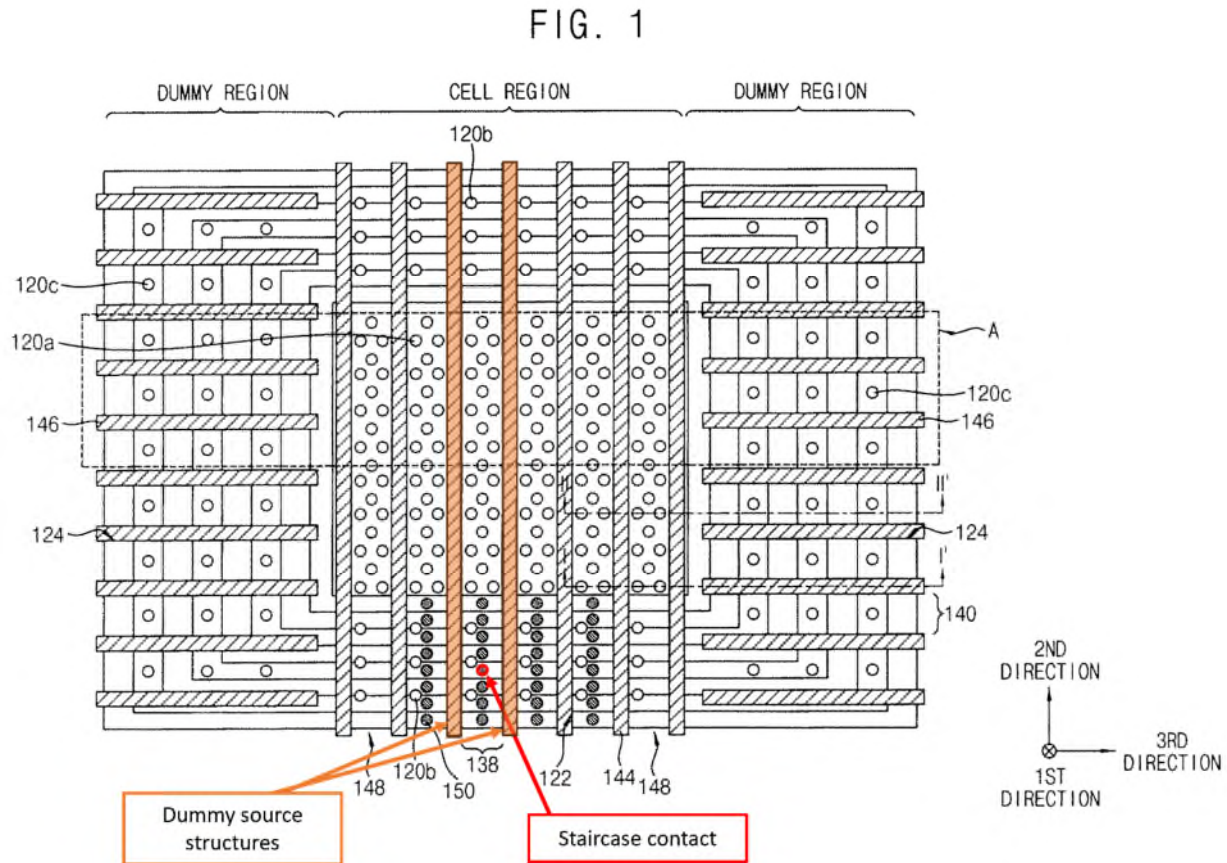


Id., Fig. 1 (annotated); Banerjee ¶¶ 164-66.

Note that a row is “a number of objects arranged in a usually straight line.” (<https://www.merriam-webster.com/dictionary/row>). The above row is like a row of match sticks going from north to south. Note that the *plurality of dummy source structures* includes all of the *dummy source structures* of Park such that they *surround the staircase contacts*. Banerjee ¶ 167.

Shown below is a second mapping in which *the plurality of dummy source structures* (in orange) are two *dummy source structures*, and there are *at least two of the plurality of dummy source structures* (in orange) arranged in *a first row that*

extends along a first lateral direction. See Park, 26:26-29. Here, the row is like a row of match sticks going from west to east.



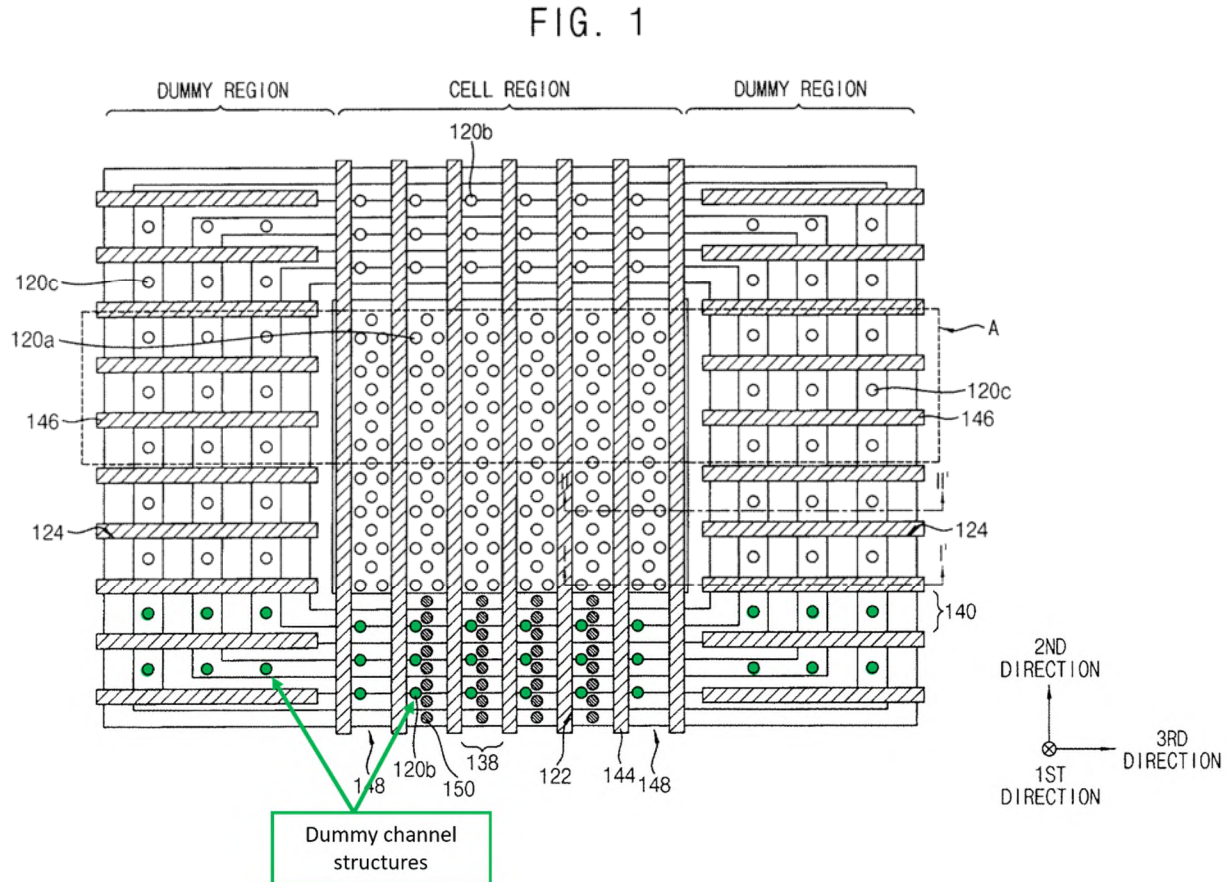
Id., Fig. 1 (annotated); Banerjee ¶ 169.

C. Claim 7:

1. [7] “The 3D memory device of claim 5, further comprising a plurality of dummy channel structures surrounding the staircase contact, each dummy channel structure extending vertically through the staircase structure.”

Park discloses, or at least renders obvious, this limitation. This analysis applies both mappings in claim 5.

First, Park discloses *dummy channel structures* 120b (in the wiring region) and 120c (in the dummy region):



Park, Fig. 1; Banerjee ¶¶ 171.

Structures 120b are *channel structures*. Park, 6:19-26 (“The first and second channel structures 120a and 120b may each include a semiconductor pattern 110, a channel layer 114 extending from a top surface of the semiconductor pattern 110 in the first direction, a dielectric layer structure 112 surrounding an outer sidewall of the channel layer 114, a filling pattern 116 in the channel layer 114, and a pad 118

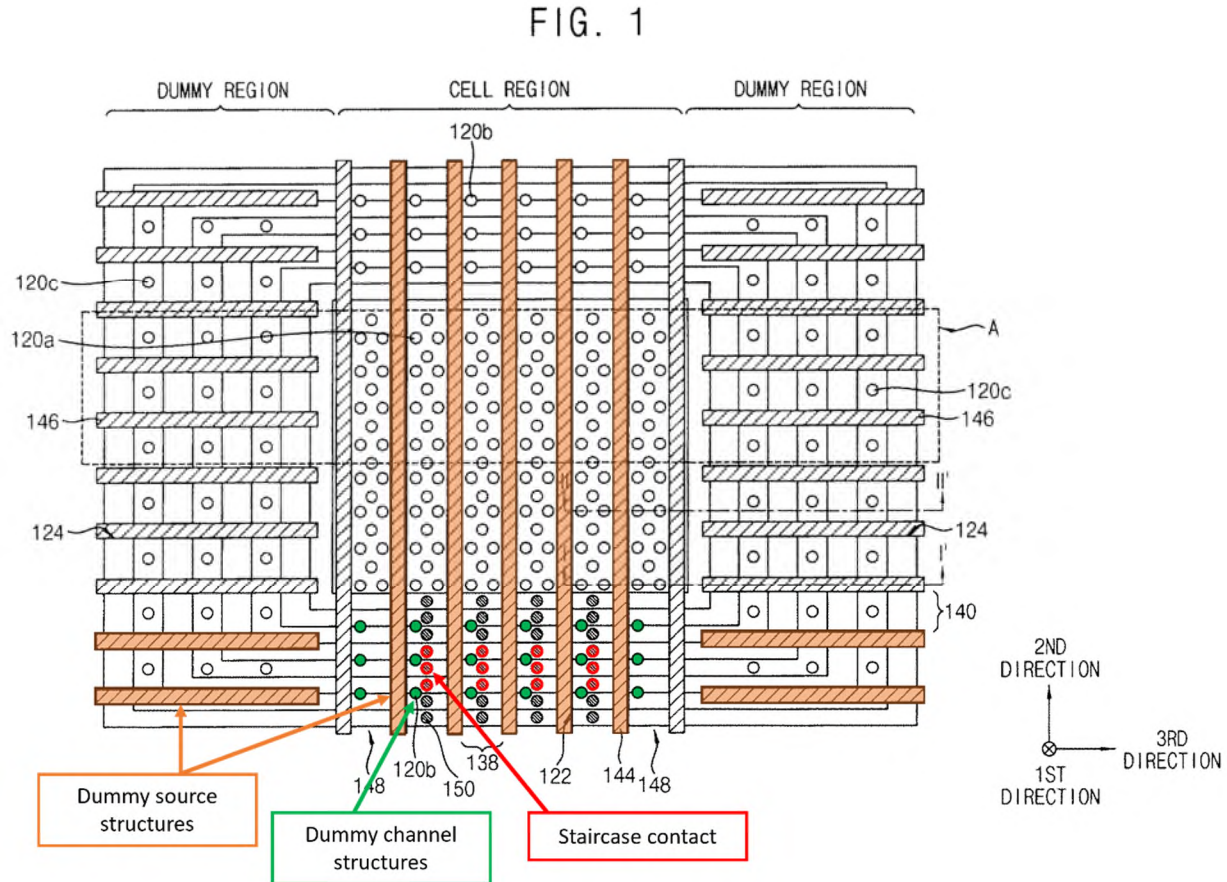
disposed on the dielectric layer 112, the channel layer 114, and the filling pattern 116.”); Banerjee ¶¶ 171-72.

Structures 120b are *dummy* structures. Park, 7:45-51 (“A plurality of the second channel structures 120b may not be in contact with the wirings, or may be spaced apart from the wirings.”); Banerjee ¶ 173. Specifically, structures 120b are not operable, and thus dummies, because they are not connected to the wiring. *Id.*

Structures 120b and 120c may be the same structures and thus the above analysis equally applies to 120c. Park, 8:55-65 (“A third channel structure 120c having a construction substantially the same as that of the first channel structure 120a may be disposed on the dummy region. The third channel structure 120c may not serve as a channel of the memory cell, and may merely serve as a supporting pillar of the second structure 140. A plurality of the third channel structures 120c may be provided in an arrangement different from those of the first channel structures 120a and/or the second channel structures 120b. In example embodiments, a density in a unit area of the third channel structures 120c may be less than that of the first channel structures 120a.”); Banerjee ¶ 174.

Second, Park’s *dummy channel structures* 120b *surround[] the staircase contact*. Under claim 5’s first mapping, for example, Park’s *dummy channel structures* 120b *surround[] the staircase contact[s]*. Also note that *dummy channel*

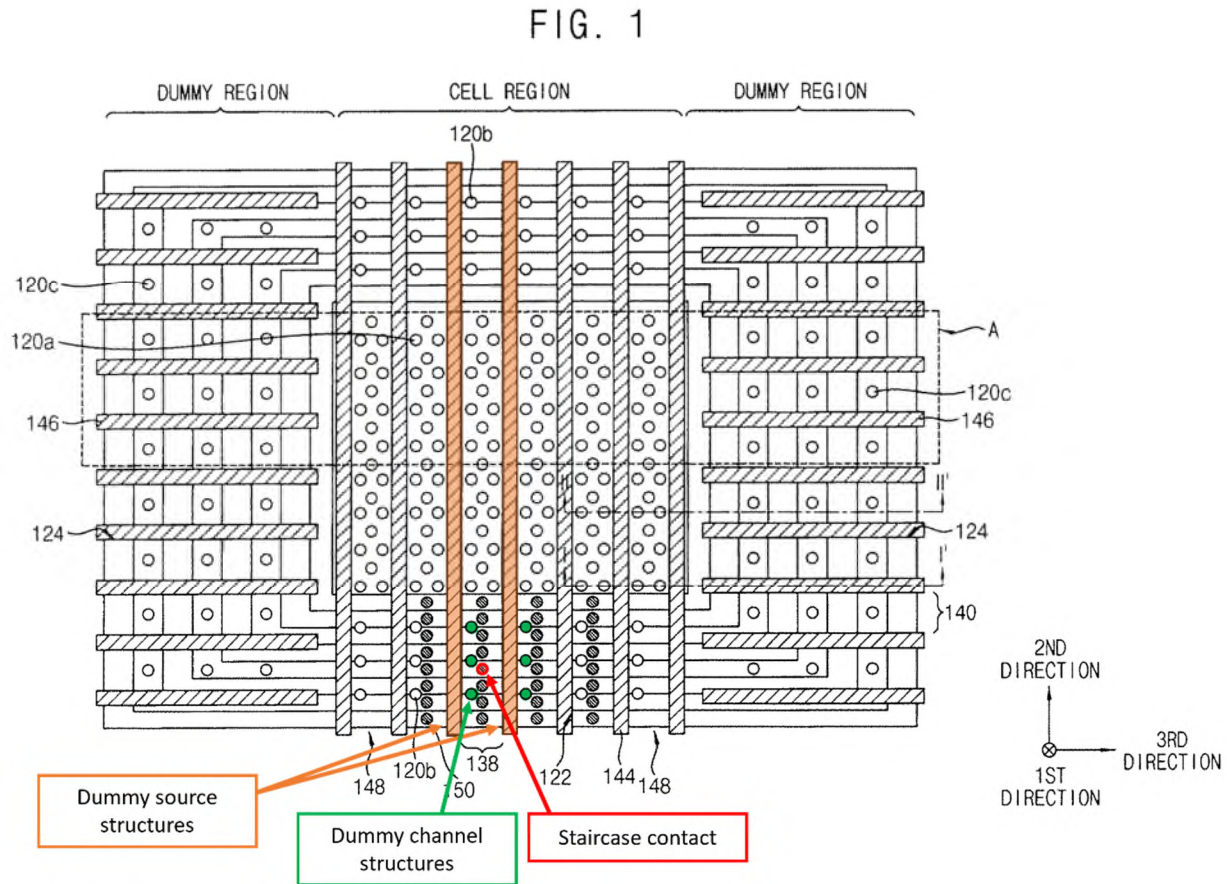
structures 120c shown above, together with the *dummy channel structures* 120b, likewise surround the staircase contacts.



Park, Fig. 1. By way of another example, *the staircase contact* may be one of the contacts in the middle of the wiring region (instead of all of them, as shown above). In this case, there are *dummy channel structures* 120b surrounding the *contact*. See §VII.B; Banerjee ¶ 175.

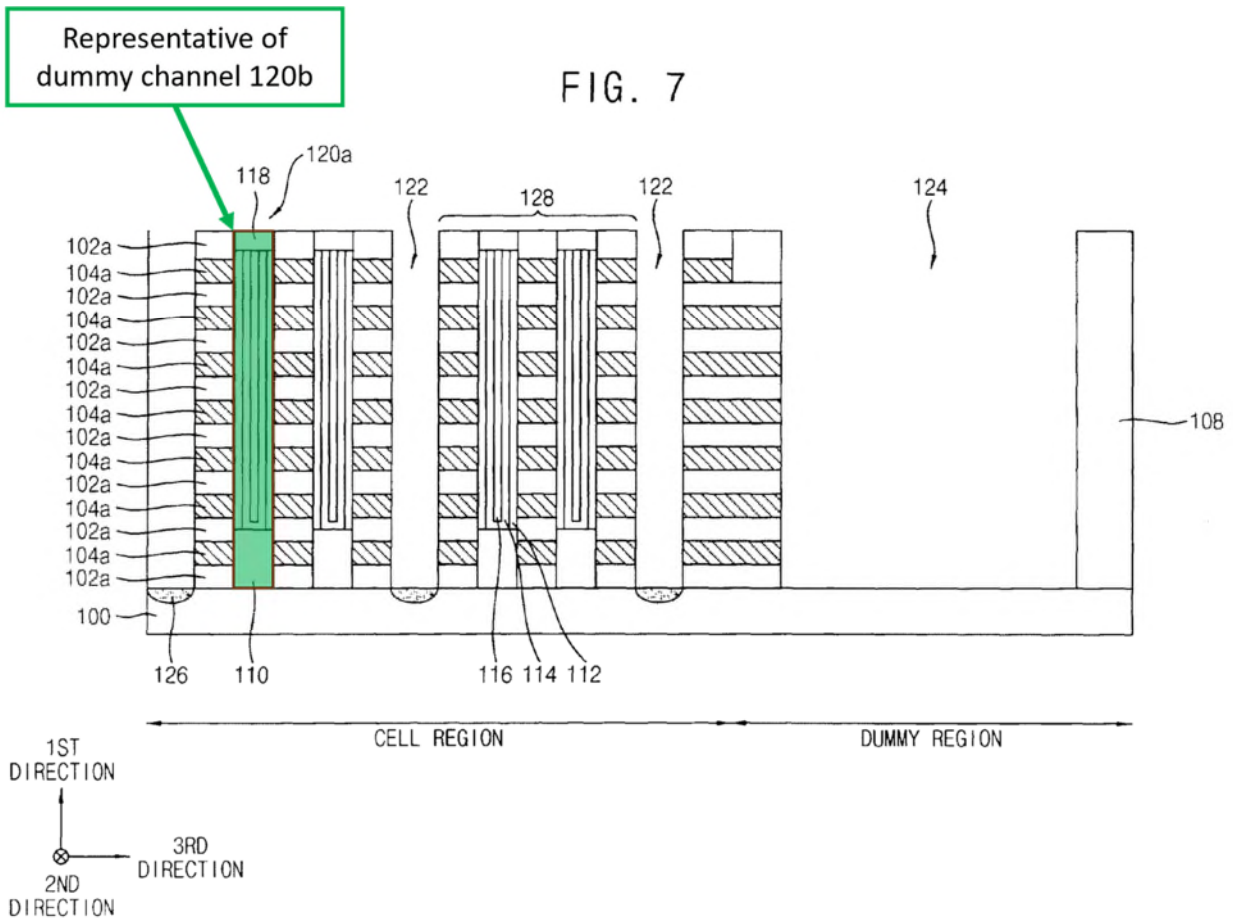
As §X.B discusses, a second mapping is *the plurality of dummy source structures* (in orange) are two *dummy source structures*, in which case there are *at least two of the plurality of dummy source structures* (in orange) arranged in a *first*

row that extends along a first lateral direction. See Park, 26:26-29. Here, the row is like a row of match sticks going from west to east. Further, *the dummy channel structures* (shown in green below) *surround the staircase contact.*



Id., Fig. 1 (annotated). Above, there is a *dummy source structure* between *the staircase contact* and certain *dummy channel structures*. Consistent with the plain claim language, PO agrees that *dummy channel structures* may *surround the staircase contact* even if there are *dummy source contacts* between *the staircase contact* and the *dummy channel structures*. Ex. 1026, 23; Banerjee ¶¶ 176-77.

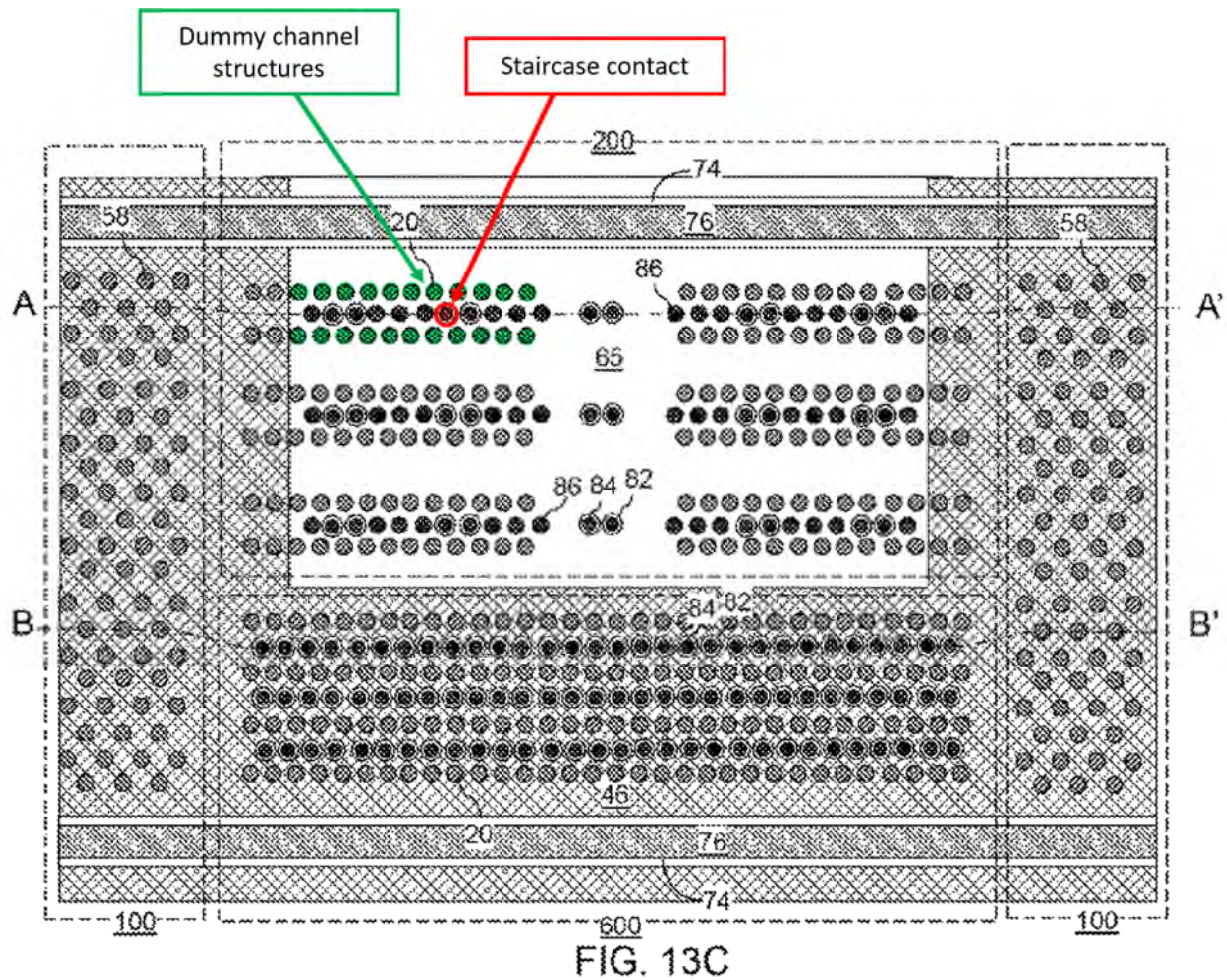
Third, Park's *dummy channel structures* 120b *extend[] vertically through the staircase structure*. Park, 15:26-32 ("Processes substantially the same as or similar to those illustrated with reference to FIGS. 5 and 6 may be performed to form a mold structure 106 on a substrate, and first to third channel structures 120a, 120b and 120c extending through the mold structure 106."). Note that Figure 6 only depicts 120a, though it has the same structure as 120b (except 120b are dummy channels that do not connect to wiring). *Id.*, 7:45-51; 11:59-65 ("The first to third channel structures 120a, 120b, and 120c may have substantially the same construction, while only the first channel structures 120a are illustrated in FIG. 6. The first channel structures 120a may substantially serve as a portion of the memory cells. The second and third channel structures 120b and 120c may serve as pillars supporting both portions of the mold structure 106."). The dummy channels 120b serve as support pillars. *Id.*; Banerjee ¶¶ 178-79.



To the extent that Patent Owner argues that the claim requires *dummy channel structures* directly on both sides of the staircase contact (without intervening *dummy source structures*), Patent Owner would be incorrect, because the claim includes no such limitation. And again, Patent Owner asserts in the district court litigation that the *dummy channel structures* can *surround* the *staircase contact* even if there are intervening dummy source structures between the dummy channel structures and staircase contacts. Ex. 1026, 19, 21, 23.

Regardless, Park in view of the knowledge of a POSITA renders obvious *dummy channel structures* directly on both sides of the staircase contact (without

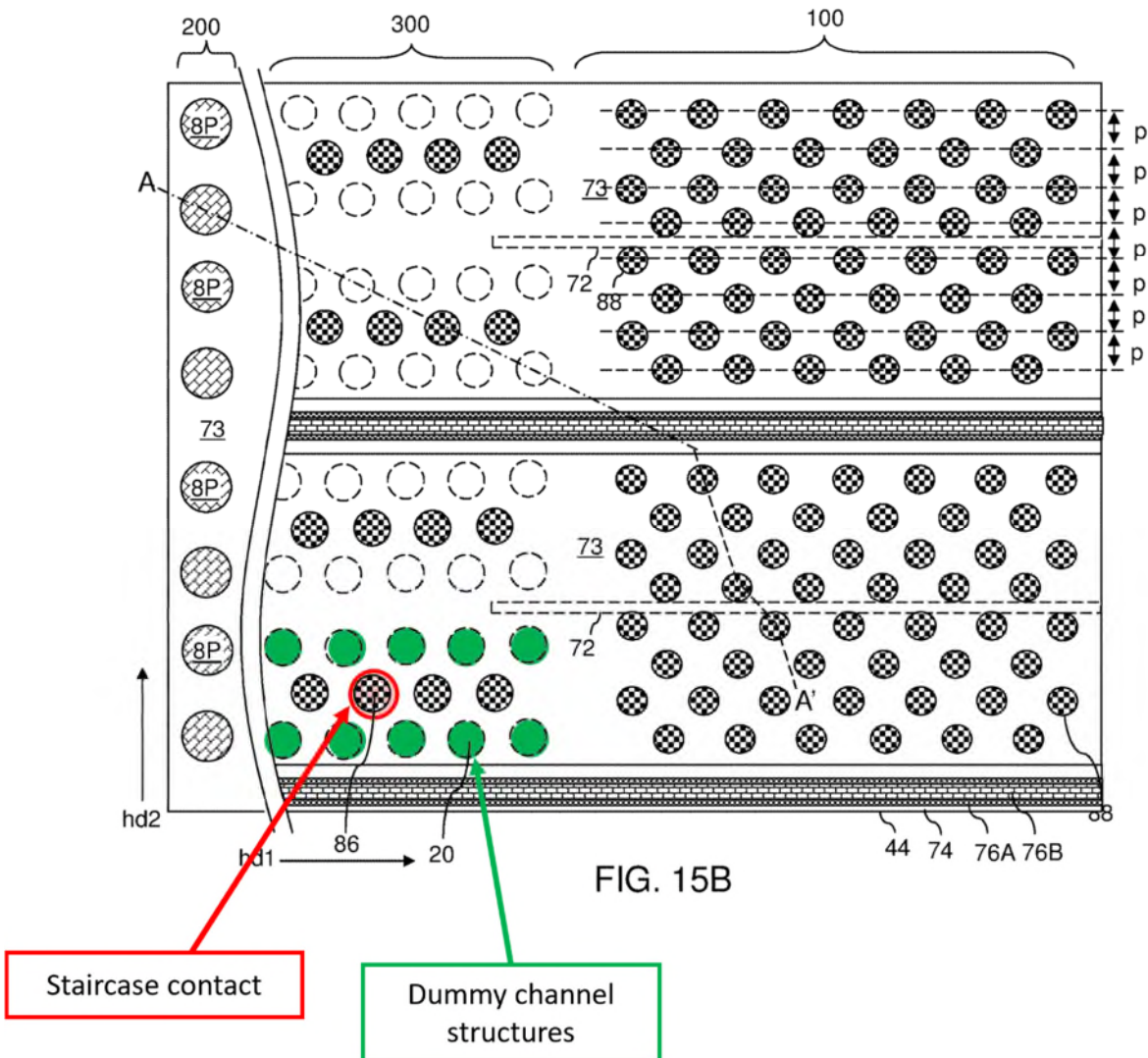
intervening *dummy source structures*). Banerjee ¶¶ 180-81. Park does not limit the arrangement of the dummy channels 120b to any specific arrangement and makes clear that its figures are example embodiments. Park, 7:47-51 (“The second channel structures 120b may have an arrangement different from that of the first channel structures 120a. In example embodiments, a density in a unit area of the second channel structures 120b may be less than that of the first channel structures 120a.”). Recall that *dummy channel structures* 120b are support pillars. *Id.*, 11:59-65. For example, these support pillar provide support during the sacrificial gate replacement process. *Id.*, 12:41-13:13. The knowledge of a POSITA includes lining each side of the staircase contacts with dummy support pillars, and more specifically, with *dummy channel structures* (just like structures 120b of Park). For example, Ogawa discloses support pillars 20 that surround staircase contacts 86 with rows of pillars 20 on each side of the contacts 86:



Ogawa, Fig. 13C (annotated); 20:4-24 (“A support pillar structure 20 formed in a word line contact via region 200 is illustrated in FIG. 7I. ... All of the support pillar structures 20 formed in connection regions 600 can extend through each layer within the alternating stack (32, 42), and does not contact any retro-stepped dielectric material portion 65.”), 28:22-24 (“The contact via structures (i.e., the word line contact via structures 86) can vertically extend through the retro-stepped dielectric material portion 65.”). Ogawa’s support pillar structures 20 are dummy channels. *Id.*, 13:51-14:61 (filling support openings 19, which become support pillars 20, with

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Kai discloses the same rows of dummy channel structures as Ogawa:

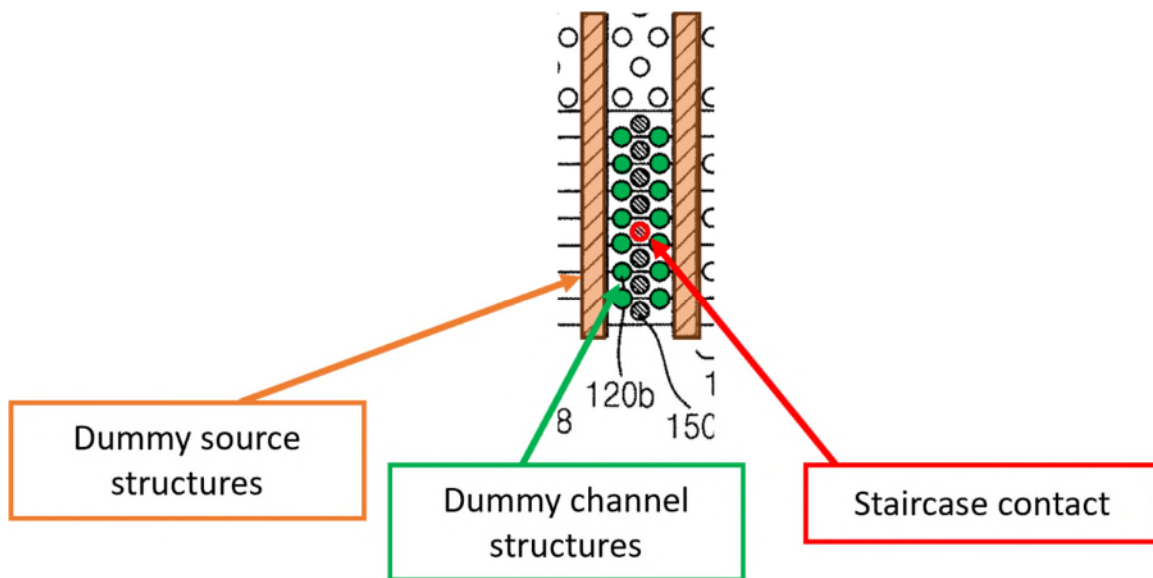


Kai, Fig. 15B.

In Kai, the staircase contacts are 86. Kai, 25:58-26:2 (“Referring to FIGS. 15A and 15B, additional contact via structures (88, 86, 8P) can be formed through the contact level dielectric layer 73, and optionally through the retro-stepped dielectric material portion 65. . . . Word line contact via structures 86 can be formed on the electrically conductive layers 46 through the contact level dielectric layer 73, and through the retro-stepped dielectric material portion 65.”). The dummy channel structures, which are support pillars and may extend through the stack, are 20. *Id.*, 16:29-39 (“Referring to FIGS. 6A and 6B, the exemplary structure is illustrated after formation of memory opening fill structures 58 and support pillar structure 20 within the memory openings 49 and the support openings 19, respectively. . . . An instance of the support pillar structure 20 can be formed within each support opening 19 of the structure of FIGS. 4A and 4B. The support pillar structures 20 can be formed through the retro-stepped dielectric material portion 65 in the terrace region.”), 9:45-48 (“The memory openings 49 and the support openings 19 can extend from the top surface of the alternating stack (32, 42) to at least the horizontal plane including the topmost surface of the semiconductor material layer 10.”), 16:13-27 (“Each combination of a memory film 50 and a vertical semiconductor channel 60 within a memory opening 49 constitutes a memory stack structure 55. . . . Each combination of a pedestal channel portion 11 (if present), a memory film 50, a vertical semiconductor channel 60, a dielectric core 62, and a drain region 63 within each

support opening 19 fills the respective support openings 19, and constitutes a support pillar structure 20.”); Banerjee ¶¶ 183-84.

Accordingly, in view of Park’s non-limiting disclosure of *dummy channel structures surrounding the staircase contact[s]* (see Park, 7:47-51) and the knowledge of a POSITA that such dummy channel structures may be formed in rows that surround the staircase contact (see Ogawa and Kai disclosures above), it would have been obvious that Park’s *dummy channel structures* 120b could be two rows on each side of the staircase contact:



Park, Fig. 1 (modified). The above provides an example of two rows—one on the left and one on the right—of an exemplary staircase contact. Banerjee ¶¶ 185-86. Under both mappings of claim 5, when *the dummy channel structures* are the above rows, the *dummy channel structures surround the staircase contact[s]*.

There are several advantages to including the additional rows of dummy channel structures in Park. Banerjee ¶ 187. First, the additional dummy structures would have been understood to provide additional support. For example, Masamori discloses that adding additional dummy channels “provide[s] additional structural support during replacement of the [sacrificial gate layers].” Ex. 1027, 30:14-27; *see also id.*, 15:3-22 (structures 20 are dummy channel structures). This is directly applicable to Park, because Park replaces sacrificial gate layers. Park, 9:47-60. In view of the knowledge of a POSITA, it would have been understood that at least including the additional rows would be advantageous. Banerjee ¶¶ 188-89. Second, adding the additional dummy structures would result in reducing the likelihood of defective bits on the edge of the memory cell region, because the addition of the additional rows extends the memory cell pattern for those respective columns into the dummy region. *Id.*, ¶¶ 190-91. It was well known that when a pattern stops (instead of extending into the dummy region), defects occur on the edge. *Id.*, ¶ 192 (citing Ex. 1028, 8:47-53 and Ex. 1029, 2:20-43 to explain the edge effect). Third, adding the additional dummy structures would result in an overall more uniform feature pattern, which reduces processing issues. *Id.*, ¶¶ 193-95 (citing Ex. 1030, 11 to explain this processing issue).

The adding the additional dummy structures would have been routine and a POSITA would have had a high expectation of success. First, Park already discloses

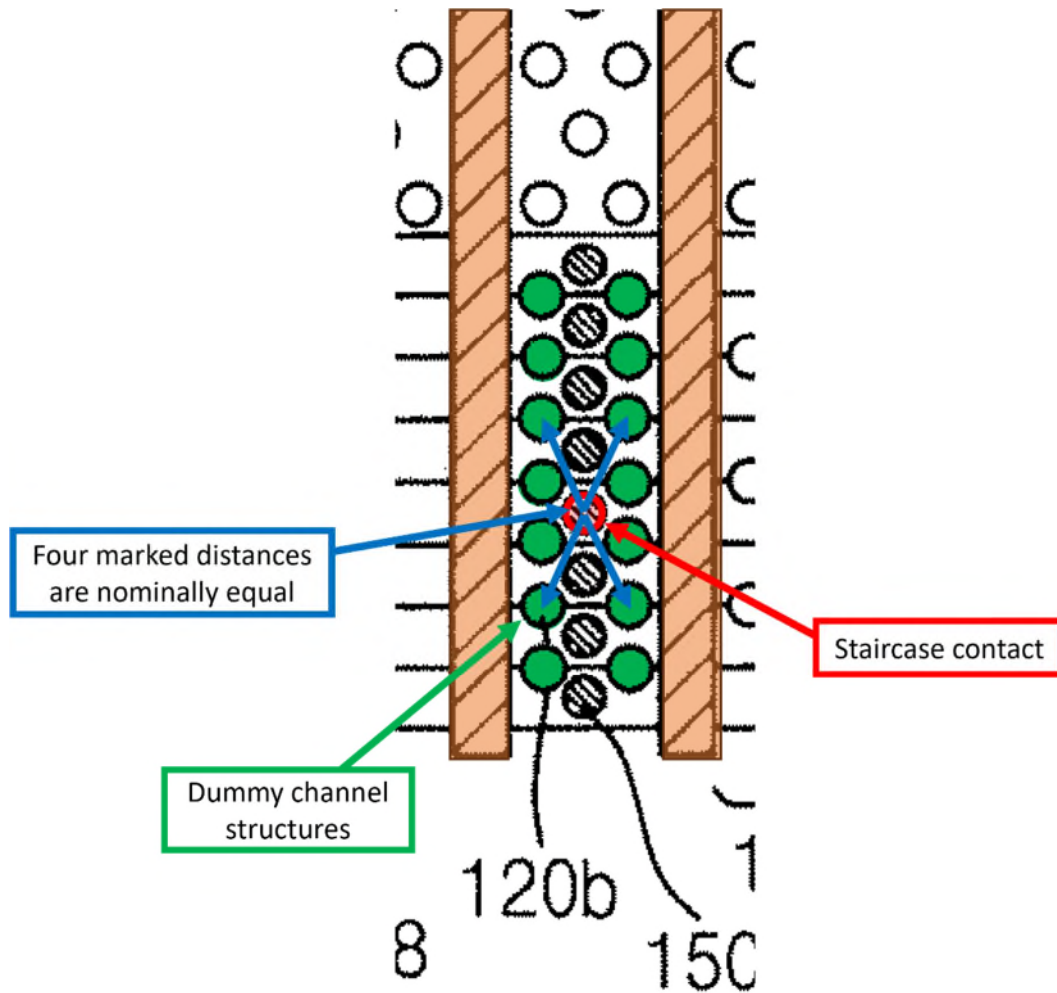
such dummy channel structures. Second, for the reasons above, the additional dummy channel structures would reduce processing issues. Banerjee ¶ 196.

D. Claim 8:

1. [8] “The 3D memory device of claim 7, wherein the plurality of dummy channel structures are of nominally equal lateral distances to the staircase contact.”

Park renders obvious this limitation. This analysis applies only to the second mapping under claim 5 (*the plurality of dummy source structures* is only the two *structures* below).

As the analysis under claim 7 demonstrates, it would have been obvious to include rows of Park’s dummy structures 120b on each side of the staircase contact. In such a case, *the plurality of dummy channel structures are of nominally equal lateral distances to the staircase contact*. Likewise, viewing *four dummy channel structures* immediately around staircase contact, these four are likewise equal distance from the *staircase contact*.



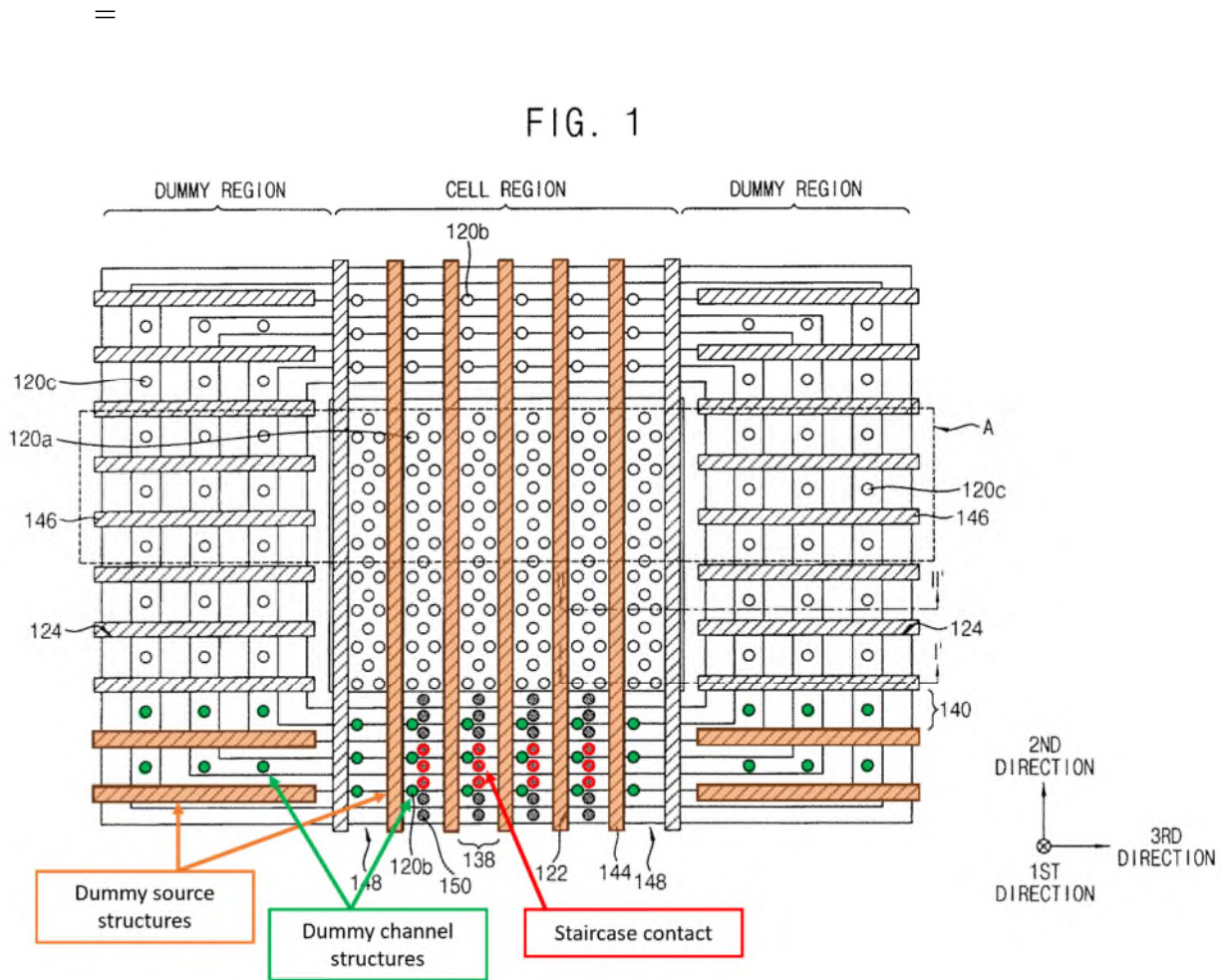
Note that Patent Owner likewise interprets such an arrangement to satisfy this claim language. Ex. 1026, 22. Here, *the plurality of dummy source structures* are only the above two *dummy source structures*, which *surround the staircase contact*. Banerjee ¶¶ 198-99.

E. Claim 9:

1. [9] “The 3D memory device of claim 7, wherein in the plan view, the plurality of dummy source structures interleave with the plurality of dummy channel structures.”

Park discloses, or at least renders obvious, this limitation. This analysis applies to both mappings of claim 5.

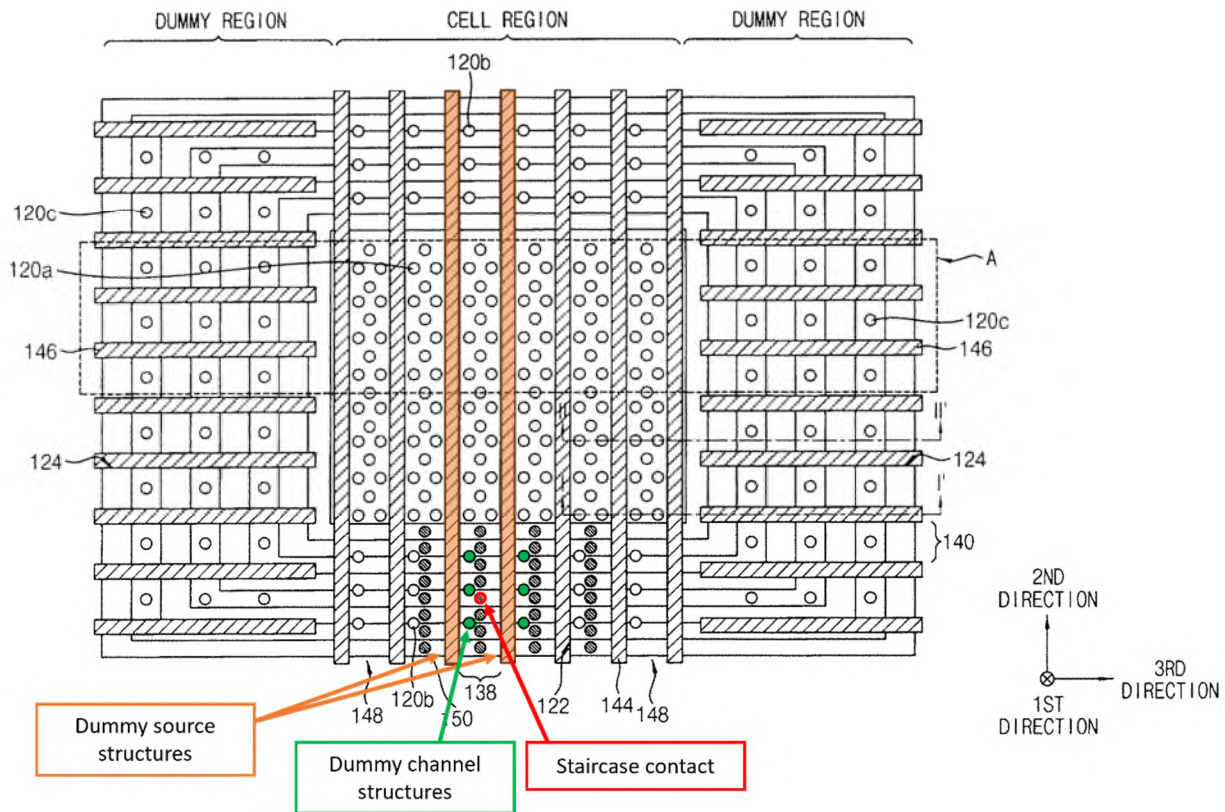
First, under the first mapping of claim 5, Park’s *plurality of dummy source structures interleave with the plurality of dummy channel structures*. As can be seen below, there are *dummy source structures* between the *dummy channel structures* (120b and 120c).



Park, Fig. 1; Banerjee ¶ 201.

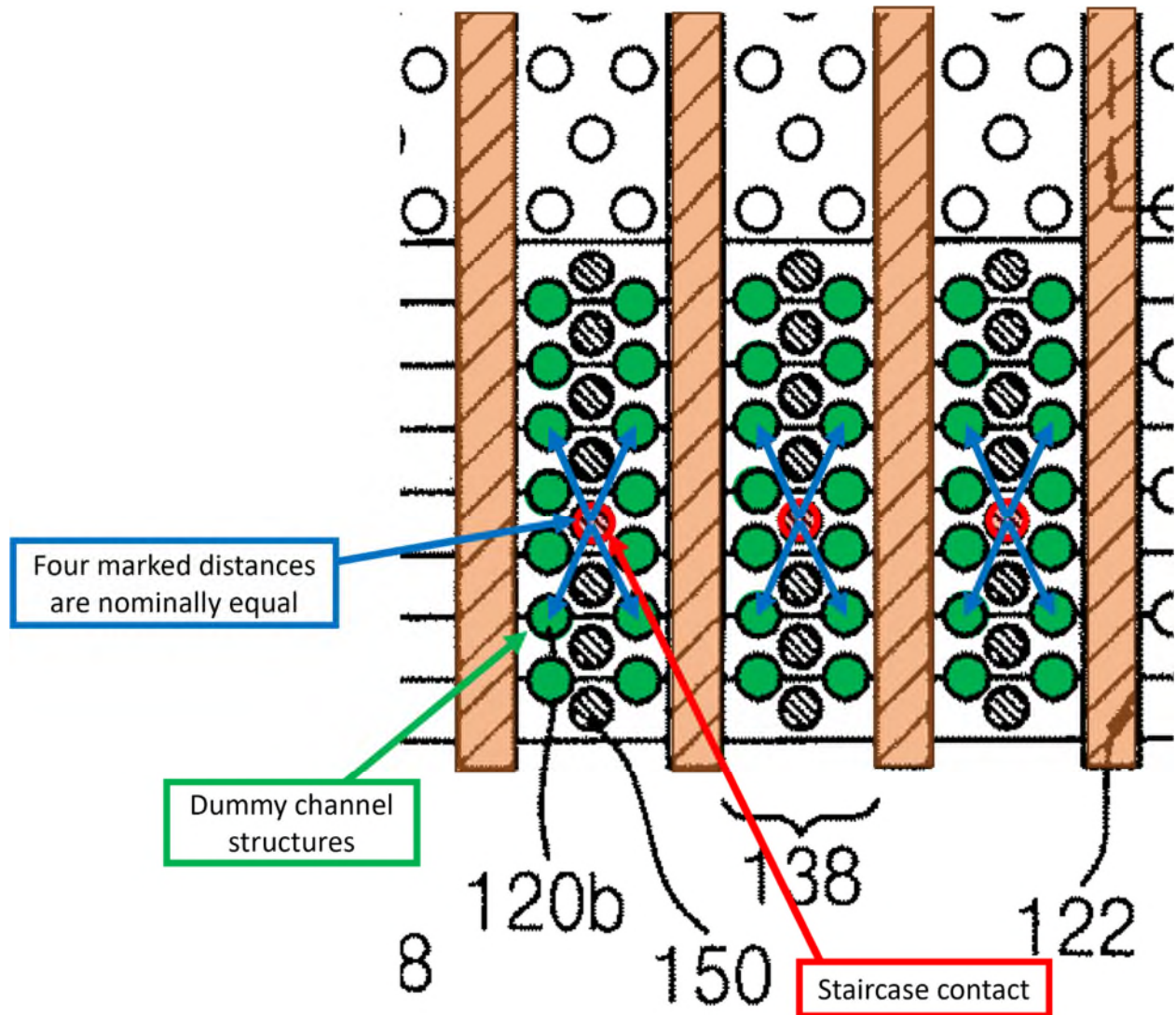
As §X.B discusses, under the second mapping of claim 5 in which *the plurality of dummy source structures* (in orange) are two *dummy source structures*, *the dummy channel structures* (shown in green below) *surround the staircase contact*. And *the plurality of dummy source structures interleave with the plurality of dummy channel structures*.

FIG. 1



Park, Fig. 1 (annotated); Banerjee ¶ 202.

Next, the analysis under claim 7 (*see* §X.C) demonstrates that, under either of the above mappings, it would have been obvious to include rows of dummy channel structures along each side of a staircase contact. Here, too, Park's *dummy source structures interleave* with the *dummy channel structures*. As shown below, Park's *dummy source structures* are between the *dummy channel structures*.



Park, Fig. 1 (modified); Banerjee ¶ 203.

Note that Patent Owner does not contend that *interleave* requires a pattern of a single dummy source structure, a single dummy channel structure, a single dummy source structure, a single dummy channel structure, etc. Rather, Patent Owner agrees that *interleave*, as the plain language demands, simply means “come

between.”⁷ Banerjee ¶ 204. For example, Patent Owner interprets this limitation to include within its scope the following pattern: a row of dummy channel structure, *two* rows of dummy source structures, a row of dummy channel structure, etc. Ex. 1026, 23.

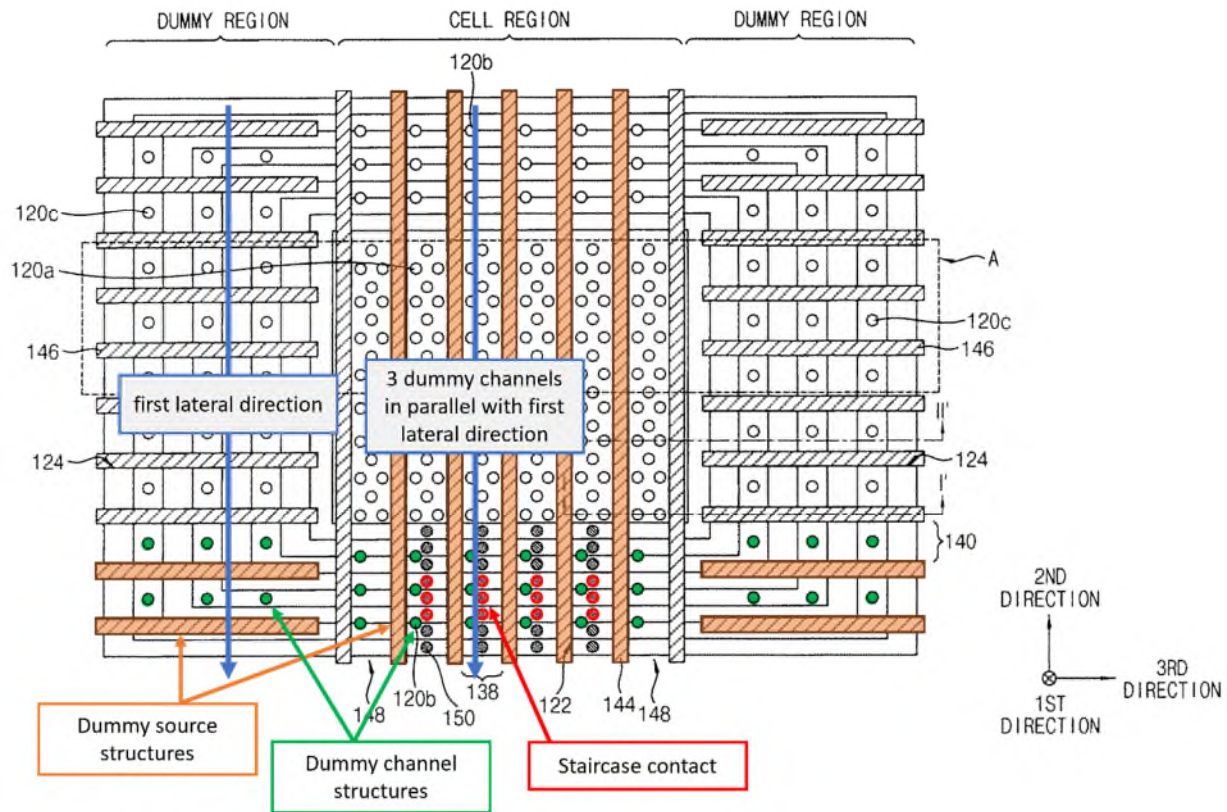
F. Claim 10:

1. [10] “The 3D memory device of claim 7, wherein in the plan view, at least two of the plurality of dummy channel structures are arranged in a third row that extends along a third lateral direction in parallel with the first or the second lateral direction.”

Park discloses, or at least renders obvious, this limitation. This analysis applies to both mappings of claim 5.

Under the first mapping, *at least two of the plurality of dummy channel structures* 120b are in *a third row that extends along a third lateral direction* (north to south) *in parallel with the first or the second lateral direction* (parallel to the first row of *dummy source structures*, see claim 5). Specifically, each set of three *channel structures* 120b (in green) (*at least two of the plurality of dummy channel structures*) that are in the wiring region (below, in the second direction, the cell region) are in a *row* that runs north to south. This is *parallel* to the *dummy source structures* in the dummy region that are like match sticks also running north to south.

⁷ <https://www.merriam-webster.com/dictionary/intervene>.

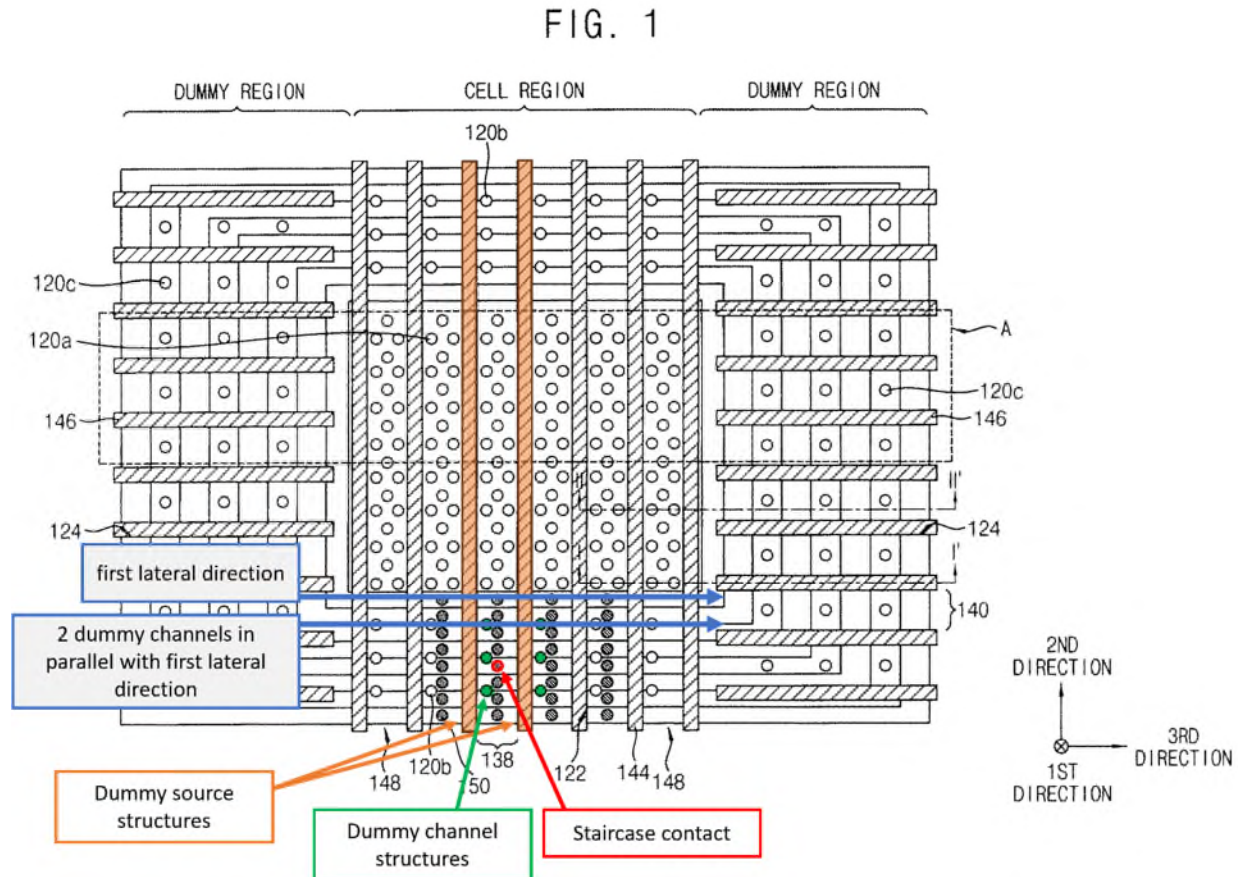
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Park, Fig. 1; Banerjee ¶ 206.

Under the second mapping,⁸ *at least two of the plurality of dummy channel structures* 120b are in *a third row that extends along a third lateral direction* (west to east) *in parallel with the first or the second lateral direction* (parallel to two *dummy source structures* that are in row from west to east, see claim 5). Specifically, a set of two *channel structures* 120b (in green) (*at least two of the plurality of dummy*

⁸ Were PO to argue that two is not a “row,” the example can expand to include an additional *staircase contact*.

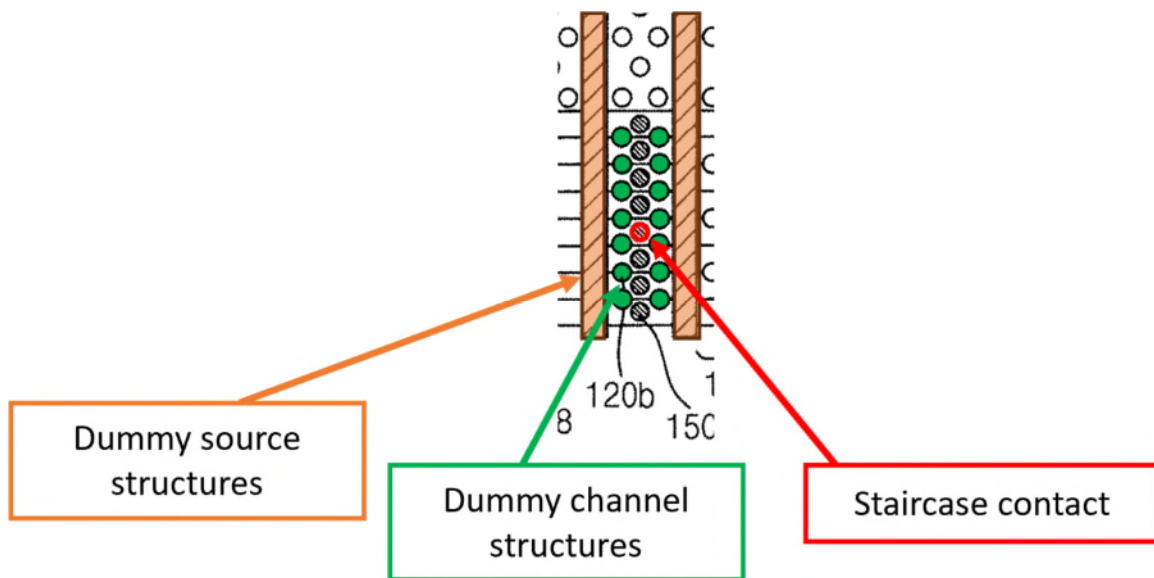
channel structures) that are in the wiring region (below, in the second direction, the cell region) are in a *row* that runs west to east. This is *parallel* to the *dummy source structures* in the wiring region that are like match sticks also running west to east.



Park, Fig. 1 (annotated); Banerjee ¶ 207.

Next, the analysis under claim 7 (*see* §X.C) demonstrates that it would have been obvious to include rows of dummy channel structures along each side of a staircase contact. This obvious arrangement likewise satisfies the claim under both mappings of claim 5. Here, too, *at least two* of the *dummy channel structures* 120b (shown in green) are in *a third row that extends along a third lateral direction*

(mapping 1: north to south; mapping 2: west to east) *in parallel with the first or the second lateral direction* (parallel to the first row of *dummy source structures*, which are in a row, under mapping 1: north to south, and under mapping 2: west to east), *see claim 5*). Below adds the exemplary obvious rows of dummy channel structures to line the sides of one set of staircase contacts for illustration purposes.



Park, Fig. 1 (modified); Banerjee ¶¶ 208-209.

XI. SECONDARY CONSIDERATIONS

Petitioner is unaware of any applicable secondary considerations of nonobviousness. None were identified during prosecution. *See generally* Ex. 1002. Even if such considerations existed, none would overcome the strong *prima facie* showing of obviousness.

XII. CONCLUSION

Petitioner respectfully requests that the Board enter a final written decision finding the Challenged Claims unpatentable.

Respectfully submitted,

ORRICK, HERRINGTON & SUTCLIFFE LLP

Dated: May 17, 2024

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CERTIFICATE OF COMPLIANCE

The undersigned certifies that the foregoing PETITION FOR *INTER PARTES* REVIEW complies with the type volume limitation in 37 C.F.R. § 42.24(a). According to the utilized word-processing system's word count, the petition—excluding the caption, table of contents, table of exhibits, mandatory notices, certificate of word count, and certificate of service—contains 12,129 words.

Dated: May 17, 2024

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CERTIFICATE OF SERVICE

The undersigned hereby confirms that the foregoing Petition for *Inter Partes* Review and associated exhibits were caused to be served on May 17, 2024 via overnight courier upon the following counsel of record for Patent Owner:

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