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(71) **Applicant** Yangtze Memory Technologies Co., Ltd.

Address Room 7018, No. 18 Huaguang Avenue, Guandong Science and Technology Industrial Park, Donghu Development Zone, Hongshan District, Wuhan City, Hubei Province 430074

(72) **Inventor** Liu Jun

(74) **Patent agency** Shanghai Yingsheng Intellectual Property Agency (General Partnership) 31294

Agent Dong Lin Chen Lili

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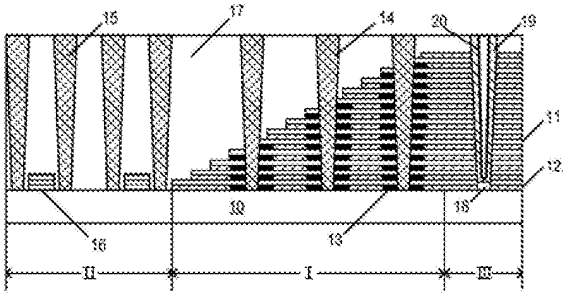
(54) Name of invention

Three-dimensional Memory and its Manufacturing Method

(57) Abstract

The present invention relates to the field of semiconductor manufacturing technology, and in particular to a three-dimensional memory and its manufacturing method. The three-dimensional memory includes: A substrate; a stacked structure formed on the substrate, which includes several grid layers arranged sequentially in a direction perpendicular to the substrate, and the end of the stacked structure has a step region; a conductive support pillar that penetrates the stacked structure of the step area in a direction perpendicular to the substrate; an isolation layer that is located between the conductive support pillar and the grid layer, and is used to electrically isolate the conductive support pillar and the grid layer. The invention avoids the problem of uneven morphology of the support pillar in the step area formed by the SEG method, ensures the productivity of the three-dimensional memory, and improves the performance of the three-dimensional memory.



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1. A three-dimensional memory, characterized in that it comprises:

A substrate;

A stacked structure formed on the substrate, which includes several grid layers arranged sequentially in a direction perpendicular to the substrate, and the end of the stacked structure has a step region

A conductive support pillar that penetrates the stacked structure of the step area in a direction perpendicular to the substrate;

An isolation layer that is located between the conductive support pillar and the grid layer, and is used to electrically isolate the conductive support pillar and the grid layer.

2. The three-dimensional memory according to Claim 1, characterized in that the three-dimensional memory includes several layers of isolation layers, and one layer of the isolation layer is arranged in the same layer as the grid layer.

3. The three-dimensional memory according to Claim 2, characterized in that the stacked structure also includes an interlayer insulating layer filled between two adjacent grid layers; several layers of the isolation layer are alternately stacked with the interlayer insulating layer in a direction perpendicular to the substrate.

4. The three-dimensional memory according to any one of claims 1 to 3, characterized in that the isolation layer covers side walls of the conductive support pillar.

5. The three-dimensional memory according to Claim 1, characterized in that, it also includes:

A peripheral area is provided around the periphery of the stacked structure, and a peripheral circuit is formed in the peripheral area;

A dielectric layer covering the peripheral area and the stacked structure;

A conductive plug penetrates the dielectric layer above the peripheral area in a direction perpendicular to the substrate and is connected to the peripheral circuit.

6. The three-dimensional memory according to Claim 5, characterized in that the conductive plug and the conductive support pillar are made of the same material and have the same height.

7. The three-dimensional memory according to Claim 1, characterized in that, it also includes:

A peripheral region, which is stacked and arranged below the stacked structure in a direction perpendicular to the substrate, and a peripheral circuit is formed in the peripheral region;

A dielectric layer covering the peripheral area and the stacked structure;

A conductive plug penetrates the dielectric layer above the peripheral area in a direction perpendicular to the substrate and is connected to the peripheral circuit.

8. The three-dimensional memory according to Claim 1, characterized in that the stacked structure further includes a core area, and the step area is located at the periphery of the core area;

The three-dimensional memory also includes:

A storage string passing through the stacked structure of the core area, the storage string including:

Epitaxial semiconductor layer;

A channel layer and a memory layer are located on the epitaxial semiconductor layer, and the memory layer is located on the periphery of the channel layer.

9. The three-dimensional memory according to Claim 1, characterized in that the three-dimensional memory is a 3D NAND memory.

10. A method of manufacturing a three-dimensional memory, characterized in that it includes the following steps:

Provide a substrate, where there is a stacked layer on the substrate, the stacked layer includes

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several grid layers arranged in sequence in a direction perpendicular to the substrate, and the end of the stacked layer has a step region;

Form through holes, where the through hole penetrates the stacked layers of the step region in a direction perpendicular to the substrate;

Form an isolation layer around the periphery of the through hole;

Metal is filled into the through hole to form a conductive support pillar, and the isolation layer is located between the conductive support pillar and the grid layer to electrically isolate the conductive support pillar and the grid layer.

11. The manufacturing method of a three-dimensional memory according to Claim 10, characterized in that the stacked layers further include an interlayer insulating layer filled between two adjacent grid layers; and the following steps are further included after forming the conductive support pillar:

Remove the grid layer in the stacked layer to form a gap area between two adjacent interlayer insulating layers;

Fill the gap area with conductive material to form a grid layer.

12. The method of manufacturing a three-dimensional memory according to Claim 11, characterized in that the specific steps of forming an isolation layer around the through hole include:

Etch back part of the grid layer along the through hole to form an opening between adjacent interlayer insulating layers;

Form an insulating isolation layer, and the isolation layer is at least filled in the opening.

13. The manufacturing method of a three-dimensional memory according to Claim 10, characterized in that the specific steps of forming an isolation layer around the periphery of the through hole include:

Deposit an insulating material on the sidewall of the through hole to form the isolation layer.

14. The method of manufacturing a three-dimensional memory according to Claim 10, characterized in that the substrate further includes: A peripheral area, the peripheral area is arranged on the periphery of the stacked layer, and a peripheral circuit is formed in the peripheral area; the specific steps of forming a through hole include:

Deposit a dielectric layer covering the stacked layer and the peripheral area;

Etch the step region and the peripheral region simultaneously, a through hole penetrating the dielectric layer and the stacked layer is formed in the step region, and a contact hole penetrating the dielectric layer is formed in the peripheral region at the same time.

15. The method of manufacturing a three-dimensional memory according to Claim 10, characterized in that the substrate further includes: A peripheral area, the peripheral area is stacked under the stacked layer in a direction perpendicular to the substrate, and a peripheral circuit is formed in the peripheral area;

The specific steps for forming vias include:

Deposit a dielectric layer covering the stacked layer and the peripheral area;

Etch the step region and the peripheral region simultaneously, a through hole penetrating the dielectric layer and the stacked layer is formed in the step region, and a contact hole penetrating

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the dielectric layer is formed in the peripheral region at the same time.

16. The manufacturing method of a three-dimensional memory according to Claim 14 or 15, characterized in that the specific steps of filling metal into the through holes to form conductive support pillar include:

At the same time, metal is deposited in the through hole and the contact hole, the conductive support pillar is formed in the step area, and a conductive plug is formed in the peripheral area; the conductive plug is connected to the peripheral circuit.

17. The manufacturing method of a three-dimensional memory according to Claim 10, characterized in that the stacked layer further includes a core storage area, and the step area is located at the periphery of the core storage area;

The manufacturing method of the three-dimensional memory also includes the following steps:

Form a channel hole while forming the through hole, the channel hole penetrating through the stacked layer of the core storage area in a direction perpendicular to the substrate;

Form an epitaxial semiconductor layer covering the bottom of the channel hole;

Form a memory layer covering sidewalls of the channel hole;

Form a channel layer, and the channel layer covers the surface of the memory layer.

18. The method of manufacturing a three-dimensional memory according to Claim 10, characterized in that the three-dimensional memory is a 3D NAND memory.

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Three-dimensional Memory and its Manufacturing Method

Technical field

[0001] The present invention relates to the field of semiconductor manufacturing technology, and in particular to a three-dimensional memory and its manufacturing method.

Background technology

[0002] With the development of technology, the semiconductor industry continues to seek new methods of production so that each memory die in a memory device has a greater number of memory cells. In non-volatile memory, such as NAND memory, one way to increase memory density is through the use of vertical memory arrays, that is, 3D NAND (three-dimensional NAND) memory; with the increasing level of integration, 3D NAND memory has developed from 32 layers to 64 layers, or even higher layers. CTF (Charge Trap Flash, charge trap flash) type 3D NAND memory is currently a cutting-edge memory technology with great development potential.

[0003] In a CTF type 3D NAND memory, there is a stacked structure formed by alternately stacking interlayer insulating layers and gate electrodes. The stacked structure includes a core region and a step region provided around the core region. The core area is used for storing information; the step area is located at the end of the stacking structure and is used to transmit control information to the core area to achieve the reading and writing of information in the core area. Of which, the step area has a support pillar that penetrates the stacked structure to support the stacked structure and prevent the stacked structure from collapsing.

[0004] However, the structural appearance of the existing support pillar is poor, which seriously affects the performance of the memory. Therefore, how to improve the structural shape of the support pillar and improve the performance of the memory is an urgent technical problem that needs to be solved.

Content of the invention

[0005] The present invention provides a three-dimensional memory and its manufacturing method to solve the problem of poor structural appearance of the support pillar in the step area in the existing three-dimensional memory and improve the performance of the memory.

[0006] In order to solve the above problems, the present invention provides a three-dimensional memory, including:

[0007] Substrate;

[0008] A stacked structure formed on the substrate, including several grid layers arranged sequentially in a direction perpendicular to the substrate, the end of the stacked structure having a step region;

[0009] Conductive support pillar, a stacked structure that penetrates the step area in a direction perpendicular to the substrate;

[0010] An isolation layer is located between the conductive support pillar and the grid layer, and is used to electrically isolate the conductive support pillar and the grid layer.

[0011] Preferably, the three-dimensional memory includes several layers of the isolation layer, and one layer of the isolation layer is arranged in the same layer as the grid layer.

[0012] Preferably, the stacked structure further includes an interlayer insulating layer filled

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between two adjacent grid layers, and several layers of the isolation layer are arranged in a direction perpendicular to the substrate. The interlayer insulating layers are alternately stacked and arranged.

[0013] Preferably, the isolation layer covers the side wall of the conductive support pillar.

[0014] Preferably, it also includes:

[0015] A peripheral area is provided around the periphery of the stacked structure, and a peripheral circuit is formed in the peripheral area;

[0016] Dielectric layer, covering the peripheral area and the stacked structure;

[0017] A conductive plug penetrates the dielectric layer above the peripheral area in a direction perpendicular to the substrate and is connected to the peripheral circuit.

[0018] Preferably, the conductive plug and the conductive support pillar are made of the same material and have the same height.

[0019] Preferably, it also includes:

[0020] Peripheral areas, stacked and disposed below the stacked structure in a direction perpendicular to the substrate, with peripheral circuits formed in the peripheral areas;

[0021] Dielectric layer, covering the peripheral area and the stacked structure;

[0022] A conductive plug penetrates the dielectric layer above the peripheral area in a direction perpendicular to the substrate and is connected to the peripheral circuit.

[0023] Preferably, the stacked structure further includes a core area, and the step area is located at the periphery of the core area;

[0024] The three-dimensional memory also includes:

[0025] A storage string passing through the stacked structure of the core area, the storage string including:

[0026] Epitaxial semiconductor layer;

[0027] A channel layer and a memory layer located on the epitaxial semiconductor layer, and the memory layer is located on the periphery of the channel layer.

[0028] Preferably, the three-dimensional memory is a 3D NAND memory.

[0029] In order to solve the above problems, the present invention also provides a manufacturing method of a three-dimensional memory, including the following steps:

[0030] Provide a substrate with a stacked layer on the substrate. The stacked layer includes several grid layers arranged in sequence in a direction perpendicular to the substrate. The end of the stacked layer has stepped area;

[0031] Form through holes that penetrate the stacked layers of the step region in a direction perpendicular to the substrate;

[0032] Form an isolation layer around the periphery of the through hole;

[0033] Fill the through holes with metal to form conductive support pillar. The isolation layer is located between the conductive support pillar and the grid layer to electrically isolate the conductive support pillar and the grid layer.

[0034] Preferably, the stacked layer further includes an interlayer insulating layer filled between two adjacent grid layers; after forming the conductive support pillar, the following steps are also included:

[0035] Remove the grid layer in the stacked layer to form a gap area between two adjacent interlayer insulating layers;

[0036] Fill the gap area with conductive material to form a grid layer.

[0037] Preferably, the specific steps of forming an isolation layer around the through hole

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include:

[0038] Etch back part of the grid layer along the through hole to form an opening between adjacent interlayer insulating layers;

[0039] Form an insulating isolation layer, and the isolation layer is at least filled in the opening.

[0040] Preferably, the specific steps of forming an isolation layer around the through hole include:

[0041] Deposit insulating material on the sidewall of the through hole to form the isolation layer.

[0042] Preferably, the substrate further includes: A peripheral area, the peripheral area is arranged on the periphery of the stacked layer, and a peripheral circuit is formed in the peripheral area; the specific steps of forming a through hole include:

[0043] Deposit a dielectric layer that covers the stacked layer and the peripheral area;

[0044] Etch the step region and the peripheral region simultaneously, form through holes penetrating the dielectric layer and the stacked layer in the step region, and simultaneously form through holes in the peripheral region. contact holes in the dielectric layer.

[0045] Preferably, the substrate further includes: A peripheral area, the peripheral area is stacked under the stacked layer in a direction perpendicular to the substrate, and a peripheral circuit is formed in the peripheral area; the specific steps of forming a through hole include:

[0046] Deposit a dielectric layer covering the stacked layer and the peripheral area;

[0047] Etch the step region and the peripheral region simultaneously, form through holes penetrating the dielectric layer and the stacked layer in the step region, and simultaneously form through holes in the peripheral region. contact holes in the dielectric layer.

[0048] Preferably, the specific steps of filling metal into the through holes to form conductive support pillar include:

[0049] Simultaneously deposit metal in the through hole and the contact hole, form the conductive support pillar in the step area, and simultaneously form a conductive plug in the peripheral area; the conductive plug is connected to the peripheral circuit.

[0050] Preferably, the stacked layer further includes a core storage area, and the step area is located at the periphery of the core storage area;

[0051] The manufacturing method of the three-dimensional memory further includes the following steps:

[0052] Form a channel hole while forming the through hole, the channel hole penetrating through the stacked layer of the core storage area in a direction perpendicular to the substrate;

[0053] Form an epitaxial semiconductor layer, the epitaxial semiconductor layer covers the bottom of the channel hole;

[0054] Form a memory layer covering the sidewalls of the channel hole;

[0055] Form a channel layer, and the channel layer covers the surface of the memory layer.

[0056] Preferably, the three-dimensional memory is a 3D NAND memory.

[0057] The three-dimensional memory and its manufacturing method provided by the present invention use conductive support pillar in the step area of the stacked structure to support the stacked structure. Compared with the traditional etching in the step area to form channel holes, and compared with the method of using Selective Epitaxy Growth (SEG) technology to grow silicon in the channel holes to form support pillar, the conductive support pillar formed by the present invention can avoid the morphology of the support pillar caused by the selective epitaxy growth technology. The problem of unevenness ensures the yield of three-dimensional memory and

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improves the performance of three-dimensional memory.

Picture description

[0058] Figure 1 is a schematic structural diagram of a three-dimensional memory in a specific embodiment of the present invention;

[0059] Figure 2 is a flow chart of the manufacturing method of the three-dimensional memory in the specific embodiment of the present invention;

[0060] Figures 3A-3G are schematic cross-sectional views of the main processes in the three-dimensional memory manufacturing process in specific embodiments of the present invention.

Specific embodiments

[0061] The specific embodiments of the three-dimensional memory and its manufacturing method provided by the present invention will be described in detail below with reference to the accompanying drawings.

[0062] In the manufacturing process of three-dimensional memory, a stacked structure consisting of interlayer insulating layers and grid layers alternately stacked in the direction vertical to the substrate is first formed, and then a stacked structure composed of interlayer insulating layers and grid layers stacked alternately along the vertical direction is formed through a metallization step. The interlayer insulating layer and the grid layer are alternately stacked in the direction of the substrate to form a stacked structure. Among them, the metallization step refers to: The grid layer in the stacked structure is removed to form a gap area between adjacent interlayer insulating layers; the gap area is then filled with conductive material to form a gate electrode layer. In this process, in order to avoid collapse of the stacked structure after the void area is formed, it is usually necessary to form support pillar penetrating the stacked structure in the stacked structure before the metallization step.

[0063] The stacked structure includes a core region and a step region provided around the core region. The core area is used for storing information; the step area is located at the end of the stacking structure and is used to transmit control information to the core area to achieve the reading and writing of information in the core area. The support pillar is distributed in the core area and the step area. Generally speaking, the support pillar in the core area and the step area are formed using the same process: That is, a channel hole is first formed in the stacked structure, and then a layer of silicon is grown at the bottom of the channel hole using selective epitaxy growth (SEG) technology. However, due to the large pattern density in the step area, the silicon layer grown in the channel hole in the step area using selective epitaxial growth technology has an uneven structure and poor morphology, which seriously affects the performance of the three-dimensional memory and may even lead to the scrapping of the three-dimensional memory, affecting the productivity of the three-dimensional memory.

[0064] In order to solve this problem, this specific embodiment provides a three-dimensional memory. Figure 1 is a schematic structural diagram of the three-dimensional memory in the specific embodiment of the present invention. The three-dimensional memory provided by this specific embodiment is preferably a 3D NAND memory, and more preferably a CTF 3D NAND memory.

[0065] As shown in Figure 1, the three-dimensional memory provided by this specific embodiment includes a substrate 10, a stacked structure, a conductive support pillar 14 and an isolation layer 13. The stacked structure is formed on the substrate 10 and includes several grid

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layers 12 arranged sequentially in a direction perpendicular to the substrate 10. The end of the stacked structure has a step region I; the conductive support pillar 14 penetrates the stacked structure of the step region I in a direction perpendicular to the substrate 10; the isolation layer 13 is located between the conductive support pillar 14 and the grid layers 12, and is used to electrically isolate the conductive support pillar 14 and the grid layers 12. Preferably, the conductive support pillar 14 is made of titanium, titanium nitride or tungsten.

[0066] This specific embodiment avoids the defects caused by using selective epitaxial growth technology to grow a silicon layer to form support pillar in the step area by forming conductive support pillar 14 in the step area I, improving the morphology of the support pillar and improving the performance of the three-dimensional memory.

[0067] The isolation layer 13 is used to isolate the conductive support pillar 14 and the grid layers 12 to avoid affecting the electrical signals transmitted in the grid layers 12. In order to improve the electrical isolation effect to ensure stable performance of the three-dimensional memory, preferably, the three-dimensional memory comprises several layers of the isolation layer 13 and one layer of the isolation layer 13 is provided in-line with the grid layers 12. More preferably, the stacked structure further comprises an interlayer insulation layer 11 filled between adjacent two layers of the grid layers 12; several layers of the insulation layers 13 are alternately stacked with the interlayer insulation layer 11 in a direction perpendicular to the substrate 10.

[0068] Specifically, due to the increase in the number of stacked layers of the stacked structure, the through holes used to form the conductive support pillar 14 have a higher aspect ratio. In order to further ensure that the conductive support pillar 14, and achieve electrical insulation between the conductive support pillar 14 and the grid layers 12. In this specific embodiment, the isolation layer 13 and the grid layers 12 are arranged in the same layer, and the isolation layer 13 is located between the grid layers 12 and the conductive support pillar 14.

[0069] In order to simplify the manufacturing process, preferably, the isolation layer 13 covers the side walls of the conductive support pillar 14. This kind of structure is particularly suitable when the number of stacked layers of the stacked structure is small or the width of the conductive support pillar 14 is large.

[0070] Specifically, the stacked structure includes a core region III and a step region I provided around the core region III. The step area I is located at the end of the stacked structure, and the step area I includes several layers of steps. In the stacked structure, an adjacent layer of interlayer insulation layer 11 and a layer of gate electrode layer 12 form an insulation/grid layer pair. The step region I includes several layers of steps arranged in a direction perpendicular to the substrate 10. Each layer of steps includes one insulation/grid layer pair or multiple insulation/grid layer pairs, and the insulation/grid layer pair in the lower step protrudes from the insulation/grid layer pair in the upper step along the horizontal direction. The area in the stacked structure except the step area is the core area III, and the core area III is used for data storage.

[0071] In this specific embodiment, the number of stacked layers of the stacked structure may be 32 layers, 64 layers, or other layers, and those skilled in the art can set it according to actual needs. Generally speaking, the greater the number of stacked layers of the stacked structure, the higher the integration level of the corresponding three-dimensional memory. The grid layers 12 is preferably made of tungsten. The specific material of the isolation layer 13 can be selected by those skilled in the art according to actual needs. It is preferably the same material as the interlayer insulating layer 11, such as oxide.

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[0072] In order to simplify the manufacturing process, preferably, the three-dimensional memory also includes: Peripheral area II is arranged around the periphery of the stacked structure, and peripheral circuits are formed in the peripheral area II; dielectric layer 17 covers the peripheral area II and the stacked structure; conductive plug 15 penetrates the dielectric layer 17 above the peripheral area II in a direction perpendicular to the substrate 10 and is connected to the peripheral circuit.

[0073] Preferably, the conductive plug 15 and the conductive support pillar 14 are made of the same material and have the same height. Specifically, as shown in Figure 1, one end of the conductive plug 15 is connected to the source or drain of the CMOS transistor 16 in the peripheral circuit, and the other end is connected to an interconnection structure (not shown). The conductive plug 15 is used to transmit electrical signals to the CMOS transistor 16. Since the conductive plug 15 and the conductive support pillar 14 are made of the same material and have the same height, they can be formed simultaneously, thereby further simplifying the manufacturing process of the three-dimensional memory.

[0074] Or, preferably, the three-dimensional memory also includes: A peripheral region is stacked under the stacked structure in a direction perpendicular to the substrate, and a peripheral circuit is formed in the peripheral region; a dielectric layer covers the peripheral region and the stacked structure; conductive plug penetrates the dielectric layer above the peripheral area in a direction perpendicular to the substrate and is connected to the peripheral circuit. Specifically, one end of the conductive plug is connected to the source or drain of the CMOS transistor in the peripheral circuit, and the other end is connected to the interconnection structure. At this time, the three-dimensional memory is PUC (Periphery Under Cell, the lower peripheral circuit of the unit).

[0075] More preferably, the three-dimensional memory also includes: A layer of insulating material covering the side walls of the conductive plug 15. The insulating material layer can be formed simultaneously with the isolation layer 13, thereby further simplifying the manufacturing process of the three-dimensional memory and improving the production efficiency of the three-dimensional memory.

[0076] Preferably, the stacked structure further includes a core area III, and the step area I is located at the periphery of the core area III; the three-dimensional memory also includes: A storage string passing through the stacked structure of the core area III; the storage string includes: The epitaxial semiconductor layer 18, the channel layer 20 located on the epitaxial semiconductor layer 18 and the memory layer 19, the memory layer 19 is located on the periphery of the channel layer 20. The memory layer 19 includes one or more layers selected from the group consisting of a charge tunneling layer, a charge trapping layer, and a charge blocking layer.

[0077] Not only that, this embodiment also provides a manufacturing method of a three-dimensional memory. Figure 2 is a flow chart of the manufacturing method of a three-dimensional memory in the specific embodiment of the invention. Figures 3A-3G are the schematic cross-sectional views of the main process in the three-dimensional memory manufacturing process in the specific embodiment of the present invention. See Figure 1 for the specific structure of the three-dimensional memory formed in this specific embodiment. Among them, the three-dimensional memory formed in this specific embodiment is preferably a 3D NAND memory, and more preferably a CTF 3D NAND memory.

[0078] As shown in Figures 1, 2, and 3A-3G, the manufacturing method of the three-dimensional memory provided by this specific embodiment includes the following steps:

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[0079] Step S21, as shown in Figure 3A, provides a substrate 10. There are stacked layers on the substrate 10. The stacked layer includes several grid layers 30 arranged in sequence in a direction perpendicular to the substrate 10. The ends of the stacked layers have step regions IV. The substrate 10 may be a Si substrate, a Ge substrate, a SiGe substrate, SOI (Silicon On Insulator, silicon on insulator) or GOI (Germanium On Insulator, germanium on insulator), etc. In this specific embodiment, the substrate 20 is preferably a silicon substrate for supporting a device structure thereon. The grid layers 30 may be gates in the final three-dimensional memory product (for example, a polysilicon gate); or they may be a dummy gates (for example, a nitride).

[0080] Step S22, as shown in Figure 3C, forms a through hole 31 that penetrates the stacked layer of the step region IV in a direction perpendicular to the substrate 10. The specific method of forming the through hole 31 may be dry etching or wet etching.

[0081] Step S23, as shown in Figure 3E, forms an isolation layer 13 around the through hole 31. The specific method of forming the isolation layer 13 may be chemical deposition, physical deposition or atomic layer deposition in the through hole 31.

[0082] Step S24, as shown in Figure 3F, fills metal into the through hole 31 to form a conductive support pillar 14. The isolation layer 13 is located between the conductive support pillar 14 and the grid layers 30 to electrically isolate the conductive support pillar 14 and the grid layers 30. The specific method of depositing metal in the through hole 31 may also be chemical deposition, physical deposition or atomic layer deposition.

[0083] When the grid layer is a dummy gate composed of nitride and other materials, in order to form the final gate structure, preferably, the stacked layer also includes an interlayer insulating layer 11 filled between two adjacent layers of the grid layers 30; after forming the conductive support pillar 14, the following steps are also included:

[0084] Remove the grid layers 30 in the stacked layer to form a gap area between two adjacent interlayer insulating layer 11;

[0085] Fill the gap area with conductive material to form the grid layers 12, as shown in Figure 3G. At this time, the grid layers 30 serve as a sacrificial layer. Of which, the conductive material is preferably tungsten.

[0086] Specifically, there is a step region IV at the end of the stacked layer. An adjacent layer of interlayer insulation layer 11 and a layer of gate 30 form an insulation/grid layer pair. The step region includes several layers of steps stacked in a direction perpendicular to the substrate 10. Each step has one insulating/grid layer pair or multiple insulating/grid layer pairs, and the insulation/grid layer pair in the lower step protrudes from the insulation/grid layer pair in the upper step along the horizontal direction. The material of the interlayer insulating layer 11 may be, but is not limited to, oxide.

[0087] In order to further improve the overall appearance of the conductive support pillar, preferably, the specific steps of forming the isolation layer 13 on the periphery of the through hole 31 include:

[0088] (I) As shown in Figure 3D, a portion of the grid layers 30 is etched back along the through hole 31 to form an opening 33 between adjacent interlayer insulation 11. Among them, the specific method of etching back part of the grid layers 30 along the through hole 31 can adopt a wet etching process, and use anisotropic etching to control the etching rate of the grid layers 30 by the etching liquid to be greater than the etching rate of the interlayer insulating layer 11. In this way, the end of the grid layers 30 can be removed without affecting the interlayer insulating layer 11 or having

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a small impact. The etching liquid is preferably phosphoric acid with a temperature within a preset range.

[0089] (II) As shown in Figure 3E, an insulating isolation layer 13 is formed, and the isolation layer 13 is at least filled in the opening 33. Among them, the method of depositing the insulating material to form the insulating isolation layer 13 is preferably atomic layer deposition. The isolation layer 13 may only be filled in the opening 32, or may also cover the side walls of the through hole 31.

[0090] In order to simplify the manufacturing process, preferably, the specific steps of forming the isolation layer 13 on the periphery of the through hole 31 include:

[0091] Deposit insulating material on the sidewall of the through hole 31 to form the isolation layer 13. The method of depositing the insulating material on the sidewall of the through hole 31 may be chemical deposition, physical deposition or atomic layer deposition.

[0092] Preferably, the substrate 10 further includes: Peripheral area II, the peripheral area II is arranged on the periphery of the stacked layer, and a peripheral circuit is formed in the peripheral area II; the specific steps of forming a through hole include:

[0093] As shown in Figure 3B, a dielectric layer 17 is deposited, and the dielectric layer 17 covers the stacked layer and the peripheral area II;

[0094] As shown in Figure 3C, the step region IV and the peripheral region II are etched simultaneously, and a through hole 31 penetrating the dielectric layer 17 and the stacked layer is formed in the step region IV, and at the same time, a contact hole 32 penetrating the dielectric layer 17 is formed in the peripheral area II.

[0095] Or, when manufacturing a PUC type three-dimensional memory, preferably, the substrate also includes: A peripheral area, the peripheral area is stacked under the stacked layer in a direction perpendicular to the substrate, and a peripheral circuit is formed in the peripheral area; the specific steps of forming a through hole include:

[0096] Deposit a dielectric layer covering the stacked layer and the peripheral area;

[0097] Etch the step region and the peripheral region simultaneously, form through holes penetrating the dielectric layer and the stacked layer in the step region, and simultaneously form through holes in the peripheral region. contact holes in the dielectric layer.

[0098] More preferably, the specific steps of filling metal into the through hole 31 to form the conductive support pillar 14 include:

[0099] As shown in Figure 3F, metal is deposited in the through hole 31 and the contact hole 32 at the same time, the conductive support pillar 14 is formed in the step area IV, and at the same time, a conductive plug 15 is formed in the peripheral area II; the conductive plug 15 is connected to the peripheral circuit. Specifically, one end of the conductive plug 15 is connected to the peripheral circuit, and the other end is used to connect to an interconnection structure (not shown).

[0100] In this specific embodiment, while forming the conductive support pillar 14 in the step area, a conductive plug 15 is formed in the peripheral area II, which ensures the morphology of the conductive support pillars 14 in the step area, improves the performance of the three-dimensional memory, and combines the steps of forming the conductive plugs 15 and the steps of forming the conductive support pillars 14 into one, simplifying the manufacturing process of the three-dimensional memory.

[0101] Preferably, the stacked layer further includes a core storage area V, and the step area IV is located at the periphery of the core storage area V; the manufacturing method of the three-dimensional memory further includes the following steps:

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[0102] As shown in Figure 3C, a channel hole 34 is formed while forming the through hole 31, and the channel hole 34 penetrates the stacked layer of the core storage area V in a direction perpendicular to the substrate 10;

[0103] As shown in Figure 3D, an epitaxial semiconductor layer 18 is formed, and the epitaxial semiconductor layer 18 covers the bottom of the channel hole 34;

[0104] Form a memory layer 19 that covers the sidewalls of the channel hole 34;

[0105] Form a channel layer 20, and the channel layer 20 covers the surface of the memory layer 19.

[0106] Of which, the epitaxial semiconductor layer 18 may be grown using a SEG process. The memory layer 19 includes one or more layers selected from the group consisting of a charge tunneling layer, a charge trapping layer, and a charge blocking layer.

[0107] The three-dimensional memory and its manufacturing method provided by this specific embodiment use conductive support pillar in the step area of the stacked structure to support the stacked structure. Compared with the traditional etching to form channels in the step area, and compared with the method of using selective epitaxy growth (SEG) technology to grow silicon in the channel holes to form support pillar, the conductive support pillar formed by the present invention can avoid the problem of uneven morphology of the support pillar caused by selective epitaxial growth technology, ensure the productivity of the three-dimensional memory, and improve the performance of the three-dimensional memory.

[0108] The above are only preferred embodiments of the present invention. It should be pointed out that those of ordinary skill in the art can also make several improvements and modifications without departing from the principles of the present invention. These improvements and modifications should also be regarded as the protection scope of the present invention.

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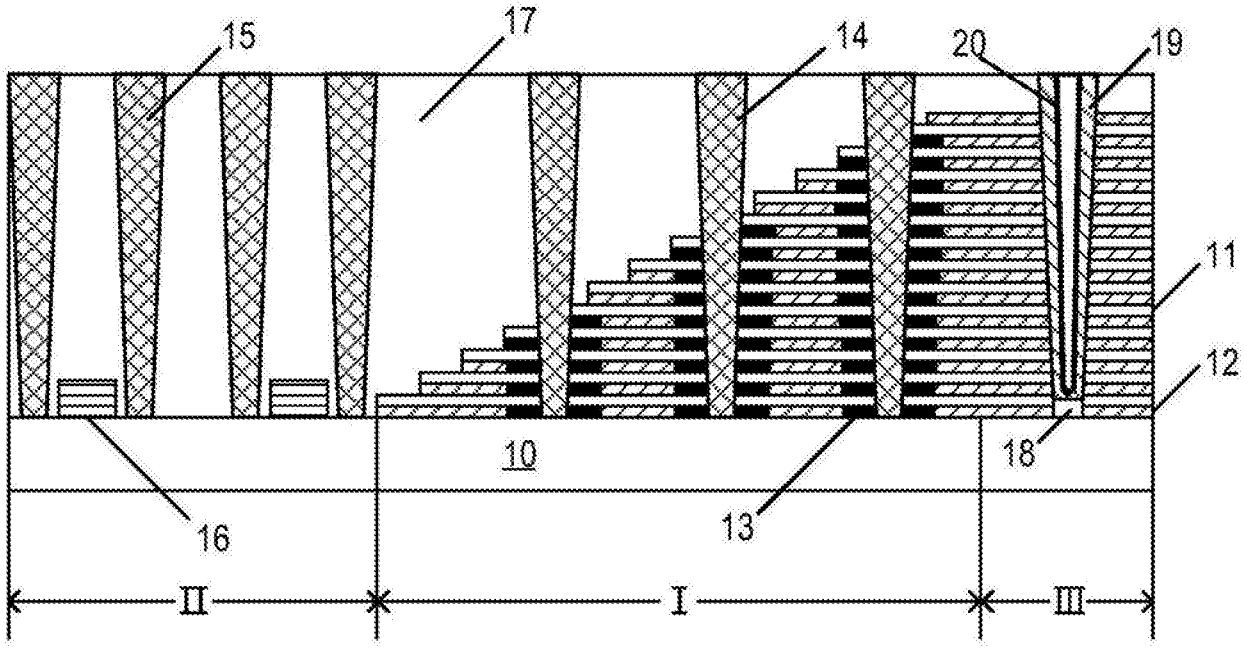

Figure 1

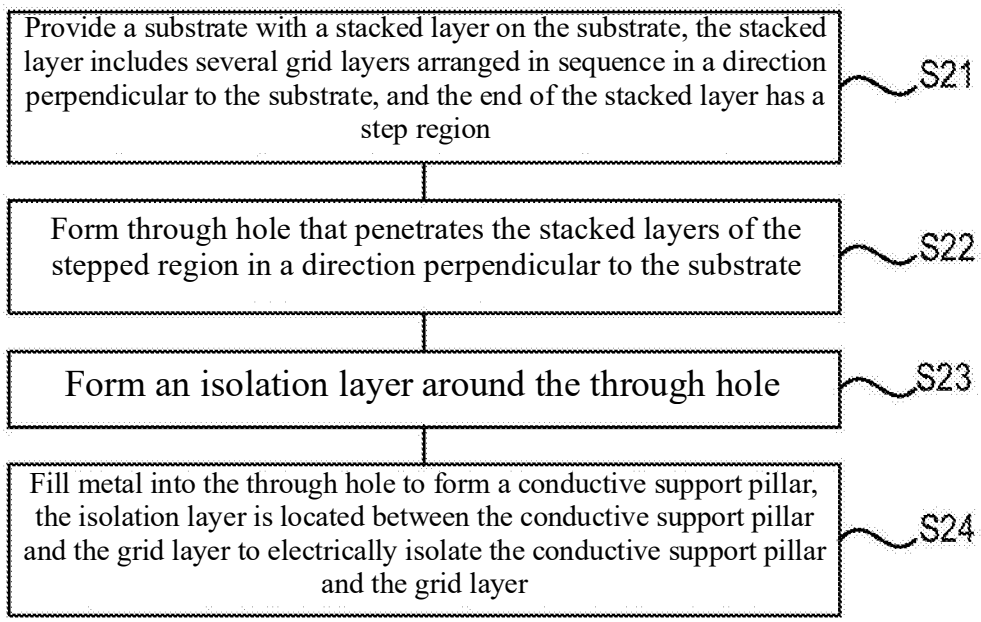

Figure 2

Micron Ex. 1012, p. 14
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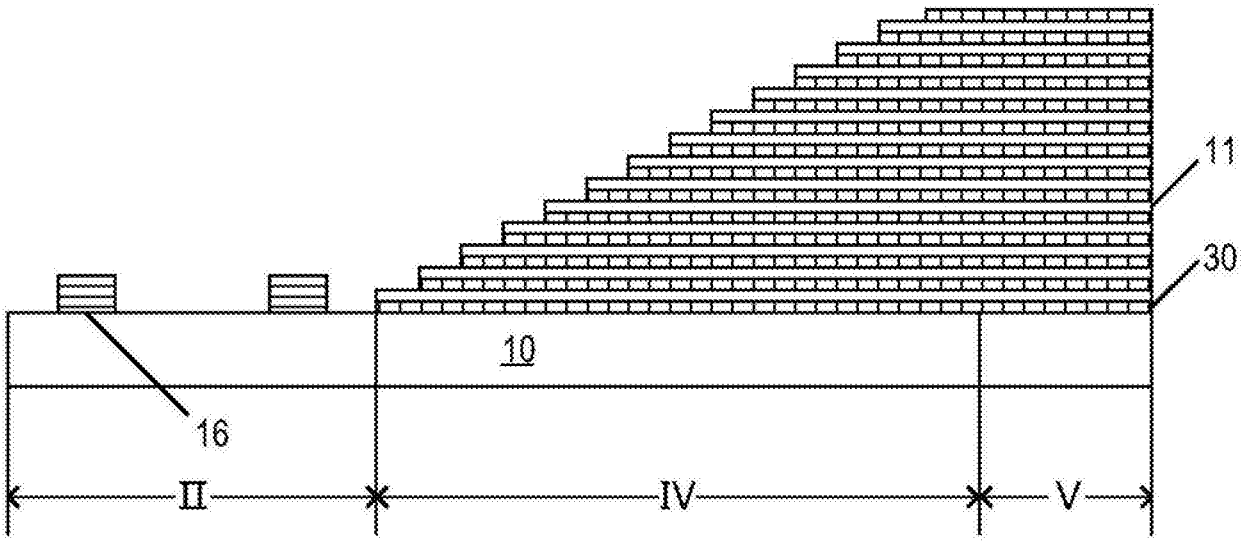

Figure 3A

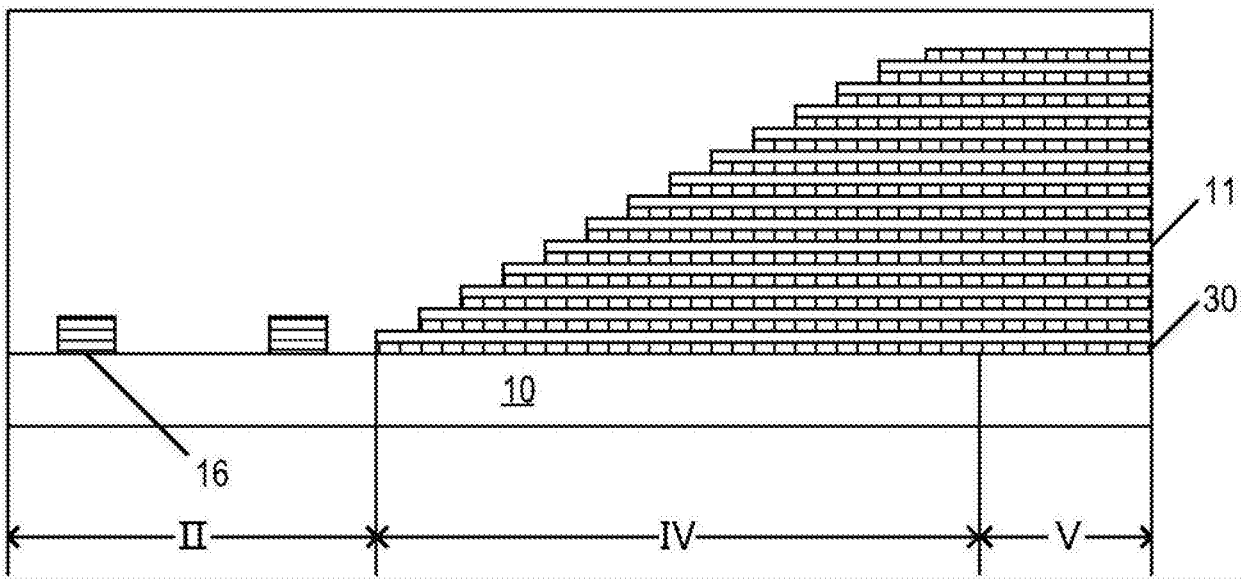

Figure 3B

Micron Ex. 1012, p. 15
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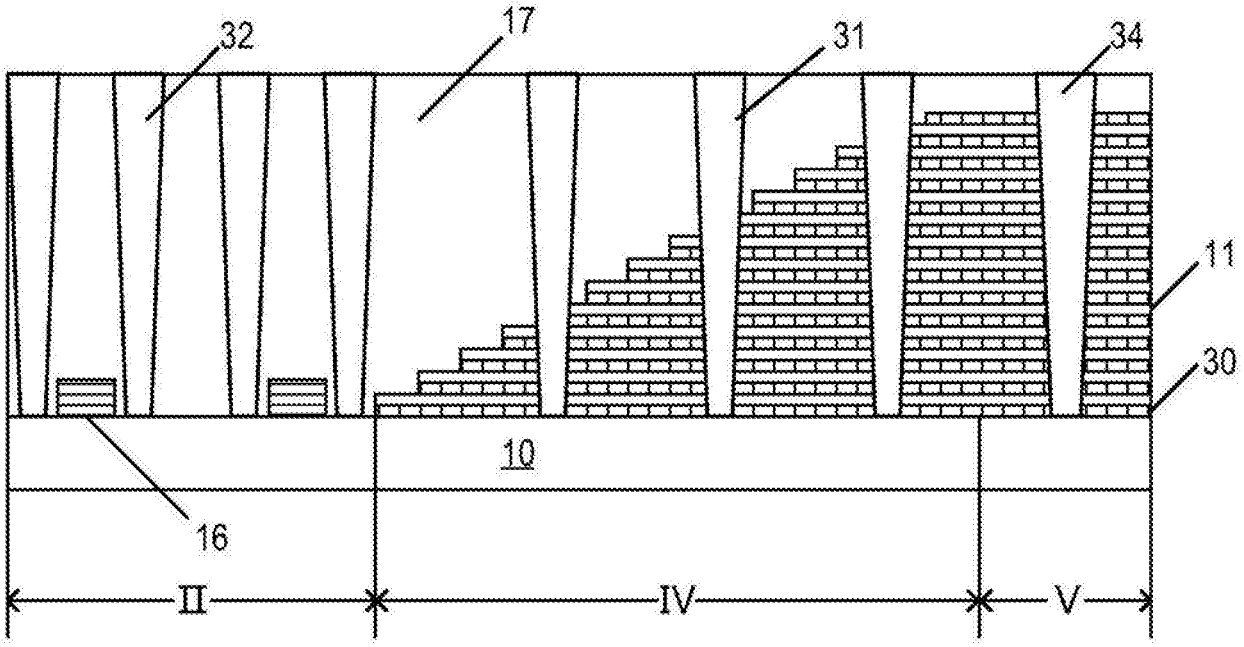

Figure 3C

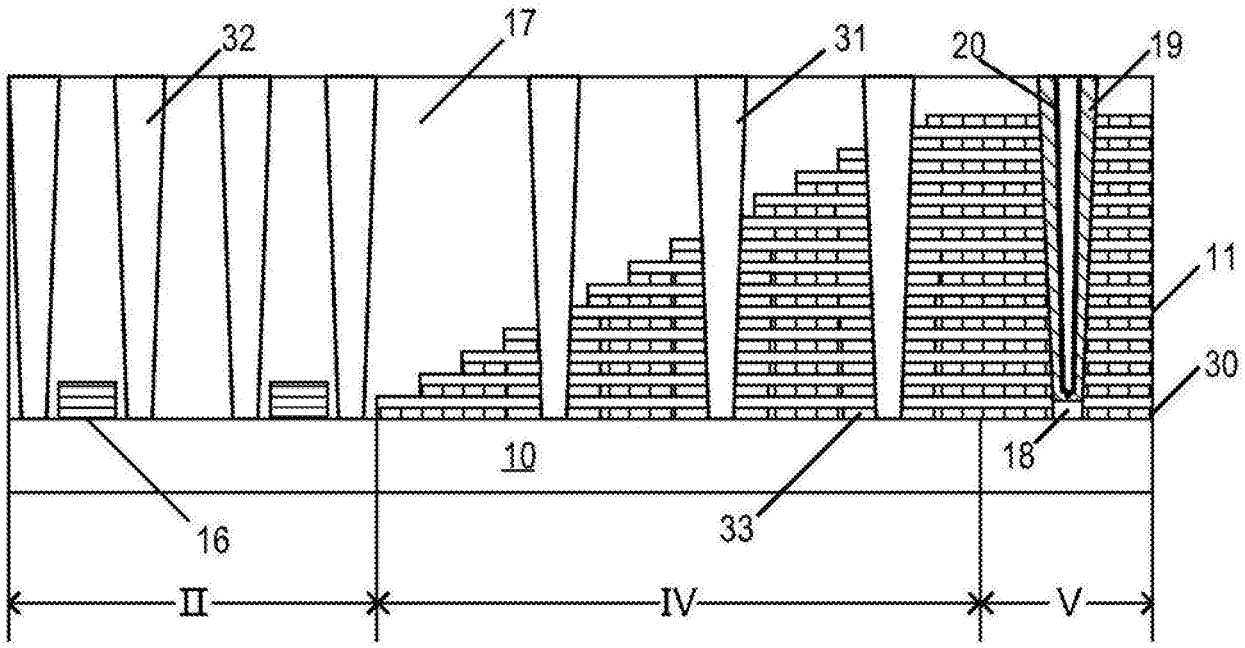

Figure 3D

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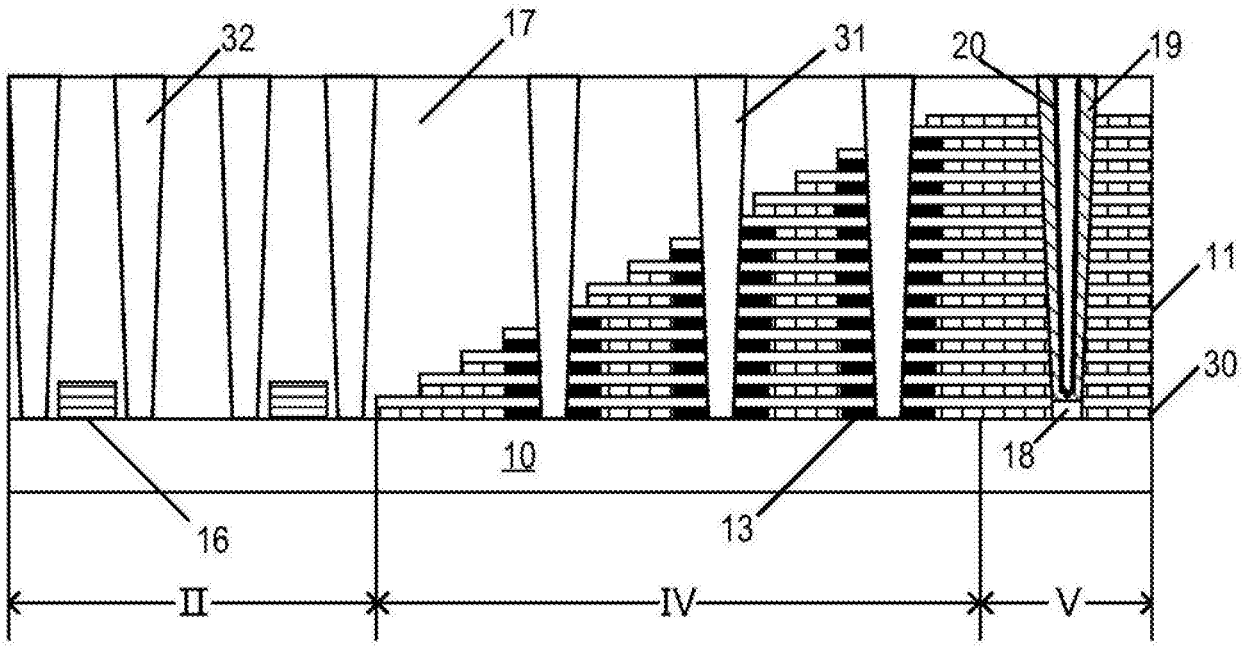

Figure 3E

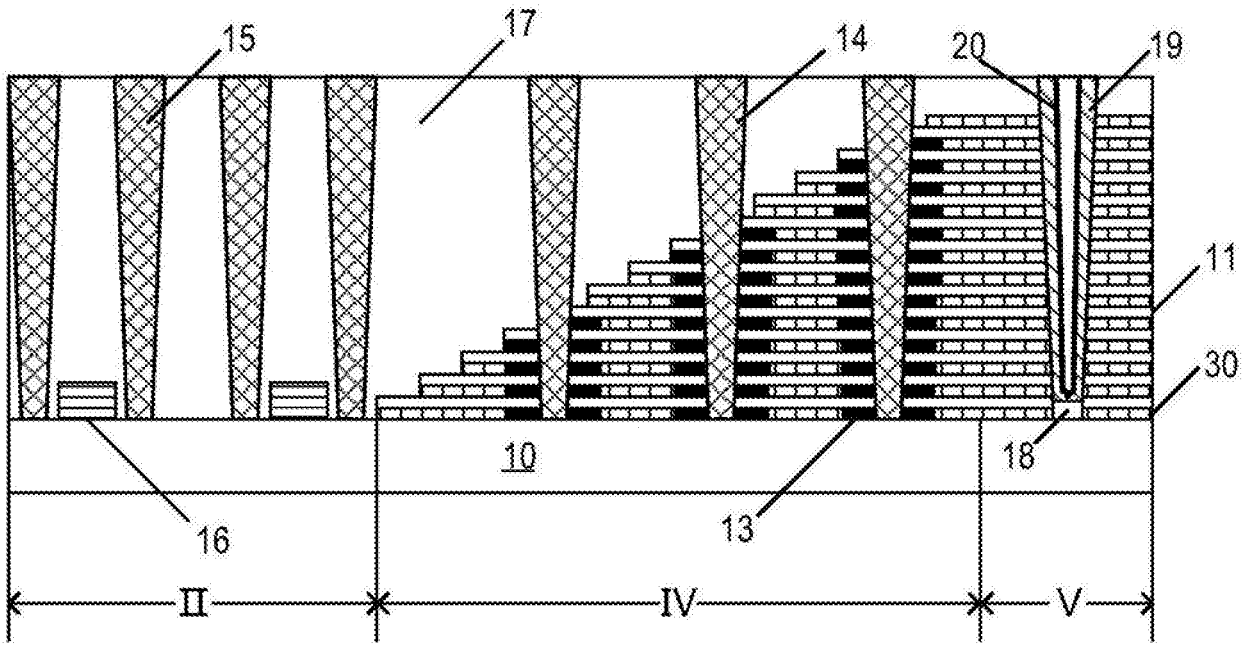

Figure 3F

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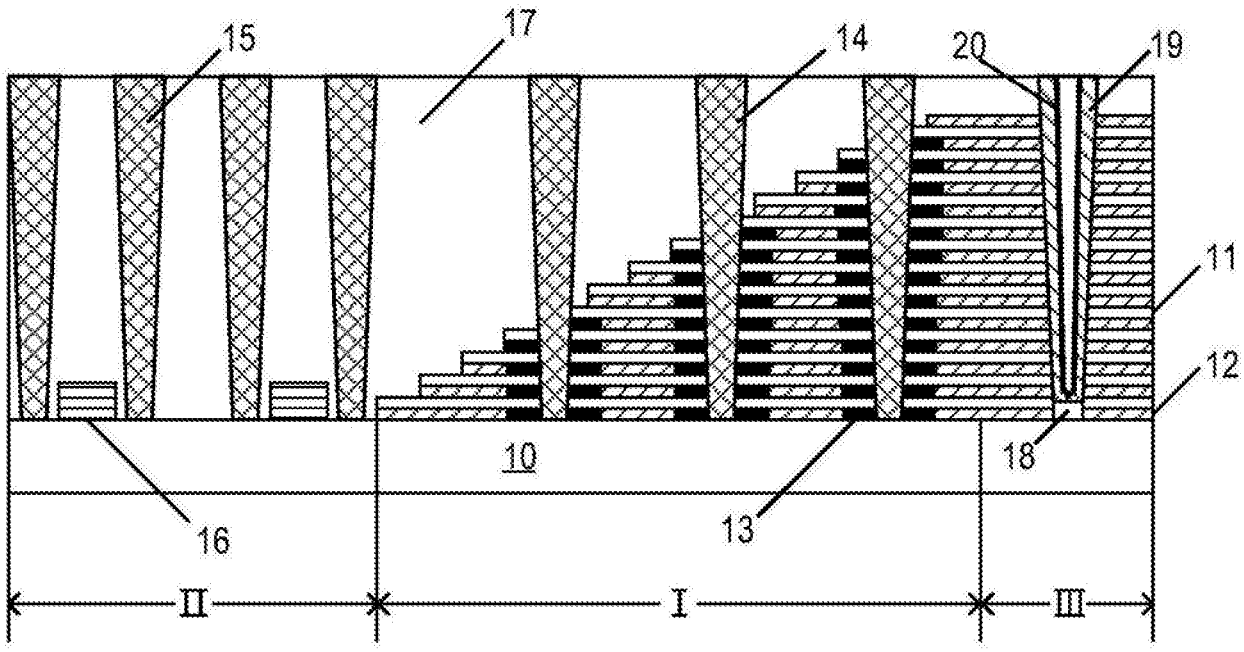

Figure 3G

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TRANSPERFECT

February 28, 2024

Certification

Translator's Declaration:

I, Karen Lee, hereby declare:

That I possess advanced knowledge of the Chinese and English languages.

My qualifications are as follows: 8 years of experience as a professional translator/interpreter, studied Mandarin Chinese at New York University.

The attached Chinese into English translation has been translated by me and to the best of my knowledge and belief, it is a true and accurate translation of:

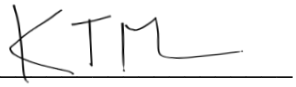
CN108766971A

I understand that willful false statement and link are punishable by fine or imprisonment, or both (18 U.S.C. 1001) and may jeopardize the validity of the application or any patent issuing thereon. I declare under the penalty of the perjury that all statements made herein of my own knowledge are true and all statements made on information and belief are believed to be true.

Karen Lee

Sworn to before me this

28th of February 2024



Signature, Notary Public

KEVIN T. MULRYAN
Notary Public, State of New York
Reg. No. 02MU6375986
Qualified in New York County
Commission Expires 6/4/2026

Stamp, Notary Public

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