

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,

Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,

Patent Owner.

Case IPR2024-00910
Patent 10,861,872

**PATENT OWNER'S PRELIMINARY RESPONSE
UNDER 37 C.F.R. § 42.107**

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Exhibit	Description
Ex. 2001	Joint Claim Construction and Prehearing Statement

LIST OF ABBREVIATIONS

Abbreviation	Term
'872	U.S. Pat. No. 10,861,872
'872FH	File History of U.S. Pat. No. 10,861,872
Challenged Claims	'872, Claims 7-10
Office	U.S. Patent and Trademark Office
Parallel district court litigation	<i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , NDCA-3-23-cv-05792 (N.D. Cal.)
Park	U.S. Pat. No. 9,859,297
Patent Owner or PO	Yangtze Memory Technologies Co. Ltd.
Petition or Pet.	Petition for <i>Inter Partes</i> Review of U.S. Patent No. 10,861,872 (IPR2024-00910, Paper 1)
Petitioner	Micron Technology, Inc.
POSITA	Person of ordinary skill in the art
Previously-Challenged Claims	'872, Claims 1-6, 11-13
Previously-Filed Pet.	Petition for <i>Inter Partes</i> Review of U.S. Patent No. 10,861,872 (IPR2024-00789, Paper 1)

Pursuant to §42.107, ¹ Patent Owner submits this Preliminary Response to the above-captioned Petition, which should be denied in its entirety based on Petitioner's failure to show a reasonable likelihood of prevailing on any asserted ground as to any Challenged Claim.

I. INTRODUCTION

This proceeding relates to the second of two *inter partes* review petitions filed by Petitioner concerning U.S. Patent No. 10,861,872 ("’872 patent") and should be denied institution for at least the same reasons identified in Patent Owner's prior Preliminary Response.² Petitioner's second IPR challenges dependent claims 7-10 ("the Challenged Claims") and raises the same ground based on the Park reference for independent claim 1, on which the Challenged Claims depend, as the first IPR. This Preliminary Response presents the same arguments that were raised in the first

¹ All emphasis and color annotations herein are added, and all statutory and regulatory citations are to either 35 U.S.C. or 37 C.F.R., as the context indicates, unless otherwise stated.

² PO does not oppose Petitioner's claim that it needed a second petition (Paper 3), but disputes Petitioner's assertions that PO's identification of asserted claims was belated, that PO's infringement allegations are without merit and could not have been credibly alleged, and that PO has asserted a large number of '872 claims.

proceeding regarding the Park ground for independent claim 1 as well as additional arguments that address the Challenged Claims specifically.

As set forth in Patent Owner's earlier Preliminary Response, Petitioner's previously filed IPR2024-00789 (Pap. 1) challenging claims 1-6 and 11-13 should be denied institution. IPR2024-00789, Pap. 11. The Challenged Claims in this IPR all depend directly or indirectly from previously challenged dependent claim 5, which in turn depends from previously challenged independent claim 1, and Petitioner relies on the same Park ground again here. Pet. 1. Accordingly, Patent Owner presents the same arguments here as to the limitations of claim 1, which are required by all Challenged Claims. In addition, because all Challenged Claims include the limitations of claims 5 and 7, Patent Owner presents additional arguments as to those limitations. The previously-filed Preliminary Response in IPR2024-00789 did not address dependent claims 5 and 7 because the limitations were not common to all (claim 5) or any (claim 7) of the challenged claims in that proceeding, and therefore would not have affected the Board's analysis of whether to grant institution. For the same reason, any decision by the Board to institute IPR2024-00789 does not mean that a reasonable likelihood of success also exists in this proceeding.

The '872 is directed to a novel and improved three-dimensional memory structure scheme that mitigates problems arising from semiconductor device

fabrication processes involving depositing conductive materials into voids formed in memory devices. Ex. 1001, 4:64-65, 5:22-33. The relevant prior art at the time employed gate line slit structures to fill lateral recesses in memory devices to form, for example, gate electrodes and gate lines of the device. Ex. 1001, 4:30-33. But, with advances in 3D memory device architecture, the prior art fabrication techniques presented drawbacks, including nonuniformity resulting in a bowing of the semiconductor wafer, which contributed to yield loss during manufacturing. Ex. 1011, 5:22-30.

The '872 introduced a different memory device architecture that uses dummy source structures and dummy channel structures to solve the problems caused by gate line structures. Ex. 1001, 1:39-42, 5:31-36, 8:20-24. The new architecture taught by the '872 and recited in the claims is characterized by arranging the dummy source structures and dummy channel structures such that they surround a staircase contact. This includes arranging the dummy source structures and dummy channel structures in a particular pattern, layout, or design based on the size of the staircase region. *Id.* 8:49-51, 6:41-46, 6:61-62. Such an arrangement is advantageous, for example, because it allows the deposited conductive material to travel “shorter distances to fill up the lateral recesses,” thus allowing the formed gate electrodes and gate lines to be “less susceptible to voids or density nonuniformity.” Ex. 1001, 4:52-58.

Institution should be denied because the Petition fails to establish a reasonable likelihood of prevailing with respect to any of the Challenged Claims.

Petitioner relies only on the “Park” reference (Ex. 1005) for each limitation of the Challenged Claims, but fails to show that Park discloses or renders obvious at least four separate requirements of the Challenged Claims. As an initial matter, Petitioner does not assert that Park anticipates any of the Challenged Claims, and seemingly concedes that the art does not explicitly disclose certain features, such as limitations relating to the claimed “dummy source structures” and “dummy channel structures.” *See* Pet., 10. Instead, Petitioner raises obviousness arguments based on a mix of incorrect claim constructions, faulty analysis, and impermissible hindsight.

First, Park does not disclose or render obvious that its alleged dummy source structures are “surrounding the staircase contact,” as required by claim 1 and thus the Challenged Claims, because Park’s contact is merely “between” two alleged dummy source structures. Indeed, the applicant admitted prior art (“AAPA”) in the ’872 presented this same structure and the claims were properly allowed over the AAPA during prosecution.

Second, Petitioner has not shown that Park discloses or renders obvious “dummy source structures,” as required by claim 1 and thus the Challenged Claims, because Park’s purported dummy source structures actually function as a source for the memory cell and are therefore not “dummy source structures.”

Tellingly, Petitioner relies on “common source lines” as the “dummy source structures” that allegedly surround the contacts (as separately required)—as opposed to the “dummy source lines,” which do not. Attempting to circumvent this problem, Petitioner presents a flawed claim construction for the term—reading out the requirement that this be a “dummy” source structure.

Third, Park neither discloses nor renders obvious that its alleged dummy source structures in plan view are “arranged in a first row that extends along a first lateral direction,” as recited by claim 5 and thus the Challenged Claims, because Park’s alleged dummy source structures instead span the entire cell region of the memory device, rather than merely a row.

Fourth, Park fails to disclose or render obvious that its alleged dummy channel structures are “surrounding the staircase contact” (claim 7) as there is another intervening component that separates the alleged dummy channel structure from the alleged staircase contact on one of the two sides—preventing the structures from encircling the contact. Recognizing this shortfall, Petitioner argues that a POSITA would have been motivated to modify Park, but not one of the alleged rationales motivates the hindsight-based modification proposed by Petitioner. Instead, both Park and the additional references that Petitioner cites demonstrate that a POSITA would not have made the proposed modifications.

Because the sole reference Petitioner relies on fails to disclose or render

obvious limitations of the Challenged Claims, the Board should deny institution.

II. THE CLAIMED INVENTION OF THE '872 PATENT

The claimed invention of the '872 is directed to “an improved 3D [three-dimensional] memory structure scheme” that mitigates problems arising from semiconductor device fabrication processes, which contribute to production yield loss and device performance variability. Ex. 1001, 4:64-65, 5:22-33.

Specifically, the '872 is directed to improving a semiconductor fabrication technique for 3D memory structures. Ex. 1001, 1:15-18, 4:30-33. As 3D memory devices are “scaled to smaller sizes” and “feature sizes of memory cells approach a lower limit,” fabrication becomes more challenging. Ex. 1001, 1:18-22, 4:37-38. To illustrate these challenges, the '872 describes the common approach of using openings, called gate line slits (GLSs), to deposit conductive material into trenches (or “lateral recesses”) that extend laterally in the memory array of a memory device. Ex. 1001, 4:44-49, 5:17-20. Once filled with conductive material, the trenches form the device gate lines. The **GLS**, as depicted in the color-annotated version of the '872's Fig. 5 below, has “a dimension along the extending direction (or the x-direction) much greater than the dimension along the expanding dimension (or the y-direction)).” Ex. 1011, 5:22-30. As a result of this shape, formation of the GLS “can contribute to unbalanced variations of wafer flatness (e.g., wafer warpage bias) in different directions,” which “can have an adverse impact on the photolithography

process to form device patterns, leading to potential die yield loss.” *Id.*

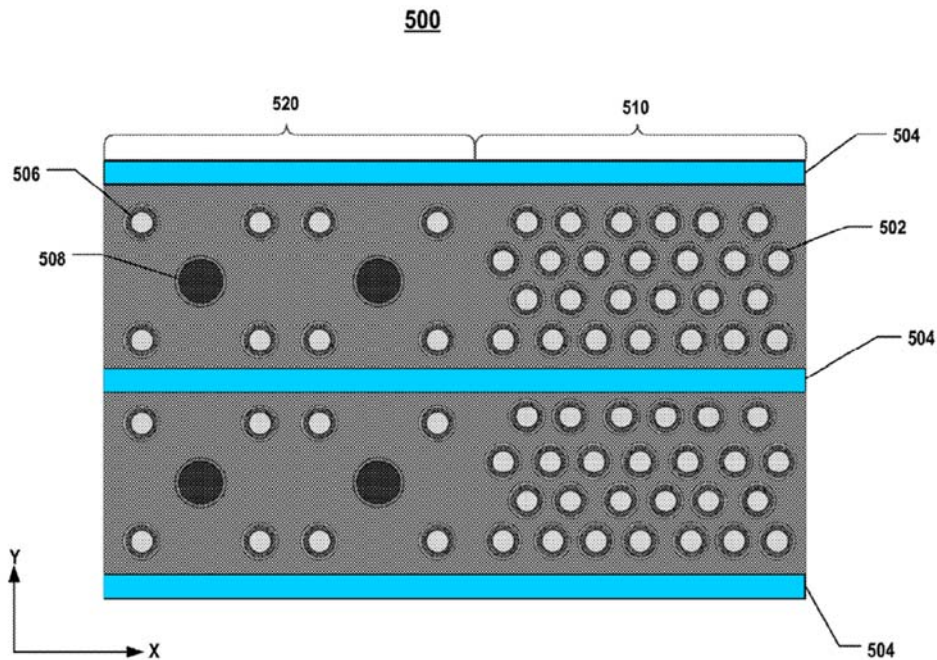


FIG. 5

Ex. 1001, Fig. 5 (annotated).

The '872 solves this issue, for example, by “**replacing** the GLSs” with “a plurality of dummy source structures,” each which “extend[s] vertically” through the staircase structure on “one side of the memory stack.” Ex. 1001, 1:39-42, 5:31-36 (emphasis added). That is, the claimed invention of the '872 allows for “**removing** GLSs from the staircase region” altogether. Ex. 1001, 8:22-23 (emphasis added). The dummy source structures can be “arranged in a pattern” such that gate electrodes or gate lines are formed with “improved uniformity and quality.” Ex. 1001, 4:43-52. The specific arrangement of the dummy source structures, as taught

by the '872, is advantageous because it allows the deposited conductive material to travel “shorter distances to fill up the lateral recesses,” thus allowing the formed structures to be “less susceptible to voids or density nonuniformity.” Ex. 1001, 4:52-58.

An exemplary arrangement of **dummy source structures** is depicted in the plan view in the color-annotated version of the '872's Fig. 1A, below. The **dummy source structures** are “arranged in a pattern,” meaning in an arrangement that is “repeated at a regular interval.” Ex. 1001, 7:61-8:1. The '872 further teaches that the **dummy source structures** “surround **staircase contacts 122** of nominally same lateral distances to the respective **staircase contacts 122**” so that, as one example, the deposited “conductive material for forming the gate electrodes may travel nominally same distances to surrounding lateral recesses” to fill the lateral recesses, which “facilitat[es]” the fabrication process such that the gate electrodes are formed “with improved uniformity and quality” and “warpage bias” of the memory device is reduced. Ex. 1001, 8:25-34, 8:45-49. The '872 emphasizes that the “symmetrical architecture” of dummy source structures is advantageous because it “can improve the performance and efficiency of etching processes,” which are additional processes in fabricating the memory device. Ex. 8:49-51. The '872 further teaches that the **dummy source structures** are “located adjacent to **staircase contact 122**,” meaning there are “no other components”

between staircase contact 122 and each of the dummy source structures. Ex. 1001, 6:41-46. The '872 further teaches “at least two **dummy source structures**” are “arranged in a **first row 132** that extends along a first lateral direction,” which is the x-direction that is left-to-right, as shown in Fig. 1A below. '872, 6:51-54; *see also* '872, 2:38-40.

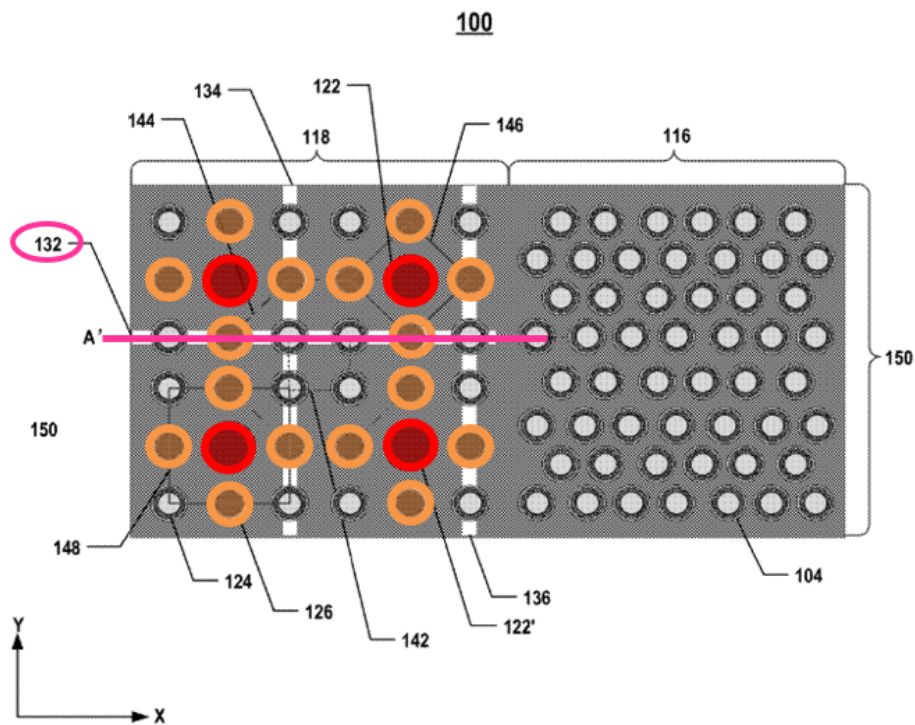


FIG. 1A

Ex. 1001, Fig. 1A (annotated).

Other exemplary images of the dummy source structure arrangement entail arranging the dummy source structures symmetrically around **staircase contacts 122**, such that each structure is nominally the same lateral distance to the respective **staircase contacts 122**. Additionally, in each of the embodiments of

the '872, each of the **dummy source structures** is located adjacent to a **staircase contact 122**, such that there are no other components located between. These arrangements are depicted in Figs. 1B-1C, below. The '872 does not include any illustrations of the dummy source structure arrangement in plan view other than those depicted in Figs. 1A-1C.

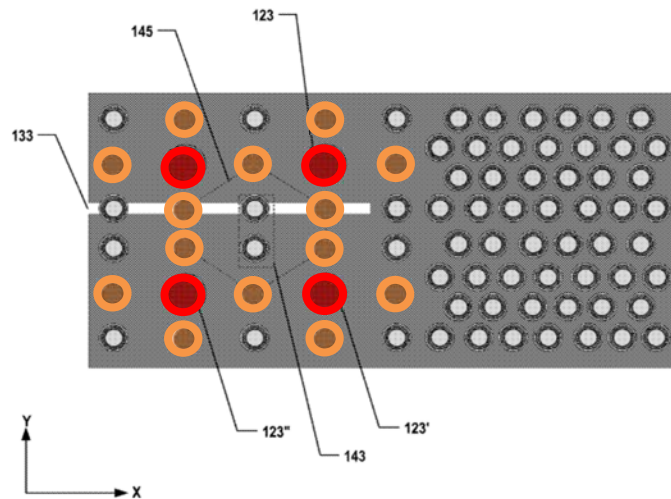


FIG. 1B

Ex. 1001, Fig. 1B (annotated).

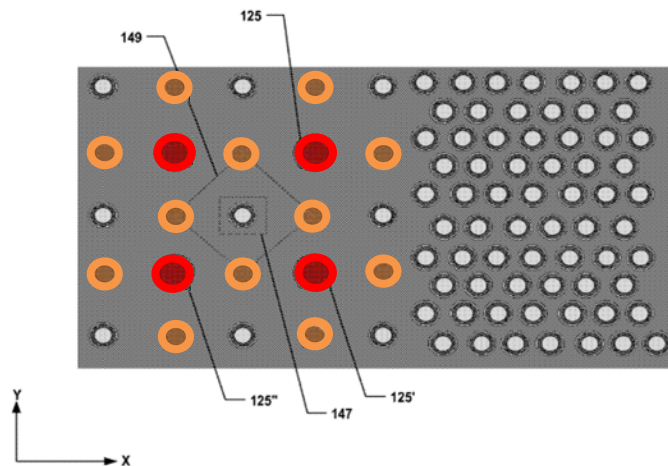


FIG. 1C

Ex. 1001, Fig. 1C (annotated).

The memory structure of the '872 also includes an “array of **dummy channel structures**” in staircase region 118, annotated in Fig. 1A below. '872, 1:48-50; *see also* '872, 6:31-37. The **dummy channel structures** are included in the memory device because they “prevent oxide layer bending” and “further increase the stability of [the] staircase region [] during etching processes.” '872, 4:33-37, 8:42-45. The **dummy channel structures** are interleaved with the dummy source structures within the staircase region. '872, 7:9-10. For example, the **dummy source structures** are arranged among the array of **dummy channel structures**. '872, 7:10-14. Each **dummy channel structure** “extends vertically through” the staircase structure. '872, 11:25-28. Like the dummy source structures, each **dummy channel structure** “surrounds a **staircase contact**.” '872, 6:60-62. These structures are arranged “symmetrical[ly]” as to “improve the performance and efficiency of etching processes.” '872, 8:49-51. For instance, the **dummy channel structures** may be “evenly distributed around” the **staircase contact**, maintaining “nominally equal lateral distances” from it. '872, 6:62-67, 11:31-33. Additionally, the arrangement entails that at least two of the **dummy channel structures** are “arranged in a **third row 136** that extends along a third lateral direction,” which is “parallel to the y-direction.” '872, 7:1-4; *see also* '872, 7:4-8.

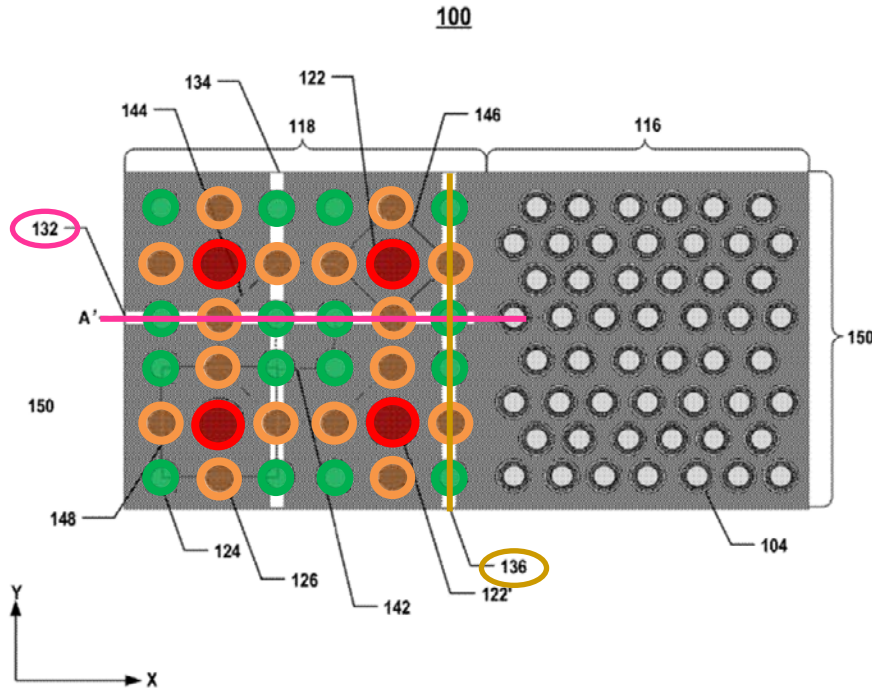


FIG. 1A

Ex. 1001, Fig. 1A (annotated).

The memory device of the '872 includes: (1) **substrate** with “two lateral surfaces extending laterally in the x-y plane” (Ex. 1001, 9:3-5); (2) “**memory stack 160**” that includes “interleaved conductive layers 106 and dielectric layers 108” and “a staircase structure 175” on “[a]t least [] one side in the lateral direction” (Ex. 1001, 9:67-10:3); (3) “dummy source structure 178” that includes “a dummy source hole filled with conductive materials as **a contact 179**”; and (4) a “spacer 177 made of any suitable dielectric materials (e.g., silicon oxide) between contact 179 and memory stack 160 to electrically separate surrounding conductive layers 106 in memory stack 160 from contact 179” (Ex. 1001, 11:39-43). A cross-section view of the memory device, depicting the

dummy source structure, is below.

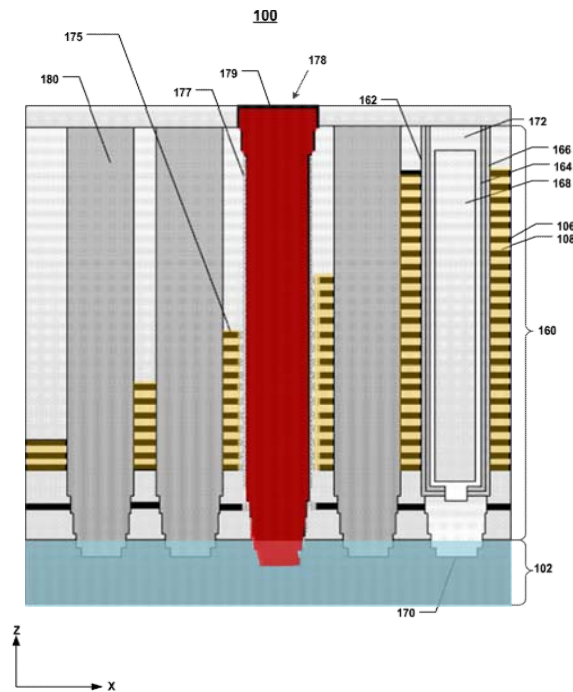


FIG. 1D

Ex. 1001, Fig. 1D (annotated).

The Challenged Claims include and depend from claim 7, which depends from claim 5, which depends from independent claim 1. These claims are directed to aspects of the above-described invention:

[1.pre] A three-dimensional (3D) memory device, comprising:

[1.a] a substrate;

[1.b] a memory stack comprising interleaved conductive layers and dielectric layers on the substrate;

[1.c] a staircase structure on one side of the memory stack;

[1.d] a staircase contact in the staircase structure; and

[1.e] a plurality of dummy source structures each extending vertically through the staircase structure, the plurality of dummy source structures surrounding the staircase contact,

[1.f] wherein each of the dummy source structures comprises a conductive contact.

[5] The 3D memory device of claim 1, wherein in a plan view, at least two of the plurality of dummy source structures are arranged in a first row that extends along a first lateral direction.

[7] The 3D memory device of claim 5, further comprising a plurality of dummy channel structures surrounding the staircase contact, each dummy channel structure extending vertically through the staircase structure.

III. FILE HISTORY

The claims of the '872 remain patentable over the prior art for at least the same reasons identified during prosecution. As discussed further below in §VI, the prior art does not disclose or render obvious, *inter alia*, the claimed “dummy source structures” that comprise a “conductive contact” of the '872. Claims directed to this limitation were allowed after extensive prosecution and consideration of numerous prior art references.

The '872 was filed on May 2, 2019. During the pendency of the '872 patent application, Applicant was required to restrict the invention to that of a “three-dimensional (3D) memory device” or “a method for forming” the same. Ex. 1002

(Part 1 of 2), 458 (5/21/2020 Requirement for Restriction/Elections). Applicant elected claims that restricted the invention of the '872 to that of a “three-dimensional (3D) memory device.” Ex. 1002 (Part 1 of 2), 466 (5/22/2020 Applicant Arguments/Remarks Made in an Amendment).

The Examiner then rejected the claims under 35 U.S.C. § 102(a)(1) as being allegedly anticipated by and under 35 U.S.C. § 103 as being allegedly obvious over U.S. Pub. No. 2016/0293622 (“Jeong”). Ex. 1002 (Part 1 of 2), 468-78 (6/11/2020 Office Action). In supporting this assertion, the Examiner mapped the '872's claimed “plurality of dummy source structures” to Jeong's “dummy pillars” because “like the dummy source of the instant application, [they] function as a mechanical support for conductive layers” of a memory stack. Ex. 1002 (Part 1 of 2), 470, 474, 476-77 (6/11/2020 Office Action). During a telephonic Applicant-initiated interview, Applicant discussed with the Examiner the distinction between the claimed “dummy source” and the “dummy pillar” of Jeong. Ex. 1002 (Part 1 of 2), 505 (8/14/2020 Applicant-Initiated Interview Summary, Office Action Appendix). Based on these discussions, Applicant subsequently filed an amendment to the claims, further limiting the independent claims to recite, “wherein each of the dummy source structures comprises a conductive contact.” Ex. 1002 (Part 2 of 2), 510, 513 (8/18/2020 Request for Reconsideration After Non-Final Rejection). Applicant stated that the “dummy pillars in Jeong are different from the claimed

‘dummy source structure’ in amended independent claims 1 and 8 at least because the dummy pillars do not include conductive contacts,” explaining:

Nothing in Jeong’s pillar is conductive contact, as the pillar consists of insulating layers, a semiconductor pattern, and a charge storage layer. By contrast, as explained at paragraph [0057] of the present application: ‘In some embodiments, ***dummy source structure 178 includes a dummy source hole filled with conductive materials as a contact 179.*** Dummy source structure 178 can further include a spacer 177 made of any suitable dielectric materials (e.g., silicon oxide) between contact 179 and memory stack 160 to electrically separate surrounding conductive layers 106 in memory stack 160 from contact 179. As a result, dummy source structures 178 can laterally separate 3D memory device 100 into multiple memory regions, such as memory blocks.’

Id., 514-15 (emphasis added). The Applicant reiterated that the claimed “dummy source structure” includes “a contact” made of “conductive materials,” and that Jeong’s structure made solely of “insulating layers,” a layer containing a “semiconductor pattern,” and a “charge storage layer” did not meet this criterion. *Id.* In making this argument, the Applicant cited to a section of the specification that additionally states that the claimed “dummy source structure” ***can*** function to “laterally separate” the three-dimensional memory device into “multiple memory regions” ***to the extent that*** the “dummy source structure” includes “a spacer [] made of any suitable dielectric materials,” such as “silicon oxide,” situated “between contact 179 and memory stack 160.” *Id.* Neither the spacer nor the functionality of laterally separating the memory device into regions of memory is recited in any of the independent claims of the ’872. As such, these features were not necessary to

overcome the prior art of record.

The Examiner subsequently allowed all pending claims and did so after reviewing four additional prior art references identified by the Applicant in a later-submitted Information Disclosure Statement.³ Ex. 1002 (Part 2 of 2), 1-6 (10/26/2020 Notice of Allowance), Ex. 1002 (Part 2 of 2) 1-2 (10/30/2020 Information Disclosure Statement), Ex. 1002 (Part 2 of 2), 236-37 (11/9/2020 Notice of Allowance) (“The reasons for allowance have not changed since the previous Office Action (Notice of Allowance, mailed on 10/26/2020).”). The Examiner stated in the Reasons for Allowance that the prior art of record does not teach or render obvious the limitation “*wherein each of the dummy source structures comprises a conductive contact.*” Ex. 1002 (Part 2 of 2), 7 (10/26/2020 Notice of Allowance) (emphasis in the original). The Examiner further stated, “the individual limitations

³ Petitioner incorrectly asserts that “Examiner did not consider any other prior art references in connection with or following the August 14, 2020 claim amendments.” Pet., 28. An Information Disclosure Statement, which identified an additional four foreign patent documents, was submitted by Applicant on October 30, 2020, complied with the provisions of 37 C.F.R. § 1.97, and was considered by the Examiner. Ex. 1002 (Part 2 of 2) 1-2 (10/30/2020 Information Disclosure Statement), Ex. 1002 (Part 2 of 2), 237 (11/9/2020 Notice of Allowance).

may be found in a plurality of prior arts but there is no motivation to combine,” and “[b]ecause no reference alone teaches all the limitations, nor is there any motivation to combine the prior arts to construct all the limitations of” independent pending claims 1 and 8, the independent claims are “deemed patentable over the prior arts.” *Id.*, 7-10. The ’872 issued on December 8, 2020 with twenty claims. Ex. 1002 (Part 2 of 2), 272 (Issue Notification).

IV. CLAIM CONSTRUCTION

Petitioner relies on substantively identical claim construction arguments regarding the same two claim terms “dummy source structures” and “surrounding” as it presented in its previously-filed petition, IPR2024-00789. Pet. 1. Petitioner does not identify any other terms for construction. Accordingly, Patent Owner provides substantively similar rebuttal arguments for these claim terms.

The Board construes claim terms “using the same claim construction standard that would be used to construe the claim in a civil action.” §42.100(b). Under this standard, claim terms are “generally given their ordinary and customary meaning” to a person of ordinary skill in the art. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (*en banc*). A person of ordinary skill in the art (“POSITA”) ascertains the meaning of the claims based on the claim language, specification, prosecution history, and relevant extrinsic evidence, although the claims and patent specification are the primary sources for construing claims. *Id.*, 1314-16.

The parties have exchanged preliminary proposed claim constructions in the parallel district court proceeding, which includes the term “dummy source structure” but does not include “surrounding.” *See* Ex. 2001 (Joint Claim Construction Statement). The Petition raises proposed constructions for two terms: “dummy source structure” and “surrounding,” which Patent Owner addresses below. Other than the terms “dummy source structure” and “surrounding,” Patent Owner submits that constructions of the claim terms are not necessary to assess whether the prior art reads on the Challenged Claims for the purposes of institution. Patent Owner, however, reserves the right to modify its proposed constructions and to raise further claim construction issues if the Board institutes IPR, and to raise claim construction issues in the underlying district court proceedings.

A. “dummy source structure” (Challenged Claims 7-10, and Previously-Challenged Claims 1-6, 11-13)

The term “dummy source structure” should be construed according to its plain and ordinary meaning as a structure that does not function as a source. Petitioner proposed construing this term as “structure[s] that occupies the void that was used for the gate replacement process,” but Petitioner’s proposal fails to differentiate between “dummy” source structures and non-dummy source structures and would impermissibly limit the language of an apparatus according to the process by which the apparatus is made.

1. Patent Owner's Construction Is Supported by the Intrinsic Evidence

Consistent with the plain and ordinary meaning and the intrinsic record, “dummy source structure” should be construed as a structure that does not function as a source to the memory cells. The claim term at issue is “dummy source structure” rather than “source structure,” and Patent Owner’s construction properly gives meaning to the word “dummy.”

Moreover, the '872 teaches that the dummy source structures do not function as a source to the memory cells. “[S]ource” is used consistently in reference to source to gates of the memory cells. *See, e.g.*, '872, 16:33-38, 11:8-9. Whereas, the “dummy source structures”—as the qualifying term “dummy” suggests—“function[] as a mechanical supporting structure” ('872, 16:38-44), rather than source structures. And while the '872 teaches that the dummy source structures may function as “interconnects to connect 3D memory device 100 with *other* peripheral devices,” the '872 nowhere describes the dummy source structure functioning as a source to the memory cells. *See, e.g.*, '872, 5:40-43, 11:46-49. As the specification explains, the dummy source hole is filled with “dielectric materials, conductive materials, or any combination thereof” so that a “dummy source structure 246 including spacer 242 and contact 244 is thereby formed in the dummy source hole.” Ex. 1001, 16:28-31, 16:56-63. “When conductive materials are used to fill dummy source hole 212 (e.g., contact 244), the dummy source

structure 246 may function as an interconnect to connect 3D memory device 100 with other peripheral devices,” and “[w]hen dielectric materials are used to fill dummy source hole 212, dummy source structure 246 may function as a mechanical support structure to improve the stability of the staircase region.” Ex. 1001, 16:63-17:3. At no point does the specification suggest that a dummy source structure can function, in contradiction to its name, as a source to the memory cells.

In the first IPR challenging the '872, Petitioner premised its arguments on misunderstandings of the specification. Specifically, Petitioner's reliance on the following passage is misplaced as it never says that a “dummy” source structure is the same as a “source structure”: “In some embodiments, dummy source structure 246 may not connect to channel structures in the inner region.” '872, 16:38-40. Even if the use of the permissive “may” language in the '872 suggests embodiments of a dummy source structure may or “may not connect to channel structures,” neither teaching suggests that dummy source structures “function as a source to the memory cells.” For example, while one end of the dummy source structure may connect to channel structures via the substrate, the other end of the dummy source structure may be an electrical dead end or may connect to peripheral devices. And while the '872 explains that “the dummy source structure 246 may function as an interconnect to connect 3D memory device 100 with other

peripheral devices,” it does not teach that the dummy source structure may function as an interconnect to a supply that provides source to the memory cells. ’872, 16:66-17:3 (emphasis added). There is simply no teaching that the dummy source structure provides a source to the memory cells. PO’s construction is consistent with all disclosed embodiments.

As such, “dummy source structure” should be construed as a structure that does not function as a source to the memory cells.

2. Petitioner’s Proposed Construction Fails to Give Meaning to “Dummy” Source Structure, and Improperly Limits the Term to a Process of Manufacture

Petitioner’s proposal that “dummy source structure” should be construed as a “structure that occupies the void that was used for the gate replacement process” fails to differentiate between “dummy” source structures and non-dummy source structures, and would impermissibly limit the language of an apparatus according to the process by which the apparatus is made.

First, Petitioner’s proposed construction is improper because it ignores the plain meaning of the term and fails to differentiate between dummy source structures and non-dummy source structures (*i.e.*, actual source structures that function as the source for memory cells). *See Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1119 (Fed. Cir. 2004) (rejecting “interpretation [that] largely reads the term ‘operatively’ out of the phrase

‘operatively connected’”). “[D]ummy” is a descriptor of “source structure,” and should be given meaning when construed. *Littelfuse, Inc. v. Mersen USA EP Corp.*, 29 F.4th 1376, 1381 (Fed. Cir. 2022) (“give meaning to the term ‘fastening stem’ by looking to the meaning of the words ‘fastening’ and ‘stem’ as used in the patent”).

Indeed, structures that occupy (or are formed from) voids used for gate replacement processes can be either dummy source structures, if they do not function as a source, or source structures if they do function as a source for the memory cells. Petitioner ignores the distinction between the two types of structures and their functions. A dummy source structure was a type of dummy structure that was used for the purposes of improving integrated circuit functionality and manufacturing yield. For example, dummy structures mimic the physical properties of non-dummy structures, but do not perform the primary function of its non-dummy counterpart—functioning as the source. Instead, dummy structures can serve, for example, as load-bearing structures during semiconductor device fabrication, which reduces mechanical stress on non-dummy structures during fabrication. ’872, 5:5:21-48. For instance, while dummy source structures may be comprised of conductive material and thus may function, *e.g.*, as an “interconnect between the 3D memory device and peripheral devices” (’872, 5:37-43), they do not function as the source for memory cells. Petitioner’s

proposed construction ignores this key difference and does not properly distinguish between dummy and non-dummy source structures.

Second, Petitioner’s proposed construction impermissibly attempts to limit the language of an apparatus—here, the claimed three-dimensional memory device—in such a way as to dictate the process by which the apparatus is made. As the Federal Circuit has held, “[a] novel product that meets the criteria of patentability is not limited to the process by which it was made.” *Vanguard Prods. Corp. v. Parker Hannifin Corp.*, 234 F.3d 1370, 1372-73 (Fed. Cir. 2000). And, while “process steps can be treated as part of a product claim if the patentee has made clear that the process steps are an essential part of the claimed invention,” that is not the case here. *See Cont’l Circuits LLC v. Intel Corp.*, 915 F.3d 788, 799 (Fed. Cir. 2019).

Here, the Challenged Claims are directed to an apparatus—not a product by process or method of manufacture. Indeed, as discussed in connection with §III, during prosecution Applicant expressly elected to restrict the invention to the claimed 3D memory device to the apparatus itself, and not to any process by which the device or its features are made. Ex. 1002 (Part 1 of 2), 458 (5/21/2020 Requirement for Restriction/Elections).

Third, Petitioner also has not shown that the “gate replacement process” required by its construction is an essential part of the claimed invention such that it

should be read into the claims through the construction of “dummy source structure.” Petitioner does not cite to any lexicography or disclaimer that would support such a construction. Instead, Petitioner relies on one disclosure, which, in full, reads:

“Also, the arrangement of the dummy source structures may allow the gate electrodes/word lines to be formed with improved uniformity and quality, reducing the resistivity of the gate electrodes/word lines. ***For example, the gate-replacement process can be performed to deposit a conductive material through the dummy source holes that subsequently form the dummy source structures.*** Because the conductive material travels shorter distances to fill up the lateral recesses for forming the gate electrodes, the gate electrodes are less susceptible to voids or density nonuniformity.”

Pet., 30-31 (citing ’872, 5:49-58) (emphasis added). This statement, on its face, is merely an “***example***” of how the claimed dummy source structures “***can***” be formed and does not suggest that “a gate-replacement process” is an essential part of the claimed invention. Indeed, the specification repeatedly qualifies the use of the “gate-replacement process” as merely one possible manufacturing method. See *e.g.*, ’872, 4:30-33 (“[A] gate-replacement process is ***often*** used”), 5:52-55 (“the gate-replacement process ***can*** be performed to deposit a conductive material

through the dummy source holes”), 16:40-49 (“***In some embodiments*** ... dummy source structure 246 ***may***...function[] as a mechanical supporting structure after gate-replacement process.... ***In some embodiments***, ... dummy source structure 246 ***may*** ... still reach the lower part of the dielectric stack to carry out the gate-replacement process.”). In addition, the ’872 teaches that the dummy source structures can be formed a number of ways using “one or more thin film deposition processes including ALD [atomic layer deposition], CVD [chemical vapor deposition], PVD [physical vapor deposition], any other suitable processes, or any combination thereof.” Ex. 1001, 13:55-64; *see also* Ex. 1001, 12:34-36 (defining acronyms), 19:61-20:2 (explaining that “Summary and Abstract sections may set forth one or more but not all exemplary embodiments of the present disclosure as contemplated by the inventor(s)” and that the “breadth and scope of the present disclosure should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the [] claims and their equivalents”).

Finally, Petitioner’s construction attempts to impermissibly narrow the scope of the claim by limiting it to one particular disclosed embodiment: gate replacement process. *See In re Am. Acad. of Sci. Tech. Ctr.*, 367 F.3d 1359, 1369 (Fed. Cir. 2004) (“We have cautioned against reading limitations into a claim from the preferred embodiment described in the specification, even if it is the only

embodiment described, absent clear disclaimer in the specification.”); *see also* *Superguide Corp. v. DirecTV Enterprises, Inc.*, 358 F.3d 870, 875 (Fed. Cir. 2004); *Liebel-Flarsheim Co. v. Medrad Inc.*, 358 F.3d 898, 906 (Fed. Cir. 2004) (discussing recent cases wherein the court expressly rejected the contention that if a patent describes only a single embodiment, the claims of the patent must be construed as being limited to that embodiment).

For each of these reasons, the Board should reject Petitioner’s proposal to construe “dummy source structure” as a “structure that occupies the void that was used for the gate replacement process.”

B. “surrounding” (Challenged Claims 7-10, and Previously-Challenged Claims 1, 13)

The term “surrounding” should be given its plain and ordinary meaning, which, contrary to Petitioner’s arguments, requires features that are more than just on two sides with another structure “between.”

As an initial matter, the Board need not resolve the full scope of “surrounding” and need not determine whether it requires “fully encircling.” Petitioner has alleged that the claimed “plurality of dummy source structures surrounding the staircase contact” of Claim 1 is satisfied “by structures on two sides” of the object. Pet., 65; *see generally* Pet., 54-66. Similarly, Patent Owner’s arguments directed to this limitation (§VI.A.1) turn on whether “surrounding” encompasses structures on only two sides. Thus, the Board need only resolve

whether “surrounding” encompasses structures on only two sides. The Board does not need to reach Petitioner’s purported clarification that “surrounding” does not “require fully encircling” because the Board is required to construe terms “only to the extent necessary to resolve the controversy.” *Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019).

The term “surrounding” does not encompass features that are merely on two sides. First, the claim term at issue is “surrounding” rather than “between.” Indeed, the claims expressly distinguish the concepts of “surrounding” and “between.” The term “between” is used when reciting the concept of being located in the middle of two structures and “surrounding” is used when reciting the concept of being located in the middle of more than two structures. *Compare* ’872 Claim 17 (“wherein at least *one dummy channel structure is surrounded by at least eight dummy source structures*”) with ’872, Claim 11 (“wherein at least *one dummy source structure is located between the first and second staircase structure*”); *see also, e.g.*, Claim 12, Claim 15, Claim 16.

The ’872 specification likewise repeatedly uses the terms “surrounding” and “between” to describe different concepts. As in the claims, the specification uses “between” when discussing the concept of being located in the middle of two structures and “surrounding” when discussing the concept of being located in the middle of more than two structures:

As shown in FIG. 1A, multiple dummy source structures, such as the four dummy source structures indicated by a diamond shape 146, may surround a staircase contact, such as staircase contact 122. ... [¶] ...

A plurality of dummy channel structures, such as the four dummy channel structures indicated by square shape 148, may surround a staircase contact. The four dummy channel structures may be spaced with nominally equal lateral distances to the staircase contact, as shown in FIG. 1A. In other words, the dummy channel structures surrounding a staircase contact may be evenly distributed around the staircase contact. ... [¶] ... In some embodiments, at least one dummy source structure may be located between two staircase contacts. For example, FIG. 1A shows that two dummy source structures are located between staircase contacts 122 and 122'. FIG. 1B shows another embodiment in which two dummy source structures are located between staircase contacts 123 and 123', while one dummy source structure is located between staircase contacts 123' and 123". FIG. 1C shows yet another embodiment in which one dummy source structure is located between staircase contacts 125 and 125', and one dummy source structure is located between stair case contacts 125' and 125". Other numbers of dummy source structures may also be disposed between two staircase contacts."

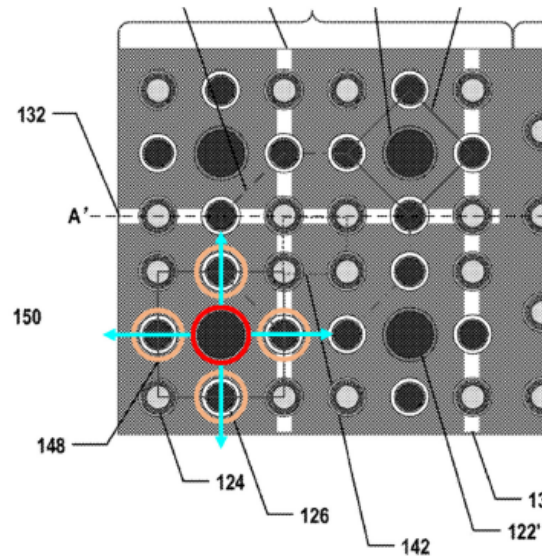
'872, 6:38-7:28 (emphasis added). This distinction is used consistently throughout the specification, including when the structures are slits. '872, 4:56-61 ("[D]ummy channel holes are formed between adjacent GLS").

Nothing in the '872 teaches that a staircase contact can be "surrounded" by

just two dummy source structures. If structures placed on only two sides of an object was within the scope of the plain meaning of “surrounding,” then there would have been no need for the ’872 to consistently use different terminology—“located between”—when there are structures on just two sides.

Petitioner’s argument that the specification contemplates “less than four dummy source structures that ‘surround’ a word line contact” (Pet., 33 (citing ’872 8:8-11)) is irrelevant. The dispute is not whether less than four (*e.g.*, three) dummy structures can “surround” a word line contact, the dispute is whether exactly two parallel dummy structures can “surround” a word line contact.

Petitioner argues that Figure 1A demonstrates that “‘surrounded includes being able to draw four lines outward from the staircase contact with each line being separated from the others by 90 degrees and intersecting a dummy source structure” (Pet., 35), but this argument is convoluted and a far departure from the plain meaning of “surrounding.” Even if “surrounding” was defined by some minimum angle between structures (as described by Petitioner), Figure 1A illustrates a separation of 90 degrees from the **center** of such structures:



Pet., 36 (Petitioner’s annotations). Thus, this configuration disclosed in the specification with four dummy source structures at 90 degrees is different from—and does not provide support for—a configuration having only two dummy structures, *i.e.* where the angle is 180 degrees.

Finally, Petitioner’s extrinsic evidence should be given little weight. Petitioner fails to explain the relevance that a lay description of an “isthmus” (provided by the website “<https://www.studycountry-com/wiki/what-is-a-piece-of-land-surrounded-by-water-on-2-sides>” in March of 2024) has to the meaning of “surrounding” as used by the ’872. Pet., 37 (citing Ex. 1018). Similarly, Petitioner’s reliance on U.S. Pat. No. 9,530,492 (the “’492 patent”) is misplaced. Pet., 37 (citing Ex. 1019, 2:14-16). Although the ’492 patent states that “the conventional SBPI operations are strongly affected by the stored Vts of two surrounding NAND cells dispersed in the adjacent left and right BLs” (Ex. 1019,

2:14-16), this passage is merely referring to the effects of NAND cells in the surroundings (*i.e.*, in the vicinity). The '492 patent does not suggest that two NAND cells can surround SBPI operations. And even if Petitioner's interpretation of the '492 patent were correct, it cannot overcome the consistent usage of "surrounding" in the '872 patent, consistent with the plain meaning.

V. BACKGROUND OF THE ASSERTED PRIOR ART

A. U.S. Patent No. 9,859,297 ("Park") (Ex. 1005)

Petitioner does not contend that Park anticipates the Challenged Claims, and instead falls back to raising obviousness arguments, which also fail.

Park discloses aspects of a memory device upon which the '872 improves. Park describes a semiconductor device including: a substrate having a cell region and stepped dummy region; a common source line ("CSL"); gate lines; insulating interlayer patterns; dummy patterns; and dummy source lines. Ex. 1005, 6:1-9:3, Figs. 1-2. Park's semiconductor device includes both **common source lines**, which function as a common source for the memory cell (and are therefore not dummy source structures), and **dummy source lines** in the dummy region. Ex. 1005, 13:53-58, 23:1-4, Fig. 1, Fig. 13. As illustrated in Figures 1 and 13 below, **common source lines** extend in the "1st direction" and "2nd direction," and are spaced apart from each other along the "3rd direction," of the cell region; the **dummy source lines**, on the other hand, extend in the "1st direction" and "3rd

direction,” and are spaced apart from each other along the “2nd direction,” of the dummy region:

FIG. 13

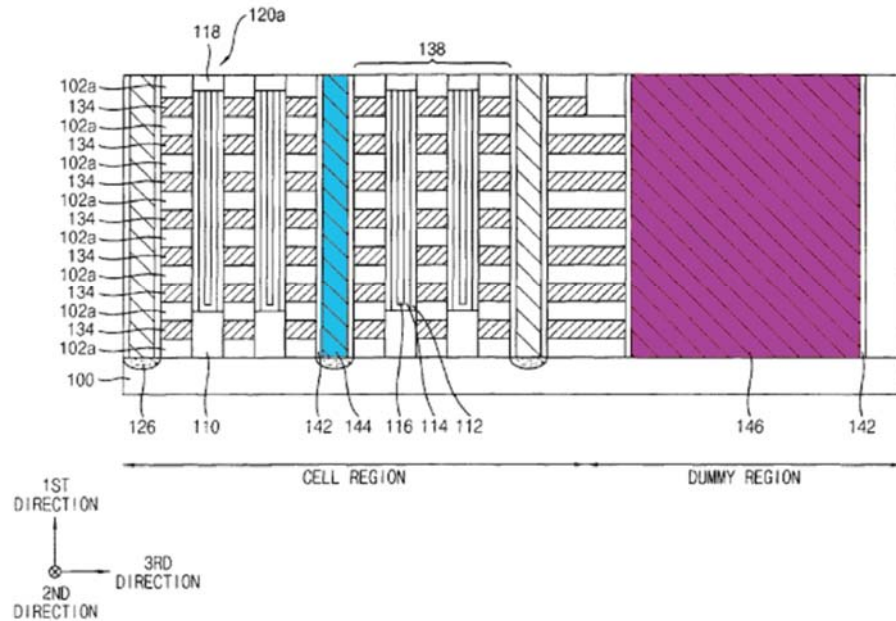
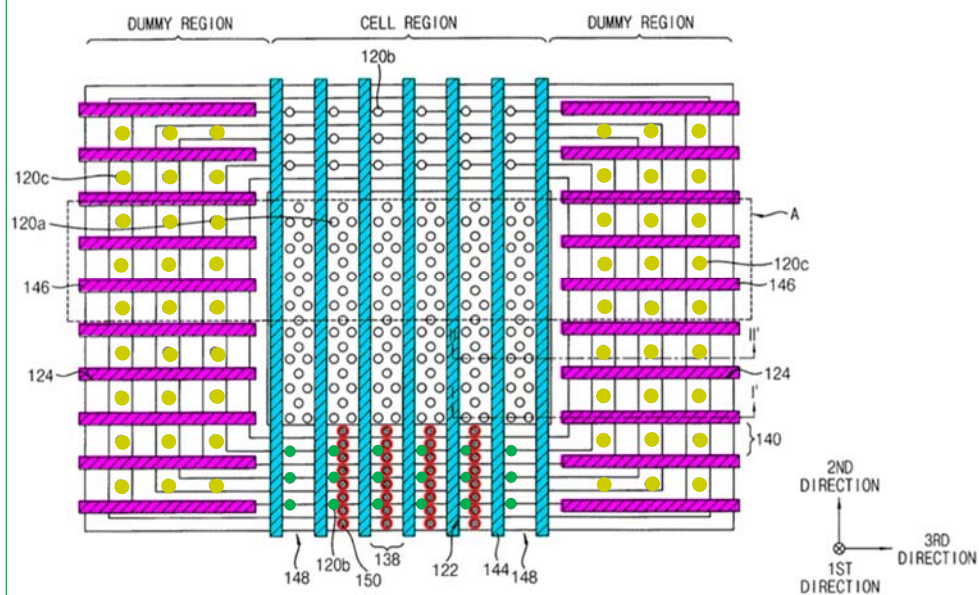


FIG. 1



Ex. 1005, Fig. 13, Fig. 1, 3:6-9.

Park further discloses that between the **common source lines** is a wiring region, where **contact plugs** (annotated in red in Figure 1 above) are formed in contact holes etched through the upper insulation layers and electrically connect to the gate lines. Ex. 1005, Fig. 1, 7:26-37, 13:60-54. Because Park's contact plugs are just between two **common source lines**, the **common source lines** do not surround the **contact plugs**. See Ex. 1005, Fig. 1. Park's **dummy source lines** also do not surround the **contact plugs** as shown above in Fig. 1. Furthermore, Park's **common source lines** are not arranged in a first row that extends along a first lateral direction because these structures instead occupy the entire region.

Park's memory device also includes **second channel structures 120b** (colored green in Figure 1 above) that are "disposed" in the wiring region. Park, 6:19-22, 7:40-41. These structures are not "surrounding" the **contact plugs** because a **common source line** acts as an intervening barrier that completely separates the **structures 120b** from the **contact plug** on one of the two sides.

Park's memory device also includes **third channel structures 120c** (colored yellow in Figure 1 above), which are "disposed" in the dummy region. Park, 8:55-57. These structures also are not "surrounding" the **contact plugs** for the same reason discussed above.

**VI. PETITIONER FAILS TO ESTABLISH A REASONABLE
LIKELIHOOD THAT IT WOULD PREVAIL WITH RESPECT TO
THE CHALLENGED CLAIMS**

Petitioner fails to establish a reasonable likelihood that it would prevail with respect to the Challenged Claims because Petitioner has failed to show that the prior art discloses or renders obvious the limitations of the Challenged Claims relating to the “dummy source structures” and “dummy channel structures.” As explained below, Petitioner asserts only that Park individually shows these features. Petitioner’s arguments fail.

First, Park does not disclose or render obvious that its alleged dummy source structures are “surrounding the staircase contact” as required by claim 1, which all the Challenged Claims depend directly or indirectly from, because the contact is merely “between” the alleged dummy source structures, and under the proper construction of “surrounding” (§IV.B), it is insufficient to be merely “between” two dummy source structures.

Second, Petitioner has not shown that Park discloses or renders obvious “dummy source structures” (as required by claim 1) because the purported dummy source structures function as a source and are therefore not “dummy source structures” as properly construed.

Third, Park does not disclose or render obvious that the purported dummy source structures in plan view are “arranged in a first row that extends along a first

lateral direction” (as required by claim 5) because the structures fill the entire cell region of the memory device, rather than merely a row.

Fourth, Park does not disclose or render obvious that its alleged dummy channel structures are “surrounding” the purported staircase contact (as required by claim 7) because there is an intervening structure—a long common source line extending the entire length of the cell region—that completely separates the alleged dummy channel structure from the staircase contract. Petitioner proposes a modification of Park to address this deficiency, but the alleged rationales do not actually motivate the specific modification of Park proposed by Petitioner, and instead the proposed modification is based on nothing more than impermissible hindsight.

Each of the above arguments apply to all of the Challenged Claims. As explained in § I (Introduction), Petitioner relies on its analysis from Ground 1 (Park) in IPR2024-00789 (the first ’872 Petition) to address the limitations of independent claim 1 and dependent claim 5, from which the Challenged Claims depend. Pet. 1. Accordingly, Patent Owner provides the same substantive arguments—the first and second arguments summarized above—to rebut Petitioner’s use of Park in this IPR with respect to claim 1. In addition, the third and fourth arguments address additional elements recited in claims 5 and 7, respectively, that are common to all Challenged Claims in this IPR. Accordingly,

any one of these four issues is sufficient to show that the Petition fails to establish a reasonable likelihood of prevailing with respect to any of the Challenged Claims.

A. Park Does Not Disclose or Render Obvious Multiple Independent Requirements of Limitation [1.e] of the Challenged Claims

Petitioner fails to show that Park discloses or renders obvious limitation [1.e]: “a plurality of dummy source structures each extending vertically through the staircase structure, the plurality of dummy source structures surrounding the staircase contact.” Park’s common source lines and dummy source lines, alone or collectively, are not “surrounding” the purported “staircase contact.” Instead, Park’s disclosures are nearly identical to the very prior art that the invention of the ’872 improves upon. Moreover, Ground 1 is reliant on Petitioner’s incorrect construction for “dummy source structure” and the misunderstanding that this term is met by Park’s common source line—it is not.

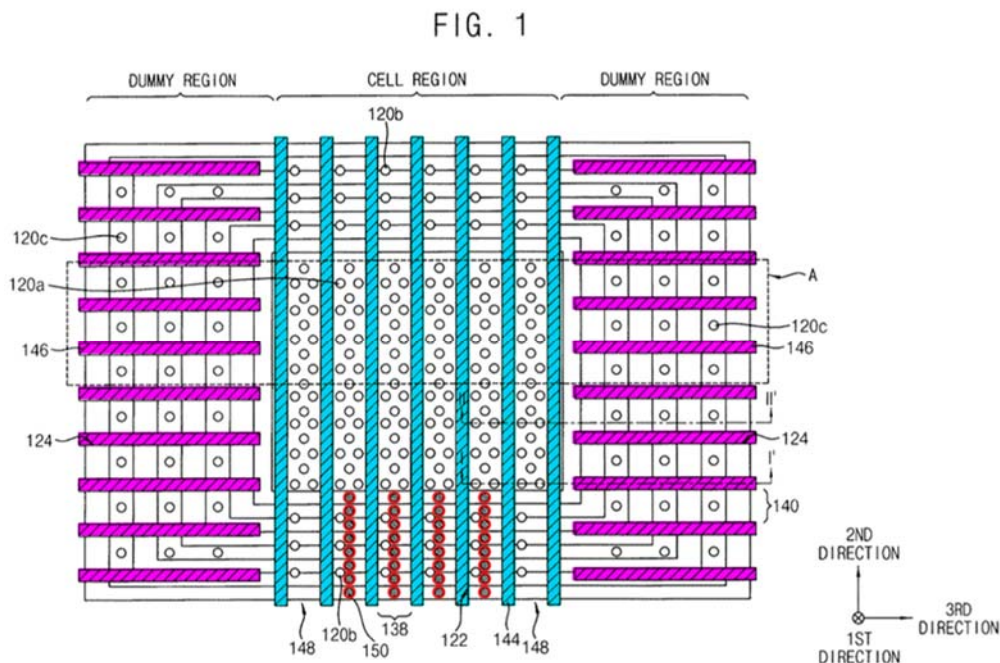
1. Park’s Common Source Lines and Dummy Source Lines, Alone or in Combination, Are Not “Surrounding” the Contact Plugs

Park’s alleged dummy source structures are not “surrounding the staircase contact” as required by the Challenged Claims because, under the proper construction of “surrounding” (§IV.B), it is insufficient for the alleged staircase contact to be merely “between” two dummy source structures.

All Challenged Claims require “the plurality of dummy source structures” to be “surrounding the staircase contact.” Petitioner maps the claimed “staircase

contact” to a subset of Park’s contact plugs 150 (Pet., 54) and maps the claimed “dummy source structures” to Park’s common source lines 144 and dummy source lines 146, collectively. *See* Pet., 54-62. Although Petitioner argues that common source lines 144 and dummy source lines 146 collectively surround the contact plugs 150 (Pet., 62), Petitioner’s explanation focuses solely on the common source lines 144 alone. *See* Pet., 62-66. Specifically, Petitioner argues that “[c]ommon source lines 144 alone surround the staircase contacts, and that is all that is necessary to satisfy claim 1.” Pet., 63-64. Nevertheless, the flaws in Petitioner’s arguments apply to both types of lines.

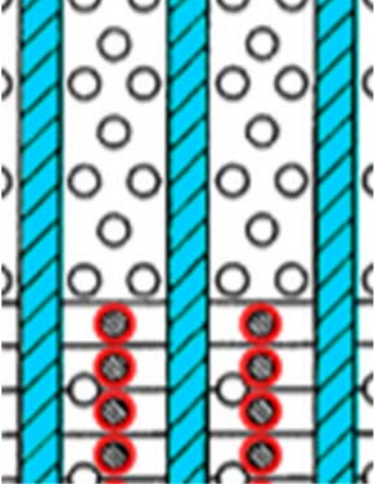
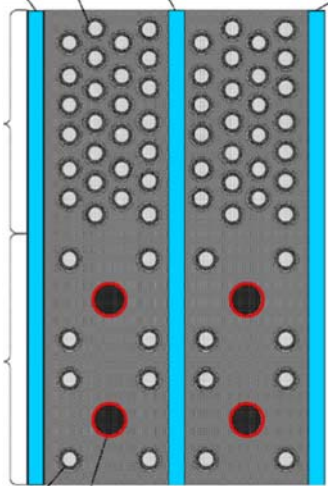
As a preliminary matter, Park’s **dummy source lines 146** do not “surround” the **contact plugs** as depicted below:



Ex. 1005, Fig. 1 (annotated). The **dummy source lines 146** are nowhere near the **contact plugs**, which is likely why Petitioner's analysis (Pet. 62-66) focuses solely on the common source lines 144. Moreover, the **dummy source lines 146** have the same deficiencies discussed below with respect to the common source lines 144.

Park's **common source lines 144** also do not "surround" contact plug 150. As discussed in §IV.B, the plain meaning of the term "surrounding" is not satisfied by structures on two sides of an object that is merely between those two structures. Under the plain meaning, there is no dispute that Park's common source lines 144 fail to disclose or render obvious this limitation.

Moreover, Petitioner overlooks that the configuration of Park's common source line 144 and contact plug 150 is precisely the configuration that the invention distinguished over the admitted prior art. Below is a side-by-side comparison of the relevant portions:

	
Excerpt of Park, Fig. 1 (highlighting contact plugs 150 in red between parallel common source line 144 in blue). <i>See also</i> Ex. 1005, 2:46-47, 5:27-33, 6:15-17; Pet. 63.	'872, Fig. 5 (rotated view of admitted prior art, illustrating staircase contacts 508 in red between parallel gate line slits 504 in blue). <i>See also</i> Ex. 1001, 5:1-14.

The '872 discloses that the prior art gate line slits (GLSs) extend through a staircase region that includes staircase contacts 508. Ex. 1001, 5:1-8. Similarly, Park's common source lines 144 cross through the wiring region that contain contact plugs 150. Ex. 1006, 13:62-64. The '872 discloses that characteristics of "the shape of GLS 504" is "a slit shape with a dimension along the extending direction (or the x-direction) much greater than the dimension along the expanding dimension (or the y-direction)." Ex. 1001, 5:23-25. Similarly, Park's common source lines 144 "extend in the second direction" in "a plan view," in which the "second direction [is] parallel to the top surface of the substrate," and much greater than in the third direction. Accordingly, Park's common source lines 144

geometry and arrangement are identical to that of the prior art GLSs that the '872 improved upon. Notably, the '872 patent uses the term “between”—not “surround”—to describe the “dummy channel holes [] between adjacent GLSs” in the admitted prior art. '872, 4:56-57. Accordingly, Park discloses, at best, the same configuration of staircase contacts “between” parallel gate line slits, rather than “surround[ed]” by dummy source structures.

Thus, under the proper construction of “surrounding” which does not include features that are merely on two sides with another structure “between,” Park’s alleged dummy source structures are not “surrounding the staircase contact” as required by the Challenged Claims.

2. Park’s Common Source Lines Are Not “Dummy Source Structures”

Petitioner has not shown that Park discloses or renders obvious “dummy source structures” because the purported dummy source structures, Park’s common source lines, function as a source and are not “dummy source structures” as properly construed.

All Challenged Claims require “a plurality of dummy source structures.” As discussed in §IV.A, the claimed “dummy source structure” is a structure that does not function as a source. While Park discloses “dummy source lines,” Petitioner instead maps the claimed “dummy source structures” to Park’s common source lines 144 (Pet., 54-62). But Park’s common source lines 144 are not dummy source

structures because they function as a source to the memory cells and are, therefore, actual—not dummy—source structures.

As an initial matter, while Petitioner alleges that Park’s common source lines 144 and dummy source lines 146 are collectively “a plurality of dummy source structures,” Petitioner maps **only** the common source lines to other limitations of the claims relating to the dummy source structure, such as the requirement that “the plurality of dummy source structures surrounding the staircase contact” as discussed above. Pet., 54-68. For example, with respect to the “dummy source lines,” Petitioner has failed to even attempt to show that they surround a contact plug, as discussed above. And with respect to the “common source lines 144,” Petitioner must show that those particular alleged dummy source structures are in fact “dummy source structures.” They are not.

Park’s common source lines 144 are not “dummy source structure[s]” because they function as a source. Park expressly distinguishes between the “common source line” for the memory cell structure, which functions as the source line, and a “dummy source line.” See, e.g., Park, 6:1-11, 7:59-60, 13:39-41. Similarly, the figures of Park show separate regions where the common source line and dummy source lines are located—the common source line is in the “cell region” and the dummy source line is in the “dummy region.” Park, Fig. 1. Thus, Park’s common source lines 144 are not dummy source structures.

Petitioner incorrectly attempts to equate Park’s common source line to the ’872 patent’s teaching that “‘dummy source structures’ can [make] ‘contact with the substrate and may provide interconnect between the 3D memory device and peripheral devices.’” Pet., 59-60 (omitting citations). Contrary to Petitioner’s suggestion, the ’872 patent’s disclosure that “dummy source structures” may “serve as an interconnect between the 3D memory devices and peripheral devices” (Ex. 1001, 5:40-43) does not suggest that Park’s common source line is also a dummy structure. Specifically, the interconnect referenced in the ’872 patent is not a source line. The ’872 explains that the “peripheral device” that the dummy source structure may connect to includes “peripheral circuits used for facilitating the operation of the 3D memory device 100, such as page buffers, decoders, and latches.” Ex. 1001, 9:37-40. As such, the ’872 “dummy source structure” does not function as a source to a memory cell. Park’s common source lines 144, on the other hand, do function as the source to memory cells, and therefore common source lines 144 are *actual* source structures and not “*dummy*” source structures.

B. Park Does Not Disclose “Dummy Source Structures” That Are “Arranged in a First Row That Extends Along a First Lateral Direction” as Required by the Challenged Claims and Recited in Claim 5

Park’s alleged dummy source structures are not “arranged in a first row that extends along a first lateral direction,” as recited in claim 5 and required by the Challenged Claims depending therefrom, because in the plan view the alleged

dummy source structures span the entire cell region and, therefore, are not “arranged in a row.”

The Challenged Claims all depend directly or indirectly from dependent claim 5, which recites the memory device of claim 1 “wherein in a plan view, at least two of the plurality of dummy source structures are arranged in a first row that extends along a first lateral direction.” For example, Figure 1A of the ’872 shows at least two dummy source structures (orange) arranged in row 132:

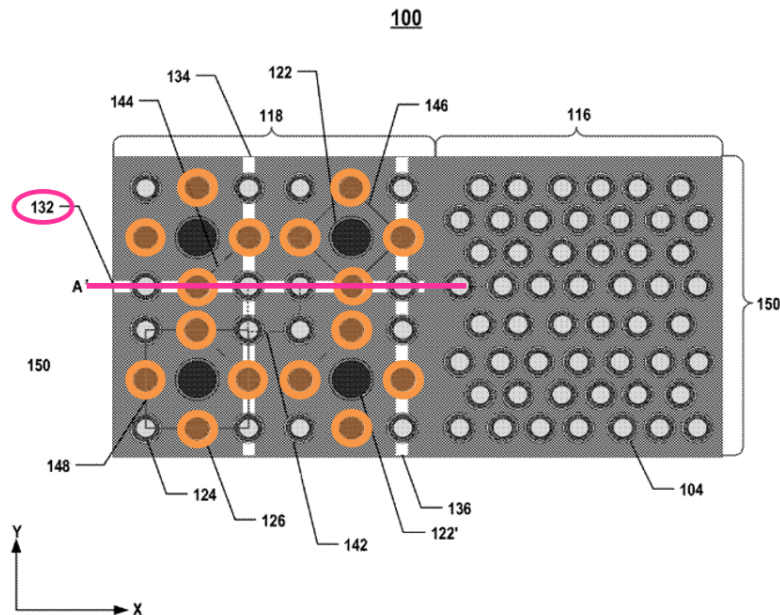


FIG. 1A

’872, Fig. 1A (annotated).

A discussed in § VI.A, Petitioner erroneously maps the claimed “dummy source structures” to Park’s common source lines 144 and dummy source lines 146. See Pet., 54-62. Petitioner likewise provides two mappings for the “at least two of the plurality of dummy source structures”: (1) the two center common

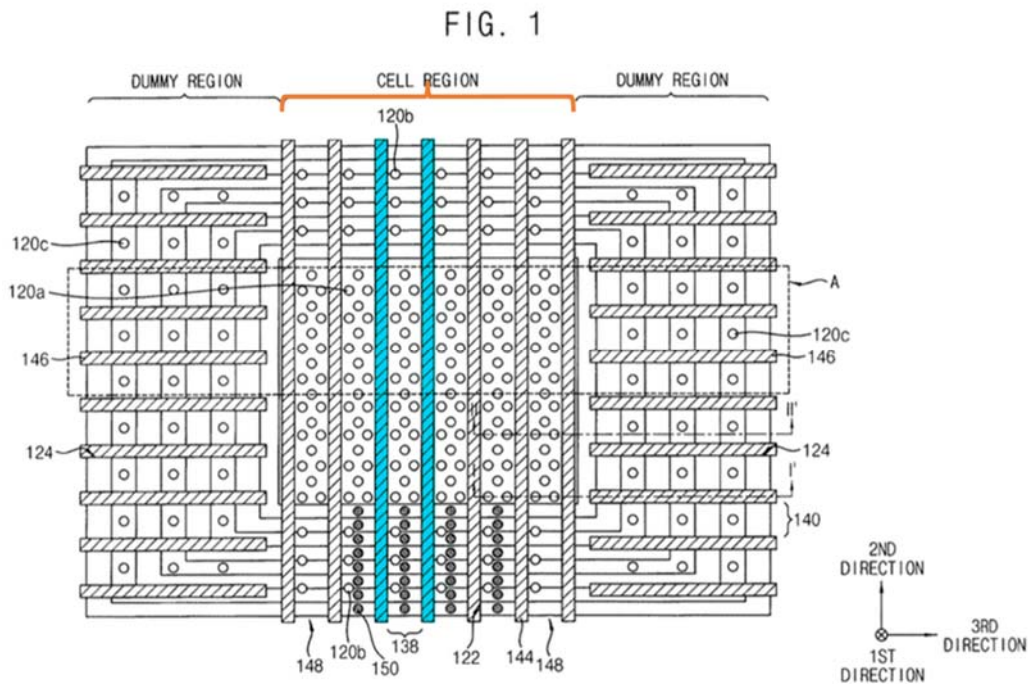
source lines and (2) the left-sided, bottom two dummy source lines. Pet., 69-71.

Petitioner cites an extrinsic definition of a row, *i.e.*, “a number of objects arranged in a usually straight line” (Pet., 70 (citing a Merriam Webster definition of “row”)), and uses a matchsticks analogy to argue that the dummy source lines in the first mapping are “like a row of match sticks going from north to south,” and thus are arranged in a first row that extends along a first lateral direction. Pet., 69-70.

Similarly, Petitioner argues that the common source lines in its second mapping are “like a row of match sticks going from west to east,” and thus are arranged in a first row that extends along a first lateral direction based on the same reasoning. Pet., 70-71.

Petitioner’s arguments are flawed—the identified structures are not arranged in a row that extends in a lateral direction in plan view. As an initial matter, as discussed in §VI.A.2, Park’s common source lines 144 are not dummy source structures because they function as a source to memory cells. And as discussed in §VI.A.1, Park’s dummy source lines 146 cannot be the claimed dummy source structures because the Petition does not map them to every element limiting the claimed dummy source structures. Specifically, Petitioner maps only the common source lines 144 to the element requiring that the claimed dummy source structures surround the contact plugs, and does not even attempt to explain how dummy source lines 146 surround a contact plug. See Pet., 62-66; § VI.A.

For the **common source lines**—the one structure that Petitioner has attempted to map to all the “dummy source structure” limitations—Petitioner further fails to show dummy source structures “arranged in a first row that extends along a first lateral direction” as required by the Challenged Claims. In Petitioner’s mapping, two of Park’s **common source lines** are adjacent to each other in a direction identified as the “3RD DIRECTION” in Park’s Figure 1:



Ex. 1005, Fig. 1 (annotated); Pet., 71. However, these **common source lines** are not “arranged in a first row.” While the **common source lines** are aligned laterally (in the “3RD DIRECTION”), they each extend across the *entire* cell region in the “2ND DIRECTION” (annotated in orange in Figure 1 above), rather than in a row.

This extension means that the **common source lines** occupy the entire space of the cell region, rather than being organized in row.

Thus, Park's alleged dummy source structures are not "arranged in a first row that extends along a first lateral direction" as required by the Challenged Claims.

C. Park Does Not Disclose or Render Obvious a Plurality of Dummy Channel Structures "Surrounding" the Staircase Contact as Required by the Challenged Claims and Recited in Claim 7

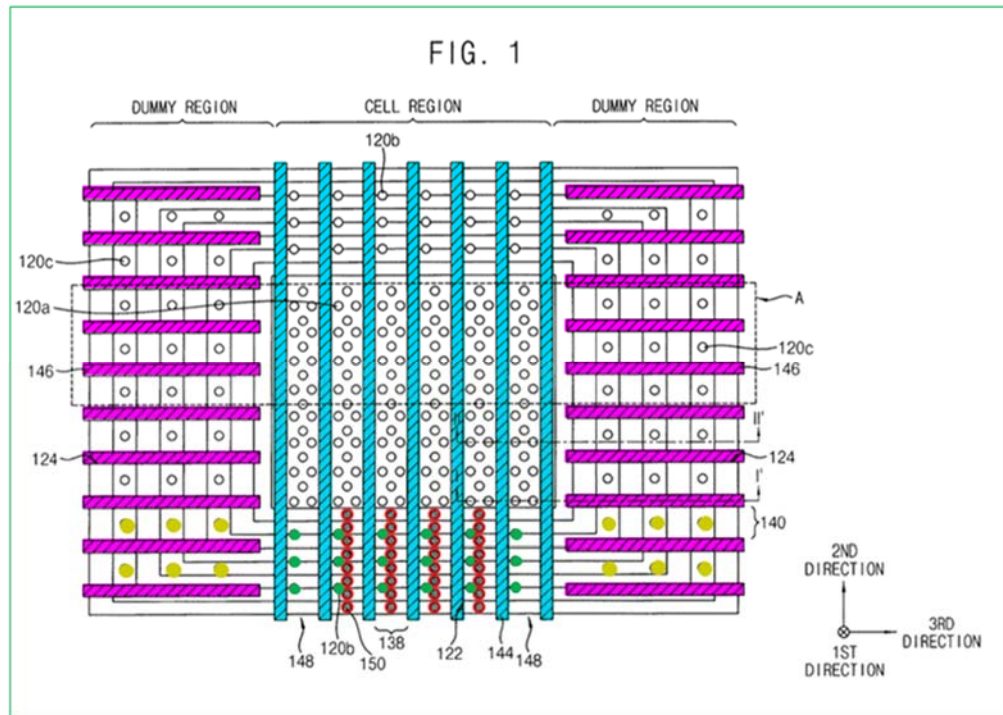
Petitioner fails to show that Park discloses or renders obvious "a plurality of dummy channel structures surrounding the staircase contact" as recited in claim 7 and required by the Challenged Claims because, under the proper construction of surrounding (§IV.B), Park's alleged dummy channel structures are not "surrounding" the alleged staircase contact. Instead, Park's staircase contacts are merely "between" adjacent structures, with one side having an intervening barrier that completely separates the alleged staircase contact from the alleged dummy channel structure. Recognizing this deficiency, Petitioner argues a POSITA would have been motivated to modify Park with additional dummy channel structures so that they surround the purported staircase contact. However, Petitioner's alleged motivations do not actually motivate the specific modification of Park proposed by Petitioner, and instead the proposed modification is based on nothing more than impermissible hindsight.

1. Park’s Alleged Dummy Channel Structures Are Not “Surrounding” a Staircase Contact

Petitioner has not shown that Park discloses that a plurality of the alleged “dummy channel structures” are “surrounding the staircase contact” because Park includes an intervening barrier on one side that completely separates the alleged staircase contact from the alleged dummy channel structure.

All Challenged Claims require that the claimed memory device further comprises “a plurality of dummy channel surrounding the staircase contact,” as recited in claim 7.⁴ Petitioner maps Park’s **contact plugs 150** to the claimed “staircase contact” (Pet., 52-54) and Park’s **second channel structures 120b** and **third channel structures 120c** (Pet., 71-73) to the claimed “dummy channel structures” (Pet., 71-73), as shown below.

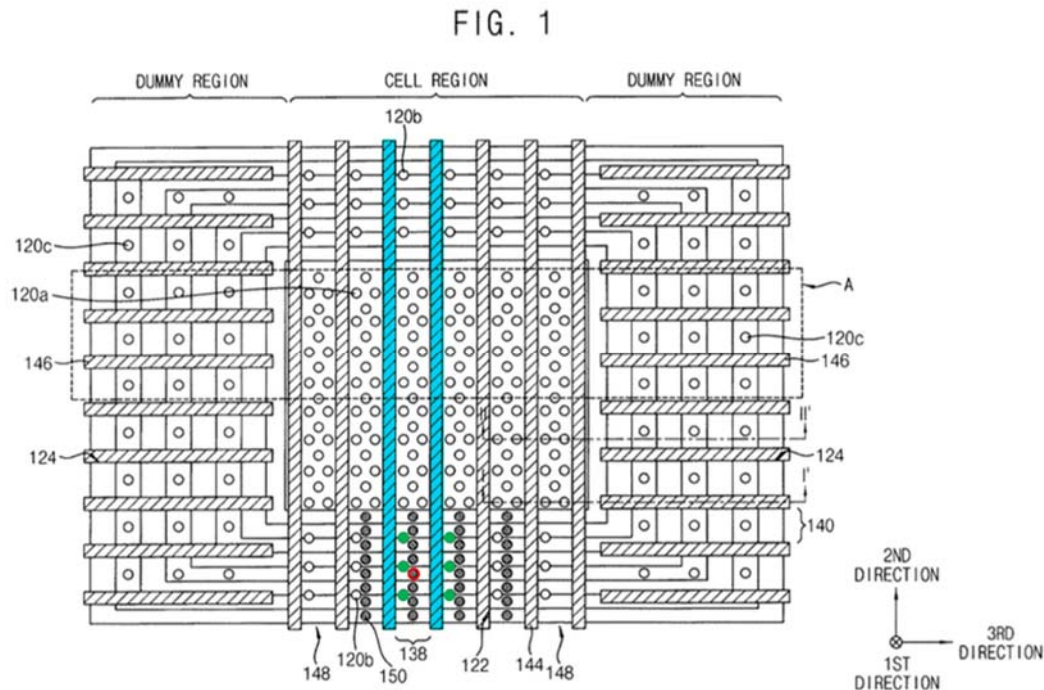
⁴ Challenged Claim 7 recites that the claimed memory device further comprises “a plurality of dummy channel surrounding the staircase contact,” and Challenged Claims 8-10 depend from claim 7.



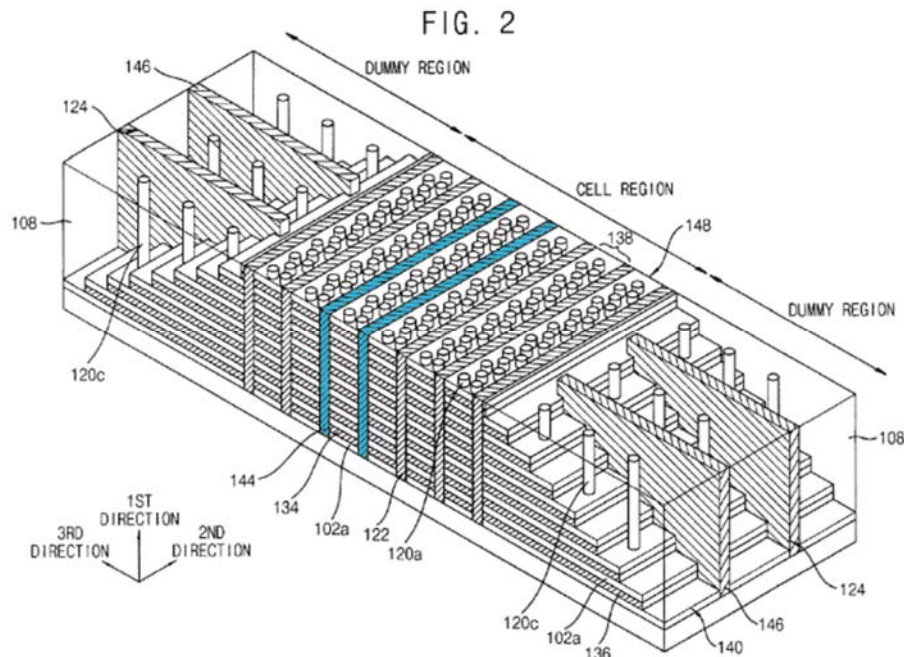
Ex. 1005, Fig. 1 (annotated). Although there are other **second channel structures 120b** and **third channel structures 120c** in Figure 1 that are not highlighted, they do not add to the analysis and Petitioner's mapping therefore focuses only on those that are highlighted. Specifically, Petitioner asserts that Park's **second channel structures 120b** surround one of the **contact plugs 150** (Pet., 73), and as another example asserts that Park's **second channel structures 120b** together with **third channel structures 120c** surround one of the **contact plugs 150** (Pet., 73-74).

Park's alleged channel structures do not "surround" the **contact plugs 150**. As discussed in §IV.B, the plain meaning of the term "surrounding" is not satisfied by structures that are merely on two sides of an object. Figure 1 of Park, however, does not even have dummy source structures on two sides, let alone "surrounding,"

the staircase contact. Instead, directly adjacent to each **contact plug** on the left or right is an intervening barrier: Park's **common source line 144**.



Ex. 1005, Fig. 1 (annotated); *see also* Pet., 75. Park's **common source lines** extend fully from the top to bottom of the cell region in what Park refers to as the “2ND DIRECTION” and are positioned directly adjacent to **contact plug**. In addition, Park's **common source lines** extend in the “1ST DIRECTION” throughout the full height of the memory stack, as illustrated in Park's Figure 2.



Ex. 1005, Fig. 2 (annotated). Therefore, the common source line acts as an intervening barrier that completely separates the **structures 120b** from the **contact plug** on one side, thereby preventing the **structures 120b** from surrounding the **contact plug**. For the same reason, the collective group of **structures 120b** and **structures 120c** also do not surround a **contact plug**, due to the common source lines that act as intervening barriers.

Petitioner's argument that the plain and ordinary meaning of "surrounding" is satisfied even if there are intervening structures (Pet., 75) is misplaced. When an intervening structure completely separates an object and the elements that purportedly surround it, there is no surrounding. Petitioner identifies no intrinsic support for its interpretation of "surrounding," and its arguments appears

to be based entirely on a misrepresentation of infringement contentions from the parallel district court litigation. Pet., 75 (citing Ex. 1026, 23), 77 (citing Ex. 1026, 19, 21, 23). The contentions do not address any situation that is comparable to Park, where there is an intervening barrier extending the length of the memory cell region, thereby completely separating the alleged summary channel structure from the staircase contact. Thus, Petitioner’s reliance on the contentions is misplaced, and it has no support for its proposed mapping.

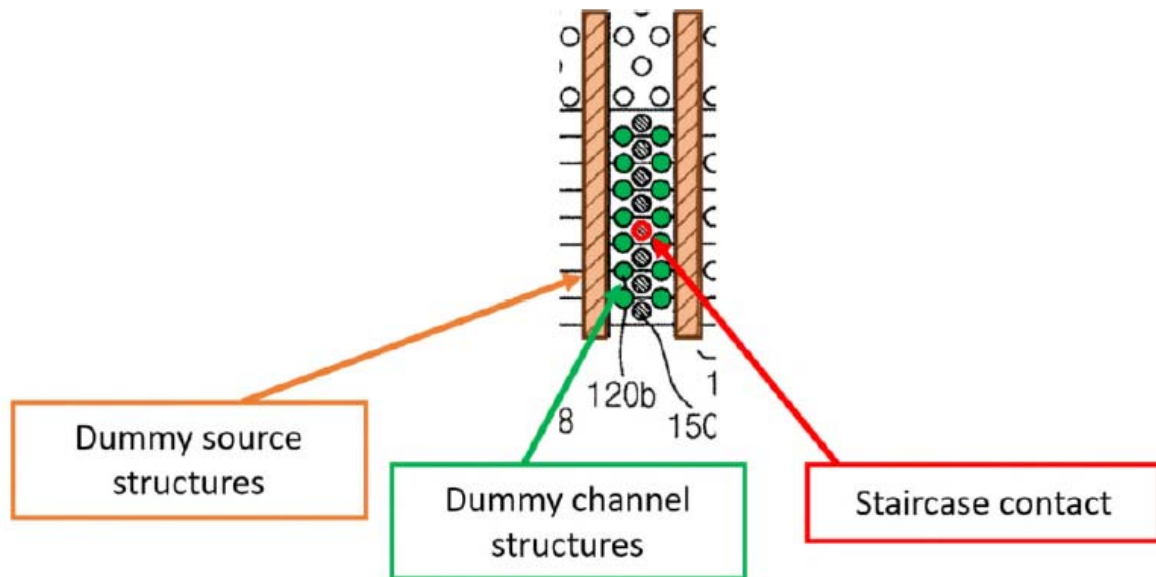
Under the plain and ordinary meaning of “surrounding,” Park fails to disclose “dummy channel structures” that are “surrounding the staircase contact.”

2. Petitioner Fails to Show That a POSITA Would Have Been Motivated to Modify Park to Include Channel Structures “Surrounding” a Contact Plug

Realizing that Park does not disclose “dummy channel structures” “surrounding the staircase contact,” Petitioner alleges that adding additional dummy channel structures would have been obvious in view of the knowledge of a POSITA (Pet., 77-84), but Petitioner’s alleged motivations do not actually motivate the specific modification of Park proposed by Petitioner, and instead the proposed modification is based on nothing more than impermissible hindsight.

Petitioner argues that a POSITA would have found it obvious to make at least two modifications to Park: (1) “lining each side of the [purported] staircase contacts with dummy support pillars, and more specifically, dummy channel

structures (just like structures 120b of Park),” and (2) incorporating multiple additional dummy channel structures for increased density, even on the side that already had such structures, as shown in the Petition’s revised diagram below.



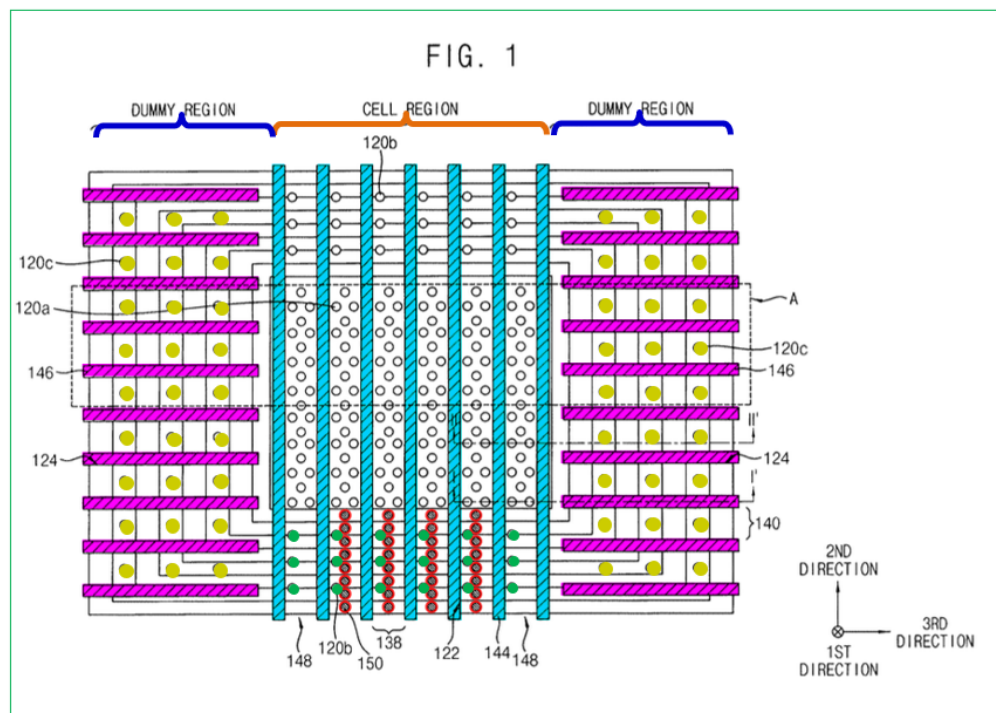
Pet., 82 (Petitioner’s demonstrative). In addition, as shown, Petitioner proposes adding such structures only in the bottom of the wiring region, rather than in other regions of the memory device. In proposing these modifications, Petitioner relies on two background references, Ogawa (Ex. 1024) and Kai (Ex. 1025), arguing that each discloses dummy channels surrounding staircase contacts. Pet., 18-19, 78-82.

Petitioner’s three-pronged obviousness analysis does not support the actual modifications proposed, and instead relies on impermissible hindsight.

First, Petitioner’s argues that “additional dummy structures would have been understood to provide additional support” (Pet. 83 (citing Ex. 1027, 30:14-27,

15:3-22)), but the cited exhibit merely teaches that “support structures” can enhance the structural integrity of a semiconductor device during fabrication, specifically when etching sacrificial layers—a point that Park already recognizes and addresses. In fact, Park explicitly states that its second channel structures 120b function as “supporting pillars” to “support[] portions of the mold structure” during the etching process that removes sacrificial layers. *See, e.g.*, ’872, 9:61-10:5 (“[T]he sacrificial layers 104 may be etched using the photoresist pattern as an etching mask. ... Next, the insulating interlayers 102 and the sacrificial layers 104 may be etched using the photoresist pattern as the etching mask again. Etching processes may be repeated in a similar manner as described above to obtain the mold structure 106.”), 11:63-65 (“The second and third channel structures 120b and 120c may serve as pillars supporting both portions of the mold structure 106.”). Petitioner fails to demonstrate any inadequacy in Park’s existing design that would have prompted a POSITA to add additional supporting structures. For example, Petitioner fails to identify anything in Park suggesting that the support provided by these second channel structure is inadequate or requires any further enhancement. Likewise, the cited background references, Ogawa and Kai, do not teach any benefit of the particular arrangement shown in those references relative to the arrangement in Park.

Moreover, even if Park disclosed a need for additional support (it does not), Petitioner offers no rationale for why a POSITA would have been motivated to incorporate additional channel structures to the **wiring region**—a portion of the cell region that already has a high density of channel structures, i.e. **second channel structures 120b**. Indeed, other regions of the device, including the dummy regions, contain more unutilized space (*i.e.*, white space) for adding additional structures. *Compare* the arrangement of structures in the wiring region within the cell region (orange) *to* those in the dummy regions (dark blue):



Ex. 1005, Fig. 1 (annotated). This confirms that Petitioner's proposal to add channel structures in the specific location it proposes, rather than anywhere else in

the device, is based on hindsight reconstruction of the claimed invention, using the patent as a roadmap.

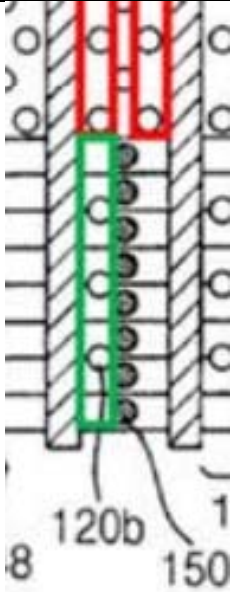
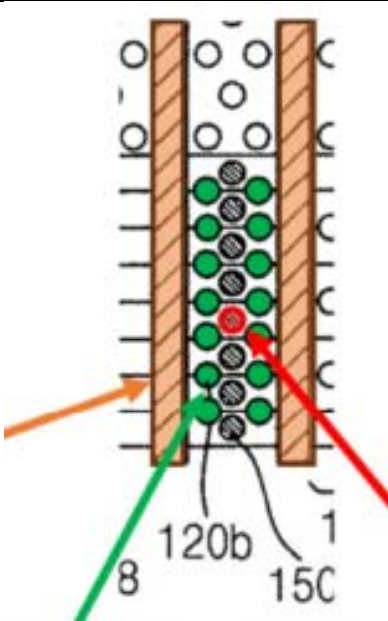
Second, Petitioner contends that “additional dummy structures would result in reducing the likelihood of defective bits on the edge of the memory cell region” by “extend[ing] the memory cell pattern ... into the dummy region” (Pet., 83 (citing Ex. 1028, 8:47-53; Ex. 1029, 2:20-43)), but Petitioner fails to explain how these additional dummy channel structures would actually extend the memory cell pattern into the dummy region. As shown in Figure 1 of Park, the **second channel structures 120b** that Petitioner proposes modifying for increased density are in the cell region of the device, not the dummy region. And by Petitioner’s own admission, the **second channel structures 120b** extend only vertically in Park’s “1ST DIRECTION” (into the page), not horizontally in Park’s “3RD DIRECTION” toward the dummy regions. *See, e.g.*, Pet. 76-77 (and accompanying annotated figure, Figure 7). Petitioner does not propose any modification to **second channel structures 120b** that would result in their addition to the dummy regions of the memory device. Moreover, even if such a modification were proposed or somehow implied, Petitioner has not explained where specifically such structures would be added to the dummy region or why their addition to the **dummy region** would be relevant to a POSITA’s motivation to add such structures to the **cell region** where the alleged contact plugs are located.

Consequently, there is no basis for Petitioner's argument that its modification would be motivated by reducing likelihood of defective bits by extending the memory cell pattern into the dummy region.

Third, Petitioner contends that “adding the additional dummy structures would result in an overall more uniform feature pattern, which reduces processing issues” (Pet., 83 (citing Ex. 1030, 11)), but the reference cited by Petitioner and its expert does not teach or suggest that adding additional structures in the proposed configuration would reduce processing issues. As an initial matter, while the reference states that low- k_1 optical lithography techniques such as “quadrupole illumination” are “more useful in regular patterns,” this is not referring to the periodicity of structures as claimed by Petitioner's expert. Ex. 1030, 11; Ex. 1003 ¶193. Rather, the reference explains that this regularity refers to the feature shape and orientation, with the lithography technique able to enhance “horizontal or vertical lines” while “degrad[ing] 45° orientations.” Ex. 1030, 11. Accordingly, the technique is less useful in designs where features are “completely irregular” and more useful in “regular patterns like memories” that generally have lots of horizontal and vertical lines. *Id.* Thus, there is no teaching or suggestion in the cited art that the usefulness of the described lithography technique is affected by how often a circular feature *repeats*. Likewise, there is no teaching or suggestion

that the technique is improved by adding ***additional structures*** as proposed by Petitioner.

Even if Petitioner were correct that the art teaches or suggests that processing issues are reduced by having a more regular feature pattern, the proposed modification does not actually result in a more regular pattern. Instead, the proposed modification would make the wiring region at the bottom of the cell region ***more dissimilar*** from the top of the cell region, potentially exacerbating the very issues Petitioner seeks to address. *Compare* Petitioner's annotation of the unmodified device (left), which has a uniform spacing between the channel structures, *with* Petitioner's annotation of the modified device (right), which has a change in periodicity between the channel structures in the upper and lower portions of the cell region:

	
Ex. 1003 ¶190 (annotations added by Petitioner).	Pet., 82 (annotations added by Petitioner).

Thus, the reference cited by Petitioner and the arguments presented by its expert do not provide a motivation to modify Park as proposed.

As demonstrated above, none of Petitioner’s proposed rationales would have motivated a POSITA to make the specific modification of Park proposed by Petitioner. Without any valid motivation to modify Park in the manner proposed, Petitioner’s obviousness argument relies solely on impermissible hindsight to attempt a reconstruction of the claimed invention and should be rejected. *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006) (“Rejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some

articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.”).

VII. CONCLUSION

For the foregoing reasons, Patent Owner respectfully requests that the Board deny institution.

Dated: September 13, 2024

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CERTIFICATE OF WORD COUNT

The undersigned certifies that the foregoing PATENT OWNER'S PRELIMINARY RESPONSE UNDER 37 C.F.R. § 42.107 complies with the type-volume limitation in 37 C.F.R. § 42.24(b)(1). According to the word-processing system's word count, the brief contains 11,264 words, excluding the parts of the brief exempted by 37 C.F.R. § 42.24(b).

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CERTIFICATE OF SERVICE

The undersigned certifies that the foregoing PATENT OWNER'S PRELIMINARY RESPONSE UNDER 37 C.F.R. § 42.107 was served in its entirety by filing through the Patent Trial and Appeal Case Tracking System (P-TACTS), as well as providing a courtesy copy via e-mail to the following attorneys of record for Petitioner listed below:

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